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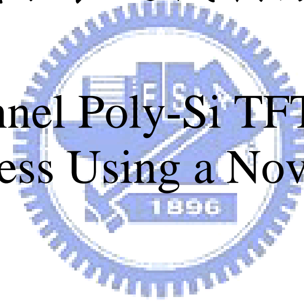
碩 士 論 文

利用新穎結構對Ｐ型複晶矽薄膜電晶體進行之熱載子衰退機制分析



A Study of P-Channel Poly-Si TFT Degradation under Hot-Carrier Stress Using a Novel Test Structure

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摘　要

在本篇論文中，我們利用新穎的測試結構（稱為“熱載子薄膜電晶體”）來對P型複晶矽薄膜電晶體進行熱載子效應的研究。在製程上，它與標準的製程無異，我們不需要增加額外的步驟就能把元件製作出來。此測試結構包含了一組測試電晶體與三組感測電晶體，而此三組感測電晶體分別垂直置放於測試電晶體的通道上。這種設計能有效的偵測出通道在施加偏壓測試後不同區域的受損情況，以及提高區域受損情況之偵測靈敏度。

在研究中，我們分別對P型複晶矽薄膜電晶體進行直流偏壓及交流偏壓的熱載子測試。利用嵌入式的感測電晶體，能夠清楚的觀測出通道中主要的受損區域及陷入閘極氧化層的電子都集中於靠近汲極的位置，而這些結果在傳統的薄膜電晶體中是無法直接感測得出來的。對元件作直流偏壓測試後的結果顯示，當施以閘極直流偏壓大約等於臨界電壓時，元件的受損程度最為嚴重。而在交流偏壓測試中，其頻率、上升時間及下降時間等因素對於元件之影響將進行深入研究與探討。由實驗結果可以證明出，在電壓瞬變的階段會對元件產生額外的損害，而當上升時間或下降時間縮短時，元件會受到更嚴重的額外損害。其可能的受損機制將在本論文中提出。

A Study of P-Channel Poly-Si TFT Degradation under Hot-Carrier Stress Using a Novel Test Structure

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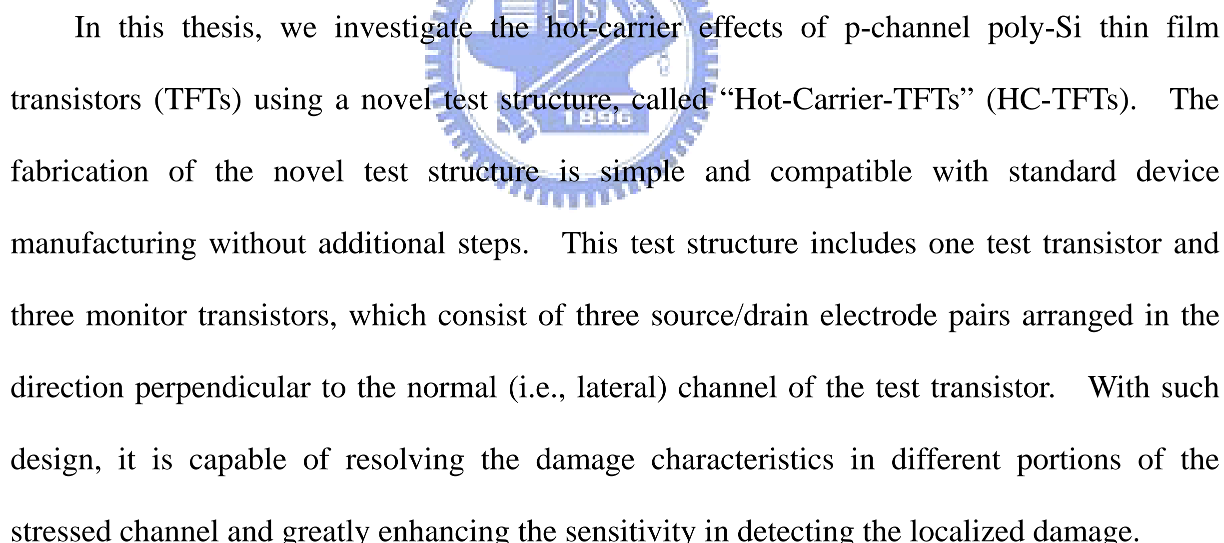
ABSTRACT



In this thesis, we investigate the hot-carrier effects of p-channel poly-Si thin film transistors (TFTs) using a novel test structure, called “Hot-Carrier-TFTs” (HC-TFTs). The fabrication of the novel test structure is simple and compatible with standard device manufacturing without additional steps. This test structure includes one test transistor and three monitor transistors, which consist of three source/drain electrode pairs arranged in the direction perpendicular to the normal (i.e., lateral) channel of the test transistor. With such design, it is capable of resolving the damage characteristics in different portions of the stressed channel and greatly enhancing the sensitivity in detecting the localized damage.

In this study, both static and dynamic hot-carrier stress tests were applied to the p-channel poly-Si TFTs. Using the embedded monitor transistors, in these tests we can clearly observe major damages, including the trapping of electrons in the gate oxide and defect generation in the poly-Si channel near the drain of the test transistor which is the conventional test structure can not directly sense. For an applied specific drain bias applied during the stress period, the most serious degradation of the test devices occurs under the

static stress condition when the gate voltage is close to the threshold voltage. In the dynamic stress test, the effects of input signal factor including frequency, rising time and falling time, were investigated and discussed. The experimental results provide unambiguous evidence that the additional damage occurs during the transient stages, and the device degradation becomes even worse as the rising / falling time is shortened. Possible damage scenarios are proposed to explain the experimental findings.

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Chapter 1
Introduction

1.1 An Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In past years, the hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) are commonly used in active matrix liquid crystal displays (AMLCDs) as the pixel switching transistors [1]. a-Si:H TFTs have many advantages, such as their low-temperature fabrication process which is compatible with low-cost and large glass substrates, and low leakage current because of high off-state resistivity. However, the current driving capacity of a-Si:H TFTs is not good enough due to the low electron field-effect mobility (<1 cm^2/V-s), limiting further development of this technology for industrial applications. As a concern, in a panel system usually the driver chips are made up together with the other application-specified integrated circuits (ASIC) on printed circuit board (PCB). However, the integration of logic circuitries and other chip components on the same substrate is very desirable in terms of cost reduction and system performance improvement.

For this reason, low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) which provide higher electron field-effect mobility and better reliability [2] have attracted much attention and have been widely investigated in industrial applications nowadays, such as active-matrix liquid-crystal displays (AMLCDs) [3-5], electrically programmable read-only memories (EPROMs) [6] , electrically erasable programmable read-only memories (EEPROMs) [7] [8], high-density static random access memories

(SRAMs) [9], dynamic random access memories (DRAMs) [10] as well as candidates for 3-D ICs' applications [11], etc. Among the above-mentioned applications, active-matrix liquid-crystal displays (AMLCDs) are the major driving force to advance the developments of poly-Si TFT technologies.

However, some problems still exist in applications involving poly-Si TFTs. In comparison with single-crystalline silicon, poly-Si films are abundant in grain-boundary defects and intra-grain defects distributing in the channel region. During device operation, actions of these charge-trapping centers significantly affect the electrical characteristics of poly-Si TFTs. The higher amount of defects contained in the channel region requires a larger gate voltage to turn on the device. In other words, additional charges induced by excessive gate voltage are required to fill the larger number of traps before the TFTs are turned on. The defects may also severely degrade the ON current. In addition, leakage current increases with increasing voltage difference between gate and drain due to the prevalence of trap-assisted field emission or trap-assisted thermionic field emission via trap states (defects) in the depletion region near the drain. The relatively large leakage current represents one of the most severe issues of conventional poly-Si TFTs under OFF-state operation. As mentioned above, the location and amount of defect traps have a significant impact on the electrical characteristics of poly-Si TFTs in terms of poorer ON/OFF current ratio and higher power consumption.

From the above discussion it is reasonable to conclude that the most effective approach to improve the electrical characteristics of poly-Si TFTs is to reduce the content of defects by improving the crystalline quality of poly-Si thin films. For this purpose, to enlarge the grain size of the film is an effective method. Hence, a number of crystallization techniques have been developed, such as solid-phase crystallization (SPC) [12], laser crystallization [13] and metal-induced-lateral crystallization (MILC) [14].

Nowadays poly-Si TFTs with carrier mobility larger than 100 $cm^2/V\text{-}s$, a value sufficiently high to meet the requirement of peripheral driving circuits, is easily achievable with modern technology [15]. This enables the integration of drivers on the same panel to reduce the size and manufacture cost of the whole system. Higher drive current can also reduce the surface area of poly-Si TFT to yield a larger aperture ratio in each pixel over the a-Si:H TFT case. This feature allows a higher panel resolution for LTPS products. With these advantages, LTPS is expected to become more and more important in the future.

1.2 Reliability Issues in LTPS TFTs

The stability of device characteristics under long-term operation is important for circuit applications. Consequently, reliability characteristics of LTPS TFTs must be carefully addressed before they can be applied to driving elements in AMOLEDs or advanced circuitry such as data-driver in AMLCDs. In this regard, it should be noted that the unique fabrication processes of LTPS TFTs and the intrinsic material properties of crystallized poly-Si bring about the reliability issues in LTPS TFTs which are different from those in the conventional MOSFETs.

1.2.1 Process-related Issues

Generally the gate oxide used in LTPS TFTs is deposited at low temperature by CVD methods. As a result, it always show poorer physical and electrical quality, such as lower oxide density, higher gate leakage current, and lower breakdown field than that of thermal gate oxide in single-crystal Si MOSFETs which is grown by a high-temperature method. Besides, the mobile ions, Si-OH and/or Si-H bonds, as well as fixed charges are more likely to exist in low-temperature deposited gate oxide which may cause stability issues of LTPS TFTs [16]-[20].

In general, crystallized poly-Si contains many weak strained Si-Si bonds and dangling bonds. In addition, although the hydrogenation process tends to passivate parts of the defects, it may also create a large amount of weak Si-H bonds in poly-Si. These weak bonds can be easily broken during device operation, and result in the change in device characteristics [21] [22].

The laser crystallization process has been widely applied to enlarge the grain size of poly-Si films, but the treatment itself may induce surface protrusion of poly-Si and enhance the local electric field near the interface between the gate oxide and the poly-Si channel [23]. This would also degrade the reliability of TFTs under high gate bias operation.

1.2.2 Results from Degradation under Operation

Degradation in characteristics of solid-state devices under stress tests was well-known and widely reported. Poly-Si TFTs suffer from several degradation mechanisms, such as hot carrier effect [24] and self-heating effect [25], etc. The degradation caused by hot carriers generated by the high electric field near the drain junction has been widely investigated in MOSFETs, and it also represents an important reliability issue for LTPS TFTs. In the event the conduction carriers are heated up efficiently by the high electric field and become "hot carriers" (high-energy carriers) to cause the damage located at the interface between the channel and the gate oxide and inside the active channel region of poly-Si TFTs. Thus, the weak bonds existing in poly-Si would be broken easily by these high-energy carriers, and creating many new defect states and oxide charges. The degree of degradation depends on the strength of drain electric field, and serious degradation can be resulted in the hot-carrier operation mode. Generally, introducing electric-field-relief TFT structures, such as lightly-doped drain (LDD), offset drain, and gate-overlapped LDD, can reduce the degree of hot carrier degradation.

As the devices are operated under ON-state with high bias conditions, the power dissipation in the device is high and may cause an increase in device temperature due to Joule heating, which is known as self-heating or thermal effects [26]. Since the glass substrate is a poor thermal-conducting media, heat generated during device operation is difficult to dissipate. Consequently, the device temperature can rise to a degree which causes bonds breaking, or even burns out the device. The degradation rate caused by self-heating depends on the operation power and the capability of heat dissipation of the device. In general, wide-channel TFTs and/or small-size TFTs suffer more seriously from self-heating [27] [28].

1.3 Motivation of this Study

LTPS TFTs are an important technology in industrial applications. In order to further advance the technology and extend its application scope, significant improvement in reliability of LTPS TFTs is essential. Therefore, the understanding of reliability mechanisms becomes more and more important. Moreover, CMOS technology is necessary for driving circuits, which means that the task of reliability investigation is not only restricted to n-channel LTPS TFTs but also apply to p-channel ones. In this regard, the hot-carrier effects and associated mechanisms of n-channel LTPS TFTs under either DC (static) or AC (dynamic) stress have been widely explored and discussed [24] [27]-[33]. However, few efforts are done to p-channel LTPS TFTs to this date.

As mentioned above, hot carriers are generated during normal device operation by the high-electric field presenting near the drain side. Charges trapped into the gate oxide and interface trap generation may occur and lead to device degradation. In contrast to the MOSFETs, the situation becomes even more complicated for poly-Si TFTs due to the lack of substrate contact in typical device configuration, as well as the large amount of potential defect sites existing at the grain boundaries in the channel. In the past, a lot of research

efforts have been made to study the degradation mechanism of static hot-carrier operation [34]-[38]. The results indicated that the damage regions could be situated in local regions of the channel which can be predicted using simulation and probed using measurement techniques [39] [40]. However, all of these existing techniques cannot directly resolve the location-dependent damage characteristics. Concurrently, in recent years, many works have investigated the degradation mechanisms of dynamic hot-carrier operation [29]-[33]. The situation becomes more complicated than that during static operation since the degradation is related to the different stages of the AC stress signal. It is still difficult to resolve and understand the detailed mechanisms responsible for the damage induced in different parts of the channel of the stressed device.

In this study, we use a novel test structure which was proposed by our group previously [41] [42] to study the hot-carrier effects of p-channel LTPS TFTs. The unique tester, which is introduced in Chapter 2, is designed for spatially resolving the non-uniform damage induced by hot-carriers. With such capability, it was employed in this thesis to investigate the hot-carrier degradation caused by either DC (static) or AC (dynamic) stress tests for p-channel LTPS TFTs. The characteristics of such structure under various stress conditions including the gate and drain voltages, stressing time, frequency and falling/rising time, were characterized and discussed to verify the degradation mechanisms under DC/AC stress.

1.4 Thesis Organization

The thesis is split into five chapters. After a brief introduction of LTPS TFTs, the reliability issues, and the motivation of this study given in this chapter, we describe the device structure of the novel tester, dubbed as HC-TFTs, and the fabrication process in Chapter 2. This chapter also contains the description of the DC/AC stress measurement system setup and measurement scheme.

In Chapter 3, the novel HC-TFT devices are used to analyze related reliability issues. We observe the influence of several DC (static) stress conditions on the test structure and discuss the results and explain the degradation mechanisms.

In Chapter 4, we present the results of the AC stress measurements. Analysis of the electrical characteristics of the test structure under different AC stress conditions is given. Effects of stress configurations and the AC stress conditions, including frequency and transient stages are also explored and addressed.

Finally, we summarize the conclusion and suggest future work in Chapter 5.

Chapter 2
Device Fabrication and Measurement Schemes

2.1 Device Fabrication and Operating Principles of HC-TFTs

Figure 2-1 shows a cross-section of the test structure. First, a 100nm-thick thermal oxide was grown in a furnace on 6-inch silicon wafers to simulate the glass substrate. Then, a 100nm thick a-Si layer was deposited as active layer by a low pressure chemical vapor deposition (LPCVD) system at 550 ℃. Next, the a-Si was crystallized into poly-Si by solid phase crystallization (SPC) annealing step performed at 600 ℃ for 24hr in N_2 ambient. Afterwards, the wafers were subjected to photolithography and etching steps for the definition of active region. A 30nm-thick TEOS-oxide layer and a 150nm-thick poly-Si layer were then subsequently deposited by LPCVD system, followed by the patterning of the poly-Si layer to serve as the gate electrode. Subsequently, a self-aligned ion implantation was used to form p^+ gate and p^+ source/drain simultaneously with BF_2^+ ions for p-channel TFTs. The implant energy was 50 keV with a dose of 5×10^{15} cm^{-2}. A LPCVD oxide layer of 200 nm was used as the passivation layer to prevent the penetration of humidity and impurity, followed by contact-hole formation. After the metallization step, the test structure further received a plasma treatment in NH_3 ambient at 300 ℃ in order to reduce the structural defects and improve devices performance.

The top view of the HC-TFTs test structure is shown in Fig. 2-2. It can be seen that the

test structure is configured with four pairs of p^+ electrodes at the edges of the channel. In the x- (i.e., horizontal)-direction as shown in Fig. 2-3a, the device consisting of one pair of p^+ regions alongside the lateral channel is called the "test transistor (TT)", which will be subjected to the hot-carrier stress by applying a high voltage to its drain for inducing the HC degradations. In the y-(i.e., vertical)-direction as shown in Fig. 2-3b, the other three pairs of p^+ regions and the channel regions form the three transistors called "monitor transistor (MTs)", which are used to observe the degradation incurred at different regions of the test transistor channel after hot-carrier stress. In other words, the current–voltage (I–V) characteristics of the MTs could be characterized before and after the HC test to study the extent and evolution of degradation. The p^+ poly-gate covering the whole channel region serves as the common gate for TT and all three MTs. In Fig.2-3b, according to their relative position in the channel of the test structure, the three MTs are denoted as SMT (i.e., source-side MT), CMT (i.e., central MT), and DMT (i.e., drain-side MT). This unique configuration allows us to investigate the damage locations, and identify the associated mechanisms at different locations along the channel of the test transistor after stressing.

Furthermore, in order to prevent dopant diffusion from the drain (source) of the TT to the channel region of DMT (SMT) which may lead to failure of the MT, the mask has been designed with an offset region which is located between the DMT (SMT) and the drain (source) of the TT. However, this design raises an issue that the MTs would be blind to detect the degradation induced in the offset region (see Fig. 2-4). The offset region near drain of the TT is expected to be the main damage region, because it is supposed to receive the highest electrical field during hot-carrier stress. To address this issue, one method was proposed [43]. The method is to change the current path of measurement, as shown in Fig. 2-5 (a), in which one p^+ region of the DMT and the drain of the TT are treated as the "source" and "drain" terminals in the measurements. Such characterization scheme is dubbed as

"short-DMT" measurements in this work. Executing this method can help sense the damage characteristics in the offset region clearly.

Figures 2-5 (a) and (b) specify the "normal' and "reverse" modes of TT and short-DMT measurements. In normal measurements, the nominal gate and drain are negatively biased with respect to the nominal source (which is set to ground). In order to analyze devices in details, reverse measurements that have the nominal gate and source negatively biased with respect to drain (which is set at ground) are also executed and are denoted as "Reverse short-DMT" and "Reverse TT", as shown in Fig. 2-5.

2.2 Measurement Schemes

Normal experimental procedure carried out in this work is to perform various DC/AC hot-carrier stress on the TT first, then the characteristics (e.g., I_{DS} - V_{GS}) of the TT and MTs before and after hot-carrier stress were measured and analyzed.

Execution of DC stress and measurements of the subthreshold and output characteristics of the test devices were done by a Keithley 4200 semiconductor characterization system with Keithley Interactive Test Environment (KITE) software. AC stress and measurements were performed using Keithley pulse generator 4200-PG2 in the same system. Temperature-regulated hot chuck was used to control and fix the temperature of the wafers at 30 ℃ during both DC and AC stress periods.

2.3 Definition and Extraction of Device Parameters

The threshold voltage of MTs is defined as the value of V_{GS} when the drain-current (I_{DS}) equals $10nA \times \frac{W}{L}$ at V_{DS} of -0.1V, where W and L are channel width and channel length, respectively. The extracted value with this method is donated as "V_{th}". Besides, due to the

large number of defects generated in the channel during the stress, the threshold voltage of TT is strongly influenced by the severe degradation of subthreshold swing. In line with this, V_{th} of TT is redefined as V_{GS} when I_{DS} equals $1nA \times \frac{W}{L}$ at V_{DS} of -0.1V. This method is adopted in most studies on the HC reliability of poly-Si TFTs because of its simplicity in measurement. Moreover, the definition of ΔV_{th} is defined in the following equations:

$$\Delta V_{th} = V_{th,stress} - V_{th,fresh} \qquad \text{(Eq. 2-1).}$$

where $V_{th,fresh}$ and $V_{th,stress}$ are the threshold voltage before and after stressing, respectively.

Furthermore, the degradation of on-current is a useful indicator for observing the characteristics of device under hot-carrier stress. In this work, from the measured I_{DS}-V_{GS} curve at V_{DS} = -0.1V, the on-current is extracted at $V_{GS} - \Delta V_{th}$ = -15V. The degradation (%) of the on-current is defined as $(\Delta I_{on} / I_{on,fresh}) \times 100\%$, where $\Delta I_{on} = (I_{on,stress} - I_{on,fresh})$, $I_{on,fresh}$ is the initial on-current (i.e., fresh condition), and $I_{on,stress}$ is the on-current after stressing.

Chapter 3
HC-TFTs under DC stress

3.1 DC Stress Conditions

In this chapter, the static stress is used to degrade the HC-TFTs for the evaluation of the HC effects. In addition to recording the shift of electrical parameters of the test transistor, electrical characteristics of the monitor transistors embedded in the same test structure are also analyzed, which are extremely useful for understanding of the degradation induced in different parts of the channel. The basic parameters of DC signals consist of gate voltage (V_G), drain voltage (V_D), source voltage (V_S), and stress time. Throughout this work the source was fixed at ground the temperature of test environment was kept at 30 ℃. The total stress time is 1000 sec unless it is specified otherwise. Different combinations of V_G and V_D were chosen to investigate the degradation of HC-TFTs under hot-carrier DC stress.

3.2 Degradation Mechanisms of p-channel Poly-Si TFTs under Static Stress

Figure 3-1 depicts the hot-carrier degradation mechanisms of p-channel poly-Si TFTs under DC stress. As the absolute magnitude of the drain bias is high, holes can obtain energy from the high electric field in the drain junction and become "hot carriers", which would cause impact ionization and lead to the generation of electron-hole pairs. The hot carriers may release their energy inside the channel or near channel/oxide interface, thus additional defects and interface states are thus created. These generated defects and

interface states would degrade the subthershold swing and mobility of the device and cause the on-current degradation. Moreover, portions of the hot electrons generated by impact ionization would surmount the barrier height at the oxide interface and inject into the gate oxide. Trapping of the electrons shifts the device's threshold voltage. Injection efficiency depends on the strength of the vertical electric field at the injection spot.

3.3 HC Stress under Mild Stress Bias

Typical subthreshold characteristics of the lateral test transistor before and after DC stress are shown in Fig. 3-2. The test transistor was stressed with V_G = -7.5 V and V_D = -20 V for 1000 sec. The I_D-V_G curve shows only a negligible shift after stressing under the above-specified mild stress condition. In the figures the only noticeable change is the off-state leakage current under normal mode which will be addressed later. Thus the information provided by the conventional test transistor is unclear and insufficient, so we do not know details about the major damage location in the stressed channel [37] [38], nor the degradation mechanisms. Therefore, the subthreshold characteristics of different independent monitor transistors (MTs) in the test structure are also measured to resolve these deficiencies, and the results are shown in Fig. 3-3.

As compared with the characteristics of TT under reverse-mode measurements shown in Fig.3-2 (b), it can be seen that the off-state leakage current of normal mode is reduced and becomes independent of the gate bias after hot-carrier stress, as shown in Fig.3-2 (a). This phenomenon can be explained by the band diagrams illustrated in Fig.3-4. In Fig. 3-4 (a), due to the strong electric field in the drain near the oxide interface, the field emission of conduction holes leaving the electrons to cause the band-to-band tunneling (BTBT) current. When the device was stressed under hot-carrier condition, portions of the electrons generated by impact ionization are trapped in the gate oxide near the drain side as mentioned in last

section, so the electric field is reduced and the BTBT current is suppressed, as shown in Fig. 3-4(b). Note that the reduction of off-state leakage after hot-carrier stress was not observed in n-channel poly-TFTs [41] [42]. This is attributed to the smaller effective mass as well as the smaller energy barrier height at Si/SiO_2 interface for electrons, compared with the holes, so hole trapping is less likely to occur in the case of n-channel devices.

The subthreshold characteristics of different MTs embedded in the same test structure studied in Fig. 3-2 are shown in Fig. 3-3. It can be seen that no visible damage occurs in the SMT and CMT. However, the DMT and short-DMT show significantly degraded on-current and positive shift in threshold voltage. This proves the above statements about the trapping of electrons in the oxide near the drain side of the TT.

Fig. 3-5 shows the degradation of on-current of TT and all MTs as a function of stress V_G with V_D = -20 V for 1000 sec. The results indicate that the degradation trend of TT is followed by that of DMT and short-DMT, pinpointing the location where major damage is induced. Moreover, both DMT and short-DMT exhibit higher degradation than the TT, especially the latter one. This demonstrates the high sensitivity of the test structure in resolving the location–dependent damage characteristics.

3.4 HC Stress under Severe Stress Bias

In Fig. 3-6, the test transistor was stressed under a hot-carrier stress biases of V_G = -7.5 V and V_D = -25 V, much severe than that executed in the previous section, for 1000 sec. As expected, the resultant degradations in the device characteristics in terms of increased subthershold slope and reduced on-current are much bigger than those under mild stress shown in Fig. 3-2. In Figure 3-6(a), relative to the post-stress I_D-V_G curve which was measured at high absolute drain bias of V_D=-3 V, the shift of I_D-V_G curve after hot-carrier DC stress is more significant when the lateral test transistor was measured at low absolute drain

bias of V_D=-0.1 V. This represents an evidence that most of the damage events occur in the channel near the drain side of the test transistor [44]. Hot-carrier stress can generate extra interface states and/or grain-boundary defects, and form a defect-rich and resistive region in the channel near the drain side [45]. As a larger absolute magnitude of drain bias is applied during the measurements of transfer characteristics, the depletion region near the drain side extends more deeply into the channel and effectively screens out the defects induced in the region, thus relieving the post-stress I_D–V_G shift. In contrast, the subthreshold characteristics of TT under reverse-mode shown in Fig. 3-6(b) show clear shift after stress regardless of the drain bias (-0.1 or -3 V). Under such mode of measurements the damaged region which contributes a high resistance is close to the source side and cannot be screened out by the drain bias. The situation can be schematically illustrated in Figure 3-7 [46]. Damage induced by hot carriers can form a potential energy hump near the nominal drain side of the TT, as shown in Fig. 3-7 (a). A high absolute drain bias tends to drop the energy barrier height and thus the degradation of subthreshold characteristics is screened out with the modified band diagram shown in Fig. 3-7 (b). Under reverse-mode of measurements the voltages applied to the nominal drain and source of the TT are switched, the band diagram changes to that shown in Fig. 3-7 (c). Under the situation the carriers are still obstructed by the potential energy hump leading to the degradation in the on-current.

Moreover, the subthreshold characteristics of MTs contained in the same test structure studied in Fig. 3-6 are shown in Fig. 3-8. The on-current degradation of DMT is the most obvious, while both SMT and CMT exhibit negligible shift in I_D-V_G curves. In Figure 3-9, it shows that much severe on-current and subthreshold swing degradation, and threshold voltage shift occur in the short-DMT than the TT and the other MTs do. The reverse-mode measurement of the short-DMT shown in Fig. 3-9 (b) also reveals the effect of potential energy hump property near the drain side. These results unambiguously show that the major

damages are induced in the region of short-DMT and DMT, including the ungated drain region of the TT.

By increasing the absolute magnitude of the drain stress bias, the carriers may obtain more energy to generate more damage near the drain side of the channel due to the increased electric field. Figure 3-10 shows the on-current degradation of TT and different MTs as a function of stress V_D with V_G= -7.5 V for 1000 sec. The on-current degradation of TT and DMT becomes much severe with increasing magnitude of the drain stress bias. Moreover, in Fig. 3-11, because the vertical electric field near the drain is increased with increasing absolute magnitude of the drain bias, more electrons generated by impact ionization are trapped in the gate oxide near the drain side and result in the positive threshold voltage shift of DMT. These results fit in with our experimental observations. Note that the threshold voltage of TT shows negative shift as the absolute drain bias is high. This is attributed to the severe degradation of subthreshold swing due to the large amount of defects generated in the channel during the stress.

Figure 3-12 shows the on-current degradation of TT and different MTs as a function of stress V_G with V_D= -25 V for 1000 sec. It can be seen that the trend of on-current degradation of TT and DMT are similar, indicating that the major damage region of the test transistor is located near the drain side. When the absolute gate voltage is lower than the threshold voltage, not enough carriers are induced in the channel, so the degradation is not serious. When the absolute gate voltage is larger than threshold voltage and a high absolute drain voltage is applied, it can induce a significant amount of hot carriers and the resultant damage. In Fig. 3-12 the degradation peaks at a gate voltage of -7.5 V. As the absolute gate voltage gets larger, the degradation in on current is decreased. This might be due to the reduction of maximum field strength inside the channel.

The threshold voltage of TT and different MTs as a function of stress V_G with V_D= -25 V

for 1000 sec is shown in Fig. 3-13. It can assist us to more clearly understand the results shown in Fig. 3-12. We can see that the effect of gate voltage is most significant for DMT. When the absolute gate voltage is very low and close to V_G=0 V, it will induce a very high vertical electric field across the oxide near the drain side and cause a lot of electrons to be injected into and then trapped in the gate oxide. The situation is illustrated in Fig. 3-14. These results in the positive threshold voltage shift of DMT and generate interface states at channel/oxide interface near drain side, and leads to the on-current degradation of DMT as shown in Fig. 3-12. As the absolute gate voltage is bigger than the threshold voltage and a high vertical electric field is maintained near drain side, the peak of electric field occurs at the space charge region near the drain side which tends to generate hot carriers and resultant damage. When the absolute gate voltage continues to increase, the peak electric field in the space charge region weakens and the high-field region distributes to the region of DMT. This leads to more electrons being trapped in the gate oxide in the channel region of DMT to cause positive threshold voltage shift of DMT, as shown in Fig. 3-15. However, due to the decrease in the peak electric field, the degradation is also reduced at a higher absolute gate voltage.

To summarize, the MTs contained in the HC-TFTs show the capability of resolving the detailed degradation mechanisms occurring at different parts of the conventional channel. Moreover a high sensitivity is also demonstrated. Therefore the special design of the HC-TFTs can be employed to help identify the major damage location.

Chapter 4
HC-TFTs under AC stress

In this chapter, the hot-carrier induced degradation in TFTs under dynamic operations is investigated using the proposed HC-TFTs structure. The test samples were prepared with the same method described in previous chapter and detailed process flow can be found in Chapter 2.

4.1 AC Stress Conditions

Figure 4-1(a) shows the waveform of the AC signal applied during stress. The basic parameters of AC signal include frequency (Freq.), signal high level (V_{G_high}), signal low level (V_{G_low}), low-level time (t_{low}), rising time (tr), falling time (tf), and duty ratio.

Under AC stress, a pulse voltage is applied to the gate by Keithiley 4200-PG2 pulse generator, source is grounded and a high absolute voltage (negative for p-channel devices) is applied to the drain, as shown in Fig. 4-1(b). Falling time (tf) is the time that voltage signal falls from 90% to 10% of the amplitude ($V_{G_high} – V_{G_low}$), while rising time (tr) is defined as the time that the voltage signal rises from 10% to 90% of the amplitude ($V_{G_high} – V_{G_low}$). Duty ratio is defined as the ratio of the time when pulse voltage is V_{G_low} (t_{low} in Fig. 4-1(a)) to the duration of one pulse cycle. The total stress time is the summation of t_{low} under the stress condition. The standard AC stress condition used in the experiment is with gate voltage swing from -10 V (V_{G_low}) to 0 V (V_{G_high}), drain voltage of -25 V, frequency of 500 kHz, both tr and tf of 100 ns, duty ratio of 50%, and the total stressing time (total t_{low}) of 500

sec. Certainly more information could be acquired as the above parameters are varied to study their impact on the device degradation. In this study, the frequency is varied from 100 kHz to 1MHz, and both tr and tf are varied from 100 ns to 10 ns.

4.2 Effects of Frequency

Typical characteristics of the transistors contained in a test sample stressed under the standard AC stress condition with total stress time (total t_{low}) = 500sec are shown in Fig. 4-2 and Fig. 4-3. Fig. 4-2 shows I_D-V_G curves of the TT before and after AC stress under normal- and reverse-mode of measurements, respectively. With such stress condition, hot-carrier induced degradation is so minor and difficult to detect with the TT. This is similar to the situation encountered in previous chapter and again we can employ the MTs also embedded in the same test structure to help address the issue, and the results are shown in Fig. 4-3. In Figs. 4-3 (a) and (b), it can be seen that the SMT and CMT exhibit negligible degradation in the I_D-V_G curves after AC stress. In contrast, Figs. 4-3 (c) and (d) show significant shift in subthreshold characteristics of DMT and short-DMT. Device degradations in terms of on-current degradation and threshold voltage shift are observed obviously after AC stress. This is an indication that defects, like interface states and traps in the grain-boundaries are generated and form a defect-rich region. Moreover, electrons are trapped in the gate oxide near the drain side of TT after the AC stress. Again, these effects can be easily detected by the DMT and short-DMT, demonstrating the greater sensitivity of the proposed structure over the conventional test structure. Basically, the features associated with the AC HC stress are similar to those under static stress presented in last chapter.

To more clearly understand the AC effect on the device degradation, frequency of the AC signal was varied. Figure 4-4 shows the subthreshold characteristics of devices stressed before and after 500 sec AC stress with 100 kHz and 1 MHz. In the figures major

parameters of the AC stress are the same as those in standard condition except the frequency. Fig. 4-5 shows the subthreshold characteristics of the DMT and short-DMT corresponding to the devices studies in Fig. 4-4. In these figures, it can be seen that the degradation of device under high-frequency AC stress is much severe than that under low-frequency AC stress. Figure 4-6 and Fig. 4-7 show the on-current degradation and threshold voltage shift of TT and MTs after 500 sec AC stress as function of frequency, respectively. The results indicate that the damage induced in SMT and CMT is negligible and almost independent of the frequency. The on-current degradation is significant for the TT and DMT and increases with increasing frequency. This indicates that additional damage is generated near the drain side as the frequency increases. Moreover, the DMT always shows higher degree of degradation as compared with the TT. This is especially true in detecting the threshold voltage shift, as shown in Fig. 4-7, in which only the DMT shows significant shift. These results clearly demonstrate that the MTs of test structure can definitely resolve the non-uniform damage location and their excellent sensitivity for detecting the frequency-dependent degradation. Note in the measurements just mentioned, the total time under V_{G_low} is fixed at 500 sec, so the repetitions of the transient stages (tr and tf) are very likely the reason for the additional damage. Therefore, we identify the effect of transient stages under hot-carrier AC stress in the next section.

4.3 Effects of Transient Stages

4.3.1 Rising time

In this section we first investigate the effect of rising time. Parameters of the stress condition are the same as the standard one except the rising time. Fig. 4-8 and Fig. 4-9 show subthreshold characteristics of TT, DMT and short-DMT before and after AC stress with the rising time of 100 ns and 10 ns, respectively. The results show that the device performance

degrades more under a faster rising time of AC stress. Fig. 4-10 and Fig. 4-11 show the on-current degradation and threshold voltage shift, respectively, under AC stress with tf = 100 ns but with varying tr. Still, the DMT exhibits the most serious degradation. Moreover, the damage becomes even more severe as the rising time is shortened.

The degradation mechanism in the transient stage from V_{G_low} to V_{G_high} under AC stress is illustrated in Fig. 4-12 [47]. As shown in the illustration, a high absolute pulse voltage is applied to the gate while the source is grounded and a high absolute bias is applied to the drain. For gate pulse at V_{G_low} of -10V, a sheet of holes is induced in the channel and the damage can be attributed to impact ionization occurring near the drain side, as shown in Fig. 4-12(a), and results in on-current reduction and threshold voltage shift. This is basically the same situation encountered in static HC stress. During the transient period (V_{G_low} rise to V_{G_high}), the inversion holes remained in the channel are mainly attracted by the negative drain bias and accelerated toward the drain, resulting in additional damages and more electrons trapped in the gate oxide, as shown in Fig. 4-12(b). In the case of a slow rising time, most of the holes have enough time to relax through collisions. Thus, the hot-carrier issue is also relaxed. On the other hand, in the case of a fast rising time, the voltage drop across the drain junction is increased by ΔE (Fig. 4-12) in a short time, and more hot holes are expected to be generated, causing more damage in the regions of channel near the drain of the TT. For this reason, the on-current degradation of TT and DMT, and the threshold voltage shift of DMT are relating to rising time during AC stress.

4.3.2 Falling time

Parameters of the AC stress condition are the same as the standard one except the falling time. Figure 4-13 and Fig. 4-14 show I_D-V_G curves of TT, DMT and short-DMT before and after AC stress with falling time of 100 ns and 10 ns, respectively. The results indicate that

the degradation of device under the AC stress is higher as the falling time becomes shorter. Figure 4-15 and Fig. 4-16 show the on-current degradation and threshold voltage shift, respectively, under AC stress with fixed tr = 100 ns as function of tf. Comparing the on-current degradation and threshold voltage shift of the three MTs under AC stress, only those of the DMT increase dramatically with decreasing falling time, indicating that additional defect generation and electron trapping in gate oxide occur as the falling time is shortened.

Fig. 4-17 shows a scenario proposed for explaining the effect of falling time under AC stress. When a V_{G_high} = 0 V is applied to the gate, high gate-induced drain leakage by BTBT (Fig. 4-18)dominates the conduction due to the high voltage difference between the gate and the drain, as shown in Fig. 4-17(a). Under the situation, the channel field is more or less uniform, and the electrons appear at the tunneling junction (i.e., drain junction of the TT) would drift toward the source by the field. When the gate voltage is switched from V_{G_high} to V_{G_low}, a high voltage drop is developed at the channel/drain junction in a short time due to the formation of the inversion hole layer, as shown in Fig. 4-17(b). Portions of the electrons remained at the original tunneling junction would be accelerated by the suddenly presenting field. This leads to the generation of hot electrons and the following additional damage, including defect creation in the channel and electron trapping into the oxide (near the drain of the TT). Such phenomenon becomes more significant as the falling time is reduced. This explains why the on-current degradation of TT and DMT shown in Fig. 4-15, and threshold voltage shift of DMT shown in Fig. 4-16.

Chapter 5
Conclusions & Future Work

5.1 Conclusions

In this study, we have employed a novel test structure, the HC-TFT, to investigate the reliability issues of p-channel poly-Si TFTs. This unique test structure is designed for spatially resolving the location-dependent damage induced by hot carriers in either DC (static) or AC (dynamic) stress tests for p-channel poly-Si TFTs.

Whether static or dynamic stress, we can clearly identify that major damage is induced near the drain side of the TT in the test structure by means of the DMT and short-DMT. Moreover, electron trapping in the gate oxide near the drain side of the TT is also detected by DMT and short-DMT. In addition to the capability of spatially resolving the damage location, the proposed structure also exhibits higher sensitivity.

The HC-TFT was also employed to analyze the effects of several factors including frequency, rising time and falling time, on the damage under AC stress. Our data indicate that the device degradation under high-frequency AC stress is much worse than that under low-frequency. Moreover, the results provide unambiguous evidence that the additional damage occurs during both the voltage falling stage and rising stage. In this thesis physical degradation models have been proposed to explain those findings.

5.2 Future Work

In addition to the hot-carrier degradations in p-channel poly-Si TFTs, negative bias

temperature instability (NBTI) is another key reliability issue that is of immediate concern for practical applications of p-channel poly-Si TFTs. Unfortunately, few efforts are done for investigating the mixed effects of hot-carrier effect and NBTI. This topic is thus important and in the future, and the HC-TFT should be a useful test vehicle for this purpose. It should be also capable of identifying the degradation mechanism in different parts of the channel under various HC/NBTI stress conditions.

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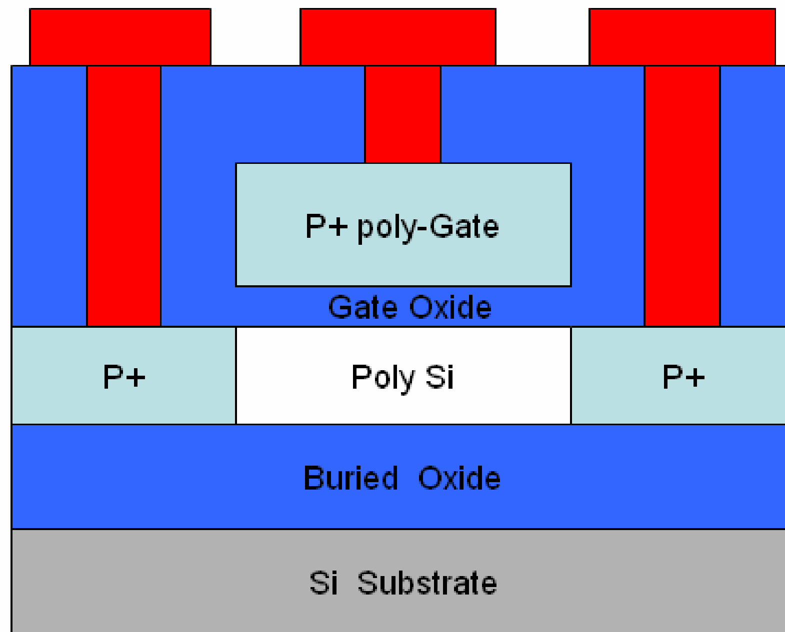


Fig. 2-1 Cross-sectional view of the test device.

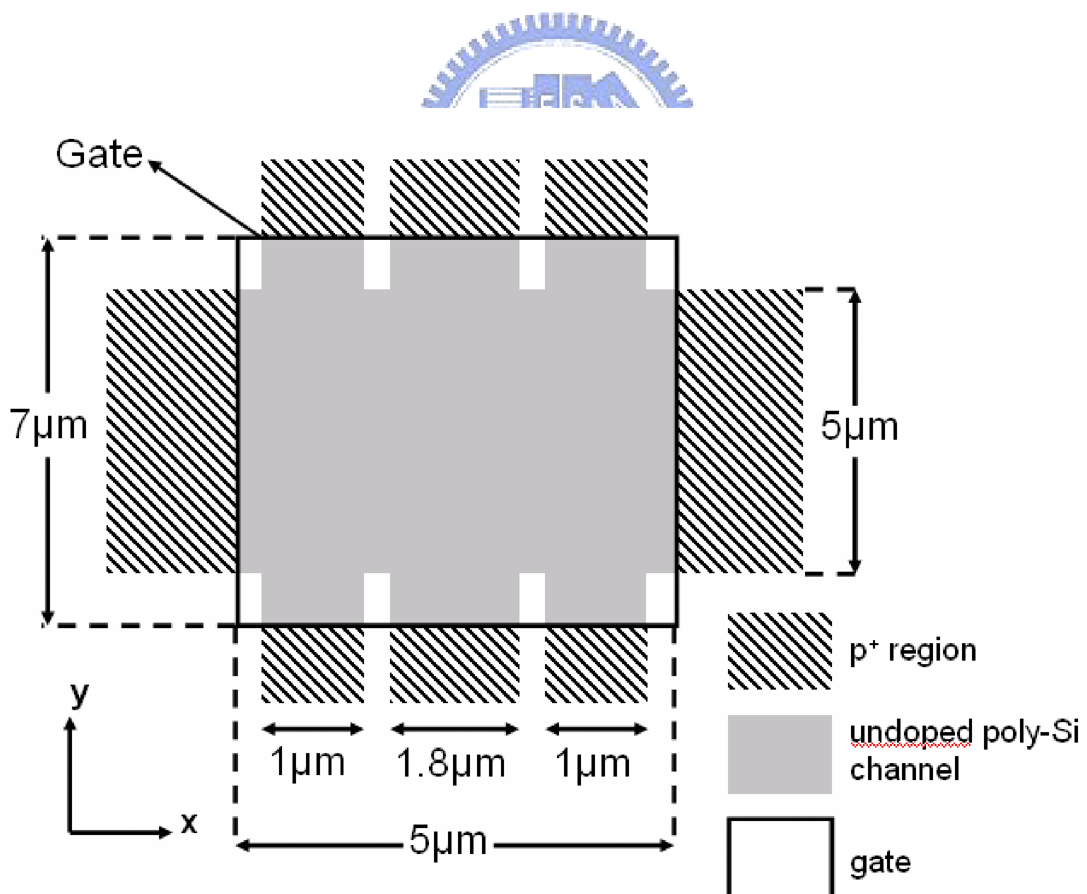
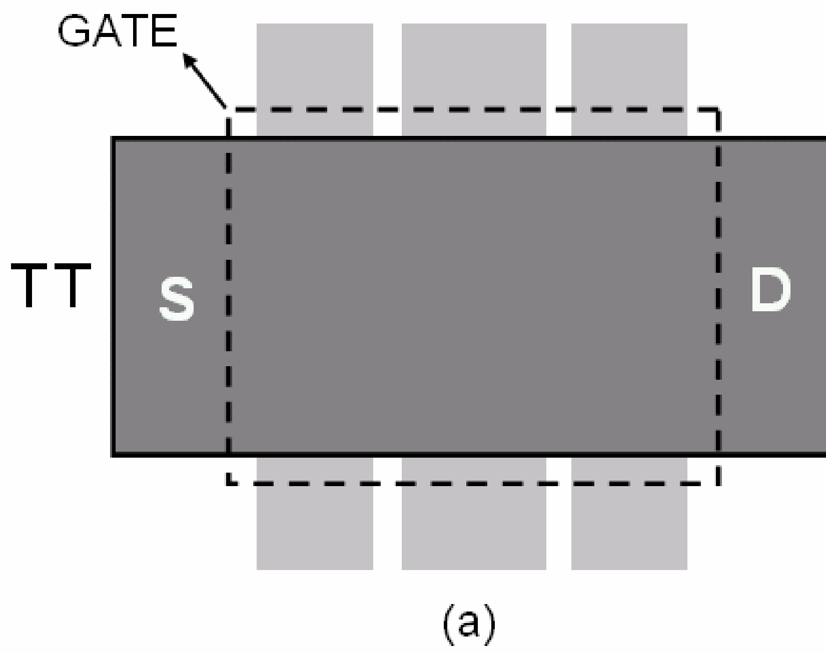


Fig. 2-2

Top view of HC-TFTs device.



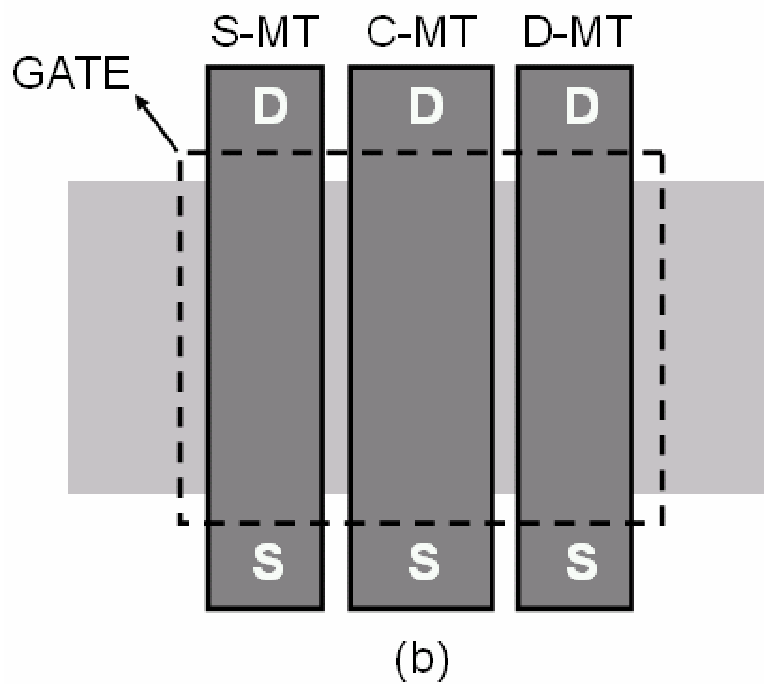


Fig. 2-3 Definition of (a) test transistor (TT) and (b) monitor transistors (MTs).

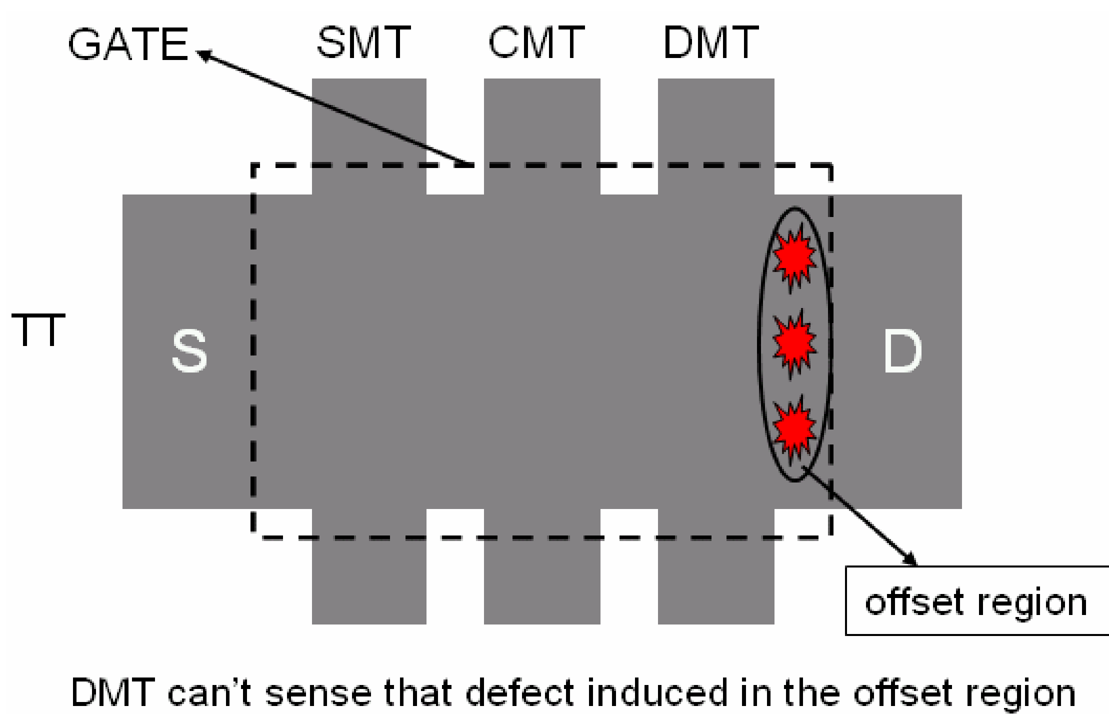


Fig. 2-4 Illustration of the major damage region in the HC-TFTs under severe HC stress condition.

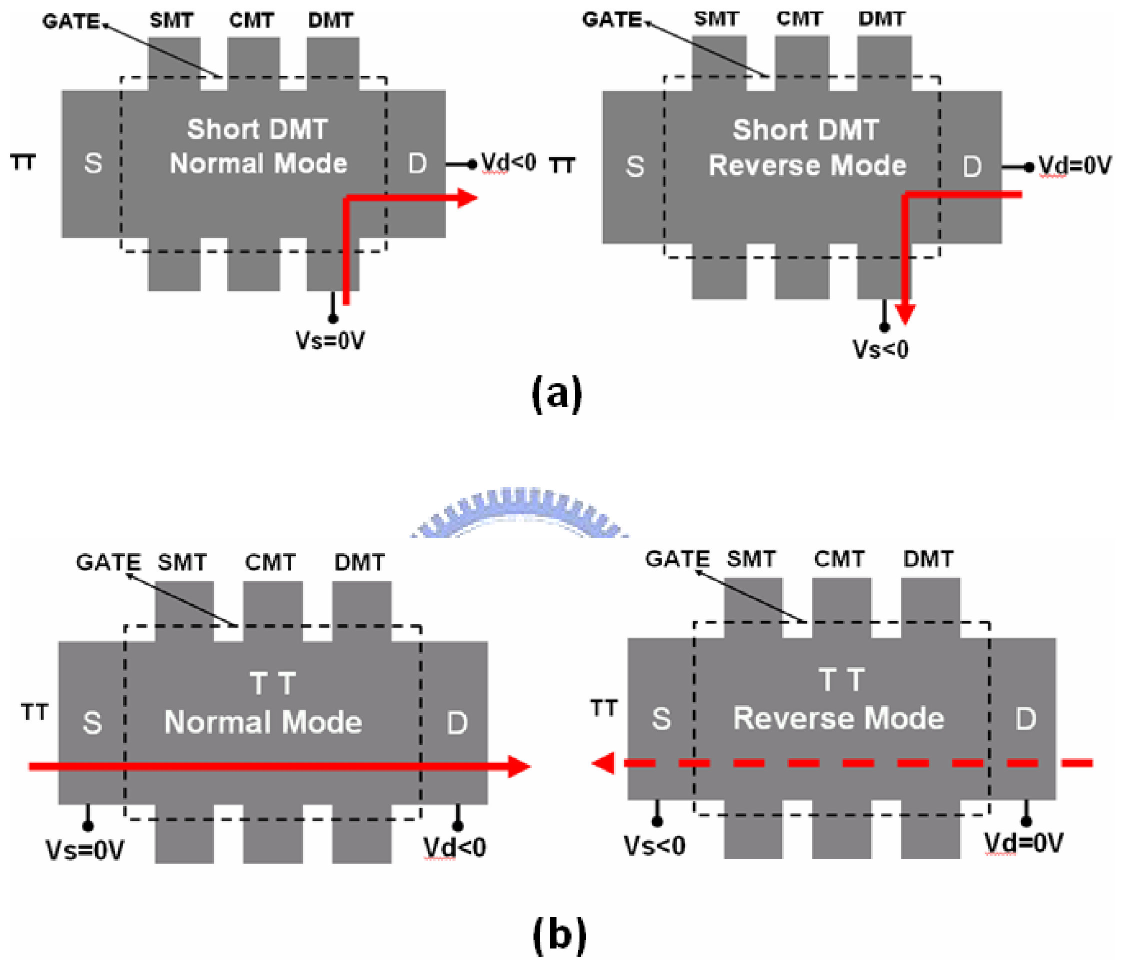


Fig. 2-5 Definition of "Normal mode" and "Reverse mode" of (a) Short-DMT and (b) test transistor.

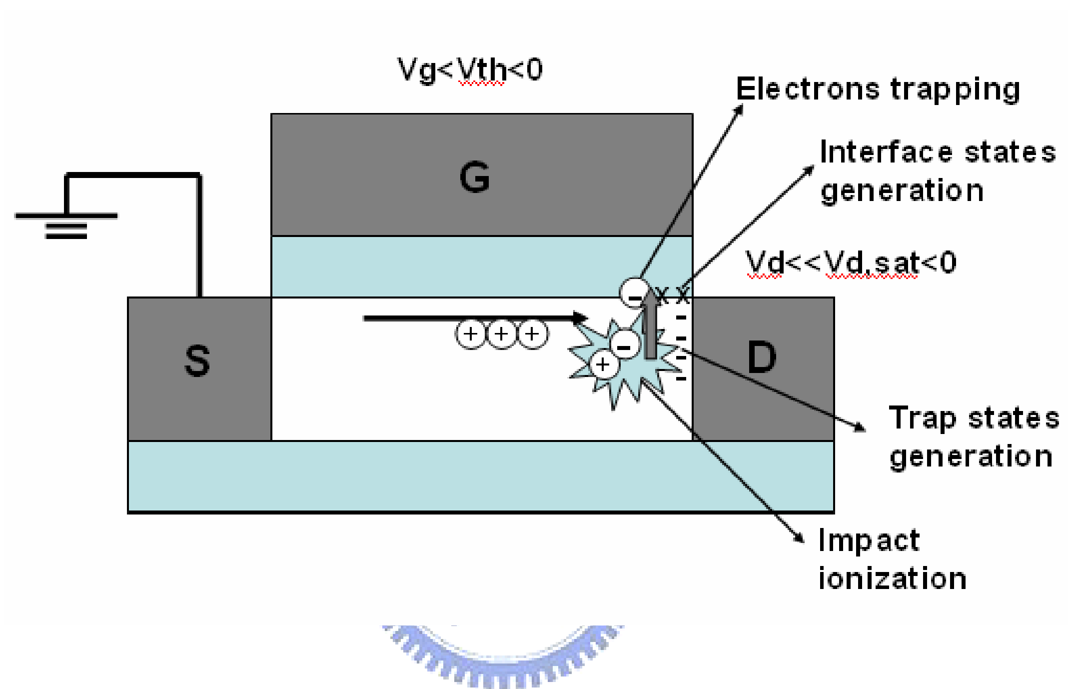


Fig. 3-1 Schematic illustration of defect types and their creation in the p-channel device caused by hot carriers.

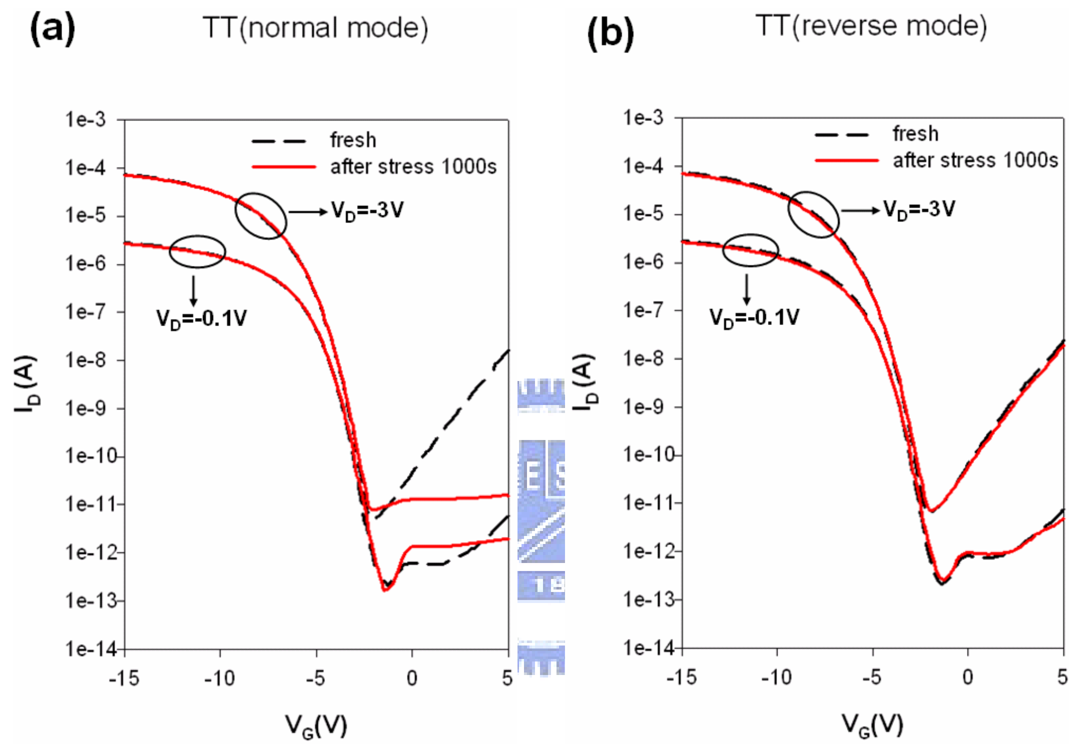


Fig. 3-2 Subthreshold characteristics of (a) normal mode and (b) reverse mode of the test transistor before and after lower DC stress at V_G/V_D of -7.5 V/-20 V for 1000 sec

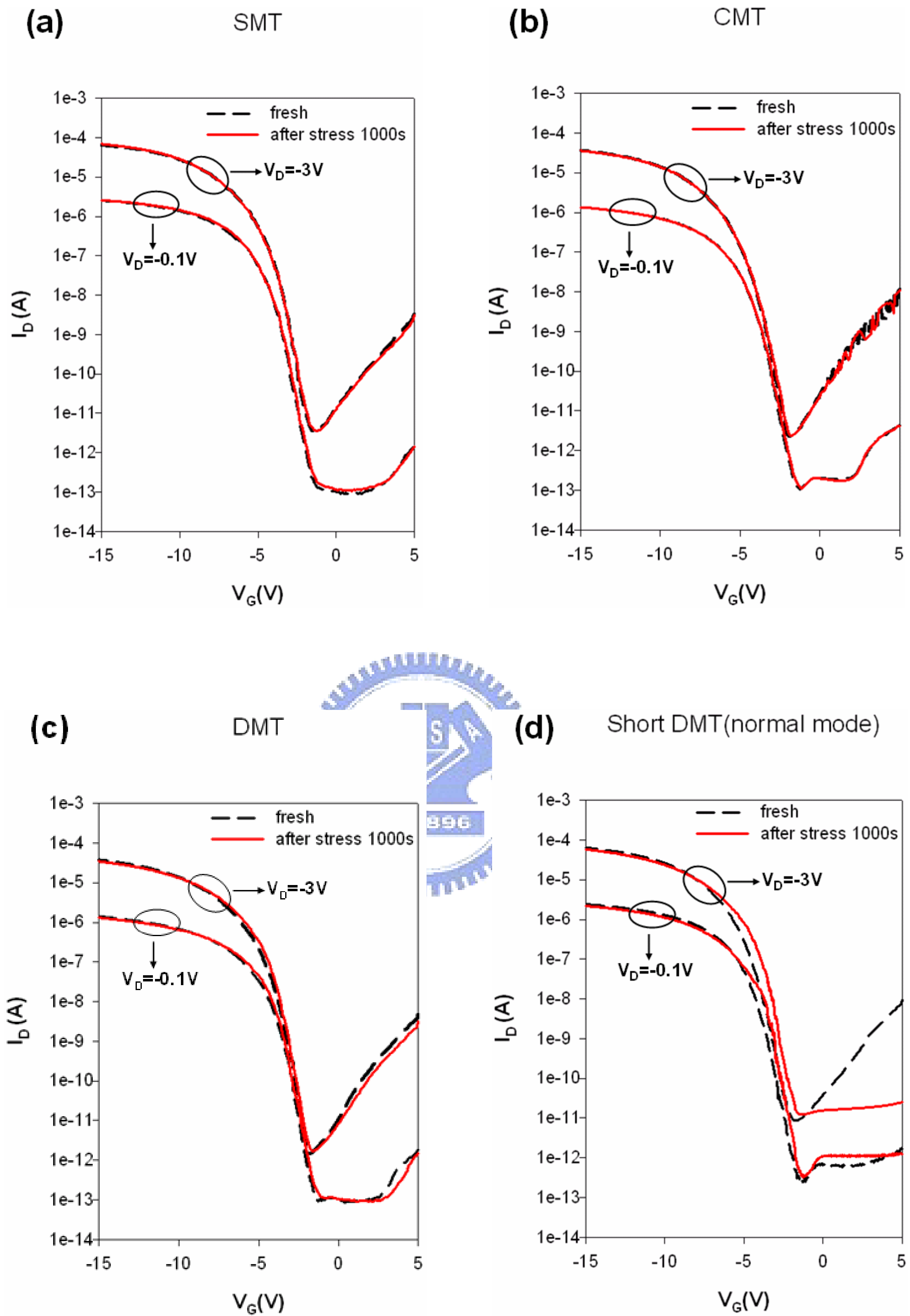


Fig. 3-3 Subthreshold characteristics of (a)SMT, (b)CMT, (c)DMT and (d)Short DMT transistors contained in the same test structure characterized in Fig. 3-2 before and after mild DC stress at V_G/V_D of -7.5 V/-20 V for 1000 sec.

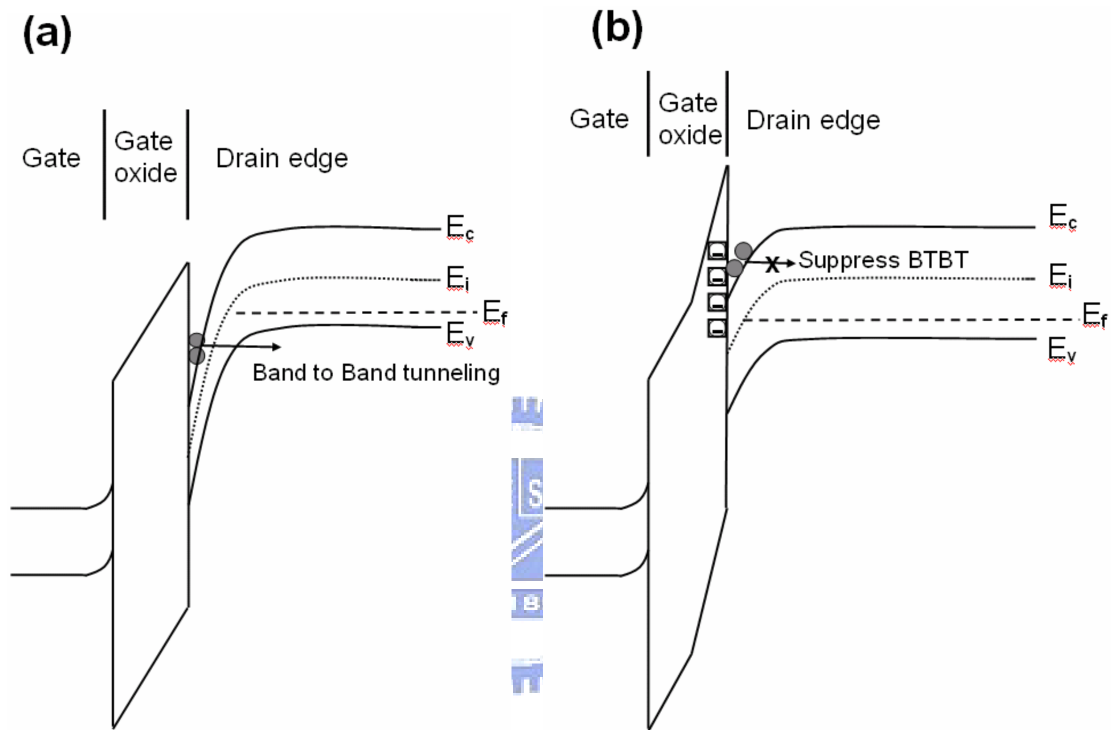


Fig. 3-4 Schematic illustrations of (a)BTBT occurring in the drain and (b)suppression of the BTBT after stress due to electron trapping in the oxide.

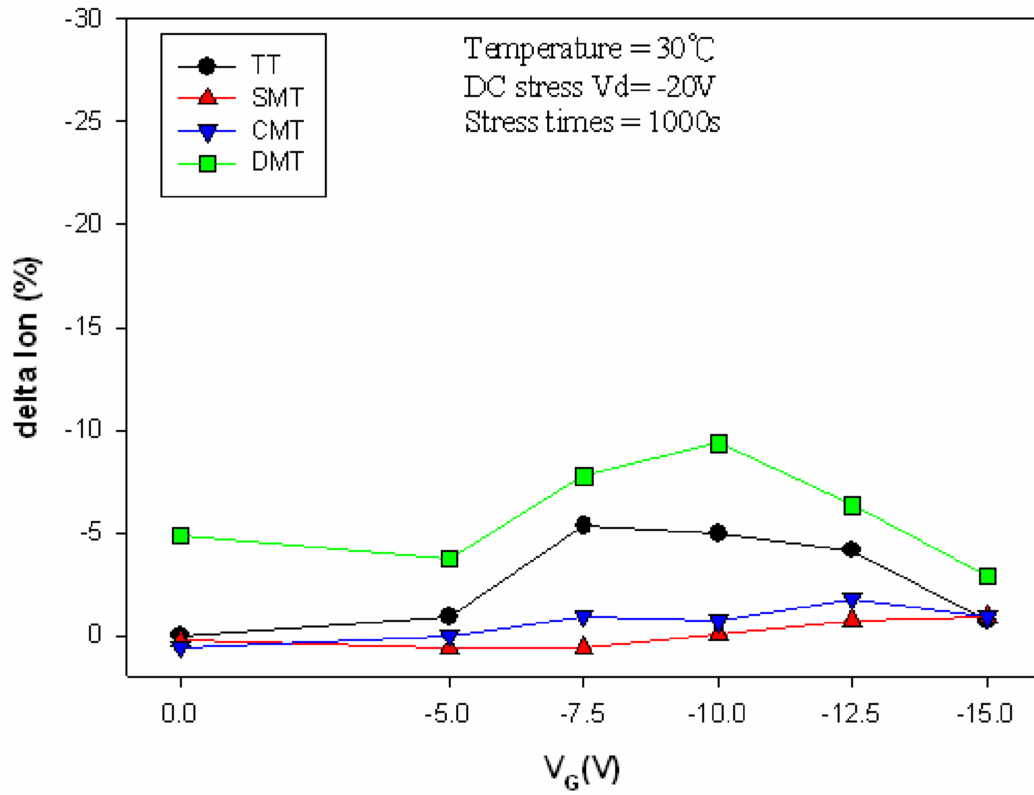


Fig. 3-5 On-current degradation of test structures under V_D of -20 V and various V_G for 1000 sec.

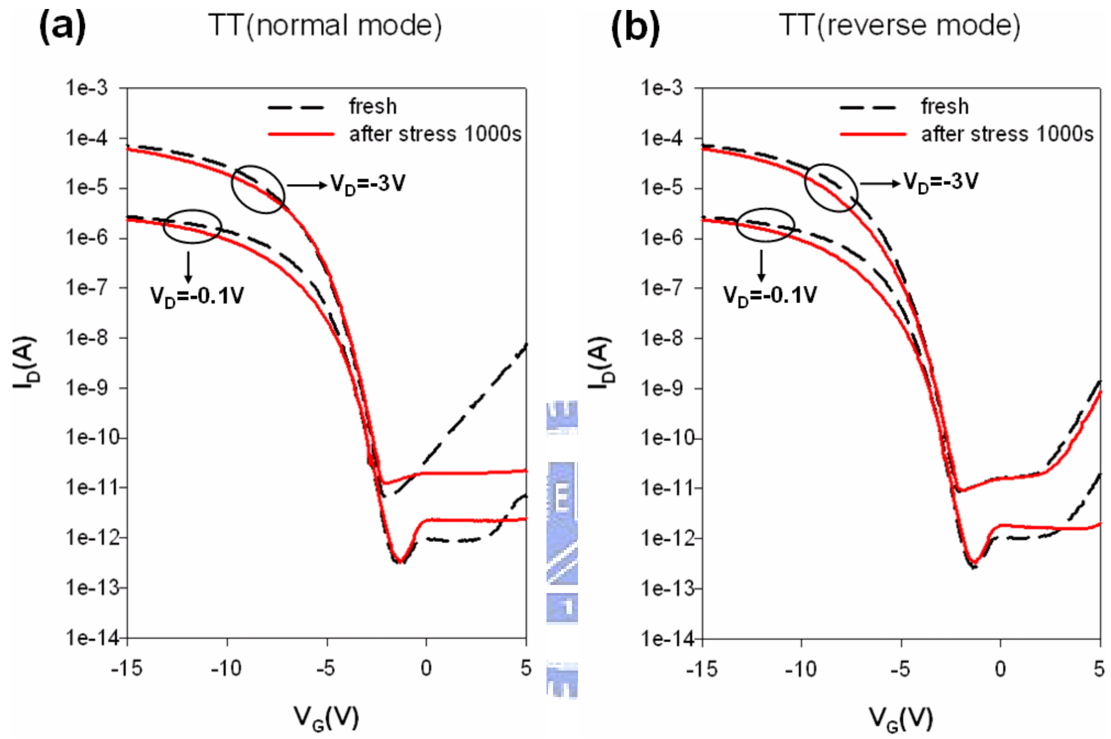
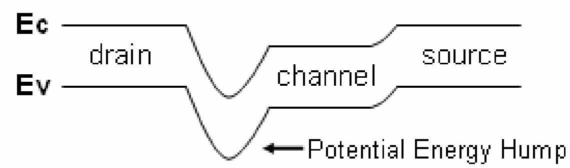
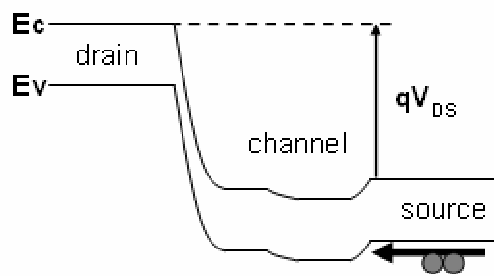
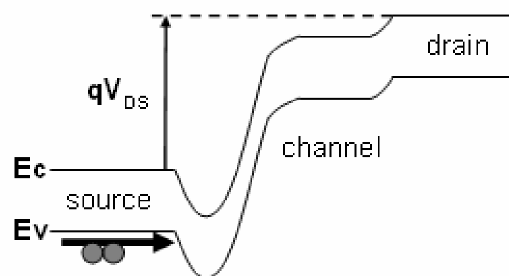


Fig. 3-6 Subthreshold characteristics of (a) normal mode and (b) reverse mode of a test transistor before and after higher DC stress at V_G/V_D of -7.5 V/-25 V for 1000 sec.



(a) After hot-carrier-induced degradation (normal mode)





(b) High V_{DS} (normal mode) **(c)** High V_{DS} (reverse mode)

Fig. 3-7 Energy band diagrams under different measurement configurations.

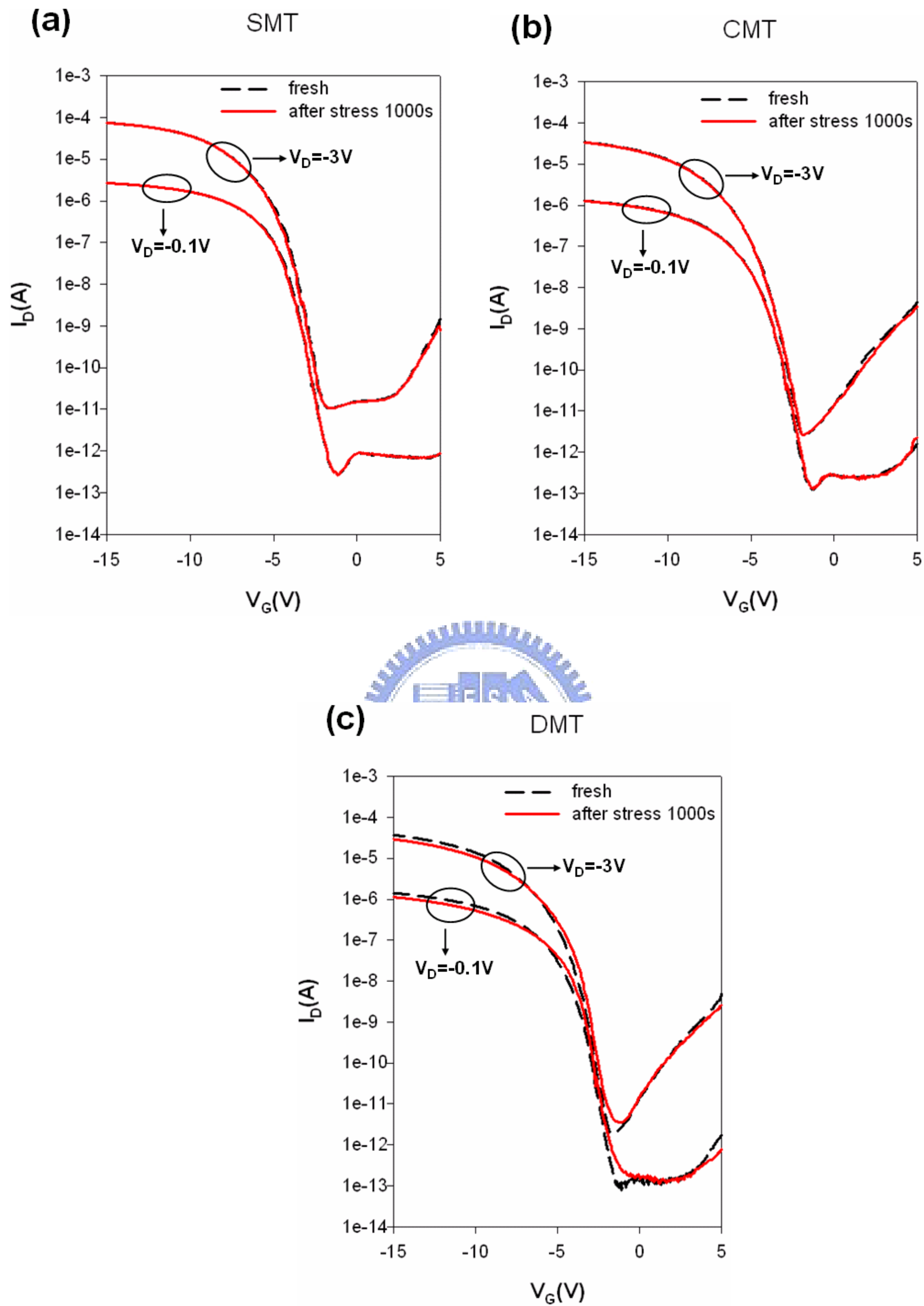


Fig. 3-8 Subthreshold characteristics of (a)SMT, (b)CMT and (c)DMT transistors contained in the same test structure characterized in Fig. 3-8 before and after higher DC stress at V_G/V_D of -7.5 V/-20 V for 1000 sec.

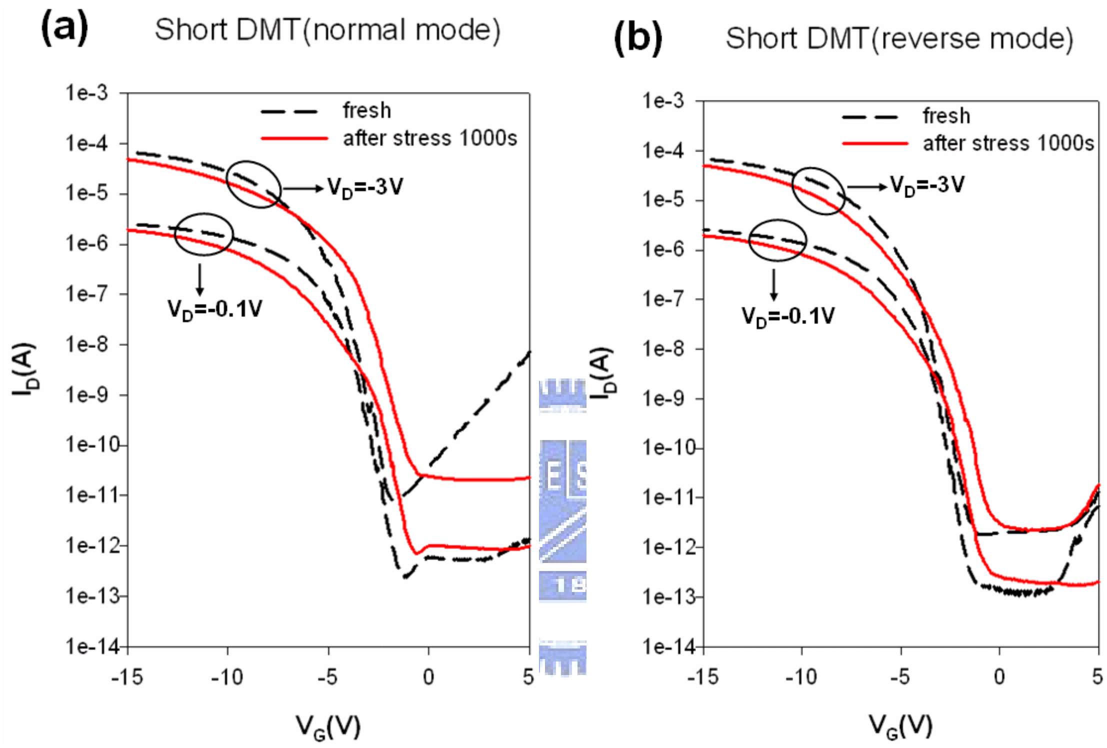


Fig. 3-9 Subthreshold characteristics of (a) normal mode and (b) reverse mode of the Short DMT before and after higher DC stress at V_G/V_D of -7.5 V/-25 V for 1000 sec

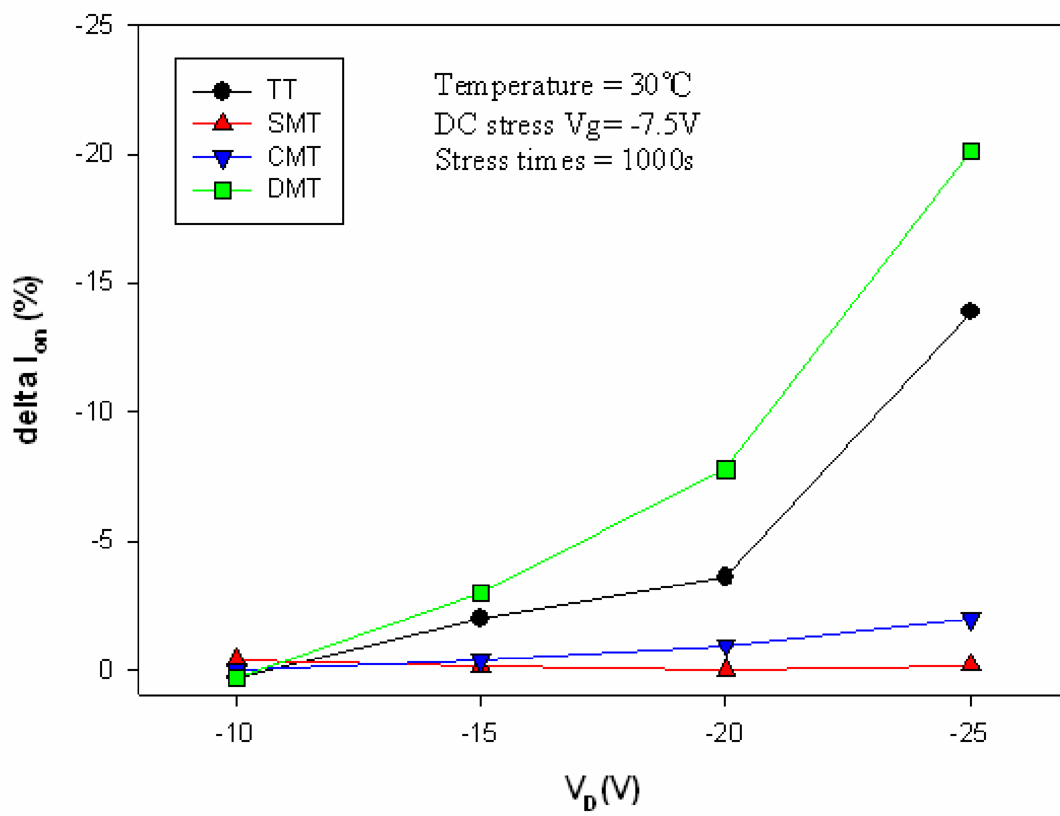


Fig. 3-10 On-current degradation of TT and different MTs as a function of stress V_D with V_G= -7.5 V for 1000 sec.

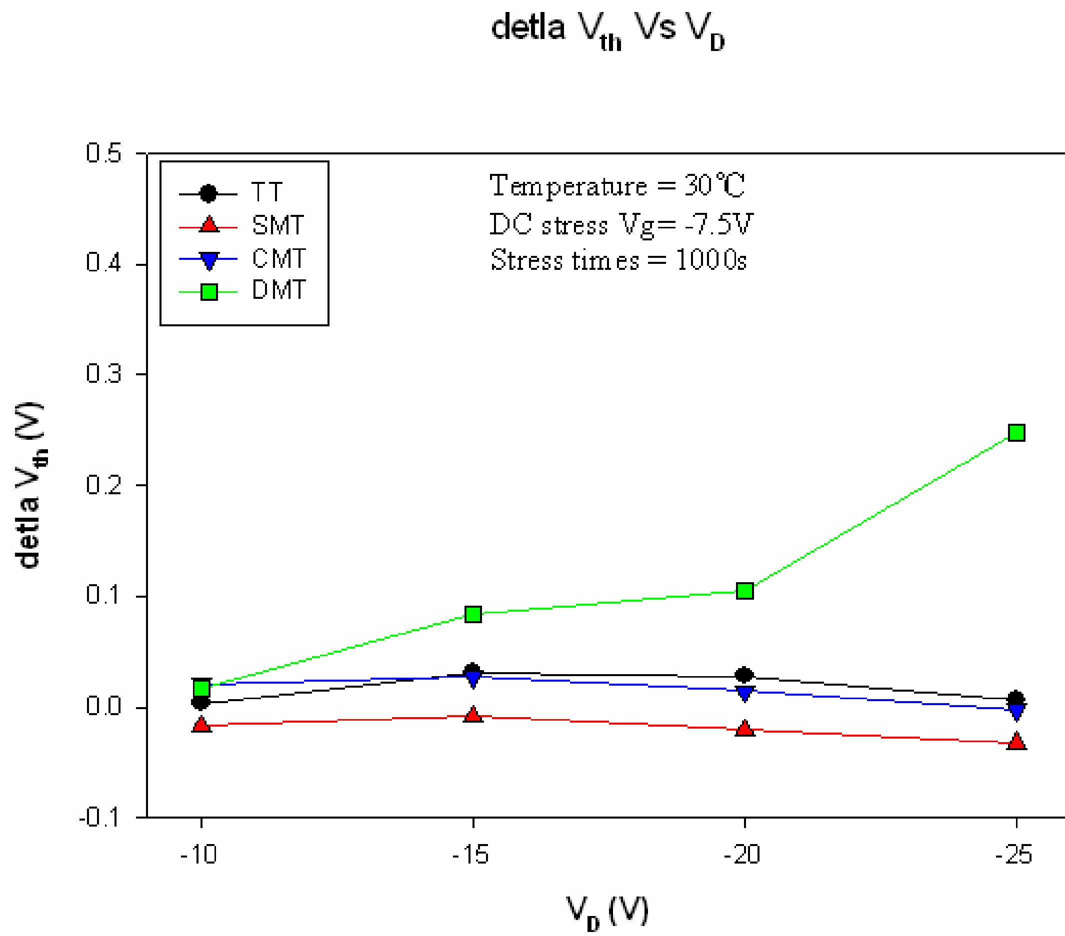


Fig. 3-11 Threshold voltage shifts of the test structure under V_G of -7.5 V and various V_D for 1000 sec.

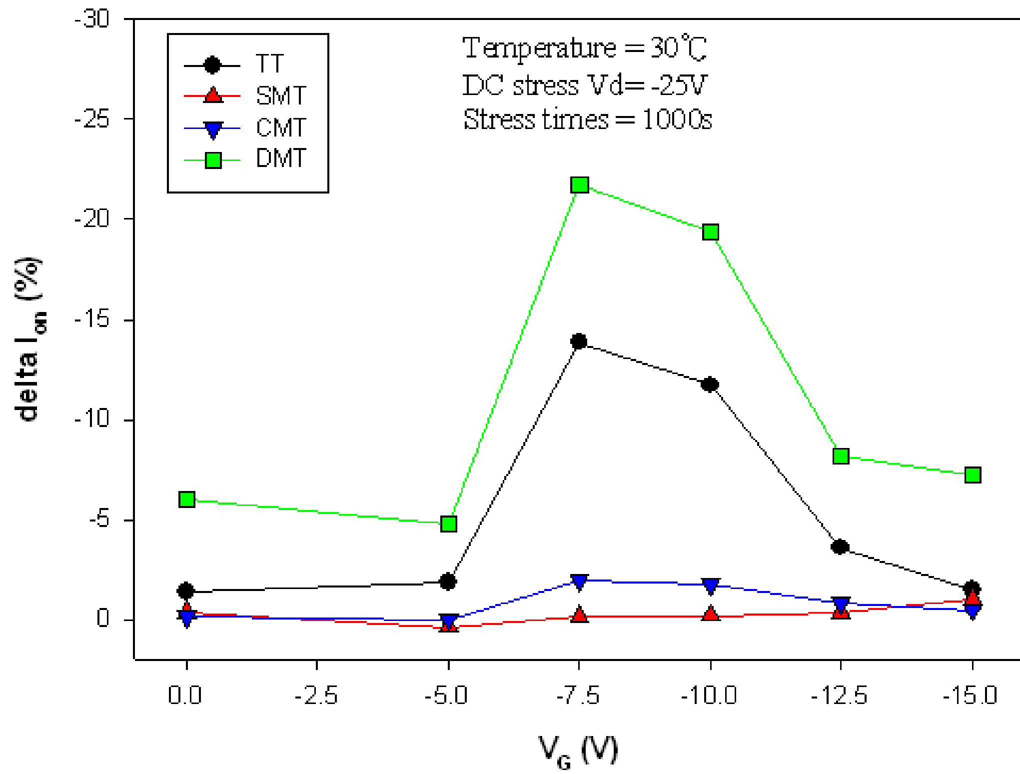


Fig. 3-12 The on-current degradation of TT and different MTs as a function of stress V_G with V_D= -25 V for 1000 sec.

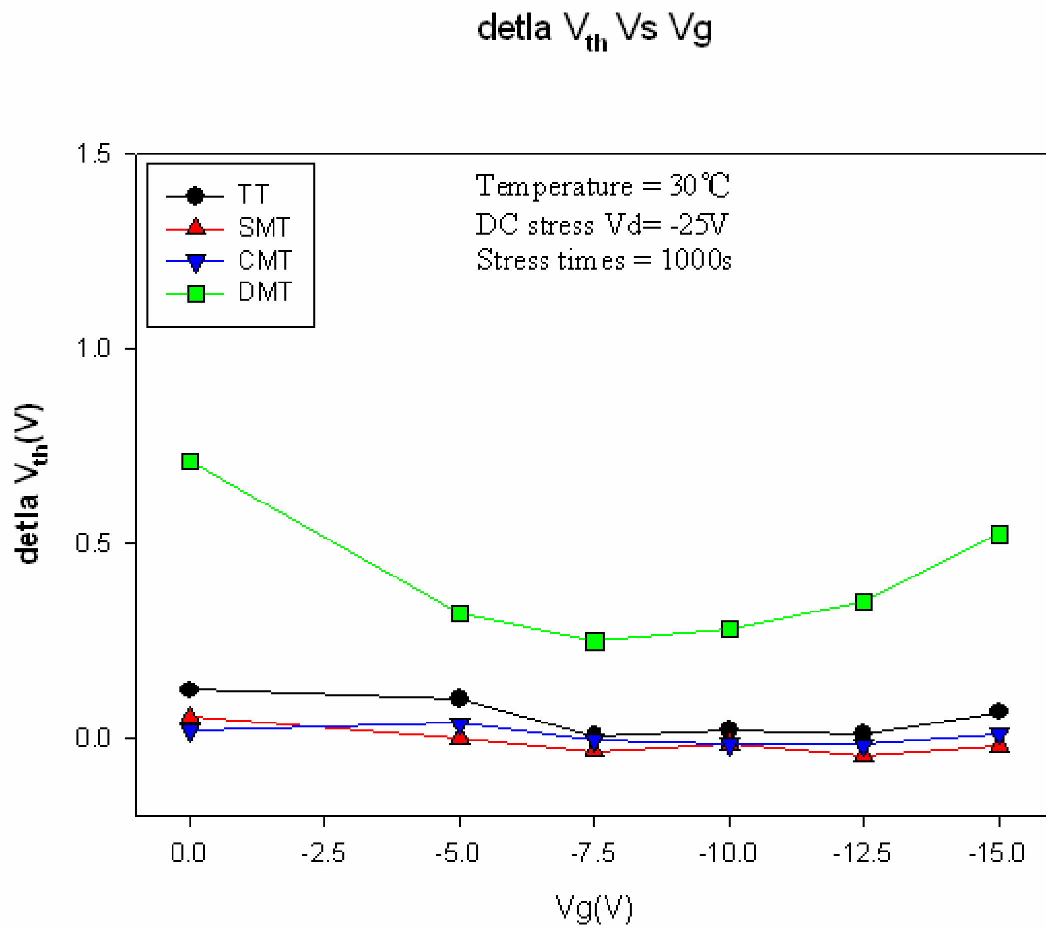


Fig. 3-13 Threshold voltage shift of the test structure under V_D of -25 V and various V_G for 1000 sec.

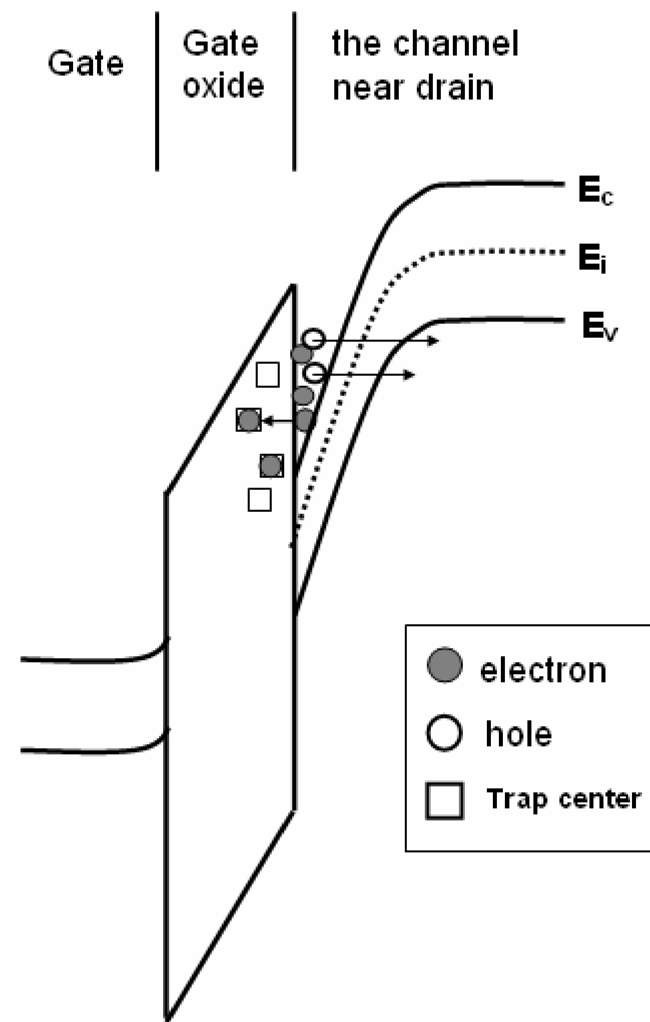


Fig. 3-14 Schematic illustration of electrons trapped in the gate oxide under high vertical electric field.

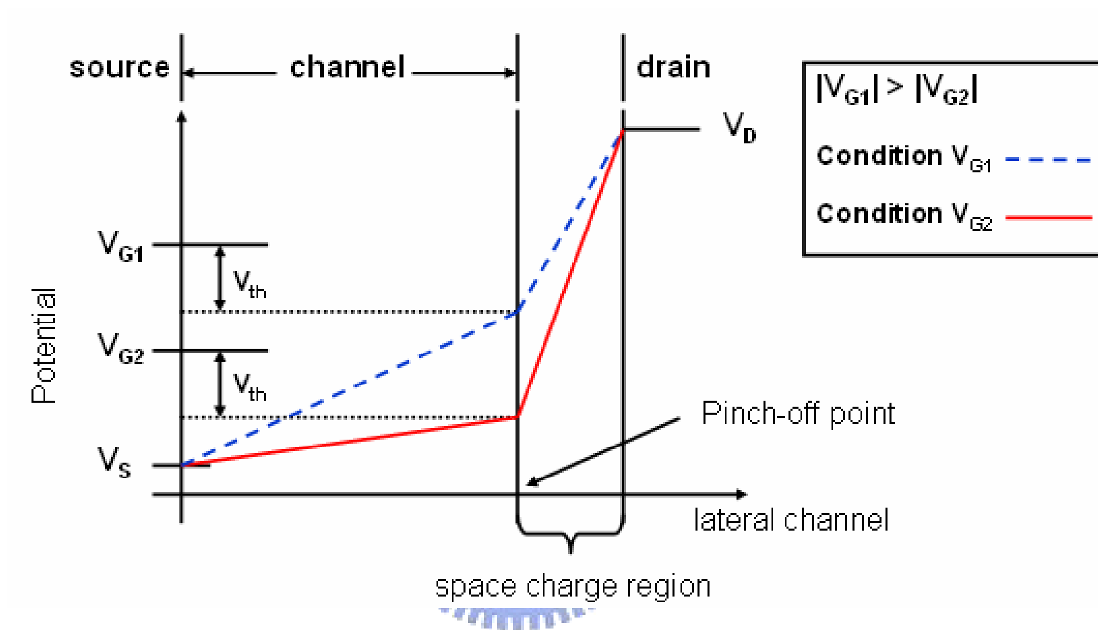


Fig.3-15 The distribution of potential and electric field at space charge region.

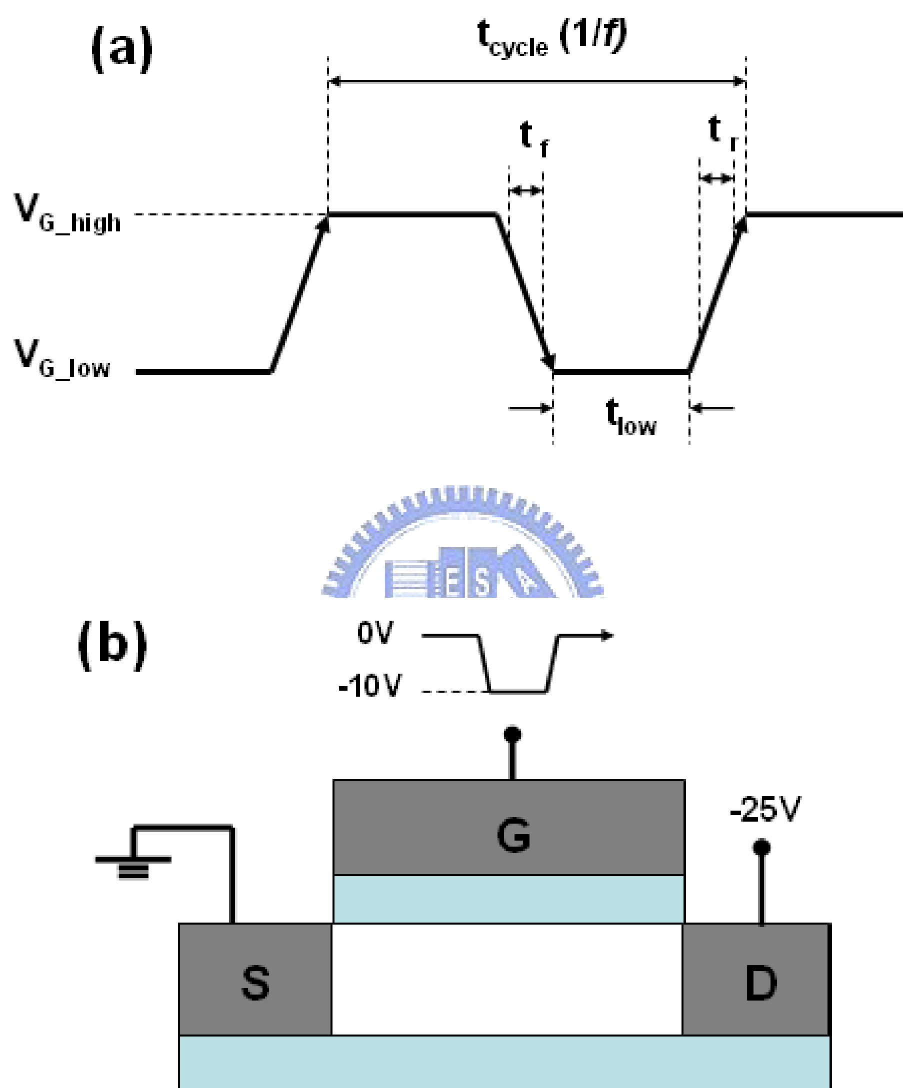


Fig. 4-1 (a) Major parameters in the AC signal train. (b) AC stress configuration.

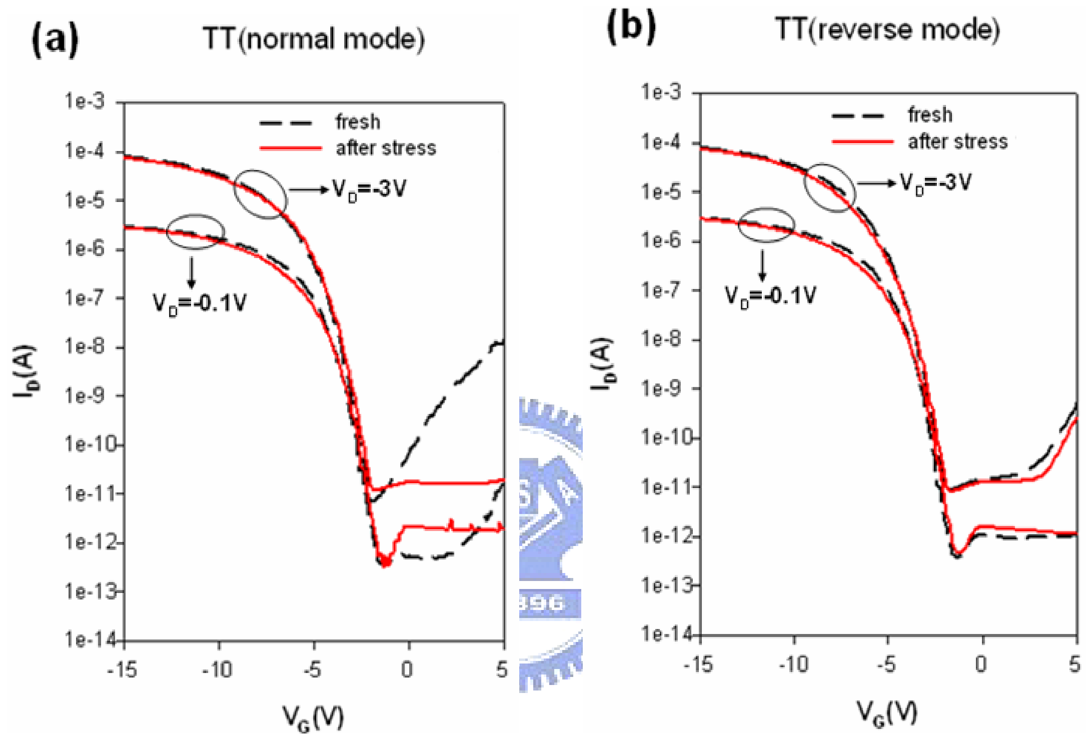


Fig. 4-2 Subthreshold characteristics of TT under (a) normal- and (b) reverse-mode of measurements before and after the AC stressing under V_{G_low}/V_D=-10 V/-25 V, freq.=500 kHz, tr=tf=100 ns and total t_{low}=500 sec.

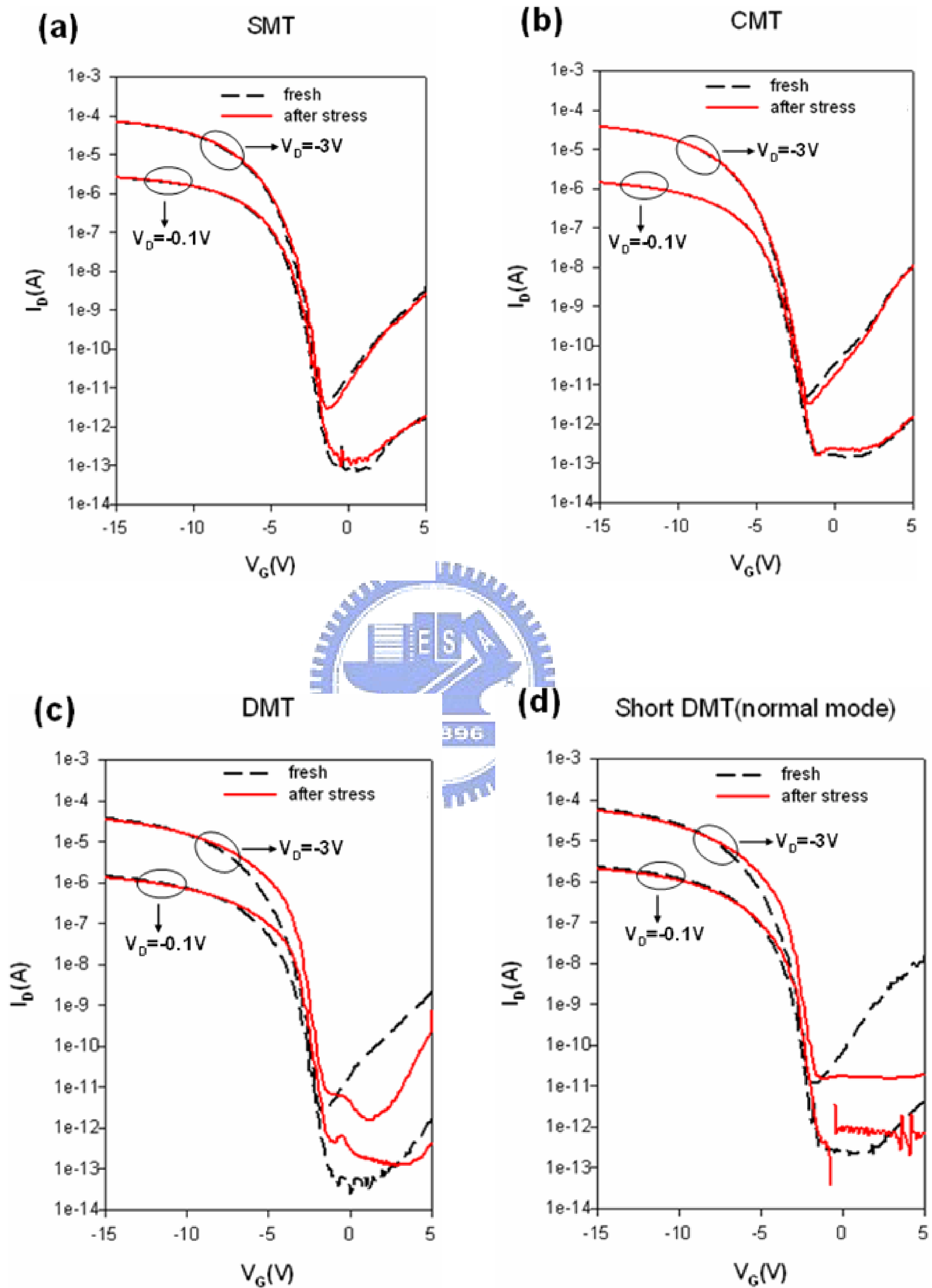


Fig. 4-3 Subthreshold characteristics of (a) SMT, (b) CMT, (c) DMT and short-DMT transistors in a test structure before and after the AC stressing under V_{G_low}/V_D=-10 V/-25 V, freq.=500 kHz, tr=tf=100 ns and total t_{low}=500 sec.

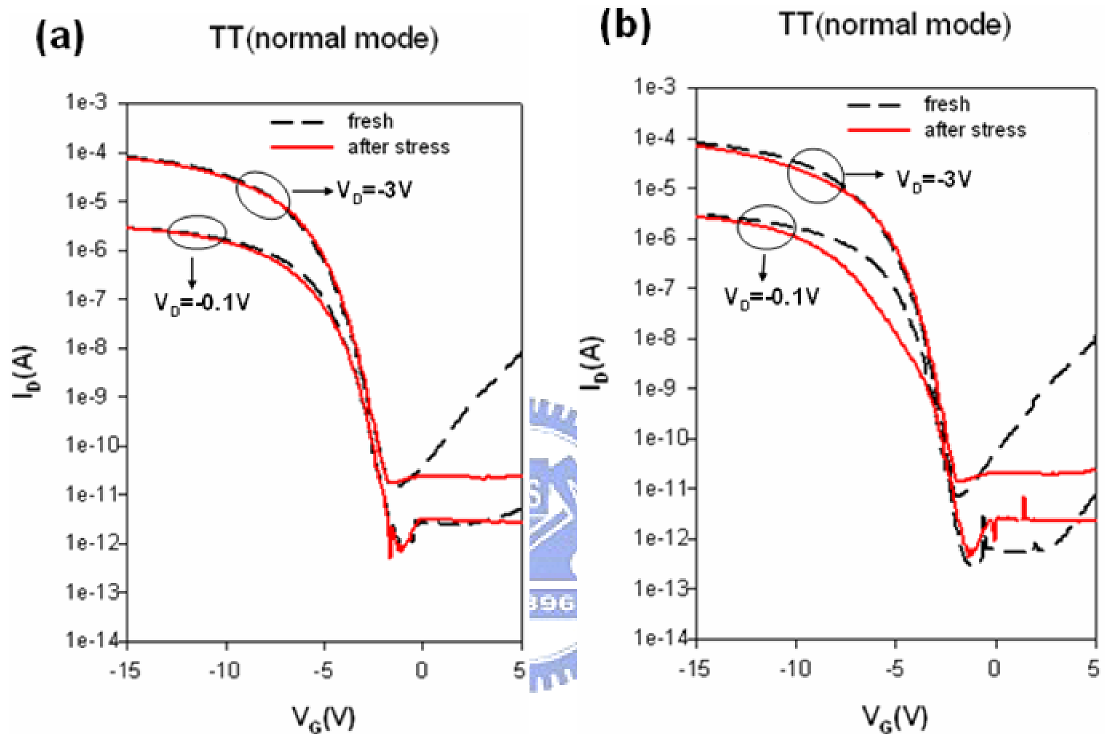


Fig. 4-4 Subthreshold characteristics of a TT before and after AC stress for 500 sec with the frequency of (a) 100 kHz and (b) 1 MHz.

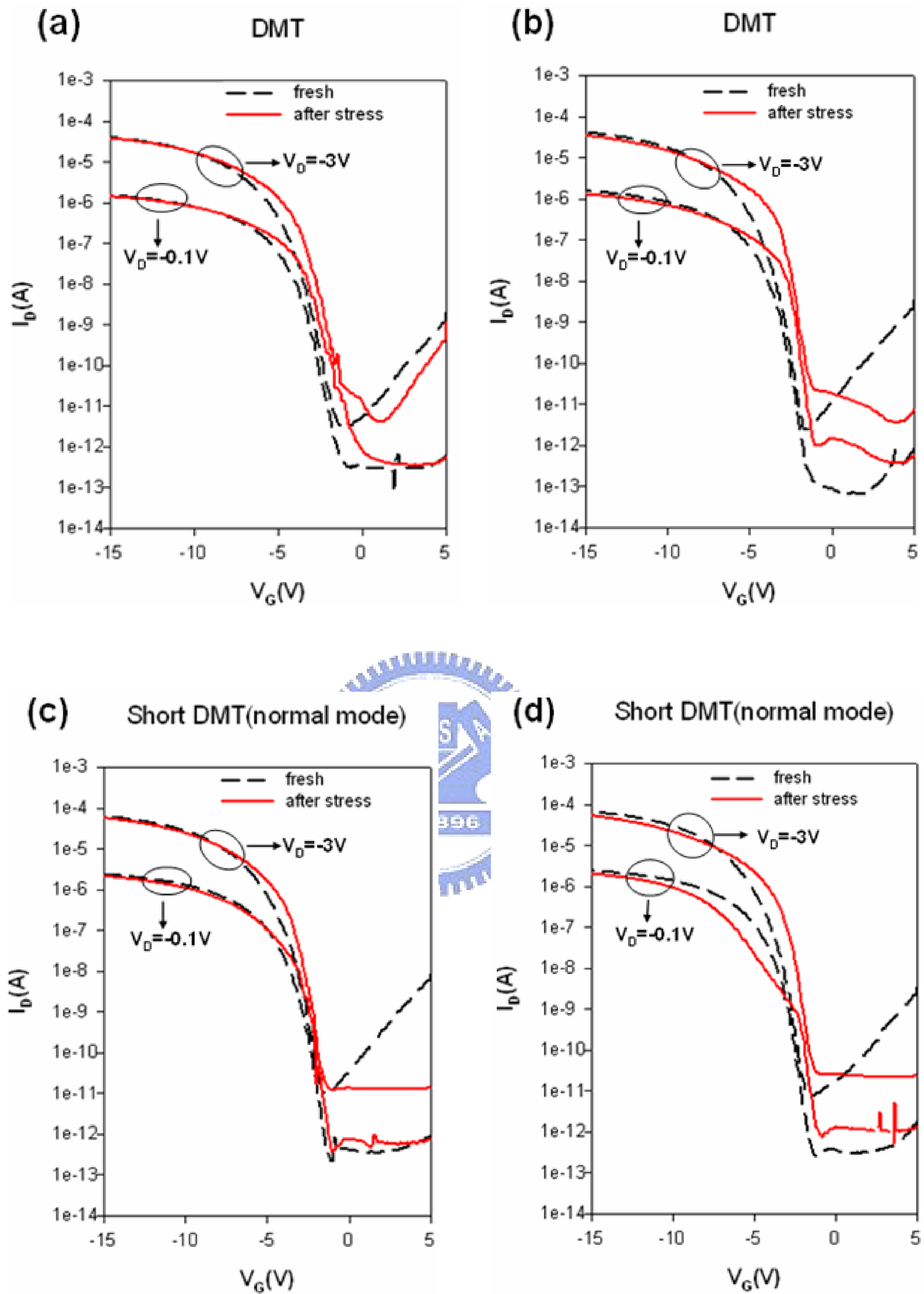


Fig. 4-5 Subthreshold characteristics before and after AC stress for 500 sec with the frequency of (a) 100 kHz and (b) 1 MHz for DMT, and (c) 100 kHz and (d) 1 MHz for short-DMT.

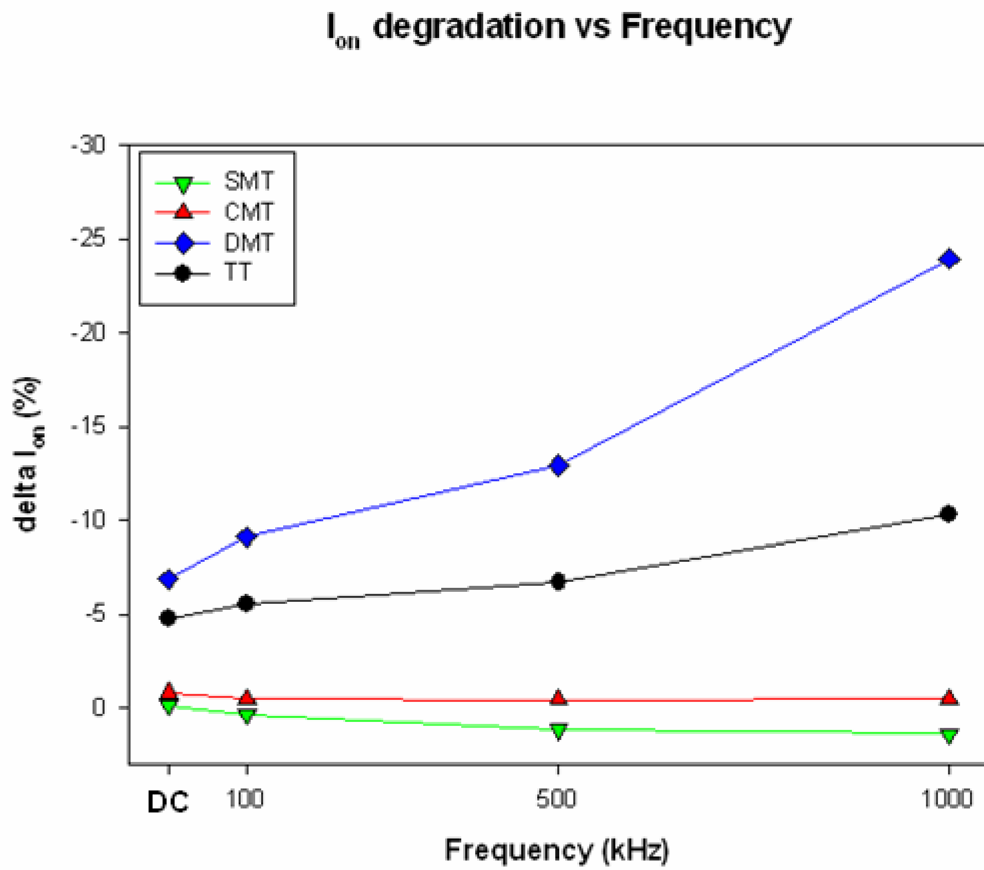


Fig. 4-6 On-current degradation as a function of frequency under AC stress.

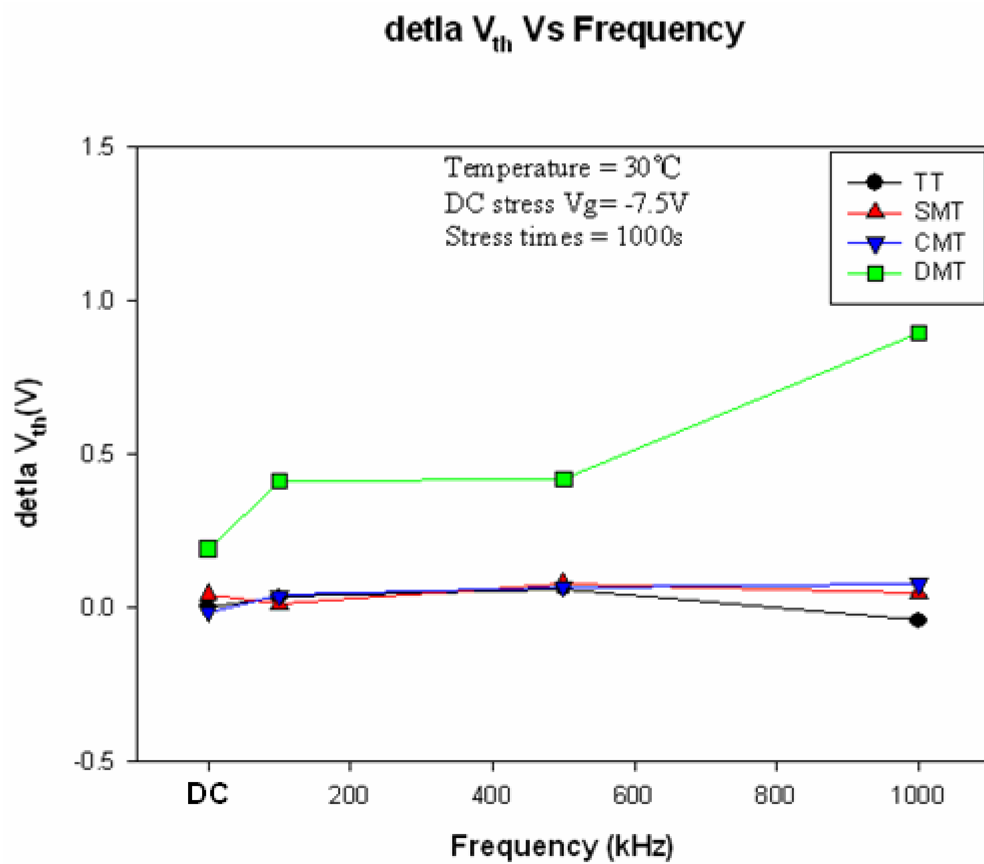


Fig. 4-7 Threshold voltage shift as a function of frequency under AC stress.

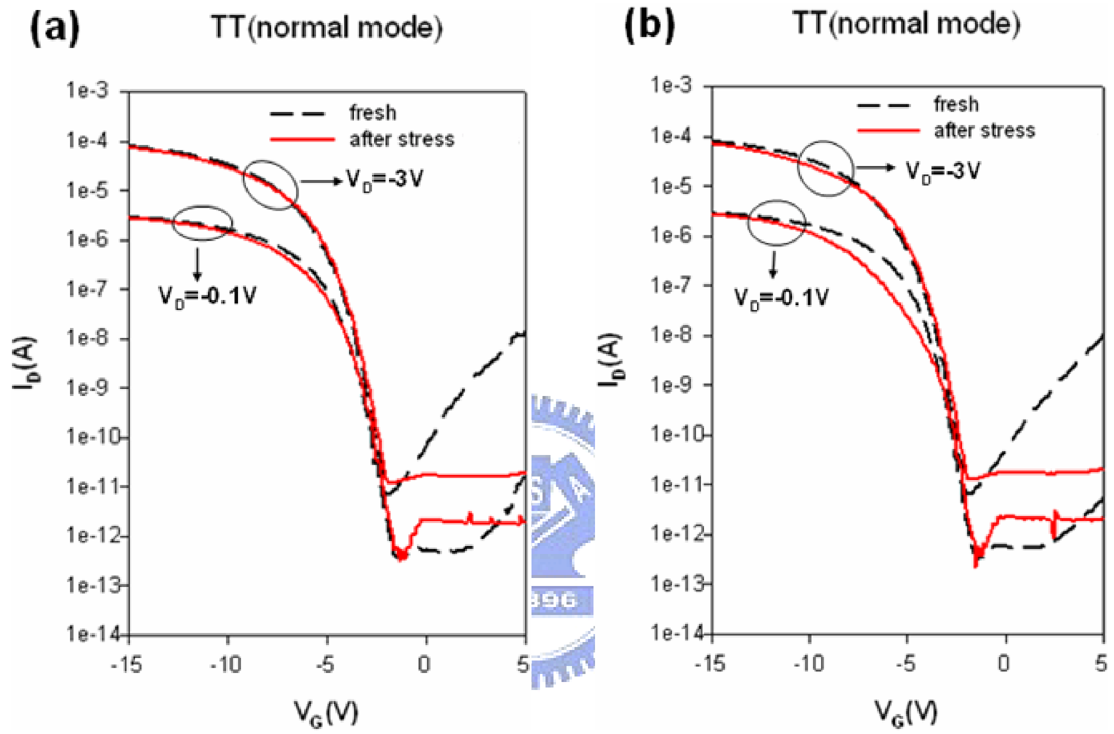


Fig. 4-8 Subthreshold characteristics before and after AC stress for 500 sec with the rising time of (a) 100 ns and (b) 10 ns for TT.

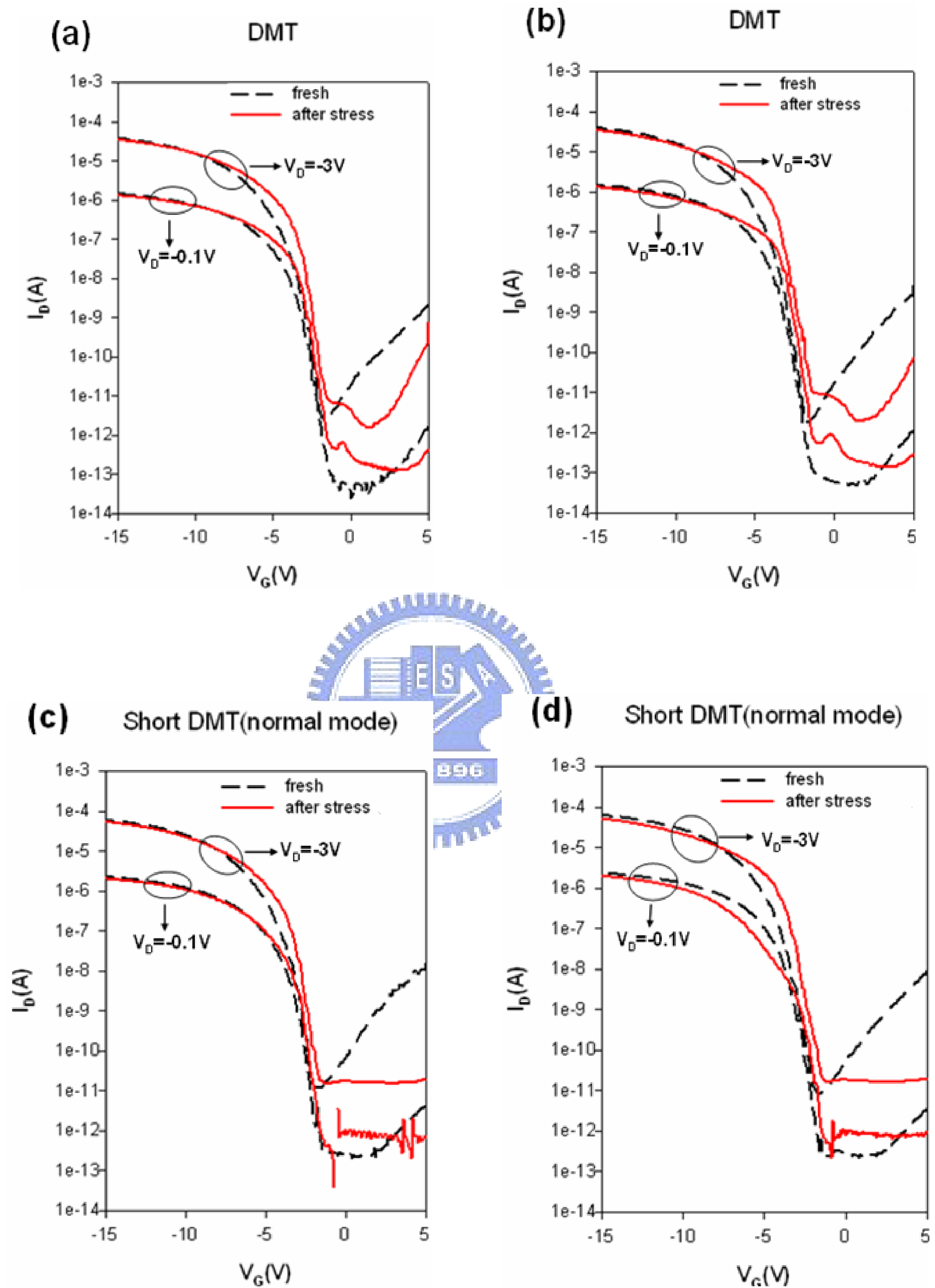


Fig. 4-9 Subthreshold characteristics before and after AC stress for 500 sec with the rising time of (a) 100 ns and (b) 10 ns for DMT, and (c) 100 ns and (d) 10 ns for short-DMT.

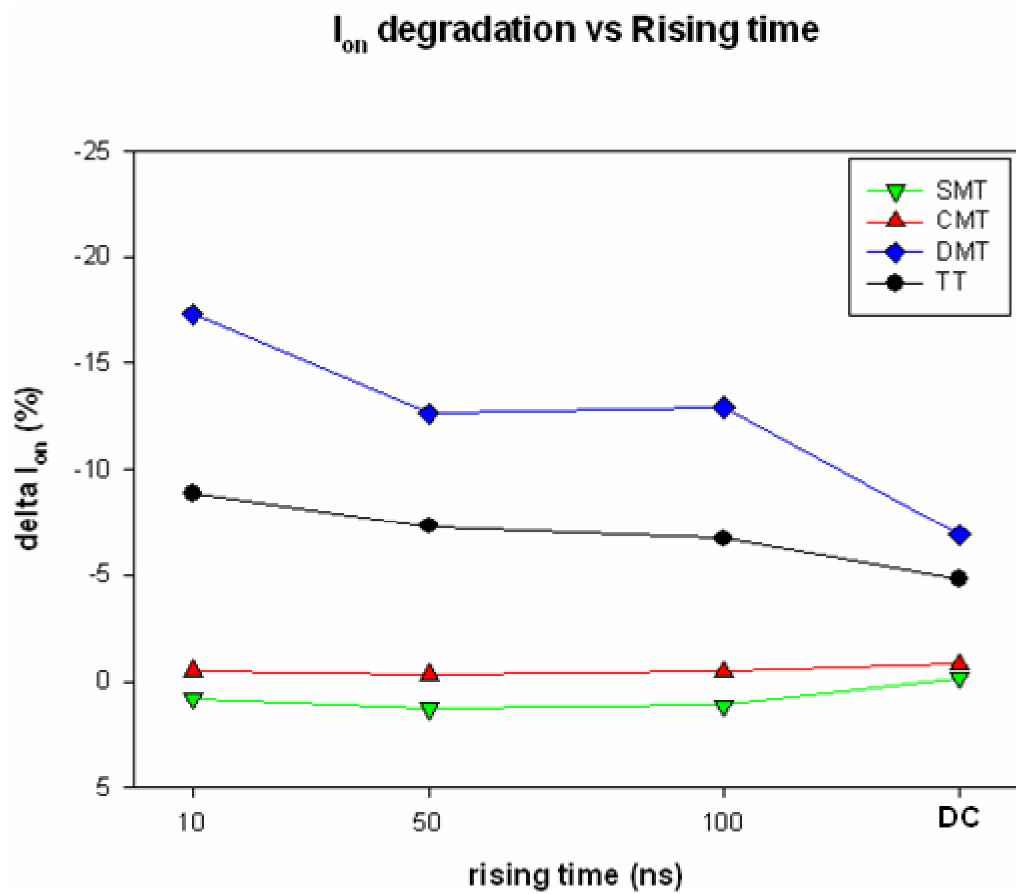


Fig. 4-10 On-current degradation as a function of rising time under AC stress.

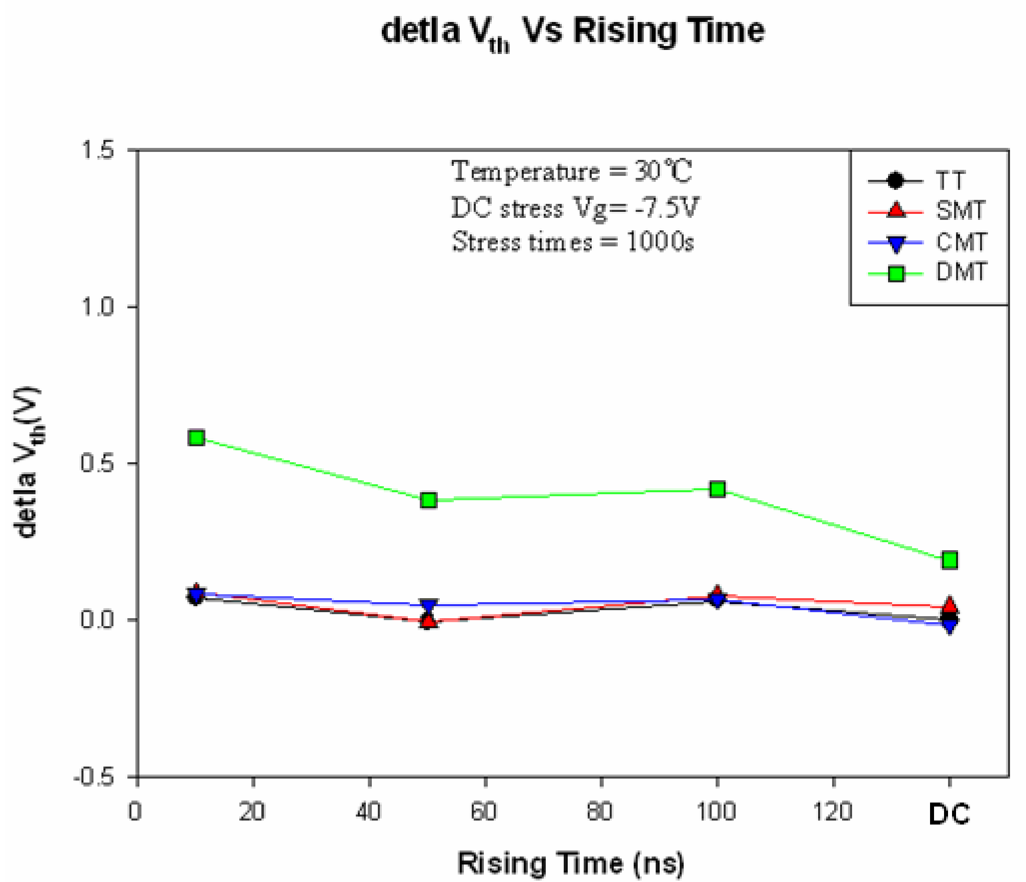


Fig. 4-11 Threshold voltage shift as a function of rising time under AC stress.

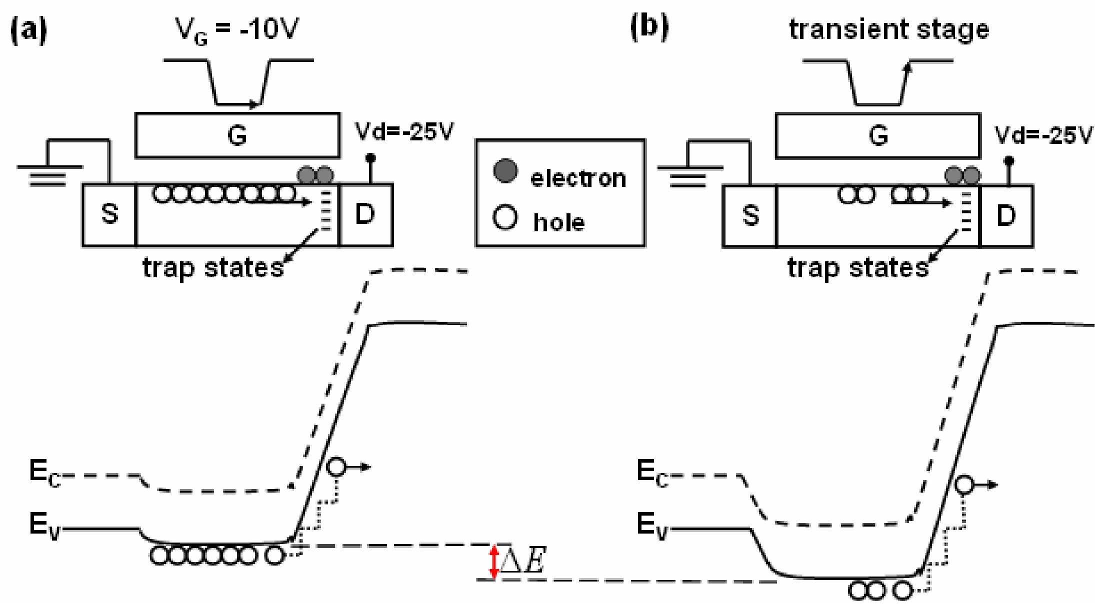


Fig. 4-12 Degradation mechanism of variable rising time under AC stress.

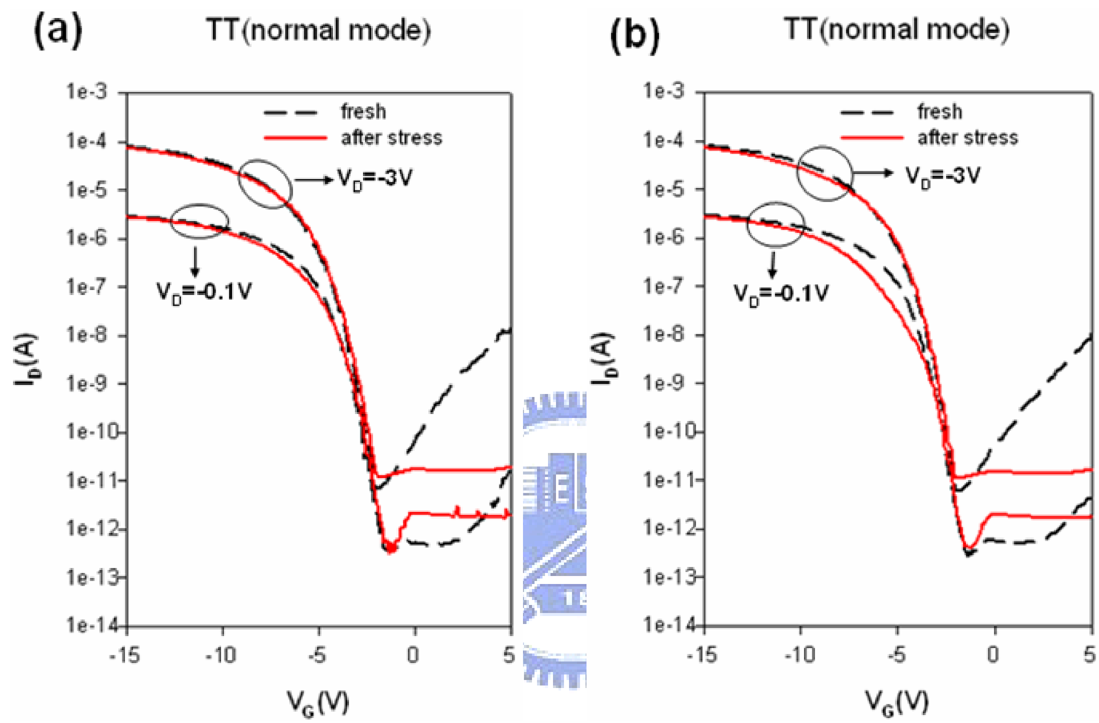


Fig. 4-13 Subthreshold characteristics before and after AC stress for 500 sec with the falling time of (a) 100 ns and (b) 10 ns for TT.

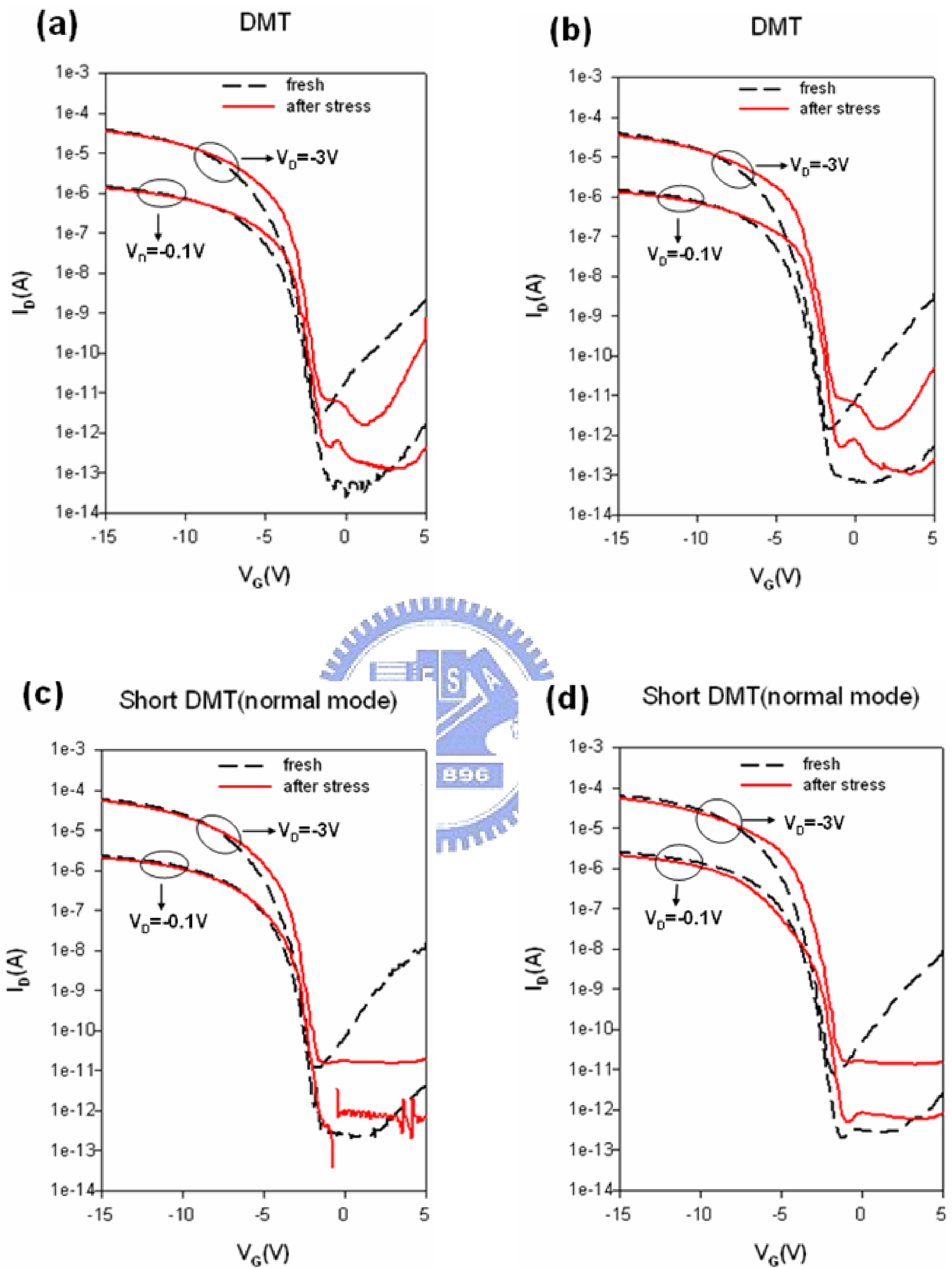


Fig. 4-14 Subthreshold characteristics before and after AC stress for 500 sec with the falling time of (a) 100 ns and (b) 10 ns for DMT, and (c) 100 ns and (d) 10 ns for short-DMT.

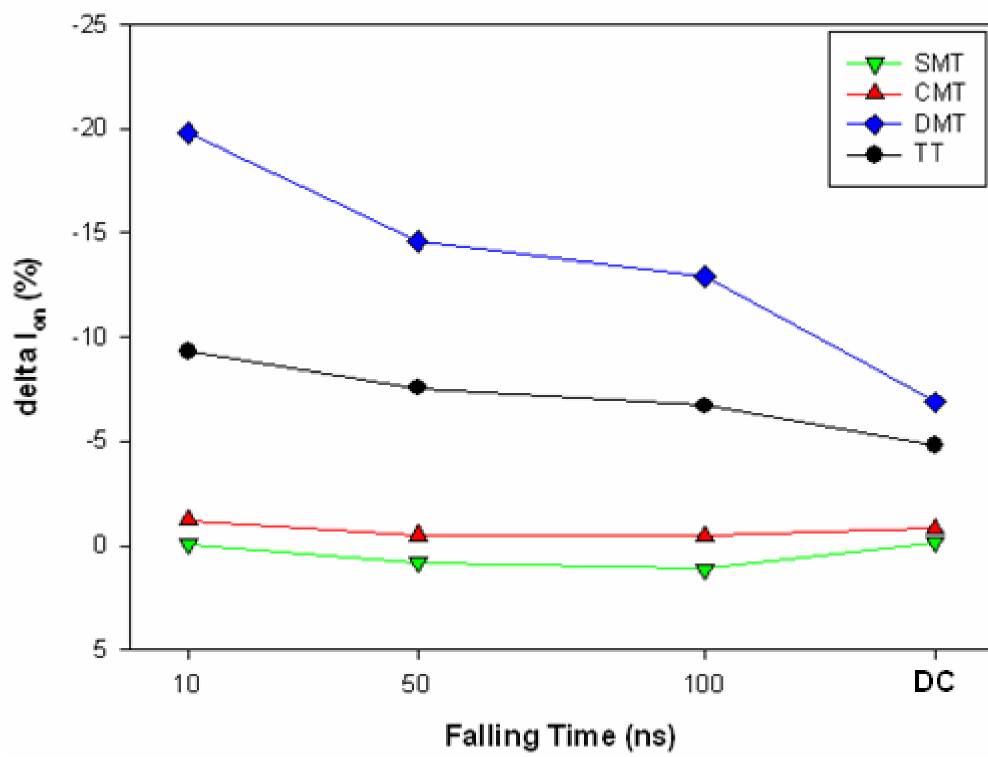


Fig. 4-15 On-current degradation as a function of falling time under AC stress.

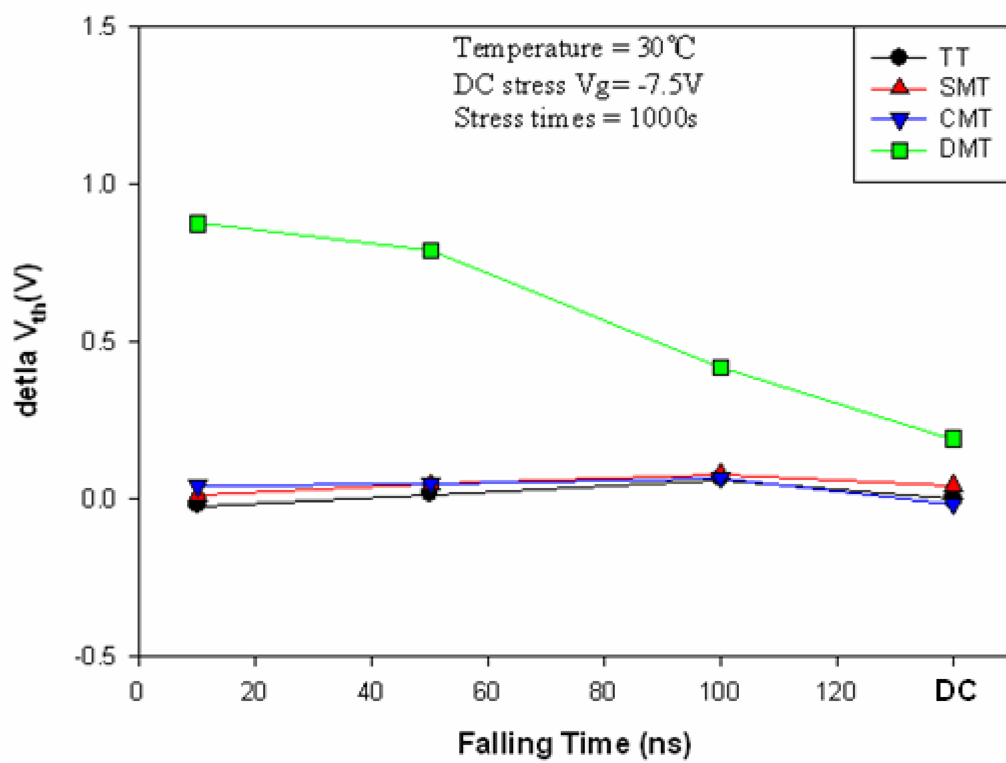


Fig. 4-16 Threshold voltage shift as a function of falling time under AC stress.

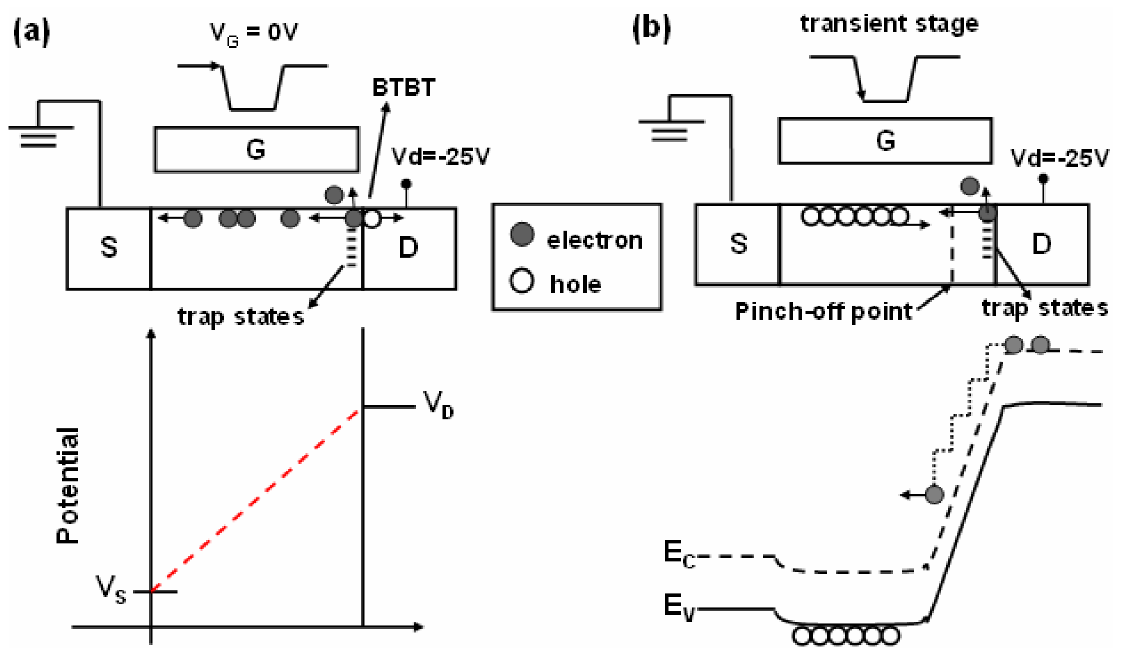


Fig. 4-17 Degradation mechanism of variable falling time under AC stress.

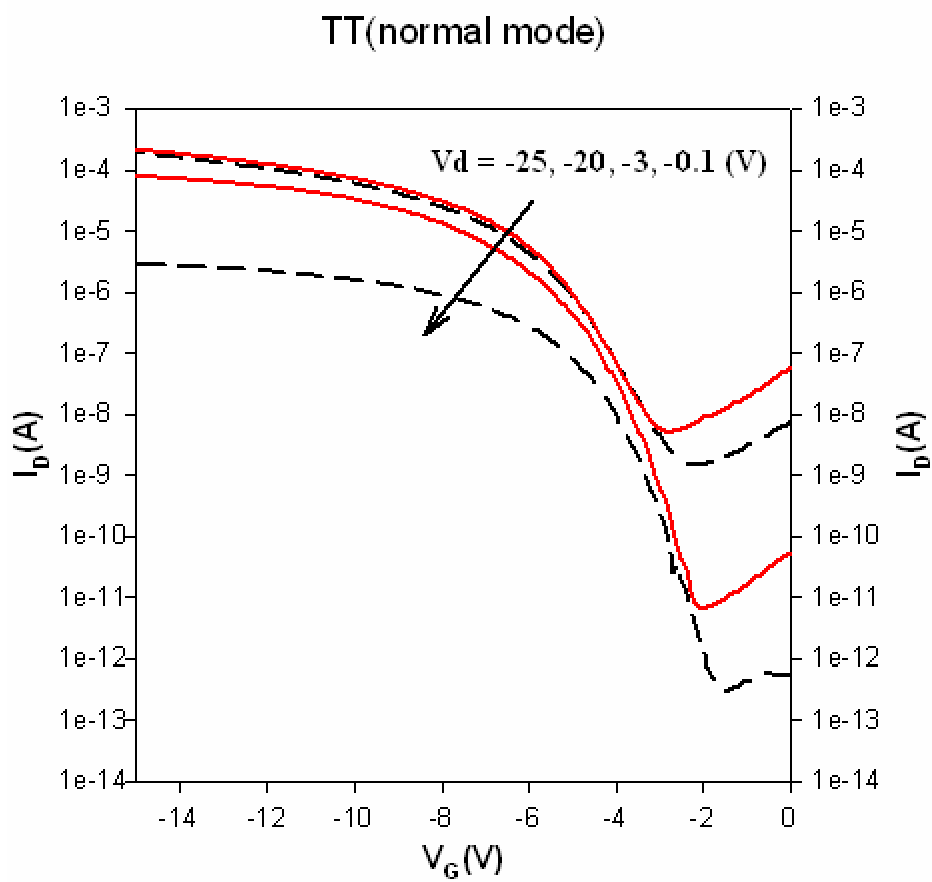


Fig. 4-18 Subthreshold characteristics of TT before stressing.

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論文題目：

利用新穎結構對 P 型複晶矽薄膜電晶體進行之熱載子衰退機制分析

A Study of P-Channel Poly-Si TFT Degradation under Hot-Carrier Stress Using a Novel Test Structure