

# 臨場濕式氧化方法在金屬鎢奈米點非揮發性記憶體之製作與研究

研究生:謝介銘

指導教授:羅正忠博士

張鼎張博士

國立交通大學

電子工程學系電子研究所

## 摘要

非揮發性記憶體(NVM)目前在元件尺寸持續微縮下的需求為高密度記憶單元、低功率損耗、快速讀寫操作、以及良好的可靠度(Reliability)。傳統浮動閘極(floatinggate)記憶體在操作過程中如果穿隧氧化層產生漏電路徑會造成所有儲存電荷流失回到矽基板，所以在資料保存時間(Retention)和耐操度(Endurance)的考量下，很難去微縮穿隧氧化層的厚度。非揮發性奈米點記憶體被提出希望可取代傳統浮動閘極記憶體，由於奈米點可視為電荷儲存層中彼此分離的儲存點，可以有效改善小尺寸記憶體元件多次操作下的資料儲存能力。近年來發展了許多方法來形成奈米點，一般而言，大多數的方法都需要長時間高溫的熱製程，這個步驟會影響現階段半導體製程中的熱預算和產能。

臨場濕式氧化方法是一種引入少許氫氣的濕式氧化過程，由於氫氣可以幫助產生更多的氧自由基，所以它相較於乾式氧化或快速升溫氧化法有更快的氧化速率，而且許多的文獻已證實用臨場濕式氧化方法所製作的氧化層有較好的品質與可靠度。在本論文中，我們利用臨場濕式氧化方法來製作鎢奈米點記憶體，分別應用在穿隧氧化層和奈米點的形成，並且和快速升溫氧化法做比較。另外，我們也將臨場濕式氧化方法的溫度、氧化時間、氫氣含量對於鎢奈米點形成的影響做詳細的探討與研究。

**Study and Fabrication on the Tungsten metal  
Nanocrystals Nonvolatile Memory  
by the Application of the In-Situ Steam-Generation  
(ISSG)**

Student: Chieh-Ming Hsieh

Advisors: Dr. Jen-Chung Lou  
Dr. Ting-Chang Chang

**Department of Electronic Engineering and Institute of Electronics  
National Chiao Tung University**

**Abstract**

Current requirements of nonvolatile memory (NVM) are the high density cells, low-power consumption, high-speed operation and good reliability for the scaling down devices. However, all of the charges stored in the floating gate will leak into the substrate if the tunnel oxide has a leakage path in the conventional NVM during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down in terms of charge retention and endurance characteristics. The nonvolatile nanocrystal memories are one of promising candidates to substitute for conventional floating gate memory, because the discrete storage nodes as the charge storage media have been effectively improve data retention under endurance test for the scaling down device. Many methods have been developed recently for the formation of nanocrystal. Generally, most methods need thermal treatment with high temperature and long duration. This procedure will influence thermal budget and throughput in current manufacture technology of semiconductor industry.

The in-situ-steam-generation-process (ISSG) oxidation process is a wet oxidation with some hydrogen introduced in it. It has a faster oxidation rate than dry

and RTO oxidation due to more oxygen radicals produced by hydrogen. Because of its quick oxidation rate, ISSG provides excellent quality of thin oxide and many references have demonstrated that ISSG oxide shows much better reliability property than dry or RTO oxide. In this thesis, we apply ISSG to fabricate our tungsten nanocrystals nonvolatile memory. The applications are on the tunneling oxide fabrication and nanocrystals formation, respectively. The comparisons were made between the ISSG and RTO oxidation methods. The effects of ISSG temperature, oxidation time and H<sub>2</sub> contents on tungsten nanocrystals formation are also investigated in our study.

# Contents

## Page

<b>Abstract(Chinese)</b> .....	I
<b>Abstract(English)</b> .....	II
<b>Contents</b> .....	IV
<b>Figure Captions</b> .....	VI
<b>Chapter 1 Introduction</b>	
<b>1-1 Overview of nonvolatile memory</b>	
1-1-1 SONOS Nonvolatile Memory Devices .....	3
1-1-2 Nanocrystal Nonvolatile Memory Devices .....	5
<b>1-2 Organization of the dissertation</b> .....	10
<b>Chapter 2 Basic principle of nonvolatile memory</b>	
<b>2-1 Program / Erase mechanisms</b>	
2-1-1 Hot-Electron Injection.....	15
2-1-2 Tunneling Injection.....	16
2-1-3 Band to Band Tunneling.....	18
<b>2-2 Nonvolatile memory reliability</b>	
2-2-1 Retention Time.....	19
2-2-2 Endurance.....	21
<b>2-3 The material physics and characteristics for nanocrystal</b>	
2-3-1 Quantum Confinement.....	22
2-3-2 Coulomb Blockade.....	22
<b>Chapter 3 Formation of W-NCs Nonvolatile Memory based on ISSG</b>	
<b>3-1 Motivation</b> .....	31
<b>3-2 The effect of ISSG temperature on W-NCs</b>	
3-2-1 Experimental Steps.....	32

	3-2-2 Results and discussions.....	33
	<b>3-3 The effect of ISSG oxidation time on W-NCs</b>	
	3-3-1 Experimental Steps.....	36
	3-3-2 Results and discussions.....	37
	<b>3-4 Conclusions.....</b>	<b>38</b>
<b>Chapter4</b>	<b>Comparison of different oxidation methods for W-NCs Nonvolatile Memory</b>	
	<b>4-1 Motivation.....</b>	<b>56</b>
	<b>4-2 The comparison of tunneling oxide</b>	
	4-2-1 Experimental Steps.....	56
	4-2-2 Results and discussions.....	57
	<b>4-3 The comparison of trapping layer</b>	
	4-3-1 Experimental Steps.....	59
	4-3-2 Results and discussions.....	59
	<b>4-4 Conclusions.....</b>	<b>61</b>
<b>Chapter5</b>	<b>The effect of H<sub>2</sub> content in ISSG system</b>	
	<b>5-1 Motivation.....</b>	<b>75</b>
	<b>5-2 The effect of H<sub>2</sub> content</b>	
	5-2-1 Experimental Steps.....	75
	5-2-2 Results and discussions.....	76
	<b>5-3 Conclusions.....</b>	<b>78</b>
<b>Chapter 6</b>	<b>Conclusions</b>	
	<b>6-1 Conclusions.....</b>	<b>90</b>
<b>References.....</b>		<b>91</b>

# Figure Captions

## Chapter 1

- Fig 1-1 The structure of the conventional floating-gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.....11
- Fig 1-2 The development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.....12
- Fig 1-4 The structure of the nanocrystal nonvolatile memory device. The semiconductor nanocrystals or metal nanocrystals are used as the charge storage element instead of the continuous poly-Si floating gate.....14

## Chapter 2

- Fig 2-1 I–V curves of an FG device when there is no charge stored in the FG (curve A) and when a negative charge  $\bar{Q}$  is stored in the FG (curve B).....24
- Fig 2-2 Schematic cross section of MOSFET. The energy- distribution function at point X1; Y1 is also shown.....24
- Fig 2-3 Fourth approaches to programming methods, described by Hu and White. (a) Direct tunneling (DT) (b) Fowler-Nordheim tunneling (FN)(c) modified Fowler-Nordheim tunneling (MFN) (d) trap assistant tunneling (TAT).....25
- Fig 2-4 Electron direct tunneling current from Au nanocrystals to Si substrate as a function of the electric field in tunnel oxide.....26
- Fig 2-5 Tunneling transmission coefficient through a rectangular SiO<sub>2</sub> barrier from metals with different work functions.....26
- Fig 2-6 It is evident that with a field of 7 MV/cm, the current density is about 10<sup>-8</sup> A/cm, while with a field of 10 MV/cm it is about 10<sup>-1</sup> A/cm . There is a variation of about seven orders of magnitude in tunnel current.....27
- Fig 2-7 Energy-band diagram for the proposed band to band induce hot electron injection mechanism and schematic illustration cross of the Flash

	memory with p-channel cell. Due to the positive bias to the control gate, holes are not injected into the tunnel oxide.....	27
Fig 2-8	Simulated the electron electric fields in Si substrate ( $E_{si}$ ) and in the tunnel oxide ( $E_{ox}$ ) during BBHE injection in the P-channel cell. It should be noted that although $E_{ox}$ , at the maximum band to band tunneling (BTBT) generation point is 10MV/cm, $E_{ox}$ of the electron injection point is a low 7.5MV/cm.....	28
Fig 2-9	Bandgap diagram of a SONOS device in the excess electron state, showing retention loss mechanisms: trap-to-band tunneling (TB), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE) and Poole–Frenkel emission (PF).....	29
Fig 2-10	Endurance requirement as a function of memory capacity.....	29
Fig 2-11	Threshold voltage window closure as a function of program/erase cycles on a single cell.....	30
Fig 2-12	Anomalous SILC modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase.....	30
<b>Chapter 3</b>		
Fig 3-1	Schematics of the experimental procedures for different ISSG temperature.....	40
Fig 3-2	(a) The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 850°C.....	41
Fig 3-3	(a) The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 950°C.....	42
Fig 3-4	(a) The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 1050°C.....	43

Fig 3-5	(a) The retention and (b) the endurance characteristics of 850°C.....	44
Fig 3-6	(a) The retention and (b) the endurance characteristics of 950°C.....	45
Fig 3-7	(a) The retention and (b) the endurance characteristics of 1050°C.....	46
Fig 3-8	(a) The W 4f XPS spectra and (b) Si 2p XPS spectra for 850°C, 950°C, and 1050°C.....	47
Fig 3-9	Schematics of the experimental procedures for different oxidation time.....	48
Fig 3-10	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of oxidation time 30s.....	49
Fig 3-11	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of oxidation time 60s.....	50
Fig 3-12	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of oxidation time 90s.....	51
Fig 3-13	(a) The retention and (b) the endurance characteristics of oxidation time 30s.....	52
Fig 3-14	(a) The retention and (b) the endurance characteristics of oxidation time 60s.....	53
Fig 3-15	(a) The retention and (b) the endurance characteristics of oxidation time 90s.....	54
Fig 3-16	(a) The W 4f XPS spectra and (b) Si 2p XPS spectra for oxidation time 30s, 60s, and 90s.....	55

## Chapter 4

Fig 4-1	Schematics of the experimental procedures for RTO and ISSG Tox fabrication.....	62
---------	--	----



Fig 4-2	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of RTO tunneling oxide.....	63
Fig 4-3	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of ISSG tunneling oxide.....	64
Fig 4-4	The comparison of current density-gate voltage hysteresis between RTO and ISSG tunneling oxide.....	65
Fig 4-5	(a) The retention and (b) the endurance characteristics of RTO tunneling oxide.....	66
Fig 4-6	(a) The retention and (b) the endurance characteristics of ISSG tunneling oxide.....	67
Fig 4-7	The schematics of the experimental procedures for oxidizing trapping layer by RTO and ISSG.....	68
Fig 4-8	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of RTO method .....	69
Fig 4-9	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of ISSG method.....	70
Fig 4-10	(a) The retention and (b) the endurance characteristics of RTO method.....	71
Fig 4-11	(a) The retention and (b) the endurance characteristics of ISSG method.....	72
Fig 4-12	(a) The W 4f XPS spectra for RTO method and (b) for ISSG method.....	73
Fig 4-13	(a) The Si 2p XPS spectra for RTO method and (b) for ISSG method.....	74

## Chapter 5

Fig 5-1	The schematics of the experimental procedures for the H <sub>2</sub> content 0, 2, 5,
---------	---

	10, 20, 33%.....	79
Fig 5-2	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 0% H <sub>2</sub> content.....	80
Fig 5-3	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 2% H <sub>2</sub> content.....	81
Fig 5-4	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 5% H <sub>2</sub> content.....	82
Fig 5-5	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 10% H <sub>2</sub> content.....	83
Fig 5-6	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 20% H <sub>2</sub> content.....	84
Fig 5-7	(a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 33% H <sub>2</sub> content.....	85
Fig 5-8	(a) The retention and (b) the endurance characteristics of 0% H <sub>2</sub> content.....	86
Fig 5-9	(a) The retention and (b) the endurance characteristics of 2% H <sub>2</sub> content.....	87
Fig 5-10	(a) The retention and (b) the endurance characteristics of 5% H <sub>2</sub> content.....	88
Fig 5-11	(a) The W 4f XPS spectra and (b) Si 2p XPS spectra for 0,2, 5% H <sub>2</sub> content.....	89