Chapter 1

Introduction

1.1 General Background

Today, flash memory has wide applications. It can be classified into two major markets: code storage application and data storage application. NOR type flash memory [1.1] is most suitable for code storage application, such as cellular phones, PC bios, and DVD player. NAND type flash memory [1.2] has been targeted at data storage market, such as PDA, memory cards, MP3 audio players, digital cameras, and USB flash personal disc. These products are based on nonvolatile memory. It can retain the information when the power supply is cut off. Flash memory has exhibits other advantages, such as the ability to be electrically programmed and fast simultaneous block electrical erasure, small cell size for high chip density, and good flexibility [1.3-1.4]. In addition, the flash memory fabrication process is compatible with the current CMOS process and is a suitable solution for embedded memory applications. Therefore, flash memory has replaced most of EPROMs (Erasable Programmable Read Only Memory) and EEPROMs (Electrically Erasable Programmable Read Only Memory). Since flash memory possesses these key advantages, it has become the mainstream nonvolatile memory device nowadays.

In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs [1.5]. The standard conventional floating-gate device structure is shown in Fig. 1-1. The structure is basic on a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with a modified stacking gate. The FG acts as a charge storage electrode. Charges injected into the FG

were retained there, resulting in a different threshold voltage for nonvolatile memory application.

Recently, nonvolatile memory devices are moving toward high density memory array, low cost, low power consumption, high-speed operation, and good reliability. Although conventional flash memory does not require refreshing and thus consumes less power and achieves much higher array density with a stacked floating gate structure. However, floating-gate flash memory is much slower to operation and has poor endurance. In order to improve the write/erase speed of a floating-gate device, the thickness of the tunnel oxide must be reduced. But conventional FG memory devices have limited potential for aggressive scaling of the tunnel oxide thickness. The tunnel oxide must be thin enough to allow quick and efficient charge transport to and from FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to guarantee the data integrity for 10 years. For faster operation speed, thin tunnel oxide is desirable. However, it is desirable to increase the thickness of tunnel oxide for better isolation and reliability. So there is a trade-off between speed and reliability for the optimum tunnel oxide thickness. Currently, commercial flash memory devices use tunnel oxide thicker about 8-11 nm, which results in high programming voltage and slow programming speed [1.6].

To alleviate the tunnel oxide design trade-off for floating-gate memory devices, memory-cell structures employing discrete traps as charge storage media have been proposed. In the conventional floating gate flash memory, if there is one defect created in the tunnel oxide, all the charges stored on the floating-gate will leak back to the channel or the source/drain through the weak spots. Unlike conventional continuous floating gate, charges stored in discrete nodes cannot easily redistribute amongst themselves. Therefore, only a relatively small number of nodes near the

oxide defects will be affected. Local charge storage in discrete nodes enables more aggressive scaling of the tunnel oxide by relieving the total charge loss concern. There are two promising candidates, SONOS [1.7-1.9] and nanocrystal nonvolatile memory devices [1.10-1.12], that have been demonstrated to lead to an improvement in retention time compared with conventional floating gate memory. Hence the tunnel oxide thickness can be reduced to allow faster programming and lower voltage operation.

1.1.1SONOS Nonvolatile Memory Devices

The first nitride-base devices is metal-gate nitride device MNOS (Metal/Nitride/Oxide/Silicon) which was reported in 1967 by Wegener et al [1.13]. However, it is well known that silicon nitride film contains many carrier traps which cause threshold voltage shift. Then the silicon nitride trap-based devices are extensively studied for charge storage device application in the early 70s. Fig. 1-2 illustrates the progression of device cross section, which has led to the present SONOS device structure. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30V. In the late 1970s and early 1980s, scaling moved to n-channel SNOS devices with write/erase voltages of 14-18V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12V. The advantages of the ONO triple dielectric structure are: (1) lower programming voltage since the blocking action of the top oxide removes any limitation on the reduction of the nitride thickness; (2) charge injection from and to the gate electrode is minimized for both gate polarities, particularly for hole injection; (3) improved memory retention since there is minimal loss of charge to the gate electrode.

The SONOS (poly-Silicon-Oxide-Nitride-Oxide-Silicon) memory devices, as

shown in Fig. 1-3, have attracted a lot of attention due to its advantages over the traditional floating-gate flash device. These include reduced process complexity, high speed operation, lower voltage operation, improved cycling endurance, and elimination of drain-induced turn-on [1.14-1.16]. The main difference between floating-gate and SONOS structure is the method of charge storage. The charge storage media in the floating-gate structure is the conducting poly-silicon floating-gate electrode. In the SONOS memory structure, charges are stored in the physical discrete traps of silicon nitride dielectric. A typical trap has a density of the order 10^{18}-$10^{19}cm^{-3}$ according to Yang et al [1.17] and stores both electrons and holes injected from the channel. The charges cannot move freely between the discrete trap locations, hence the SONOS memory device is very robust against the defects inside the tunnel oxide and has good endurance.

The SONOS memory devices still face challenge in the future for high density nonvolatile memory application, which requires low voltage (<5V), low power consumption, long-term retention, and superior endurance. Various approaches have been proposed for improving the SONOS performance and reliability. Chen et al. demonstrated a Si_3N_4 bandgap engineering (BE) control method for better endurance and retention. A nitride with varied relative Si/N ratio throughout the film has increased the charge-trapping efficiency significantly [1.18]. Tan et al. showed that over-erase phenomenon in SONOS memory structures can be minimized by replacing silicon nitride with HfO_2 as the charge storage layer. The charge retention and endurance performance is improved by the addition of 10% Al_2O_3 in HfO_2 to form HfAlO, while maintaining the over-erase resistance of HfO_2 [1.19]. She et al. demonstrates that high-quality nitride is applied as the tunnel dielectric for a SONOS-type memory device. Compared to control devices with SiO2 tunnel dielectric, faster programming speed and better retention time are achieved with low

programming voltage [1.20]. Lee et al. presents a device structure of SiO_2/SiN/Al_2O_3 (SANOS) with TaN metal gate. It is demonstrated that the use of TaN metal gate blocks electron current through Al_2O_3 layer more efficiently than a conventional poly-silicon gate, resulting in faster program/erase speed and significant decrease of the saturation level of the erase V_T [1.21].

Chen et al. studies a polycrystalline silicon thin-film transistor (poly-Si TFT) with oxide/nitride/oxide (ONO) stack gate dielectrics and multiple nanowire channels for the applications of both nonvolatile silicon-oxide-nitride-oxide-silicon (SONOS) memory and switch transistor [1.22]. The proposed NW SONOS-TFT exhibits superior memory device characteristics with high program/erase efficiency and stable retention characteristics at high temperature. Such a SONOS-TFT is thereby highly promising for application in the future system-on-panel display applications.

New device structures are also indispensable in making flash memory more scalable. Since SONOS flash memory offers a thinner gate stack than floating gate flash memory, and a FinFET structure controls the short channel effect much better than a bulk structure. It has been demonstrated that the FinFET SONOS flash memory devices with a much smaller cell size can provide both excellent performance and reliability. Therefore, FinFET SONOS memory has potential to become the candidate for the next generation flash memory [1.23-1.24].

1.1.2 Nanocrystal Nonvolatile Memory Devices

Nanostructure nonvolatile memories are first introduced in the early 1990s. IBM researchers first proposed flash memory with a granular floating gate made out of silicon nanocrystals [1.25]. Fig. 1-4 illustrates conventional nanocrystal nonvolatile memory (NVM) device structures. It is observed that the nanocrystals are separated from each other within the gate dielectric. The term “nanocrystal” refers to a crystalline structure with a nanoscale dimension and its electronic properties seem

more similar to an atom or molecule rather than the bulk crystal. For a nanocrystal NVM device, the charge storage media is in the form of mutually isolated nanocrystals instead of the continuous poly-silicon layer. The limited size and capacitance of nanocrystals limit the numbers of stored electron; collectively the stored charges screen the gate charge and control the channel conductivity of the memory transistor.

Nanocrystal-based NVM devices have recently received much attention due to their potential to overcome the limitations of conventional polysilicon-based flash memory. Using nanocrystals as charge storage media offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing non-volatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results from the local charge storage in discrete nodes, which makes the storage more fault-tolerant and immune to the leakage caused by localized oxide defects. Further, the lateral charge migration effect between nanocrystals can be suppressed by the strongly isolation of surrounded dielectric. There are other important advantages though. First, nanocrystal memories use a more simplified fabrication process as compared to conventional stacked-gate FG NVM's by avoiding the fabrication complications and costs of a dual-poly process. Second, due to the absence of drain to FG coupling, nanocrystal memories suffer less from drain-induced-barrier-lowering (DIBL) and therefore have intrinsically better punch-through characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time [1.26]. Alternatively, it allows the use of shorter channel lengths and therefore smaller cell area. Finally, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the distributed nature of the

charge storage in the nanocrystal layer.

Research in this regime has focused on the development of fabrication processes and nanocrystal materials, and on the integration of nanocrystal-based storage layers in actual memory devices.

The fabrication of a nonvolatile memory cell requires a perfect control of four main parameters: (1) the tunnel oxide thickness, (2) the nanocrystal density, (3) the nanocrystal size, and (4) the control oxide thickness. An important consideration is the average size and aerial density of the nanocrystals. Larger-size nanocrystal array provides higher program/erase efficient due to small quantum confinement and coulomb blockade effects, and hence larger tunneling probability. However, it is desirable to reduce the nanocrystal size for better reliability (stress induced leakage during retention). So there is a trade-off between programming speed and reliability in selecting the nanocrystal size. A typical target is a density of at least $10^{12}cm^{-2}$, and requires nanocrystal size of 5nm and below. Moreover, good process control is needed with regards to such nanocrystal features as: planar nanocrystal layer; inter-crystal interaction (lateral isolation); and crystal doping (type and level). Finally, it is preferred that the fabrication process is simple and that it uses standard semiconductor equipment.

After the first proposal of a memory transistor using silicon nanocrystals as floating gates. In order to improve the data retention in NVM, double layer Si nanocrystals memory has been investigated [1.27]. It seems interesting to use Ge nanocrystals rather than Si nanocrystals because of its smaller band gap. Indeed King and Hu have recently demonstrated the superior memory properties of Ge based nanocrystal memories over those based on Si [1.28]. Recently, germanium/silicon (Ge/Si) nanocrystals have been reported to possess superior charge retention capability than Ge or Si nanocrystals. This is due to the fact that Ge has a smaller

band gap than Si and thus by introducing a Si interface around the Ge nanocrystal, it would create an additional barrier height at the Ge/Si interface which makes it harder for electrons to leak out of the nanocrystal [1.29-1.30]. However, semiconductor nanocrystal memory may not be the ultimate solution to nonvolatile memory scaling, although it still attracts a lot of attention now.

In optimizing nanocrystal NVM devices, the ideal goal is to achieve the fast write/erase of DRAM and the long retention time of Flash memories simultaneously. For this purpose we need to create an asymmetry in charge transport through the gate dielectric to maximize the IG, Write/Erase/ IG, Retention ratio. One approach for achieving this goal is to engineer the depth of the potential well at the storage nodes, thus creating a small barrier for writing and a large barrier for retention between the substrate and the storage nodes. This can be achieved if the storage nodes are made of metal nanocrystals by engineering the metal work function. The major advantages of metal nanocrystals over semiconductor nanocrystals include higher density of states around the Fermi level, scalability for the nanocrystal size, a wide range of available work functions, and smaller energy perturbation due to carrier confinement [1.31]. In addition, an electrostatic modeling from both analytical formulation and numerical simulation is demonstrated that the metal nanocrystals will significantly enhance the electric field between the nanocrystal and the sensing channel set up by the control gate bias, and hence can achieve much higher efficiency in low-voltage P/E [1.32].

Toward better NVM device performance and reliability, numerous attempts have been made using metal nanocrystals. Liu et al. reported the growth of Au, Pt, and Ag nanocrystals on SiO_2 using an e-beam deposition method [1.31]. Lee et al. proposed a NVM structure using the Ni nanocrystals and high-k dielectrics [1.33]. Chen et al. present the stacked Ni silicide nanocrystal memory was fabricated by sputtering a comix target followed by a low temperature RTO process [1.34]. W nanocrystals on

atomic-layer-deposited HfAlO/Al_2O_3 tunnel oxide were presented for application in a memory device [1.35]. Using W nanocrystal double layers embedded in HfAlO to enhancement of memory window was demonstrated from the short channel devices down to 100nm [1.36]. Tang et al demonstrate that a chaperonin protein lattice can be used as a template to assemble PbSe and Co nanocrystal arrays for Flash memory fabrication. This provides a new approach to achieve a high density and good distribution uniformity nanocrystal array [1.37].

In the future, the primary drivers behind nanocrystal memories are the potential to scale the tunnel oxide thickness, resulting in lower operating voltages, and the simplicity of a single poly-silicon process. But there are still challenges await nanocrystal memories in the long road to commercialization. Nanocrystal memories have yet to deliver on most of their promises. In reality, part of the voltage gain is offset because of the poor control gate coupling. For fabrication processes, it is hard to control the uniformity of the nanocrystal size and their physical locations in the channel. It is not a surprise that nanocrystal memories exhibit large device-to-device variation. Moreover, it has yet to be demonstrated that both the nominal and the statistical retention behavior are sufficient to meet true non-volatility requirements. Although single-dot memories have been demonstrated [1.38-1.39], but a more fundamental understanding of the scaling limits of nanocrystal memories is necessary, concentrating especially on the aspect of controlling channel conductance when relying on only a few discrete charge centers [1.40]. Finally, in order for that to happen, their claimed benefits will need to be more unambiguously substantiated, and a more appealing bundle of memory features will have to be demonstrated.

1-2. Organization of the dissertation

This dissertation is divided into six chapters. The contents in each chapter are described as follows：

In chapter 1, the nanocrystal in non-volatile memory applications of the research background will be introduced in this chapter.

In chapter 2, the non-volatile memory of the principle

In chapter 3, formation of W-NCs Nonvolatile Memory based on ISSG and the study for the effects of temperature and oxidation time on W-NCs formation

In chapter 4, comparison of ISSG oxidation method with RTO for W-NCs Nonvolatile Memory

In chapter 5, The effect of H_2 content in ISSG system

In chapter 6, the conclusions

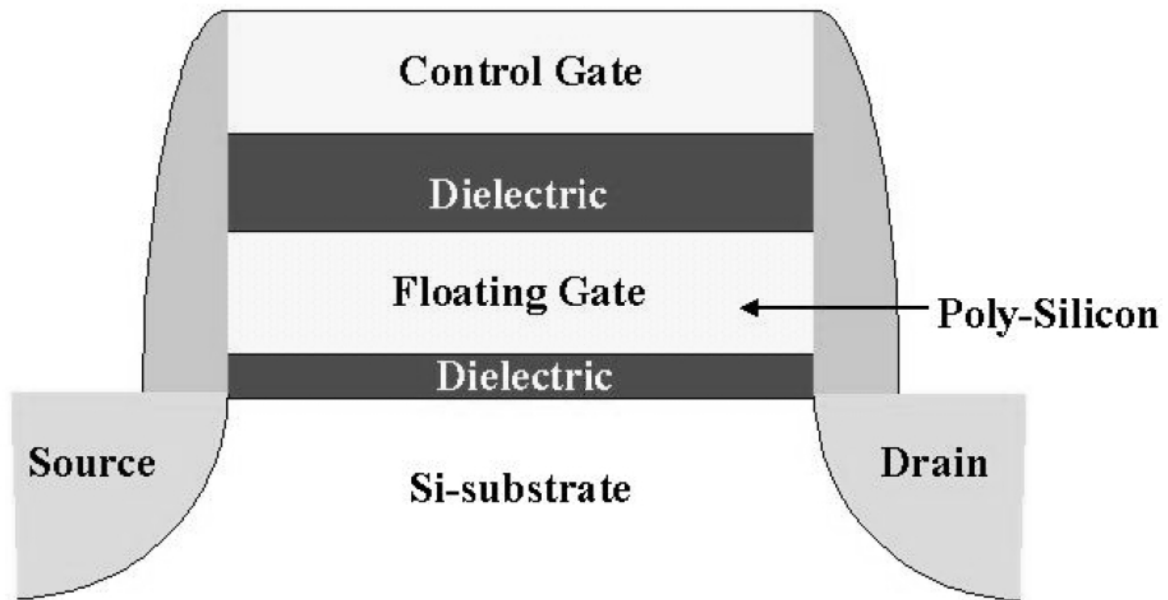


Figure 1-1 The structure of the conventional floating-gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.

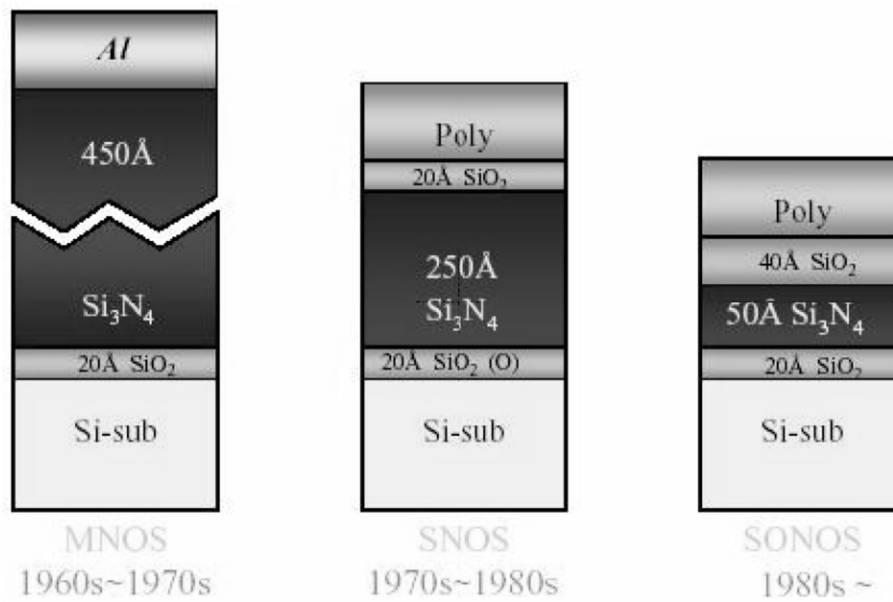


Figure 1-2 The development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

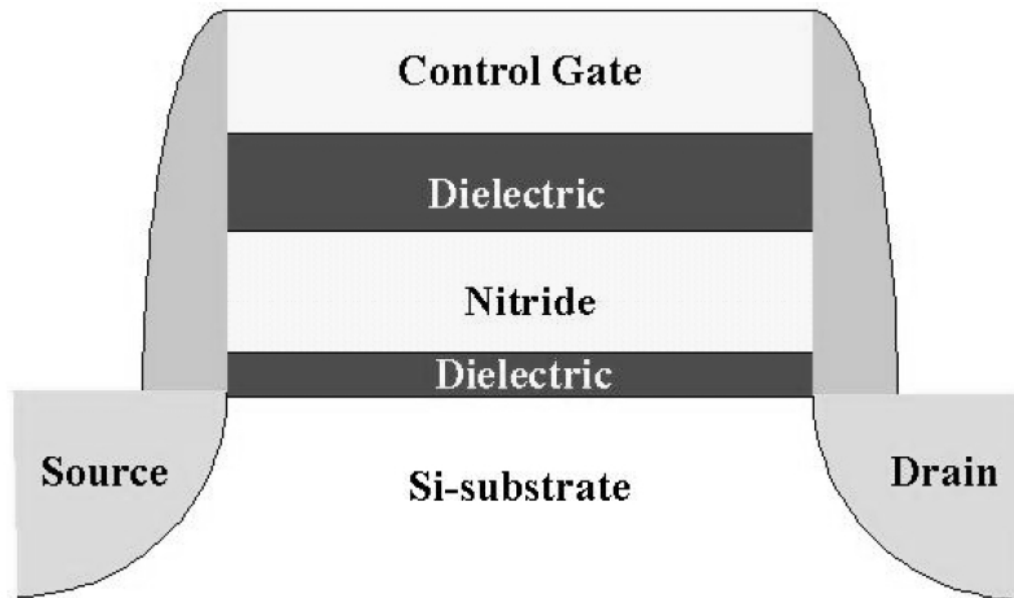
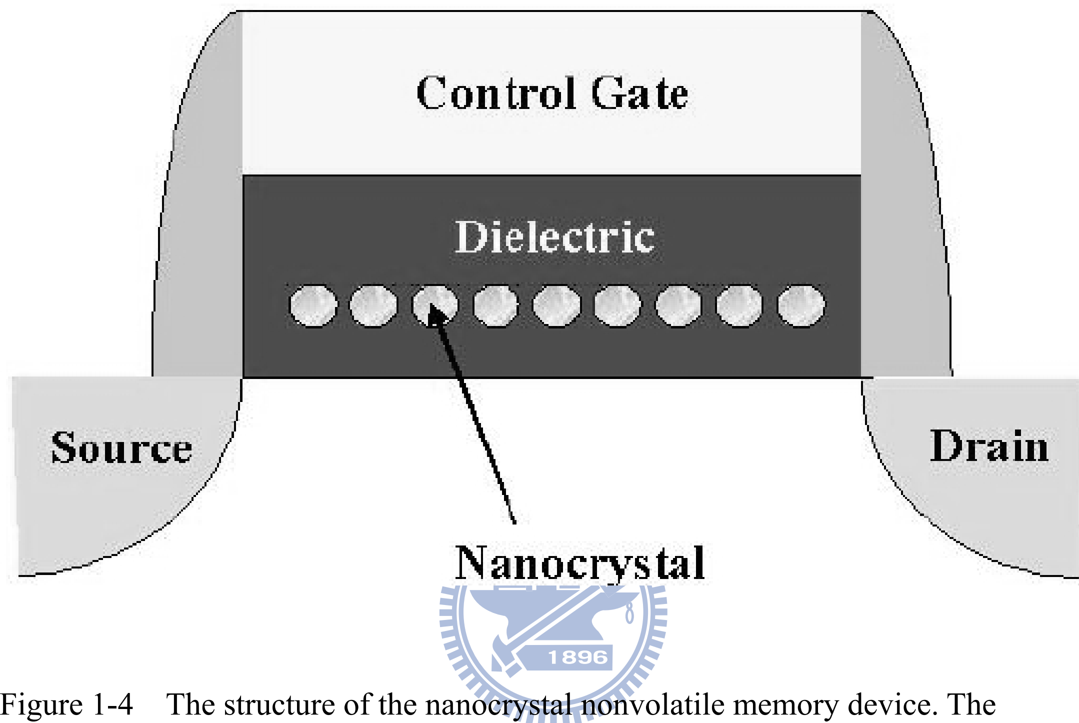


Figure 1-3 The structure of the SONOS nonvolatile memory device. The nitride layer is used as the charge trapping media**.**

ES



1896

Figure 1-4 The structure of the nanocrystal nonvolatile memory device. The semiconductor nanocrystals or metal nanocrystals are used as the charge storage element instead of the continuous poly-Si floating gate.

chapter 2

Basic principle of nonvolatile memory

2-1. Program / Erase mechanisms

Most of operations on novel nonvolatile memories, such as nanocrystal and SONOS memories are base on the concept of Flash memory. If a datum has to be stored in a bit of the memory, there are different procedures. The threshold voltage shift of a Flash transistor can be written as [2.1-2.2]:

$$\Delta V_T = -\frac{\overline{Q}}{C_{FC}}$$

where $\overline{Q}$ is the charge weighted with respect to its position in the gate oxide, and the capacitances between the floating gate (FG) and control gate. The threshold voltage of the memory cell can be altered by changing the amount of charge present between the gate and the channel, corresponding to the two states of the memory cell, i.e., the binary values ("1" and "0") of the stored bit. Fig. 2.1 shows the threshold voltage shift between two states in a Flash memory. To a nonvolatile memory, it can be "written" into either state "1" or "0" by either "programming" or "erasing" methods, which are decided by the definition of memory cell itself. There are many solutions to achieve "programming" or "erasing". In general, hot carrier electron injection, tunneling and band to band tunneling are three kinds of common operation mechanism employed in novel nonvolatile memories. The three mechanisms will lead difference characteristics for nonvolatile memories.

2-1-1. Hot-Electron injection (HEI)

The physical mechanism of HEI is relatively simple to understand qualitatively.

An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100 kV/cm [2.3]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges (channel hot electron, CHE). Fig. 2.2 shows schematic representation of HEI MOSFET and the energy-distribution function with different fields. In the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection rarely is employed in nonvolatile memory operation.

2-1-2. Tunneling injection

Tunneling mechanisms are demonstrated in quantum mechanics. Basically, tunneling injection must to have available states on the other side of the barrier for the carriers to tunnel into. If we assume elastic tunneling, this is a reasonable assumption due to the thin oxide thickness involved. Namely, no energy loss during tunneling processes. Tunneling through the oxide can be attributed to different carrier-injection mechanisms. Which process applies depends on the oxide thickness and the applied gate field or voltage. Direct tunneling (DT), Fowler-Nordheim tunneling (FN), modified Fowler-Nordheim tunneling (MFN) and trap assistant tunneling (TAT) are the main programming mechanisms employed in memory [2.4-2.7] as shown in Fig.2.3.

1. **Direct tunneling**

For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [2.8]. As a result, F-N tunneling cannot serve as

an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. The direct tunneling is employed in nanocrystal memories instead. Fig.2.4 shows a simulated electron tunneling current from metal to Si substrate as a function of electric field in oxide. The metal used in the simulation is Au and the oxide thickness is set to be 2 nm.

In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height, two to four orders of magnitude reduction in leakage current can still be achieved if large work function metals, such as Au or Pt [1.14]. Fig.2.5 shows the transmission coefficients for electrons tunneling through a rectangular oxide barrier, calculated by one-dimensional Wentzel–Kramers–Brillouin (WKB) approximation.

2. Fowler-Nordheim tunneling

The Fowler–Nordheim (FN) tunneling mechanism occurs when applying a strong electric field (in the range of 8–10 MV/cm) across a thin oxide. In these conditions, the energy band diagram of the oxide region is very steep. Therefore, there is a high probability of electrons' passing through the energy barrier itself. Using a free-electron gas model for the metal and the WKB approximation for the tunneling probability [2.9], one obtains the following expression for current density [2.10]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp\left[\frac{-4(2m_{OX}^*)^{1/2}\Phi_B^{3/2}}{3\hbar qF}\right]$$

Where Φ_B is the barrier height, m_{OX}^* is the effective mass of the electron in the forbidden gap of the dielectric, h is the Planck's constant, q is the electronic charge, and F is the electric field through the oxide. Fig. 2.6 [2.11] shows log J versus F. In fact, in Fig. 2.7, it is evident that with a field of 7 MV/cm, the current density is about 10^{-8} A/cm, while with a field of 10 MV/cm it is about 10^{-1} A/cm. There is a variation

of about seven orders of magnitude in tunnel current. A slightly greater field range allows a difference of 12 orders of magnitude. However, the exponential dependence of tunnel current on the oxide-electric field causes some critical problems of process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states.

3. Modified Fowler–Nordheim tunneling

Modified Fowler–Nordheim tunneling (MFN) is similar to the tradition FN tunneling mechanism, yet the carriers enter the nitride at a distance further from the tunnel oxide-nitride interface. MFN mechanism is frequently observed in SONOS memories. The SONOS memory is designed for low-voltage operation (<10 V, depending on the Equivalent oxide thickness), a relatively weak electrical field couldn't inject charges by DT or FN mechanism.

4. Trap assistant tunneling

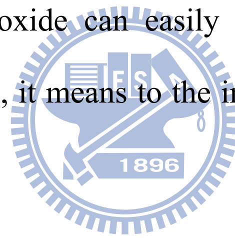
The charge storage mediums with many traps may cause another tunneling mechanism. For example, the charges tunnel through a thin oxide and arrive to the traps of nitride layer at very low electrical field in SONOS systems. During trap assisted injection the traps are emptied with a smaller time constant then they are filled. The charge carriers are thus injected at the same distance into the nitride as for MFN injection. Because of the sufficient injection current, trap assistant tunneling may influence in retention [2.12].

2-1-3. Band to band tunneling

Band to band tunneling application to nonvolatile memory was first proposed in 1989. I. C. Chen and et al. demonstrated a high injection efficiency (~1%) method to programming EPROM devices [2.13]. Fig. 2.7 shows the energy-band diagram during the band to band tunneling induced hot electron (BBHE) injection. When

band-bending is higher than the energy gap of the semiconductor, the tunneling electron (labeled A) from the valence band to the conduction band becomes significant. The electrons are accelerated by a lateral electric field toward the channel region and some of the electrons with sufficient energy can surmount the potential barrier of SiO_2 like hot electron injection [2.13-2.15].

Fig. 2.8 shows device-simulation of the BBHE injection operation. As shown in this figure, the electric field in the tunnel oxide (E_{OX}) at the hot electron injection point is a low 7.5MV/cm at the bias condition of Vd=-6V, Vg=6V (Ig=2nA/cell) [2.16]. It is reduction of the vertical electric field strength in the tunnel oxide at the injection point since the E_{OX} exceeding 13MV/cm is necessary to obtain the same Ig in the case of the edge-FN in the N-channel cell. Due to the small oxide field, the electron influence through the oxide can easily reach hundreds of coulombs per square centimeter without failure, it means to the improvement reliability of memory cells.



2-2. Nonvolatile memory reliability

For a nonvolatile memory, the important to concern is distinguishing the state in cell. However, in many times operation and charges storage for a long term, the state is not obvious with charges loss. Endurance and retention experiments are performed to investigate Flash-cell reliability.

2-2-1 Retention Time

In any nonvolatile memory technology, it is essential to retain data for over ten years. This means the loss of charge stored in the storage medium must be as minimal as possible. For example, in modern Flash cells, FG capacitance is approximately 1 fF. A loss of only 1 fC can cause a 1V threshold voltage shift. If we consider the

constraints on data retention in ten years, this means that a loss of less than five electrons per day can be tolerated [2.1].

Possible causes of charge loss are:

1) by tunneling or thermionic emission mechanisms;

2) defects in the tunnel oxide;

3) detrapping of charge from insulating layers surrounding the storage medium.

First, several discharge mechanisms may be responsible for time and temperature dependent retention behavior of nonvolatile memory devices. Fig.2.9 shows a bandgap diagram of a SONOS device in the excess electron state [2.7], illustrating trap-to-band tunneling, trap-to-trap tunneling, and band-to-trap tunneling, thermal excitation and Poole-Frenkel emission retention loss mechanisms. These mechanisms may be classified into two categories. The first category contains tunneling processes that are not temperature sensitive (trap-to band tunneling, trap-to-trap tunneling, and band-to-trap tunneling). The second category contains those mechanisms that are temperature dependent. Trapped electrons may redistribute vertically inside the nitride by Poole–Frenkel emission, which will give rise to a shift in the threshold voltage. Moreover, at elevated temperatures, trapped electrons can also be thermally excited out of the nitride traps and into the conduction band of the nitride (thermal excitation), and drift toward the tunnel oxide, followed by a subsequent tunneling to the silicon substrate.

Secondly, the generation of defects in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter to the physical mechanisms that are used to program and erase the cell.

Electrons can be trapped in the insulating layers surrounding the storage medium during wafer processing, as a result of the so-called plasma damage, or even during the UV exposure normally used to bring the cell in a well-defined state at the end of

the process. The electrons can subsequently de-trap with time, especially at high temperature. The charge variation results in a variation of the storage medium potential and thus in cell decrease [2.17].

The retention capability of Flash memories has to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

2-2-2. Endurance

Endurance is the number of erase/write operations that the memory will complete and continue to operate as specified in the data sheet. Generally speaking, Flash products are specified for 10^6 erase/program cycles. Nevertheless, the endurance requirement may be relaxed with the increase of memory density for the other using. Fig.2.10 shows the Endurance requirement of NAND Flash memories [2.18]. The endurance requirement was relaxed to 100K cycles for 256 MB density. In the higher density, a certain cell in a block has less possibility to be written and erased since the memory operation on the cell is repeated after using up the whole memory blocks. The endurance requirement is sufficient for the user to take 700 photos with a 1MB size every day for 10 years [2.18].

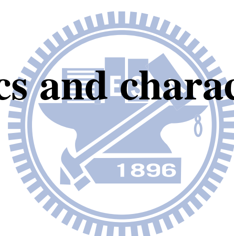
A typical result of an endurance test on a single cell is shown in Fig.2.11. As the experiment was performed applying constant pulses, the variations of program and erase threshold voltage levels are described as “program/erase threshold voltage window closure” and give a measure of the tunnel oxide aging [2.17 , 2.19].

In particular, the reduction of the programmed threshold with cycling is due to trap generation in the oxide and interface state generation at the drain side of the channel. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge. The initial lowering of the erase is due to a pile-up of positive charge which enhances tunneling

efficiency, while the long-term increase of the erase is due to a generation of negative traps.

Moreover, a high field stress on thin oxide is known to increase the current density at low electric field. The excess current component, which causes a significant deviation from the current–voltage curves from the theoretical F-N characteristics at low field, is known as stress-induced leakage current (SILC). SILC is clearly attributed by stress-induced oxide defects, which leads to a trap assisted tunneling (see Fig. 2.12). The main parameters controlling SILC are the stress field, the amount of charge injected during the stress, and the oxide thickness. For fixed stress conditions, the leakage current increases strongly with decreasing oxide thickness [2.21-2.23].

2-3. The material physics and characteristics for nanocrystal memory


1896

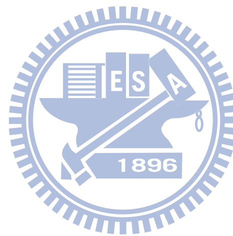
2-3-1. Quantum confinement

The quantum dot, is quasi-zero-dimensional nanoscaled material, and is composed by small amount atoms. The quantum confinement energy dependence on nanocrystal size has been researched both experimentally and theoretically according to the tight-binding model [2.23]. The quantum confinement effect becomes significant when the nanocrystal size shrinks to the nanometer range, which causes the conduction band in the nanocrystal to shift to higher energy compared with bulk material [2.24]. The discontinue energy level will be expected to impact the nanoelectronics.

2-3-2. Coulomb blockade

The stored electron charge will raise the nanocrystal potential energy and reduce

the electric field across the tunnel oxide, resulting in reduction of the tunneling current density during the write process. It is more dominant at low programming voltages (<3V). The Coulomb blockade effect can effectively inhibit the electron tunneling at low gate voltage and improve the flash memory array immunity to disturbance. However, the reduced Coulomb blockade effect can be achieved by employing large size nanocrystals for large tunneling current and fast programming speed are considered. The Coulomb blockade effect has a serious effect on the retention time. Large tendency for electrons stored in nanocrystals will tunnel back into the channel if the potential energy is high in retention mode



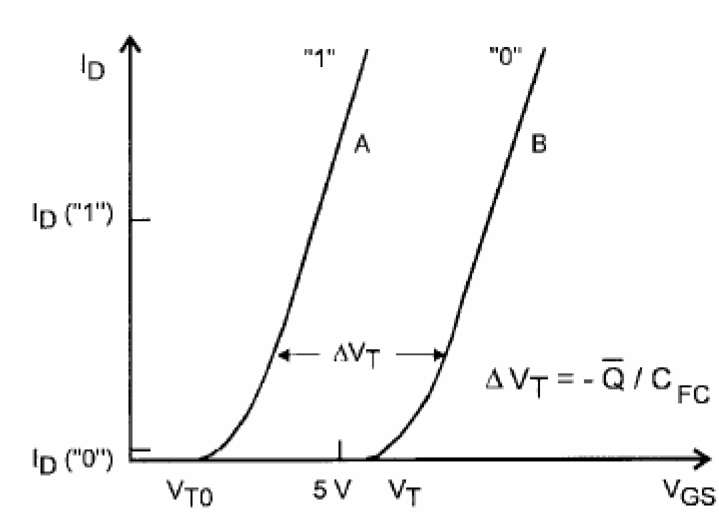
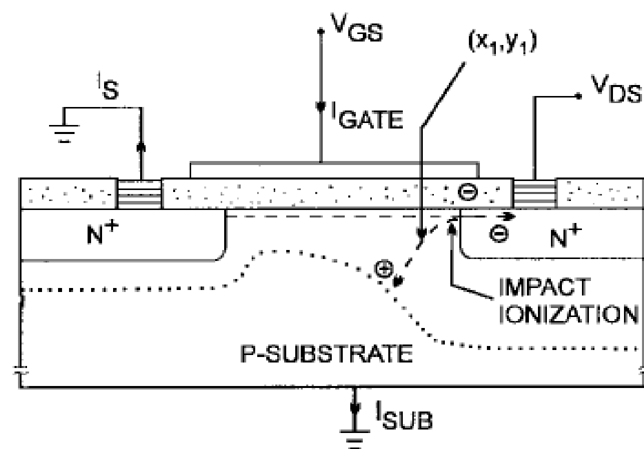


Fig. 2-1 I–V curves of an FG device when there is no charge stored in the FG (curve A) and when a negative charge $\overline{Q}$ is stored in the FG (curve B).



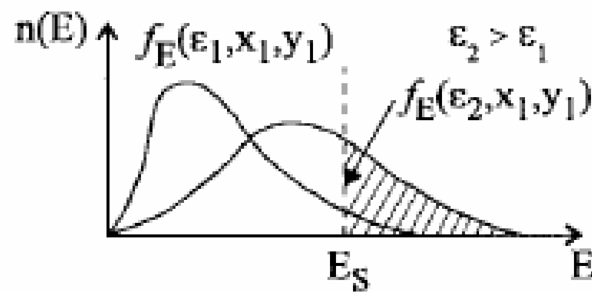


Fig. 2-2 Schematic cross section of MOSFET. The energy- distribution function at point X1; Y1 is also shown.

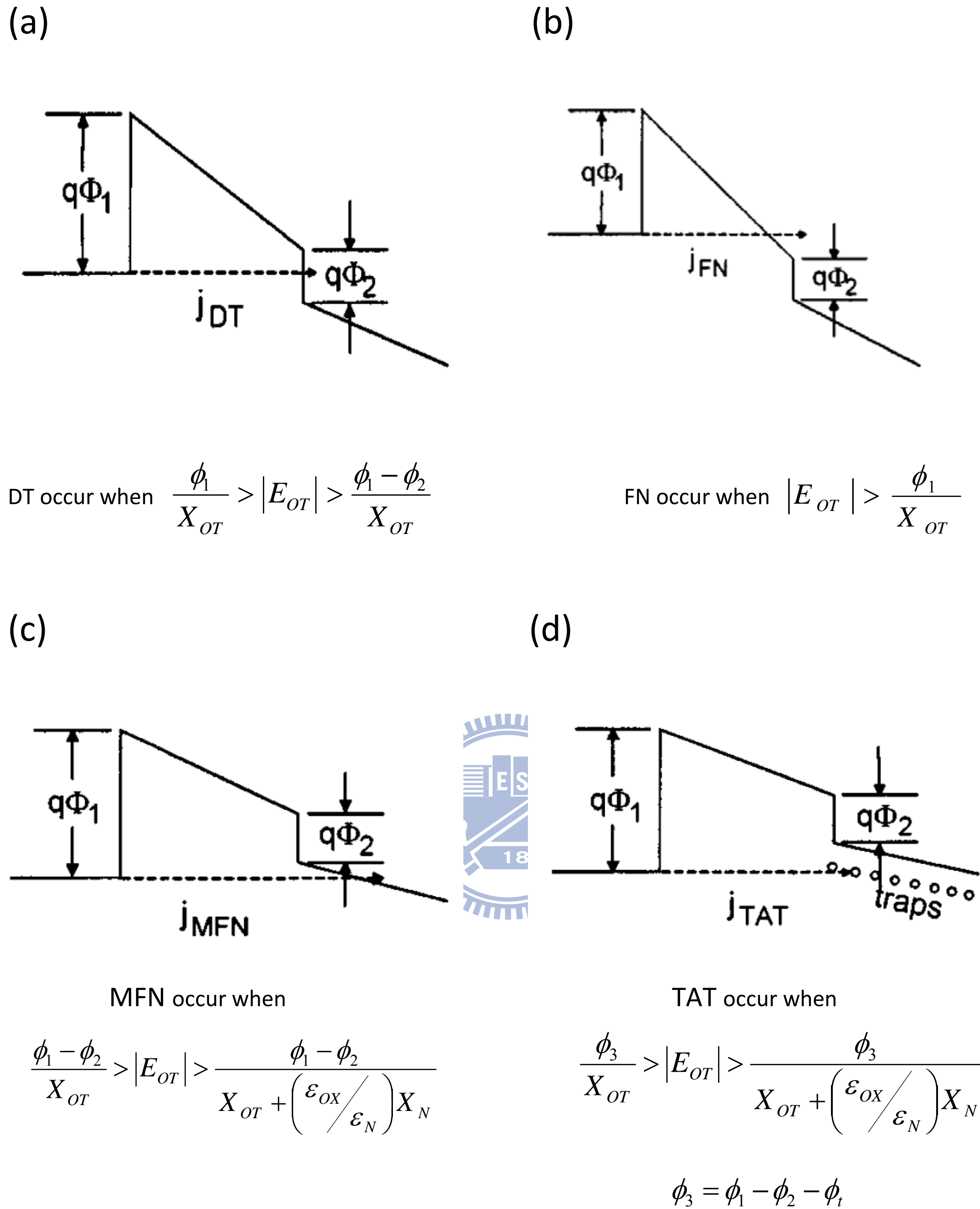


Fig.2-3 Fourth approaches to programming methods, described by Hu and White. (a) Direct tunneling (DT) (b) Fowler-Nordheim tunneling (FN) (c) modified Fowler-Nordheim tunneling (MFN) (d) trap assistant tunneling (TAT).

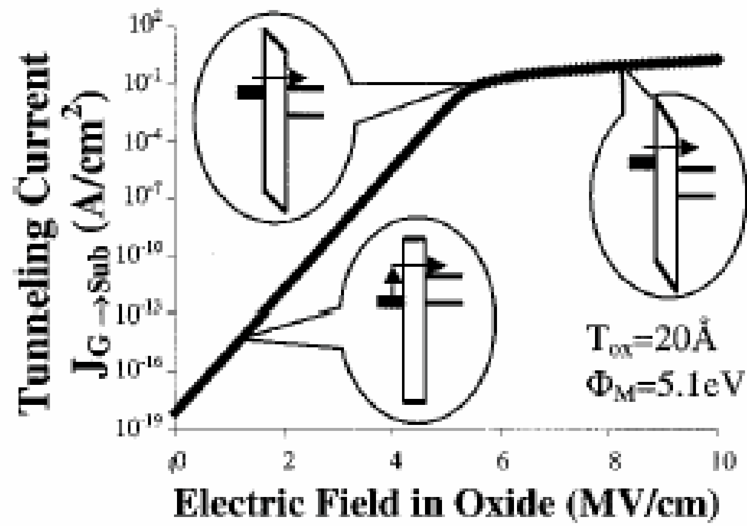


Fig. 2-4 Electron direct tunneling current from Au nanocrystals to Si substrate as a function of the electric field in tunnel oxide.

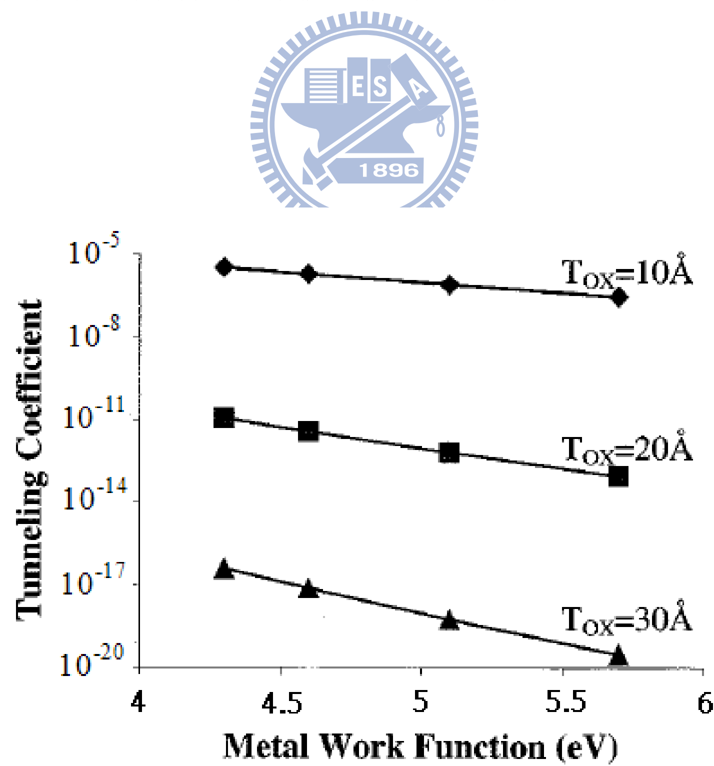


Fig. 2-5 Tunneling transmission coefficient through a rectangular SiO_2 barrier from metals with different work functions.

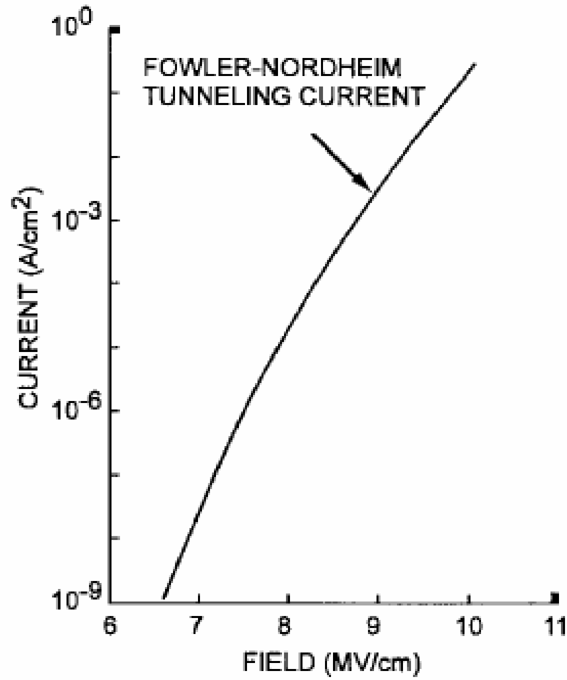


Fig. 2-6 It is evident that with a field of 7 MV/cm, the current density is about 10^{-8} A/cm, while with a field of 10 MV/cm it is about 10^{-1} A/cm . There is a variation of about seven orders of magnitude in tunnel current.

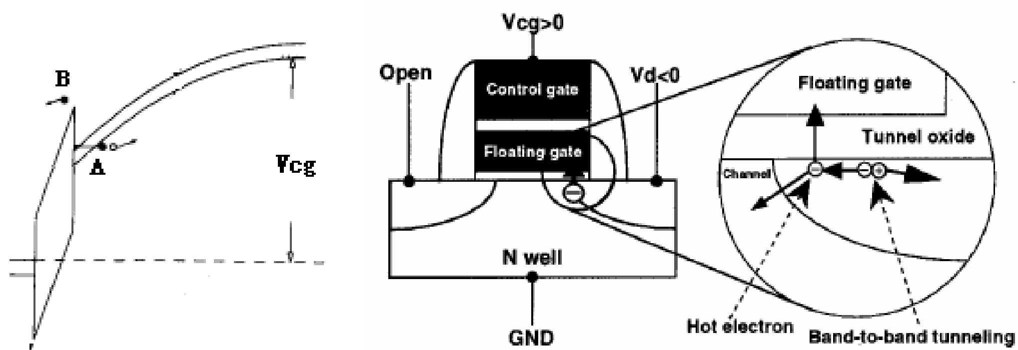


Fig. 2-7 Energy-band diagram for the proposed band to band induce hot electron injection mechanism and schematic illustration cross of the Flash memory with p-channel cell. Due to the positive bias to the control gate, holes are not injected into the tunnel oxide.

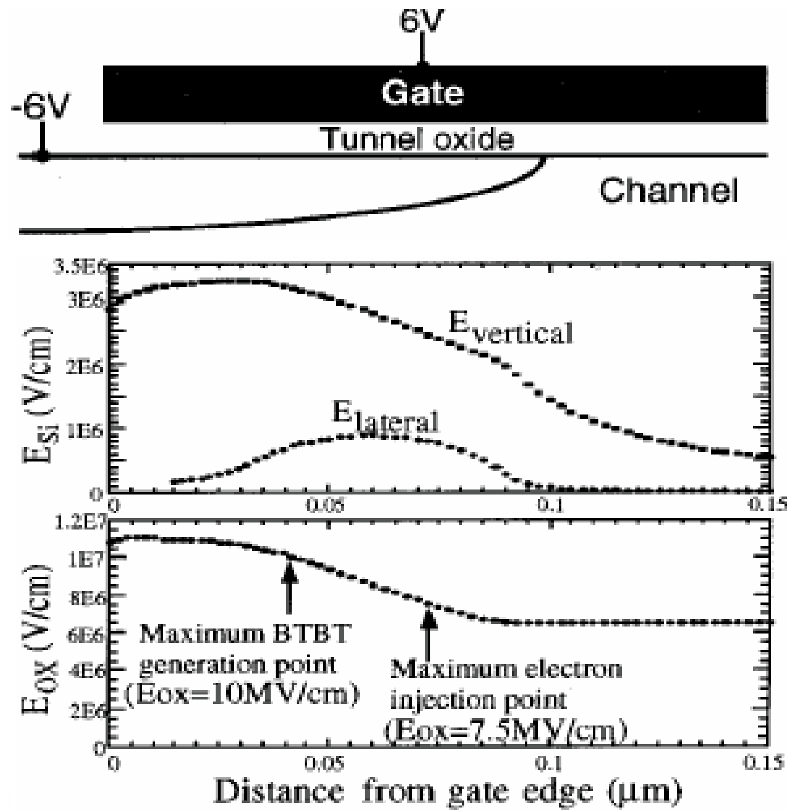


Fig. 2-8 Simulated the electron electric fields in Si substrate (Esi) and in the tunnel oxide (Eox) during BBHE injection in the P-channel cell. It should be noted that although Eox, at the maximum bnad to band tunneling (BTBT) generation point is 10MV/cm, Eox of the electron injection point is a low 7.5MV/cm.

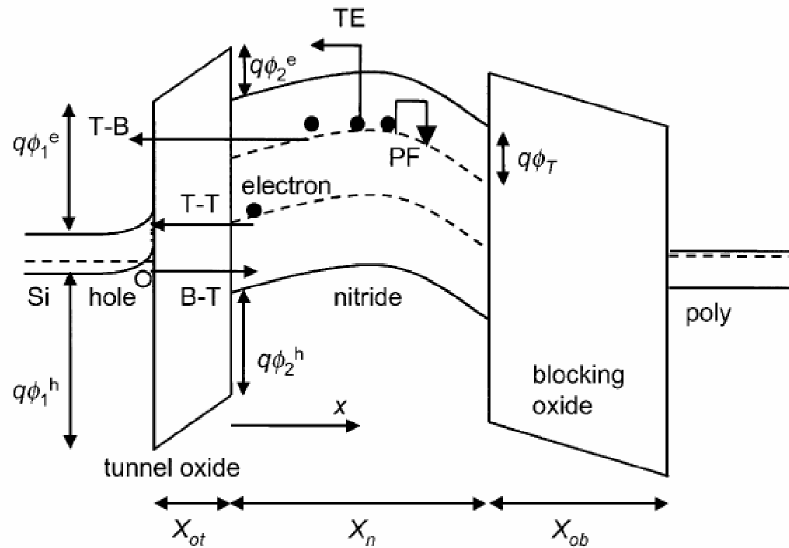


Fig. 2-9 Bandgap diagram of a SONOS device in the excess electron state, showing retention loss mechanisms: trap-to-band tunneling (TB), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE) and Poole–Frenkel emission (PF).

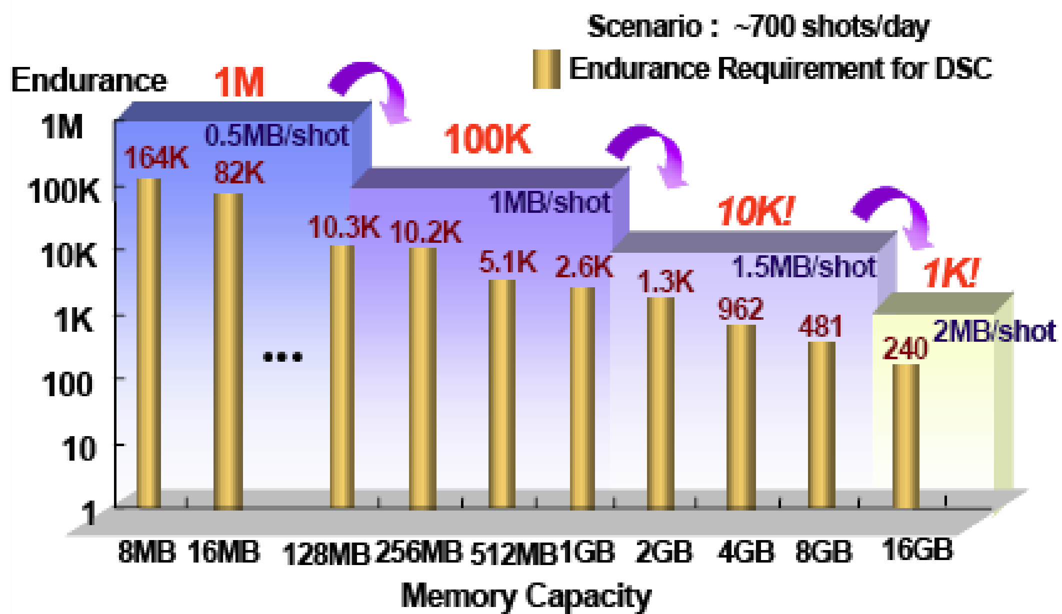


Fig. 2-10 Endurance requirement as a function of memory capacity.

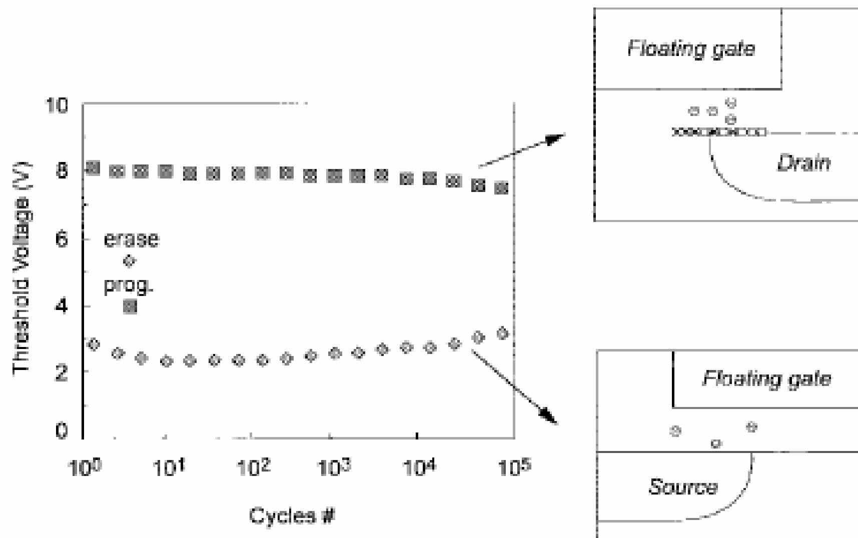
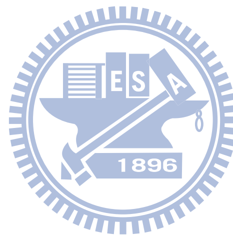


Fig. 2-11 Threshold voltage window closure as a function of program/erase cycles on a single cell.



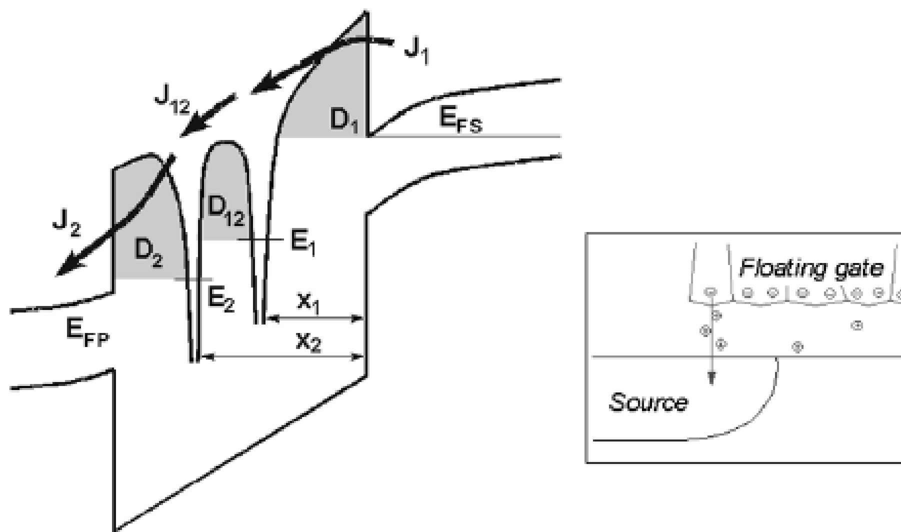


Fig. 2-12 Anomalous SILC modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase.

Chapter 3

Formation of W-NCs Nonvolatile Memory based on ISSG

3.1 Motivation

The continuous scaling of device structure for flash memory increases higher packing density and enhances device performance, Therefore, further scaling of gate dielectric thickness is an inevitable trend .However, the thinner tunnel oxide may cause the degradation of charge storage ability. Recently, the use of a floating gate composed of distributed nanocystals reduce the problems of charge loss encountered in conventional floating-gate memories (e.g.,SONOS, MONOS and SOHOS), so improving retention properties .

Nowadays, the novel nanocystal nonvolatile memory devices have been investigated widely [3.1], especially for metallic nanocystals memories. The major advantages of metal nanocystals over their semiconductor counterparts include higher density of states around the Fermi level, stronger coupling with the conduction channel, better size scalability, a wide range of available work functions , and smaller energy perturbation due to carrier confinement [3.2].

The quality of tunnel oxide is also an important issue for device reliability. It has been reported that intrinsic defects in the bulk oxide control the reliability of thick oxide whereas with the scaling down of memory devices, the thin oxide reliability is governed by the interface roughness and the structural defects within the transition layer near the Si/SiO_2 interface. Some methods that attain high quality thin oxide film by atomic oxygen generated using an ultraviolet ozone(UVO_3) oxidation process or active oxygen radicals utilizing an oxygen –remote-plasma process are presented, [3.3], [3.4]. In addition, more and more references have demonstrated that wet or steam oxide shows much better reliability property than dry or RTO oxide, [3.5], [3.6]. The reliability tests such as SILC, TBD, QBD indeed exhibit significantly improved properties for wet or steam oxide. The reasons why steam oxidation can provide excellent quality of thin oxide film are primary due to the minimized Si/SiO_2 interface roughness and reduced compressive stress within the strained structural transition layer[3.7], [3.8].

In this thesis, we choose tungsten material to form our metal nanocrystal memory. Because of its large work function(4.6eV), tungsten nanocrystals(W-NCS) can bring about deep quantum well which enhances better retention. Besides, tungsten has been proven to be compatible to Si-based complementary metal-oxide-semiconductor(CMOS) devices and applied in the form of contact plugs and bit lines [3.9]. Some methods have been developed recently for the preparation of tungsten nanocrystal nonvolatile memory. Such as, S. K. Samanta sputtered tungsten thin film, followed by RTA , to fabricate self-assembled tungsten nanocrystals memory [3.9], [3.10], T. C. Chang also deposite a tungsten-rich tungsten silicide layer,W_5Si_3. After capping an amorphous Si layer, the sample was dry oxidized at 900°C to form tungsten nanocrystals precipitated and embedded in silicon oxide.

From our study, we proposed a new method to form tungsten metal nanocrystal memory. According to the advantages of using steam oxidation process mentioned before, we decide to adopt in-situ-steam-generation (ISSG) method to oxidize tapping layer which was composed of tungsten silicide(WSi_2) and a-Si. Since ISSG has higher oxidation rate than that of conventional dry oxidation or RTO, tungsten silicide , the trapping layer, could be oxidized more completely. Also, the a-Si layer was used for adjusting the concentration of W atoms to avoid the formation of WO_3 after thermal oxidation. The exploitation of ISSG makes tungsten nanocrystals precipitate easily and its surrounding dielectric layer has less interface states. We expect the application of ISSG could ameliorate the electrical characteristics of tungsten nanocrystals nonvolatile memory.

In this chapter, we apply ISSG method to fabricate tunnel oxide and trapping layer. The subject of this chapter is to discuss the effect of ISSG oxidation temperature and time on forming tungsten nanocrystals. Here, here,we fixed the H_2 content of ISSG system.

3-2 The effect of ISSG temperature on W-NCs

3-2-1 Experimental Steps

Fig. 3-1 showed the schematic diagram of fabricating procedure, labeled as structure I. First, a single-crystal 8 inch (100) oriented p-type silicon wafer was chemically cleaned by standard RCA cleaning. Then, a 5-nm-thick thermal oxide was grown on p-type Si substrate by rapid thermal oxidation in an in situ steam generation system(ISSG) as a tunnel oxide. After growing tunnel oxide, we deposited a tungsten

silicide film(WSi_2) which has thickness of 4nm by low pressure chemical vapor deposition furnace(LPCVD).Subsequently, a 6-nm-thick amorphous silicon (a-Si) was also deposited by the same system. After finishing WSi2/a-Si double layer structure, the high temperature thermal oxidation was performed in the rapid thermal anneal system where both oxygen and hydrogen flow. This system is usually called in situ steam generation (ISSG) process. This procedure was executed to let WSi_2 precipitate tungsten nanocystals and form silicon oxide as its surrounding dielectric. We want to investigate the effects of different oxidation temperature on formation of tungsten nanocrystals. Thus, a thermal oxidation process was used by ISSG system for 850°C, 950°C, 1050°C, respectively. Afterward, a followed 50nm silicon oxide was deposited by PECVD system to form an enough thick control oxide. Finally, the Al gate electrode was deposited by the use of thermal coater and then patterned.

The electrical characteristics, such as capacitance-voltage (C-V), and current density-voltage (J-V) were measured by Keithley 4200 and HP4284 Precision LCR Meter with frequency of 100 kHz. The material analysis, for instance, transmission electron microscopy (TEM) and XPS, were made to assist us in micro-structure analysis.

3-2-2 Results and discussions

(A) C-V measurements & TEM analysis

In this theme, we investigate the oxidation temperature how to influence the formation of W-NCs and its corresponding electrical characteristics. Here, we discuss three conditions of different oxidation temperature (850, 950, 1050°C) but with the same oxidation time (60s). First, fig. 3-2(a) shows the capacitance-voltage hysteresis (C-V) of structure I which oxidized at 850°C. It has only 2V memory windows under V_G-V_{FB}=10V bidirectional voltage sweep. Besides, its C-V memory window reveals the characteristic that only hole carriers could be trapped effectively. On the other hand, fig. 3-2(b) exhibits its cross-section TEM analysis. It is observed that under oxidation temperature of 850°C, the trapping layer WSi2 seemed to be still an almost continuous film, seldom tungsten nanocrystals be formed. The C-V hysteresis of sample oxidized at 950°C, structure 2, is shown in fig. 3-3(a). It has a larger memory window of 9V, and from the cross-section TEM image, fig. 3-3(b), we could see this trapping layer have been formed the discrete nanocrystals with the size of about 9nm. The last condition, 1050°C, the structure 3, which is the highest temperature in our study, reveals nearly 2V windows. From this C-V hysteresis, fig. 3-4(a) the sample has less sharp C-V swing than the other two samples. The TEM diagram, fig. 3-4(b)

also exhibits obviously the nucleation and isolation of W nanocystals and the size of NCs is approximately 10nm.Nevertheless, the tunneling oxide of 1050°C seems to be reduced as compared with that of the other two structures. All of these three structures have enough C-V memory windows to define“1”and“0”states.

(B) Reliability tests (retention & endurance)

In this theme, we detict the retention and endurance measurements for these three different oxidation temperature conditions. On our retention test performed at room temperature, the stress added to samples lets the flat band shift ± 1V from a quasi-neutral state to a charged state, programmed and erased state, respectively. Fig. 3-5(a) reveals the retention property for oxidizing at 850°C. When the carriers inject from Si substrate and store in trapping layer, the stored charges may easily escape from nanocrystals to the Si substrate through the raise of nanocrystal potential energy. Hence, the decay speed of its memory window for both programmed state and erased state is fast during initial 100 seconds. On the other hand, the higher decay rate is likely to result from some shallow trapping states in NCs. The decay rate will gradually become slow during the retention time. After the pass of 1000 seconds, the sample oxidized at 850°C only has a 0.28 memory window(charge remained ratio is about 14%). Fig. 3-5(b) shows the endurance test for oxidizing at 850°C. The pulses under V_G-V_{FB}=10V 1ms condition were applied to evaluate endurance characteristics for the program and erase operation of these three samples. We can see no apparent degradation for its memory window under this pulse condition after 10^6 cycles P/E operations. From this result, we can infer that not enough defects which could create leakage paths and degrade charge storage capability were produced during these P/E operations. Fig. 3-6(a) and Fig. 3-6(b) show the characteristics of retention and endurance measurement, respectively, for sample oxidized at 950°C .Also, its decay rate for retention is initially quick. The decay rate gradually became slow after several ten seconds and the memory window retained 0.92V(charge remained ratio is about 42%), after 1000 seconds. The endurance test reveals the characteristics for sample oxidized at 950°C could be maintained after 10^6 cycles P/E operations. Fig. 3-7(a) and Fig. 3-7(b) show the characteristics of retention and endurance measurement, respectively, for sample oxidized at 1050°C. Almost all of the charges loss within 10s for retention measurement. Fig. 3-7(b) shows its endurance property could be maintained after 10^6 cycles P/E operations.

.

(D)Material analysis and Discussion

In our work, we examined the chemical composition of the oxidized trapping layer by XPS analysis using Al Kx(1486.6eV) x-ray radiation. According to the oxidation mechanics of ISSG system mentioned before, we expect that the WSi_2 film, trapping layer, was oxidized to form W-NCs embedded in SiO_2 layer during ISSG process. Fig. 3-8(a) exhibits the W 4f XPS spectra of different oxidation temperature conditions. It can be found that this spectrum has two main peaks which represent $4f_{7/2}$ and $4f_{5/2}$ binding energy, respectively. It can be thought that each of these two main peaks is composed of two sub-peaks which stand for W-W bond and W-Si bond. The binding energies for W-W bond are 31.4eV($4f_{7/2}$) and 33.5eV($4f_{5/2}$), [3.11], [3.12]. W-Si binding energies are located at 30.8eV and 32.9eV, respectively [3.11], [3.12].Fig. 3-8(b) also shows the Si 2p XPS spectra of different oxidation temperature conditions. There are two main peaks in this spectrum. One is composed of the peaks for SiO_2 and SiO_x binding energy located at 104eV and 103.2eV. The Si-W(100eV) and Si-Si(99.2eV) sub-peaks constitute the other main peak [3.11], [3.12]. From fig. 3-8(a), the higher temperature is, the larger the peak intensity of W-W bond is. The tendency for the peak intensity of W-Si bond is opposite to that for W-W bond when the temperature gets higher. According to the Si spectra, fig. 3-8(b), the Si-O peak shifts a little to higher binding energy and the intensity of Si-W, Si-Si peaks reduce when temperature becomes higher. At 850°C, the W-Si peak is larger than W-W peak, fig. 3-8(a). It infers that not enough thermal energy lets WSi_2 oxidize completely, so a nearly continuous film is seen from TEM. This case makes few W-NCs produced and results in only 2V memory window, which is smaller than others. Fig. 3-8(a) also shows that the intensity of W-W peak is larger than that of W-Si at both 950°C and 1050°C.This agrees with the images of TEM, fig. 3-2(b) and fig. 3-3(b), that NCs formed obviously, so structure 2 has larger memory window(10V), fig. 3-2(a). The structure 3 has smaller window(2V), fig. 3-3(a), because the agglomeration of existing NCs at high temperature(1050°C) makes the density of NCs reduce. The Si XPS spectra, fig. 3-8(b), also shows the reduced intensity of Si-W and Si-Si bond with increased temperature, which indicates higher temperature helps the formation of NCs. Therefore, the temperature needed to form W-NCs from WSi_2 by ISSG system should be higher than 950°C, if we fixed the oxidation time at 60 seconds. On our retention measurement, the best condition is oxidized at 950°C (structure 2). This could be explained that the surrounding dielectric of W-NCs, SiO_x, oxidized more completely to form SiO_2 at higher temperature according to Si XPS spectra which indicates the Si-O bond shifts to higher binding energy when temperature increases, and this lets surrounding defects reduce. Therefore, it prevents the carriers stored in NCs from escaping to neighbor NCs, Al gate, or Si substrate by trap-assist tunneling, so improving the retention characteristic. As for the structure 3, W-NCs become larger

and larger at 1050°C, so they (W-NCs) compress tunneling oxide. This may bring about some interface traps around the tunneling oxide and Si substrate. Consequently, its retention characteristic and CV swing are degraded. No degradation in the endurance tests for these three conditions implies that the structures are so strong that no defects are created during P/E operation, even for 10^6 cycle operations.

3-3 The effect of ISSG oxidation time on W-NCs

3-3-1 Experimental Steps

Fig. 3-9 showed the schematic diagram of fabricating procedure, labeled as structure I. First, a single-crystal 8 inch (100) oriented p-type silicon wafer was chemically cleaned by standard RCA cleaning. Then, a 5-nm-thick thermal oxide was grown on p-type Si substrate by rapid thermal oxidation in an in situ steam generation system (ISSG) as a tunnel oxide. After growing tunnel oxide, we deposited a tungsten silicide film (WSi_2) which has thickness of 4nm by low pressure chemical vapor deposition furnace (LPCVD). Subsequently, a 6-nm-thick amorphous silicon (a-Si) was also deposited by the same system. After finishing WSi_2/a-Si double layer structure, the high temperature thermal oxidation was performed in the rapid thermal anneal system where both oxygen and hydrogen flow. This system is usually called in situ steam generation (ISSG) process. This procedure was executed to let WSi_2 precipitate tungsten nanocystals and form silicon oxide as its surrounding dielectric. We want to investigate the effects of different oxidation time on formation of tungsten nanocrystals. Thus, a thermal oxidation process was used by ISSG system for 30s, 60s, and 90s, respectively. Afterward, a followed 50nm silicon oxide was deposited by PECVD system to form an enough thick control oxide. Finally, the Al gate electrode was deposited by the use of thermal coater and then patterned.

The electrical characteristics, such as capacitance-voltage (C-V), and current density-voltage (J-V) were measured by Keithley 4200 and HP4284 Precision LCR Meter with frequency of 100 kHz. The material analysis, for instance, transmission electron microscopy (TEM) and XPS, were made to assist us in micro-structure analysis.

3-3-2 Results and discussions

(A) C-V measurements & TEM analysis

In this subject, we investigate the oxidation time how to influence the formation of W-NCs and its corresponding electrical characteristics. We discuss three conditions of different oxidation time (30, 60, 90s) but at the same oxidation temperature, 950°C, which is the optimum temperature for W-NCs formation. First, fig. 3-10(a) shows the capacitance-voltage hysteresis (C-V) of structure 4 which oxidized with 30s. It has a very large memory windows, 13V, under V_G-V_{FB}=10V bidirectional voltage sweep. On the other hand, fig. 3-10(b) exhibits its cross-section TEM analysis. It is observed that the trapping layer WSi2 seemed to be still an almost continuous film, just like structure 2. The C-V hysteresis of sample oxidized for 60s, structure 2, is shown in fig. 3-11(a). It has a larger memory window of 9V, and from the cross-section TEM image, fig. 3-11(b), we could see this trapping layer have been formed the discrete nanocrystals with the size of about 9nm. The last condition, 90s, the structure 5, which is the longest oxidation time in our study, reveals, its memory windows could range from 6V to 10V, fig. 3-12(a). The TEM diagram, fig. 3-12(b) also exhibits obviously the nucleation and isolation of nanocystals .Nevertheless, the size of NCs is not uniform for structure 5. All of these three structures have enough C-V memory windows to define“1”and“0”states.

(B) Reliability tests (retention & endurance)

In this theme, we describe the retention and endurance measurements for these three different oxidation time conditions. The stress conditions performed to our retention and endurance test here are the same as those mentioned at last subject (the subject about temperature effect). Fig. 3-13(a) reveals the retention property for structure 4(30s). Its memory window drops rapidly and lost most of it for both programmed state and erased state within initial several ten seconds. Consequently, it only remained a 0.28 memory window (charge remained ratio is about 24%). Fig. 3-13(b) shows the endurance test for the structure 4(30s). We can also see no apparent degradation for its memory window under this pulse condition after 10^6 cycles P/E operations. Fig. 3-14(a) and Fig. 3-14(b) show the characteristics of retention and endurance measurements for structure 2. The retention of structure 2 is steady after initial decay. Finally, the memory window remained 0.92V(charge remained ratio is about 42%) after 1000 seconds. The endurance test reveals the characteristics for structure 2 could be maintained after 10^6 cycles P/E operations. Fig. 3-15(a) and Fig.

3-15(b) exhibit the retention and endurance characteristics for structure 5. It could be found that the retention characteristic of structure 5 is similar to that of structure 2, but the charge remained ratio after 1000 seconds for structure 5 is 49% better than that of structure 2. The performance of structure 5 on endurance measurement shows no apparent degradation after 10^6 operation cycles.

(C)Material analysis and Discussion

The image of TEM, fig. 3-9(b), reveals the nearly continuous trapping layer for structure 4. W XPS spectra, fig. 3-16(a), and Si XPS spectra, fig. 3-16(b), also exhibit the obvious W-Si, Si-Si peaks and incomplete surrounding oxide in it. These results confirm the trapping layer of structure 4 didn't oxidize completely. The W-NCs just formed and many defects surrounded NCs exist in the trapping layer, so they cause the large memory window, 13V, for structure 4, fig. 3-9(a). Also, the retention of structure 4, fig. 3-12(a), drops rapidly and lost most of its memory window due to these defects assisting charges in escaping from W-NCs. As the analyses mentioned before, the structure 2 has enough memory window to define 1", "0"states, fig. 3-2(a), and its retention property compares well with the structure 4, fig. 3-13(a). According to the TEM, fig. 3-10(b), and XPS analysis, fig. 3-16(a), (b) of structure 5, its trapping layer oxidized most completely among these three structures due to longer oxidation time. The longer oxidation time improves the W- NCs precipitating and quality of neighbor oxide. The excellent retention characteristic of structure 5 agrees with material analyses we made before. Nevertheless, it could be seen from TEM, fig. 3-10(b), that the 90s of oxidation time makes W-NCs re-agglomerate to form larger NCs. But not enough thermal energy to lets W-NCs re-agglomerate uniformly. hence, the structure 5 has the various size of memory window. In the endurance test, Fig. 3-16, it indicates the memory window of all structures can be remained after 10^6 program/erase cycles. The effect of oxidation time is similar to that of temperature. The reduced intensity of W-Si, Si-Si bond and the shift to higher energy for Si-O bond from XPS analysis demonstrated suitable oxidation time helps the precipitating for discrete, uniform size of W-NCs and repairs the surrounding defects.

3-4. Conclusions

The effects of oxidation temperature and time on the W-NCs formation are discussed in this chapter. We investigate different temperature (1050, 950, 850°C) with fixed oxidation time 60s, and different oxidation time (30, 60, 90s) with fixed temperature 950°C. It is found that the oxidation temperature, time above 950°C and

60s are needed to form well-discrete W-NCs and have good enough retention property from its corresponding TEM image and electrical measurements. The reduced intensity of W-Si, Si-Si bond and the shift to higher energy for Si-O bond with increased temperature or time from XPS analysis also demonstrate this tendency. But, too high oxidation temperature (1050°C, 60s) or too long oxidation time(950°C ,90s) may cause the size of NCs to become bigger and various, which could reduce NCs density and degrade the electrical characteristics, on re-agglomerating process. Hence, we infer the optimum oxidation condition to fabricate W-NCs memory device by ISSG system is at 950°C, 60s, when the H_2 content is fixed at 2%.

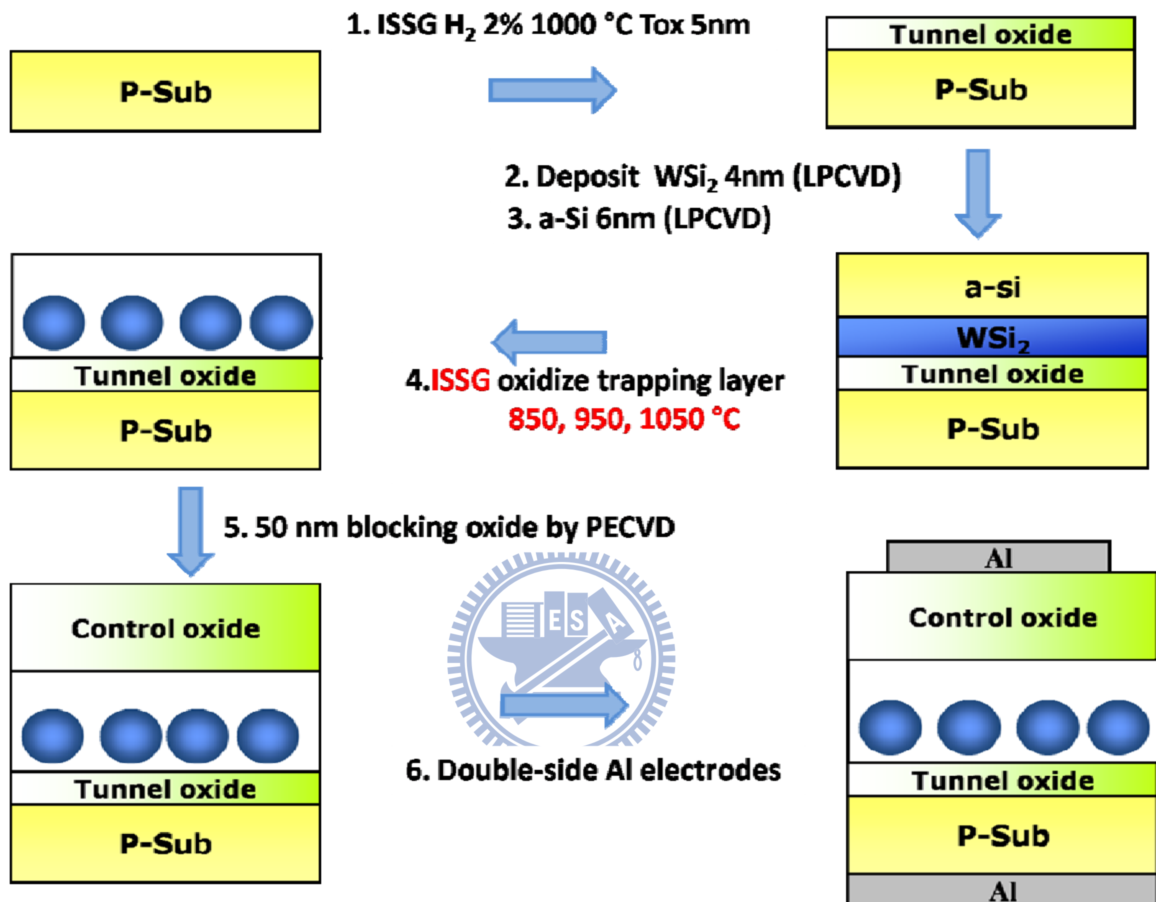
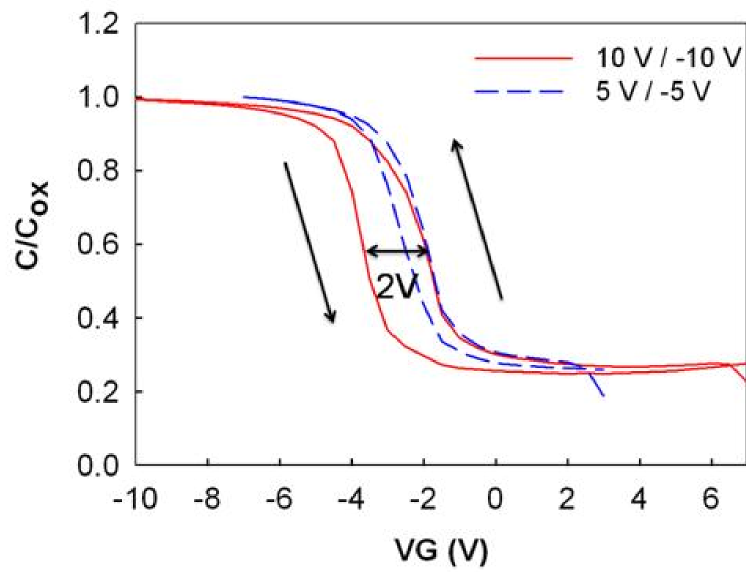
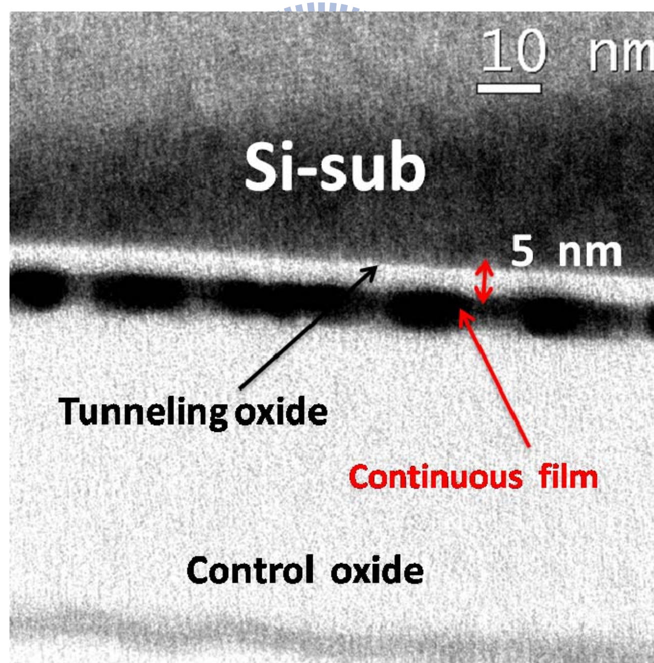


Fig. 3-1 Schematics of the experimental procedures for different ISSG temperature.

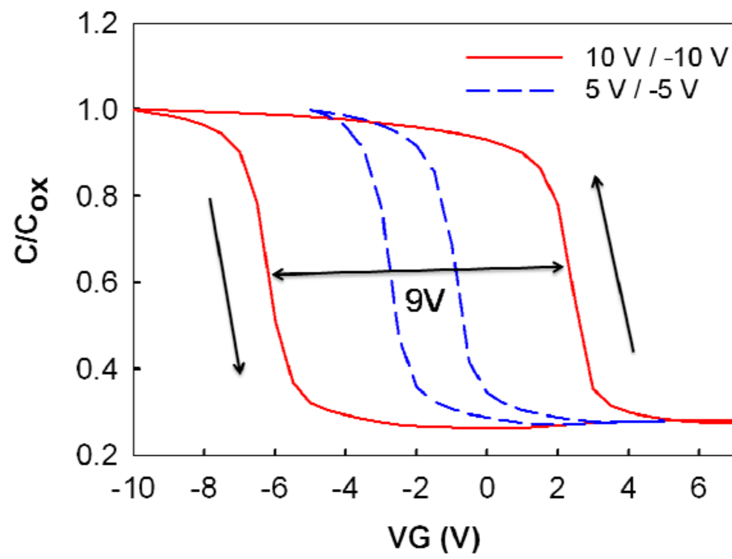


(a)

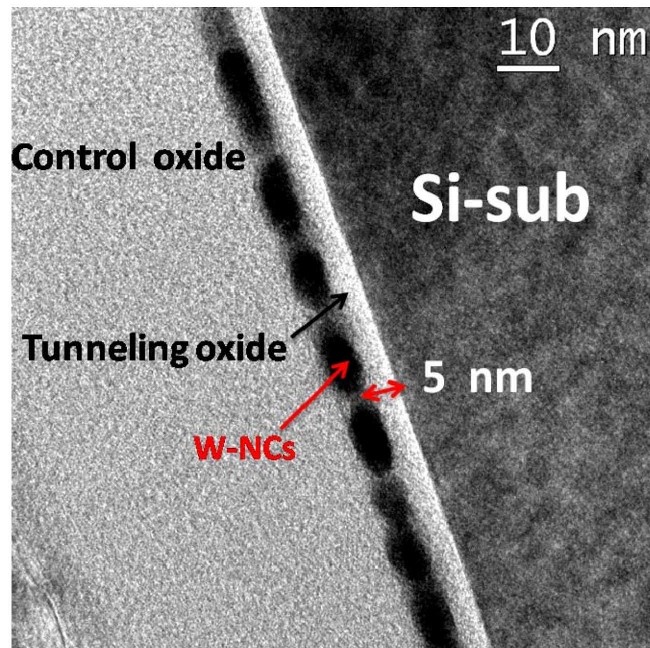


(b)

Fig. 3-2 (a) The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 850°C

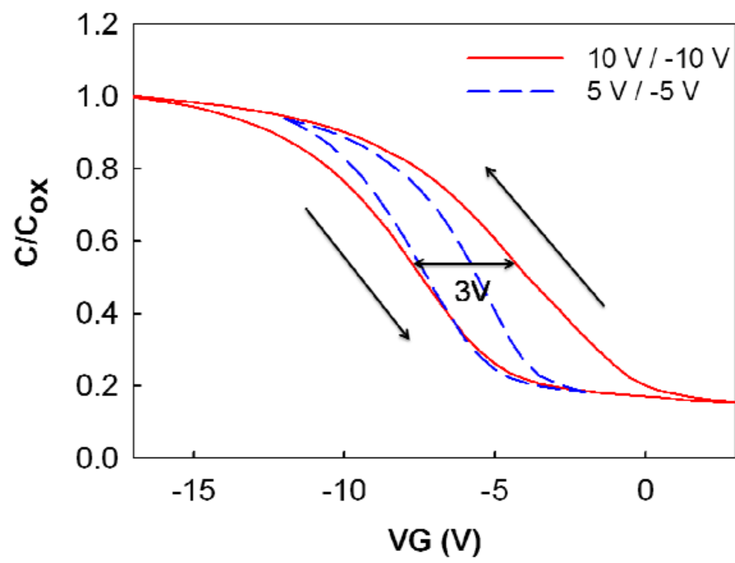


(a)

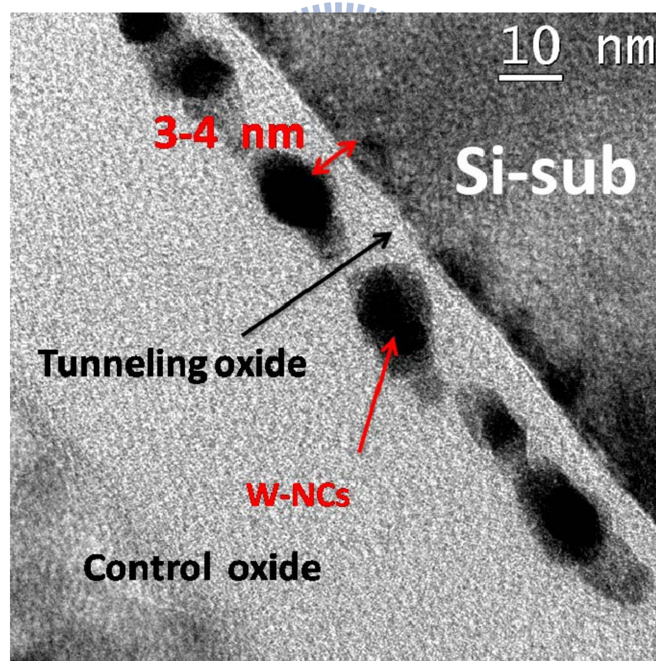


(b)

Fig. 3-3 (a) The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 950°C

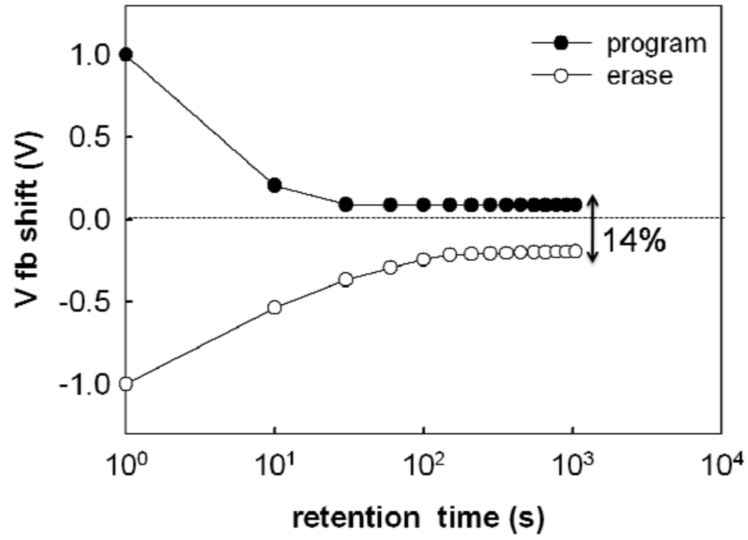


(a)

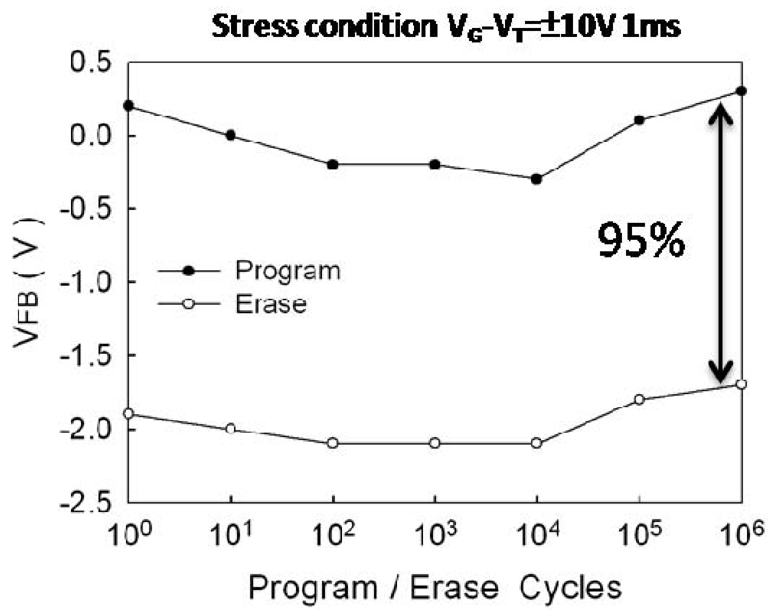


(b)

Fig. 3-4 (a) The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 1050°C

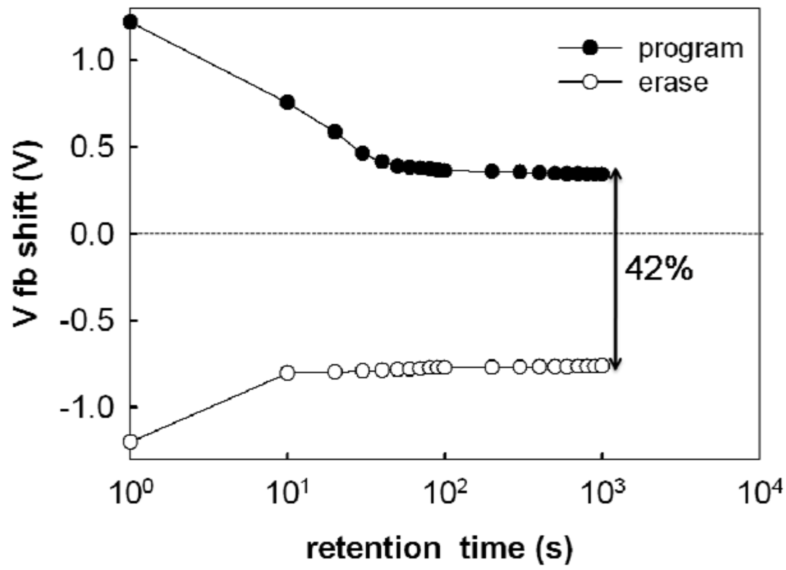


(a)

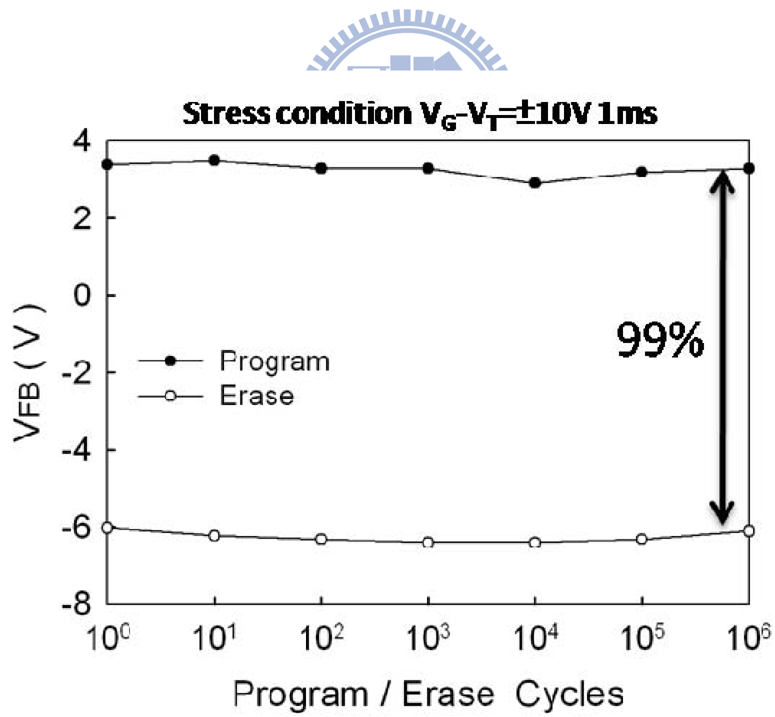


(b)

Fig. 3-5 (a) The retention and (b) the endurance characteristics of 850°C

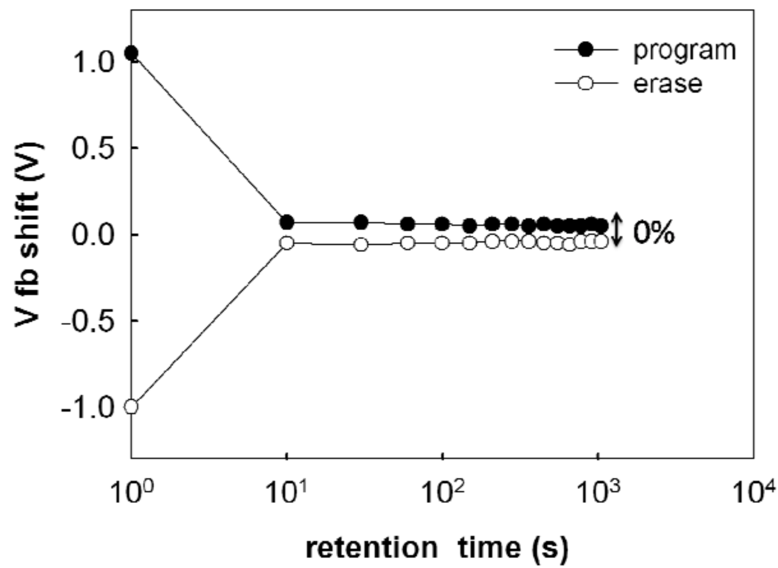


(a)

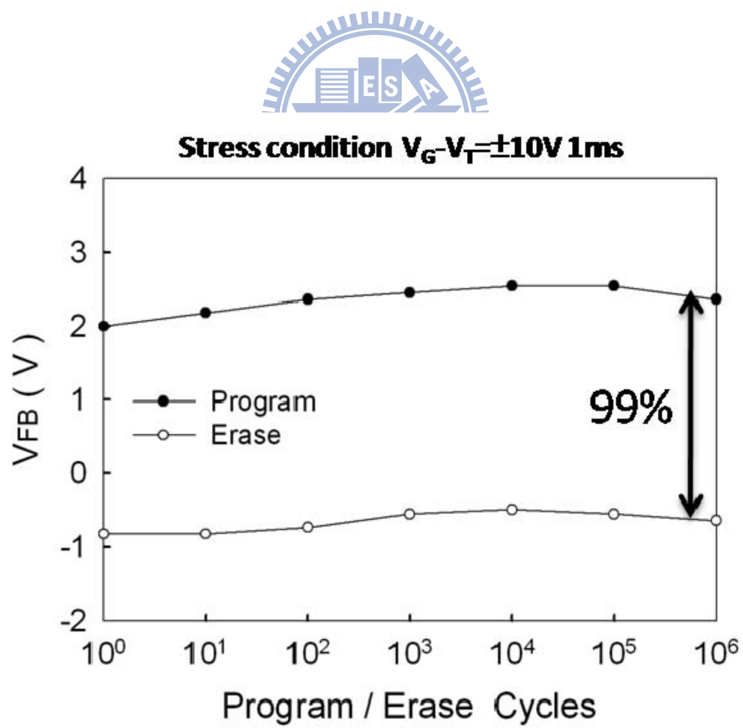


(b)

Fig. 3-6(a) The retention and (b) the endurance characteristics of 950°C



(a)



(b)

Fig. 3-7(a) The retention and (b) the endurance characteristics of 1050°C

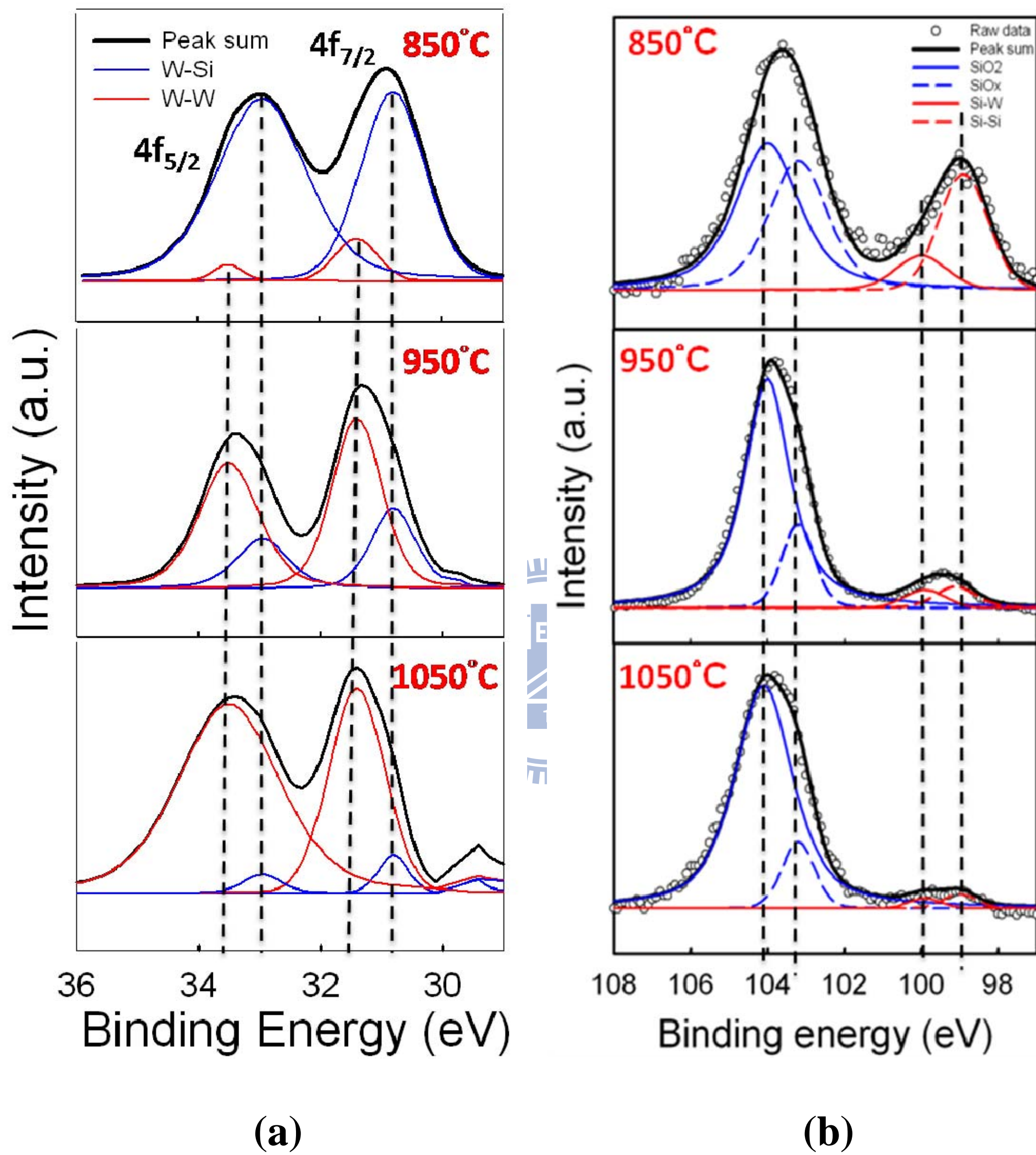


Fig. 3-8 (a) The W 4f XPS spectra and (b) Si 2p XPS spectra for 850°C, 950°C, and 1050°C

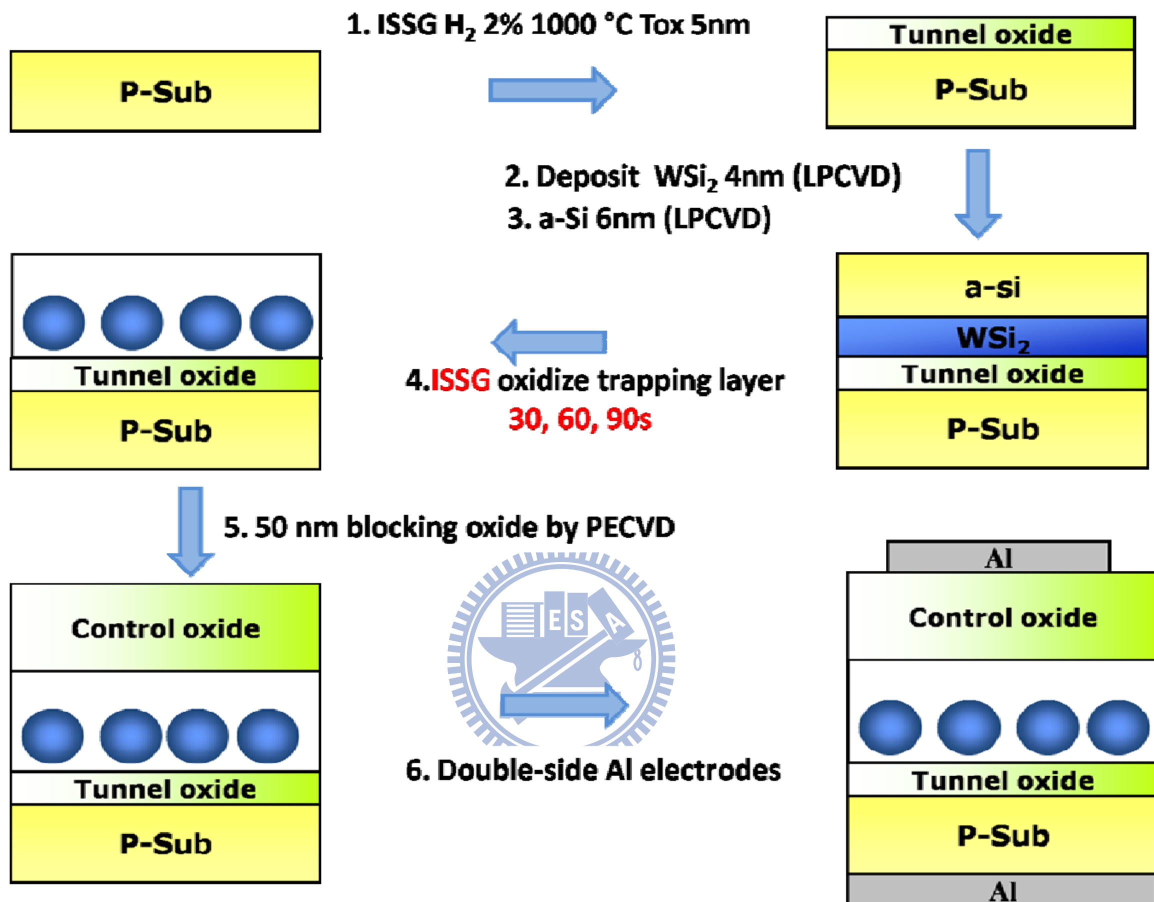
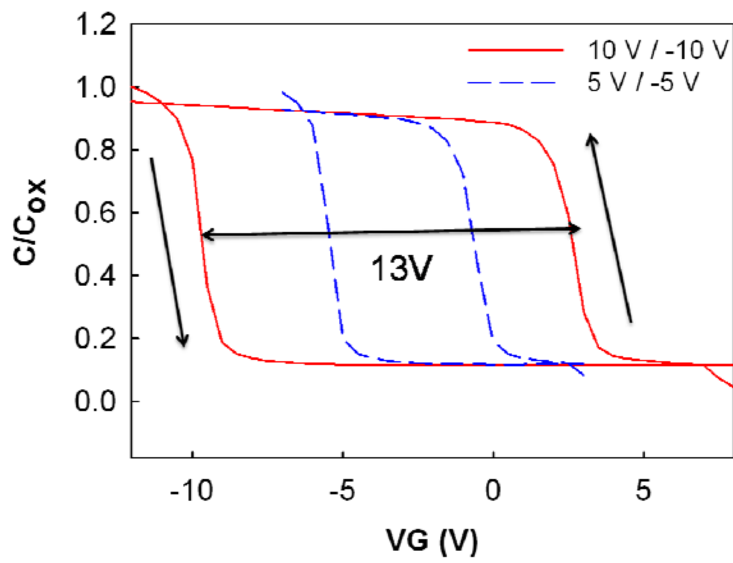
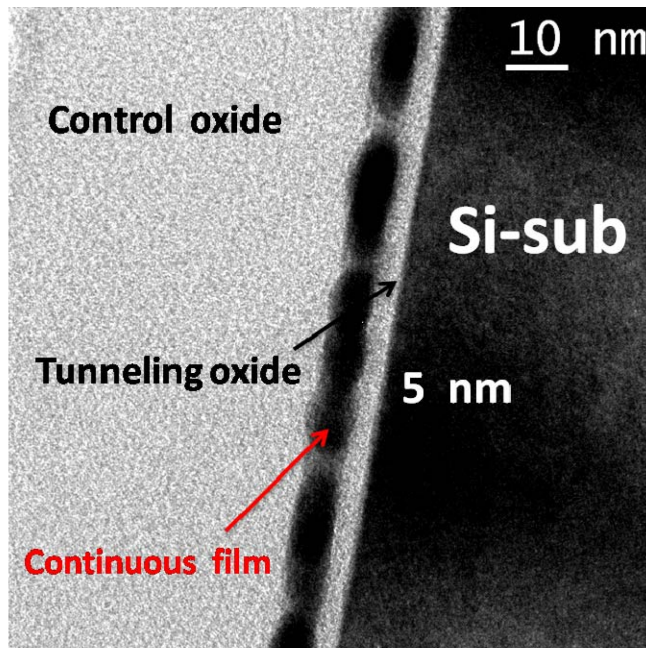


Fig. 3-9 Schematics of the experimental procedures for different oxidation time

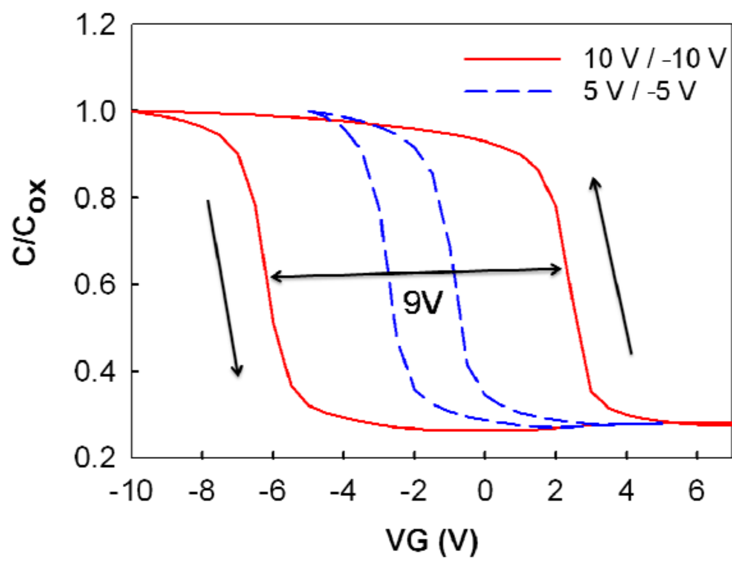


(a)

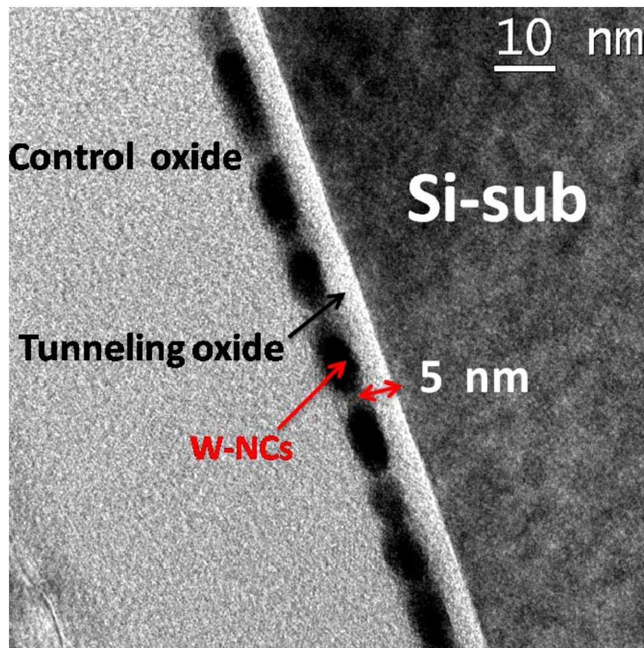


(b)

Fig.3-10 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of oxidation time 30s

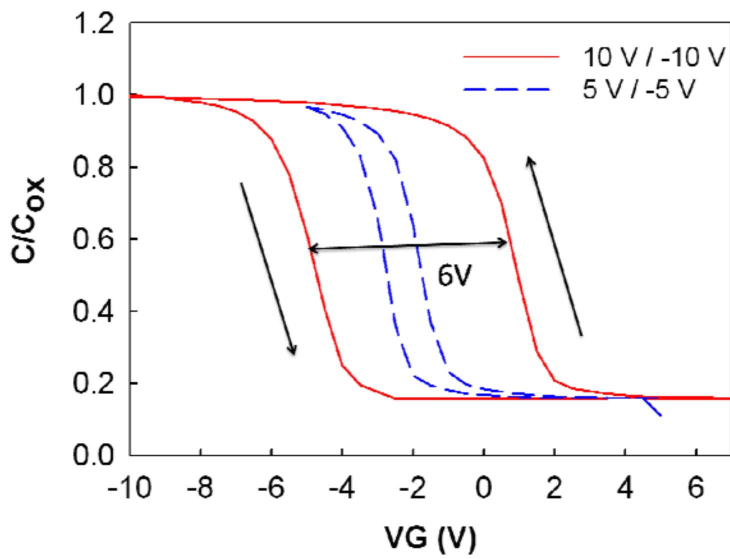


(a)

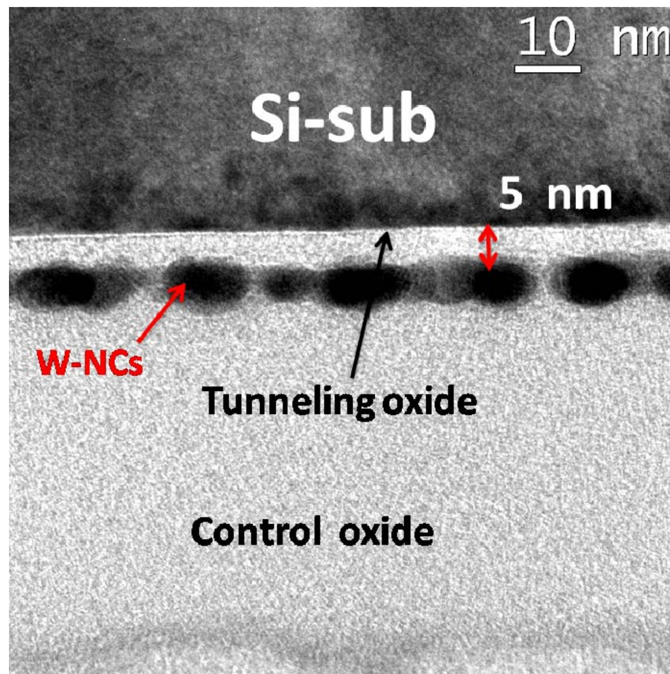


(b)

Fig.3-11 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of oxidation time 60s

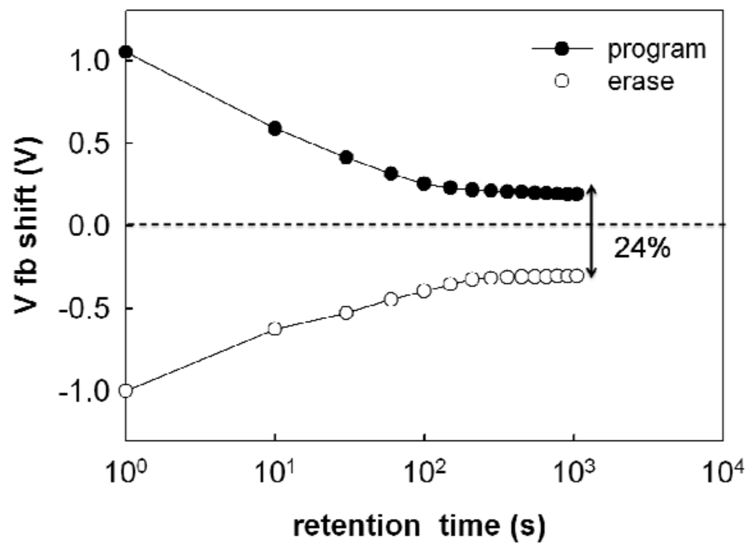


(a)

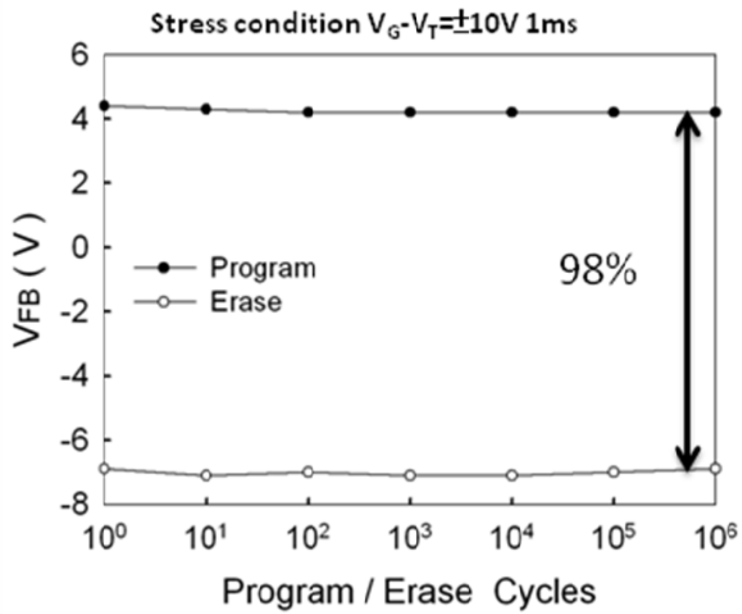


(b)

Fig.3-12 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of oxidation time 90s

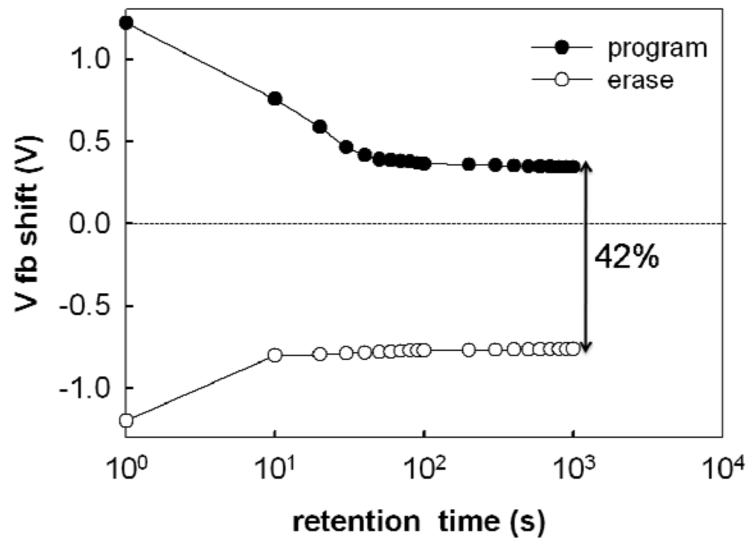


(a)

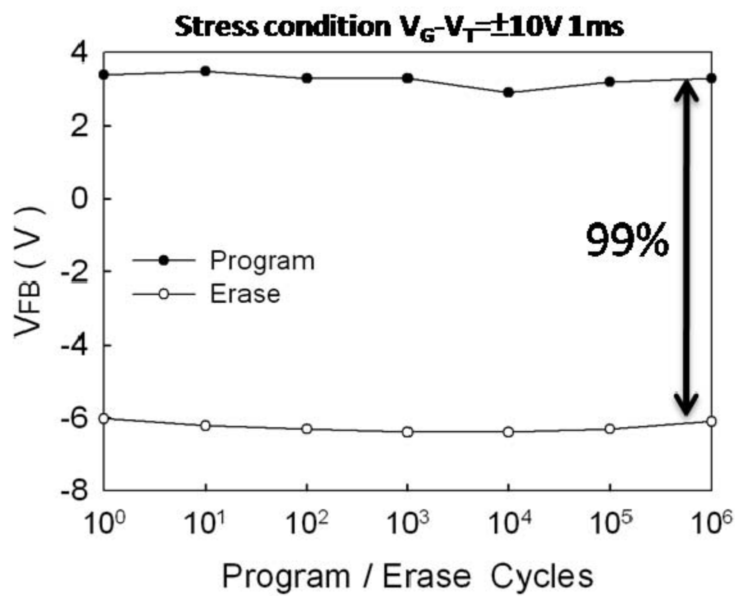


(b)

Fig. 3-13 (a) The retention and (b) the endurance characteristics of oxidation time 30s

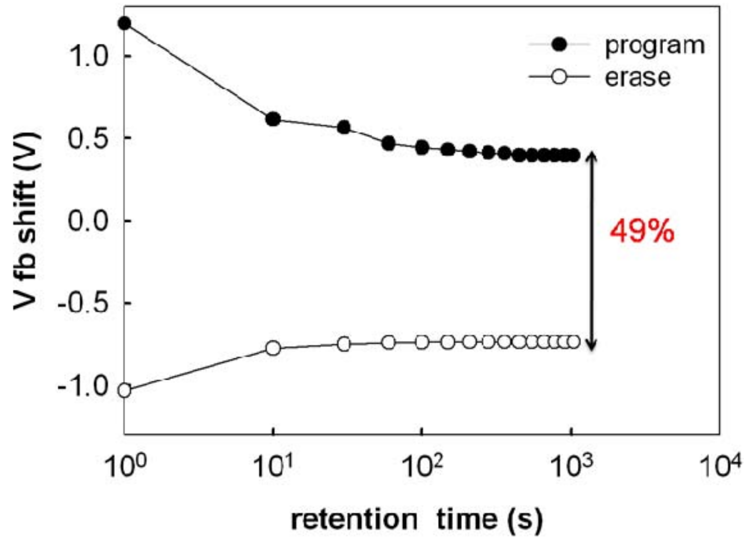


(a)

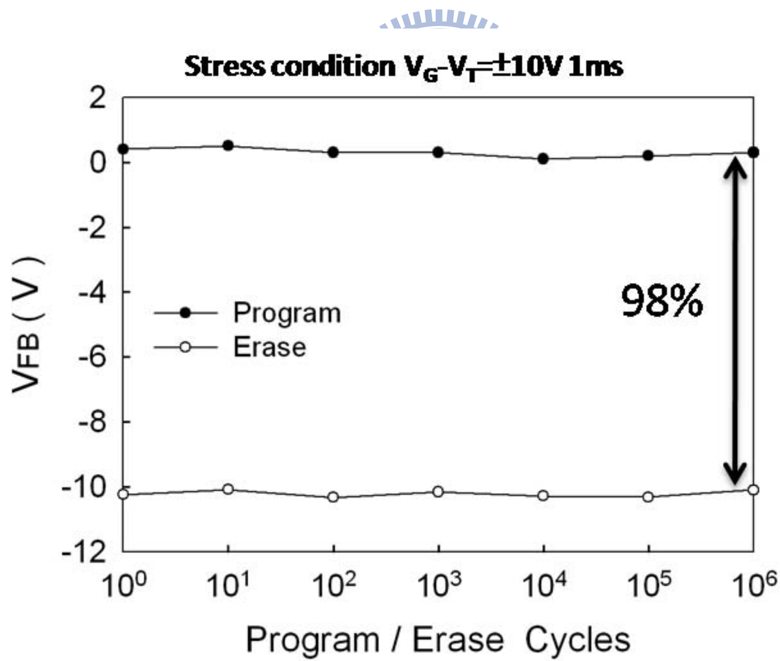


(b)

Fig. 3-14 (a) The retention and (b) the endurance characteristics of oxidation time 60s



(a)



(b)

Fig. 3-15 (a) The retention and (b) the endurance characteristics of oxidation time 90s

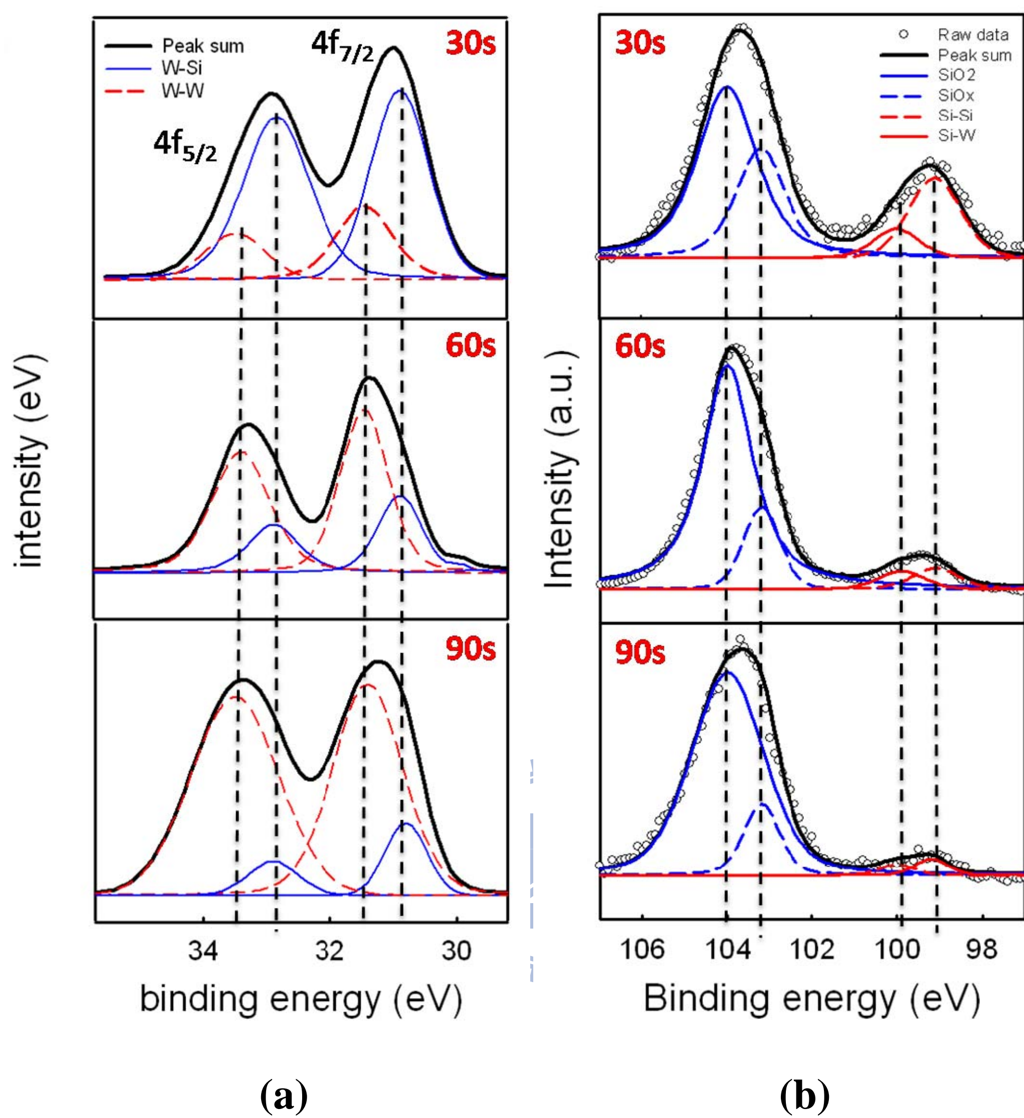


Fig. 3-16 (a) The W 4f XPS spectra and (b) Si 2p XPS spectra for oxidation time 30s, 60s, and 90s

Chapter 4
Comparison of different oxidation methods for W-NCs Nonvolatile Memory

4.1 Motivation

There is a trend for scaling tunneling oxide in order to increasing device density and performance. Therefore, interface roughness and structural defects become more and more important issues on fabricating tunneling oxide. Recently, many references have reported that wet or steam oxidation possesses better oxidizing ability than that of RTO, dry oxidation to resolve two main problems mentioned before when depositing thin oxide film [4.1]. Also, the reliability tests such as SILC, TBD, QBD indeed demonstrate significantly improved properties for wet or steam oxide [4.2].

In this chapter, we investigate two oxidation methods applied to tunneling oxide and trapping layer of our W-NCs memory devices. One is RTO oxidation, and the other is ISSG oxidation. The electrical measurements (C-V, I-V, reliability tests) and corresponding material analyses (TEM& XPS) are made for comparison.

4-2 The comparison of tunneling oxide

4-2-1 Experimental Steps

Fig. 4-1 showed the schematic diagram of fabricating procedure. First, a single-crystal 8 inch (100) oriented p-type silicon wafer was chemically cleaned by standard RCA cleaning. Then, a 5-nm-thick thermal oxide was grown on p-type Si substrate by rapid thermal oxidation (RTO) or in situ steam generation (ISSG) as a tunnel oxide. Then, we deposited a tungsten silicide film(WSi_2) which has thickness of 4nm by low pressure chemical vapor deposition furnace(LPCVD). Subsequently, a 6-nm-thick amorphous silicon (a-Si) was also deposited by the same system. After finishing WSi_2/a-Si double layer structure, we use RTO or ISSG system to oxidize trapping layer. This procedure was executed to let WSi_2 precipitate tungsten nanocystals and form silicon oxide as its surrounding dielectric. We want to

investigate the effects of different oxidation methods on tunneling and trapping layer. Thus, a RTO and ISSG tunneling oxide was fabricated at 1000°C, labeled as structure a and b, respectively. The trapping layer of these two structures was oxidized by RTO system at 950°C 60s. On the other hand, the trapping layer of structure c and d were oxidized by RTO and ISSG system at 950°C 60s, respectively with the same RTO tunneling oxide. Afterward, a followed 50nm silicon oxide was deposited by PECVD system to form an enough thick control oxide. Finally, the Al gate electrode was deposited by the use of thermal coater and then patterned.

The electrical characteristics, such as capacitance-voltage (C-V), and current density-voltage (J-V) were measured by Keithley 4200 and HP4284 Precision LCR Meter with frequency of 100 kHz. The material analysis, for instance, transmission electron microscopy (TEM) and XPS, were made to assist us in micro-structure analysis.

4-2-2 Results and discussions

(A) C-V measurements & TEM analysis

In this subject, we investigate the oxidation methods how to influence the formation of tunneling oxide and its corresponding electrical characteristics. We discuss two ways for depositing tunneling oxide, RTO and ISSG, at the same temperature 1000°C. Also, the same trapping layer oxidation condition, RTO 950°C 60s, was used. First, fig. 4-2(a) shows the capacitance-voltage hysteresis (C-V) of structure A, which has RTO tunneling oxide. It has a large memory windows, 10V, under V_G-V_{FB}=10V bidirectional voltage sweep. On the other hand, fig. 4-2(b) exhibits its cross-section TEM analysis. It is observed that the tunneling oxide of structure A has a thickness of 5nm and discrete NCs embedded in surrounding dielectrics. The C-V hysteresis of sample having ISSG tunneling oxide, structure B, is shown in fig. 4-3(a). It has a smaller memory window of 5V, and from the cross-section TEM image, fig. 4-3(b), we could see its tunneling oxide thickness is the same as structure A, 5nm. This trapping layer also formed the discrete NCs like that of structure A due to the same oxidation condition. All of these two structures have enough C-V memory windows to define“1”and“0”states.

(B) I-V measurement

The current density-voltage (J-V) characteristics of these two different conditions were measured by gate voltage sweeping from 0V to 10V and 0V to -10V. J-V result is shown in fig. 4-4. The structure B (ISSG tunneling oxide) has smaller

leakage current density than that of structure A (RTO tunneling oxide). Their leakage current density are about the order of 10^{-7}.

(C) Reliability tests (retention & endurance)

In this theme, we describe the retention and endurance measurements for these two structures, whose tunneling oxide oxidized by RTO and ISSG system. The stress conditions performed to our retention and endurance test here are the same as those at last two subjects (the subject about temperature and time effects). Fig. 4-5(a) reveals the retention property for structure A. Its memory window drops rapidly initially. Consequently, it lost all of its memory window only after several hundreds seconds. Fig. 4-5(b) shows the endurance test for the structure A. There is a little degradation for its memory window under this pulse condition. The magnitude of its memory window reduced to 89% of that before pulse stress after 10^6 cycles P/E operations. Fig. 4-6(a) and Fig. 4-6(b) show the characteristics of retention and endurance measurements for structure B. The memory window of structure B gradually and continually decays on the whole retention process. Finally, the memory window remained about 0.44V (charge remained ratio is about 22%) after 1000 seconds. The endurance test reveals the characteristics for structure B could be maintained after 10^6 cycles P/E operations.

(D) Analysis and Discussion

The magnitude of memory window has a conspicuous difference between these two structures, fig 4-2(a), fig 4-3(a). Their trapping layers are oxidized on the same condition, RTO 950°C 60s, and the images of TEM show they have the resemblance to each other, fig 4-2(b), fig 4-3(b). Hence, we exclude the factor of trapping layer which may cause the difference of their memory window. We guess the main factor is only the different oxidation method for depositing tunneling oxide. Different oxidation methods may influence the thickness and the quality of tunneling oxide which determine the carrier injection through tunneling oxide. It is observed that they have the same thickness of tunneling oxide, 5nm, from TEM, fig 4-2(b), fig 4-3(b). We consider only the quality of tunneling oxide could probably effect the magnitude of memory window. From J-V results that the structure B (ISSG tunneling oxide) has smaller leakage current density than that of structure A (RTO tunneling oxide), we infer the ISSG oxide has well oxidizing ability to reduce defects produced in it, so the trap-assist-tunneling current could be cut down. The better quality of ISSG oxide obstructs the injection of carrier, so the magnitude of memory window of ISSG oxide smaller than that of RTO oxide observed. The retention measurement also supports our argument. The structure B (ISSG tunneling oxide) has better retention property

than that of structure A (RTO tunneling oxide), Fig. 4-5(a), Fig. 4-6(a). The charges stored in NCs could escape to neighbor NCs by surrounding defects ( ) or to substrate through tunneling oxide ( ). Both structures have similar leakage to neighbor NCs due to the same trapping layer oxidation condition. Hence, only the leakage to substrate through tunneling oxide causes the difference of the retention property. The ISSG tunneling oxide has better quality of oxide, so charges stored in NCs escape to substrate by trap-assist-tunneling more difficultly. Consequently, ISSG tunneling oxide could improve retention property.

4-3 The comparison of trapping layer

4-3-1 Experimental Steps

Fig. 4-7 showed the schematic diagram of fabricating procedure. First, a single-crystal 8 inch (100) oriented p-type silicon wafer was chemically cleaned by standard RCA cleaning. Then, a 5-nm-thick thermal oxide was grown on p-type Si substrate by rapid thermal oxidation (RTO) or in situ steam generation (ISSG) as a tunnel oxide. Then, we deposited a tungsten silicide film(WSi_2) which has thickness of 4nm by low pressure chemical vapor deposition furnace(LPCVD). Subsequently, a 6-nm-thick amorphous silicon (a-Si) was also deposited by the same system. After finishing WSi_2/a-Si double layer structure, we use RTO or ISSG system to oxidize trapping layer. This procedure was executed to let WSi_2 precipitate tungsten nanocystals and form silicon oxide as its surrounding dielectric. We want to investigate the effects of different oxidation methods on tunneling and trapping layer. Thus, a RTO and ISSG tunneling oxide was fabricated at 1000°C, labeled as structure a and b, respectively. The trapping layer of these two structures was oxidized by RTO system at 950°C 60s. On the other hand, the trapping layer of structure c and d were oxidized by RTO and ISSG system at 950°C 60s, respectively with the same RTO tunneling oxide. Afterward, a followed 50nm silicon oxide was deposited by PECVD system to form an enough thick control oxide. Finally, the Al gate electrode was deposited by the use of thermal coater and then patterned.

4-3-2 Results and discussions

(A) C-V measurements & TEM analysis

In this subject, we investigate the oxidation methods how to influence the

formation of W-NCs in trapping layer and its corresponding electrical characteristics. We discuss two ways for oxidizing trapping layer, RTO and ISSG, at the same condition 950°C 60s. Also, the same ISSG tunneling oxide at 1000°C was used. First, fig. 4-8(a) shows the capacitance-voltage hysteresis (C-V) of structure C, whose trapping layer oxidized by ISSG. It has memory window of 5V under V_G-V_{FB}=10V bidirectional voltage sweep. On the other hand, fig. 4-8(b) exhibits its cross-section TEM analysis. It is observed that the tunneling oxide has a thickness of 5nm and discrete NCs embedded in surrounding dielectrics. The C-V hysteresis of structure D is shown in fig. 4-9(a). It has a larger memory window of 10V, and from the cross-section TEM image, fig. 4-9(b), we could see its tunneling oxide thickness is the same as structure B, 5nm. We could see this trapping layer form more discrete nanocrystals with the size of about 9nm. All of these two structures have enough C-V memory windows to define"1"and"0"states.

(B) Reliability tests (retention & endurance)

In this theme, we describe the retention and endurance measurements for these two structures, whose trapping layer oxidized by RTO and ISSG system at the same condition 950°C 60s. The stress conditions performed to our retention and endurance test here are the same as those at last two subjects (the subject about temperature and time effects). Fig. 4-10(a) and Fig. 4-10(b) show the characteristics of retention and endurance measurements for structure C. The memory window of structure C gradually and continually decays on the whole retention process. Finally, the memory window remained about 0.44V (charge remained ratio is about 22%) after 1000 seconds. The endurance test reveals the characteristics for structure C could be maintained after 10^6 cycles P/E operations. Fig. 4-11(a) and Fig. 4-11(b) show the characteristics of retention and endurance measurements for structure D. The retention of structure D is steady after initial decay. Finally, the memory window remained 0.92V (charge remained ratio is about 42%) after 1000 seconds. The endurance test reveals the characteristics for structure D could be maintained after 10^6 cycles P/E operations.

(C)Material analysis and Discussion

There is an obvious difference on the magnitude of memory window for these two structures, fig. 4-10(a), fig. 4-11(a). The structure D has a larger memory window than that of structure C. The retention tests also show the structure D has better property. We consider their tunneling oxides don't cause this difference because of the same oxidation method and the same thickness from TEM image. Therefore, we think the

major factor is the different oxidation condition on trapping layer. The XPS analysis we made could help to explain it. The W XPS spectra, fig. 4-12(a) and fig. 4-12(b), show the structure D has higher intensity of W-W peak and smaller for W-Si. Besides, the Si XPS spectra, fig. 4-13(a) and fig. 4-13(b) also reveal the structure D has a more completed SiO_2 bond and less intensity of W-Si and Si-Si peaks. According to these material analyses, we infer the ISSG method applied to oxidize trapping layer has better oxidizing ability than that of RTO to form discrete W-NCs and good enough surrounding dielectric. The structure D has fewer surrounding defects for charges stored in NCs to assist them in escaping to neighbor NCs. Consequently, the larger memory window and better retention property for structure D are expected and observed.

4-4. Conclusions

In this chapter, we compare the ISSG method with RTO method on applying to deposit tunneling oxide and oxidize trapping layer. The samples with ISSG and RTO tunneling oxide are fabricated, respectively at the same oxidized trapping layer condition, RTO 950°C 60s, (structure A and B). On the other hand, the trapping layers of samples oxidized by ISSG and RTO with the same ISSG tunneling oxide are also made, (structure C and D). According to the electrical measurements (C-V, I-V, reliability tests), it is obviously found that applying ISSG to our devices exhibits much better properties than applying RTO. From TEM images and XPS analyses, we also observe the ISSG method provides better oxidizing ability to form discrete W-NCs and more completed surrounding dielectric.

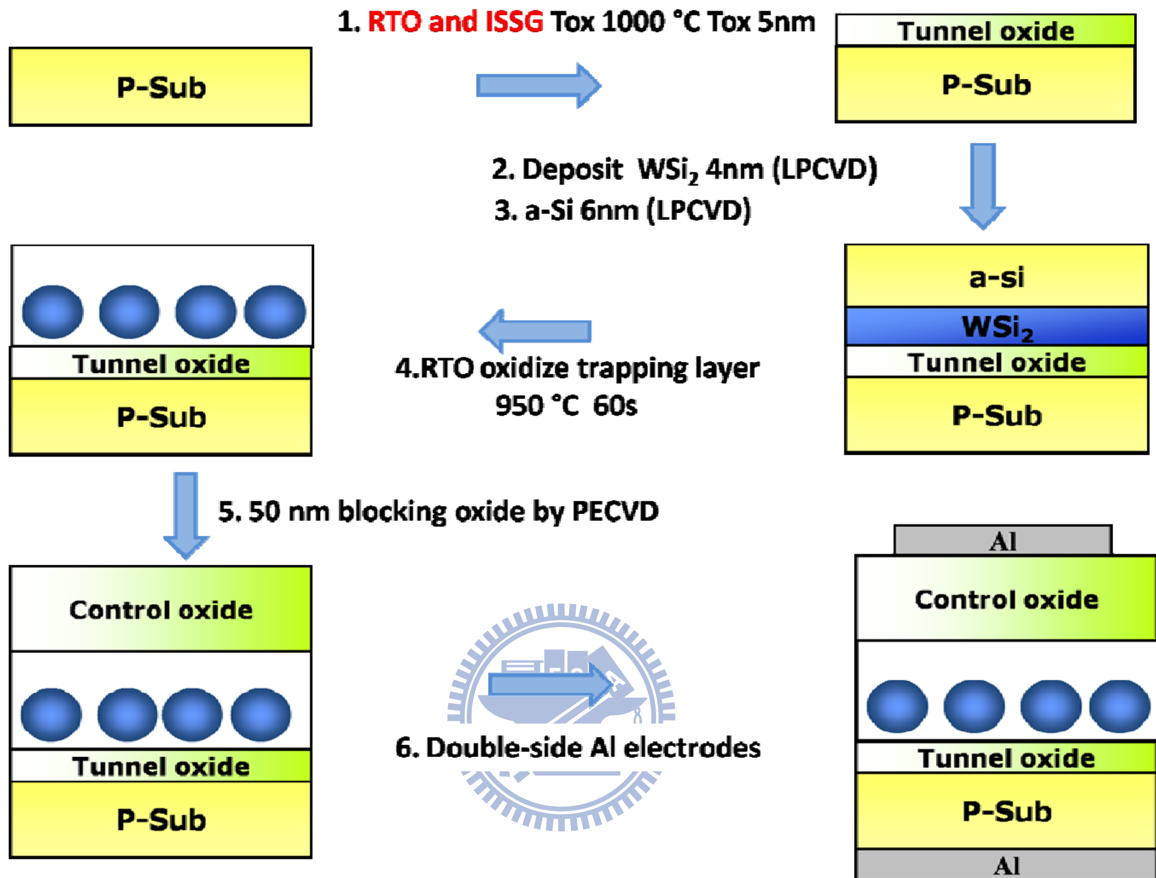
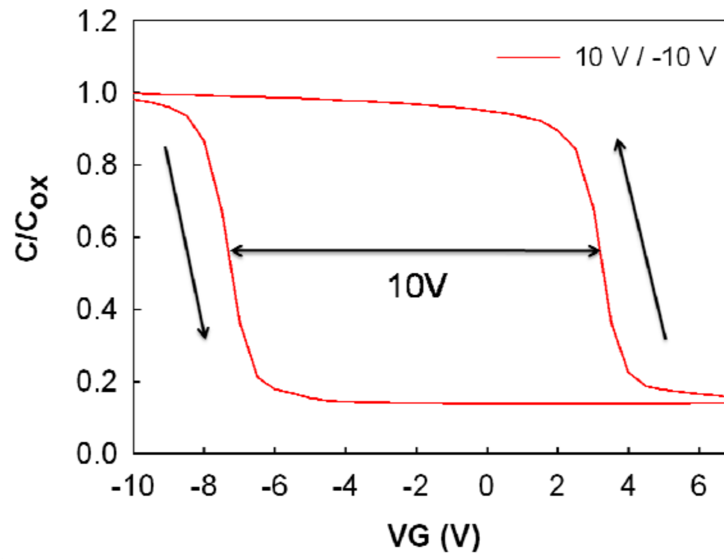
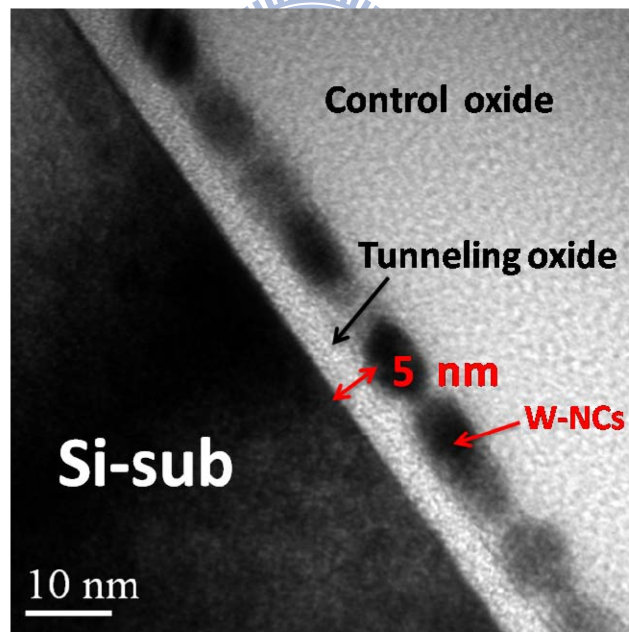


Fig. 4-1 Schematics of the experimental procedures for RTO and ISSG Tox fabrication

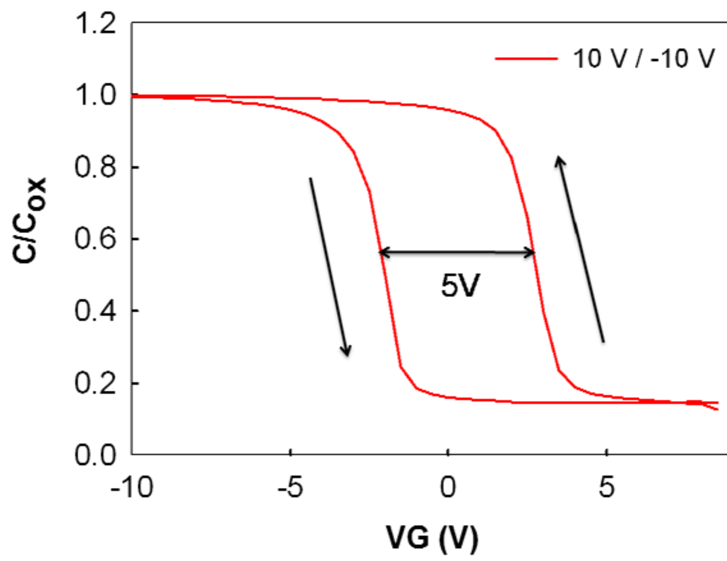


(a)

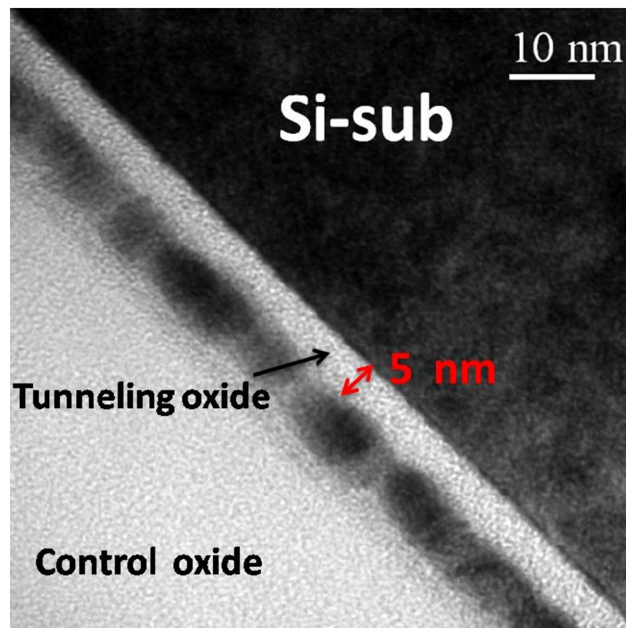


(b)

Fig.4-2 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of RTO tunneling oxide



(a)



(b)

Fig.4-3 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of ISSG tunneling oxide

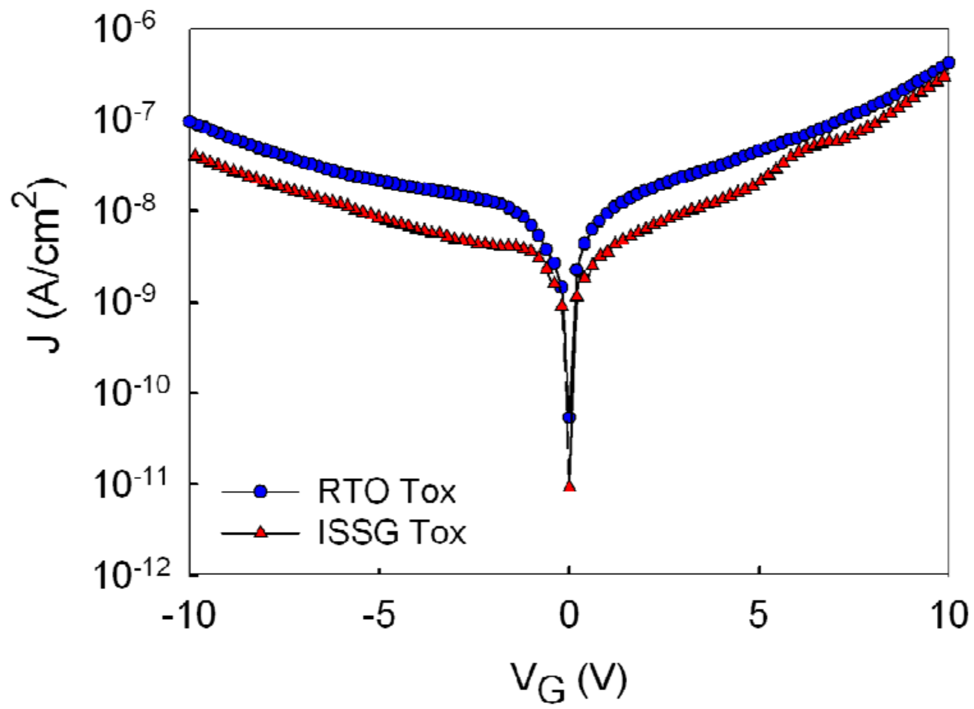
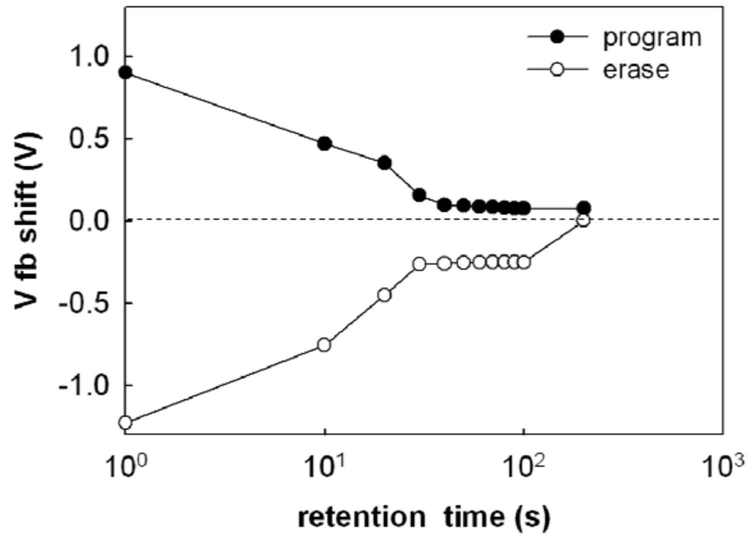
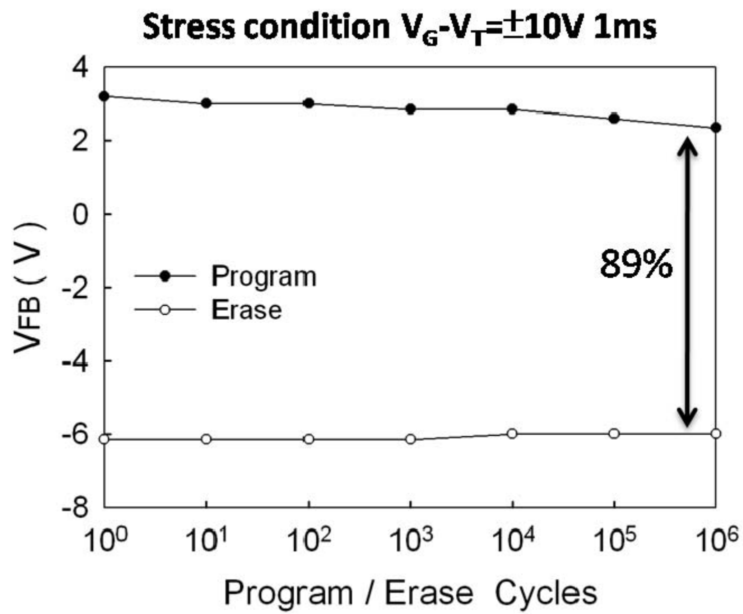


Fig. 4-4 The comparison of current density-gate voltage hysteresis between RTO and ISSG tunneling oxide

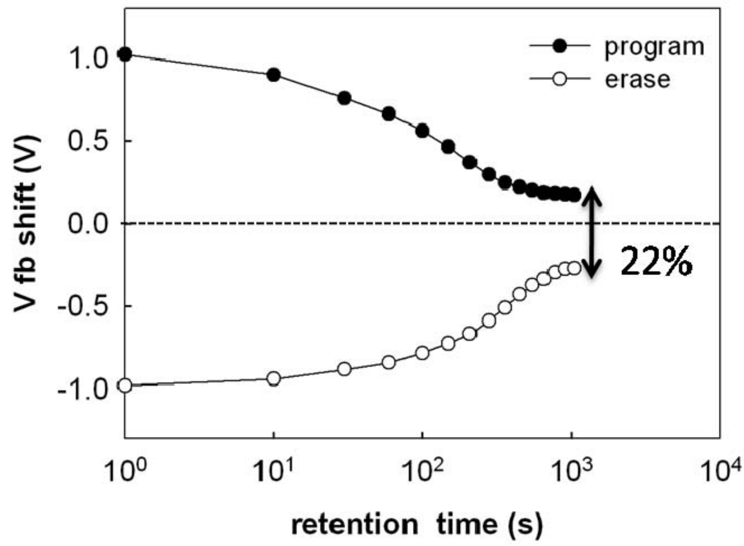


(a)

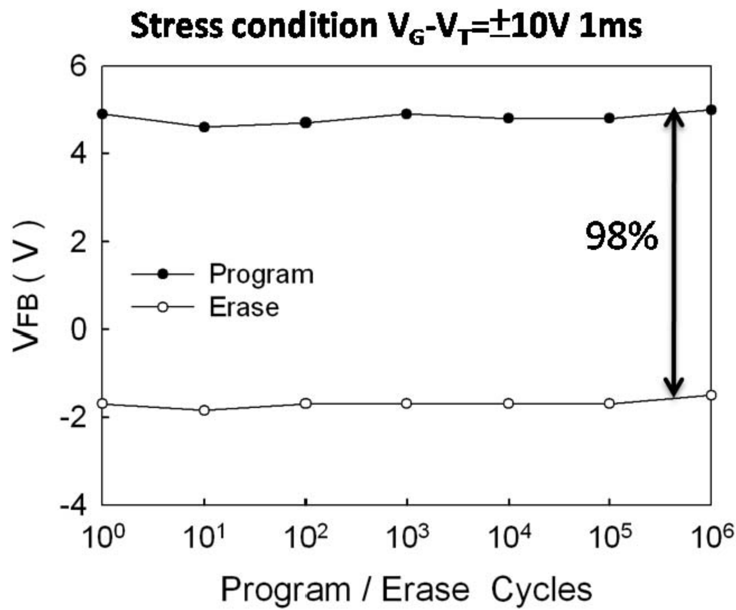


(b)

Fig. 4-5 (a) The retention and (b) the endurance characteristics of RTO tunneling oxide



(a)



(b)

Fig. 4-6 (a) The retention and (b) the endurance characteristics of ISSG tunneling oxide

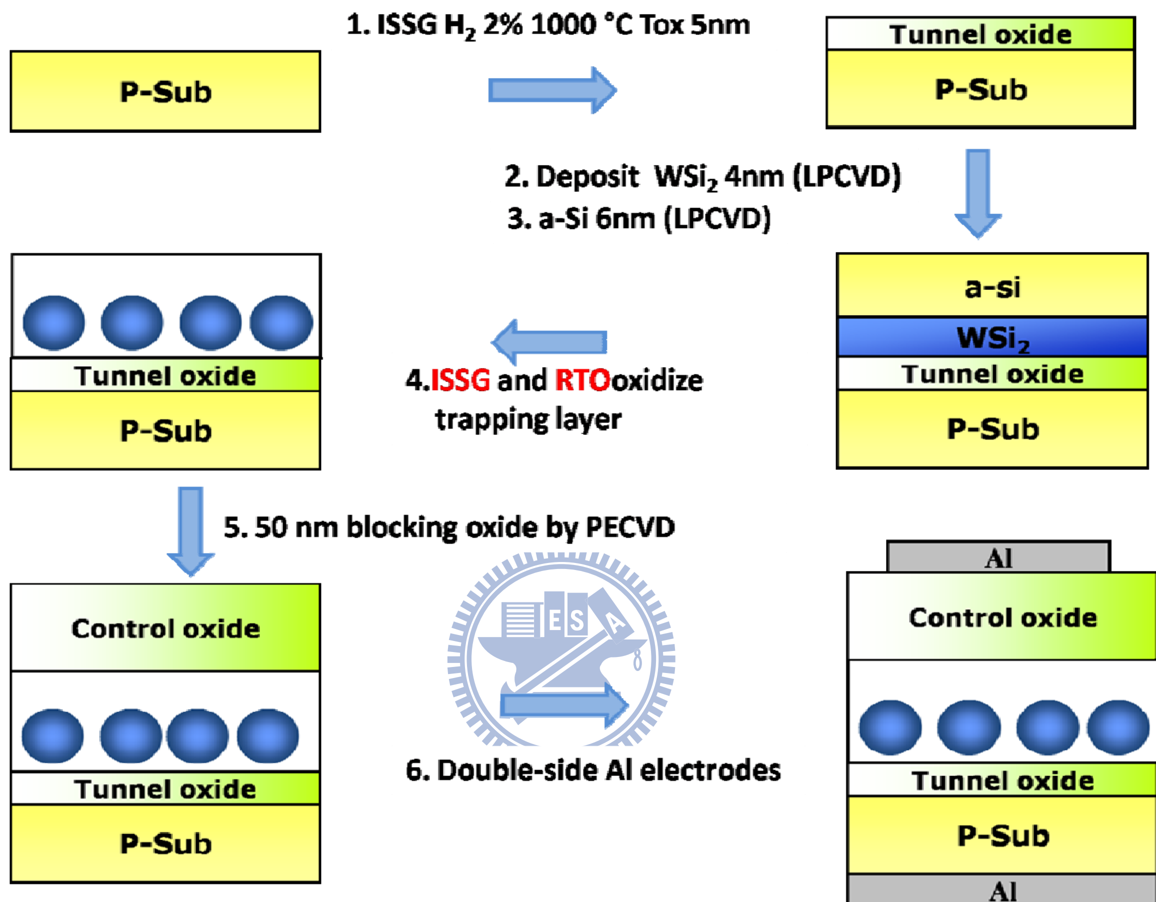
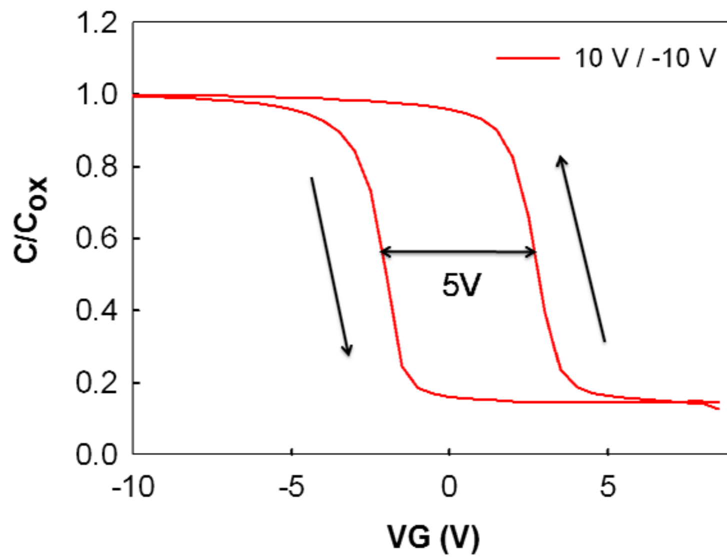
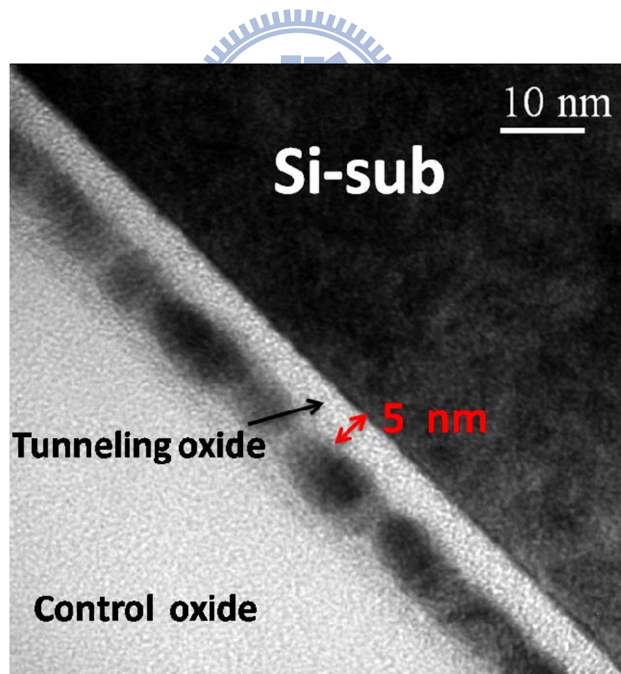


Fig. 4-7 The schematics of the experimental procedures for oxidizing trapping layer by RTO and ISSG

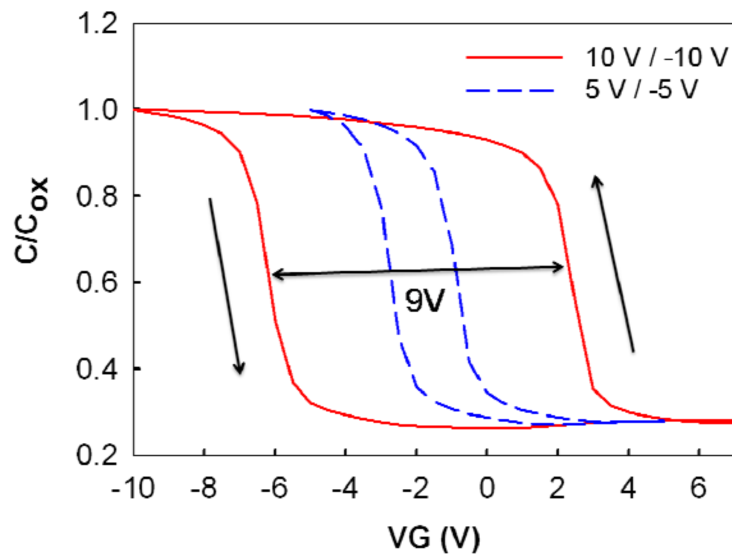


(a)

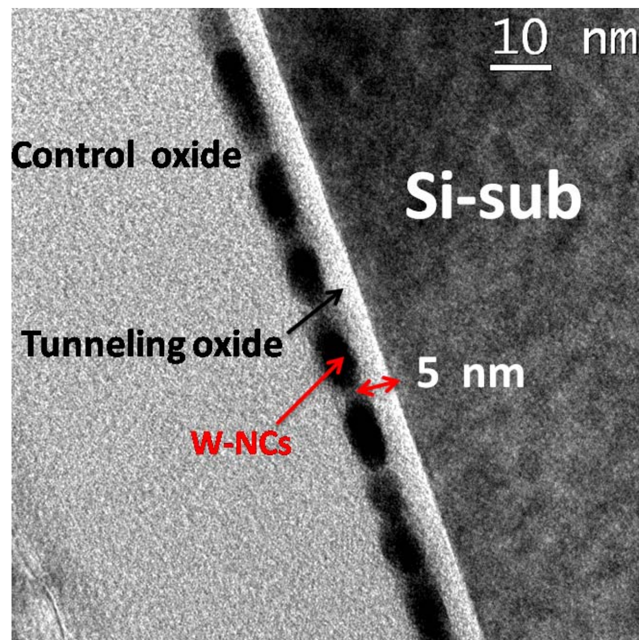


(b)

Fig.4-8 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of RTO method

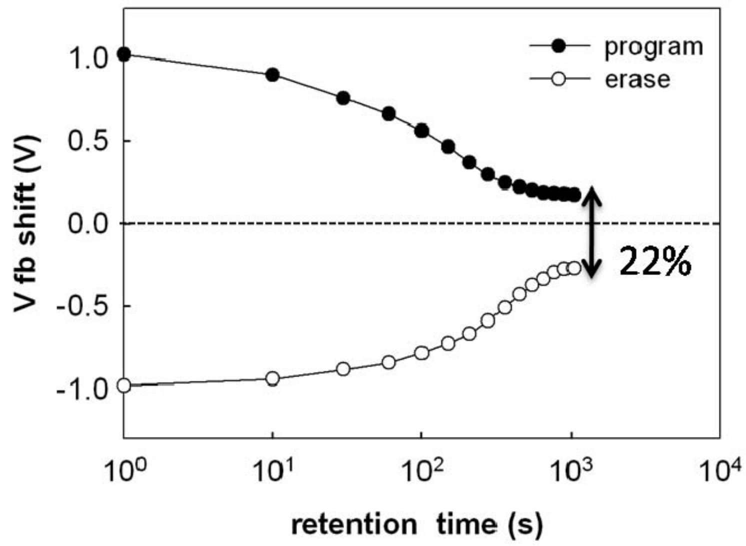


(a)

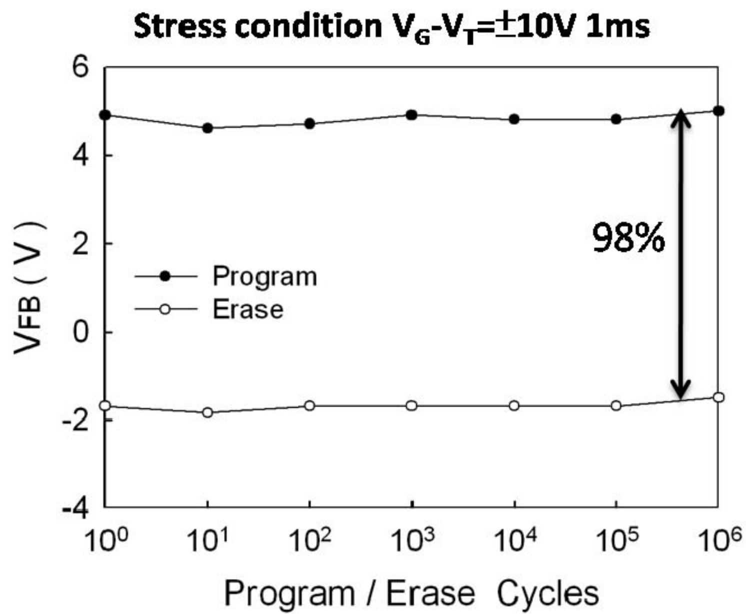


(b)

Fig.4-9 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of ISSG method

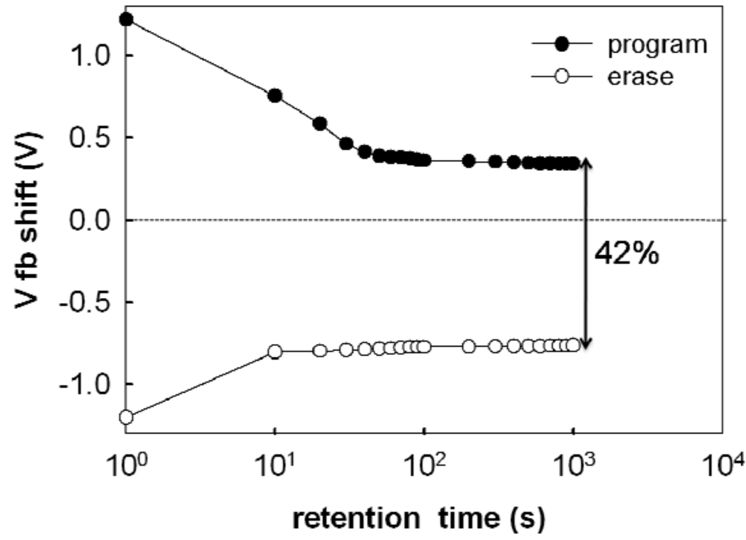


(a)

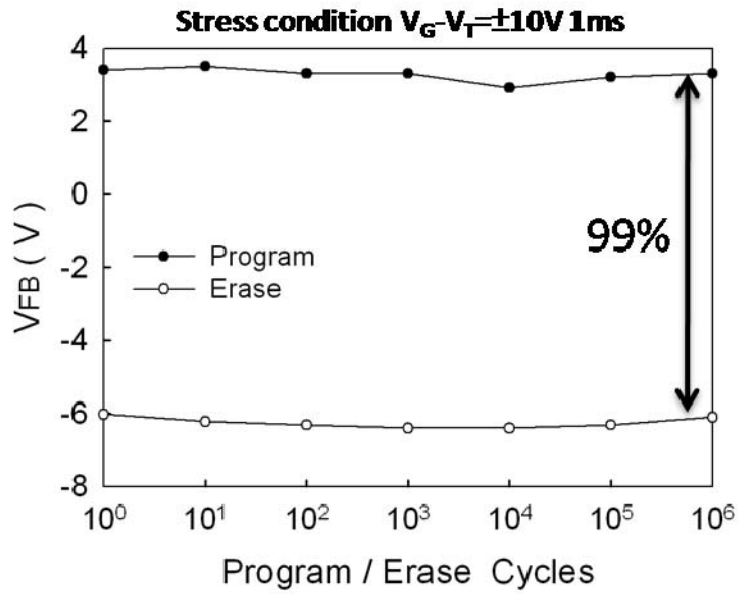


(b)

Fig.4-10 (a) The retention and (b) the endurance characteristics of RTO method

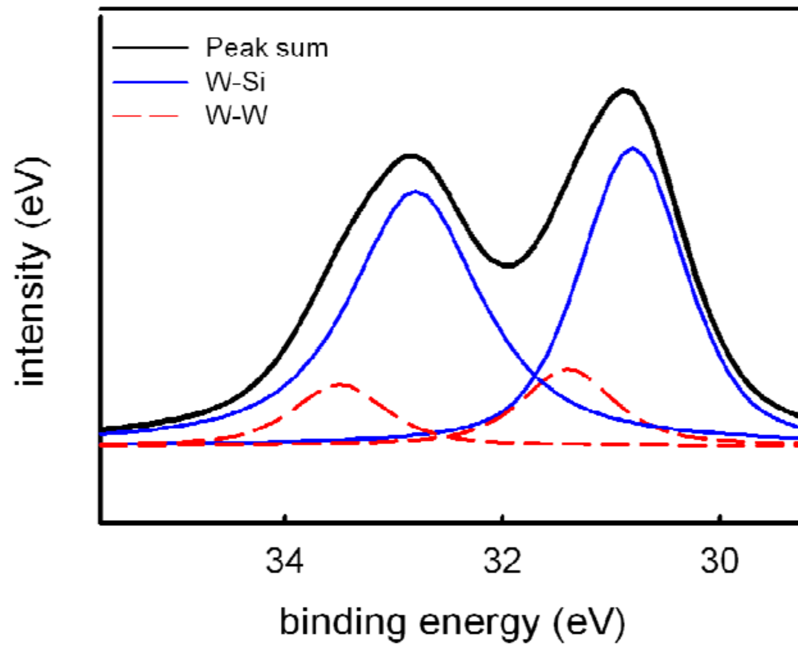


(a)

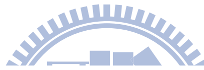


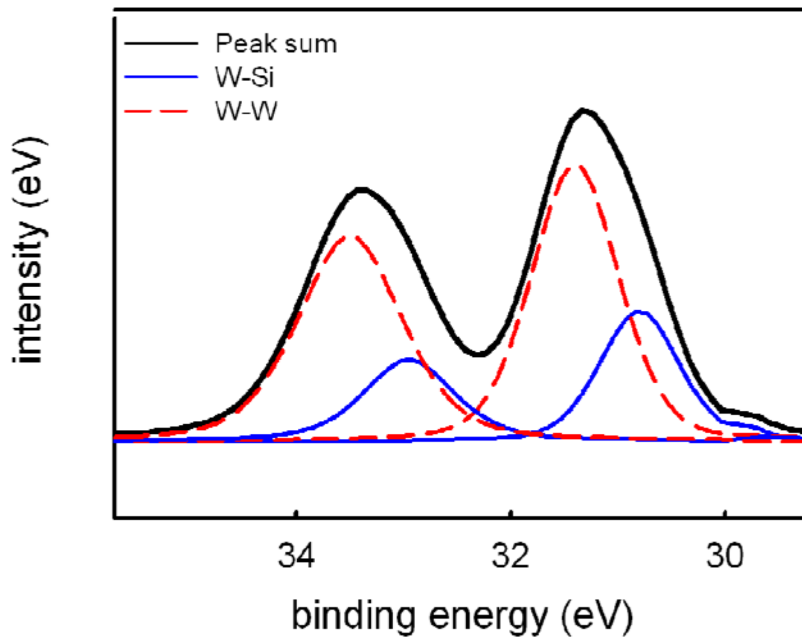
(b)

Fig.4-11 (a) The retention and (b) the endurance characteristics of ISSG method



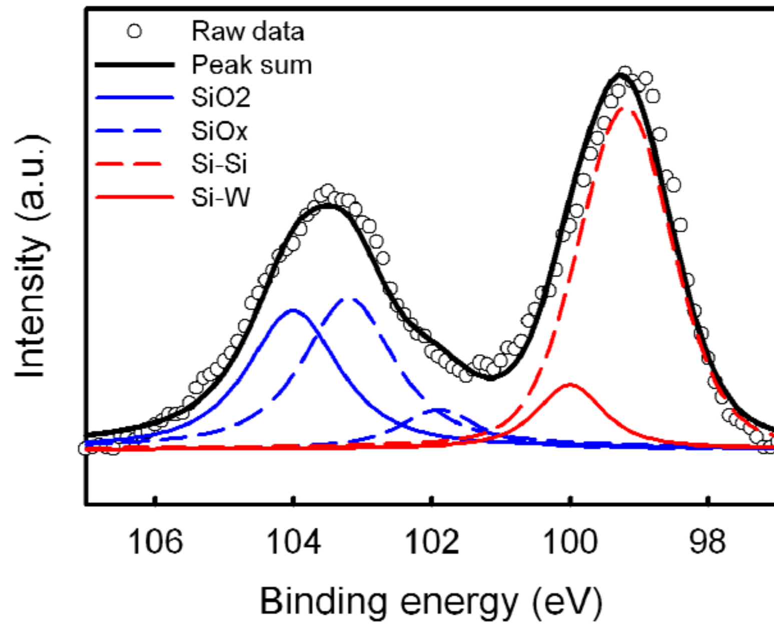
(a)



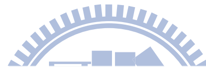


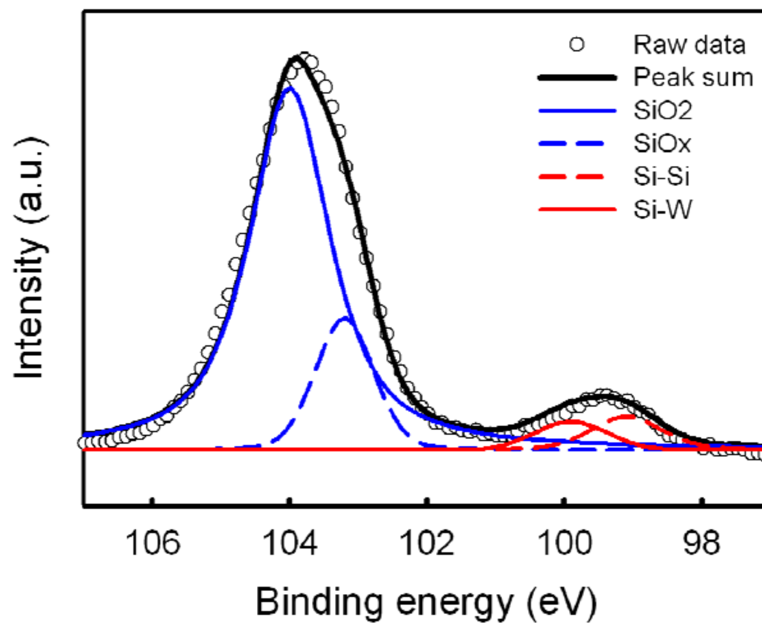
(b)

Fig. 4-12 (a) The W 4f XPS spectra for RTO method and (b) for ISSG method



(a)





(b)

Fig. 4-13 (a) The Si 2p XPS spectra for RTO method and (b) for ISSG method

Chapter 5

The effect of H_2 content in ISSG system

5.1 Motivation

In last chapter, we found that the ISSG method has better oxidizing ability than RTO to form completed W-NCs and surrounding dielectric, so keeping stored charges from escaping to neighbor NCs by defects in surrounding oxide. The difference between them is that ISSG contains hydrogen (H_2) which RTO don't have during oxidation process. Some references also propose the increased content of H_2 could accelerate the oxidation rate on the content range of 0.5-2 % [5.1]. Besides, also some references have demonstrated that applying ISSG to deposit thin oxide film shows much better reliability properties than that of RTO [5.2]. The above references agree with our experimental results and arguments. Hence, we want to investigate the tendency or effect on our memory devices when the content of H_2 increases during ISSG oxidation process.

In this chapter, we oxidize trapping layer with 0% (RTO), 2%, 5%, 10%, 20%, 33% H_2 concentration in ISSG system fixed at 950°C 60s. all of these structures have the same ISSG tunneling oxide. The electrical measurements (C-V, I-V, reliability tests) and corresponding material analyses (TEM& XPS) are made for comparison.

5-2 The effect of H_2 content

5-2-1 Experimental Steps

Fig. 5-1 showed the schematic diagram of fabricating procedure. First, a single-crystal 8 inch (100) oriented p-type silicon wafer was chemically cleaned by standard RCA cleaning. Then, a 5-nm-thick thermal oxide was grown on p-type Si substrate by in situ steam generation (ISSG) as a tunnel oxide. Then, we deposited a tungsten silicide film(WSi_2) which has thickness of 4nm by low pressure chemical vapor deposition furnace(LPCVD). Subsequently, a 6-nm-thick amorphous silicon (a-Si) was also deposited by the same system. After finishing WSi_2/a-Si double layer structure, we used ISSG system to oxidize trapping layer at 950°C 60s. This procedure was executed to let WSi_2 precipitate tungsten nanocystals and form silicon

oxide as its surrounding dielectric. On oxidizing trapping layer process, the H_2 concentration was adjusted from 0% to 33%. There are five different H_2 contents, 0% (RTO), 2%, 5%, 10%, 20%, 33%, and labeled as structure 1 , 2, 3, 4, 5, respectively. We want to investigate the effect and tendency of different H_2 concentration on oxidizing trapping layer. Afterward, a followed 50nm silicon oxide was deposited by PECVD system to form an enough thick control oxide. Finally, the Al gate electrode was deposited by the use of thermal coater and then patterned.

The electrical characteristics, such as capacitance-voltage (C-V), and current density-voltage (J-V) were measured by Keithley 4200 and HP4284 Precision LCR Meter with frequency of 100 kHz. The material analysis, for instance, transmission electron microscopy (TEM) and XPS, were made to assist us in micro-structure analysis.

5-2-2 Results and discussions

(A) C-V measurements & TEM analysis

In this subject, we investigate the H_2 content in ISSG system how to influence the oxidation of trapping layer and its corresponding electrical characteristics. There are five different H_2 contents during oxidizing trapping layer process, 0% (RTO), 2%, 5%, 10%, 20%, 33%, and labeled as structure 1 , 2, 3, 4, 5, respectively. First, fig. 5-2(a) shows the capacitance-voltage hysteresis (C-V) of structure 1. It has a smaller memory windows, 5V, under V_G-V_{FB}=10V bidirectional voltage sweep. On the other hand, fig. 5-2(b) exhibits its cross-section TEM analysis. We could see this trapping layer form discrete nanocrystals. The C-V hysteresis of structure 2 is shown in fig. 5-3(a). It has a larger memory window of 9V, and from the cross-section TEM image, fig. 5-3(b), we could see this trapping layer form more discrete nanocrystals with the size of about 9nm. The C-V hysteresis of structure 3, fig. 5-4(a), shows it has a large memory window of 10V . Its image of TEM, fig. 5-4(b), reveals the nearly same size of NCs as that of structure 2. However, when the H_2 content increases above 10% to 33%, it could be found that the structure 3, 4, 5 almost have no memory windows even under V_G-V_{FB}=15V bidirectional voltage sweep, fig. 5-5(a), fig. 5-6(a) and fig. 5-7(a). The TEM images exhibit they are similar to each other. All of these three structures don't have discrete enough W-NCs like that of structure 2 or 3, fig. 5-5(b), fig. 5-6(b) and fig. 5-7(b). The structure 1, 2, and 3 have enough C-V memory windows to define"1"and"0"states.

(B) Reliability tests (retention & endurance)

In this theme, we describe the retention and endurance measurements for these five structures with different H_2 content in ISSG system. The stress conditions performed to our retention and endurance test here are the same as those at subjects mentioned before. Fig. 5-8(a) reveals the retention property for structure 1. The memory window of structure 1 gradually and continually decays on the whole retention process. Finally, the memory window remained about 0.44V (charge remained ratio is about 22%) after 1000 seconds. Fig. 5-9(a) shows the characteristics of retention measurements for structure 2. The retention of structure 2 is steady after initial decay. Finally, the memory window remained 0.92V (charge remained ratio is about 42%) after 1000 seconds. The retention of structure 3, fig. 5-10(a), exhibits that it becomes steady quickly after only several ten seconds, and we found the storage for hole is steady and has nearly no loss during the process. Hence, the memory window could remained about 1.1V (charge remained ratio is about 55%) after 1000 seconds. The endurance tests for structure 1, 2, 3 reveals their memory window could be maintained after 10^6 cycles P/E operations, Fig. 5-8(b), Fig. 5-9(b), and Fig. 5-10(b). The structure 4, 5, 6 have no memory window under V_G-V_{FB}=10,15V bidirectional voltage sweep, and their C-V properties would be abnormal under higher voltage sweep than 15V. Therefore, we don't measure their reliability tests such as retention and endurance.

(C)Material analysis and Discussion

We found that the samples whose trapping layers oxidized by ISSG with low H_2 content (2% and 5%) could have large enough memory window, 9V and 10V, to define"1"and"0"states, fig. 5-3(a), fig. 5-4(a). The sample with trapping layer oxidized by RTO (0%) has smaller memory window compared with samples which has 2% and 5% H_2 content during oxidation process, but it still has 4.5V memory window to differentiate between 1"and"0"states. However, when we increase H_2 content in ISSG system above 10% to 33%, those samples with 10%, 20%, 33% nearly have no memory window. Hence, there are two tendencies for the relation between memory window and H_2 content. At low H_2 concentration rang, the higher H_2 content is, the larger memory window it has. When the trapping layer of samples oxidized with higher H_2 concentration above 10%, they don't have memory window. So we separate this subject into two parts to discuss. One part is for low H_2 concentration (0%, 2% and 5%), and the other is for high H_2 content (10%, 20%, 33%). The reliability measurements for low H_2 concentration also show the trend that the added and increased H_2 content could improve retention property. From W and Si

XPS analyses of samples with low H_2 content, fig. 5-11(a) and fig. 5-11(b), we observe the increased intensity of W-W and reduced intensities of Si-Si, W-Si peaks with increased H_2 content, so the higher H_2 concentration enhances the oxidation rate to form more W-NCs to storage charges. Besides, the peak of oxide shifts to higher energy also show stronger oxide bond produced and completely oxidized surrounding oxide avoids loss of charges through its defects. This is because the add of H_2 in oxidation process helps oxygen to dissociate to oxygen radicals, which enormously enhance oxidation rate (5.3). The higher H_2 content above 10% which causes no memory window and seldom discrete enough W-NCs let us guess too high H_2 concentration may obstruct the oxidation. Hence, we make a SIMS analysis, fig. 5-10(a), for samples with 2% and 33% H_2 content to investigate whether the high hydrogen content can retard the oxidation. From fig. 5-10(a), we observe the oxygen signal in trapping layer is larger for sample with 2% than sample with 33%. This result proves the expectation that too many H_2 can retard the oxidation.

5-3. Conclusions

The H_2 content split experiment shows two trends. For lower hydrogen concentration (from 0% to 5%), it is founded that ISSG shows better oxidizing ability for WSi2 and form oxide completely. But for hydrogen high content (from 10% to 33%), a continuous W metal layer is observed and the memory property disappears.

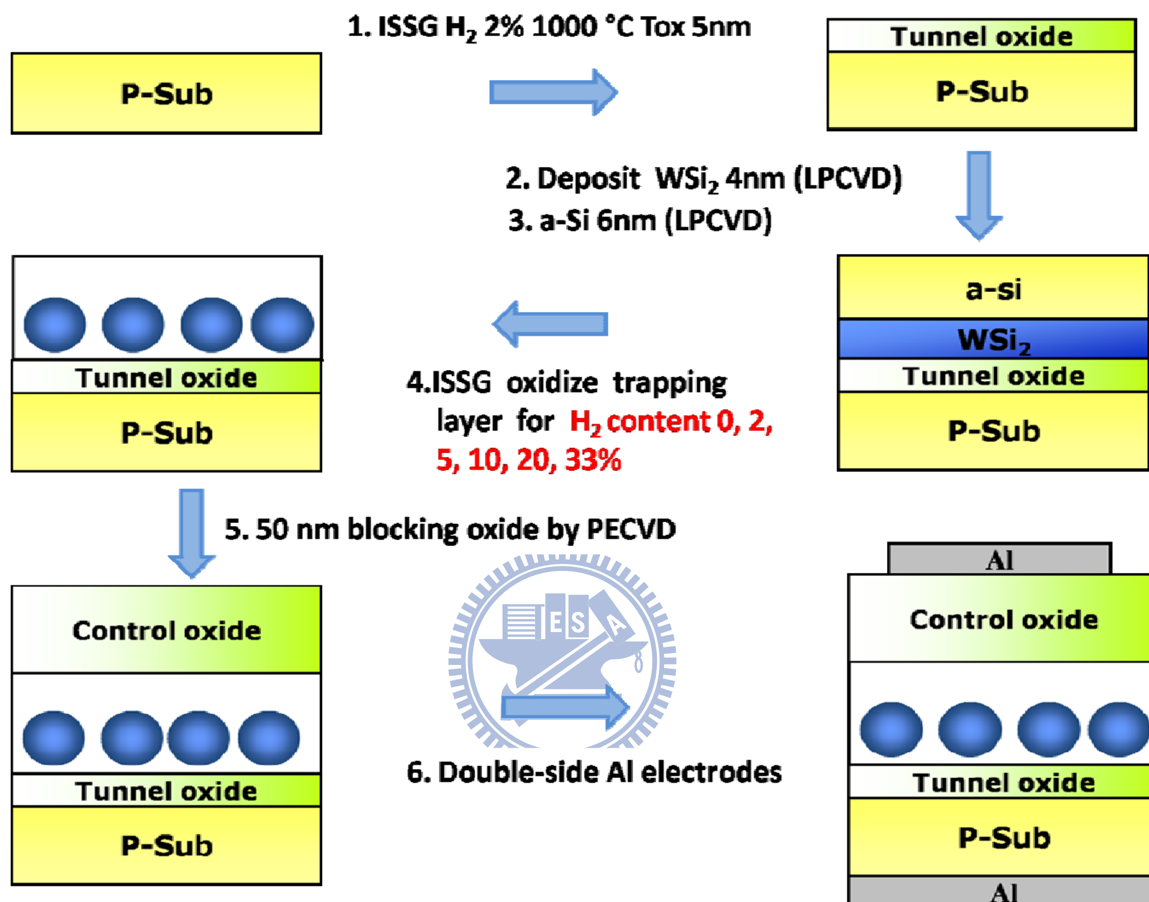
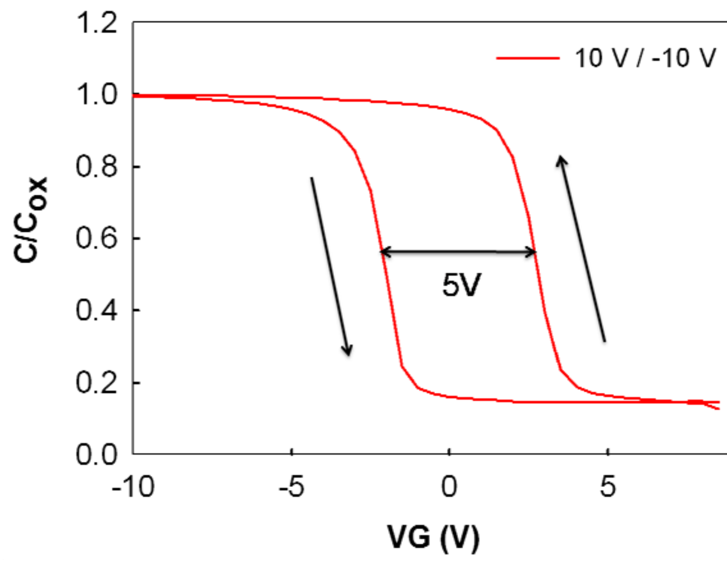
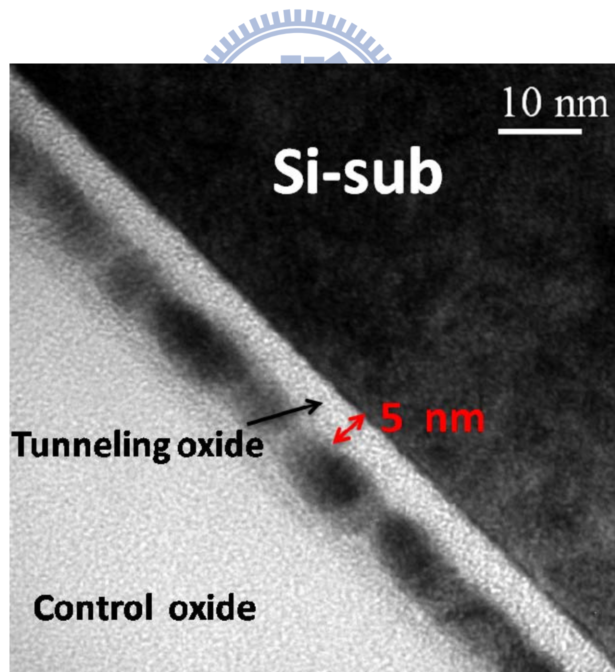


Fig. 5-1 The schematics of the experimental procedures for the H_2 content 0, 2, 5, 10, 20, 33%

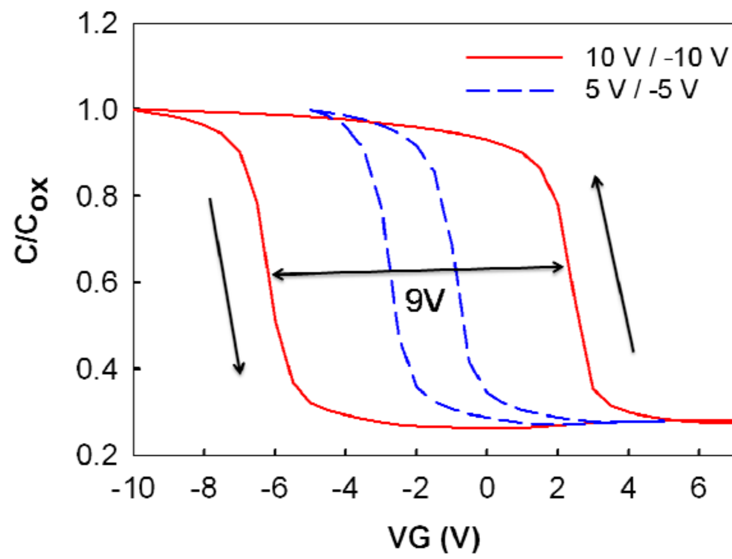


(a)

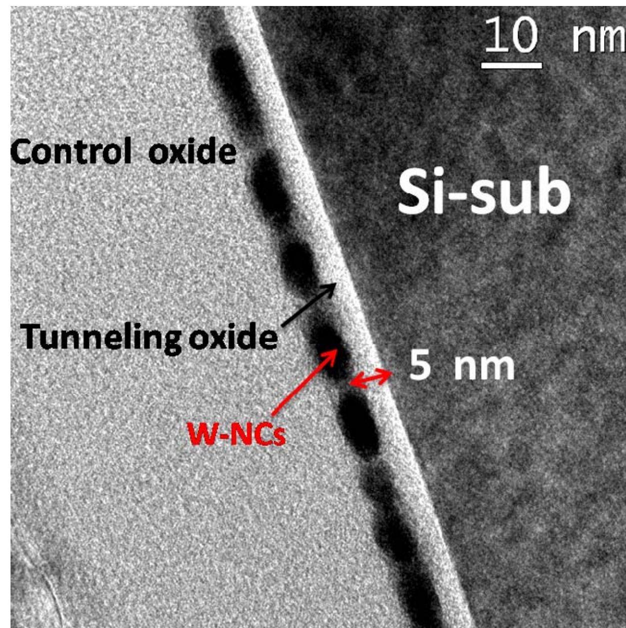


(b)

Fig.5-2 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 0% H_2 content

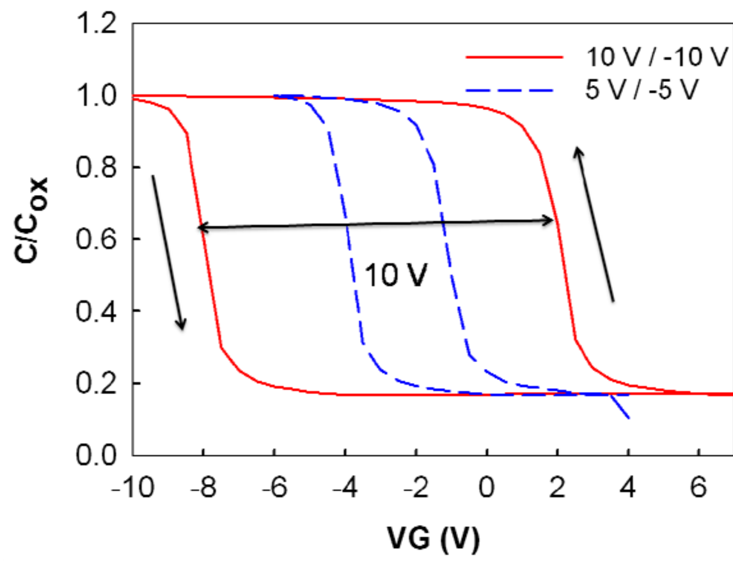


(a)

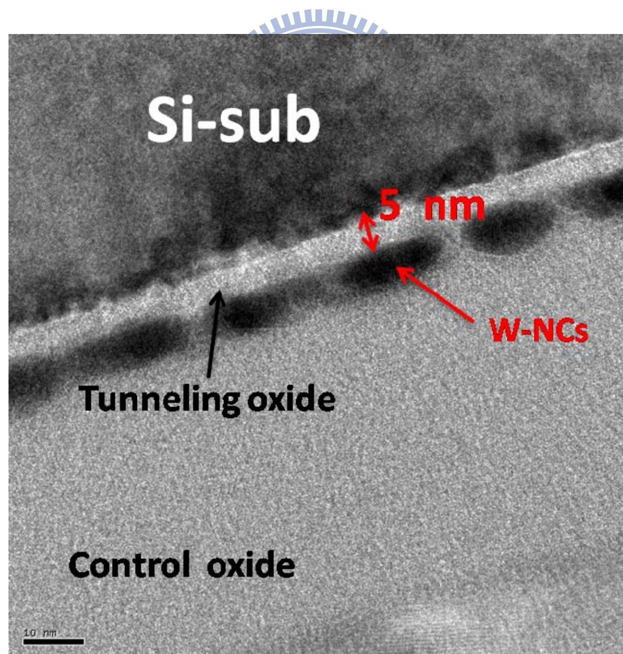


(b)

Fig.5-3 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 2% H_2 content

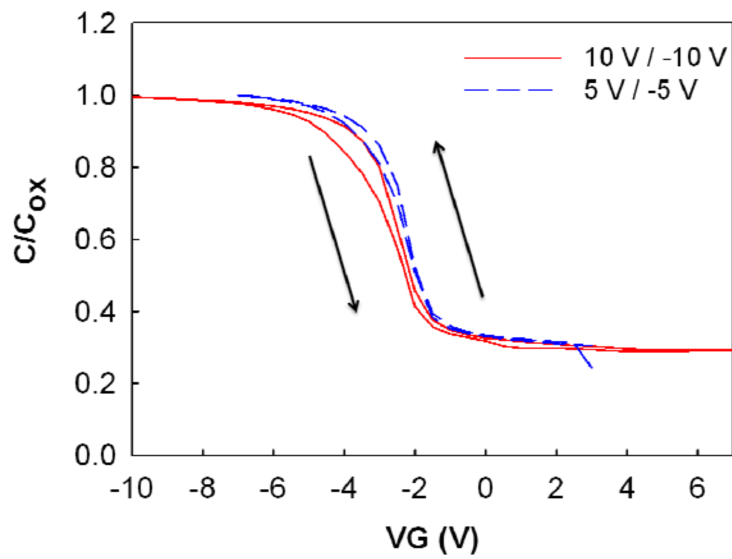


(a)

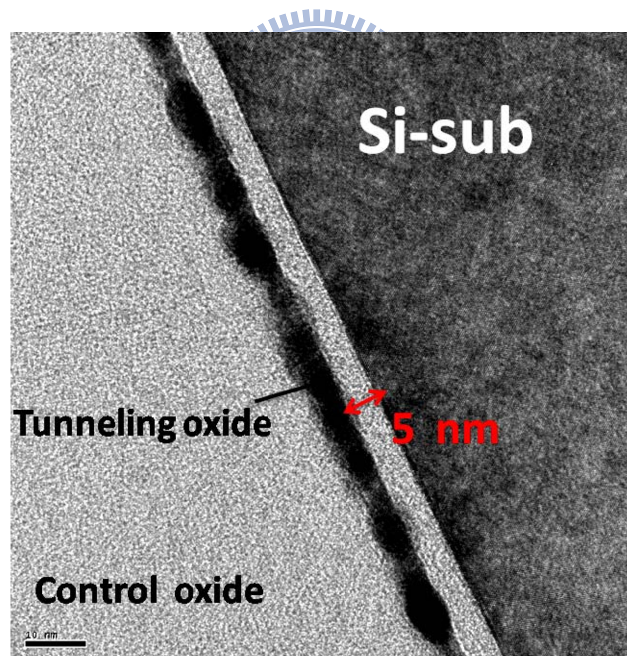


(b)

Fig.5-4 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 5% H_2 content

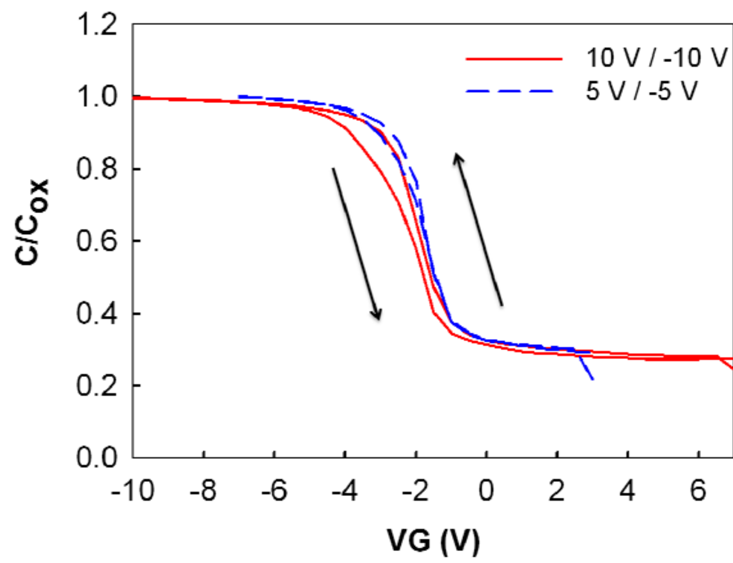


(a)

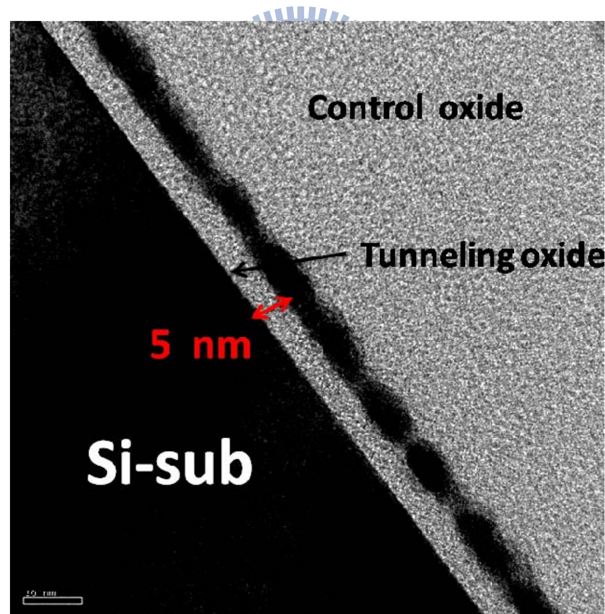


(b)

Fig.5-5 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 10% H_2 content

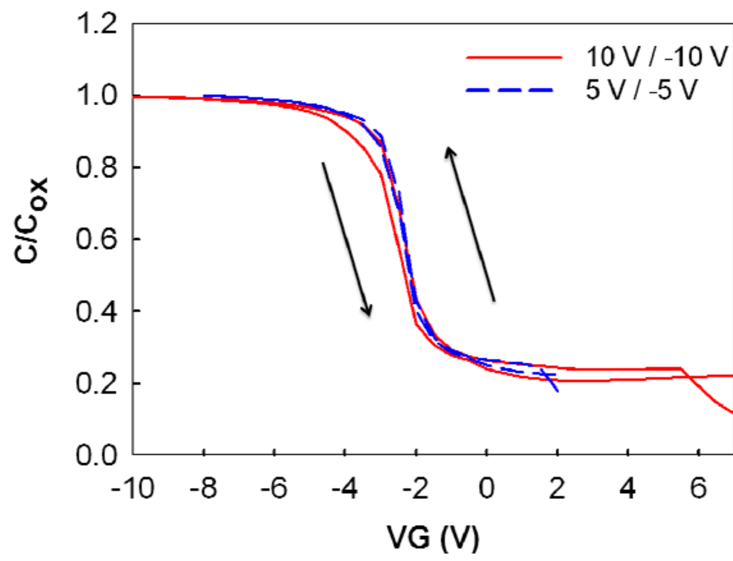


(a)

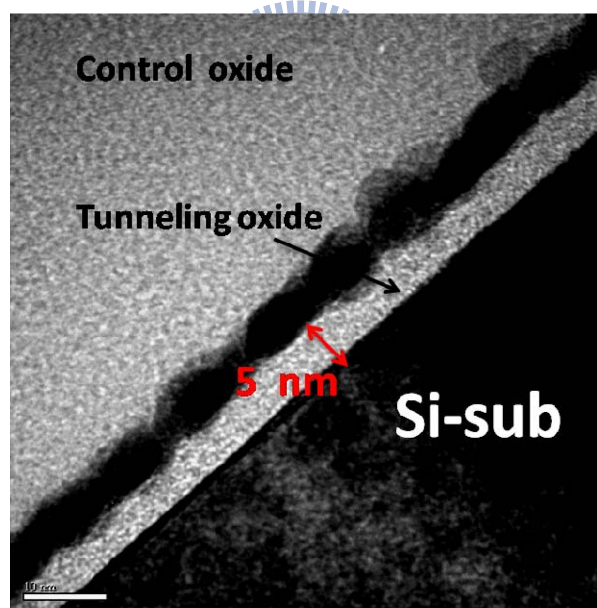


(b)

Fig.5-6 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 20% H_2 content

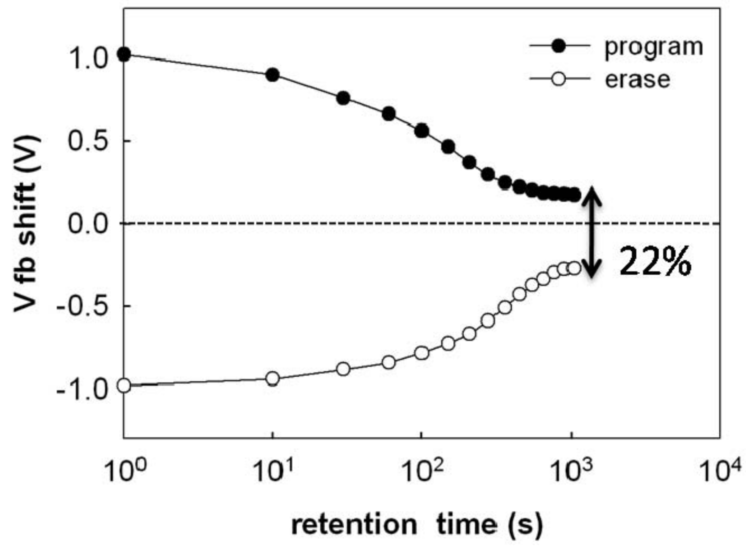


(a)

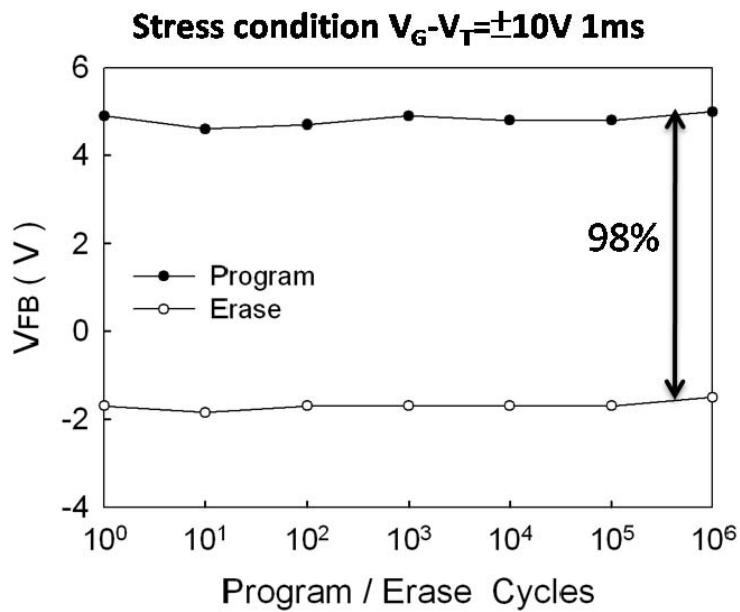


(b)

Fig.5-7 (a)The Capacitance-Voltage (C-V) hysteresis and (b) The Cross-sectional TEM image of 33% H_2 content

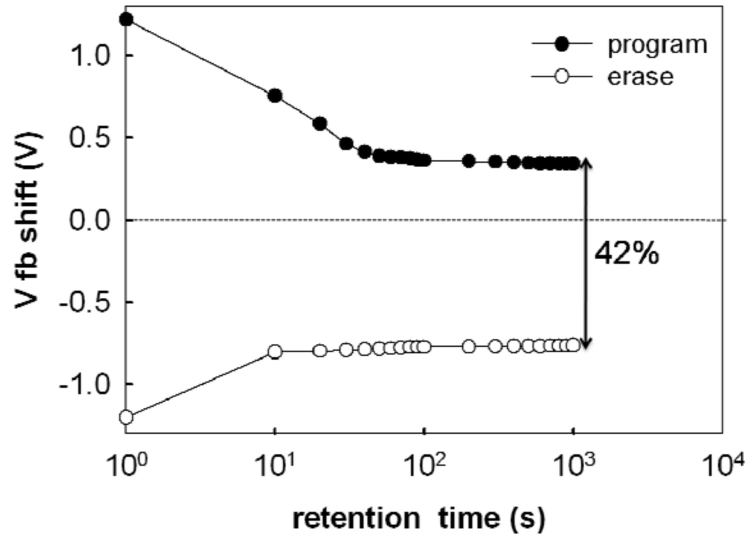


(a)

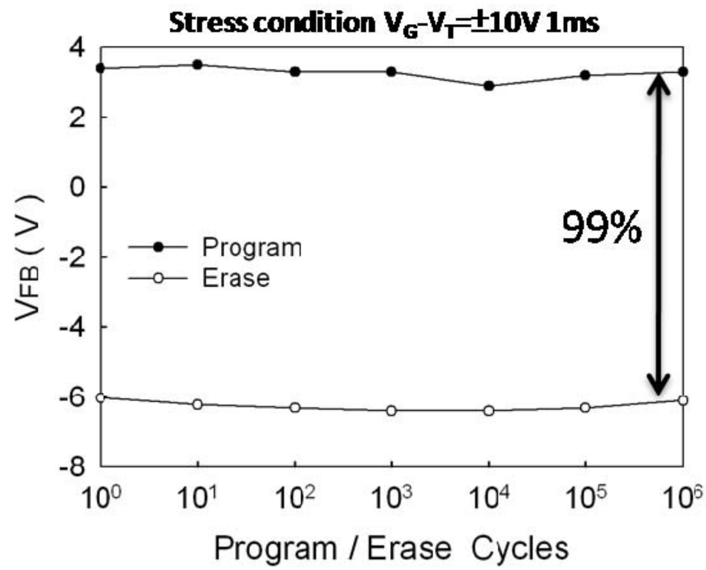


(b)

Fig.5-8 (a) The retention and (b) the endurance characteristics of 0% H_2 content

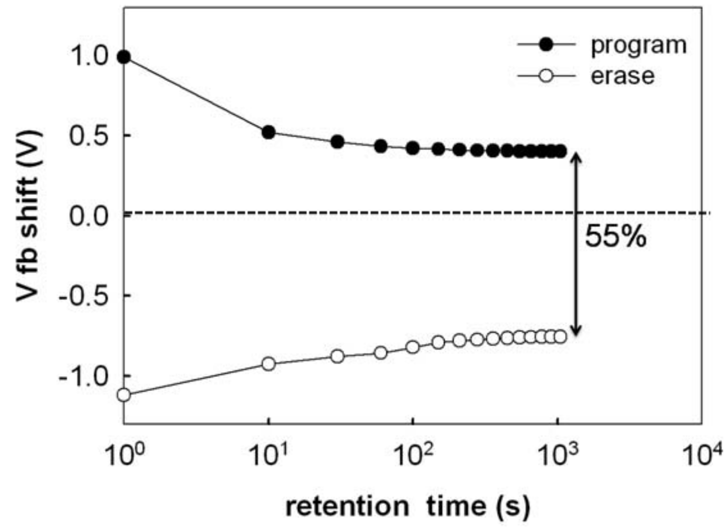


(a)

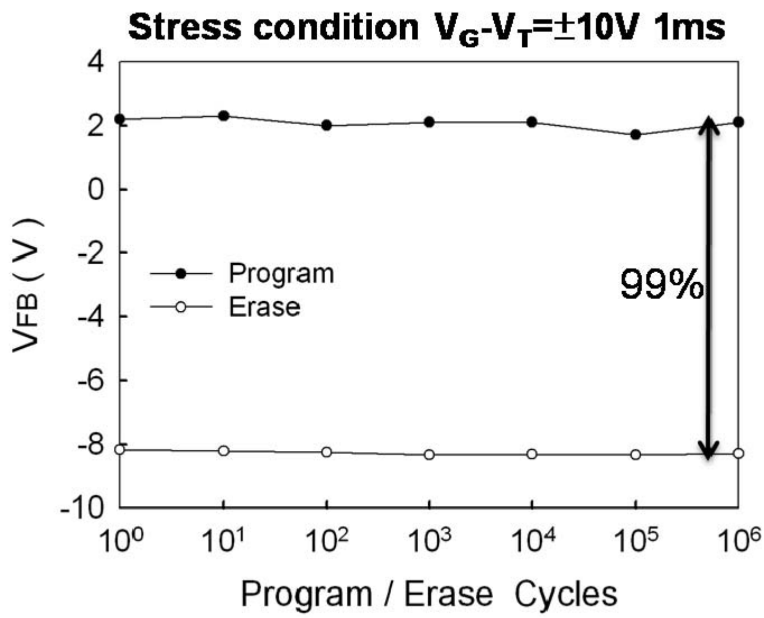


(b)

Fig.5-9 (a) The retention and (b) the endurance characteristics of 2% H_2 content



(a)



(b)

Fig.5-10 (a) The retention and (b) the endurance characteristics of 5% H_2 content

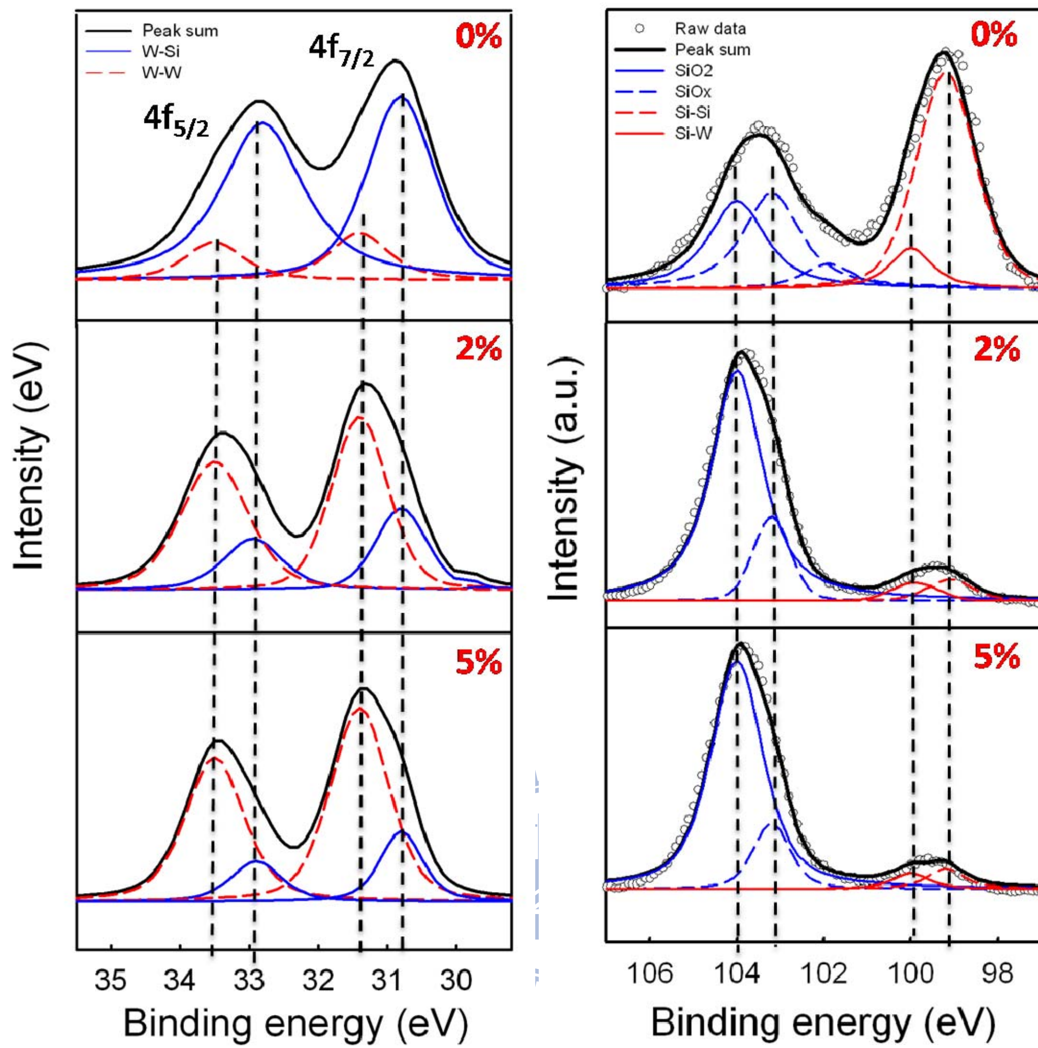


Fig. 5-11 (a) The W 4f XPS spectra and (b) Si 2p XPS spectra for 0,2, 5% H_2 content

Chapter 6
Conclusions

6-1. Conclusions.

1. The ISSG tunneling oxide has a better reliability than RTO tunneling oxide .

2. The ISSG method could oxidize WSi_2 more completely to form W-dot, and form oxide more completely. Therefore, it has a larger memory window and better retention property than RTO method.

3. The ISSG oxidation temperature should be increased to 950°C to form NCs ,but higher temperature (1050°C) may form larger NCs and degrade the tunneling oxide quality.

4. Longer ISSG oxidation time could oxidize WSi_2 more completely and results in better quality of oxide. Therefore, it shows better retention property for longer oxidation time.

5. The H_2 content split experiment shows two trends, For lower hydrogen concentration (from 0% to 5%), it is founded that ISSG shows better oxidizing ability for WSi2 and form oxide completely. But for hydrogen high content (from 10% to 33%), a continuous W metal layer is observed and the memory property disappears.

Reference

Chapter 1

[1.1] S. Lai, Future Trends of Nonvolatile Memory Technology, December 2001.

[1.2] S. Aritome, IEEE IEDM Tech. Dig., 2000, p.763.

[1.3] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells—An overview" *Proc. IEEE*, vol. 85, pp. 1248–1271, Aug. 1997.

[1.4] Roberto Bez, Emilio Camerlenghi, Alberto Modelli, and Angelo Visconti, "Introduction to Flash Memory" *Proc. IEEE*, vol. 91, NO.4, April 2003.

[1.5] D. Kahng and S. M. Sze, "A floating gate and its application to memory devices", *Bell Syst. Tech,* 46, 1288 (1967).

[1.6] J. D. Blauwe, "Nanocrystal nonvolatile memory devices", *IEEE Transaction on Nanotechnology*, 1, 72 (2002).

[1.7] M. H. White, Y. Yang, A. Purwar, and M. L. French, "A low voltage SONOS nonvolatile semiconductor memory technology", *IEEE Int'l Nonvolatile Memory Technology Conference*, 52 (1996).

[1.8] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE circuits & devices*, 16, 22 (2000).

[1.9] H. E. Maes, J. Witters, and G. Groeseneken, *Proc. 17 European Solid State Devices Res. Conf. Bologna 1987*, 157 (1988).

[1.10] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, "Volatile and non-volatile memories in silicon with nano-crystal storage", *IEEE Int. Electron Devices Meeting Tech. Dig.*, 521 (1995).

[1.11] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee, "Room temperature operation of a quantum-dot flash memory", *IEEE Electron Device Lett.*, 18,

278 (1997).

[1.12] Y. C. King, T. J. King, and C. Hu, “MOS memory using germanium nanocrystals formed by thermal oxidation of $Si_{1-x}Ge_x$”, *IEEE Int. Electron Devices Meeting Tech. Dig*., 115 (1998).

[1.13] H.A.R. Wegener, A.J. Lincoln, H.C. Pao, M.R. O’Connell, and R.E. Oleksiak, The variable threshold transistor, a new electrically alterable, non-destructive read-only storage device,” *IEEE IEDM Tech. Dig*., Washington, D.C., 1967.

[1.14] T.Y.Chan, K.K.Young and C.Hu, “A true single-transistor oxide- nitride-oxide EEPROM device”. *IEEE Electron Device Letters*, vol.8, no.3, pp.93-95, 1987.

[1.15] M.K. Cho and D.M.Kim, “High performance SONOS memory cells free of drain turn-on and over-erase: compatibility issue with current flash technology”, *IEEE Electron Device Lett*ers, pp.399-401, Vol.21, No.8, 2000.

[1.16] I. Fijiwara, H.Aozasa, K.Nomoto, S.Tanaka and T.Kobayashi, “ High speed program/erase sub 100nm MONOS memory cell”, *Proc. 18th Non-Volatile Semiconductor Memory Workshop*, p. 75, 2001.

[1.17] H. Reisinger, M. Franosch, B. Hasler, and T. Bohm, *Symp. on VLSI Tech. Dig.* , 9A-2, 113 (1997).

[1.18] C. Tung-Sheng, W. Kuo-Hong, C. Hsien, and K. Chi-Hsing, “Performance improvement of SONOS memory by bandgap engineering of charge-trappinglayer”, *IEEE Electron Device Lett.*, vol. 25, no. 3, pp.205–207, Mar. 2004.

[1.19] Y. N. Tan, W. K. Chim, and B. J. Cho, W. K. Choi, “Over-Erase Phenomenon in SONOS-Type Flash Memory and its Minimization Using a Hafnium Oxide Charge Storage Layer”, IEEE Transations on Eelectron Devices, vol.51, no.7, July 2004.

[1.20] Min She, Hideki Takeuchi, and Tsu-Jae King, “Silicon-Nitride as a Tunnel

Dielectric for Improved SONOS-Type Flash Memory", IEEE Electron Device Letters, vol. 24, no. 5, MAY 2003.

[1.21] Chang-Hyun Lee, Kyu-Charn Park, and Kinam Kim, "Charge-trapping memory cell of SiO_2/SiN/high-*k* dielectric Al_2O_3 with TaN metal gate for suppressing backward-tunneling effect", Applied Physics Letters 87, 073510 (2005)

[1.22] Shih-Ching Chen, Ting-Chang Chang, Po-Tsun Liu, Yung-Chun Wu, and Ping-Hung Yeh, "Nonvolatile polycrystalline silicon thin-film-transistor memory with oxide/nitride/oxide stack gate dielectrics and nanowire channels", Applied Physics Letters 90, 122111 (2007)

[1.23] Peiqi Xuan, Min She, Bruce Harteneck, Alex Liddle, Jefkey Bokor, and Tsu-Jae King, "FinFET SONOS Flash Memory for Embedded Applications", IEEE IEDM 609-612 (2003).

[1.24] Tzu-Hsuan Hsu, Hang Ting Lue, Ya-Chin King, Jung-Yu Hsieh, Erh-Kun Lai, Kuang-Yeu Hsieh, and Chih-Yuan Lu, "A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory", IEEE Electron Device Letters, vol. 28, no. 5, MAY 2007.

[1.25] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and Doug Buchanan, IEDM Tech. Dig., p.521 (1995)

[1.26] J De Blauwe, "Nanocrystal nonvolatile memory devices", IEEE Trans. Nanotechnol, 2002.

[1.27] R. Ohba, N. Sugiyama, K. Uchida, J. Koga, and A. Toriumi, IEEE Trans. Electron Devices **49**, 1392 (2002).

[1.28] Y. C. King, T. J. King, and C. Hu, IEEE Trans. Electron Devices **48**, 696 (2001)

[1.29] Y. Shi *et al.*, in Proceedings of the First Joint Symposium on Opto- and Microelectronic Devices and Circuits, 2000, pp. 142–145.

[1.30] H. G. Yang, Y. Shi, S. L. Gu, B. Shen, P. Han, R. Zhang, and Y. D. Zhang, Microelectron. J. **34**, 71 (2003).

[1.31] Zengtao Liu, Chungho Lee, Venkat Narayanan, Gen Pei, and Edwin Chihchuan Kan, "Metal Nanocrystal Memories—Part I: Device Design and Fabrication", IEEE Trans. Electron Devices, VOL. 49, NO. 9, SEPTEMBER 2002.

[1.32] Chungho Lee, Udayan Ganguly, Venkat Narayanan, and Tuo-Hung Hou, "Asymmetric Electric Field Enhancement in Nanocrystal Memories", IEEE Eelectron Electron Letters, vol. 26, NO. 12, DECEMBER 2005.

[1.33] Jong Jin Leea, Yoshinao Harada Jung, Woo Pyun, and Dim-Lee Kwong "Nickel nanocrystal formation on HfO2 dielectric for nonvolatile memory device applications", Applied Physics Letters 86, 103505 (2005)

[1.34] Wei-Ren Chen, Ting-Chang Chang, Po-Tsun Liu, Po-Sun Lin, Chun-Hao Tu, and Chun-Yen Chang "Formation of stacked Ni silicide nanocrystals for nonvolatile memory application", Applied Physics Letters 90, 112108 (2007)

[1.35] S. K. Samanta, Won Jong Yoo, and Ganesh Samudra, "Tungsten nanocrystals embedded in high-*k* materials for memory application", Applied Physics Letters 87, 113110 (2005)

[1.36] S. K. Samanta, P. K. Singh, Won Jong Yoo, Ganesh Samudra, and Yee-Chia Yeo, "Enhancement of Memory Window in Short Channel Non-Volatile Memory Devices Using Double Layer Tungsten Nanocrystals", IEEE (2005)

[1.37] Shan Tang, Chuanbin Mao, Yueran Liu, and Sanjay K. Banerjee "Protein-Mediated Nanocrystal Assembly for Flash Memory Fabrication", IEEE Trans. on Electron Letters, vol. 54, no. 3, March 2007.

[1.38] L. Guo, E. Leobandung, and S. Y. Chou, "Si single-electron MOS memory with nanoscale floating-gate and narrow channel," in *Int. Electron Devices Meeting Tech. Dig.*, 1996, pp. 955–956.

[1.39] N. Takahashi, H. Ishikuro, and T. Hiramoto, “A directional current switch using silicon electron transistors controlled by charge injection into silicon nano-crystal floating dots,” in *Int. Electron Devices Meeting Tech. Dig.*, 1999, pp. 371–374.

[1.40] J. Wahl, H. Silva, A. Gokirmak, A. Kumar, J. J. Welser, and S. Tiwari, “Write, erase and storage times in nanocrystal memories and the role of interface states,” in *Int. Electron Devices Meeting Tech. Dig.*, 1999, pp. 375–378.

Chapter 2

[2.1] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, “Flash Memory Cells—An Overview,” Proc. of The IEEE, 85, 1248 (1997).

[2.2] M. Woods, “Nonvolatile Semiconductor Memories: Technologies, Design, and Application,” C. Hu, Ed. New York: IEEE Press, (1991) ch. 3, p.59.

[2.3] P. E. Cottrell, R. R. Troutman, and T. H. Ning, “Hot-electron emission in n-channel IGFET’s”, IEEE J. Solid-State Circuits, vol. 14, pp. 442-455 (1979).

[2.4] J. Bu, M. H. White, “Design considerations in scaled SONOS nonvolatile memory,” Solid-State Electron., 45, 113 (2001).

[2.5] M. L. French, M. H. White., “Design considerations in scaled SONOS nonvolatile memory devices,” Solid-State Electron., p.1913 (1995).

[2.6] M. L. French, C. Y. Chen, H. Sathianathan, M. H. White., “Design and scaling of a SONOS multidielectric device for nonvolatile memory applications,” IEEE Trans. Comp. Pack. and Manu. Tech. part A., 17, 390 (1994).

[2.7] Y. Wang , M. H. White, “An analytical retention model for SONOS nonvolatile memory devices in the excess electron state,” Solid-State Electron., p.97 (2005).

[2.8] Y. S. Hisamune, K. Kanamori, T. Kubota, Y. Suzuki, M. Tsukiji, E. Hasegawa,

A. Ishitani, and T. Okazawa," A high capacitive-coupling ratio (HiCR) cell for 3 V-only 64 Mbitand future flash memories," IEDM Tech. Dig., p.19 (1993).

[2.9] J. Moll, "Physics of Semiconductors," New York: McGraw-Hill, (1964).

[2.10] M. Lezlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO_2," J. Appl. Phys., 40, 278 (1969).

[2.11] "IEDM 90 short course: Non-volatile memory," IEEE, San Francisco, CA, 1990.

[2.12] C. Sevensson and I. Lundstrom, "Trap-assisted charge injection in MNOS structures," J. Appl. Phys., 44, 4657 (1973).

[2.13] I. C. Chen, C. Kaya, and J. Paterson, "Band-to-band tunneling induced substrate hot-electron (BBISHE) injection : a new programming mechanism for nonvolatile memory devices," IEDM Tech. Dig., p.263 (1989).

[2.14] I. C. Chen, C. Kaya, and J. Paterson, "Gate current injection initiated by electron band-to-band tunneling in MOS devices," IEDM Tech. Dig., p.263 (1989).

[2.15] T. Ohnakado, K. Mitsunaga, M. Nunoshita, H. Onoda, K. Sakakibara, N. Tsuji, N. Ajika, M. Hatanaka and H. Miyoshi, "Novel electron injection method using band-to-band tunneling induced hot electrons (BBHE) for flash memory with a P-channel cell," IEDM Tech. Dig., p.279 (1995).

[2.16] T. Ohnakado, K. Mitsunaga, M. Nunoshita, H. Onoda, K. Sakakibara, N. Tsuji, N. Ajika, M. Hatanaka and H. Miyoshi, IEDM Tech. Dig., p.279 (1995).

[2.17] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to Flash Memory," Proc. of the IEEE., 91, 489 (2003).

[2.18] K. Kim, J. Choi, "Future Outlook of NAND Flash Technology for 40nm Node and Beyond," Proc. IEEE NVSMW, p.9 (2006).

[2.19] P. Cappelletti, R. Bez, D. Cantarelli, and L. Fratin, "Failure mechanisms of

flash cell in program erase cycling," IEDM Tech. Dig., p.291 (1994).

[2.20] D. Ielmini, A. Spinelli, A. Lacaita, and A. Modelli, "Statistical modeling of reliability and scaling projections for flash memories," IEDM Tech. Dig., p.32.2.1 (2001).

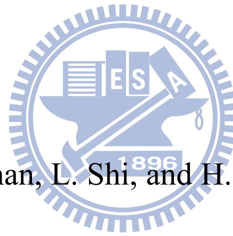
[2.21] D. Ielmini, A. S. Spinelli, A. L. Lacaita, L. Confalonieri, and A. Visconti, Proc. IRPS, p.73 (2001).

[2.22] D. Ielmini, A. S. Spinelli, A. L. Lacaita, R. Leone, and A. Visconti, Proc. IRPS, p.1 (2002).

[2.23] Y. M. Niquet, G. Allan, C. Delerue and M. Lannoo," Quantum confinement in germanium nanocrystals," Appl. Phys. Lett., 77, 1182 (2000).

[2.24] T. Takagahara and K.Takeda, Phys. Rev. B, vol.46, p.15578 (1992).

Chapter 3



[3.1] S. Tiwari, F. Rana, K. Chan, L. Shi, and H. hanafi, Appl. Phys. Lett. 69, 1232 (1996)

[3.2] Z. Liu, C.Lee, V. Narayanan, G Pei, and E. C. Kan, "Metal nanocrystal Memory-Part I: Device Design and Fabrication", IEEE Tran Electron Devices, vol.49, pp. 1606 (2002)

[3.3] G .D. Wilk, and B. Brar, "Electrical Characteristics of High-Quality Sub-2.5nm Oxide Grown by Ultraviolet Ozone Exposure at Low Temperature. ", IEEE Electron Device Lett., vol. 20, no. 3, p. 132-134, 1999.

[3.4] M. Nagamine, H. Itoh, H. Satake, and A. Toriumi, "Radical Oxygen Process for Highly Reliable SiO_2 with Higher Film-Density and Smoother SiO_2/Si Interface. ", IEDM Tech. Digest, p. 593-596, 1998.

[3.5] S. Ikeda, M. Okihara, H. Uchida, and N. Hirashita, "Cross-sectional Transmission Electron Microscope Studies on Intrinsic Breakdown Spots of Thin Gate Oxide.", Jpn. J. Appl. Phys., vol. 36, (1997) Pt. 1, no. 5A,

p.2561-2564.

[3.6] N. Kimizuka, T. Yamamoto and T. Mogami, "A New Degradation Scheme for Direct-tunneling Ultrathin Gate Dielectric.", VLSI Tech. Symp., p. 162-163,1998.

[3.7] K. Eriguchi, Y. Harada, and M. Niwa, "Influence of 1nm-Thick Structural Strained-Layer near SiO_2/Si Interface on Sub-1nm-Thick Gate Oxide Reliability", IEDM Tech. Digest, p. 175-178, 1998.

[3.8] K.G. Reid, H. Tseng, R. Hegde, G. Miner, and G.C. Xing, "Dilute Steam Rapid Thermal Oxidation for 3nm Gate Oxides", Electrochem. Soc. Symp. Proc., 99-10)p. 23-30 (1999)

[3.9] S. K. Samanta, W. J. Yoo, G. Samudra, E. S. Tok, L. K. Bera, and N. Balasubramanian, "Tunsten nanocrystals embedded in high-k materials for memory aaplication", Applied Physics Letters.,vol. 87, Art. No. 113110 (2005)

[3.10] M. Takata, S. Kondoh, T. Sakaguchi, H. Choi, J. C. Shim, H. Kurino, and M.Koyanagi, Tech. Dig. –Int. Electron Devices Meet. 2003, 553.

[3.11] K. Akimoto, "Chemical Bonding of W-Si Compounds.", Appl. Phys. Lett. 41(1), 1978.

[3.12] C. M. Lin, J. S. Chen, "The Influence of Si Content on the Work Function of $W_{1-x}Si_x$ (x<14 atom %) Gate Electrodes. ", Electrochemical and Solid-State Letters, 11 (4) H99-H102 (2008)

Chapter 4

[4.1] T. Y. Lou, M. Laughery, G. A. Brown, ”Effect of H_2 Content on Reliability of Ultrathin In-Situ Steam Generated (ISSG) SiO_2. ”, IEEE Electron Device Letters, vol. 21, no. 9, 2000.

[4.2] T. Y. Lou, H. N. Al-Shareef, G. A. Brown, M. Laughery, V.H.C. Watt, ”Correlation between the Reliability of Ultra-Thin ISSG SiO_2 and Hydrogen Content. ”, In Challenges in Process Integration and Device Technology, vol. 4181 (2000).

Chapter 5

[5.1] T. Y. Lou, M. Laughery, G. A. Brown, ”Effect of H_2 Content on Reliability of Ultrathin In-Situ Steam Generated (ISSG) SiO_2. ”, IEEE Electron Device Letters, vol. 21, no. 9, 2000.

[5.2] D. Brazzelli, G. Ghidini, B. Crivelli, R. Zonca, M. Bersani, ”High Quality Thin Oxynitride by RTP Annealing of IN Situ Steam Generation Oxides for Flash Memory Applications. ”, Solid-State Electronics 45 (2001).