國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

以四埠散射參數量測射頻金氧半電晶體特性並製作其高頻等效電路模型

Characterization and Modeling of RF MOSFET's Based on Four-Port Scattering-Parameter Measurement

研 究 生 ：吳師道

指導教授 ：張俊彥 博士

中華民國 九十四 年 七 月

以四埠散射參數量測射頻金氧半電晶體特性並製作其高頻等效電路模型

Characterization and modeling of RF MOSFET's Based on Four-Port Scattering-Parameter Measurement

研 究 生：吳師道　　　　Student：Shih-Dao Wu

指導教授：張俊彥 博士　　　　Advisor：Dr. Chun-Yen Chang

國立交通大學

電子工程學系 電子研究所

博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering & Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
In Electronics Engineering
June 2005
Hsinchu, Taiwan, Republic of China

中華民國九十四年六月

以四埠散射參數量測射頻金氧半電晶體特性並製作其高頻等效電路模型

學生：吳師道　　　　　　　　　　　　　　　　指導教授：張俊彥 博士

國立交通大學 電子工程學系 電子研究所

摘　　要

先進的互補金氧半製程使得射頻金氧半電晶體成為製造快速成長的無線通訊產品的候選者之一，以金氧半電晶體設計無線通訊電路，將有希望把無線通訊系統中的前端射頻模組、基頻電路、數位處理電路三部分整合在單一晶片中，如此不但可降低生產成本，也增加了通訊產品的可攜性。然而以金氧半電晶體設計射頻電路具有一定的挑戰性，因為元件內部會產生複雜的訊號耦合，特別是基板的部分，因此提供可以準確預測元件高頻特性的元件模型供電路設計者使用，是當前的要務。傳統雙埠量測方式並無法有效的完整探測四端點金氧半電晶體特性，通常必須將金氧半電晶體設定為共源組態，將源極和基板連接在一起並接地，以配合雙埠量測系統，如此將無法量測源極與基板之間的訊號耦合效應，也無法將汲極與基板間的耦合效應從汲極的輸出特性中分離。本論文提出並實現了以四埠散射參數在晶量測金氧半電晶體的量測方式。

在本論文中，首先重新整理基本的單埠散射參數原理，並將其觀念延

伸至多埠的應用，另外也簡介了本研究所使用的四埠參數量測系統及其校正的原理。

接著提出了四埠量測所使用的在晶量測結構，包括了去除量測結構本身寄生效應的傀儡結構，並發展了去除量測結構寄生效應的方法。利用這些四埠測試結構，實現了以四埠參數量測射頻電晶體的構想，一次的四埠參數量測，即可獲得電晶體操作在共源、共閘、共汲的高頻特性。

此外本論文也提出了具有合理基板電容電阻寄生元件的金氧半電晶體小訊號等效電路模型，並根據四埠量測所得的金氧半電晶體高頻特性，發展粹取小訊號等效電路模型中各元件參數值之方法，實驗中並粹取了不同尺寸的金氧半電晶體等效電路模型中的相關參數，粹取得隨元件尺寸縮小放大的模型參數。

最後，將小訊號等效墊路模型以及根據四埠量測資料粹取出的電路參數以電路模擬軟體模擬其輸出特性，並將此模擬特性與實際量測的高頻特性比較，在 100MHz 到 20GHz 的量測頻率範圍內，獲得優良的模擬結果。

Characterization and modeling of RF MOSFET's Based on Four-Port Scattering-Parameter Measurement

student：Shih-Dao Wu　　　　　　Advisors：Dr. Chun-Yen Chang

Department of Electronics Engineering and Institute of Electronics
National Chiao Tung University

ABSTRACT

With superior advancement of CMOS technologies, RF MOSFET's have become an important candidate for the rapid growing wireless communication applications. Communication applications base on COMS technologies are potential to integrate the RF front end, base-band and DSP module together on a single chip, which not only improve the production cost but also the portability of modern communication applications. However, designing RF circuit base on CMOS devices is a challenge since the complex signal coupling inside the device, especially the substrate coupling effect. Therefore, establishing a model accurately predicts the RF behaviors of CMOS devices is an urgent mission. The traditional two-port characterization method is inefficient to investigate the detail RF behavior of a four terminal MOSFET. The MOSFET is a device with four terminals and will be always arranged in two-port common source configuration with its source and body grounded to fit the traditional two-port measurement system. Tying the source and body together

will result in some consequences that the coupling path between the source and body will not be able to be characterized and the coupling between drain and body will not be able to separated from the output characteristics either.

In this thesis, the four-port S-parameter measurement was proposed and demonstrated for the usage of on-wafer characterization of RF MOSFET's.

First of all, the basic principles of one-port scattering parameter were reviewed and were extended for multi-port application. The four-port system was also introduced including the calibration methodology.

Next, the four-port test structures for characterizing RF MOSFET's including dummy structures were proposed. The corresponding de-embedding method was also developed. With the proposed test structures and MOSFET device, the RF characteristics of the MOSFET configured in common source, common gate, and common drain mode was characterized at one four-port measurement procedure.

Then, small-signal equivalent circuits with reasonable substrate R-C network for device in different operation mode were proposed and discussed. Extraction methods of the components in these equivalent circuits according to the four-port measurement data were deduced in detail. The extractions of the components for devices in different dimensions were also demonstrated, good scalability of the extracted values with the device dimensions was observed.

Finally, the output characteristics of the proposed small-signal equivalent circuits were simulated according to the components extracted from the four-port measurement. The simulated results were compared with the measurement data; good agreement of the Y-parameters from 100MHz to 20GHz was obtained, which suggest the feasibility of applying four-port on-wafer measurement for characterizing RF MOSFET's.

Contents

Chinese Abstract i

English Abstract iii

Figure Captions v

Table Captions xiii

Chapter 1 Introduction 1

Chapter 2 Multi-Port Scattering Parameters and Four-Port Measurement System 7

2.1 Introduction 7

2.2 Multi-Port Scattering Parameters 8

2.3 Four-Port Measurement System 16

2.3.1 Four-Port Measurement System 16

2.3.2 Calibration 16

2.4 Summary 18

Chapter 3 Characterizing RF MOSFET's by Four-Port Measurement 25

3.1 Motivation 25

3.2 Four-Port RF MOSFET's 26

3.3 Dummy Structures and De-Embedding Procedure 27

3.4 Four-Port Y-parameters and Port Reduction 29

3.5 Measurement Results and Discussions 30

3.5.1 Measurement Results of Devices with Different Dimensions 30

3.5.2 Two-Port Scattering Parameter of The Common Source, Common Drain, and Common Gate RF MOSFET,s 32

3.6 Summary 35

Chapter 4 Small-Signal Equivalent Circuit Model of RF MOSFET and Parameter Extraction 59

4.1 Motivation 59
4.2 Small-Signal Equivalent Circuits of RF MOSFET's 61
4.3 Parameter Extraction 64
4.3.1 Extraction of Extrinsic Parasitic Components in the Equivalent circuit of Cold MOSFET's 64
4.3.2 Extraction of Components in the Equivalent Circuit of MOSFET's in Linear Region 68
4.3.3 Extraction of intrinsic components in saturation region 69
4.4 Results and Discussions 72
4.4.1 Extractied Results of Cold Devices 73
4.4.2 Extracted Results of Devices Linear Region 74
4.4.3 Extracted Results of Saturation Devices 76
4.5 Summary 77
Chapter 5 Verification of Small-Signal Equivalent Circuit Model 135
5.1 Motivation 135
5.2 Simulation of the Equivalent Circuits 135
5.3 Results and Discussions 136
5.4 Summary 139
Chapter 6 Conclusion and Suggestions for Future Works 157
6.1 Conclusion of This Study 157
6.2 Suggestions for Future Works 158
References 159
Publication List 163

Figure Captions

Chapter 1

Fig.1.1 (a) Conventional two-port test structure for common source MOSFET.

(b) Fictional two-port test structure for common gate MOSFET.

(c) Fictional two-port test structure for common drain MOSFET.

Chapter 2

Fig.2.1 One port network.

Fig.2.2 Generator with conjugate matched load used to define “incident” components I_i and V_i.

Fig.2.3 An n-port network with generators.

Fig.2.4 Agilent N1957B Physical Layer Test System.

Fig.2.5 Architecture of VNA test ports and the systematic errors.

Fig.2.6 The full 4-port error model and the 48 error terms.

Chapter 3

Fig.3.1 (a) Schematics of test structure and the RF MOSFET.

(b) The top view photograph of the test structure and the RF MOSFET.

Fig.3.2 Test structure for the four-port measurement.

Fig.3.3 OPEN dummy structure for the four-port measurement.

Fig.3.4 The equivalent circuit of the test structure.

Fig.3.5 SHORT dummy structure for the four-port measurement.

Fig.3.6 The difference of input admittance at port2 (body signal pad) between the open dummy shown in Fig.3.3 and an ordinary open dummy without substrate contact ring.

Fig.3.7 S_{GG}, S_{DD}, S_{SS}, and S_{BB} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.8 S_{GB} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.9 S_{GD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.10 S_{GS} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.11 S_{BG} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.12 S_{BD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.13 S_{BS} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.14 S_{DG} and S_{SG} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.15 S_{DB} and S_{SB} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.16 S_{SD} and S_{DS} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

Fig.3.17 S_{GG} and S_{DD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common source configuration, which are biased at VG=VD=1V.

Fig.3.18 S_{DG} and S_{GD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common source configuration, which are biased at VG=VD=1V.

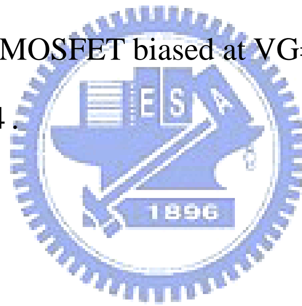
Fig.3.19 S_{GG} and S_{SS} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common drain configuration, which are biased at VG=VD=1V.

Fig.3.20 S_{GS} and S_{SG} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common drain configuration, which are biased at VG=VD=1V.

Fig.3.21 S_{SS} and S_{DD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common gate configuration, which are biased at VG=VD=1V.

Fig.3.22 S_{DS} and S_{SD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common gate configuration, which are biased at VG=VD=1V.

Fig.3.23 The common source S-parameters obtained from a 4-port NMOSFET and a conventional 2-port NMOSFET biased at VG=VD=1V. The gate widths of these two devices are $7.2\mu m\times 4$.



Chapter 4

Fig.4.1 The cross-sectional structure and top view of a four-terminal MOSFET.

Fig.4.2 The small signal equivalent circuit of a four-terminal RF MOSFET including the intrinsic and extrinsic parts.

Fig.4.3 The small signal equivalent circuit of a cold MOSFET, in which the intrinsic part of the MOSFET is neglected.

Fig.4.4 The small signal equivalent circuit of a cold MOSFET with RS and RD neglected.

Fig.4.5 The small signal equivalent circuit of a MOSFET biased in linear region.

Fig.4.6 The small signal equivalent circuit of a saturated MOSFET with the R_S and R_D neglected.

Fig.4.7 The measured Re[Y_{GG}] and Im[Y_{GG}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.8 The measured Im[Y_{DG}] and Im[Y_{SG}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.9 (a) The measured Im[Y_{BD}] and Im[Y_{BS}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

(b) The measured Re[Y_{BD}] and Re[Y_{BS}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.10 (a) The measured Im[Y_{GB}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

(b) The measured Re[Y_{GB}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.11 The extracted C_{GSO} and C_{GDO} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.12 -Im[Y_{SB}]/ω of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.13 The extracted C_{SBO} and C_{SBE} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.14 The extracted C_{DBO} and C_{DBE} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.15 The extracted C_{GBO} and C_{GBE} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.16 The extracted R_{SB} and R_{DB} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.17 The extracted R_{GB} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.18 The extracted R_{SDB} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

Fig.4.19 (a) The extracted C_{GS} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{GS} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{GS} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.20 (a) The extracted C_{GD} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{GD} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{GD} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.21 (a) The extracted $-Im[Y_{GB}]/\omega$ of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted $-Im[Y_{GB}]/\omega$ of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted $-Im[Y_{GB}]/\omega$ of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.22 (a) The extracted R_G of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted R_G of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted R_G of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.23 (a) The extracted $R_{CH}+R_S+R_D$ of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted $R_{CH}+R_S+R_D$ of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted $R_{CH}+R_S+R_D$ of M3($12\mu m \times 4$) biased at different V_G.

(d) $R_{CH}+R_S+R_D$ versus $(V_G - V_{TH})^{-1}$ of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$).

Fig.4.24 (a) The extracted C_{SB} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{SB} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{SB} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.25 (a) The extracted C_{SBE} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{SBE} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{SBE} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.26 (a) The extracted C_{DB} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{DB} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{DB} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.27 (a) The extracted C_{SBE} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{SBE} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{SBE} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.28 (a) The extracted C_{GB} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{GB} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{GB} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.29 (a) The extracted C_{GBE} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted C_{GBE} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{GBE} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.30 (a) The extracted R_{SB} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted R_{SB} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted R_{SB} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.31 (a) The extracted R_{DB} of M1($3.6\mu m \times 4$) biased at different V_G.

(b) The extracted R_{DB} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted R_{DB} of M3($12\mu m \times 4$) biased at different V_G.

Fig.4.32 (a) The extracted C_{GS} and C_{GD} of saturation M1($3.6\mu m \times 4$).

(b) The extracted C_{GS} and C_{GD} of saturation M2($7.2\mu m \times 4$)..

(c) The extracted C_{GS} and C_{GD} of saturation M3($12\mu m \times 4$).

Fig.4.33 (a) The extracted g_m and g_{mb} of saturation M1($3.6\mu m \times 4$).

(b) The extracted g_m and g_{mb} of saturation M2($7.2\mu m \times 4$).

(c) The extracted g_m and g_{mb} of saturation M3($12\mu m \times 4$).

Fig.4.34 (a) The extracted C_m and C_{mb} of saturation M1($3.6\mu m \times 4$).

(b) The extracted C_m and C_{mb} of saturation M2($7.2\mu m \times 4$).

(c) The extracted C_m and C_{mb} of saturation M3($12\mu m \times 4$).

Fig.4.35 (a) The extracted R_G of saturation M1($3.6\mu m \times 4$).

(b) The extracted R_G of saturation M2($7.2\mu m \times 4$).

(c) The extracted R_G of saturation M3($12\mu m \times 4$).

Fig.4.36 (a) The extracted C_{SB} and C_{DB} of saturation M1($3.6\mu m \times 4$).

(b) The extracted C_{SB} and C_{DB} of saturation M2($7.2\mu m \times 4$).

(c) The extracted C_{SB} and C_{DB} of saturation M3($12\mu m \times 4$).

Fig.4.37 (a) The extracted R_{SB} and R_{DB} of saturation M1($3.6\mu m \times 4$).

(b) The extracted R_{SB} and R_{DB} of saturation M2($7.2\mu m \times 4$).

(c) The extracted R_{SB} and R_{DB} of saturation M3($12\mu m \times 4$).

Chapter 5

Fig.5.1 (a) Measured and simulated Im[Y_{GG}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated R_E[Y_{GG}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.2 (a) Measured and simulated Im[Y_{DD}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated R_E [Y_{DD}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.3 (a) Measured and simulated Im[Y_{SS}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated R_E[Y_{SS}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.4 (a) Measured and simulated Im[Y_{BB}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated R_E[Y_{BB}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.5 (a) Measured and simulated Im[Y_{GD}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated R_E[Y_{GD}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.6 (a) Measured and simulated Im[Y_{GS}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated R_E[Y_{GS}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.7 (a) Measured and simulated Im[Y_{GB}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re [Y_{GB}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.8 (a) Measured and simulated Im[Y_{BG}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re [Y_{BG}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.9 (a) Measured and simulated Im[Y_{BD}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re [Y_{BD}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.10 (a) Measured and simulated Im[Y_{BS}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re [Y_{BS}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.11 (a) Measured and simulated Im[Y_{DG}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re[Y_{DG}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.12 (a) Measured and simulated Im[Y_{DB}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re [Y_{DB}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.13 (a) Measured and simulated Im[Y_{DS}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re[Y_{DS}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.14 (a) Measured and simulated Im[Y_{SG}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated Re[Y_{SG}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.15 (a) Measured and simulated Im[Y_{SB}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated RE[Y_{SB}] of M1, M2, and M3 biased VG=VD=1V.

Fig.5.16 (a) Measured and simulated Im[Y_{SD}] of M1, M2, and M3 biased VG=VD=1V.

(b) Measured and simulated RE[Y_{SD}] of M1, M2, and M3 biased VG=VD=1V.

Table Caption

Chapter 5

Table 5.1 (a) The extracted values of the components for the small-signal equivalent circuit model of M1 devices ($3.6\mu m \times 4$).

(b) The extracted values of the components for the small-signal equivalent circuit model of M2 devices ($7.2\mu m \times 4$).

(c) The extracted values of the components for the small-signal equivalent circuit model of M3 devices ($12\mu m \times 4$).

Chapter 1
Introduction

1.1 Introduction and motivation

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most important device for VLSI, ULSI circuits such as microprocessors and semiconductor memories. It has many acronyms including IGFET (insulated-gate field-effect transistor), MISFET (metal-insulator-semiconductor field-effect transistor), and MOST (metal-oxide-semiconductor transistor). The principle of the surface field-effect transistor was first proposed in the early 1925 by Julius Lilienfeld [1], but he never constructed a working device. Before co-inventing the bipolar transistor, William Shockley also tried to modulate the conductivity of a semiconductor to create a field-effect transistor [2], however, problems with his materials system, copper oxide, prevented his success. In 1960, Kahng and Atalla [3]-[4] proposed and fabricated the first MOSFET using a thermally oxidized silicon structure. Than the basic device characteristics, device physics, and applications were widely studied and reviewed.

Traditionally, the high frequency properties of silicon MOSFETs have been considered inferior to other technologies, including silicon bipolar transistors and transistors based on Ⅲ-Ⅴmaterials such as gallium arsenide. However, the CMOS technology has now reached a state of evolution, in terms of both frequency and noise, where it is becoming a serious contender for radio frequency applications in the GHz range. Nowadays, the cutoff frequency of deep-submicron CMOS processes typically reaches 100GHz for 0.13mm technology making them capable to operate well into GHz range which covers many popular wireless products such as cell phones, global position system, Bluetooth. Adopting CMOS processes to radio frequency applications has great benefits of low cost, high-level integration, and the ability to combine the RF front-end and base band circuits together [5]-[7].

An important issue on adopting CMOS for RF applications is the availability of accurate model of RF CMOS for circuit design. However, differences between the RF MOSFET and conventional high frequency transistors make the proper modeling of RF MOSFET complicated and difficult. Two major differences exist; one is related to the substrate materials. MOSFET's are fabricated on a silicon substrate, which lacks of semi-insulating property as a gallium arsenide substrate. Essentially, the intrinsic resistivity of silicon (2.3×10^5 ohm-cm) is much lower lower than that of gallium arsenide (10^8 ohm-cm) due to more plentiful carriers in the intrinsic condition. In addition to intrinsic condition, in a practical CMOS process, the silicon substrate is typically doped to have carrier concentration ranging from about 10^{15} cm^{-3} to about 10^{18} cm^{-3}, which corresponds to resistivity of 0.01 to 10 ohm-cm. The lower resistivity of the silicon substrate results in larger and lossier parasitics related to the substrate. The performance of the integrated CMOS RF circuits is often limited by these parasictics. In RF MOSFET's, the influence of the distributed substrate resistance becomes significant as the operation frequency increases [8]-[12]. At low frequencies, the impedance of the junction capacitance is large that the substrate resistance may not be seen from the drain terminal. However, as operation frequency increases, the impedance of the junction capacitance reduces and the effects of the substrate resistance become obvious. At high frequencies, the signals in RF MOSFET's are coupled through the substrate R-C network in a complex way. The substrate signal coupling mainly affects the small signal output characteristics, which are important for RF design. The other difference arises form the device structure of MOSFET's. The conventional high-frequency FET's have three terminals: a gate, a source, and a drain. Bipolar transistors are also three terminal devices, having an emitter, a base, and a collector. However the MOSFET has a fourth terminal, the body. The body is doped opposite to source and drain regions to isolate these two regions by reverse-biased p-n junctions. The body terminal is typically connected to ground (the lowest potential used in the circuit) for an n-MOSFET and V_{dd} (the highest potential used in the circuit) for a p-MOSFET to prevent the source and drain junctions from being forward-biased in any case. In many

cases, the source and body of the MOSFET are tied together. Even for this configuration, a MOSFET cannot be treated as a three-terminal device since the potential of the intrinsic body node is neither as the extrinsic body terminal nor as the source. It is much more difficult to explain and predict the behavior of the four-terminal device than that of the three-terminal device. A three-terminal device can be treated as a two-port network, where the four complex numbers are enough to characterize the device. However, nine complex numbers are required to characterize a four-terminal device. In other word, multi-port (at least three-port required) on wafer measurement technique is required, but unfortunately there is still no such solution.

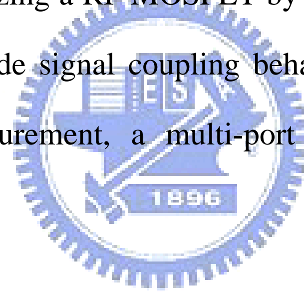
In most cases, the test structure of RF MOSFET is usually arranged in common source configuration with the source and body terminals are tied together and grounded. And the device can be characterized by performing an on-wafer S-parameter measurement by a 2-port network analyzer. Figure 1(a) shows the test structure of an RF nMOSFET schematically. Since the source and body are tied together and the 2-port measurement can only provide 4 independent complex s-parameters, the internal coupling between intrinsic source/body and drain/body could not be directly observed according the 2-port measurement data. The coupling effect arisen from the substrate can only be fitted or guessed according limited 2-port data.

In addition to common source configuration, common gate and common drain condition also appears in RF analog circuits like cascade-type LNA [13]-[15] and transimpedance amplifiers [16]. However, characterizing a MOSFET in common gate (CG) or common drain (CD) configuration by using the traditional 2-port test structure will encounter some problems. Figure 1(b) shows the CG NMOSFET within a traditional 2-port Ground-Signal-Ground RF test structure. In order to operate the device in saturation region, the DC bias voltage applied on gate terminal has to be larger than that applied on the source. However, the body terminal of the device is also connected to the ground metal of the test structure, it will cause the substrate-source junction to be forward biased. There exists the similar situation in common drain configuration shown in Fig. 1(c), the substrate-source junction will be forward biased if

the applied drain voltage were larger than source voltage. There is another method to obtain CG and CS s-parameters which similar to the method used in BJT. In BJT amplifiers, the 2-port network parameters of common base and common collector configurations can be converted from measured common emitter data [17]-[18]. However, unlike BJT's, MOSFET's are 4-terminal devices, adopting this method to a MOSFET device may cause error.

In real CMOS IC's, the body terminals are not always connected to source terminals of every single device. In fact, they are connected to the ground for nMOSFET (V_{dd} for pMOSFET) while source terminals maybe not. The source and body terminals may have voltage drops between them. The traditional 2-port GSG test structure is unable to adapt this bias condition since the source and body are tied together.

As discussed above, characterizing a RF MOSFET by using 2-port measurement really limits the further exploration of inside signal coupling behavior of this device. To overcome the insufficiency of 2-port measurement, a multi-port on-wafer measurement technique is required.



1.2 Organization of the thesis

In this thesis, issues about characterization of RF MOSFET' based on four-port system, parameters extraction for small-signal equivalent circuits, and the performance of the device model will be coverd.

In chapter 1, an introduction to this thesis is brief addressed.

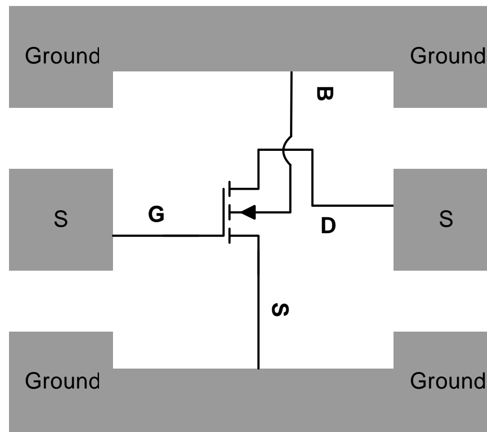
In chapter2, the basic concepts of the scattering parameters will be reviewed. And the four-port measurement system adopted in this study will be briefly introduced.

In chapter 3, the characterization of RF MOSFET's based on the four-port measurement will be demonstrated. The test structures for the DUT's and the dummy stuructures for de-embedding process will also be addressed.

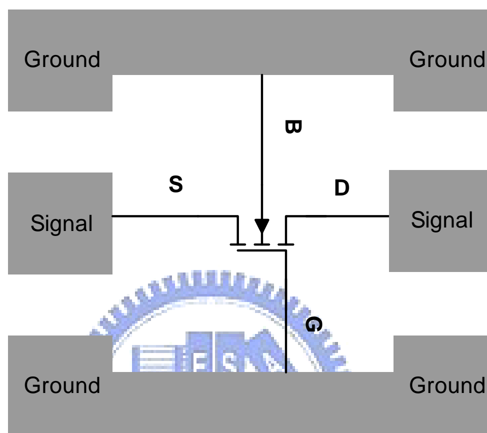
In chapter 4, small-signals equivalent circuits for the devices with different bias conditions and the corresponding parameter extractions will be discussed.

In chapter 5, the proposed model and the parameters extracted from the four-port measurement will be verified.

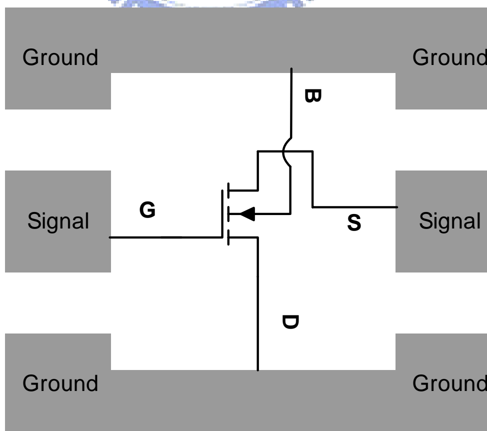
Finally, conclusions for this thesis and suggestions for future works will be given in chapter 6.



(a) Common Source



(b) Common Gate



(c) Common Drain

Fig.1.1 (a) Conventional two-port test structure for common source MOSFET.

(b) Fictional two-port test structure for common gate MOSFET.

(c) Fictional two-port test structure for common drain MOSFET.

Chapter2
Multi-Port Scattering Parameters and Four-Port Measurement System

2.1 Introduction

To model an RF MOSFET to the giga-hertz range relies on reliable DC and high- frequency measurement. The characterization of electronic components in the DC domain is relatively simple and only requires a voltmeter and amperemeter. However, characterizing the frequency performance of the device is more complex since it involves the magnitude dependence and phase shift of the currents and voltages on each terminal of an RF MOSFET. The modeling device is operated under its originally intended conditions with DC bias is applied to all the terminals and additional small-signal RF excitation is applied. The sine currents and voltages at all terminals of the device have to be measured, with magnitude and phase. A natural choice for such characterization would be open-circuit impedance characterization (z-parameters), short-circuit admittance characterization (y-parameters), or hybrid characterization (h-parameters) from linear network theory. These parameters can be used to describe the electrical behavior of the device (or network), including any source and load conditions. For such parameters, the voltage or current as a function of frequency and bias at the ports of the device must be measured. However, at high frequency, it is very hard to implement pure “open” or “short” terminations at the device ports. One cannot simply connect a voltmeter or current probe and get accurate measurement due to the parasitic impedances of the test structure and probes themselves.

Therefore, some other way of characterizing high-frequency networks is required that doesn’t have these drawbacks. The scattering parameter (s-parameter) that relate to familiar parameters such as gain, loss, and reflection coefficient is developed. The s-parameters are relatively simple to measure, and do not require pure “open”, “short” terminations to the

device. Different to Y, Z, or H parameters, they relate to the traveling waves that are scattered or reflected when a network is inserted into a transmission line of a certain characteristic impedance Z_0. While s-parameters are measured, Z, Y, or H-parameters can all be derived from the measured s-parameters if necessary.

At high frequencies above about 1 GHz, S-parameter measurement is the easiest and the most reliable way to measure the network characteristics of a certain functional block. A great number of models and corresponding parameter extraction methods from S-parameter measurement data have been proposed for various kinds of two-port networks such as passive devices and transistors [19]-[23]. In present, the most common system used for s-parameter measurement is 2-port system. Its core is a 2-port network analyzer. However, a multi-port system has similar theory with a multi-port system, and it's rather simple to extend 2-port concept to multi-port system. In this chapter, the fundamental one-port s-parameter and characterization method will be briefly introduced first. Than the theory of extending one-port s-parameter to multi-port s-parameters will be discussed. Additionally, the methods of transferring multi-port s-parameters to Z-, Y-parameters will also be addressed. Finally, the 4-port equipment and calibration method used in this study will be presented.

2.2 Multi-Port Scattering Parameters

Scattering implies causing something to separate into different components, and scattering parameters provide a measure of the degree of separation and the magnitude of different components. Scattering is relatively easy to visualize when the scattered components actually exist. For example, when light falls on an atom, the electronic motions are changed such that light is reemitted. This reemitted light is called scattered light, and its amplitude is related to a scattering constant of the atom.

However, the scattering concept is more difficult to visualize when the incident and reflected components do not actually exist. Such is the case for a transistor connects to its load through a lumped matching network. Here it is necessary to define what is meant by "incident" and

'reflected" components because they cannot be identified otherwise. Therefore the incident current is defined as the current which the transistor would deliver to a conjugate matched load. The fact that the matching network which is actually connected to the transistor may not necessarily provide a conjugate-matched load. It dose not alter the validity of the incident current definition since the incident current can be different from the actual current delivered to the matching network, their difference is defined as the reflected current. Defining statements are also made for incident and reflected voltages. Therefore, when the scattering concept is applied to lumped circuit, the actual currents and voltages can be separated components according to appropriate definitions.

2.2.1 the one-port network

The scattering concept is perhaps best illustrated by considering the one-port network shown in Fig. 2.1. The actual current and voltage are

$$I = \frac{E}{Z_0 + Z_L} \tag{1}$$

and

$$V = \frac{EZ_L}{Z_0 + Z_L} \tag{2}$$

in which Z_0 is considered to be internal impedance of the generator.

The incident components are obtained when the generator is connected to a conjugate matched load Z_0^*, as in Fig. 2.2. Thus

$$I_i = \frac{E}{Z_0 + Z_0^*} = \frac{E}{2\,\mathrm{Re}\,Z_0} \tag{3}$$

and

$$V_i = \frac{EZ_0^*}{Z_0 + Z_0^*} = \frac{EZ_0^*}{2\,\mathrm{Re}\,Z_0} \tag{4}$$

where Re stands for real part of the value.

The reflected components are calculated using the defining decomposition equations

$$I = I_i - I_r \tag{5}$$

and

$$V = V_i - V_r \tag{6}$$

Using (1) and (3) in (5), the reflected current can be expressed as

$$\begin{aligned} I_r &= I_i - I \\ &= \left(\frac{Z_L - Z_0^*}{Z_L + Z_0} \right) I_i \\ &= S^I I_i \end{aligned} \tag{7}$$

where $S^I = \left(Z_L - Z_0^*\right) / \left(Z_L + Z_0\right)$ is a current scattering parameter for the one port circuit.

Similarly, using (2) and (4) in (6), the reflected voltage can be expressed as

$$\begin{aligned} V_r &= V_i - V \\ &= \frac{Z_0}{Z_0^*} \left(\frac{Z_L - Z_0^*}{Z_L + Z_0} \right) V_i \\ &= \frac{Z_0}{Z_0^*} S^I V_i = S^V V_i \end{aligned} \tag{8}$$

where $S^V = \left(Z_0 / Z_0^*\right) S^I$ is a voltage scattering parameter for the one-port circuit.

It is also readily shown that

$$V_i = Z_0^* I_i \tag{9a}$$

and

$$V_r = Z_0 I_r \tag{9b}$$

The incident and reflected components are related to each other through the impedances and the scattering parameters as defined. Each scattering parameter and reflected component is zero when $Z_L = Z_0^*$.

The impedance Z_0 is often made to be a pure resistance $R_0 > 0$, so that $Z_0 = R_0$, and it is used as a normalizing or reference resistance. It is usual to consider the reference resistance equal to 50Ω, particularly if scattering-parameter measurements are made using 50Ω lines and termination. If $Z_0 = R_0$ and $Z_0^* = R_0$, then

$$S^I = S^V = \frac{Z_L - R_0}{Z_L + R_0} \tag{10}$$

For this case the current and voltage scattering parameters of the one-port circuit are equal, and have exactly the same form as the reflection coefficient of a transmission line having a characteristic resistance R_0 and terminated in a load Z_L. The scattering parameters of the port are equal to zero if its impedence is the same as the reference resistance R_0. Also, for this case (9a) and (9b) become

$$V_i = R_0 I_i \tag{11a}$$

and

$$V_r = R_0 I_r \tag{11b}$$

2.2.2 the n-port network

the scattering parameters for the n-port network shown in Fig. 2.3 are developed using matrix algebra. It is assumed that the individual generators are independent of each other. This means that the matrix [Z0] representing internal impedances contains no cross-coupling terms, and is given by the diagonal matrix

$$[Z_0] = \begin{bmatrix} Z_{01} & 0 & \cdots & 0 \\ 0 & Z_{02} & \cdots & 0 \\ \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & Z_{0n} \end{bmatrix} \tag{12}$$

The incident and reflected components at the ports are related to the actual voltages and currents by the column matrices

$$[I] = [I_i] - [I_r] \tag{13a}$$

and

$$[V] = [V_i] - [V_r] \tag{13a}$$

The incident and reflected components are related by

$$[V_i] = \left[Z_0^*\right][I_i] \tag{14a}$$

and

$$[V_r] = [Z_0][I_r] \tag{14b}$$

which correspond to the one-port case of (9a) and (9b).

The open-circuit impedance-parameter relationship for the n-port network is

$$[V]=[z][I] \tag{15}$$

The incident and reflected components can be determined from (12)-(15) as follows:

$$[V_r]=[V]-[V_i]=[z][I]-\left[Z_0^*\right][I_i]$$

or

$$[Z_0][I_r]=[z]([I_i]-[I_r])-\left[Z_0^*\right][I_i]$$

Combine terms to obtain

$$([z]+[Z_0])[I_r]=\left([z]-\left[Z_0^*\right]\right)[I_i]$$

Multiply by $([z]+[Z_0])^{-1}$ to obtain

$$\begin{aligned}[I_r]&=([z]+[Z_0])^{-1}\left([z]-\left[Z_0^*\right]\right)[I_i]\\&=\left[S^I\right][I_i]\end{aligned} \tag{16}$$

where

$$\left[S^I\right]=([z]+[Z_0])^{-1}\left([z]-\left[Z_0^*\right]\right) \tag{16a}$$

is the current scattering-parameter matrix that is analogous to that for the one-port case given in (7).

Similarly, using the short-circuit admittance-parameter relationship

$$[I]=[y][V] \tag{17}$$

it is found that

$$\begin{aligned}[V_r]&=-([Y_0]+[y])^{-1}\left([y]-\left[Y_0^*\right]\right)[V_i]\\&=\left[S^V\right][V_i]\end{aligned} \tag{18}$$

where

$$[y]=[z]^{-1},\ [Y_0]=[Z_0]^{-1}$$

and

$$\left[S^V\right]=-([Y_0]+[y])^{-1}\left([y]-\left[Y_0^*\right]\right) \tag{19}$$

is the voltage scattering-parameter matrix.

2.2.3 normalized scattering parameters

The normalized incident and reflected components is defined as

$$\begin{aligned}[a] &= \frac{1}{\sqrt{2}}\left([Z_0]+\left[Z_0^*\right]\right)^{1/2}[I_i] \\ &= [\operatorname{Re} Z_o]^{1/2}[I_i]\end{aligned} \tag{20}$$

and

$$\begin{aligned}[b] &= \frac{1}{\sqrt{2}}\left([Z_0]+\left[Z_0^*\right]\right)^{1/2}[I_r] \\ &= [\operatorname{Re} Z_o]^{1/2}[I_r]\end{aligned} \tag{21}$$

where

$$\begin{aligned}\frac{1}{\sqrt{2}}\left([Z_0]+\left[Z_0^*\right]\right)^{1/2} &= [\operatorname{Re} Z_o]^{1/2} \\ &= \begin{bmatrix} \sqrt{\operatorname{Re} Z_{01}} & 0 & \cdots & 0 \\ 0 & \sqrt{\operatorname{Re} Z_{02}} & \cdots & 0 \\ \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & \sqrt{\operatorname{Re} Z_{0n}} \end{bmatrix}\end{aligned} \tag{22}$$

Then combining (16) with (20) and (21) yields

$$\begin{aligned}[\operatorname{Re} Z_0]^{-1/2}[b] = [I_r] &= \left[S^I\right][I_i] \\ &= \left[S^I\right][\operatorname{Re} Z_0]^{-1/2}[a]\end{aligned}$$

Multiplying by $[\operatorname{Re} Z_0]^{1/2}$ yields

$$[b] = [\operatorname{Re} Z_0]^{1/2}\left[S^I\right][\operatorname{Re} Z_0]^{-1/2}[a]$$

or

$$[b] = [S][a] \tag{23}$$

where

$$[\mathrm{Re}\,Z_o]^{-1/2} = \begin{bmatrix} \frac{1}{\sqrt{\mathrm{Re}\,Z_{01}}} & 0 & \cdots & 0 \\ 0 & \frac{1}{\sqrt{\mathrm{Re}\,Z_{02}}} & \cdots & 0 \\ \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & \frac{1}{\sqrt{\mathrm{Re}\,Z_{0n}}} \end{bmatrix} \quad (24)$$

and

$$[S] = [\mathrm{Re}\,Z_0]^{1/2}\left[S^I\right][\mathrm{Re}\,Z_0]^{-1/2} \quad (25)$$

The matrix $[S]$ thus obtained is called the normalized scattering matrix, and its elements are called normalized scattering parameters, or simply scattering parameters. These are the parameters that are usually meant when reference is made to scattering parameters.

It can be shown that

$$\left[S^I\right] = [Z_0]^{-1}\left[S^V\right]\left[Z_0^*\right] \quad (26)$$

If the impedance matrix does not exist for a particular n-port network, but the admittance matrix exists, the scattering parameters can be calculated using (19), (25), and (26).

If $[Z_0] = \left[Z_0^*\right] = [R_0]$, then

$$\left[S^I\right] = \left([z]+[R_0]\right)^{-1}\left([z]-[R_0]\right) \quad (27)$$

and

$$[S] = [R_0]^{1/2}\left[S^I\right][R_0]^{-1/2} \quad (28)$$

Expansion (28) shows that

$$[S] = [S^I] \tag{29}$$

if the reference resistances at all ports are equal.

Using the typical conditions

$$[Z_0] = [Z_0^*] = \left[\frac{1}{Y_0}\right] = [R_0] \tag{30}$$

with all resistances equal results in

$$[S] = [S^I] = [S^V] \tag{31}$$

Thus (16a) becomes

$$([z]+[R_0])[S] = [z]-[R_0] \tag{32}$$

Solve for $[z]$ to obtain

$$[z] = [R_0]([I]+[S])([I]-[S])^{-1} \tag{33}$$

where $[I]$ is the unit diagonal matrix. Since $[R_0]$ has equal value along the diagonal, (33) becomes

$$[z'] = \left[\frac{z}{R_0}\right] = ([I]+[S])([I]-[S])^{-1} \tag{34}$$

where $[z']$ represents the normalized parameters obtained by dividing the actual z-parameters by R_0. Also, using (30) and (31) yields for (19)

$$([Y_0]+[y])[S] = -([y]-[Y_0^*]) \tag{35}$$

Solve for $[y]$ to obtain

$$[y]=[Y_0]([I]-[S])([I]+[S])^{-1} \tag{36}$$

Since $[Y_0]$ has equal values along the diagonal, (36) becomes

$$[y']=[R_0 y]=([I]-[S])([I]+[S])^{-1} \tag{37}$$

where $[y']$ represents the normalized parameters obtained by multiplying the actual y-parameters by R_0.

2.3 Four-port measurement system

2.3.1 Four-port measurement system

A vector network analyzer (VNA) is an instrument, which sends stimulus and receives response to characterize a device under test (DUT). A sine wave is transmitted into the DUT while tuned receiver are swept in lockstep, providing both reflection and transmission properties. VNA is known to have the most accurate calibration standard of any test and measurement instrumentation. The raw measurement results of a VNA are calibrated using frequency domain artifacts – each measurement is accurate, repeatable and traceable, and its measurements are often expressed as scattering parameters. The 4-port VNA used for characterizing RF MOSFET's in this study is the Agilent N1957B Physical Layer Test System and is shown in Fig. 2.4. This system consists of a standard 2-port VNA (Agilent E8364B) capable to perform s-parameter measurements from 10MHz to 50GHz, a test set (Agilent N4421B), and PC-based control software. The test set converts the standard 2-port VNA to a 4-port VNA, thus enabling characterization of a 4-port DUT. In addition to the 4-port NWA, an Agilent 4156 used as a 4-channel DC source is incorporated with 4 bias-tees to provide the required DC bias voltage during s-parameter measurement.

2.3.2 Calibration

Measurement calibration is an accuracy enhancement procedure that effectively removes the measurement errors that cause uncertainty in measuring a DUT. Measurement errors can be classified into three categories: drift errors, random errors, and systematic errors. Drift errors are caused by deviations in performance of the measuring instrument that occur after calibration. Major causes are the thermal expansion of connecting cables and the thermal drift of the frequency converter within the measuring instrument. These errors can be reduced by carrying out frequent calibrations as the ambient temperature changes or by maintaining a stable ambient temperature during the course of a measurement. Random errors occur irregularly along the time axis. Since random errors are unpredictable, they cannot be eliminated in a calibration. The main contributors to random errors are instrument noise such as, source phase noise, sampler noise, and IF noise. The accurate source and phase-locked receiver of the network analyzer greatly minimizes these random errors. Systematic errors are caused by imperfections in the measuring instrument and the test setup (cables, connectors, RF probe, etc.). Assuming these errors are repeatable and their characteristics do not change relative to time, then it is possible to eliminate these errors mathematically at the time of measurement by determine the characteristics of these errors in a calibration. There are six types of systematic errors: directivity and crosstalk related to signal leakage, source and load impedance mismatches related to signals being reflected, and frequency response error caused by reflection and transmission tracking with the test receivers. A VNA has 2 receivers for each test port, the reference receiver and the test receiver (transmission measurement or reflection measurement) and allows one to perform measurements using these receivers at the same time. Figure 2.5 shows the architecture of the test ports of a VNA and systematic errors. For the 4-port VNA, there exist four directivity-error terms (E_d), twelve crosstalk-error terms (E_x), four source-mismatch error terms (E_s), twelve load-mismatch error terms (E_l), four reflection tracking error terms (E_r), and twelve transmission tracking error terms (E_t). The full 4-port error model and the 48 error terms mentioned above are shown schematically in Fig. 2.6. The most common calibration method used to characterize the systematic errors is Short-

Open-Load-Through (SOLT) calibration [24]-[25]. In full 4-port calibration, calibration data are measured by connecting an SHORT standard, OPEN standard, an LOAD standard to the 4-test port, and THRU standard between each two ports. According to SOLT method, the 48 error terms for the 4-port NWA can be calculated from the measured calibration data. The calibration data will be stored in the memory of VNA, and the measured RAW data will be processed automatically during the measuring procedure is going. The imperfection effect of the VNA and the parasitics of the cables, connectors, and probes can all be eliminated and results in a measurement data as close to the intrinsic data of the DUT as possible.

2.4 Summary

In this chapter, the fundamental one-port scattering parameter is brief introduced. Then, deduce of multi-port scattering parameters according to the one-port concept is demonstrated. The conversion of multi-port scattering parameters to Z- and Y- parameters, which are important in the following studies of RF MOSFET modeling are also addressed. Finally, the 4-port vector network analyzer used in this study is introduced; the calibration of this 4-port VNA is also described conceptually.

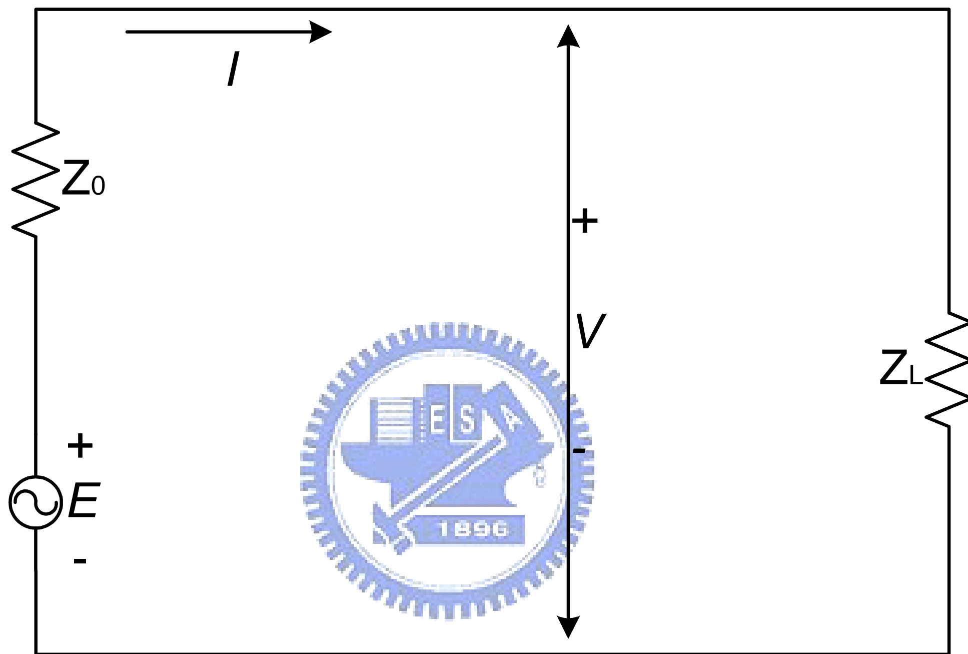


Fig.2.1 One port network.

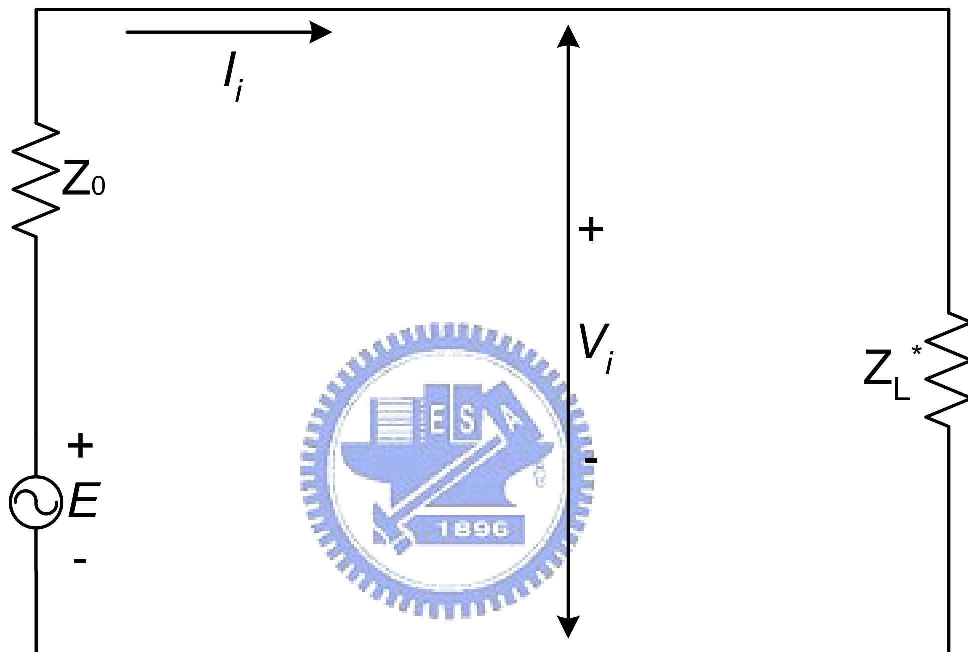


Fig.2.2Generator with conjugate matched load used to define “incident” components I_i and V_i.

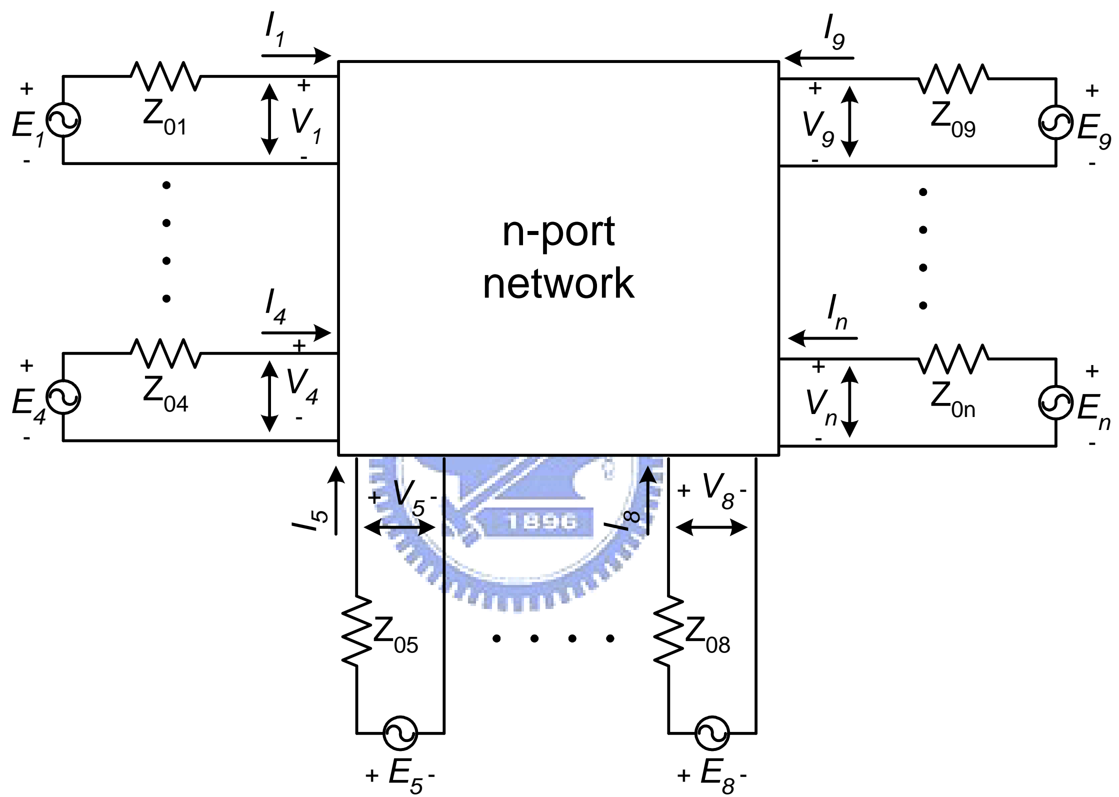


Fig.2.3 An n-port network with generators.

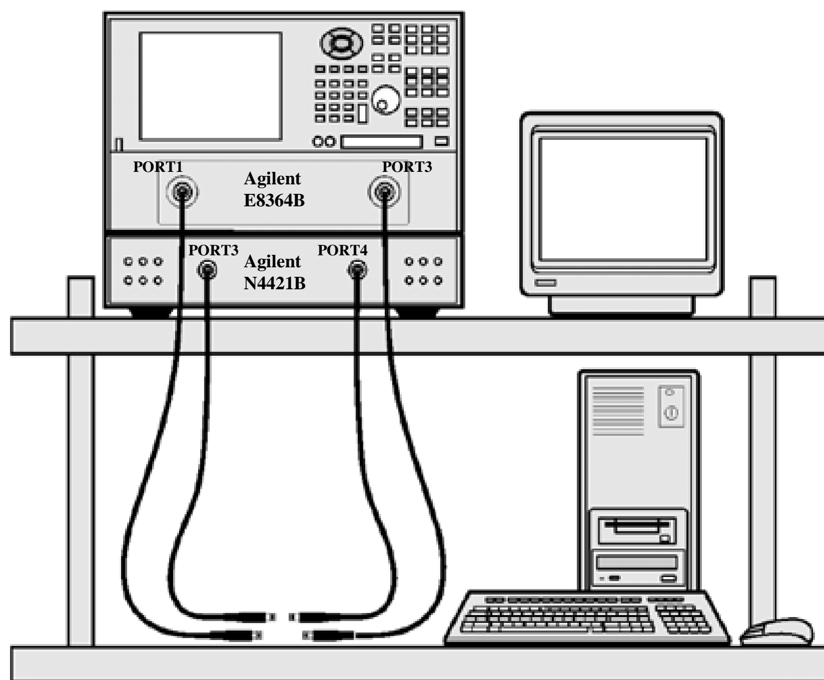


Fig.2.4 Agilent N1957B Physical Layer Test System.

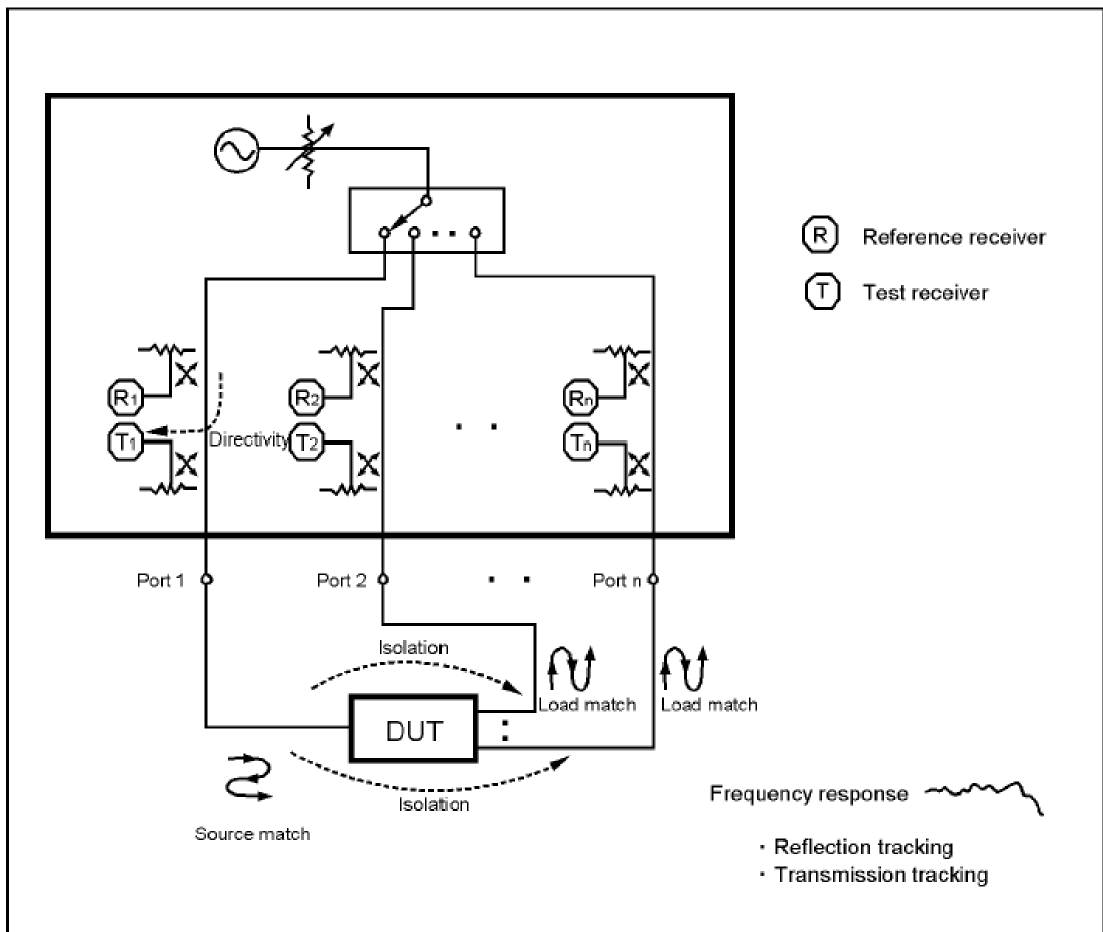


Fig.2.5 Architecture of VNA test ports and the systematic errors.

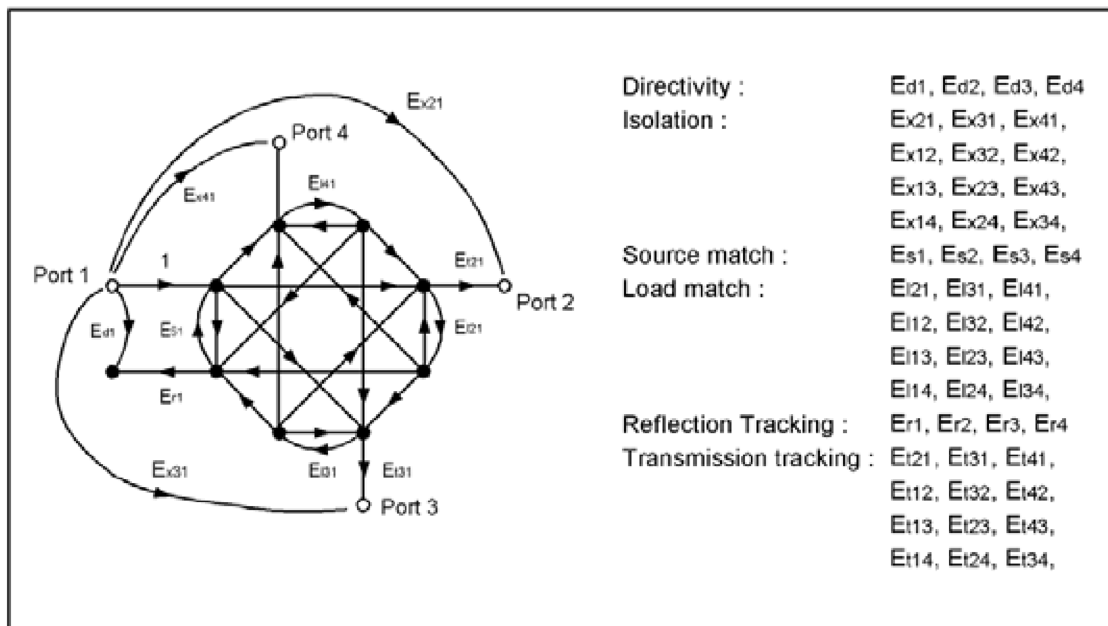


Fig.2.6 The full 4-port error model and the 48 error terms.

Chapter 3
Characterizing RF MOSFET's by Four-Port Measurement

3.1 Motivation

The high F_t and high-level integration ability of modern CMOS technology make that GHz range applications of RF MOSFET more popular today. In most cases, MOSFET's are designed as common source amplifiers in analog and RF circuits. Therefore, the characterization method of a MOSFET is usually arranging the device as a 2-port amplifier in common source configuration, and perform on-wafer S-parameter measurement by conventional 2-port network analyzer. In addition to common source configuration, common gate and common drain condition also appears in RF analog circuits as mentioned in chapter one. To characterize a MOSFET in common gate (CG) or common drain (CD) configuration by using the traditional 2-port test structure will encounter problems. While fitting a RF MOSFET in a 2-port test structure, two of the four terminals of the MOSFET must be connected together. On the other word, the body must be connected to the other terminal witch is intended to be "commoned". In the case of common source, since the source and body are tied together and connected to ground, the DC bias can be easily applied for the device to operate in saturation mode. In the case of common gate configuration, however, the common terminal gate cannot be tied with body. The DC bias voltage applied on gate terminal has to be larger than that applied on the source in order to operate the device in saturation region. If the body was tied with gate, it will cause the substrate-source junction to be forward biased, which violates the principle of operating a MOSFET. There exists similar situation in the case of common drain configuration. The substrate-source junction will be forward biased if the body was tied with the drain. Besides the bias problem of common gate and common drain cases, in real CMOS IC's, the body terminals are not always connected to

source terminals of every single device. In fact, they are connected to the ground or the most negative potential in the circuits while source terminals maybe not. The source and substrate terminals may have voltage drops between them. The traditional 2-port GSG test structure is unable to adapt this bias condition.

An efficient way to overcome theses problems is to fit the four-terminal RF MOSFET to a multi-port test structure that has at least three ports. In this chapter, a four-port test structure for s-parameter measurement of RF MOSFET's is proposed. The DC bias voltage on each terminal will be applied independently. The data of RF MOSFET in CS, CG, and CD configurations can all be characterized by a single proposed four-port test structure. Besides, the s-parameters of RF MOSFET's in common source configuration under different substrate biases are also observed.

3.2 Four-Port RF MOSFET's

The devices used in this study are RF MOSFET's fabricated with 0.13μm CMOS process of UMC. General multi-finger gate structure is adopted for the devices, and the finger number is four for all devices but with different finger length. Four gate fingers means the devices are unsymmetrical, since there will be two source and three drain junctions or two drain and three source junctions depend on the connection and applied voltage of source/drain terminals. The layout of the RF MOSFET is designed as the gate, drain, source and body terminals were connected individually to four signal pads of a four-port test structure. Figure 3.1a shows the test structure and the RF MOSFET schematically. Figure 3.1b is the top view photograph of the DUT. These four signal pads incorporated with a reference ground form a 4-port Ground-Signal Ground (GSG) test structure and the RF MOSFET can be treated as a 4-port device and characterized by 4-port measurement.

The on-wafer four-port measurement of this test structure was accomplished by the Agilent PLTS 50GHz 4-port system incorporated with a Cascade Microtech probe station and four RF probes. Since the port positions in this test structure are orthogonal, the generally used SOLT (short, open, load, thru) calibration procedure is not usable in this condition [10,11]. In SOLT calibration procedure, the RF properties of the four standard (SHORT, OPEN, LOAD, THRU) must be define clearly. In conventional two-port SOLT calibration, the THRU standards are always fabricated short and strait and has characteristic impedance of 50Ω. This kind of well behavior THRU line can be simply specified by a delay time and character impedance. However, specifying an orthogonal THRU standard just by delay time and characteristic impedance is inefficient since the behavior of orthogonal THRU is much more complex. One solution for this kind of orthogonal or other undefined THRUs is conducting a SOLR calibration procedure. By SOLR calibration method, the definite THRU specification is not necessary. The only thing it needs about the THRU standard is the approximate delay time. According to the SOLR and the approximate delay time, a set of two-port scattering parameters represent the orthogonal THRU can be obtained. And the error terms can still be calculated out. However, the PLTS system used to conduct the four-port measurement doesn't equip with SOLT calibration procedure in its control software. The calibration method used this study is still the SOLT method, but with the specification of orthogonal THRU obtained by a two-port measurement in which the two-port were posited in right angle and calibrated by SOLR method.

3.3 Dummy Structures and De-Embedding Procedure

The proposed four-port test structure is shown in Fig.3.2 three-dimensionally. The signal metal connections are mainly routed by top metal layer and are shielded by the bottom metal layer connected to ground. The test structure with the body signal pad connected to substrate

is shown in Fig.3.3. This test structure exhibits several parasics and the equivalent circuit of the test structure is shown in Fig. 3.4. In this circuit, the four Y_{pad} components represent the shunt admittances across the individual signal pad and the surrounding ground metal. In this 4-port test structure, the signal pad of port2 corresponding to the body terminal is connected to the silicon substrate through substrate contacts. The substrate contacts is arranged in ring-type and surrounding the active area of the NMOSFET. This, however, will cause a kind of unique parasitic in the area outside the active region. The substrate area outside the contact ring will exhibit as extrinsic shunt parasitics between substrate and the ground metal which shields the substrate loss form coupling to the signal metal connections of the other three terminals. The components Y_{sub} are corresponding to this parasitic. The substrate area outside the contact ring but isn't shielded by the bottom metal layer (M1) will form another shunt parasitic components between substrate and each signal metal traces of other three terminals. In other words, the substrate loss will be coupled to the signal metal traces of the other three terminals via these shunt parasitics and they are corresponding to the three Y_{ps} components in Fig.3.4. The four Z_s components in Fig.3.4 represent the series impedances of signal metal trace. To obtain the intrinsic RF characteristic of the DUT, these parasitics must be removed firstly.

The Y_{pad}, Y_{sub}, Y_{ps}, and the shunt admittance components exist between each 2 signal pads that aren't shown in Fig.3.4 can be de-embedded from the raw measurement data of 4-port NMOSFET by performing open de-embedding procedure according to the same structure shown in Fig.3.3. This is the same test structure with the proposed 4-port NMOSFET except that the NMOSFET is taken out. It can be treated as a special open dummy for the four-port test structure. The Z_s components can be de-embedded out by performing short de-embedding procedure, and the short dummy structure shown in Fig.3.5. In this short dummy structure, all signal connections including the vias between metal layers are shorten by the bottom metal layer.

During the de-embedding process, the raw 4-port S-parameters matrix S_{RAW} of the 4port nMOSFET is firstly transferred to Y-parameters Y_{RAW} according to Eq. 1 [12].

$$[Y]=[I-S]\bullet[I+S]^{-1} \qquad (3\text{-}1)$$

The I in Eq.3-1 represents a 4x4 identity matrix. According to Eq.3-1, the measured four-port S-parameters of the special open dummy shown in Fig.3.3 can also obtained as Y_{open}. According to Eq.3-2, the 4-port Z-parameters of the short dummy structure can be obtained as Z_{short}.

$$[Z]=[I+S]\bullet[I-S]^{-1} \qquad (3\text{-}2)$$

The intrinsic Y-parameters of the 4-port NMOSFET Y_d can be derived from Eq.3-3.

$$[Y_d]=\left[[Y_{RAW}-Y_{open}]^{-1}-Z_{short}\right]^{-1} \qquad (3\text{-}3)$$

Figure 3.6 compares the difference of input admittance at port2 (body signal pad) between the special open dummy and an ordinary open dummy without substrate contact ring. The proposed open dummy exhibits the parasitic Y_{sub} shown in Fig.3.4, which need to be de-embedded from the raw measurement data of the DUT while the ordinary open dummy exhibits merely the Y_{pad} parasitic component.

3.4 Four-Port Y-parameters and Port Reduction

According the definition, the Y-parameters of the proposed NMOSFET can be expressed as:

$$\begin{bmatrix} i_G \\ i_D \\ i_S \\ i_B \end{bmatrix} = \begin{bmatrix} y_{GG} & y_{GD} & y_{GS} & y_{GB} \\ y_{DG} & y_{DD} & y_{DS} & y_{DB} \\ y_{SG} & y_{SD} & y_{SS} & y_{SB} \\ y_{BG} & y_{BD} & y_{BS} & y_{BB} \end{bmatrix} \begin{bmatrix} v_G \\ v_D \\ v_S \\ v_B \end{bmatrix} \qquad (3\text{-}4)$$

In the proposed NMOSFET test structure, the NMOSFET has its four terminals connecting to four signal pads, therefore, the Y-matrix of this device represent a NMOSFET without any common terminal. According to Eq. 3-4, grounding a terminal is simply giving the

corresponding voltage source a zero value, and the remained sub-matrix will be the Y-matrix represents the resulting configuration of the NMOSFET. Therefore, the 4x4 matrix of four-port Y-parameters will be easily reduced to three-port or two-port Y-matrix depending on the requirement.

The grounded terminals of CS configuration is source and body terminals, therefore, the CS two-port Y-matrix can be obtained by setting $v_S = 0$ and $v_B = 0$ in Eq.3-4. And the two-port CS Y-matrix is just the sub-matrix corresponding to [i_G, i_D] and [v_G,v_D], it can be expressed as Eq. 3-5.

$$\begin{bmatrix} i_G \\ i_D \end{bmatrix} = \begin{bmatrix} y_{GG} & y_{GD} \\ y_{DG} & y_{DD} \end{bmatrix} \begin{bmatrix} v_G \\ v_D \end{bmatrix} \quad (3\text{-}5)$$

Similarly, the CG and CD Y-matrix can be also obtained in the same manner and can be expressed as Eq.3-6 and Eq.3-7, respectively.

$$\begin{bmatrix} i_S \\ i_D \end{bmatrix} = \begin{bmatrix} y_{SS} & y_{SD} \\ y_{DS} & y_{DD} \end{bmatrix} \begin{bmatrix} v_S \\ v_D \end{bmatrix} \quad (3\text{-}6)$$

$$\begin{bmatrix} i_G \\ i_S \end{bmatrix} = \begin{bmatrix} y_{GG} & y_{GS} \\ y_{SG} & y_{SS} \end{bmatrix} \begin{bmatrix} v_G \\ v_S \end{bmatrix} \quad (3\text{-}7)$$

3.5 Measurement Results and Discussions

3.5.1 Measurement Results of Devices with Different Dimensions

Three 0.13 μm multi-finger NMOSFET's with different gate widths were characterized from 100MHz to 20GHz. The gate finger lengths are 3.6 (M1), 7.2 (M2) and 12 μm (M3), and with the same finger number four. And the total gate width of each device is 14.4, 28.8 and 48 μm for M1, M2, and M3, respectively. The devices are biased at V_G=1V, V_D=1V,V_S=0V, and V_B=0V. The drain currents are 6, 11, 20 mA corresponding to M1, M2, and M3.

Figure 3.7 shows the reflection four-port scattering parameters S_{GG}, S_{DD}, S_{SS}, and S_{BB} on each terminal of M1, M2, and M3 in a smith chart. The three S_{GG} curves almost extend along the same R circle but with different length as frequency increases. The wider the gate width of the device is, the longer the S_{GG} curve goes. It represents the input capacitance at gate scales with total gate width of each device. The S_{DD} curves show the finite output resistance of the devices. The wider the device gate width is, the smaller the output resistance presents at drain. They also reveal that the output capacitance of each device also scale with the device dimension. The S_{SS} curves of the three devices are also shown. It shows there exists inductive input impedance at source terminal and is also scaled with the device dimension. The input inductance appears at source is mainly caused by two factors. The first one is the resistance appears at gate terminal, which will produce an input inductance component at source. The second one is the imaginary part of the current source ($-\omega C_m$), witch will also produce an input inductance at source terminal. This inductance component can be deduced from the small-signal equivalent circuit of an RF NMOSFET, but was observed from directly measured data for the first time since it cannot be observed from two-port measurement data. Figure 3.8 shows the measured S_{GB} of the three devices, the test signal transmitted from body to gate via substrate resistances and small capacitance that exists between substrate and gate. The measured S_{GD}, S_{GS}, S_{BG}, S_{BD}, and S_{BS} are shown in Fig. 3.9, Fig 3.10, Fig. 3.11, Fig. 3.12, and Fig. 3.13, respectively. They all exhibits test signal transmitted from one port to another via capacitive and resistive components. These components are passive in a RF MOSFET. It can be easily observed that these parameters are also scaled with the device dimension. A particular phenomenon is observed that the S_{GB} and S_{BG} of saturation MOSFET's are different while they are identical if the devices are not applied bias voltages on each terminal. This is due to that the when signal is sent to body, it will transmit to gate via substrate resistance and parasitic capacitance between this terminal. In the other hand, the signal applied at substrate will influence the carriers in the channel of the device due to body effect. However, if the signal is sent to gate, the carriers in the channel of the NMOSFET will be influenced directly

by the test signal, and the fluctuation of carriers in channel than couple to the substrate. The different mechanism results in different S_{GB} and S_{BG}.

Figure 3.14 shows the S_{DG} and S_{SG} of the three devices. S_{DG} represents a measurement of signal transmits form gate to drain resembles to the S_{21} in the case of the DUT is arranged in two-port common source configuration. S_{DG} is primarily caused by the transconductance of the devices and exhibit 180 degrees phase at low frequency. S_{SG}, which cannot be measured from two-port DUT's, is the measurement of test signal transmits from gate to source. This transmission is also caused by the transconductance of the DUT, but will be in phase with the signal applied at gate. The S_{SG} is related to the forward transmission of the device configured in two-port common drain mode, or so-called source follower.

Figure 3.15 shows the measured S_{DB} and S_{SB}. S_{DB} is caused mainly by back-gate bias effect or so called body effect. According to this effect, the body acts as a second gate of the device and will slightly control the drain current. Therefore, S_{DB} is similar to S_{DG} and has 180 degrees phase at low frequency. The S_{SB} is also induced by body effect. The signal applied on body will result a signal at source with the same phase at low frequency.

Figure 3.16 shows the S_{DS} and S_{SD} of the three devices. S_{DS} is a measurement of signal transmits from source to drain, which is related to the device configured in two-port common gate configuration. While a test signal is applied at source, the channel current will be controlled by this signal hence the results an output signals at drain. The test signal will be in phase with the resulted signal at drain at low frequency, therefore, the contour of S_{DS} started from the 0 degree axis of the polar chart. The S_{SD} mainly induced from the finite resistance exists between drain and source, which is resulted from the channel length modulation effect of MOSFET devices.

3.5.2 Two-Port Scattering Parameter of The Common Source, Common Drain, and Common Gate RF MOSFET,s

The measured four-port scattering parameters were transferred to the two-port scattering parameters of devices in common source, common drain, and common gate configurations according to Eq. 3-1, Eq. 3-4, Eq. 3-5, Eq. 3-6, and Eq 3-7.

Figure 3.17 shows two-port common source reflection parameters, S_{GG} and S_{DD}, which are transferred from four-port data. Figure. 3.18 shows the corresponding transmission parameters, S_{GD} and S_{DG}. Since the 50Ω termination connected between source and ground in the four-port VNA is shorten (short the source and ground) theoretically while converting the four-port scattering parameters to two-port case, it is obviously the two-port parameters are all different with the correspondent parameters in four-port case. The most easily to be observed is the S_{DG}, whose magnitude was enlarged since the 50Ω resistance was removed. The S_{GG} curves in Fig. 3.17 also shows that common source devices have larger input capacitance than the four-port MOSFET's since more serious Miller effect due the larger gain of common source devices. Comparing the S_{DD} curves in Fig. 3.7 and Fig. 3.18, it's also observed that the drain output resistances of common source devices are smaller than that of four-port devices since the source terminals of the common source devices are grounded.

Figure 3.19 shows the two-port reflection parameters of devices in common drain configuration. A MOSFET in common drain configuration is also called a source follower, which theoretically can produce an output signal almost identical to the input signal but with a smaller output resistance. The contours of reflection parameters at gate (S_{GG}) are similar to the S_{GG} contours of common source configuration shown in Fig. 3.17, but with a shorter length in the smith chart. This means the input capacitance at gate terminal of a MOSFET in common source configuration is much larger than the input capacitance at the same gate terminal of the same device but is configured in common drain configuration. This is due to the well-known Miller effect, the input capacitance of the common source MOSFET will be amplified approximately by the magnitude of the voltage gain ($1-A_V$) of the device. The S_{SS} curves in Fig. 3.19 show the output impedance is also inductive. As have mentioned

previously, the inductive impedance at source is caused by the resistance appears at gate and the transcapacitance C_m. Figure 3.20 shows the two-port transmission scattering parameters of devices in common drain configuration.

The two-port reflection scattering parameters of the devices in common gate configuration, S_{SS} and S_{GG}, are shown in Fig. 3.21. Devices operated in this configuration are mainly used as a current buffer. S_{SS} curves show that the input impedances are inductive, resistive or capacitive depends on the device dimension. This is due to the gate terminals are grounded, which in terms reduces the resistance appears at gate terminal (without 50Ω termination). Therefore the inductive components at source terminals are reduced. In addition to the inductive component induced from the gate resistance and transconductance C_m, the input impedance at source terminal is also affected by the source/substrate junction capacitance. In lager device M3, the inductive component induced from larger gate resistance and C_m will larger enough to maintain the inductive input impedance at source. However, as the device dimension decreases, the input impedance caused by inductive component due to smaller gate resistance and C_m combined with the capacitive source/substrate junction will become resistive or capacitive. Figure 3.22 shows the two-port S_{DS} and S_{SD} parameters of the devices in common gate mode.

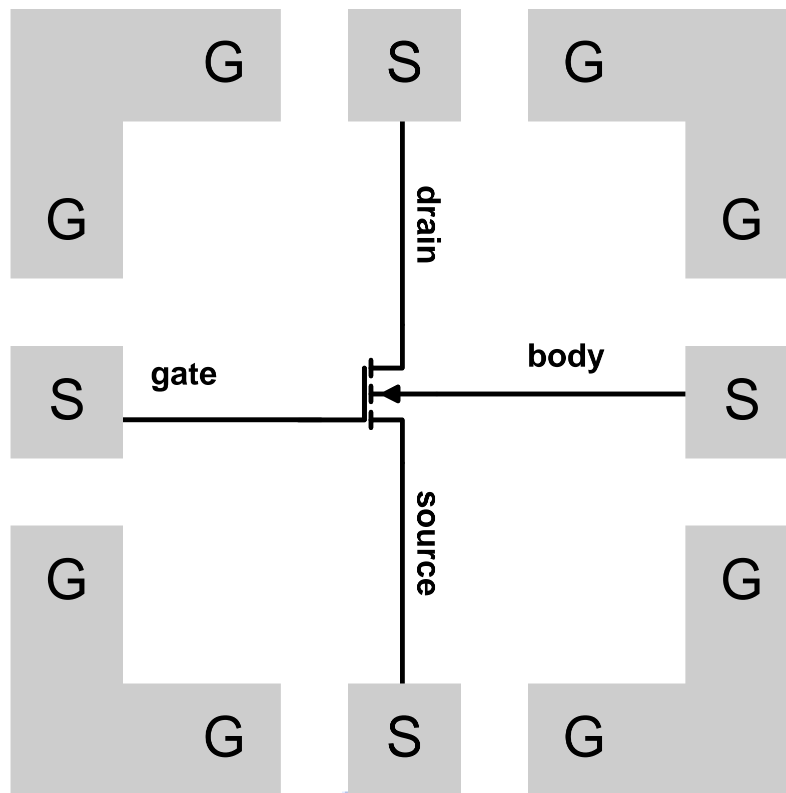
A conventional two-port test structure with a NMOSFET configured in common source mode was measured with two-port VNA. The dimension of this two-port NMOSFET is the same with the M2 ($7.2\mu m \times 4$) four-port counterpart. The measured two-port scattering parameters are compared to the two-port common source data conversed from the four-port scattering parameters of M2 device. The results are shown in Fig.3.23 and they rather agree with each other. However, devices in common gate and common drain configuration cannot be implemented by conventional two-port test structure as described in previous section, the comparisons similar to the common source case are absence.

3.6 Summary

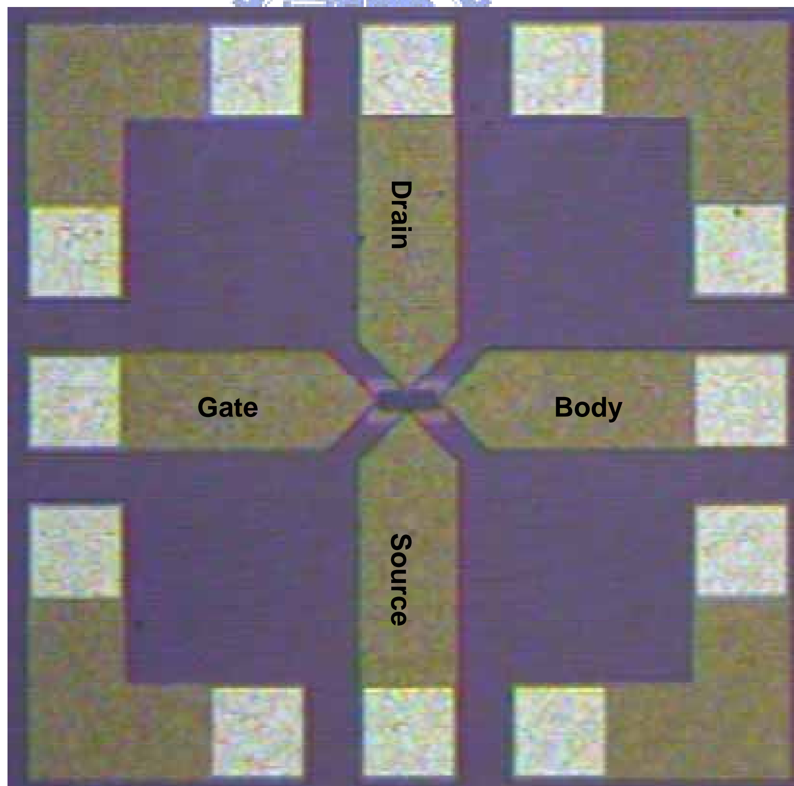
Four-port test structure for characterizing MOSFET's is presented in this chapter. The dummy structures including a special open dummy are also shown. The parasitic components of the proposed test structure and de-embedding procedures are clearly explained. Than the measured sixteen four-port scattering parameters are all illustrated by figures and explained in detail.

The theory and method of reducing four-port Y-parameters to two-port Y-parameters of MOSFET's in common source, common gate and common drain configurations is also demonstrated. The common source, common gate, and common drain data can be directly conversed from the measured four-port scattering parameter of the proposed test structure. Only one single DUT and one measurement procedure are needed to obtain these data. Three MOSFET's in different dimensions are characterized by 4-port measurement, and all the obtained parameters are scaled with the device dimensions.

In contrast with the limitation of a conventional 2-port test structure, the 4-port test structure will more powerful for fully characterizing MOSFET devices.



(a)



(b)

Fig.3.1 (a) Schematics of test structure and the RF MOSFET.

(b) The top view photograph of the test structure and the RF MOSFET.

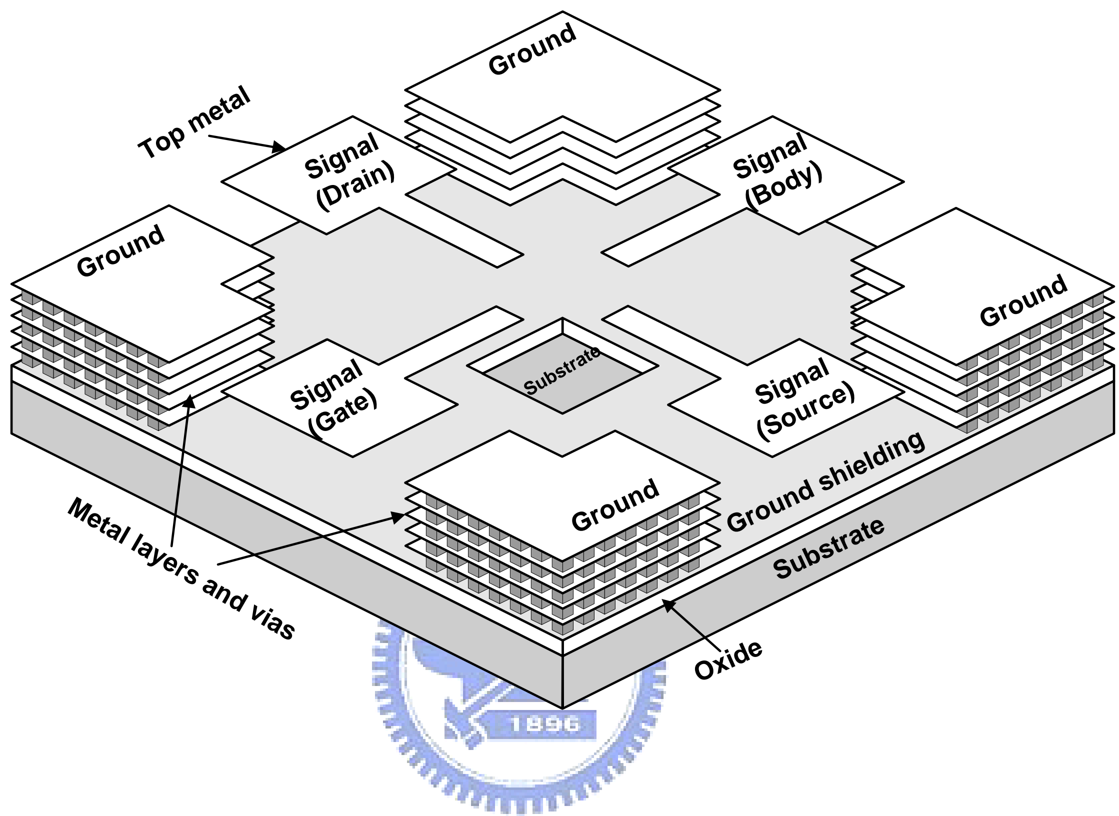


Fig.3.2 Test structure for the four-port measurement.

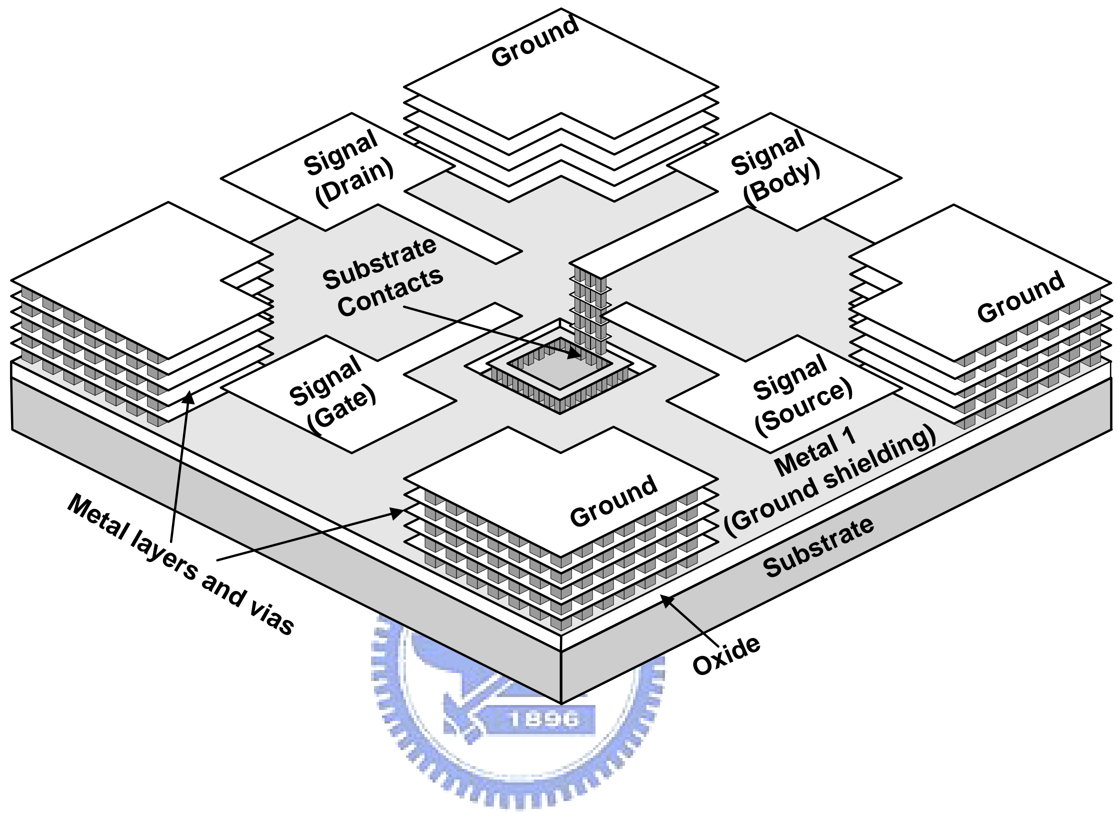


Fig.3.3 OPEN dummy structure for the four-port measurement.

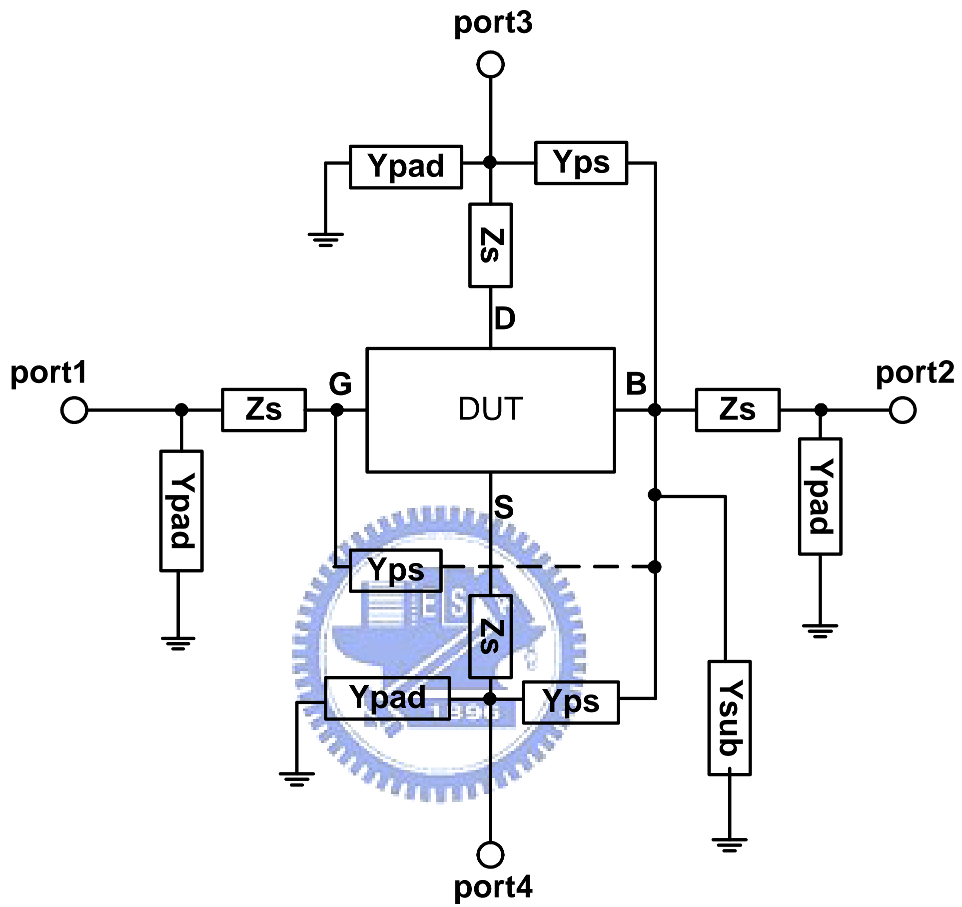


Fig.3.4 The equivalent circuit of the test structure.

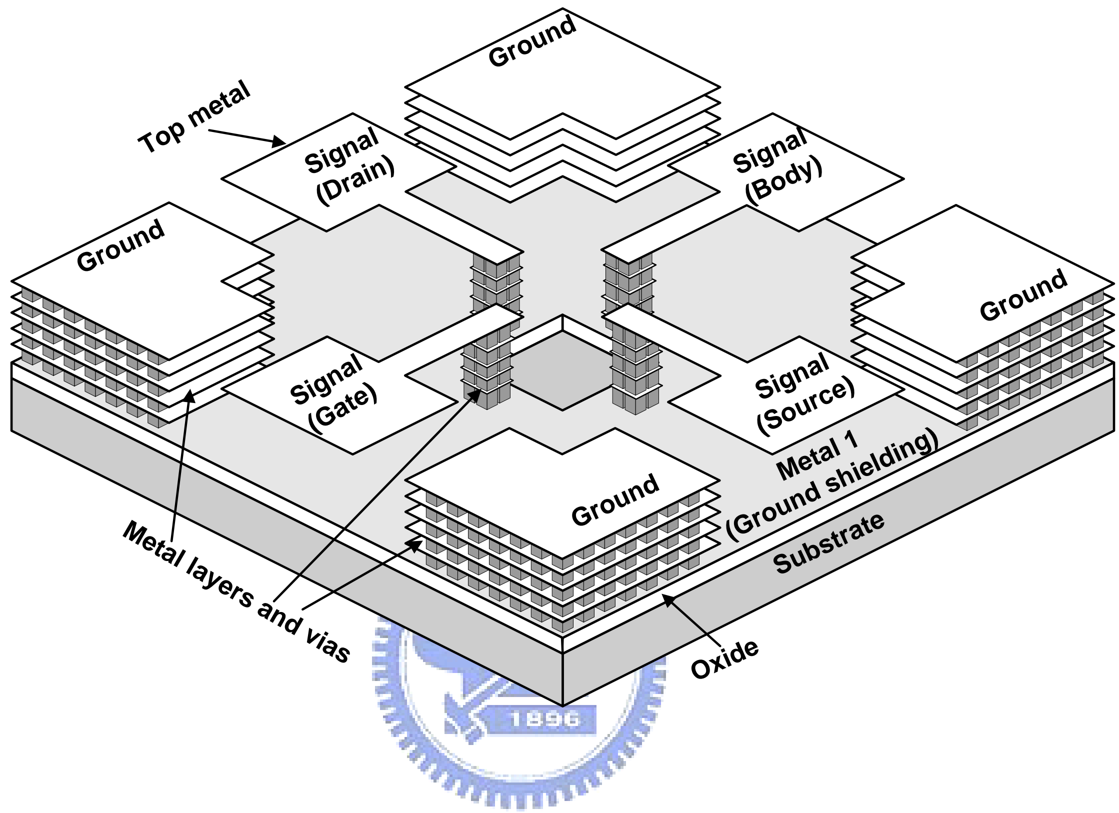


Fig.3.5 SHORT dummy structure for the four-port measurement.

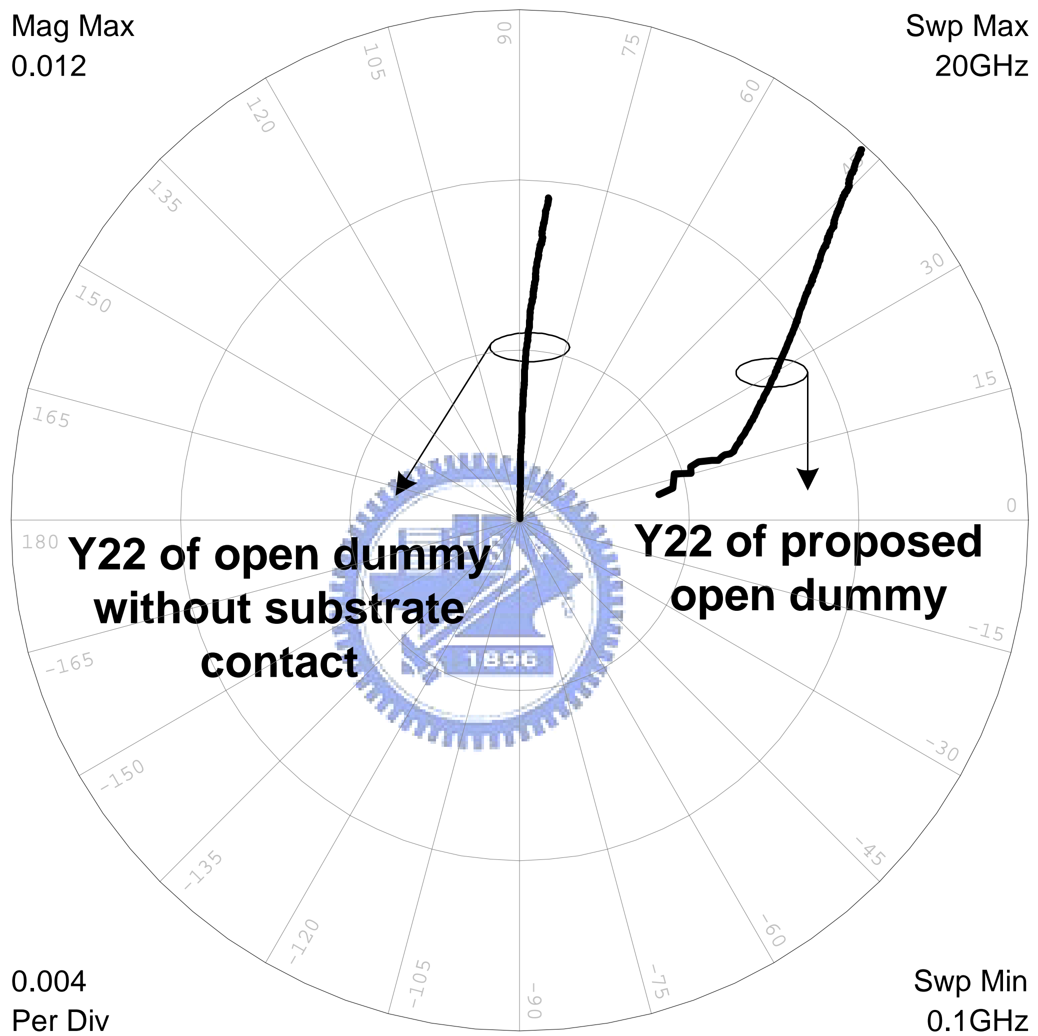


Fig.3.6 The difference of input admittance at port2 (body signal pad) between the open dummy shown in Fig.3.3 and an ordinary open dummy without substrate contact ring.

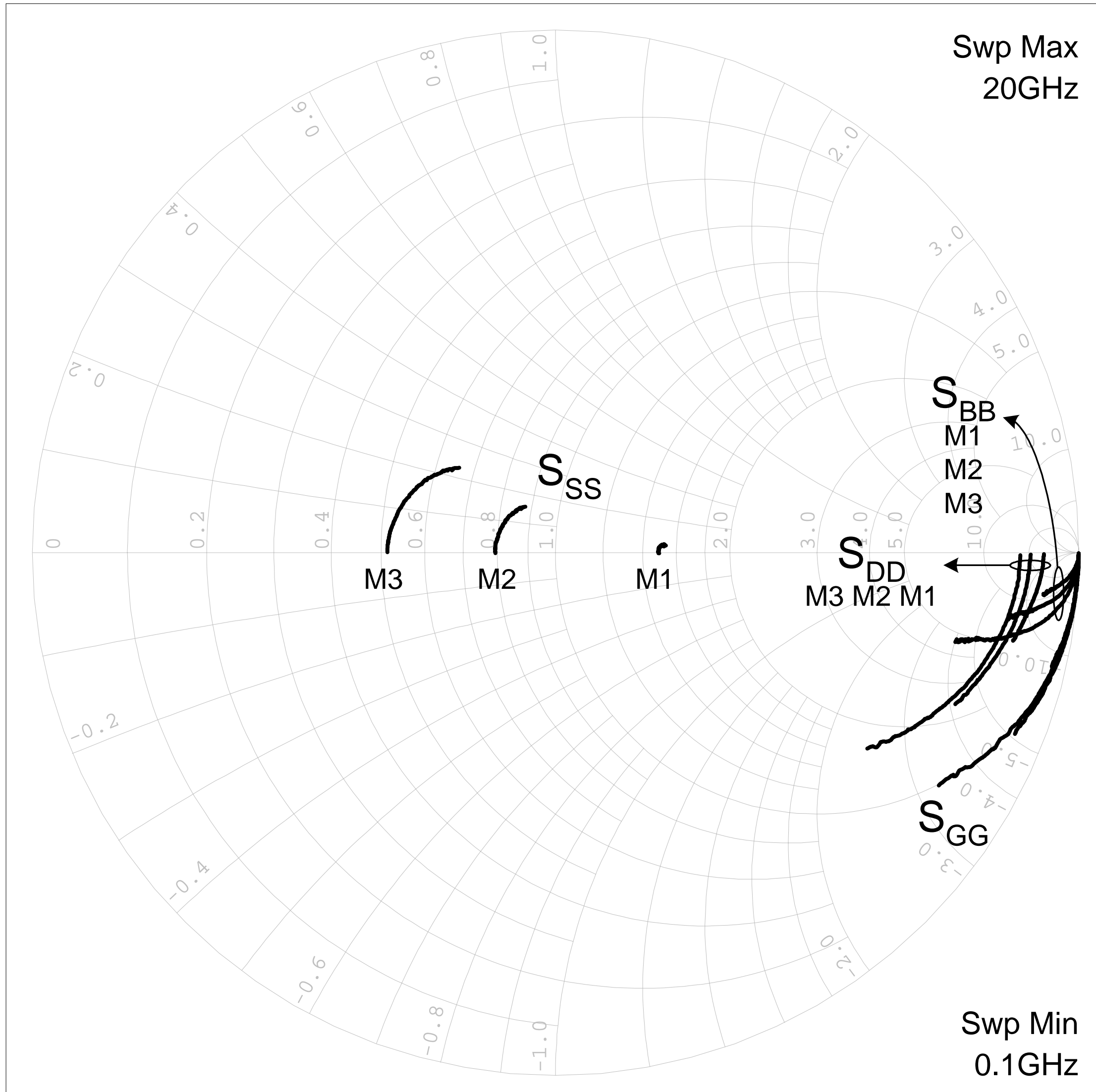


Fig.3.7 S_{GG}, S_{DD}, S_{SS}, and S_{BB} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

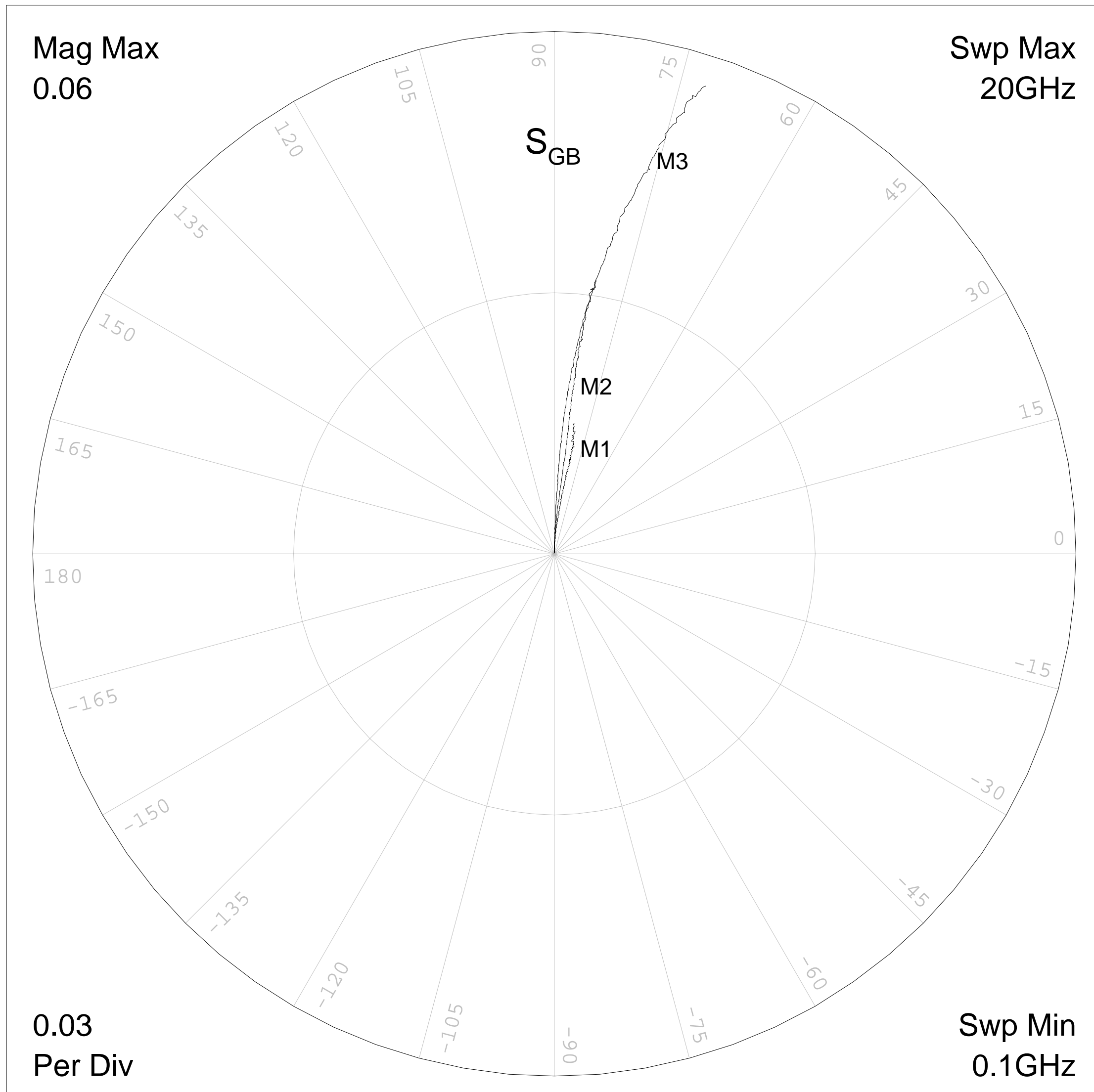


Fig.3.8 S_{GB} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

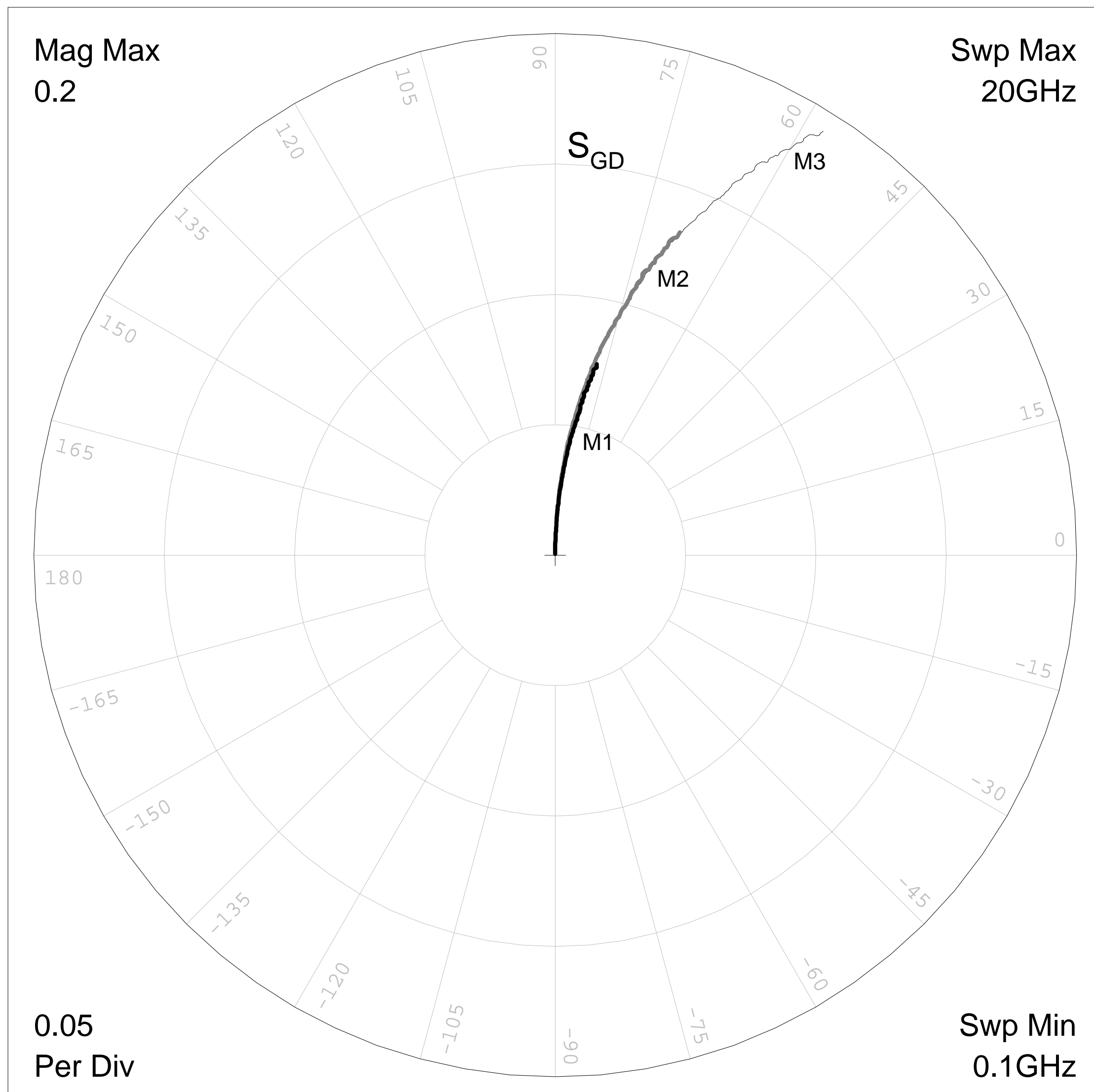


Fig.3.9 S_{GD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=1V.

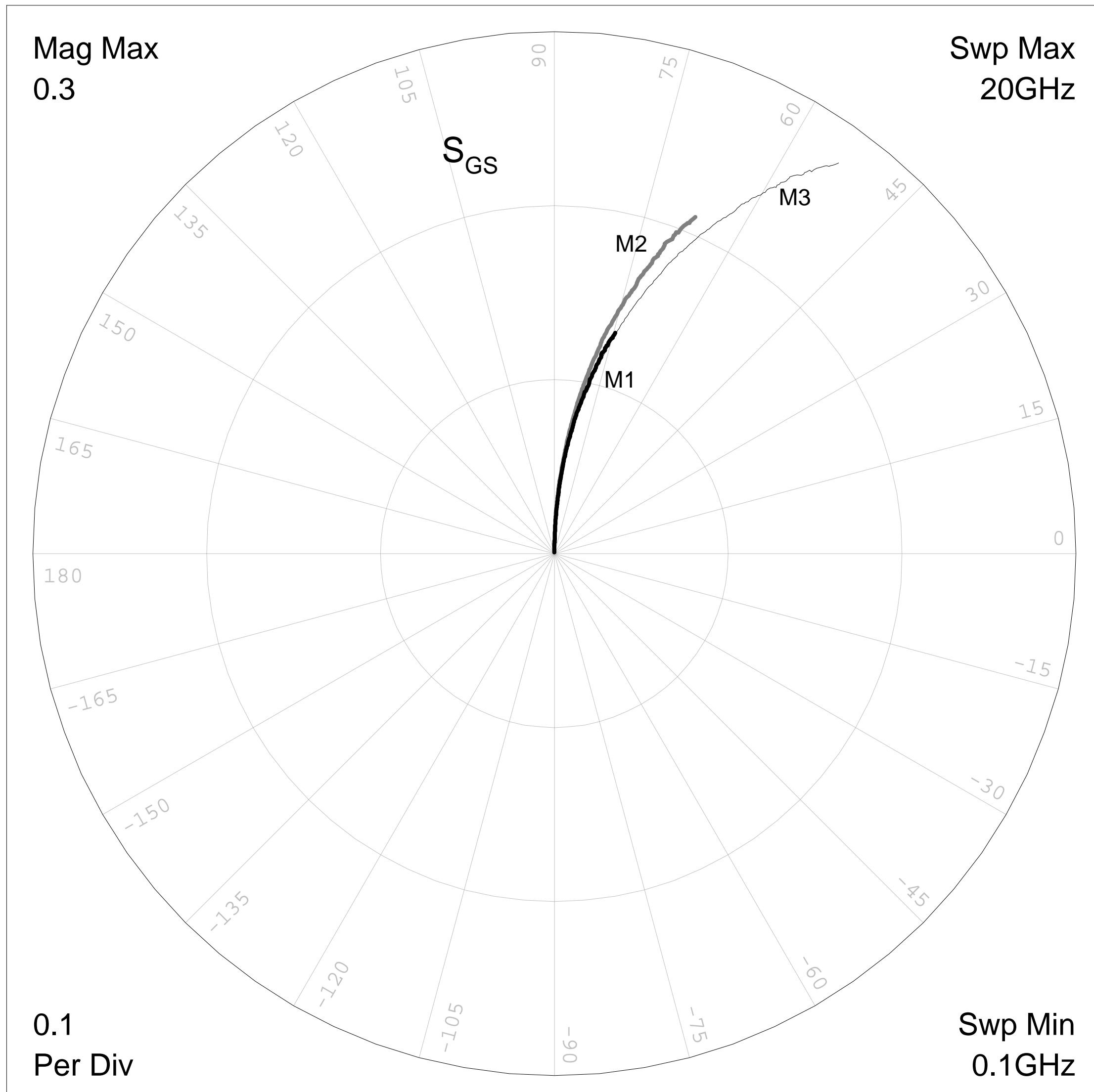


Fig.3.10 S_{GS} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

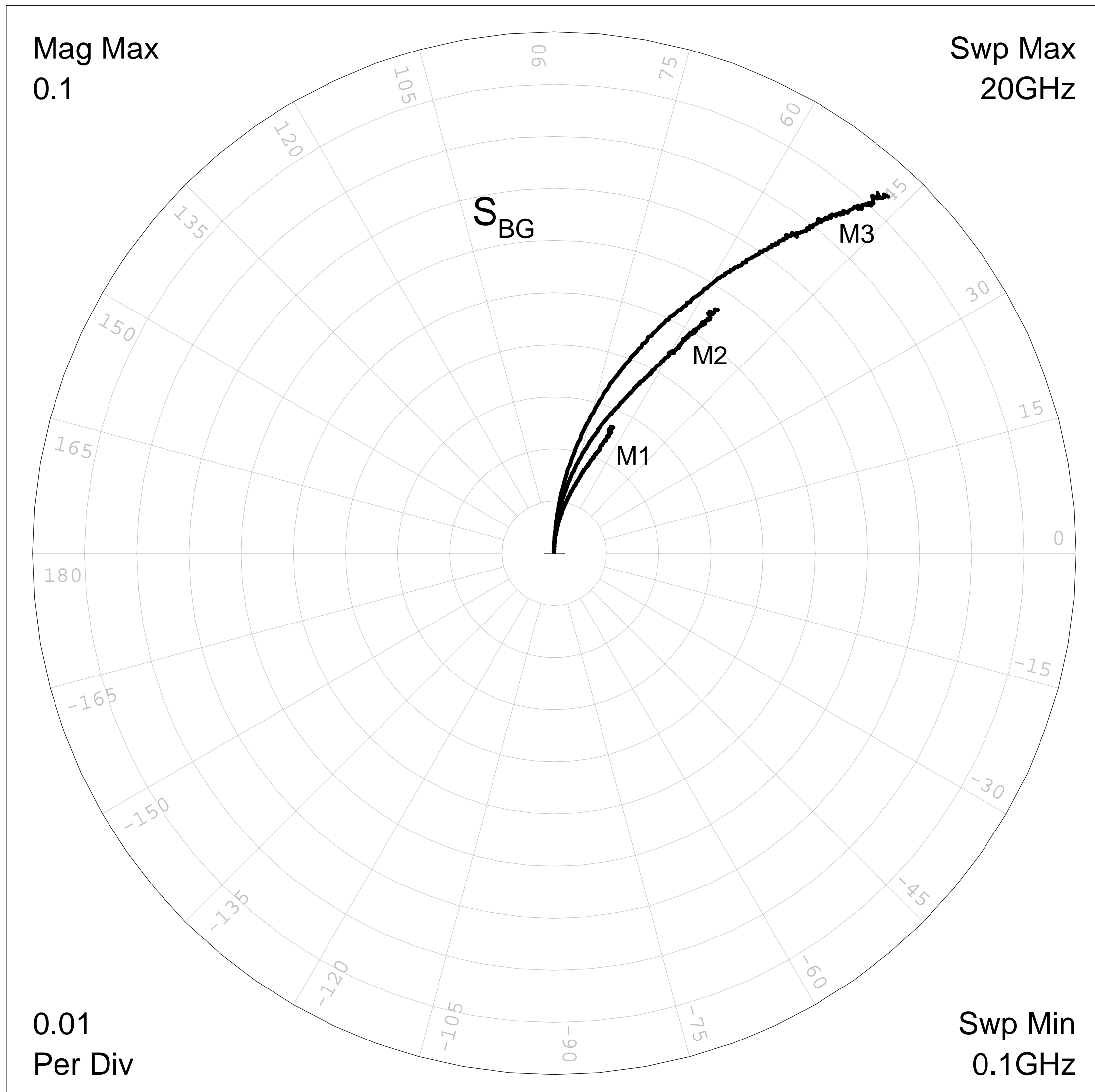


Fig.3.11 S_{BG} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

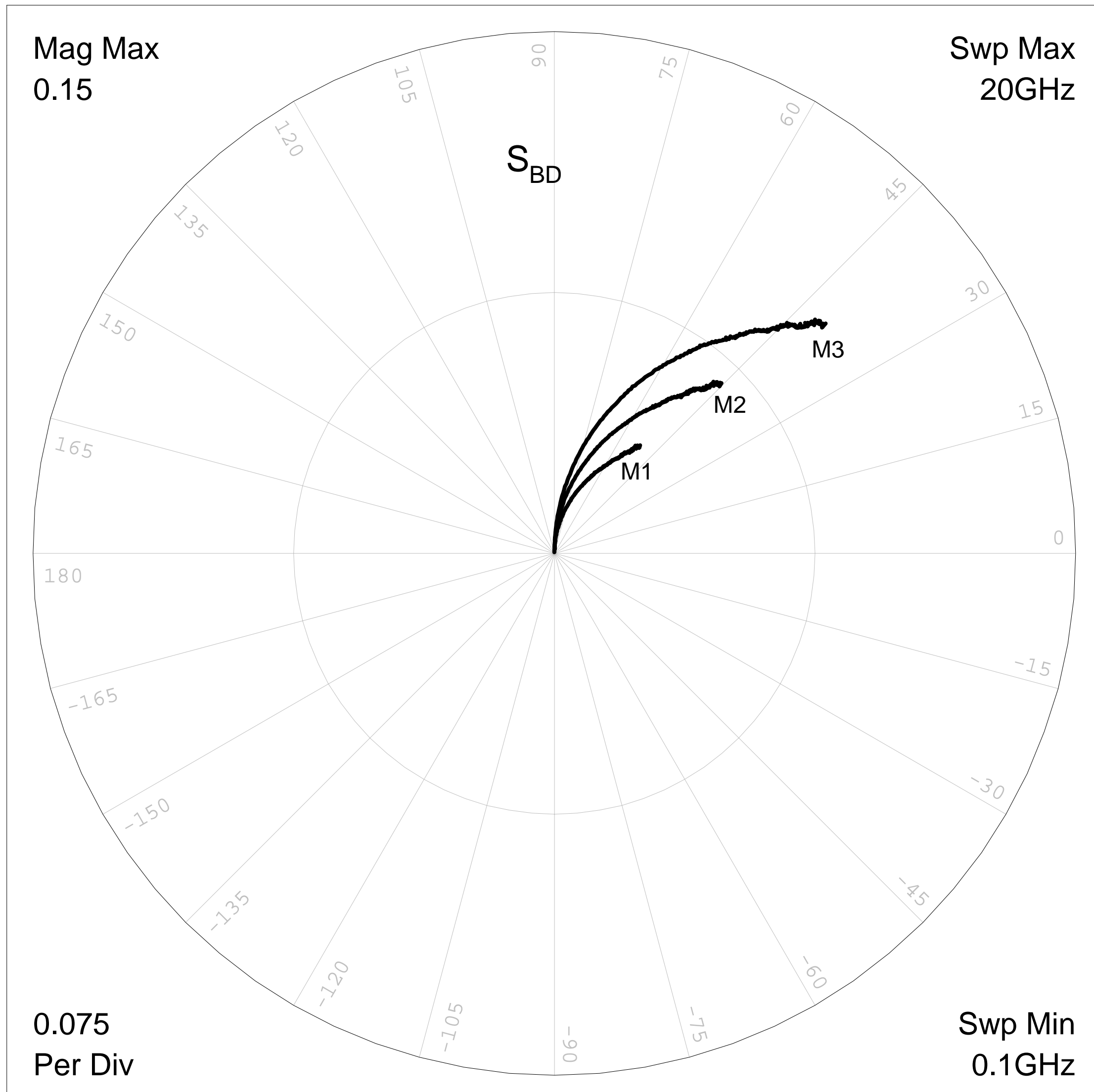


Fig.3.12 S_{BD} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

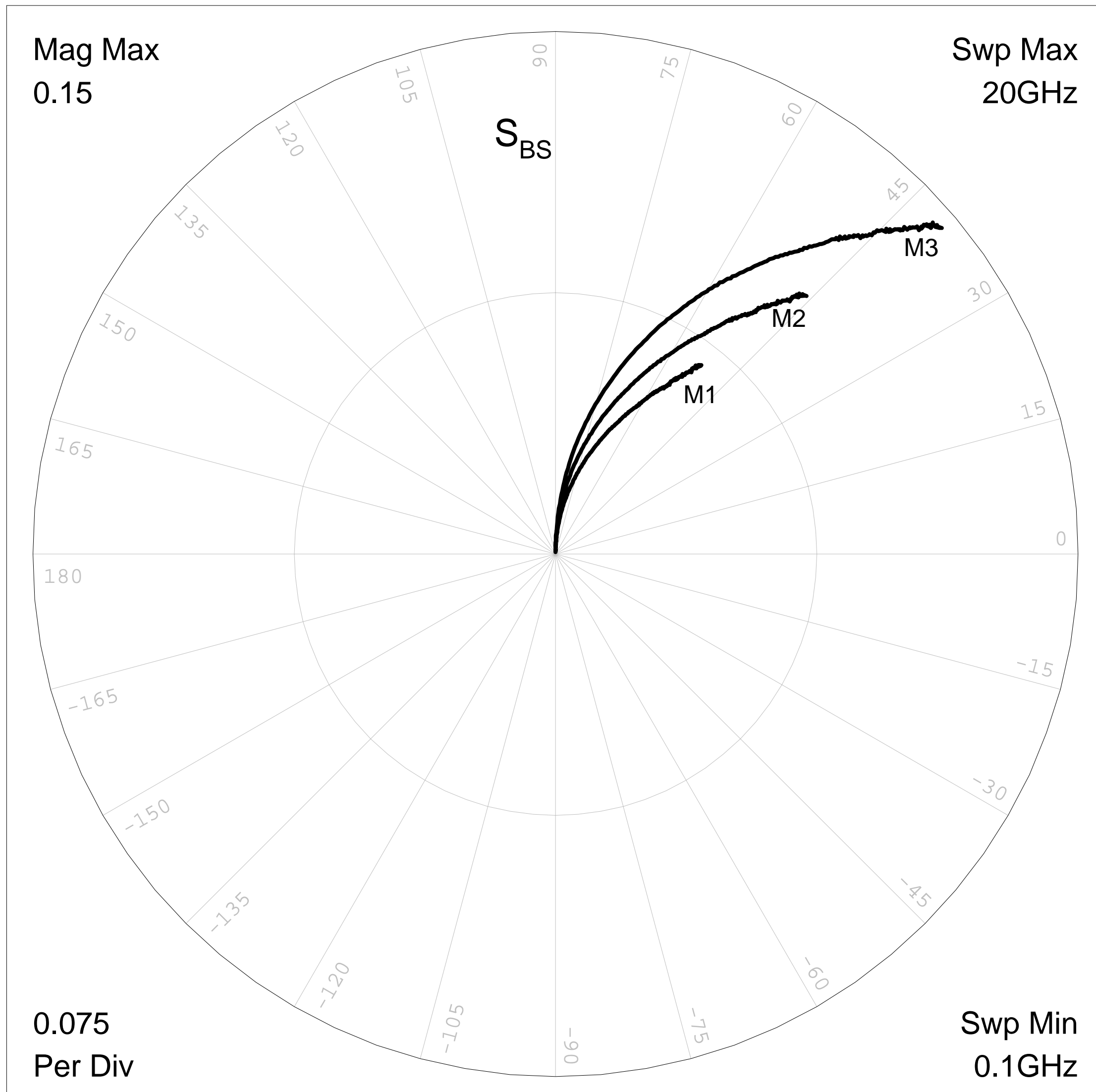


Fig.3.13 S_{BS} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

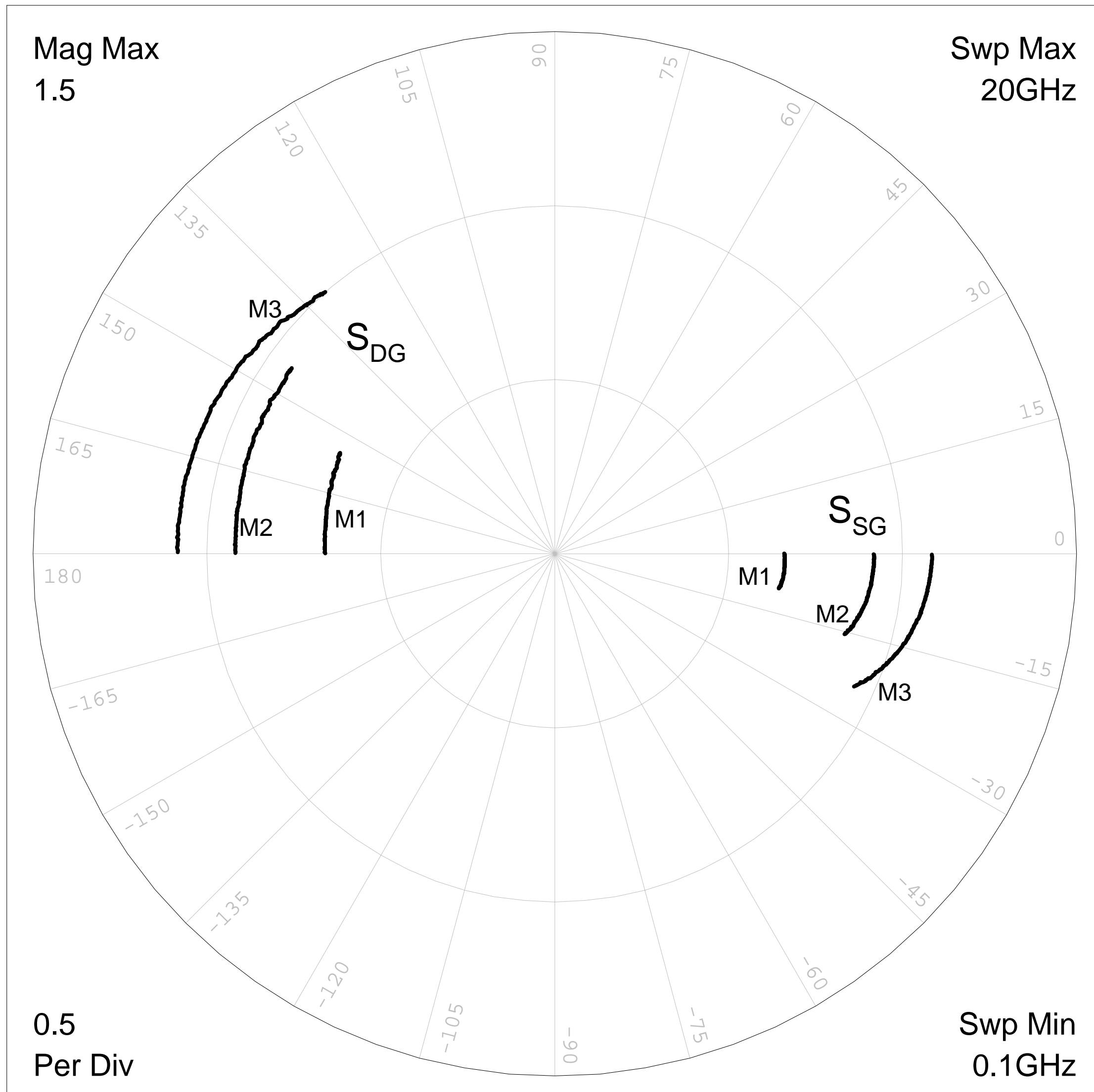


Fig.3.14 S_{DG} and S_{SG} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

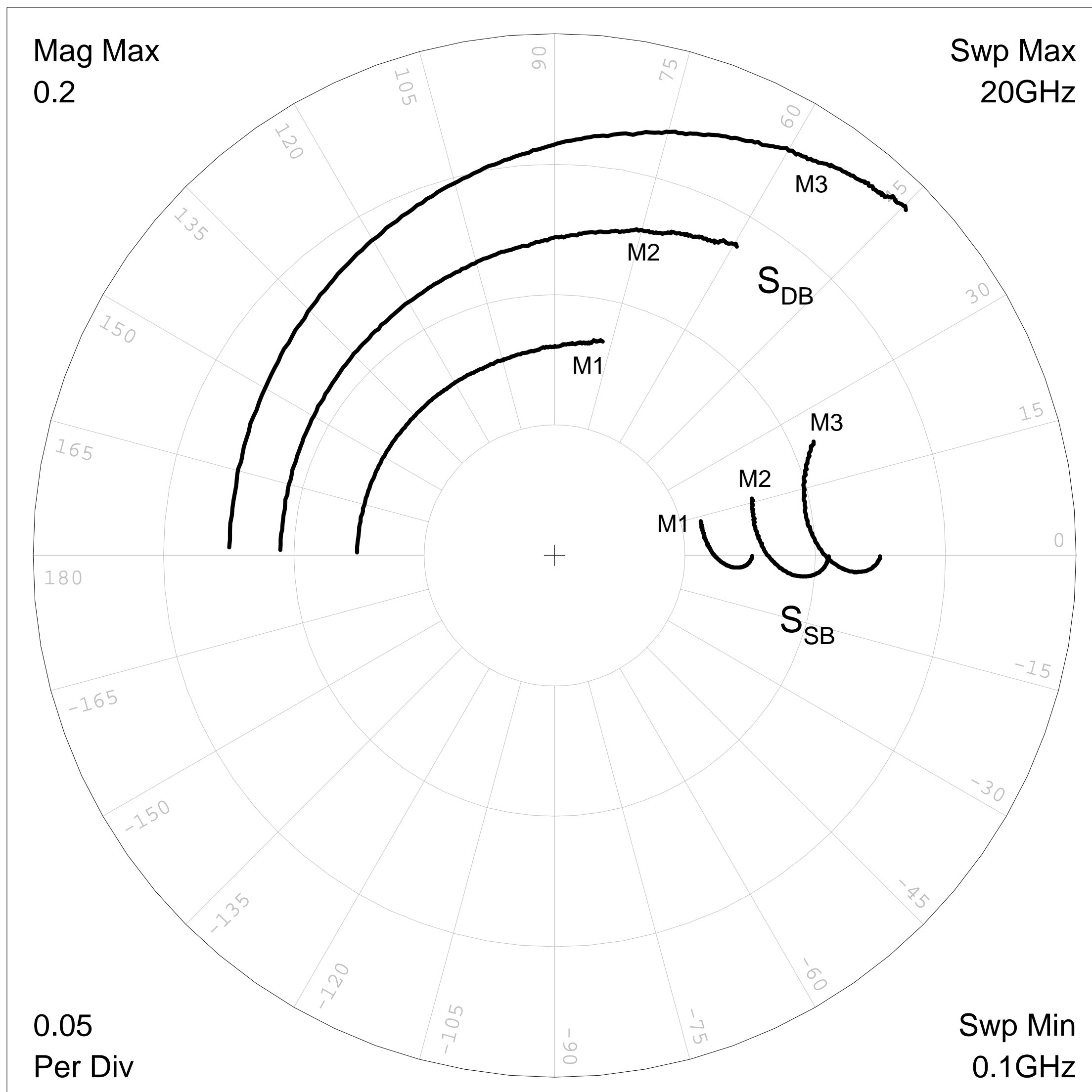


Fig.3.15 S_{DB} and S_{SB} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

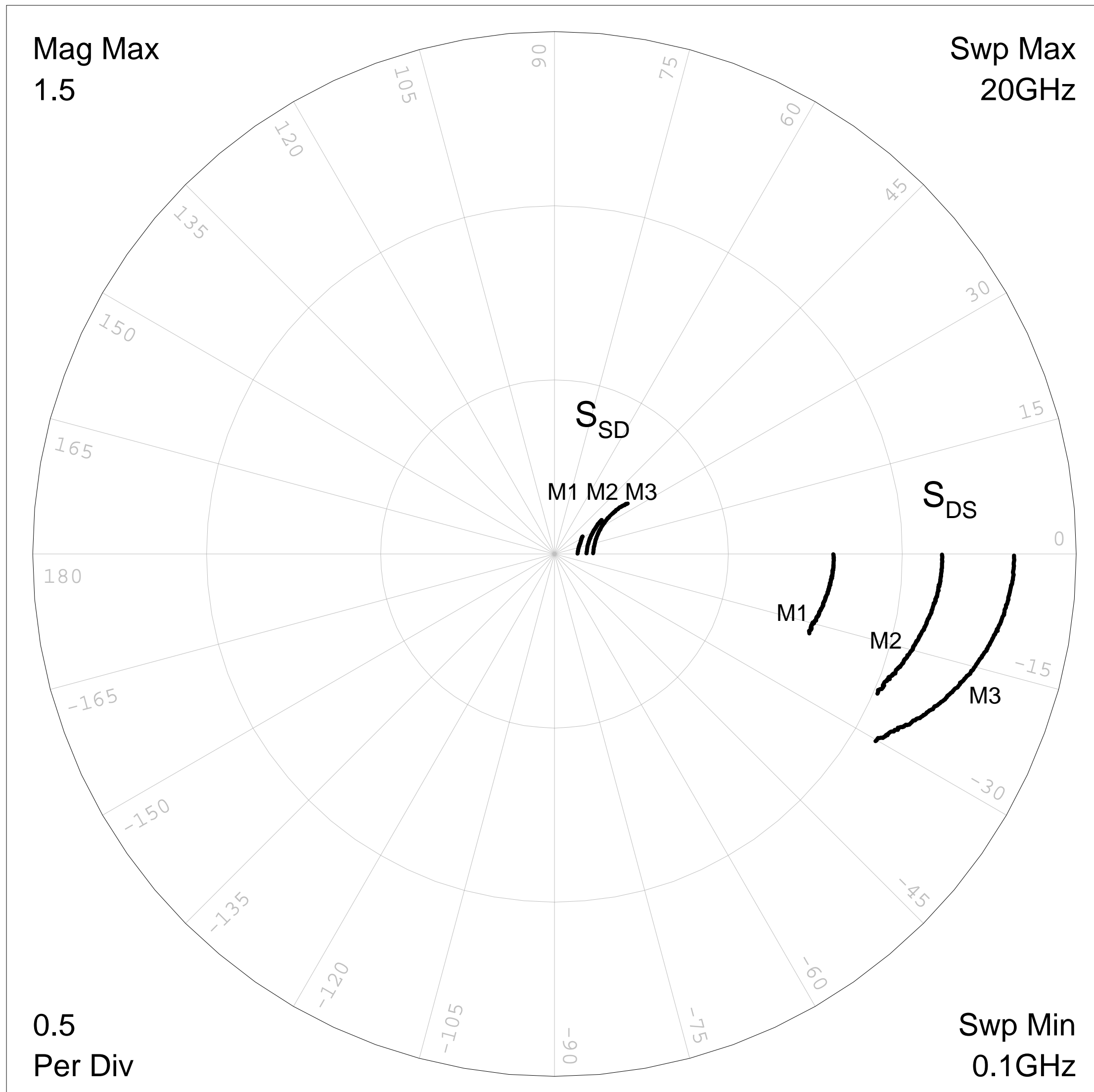


Fig.3.16 S_{SD} and S_{DS} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=1V.

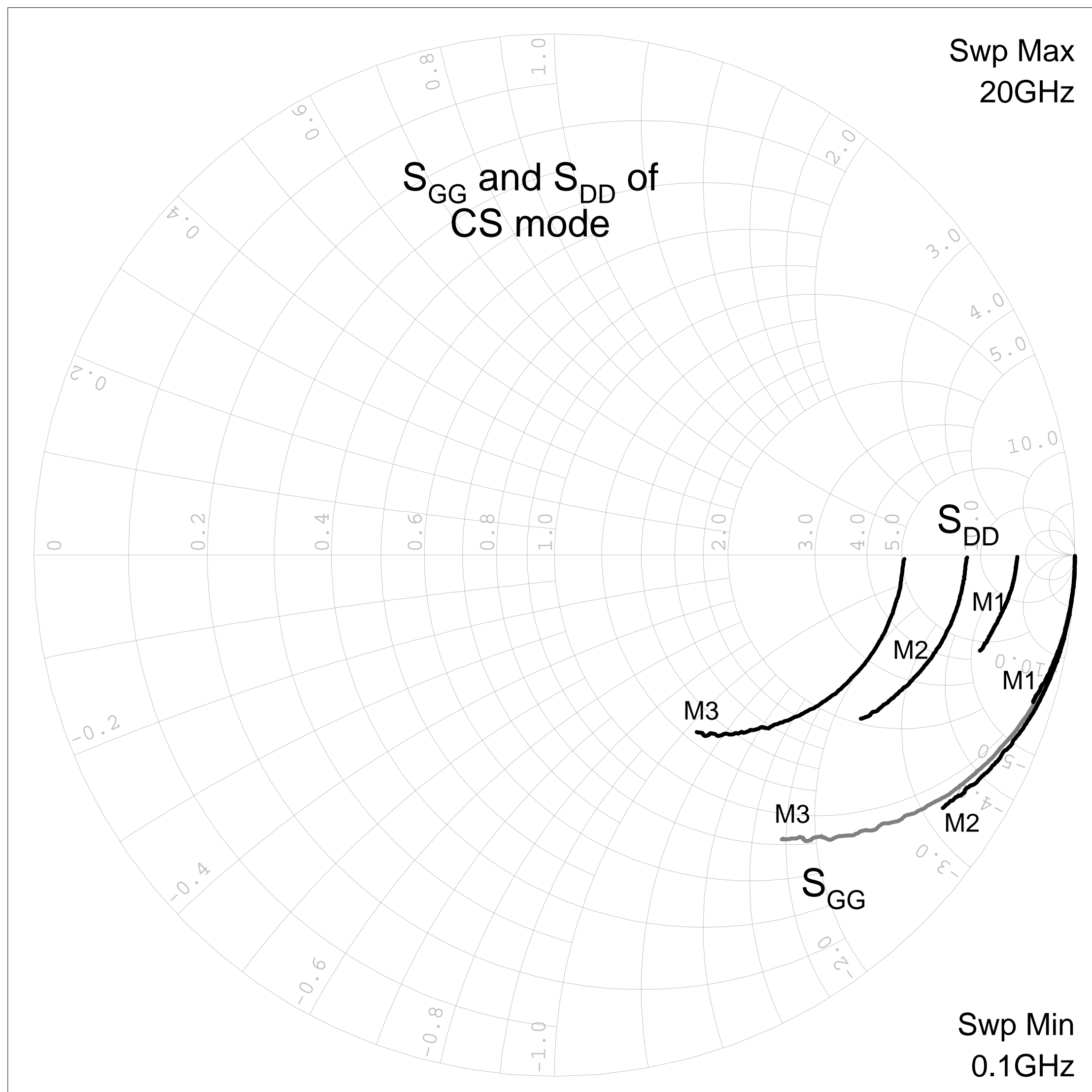


Fig.3.17 S_{GG} and S_{DD} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices in common source configuration, which are biased at VG=VD=1V.

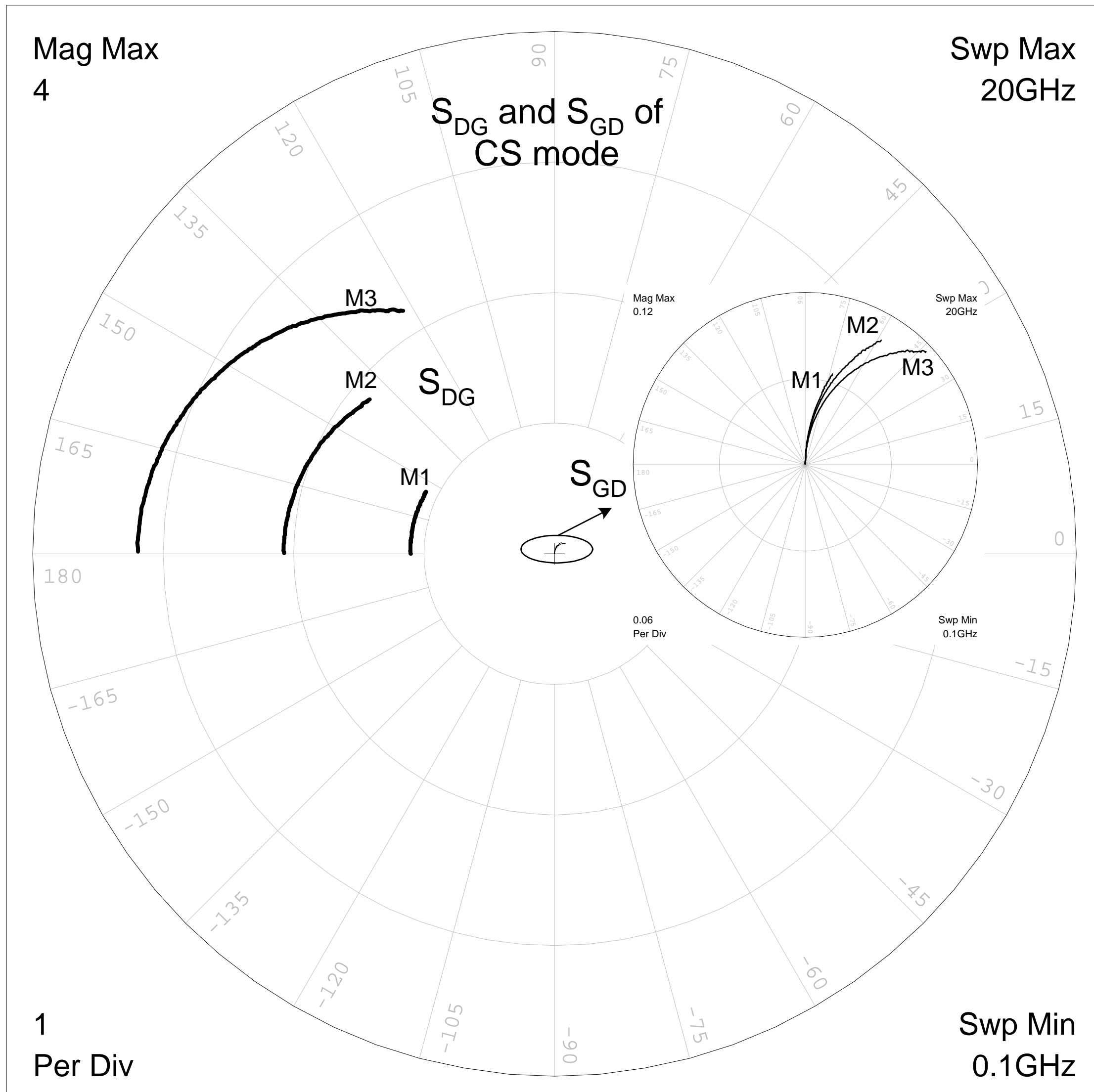


Fig.3.18 S_{DG} and S_{GD} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common source configuration, which are biased at VG=VD=1V.

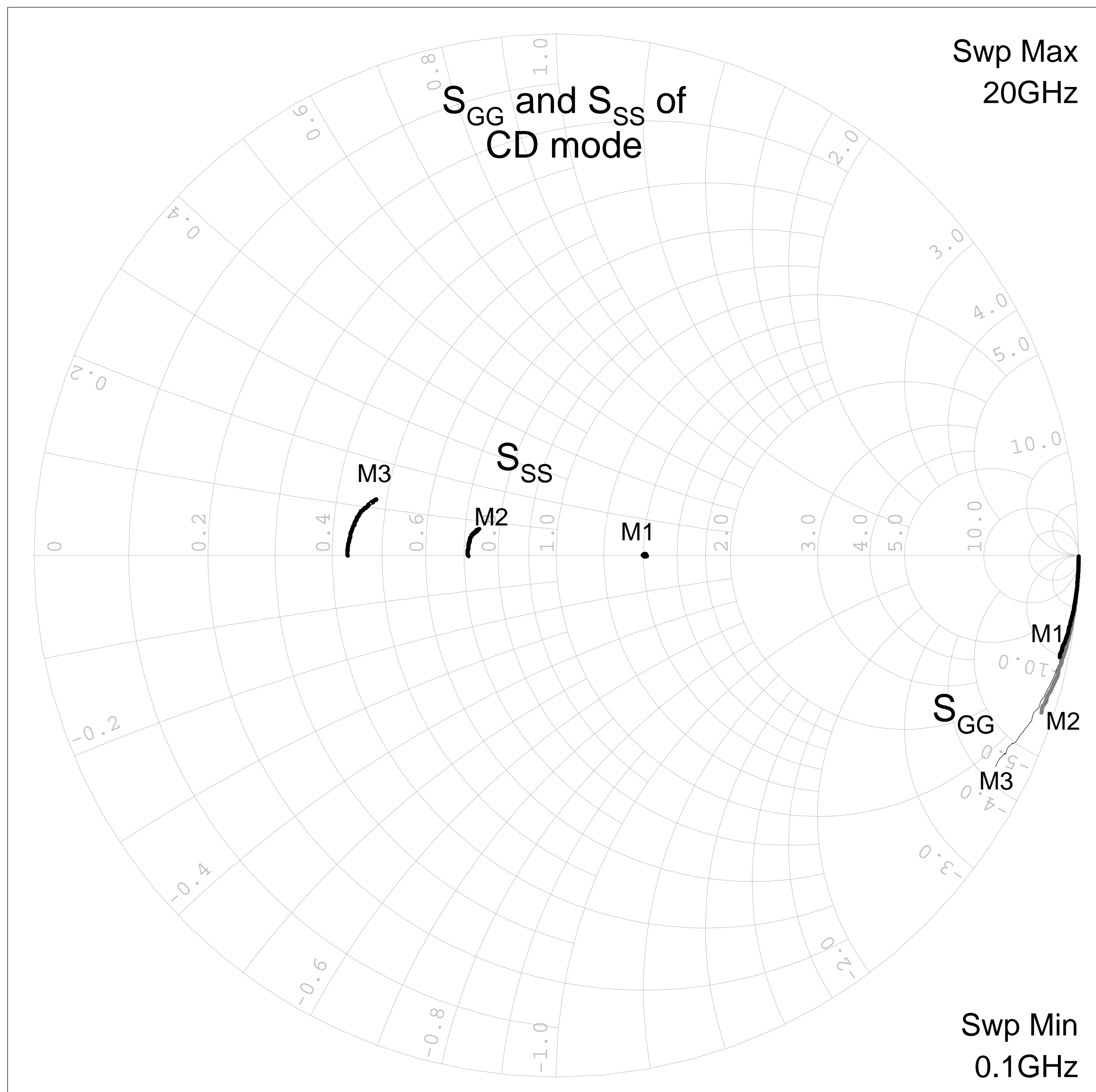


Fig.3.19 S_{GG} and S_{SS} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices in common drain configuration, which are biased at VG=VD=1V.

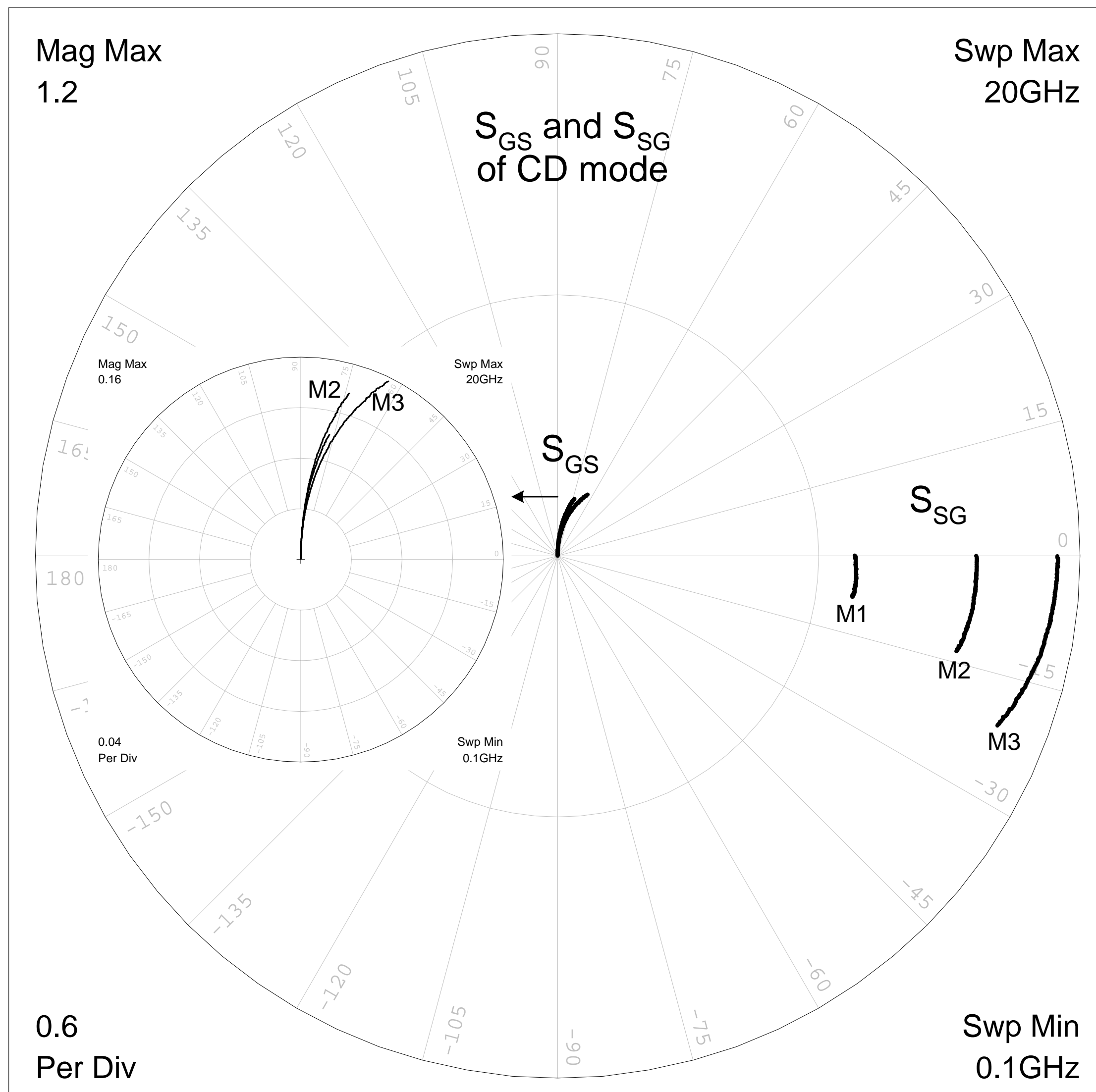


Fig.3.20 S_{GS} and S_{SG} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices in common drain configuration, which are biased at VG=VD=1V.

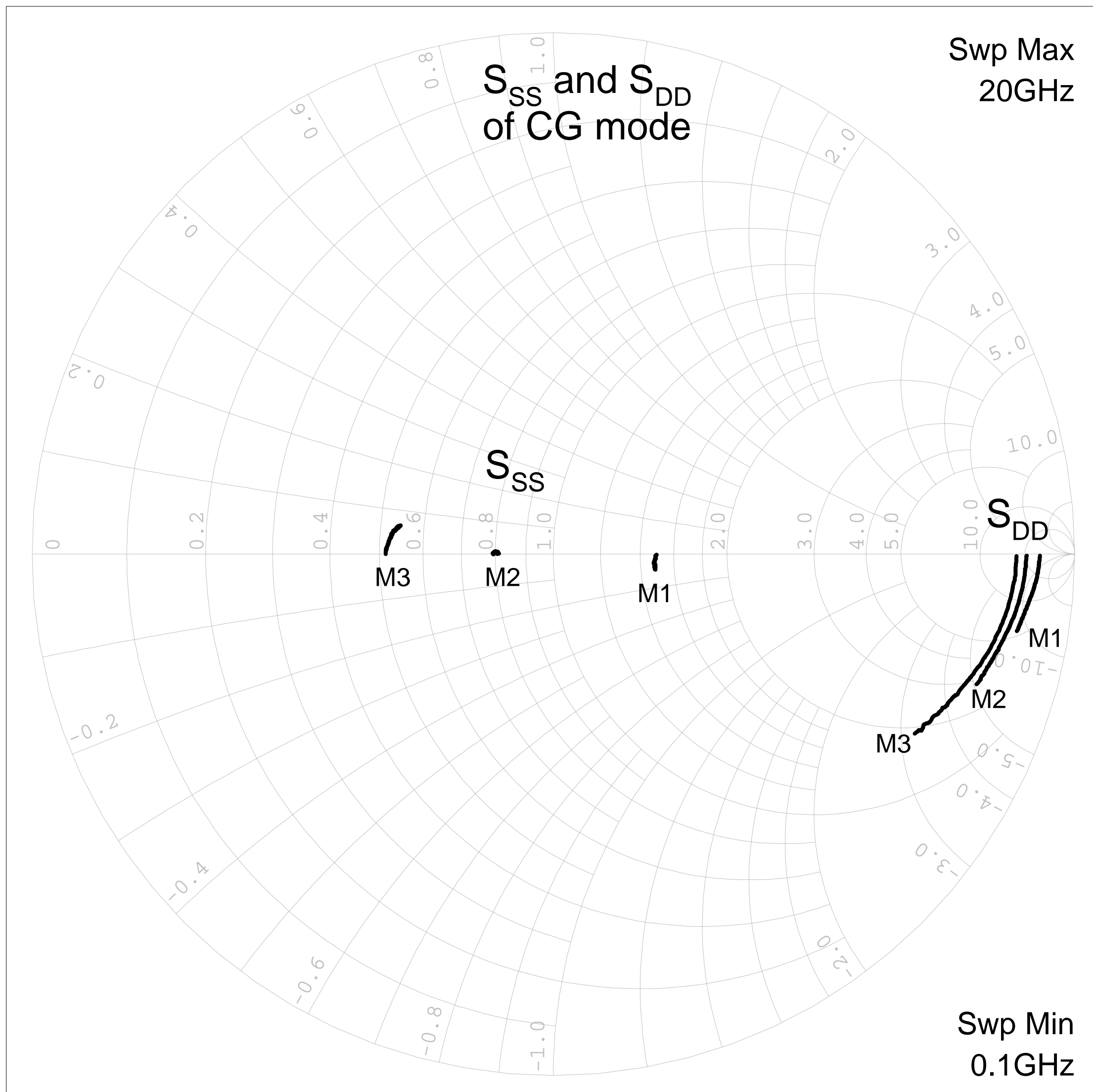


Fig.3.21 S_{SS} and S_{DD} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices in common gate configuration, which are biased at VG=VD=1V.

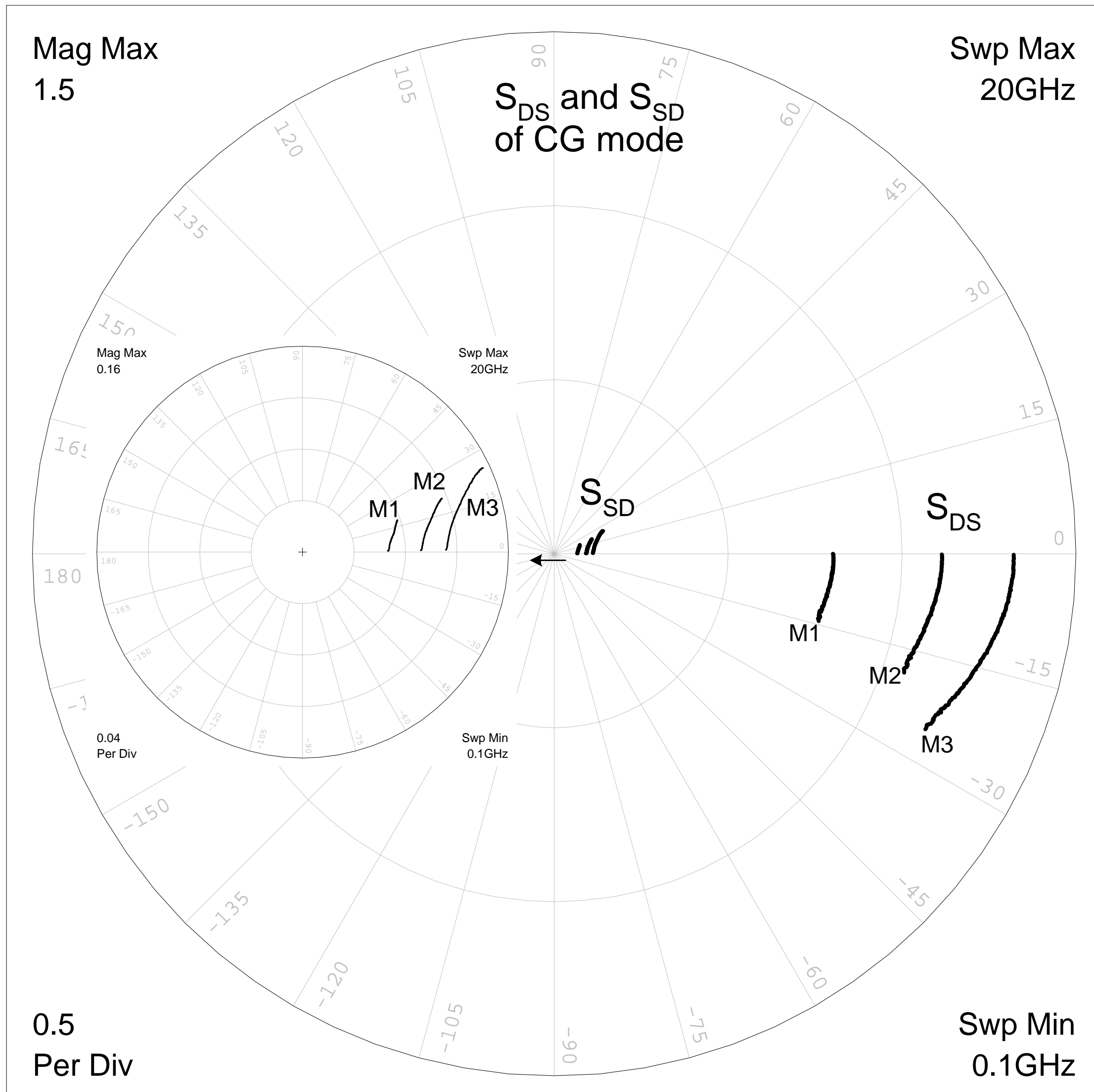


Fig.3.22 S_{DS} and S_{SD} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices in common gate configuration, which are biased at VG=VD=1V.

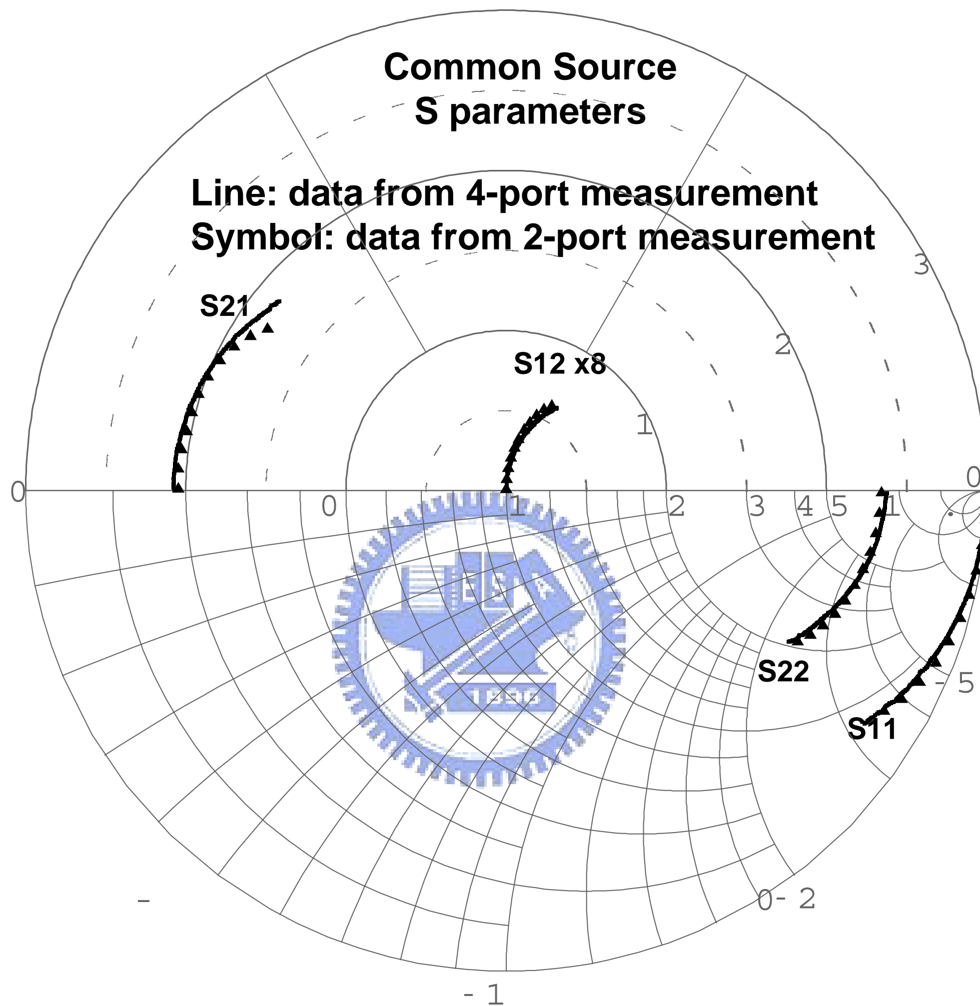


Fig.3.23 The common source S-parameters obtained from a 4-port NMOSFET and a conventional 2-port NMOSFET biased at VG=VD=1V. The gate widths of these two devices are $7.2\mu m \times 4$.

Chapter 4

Small-Signal Equivalent Circuit Model of RF MOSFET and Parameter Extraction

4.1 Motivation

Until not long ago, most RF circuits and systems have been implemented with either compound semiconductor transistor, such as GaAs MESFETs, HEMTs, HBTs, or silicon BJTs. The microwave properties of silicon MOSFET's were inferior to these high-frequency transistors. However, the continuous down-scaling of the CMOS technology has made it a candidate for RF applications. The 0.18μm CMOS technology exhibits nearly 50GHz of cut-off frequency and 0.5 dB of minimum noise figure at 2GHz operation frequency. The recent easily available 0.13 μm CMOS technology exhibits even higher cut-off frequency of 90GHz and lower minimum noise figure of 0.3 dB at 2.4 GHz operation frequency. These figures indicate excellent potential of the current CMOS technology for RF applications operating at several GHz.

In addition to its sufficient potential, the CMOS technology is very attractive as an RF technology because CMOS provides advantages such as low coast, high-level integration. Using the CMOS technology it is possible to integrate RF circuits, low-frequency analog circuits, and digital circuits in a single chip. However, differences between the RF MOSFET and conventional high-frequency transistors make it complicated and difficult to properly model an RF MOSFET. This, on the other hand, prevents using CMOS technology in RF circuit. The differences include substrate material and the device structure of the MOSFETs.

MOSFET's are fabricated on a silicon substrate, which has much lower resistivity than the gallium-arsenide substrate. The lower resistivity of silicon substrate results in larger and more

lossy parasitics related to substrate. In RF MOSFET's the influence of the distributed substrate resistance become significant as the operation frequency increases. At low frequencies, the impedance of the junction capacitance is very large that the substrate resistance may not be seen from the drain terminal. However, as the operation frequency increases, the impedance of the junction capacitance reduces and the effects of substrate resistance become apparent. At high frequencies, combined with the fact that the MOSFET is a four-terminal device, the signals in RF MOSFET's are coupled through the substrate R-C network in a complex way. The substrate signal coupling serious affects the small signal output characteristics, which are important for RF circuits design.

The convention high-frequency FET's have three terminals, a gate, a source, and a drain. However, the RF MOSFET has the fourth terminal, the body. The body is doped opposite to the source and drain regions to isolate theses two regions by reversed-biased p-n junctions. The basic concept of FET operation is to control the current flow between the source and drain by the electrical field induced from the gate voltage. In a MOSFET, the change in the body potential can also cause the change of drain current. This current control mechanism by body potential is very similar to that by gate voltage, although it is much less efficient than the control mechanism of gate voltage. Thus the MOSFET is essentially a four-terminal device. In many cases, the source and body of MOSFET are connected together. Even for this situation, the MOSFET is still a four-terminal device since the potential of the intrinsic body node is not the same as the potential of the extrinsic body. The source has the similar situation. With DC excitations, the almost negligible substrate current makes that the intrinsic and extrinsic body have almost the same potential. However, the source current is generally not negligible, so does the potential difference between intrinsic and extrinsic source nodes. With AC excitations, the AC body current becomes significant as the excitation frequency increases. The AC current come from drain, source, and gate will flow through entire substrate R-C network and make the potentials of intrinsic and extrinsic body nodes different.

It is more difficult to explain and predict the behavior of a four-terminal device than that of a three-terminal device; especially the four-terminal device is treated as a two-port network while using conventional characterizing techniques. The conventional two-port scattering parameters would not contain enough information to explore the interior components of a four-terminal device such as a RF MOSFET. In this chapter, the model of an RF MOSFET and extraction of corresponding parameters based on four-port scattering parameters is proposed.

4.2 Small-Signal Equivalent Circuits of RF MOSFET's

In most of the commercially available circuit simulators, MOS transistor models have been originally developed for digital and low frequency analog circuit design [26]-[27], which focus on the DC drain current, conductance, and intrinsic charge/capacitance behavior up to the megahertz range. However, as the operation frequency increases to the gigahertz range, the importance of the extrinsic components rivals that of the intrinsic counter-part. Therefore, a RF model with the consideration of the HF behavior of both intrinsic and extrinsic components in MOSFET's is important to achieve accurate and predictive results in simulation of a designed circuit. Compared with the MOSFET models for both digital and analog application at low frequency, compact models for high-frequency applications are more difficult to develop due to the additional requirements of bias dependence and geometry scaling of the parasitic components as well as the requirements of accurate prediction of the distortion and noise behavior. A common modeling approach for RF applications is to build sub-circuits based on the intrinsic MOSFET that has been modeled well for analog application [28]-[31]. The accuracy of such model depends on how to establish sub-circuits with the correct understanding of the device physics in high-frequency operation, how to model the

high-frequency behavior of intrinsic devices and extrinsic parasitics, and how to extract parameters appropriately for the elements of the sub-circuits. Since scattering-parameter measurement is the only practical method, and also the measurement method adopted in this study, to characterize the high-frequency performance of devices, circuits, and systems. Thus a RF model and its parameter extraction scheme had better be based on a small-signal model because the scattering-parameter measurement is a small-signal measurement.

Figure 4.1 shows the cross-sectional structure of a four-terminal MOSFET. It can be divided to intrinsic part and extrinsic part. The extrinsic part consists of all the parasitic components, such as the gate resistance R_G, gate/source overlap capacitance C_{GSO}, gate/drain overlap capacitance C_{GDO}, gate/bulk overlap capacitance C_{GBO}, source series resistance R_S, drain serious resistance R_D, source/bulk junction diode D_{SB}, drain bulk junction diode D_{DB}, and substrate resistances R_{SB}, R_{DB}, and R_{DSB}. The intrinsic part is the core of the device without including those parasitics. Even though it is desirable to design and fabricate MOSFETs without these parasitics, they cannot be avoided in reality. Some of them may not be noticeable in DC and low frequency operation. However, they will influence the device performance significantly at high frequency. Equivalent circuits have been an effective approach to analyze the electrical behavior of a device by representing the above components. Figure 4.2 shows the proposed small signal equivalent circuit of the four-terminal RF MOSFET including the intrinsic and extrinsic part. The R_G, R_S, R_D, R_{SB}, R_{DB}, and R_{SDB} are correspondent to the components shown in Fig.4.1. The C_{GS} including the intrinsic capacitance C_{GSI} not shown in Fig.4.1 and the extrinsic gate/source overlap capacitance C_{GSO}. It can be expressed as Eq.4-1.

$$C_{GS} = C_{GSI} + C_{GSO} \tag{4-1}$$

Similarly, the C_{GD} includes the intrinsic and extrinsic parts and can be expressed as Eq.4-2.

$$C_{GS} = C_{GSI} + C_{GSO} \tag{4-2}$$

The C_{DB} and C_{SB} in Fig. 4.2 represent the junction capacitances of the reversed source/bulk

and drain/bulk junctions. In addition to the C_{DB} and C_{SB}, there exist two capacitance components, C_{SBE}, C_{DBE} between source/bulk and drain/bulk which are not arisen from the junction capacitances but caused by metal connections or other parasitic capacitances between source/bulk and drain/bulk. Between gate and bulk, there exists an overlap capacitance, C_{GBE}, which is caused by the metal connections and independent of bias condition. In addition to C_{GBE}, there is also a capacitance arisen from the gate oxide and will be in-series with a resistance substrate component, R_{GB}.

The four voltage-controlled current source can be expressed as:

$$I_m = \left(g_m - j\omega C_m\right) v_{GSi} \tag{4-3}$$

$$I_{ms} = \left(g_{mb} - j\omega C_{mb}\right) v_{BSi} \tag{4-4}$$

$$I_{md} = \left(g_{ds} + j\omega C_{SDi}\right) v_{DSi} \tag{4-5}$$

$$I_{mx} = j\omega C_{mgb} v_{GBi} \tag{4-6}$$

The g_m, g_{mb}, and g_{ds} are the transconductance, bulk transconductance, and channel conductance of the device respectively. C_m is the transcapacitance between the gate and drain terminal. C_{mb} is the transcapacitance between the drain and body terminal. C_{mgb} is the transcapacitance between the gate and body terminal. These transcapacitances can be expressed as Eq.4-7, Eq.4-8, and Eq.4-9.

$$C_m = C_{DGi} - C_{GDi} \tag{4-7}$$

$$C_{mb} = C_{DBi} - C_{BDi} \tag{4-8}$$

$$C_{mgb} = C_{GBi} - C_{BGi} \tag{4-9}$$

These transcapacitances arise from the operation of the MOSFET. For example, if a small-signal voltage is applied at the drain, the resulting small-signal current entering the gate will be $-C_{GD}(dv_d/dt)$. C_{GD} actually represent the effect of drain terminal on gate terminal. However, although the capacitance C_{GD} is connected between gate and drain, it does not

model the total effect of gate on drain. Since if a small-signal voltage is applied at the gate, the amount of charge in the inversion layer will be changed, which will also change the small-signal drain current. The small-signal current entering the drain indeed is $g_m v_g - (C_{GD} + C_m)(dv_g/dt)$. Note that not only is there a conductive current but also a capacitive current different form $-C_{GD}(dv_d/dt)$. Thus $C_{GD} + C_m$ represent the effect of gate on drain and is different from C_{GD}. C_m is an element models the different effect of the gate and drain on each other in terms of charging currents [32].

4.3 parameter extraction

4.3.1 Extraction of Extrinsic Parasitic Components in the Equivalent circuit of Cold MOSFET's

The intrinsic part or say the voltage-controlled current sources of a MOSFET will exist only if the device is biased properly. Considering a MOSFET with no DC bias applied, the intrinsic part of the MOSFET will vanish. The remained components in the small-signal equivalent circuit will be the extrinsic part of the device. The equivalent circuit shown in Fig.4.2 then can be simplified by removing the voltage-controlled current sources and becomes the equivalent circuit shown in Fig.4.3. Below a certain operation frequency range, an assumption is given that the values of R_S and R_D are much smaller than the impedance of C_{GSO}, C_{GDO}, C_{SBO}, C_{DBO}, and C_{GBO}. According to this assumption, R_S and R_D can be neglected while the test frequency below a certain value. Therefore, the equivalent circuit in Fig.4.3 was further simplified to the circuits in Fig.4.4. The y-parameters of this equivalent circuit can be easily derived according the definition. There will be sixteen y-parameters and nine of them are independent for a four-terminal circuit. However, since this is an equivalent circuit consists of passive

components, it is reciprocal. The transadmittances between any two terminals in both directions will equal to each other. Therefore, only six of the sixteen y-parameters are independent, another ten can be derived from these six y-parameters. Five independent and one dependent y-parameters of the equivalent sown in Fig4.4 were derived as below.

$$Y_{GG} = \left(R_G + \left(j\omega\left(C_{GSO} + C_{GDO} + C_{GBE}\right) + \frac{j\omega C_{GBO} + \omega^2 C_{GBO}{}^2 R_{GB}}{1 + \omega^2 C_{GBO}{}^2 R_{GB}{}^2} \right)^{-1} \right)^{-1} \quad (4\text{-}10)$$

$$Y_{SG} = -\left(R_G + \left(j\omega\left(C_{GSO} + C_{GDO} + C_{GBE}\right) + \frac{j\omega C_{GBO} + \omega^2 C_{GBO}{}^2 R_{GB}}{1 + \omega^2 C_{GBO}{}^2 R_{GB}{}^2} \right)^{-1} \right)^{-1} \times \frac{C_{GSO}}{C_{GSO} + C_{GDO} + C_{GBO}} \quad (4\text{-}11)$$

$$Y_{DG} = -\left(R_G + \left(j\omega\left(C_{GSO} + C_{GDO} + C_{GBE}\right) + \frac{j\omega C_{GBO} + \omega^2 C_{GBO}{}^2 R_{GB}}{1 + \omega^2 C_{GBO}{}^2 R_{GB}{}^2} \right)^{-1} \right)^{-1} \times \frac{C_{GDO}}{C_{GSO} + C_{GDO} + C_{GBO}} \quad (4\text{-}12)$$

$$Y_{GB} = -\left(Y_{GG} + Y_{SG} + Y_{DG}\right) \quad (4\text{-}13)$$

Since the equivalent circuit is reciprocal, the Y_{BD} and Y_{BS} will equals to Y_{DB} and Y_{SB}. If a test voltage source was placed at body terminal, it will be foreseen that the R_{DSB} can be neglected while calculating Y_{DB} and Y_{SB} since the voltage drop across R_{DSB} is neglected. According to simulation results, it's also found that the R_{DSB} has minor effect on Y_{BD} and Y_{BS}. Therefore, it was neglected while deriving the Y_{BD} and Y_{BS} and the resulting expression are shown in Eq.4-14 and Eq.4-15.

$$Y_{BD} = -\left(j\omega C_{DBE} + \frac{j\omega C_{DBO} + \omega^2 C_{DBO}{}^2 R_{DB}}{1 + \omega^2 C_{DBO}{}^2 R_{DB}{}^2} \right) \quad (4\text{-}14)$$

$$Y_{BS} = -\left(j\omega C_{SBE} + \frac{j\omega C_{SBO} + \omega^2 C_{SBO}{}^2 R_{SB}}{1 + \omega^2 C_{SBO}{}^2 R_{SB}{}^2} \right) \quad (4\text{-}15)$$

Equations 4-10 to 4-15 are the exact expression of the six corresponding y-parameters of the equivalent circuit. However, the expanding expression will very complex and enormous to

solve the contained components. Therefore, further simplification is required. At appropriate frequencies, it can be assumed that the higher order terms of $\omega C_x R_x$ are neglected while compared with the constant one and first order terms in these equations. Then the Y_{GG}, Y_{SG}, Y_{DG} can be simplified to Eq.4-17 to Eq.4-19.

$$Y_{GG} \approx j\omega\left(C_{GSO}+C_{GDO}+C_{GBO}+C_{GBE}\right)+(C_{GSO}+C_{GDO}+C_{GBO}+C_{GBE})^2 R_G \quad (4\text{-}17)$$

$$Y_{SG} \approx -j\omega C_{GSO}-\omega^2 C_{GSO}\left(C_{GSO}+C_{GDO}+C_{GBO}\right)R_G \quad (4\text{-}18)$$

$$Y_{DG} \approx -j\omega C_{GDO}-\omega^2 C_{GDO}\left(C_{GSO}+C_{GDO}+C_{GBO}\right)R_G \quad (4\text{-}19)$$

According to Eq.4-18 and Eq.4-19, C_{GSO} and C_{GDO} can be expressed as Eq.4-20 and Eq.4-21.

$$C_{GSO} \approx \frac{-\text{Im}\left[Y_{SG}\right]}{\omega} \quad (4\text{-}20)$$

$$C_{GDO} \approx \frac{-\text{Im}\left[Y_{DG}\right]}{\omega} \quad (4\text{-}21)$$

Substituting Eq.4-18 and Eq.4-19 into Eq.4-17, the C_{GBO} can be derived as Eq.4-22.

$$C_{GBO}+C_{GBE} \approx \frac{\text{Im}\left[Y_{GG}\right]+\text{Im}\left[Y_{SG}\right]+\text{Im}\left[Y_{DG}\right]}{\omega} \quad (4\text{-}22)$$

According to Eq.4-17, the gate resistance R_G can be approximately derived by dividing the real part of Y_{GG} by imaginary part of Y_{GG}.

$$R_G \approx \frac{\text{Re}\left[Y_{GG}\right]}{\text{Im}\left[Y_{GG}\right]} \quad (4\text{-}23)$$

However, the effect of R_S, R_D and R_{GB} are not excluded from the extracted results of R_G. According to Eq.4-14, at low frequency range, the imaginary part of Y_{BD} is approximated to the sum of ωC_{DBO} and ωC_{DBE}. They could not be separated if no further information provided. It's also found that the real part of Y_{BD} is independent of C_{DBE} but only the function of C_{DBO} and R_{DB}. Therefore, the values of C_{DBO} and R_{DB} can be extracted from the real part of Y_{BD} at different frequencies, in theory. The deduction is demonstrated below.

$$\text{Re}\left[Y_{BD}\right]=-\frac{\omega^2 C_{DBO}{}^2 R_{DB}}{1+\omega^2 C_{DBO}{}^2 R_{DB}{}^2}$$

$$\mathrm{Re}\left[Y_{BD}\right]+\mathrm{Re}\left[Y_{BD}\right]\omega^2 {C_{DBO}}^2 {R_{DB}}^2+\omega^2 {C_{DBO}}^2 R_{DB}=0 \tag{4-24}$$

Equation 4-24 corresponds to two different frequencies ω_1 and ω_1 can be expressed as:

$$\mathrm{Re}\left[Y_{BD}(\omega_1)\right]+\mathrm{Re}\left[Y_{BD}(\omega_1)\right]{\omega_1}^2 {C_{DBO}}^2 {R_{DB}}^2+{\omega_1}^2 {C_{DBO}}^2 R_{DB}=0 \tag{4-25}$$

$$\mathrm{Re}\left[Y_{BD}(\omega_2)\right]+\mathrm{Re}\left[Y_{BD}(\omega_2)\right]{\omega_2}^2 {C_{DBO}}^2 {R_{DB}}^2+{\omega_2}^2 {C_{DBO}}^2 R_{DB}=0 \tag{4-26}$$

From Eq.4-25 and Eq.4-26, ${C_{DBO}}^2 {R_{DB}}^2$ and ${C_{DBO}}^2 R_{DB}$ can be solved as:

$${C_{DBO}}^2 {R_{DB}}^2=\frac{\mathrm{Re}\left[Y_{BD}(\omega_2)\right]/{\omega_2}^2-\mathrm{Re}\left[Y_{BD}(\omega_1)\right]/{\omega_1}^2}{\mathrm{Re}\left[Y_{BD}(\omega_1)\right]-\mathrm{Re}\left[Y_{BD}(\omega_2)\right]} \tag{4-27}$$

$${C_{DBO}}^2 R_{DB}=\mathrm{Re}\left[Y_{BD}(\omega_1)\right]\frac{\mathrm{Re}\left[Y_{BD}(\omega_2)\right]/{\omega_2}^2-\mathrm{Re}\left[Y_{BD}(\omega_1)\right]/{\omega_1}^2}{\mathrm{Re}\left[Y_{BD}(\omega_1)\right]-\mathrm{Re}\left[Y_{BD}(\omega_2)\right]}+\frac{\mathrm{Re}\left[Y_{BD}(\omega_1)\right]}{{\omega_1}^2} \tag{4-28}$$

The value of R_{DB} can be obtained by dividing Eq.4-27 to 4-28. Then, substituting RDB to Eq.4-27 or Eq.4-28, the C_{DBO} can also be extracted. Since the sum of C_{DBO} and C_{DBE} is approximately equals to the value of Y_{BD} at low frequencies, the C_{DBE} can also be obtained. Similarly, the C_{SBO}, C_{SBE} and R_{SB} can be extracted by this approach, so do the C_{GBO}, C_{GBE} and R_{GB}.

The expression of R_{DSB} is very complex and difficult to simplify, therefore it cannot be extracted by a compact equation. However, since the value of other components in Fig.4.4 are known, they can be de-embedded out from the measured data and the value of R_{DSB} can be obtained.

According to the data measured from a cold DUT and the simplified equivalent circuit, the method of extracting extrinsic components in Fig.4.4 are deduced. According to some literature [33]-[35], the substrate resistances of a NMOSFET are almost unchanged when negative or low positive gate bias voltage was applied. The C_{GSO} and C_{GDO} are also independent of bias condition. Therefore, they may be used for the small-signal equivalent

circuit of an active NMOSFET. This will be checked later. However, the R_G, C_{DB}, C_{SB}, and C_{GB} will influent by the applied voltage, they must be re-extracted for the case of active DUT.

4.3.2 Extraction of Components in the Equivalent Circuit of MOSFET's in Linear Region

In the cold situation, the source and drain resistance of the DUT are difficult to isolate from the measured data since the impedances of extrinsic capacitors such as C_{GSO}, C_{GDO}, C_{SBO}, and C_{DBO} are much larger than that of source and drain resistances. In this section, another approach of applying DC voltages on the gate while the source, drain, and body are grounded is used. If a DC voltage higher then the threshold voltage of the NMOSFET is applied on the gate with other three terminals DC grounded, the active elements in Fig.4.2 can be replaced with a channel resistance. The small-signal equivalent in Fig.4.2 can be simplified and is shown in Fig.4.5. The real part of Y_{SD} or Y_{DS} can be approximated as:

$$\mathrm{Re}\left[Y_{SD}\right] \approx -\left(R_S + R_D + R_{CH}\right)^{-1} \tag{4-29}$$

In Eq.4-29, the R_S and R_D are almost independent of bias condition but R_{CH} isn't. The channel conductance of the MOSFET only has gate voltage applied will be proportional to the carrier concentration of the inversion layer, which is proportional to the excess gate voltage. The channel resistance can be expressed as a function and will be proportional $\left(V_G - V_{TH}\right)^{-1}$. As the gate excess voltage approaches to infinity, or say $\left(V_G - V_{TH}\right)^{-1}$ approach to zero, the R_{CH} will approach to zero in theory. Then the Eq.4-29 will become $\left(-\mathrm{Re}\left[Y_{SD}\right]\right)^{-1} \approx R_S + R_D$. This can be done by plotting $\left(-\mathrm{Re}\left[Y_{SD}\right]\right)^{-1}$ versus $\left(V_G - V_{TH}\right)^{-1}$ in a rectangular plot. The intersectional point of $\left(-\mathrm{Re}\left[Y_{SD}\right]\right)^{-1}$ line and y-axis will indicate the value of $R_S + R_D$. Once the sum of source and drain resistances is obtained, the source and drain resistance be extracted since they are approximately equal.

The gate resistance can also be extracted from the device with only gate voltage applied.

While the channel of the device is induced, the C_{GBO} will be depressed to almost zero since the substrate charges is shielded by the carriers in channel. This will reduce the effect of C_{GB} and R_{GB}, which will influence the extraction of R_G. Moreover, the total gate capacitance will also increase due to the induced carriers in the channel, which will increase the amplitude of the imaginary and real part of Y_{GG} and improve the signal to noise ratio to obtain a better extracted result.

4.3.3 Extraction of intrinsic components in saturation region

MOSFET's operated in saturation region have three major current sources I_m, I_{ms}, and I_{md}, which are shown in Fig.4.2 and will contribute to the output small-signal current at drain terminal. The I_m represents the drain current caused by the voltage drop between gate and source, v_{gsi}, and was shown in Eq.4-3. The R_S is a very low-value resistance that it can be neglected at most situations except when dealing with the intrinsic transconductance g_m and intrinsic bulk transconductance g_{mb}. R_S locates at the path of source current; the voltage drop results from source current on this resistance will affect the v_{gsi} and v_{bsi}. This produces a negative feedback mechanism on the drain current and effectively reduces the extrinsic transconductace. The relation of the extrinsic and intrinsic transconductance can be approximated as:

$$g_m' \approx \frac{g_m}{1+g_m R_s} \tag{4-31}$$

Similarly, The relation of the extrinsic and intrinsic transconductance can be approximated as:

$$g_{mb}' \approx \frac{g_{mb}}{1+g_{mb} R_s} \tag{4-32}$$

In Eq.4-31 and Eq.4-32, the g_m' and g_{mb}' represent the extrinsic transconductance and extrinsic bulk conductance correspond to the transconductance includes the effect of R_S. The R_D has minor effect on the active MOSFET since its value is much lower than channel resistance $1/g_{DS}$ and the impedances of C_{GD} and C_{DB} and can be neglected to simplify the

extraction of other components. Therefore, the small-signal equivalent circuit with the extrinsic transconductances gm' and gmb', where the R_D is also neglected is shown in Fig.4.6. According to Fig.4.6, the I_m equals to $Y_{DG} \times v_{GS}$, so the I_m can be expressed as:

$$
\begin{aligned}
I_m &= Y_{DG} \times v_{GS} + j\omega C_{GD} v_{GDi} \\
&= Y_{DG} \times v_{GSi} \times \left(1 + j\omega\left(C_{GS} + C_{GD} + C_{GBE}\right) R_G\right) + j\omega C_{GD} v_{GDi} \\
&= \left(g_m' - j\omega C_m\right) v_{GSi}
\end{aligned}
$$

Therefore,

$$
g_m' - j\omega C_m = Y_{DG} \times \left(1 + j\omega\left(C_{GS} + C_{GD} + C_{GBE}\right) R_G\right) + j\omega C_{GD} \qquad (4\text{-}33)
$$

Therefore, the g_m', can be extracted from the real part of Eq.4-33, which is nearly the real part of Y_{GD}. According to the imaginary part of Eq.4-33, transcapacitance C_m can also be extracted.

The I_{ms} shown in Fig.4.6 indicates the small-signal drain current induced body potential fluctuation, which equals to $Y_{DB} \times v_{BS}$. So, I_{ms} can be written as:

$$
\begin{aligned}
I_{ms} &= Y_{DB} \times v_{BS} + j\omega C_{DB} \times v_{BSi} \\
&= Y_{DB} \times v_{BSi} \times \left(1 + j\omega C_{SB} R_{SB}\right) + j\omega C_{DB} \times v_{BSi} \\
&= \left(g_{mb}' - j\omega C_{mb}\right) v_{BSi}
\end{aligned}
$$

Therefore,

$$
g_{mb}' - j\omega C_{mb} = Y_{DB} \times v_{GSi} \times \left(1 + j\omega C_{SB} R_{SB}\right) + j\omega C_{DB} \qquad (4\text{-}34)
$$

The extrinsic bulk transconductance, g_{mb}', and the transcapacitance C_{ms} can be obtained from the real part and imaginary part of Eq.4-34, respectively.

Equation 4-5 represents the small-signal drain current results from voltage fluctuation at drain terminal, which can be approximated to $Y_{SD} \times v_{DS}$. Therefore, the Y_{SD} can expressed as:

$$
Y_{SD} = g_{DS} + j\omega C_{SD} \qquad (4\text{-}35)
$$

The output conductance g_{ds} saw at drain is simply the real part of Y_{SD}.

The I_{mx} is a substrate current induced from $C_{mgb}v_{GBi}$, it can be approximated to $C_{mgb}v_{GB}$ at moderate low frequencies by assuming that the substrate resistances is much lower than the impedances of C_{GB}, C_{SB} and C_{DB}. Then, the I_{mx} will approximately equal to the imaginary part of Y_{BG} and can expressed as:

$$\mathrm{Im}\left[Y_{GB}\right] = j\omega C_{mgb} \tag{4-36}$$

Therefore, C_{mgb} can be extracted from imaginary part of Y_{GB} at lower frequencies.

According to Fig.4.6, the Y_{GS} and Y_{GD} are expressed as Eq.4-37 and Eq.4-38.

$$Y_{GS} = -\frac{j\omega C_{GS} + \omega^2 C_{GS}(C_{GD} + C_{GS})R_G}{1 + \omega^2 (C_{GD} + C_{GS})^2 R_G} \tag{4-37}$$

$$Y_{GD} = -\left(\left(R_G^{-1} + j\omega C_{GS}^{-1}\right)^{-1} + j\omega C_{GD}^{-1}\right)^{-1} \tag{4-38}$$

By neglecting the high-order term of $\omega C_X R_X$, these two equations can be simplified to Eq.4-39 and Eq.4-40.

$$Y_{GS} \approx -j\omega C_{GS} - \omega^2 C_{GS}(C_{GD} + C_{GS})R_G \tag{4-39}$$

$$Y_{GD} \approx -j\omega C_{GD} - \omega^2 C_{GD}{}^2 R_G \tag{4-40}$$

The C_{gs} and C_{gd} of an active MOSFET can be extracted from the imaginary part of Y_{GS} and Y_{GD}.

Refering to Fig.4-6, Y_{SG} can be derived and simplified as Eq.4-41.

$$Y_{SG} \approx -\frac{g_m + j\omega C_{GS} - j\omega\left(C_{GS} + C_{GD}\right) g_m R_G}{1 + g_m R_S} \tag{4-41}$$

According to the imaginary part of Y_{SG}, R_G can also be extracted while the device is active. According to Eq.4-41, it is observed that R_G is amplified and contributes an inductive impedance value to the imaginary part of Y_{SG}. This inductive value determined by $j\omega\left(C_{GS} + C_{GD}\right) g_m R_G$ is a first-order term of $\omega C_X R_X$, which will make the extraction of R_G easier than the conventional

$\omega^2(C_{GSO}+C_{GDO}+C_{GBO})^2 R_G / \omega(C_{GSO}+C_{GDO}+C_{GBO})$ at lower frequencies since the value of $\omega^2(C_{GSO}+C_{GDO}+C_{GBO})^2 R_G$ is very low.

C_{SB} and C_{DB} of saturated MOSFET must be extracted from Y_{BS} and Y_{BD}. However, according to Fig.4-6, it is a difficult mission since the substrate R-C network is not only complex but also involved a current source I_{ms}. To simplify the work, anther approach to solve this problem is adapted. For moderate low frequencies, it can be assumed that the impedances of C_{SB} and C_{DB} are large enough that few signal are coupled to the substrate. So no current signal flow through the entire substrate and it can be treated like the intrinsic bulk terminal was grounded. Therefore, the imaginary part of Y_{BS} and Y_{BD} will almost be composed by $j\omega(C_{SB}+C_{SBE})$ and $j\omega(C_{DB}+C_{DBE})$, respectively. The C_{SBE} and C_{DBE} are almost independent of bias condition, the same values extracted from cold measurement can be used. The C_{SB} and C_{DB} be can be approximated respectively as Eq.4-42 and 4-43 at low frequencies.

$$C_{SB} \approx \frac{\mathrm{Im}[Y_{BS}]}{\omega} - C_{SBE} \tag{4-42}$$

$$C_{DB} \approx \frac{\mathrm{Im}[Y_{BD}]}{\omega} - C_{DBE} \tag{4-43}$$

4.4 Results and Discussions

The extraction methodology discussed in previous sections is based on y-parameters of the small-signal equivalent circuit of a MOSFET. Therefore, the measured four-port scattering parameters of the DUT's are transferred to y-parameters to complete the extraction. NMOSFET's of three different dimensions were measured. The gate finger lengths of these devices are 3.6, 7.2, and 12μm with finger number of four, and are marked by M1, M2, and

M3, respectively.

4.4.1 Extracted Results of Cold Devices

Figure 4.7 shows the real and imaginary part of Y_{GG} of the three cold devices. It can be seen that the three imaginary part of Y_{GG} are almost proportional to the measurement frequency as high as 20GHz, and the amplitudes of the real parts are much lower than that of imaginary parts. It indicates the impedance of $C_{GS}+C_{GD}+C_{GBE}$ is much larger than the value of R_G. Figure 4.8 also shows the same phenomena of the linear relations of C_{GSO}, C_{GDO} with frequency. Therefore, the capacitances CGSO and CGDO can be directly extracted from the imaginary part of Y_{DG} and Y_{SG}. Well extraction results was obtained and shown in Fig.4.11, the extracted capacitance values are proportional to the total gate widths of the devices and are almost independent of frequency. It's also observed that the values of C_{GSO} are slightly larger than that of C_{GDO}, this is mainly due to the different metal connection for source and drain.

Figure 4.9a and 4.9b illustrate the imaginary and real parts of Y_{BS} and Y_{BD}. Contrary to the Y_{GS} and Y_{GD}, for Y_{BS} and Y_{BD}, the amplitudes of the real parts are comparable to the imaginary part. The amplitude of imaginary part climbs slowly at higher frequency and are not linear with the frequency. Figure 4.12 shows the results, which extracts the capacitance values by just dividing the Y_{BS} and Y_{BD} by ω. Only the total capacitance can extracted at lower frequency range since the impedance of the capacitance are much larger than the series resistance at lower frequency. In the case of Y_{GB}, there exist the same phenomena and are shown in Fig. 4.10a and 4.10b. According to the extracting method discussed previous, the extracted value of C_{SBO}, C_{SBE}, C_{DBO}, C_{DBE}, C_{GBO}, and C_{GBE} are shown in Fig.4-13, Fig 4-14, and Fig. 4-15, respectively. It can be calculated that, for example, the sum of C_{SBO} and C_{SBE} in Fig.4-13 will approximate to the value of $-Y_{SB}/\omega$ at very low frequency range shown in Fig.4-12.The extracted results also show that the values of C_{SBO} are larger than that of C_{DBO} due to there is one more source junction than the drain. The extracted R_{SB}, R_{DB}, and R_{GB} are

also shown in Fig.4.16 and Fig. 4.17. It's observed that the values of R_{DB} are larger that that of R_{SB}. The extracted results of R_{DSB} are shown in Fig.4.18. It's found that the extracted results show some fluctuation with frequency. It's mainly due to that they are extracted from the real part of the corresponding y-parameters (Eq.4-24 to Eq.4-28). The signal to noise ratio of the real part seems poorer than the imaginary part. Moreover, the frequency step used for extraction will also influence the fluctuation. However, the simulation results using the different parameter values within the range of fluctuation are almost invariant.

4.4.2 Extracted Results of Devices Linear Region

While device with only V_G applied, a layer of conduction carrier is induced beneath the gate oxide. The C_{GS} and C_{GD} will increase due to the induced carries in the channel. Figure 4.19a, 4.19b, and 4.19c show the extracted C_{GS} values of M1, M2, and M3 with different V_G applied. The corresponding C_{GD} values are shown in Fig.4.20a, 4.20b, and 4.20c. It can be observed that the C_{GS} and C_{GD} increase rapidly as V_G increases to 0.6V, but will stop at certain values while the gate voltage exceeds threshold voltage (0.45V). This is due to that while V_G exceeds V_{TH} to form a strong inversion layer, the effective area of C_{GS} and C_{GD} will extend to the entire area beneath the gate, lager V_G will induce more charges, however, will not increase the C_{GS} or C_{GD} further.

Figure 4.21a, 4.21b, and 4.21c show the values of $-Y_{GB}/\omega$ for different devices under different V_G bias conditions. A phenomenon is observed that the extracted value will less dependent to frequency as V_G increases. Once the V_G exceeds V_{TH}, the extracted values are almost independent of frequency and bias independent. Since the strong inversion is formed, the effect of C_{GB} and R_{GB} will be shielded and only the values of bias independent C_{GBE} remain.

The extracted values of R_G correspond to different dimensions and gate bias voltages are shown in Fig.4.22a, 4.22b, and 4.22c. The extracted results show that R_G is almost independent of V_G and V_D while the device is in active region. The extracted values of

V_G=0.4 are slightly different from R_G of other gate voltages since the 0.4V isn't large enough to form a strong inversion layer and the substrate loss will influence the extracted result. It's also observed that the gate resistance will not scale with the device dimension. Other researches [36]-[37] had revealed that the gate resistance of a MOSFET is determined by two major factors. First one is the resistance of the poly gate and which will scale with the gate finger length and number of the device. The other factor is the coupling effect of channel resistance via the gate capacitance, which will relate to the transconductance g_m. In the device of longer gate finger length, the poly resistance will larger than a device with shorter finger length, however, the gm of the longer gate finger is larger. This makes the RG doesn't simply scale with the device dimension.

Figure 4.23a, 4.23b, and 4.23c shows the extracted values for $R_S + R_D + R_{CH}$ correspond to different device dimensions and gate bias conditions. Figure 4.23d shows the sum of these three resistances versus the inverse of effective gate drive $(V_{GS} - V_{TH})^{-1}$. It's obviously the sum or says the R_{CH} are linearly dependent on $(V_{GS} - V_{TH})^{-1}$. Therefore the intersectional point of the resistance axis and the regression lines represents the sum of R_S and R_D. The values of each intersectional point are also shown in the figure.

Figure 4.24a, 4.24b, and 4.24c show the extracted results of C_{SB} for different gate bias conditions and device dimensions. It shows the C_{SB} will slightly increase as the gate bias increase since the source/substrate junction is extended into the induced channel and the effective area of the source/substrate junction increases. However, in Fig. 4.26a, 4.26b, and 4.26c, the extracted results of C_{DB} for different device sizes and gate voltages show that the C_{DB} are less dependent than C_{SB} on the gate voltage. The actual mechanism cause this phenomenon is not clear for present. The only suspect is that during fabrication of the device, some impurities were implanted beneath the drain region to tune the threshold voltage of the device.

Figure 4.25a, 4.25b, and 4.25c show the results of C_{SBE}, it's obvious the C_{SBE} almost invariant with gate bias changed. The same trend for C_{DBE} and C_{GBE} are also shown in Fig.4.27 and Fig4.29 that they are almost independent on gate bias. The dependence of C_{GB} on V_G are shown in Fig.4.28a, 4.28b, and 4.28c. The value of C_{GB} will depressed to almost zero by the gate voltage. It concludes the similar results, which has been shown in Fig.4.21.

The extracted results of R_{SB} and R_{DB} are shown respectively in Fig.4.30 and 4.31. It shows they are almost not changed as V_G increases.

4.4.3 Extracted Results of Saturation Devices

In addition to cold device and linear operation conditions, the three devices are also biased in saturation mode to extract the modeling parameters. Three biased conditions were selected as VG=VD=0.8V, VG=VD=1V, and VG=VD=1.2V.

Figure 4.32a, 4.32b, 4.32c show the extracted C_{GS} and C_{GD} of the saturation devices. It shows the C_{GS} increases slightly as V_G and V_D increase from 0.8V to 1V, but will not increase anymore as V_G and V_D increase from 1V to 1.2V. The C_{GD} is almost independent of bias condition when device is in saturation region, and is approximately the value of C_{GDO}. It's due to that there exists a pinch-off region near the drain end of the channel, in which carriers are expelled out and hence the C_{GDi} is vanished.

Figure 4.33a, 4.33b, and 4.33c are the extracted results of g_m and g_{mb} corresponds to different bias voltages and device dimensions. They are dependent on device dimensions as expect. The extracted g_m increases as V_G increases from 0.8V to 1V, however, decreases slightly as V_G increases to 1.2V. This is due to that as V_G increases to a certain value, the resulted vertical electrical field will reduce the mobility of the carrier and hence g_m. Figure 4.34a, 4.34b, and 4.34c demonstrate the extracted results of transcapacitnce C_m and C_{ms}. It shows dependence on frequencies, but probably due to the extraction method. However, the trends can still observed, that the transcapacitances have slightly dependence on bias conditions, and strong dependence on device dimensions. The R_G of saturation devices are extracted and

shown in Fig.4.35a, 4.35b, and 4.35c. It shows that the R_G are almost invariant as the bias voltage changes from 0.8V to 1.2V. The R_G of devices with different dimensions are obviously different, the trend were discussed in previous section.

Figure 4.36a, 4.36b, and 4.36c show the extracted values of C_{SB} and C_{DB} for the three devices in different bias conditions. It can be seen that the C_{SB} is almost unchanged as V_G and V_D change. However, the values C_{DB} are decreased as V_D increased due to that the large V_D will widen the deletion region width of the reversed drain/bulk junction. Comparing the extracted values of C_{DB} with that of C_{DBO} show in Fig. 4.14, it can be found that the C_{DB} of reversed-biased drain/substrate junction are smaller than that of a cold device.

The R_{SB} and R_{DB} for the three saturation devices are shown in Fig.4.37a, 4.37b, and 4.37c. No sign of R_{SB} changes with bias voltage is observed since source and substrate are grounded. However, it shows the R_{DB} will increase slightly as the V_D increases, it seems the widen depletion region of the reversed-biased drain/substrate junction will increase the R_{DB}.

4.5 Summary

In this chapter, the small-signal equivalent circuits for three modes of device bias condition are introduced. The extraction methods for components correspond to each equivalent circuit were deduced in detail. And the extraction results were also shown. In the case of cold devices, C_{GSO}, C_{GDO}, C_{SBO}, C_{SBE}, C_{DBO}, C_{DBE}, C_{GBO}, C_{GBE}, R_{SB}, R_{DB}, and R_{DSB} were extracted. All of them are scaled with device dimensions. In the situation of linear operation mode, the R_S, R_D and R_G not dealt with in the cold device were extracted. The dependence of the components in the equivalent circuits on the applied gate voltage was also discussed. In the case of saturation device, in addition to the components have been discussed in linear operation mode, g_m, g_{mb}, C_m, and C_{mb} were also extracted.

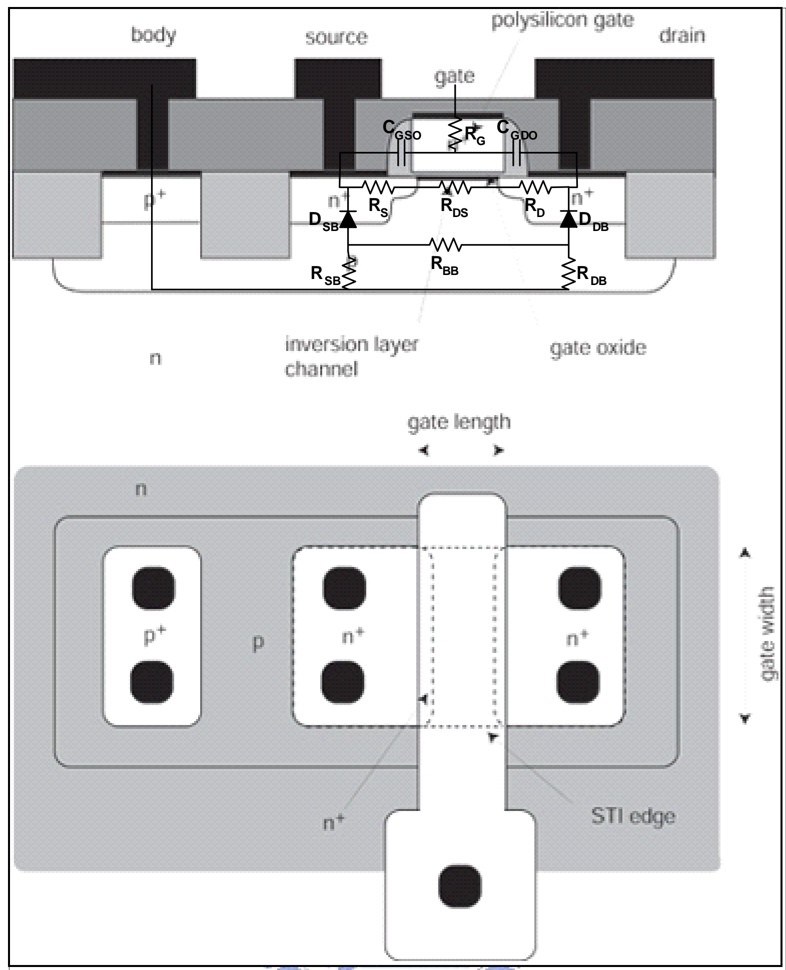


Fig.4.1 The cross-sectional structure and top view of a four-terminal MOSFET.

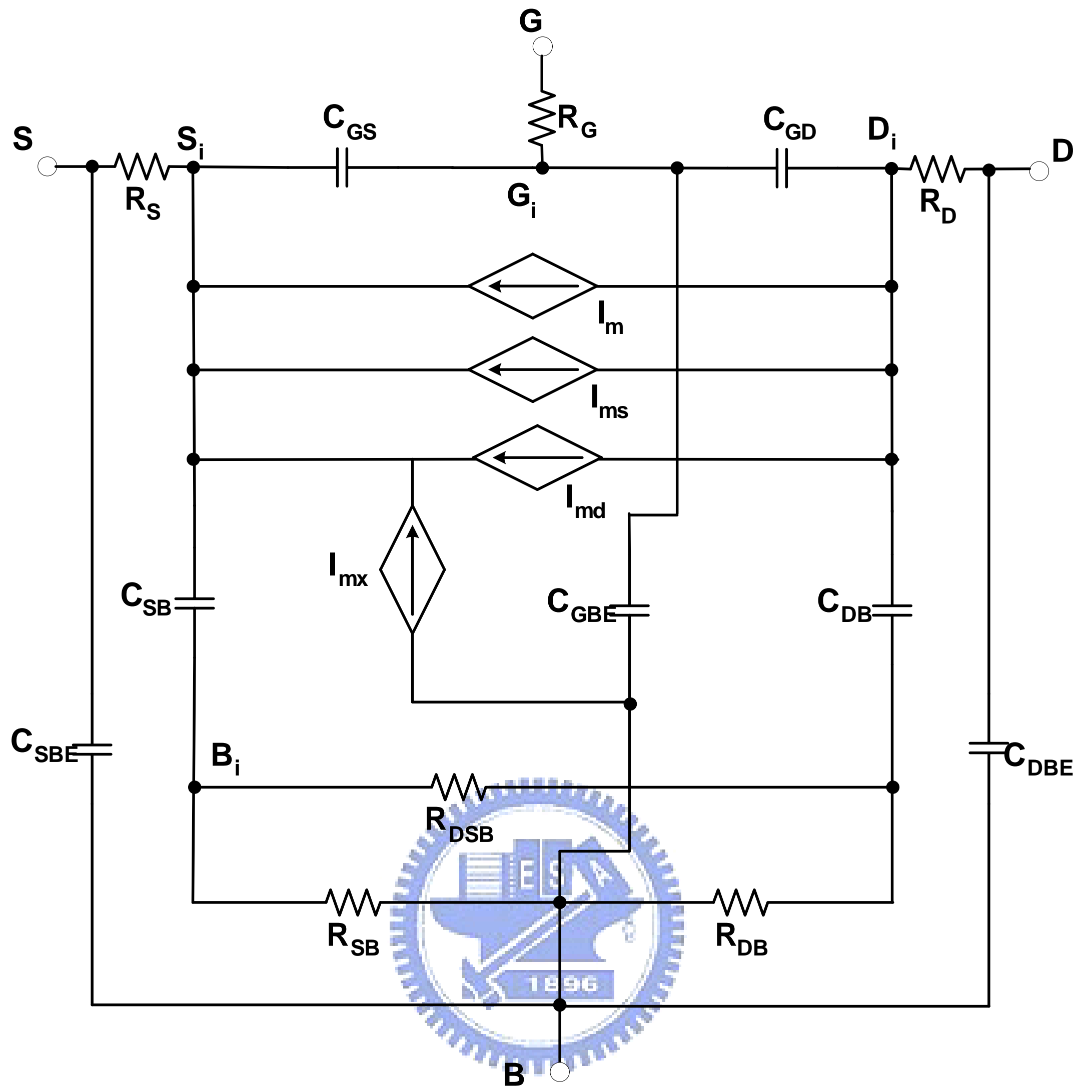


Fig.4.2 The small signal equivalent circuit of a four-terminal RF MOSFET including the intrinsic and extrinsic parts.

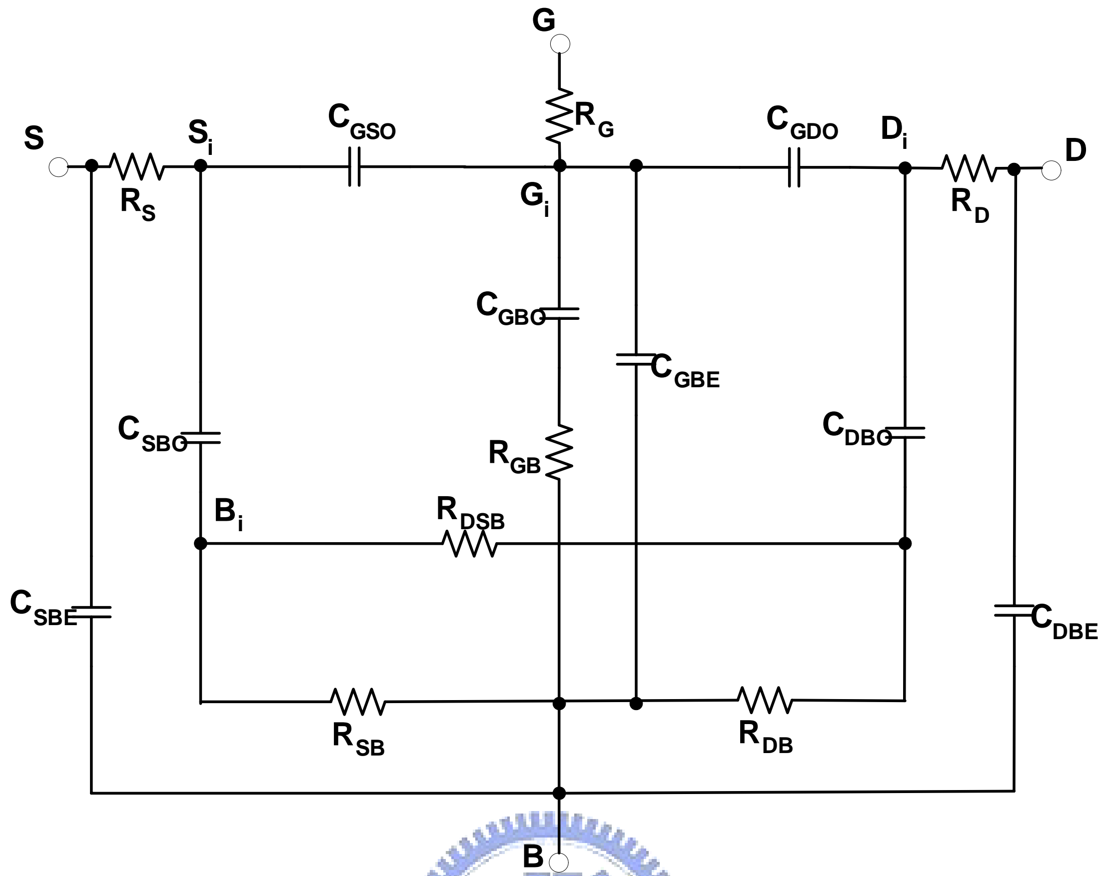


Fig.4.3 The small signal equivalent circuit of a cold MOSFET, in which the intrinsic part of the MOSFET is neglected.

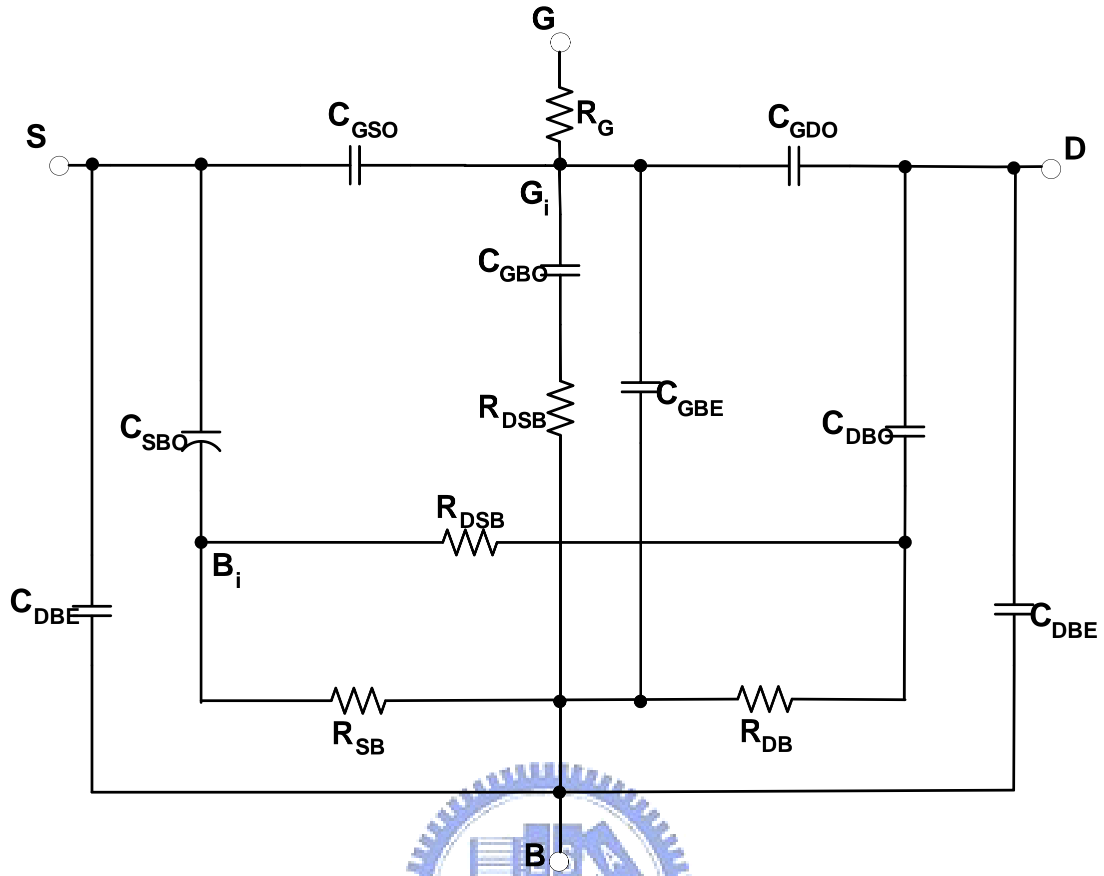


Fig.4.4 The small signal equivalent circuit of a cold MOSFET with RS and RD neglected.

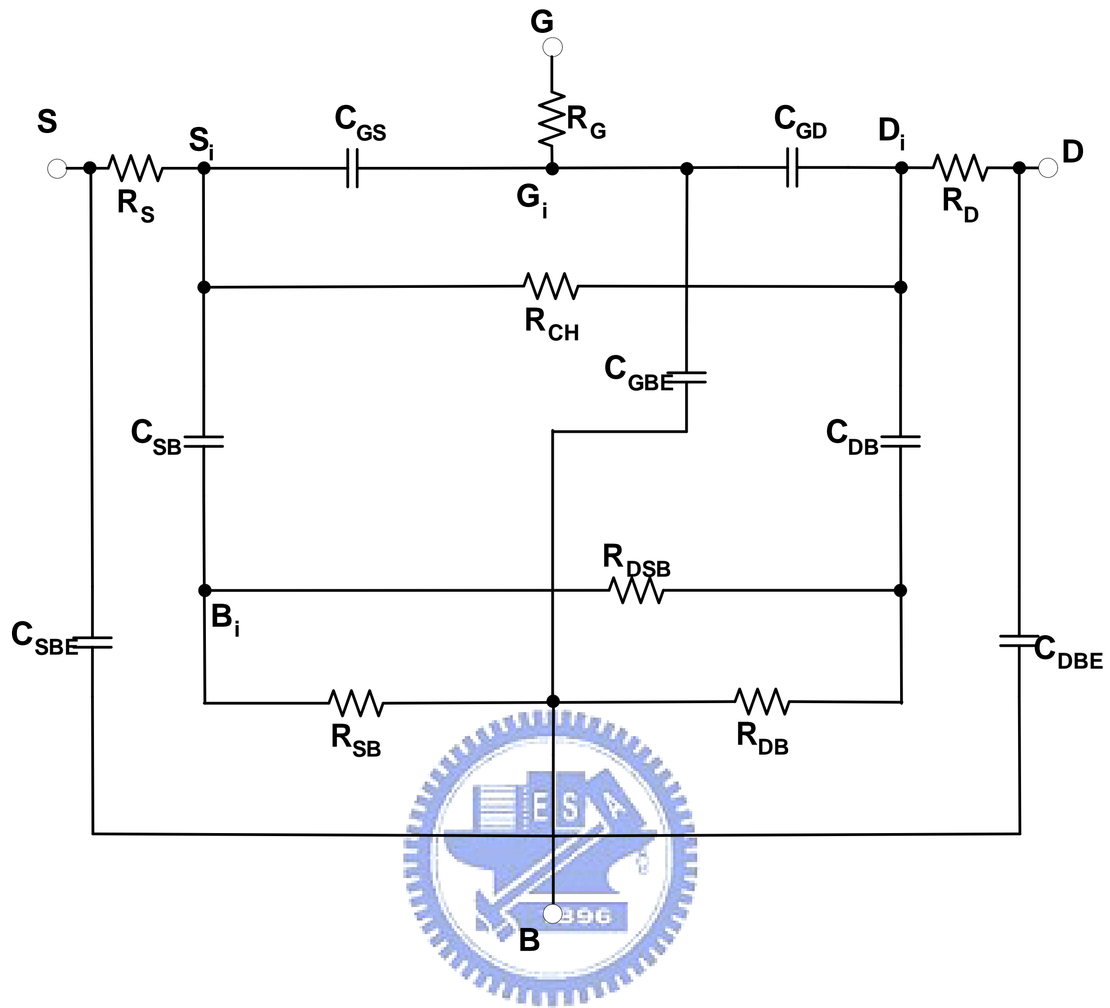


Fig.4.5 The small signal equivalent circuit of a MOSFET biased in linear region.

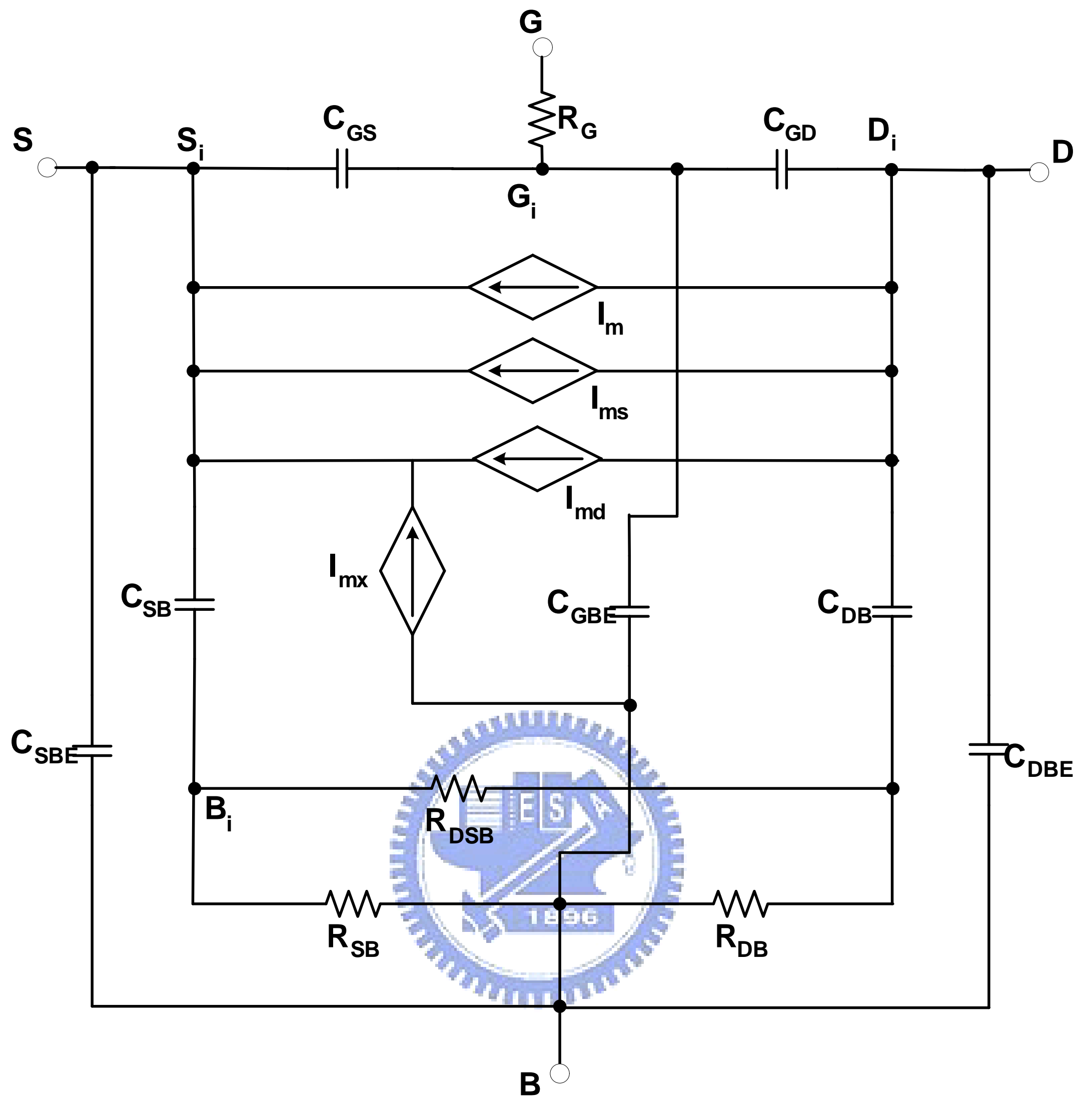
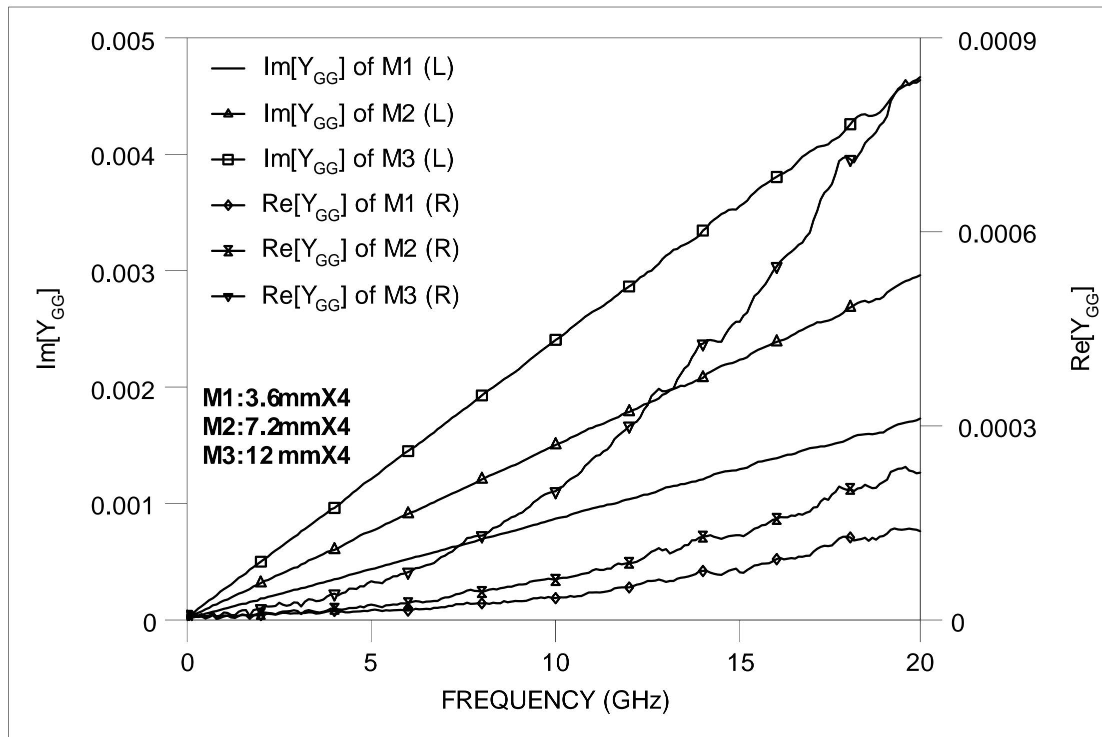


Fig.4.6 The small signal equivalent circuit of a saturated MOSFET with the R_S and R_D neglected.



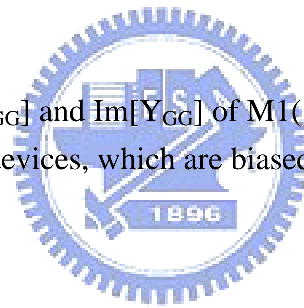
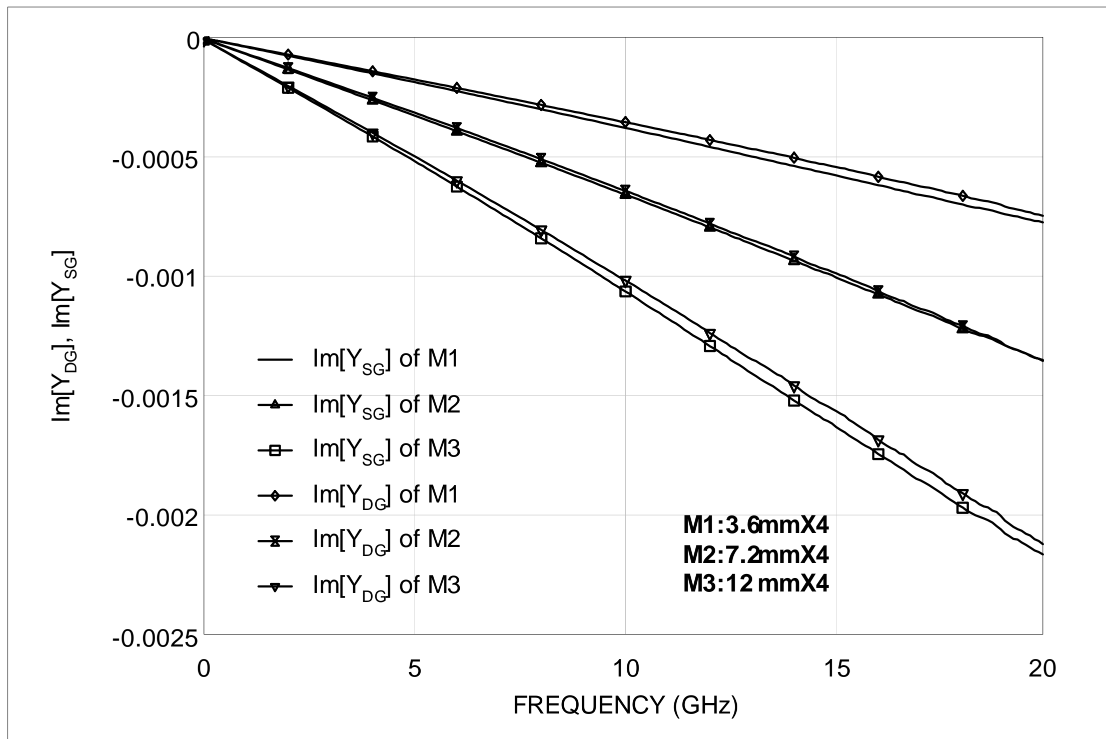


Fig.4.7 The measured Re[Y_{GG}] and Im[Y_{GG}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.



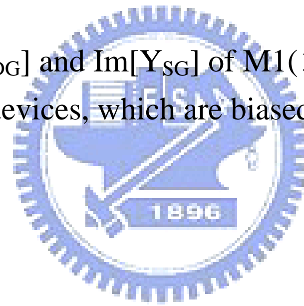
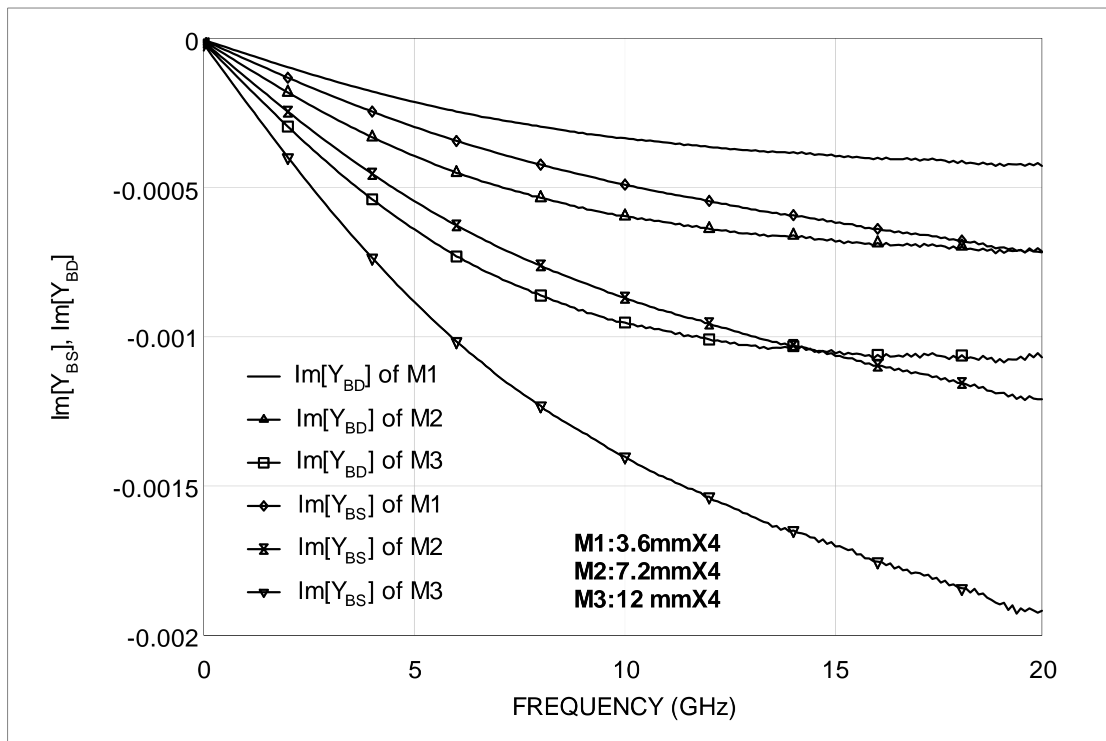
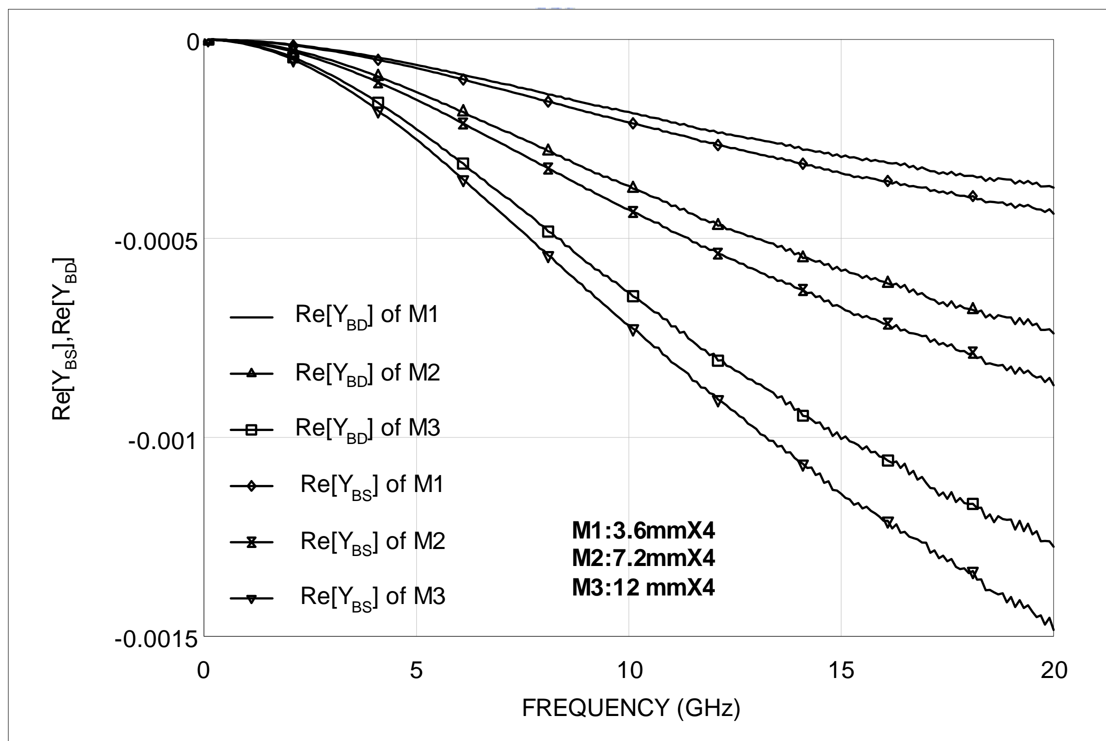


Fig.4.8 The measured Im[Y_{DG}] and Im[Y_{SG}] of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=VS=VB=0.

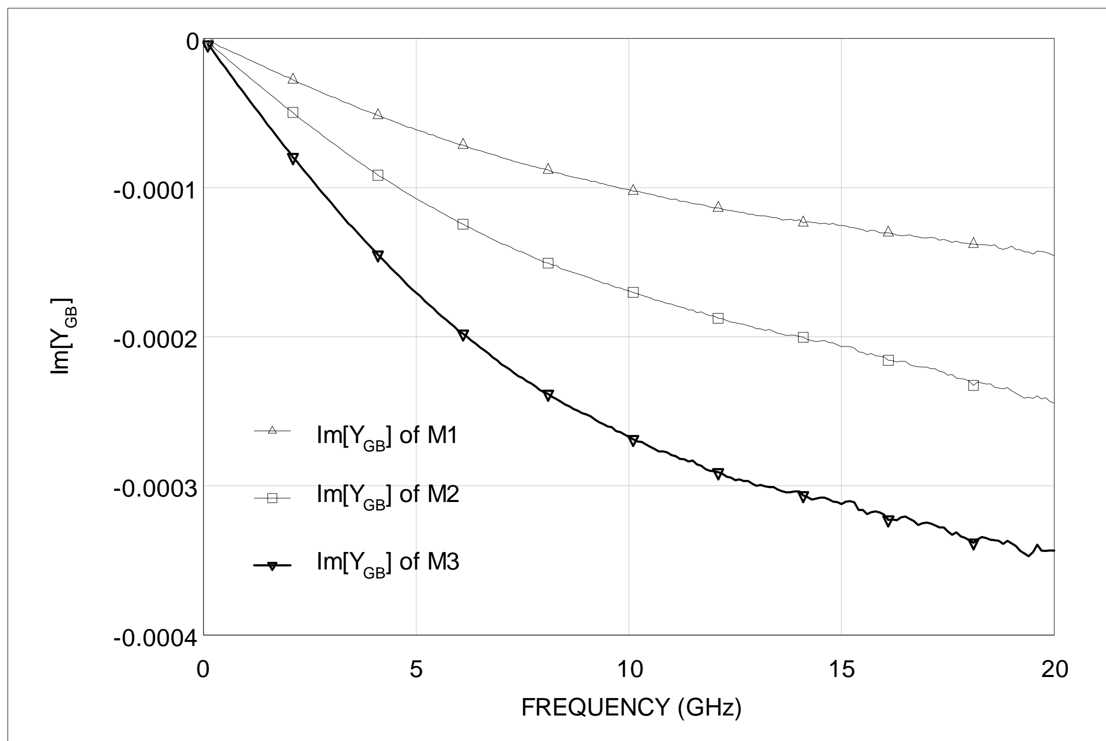


(a)

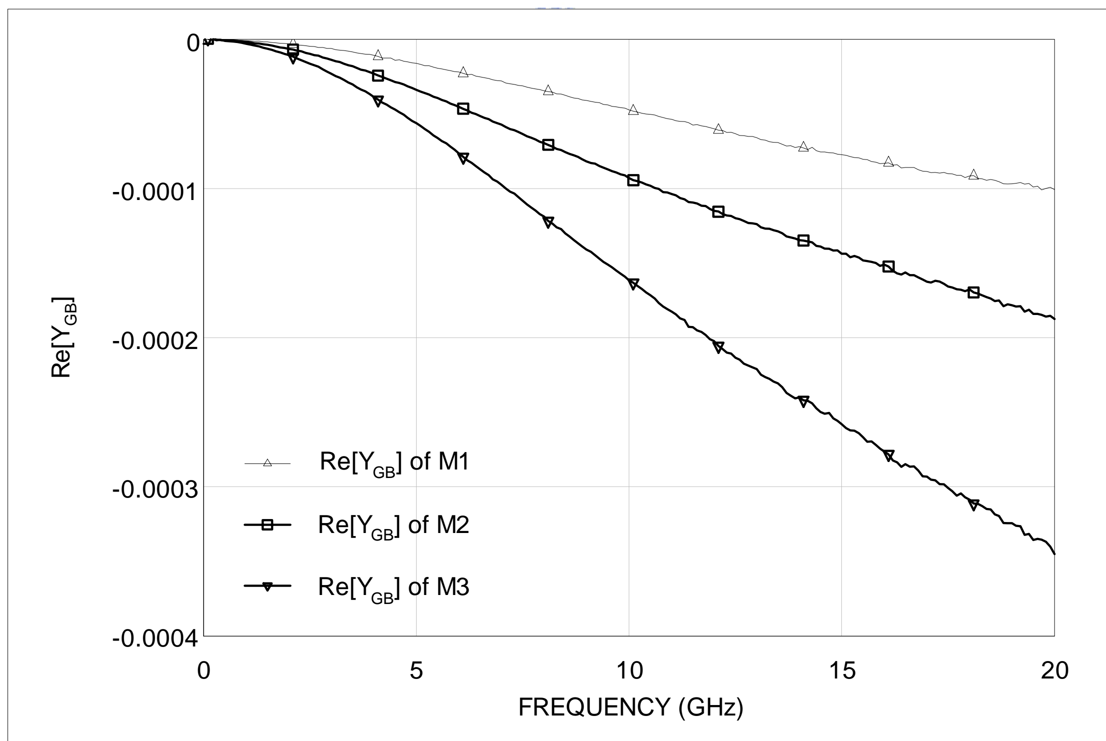


(b)

Fig.4.9 (a) The measured Im[Y_{BD}] and Im[Y_{BS}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.
(b) The measured Re[Y_{BD}] and Re[Y_{BS}] of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.



(a)



(b)

Fig.4.10 (a) The measured Im[Y_{GB}] of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=VS=VB=0.
(b) The measured Re[Y_{GB}] of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=VS=VB=0.

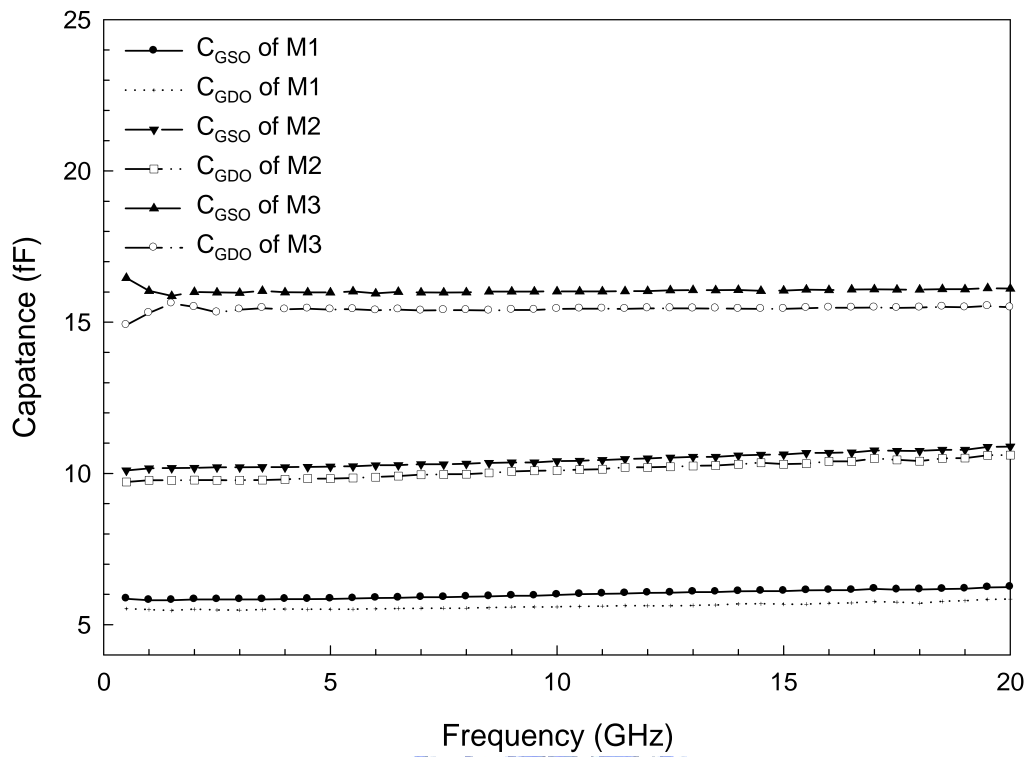


Fig.4.11 The extracted C_{GSO} and C_{GDO} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=VS=VB=0.

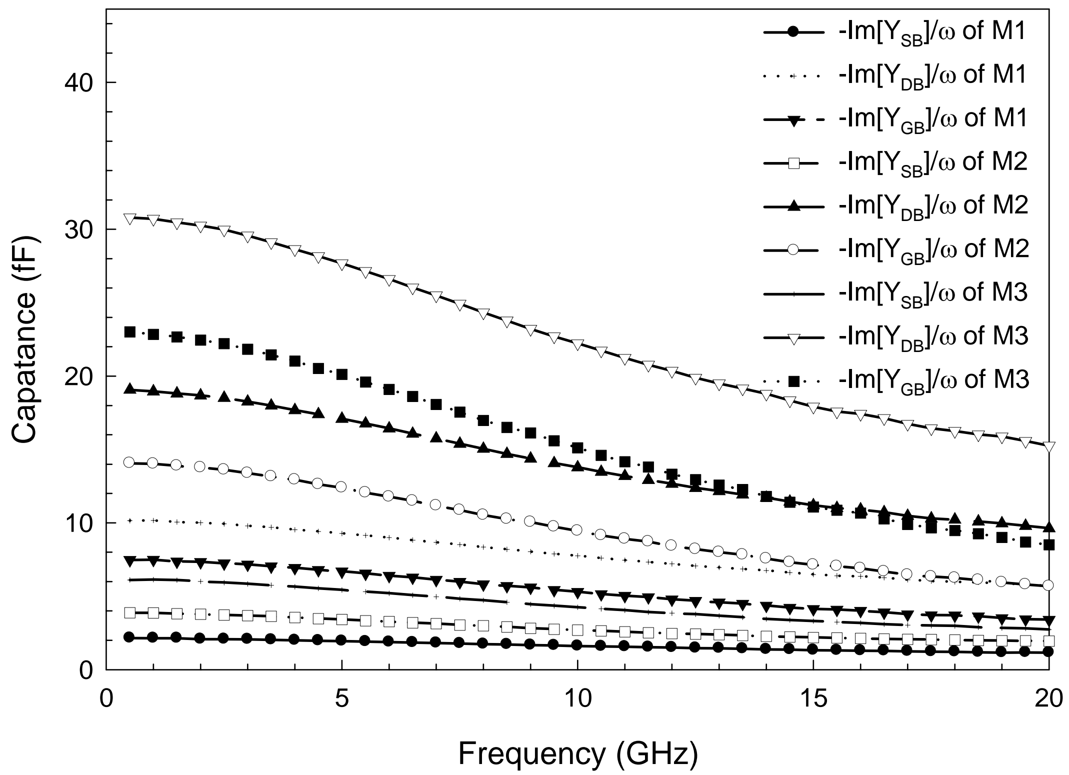


Fig.4.12 -Im[Y_{SB}]/ω of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

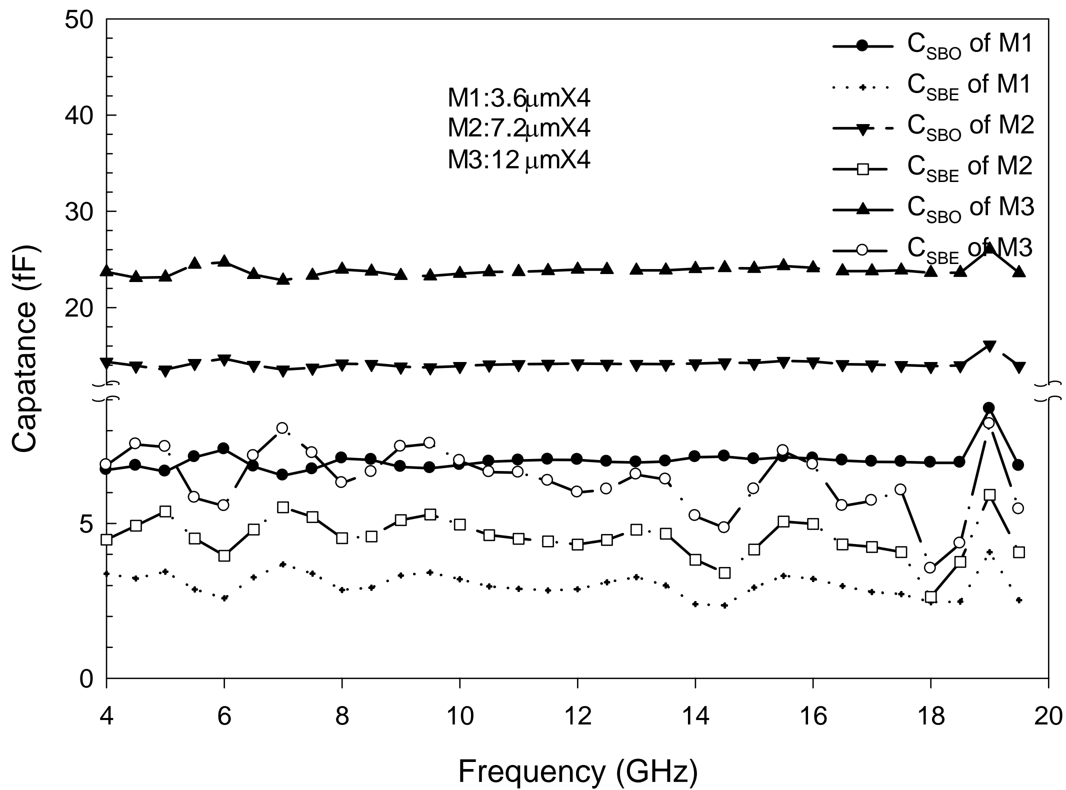


Fig.4.13 The extracted C_{SBO} and C_{SBE} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

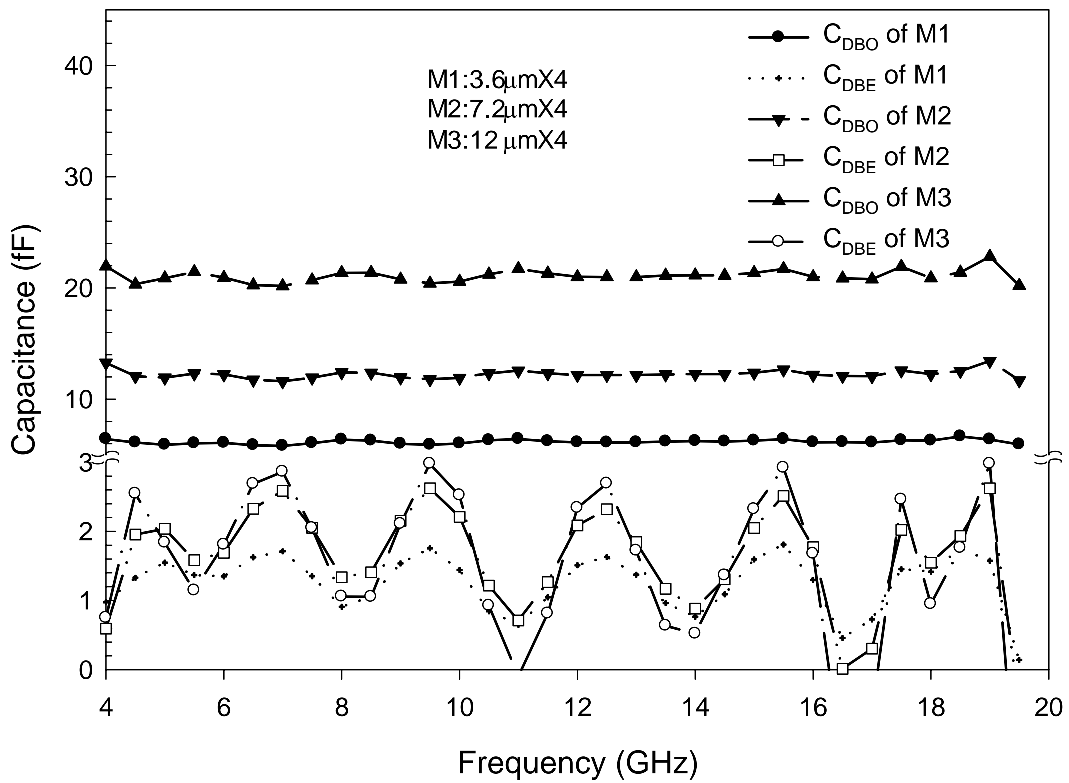


Fig.4.14 The extracted C_{DBO} and C_{DBE} of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$) devices, which are biased at VG=VD=VS=VB=0.

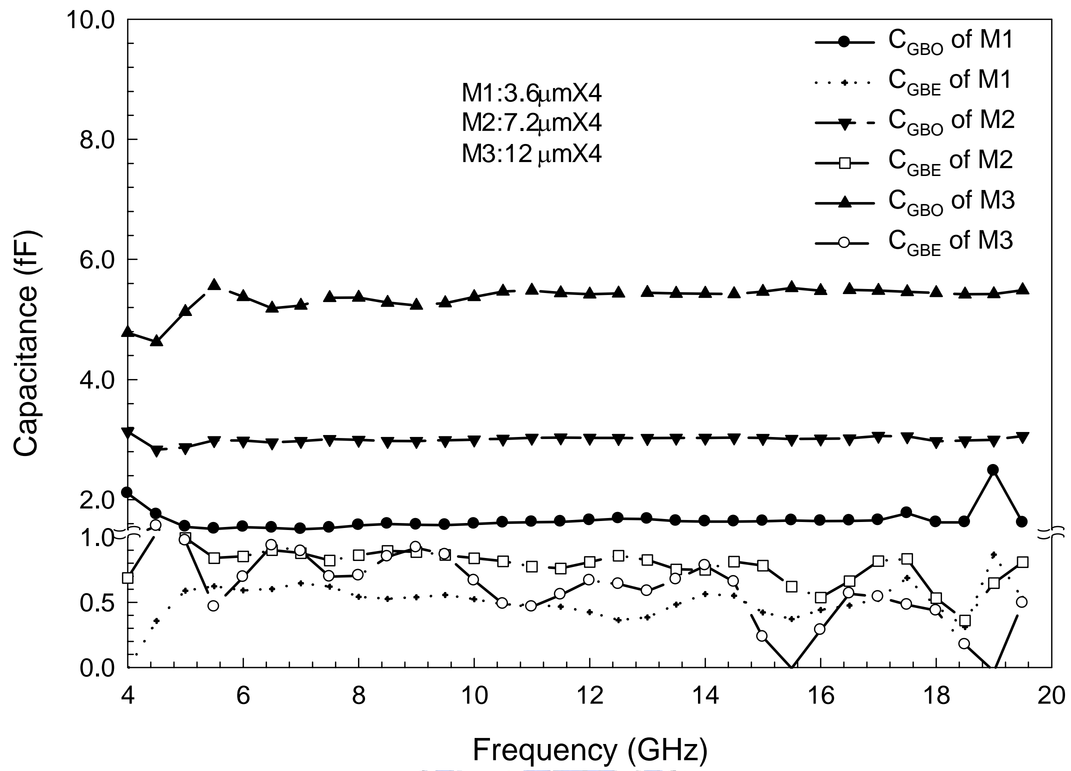


Fig.4.15 The extracted C_{GBO} and C_{GBE} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=VS=VB=0.

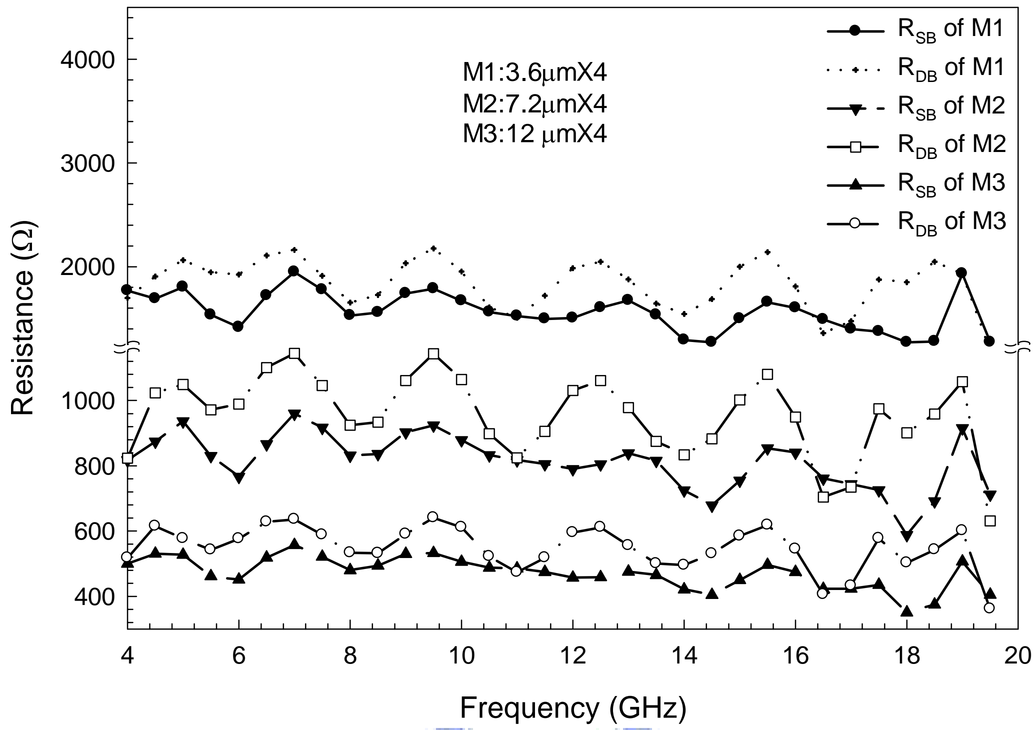


Fig.4.16 The extracted R_{SB} and R_{DB} of M1($3.6\mu m\times4$), M2($7.2\mu m\times4$), and M3($12\mu m\times4$) devices, which are biased at VG=VD=VS=VB=0.

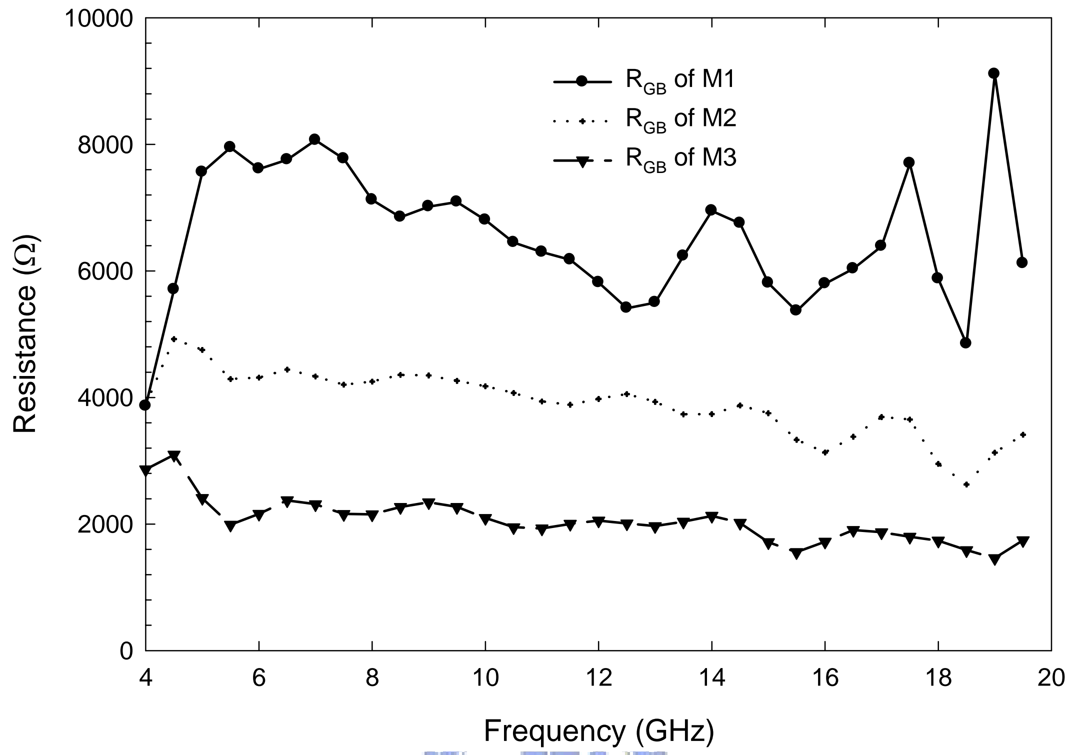


Fig.4.17 The extracted R_{GB} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=VS=VB=0.

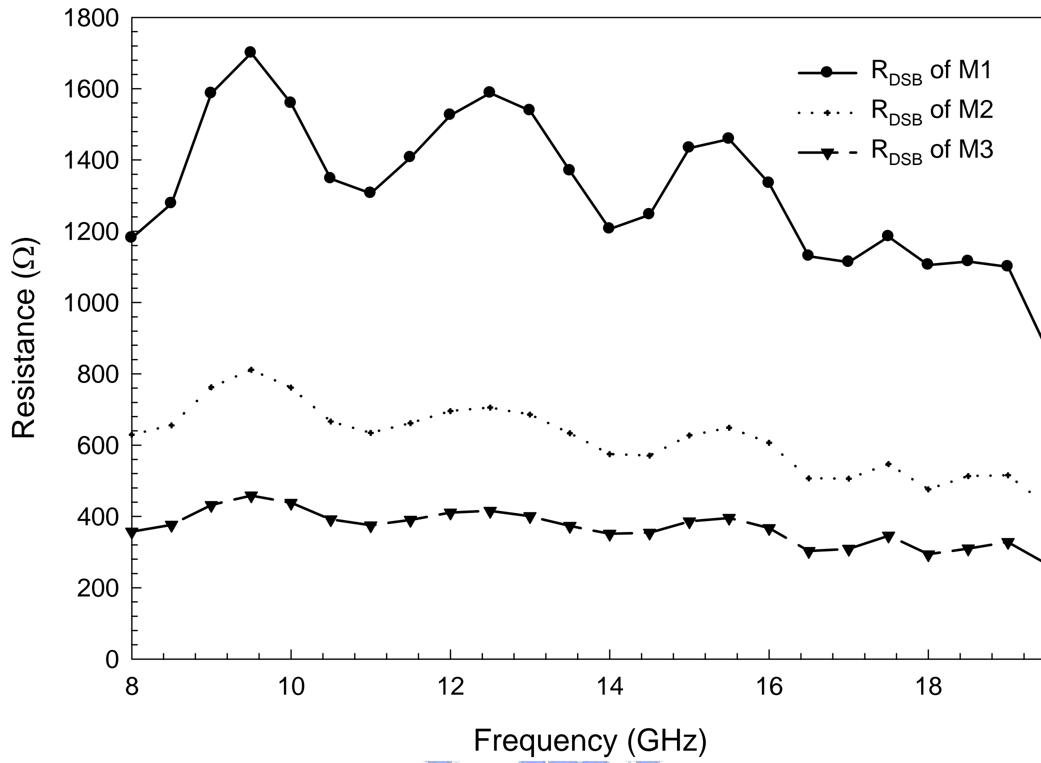
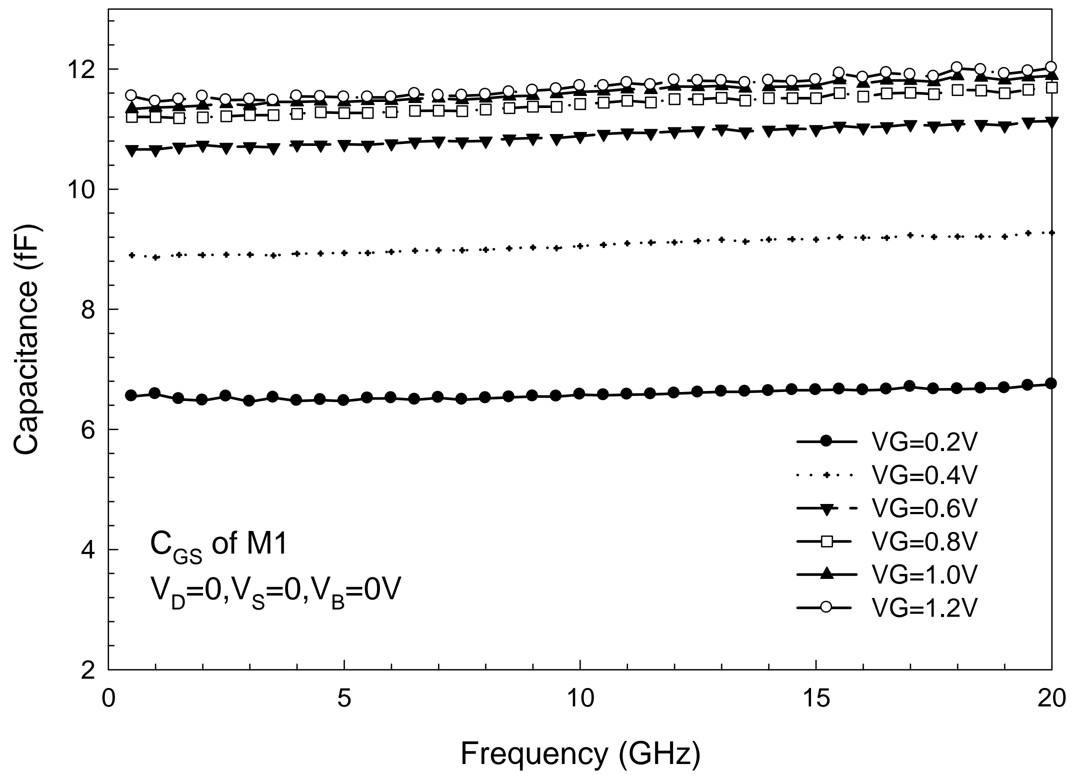
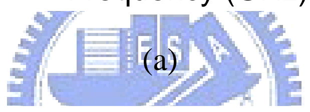
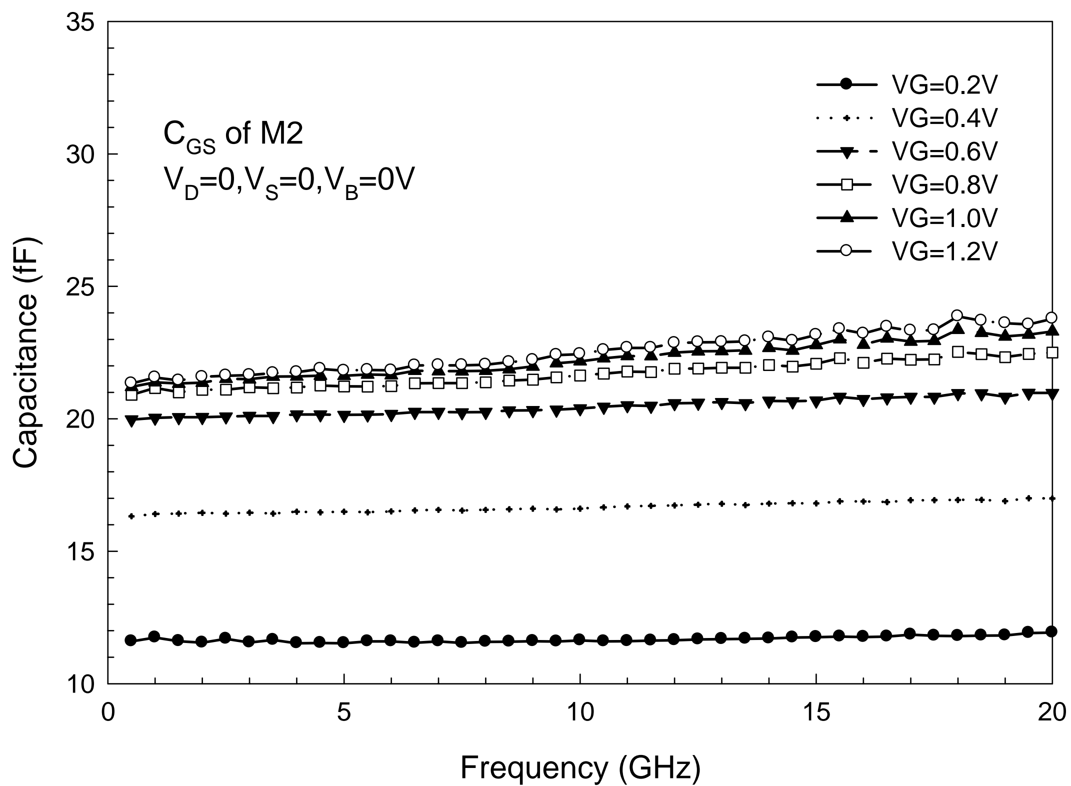


Fig.4.18 The extracted R_{SDB} of M1($3.6\mu m \times 4$), M2($7.2\mu m \times 4$), and M3($12\mu m \times 4$) devices, which are biased at VG=VD=VS=VB=0.

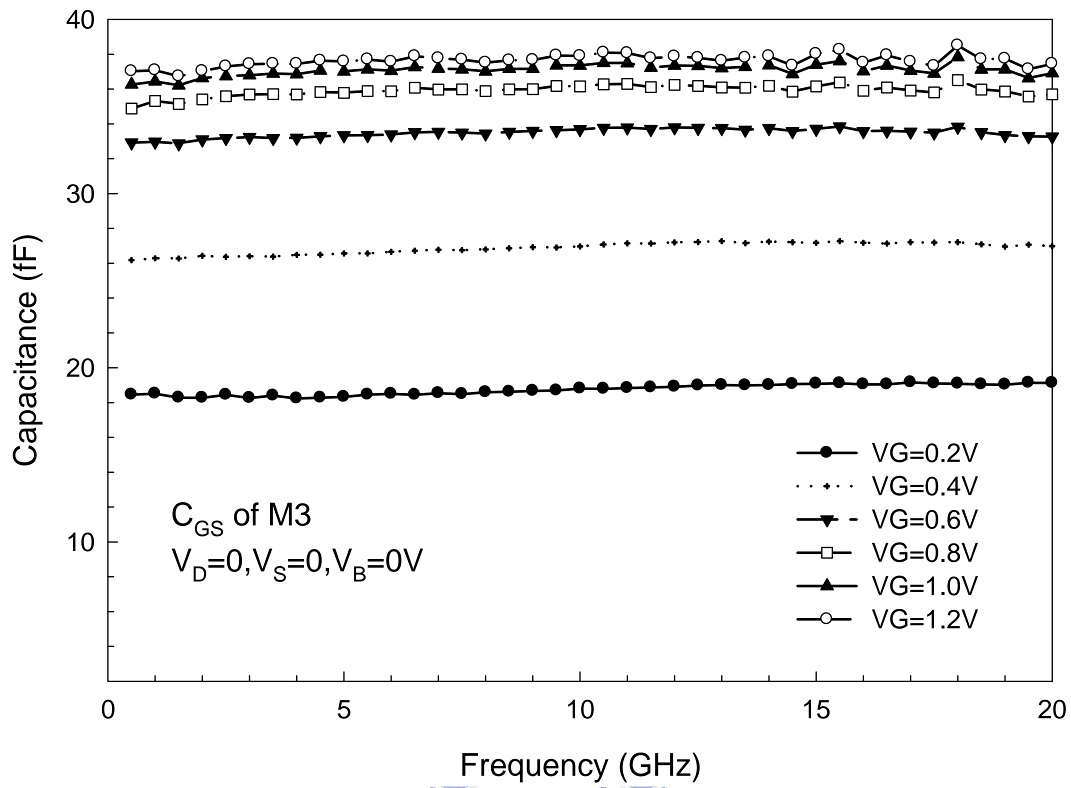




(a)

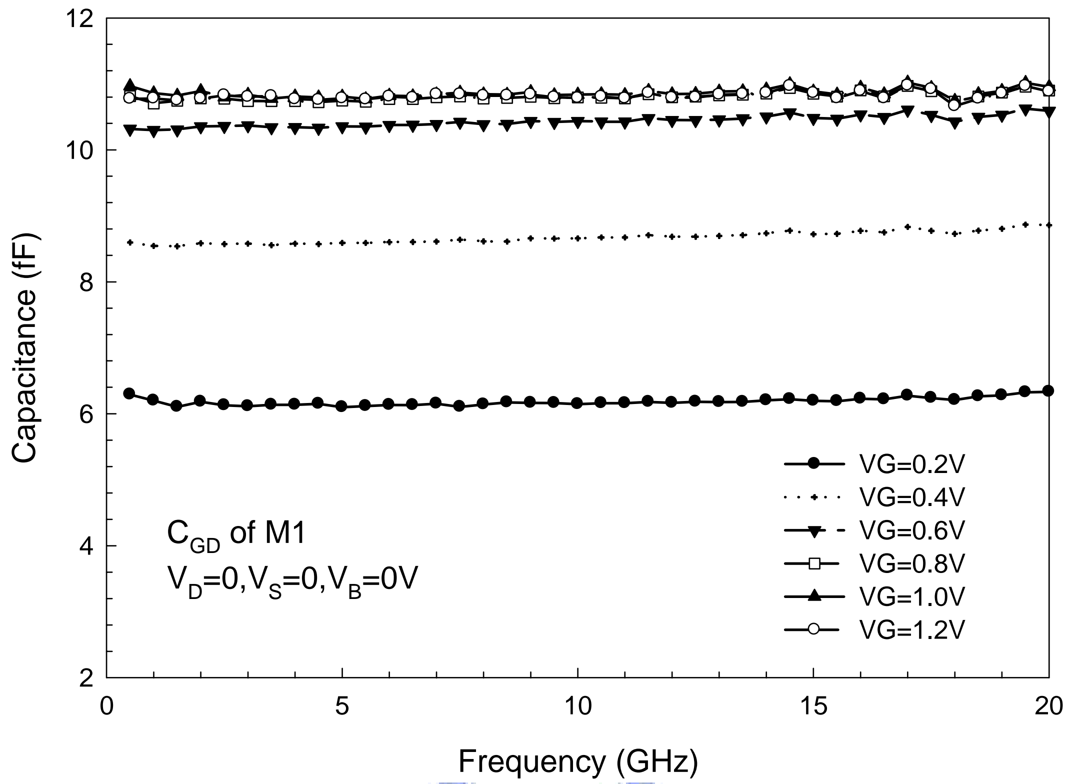


(b)

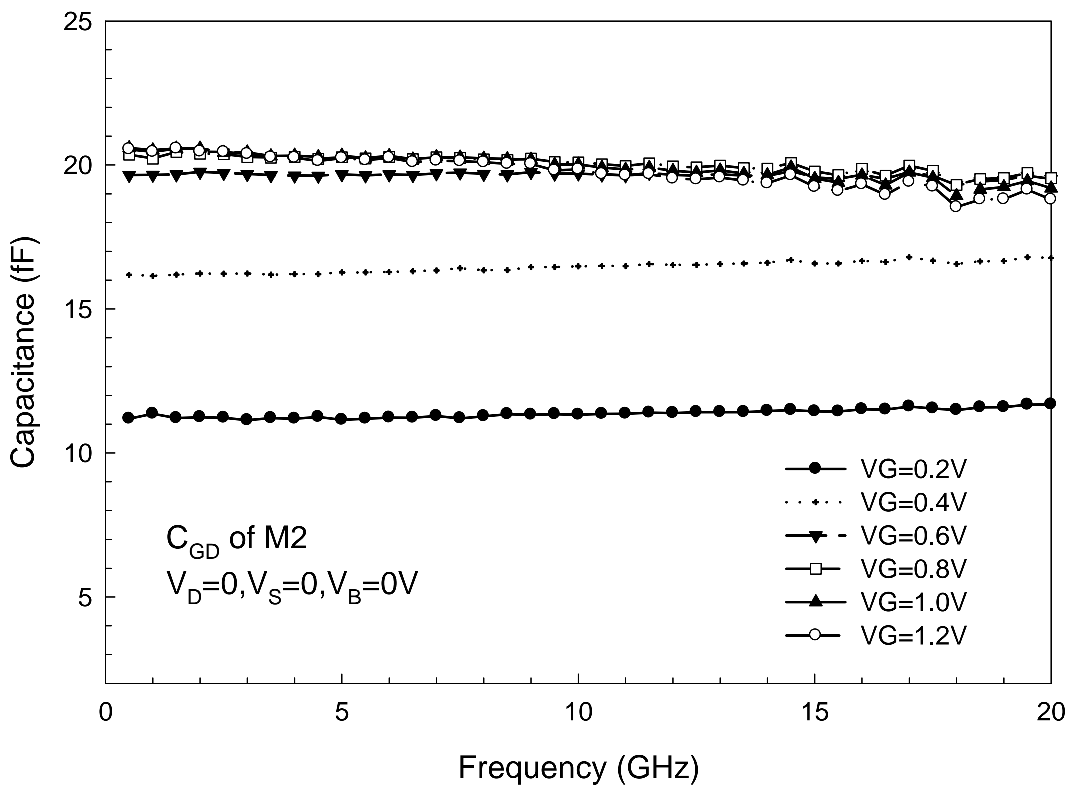


(c)

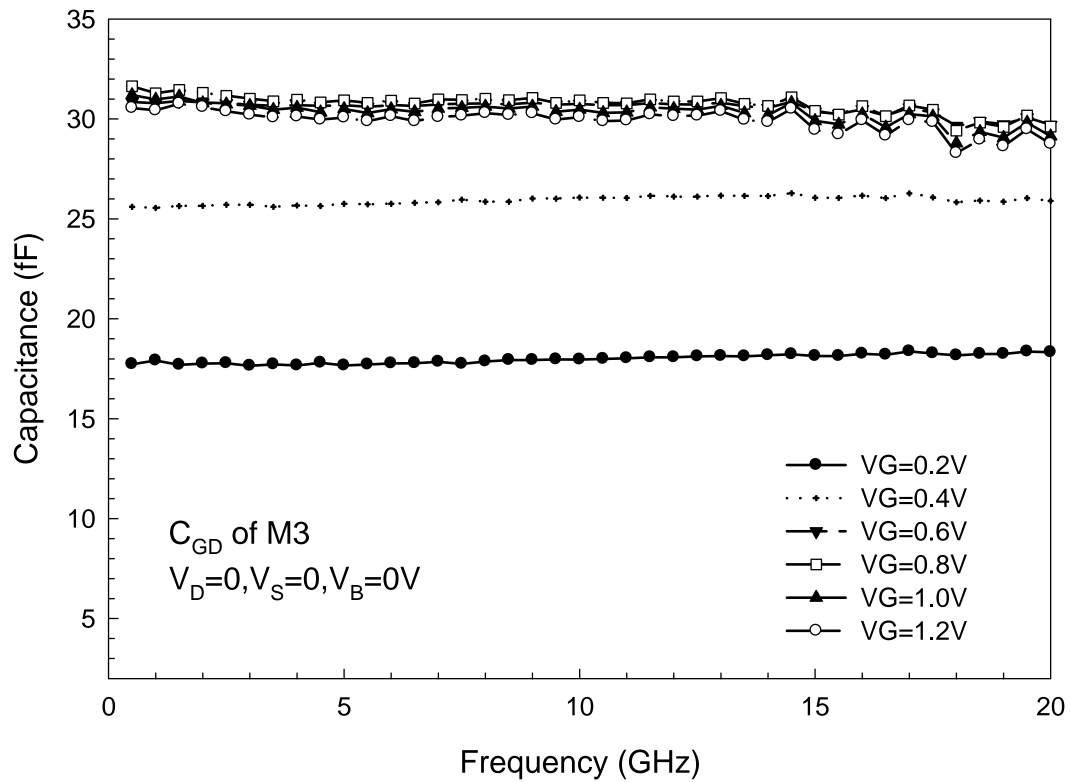
Fig.4.19 (a) The extracted C_{GS} of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted C_{GS} of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted C_{GS} of M3($12\mu m \times 4$) biased at different V_G.

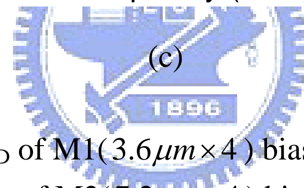


(a)



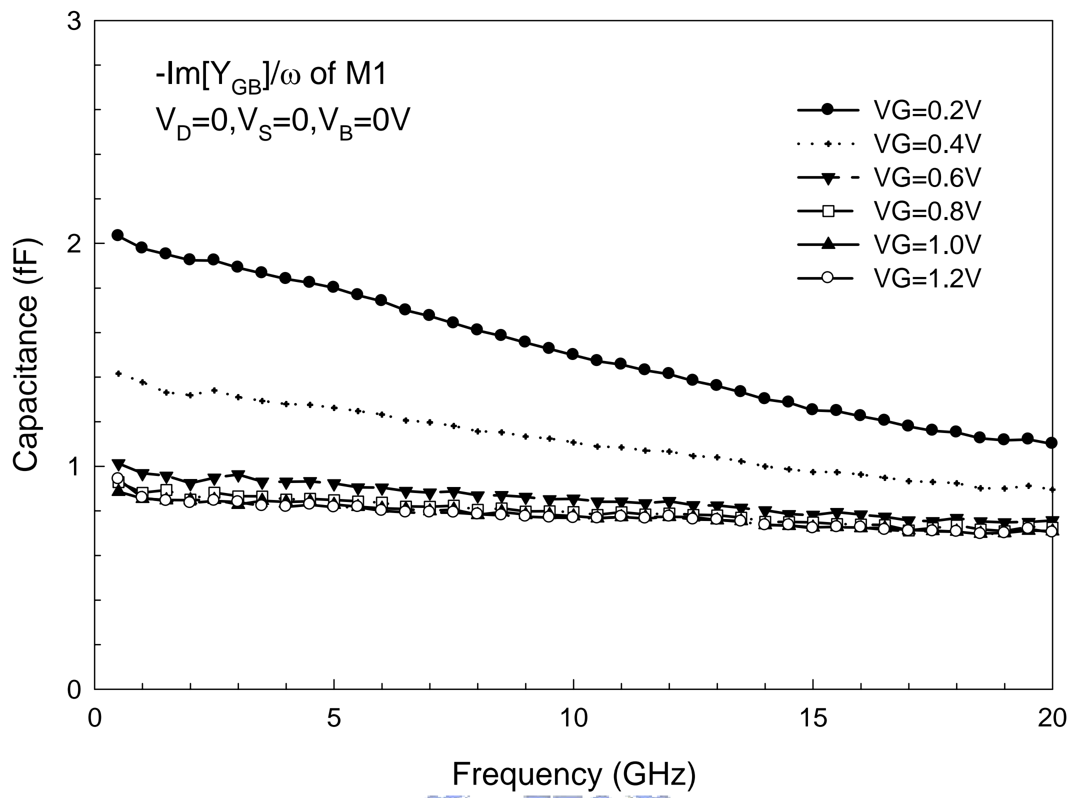
(b)

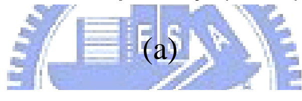




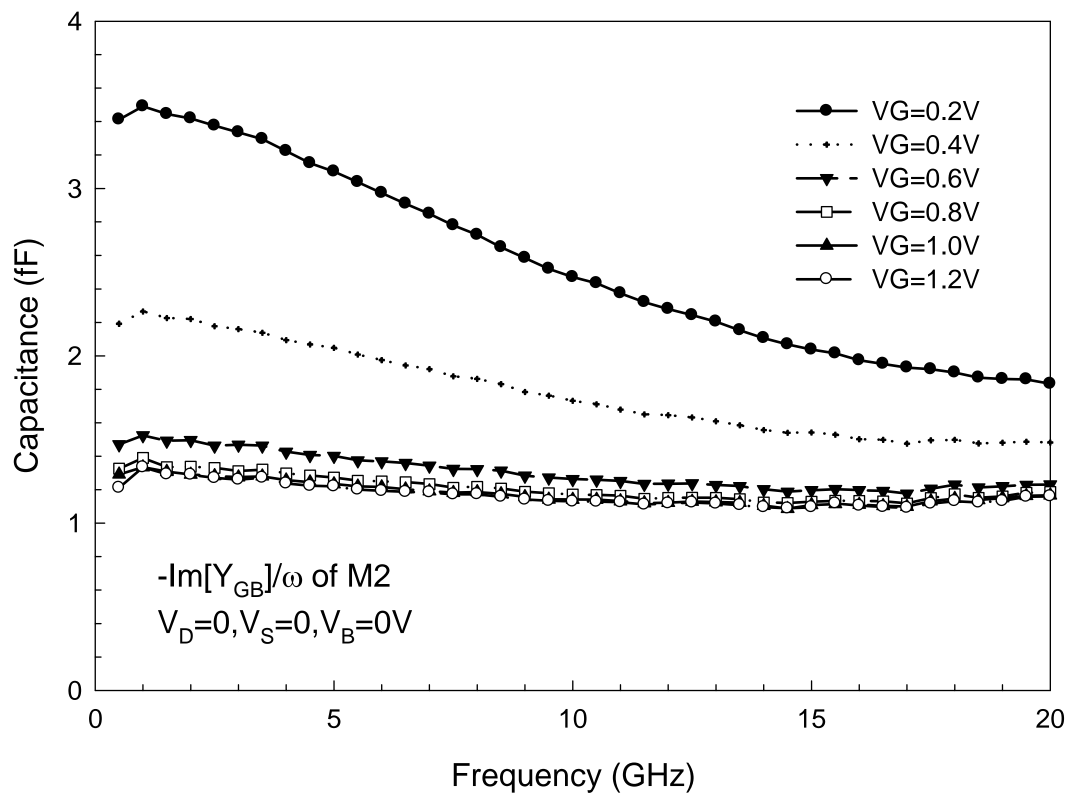
(c)

Fig.4.20 (a) The extracted C_{GD} of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted C_{GD} of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted C_{GD} of M3($12\mu m \times 4$) biased at different V_G.

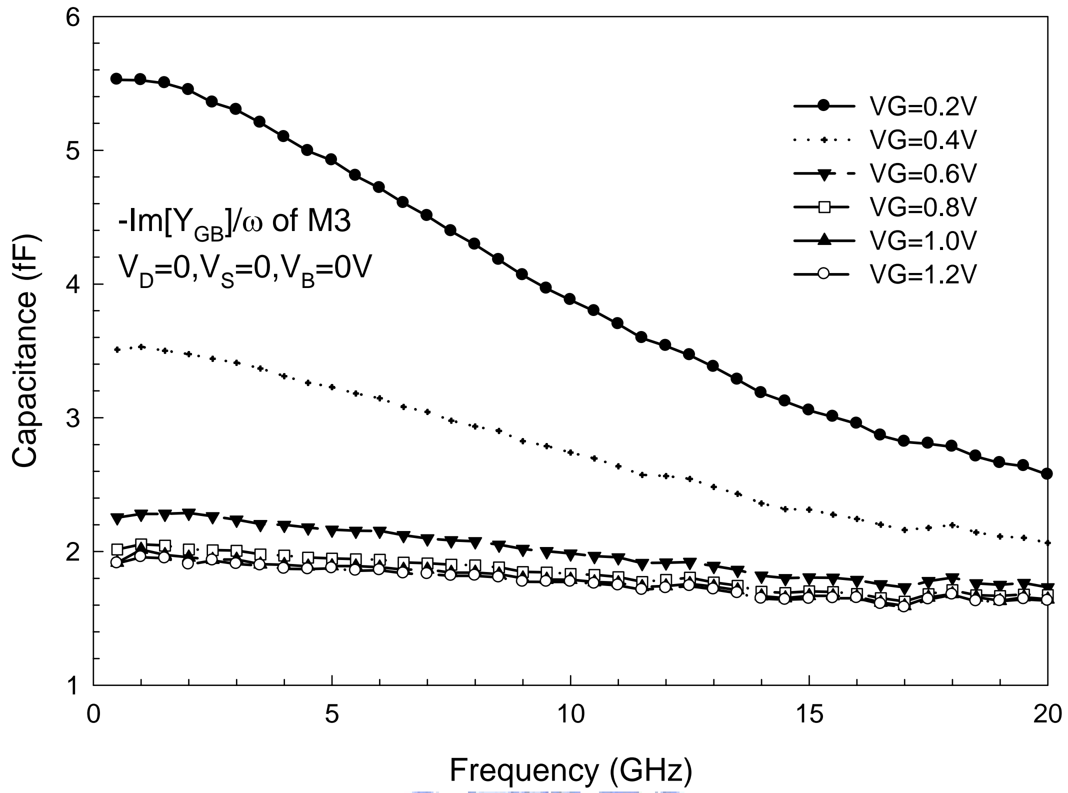




(a)

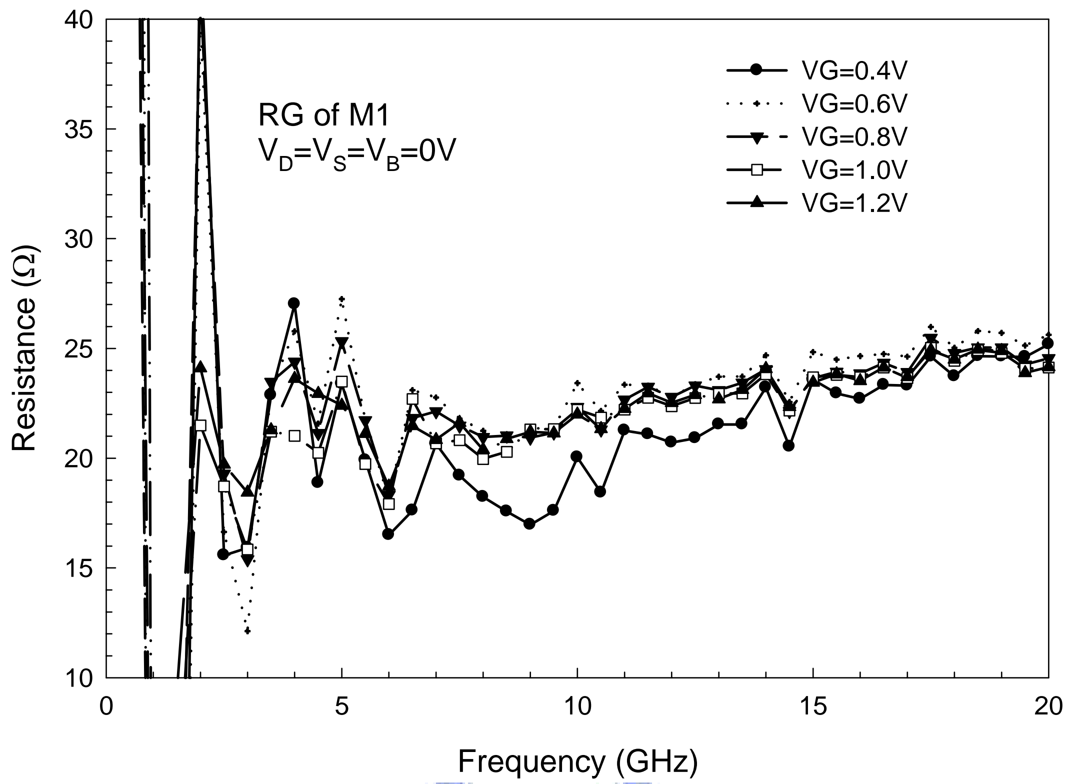


(b)

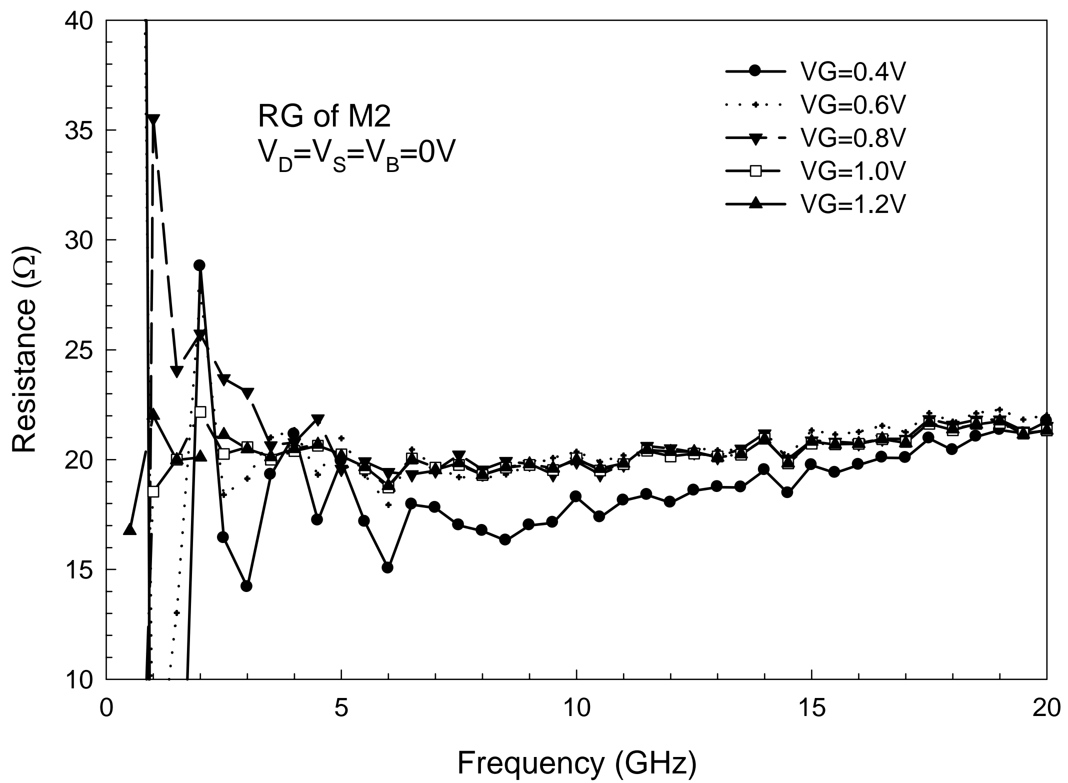


(c)

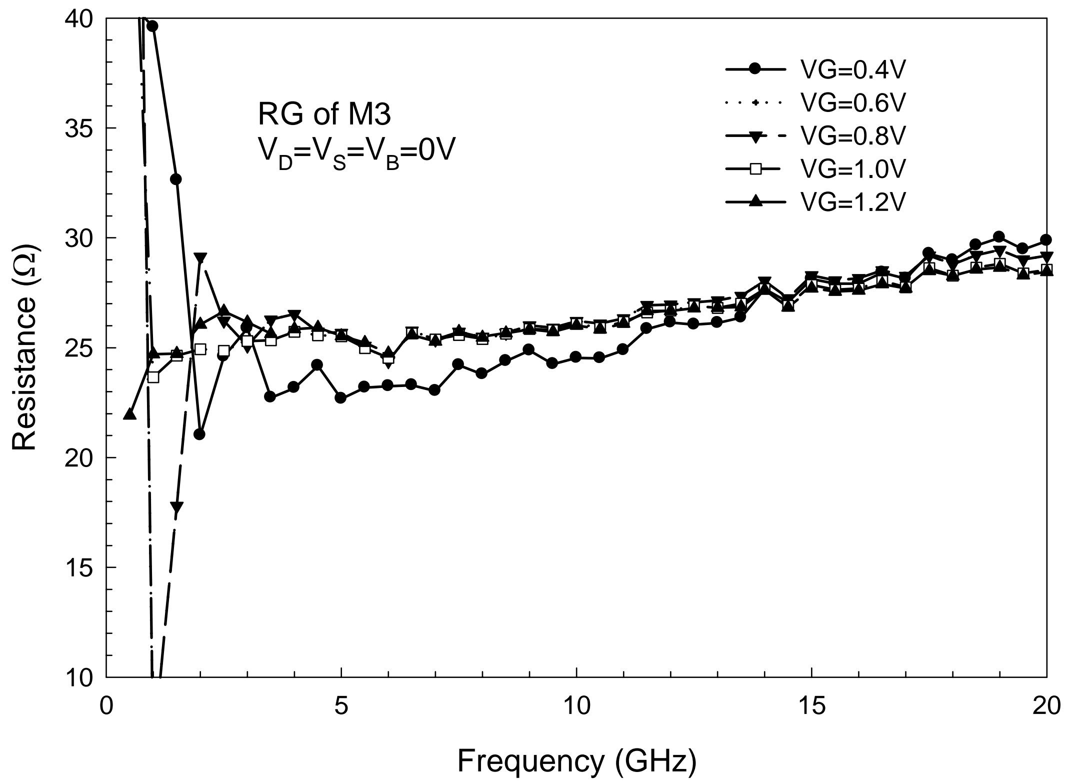
Fig.4.21 (a) The extracted $-\mathrm{Im}[Y_{GB}]/\omega$ of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted $-\mathrm{Im}[Y_{GB}]/\omega$ of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted $-\mathrm{Im}[Y_{GB}]/\omega$ of M3($12\mu m \times 4$) biased at different V_G.



(a)

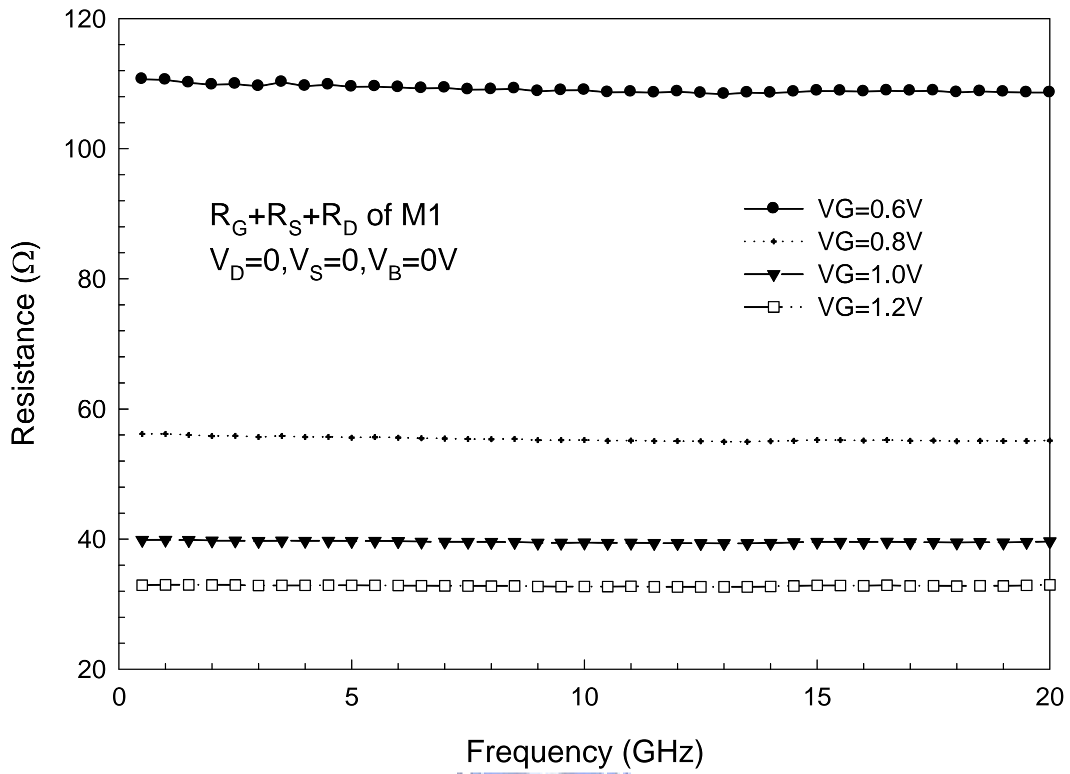


(b)

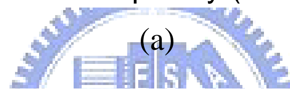


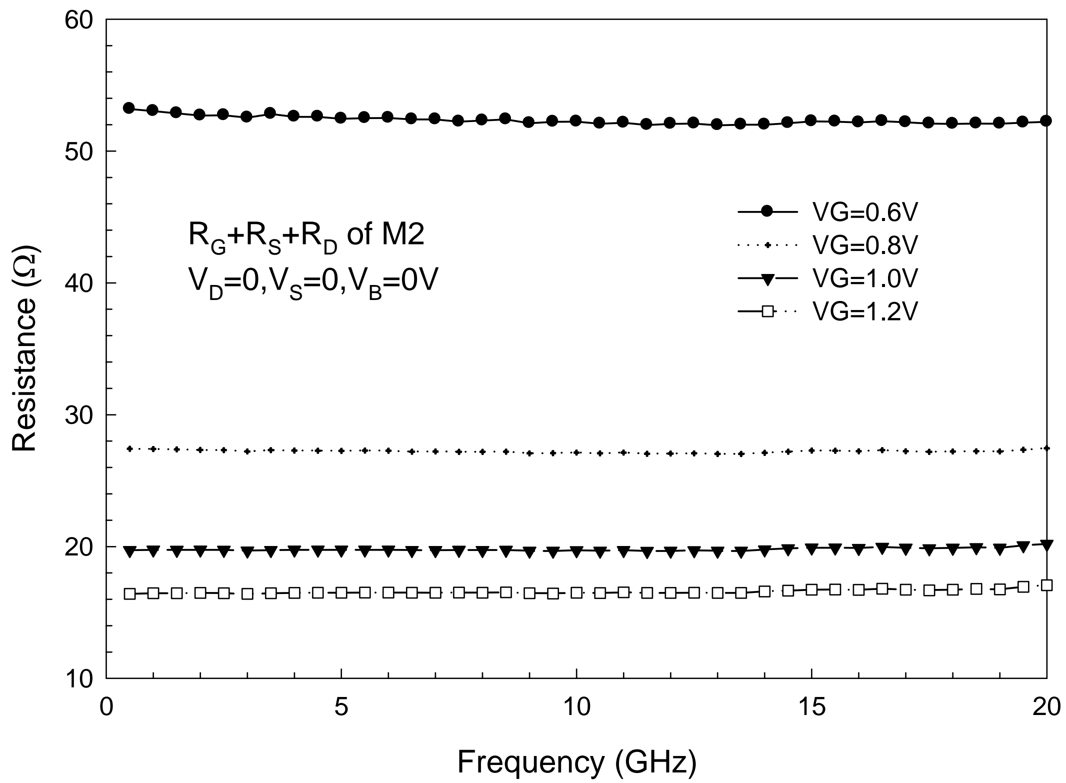
(c)

Fig.4.22 (a) The extracted R_G of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted R_G of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted R_G of M3($12\mu m \times 4$) biased at different V_G.

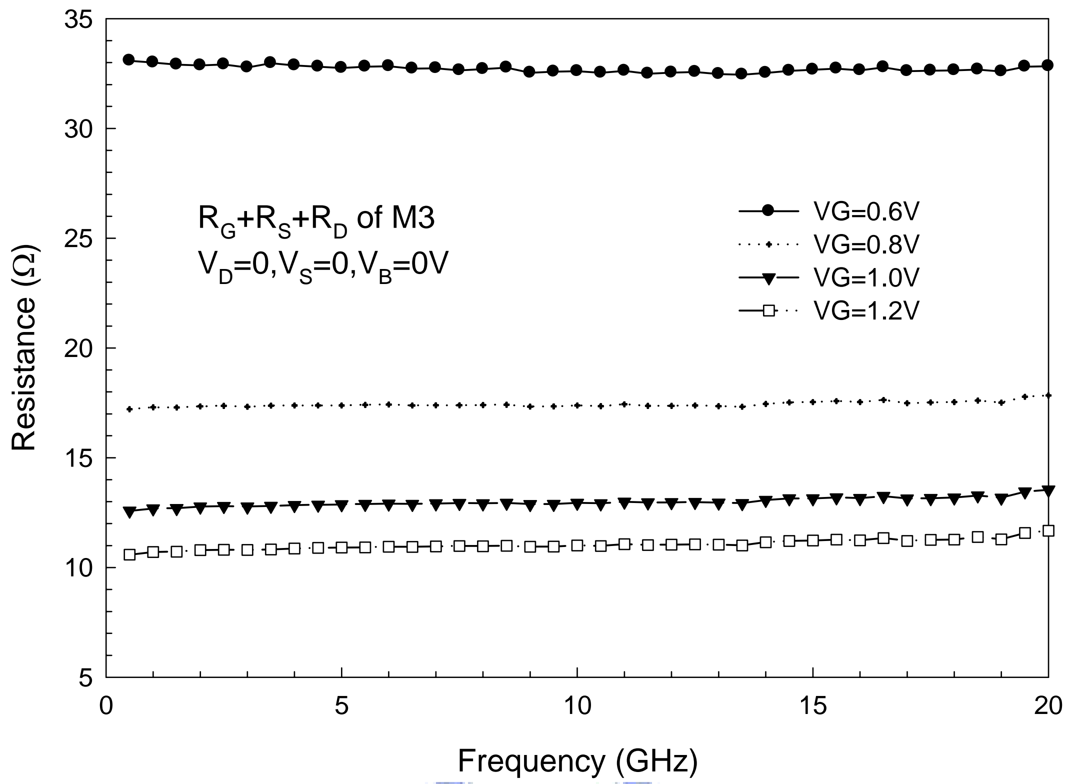


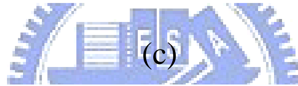
(a)



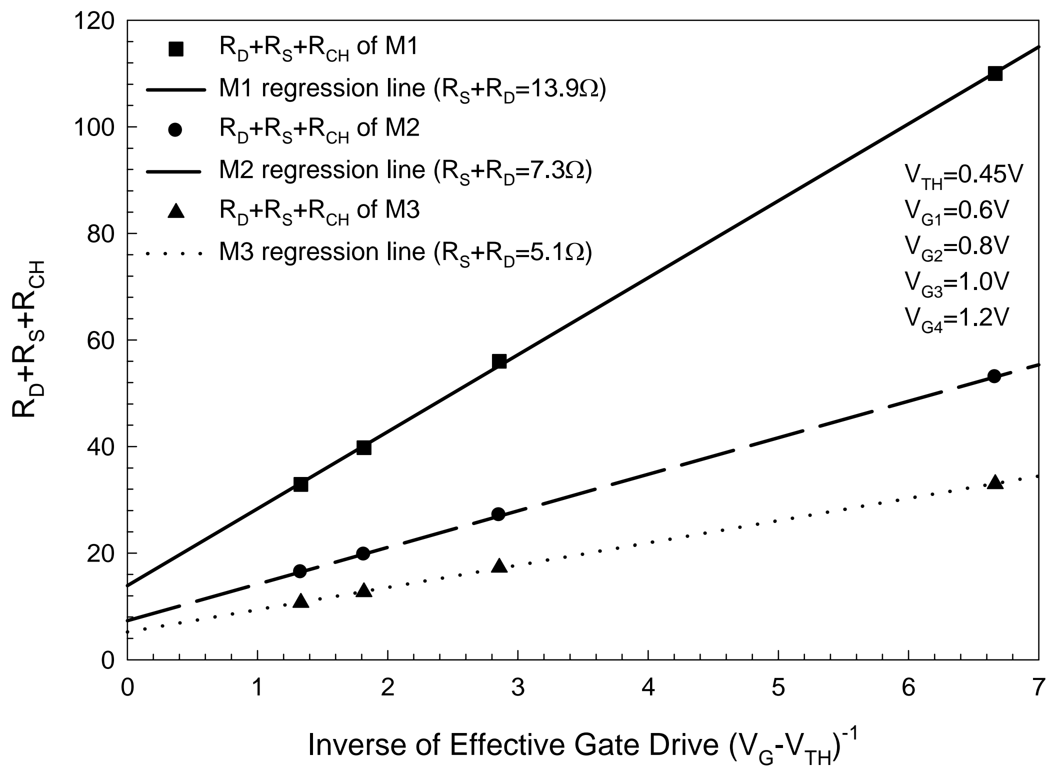


(b)



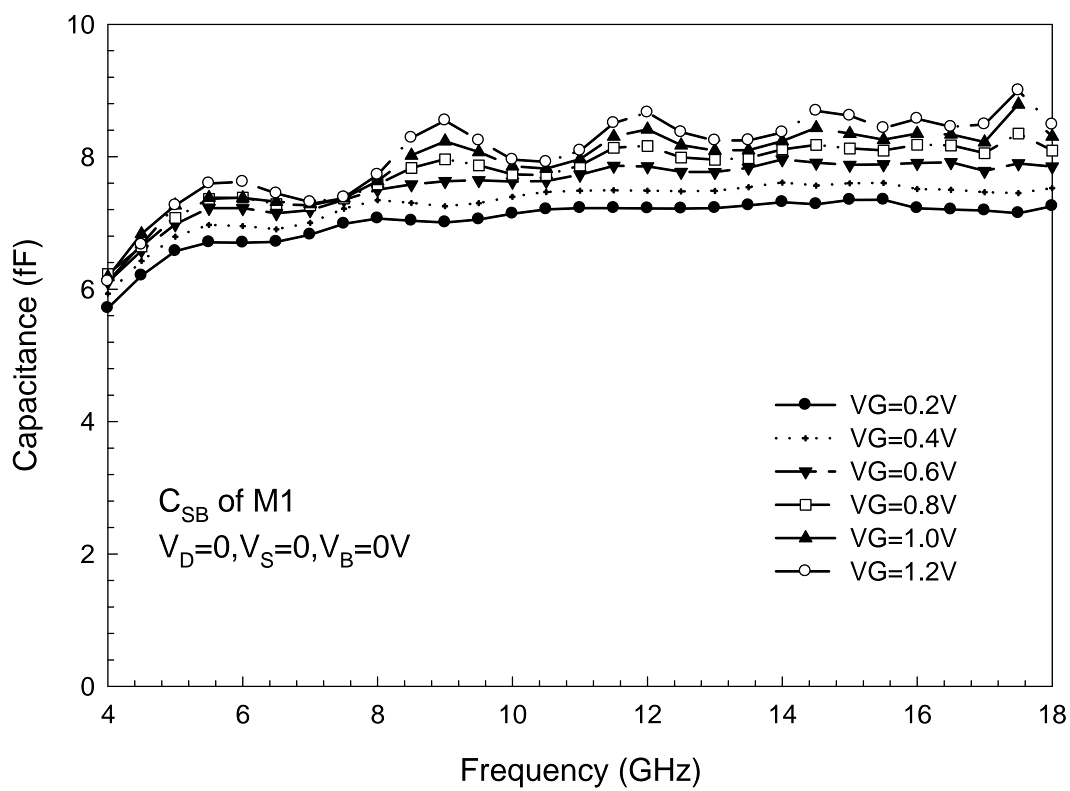


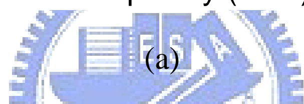
(c)



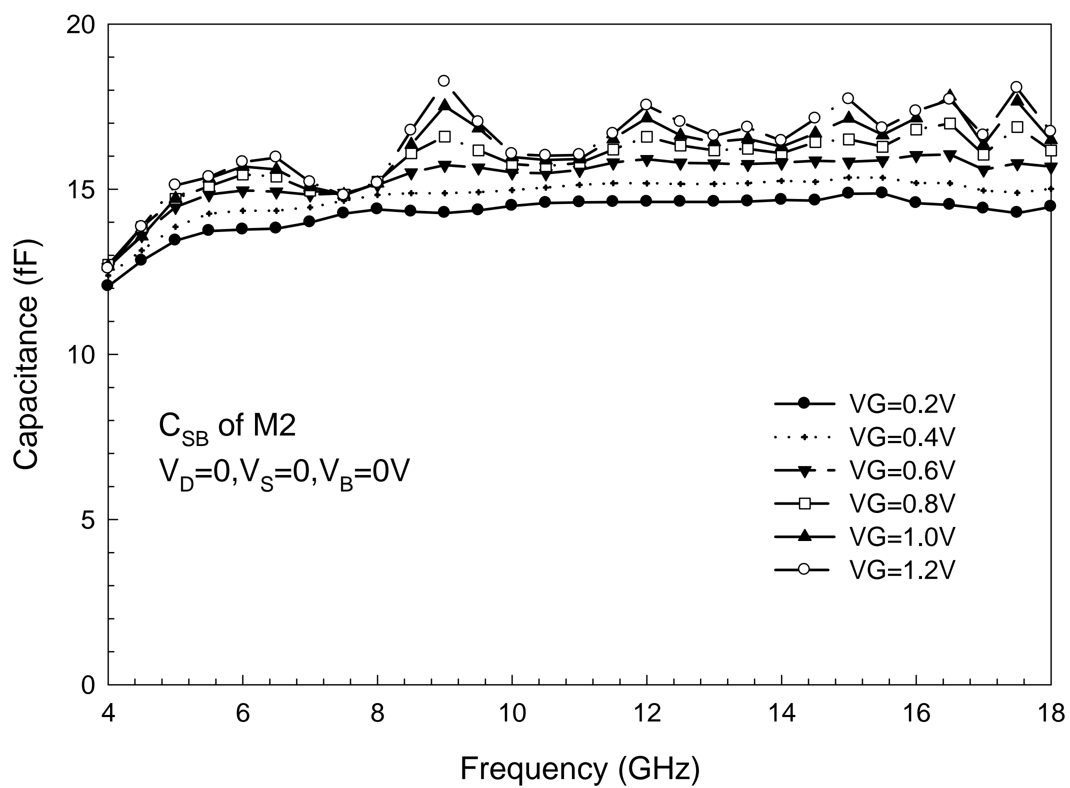
(d)

Fig.4.23 (a) The extracted $R_{CH}+R_S+R_D$ of M1($3.6\mu m\times 4$) biased at different V_G.
(b) The extracted $R_{CH}+R_S+R_D$ of M2($7.2\mu m\times 4$) biased at different V_G.
(c) The extracted $R_{CH}+R_S+R_D$ of M3($12\mu m\times 4$) biased at different V_G.
(d) $R_{CH}+R_S+R_D$ versus $\left(V_G - V_{TH}\right)^{-1}$ of M1($3.6\mu m\times 4$), M2($7.2\mu m\times 4$), and M3($12\mu m\times 4$).

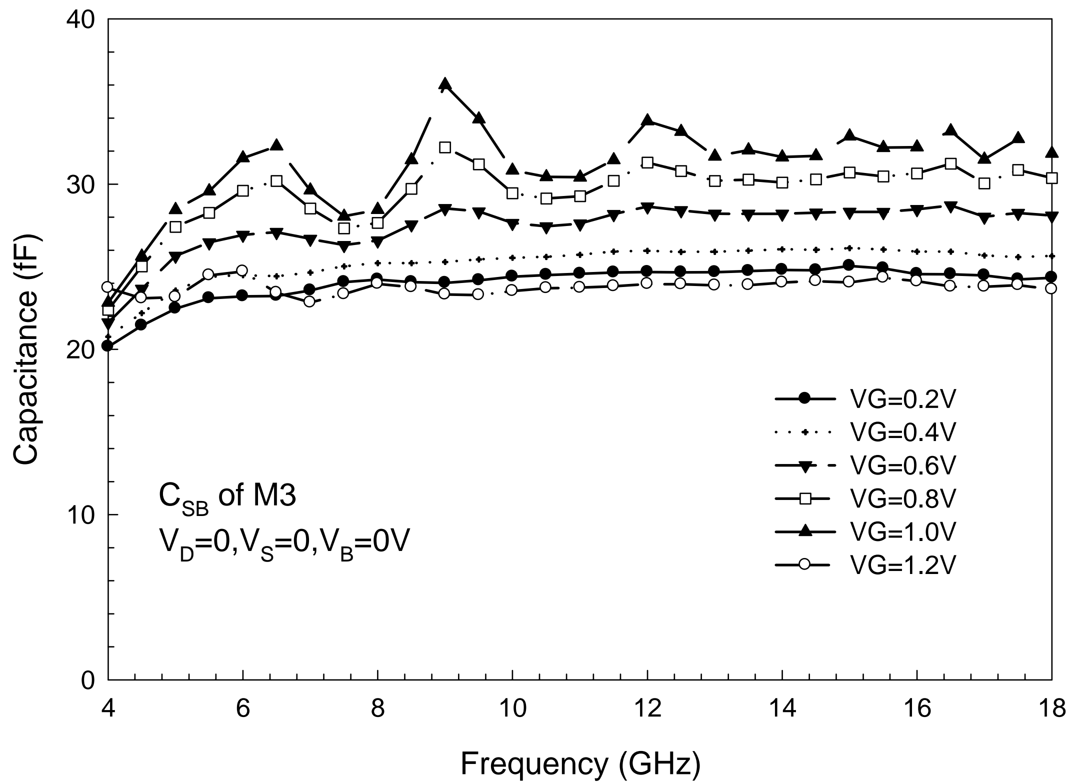




(a)



(b)

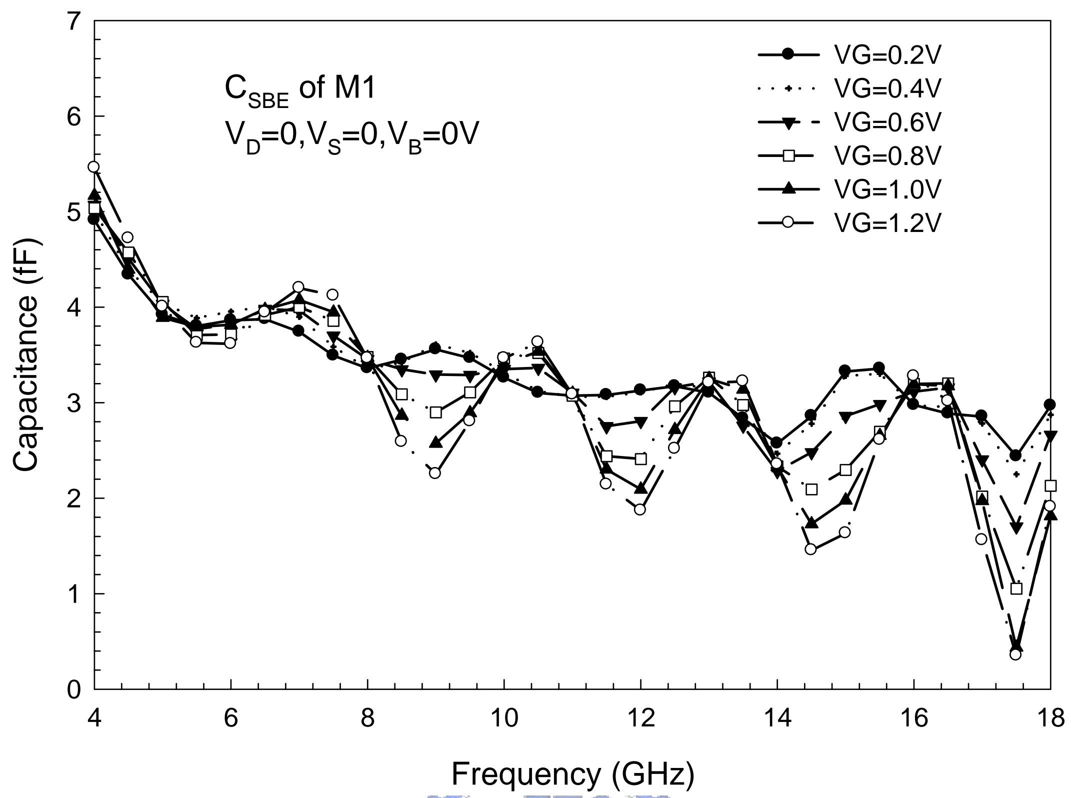


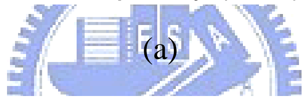
(c)

Fig.4.24 (a) The extracted C_{SB} of M1($3.6\mu m \times 4$) biased at different V_G.

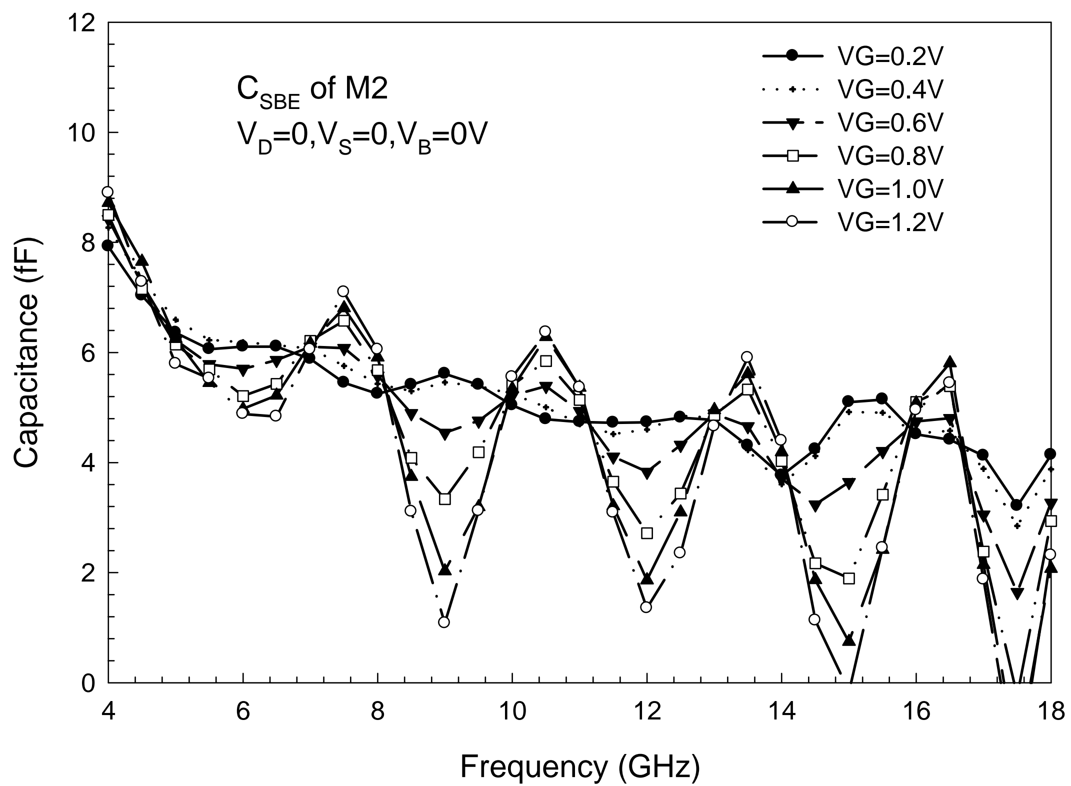
(b) The extracted C_{SB} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{SB} of M3($12\mu m \times 4$) biased at different V_G.

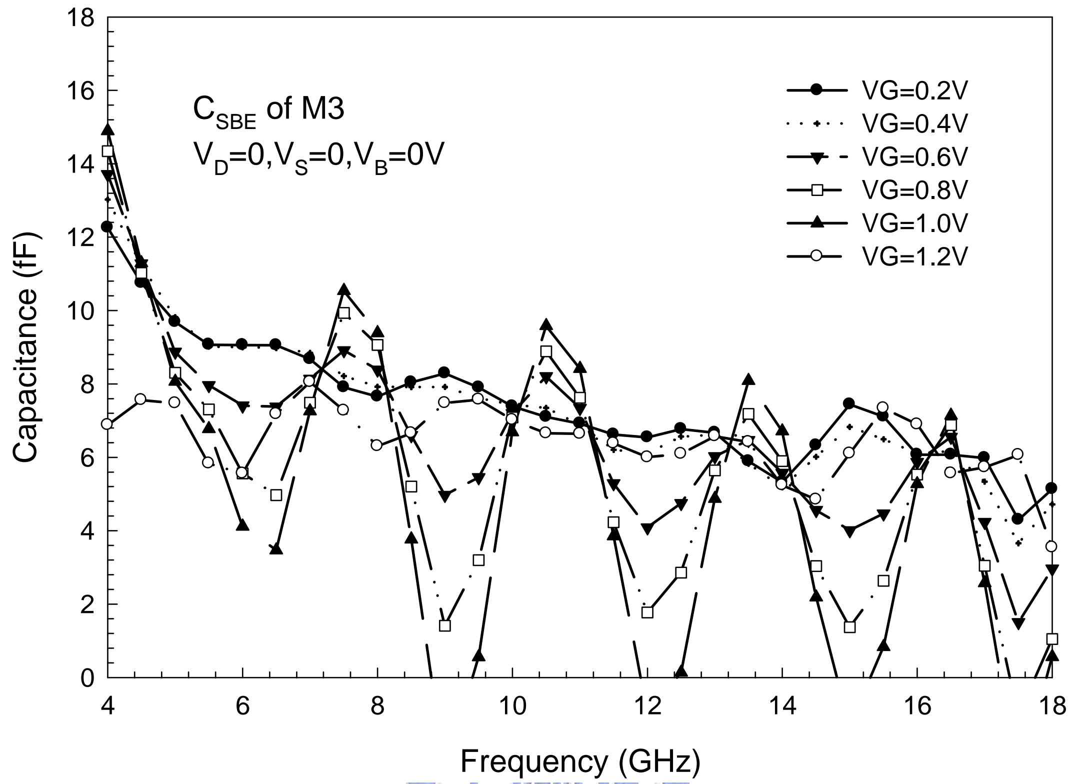




(a)

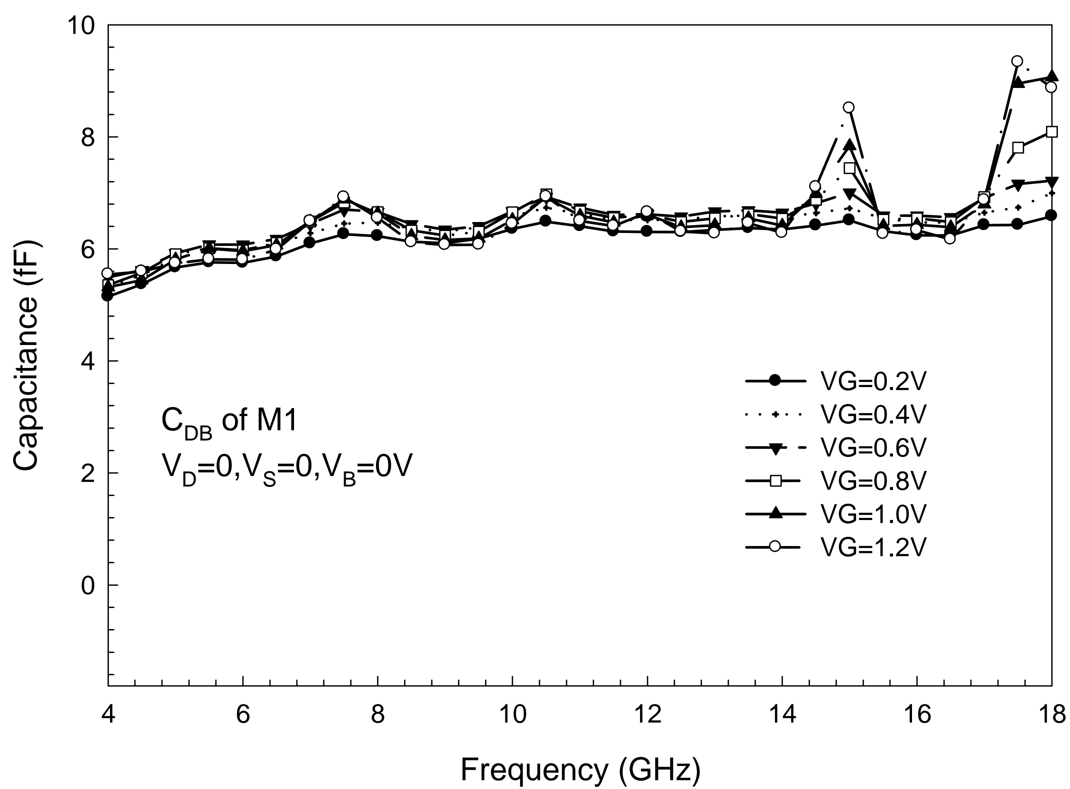


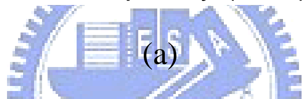
(b)



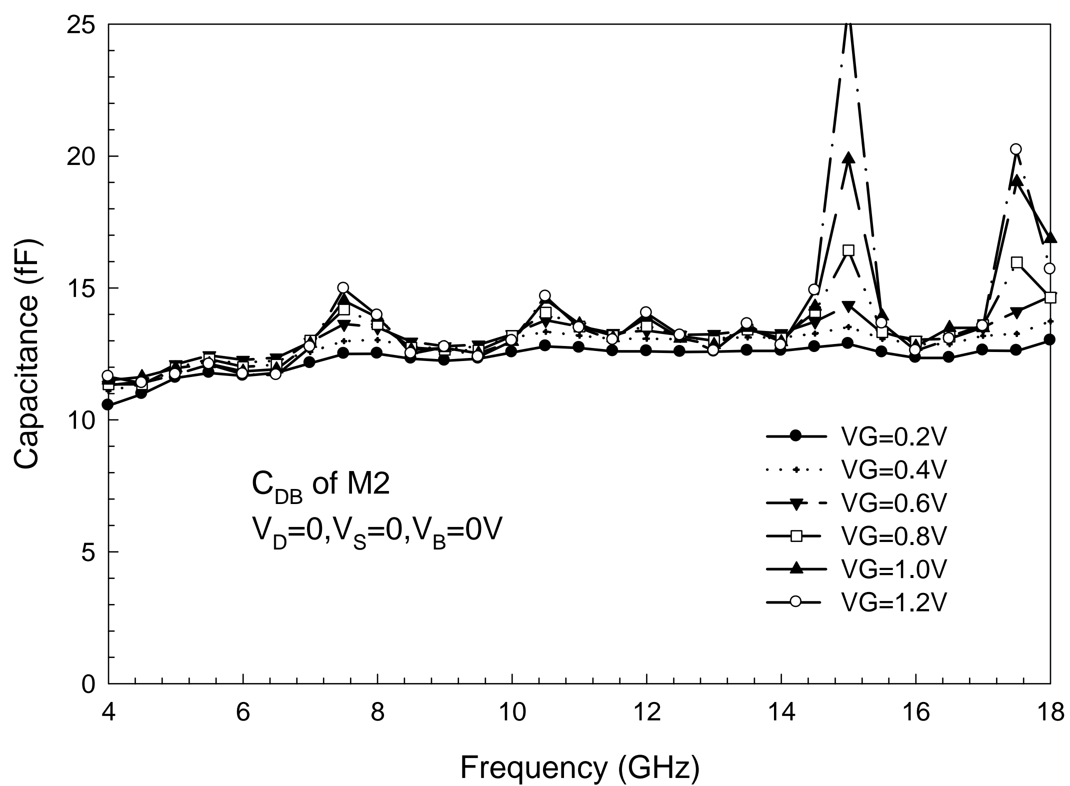
(c)

Fig.4.25 (a) The extracted C_{SBE} of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted C_{SBE} of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted C_{SBE} of M3($12\mu m \times 4$) biased at different V_G.

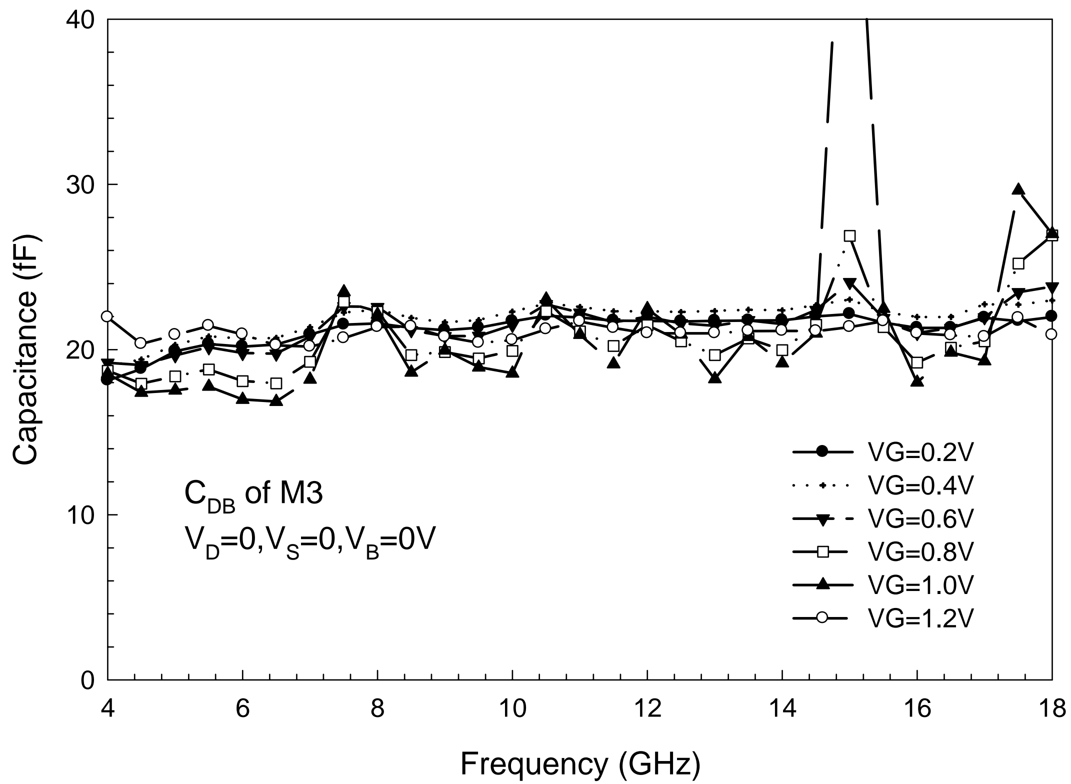


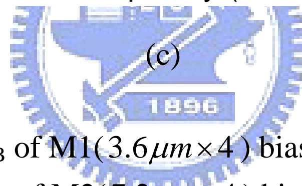


(a)



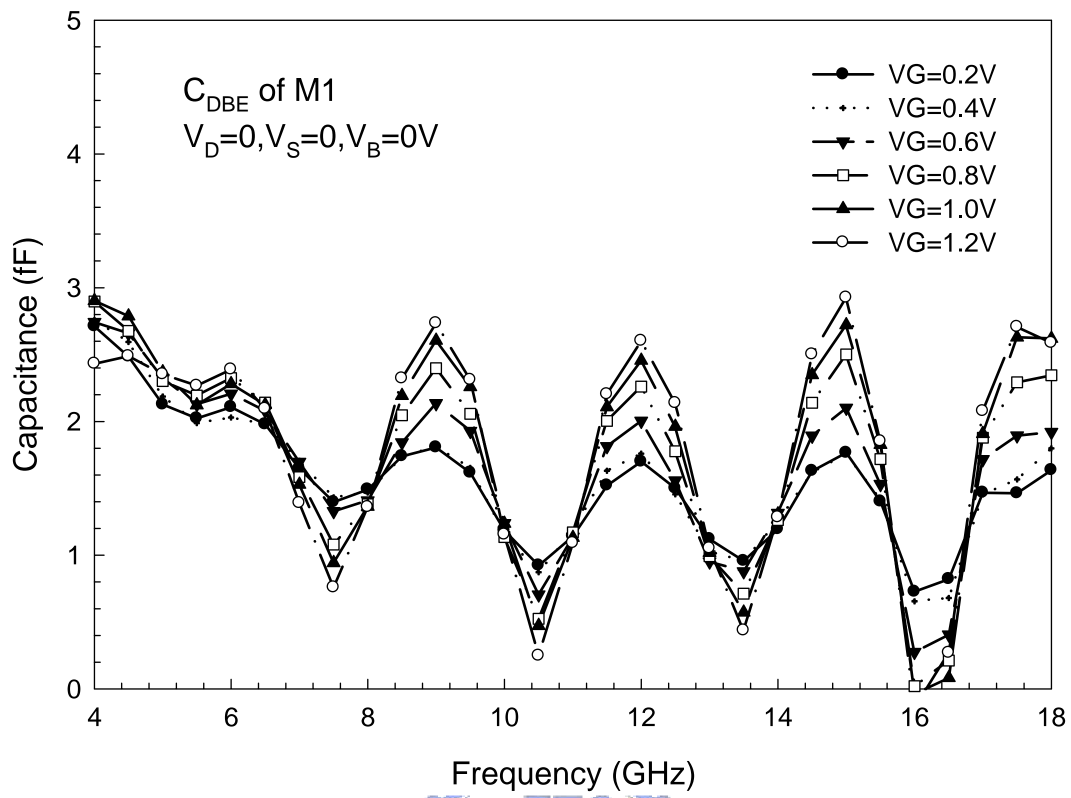
(b)

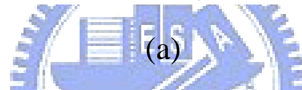




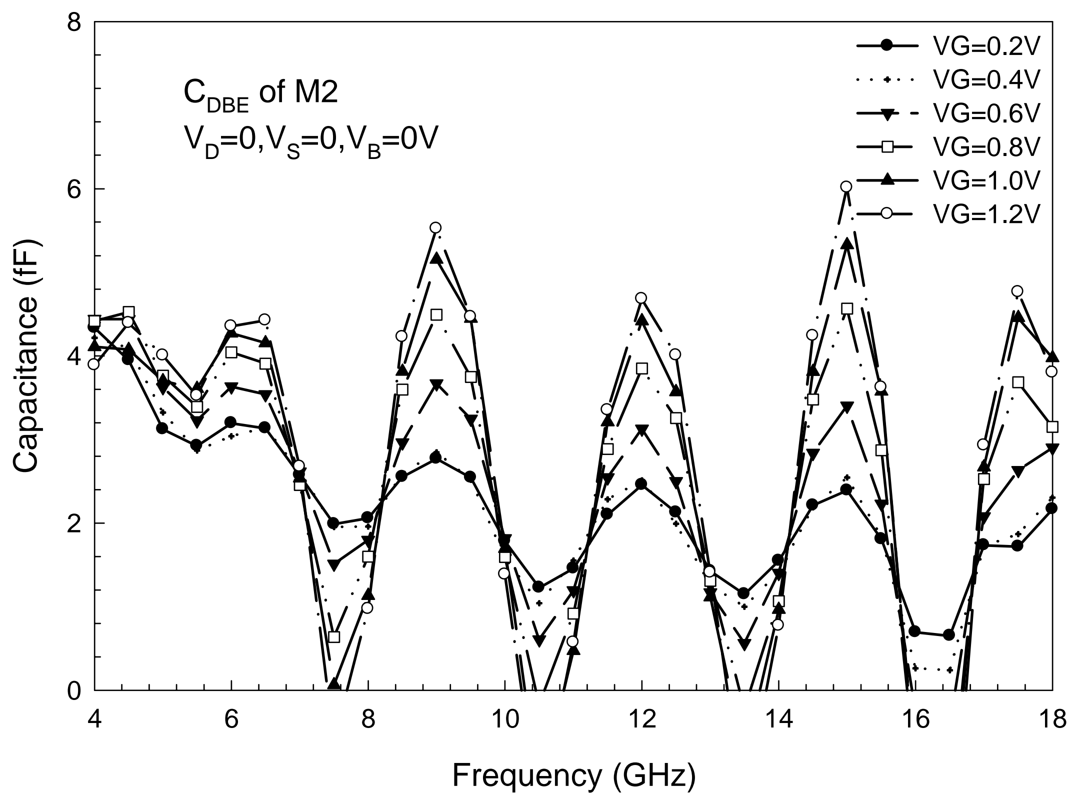
(c)

Fig.4.26 (a) The extracted C_{DB} of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted C_{DB} of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted C_{DB} of M3($12\mu m \times 4$) biased at different V_G.

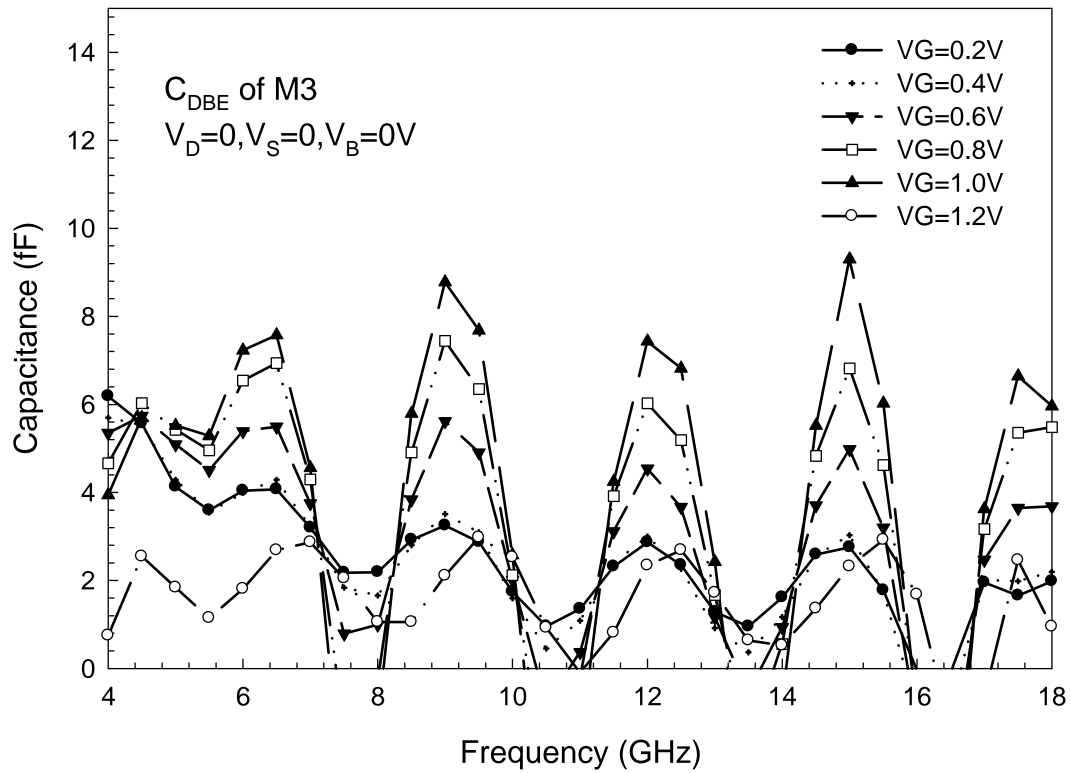




(a)

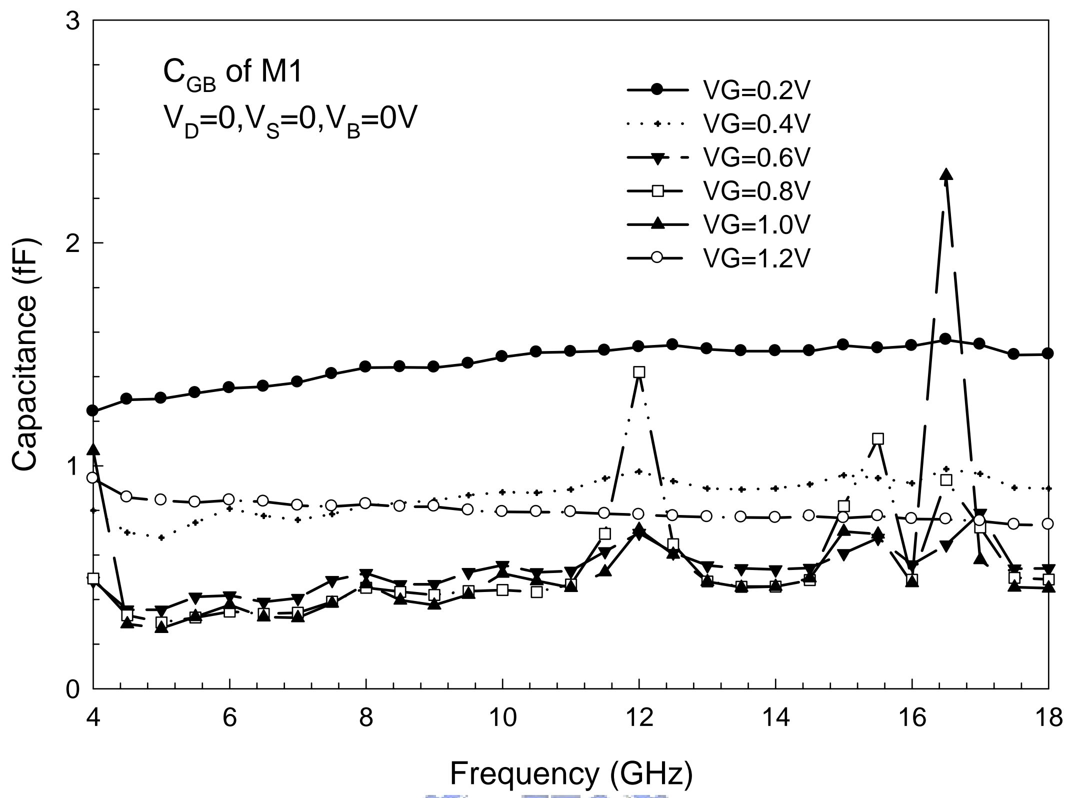


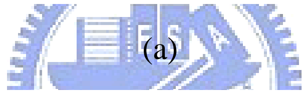
(b)



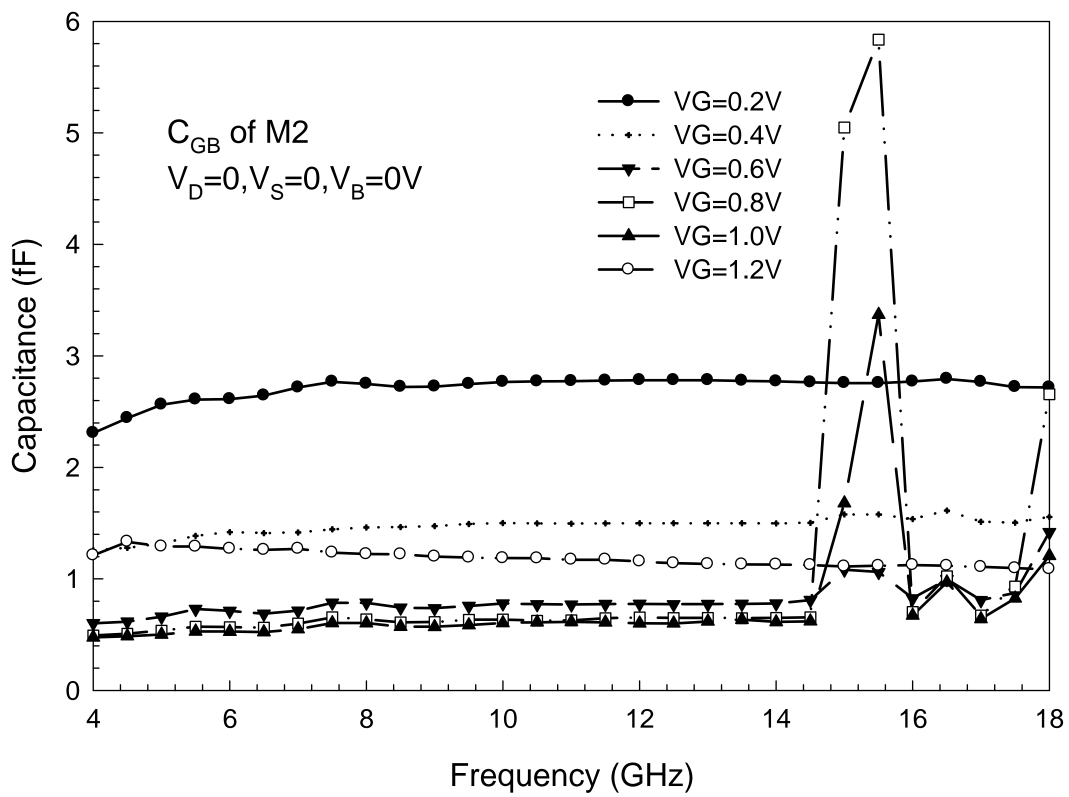
(c)

Fig.4.27 (a) The extracted C_{SBE} of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted C_{SBE} of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted C_{SBE} of M3($12\mu m \times 4$) biased at different V_G.

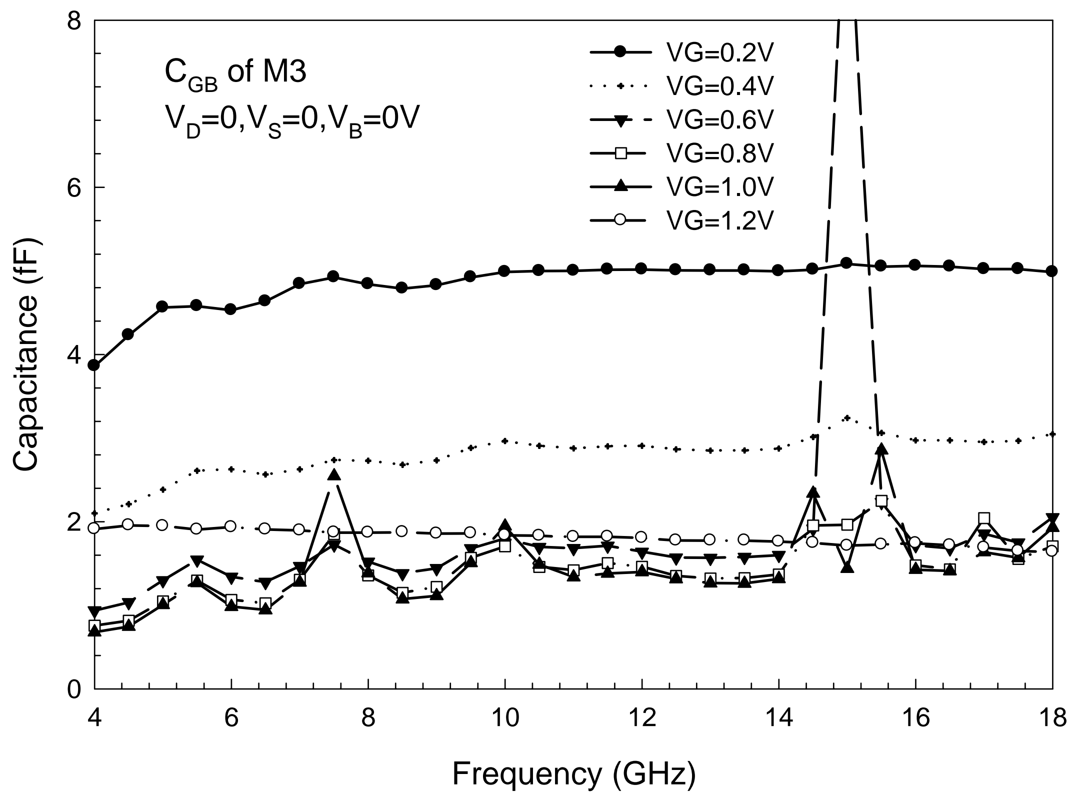




(a)



(b)

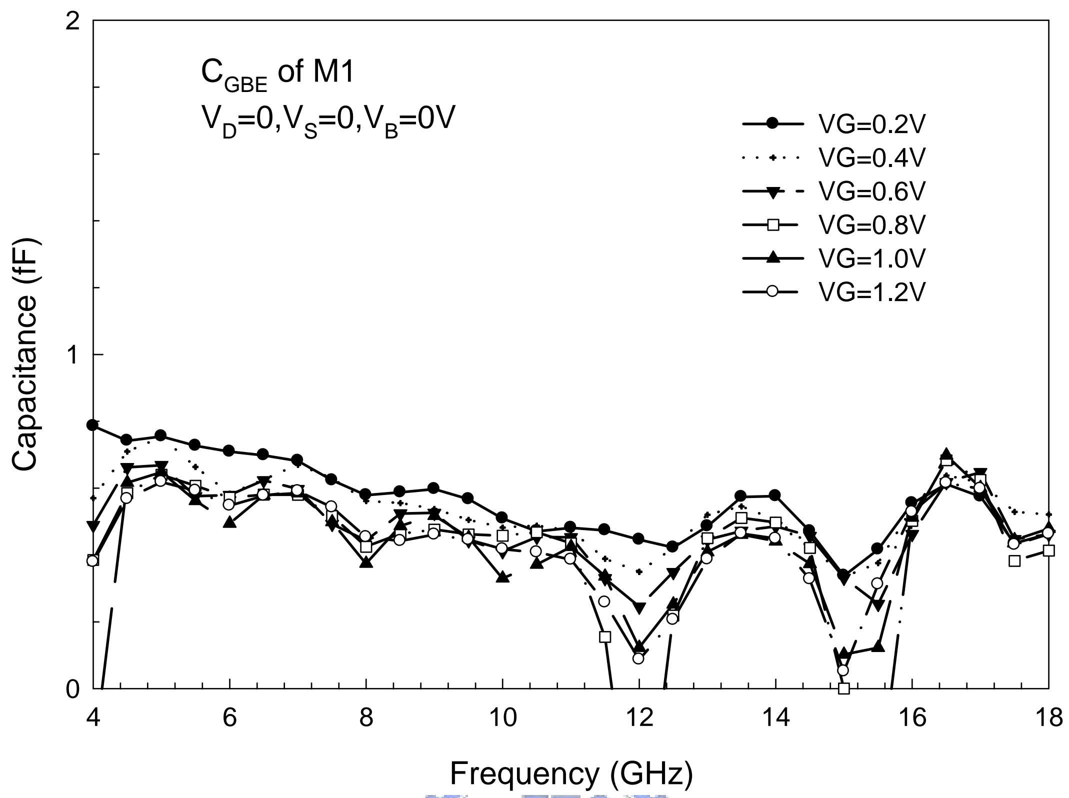


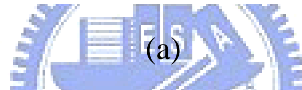
(c)

Fig.4.28 (a) The extracted C_{GB} of M1($3.6\mu m \times 4$) biased at different V_G.

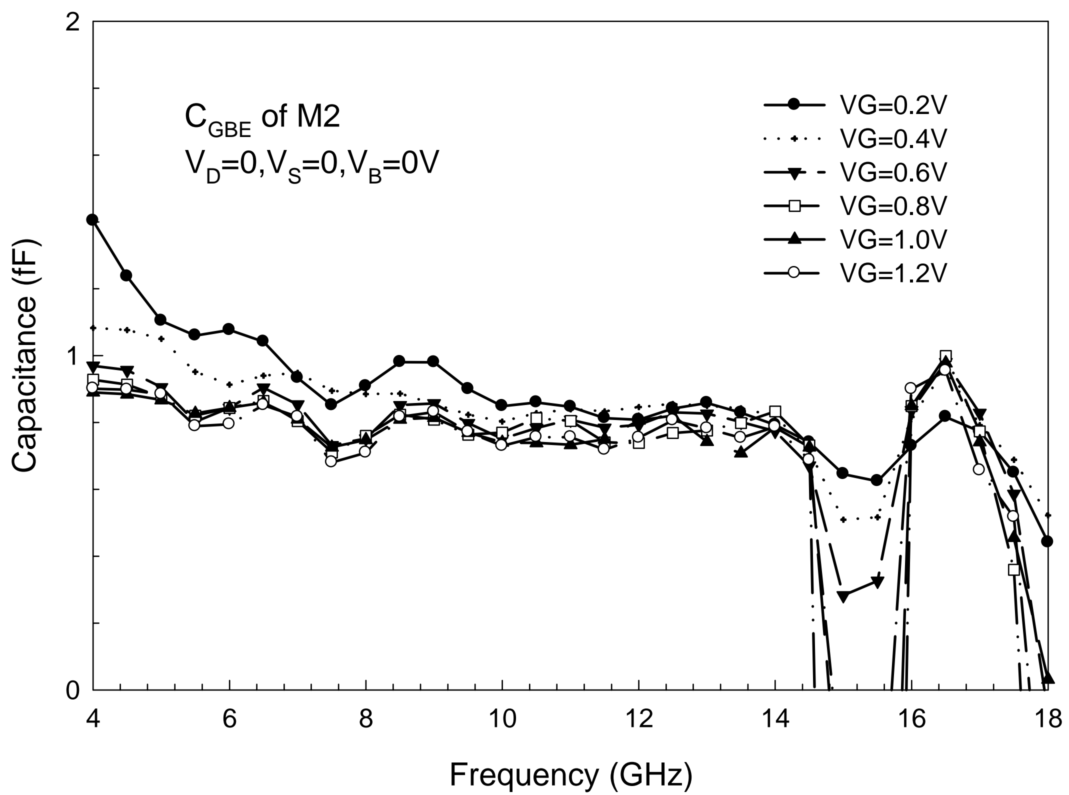
(b) The extracted C_{GB} of M2($7.2\mu m \times 4$) biased at different V_G.

(c) The extracted C_{GB} of M3($12\mu m \times 4$) biased at different V_G.

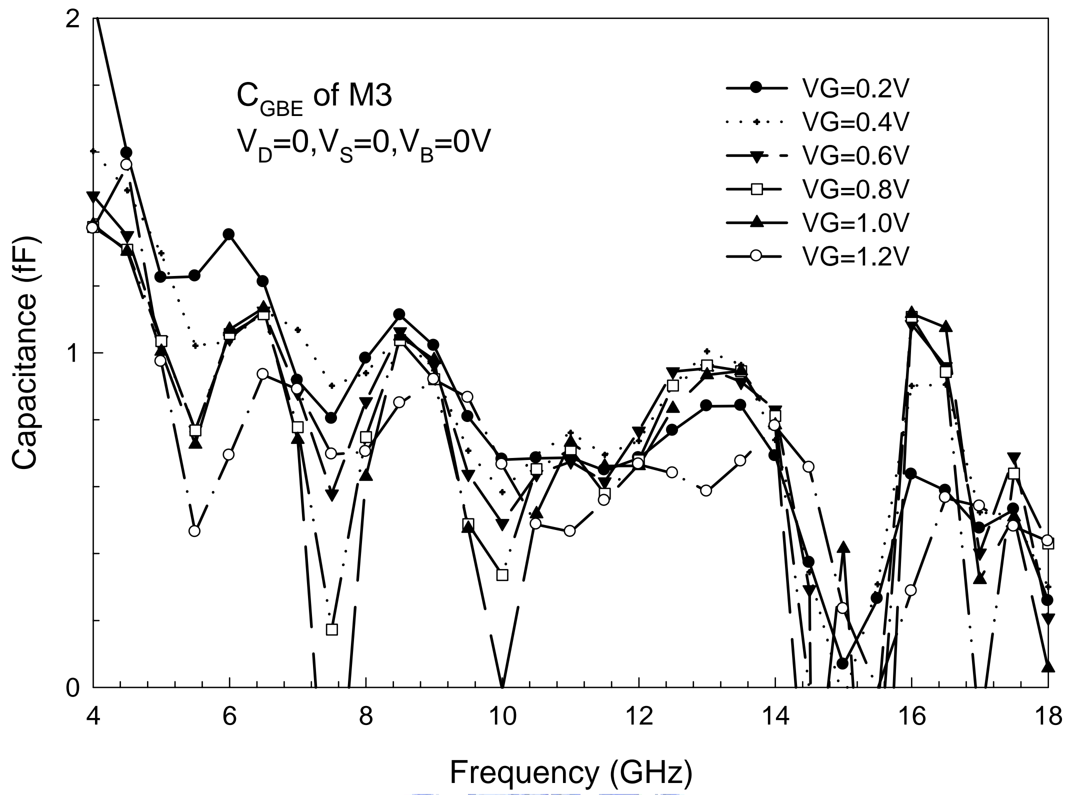


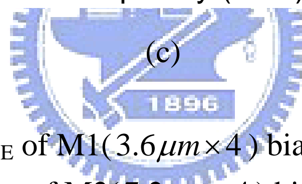


(a)



(b)



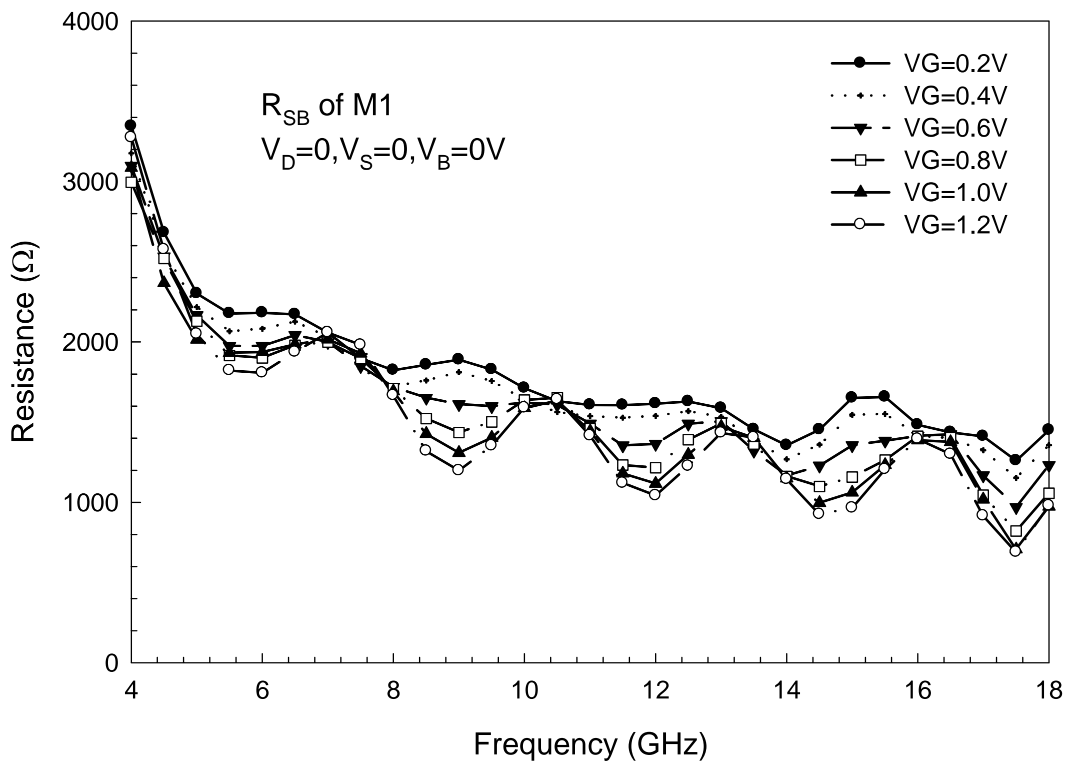


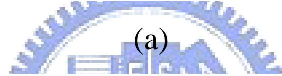
(c)

Fig.4.29 (a) The extracted C_{GBE} of M1($3.6\mu m\times 4$) biased at different V_G.

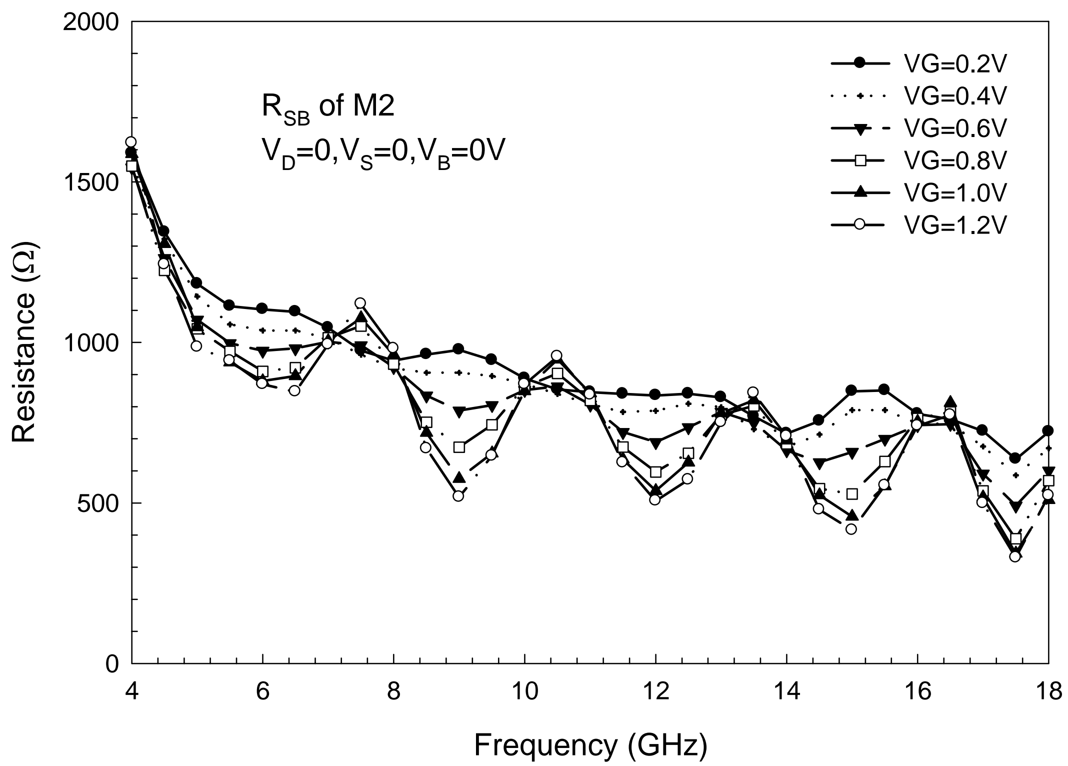
(b) The extracted C_{GBE} of M2($7.2\mu m\times 4$) biased at different V_G.

(c) The extracted C_{GBE} of M3($12\mu m\times 4$) biased at different V_G.

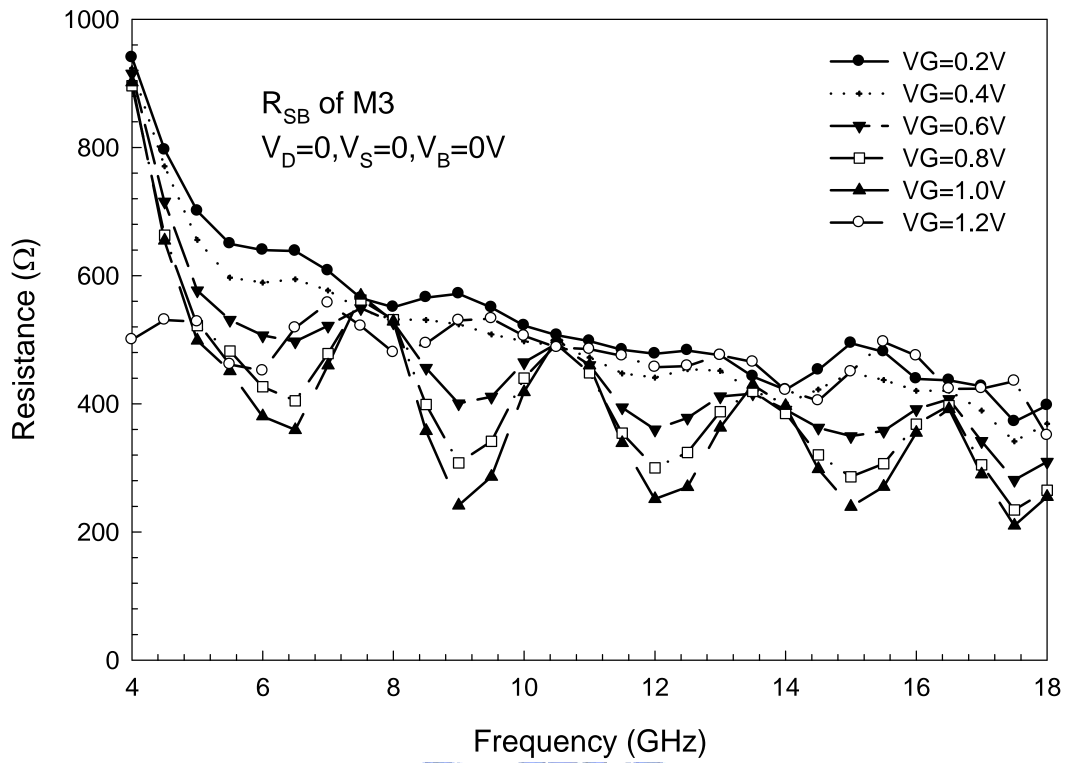




(a)



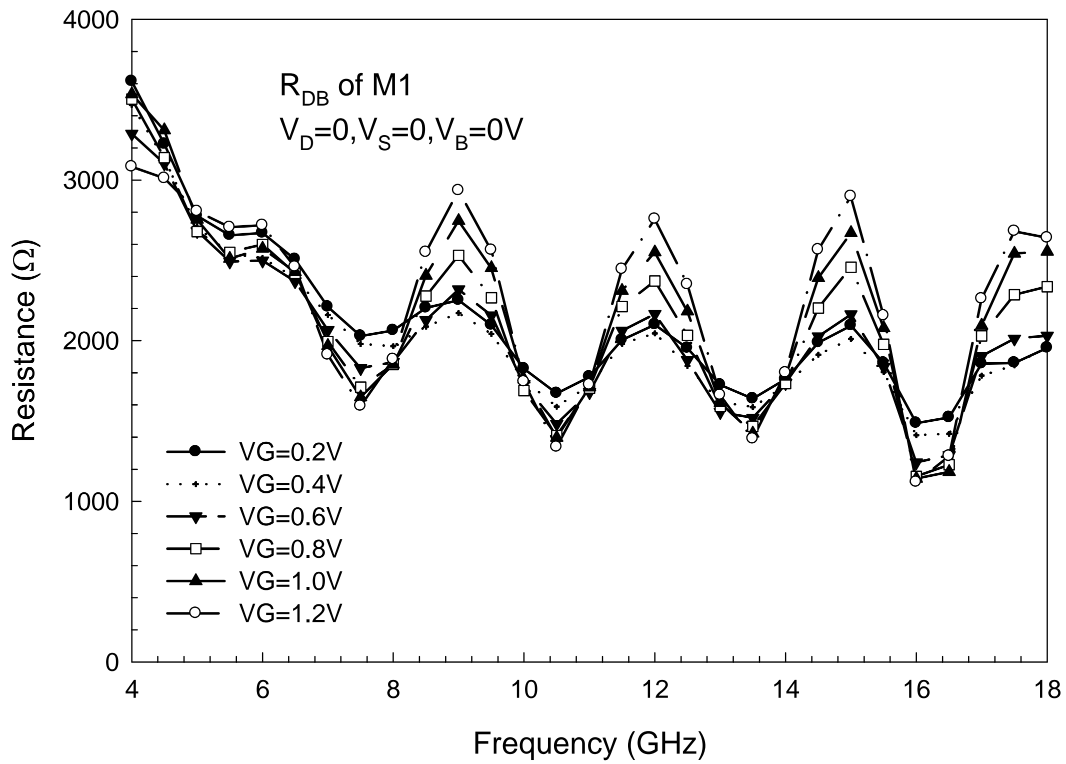
(b)



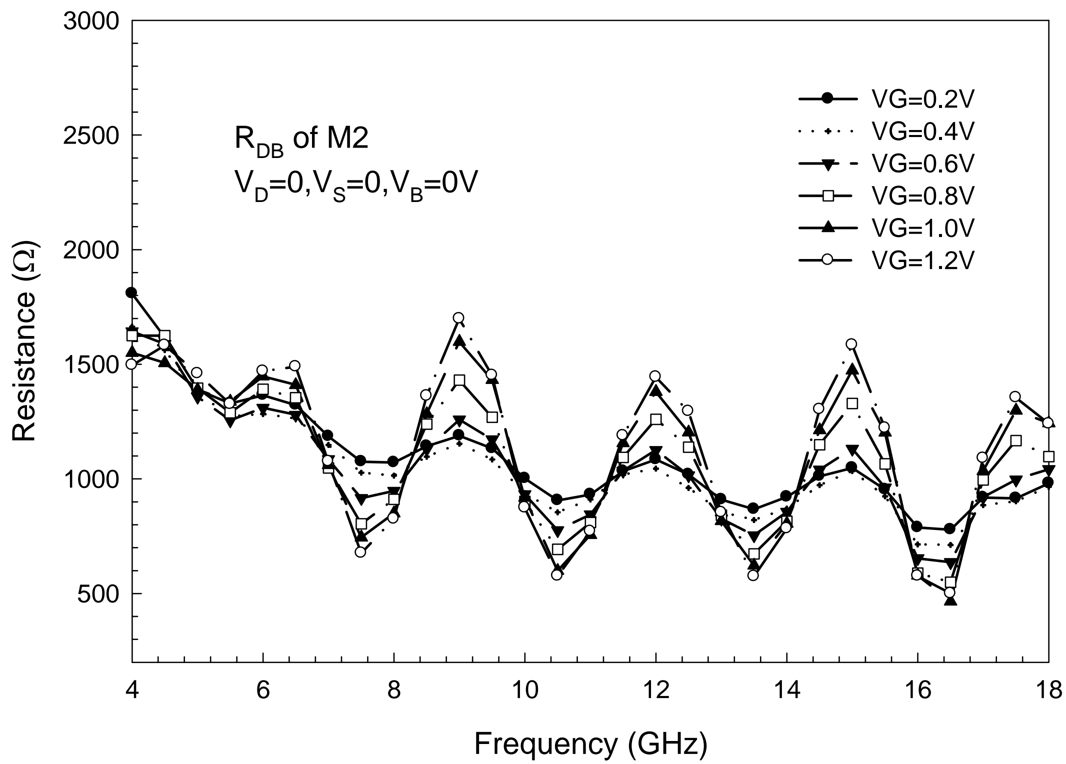
(c)

Fig.4.30 (a) The extracted R_{SB} of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted R_{SB} of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted R_{SB} of M3($12\mu m \times 4$) biased at different V_G.

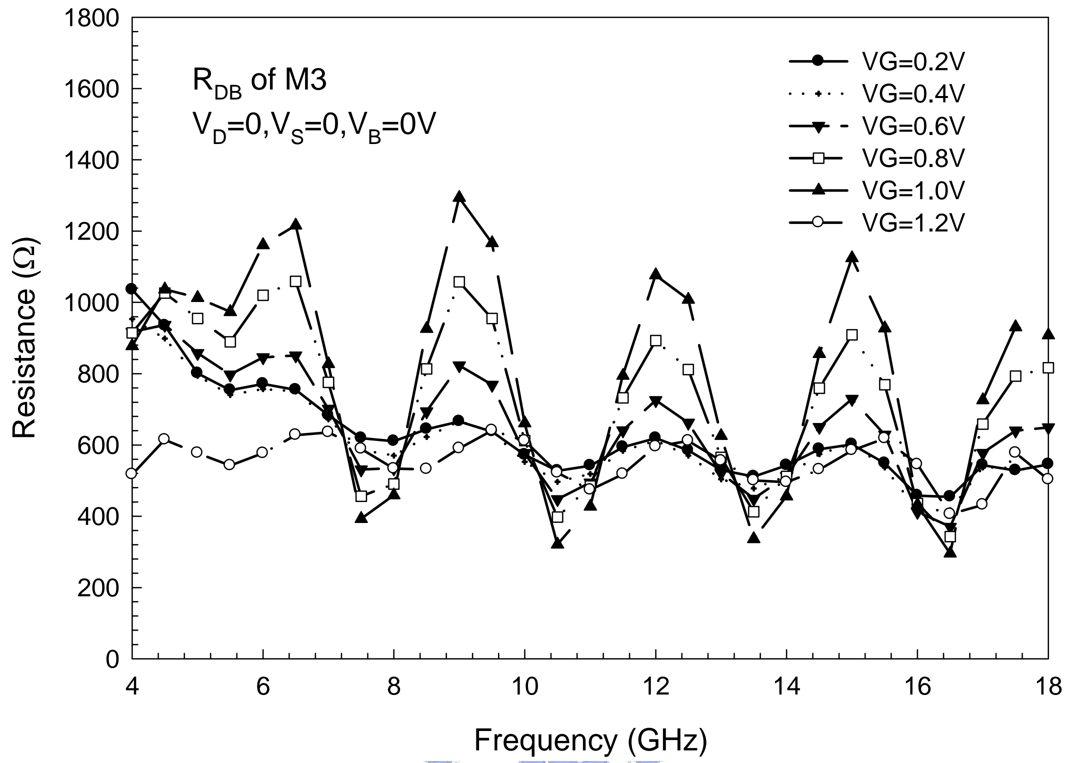
1896



(a)



(b)



(c)

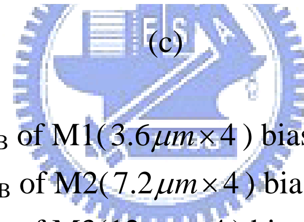
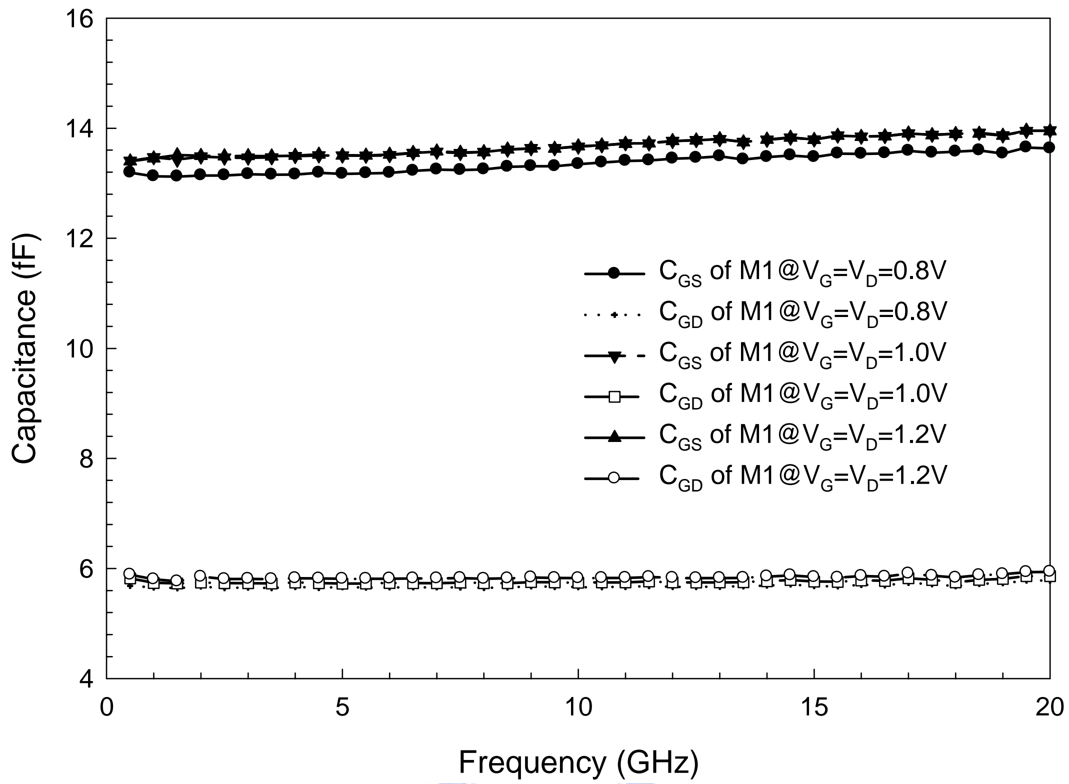
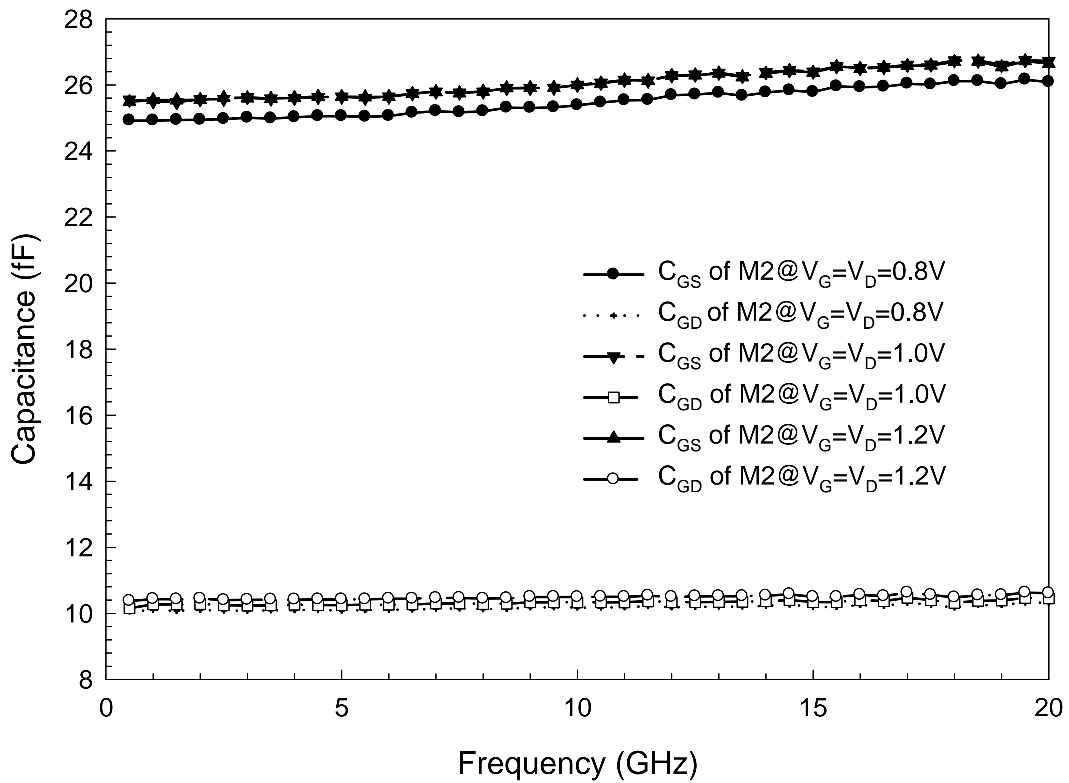


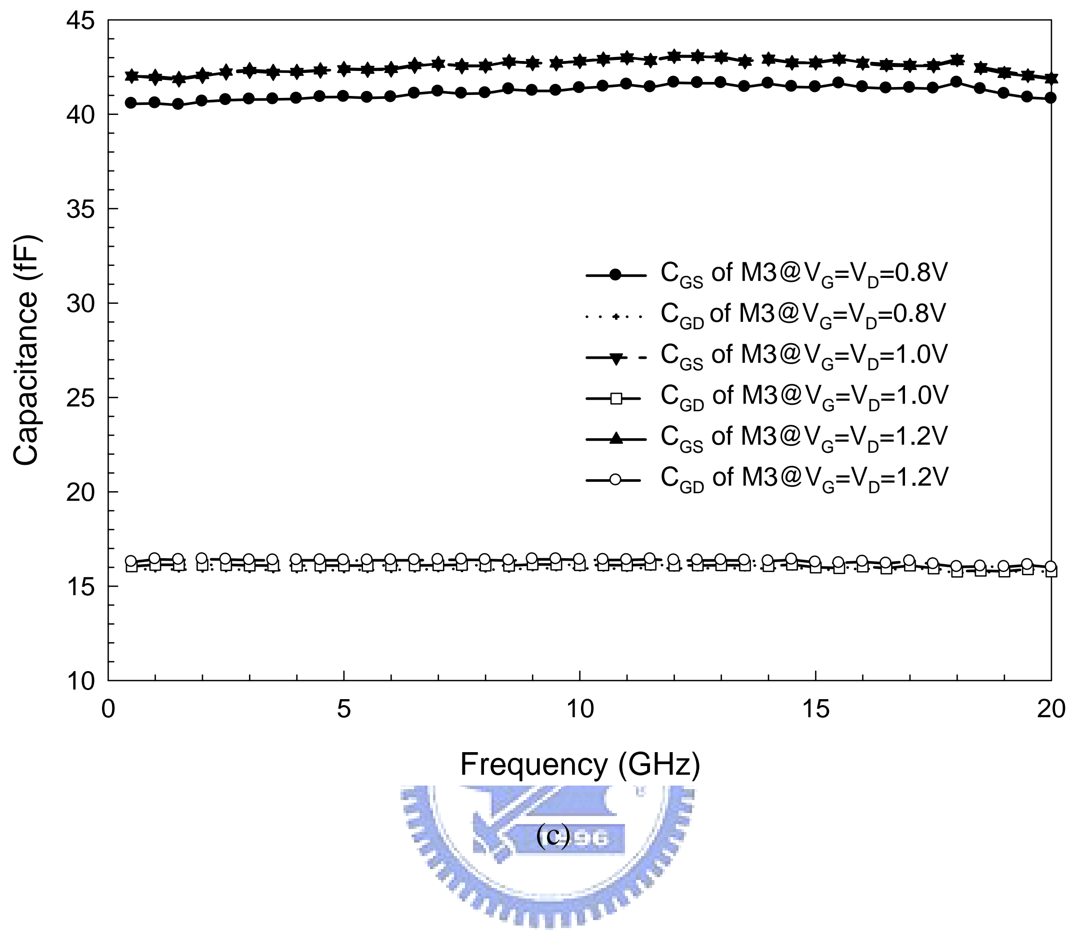
Fig.4.31 (a) The extracted R_{DB} of M1($3.6\mu m \times 4$) biased at different V_G.
(b) The extracted R_{DB} of M2($7.2\mu m \times 4$) biased at different V_G.
(c) The extracted R_{DB} of M3($12\mu m \times 4$) biased at different V_G.



(a)

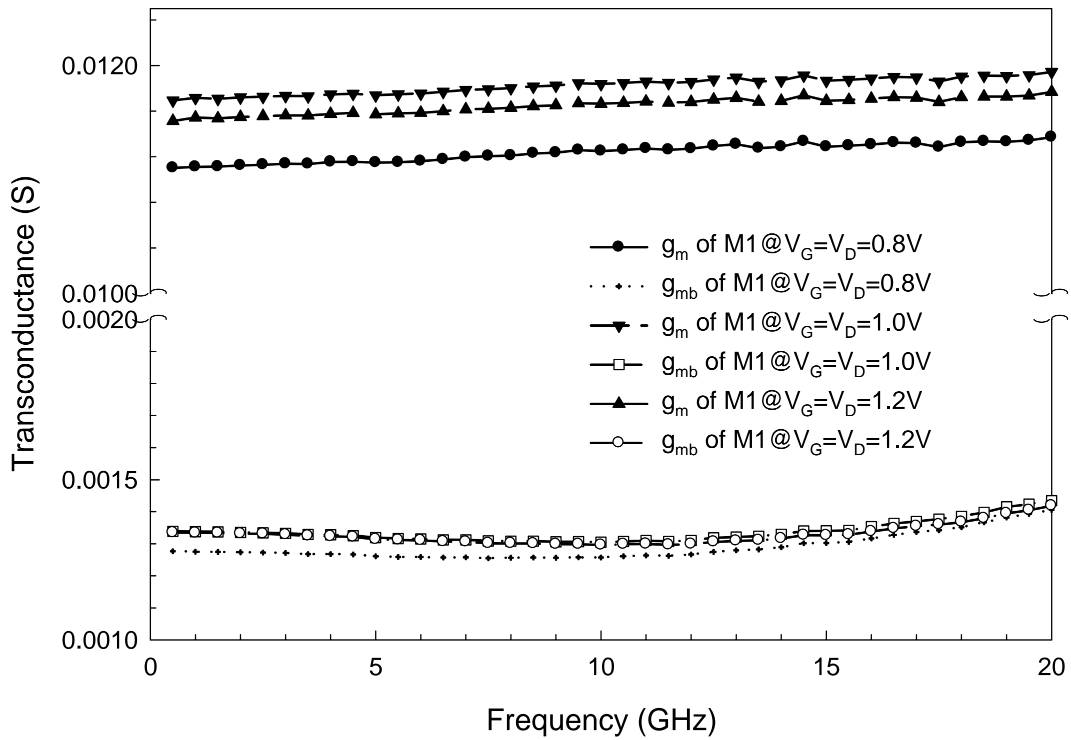


(b)

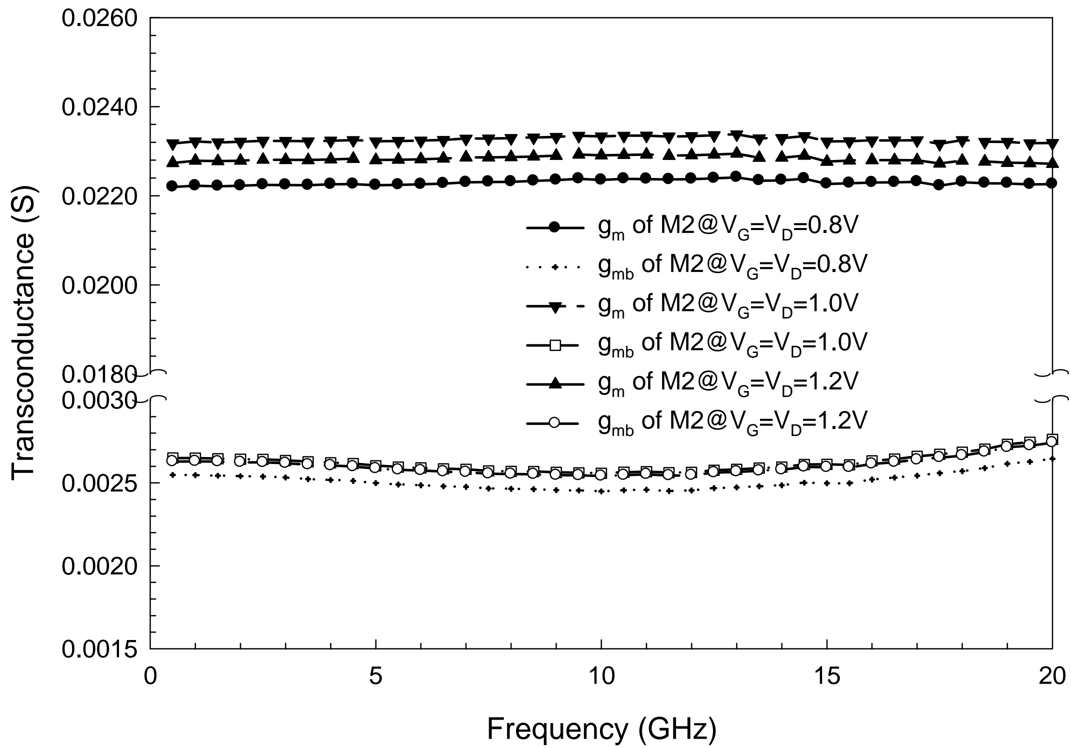


(c)

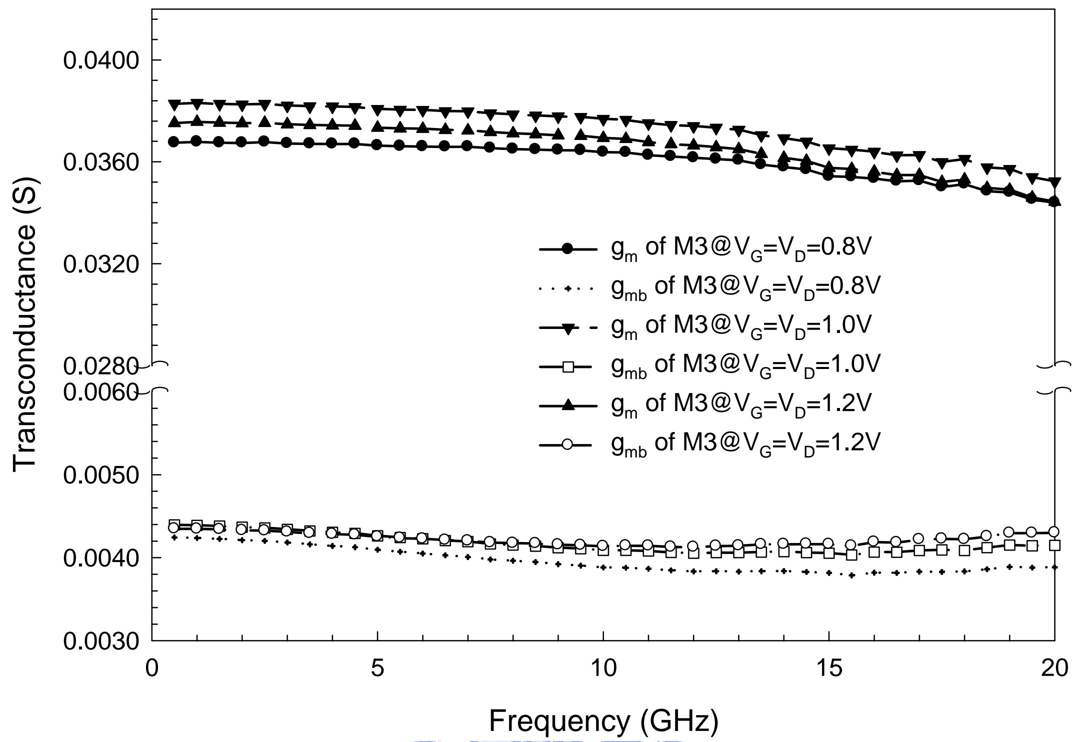
Fig.4.32 (a) The extracted C_{GS} and C_{GD} of saturation M1($3.6\mu m\times 4$).
(b) The extracted C_{GS} and C_{GD} of saturation M2($7.2\mu m\times 4$)..
(c) The extracted C_{GS} and C_{GD} of saturation M3($12\mu m\times 4$).



(a)



(b)



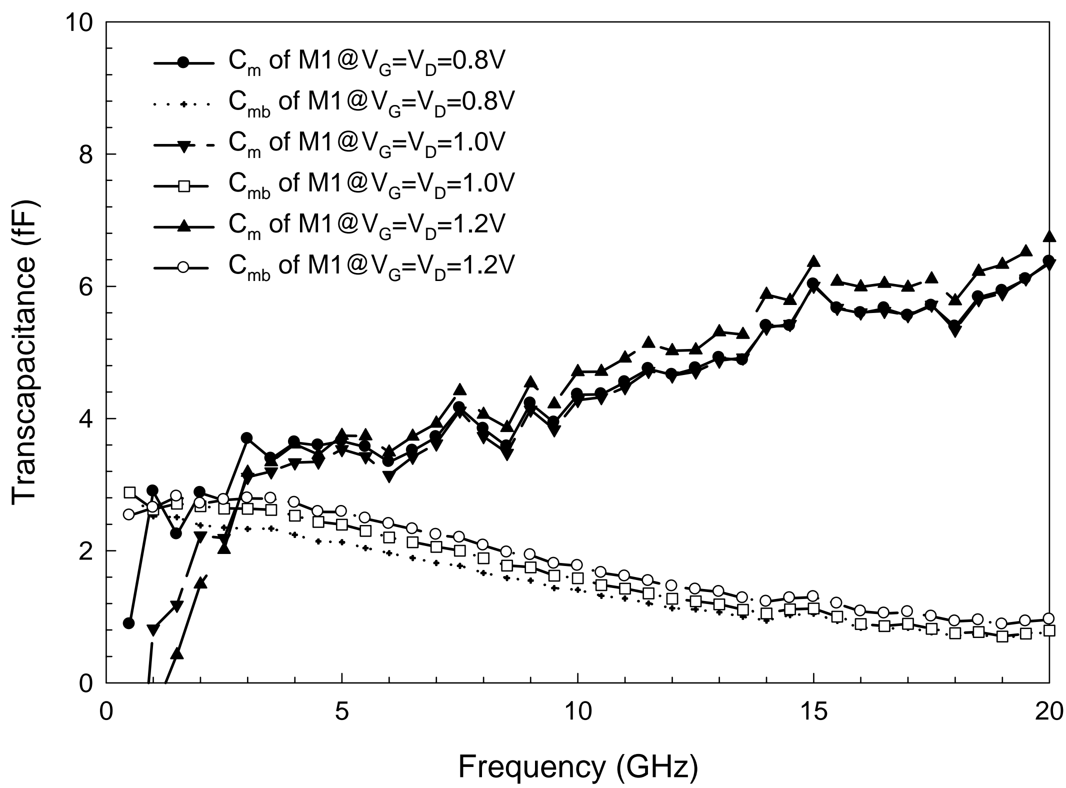
(c)

1896

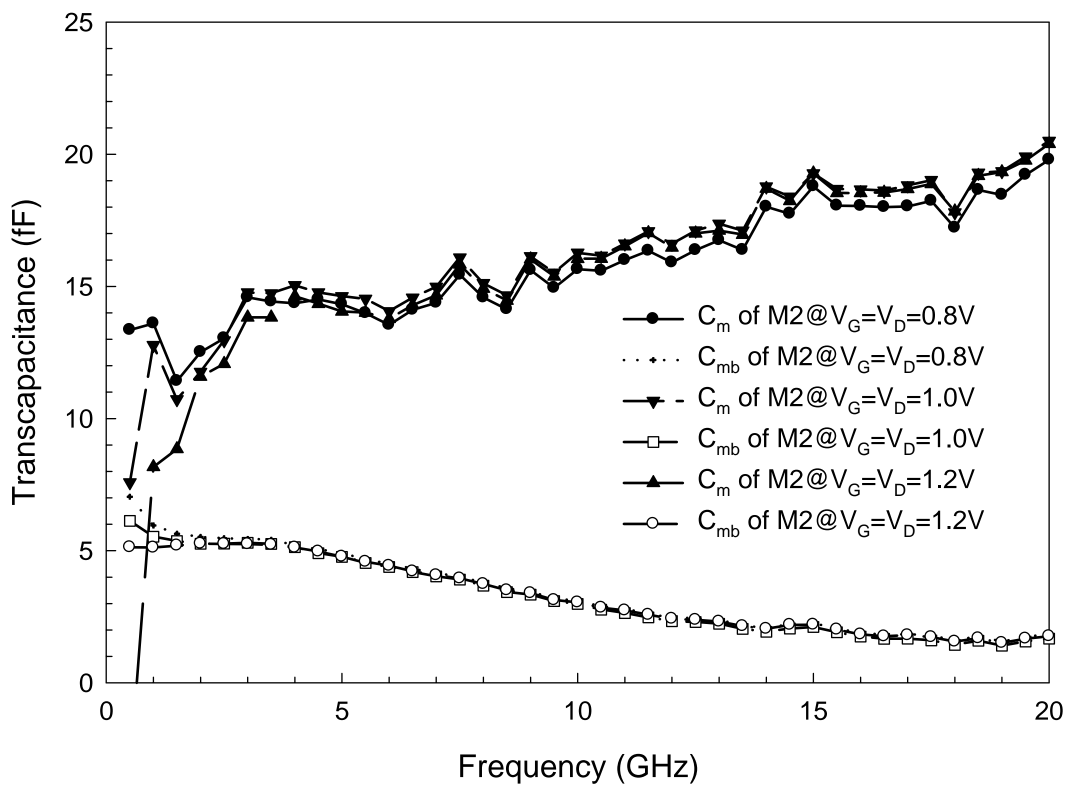
Fig.4.33 (a) The extracted g_m and g_{mb} of saturation M1($3.6\mu m \times 4$).

(b) The extracted g_m and g_{mb} of saturation M2($7.2\mu m \times 4$).

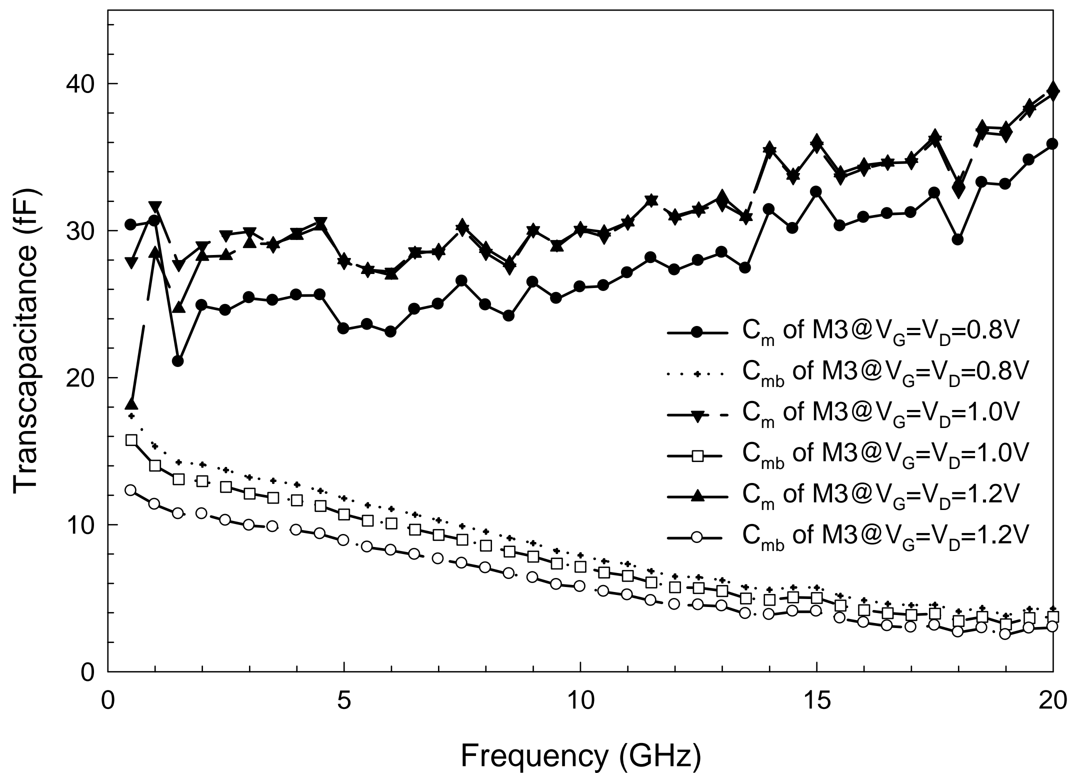
(c) The extracted g_m and g_{mb} of saturation M3($12\mu m \times 4$).



(a)

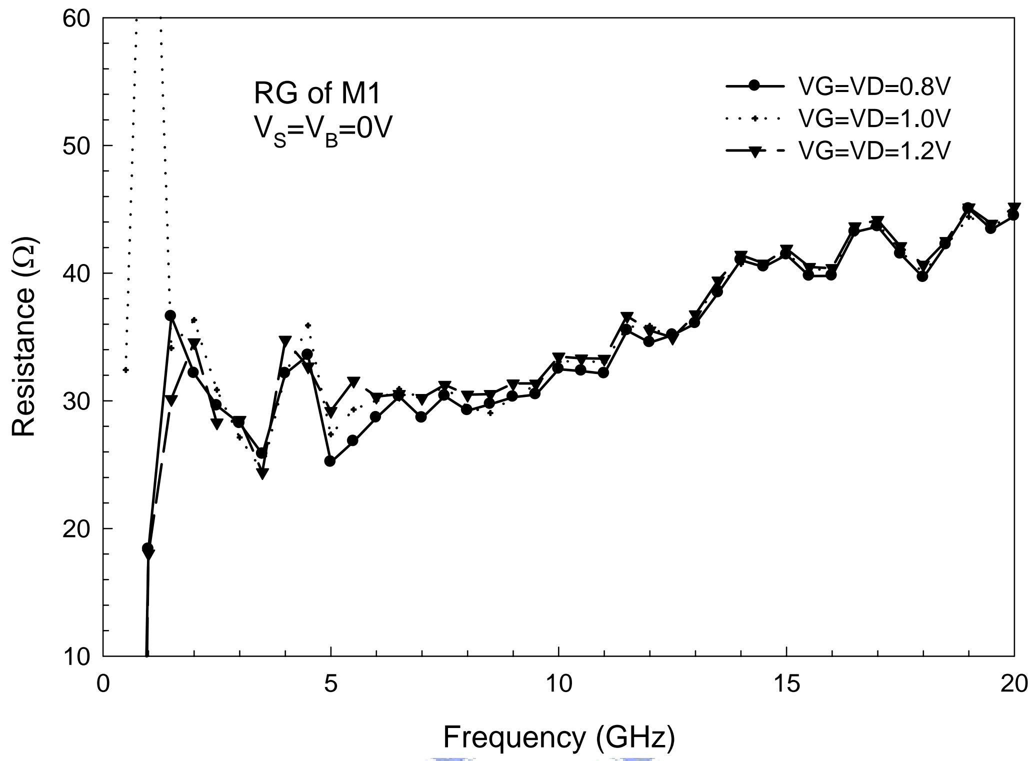


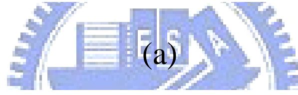
(b)



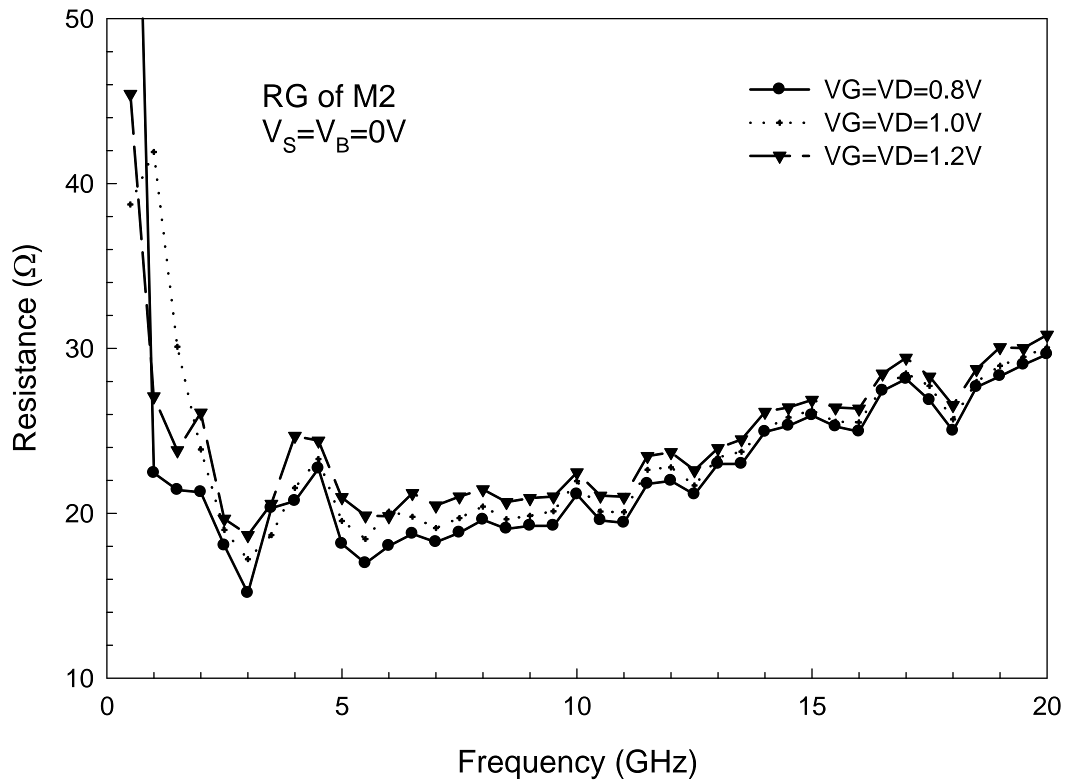
(C)

Fig.4.34 (a) The extracted C_m and C_{mb} of saturation M1($3.6\mu m \times 4$).
(b) The extracted C_m and C_{mb} of saturation M2($7.2\mu m \times 4$).
(c) The extracted C_m and C_{mb} of saturation M3($12\mu m \times 4$).

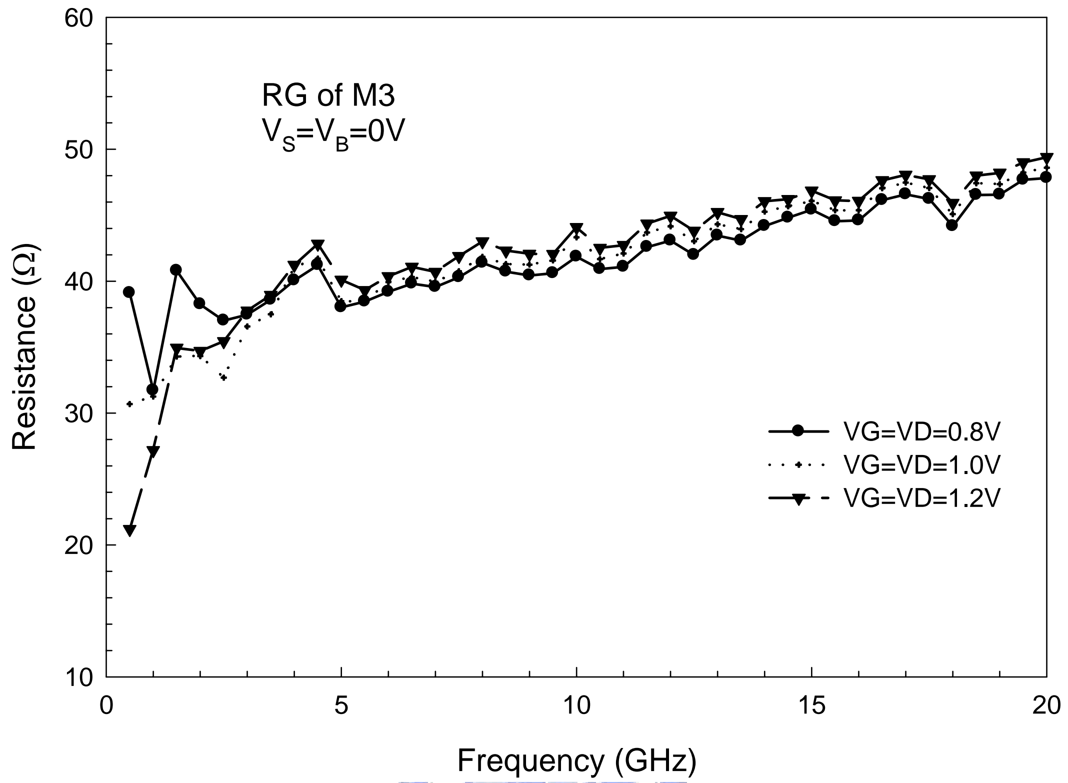




(a)

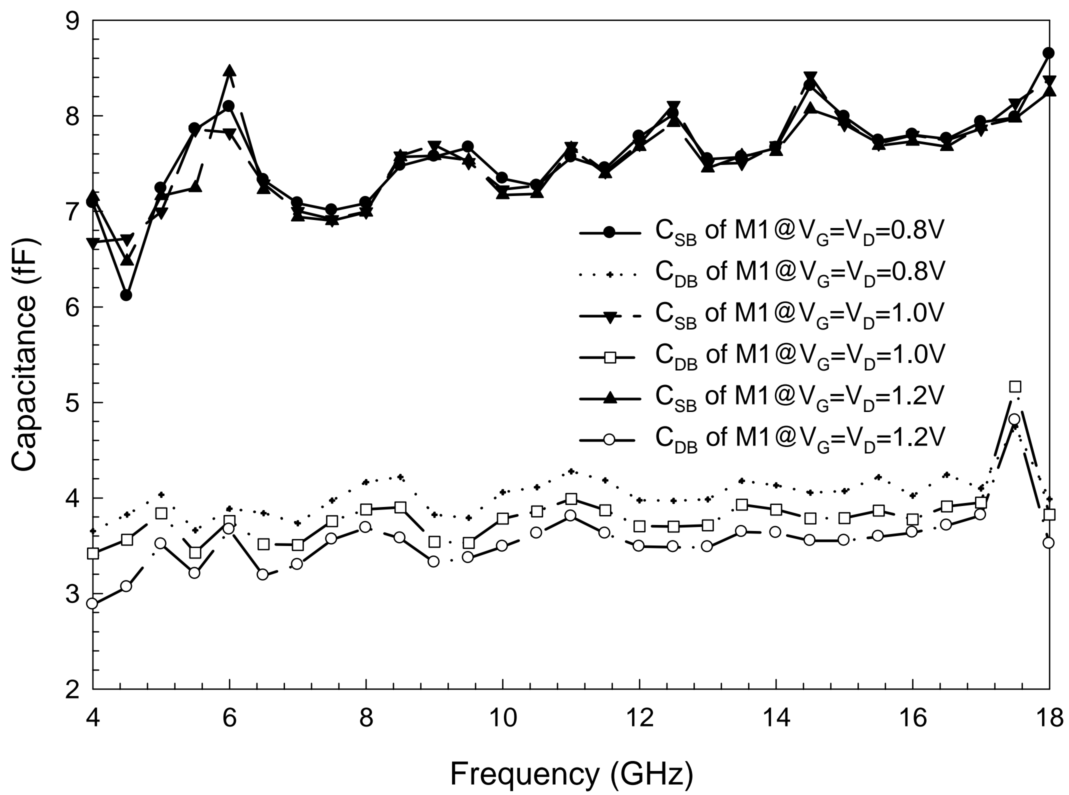


(b)

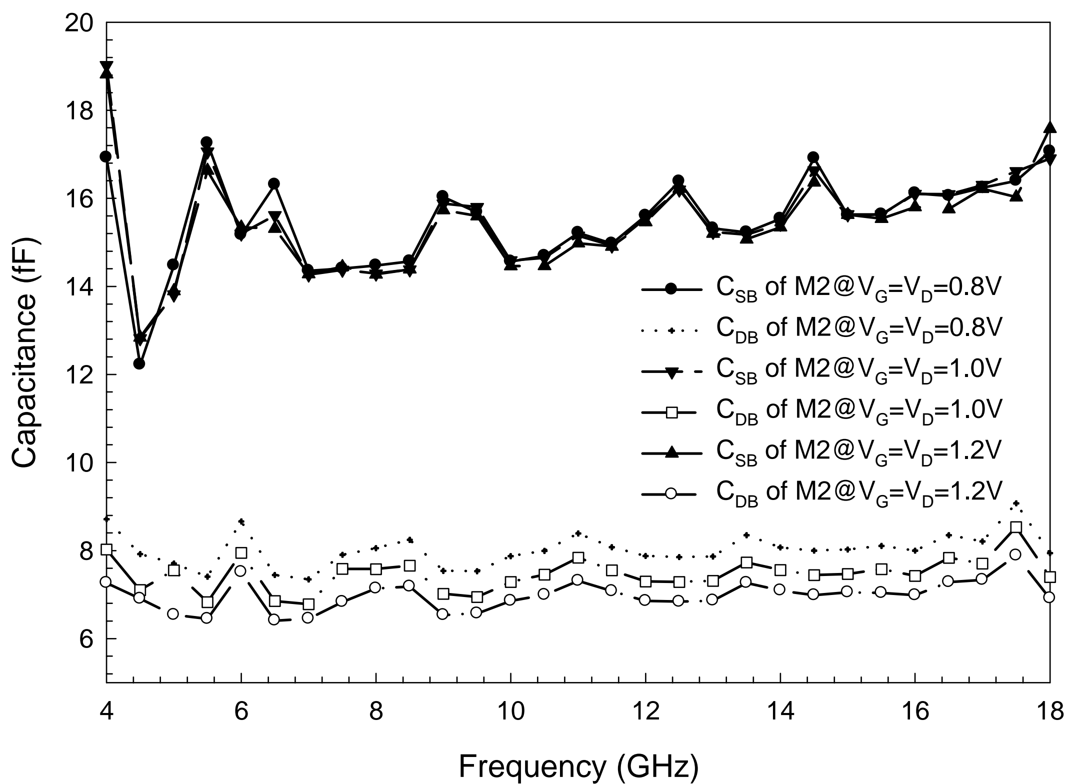


(c)

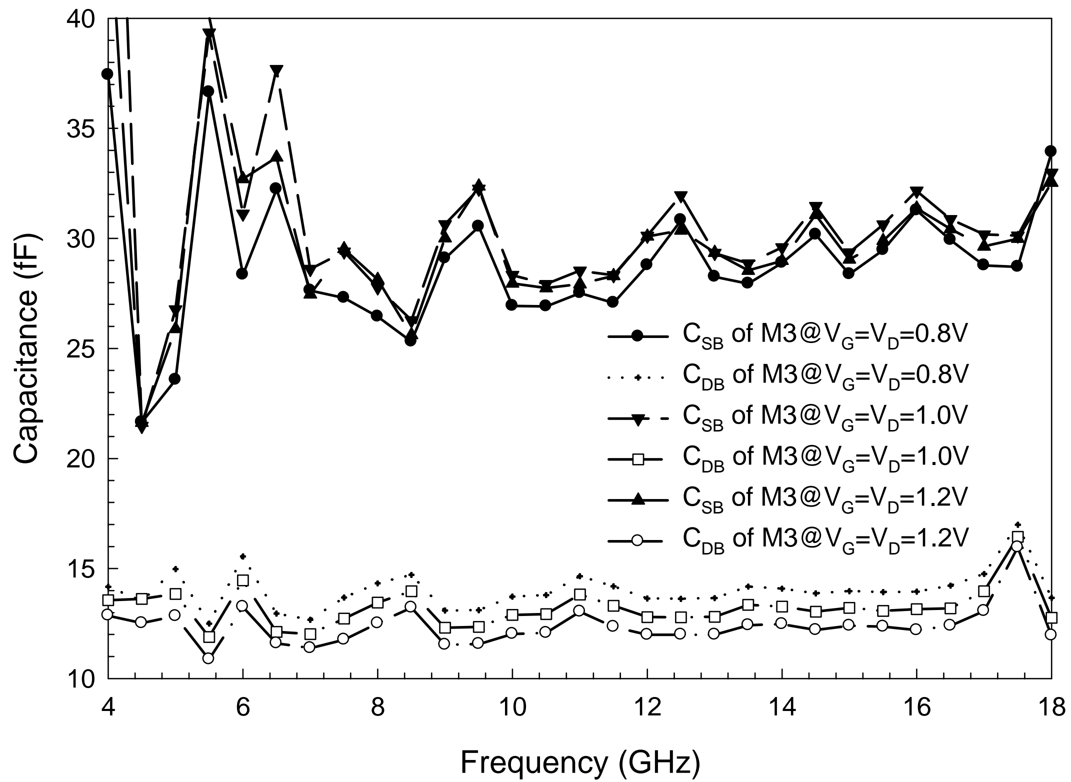
Fig.4.35 (a) The extracted R_G of saturation M1($3.6\mu m \times 4$).
(b) The extracted R_G of saturation M2($7.2\mu m \times 4$).
(c) The extracted R_G of saturation M3($12\mu m \times 4$).



(a)



(b)

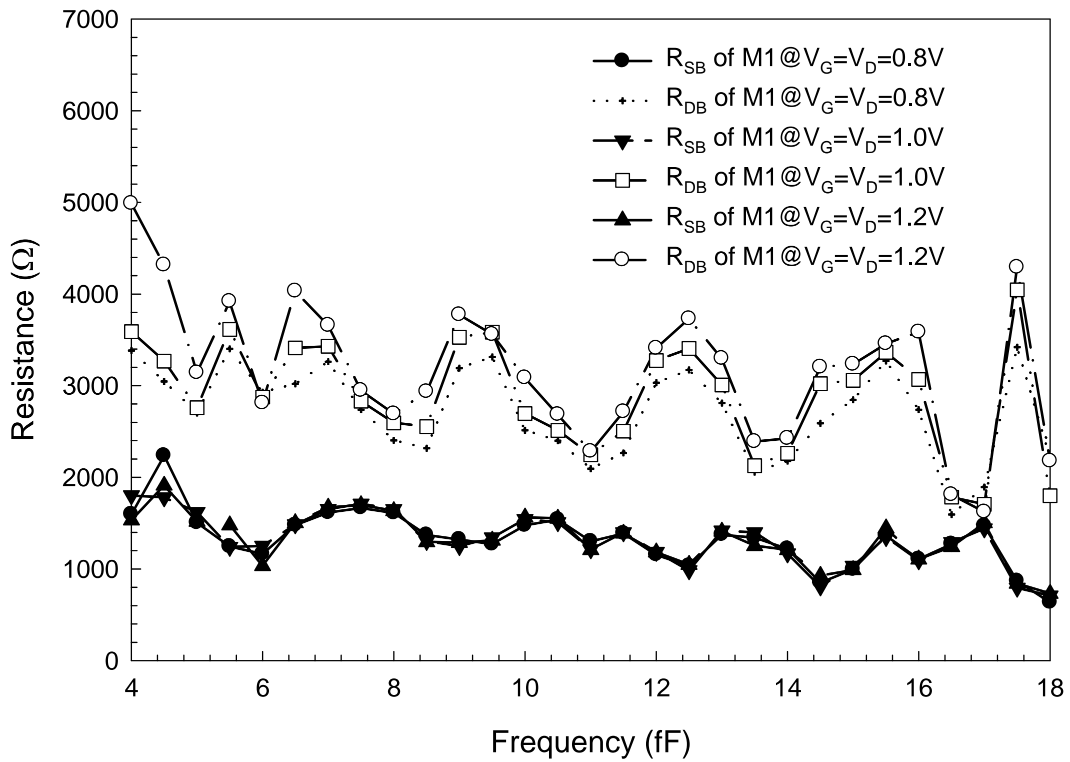


(c)

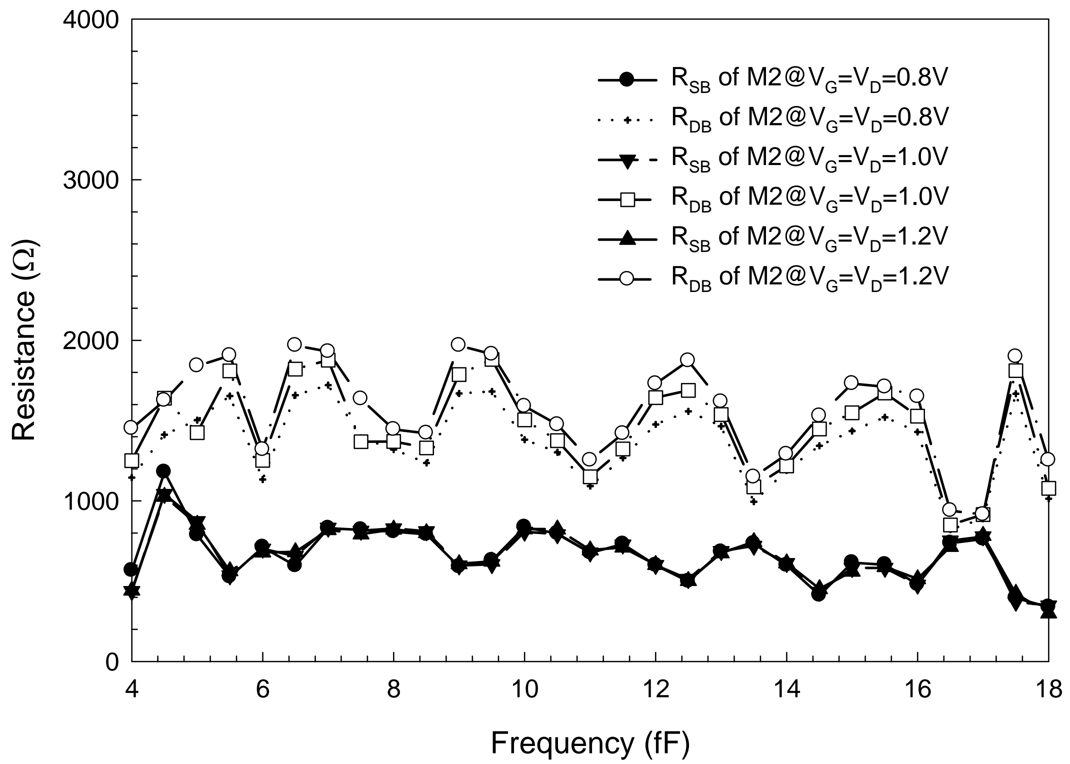
Fig.4.36 (a) The extracted C_{SB} and C_{DB} of saturation M1($3.6\mu m \times 4$).

(b) The extracted C_{SB} and C_{DB} of saturation M2($7.2\mu m \times 4$).

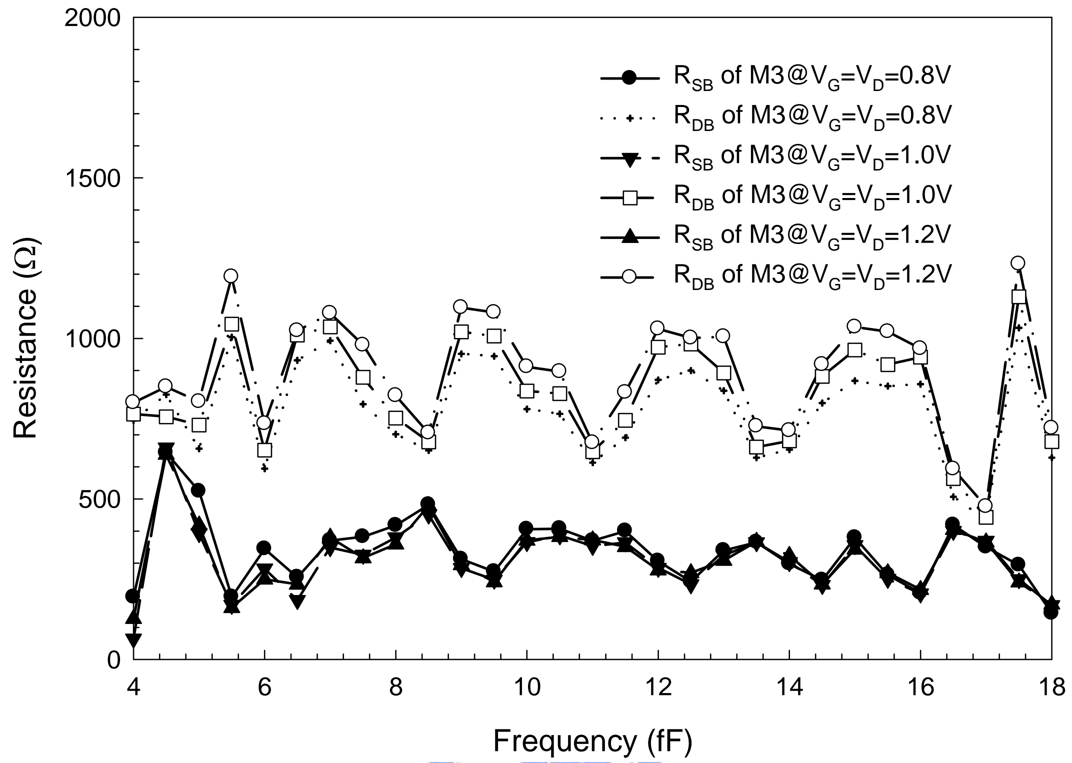
(c) The extracted C_{SB} and C_{DB} of saturation M3($12\mu m \times 4$).



(a)



(b)



(c)

Fig.4.37 (a) The extracted R_{SB} and R_{DB} of saturation M1($3.6\mu m \times 4$).
(b) The extracted R_{SB} and R_{DB} of saturation M2($7.2\mu m \times 4$).
(c) The extracted R_{SB} and R_{DB} of saturation M3($12\mu m \times 4$).

Chapter 5
Verification of Small-Signal Equivalent Circuit Model

5.1 Motivation

Modeling a RF MOSFET by a small-signal equivalent circuit is an exceptional way not only to design analog circuits but also help to well understand the high-frequency characteristics of the device. After the establishing of the equivalent circuit and the extraction of the model parameters, the small-signal equivalent circuit model has to be proven it's accurate and robust. One convenient way to verify the model is to compare the output characteristics of the model with the measurement data. In last chapter, the components in the proposed equivalent circuits for saturation RF MOSFET,s shown in Fig.4-2 have been extracted, it will be verified in this chapter.

5.2 Simulation of the Equivalent Circuits

To obtain the output characteristics of a circuit, one needs a simulator, which can input the circuit in text or graphic form includes the information such as nodes, resistors, inductors, capacitors, and dependent or independent current/voltage sources. The simulator will compute the electrical behavior of the circuit according to basic electrical laws. The most well-known circuit simulator is the SPICE program developed by university of California, Berkeley. In this study, commercial software named Advanced Design System (ADS) presented by Agilent Technologies is used for the simulation of the equivalent circuit. The equivalent circuit can be input to the simulator in the form of electrical circuit diagram by a graphical input interface, than the simulator can output the simulated results in form of network parameters such as Y-,

Z-, or S-parameters. The y-parameters were chosen for the output form since the components in the equivalent circuits are all extracted from the y-parameters of the devices.

Three set of the components for the equivalent circuits extracted from three devices with different dimensions are used. The bias condition is set at V_G=V_D=1.0V. The values of the components are shown in table 5.1a, 5.1b, and 5.1c. In these tables, the value of each component was selected approximately from the figures shown in previous chapter. Some extracted values have large deviation in figure, however, its found that these values are not sensitive to the simulation results. That is also the reason why their extracted values have certain deviation. Choosing an approximate value usually gives fair well simulation results. Some values were fine tuned in the range during the deviation of the extracted values to obtain better results. The simulation frequency range is from 100MHz to 20GHz.

5.3 Results and Discussions

The simulated and measured four-port y-parameters of each device are shown in real parts and imaginary parts individually from 100MHz to 20GHz. Figure 5.1a and 5.1b show the simulated and measured results of Y_{GG}. It can be observed the simulated imaginary parts of Y_{GG} agreed with the measured counterparts very well during the entire frequency range. The imaginary part of Y_{GG} is mainly determined by C_{GS}, C_{GD} and C_{GBE}. The results of real parts show slight difference between simulated and measured data in Fig. 5.1b. Since the amplitude of Re[Y_{GG}] are rather small, this deviations are still acceptable. The real part of Y_{GG} is a complex result determined by R_G, R_S, R_D, C_{GS}, C_{GD}, and C_{GBE}.

Figure 5.2a and 5.2b show the modeling results for Y_{DD} of the three devices. Y_{DD} is an important output admittance for a RF MOSFET, since MOSFET's are usually arranged in common source configuration. At lower frequency range, Y_{DD} is mainly determined by R_{CH},

R_S, and R_D. As frequencies increases, the amplitude of Y_{DD} will rise due to the output signal at drain terminal couples to the substrate via the reverse-biased drain/bulk junction. Therefore, at higher frequencies, the C_{DB}, C_{GS}, R_D, R_{CH}, R_S, R_{DB}, R_{SB}, and R_{DSB} all have contribution to Y_{DD}.

The measured and simulated input admittances of the source terminals of the three devices are shown in Fig.5.3a and 5.3b. The imaginary part of Y_{SS} will be influenced by R_G, C_{GS}, C_{SB}, g_m, g_{mb} and transcapcitance C_m, C_{mb}, C_{mx}. However, the C_{mx} has not been extracted from the measurement data, since the difference between C_{GB} and C_{BG} are very small and irregular. It's hardly to tell the C_{mx} from the measurement error. It's also found that the input admittance at source become more inductive as the device dimension increases, which is believed due to the larger R_G, C_m, and C_{mb} of the larger device. The real part of the Y_{SS} is dominated by g_m and g_{mb} of the device.

Figure 5.4a shows distinguish difference between the simulated and measured Im[Y_{BB}], this probably caused by the over de-embedding of the parasitics of the substrate pad. The shunt capacitance between substrate pad and ground is over de-embedded. However, the input admittance at the body terminal is the last thing one would care, since the body terminal of a MOSFET is always ac grounded.

Figure 5.5a shows the measured and simulated Im[Y_{GD}]'s, which are mainly caused by the C_{GDO} of these devices. The Im[Y_{GD}] is primarily determined by C_{GDO}. Figure 5.5b shows the modeling results of Re[Y_{GD}], which are mainly determined by C_{GDO}, R_G, and R_D.

The Y_{GS} of the three devices, which mainly caused by C_{GS} and series R_G, R_S are shown in Fig.5.6a and 5.6b. They are obviously modeled well.

Figure 5.7a and 5.7b show the Y_{GB} of the three devices. The amplitudes of Y_{GB} including imaginary and real part are very close to the Y_{BG}'s show in Fig. 5.8a and 5.8b, except for the case of M3. The Y_{BG} of M3 under V_G=V_D=1V bias condition exhibit irregular behavior, however, its amplitude is very small and has no effect on the entire device behavior.

Figure 5.9a and 5.9b show the measured and simulated Y_{BD}'s of the devices. The modeling results are also fair well. Y_{BD} is mainly caused by C_{DB} and R_{DB}. It is also the main contributor to the output admittance of drain terminal at high frequency range.

Figure 5.10a and 5.10b demonstrate the simulation results of the Y_{BS}'s, which are mainly caused by C_{SB} and R_{SB}. Y_{BS} can be used as an evaluation for the accuracy of extracted C_{SB} and R_{SB}. Poor extracted values of C_{SB} and R_{SB} will worse the modeling of entire substrate network, since the intrinsic body terminal is located between the C_{SB} and R_{SB}.

The simulated and measured Y_{DG}'s are shown in Fig. 5.11a and 5.11b. The imaginary part of Y_{DG} is caused by R_G, C_{GS}, C_{GD}, g_m, and C_m, and represents the signal delay from gate to drain terminal. The real part of Y_{DG} is very close to, however, slight smaller than the transconductance, g_m.

Figure 5.12a and 5.12b illustrate the modeling results of Y_{DB}'s, which are the main parameter to evaluate the substrate transconductance g_{mb}. The imaginary part of Y_{DB} is similar the imaginary part of Y_{DG} that it also influence by transcapacitance. During the simulation process, it is found that the Im[Y_{DG}] will be influenced by C_{SB}, R_{SB}, g_m, g_{mb} and C_{mb}, the simulation results will be exact only if these components are extracted correctly. The Re[Y_{DB}] is close related to g_{mb}. In fact, the Re[Y_{DB}] at very low frequency range is equal to g_{mb}, since at lower frequency, v_{BS} will approach to v_{BSi}. As frequency increases, the v_{BSi} will decrease due to the decreasing of the impedance of C_{SB}. Therefore the Re[Y_{DB}] decreases as frequency increases. Similarly, the Re[Y_{DB}] will be modeled well only if the values of g_{mb}, C_{SB}, and R_{SB} are extracted exactly.

Figure 5.13a and 5.13b show the modeling results of Y_{DS}'s. Y_{DS} corresponds to the trans-admittance of a two-port common gate device. It is observed that the Im[Y_{DS}] shows inductive property, as had mentioned, it is contributed by the transcapacitance C_m and C_{mb}. The Re[Y_{DS}] is dominated by g_m and g_{mb}.

The imaginary part of Y_{SG} is shown in Fig. 5.14a. An "inductive" component is also observed

in spite of C_{GS} exists between gate and source. This inductive component is induced by R_G, C_{GS}, and g_m, it is also a contributor to the inductive input impedance at source terminal. The Re[Y_{SG}] is also dominated by g_m of the device and approximately equals to the amplitude of Re[Y_{DG}].

Figure 5.15a shows the imaginary part of Y_{SB}, in which a "bending" is observed. Similar with the effect of R_G, C_{GS}, g_m act on Y_{SG}, the R_{SB}, C_{SB}, g_{mb} make Y_{SB} "inductive". However, the value of g_{mb} is much smaller than g_m, and the v_{BSi} decreases as frequency decreases. The "inductive" components produced by g_{mb} will decrease to a level, which will less than the original capacitance value of C_{SB}. Therefore, the Y_{SB} "bends" beneath the x-axis.

Figure 5.16a and 5.16b show the measured and simulated Y_{SD}'s of the devices. The Y_{SD} is another contributor to the output admittance at drain, which is mainly cause by the channel resistance $1/g_{DS}$.

5.4 Summary

The simulated y-parameters of the equivalent circuit for saturation devices are demonstrated and compared with the measurement data of the devices. Most of the measured and simulated y-parameters are agreed with each other. Phenomena arisen from each component in the equivalent circuit of an active RF MOSFET are observed and analyzed. The RF small-signal behaviors of the four-terminal RF MOSFET are modeled pretty well.

M1: VG=1V, VD=1V								
g_m(mS)	C_m(fF)	g_{mb}(mS)	C_{mb}(fF)	g_{ds}(S)	R_S(Ω)	R_D(Ω)	R_G(Ω)	C_{GS}(fF)
11.8	4.4	1.33	2	1/840	6.9	6.9	35	13.5
C_{GD}(fF)	C_{SB}(fF)	C_{SBE}(fF)	R_{SB}(Ω)	C_{DB}(fF)	C_{DBE}(fF)	R_{DB}(Ω)	C_{GBE}(fF)	R_{DSB}(Ω)
5.8	7.2	3	1500	3.5	1.5	3000	0.6	1300

(a)

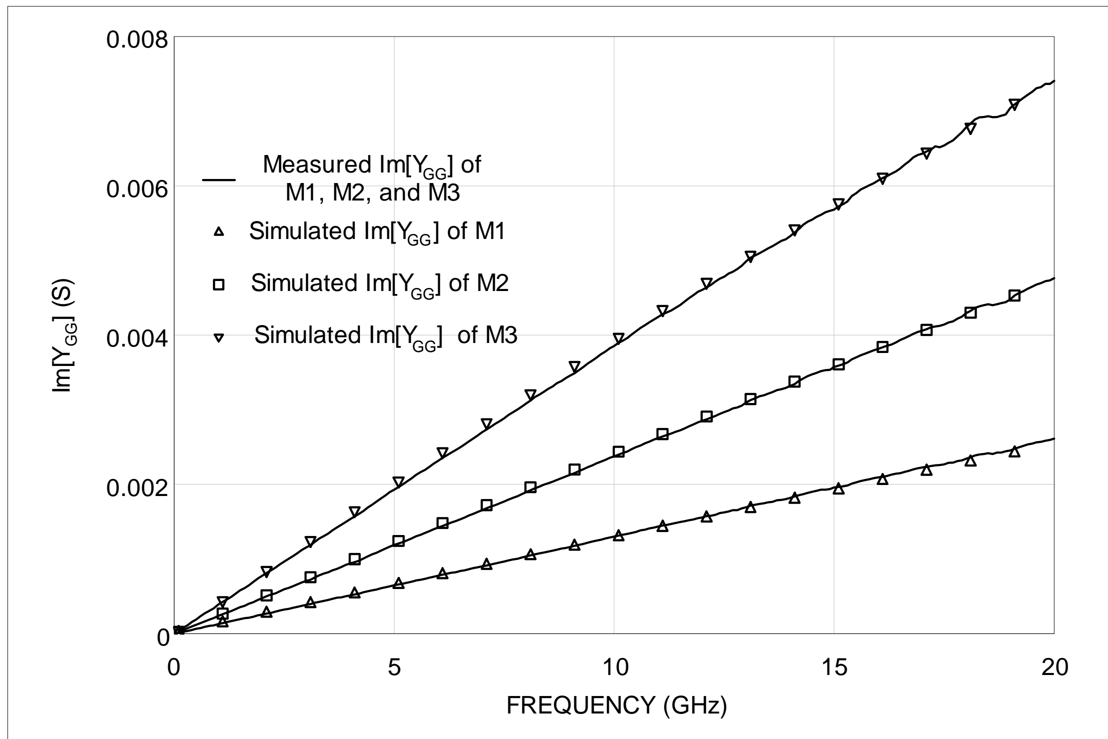
M2: VG=1V, VD=1V								
g_m(mS)	C_m(fF)	g_{mb}(mS)	C_{mb}(fF)	g_{ds}(S)	R_S(Ω)	R_D(Ω)	R_G(Ω)	C_{GS}(fF)
23.3	14	2.64	4	1/423	3.6	3.6	23	25.6
C_{GD}(fF)	C_{SB}(fF)	C_{SBE}(fF)	R_{SB}(Ω)	C_{DB}(fF)	C_{DBE}(fF)	R_{DB}(Ω)	C_{GBE}(fF)	R_{DSB}(Ω)
10.2	14.5	4.5	800	7.2	2	1500	0.9	700

(b)

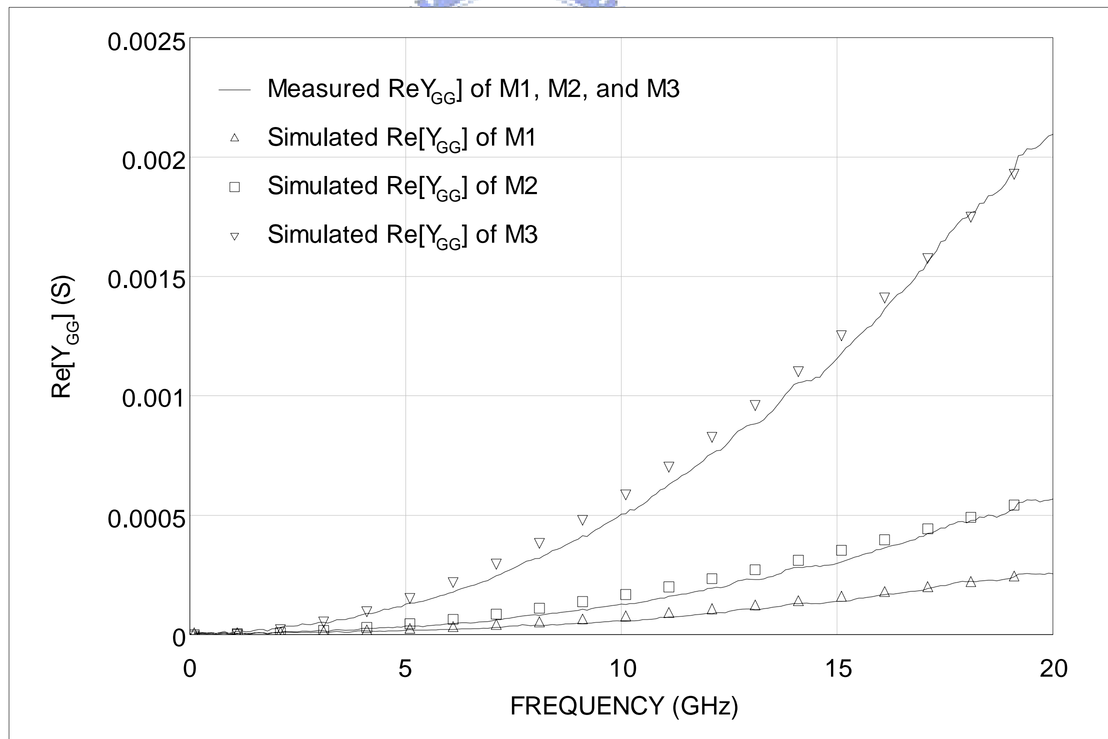
M3: VG=1V, VD=1V								
g_m(mS)	C_m(fF)	g_{mb}(mS)	C_{mb}(fF)	g_{ds}(S)	R_S(Ω)	R_D(Ω)	R_G(Ω)	C_{GS}(fF)
38.3	27	4.15	5	1/242	2.5	2.5	40	42.5
C_{GD}(fF)	C_{SB}(fF)	C_{SBE}(fF)	R_{SB}(Ω)	C_{DB}(fF)	C_{DBE}(fF)	R_{DB}(Ω)	C_{GBE}(fF)	R_{DSB}(Ω)
16	30	6	400	13	2.5	800	1	400

(c)

Table 5.1 (a) The extracted values of the components for the small-signal equivalent circuit model of M1 devices ($3.6\mu m \times 4$).
(b) The extracted values of the components for the small-signal equivalent circuit model of M2 devices ($7.2\mu m \times 4$).
(c) The extracted values of the components for the small-signal equivalent circuit model of M3 devices ($12\mu m \times 4$).

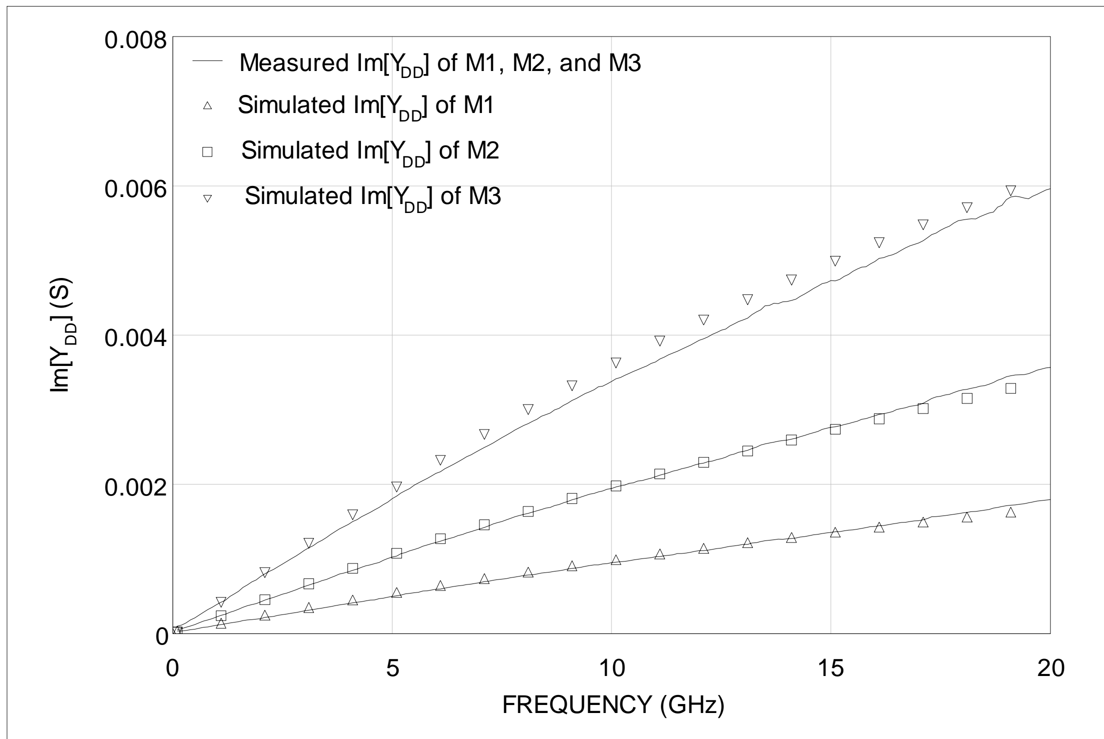


(a)

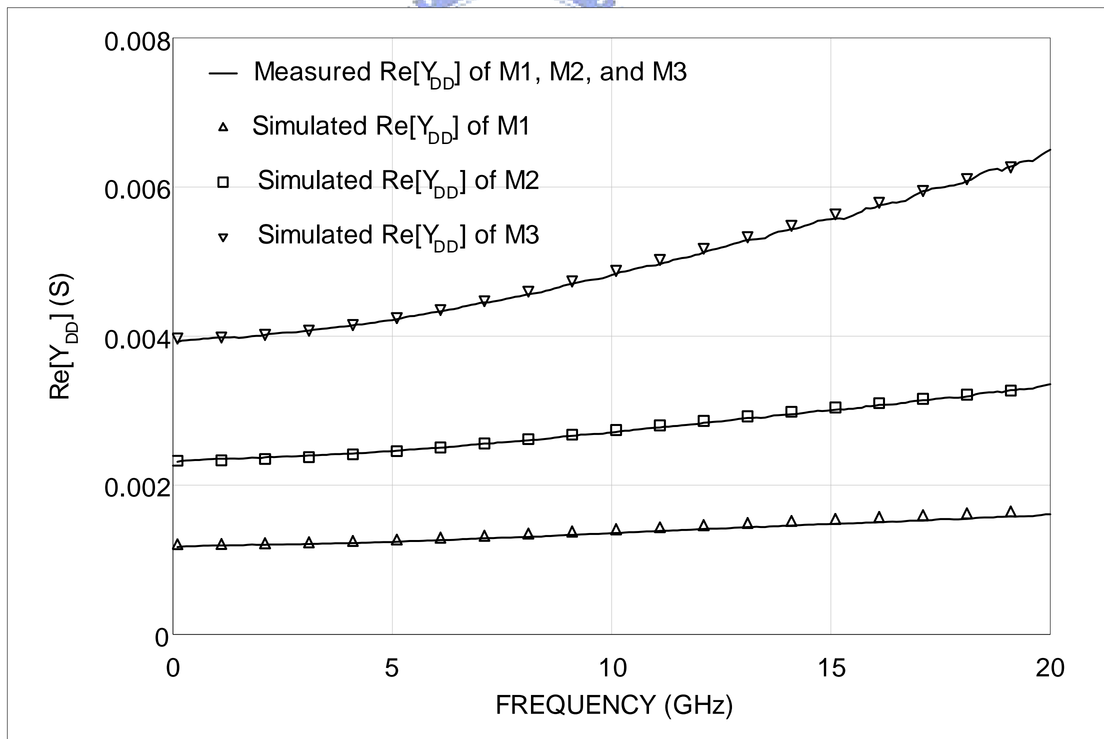


(b)

Fig.5.1 (a) Measured and simulated Im[Y_{GG}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re[Y_{GG}] of M1, M2, and M3 biased VG=VD=1V.

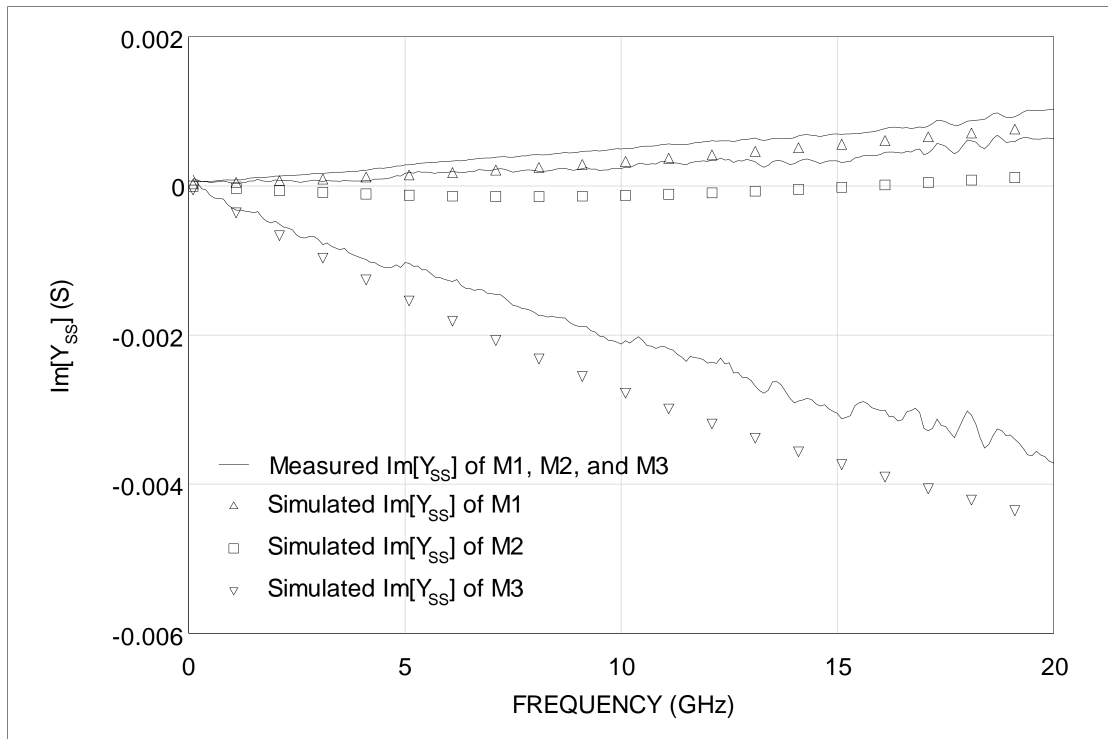


(a)

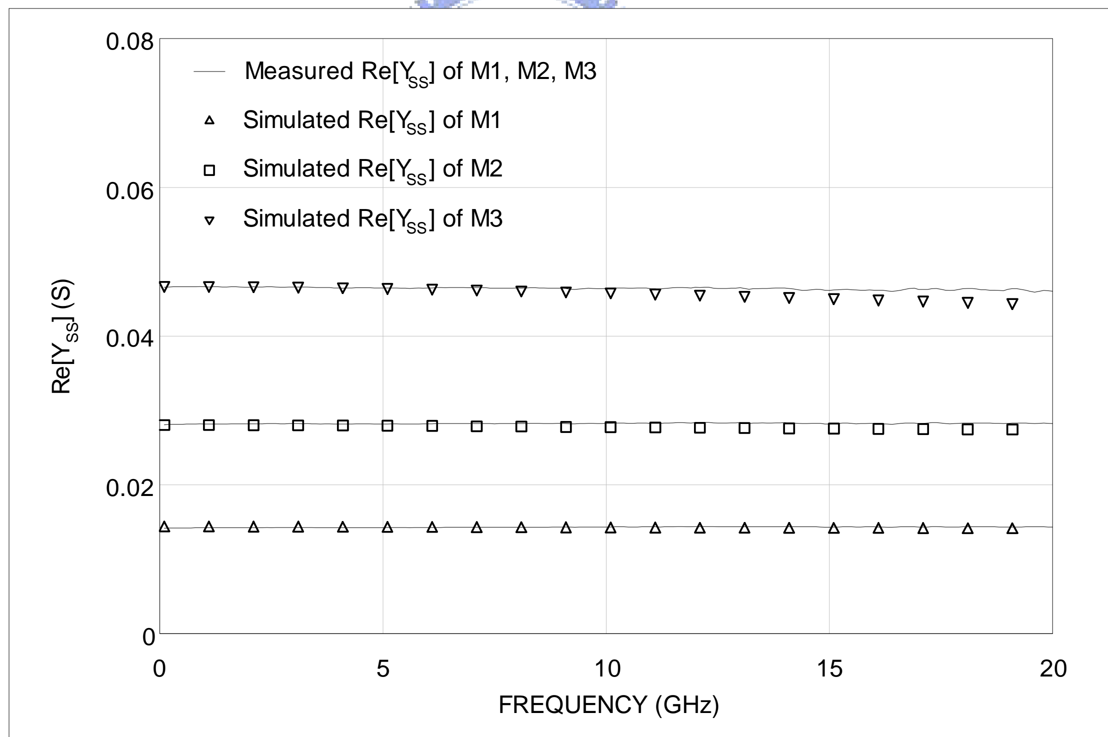


(b)

Fig.5.2 (a) Measured and simulated Im[Y_{DD}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{DD}] of M1, M2, and M3 biased VG=VD=1V.

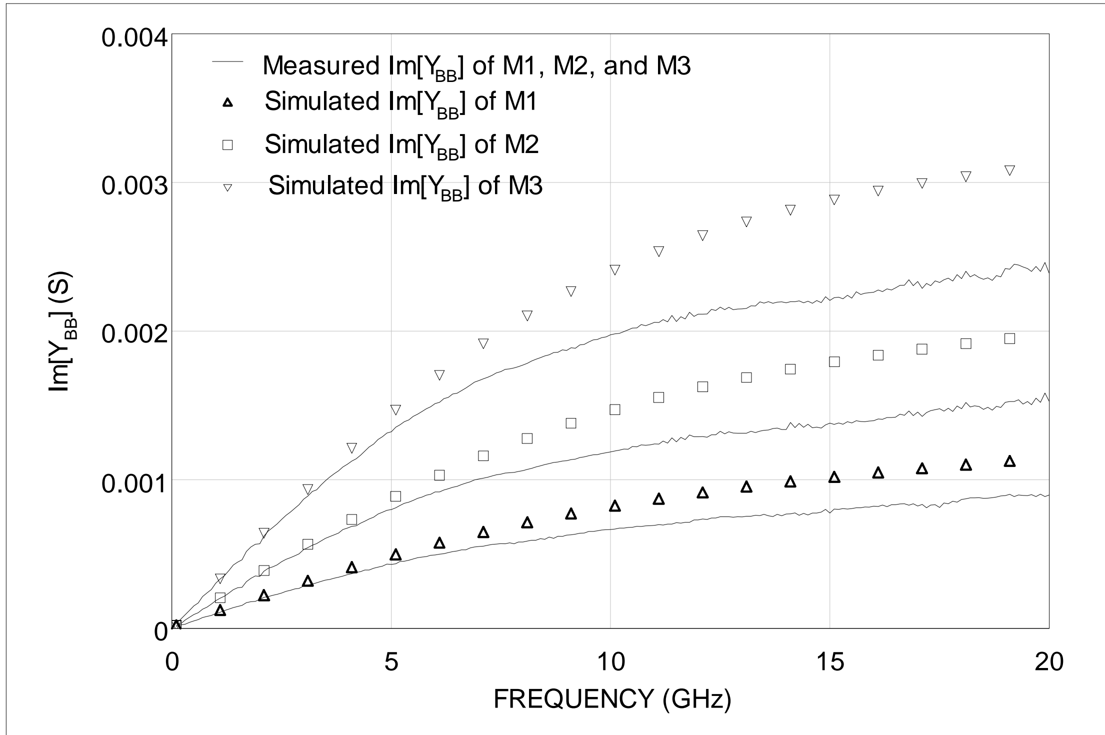


(a)

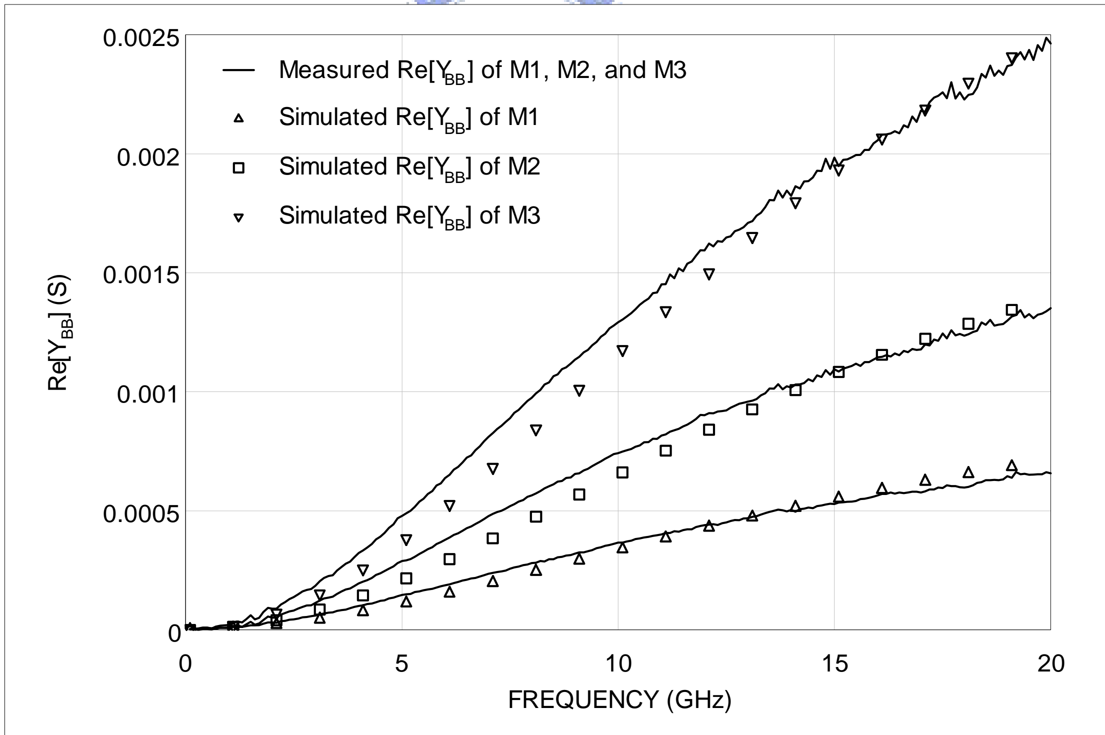


(b)

Fig.5.3 (a) Measured and simulated $Im[Y_{SS}]$ of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated $Re[Y_{SS}]$ of M1, M2, and M3 biased VG=VD=1V.

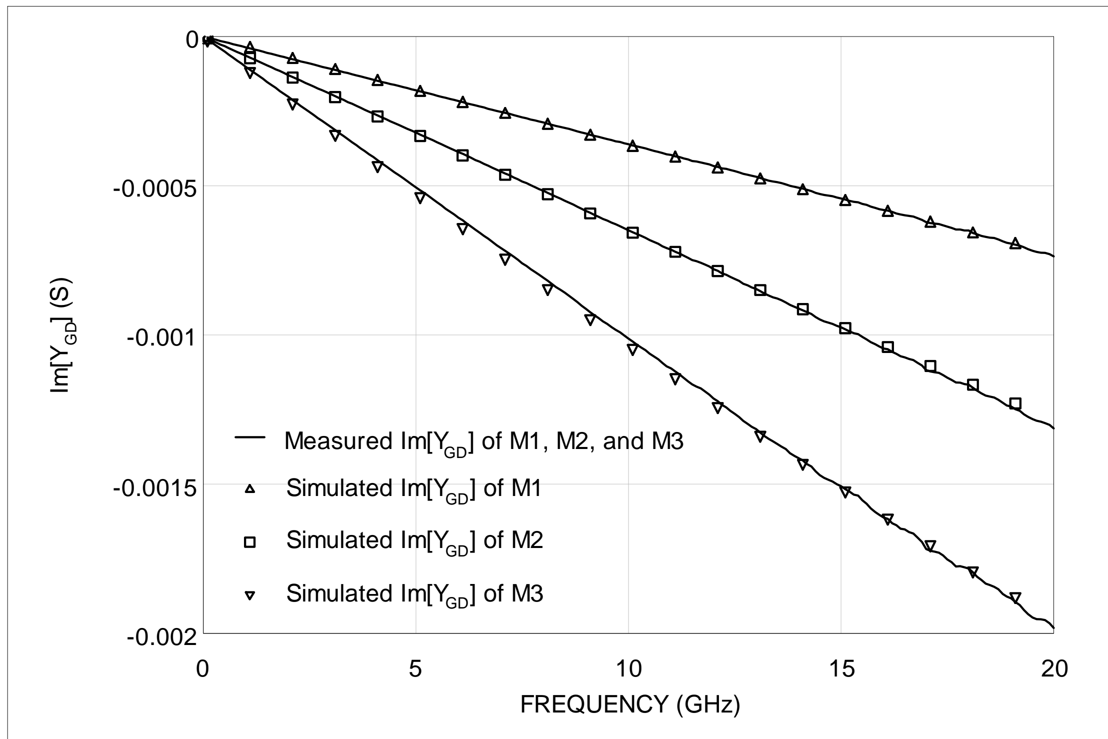


(a)

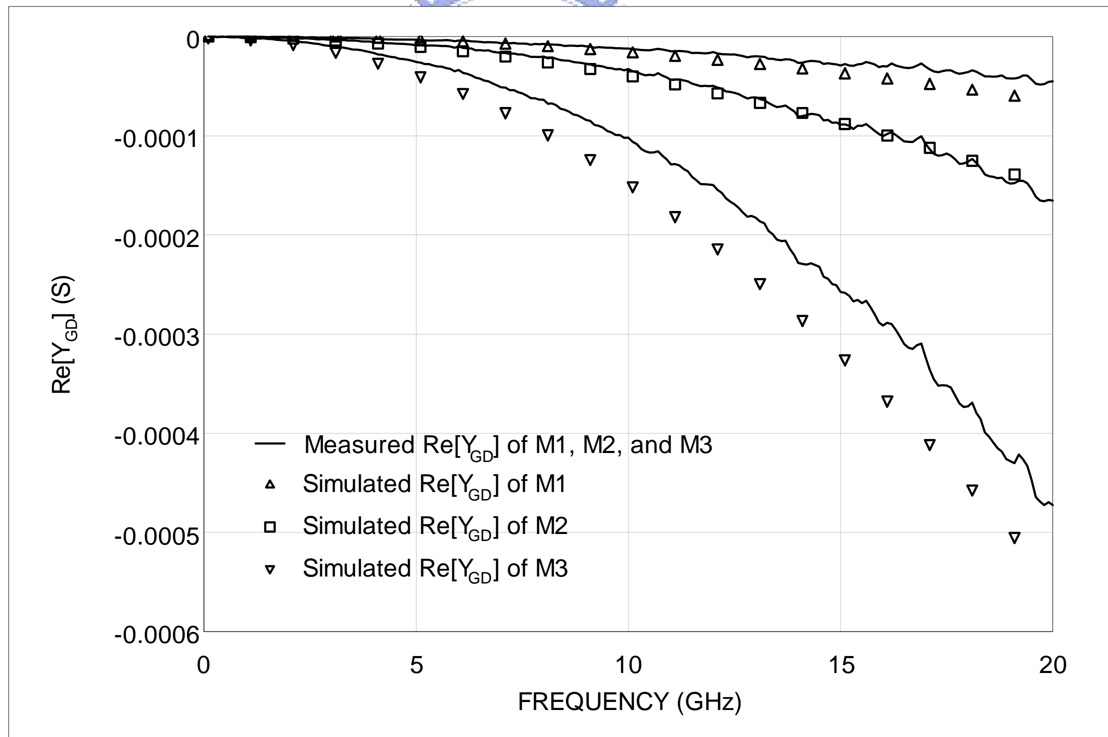


(b)

Fig.5.4 (a) Measured and simulated Im[Y_{BB}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re[Y_{BB}] of M1, M2, and M3 biased VG=VD=1V.

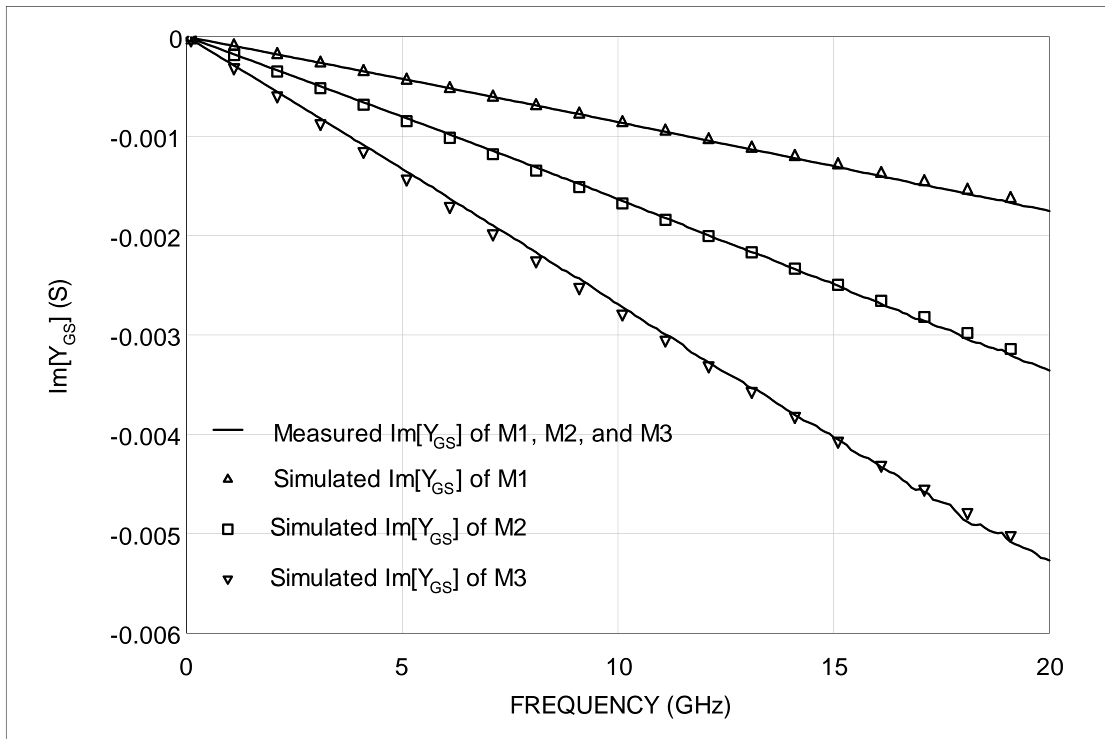


(a)

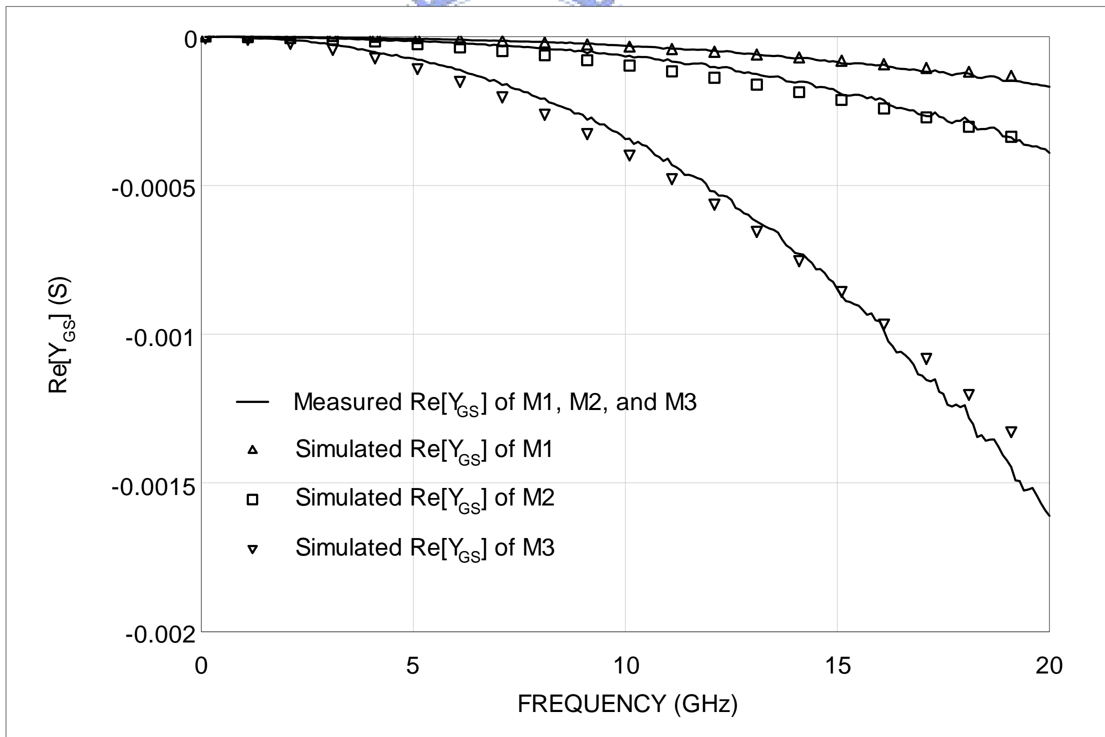


(b)

Fig.5.5 (a) Measured and simulated Im[Y_{GD}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{GD}] of M1, M2, and M3 biased VG=VD=1V.

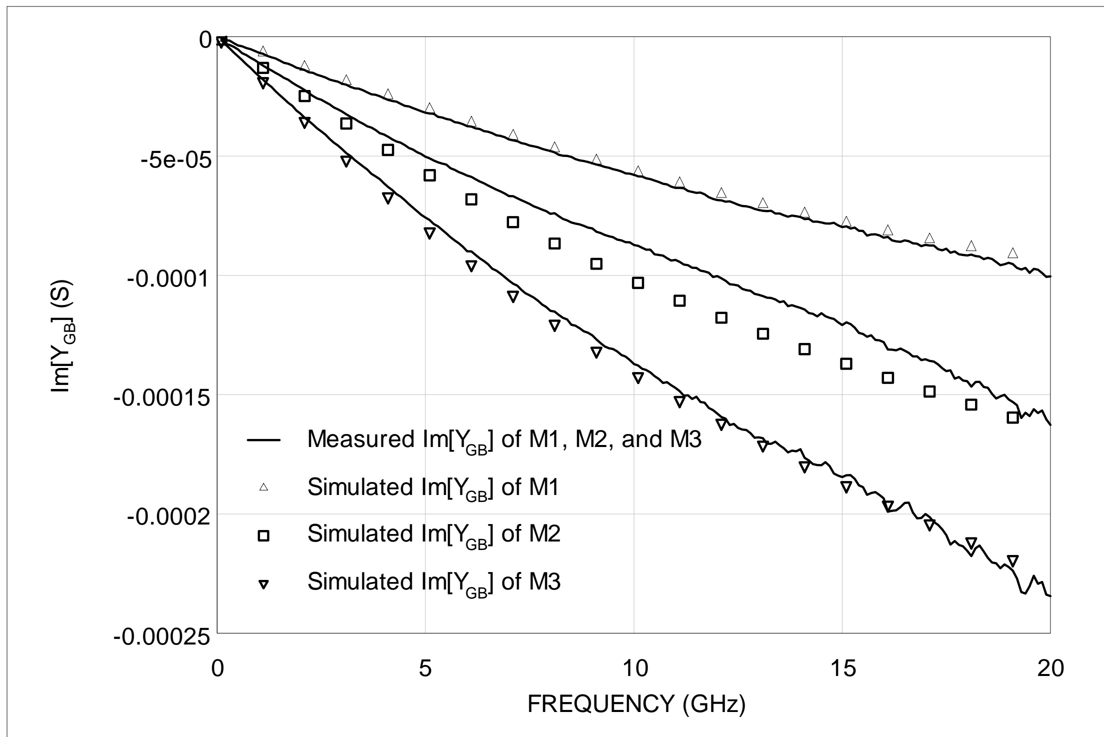


(a)

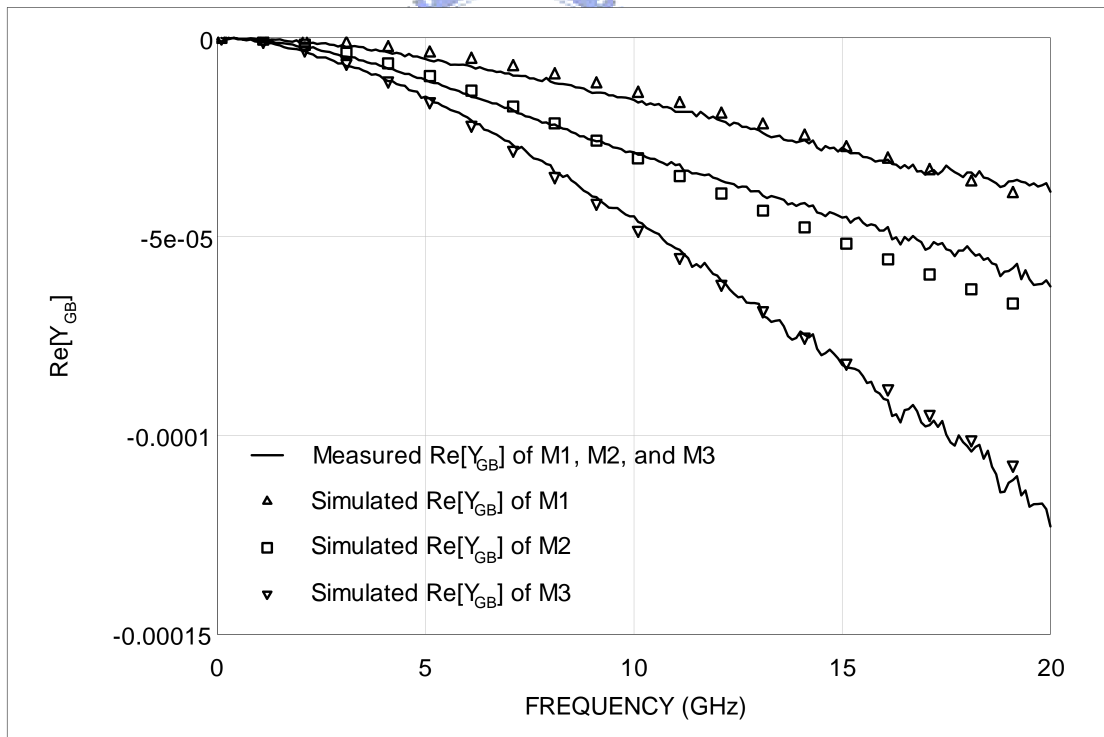


(b)

Fig.5.6 (a) Measured and simulated Im[Y_{GS}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{GS}] of M1, M2, and M3 biased VG=VD=1V.

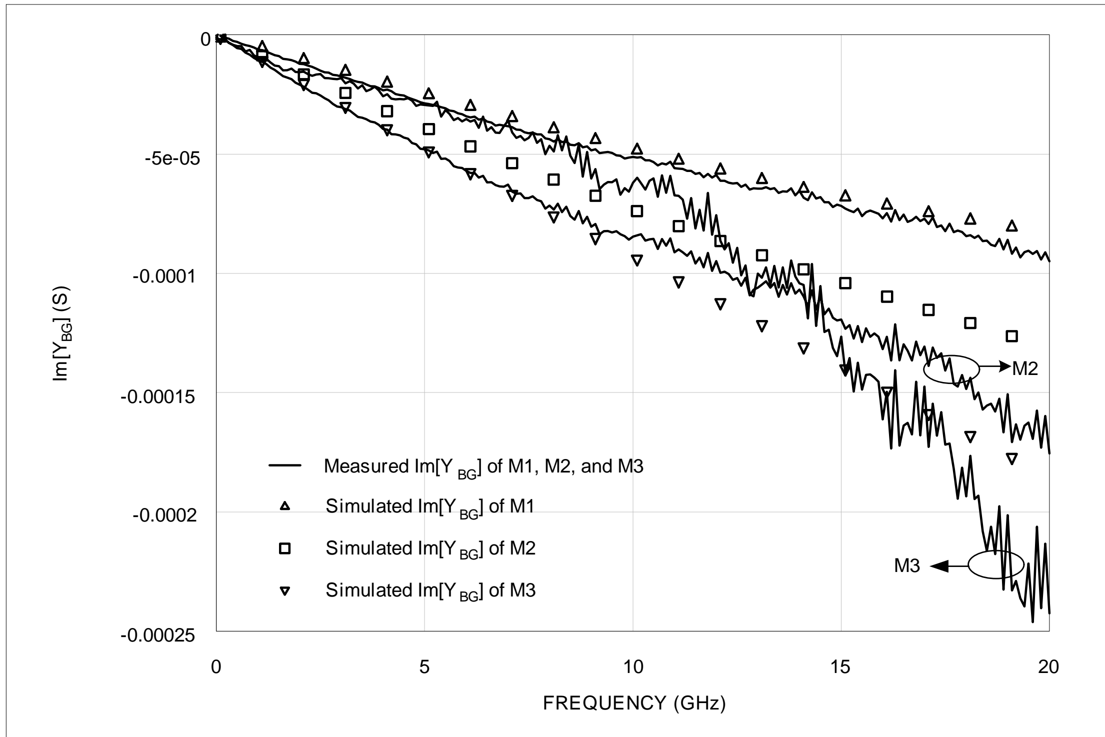


(a)

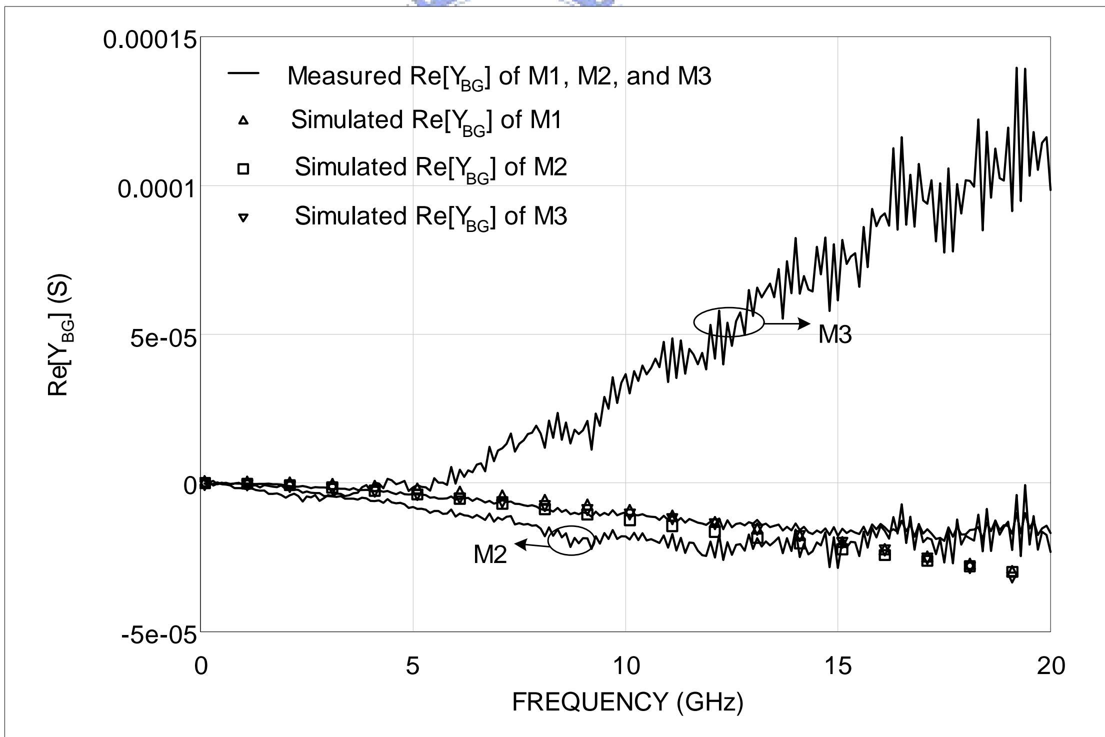


(b)

Fig.5.7 (a) Measured and simulated Im[Y_{GB}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{GB}] of M1, M2, and M3 biased VG=VD=1V.

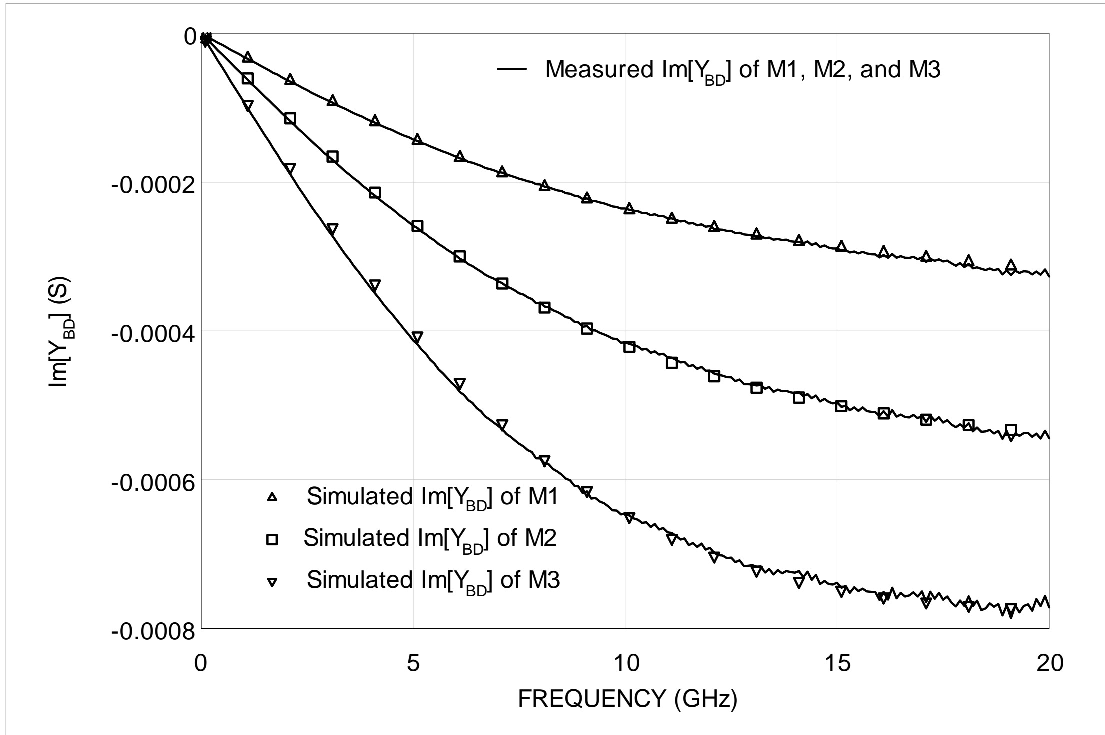


(a)

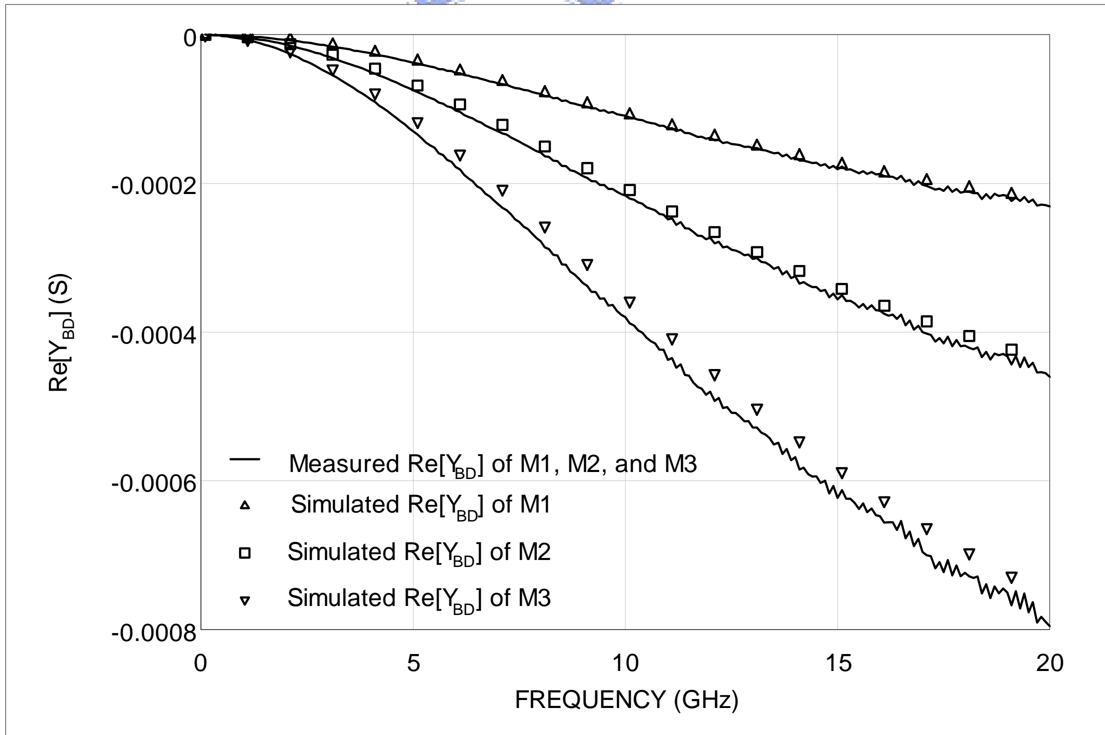


(b)

Fig.5.8 (a) Measured and simulated Im[Y_{BG}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{BG}] of M1, M2, and M3 biased VG=VD=1V.

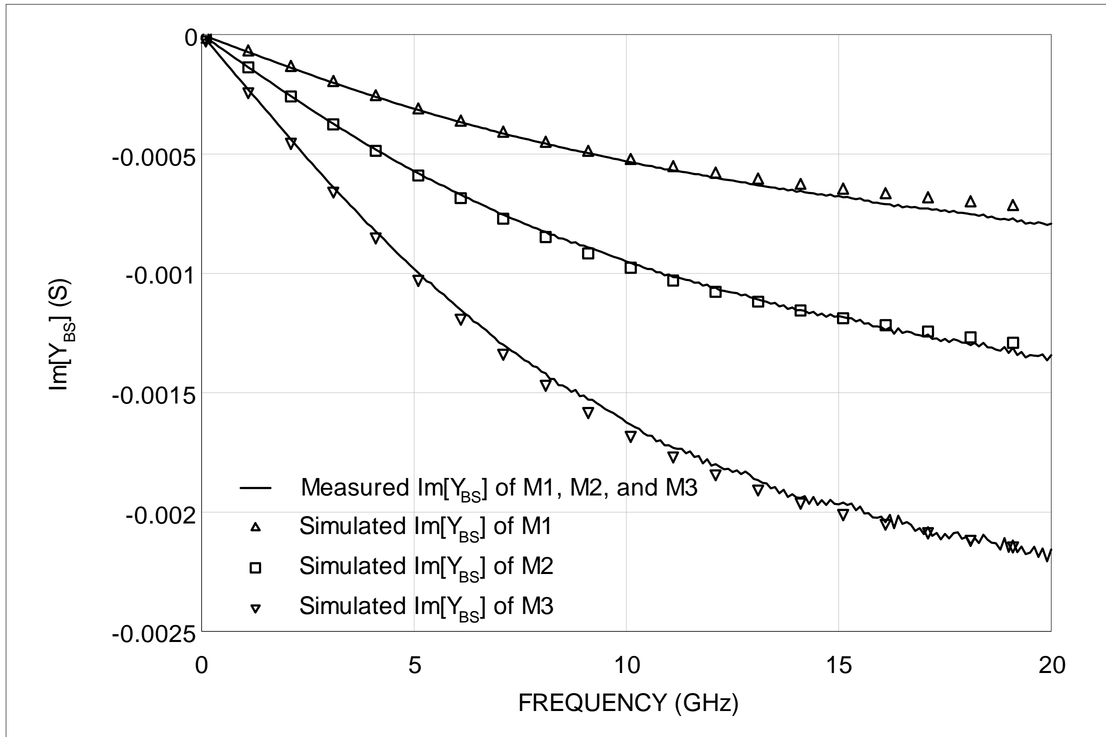


(a)

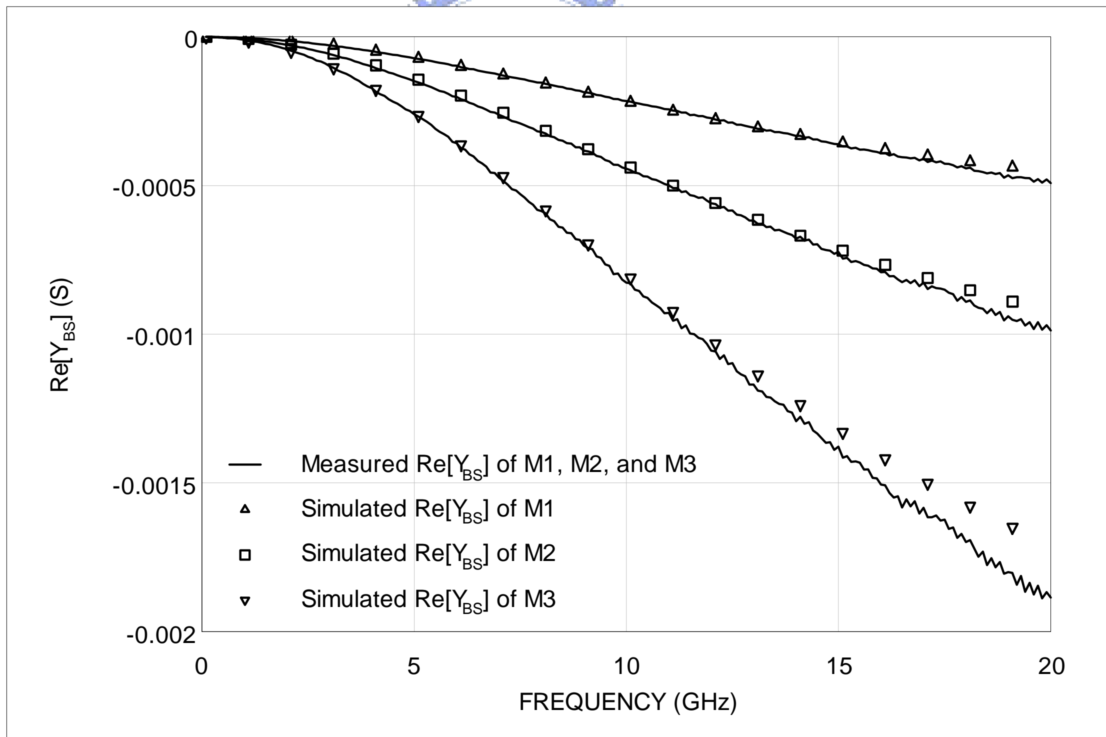


(b)

Fig.5.9 (a) Measured and simulated Im[Y_{BD}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{BD}] of M1, M2, and M3 biased VG=VD=1V.

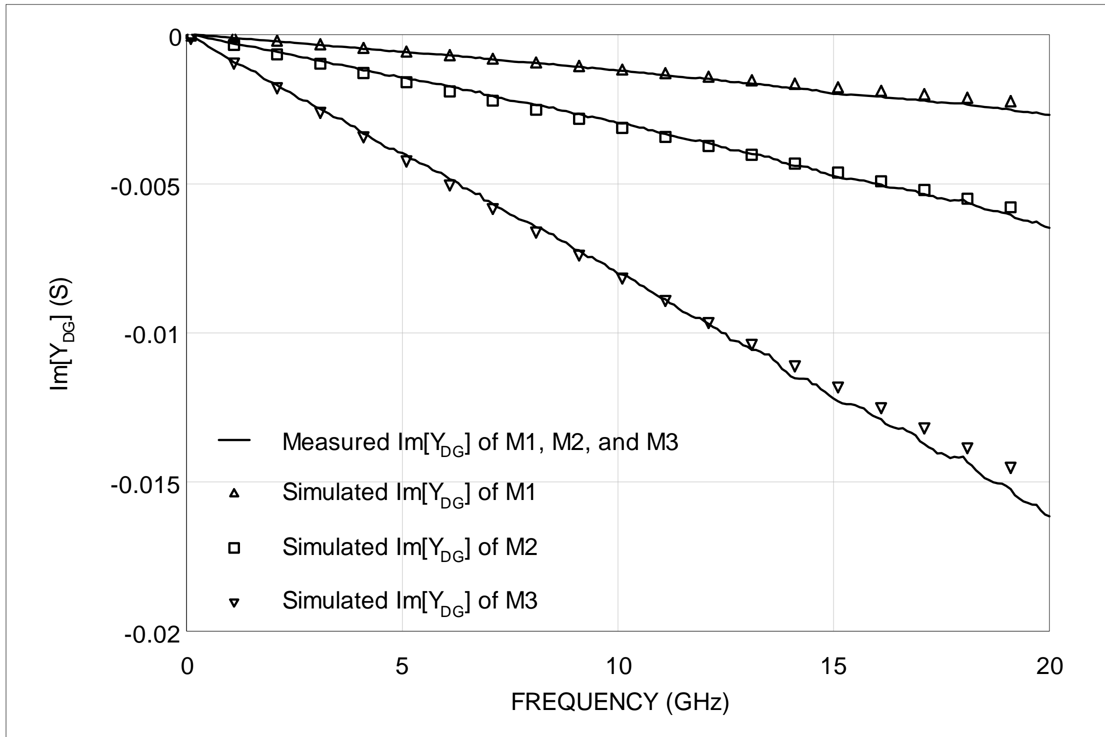


(a)

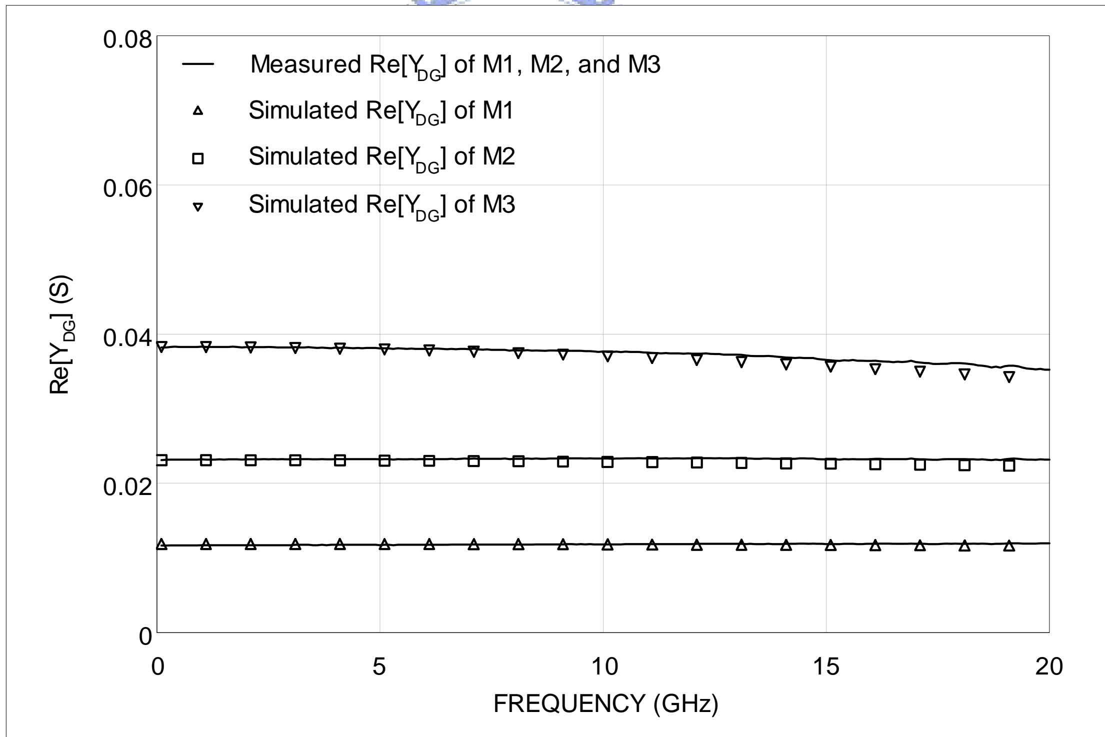


(b)

Fig.5.10 (a) Measured and simulated Im[Y_{BS}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{BS}] of M1, M2, and M3 biased VG=VD=1V.

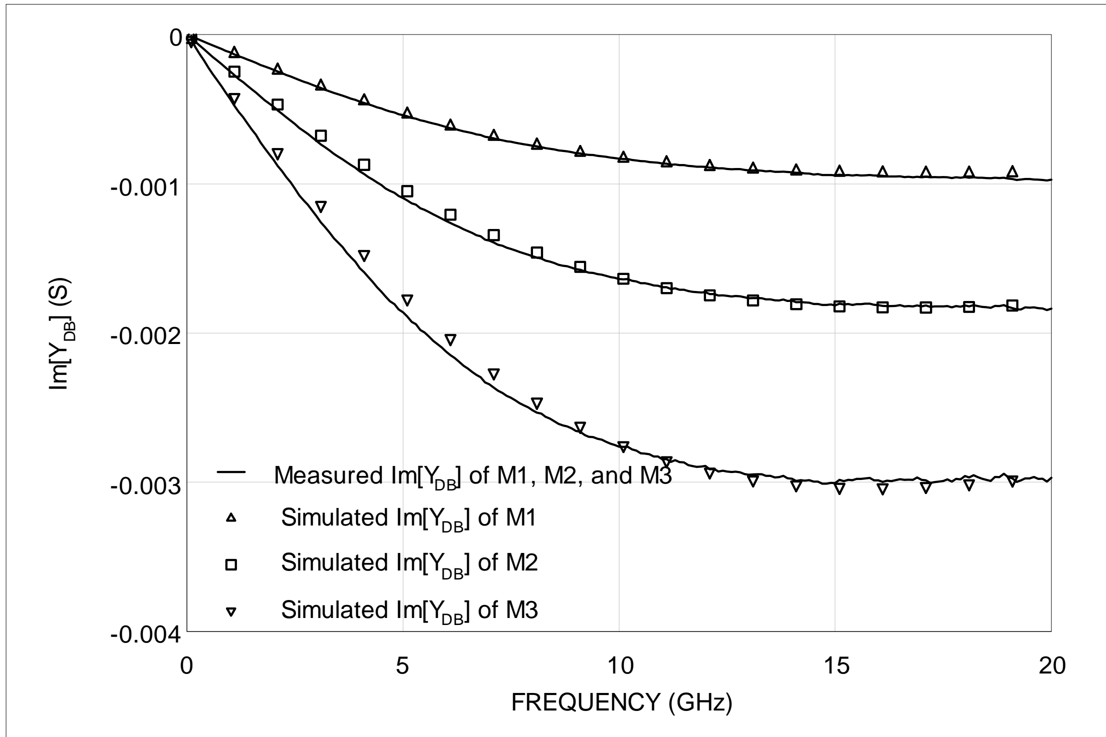


(a)

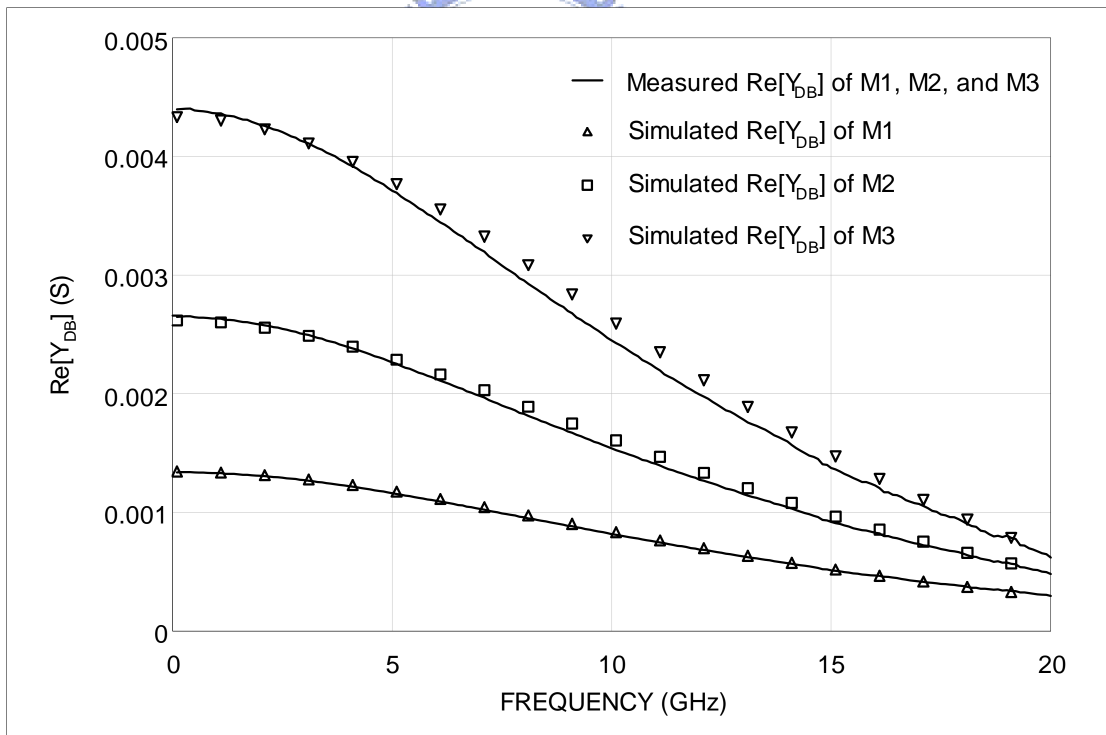


(b)

Fig.5.11 (a) Measured and simulated Im[Y_{DG}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re[Y_{DG}] of M1, M2, and M3 biased VG=VD=1V.

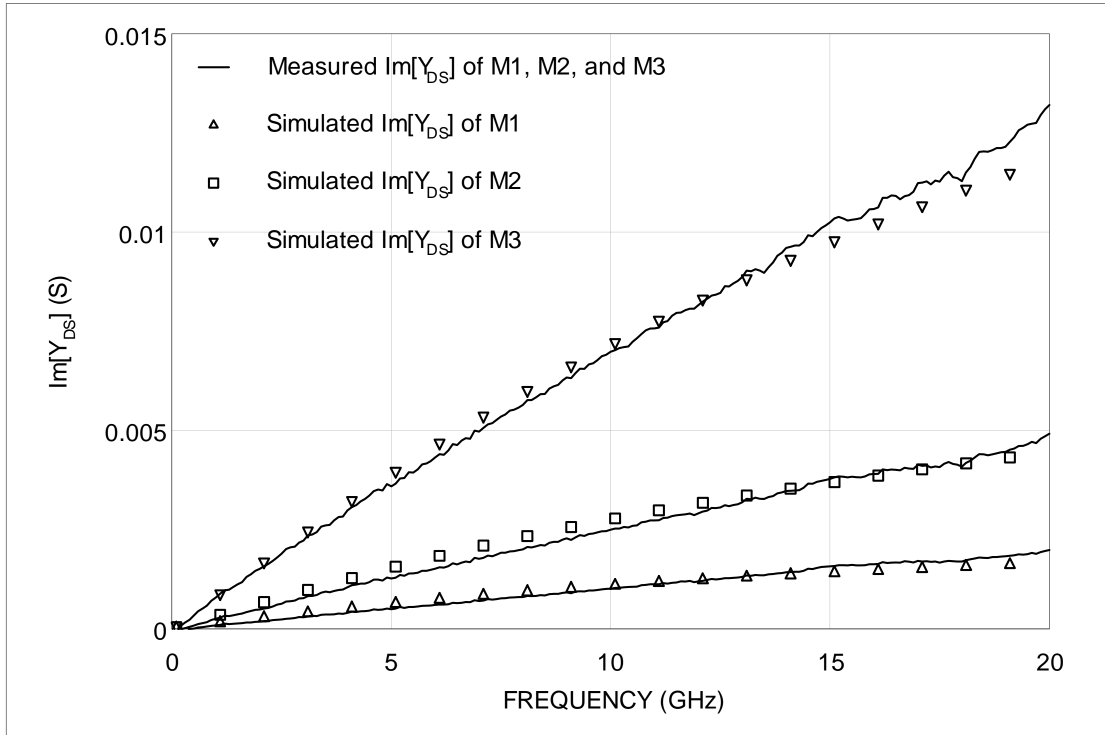


(a)

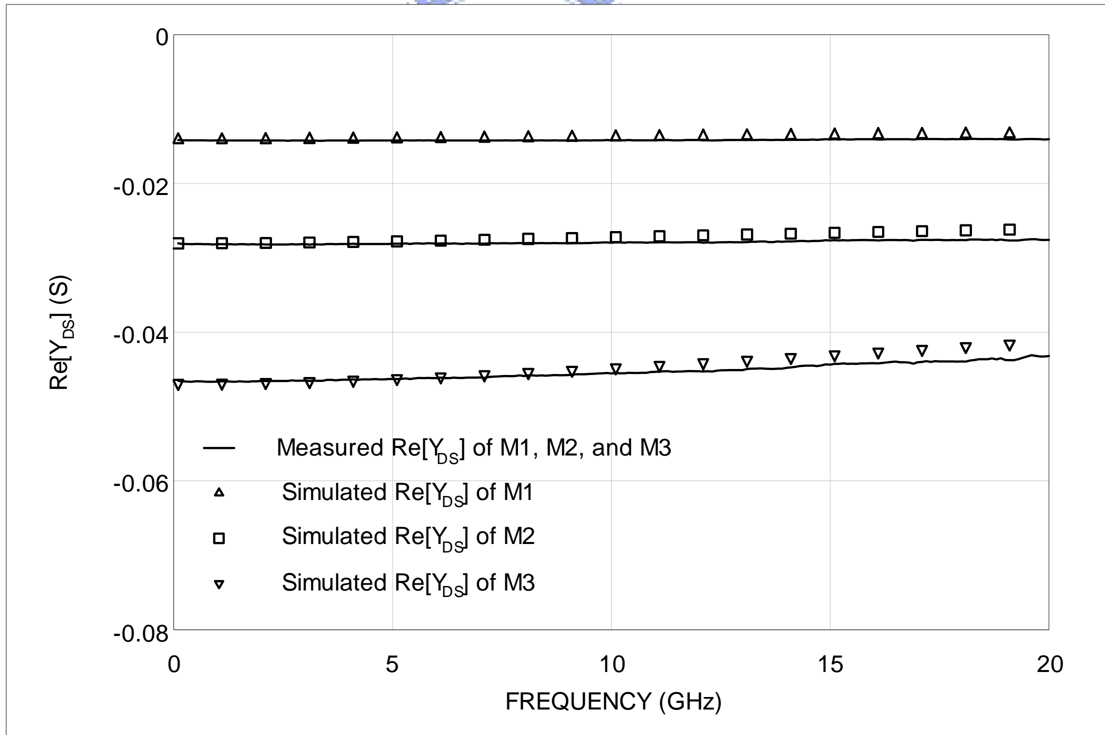


(b)

Fig.5.12 (a) Measured and simulated Im[Y_{DB}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re [Y_{DB}] of M1, M2, and M3 biased VG=VD=1V.

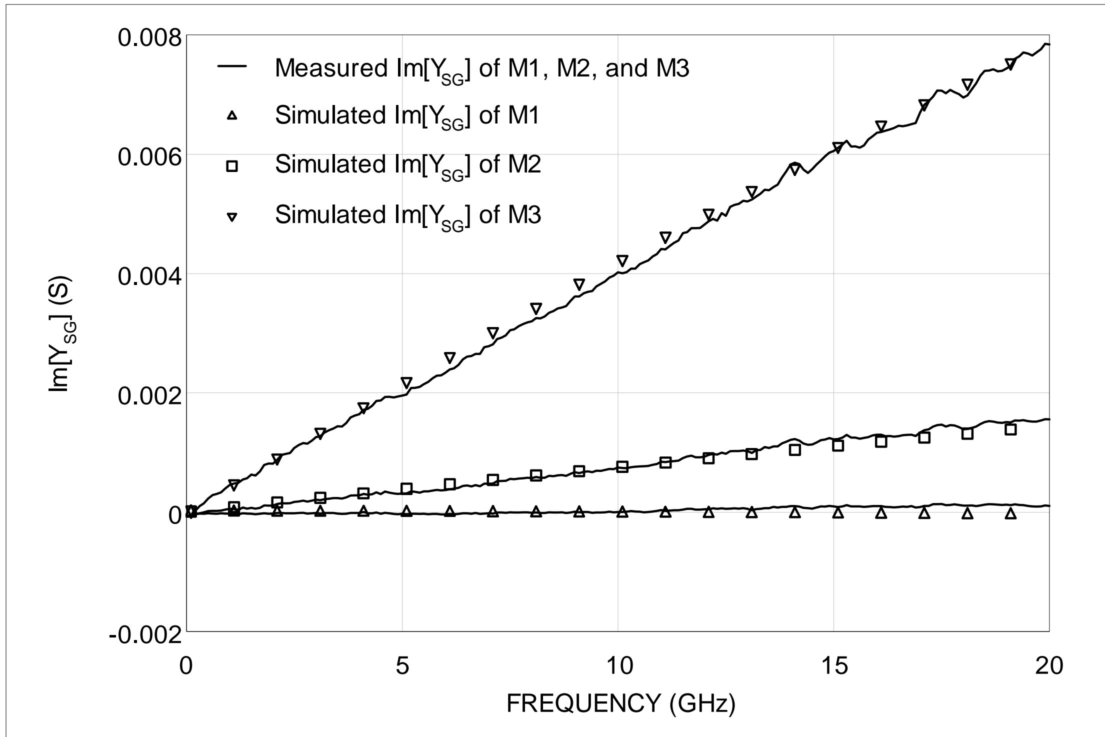


(a)

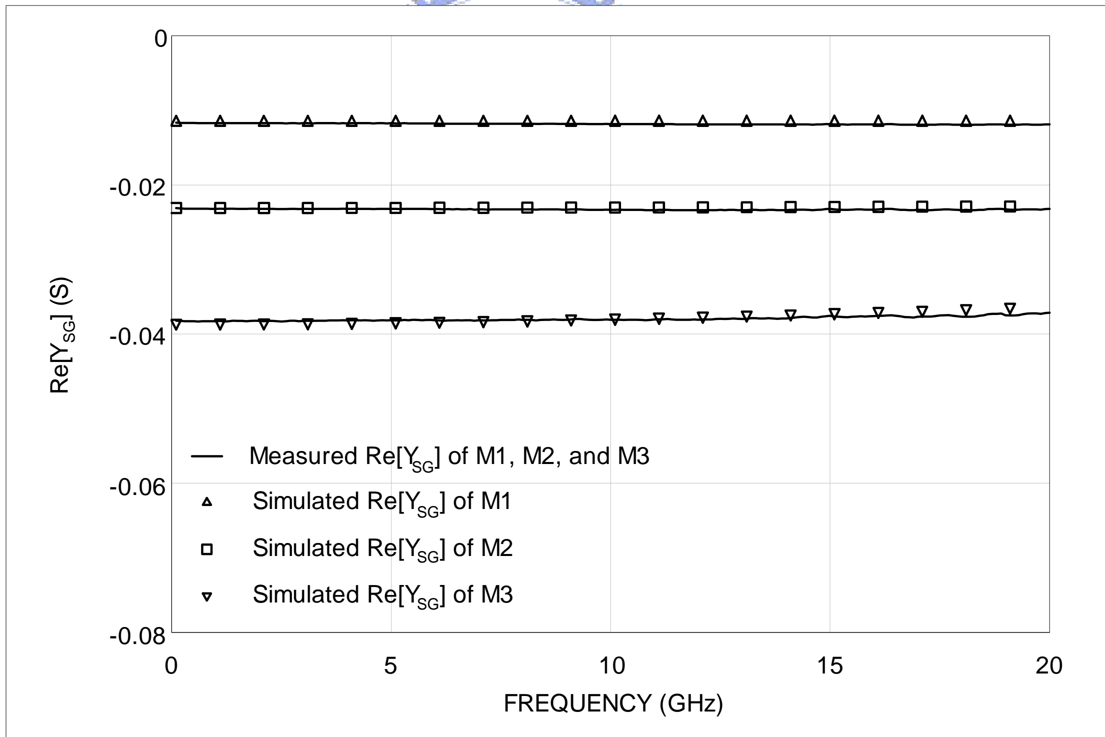


(b)

Fig.5.13 (a) Measured and simulated $Im[Y_{DS}]$ of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated $Re[Y_{DS}]$ of M1, M2, and M3 biased VG=VD=1V.

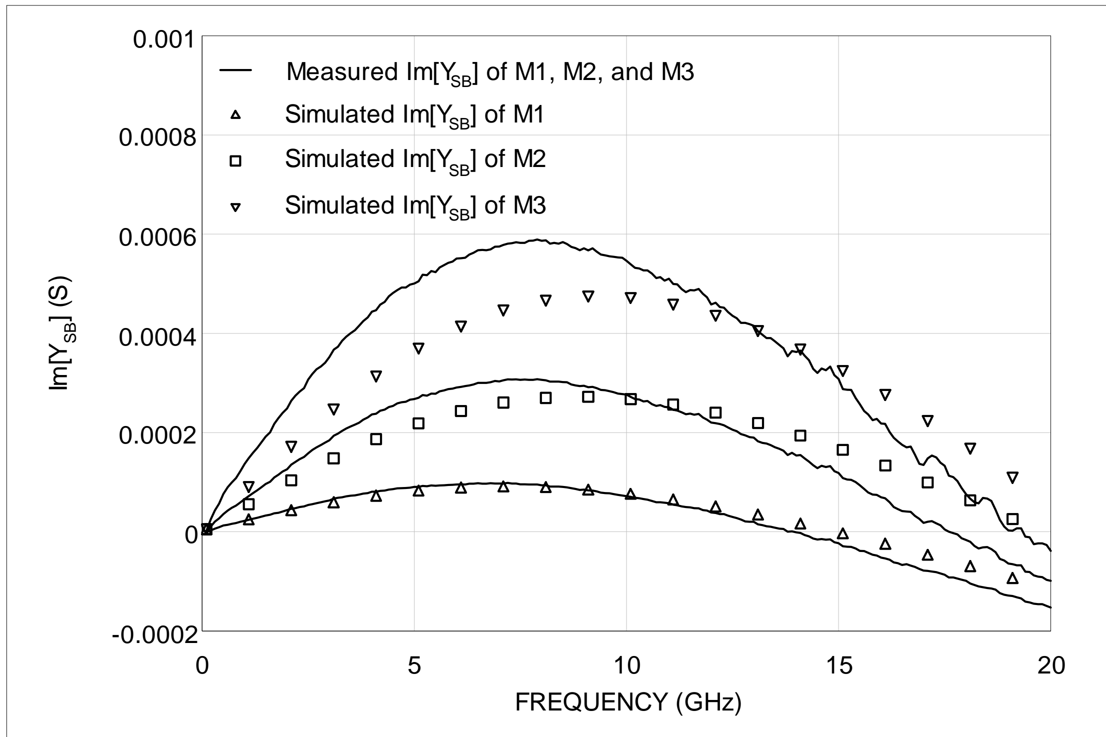


(a)

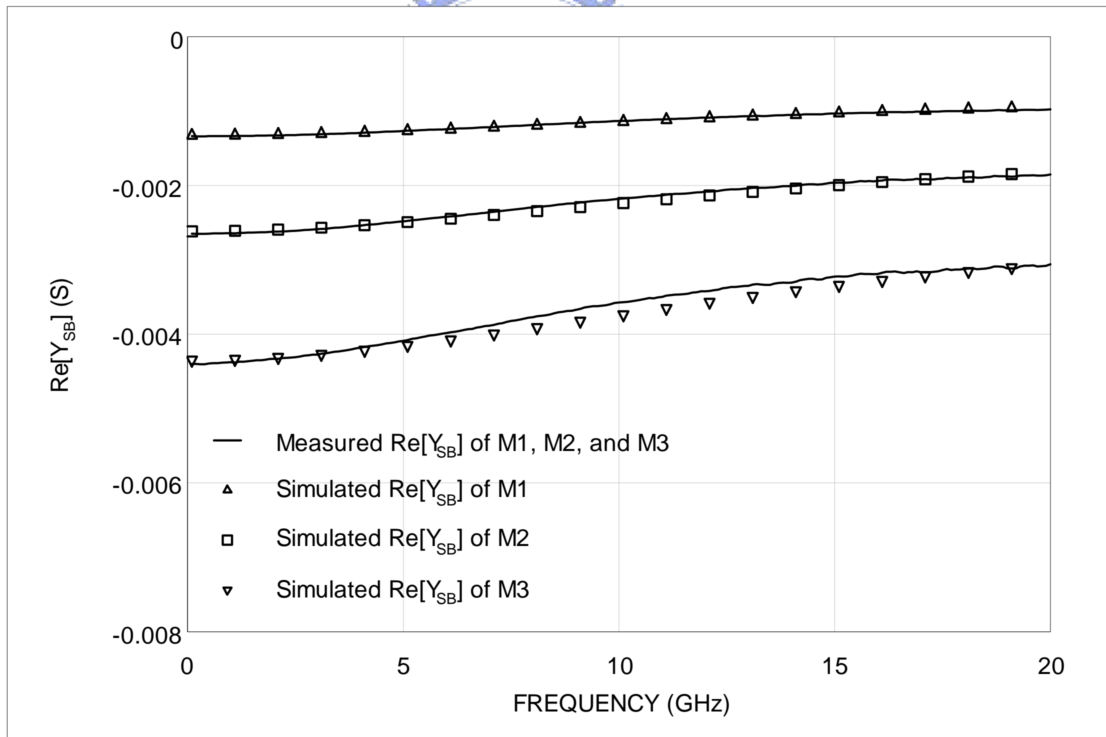


(b)

Fig.5.14 (a) Measured and simulated Im[Y_{SG}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re[Y_{SG}] of M1, M2, and M3 biased VG=VD=1V.

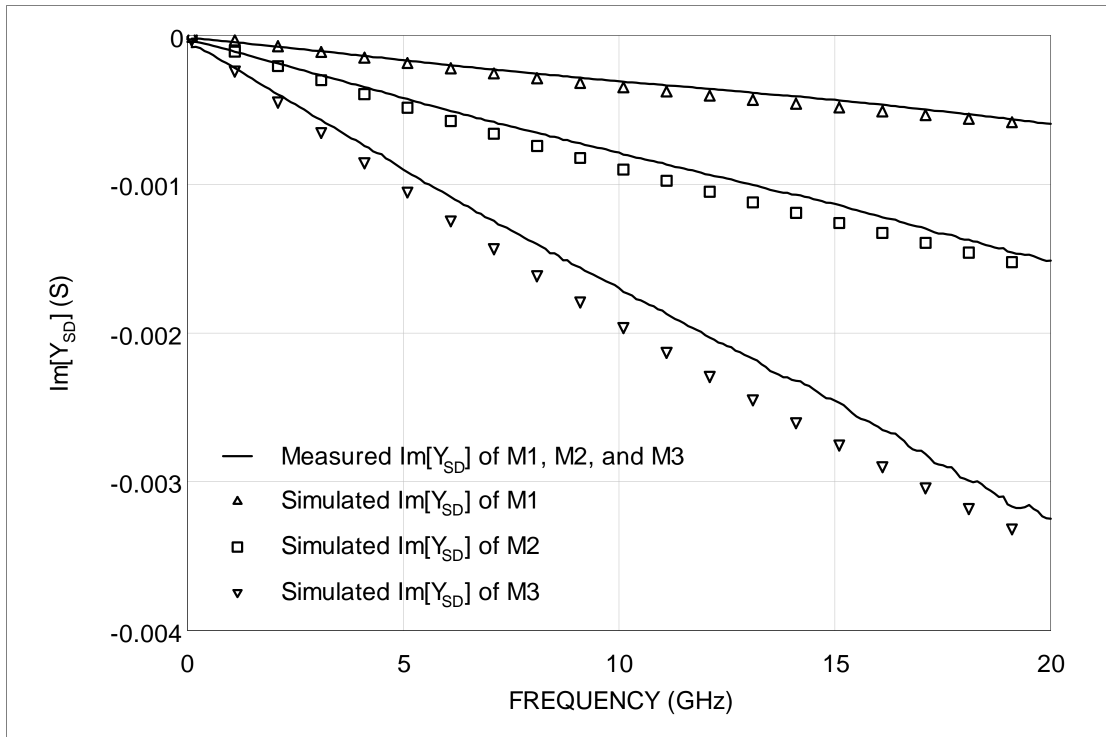


(a)

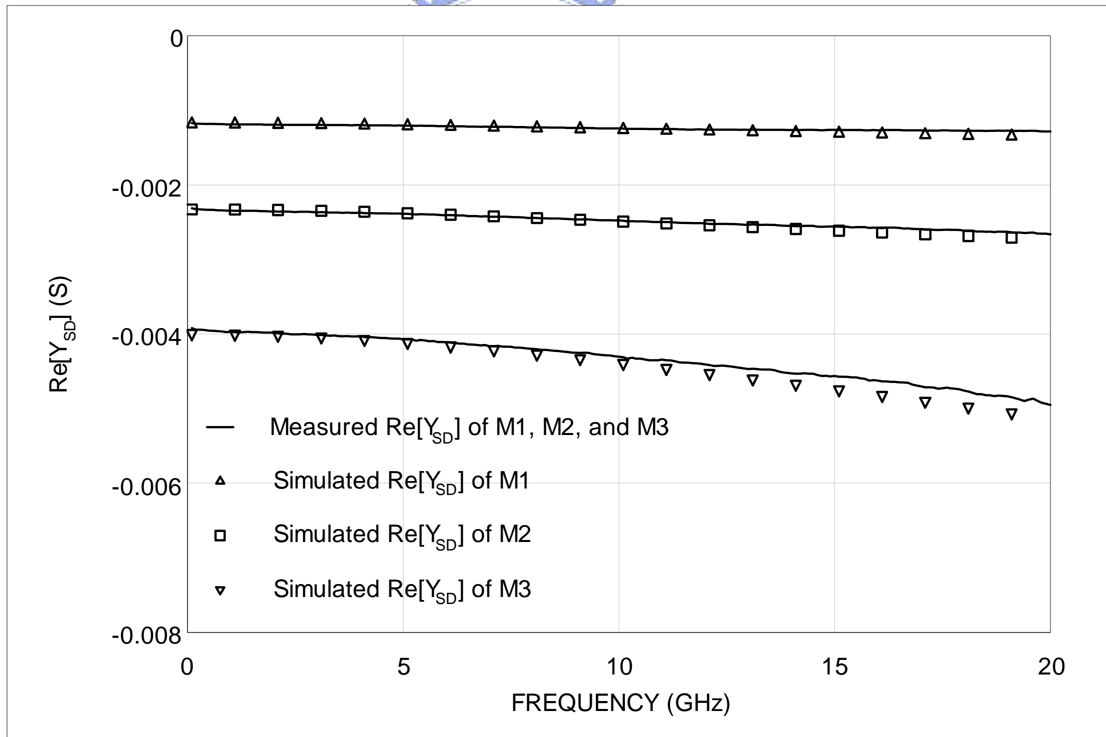


(b)

Fig.5.15 (a) Measured and simulated Im[Y_{SB}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re[Y_{SB}] of M1, M2, and M3 biased VG=VD=1V.



(a)



(b)

Fig.5.16 (a) Measured and simulated Im[Y_{SD}] of M1, M2, and M3 biased VG=VD=1V.
(b) Measured and simulated Re[Y_{SD}] of M1, M2, and M3 biased VG=VD=1V.

Chapter6

Conclusion and Suggestions for Future Works

6.1 Conclusion of This Study

With amazing advancement of CMOS technologies, RF MOSFET's have become an important candidate for the rapid growing wireless communication applications. Communication applications base on COMS technologies are potential to integrate the RF front end, base-band and DSP module together on a single chip, which not only improve the production cost but also the portability of modern communication applications. However, designing RF circuit base on CMOS devices is a challenge since the complex signal coupling inside the device, especially the substrate coupling effect. Therefore, establishing a model accurately predicts the RF behaviors of CMOS devices is an urgent mission. The traditional two-port characterization method is inefficient to investigate the detail RF behavior of a four terminal MOSFET. In this thesis, the four-port S-parameter measurement was proposed and demonstrated for the usage of on-wafer characterization of RF MOSFET's.

In chapter 2, the basic principles of one-port scattering parameters were reviewed and were extended for multi-port application.

In chapter 3, the four-port system was introduced including the calibration methodology. Moreover, test structures for characterizing RF MOSFET's including dummy structures were proposed. With the proposed test structures and MOSFET device, the RF characteristics of the MOSFET configured in common source, common gate, and common drain mode can be characterized at one four-port measurement procedure.

In chapter 4, small-signal equivalent circuits with reasonable substrate R-C network for device in different operation mode were proposed and discussed. Extraction methods of the components in these equivalent circuits were deduced in detail. The extractions of the components for devices in different dimensions were also demonstrated, good scalability of the extracted values with the device dimensions was observed.

Finally, the output characteristics of the proposed small-signal equivalent circuits were simulated according to the components extracted from the four-port measurement. The simulated results were compared with the measurement data; good agreement of the Y-parameters from 100MHz to 20GHz was obtained, which suggest the feasibility of applying four-port on-wafer measurement for characterizing RF MOSFET's.

6.2 Suggestions for Future Works

In this thesis, most studies were focus on characterization, parameter extraction, and modeling of RF MOSFET's. Some issues such as the behaviors of MOSFET's suffer from body effect or under different substrate bias could be further investigated. Moreover, applying the model based on four-port measurement to the circuit design process would be interesting and which can evaluate the accuracy of the model further.

Reference

[1] J. E. Lilienfeld, U.S. Patent 1,745,175, 1930.

[2] W. Shockley and G. L. Pearson, “Modulation of Conductance of Thin Films of Semiconductors by Surface Charges,” Phy. Rev., 74, 232, 1948

[3] D.Kahng and M. M. Atalla, “Silicon-Silicon Dioxide Field Induced Surface Devices,” IRE Solid-State Device Res. Conf., Carnegie Institute of Technology, Pittsburgh, Pa., 1960.

[4] D. Kahng, “A Historical Perspective on the Development of MOS Transistors and Related Devices,” IEEE, Trans., Electron Devices, ED-23, 655, 1976

[5] T. Cho, E. Dukatz, M. Mack, D. MacNally, M. Maringa, S. Mehata, C. Nilson, L, Plouvier, and S. Rabii, “ A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones,” Int, Solid-State Circuit Conf., 1999, p.228-229

[6] J. Rudell, J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, “ A 1.9 GHz Wide-Band IF Double Conversion CMOS Integrated Receiver For Cordless Telephone Applications,” Int. Solid-State Circuits Conf., 1997, p.304-305.

[7] A. Rofougaran, J. Y-C. Chang, M. Rofougaran, and A. Abidi, “ A 1GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver,” IEEE, J. Solid-State Circuits, Vol.31, July 1996, p.880-889.

[8] M. B. Das, “High frequency network properties of MOS transistors including the substrate resistivity effects,” IEEE Trans. Electron Devices, Vol. Ed-16, No.12, Dec. 1969, p.1049-1069.

[9] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal, and J. P. Mattia, “ RF MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model,” Int. Electron Devices

Meeting, 1997, p.309-312.

[10] J.J. Ou, X. Jin, I. Ma, C. Hu, and P.R. Gray, "CMOS RF modeling for GHz communication IC's" IEDM, 1998, 94-95.

[11] S.F. Tin, A.A. Osman, K. Mayaram, and C. Hu, " A simple subcircuit extension of the BSIM3V3 model for CMOS RF design," IEEE, J. Solid-State Circuits, Vol.35, no.4, Apr. 2000, 612-624.

[12] D.R. Pehlke, M. Schroter, A. Burstein, M. Matloubian, and M.F. Chang, "High-frequency application of MOS compact models and their development for scalable RF model libraries," Custom Integrated Circuits Conf., 1998, p.219-222.

[13] Y. Ge, and K. Mayaram, " A Comparative analysis of CMOS Low Noise Amplifiers for RF Applications," IEEE Proc. ISCAS 98, Vol.4, 1998, pp. 349-352.

[14] X. Li, H.S. Kim, M. Ismail and H. Olsson, "A Novel Design Approach for GHz CMOS Low Noise Amplifiers," IEEE RAWCON 99, 1999, pp. 285-288.

[15] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Generating All Two-MOS-Transistor Amplifiers Leads to New Wide-Band LNAs," IEEE Journal of Solid-State Circuits, Vol. 36, No.7 pp. 1032-1040 July 2001.

[16] J. Martinez-Castillo, A. Diaz-Sanchez and M. Linares-Aranda, "Differential Transimpedance Amplifiers for Communications Systems Based on Common-Gate Topology," IEEE ISCAS 2002, Vol.2, 2002, pp. 97-100.

[17] G. Gonzalez, "Microwave Transistor Amplifiers Analysis and Design," 2nd ed., New Jersey: Prentice Hall, 1996, pp. 60-61.

[18] F. Sischka, "IC-CAP Modeling Reference," Agilent Technologies, 2000, pp. 3_49-3_51.

[19] D.C. Benson, Y. Xuan, J. He, C.M. Lin, C.R. Hodges, and E. A. Logan, "Integrated passive components for RF applications," IEEE Wireless

Communication Conf., 1997, 175-180.

[20] D. Lovelace, J. Costa, and N. Camilleri, “Extracting small-signal parameters of silicon MOSFET transistors,” IEEE Trans. Microwave Theory and Techniques Symp., 1994, p.865-868.

[21] C.E. Biber, M.L. Schmatz, T. Morf, U. Lott, and W. Bachtold, “A nonlinear microwave MOSFET model for Spice simulators,” IEEE, Trans. Microwave Theory and Techniques, Vol.46, no.5, May, 1998, p.604-610.

[22] R. Sung, P. Bendix, and M.B. Das, “Extraction of high-frequency equivalent circuit parameters of submicron gate-length MOSFET’s,” IEEE Trans. Electron Devices, vol.45, no.8, Aug. 1998, p.1769-1775.

[23] S.H.M. Jen, C.C. Enz, D.R. Pehlke, M. Schroter, and B.J. Sheu, ”Accurate Modeling and parameter extraction fro MOS transistors valid up to 10 GHz,” IEEE Tran. Electron Devices, vol.46. No.11, PP.2217-2227, Nov. 1999.

[24] A. Ferrero, U. Pisani, “Two-Port Network Analyzer Calibration Using an Unknown “thru””, IEEE Microwave and Guided Wave Letters, Vol.2, No.12, Dec 1992.

[25] S. Basu, L. Hayden, “An SOLR Calibration for Accurate Measurement of Orthogonal on-wafer DUTs”, pp. 1335-1338, 1997 IEEE MTT-S Digest.

[26] Y. Cheng et al., ”A physical and scalable BSIM3V3 IV model for analog/digital circuit simulation,” IEEE Trans. Electron Devices, Vol.44, p.277-287, Feb, 1997.

[27] Mos9 manual, http://www.semiconductors.philips.com/Philips_Models.

[28] Y. Cheng, M. Schroter, C. Enz, M. Matloubian and D. Pehlke, “RF modeling Issue of deep-submicron MOSFET’s for circuit design,” Proc. of the IEEE Int. Conf. On Solid-State and Integrated Circuit Technology, p.416-419, Otc. 1998.

[29] C.C. Enz, Y. Cheng, “MOS transistor modeling for RF IC Design,” IEEE Tran. Solid-State Circuits, vol.35, No.2, Feb. 2000.

[30] C.C. Enz, “An MOS transistor model for RF IC Design Valid in all regions of operation,” IEEE Tran. Microwave Theory and Techniques, vol. 50, No. 1, Jan. 2002.

[31] W. Liu, R. Gharpurey, M.C. Chang, U. Erdogan, R. Aggarwal, and J.P. Mattia, “RF MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model,” Technical Digest of international Electron Device Meeting, p.309-312, Dec, 1997.

[32] Y.P. Tsividis, “Operation and Modeling of the MOS Transistor”, New York: McGraw-Hill, 1988.

[33] J. Han, M. Je, and H. Shin, “A simple and accurate method for extracting substrate resistance of RF MOSFETs” IEEE Electron Device Lett., Vol. 23, NO. 7, pp. 434-436, July 2002.

[34] M. Je, and H. Shin, “Gate bias dependent of substrate signal coupling effect in RF MOSFETs” IEEE Electron Lett. VOL. 24, NO. 3, pp.183-185, March 2003.

[35] Y. Cheng, and M. Matloubian “On the high-frequency characteristics of substrate resistance in RF MOSFETs” IEEE Electron Lett. VOL. 21, NO. 12, pp.604-606, Dec. 2000.

[36] X. Jin, J. J. Ou, C. H. Chen, W. Liu, and M. J. Deen, “An effective gate resistance model for CMOS RF and noise modeling,” IEDM Tech. Dig., pp. 961-964, 1998.

[37] H. W. Lin, S. S. Chung, S. C. Wong, and G. W. Huang, “An accurate RF CMOS Gate Resistance Model Compatible with HSPICE,” Proc. IEEE 2004 Int. Conf. Microelectronic Test Structure, Vol. 17, pp.227-230, March 2004.

1896

Publication List

1. **Shih-Dao Wu**, Guo-Wei Huang, Kun-Ming Chen, Chun-Yen Chang, Hua-Chou Tseng, and Tsun-Lai Hsu, "Extraction of Substrate Parameters for RF MOSFET's Based on Four-Port Measurement," IEEE Microwave And Wireless Components Letters, vol. 15, No. 6, p.437-439, June 2005.
2. **Shih-Dao Wu**, Guo-Wei Huang, Kun-Ming Chen, Hua-Chou Tseng, Tsun-Lai Hsu, and Chun-Yen Chang, "RF MOSFET Characterization by Four-Port Measurement," IEICE Trans. Electron., Vol.E88-C, No. 5, p.851-856, MAY 2005.
3. **Shih-Dao Wu**, Guo-Wei Huang, Sheng-Yo Wen, Liang-Po Chen, and Chun-Yen Chang, "Characterization of 2-port Configuration MOSFET's Amplifiers by 4-port Measurement," 2003 Asia-Pasific Microwave Conference, p.1431