國 立 交 通 大 學

電子工程學系電子研究所

碩士論文

利用熱氧化法製備氧化銅薄膜於電阻式轉態記憶體之研究

Resistive switching characteristics of the thermal-oxidized CuO memory films

研究生：黃志文

指導教授：曾俊元　教授

中華民國九十七年七月

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研究生：黃志文　　Student：Chih-Wen Huang

指導教授：曾俊元　教授　　Advisor：Prof. Tseung-Yuen Tseng

國立交通大學

電子工程學系電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics

college of Electrical and computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

July 2009

Hsinchu, Taiwan, Republic of China

中華民國六十七年七月

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國立交通大學電子工程學系電子研究所碩士班

摘要

近年來，由於非揮發性記憶體的應用與發展受到矚目，加上快閃記憶體的微縮極限，有關新世代非揮發性記憶體的發展呈現百家爭鳴的情形。其中，電阻式非揮發性記憶元件具有低功率消耗、高密度、高操作速度、高耐久性、微縮能力高及非破壞性資料讀取等優點，使其成為新世代非揮發性記憶元件的熱門人選。

而研究氧化銅這個材料的原因之一，是因為氧化銅在標準先進半導體 CMOS 製程技術中有銅導線製程做為元件之間的連接，所以氧化銅和 CMOS 製程具有很高的相容性。其次的原因是因為 NiO 做為電阻式記憶體被廣為研究，而 Ni 和 Cu 在元素週期表相鄰。進而想研究 CuO 這個氧化物材料是否有做為新一帶電阻式記憶體的潛力。這篇論文中，著重電阻轉態特性的研究與探討，其內容可分為兩大部份，包含不同限流和不同停止電壓對轉態特性的影響。藉由這兩個不同的量測方式探討導電細絲在薄膜內轉態的情況以及介面對轉態特性的影響，進而提出轉態之模型解釋實驗觀察到的現象。另外藉由不同的限流可以控制低電阻態的電阻值；而以鈦做為上電極，電阻轉態由原本無極性變為有極性狀態使轉態次數增加，並可藉由不同的停止電壓可以控制高電阻態的電阻值，在應用方面可以做為多重位元儲存記憶體的潛力。

Resistive switching characteristics of the thermal-oxidized CuO memory films

Student: Chih-Wen Huang Advisor: Prof. Tseung-Yuen Tseng

Department of Electronics Engineering and Institute of Electronics

National Chiao Tung University

Abstract

Recently, since nonvolatile memories acquire a lot of attention and flash memories are faced with the scale limit issue, the extensive studies have been carried out to discover the next generation nonvolatile memory. The resistive switching random access memories (RRAMs) having the strengths of low power consumption, and high-density integration, high speed, high endurance, nondestructive read as one of the next-generation nonvolatile memory candidates.

One reason is that the fabrication of Cu-oxide based RRAM has great advantages of full compatibility with Cu interconnection process in state-of-art complementary metal oxide semiconductor CMOS technology, promising easy integration with current semiconductor processing technology. The other reason is the material, NiO, has been studied widely. Thus, we want to investigate the potential of the material, CuO, to become resistive switching memory. In this thesis, the resistive switching characteristics are investigated, and the research can be categorized into two parts, the current compliance influence and the stop voltage influence resistive switching characteristics. By means of these two kind measures, we investigate the filament

transform in the resistive switching layer, when resistive switching occurs. We propose a model to explain the phenomenon, which was observed in experiment. The resistance of ON-state was controlled by current compliance. The polarity of resistive switching changed to bipolar switching by using Ti top electrode, and the resistance of OFF-state was controlled by stop voltage. In application, Ti/CuO/Pt device has a potential for nonvolatile multiple-valued memory device.

誌 謝

兩年前的這個時候，我還是懵懵懂懂的新生。時光飛逝，歲月如梭，如今碩士論文已經完成，也意味著人生下一個階段的開始；這兩年碩士生活受過很多人的幫忙，也經歷了很多的事情，讓我覺得能在這裡除了感到受益良多也有許許多多的回憶。

首先要特別感謝我的指導教授曾俊元教授提供良好完善的實驗環境和設備，使這篇論文能順利完成。也要謝謝侯拓宏老師在實驗上給的建議，以及胡教授在百忙之中抽空擔任我的口試委員，指出學生論文中的缺失，本篇論文更加完整。

其次，要感謝王聖裕學長在實驗上的幫忙。接著要感謝胖胖在實驗設備上以及其它的幫助。還要感謝小岱哥教我ＡＩＣ以及和我討論實驗。從從在畢業這段期間也幫了我不少的忙。也要謝謝猛男和錡哥學長在實驗上給的寶貴意見。

此外也要感謝之前畢業的學長海哥和翁翁帶我們做實驗。還有同一屆的同學們；神奇的小爆（認識一堆女生）、個性很酷的桃子（其實很有喜感）、阿賢、超會模仿葉葉、黑黑和大頭，有你們在實驗室，讓苦悶的研究生活增添不少歡笑。還有謝謝學弟們布丁、小煒、震撼在實驗上或一些雜事上的幫忙。

在我的研究生活中還有很多人值得我感謝的人。阿尼機（是個有情有義的傢伙）、侑廷（一開始騙我說不讀博班傢伙）、介銘（話不多）、耀鋒（嘴巴很鋒利）、信淵（超級高手），還有老同學阿順、大姊，已經畢業的塞哥以及室友阿諾在忙碌得一天後還有人可以聊天。在羽球場上也認識許許多多的朋友，謝謝你們和我打球。當然還有我弟鵬達，我快要比你厲害了。

最後我要感謝我最親愛的家人，我的父母一直支持我完成我的學業，我要感謝我父親黃聖財先生的支持。也要感謝我的母親張月娥女士一直默默的為家裡犧牲付出。沒有你們的支持我完成不了這個學業。

有些人有些事三言兩語說不盡，不過都在我的記憶當中。最後我想說，如果沒有你們大家的幫助也不會成就今天的我。謹以此論文獻給大家，感謝各位陪我走過這些日子也謝謝大家的幫助。

黃志文　謹識

風城 交通大學

2009 年

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Chapter 1
Introduction

1.1 Introduction to non-volatile memory

Memory can be split into two main categories: volatile and nonvolatile. Volatile memory loses any data as soon as the system is turned off; it requires constant power to remain viable. Most types of random access memory (RAM) fall into this category. Nonvolatile memory does not lose its data when the system or device is turned off. The nonvolatile memory (NVM) would keep the stored information under any conditions without power supply for Non-volatile memory is computer memory that can retain the stored information even when not powered. Examples of non-volatile memory include read-only memory, flash memory, most types of magnetic computer storage devices (e.g. hard disks, floppy disks, and magnetic tape), optical discs, and early computer storage methods such as paper tape and punch cards.a long time. The first NVM is the floating-gate nonvolatile memory, invented by S. M. Sze and D. Kahng in 1967. NVMs have been widely used in the portable devices recently, such as flash memory devices, cell phones, digital cameras, mp3 players, and personal digital assistants. A perfect NVM should have the properties including low operation voltage, simple structure, low power consumption, non-destructive readout, high operation speed, long retention time, high endurance, and small cell size. There have been many sorts of nonvolatile memories invented so far, such as flash memory, erasable programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), phase-change memory (PCRAM), ferroelectric random

access memory (FeRAM), magnetoresistive random access memory (MRAM), and resistance random access memory (RRAM). Nowadays, flash memory is the mainstream among the NVMs

The following is focused on the next generation nonvolatile memories, including MRAM, FeRAM and RRAM. Flash memories are also introduced.

1.1.1 Flash

Flash memory is a form of nonvolatile computer memory that can be electrically erased and reprogrammed, invented by Gerard Dixon.

Flash memory stores information in an array of floating gate transistors, called “cells”, each of which traditionally stores one bit of information. The latest flash memory devices, sometimes referred to as multi-level cell devices, can store more than 1 bit per cell, by using more than two levels of electrical charge, placed on the floating gate of a cell. General write times for common flash memory devices are on the order of 1 ms, about 100 times the typical 10 ns read time.

NOR flash, each cell looks similar to a standard MOSFET, is expected that it has two gates instead of just one. One gate is the control gate (CG) like in other MOS transistors, but the second is a floating gate (FG) that is insulated all around by an oxide layer. The FG is between the CG and the substrate. Because the FG is isolated by its insulating oxide layer, any electrons placed on it get trapped there and thus store the information. When electrons are on the FG, they modify (partially cancel out) the electrical field coming from the CG, which further modifies the threshold voltage (Vt) of the cell. Thus, when the cell is “read” by placing a specific voltage on the CG, electrical current will either flow or not flow, depending on the Vt of the cell, which is

controlled by the number of electrons on the FG. This presence or absence of current is sensed and translated into 1's and 0's, reproducing the stored data. In a multi-level cell device, which stores more than 1 bit of information per cell, the amount of current flow will be sensed, rather than simply detecting presence of absence of current, in order to determine the number of electrons stored on the FG. A NOR flash cell is programmed (set to a specified data value) by starting up electrons flowing from the source to the drain, then a large voltage placed on the CG provides a strong enough electrical field to suck them up onto the FG, a process called hot-electron injection. To erase (reset to all 1's, in preparation for reprogramming) a NOR flash cell, a large voltage differential is placed between the CG and source, which pulls the electrons off through quantum tunneling. In single-voltage devices (virtually all chips available today), this high voltage is generated by an on-chip charge pump. Most modern NOR flash memory components are divided into erase segments, usually called either blocks of sectors. All of the memory cells in a block must be erased at the same time. NOR programming, however, can generally be performed one byte of word at a time.

NAND flash uses tunnel injection for writing and tunnel release for erasing. NAND flash memory forms the core of the removable USB interface storage devices known as USB flash drives.

As manufacturers increase the density of flash devices, individual cells shrink and the number of electrons in any cell becomes very small. Coupling between adjacent floating gates can change the cell write characteristics. New designs, such as charge trap flash, attempt to provide better isolation between adjacent cells.

Although the flash memory is mainstream device of NVM, flash memory has the drawbacks including high operation voltage, low operation speed, and low endurance.

Furthermore, following the device scaling, the tunneling oxide will be shrunken, which then leads to large leakage current, therefore the retention time of flash memory will be reduced due to the device scaling.

1.1.2 MRAM

Magnetoresistive random access memory (MRAM) has been in development since the 1990's unlike conventional RAM chip technologies, data is not stored as electric charge of current flows, but by magnetic storage elements. The elements are formed from two ferromagnetic plates, each of which can hold a magnetic field, separated by a thin insulating layer. One of the two plates is a permanent magnet set to a particular polarity, the other's field will change to match that of an external field. A memory device is built from a grid of such cells.

Reading is accomplished by measuring the electrical resistance of the cell. A particular cell is selected by powering an associated transistor, which switched current from a supply line through the cell to ground. Due to the magnetic tunnel effect, the electrical resistance of the cell changes due to the orientation of the fields in the two plates. By measuring the resulting current, the resistance inside any particular cell can be determined, and from this the polarity of the writable plate. Typically is the two plates have the same polarity this is considered to mean "0", while if the two plates are of opposite polarity the resistance will be higher and this means "1".

Data is written to the cells using a variety of means. In the simplest, each cell lies between a pair of write lines arranged at right angles to each other, above and below the cell. When current is passed through them, an induced magnetic field is created at the junction, which the writable plate picks up. This pattern of operation is similar to

core memory, a system commonly used in the 1960s. This approach requires a fairly substantial current to generate the field, however, which makes it less interesting for low power uses, one of MRAM's disadvantages. Additionally, as the device is scaled down in size, there comes a time when the induced field overlaps adjacent cells over a small area, leading to potential false writes. This problem, the half-select (or write disturb) problem, appears to set a fairly large size for this type of cell. One experimental solution to this problem was to use circular domains written and read using the giant magnetoresistive effect, but it appears this line of research is no longer active.

1.1.3 FeRAM

Ferroelectric random access memory (FeRAM) is currently one of several advanced nonvolatile memory technologies that are attempting to gain acceptance as an alternative to flash by avoiding its key weaknesses, high program and erase voltages, slow programming speed, write-erase endurance that is limited to ~10^5 cycles. Compared to its primary competitors among the new NVRAM technologies, MRAM and PRAM, FeRAM is more mature with volume production at Fujitsu beginning in 1999. FeRAMs at 1-Mbit densities were available in high volume in 2006 form both Fujitsu and Ramtron. Limited volume production of a 4-Mbit MRAM began at Freescale semiconductor in July 2006, wile PRAM has not yet entered volume production at any manufacturer. However, none of the new NVM comes close to offering neither the high storage densities nor the low cost per storage bit of flash memory. FeRAM is competitive in specialized niche applications where its properties (low write voltage, fast write speed, and much greater write-erase endurance) give it a compelling advantage over flash memory.

A ferroelectric material has a nonlinear relationship between the applied electrical field and the apparent stored charge. Specifically, the ferroelectric characteristic has the form of a hysteresis loop, which is very similar in shape to the hysteresis loop of ferromagnetic materials. The dielectric constant of a ferroelectric is typically much higher that that of a linear dielectric because of the effects of semi-permanent electric dipoles formed in the crystal structure of the ferroelectric material. When an external electrical field is applied across a dielectric, the dipoles tend to align themselves with the field direction, produced by small shifts in the positions of atoms and shifts in the distributions of electronic charge in the crystal structure. After the charge is removed, the dipoles retain their polarization state. Typically binary 0's and 1's are stored as one of two possible electrical polarizations in each data storage cell. For example, in Fig. 1.1 a "1" is encoded using the negative remnant polarization (-P) and a "0" using the positive one (+P).

Operationally FeRAM is similar to DRAM. Writing is accomplished by applying a field across the ferroelectric layer by charging the plates on either side of it, forcing the atoms inside into the "up" or "down" orientation (depending on the polarity of the charge), thereby storing a "1" or "0". Reading is somewhat different than in DRAM. Instead of draining the (non-existent) charge, the transistor forces the cell into a particular state, say"0". If the cell already held a "0", nothing will happen in the output lines, whereas if the cell held a "1" the re-orientation of the atoms in the film will cause a brief pulse of current in the output (as they push electrons out of the metal on the "down" side). The presence of this pulse means the cell held a "1". Note that, like DRAM, reading in FeRAM is a destructive process, and requires the cell to be re-written after reading.

1.1.4 PCRAM

Phase-change memory (also known as PCM, PRAM, PCRAM, Ovonic Unified Memory, Chalcogenide RAM and C-RAM) is a type of non-volatile computer memory. PRAM uses the unique behavior of chalcogenide glass, which can be "switched" between two states, crystalline and amorphous, with the application of heat. Recent versions can achieve two additional distinct states, effectively doubling its storage capacity. PCM cell can be constructed in a number of different ways, but there are two notable methods. In one method, diodes are used as selection elements instead of transistors

This cuts down on cost, since a diode is smaller and cheaper than a transistor. Taking this one degree further, Macronix pioneered cross-point PCM, which is composed simply of a self-aligned chalcogenide cell sandwiched between the address lines (that is, with no transistor or diode selection element). In this manner, the chalcogenide itself serves as the rectifying element so the low-resistance crystalline state is never used. Instead, the cell is manipulated between distinct amorphic states. This type of cell is very low cost since it only requires two masking steps. The greatest challenge for phase-change memory has been the requirement of high programming current density (>10^7 A/cm^2, compared to 10^5-10^6 A/cm^2 for a typical transistor or diode) in the active volume.

1.1.5 RRAM

Resistive random access memory (RRAM) is another candidate for the next generation nonvolatile memory devices. Further introduction on RRAM is in the next section.

1.2 Resistive random access memory

RRAMs make good use of the resistance changes as different memory states. By electrical field or current effects, the conductivity of the memory layer can be switched between high and low resistance reproducibly. The different resistance states stands for different digital states as a memory device. The strengths of RRAM are the high cell density array, high operation speed, low power consumption, high endurance and lower scale limit. Furthermore, RRAMs have the features of nonvolatility, long retention time, and non-destructive readout. In this section, the properties are discussed in view of the structure, fabrication, material classification, operation and circuit realization. By Table 1.1, RRAM have great potential for replacing the flash memory and will become mainstream memory in the future.

1.2.1 Structure and fabrication

The basic structure for RRAM is made up of only metal-insulator-metal, MIM, which can be further integrated into 1D1R (a diode and a resistor), 1T1R (a transistor and a resistor) structures (discussed later), or 1S1R (a switching and a resistor). The top and bottom electrodes could be metals or conducting transition metal oxides, the choice of which has impacts on the resistive switching properties because of their different crystallinities, work functions and the ability of Gibbs free energy. The adhesion and among layers should be considered as well. If high temperature process is needed, the thermal stress problem should be considered. The main character of resistive switching is the insulator layer sandwiched between the electrodes. The insulator for the MIM structure actually may be not really insulating, but also semiconducting, depending on the constitution and stoichiometry. As a result, the

insulator would be called “resistance switching layer” in the following sections. Usual deposition method of resistance switching layer are many and various, including radio-frequency (RF) magnetron sputtering, reactive sputtering, e-beam evaporation, spin coating (sol-gel), thermal oxidation, metal-organic chemical vapor deposition (MOCVD), pulsed laser deposition (PLD), atomic layer deposition (ALD), plasma-enhanced atomic layer deposition (PEALD), and melt-grown by FZ method, as listed in Table 1.2. Among them, the sputtering has lower cost and wide application but poor film uniformity; e-beam evaporation and spin coating has low process cost but poor film quality as well; thermal oxidation are suitable for high reactive metal like Ni, Ti or Cu to form metal oxides and inexpensive; MOCVD, PLD, ALD, and PEALD are able to produce high quality film with good step coverage but expensive; the FZ method is able to fabricate perfect crystals with exact component proportion but not practical in semiconductor fabrication process. The different quality deposited by different methods has connection with the resistive switching characteristics.

1.2.2 Material classification

The resistive switching phenomena have been found in many materials. The research mainstream is focused on several groups, including binary oxides, perovskite oxides, manganites, and other alloy or polymers.

The binary oxides adopted in RRAM application, such as Cu_xO [1-16], TiO_2 [17-32], NiO [23-53], ZrO_2 [17-26] Al_2O_3 [66-68], HfO_2 [69,70], Fe_2O_3 [71], ZnO [72,73] and MoO_x [74], are candidates or have been widely used in other field of CMOS devices. Thus the compatibility with modern CMOS process would not be a problem. Moreover, this material group of binary oxides has simpler element components. It is easier to control the proportion of metal and oxygen elements.

Another extensively studied material group is $(Ba,Sr)(Zr,Ti)O_3$, BSZT. It has been studied as a role of the high-k dielectric for a long time [75]. Many BSZT in RRAM are doped with V [76], Cr [77,78], etc. Dopants are prone to occupy sites of intrinsic oxygen vacancies, and thus restrain the formation of them [76]. Because of the more components and the more complicated chemical environment, the control of the component proportion is not as easy as that of binary oxides.

The manganites discussed in RRAM usually represent the carrier-doped manganites with perovskite structure, $R_{1-x}A_xMnO_3$, where R and A are rare-earth and alkaline-earth ions, respectively [79-84]. They are not classified in the above perovskite system here because of their unique characteristics of conducting ferromagnets below a Curie temperature [79]. Manganites with perovskite structures exhibit a magnetoresistive response that is many orders of magnitude larger than that found for other materials, beside the electrical resistive switching behaviors. It is the epitaxial samples that are generally prepared by PLD [81,83] or floating-zone melt-growth method [79] to obtain the precise element proportion and physical properties. For the same reason of perovskite oxides, the future for manganites in RRAM is not so promising.

The other materials such as chalcogenide (GeSbTe) [85], sulfides (e.g. $Cd_{1-x}Zn_xS$ [86]), and organic materials including Rose Bengal sodium salt (RB) [87], copperphthalocyanine (CuPc) [88], 2-amino-4,5-imidazole dicarbonitrile (AIDCN) [88] and so on, have been investigated for RRAM application. The chalcogenide material has been drawing many attentions recently due to Intel's support, while the others are newly introduced to semiconductor processes. Besides, many organic polymers tend to degrade easily. Chalcogenide seems a more practical candidate in

this group of materials.

1.2.3 Operation and circuit realization

Basic operation of bistable resistive switching in a single cell can be achieved by DC sweep or pulse switching methods. Fig. 1.2 shows a typical *I*-*V* plot under DC sweep operation. Assuming the resistance state is first held in off state (high resistance state), the current suddenly increases as the DC bias sweeps toward positive direction and on state (low resistance state) is reached, which is defined as a process of "switch on" or "set" as indicated in the figure. The voltage where the current suddenly increase is the switch-on voltage. Then a negative voltage bias is applied to switch back to off state with a substantially current drop at the switch-off voltage, as indicated by the "reset" or "switch off" in the figure. It should be noted that this operation requiring different voltage polarities to switch on and off, whether positive on/negative off or positive off/negative on, is called bipolar operation. As for the unipolar operation, either polarity can be applied to switch on or off depending on the present memory state. On the basis of *I*–*V* characteristics, the switching behaviors can be classified into two types: unipolar (nonpolar) and bipolar, for which typical *I*–*V* curves are shown in Figs. 1.3a and 1.3b, respectively For the data reading operation, the bias should not exceed the range indicated as "read" in the figure to prevent memory state modification. Fig. 1.2 does not show the forming process required to initiate the resistive switching properties of as-deposited oxide films. The forming process is similar to soft oxide breakdown, leading to the conducting paths (filaments) composed of clusters of point defects. To unify and clarify the terms of operation parameters in the following text, the "switch on" and "switch off" would be used to describe the switching operation instead of "set" and "reset"; "V_{set}", "V_{reset}", "R_{on}" and "R_{off}" instead of "switch-on voltage", "switch-off voltage", "on-state resistance"

and “off-state resistance”.

In the real circuits, it is the pulse switching that is the practical operation method for its fast operation speed and lower power consumption. The waveforms of switching on and off are shown in Fig. 1.4(a) and (b) respectively. The pulse heights and widths for switch on and off must strike a balance, in which the larger the pulse heights are, the shorter the pulse widths are needed. The reading pulses with small pulse heights are designed not to modify the memory states. This non-destructive readout property can be examined by the stress test, in which memory device samples are stressed by a small voltage bias for a long period and the details are described in chapter 2.

For the memory cell array, 1D1R, 1S1R, 1T1R structure as show in Fig. 1.5-9 must be used to prevent misreading as shown in Fig. 1.7. I. G. Baek *et al.* [33] reported that if a cell is in off state and its neighboring cells are in on state, it will be misread as on state because of the leakage current path around its neighboring cells. Therefore a rectifying element is required for each cell in an array to confine the current paths. The minimum sizes for 1D1R and 1T1R structures are $4F^2$ and $6F^2$ respectively, which meet the requirement for high density arrays.

1.3 Conducting mechanisms in oxides

Based on conductivity, transition metal oxides could be insulator, semiconductor or metal depending on the composition of the oxide materials. Hence the conducting mechanisms may vary because of their different physics and chemistry. The most discussed materials in RRAM application generally belong to insulator or

semiconductor according to the constitution and stoichiometry, and the electron conduction mechanisms mostly involved are Ohmic conduction, space charge limited current, Schottky emission, and Frenkel-Poole emission. Furthermore, it is the current fitting procedure that gives insight into the conduction mechanisms.

1.3.1 Ohmic conduction

Ohmic conduction takes place when the injected carrier density is far less than the thermally-generated carrier density. Generally, it applies to the condition of low electric field region in which thermally-generated carriers are dominant in conduction. The current-voltage characteristics follow Ohm's law that the current passing through a resistor from one terminal to the other is proportional to the voltage drop across the two points. In addition, the temperature effect is also described in Ohmic conduction behavior. Due to the electron and phonon scattering effects, the conductivity rises with increasing temperature for conduction in semiconductor, while with decreasing temperature for metal conduction. The following is the expression for Ohmic conduction:

$$J = aV \exp\left(-\frac{c}{T}\right)$$

where a and c are constants respectively, and V the applied voltage.

1.3.2 Space charge limited current

The mechanism of space charge limited current (SCLC) is attributed to defects and usually exists in the dielectric stressed by high electric fields. After charge injection from an electrode, the space charge may form if the charge carriers are trapped and distributed over a region of area without being neutralized. The further flow of charge carriers would be impeded by this space charge region. It should be

noted that the injected carriers are mostly electrons. As for conductive media, the trapped carriers are able to be neutralized or screened rapidly; therefore the space charge region would not form.

The complete trapped controlled SCLC mechanism is composed of two stages [24], trap-unfilled SCLC and trap-filled SCLC, both can be written as the following expression:

$$J = \left(\frac{\theta}{\theta + 1} \right) \frac{9}{8} \varepsilon_r \varepsilon_0 \mu \frac{V^2}{L^3}$$

where J is the current density, θ is the ratio of free electron to trapped electron, N_C is the effective density of states in the conductive band, N_t is the number of emptied electron traps, ε_0 is the permittivity of free space, ε_r is the static dielectric constant, μ is the electron mobility, V is the applied voltage and L is the film thickness. At first stage, the traps are not filled with charges and the formula can be rewritten with $\theta << 1$ as the following:

$$J = \theta \frac{9}{8} \varepsilon_r \varepsilon_0 \mu \frac{V^2}{L^3}$$

As the voltage increases, the majority of traps are occupied by the injected carriers, and the current-voltage characteristics can be again rewritten with $\theta >> 1$:

$$J = \frac{9}{8} \varepsilon_r \varepsilon_0 \mu \frac{V^2}{L^3}$$

1.3.3 Thermionic emission & Drift-Diffusion current

Schottky emission is mainly attributed to the Schottky contact of the metal-insulator interface. For the carriers to transport, they must jump across the barrier height of one of the interfaces, travel through the dielectric film, and eventually reach the other side. It is the thermionic emission that enables the carriers

(mostly electrons) to overcome the interface barrier height. Therefore temperature is the key factor that energetic carriers (hot carriers) are easier to jump across the barrier. Crowell and Sze discussed the metal-semiconductor contact by using a thermionic emission-diffusion theory with two parameters, recombination velocity ν_R and effective diffusion velocity ν_D []

$$J = \frac{qN_C\upsilon_R}{1+\upsilon_R/\upsilon_D}\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_0\varepsilon_r}\right)}{kT}\right] \quad \text{.....(1.3.3.1)}$$

where J is the current density, Φ_b the Schottky barrier height, ε_0 is the permittivity of free space, ε_r is dynamic dielectric constant, E is electric field, q is electronic charge, and k is Boltzmann constant. The recombination velocity ν_R and diffusion velocity ν_D are given by, respectively

$$\upsilon_R = \frac{A^*T^2}{qN_C}$$

$$\upsilon_D = \mu E$$

where A^* denotes Richardson constant, μ is mobility.

If $v_D \gg v_R$, Eq. 1.3.3.1 is dominated by the recombination velocity ν_R and is identical with the conventional Schottky equation, The formula of Schottky emission is expressed as below:[89]

$$J = A^*T^2\exp\left(\frac{-q(\phi_b - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}}{kT}\right)$$

If $v_D \ll v_R$, Eq. 1.3.3.1 is dominated by ν_D and becomes the modified Schottky equation as:[89]

$$J = qN_C \mathrm{E}\mu \exp\left[\frac{-q\left(\varphi_B - \sqrt{q\mathrm{E}/4\pi\varepsilon_0\varepsilon_r}\right)}{kT}\right]$$

1.3.4 Frenkel-Poole emission

Frenkel-Poole emission is pretty much similar to Schottky emission mechanism. The main differences are that Frenkel-Poole emission describes the process for carriers to overcome the barriers resulted from the defect states in the dielectric material, and the barrier lowering is twice as large as that in Schottky emission mechanism. This is because trapped charge is fixed not like image charge in the metal. Temperature is also crucial for this carrier transportation process, while electric field plays a more important role in this mechanism than in Schottky emission, which suggests that field effects have greater impact on defect-related behavior. The current-voltage relationship can be written as the following formula:

$$J = qnE \exp\left(\frac{-q(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_0}}{\gamma kT}\right)$$

where n is carrier concentration, E is electric field, Φ_t the trap level, and other parameters are the same as those in Schottky emission.

When $\gamma = 1$ is called Normal Poole-Frenkel effect. This case is suit for compensation semiconductor. For N-type semiconductor, the electron concertration is $n \approx \left(\frac{N_D - N_A}{2N_A}\right) N_C \exp\left[-\frac{(E_C - E_D)}{kT}\right]$.

When $\gamma = 2$ is called Modified Poole-Frenkel effect. This case is suit for complete ionization semiconductor. The $\gamma = 2$ is due to the carrier concentration of the complete ionization semiconductor. For N-type semiconductor, the electron concertration is $n \approx \sqrt{\frac{N_A N_D}{2}} \exp\left[-\frac{(E_C - E_D)}{2kT}\right]$.

It is worth nothing that there are difference in exponent term between the Thermionic emission and Frenkel-Poole emission. Although the restoring in both effect is due Coulomb interaction between the escaping electron and positive charge is fixed for Frenkel-Poole emission but mobile with Thermionic emission, as Fig 1.10 illustrates.[30]

1.4 Models of resistive switching mechanisms

The switching mechanism of RRAM can be classified according to whether the dominant contribution comes from a thermal effect, an electronic effect, or an ionic effect. The electronic effects have three model to explain switching mechanism, respectively, Schottky barrier modulation, Carrier trapping and detrapping relation with SCLC and Metal-insulator transition. The ionic effects have two class model, one is Solid-state electrolyte (SSE), another is Oxygen vacancies migration. Each model may be applied for some combinations of electrodes and oxide materials. Many models, however, are derived by indirect observation or electrical measurements. Consequently, the switching mechanisms are still under debate due to the lack of direct evidence.

1.4.1 Thermal effect

A typical resistive switching based on a thermal effect shows a unipolar (independent polarity) characteristic. It is initiated by a voltage-induced partial dielectric breakdown in which the material in a discharge filament is modified by Joule heating. Because of the compliance current, only a weak conductive filament with a controlled resistance is formed.

This filament may be composed of the electrode metal diffused into the insulator, decomposed insulator material such as sub-oxides. During the reset transition, this conductive filament is again disrupted thermally because of high power density, similar to a traditional household fuse but on the nanoscale. Hence, we refer to this mechanism as the fuse–antifuse type. One candidate out of many is NiO. Recently, the filamentary nature of the conductive path in the ON state has been confirmed for NiO and TiO_2. Cells based on Pt/NiO/Pt thin films have been successfully integrated into CMOS (complementary metal oxide semiconductor) technology to demonstrate non-volatile memory operation. A critical parameter for this unipolar switching effect seems to be the value of the compliance current. In fact, it has recently been demonstrated that a TiO_2 thin film shows bipolar switching, and that this can be changed to unipolar switching characteristics by setting the compliance current to a larger value.[90]

1.4.2 Electronic effect

The electronic effect can be class to trapping type and electron correlation type. The former is resistive switching by trapping and setrapping at interface to modulate schottky barrier profile, or trapping electrons to change current magnitude. The latter is switching by changing electrons Coulomb repulsion.

1.4.2.1 Schottky barrier modulation

A Schottky contact is formed at the interface of low work function metal and p-type semiconductor, and high work function metal and n-type semiconductor, respectively. The barrier height determines the conductivity in these systems and can be modulated by interface states, which are charged (discharged) after the injection (ejection) of electrons. It is this interface state pinning effect that modifies the Fermi

level position and the barrier height, and consequently controls the resistive switching properties.

The switching behavior can be understood by a model for the interface considering the Schottky contact with charge-trapping interface states. This mechanism is below interface effect. The mechanism of the resistance switching was explained by the change of the Schottky barrier width at interface caused by a polarity alternation of a space charge. In the forming process, the possible cause is the electrochemical migration of oxygen atoms.

Sawa et al [83] propose interface-state-induced band bending picture, and Ti electrode is a getter for oxygen. The high density of the interface states induced by the oxygen vacancies may cause a large degree of the band bending at interface. However, the electrode of the almost same work function, have not resistive switching property.

1.4.2.2 Charge trapping and detraping model

The charge trapping and detraping model is wide-spreading especially in the material system of manganites [54-58] and perovskite oxides [70-73]. It is also applied to some binary oxides such as ZrO_2 [21,23,24] and Cu_xO [1-5]. This model can be further classified into two types in accordance with the distribution of traps, the interface-controlled and the bulk-controlled. The schematics for both mechanisms are illustrated in Fig. 1.12 and 1.13 respectively [63].

For interface-controlled trapping and detraping model, the Schottky barrier and the interface state at the interface of the electrodes and the oxide are discussed in 1.4.2.1. On the other hand, the bulk-controlled trapping and detraping model is ruled by the defect states playing a role of trapping centers in the oxide bulk. The most

common case is traping and detraping carrier with SCLC as showing Fig 1.14. When the defect states are empty, the carriers are captured by these trapping centers and make little contribution to current conduction. After all the states are occupied, the carriers would be free to drift through the oxide. Besides, the occupied defect states create an internal field that increases the bend banding (voltage drop) across the film, and further reduces the barrier height near the interface. Hence the resistance change is dominated in the bulk defect states. Generally the resistance ratio in samples of the bulk-controlled model is usually larger than that of interface-models because of greater conductivity difference between conducting (on) and insulating (off) states.

One of the major differences between trap and ionic effect is observed in current-voltage characteristics. There are two manners to distinguish from these mechanisms. First, the change of current magnitude is relatively smooth at V_{on} and V_{off} in the trap-model predominant samples compared to those of ionic effect. This would be attributed to the different nature of gradual trapping/detraping and abrupt conducting path formation/rupture processes respectively. Second, the drap model with SCLC have self-compliance phenomenon, but ionic effect to form filament does not. It should be noted that even the similar materials have different possible mechanisms because of the slight difference in the preparation process or chemical and physical properties, such as Cr:$SrZrO_3$ reported in [66] (filament) and [70] (trap), and ZrO_2 in [26] (filament) and [21] (trap), etc.

1.4.2.3 Mott transition

A Mott transition is a metal-insulator transition in transition metal oxide. It is an example where the theory of the Landau liquid does not apply anymore. Due to electric field screening the potential energy becomes much sharper (exponentially)

peaked around the equilibrium position of the atom and electrons become localized and can no longer conduct a current. Mott transition arise strongly correlated electron system (SCES)—a group of materials in which the effect of Coulomb repulsion is large. A prototype of theoretical understanding for the transition between the Mott insulator and metals was achieved by using simplified lattice fermion models, in particular, in the celebrated Hubbard model (Anderson,1959; Hubbard, 1963, 1964a, 1964b; Kanamori, 1963). The Hubbard model considers only electrons in a single band. Its Hamiltonian in a second-quantized form is given by

$$\hat{H} = t\sum_{\langle i,j\rangle}(\hat{a}_{i\uparrow}^{+}\hat{a}_{j\uparrow} + \hat{a}_{i\downarrow}^{+}\hat{a}_{j\downarrow}) + U\sum_{i}\hat{n}_{i\uparrow}\hat{n}_{i\downarrow}$$

where the creation (annihilation) of the single-band electron at site I with spin σ is denoted by $a_{i\sigma}^{\dagger}(a_{i\sigma})$ with $n_{i\sigma}$ being the number operator $n_{i\sigma} \equiv a_{i\sigma}^{\dagger}(a_{i\sigma})$.

Metal-insulator phase diagram is based on the Hubbard model. The shaded area is in principle metallic but under the strong influence of the metal-insulator transition, in which carriers are easily localized by extrinsic forces such as randomness and electron-lattice coupling. Two routes for the MIT are shown: the filling-control MIT and the bandwidth-control MIT. As shown in Fig. 1.15.

This type of transition-metal oxide in which ε_d-ε_p is assumed to be larger than U_{dd} is called a Mott-Hubbard-type compound. Because of $U_{dd}<|\varepsilon_d-\varepsilon_p|$, the charge gap in the Mott insulating phase is mainly determined by U_{dd}. In contrast, if $|\varepsilon_d-\varepsilon_p|$ is smaller than U_{dd}, the charge excitation in the Mott insulating phase is mainly determined by the charge transfer type where an added hole in the Mott insulator

mainly occupies the oxygen p s band. The difference between these two cases is schematically illustrated in Fig.1.16.

Figure 3.. H. Inoue et.al propose a mechanism for unipolar resistance switching in metal-insulator-metal sandwich structures. The commutation from the high to low resistance state and back can be achieved with successive voltage sweeps of the same polarity. Electronic correlation effects at the metal-insulator interface are found to play a key role to produce a resistive commutation effect in qualitative agreement with recent experimental reports on binary transition metal oxide based sandwich structures. [93-95]

1.4.3 Ionic effect

1.4.3.1 Solid-state electrolyte (SSE)

Solid-state electrolyte (SSE) is an emerging technology in RRAM technology. As implied by the name, the solid-state electrolyte provides a medium for metal ions to flow without being involved with any oxide breakdowns or the change in the medium structure. The basic structure for SSE RRAM is also metal-insulator-metal, MIM, with the top electrode of a more reactive metal, the insulator of an SSE, and the bottom electrode of a stable inert metal. As shown in Fig. 1.17, with a positive bias applied on the top metal, the oxidized reactive ions would penetrate into the SSE film, forming a conducting bridge and reach low resistance on-state. In the switching off process, the same or reverse bias polarity can be applied by the mechanism of Joule heating or electrochemical reaction, depending on the magnitude of switching voltages and currents and the strength of conducting bridge [49]. Due to the nature of ion diffusion, many of the concepts are common as mentioned in the filamentary model.

The main concern for this type of RRAM is the choice of ion/SSE medium combination, in which the combinations of Cu/SiO_2 [49], Cu/WO_3 [74], Cu/Ta_2O_5 [75], Cu/GdO_x [76], Ag/chalcogenide [77], and Ag/TiO_2 [78] have been proposed. The ion mobility in the medium is an essential property for switching speed [49]; the fast ion transport media, however, have potential problems in terms of retention because the conducting ion paths having been formed may be ruptured easily by the fluctuation of thermal or electrical effects [76]. Therefore the SSE of dual layer has been introduced, as shown in Fig. 1.18. The first layer provides a fast transport medium for the ions and is an ion activated layer of an ion source; the second layer is very thin and the ions have lower mobility in it, which improve the switching speed and the retention concern.

1.4.3.2 Oxygen vacancies migration

The oxygen deficient region (filaments) of a film is much more conducting than the stoichiometric region irrespective of whatever the defect type is. Generally the mobility of oxygen ions in binary oxides is much higher than metal ions, and the formation of the filaments could be induced by the rejection of O^{2-} ions [21,31]. During the filament formation process, it is the electrical field effect that takes an essential part, because the insulating parts among the filaments are stressed by the highest electrical field accompanied with point discharge effect. As for the filament rupture, it is the current-induced effect that rules the process in which Joule heating effect resulting from the current flow through the tiny filaments generates heat and raises temperature up to hundreds of degree Celsius at the local spot [68,69], providing enough energy for oxygen ions to reflow and making the conductive regions of non-stoichiometry return to insulator to rupture the filaments. Due to the stochastic formation and rupture process, the variations in the switching parameters

(V_{on}, V_{off}, R_{on} and R_{off}) are inevitable. Well-designed structures may improve these variations, as proposed by I. G. Baek *et al.* [28] and D. C. Kim *et al.* [30], that the size shrinking of cell area and the improvement at the interface between the electrodes and oxide film help confine the numbers and location of the filaments respectively, as shown in Fig. 1.8 and 1.9, and hence reduce the variation of switching on/off parameters.

Recently, the concept of tree-shaped filament structure has been proposed [20,23]. The breakdown paths (filaments) are formed in a dielectric when the carriers are injected from a local point at the electrode interface. The initial cross-sectional area of the path for the carrier conduction is quite narrow, but with the propagation of the filaments the cross section largely increases by an increasing number of secondary formed paths. Therefore the region near the cathode might contain filaments with a larger conductivity compared to the region near the anode [20]. To be more specific, it is very likely that the filament is thick at the cathode and thin at the anode if merely considering a single filament, which matters in terms of conductivity and has impact on Joule heating effect. It is at the thinnest part of a filament near the anode that most thermal energy accumulates and the filament formation and rupture occur. Experiments reported by K. M. Kim *et al.* show that only 3 ~ 10 nm of the filaments near the anode dominates the switching [23], and the schematics are shown in Fig. 1.20. Other experiment using infrared thermal microscopy gives further evidence for this model [78]. The infrared thermal micrograph of a Cr:$SrTiO_3$ single crytal is shown in Fig. 1.21, which depicts the confinement of the current path during 5-mA current load and a hot spot near the anode electrode, confirming that in the anode region the heat energy accumulates and the filament is probably thinner compared to that in the cathode region.

Function	DRAM	SRAM	Flash	OUM	MRAM	RRAM
Non-volatility	No	No	Yes	Yes	Yes	Yes
Program power	Low	Low	High	Low	High	Low
Program voltage	Lo1	Lo1	High		Medium	Low
Read dynamic margin	100-200mV	100-200mV	Delta Current	10X – 100X	20 – 40%	10X – 1000X
Write - Erase time	50ns - 50ns	8ns - 8ns	1μs – 1-100ms	10ns - 50ns	30ns - 30ns	10ns - 30ns
Read time	50ns	8ns	50ns	20ns	30ns	20ns
Program energy	Medium	High	High	Low	Medium	Low
Multi-bit storage	No	No	Yes	Yes	No	Yes
Scalability limits	Capacitor	6T	T-Ox/HV	Litho	Current	Litho
Endurance	∞	∞	10^{12}	$>10^{12}$	$?10^{15}$	$?10^{15}$
Cell size (F^2)	6-12	50-80	7-11	5-8	?	4

Table 1.Comparison of various memories

Preparation method	References
RF magnetron Sputter	ZrO_2[22], NiO[33,38], Cu_xO[41], Fe_2O_3[44], RAMO[54], BSZT[51,52]
Reactive sputter	TiO_2[9], ZrO_2[18,21], NiO[27,34,36]
E-beam evaporation	ZrO_2[23,24], NiO[37]
Spin-coating	TiO_2[14,16]
Thermal oxidation	TiO_2[11-13], NiO[31,32], Cu_xO[39,40,42,43]
MOCVD	TiO_2[1]
ALD	TiO_2[4]
PEALD	TiO_2[5,7,8]
PLD	ZrO_2[20], RAMO[55,57,58], BSZT[70-73]
Melt-grown (FZ)	RAMO[53,56]

RAMO: $R_{1-x}A_xMnO_3$

BSZT: $(Ba,Sr)(Zr,Ti)O_3$

Table 1.2. List of preparation methods of resistance switching layer.

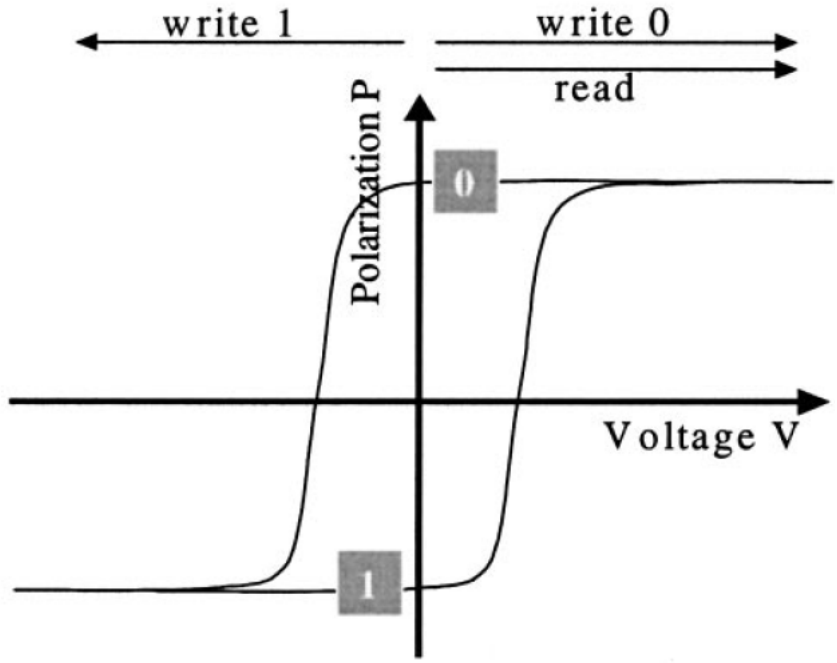


Figure 1.1. Typical polarization vs. voltage hysteresis of a ferroelectric material. [82]

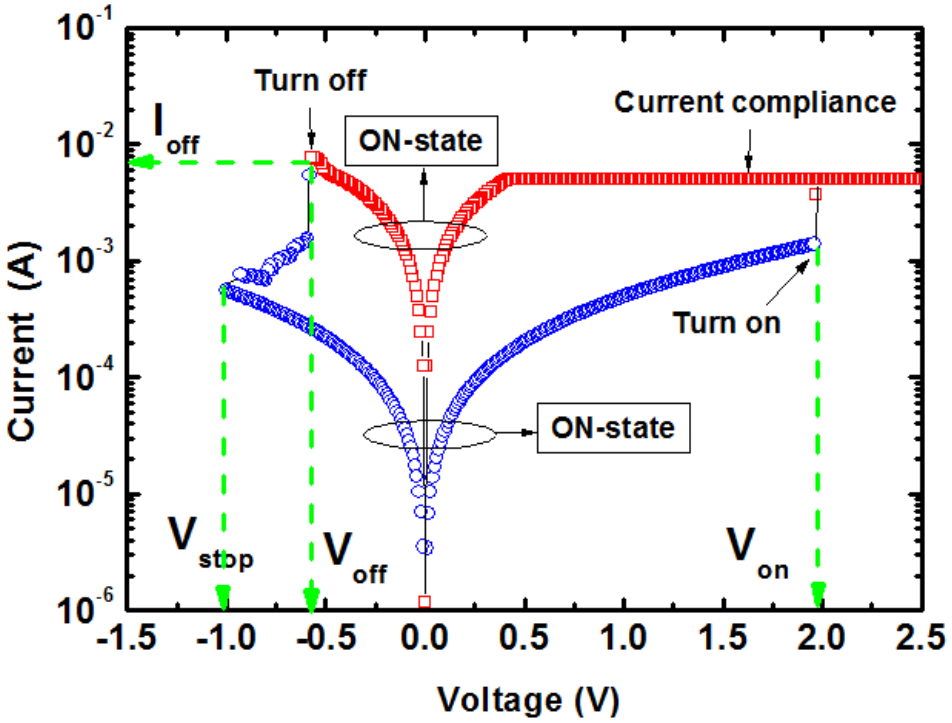


Figure 1.2. Typical *I-V* curves of RRAM switching in voltage sweeping mode.

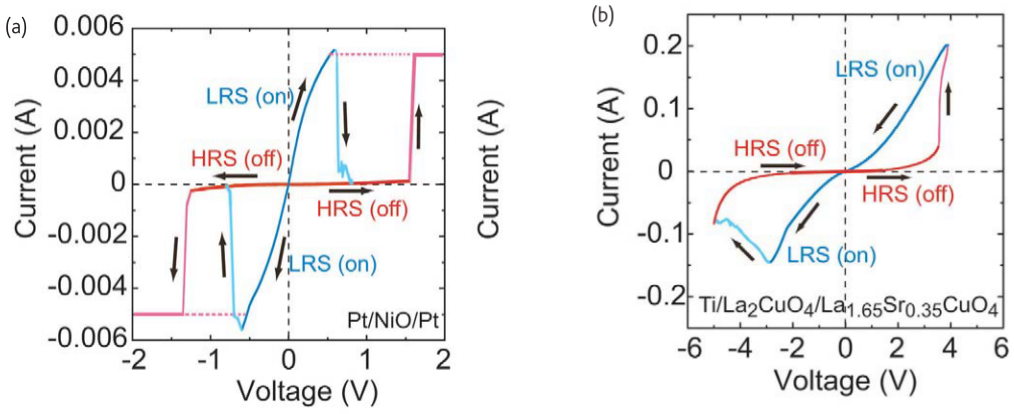


Figure 1.3. (a) Nonpolar (unipolar) switching (b) Bipolar switching. [98]

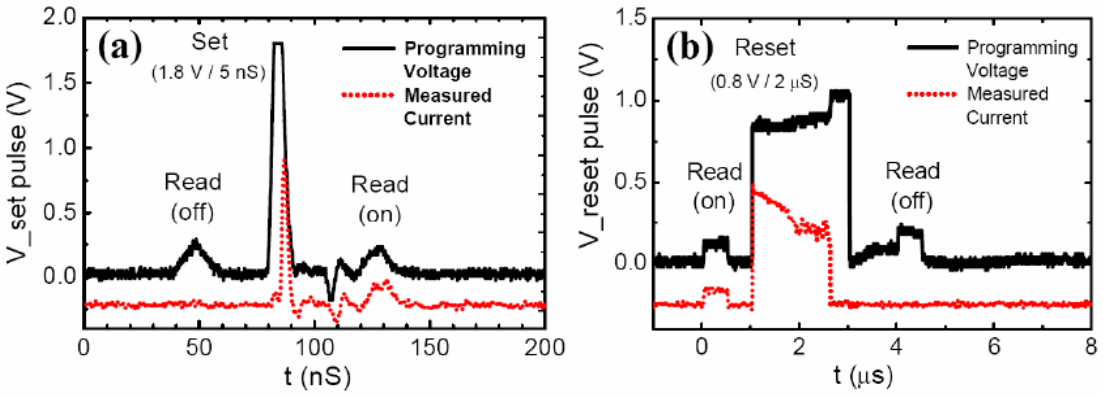


Figure 1.4. Switching dynamics monitored with programming and reading pulses. Pulse waveforms and transition for (a) switch on and (b) switch off. [33]

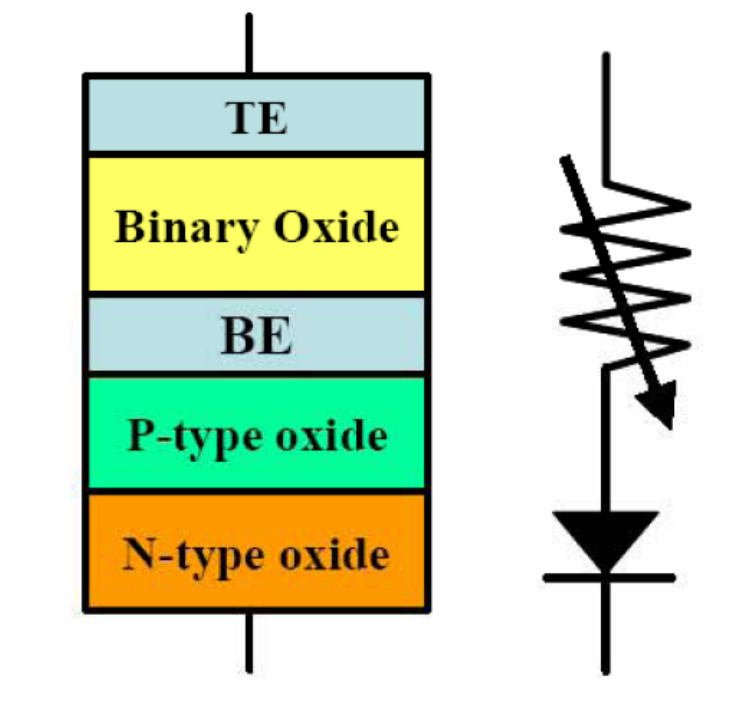


Figure 1.5. Conceptual schematic of 1D1R structure. [40]

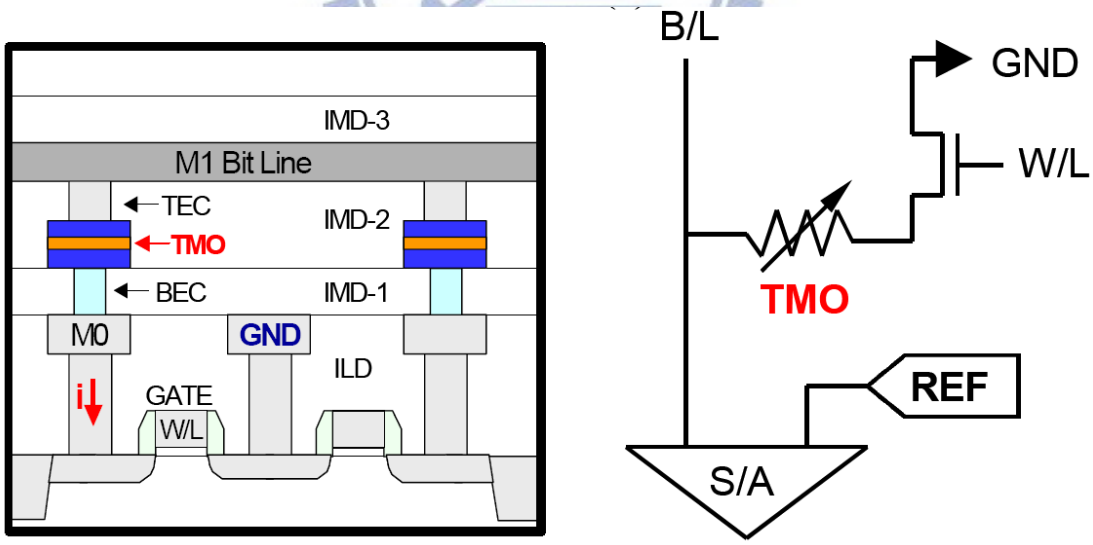


Figure 1.6. Cross-sectional schematic and basic circuit diagram of 1T1R structure. [24]

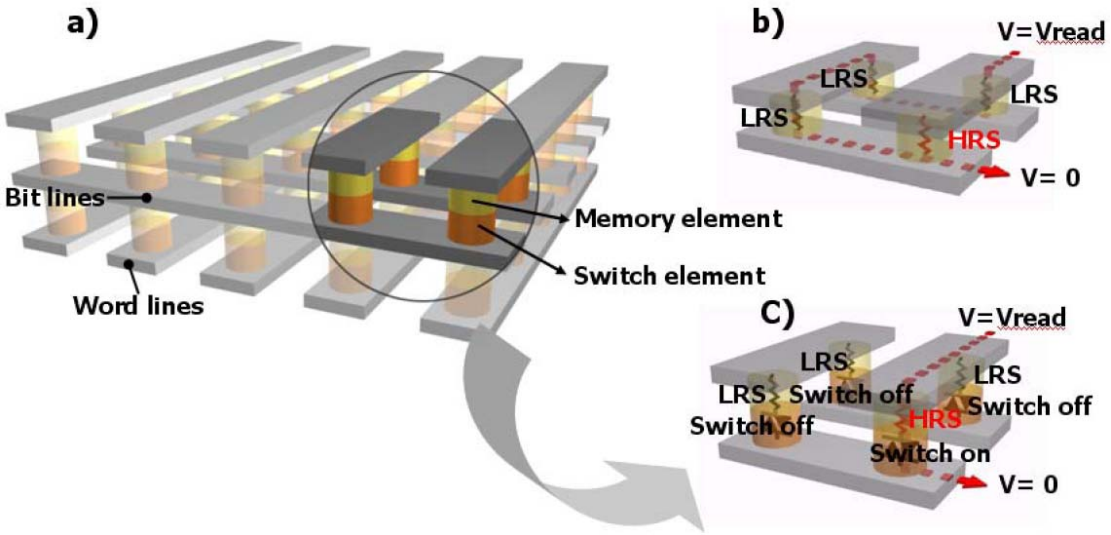


Figure 1.7. (a) Generalized cross-point structure with memory and switching elements. (b) Reading interference without switch elements. (c) Rectified reading operation with switch elements. [40]

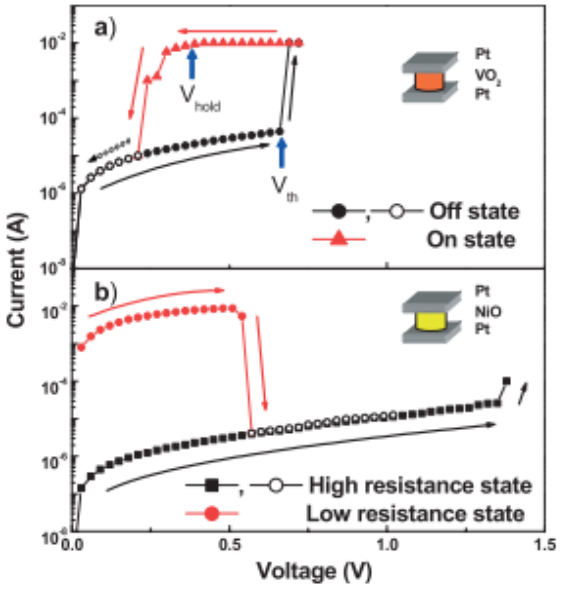


Figure 1.8. (a) Threshold switching of a Pt/VO_2/Pt switch element and (b) Bistable resistance switching demonstrated for a Pt/NiO/Pt memory element. [91]

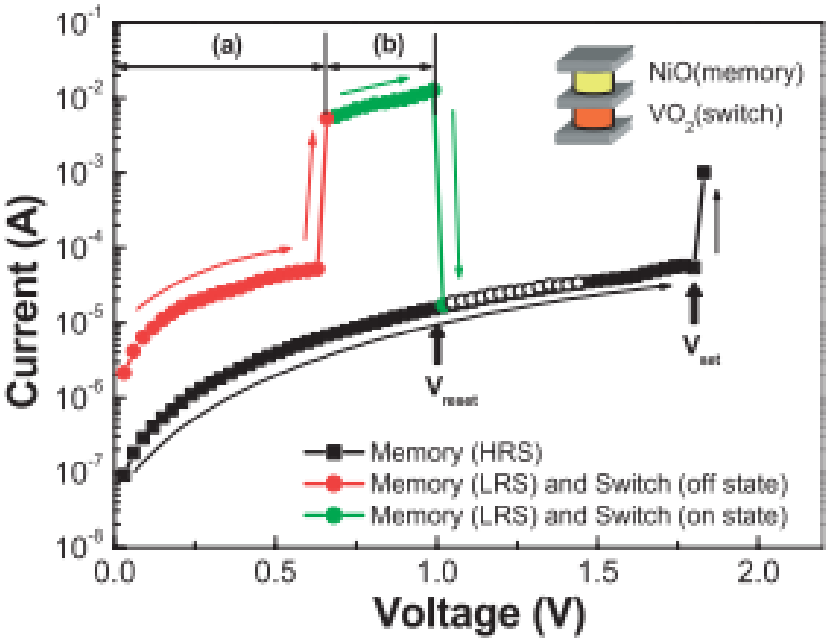


Figure 1.9. Programming characteristics of combined oxide switch and oxide memory elements. [91]

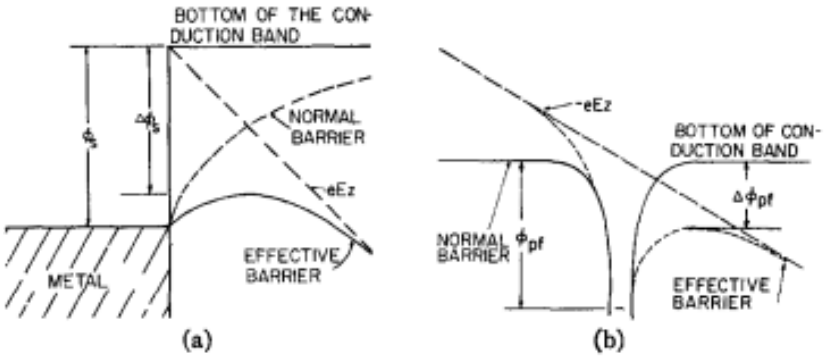


Figure 1.10. (a)The Schottky effect. (b)The Frenkel-Poole effect. [30]

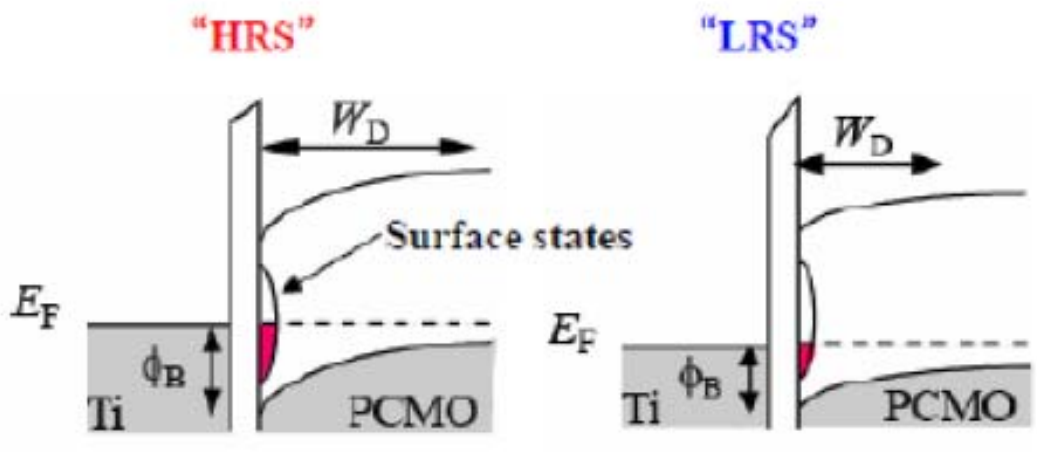


Figure 1.12. Band diagram with the conditions of interface states for on state (LRS) and off state (HRS), respectively. [63]

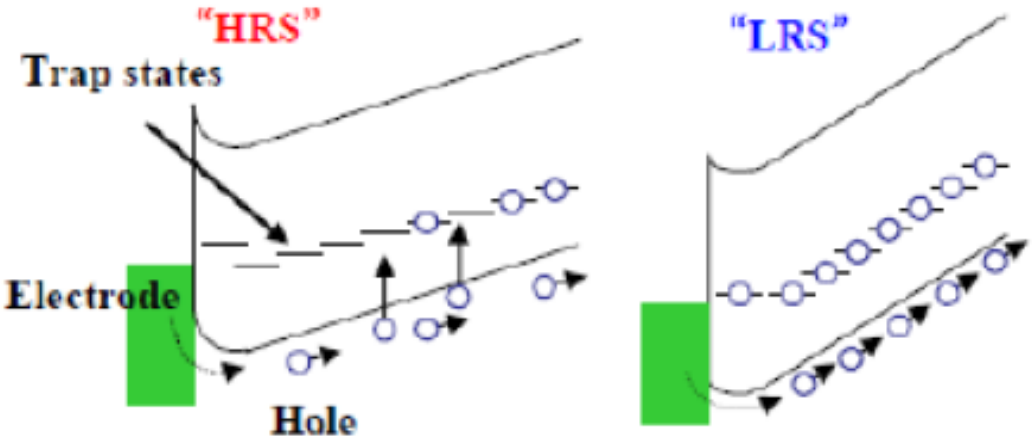


Figure 1.13. Band diagram with the condition of bulk traps for on state (LRS) and off state (HRS), respectively. [63]

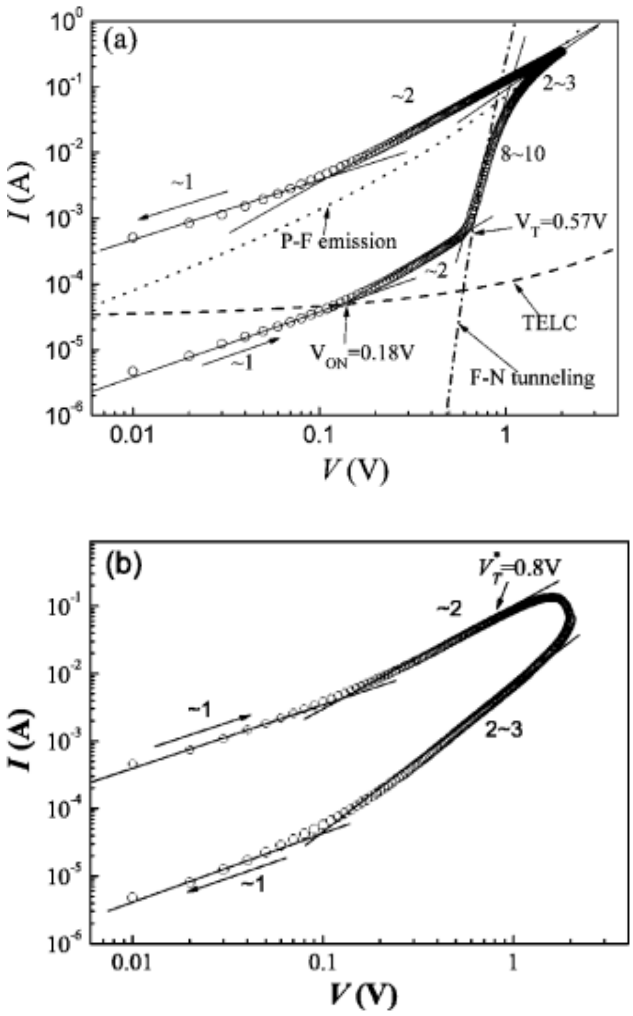


Figure 1.14. I-V characteristics of a Ag/La0.7Ca0.3MnO3 /Pt heterostructure (a) The set process (b) The reset process. [84]

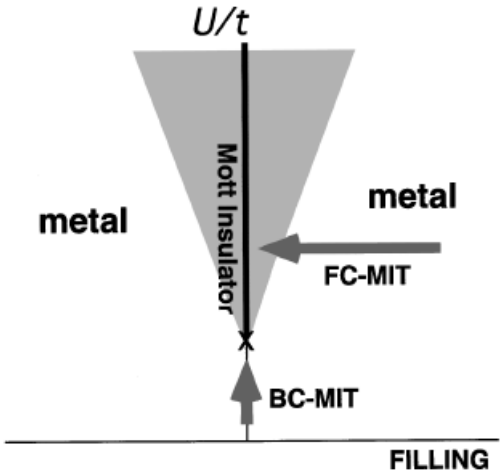


Figure 1.15. Metal-insulator phase diagram based on the Hubbard model in the plane of U/t and filling n. Two routes for the MIT (metal-insulator transition) are shown: the FC-MIT (filling-control MIT) and the BC-MIT (bandwidth-control MIT). [92]

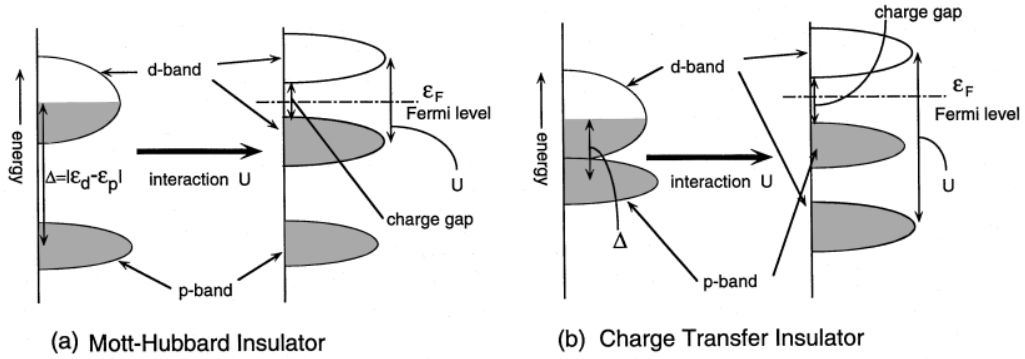


Figure 1.16. Schematic illustration of energy levels for (a) a Mott-Hubbard insulator and (b) a charge-transfer insulator generated by the d-site interaction effect. [92]

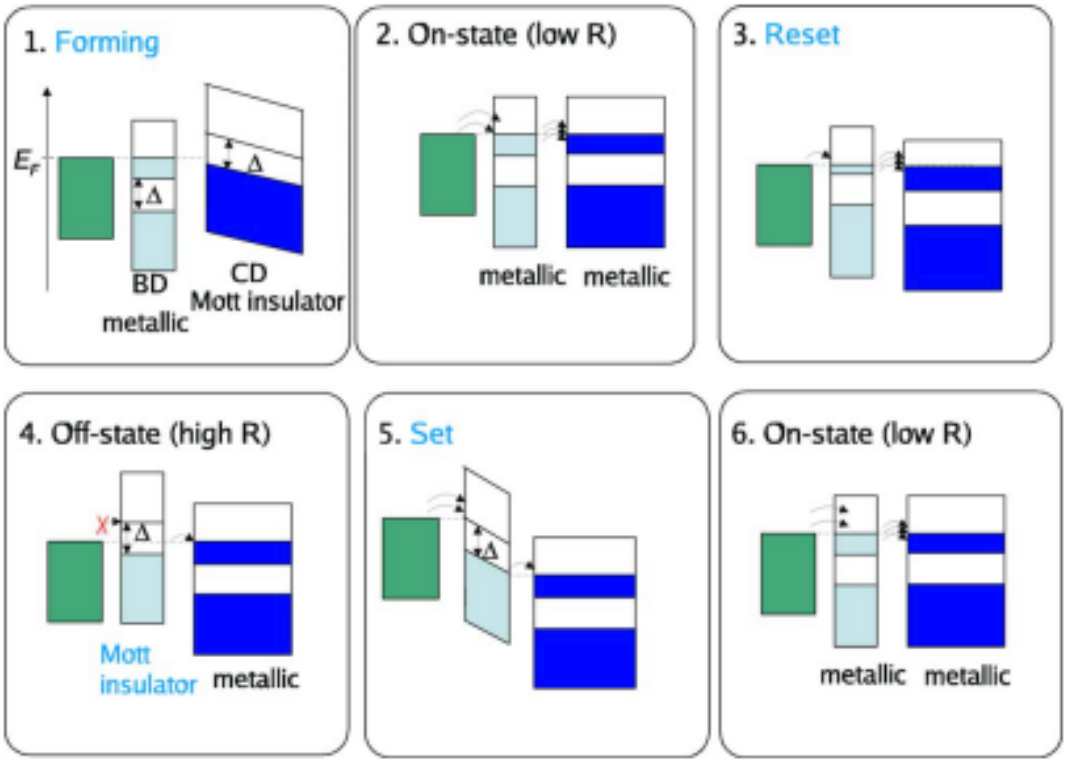


Figure 1.17.The interface Mott transition, Schematic steps of the unipolar resistive switching process. [95]

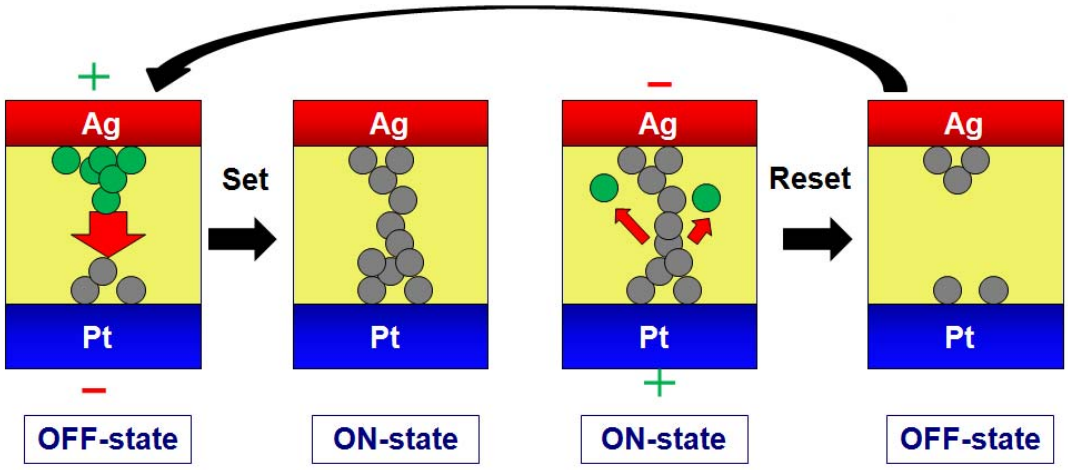


Figure 1.18. The set and reset process of the Solid-state electrolyte (SSE). The green ball represent Ag^{+} ion, the grey ball represent Ag atom. The red arrow represent the direct of the ion.

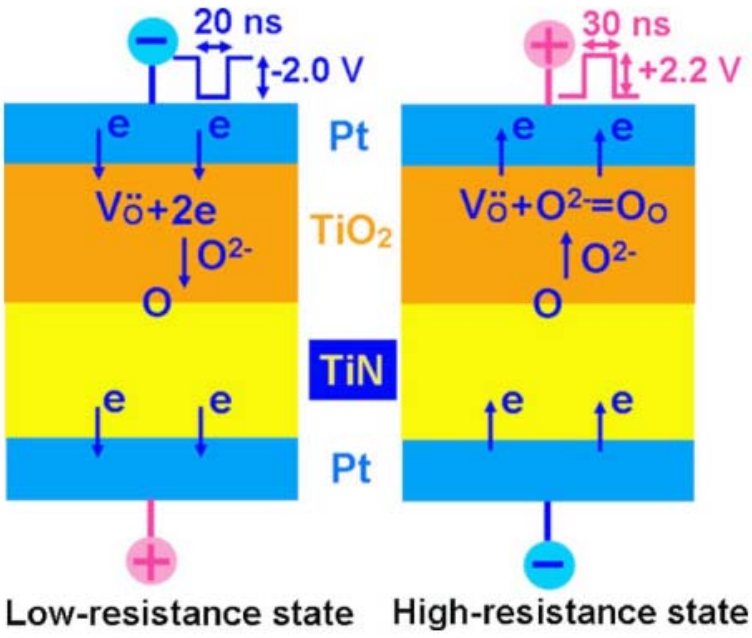


Figure 1.19. Schematic pictures of high- and low-resistive state of the specimen. [28]

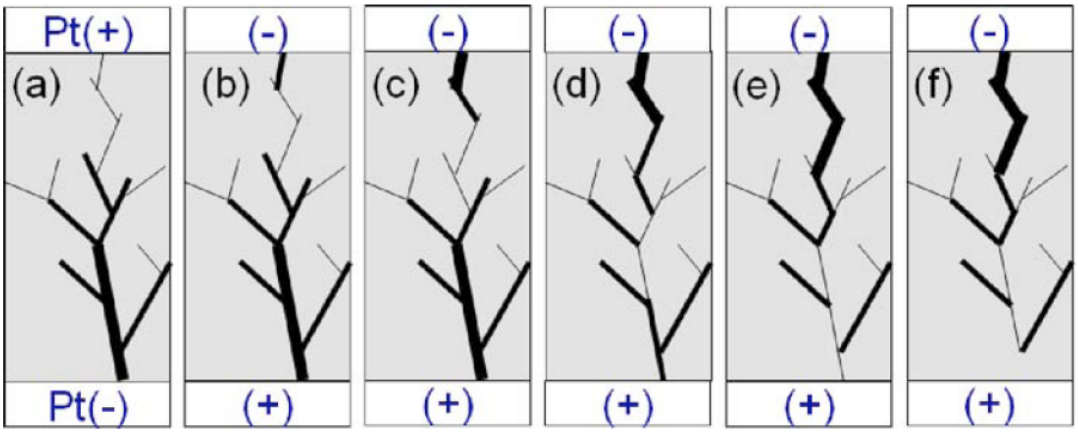


Figure 1.20. Schematic diagram for switching from on state to off state. (a) On state formed by positive bias on TE. [(b)-(e)] Nucleation and propagation of a filament when negative bias is applied on TE. (f) Off state is attained. [23]

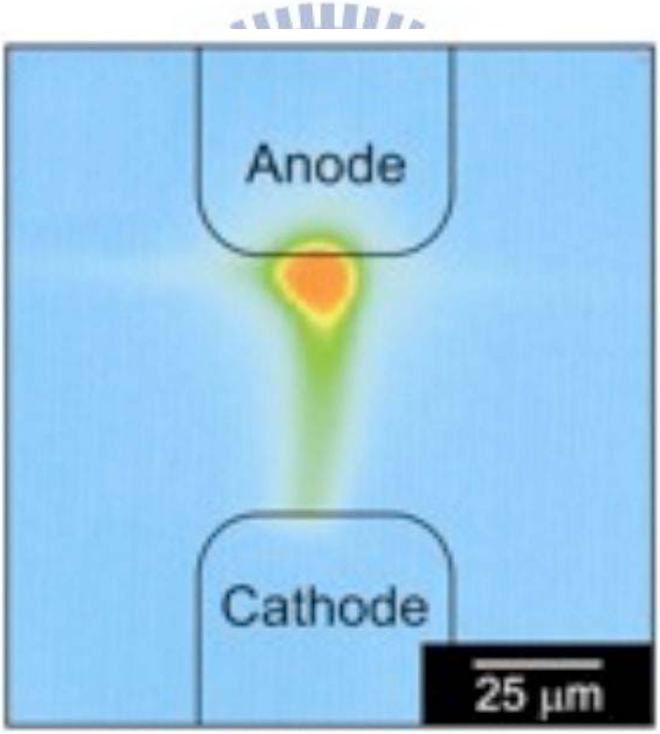


Figure 1.21. Infrared thermal micrograph of the memory cell with a current of 5 mA at a voltage of ~30 V applied. In the color scale, blue and red represent room and elevated temperatures, respectively. [78]

Chapter 2
Experiment details

2.1 Sample fabrication

The structure of the samples studied in this study is depicted in Fig. 2.1. After standard RCA clean procedure, a 100-nm-thick SiO_2 was grown on 4-inch Si. The bottom electrode, a 20-nm Ti followed by an 80-nm Pt, was deposited by e-beam evaporation on SiO_2 at room temperature. Then, the resistance switching layer was prepared with 2 steps. First a 300nm thick Cu layer was deposited on Pt/$TiSiO_2$/Si substrates by DC sputtering. Subsequently, the CuO film was grown by thermal oxidation of Cu layer. Finally, top electrodes were deposited also by e-beam evaporation and patterned by shadow masks. The process flow is depicted in Fig. 2.2, and all the details in each process are stated below.

2.1.1 Standard RCA clean

The bare Si wafers must be cleaned before further process. The RCA clean is the industry standard for removing contaminants from wafers, and the main steps are narrated as the following. The wafers were submerged in Caro's acid (also called SPM), a solution of 3:1 H_2SO_4:H_2O_2, for 10 min at around 80^{o}C to remove organic contaminants from the surface of wafer, then in 1:100 HF:H_2O (diluted HF, DHF) to etch chemical oxide produced in the previous step. The following steps were standard clean 1 (SC1) and standard clean 2 (SC2), in which the wafers were soaked in a solution with 1:4:20 NH_4OH:H_2O_2:H_2O and 1:1:6 HCl:H_2O_2:H_2O, respectively, both

for 10 min at around 80^{o}C to eliminate particles and metallic contamination. Finally, the wafers were dipped in DHF again to remove the chemical oxide grown in the previous standard clean steps. It should be noted that each step was separated by DI water rinse for 5 min.

The mechanism for Caro's acid to remove organic contaminants comes from its strong capability of dehydrating and oxidizing organic compound containing C-H bonding. As for SC1, the surface of Si wafer is oxidized by H_2O_2 into a thin SiO_2 layer, the footing layer for particles and in the meantime etched by NH_4OH. The particles attached on the surface would be removed as SiO_2 layer on the surface finally vanishes. The following SC2 step further takes I_A and II_A metal ions away, in which chlorides resulting from the combination of I_A, II_A and Cl^- would dissolve in water and thus the metal ions are eliminated. On the other hand, III_A metal ions such as Al would be reactive with NH_4OH in SC1 and generates $AlOH_3$ which later forms chlorides in SC2. Hence, to remove particles and metal ions effectively, the sequential order of SC1 and SC2 cannot be reversed.

2.1.2 Growth of SiO_2

After RCA clean, 4-in-boron-doped Si wafers were sent into a furnace immediately for thermal oxidation, in which SiO_2 was grown at 950^{o}C for 30 min in O_2 and H_2 atmosphere. The SiO_2 layer playing a role of insulating layer avoiding current leakage from the Si substrate was expected to be 200 nm in thickness.

According to different mechanisms, there are two types of thermal oxidation, dry and wet oxidation. The former is oxidized in O_2 ambient, in which oxygen ions are combined with Si atoms to form SiO_2. The diffusion barrier for oxygen ions moving

through the existed SiO_2 toward Si is getting larger as SiO_2 is becoming thicker, and thus dry oxidation is not suitable for the growth of thick SiO_2. For the 200-nm SiO_2 required in this study wet oxidation was adopted to serving an insulated layer in order to avoid current leakage from the substrate.

2.1.3 Deposition of bottom electrode

The bottom electrode was deposited by e-beam dual gun evaporator (ULVAC EBX-10C). First, a 20-nm Ti was deposited on SiO_2 to serve as an adhesion layer between SiO_2 and the upper 80-nm Pt layer subsequently *in situ* deposited to ensure excellent conductivity along Pt/Ti dual layer.

E-beam evaporator uses an electron beam to heat a metal crucible and transform solid metal pellets into the vapor of metal atoms which finally reaches the wafers and forms continuous metal film on the surface. The deposition thickness is *in situ* monitored by the crystal sensor embedded in the evaporator system. During deposition, metal film is also deposited on the crystal sensor at the same time. Thicker film reduces the crystal oscillating frequency which can be detected by the system and the thickness of the deposited film can be calculated in real time.

2.1.4 Preparation of resistive switching layer

Two steps of resistive switching layer were fabricated in this thesis. The first step was a deposition of Cu film by sputtering a metal layer, and the second step was thermal oxidation Cu film form CuO insulator film.

In the first step, 300nm thick Cu film was deposited by DC physical vapor sputter system on Pt/Ti/SiO_2/Si. The purity of the Cu metal target is 99.99%. During

film deposition, the respective parameters of the working pressure, substrate temperature, RF power, and gas flow, were $7.6*10^{-3}$Torr, 25°C, 190 W (corresponding deposition rates: 0.1nm/s), and Ar with a total flow rate of 24 sccm. To avoid oxidation with air form more the native oxide of the Cu, the device be reserved at vacuum box.

In the second step, the purpose of the step is oxidation Cu film, which is first step deposition process. Different thermal oxidation temperature and oxidation time were evaluated to oxidize the Cu films. Several process parameters such as oxidation time (15, 30, 60 min), oxidation temperature (300, 400 and 500 °C) and constant oxygen partial pressure (60sccm) were tested. In oxidation processing, we put device into thermal furnace at temperature, then the oxygen gas flow was controlled a flow meter at 60cc/min steady. The detail oxidation processing can be distinguished into three processing. In processing 1, this processing is rising temperature processing. The device was heated to oxidation temperature by 10°C per minute. In processing 2, this processing is maintenance temperature processing. There are three oxidation temperatures (300, 400 and 500 °C) and three oxidation time, totally have nine oxidation condition had be tested. In processing 3, this processing is lowing temperature processing. We adopt nature cool down to avoid thermal stress, cause damage at device. The device was toke out from furnace at room temperature.

2.1.5 Deposition of top electrodes

After the fabrication of resistance switching layer, the top electrodes were prepared to form the structure of metal/resistive switching layer/metal. For the devices, the electrodes of Ti or Pt were deposited by the same e-beam evaporator, in which the thicknesses of Ti and Pt were 150 and 80 nm respectively.

2.1.5.1 Shadow mask

The top electrodes mentioned above are patterned by the shadow mask having the dot-shaped holes with diameters of 350, 250 and 150 μm, i.e. areas of $9.26x10^{-4}$, $4.91x10^{-4}$ and $1.77x10^{-4}$ cm^2, respectively.

2.1.5.2 Lithography

For the purpose of minus the size of the top electrode, it is used photo resistance to be the mask. The characteristic of this sample is used 60mins and 200°C. First, the positive photo resistance AZ4620 is used on the Photo Resist Spinner, the 1200rps for 5 seconds and 4000rps for 25 seconds, After that, the sample is put on the hot plate at 90°C and 5mins for soft bake. And then the mask that having the 10 μm x 10μm square is exposed using the intense light for 45 seconds, this step is that the pattern can be print on the ZrO_2 layer. Finally, the sample is put in the AZ300 for 200 seconds to develop the pattern, and then rinse into the DI-water for 1 min.

The sample that has pattern is also deposited by Ti using the e-beam evaporation for 150nm, and then put it in the acetone for 1 min and rinse in the DI-water for 1 min. The purpose of this step is to lift-off for removing the photo resistance, so the top electrode is Ti can be sustained on the ZrO_2 layer, and the top electrode is 10 μm x 10μm square.

2.2 Resistive switching layer growing equipments

The fabrication of resistive switching layer used two main equipments. One is

DC sputter systems are widely adopted in film deposition due to the simple equipment structure, low cost and the capability of depositing all kinds of films; another is thermal oxidation furnace, which is heating device to oxidation. The DC sputter system and thermal oxidation furnace are detailed introduced following.

2.2.1 DC sputter system

The DC sputter mainly used to deposit metal thin film. We used Cu metal target (99.99%). The sputter system configuration is shown in Fig. 2.3, and can be class to vacuum system, pressure monitor system, gas flow control system, plasma control system. The follow simple describe the function of the each system.

For vacuum system, this system can become high vacuum in chamber. The impurities and particles will be draw out of the chamber.

For gas flow control system, Mass flow controller (MFC) is used to control the gas flow delivered into the chamber and accurately controls the ratio among different gas ingredients.

For plasma control system, this system is used to generate plasma and control the plasma power. The plasma system is of capacitor structure. This is the simplest configuration that under low pressure condition the plasma density would be too low and the number of ions (Ar^+) to bombard the target is not enough for film deposition. It is the magnetron sputter that induces higher plasma density in low pressure situation which is better for deposited film quality. The magnetic field near the target would make electrons to move in a gyro motion, which have a longer path and therefore greater chance for the electrons to collide with other species and induce the plasma of higher density.

2.2.2 Thermal oxidation furnace

Thermal oxidation is accomplished using an oxidation furnace (or diffusion furnace, since oxidation is basically a diffusion process involving oxidant species), which provides the heat needed to elevate the oxidizing ambient temperature. A furnace typically consists of: 1) a cabinet; 2) a heating system; 3) a temperature measurement and control system; 4) fused quartz process tubes where the wafers undergo oxidation; 5) a system for moving process gases into and out of the process tubes; and 6) a loading station used for loading (or unloading) wafers into (or from) the process tubes.

The heating system usually consists of several heating coils that control the temperature around the furnace tubes. The devices are placed in quartz glassware known as boats, which are supported by fused silica paddles inside the process tube. A boat can contain two devices. The oxidizing agent (oxygen or steam) then enters the process tube through its source end, subsequently diffusing to the device where the oxidation occurs.

2.3 Analyses and measurements

In this thesis, several material analyses and electrical measurements were carried out to study the relationship between material and electrical characteristics. The details are stated as the following.

2.3.1 X-ray diffraction (XRD)

X-ray crystallography is the science of determining the arrangement of atoms within a crystal from the manner in which a beam of X-rays is scattered from the

electrons within the crystal. The key step in X-ray crystallography is the diffraction of X-rays from a crystalline material. It is the elastically scattered x-ray photons that are measured in diffraction measurement, as the scattered x-rays without losing any energy carry information about the electron distribution in materials.

Generally, thin films are classified according to the crystallization. There are three types of crystallization, such as amorphous, polycrystalline, and single crystalline. X-Ray diffraction analyses are used to investigate the crystal structure and the orientation of our sample. Furthermore, the relations between the crystallization and the heat treatment can be characterized from XRD results. In the experiment, the thin films show either amorphous or poly. Follow Scherrer's formula, we could calculate the average grain size from XRD illustration:

$$D = \frac{\lambda}{\beta \times \cos\theta}$$

Where D is the apparent crystallite size (in the present case, the local strain effect was not taken into account), β is the full width at half maximum (FWHM) of the XRD peak and θ is the diffraction angle. In these analyses, X-ray is made with 0.02 degree beam divergence and operation configuration at 30KV, 20mA.

Thin film diffraction methods are used as important process development and control tools, as hard x-rays can penetrate through the epitaxial layers and measure the properties of both the film and the substrate. There are several special considerations for using XRD to characterize thin film samples. First, reflection geometry is used for these measurements as the substrates are generally too thick for transmission. Second, high angular resolution is required because the peaks from semiconductor materials are sharp due to very low defect densities in the material.

2.3.2 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is a microscopy technique whereby a beam of electrons is transmitted through an ultra thin specimen, interacting with the specimen as it passes through it. An image is formed from the electrons transmitted through the specimen, magnified and focused by an objective lens and appears on an imaging screen, a fluorescent screen in most TEMs, plus a monitor, or on a layer of photographic film, or to be detected by a sensor such as a CCD camera.

In material science/metallurgy the specimens tend to be naturally resistant to vacuum, but must be prepared as a thin foil, or etched so some portion of the specimen is thin enough for the beam to penetrate. Preparation techniques to obtain an electron transparent region include ion beam milling and wedge polishing. The focused ion beam (FIB) is a relatively new technique to prepare thin samples for TEM examination from larger specimens. Because the FIB can be used to micro-machine samples very precisely, it is possible to mill very thin membranes from a specific area of a sample, such as a semiconductor or metal.

There are a number of drawbacks to the TEM technique. Many materials require extensive sample preparation to produce a sample thin enough to be electron transparent, which makes TEM analysis a relatively time consuming process with a low throughput of samples. The structure of the sample may also be changed during the preparation process. Also the field of view is relatively small, raising the possibility that the region analyzed may not be characteristic of the whole sample. There is potential that the sample may be damaged by the electron beam, particularly in the case of biological materials.

2.3.3 Secondary ion mass spectroscopy (SIMS)

Secondary ion mass spectrometry, SIMS, is the mass spectrometry of ionized particles which are emitted when a surface, usually a solid, is bombarded by energetic primary particles which may be electrons, ions, neutrals or photons. The emitted of secondary particles will be electrons, neutral species atoms or molecules or atomic and cluster ions. The vast majority of species emitted are neutral but it is the secondary ions which are detected and analyzed by a mass spectrometer. It is this process which provides a mass spectrum of a surface and enables a detailed chemical analysis of a surface or solid to be performed.

The earliest application of SIMS was not as a surface analysis technique but as a means of detecting trace deposits of elements with very high sensitivity. To do this the primary ion flux is increased so that many layers are removed rapidly, consequently the secondary ion flux is increased such that elemental concentrations down to sub-ppm levels can be detected. The technique has been refined such that today very accurate concentration profiles can be monitored as a function of depth from the surface of the material. Although this capability finds important application in many areas of materials science, it is in the dopant analysis of semiconductor materials that SIMS has made its most dramatic contribution. In carrying out a depth profile analysis there are two main parameters for which the instrumentation and experimental procedure have to be optimized, that is the dynamic range of concentration sensitivity for the element to be analyzed and the depth resolution. In this work, we used Cs source.

2.3.4 Auger electron spectroscopy (AES)

Auger electron spectroscopy (AES) has now emerged as one of the most widely

used analytical techniques for obtaining the chemical composition of solid surfaces. The basic advantages of this technique are its high sensitivity for chemical analysis in the 5- to 20-Å region near the surface. When an electron is ejected from an inner shell of an atom the resultant vacancy can be filled by either a radiative (X-ray) or nonradiative (Auger) process. In AES the atomic core levels are ionized by the incident electron beam and the resulting Auger electrons are detected with an electron spectrometer. In our work, AES was employed to analyze the deep spectra of Cu and O element by sputtering in the resistive switching layer.

2.3.5 Electrical measurements

The electrical properties were measured by the apparatuses consisting of a probe station with Watlow 93 temperature controller, Agilent 4155C semiconductor parameter analyzer and E5250A low leakage switch, controlled by a desktop computer with the Agilent VEE software.

The electrical measurements in this thesis were divided into 5 items, in which bistable resistive switching, endurance, retention, and stress were tests of criteria for memory device application; the other item was the tests intended for the study of fundamental mechanisms of the resistive switching devices.

2.3.5.1 Bistable resistive switching

This measurement was performed by Agilent 4155C, detecting the conducting current while applying and sweeping DC biases on the devices. From the *I*-*V* curve, the on state with low resistance and high conductivity, and the off state with high resistance and low conductivity, were observed easily.

2.3.5.2 Endurance

Endurance is a key feature that memory devices must endure a enormous number of switching cycles to meet the operation requirements in many applications such as random access memory (RAM) and solid state disk (SSD) which both need many data write-in operation without any failures. In addition, it is a basic requirement in almost every type of memory devices as well.

The tests of endurance were carried out that DC biases were applied to switch on and off by at both room temperature (RT) and 150^{o}C. High temperature would accelerate the fatigue process for memory devices.

2.3.5.3 Retention

Retention is an essential performance for nonvolatile memory devices, standing for the capability of retaining memory data for a long period without any data loss. For a commercially available nonvolatile memory product, the performance of retention is requested to last 10 years.

The retention tests were carried out as the following description. First, the memory device is switched into on or off state at RT either by DC bias or pulses. Then, the data states were read out at RT once in a given period by applying a 0.1 V reading bias small enough in order not to modify the existed memory states. Between every data reading, the samples were placed in the environment of RT and 150^{o}C respectively.

2.3.5.4 Stress

Stress, or non-destructive readout, is also important for nonvolatile memory devices, in which memory data could not be modified in data reading process. It is

also a basic demand for nonvolatile memories. On the other hand, if random access memories have the property of non-destructive readout, the control circuit will not have to refresh which takes additional clock cycles to write the data back, giving rise to the increase in the operation speed.

The stress tests were implemented also by Agilent 4155C. After switched to on or off state, the device was applied with 0.1 V bias for a long period to observe if any data loss would happen. For the time period of data not modified by bias, it is equivalent that the memory states would not be affected by the same period of total pulse widths when operating under pulses.

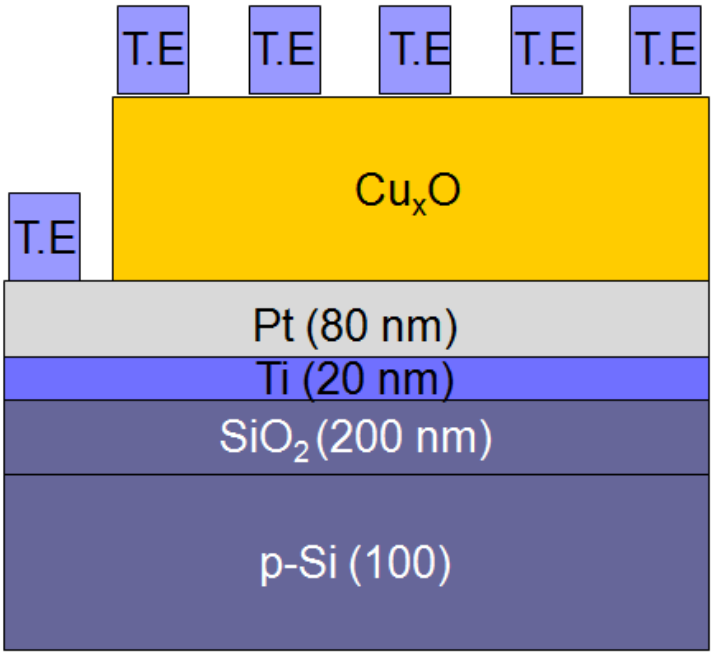


Figure 2.1. Sample structure.

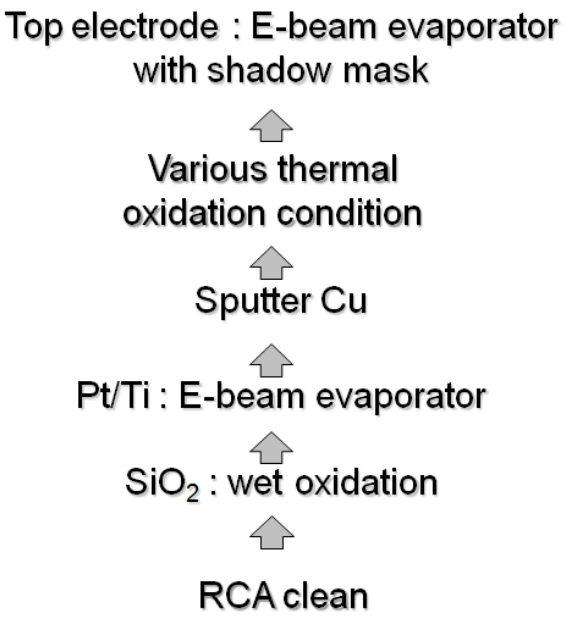


Figure 2.2. Experiment flow.

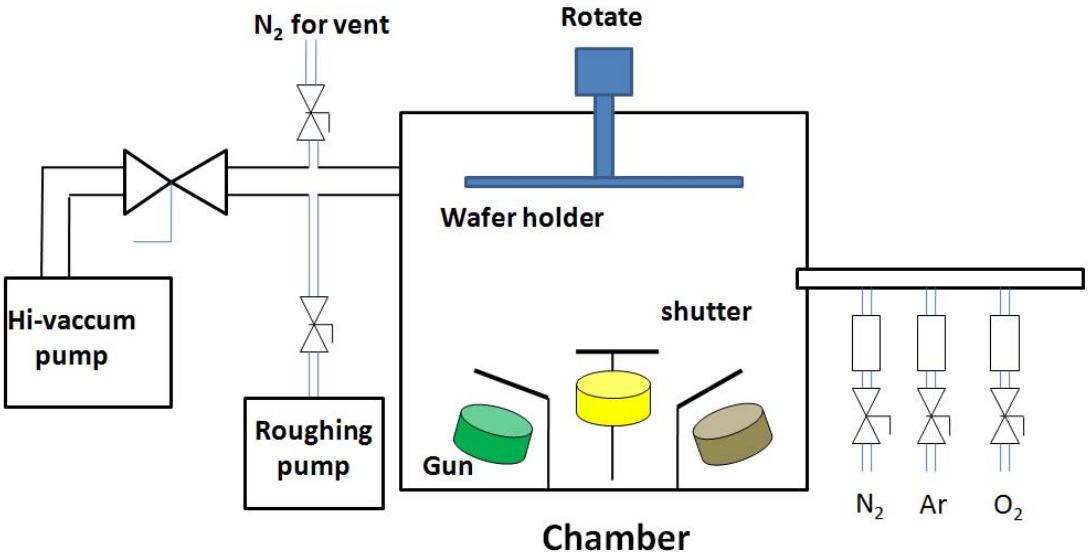


Figure 2.3. Sketch of DC sputter system components.

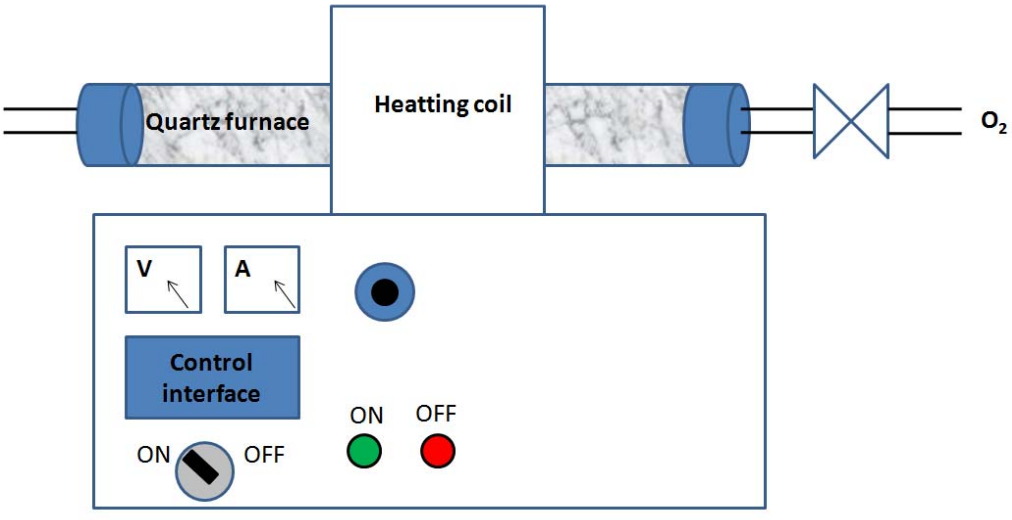


Figure 2.4. Sketch of thermal oxidation furnace system component.

Chapter 3
Results and discussion

The frame of experimental results and discussion are shown in Fig.3.1. At first, The Ti/CuO/Pt structure with different oxidation conditions are analysis to find the optimum oxidation. Secondary, the different top electrodes, Ti/CuO/Pt, Pt/CuO/Pt, and W-probe/CuO/Pt, with the same oxidation conditions are studied to confirm filament formation and rupture in the bulk of the CuO. Then, the Ti/CuO/Pt device is measured by controlling different current compliance and different reset stop voltage. At application, multiple level storing can be achieved in Ti/CuO/Pt structure by controlling current compliance at on-state or reset stop voltage at off-state. The device has a potential for non-volatile multiple-valued memory device.

3.1 CuO film with different thermal oxidation condition

After the Cu thin film deposited by DC sputtering, the devices were thermal oxidation at different oxidations. The oxidation temperature conditions are 300^{o}C, 400^{o}C, 500^{o}C, and the oxidation time conditions are 15min, 30min, 60min. Therefore, there are nine oxidation conditions to study. In different oxidation conditions to find optimum, we use Ti to be the top electrodes.

3.1.1 Electrical properties

In different thermal oxidation conditions, the resistive switching characteristics are observed by I-V curve. The operation voltages, including V_{on} and V_{off}, are both

less than 3V and suggest that the devices are appropriate for the low voltage applications. The resistive switching localized in small region. There are some properties to note, the turn-on voltage variance more than turn-off variance and the switching gradual stable when switching cycles increase.

The devices yield and endurance are showed in Fig 3.2. The oxidation conditions, 400^{o}C, 60min, have the best device yield and endurance than other conditions. The resistive switching is nonpolar switching, the nonpolar switching can be seen for either positive or negative polarity of V or I; our samples show turn-on and turn-off when alternating the polarity of V or I as seen in bipolar switching. Thus, the nonpolar and bipolar actions are coexisting in a quite unique fashion.

3.1.2 Material analyses

Fig. 3.3 shows XRD results of device with oxidation condition 400^{o}C-60min, and 500^{o}C-60min. It was found that the CuO films have a polycrystalline structure.

Fig. 3.4 and Fig. 3.5 show SIMS result of oxidation condition 400^{o}C- 15min, and 400oC-60min, respectively. It was found that the Cu film was completely oxidation.

3.2 Compare different top electrodes

The devices of the oxidation temperature at 400 ^{o}C, 60 min, were investigated that provide higher yield and endurance.

3.2.1 Relationship of ratio and voltage

The on/off ratio and voltage bias relationship is showed in Fig. 3.24. The on/off ratio is lager at small bias. Due to this reason and small read bias more damage the memory state, the read bias magnitude is setting 0.2V. The reason of the read bias taken 0.2V is 0.2V is ohmic conduction region by current fitting as show in Fig. 3.18, 3.19, 3.21, 3.22.

3.2.2 Operation mode and polarity

After forming process, the memory device remains at ON-state. Then, we need a voltage to switch the memory device back to the OFF-state and this is what we call turn-off process. If the memory is switched back to the ON-state, this is a turn-on process. In ours research, Pt/CuO/Pt devices belongs to nonpolar switching, and the *I-V* curve is symmetrical as show in Fig. 3.10-13. On the other hand, even though Ti/CuO/Pt devices belong to nonpolar switching as show in Fig. 3.6-9, the best mode is located at positive turn-on and negative turn-off mode. From now on, in this thesis, we only sweep for this best mode to investigate the electrical properties. The range of the operation voltage is located at 2V ~ -1.5V, but depicts a larger variation. In order to further confine the resistive switching phenomenon can occur without electrode of active metal, we measure CuO thin film directly by W-probe. The result of measure also show nonploar switching as show in Fig. 3.14-16. Fig. 3.17 shows that compare with Ti top electrode and W-probe, the W-probe can avoid the interface effect and small area of diameter ~ 5um.

3.2.3 Current fitting

Fig. 3.18, 3.19, 3.21 and 3.22 show that the ON-state is ohmic conduction at all voltage range, and OFF-state is ohmic conduction below 0.3V for all kinds of top

electrodes in both turn-on and turn-off process. It can be noticed that the current has a linear relationship with voltage of ON-state, which indicates that ohmic conduction is dominant in ON-state. It is suggested that conductive filament paths are formed as a bridge between top electrode and bottom electrode after the turn-on process.

Frenkel-poole emission model is extensively used investigate carrier transport behavior in insulator and semiconductor, which describe in section 1.3.4.

Fig. 3.20 and 3.23 show the logarithmic plot of I versus $V^{1/2}$ of OFF-state. The experiments data obeys a good linear relationship at high electrical field region. From the ln (I/V) $\propto V^{1/2}$ relation and Frenkel–Poole constant α calculation, carrier trapping and de-trapping of Frenkel–Poole effect is thought of as the main conduction mechanism of OFF-state. Fig. 3.20 shows that *I-V* curves were well fitted by the formula of Poole–Frenkel emission model with Pt top electrode. Fig. 3.23 shows that *I-V* curves were well fitted by the formula of Poole–Frenkel emission model with Ti top electrode.

The Pt is deep work function material and Ti is shallow work function. CuO is p-type semiconductor. In generous, the work function is 5.3eV and band gap is about 1.4eV at 400^{o}C thermal oxidation. A deep work function metal can give an Ohmic contact to a p-type semiconductor, while a Schottky barrier is formed at the interface between a shallow work function metal and a p-type semiconductor. Pt is deep work function which can is formed ohmic contact to a CuO film, but Ti is shallow work function which can give a Schottky barrier contact to a CuO film.

3.2.4 Size effect

Fig. 3.25-28 show *I-V* curve of Ti/CuO/Pt structure with top electrode area 10um*10um, and diameter 150um, 250um, and 350um. For constant current compliance value, the ON-state current is independent size, but the OFF-state current is increased with the size of top electrode. The OFF-state is homogenous current conduction, but the ON-state is the filament of inhomogeneous current conduction.

3.2.5 Endurance

The tests of endurance of Ti/CuO/Pt devices are shown in Fig. 3.31-32, and endurance of Pt/CuO/Pt devices are shown in Fig. 3.33, and endurance of W-probe/CuO/Pt devices are shown in Fig. 3.34. The Fig. 3.31 show the Ti/ CuO/Pt devices of turn-on voltage and turn off voltage at different switching cycles, while the Fig. 3.32 show ON-state and OFF-state current at different switching cycles. It is found that the Ti/CuO/Pt devices can be switched over than 500 cycles under the operation of DC sweeps, and turn-on voltage variance are large than turn-off voltage. The turn-on process is a random process. Because the DC sweeps produce more stress on the semiconductor devices than pulse switching, the Ti/CuO/Pt device expect to have more than 500 cycles with pulse operation.

3.2.5 Retention

Fig. 3.35 depict the retention of Ti/CuO/Pt devices examination. Both results show an excellent retention property of the device, in which the data of ON or OFF-states are retained after 10^5 at room temperature.

3.2.5 Stress

The stress test of Ti/CuO/Pt devices displays that both ON and OFF state are not modified after stressed under 0.2 V for 6500 s, as shown in Fig. 3.36.

The stress test of Pt/CuO/Pt devices displays that both ON and OFF state are not modified after stressed under 0.2 V for 700 s, as shown in Fig. 3.37.

The stress test of Ni/CuO/Pt devices displays that both ON and OFF state are not modified after stressed under 0.2 V for 12000 s, as shown in Fig. 3.38.

3.3 Different current compliance

The Ti/CuO/Pt devices are measured by changing current compliance in order to investigate the relation between current compliance and resistive switching property.

3.3.1 Measurement of different current compliance

Fig. 3.39-46 show *I-V* curve of switching cycles at each current compliance; 1mA, 3mA, 5mA, 10mA, 20mA, 30mA, 40mA, 50mA by an Agilent 4155C Semiconductor Parameter Analyzer. The detail methods of the measure are illustrated as follow. After forming process, the current compliance is set at 1mA. The turn-on process make device to ON-state. Continuously, the turn-off process are increase negative bias step by step until the device turn off to OFF-state. This method can avoid unnecessary damage in turn-off process. Repeat turn-on and turn-off process until more than ten times. The current compliances are increased to 3mA, 5mA, 10mA, 20mA, 30mA, 40mA, 50mA. The turn-on and turn-off process are repeat at each current compliance value.

There are some resistive switching parameters be defined in order to convenient follow discuss. Fig. 1.2 shows those parameters in *I-V* curve. The turn-off voltage (V_{off}) is the voltage of the ON-state to OFF-state, the turn-off current (I_{off}) is the current of the ON-state to OFF-state, and the stop voltage (V_{stop}) is the maximum voltage value of the sweep voltage range when turn-off process.

3.3.2 Discussion of current compliance

Fig. 3.47 shows the relation between current compliance and current at –0.2 V. The upper error bars are ON-state current variation under switching cycles, while lower error bars are OFF-state current variation under switching cycles. The ON-state current increased with current compliance, and saturate at current compliance value 20mA. The ON-state current increased with current compliance, imply that when current compliance increased, the filaments are stronger than low current compliance value, and conduction cross area more large lead to ON-state resistance decrease.

Fig. 3.48 shows that the turn-off voltage increased with current compliance, and the variation of turn-off voltage is seldom. The insert shows the relationship of current compliance and turn-off voltage is not observed any power law, and the turn-off voltage is weak dependent current compliance.

Fig. 3.49 shows that the turn-off current increased with current compliance, and the variation of turn-off current is seldom. The dotted line mark current compliance equal to turn-off current. The insert shows the relationship of power law between current compliance and turn-off voltage, and the turn-off current is strong dependent current compliance. The current compliance influence turn-off current is more sensitive than turn-off voltage can be explained as follow. The increasing power

contribute from two term

$$\Delta P = 2IR\Delta I + I^2\Delta R$$

Because ON-state is low resistance, first term can be drop. The current mainly contribute to power rather than voltage. This is suggested that power or current dominate turn-off process.

We define that turn-off power is the product of turn-off voltage and turn-off current ($P_{off} = I_{off} * V_{off}$). The turn-off power is the electric power to make device from ON-state to OFF-state. Fig. 3.50 shows that the turn-off power has linear relationship with current compliance, and the variation of turn-off current is seldom. The linear relationship between turn-off power and current compliance can be explained as follow. We make some assumption to explain the linear relationship. First, current density (J) is constant current density in filament, and weak dependent current compliance. Second, the effect switching thickness (d_s) is almost constant and independent current compliance, because the filament has small voltage drop. Third, the defect concentration per volume is independent current compliance.

The effect switching region is modeling a cylinder, is composed with defect, with effect cross section area (A_s). At turn-on process, the current compliance (I_{comp}) is

$$I_{comp} = J \cdot A_s$$

On the other hand, the defect maybe is Cu atoms, Cu ions, oxygen vacancies or CuO_x ($x<1$). The total defect number in cylinder filament is

$$\text{num. of defect} = A_s d_s \times N_t \propto I_{comp}$$

Therefore, the number of defect proportion to current compliance. In another point of view, the current pass filament in turn-off process. This locally enhances electric field and current density, hence the Joule dissipation and the temperature, which in the further accelerates the dissolution process. This positive feedback is at the basis of the sharp current drop at turn-off process [42]. When the device switched turn-off, the defect will combine with oxygen to form high resistive CuO at the effect switching region. The turn-off power should proportion to number of defect as follow.

$$\text{num. of defect} \propto P_{off} \equiv I_{off} V_{off}$$

The turn-off power would proportion to current compliance.

$$I_{comp} \propto P_{off}$$

To further confirm Joule heating effect caused the filament rupture model, the various temperature measure to observe turn-off process. Fig. 3.51 shows that turn-off process with different temperature. There is a tendency towards turn-off power decay, as a result of temperature raise.

3.3.3 Relation between temperature and current

At ON-State, as shown in Fig. 3.52, the current is decreasing with raising measurement temperature. This trend indicates that the property of ON-state is metal-like behavior. It is owing to the formation of metallic filaments in thin film. At OFF-state, as shown in Fig. 3.53, an obvious trend is investigated. The current is increasing while increasing measurement temperature. The change of conductivity

can indicate that the property of OFF-state is semiconductor-like or insulator behavior. Fig. 3.54 shows that double log *I-V* curve of turn-on process at RT and 150^{o}C, and Fig. 3.55 shows that double log *I-V* curve of turn-off process at RT and 150^{o}C. The ohmic region of OFF-state is larger at 150^{o}C. The mechanism of ohmic region of OFF-state is different from the ohmic region of ON-state. The ohmic region of OFF-state is due to thermally-generated carrier, rather than injection carrier of metal-like.

3.4 Different stop voltage

The Ti/CuO/Pt devices at voltage bias more than reset voltage, and switching cycles increase, the transition region of the turn-off process would enhanced until stable saturate.

3.4.1 Measurement of different stop voltage

This phenomenon can be explained that over drive voltage induce defect near the effect switching region.

The device operate stop voltage is more than turn-off voltage. In few switching cycles, the sharp current abruptly drop from ON-state current to OFF-state current in turn-off process. The switching cycle increase the current drop gradually. The transition region observed in turn-off process. The Ti/CuO/Pt devices observed the behavior of transition region in turn-off process at bipolar switching operation mode.

Due to the transition region phenomenon presented during turn-off process, the *I–V* characteristics of the Ti/CuO/Pt devices were investigated with different spans of voltage scan for OFF-process. Bias voltage was swept as 0 V→1.5 V (current limited

at 5mA) → 0 V→ -0.8 V (V_{stop1})→0 V→ -1 V (V_{stop2})→0 V→ -1.5 V (Vs_{top3})→0 V. As the V_{stop} increased, the higher resistance value of OFF-state increased, which demonstrating the intermediate resistance state (IRS) was shown in Fig. 3.56.

In order to further confirm the resistive switching can transfer in different IRS and controlled by stop voltage, bias voltage was swept as 3 modes, 0 V→1.5 V (current limited at 5mA→ -0.75 V (V_{stop1})→0 V→ -2 V (V_{stop2}); 0 V→1.5 V (current limited at 5mA→ -0.8 V (V_{stop1})→0 V→ -2 V (V_{stop2}); and 0 V→1.5 V (current limited at 5mA→ -1V (V_{stop1})→0 V→ -2 V (V_{stop2}) as show in Fig. 3.57-59, respectively. The stop voltage 1 was changed with different model.

Next, I-V curve were repeatable measured at different sweep range; stop voltage (V_{stop}) was varied as -0.8 V, -0.9 V, -1V, and -2 V in turn-off region as show in Fig. 3.60-63. Fig. 3.64 shows that statistics plot of current at -0.2V of ON-state and OFF-state with various stop voltage. As V_{stop} decreased, hysteresis has shrunk, OFF-state approached to ON-state. This phenomenon can be explained that filament be complete ruptured as decrease V_{stop}.

3.4.2 Discussion of different stop voltage

In order to elucidate that the V_{stop} decreased with OFF-state resistance, we proposed a possible model to explain transition region occur in turn-off process. At first, the V_{stop} increased such that over drive voltage induce defect near the effect switching region. After few switching cycles, the amount of defect would raise near the Ti/CuO interface. When voltage bias is the turn-off voltage, the filaments were rupture by Joule heating. However, the voltage bias continue to increased in negative bias, the electric field effect wound enhanced. In the beginning, the filament would be

ruptured. As the voltage bias continue to increased in negative bias, the electric field would tend to formation more thin filament to form IRS. Following, the voltage bias increased induce current crowding to generate Joule heating, the thin filament rupture again. Repeat foregoing process until voltage bias to V_{stop}.

According to previous reports, Chen et al. suggested that small changes in oxygen concentration may result in large resistance change and the oxygen stoichiometry change induced by electric field might not be uniformly distributed in the interface region [35]. Lin et al. proposed that in the turn-on process, the biased electrons found one or few conducting paths composed of possible point defects including oxygen vacancies, ionic, and electronic defects, and the OFF-process was caused by the defects would trapped electrons, thus leading to the rupture of conducting paths [76]. Form Lin et.al discusses the resistive switching property of 0.1, 0.2, and 0.3% Mo-doping SZO thin films, the apparent transition region in turn-off process with the Mo-doping percentage increased [97]. This result can support our model. As Mo-doping percentage increased, the defect concentration would be increased to enhance transition region in turn-off process.

If our model is correct, the larger current compliance would cause defect be covered by larger filament. Fig. 3.67 shows the mechanism of turn off process with transition region different current compliance. It is predicted that transition region is unapparent with current compliance increased as show in Fig. 3.68-71.

Fig. 3.72 shows the stress characteristics of IRS. In this figure, the stress of IRS is worse than ON-state and OFF-state, because the IRS is thin filament. When the CuO film was stressed by voltage 0.2 V, the soft breakdown is more easily.

3.5 Possible resistive switching model

According to the literature reviews for the proposed resistance switching mechanisms of the NiO_x film in a RRAM cell, it has been most commonly believed that the voltage stress creates multiple filamentary conducting paths in the NiO_x film due to the nonnegligible Joule heating effect [34,42,51].They have strongly suggested that the formation and rupture of the filamentary conducting paths in the NiO_x film are directly related to the low and high resistance properties of the RRAM cell. Interestingly, the "filament anodization model" [24] and the "electric faucet model" [99] have recently been suggested as possible explanations for localized filament formation and its contribution to the memory switching close to the anodic positively biased electrode.

Figure 3.73 shows that detail resistive switching mode. After the forming process on a pristine memory cell, we observed the reversible bistable resistive memory switching through a voltage sweep. Before forming process, the devices are polycrystalline by XRD. The as-grown CuO film will contain nanometer-sized conductive domains at a highly localized area, such as the grain bound aries and a TE/CuO interface, because grain boundaries are more conductive and defective than other regions.

In forming process, we assume here that the electric field plays an important role in opening the conducting paths (electric faucet) [99] as a result of the localized filament formation near the TE/CuO interface. In the forming process, filamentary conducting paths form as a soft breakdown in the dielectric material. It is expected that the percolating filamentary conducting paths will be shaped like a flash of

lightning through the increased CuO grain boundaries. However, the area of the electric faucet at the TE/CuO interface should be small. Because of the compliance current, only a weak conductive filament with a controlled resistance is formed. After forming, the devices are in ON-state.

In turn-off process, the filament ruptured by local joule heating. This conductive filament is again disrupted thermally because of high power density generated locally, The locally enhances electric field and current density, hence the Joule dissipation and the temperature, which in turn further accelerates the thermal oxidation near the TE/CuO interface e is widely considered to be the mechanism behind the rupture of the filaments. After turn off process, the devices are in OFF-state.

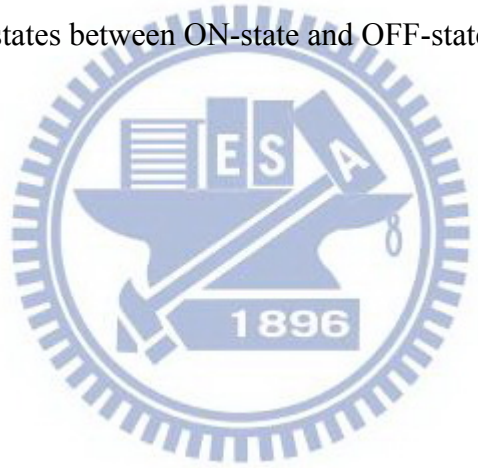
In turn-on process, the electric field induce soft breakdown at TE/CuO interface, furthermore the conductive path is random to cause turn-on voltage variation. After turn-on process, the devices are in ON-state. The reversible bistable resistive memory is switching between ON-state and OFF-state.

3.6 Multi-level application

The ON-state current is dependent on current compliance, but OFF-state current is not as show in Fig. 3.74. Thus, the multiple levels of the ON-state are only controlled by current compliance. On the other hand, the current of the OFF-state is dependent on stop voltage, but the current of the ON-state is not as show in Fig. 3.75. Thus, the multiple levels of the OFF-state are only controlled by stop voltage.

The multiple levels of the ON-state have acceptable sensing margin by choosing suitable current compliance value. Fig. 3.76 shows stress characteristics of ON-state of multi-level with Ti/CuO/Pt structure.

In application, the Ti/CuO/Pt devices can series a transistor (1T-1R configuration). The transistor of the gate voltage can limit the ON-state current of the Ti/CuO/Pt devices, so that different gate voltage can create different ON-state multilevel. Contrary to the multiple levels of the ON-state, which is determined by current compliance, the stop voltage (V_{stop}) can also determine the multiple levels of OFF-state. By controlling the amplitude of the reset stop voltage pulse, another three intermediate resistance states between ON-state and OFF-state can be produced.



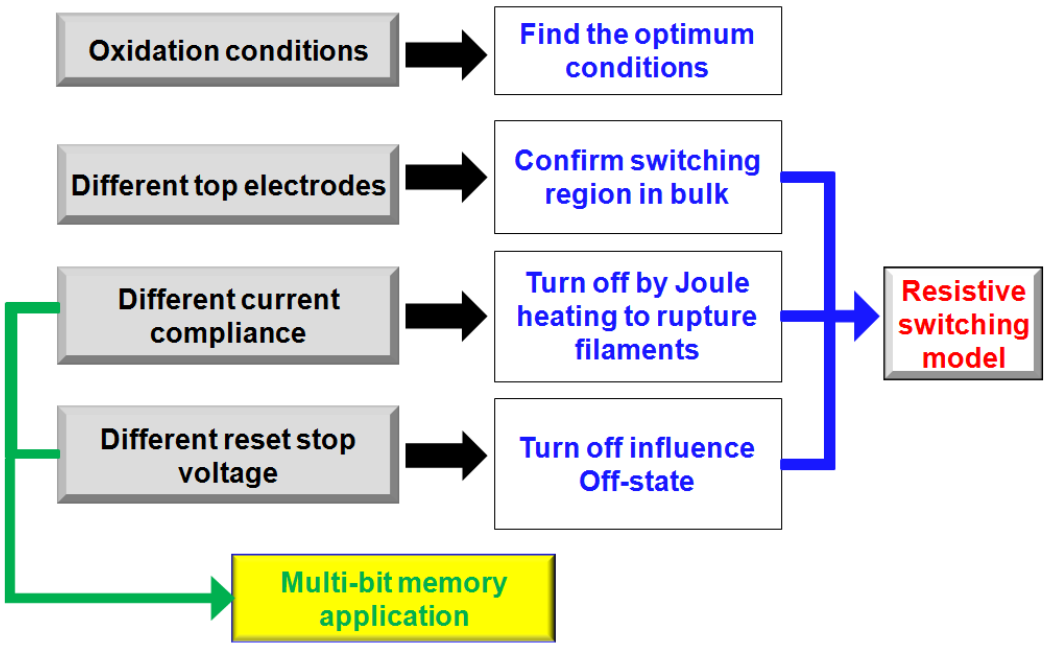


Figure 3.1. The frame of experimental results and discussion

Ti (TE) Yield	Temperature		
Time (min)	300 C	400 C	500 C
15	5%	30%	40%
30	5%	25%	30%
60	20%	75%	40%
Ti (TE) Cycle	**Temperature**		
Time (min)	300 C	400 C	500 C
15	10	100	100
30	25	35	35
60	100	500	100

Figure 3.2. The yield and endurance of oxidation condition.

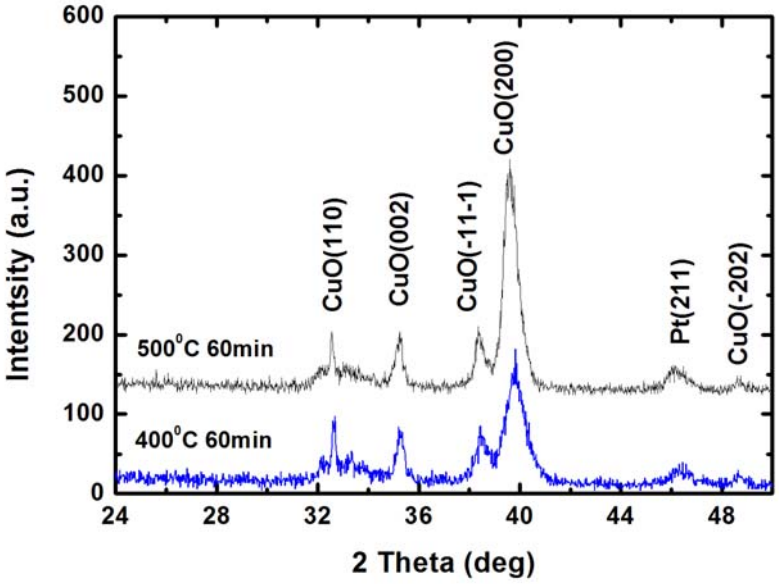


Figure 3.3. XRD results of device with oxidation condition 400°C-60min, and 500°C-60min.

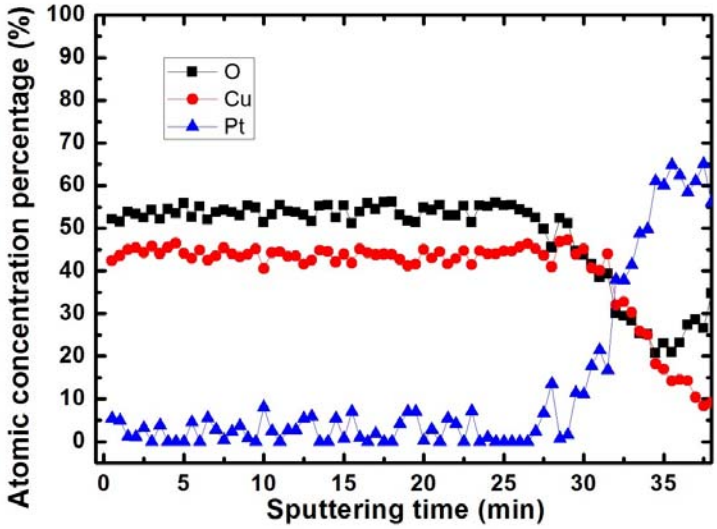


Figure 3.4. SIMS result of oxidation condition 400°C, 15min.

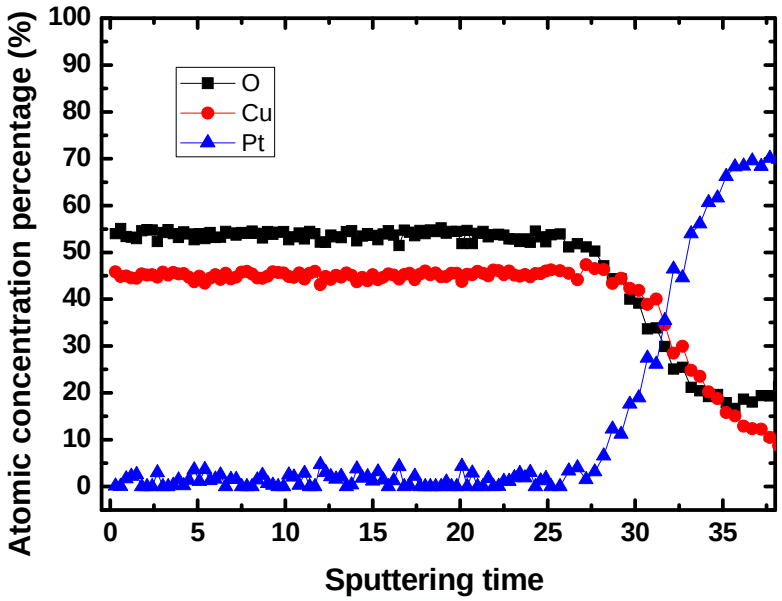


Figure 3.5. SIMS result of oxidation condition 400°C, 60min.

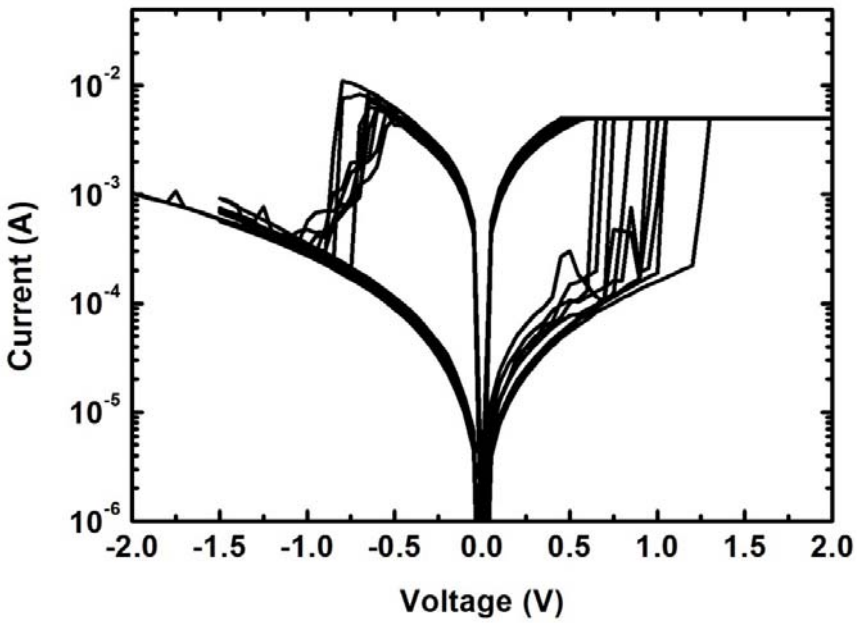


Figure 3.6. *I-V* curve of Ti/CuO/Pt structure in positive turnon and negative turn off switching mode.

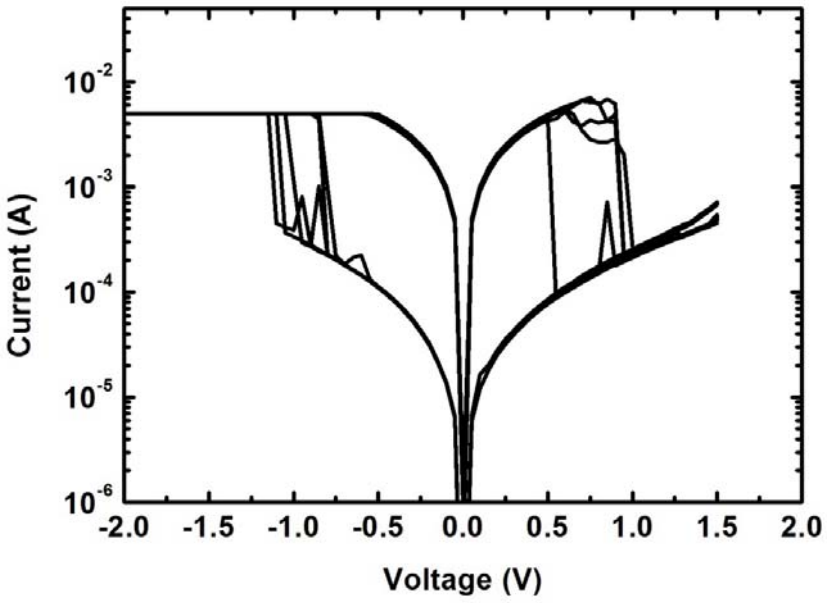


Figure 3.7. *I-V* curve of Ti/CuO/Pt structure in negative turn on and positive turn off switching mode.

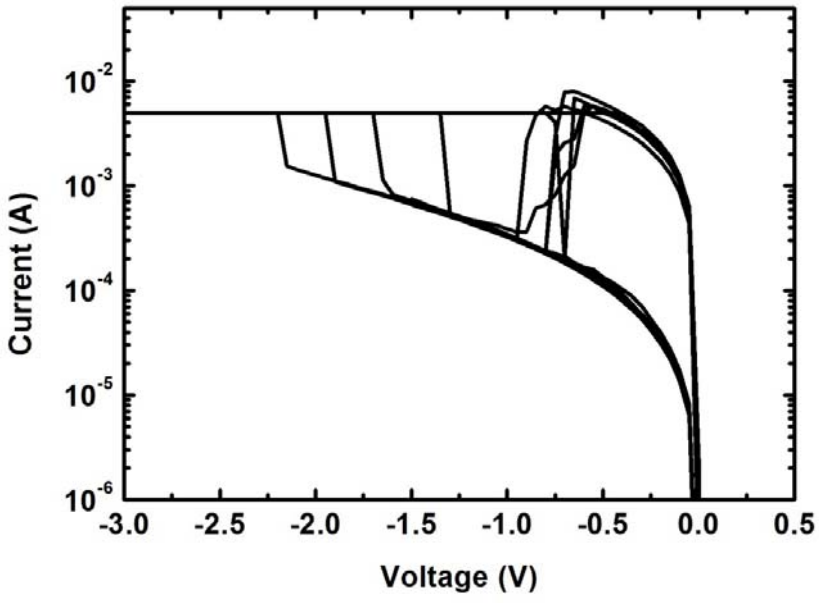


Figure3.8. *I-V* curve of Ti/CuO/Pt structure in negative turn on and negative turn off switching mode.

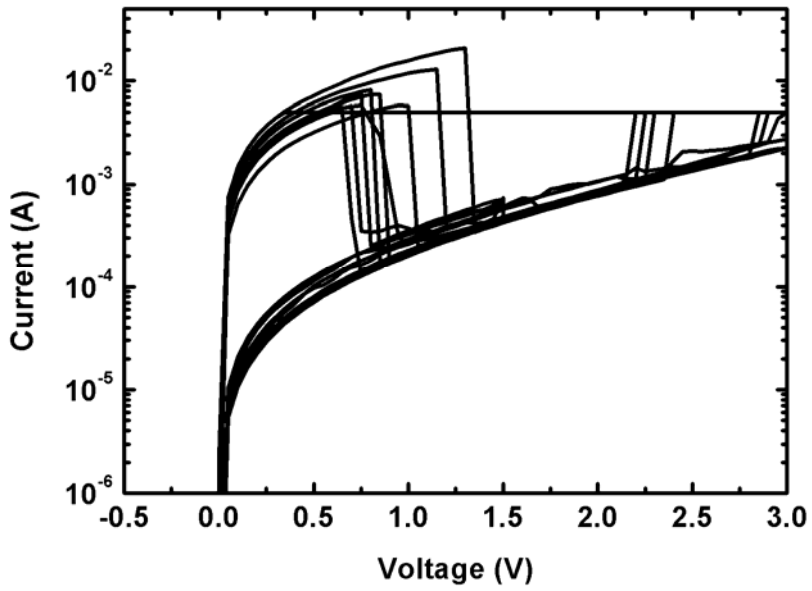


Figure 3.9. *I-V* curve of Ti/CuO/Pt structure in positive turn on and positive turn off switching mode.

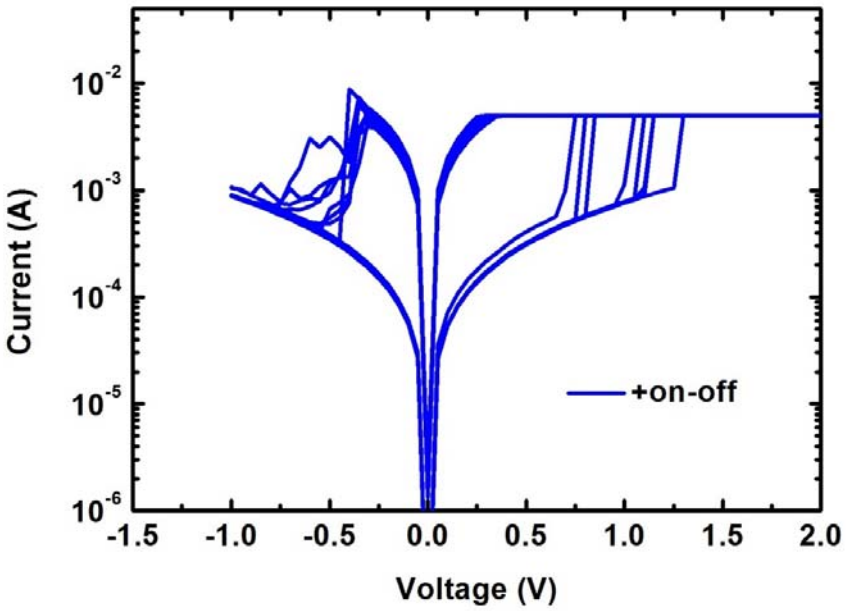


Figure 3.10. *I-V* curve of Pt/CuO/Pt structure in positive turn on and negative turn off switching mode.

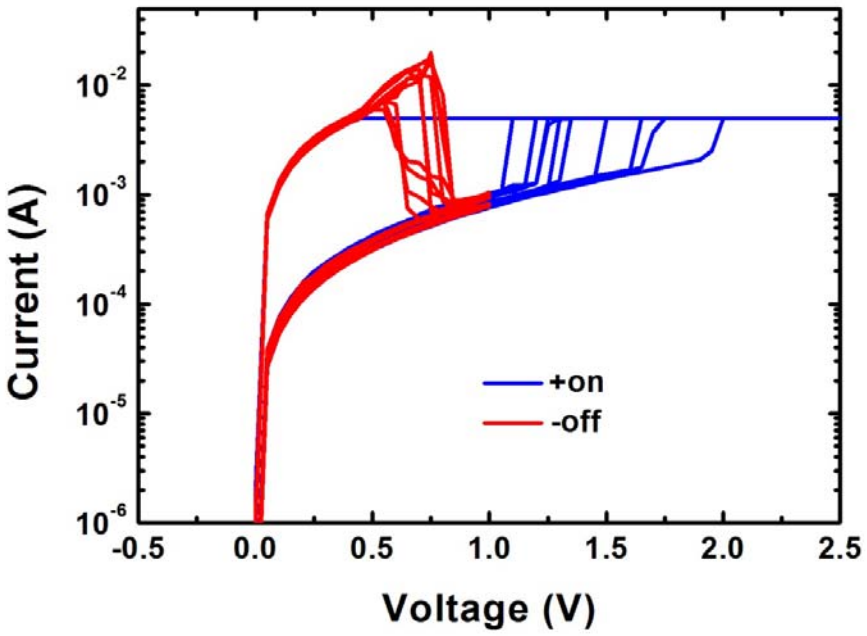


Figure 3.11. *I-V* curve of Ti/CuO/Pt structure in positive turn on and positive turn off switching mode.

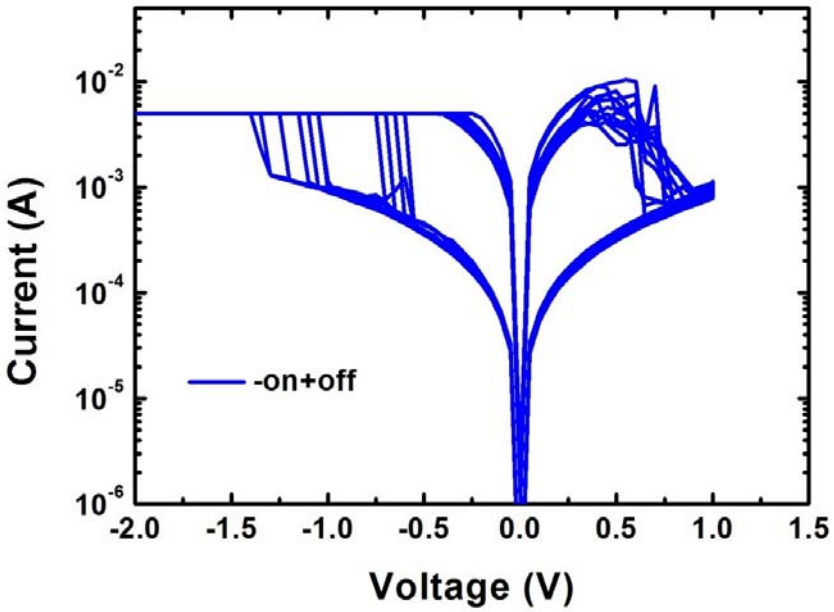


Figure 3.12. *I-V* curve of Pt/CuO/Pt structure in negative turn on and positive turn off switching mode.

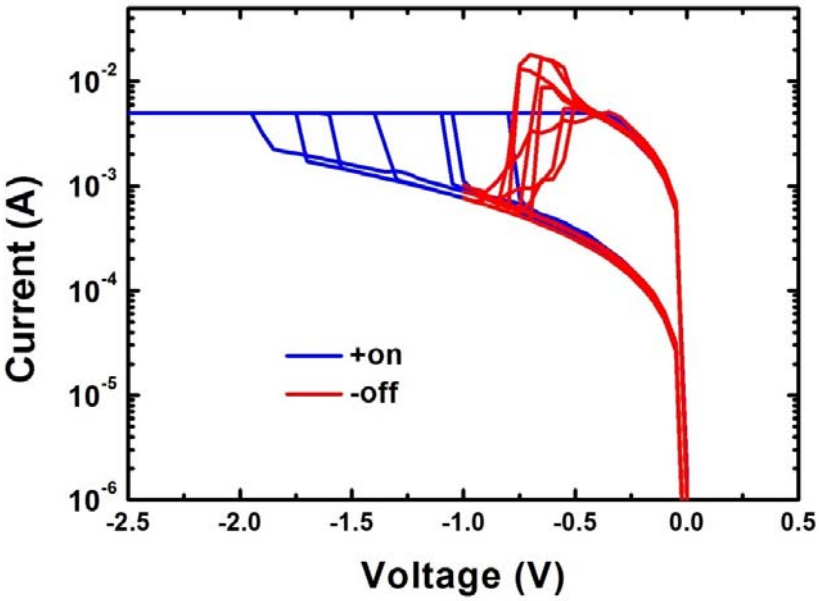


Figure 3.13. *I-V* curve of Pt/CuO/Pt structure in negative turn on and negative turn off switching mode.

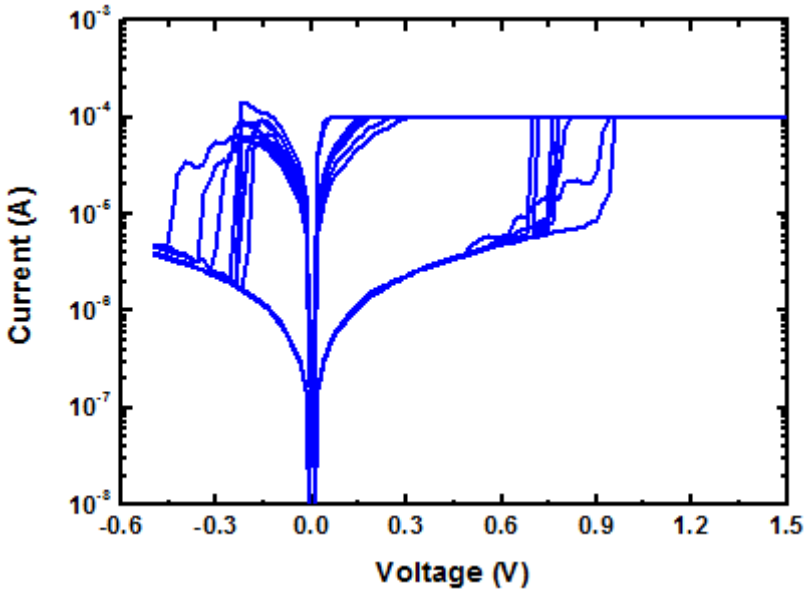


Figure 3.14. *I-V* curve of W-probe/CuO/Pt structure in positive turn on and negative turn off switching mode.

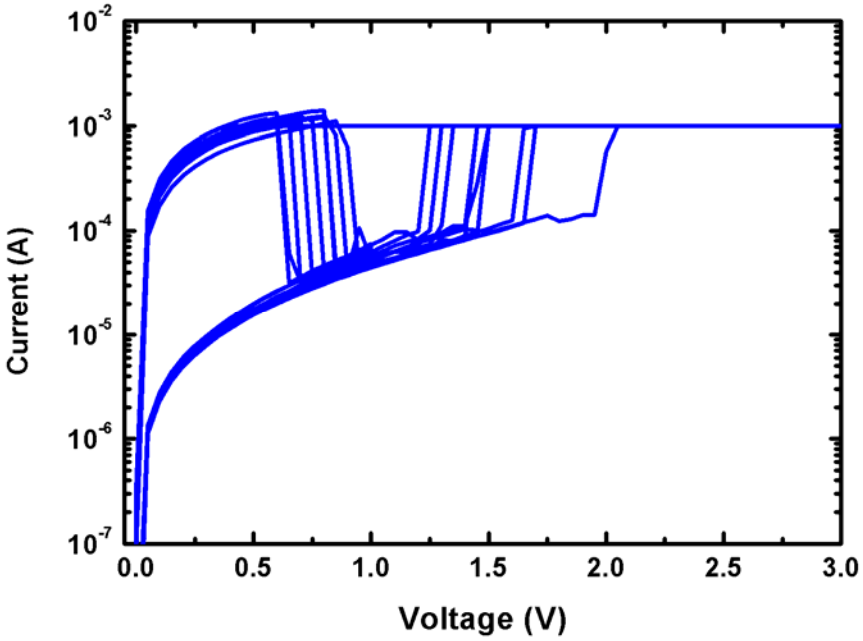


Figure 3.15. *I-V* curve of W-probe/CuO/Pt structure in positive turn on and positive turn off switching mode.

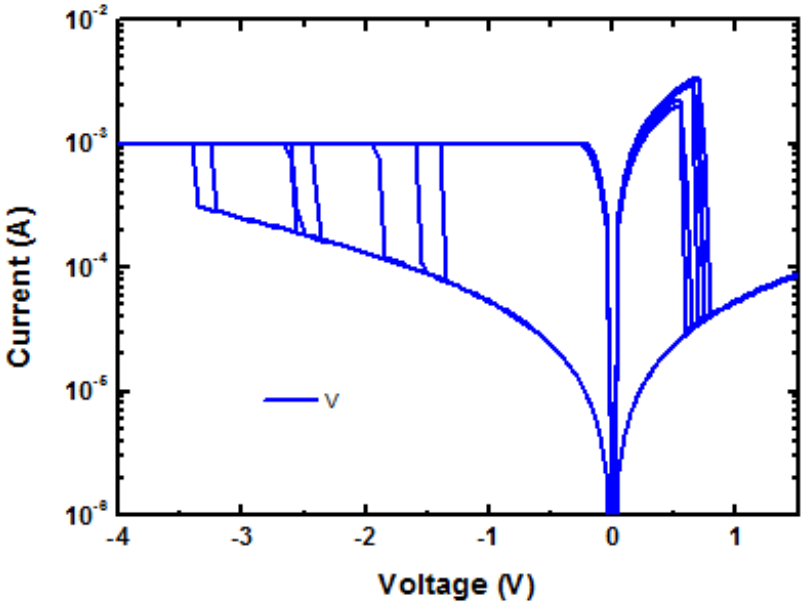


Figure 3.16. *I-V* curve of W-probe/CuO/Pt structure in negative turn on and positive turn off switching mode.

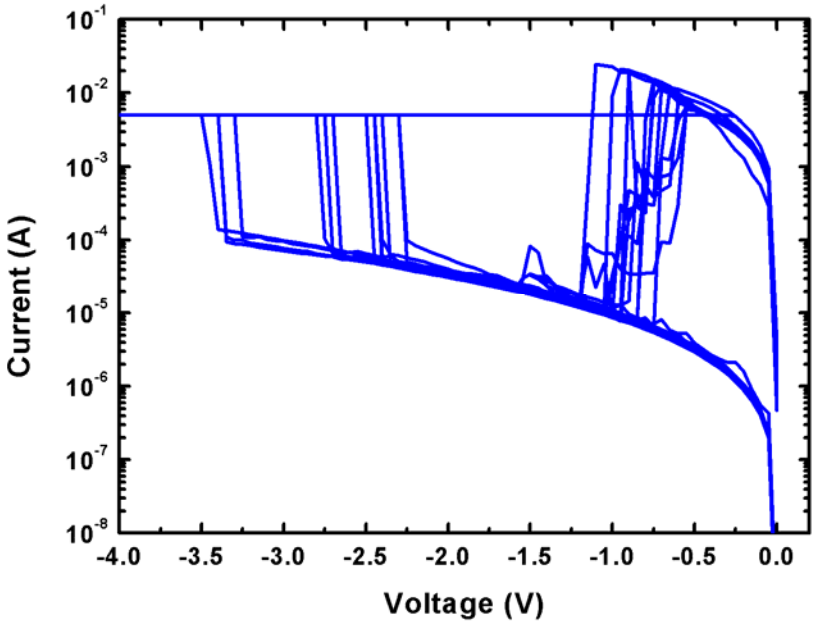


Figure 3.17. *I-V* curve of W-probe/CuO/Pt structure in negative turn on and negative turn off switching mode.

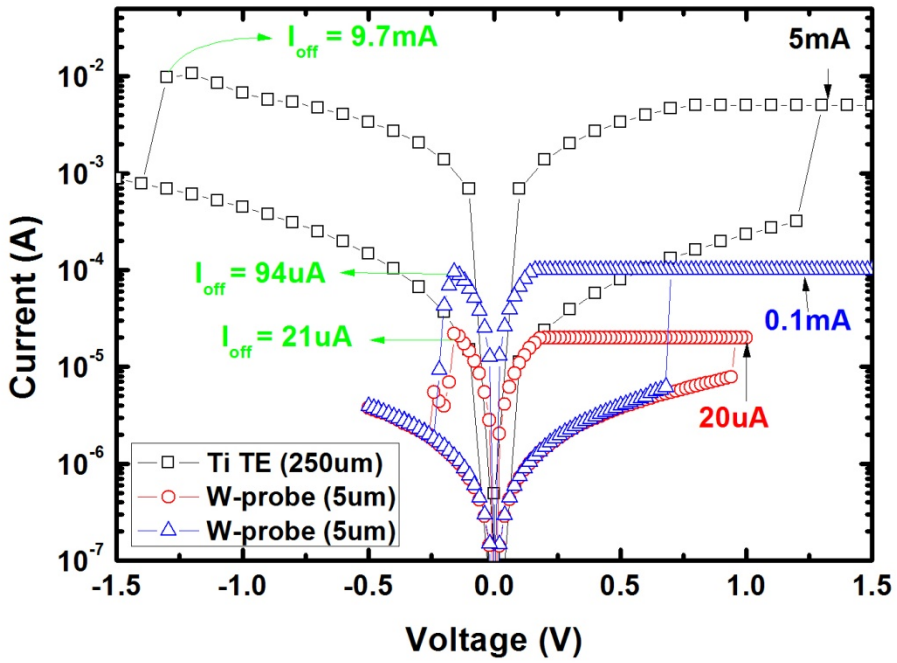


Figure 3.18. *I-V* curve of W-probe/CuO/Pt structure and Ti/CuO/Pt structure.

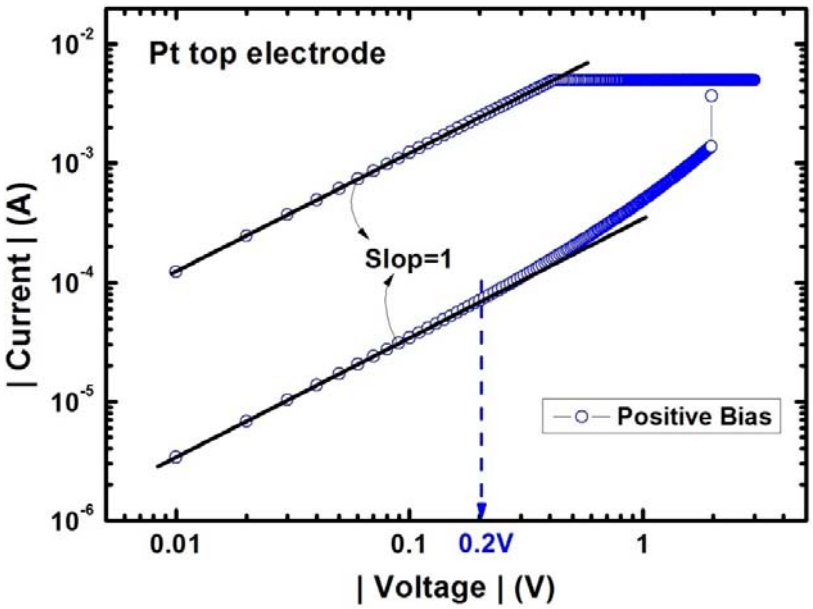


Figure 3.19. Current fitting of Ohmic conduction in turn-on process at the positive bias region for Pt top electrode.

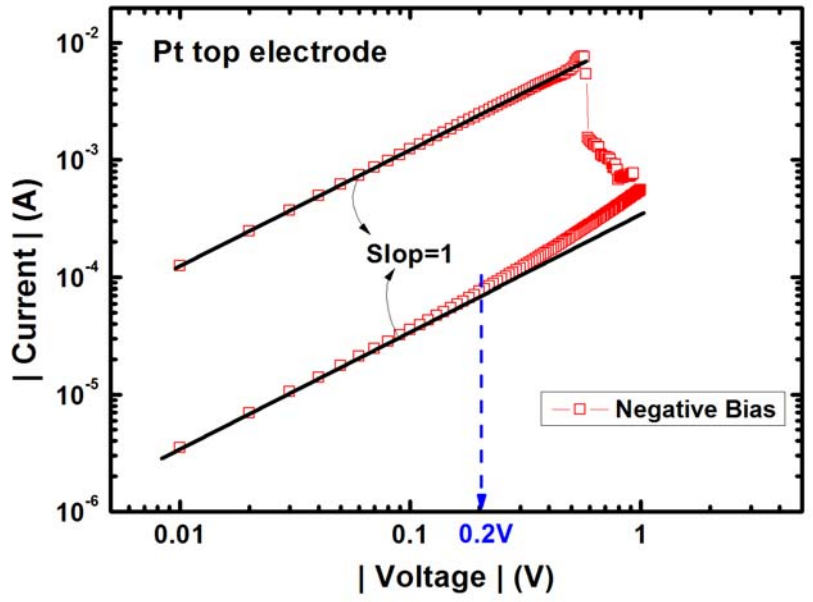


Figure 3.20. Current fitting of Ohmic conduction in turn off process at the negative bias region for Pt top electrode.

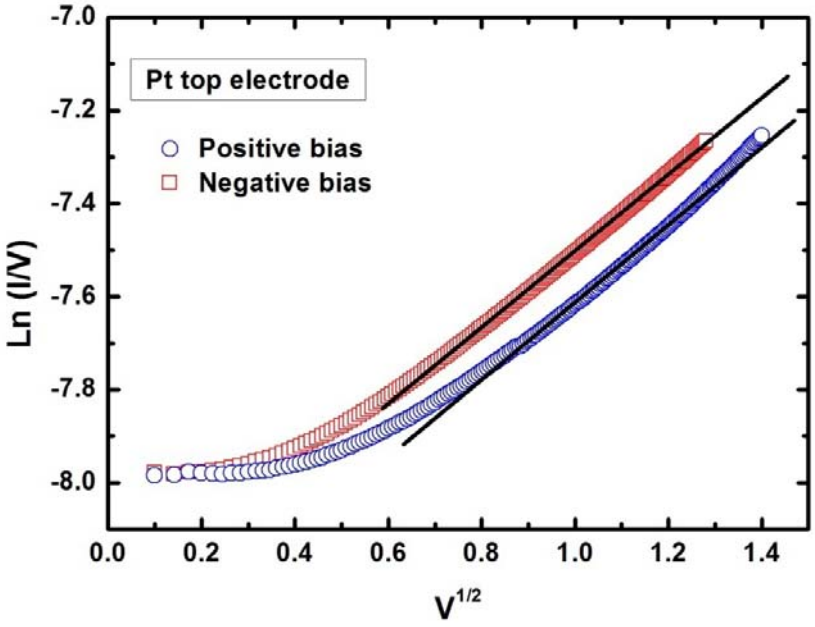


Figure 3.21. *I-V* curves were well fitted by the formula of Poole–Frenkel emission model with Pt top electrode.

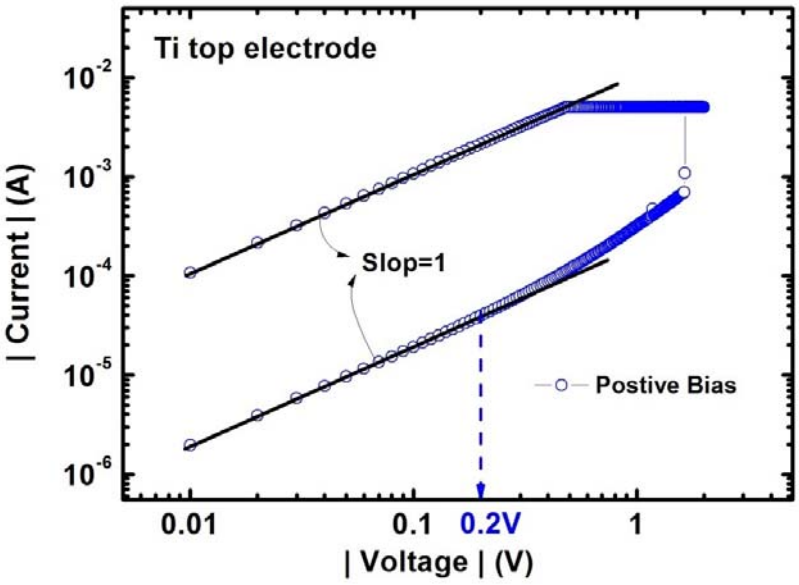


Figure 3.22. Current fitting of Ohmic conduction in turn-on process at the positive bias region for Ti top electrode.

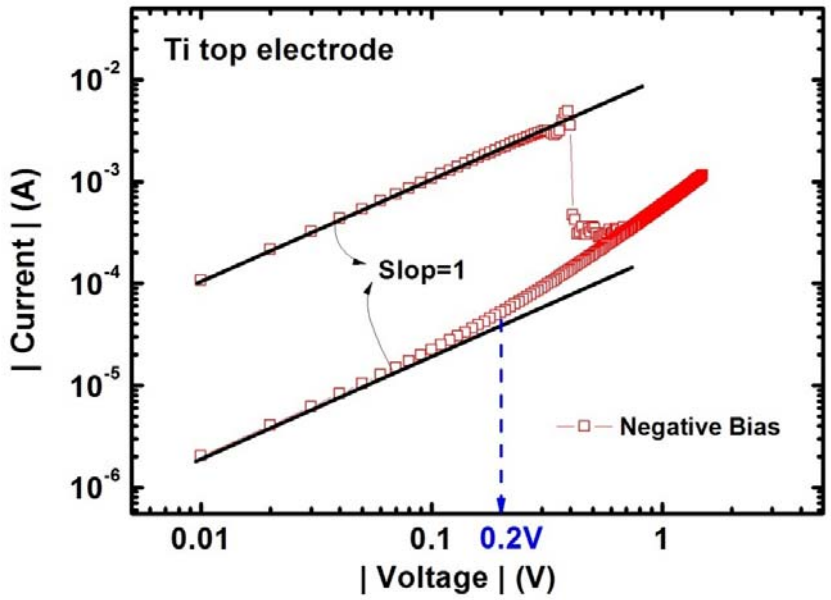


Figure 3.23. Current fitting of Ohmic conduction in turn off process at the negative bias region for Ti top electrode.

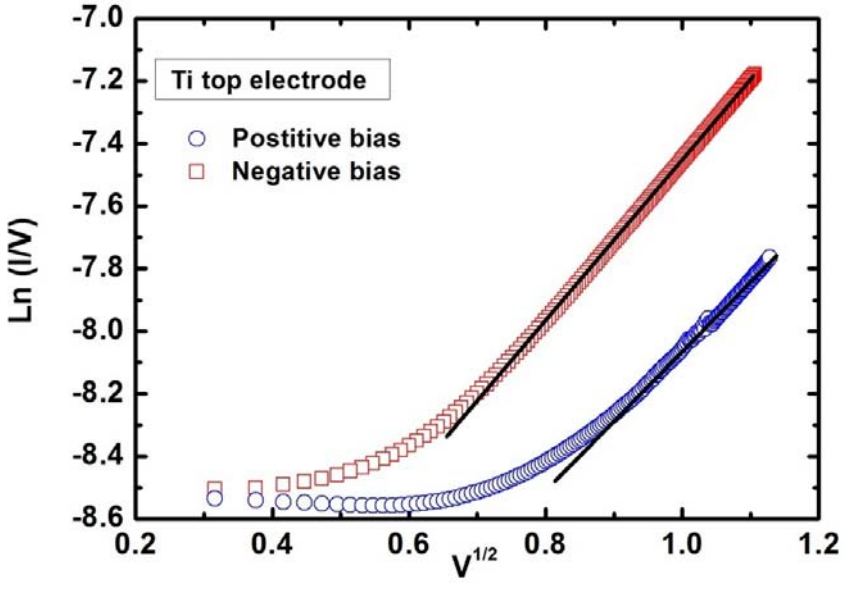


Figure 3.24. *I-V* curves were well fitted by the formula of Poole–Frenkel emission model with Ti top electrode.

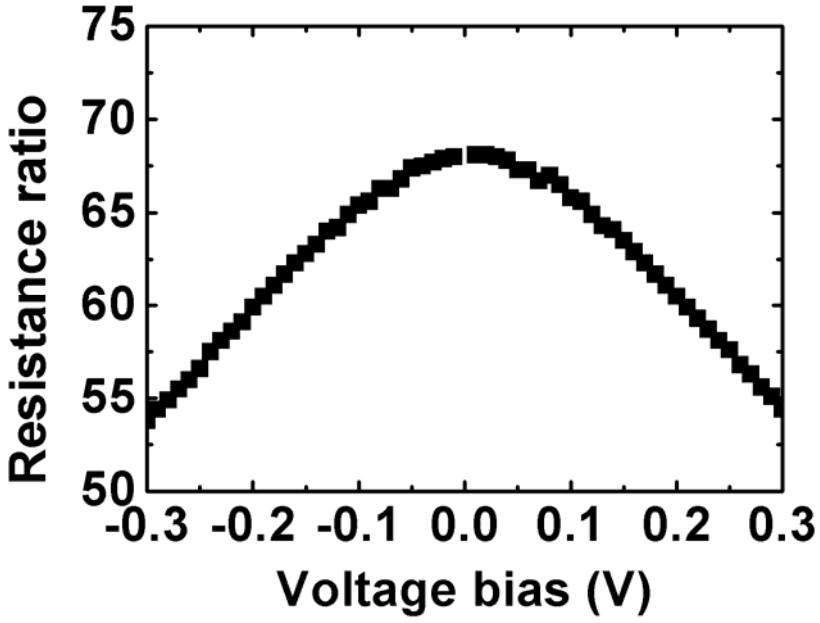


Figure 3.25. The on/off ratio of various voltage bias.

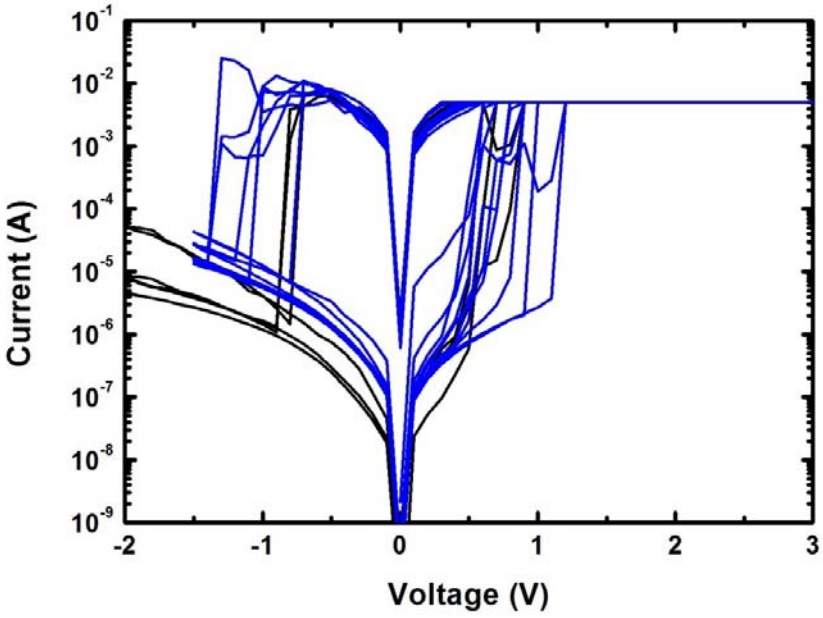


Figure 3.26. *I-V* curve of Ti/CuO/Pt structure with top electrode area 10um*10um.

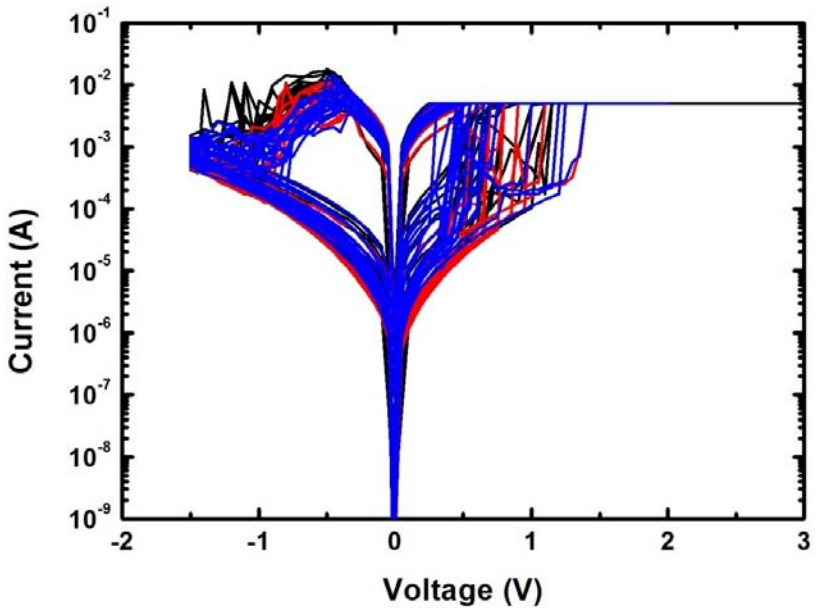


Figure 3.27. *I-V* curve of Ti/CuO/Pt structure with top electrode diameter 150um.

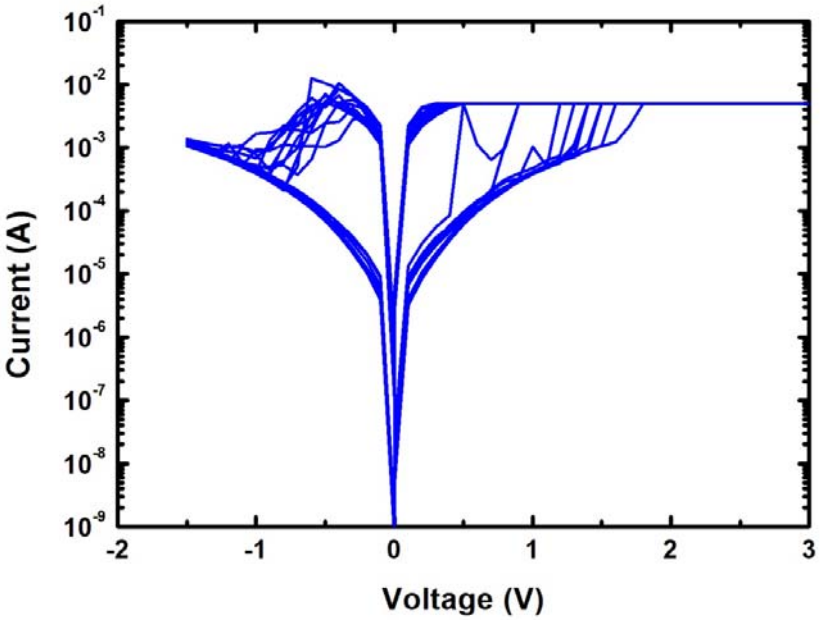


Figure 3.28. *I-V* curve of Ti/CuO/Pt structure with top electrode diameter 250um.

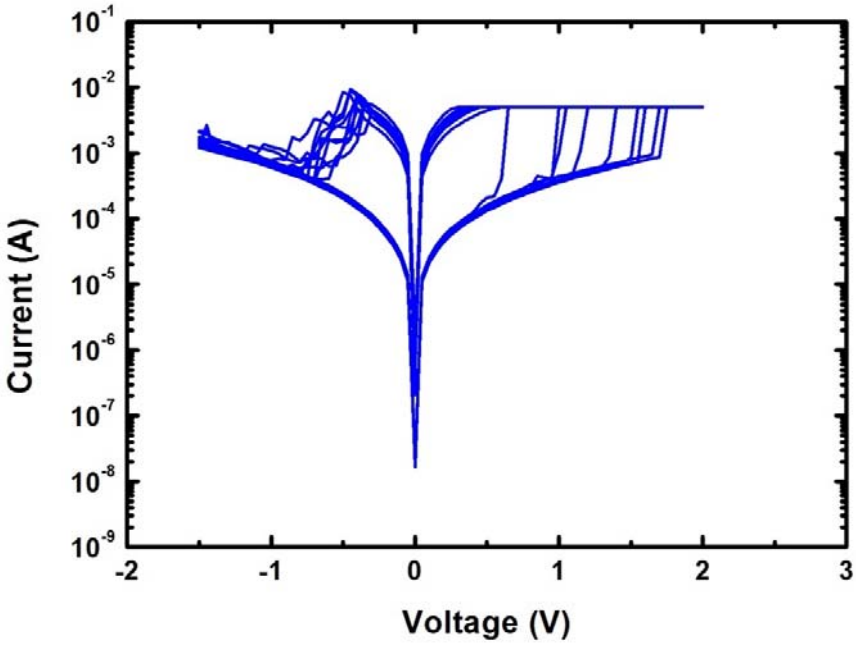


Figure 3.29. *I-V* curve of Ti/CuO/Pt structure with top electrode diameter 350um.

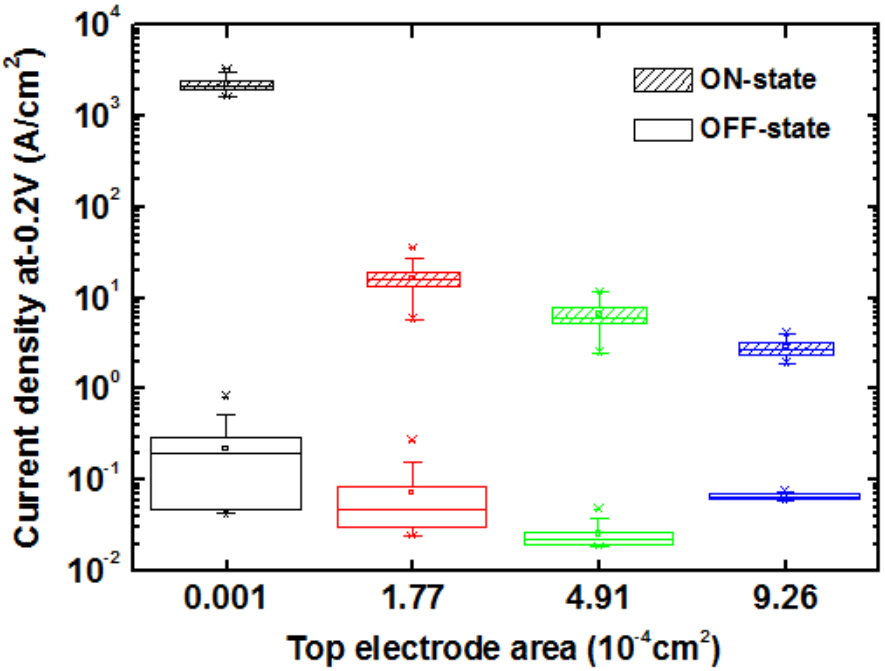


Figure 3.30. Statistics plot of ON-state and OFF-state current density at various area of top electrode.

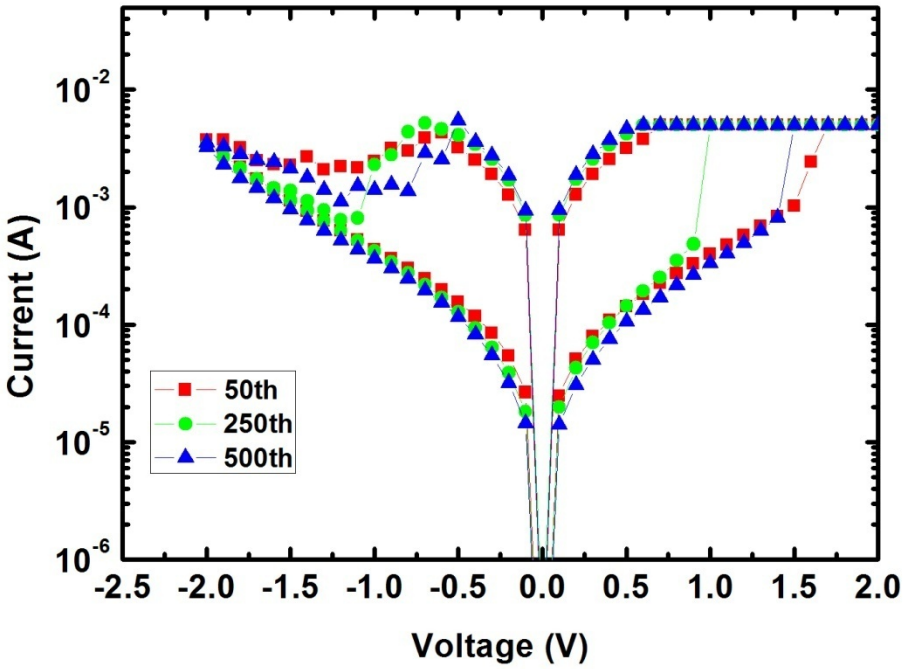


Figure 3.31. *I-V* curves of the 50th, 250th, and 500th cycles switched.

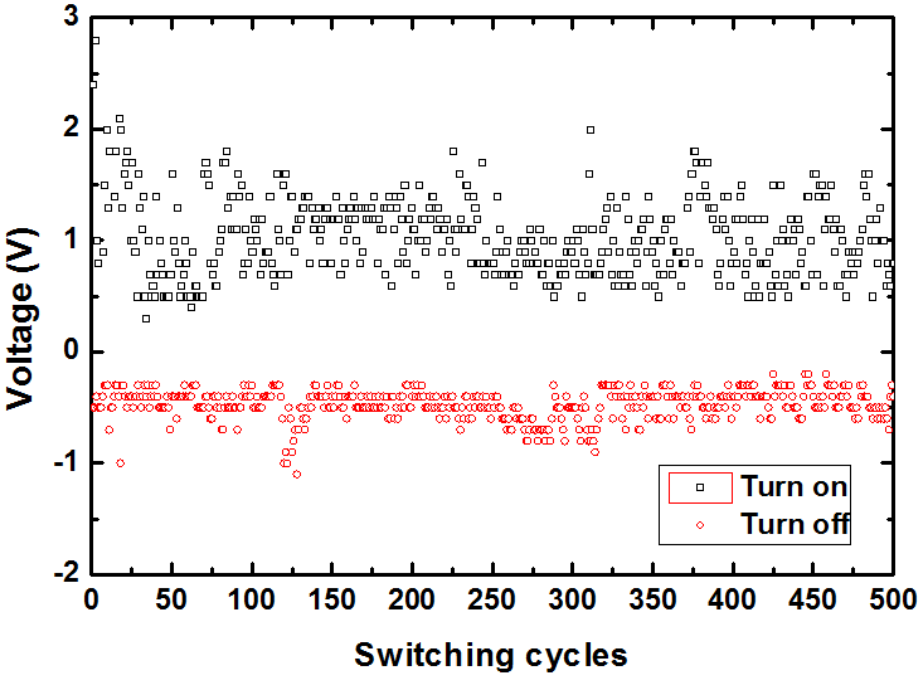


Figure 3.32. Switching cycles for turn-on voltage and turn-off voltage.

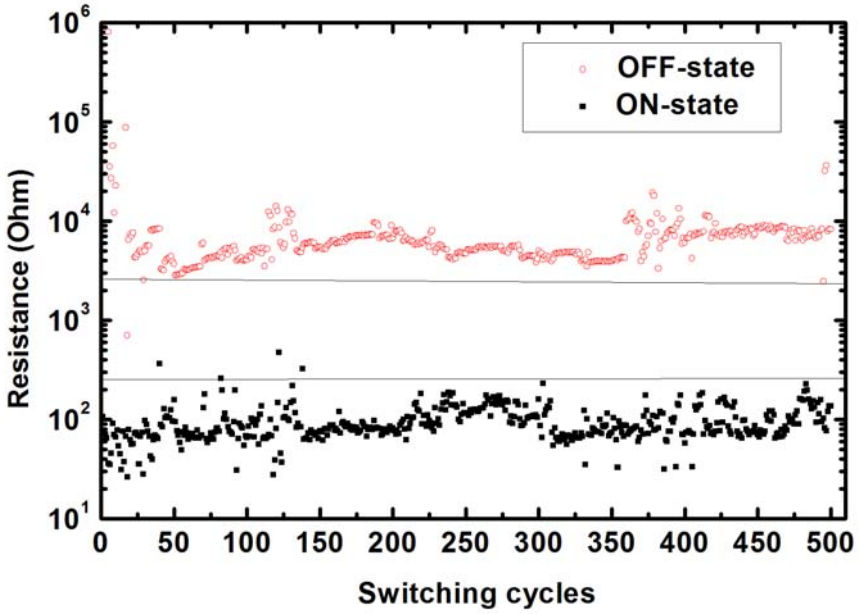


Figure 3.33. Ti/CuO/Pt devices of switching cycles for resistance at 0.2V of ON-State and OFF-state.

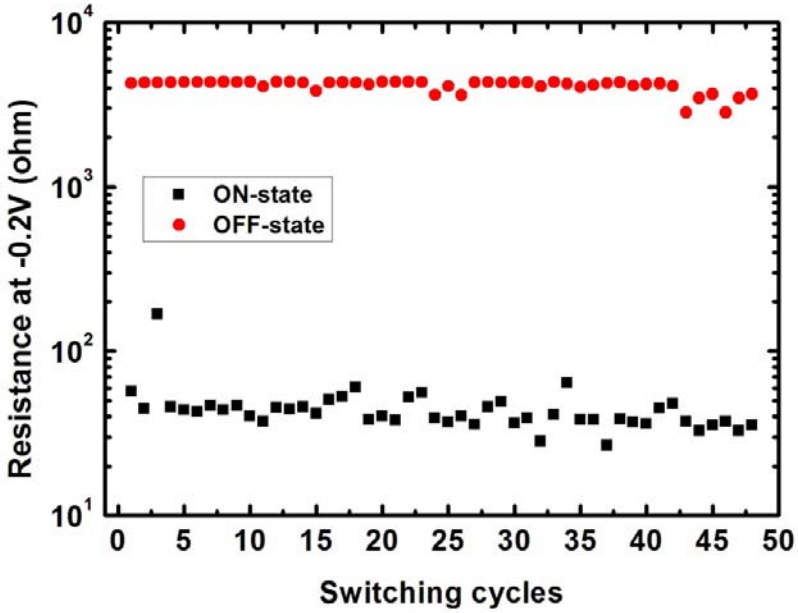


Figure 3.34. Pt/CuO/Pt devices of switching cycles for resistance at 0.2V of ON-State and OFF-state.

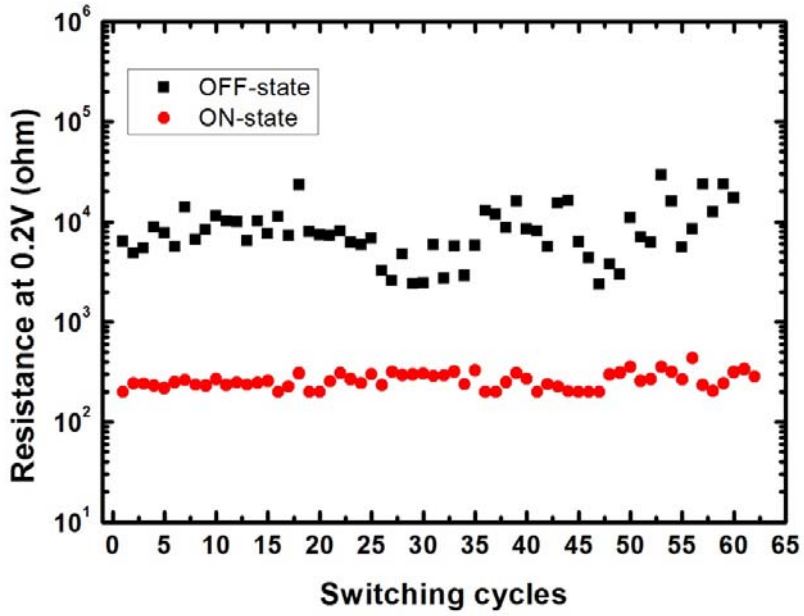


Figure 3.35. W-probe/CuO/Pt devices of switching cycles for resistance at 0.2V of ON-State and OFF-state.

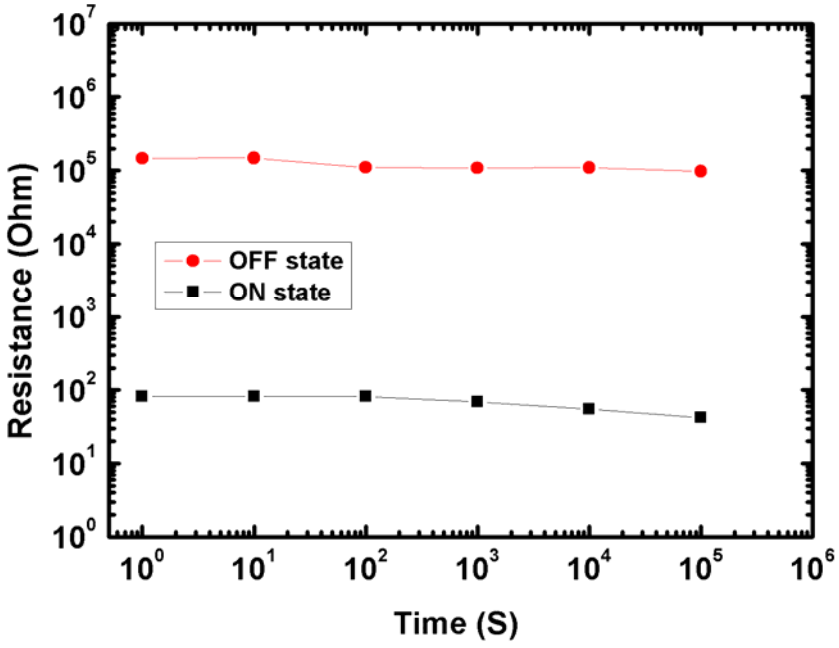


Figure 3.36. Plot of retention characteristics of ON and OFF-states.

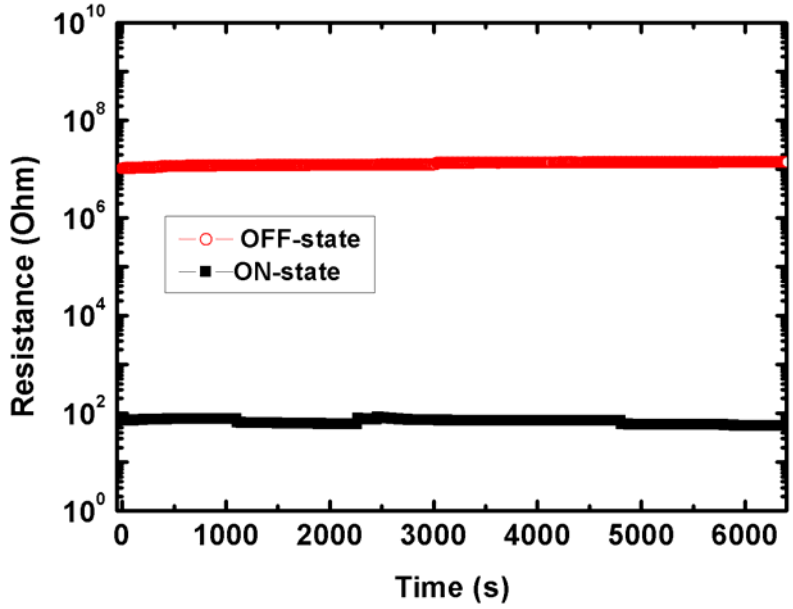


Figure 3.37. Stress characteristics of ON and OFF-states under 0.2V with Ti top electrode.

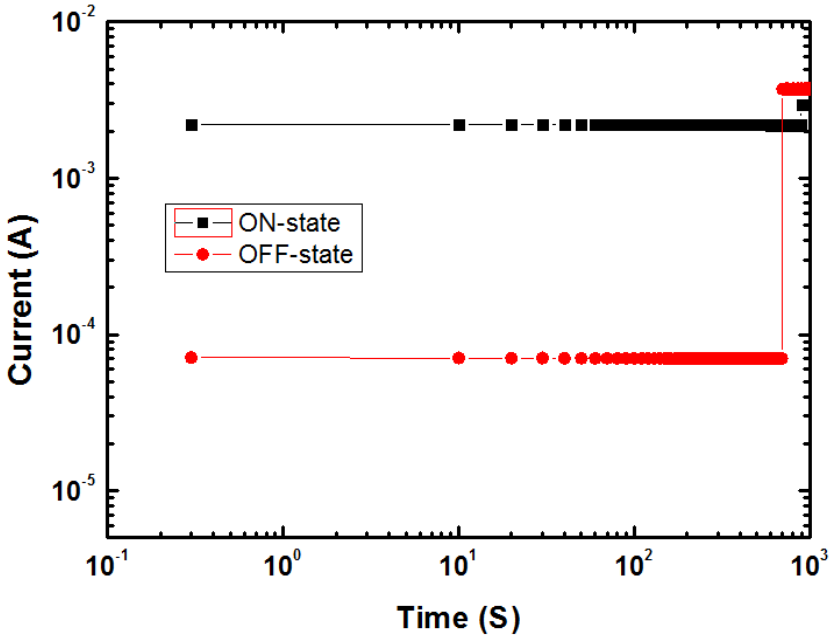


Figure 3.38. Stress characteristics of ON and OFF-states under 0.2V with Pt top electrode.

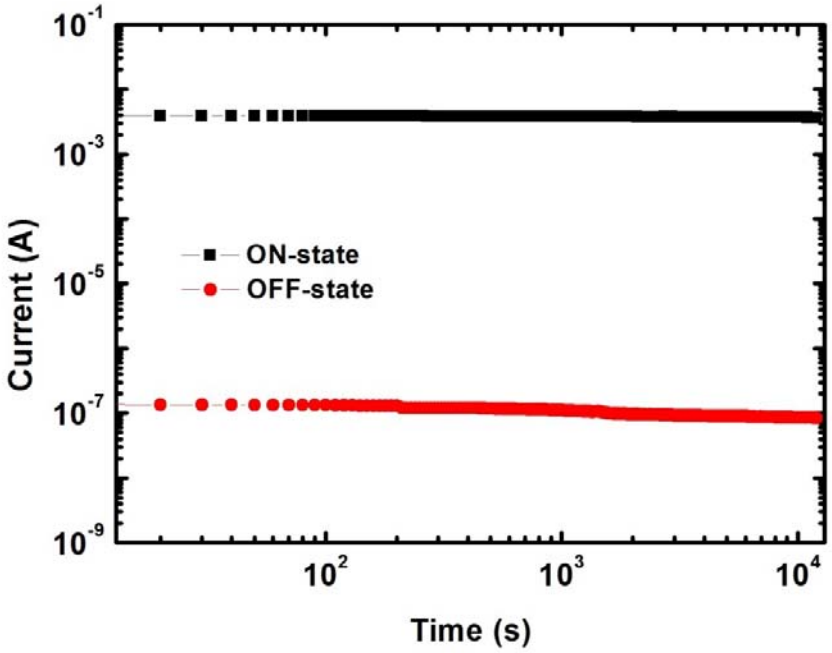


Figure 3.39. Stress characteristics of ON and OFF-states under 0.2V with Ni top electrode.

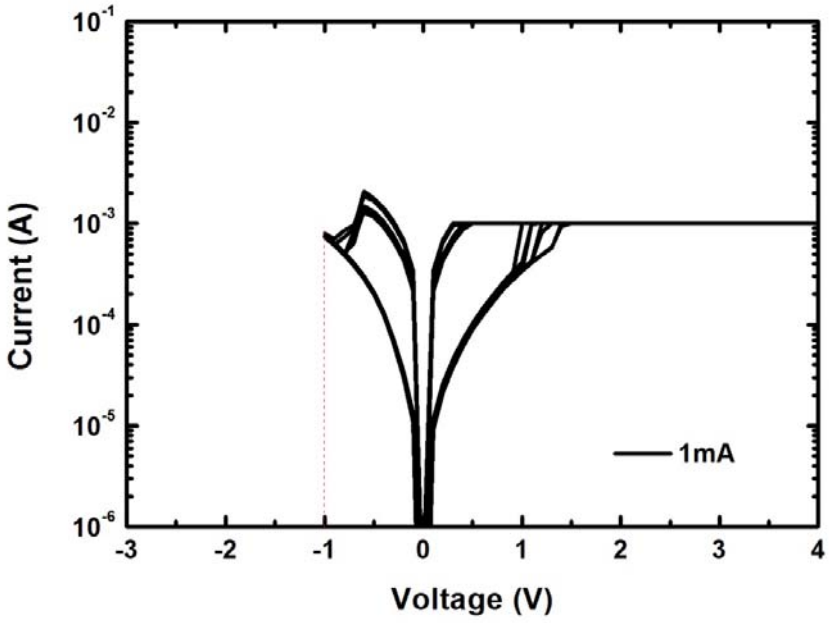


Figure 3.40. *I-V* curve were measured with a current compliance 1mA.

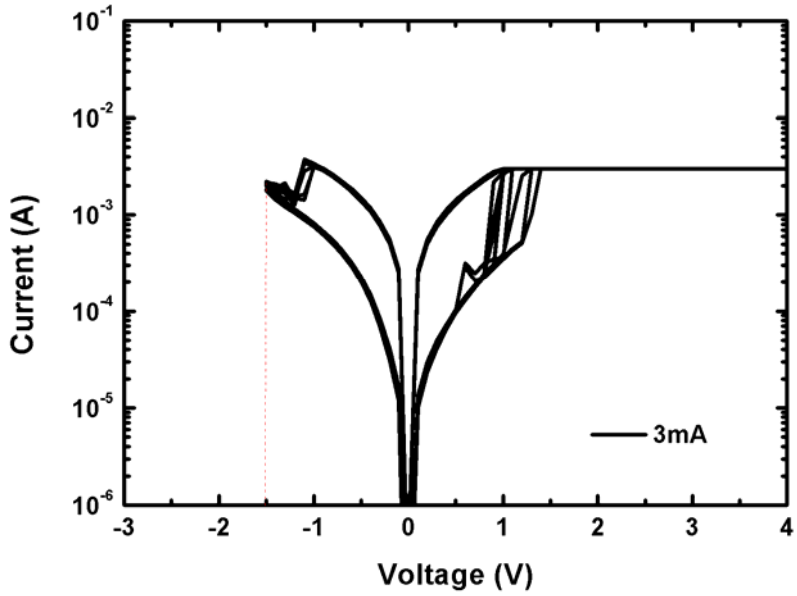


Figure 3.41. *I-V* curve were measured with a current compliance 3mA.

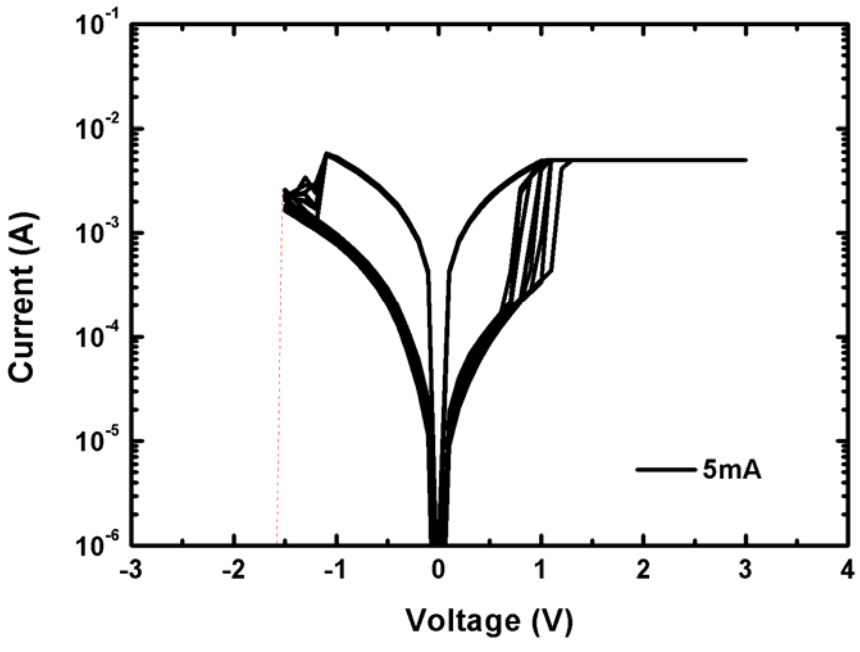


Figure 3.42. *I-V* curve were measured with a current compliance 5mA.

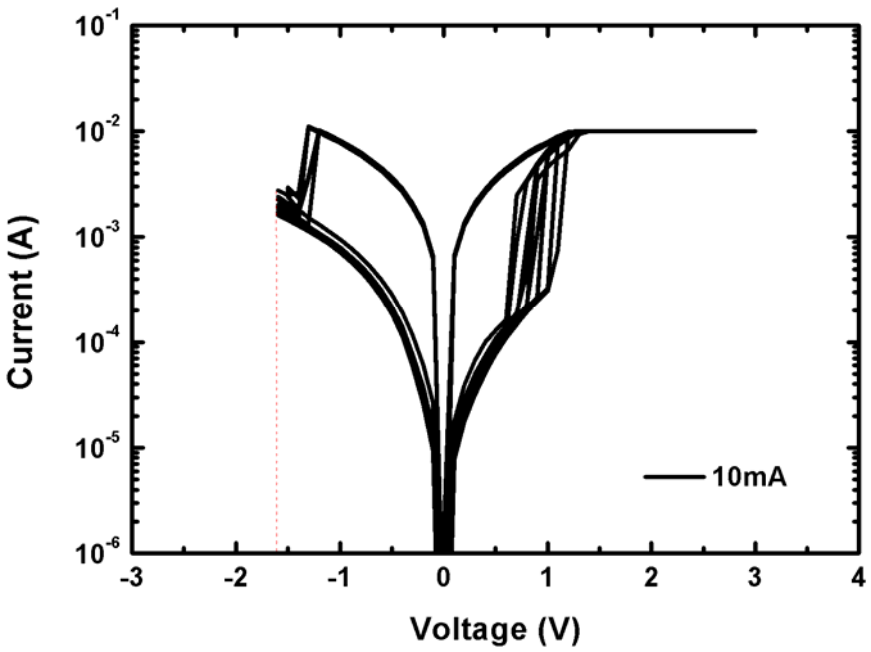


Figure 3.43. *I-V* curve were measured with a current compliance 10mA.

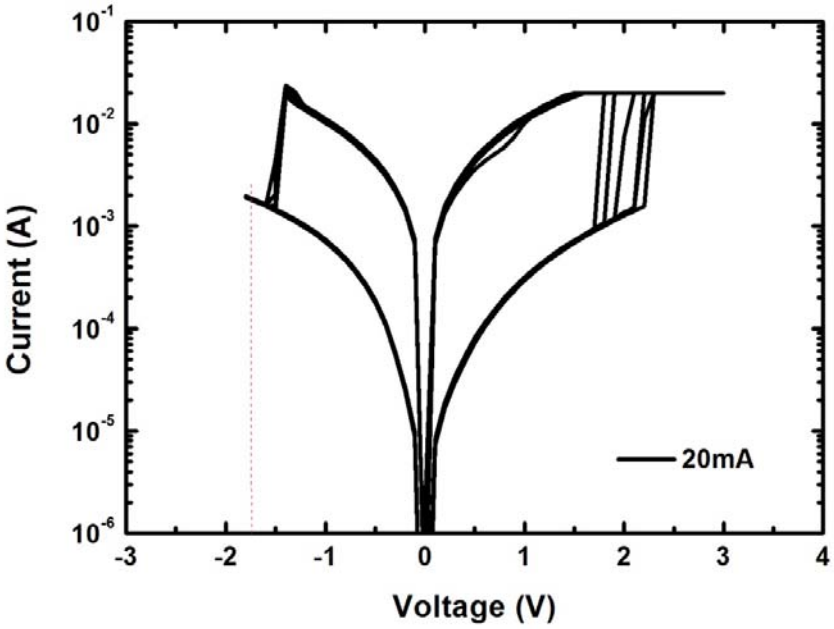


Figure 3.44. *I-V* curve were measured with a current compliance 20mA.

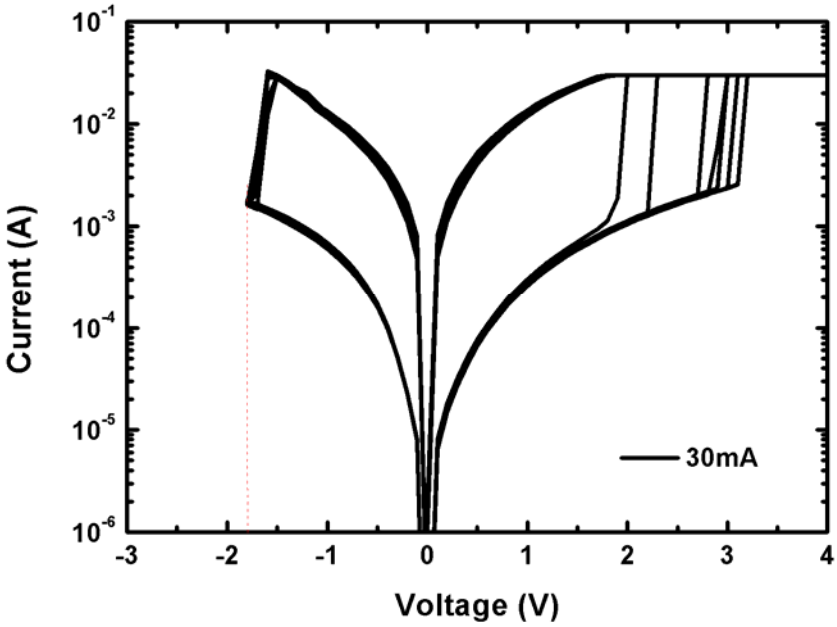


Figure 3.45. *I-V* curve were measured with a current compliance 30mA.

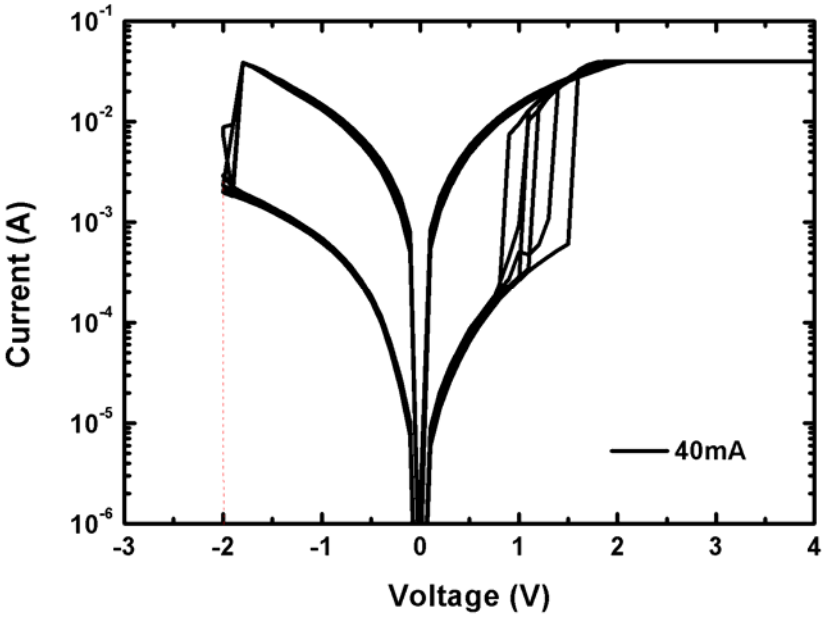


Figure 3.46. *I-V* curve were measured with a current compliance 40mA.

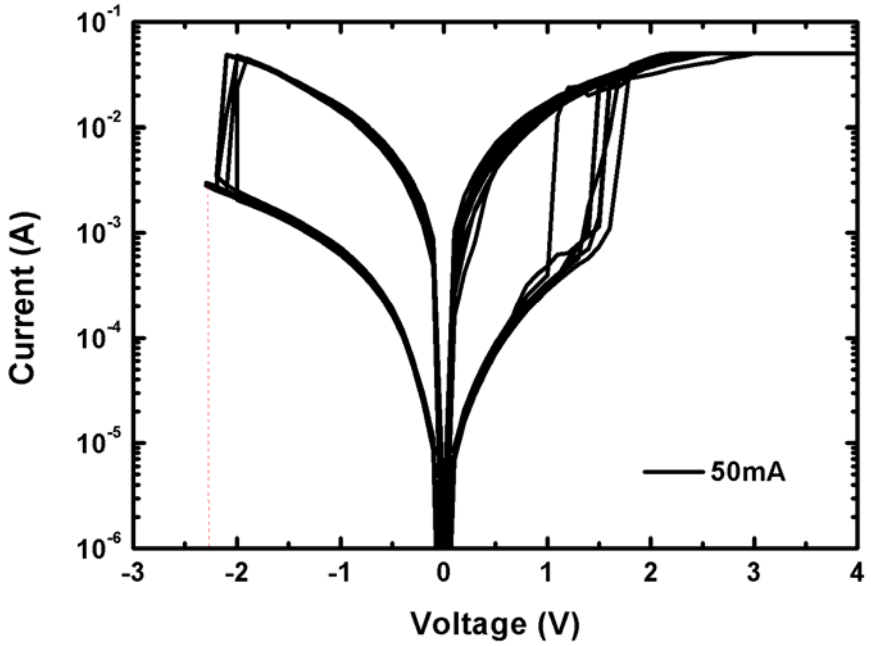


Figure 3.47. *I-V* curve were measured with a current compliance 50mA.

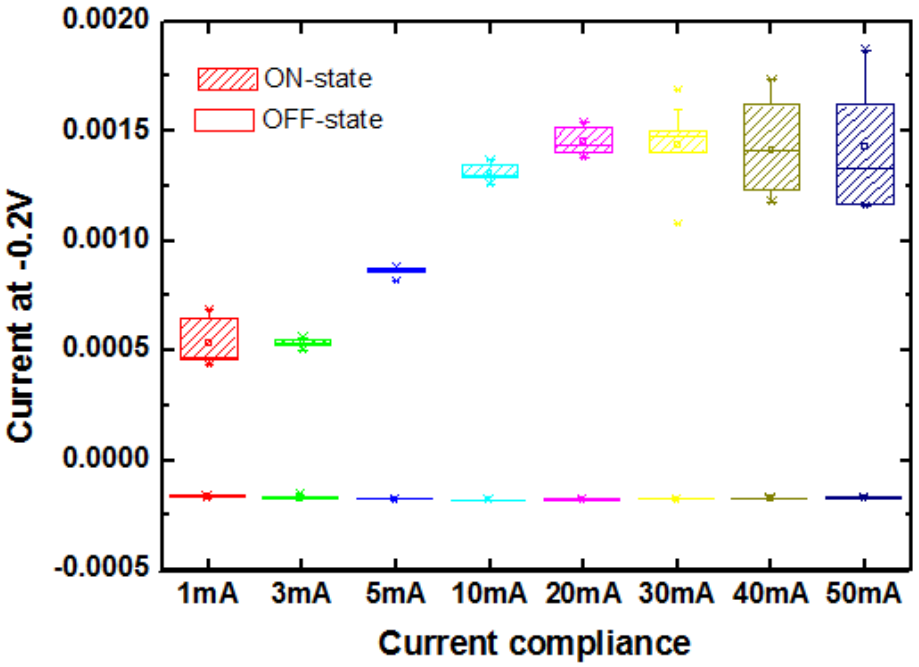


Figure 3.48. Statistics plot of ON-current and OFF-current at -0.2V with different current compliance.

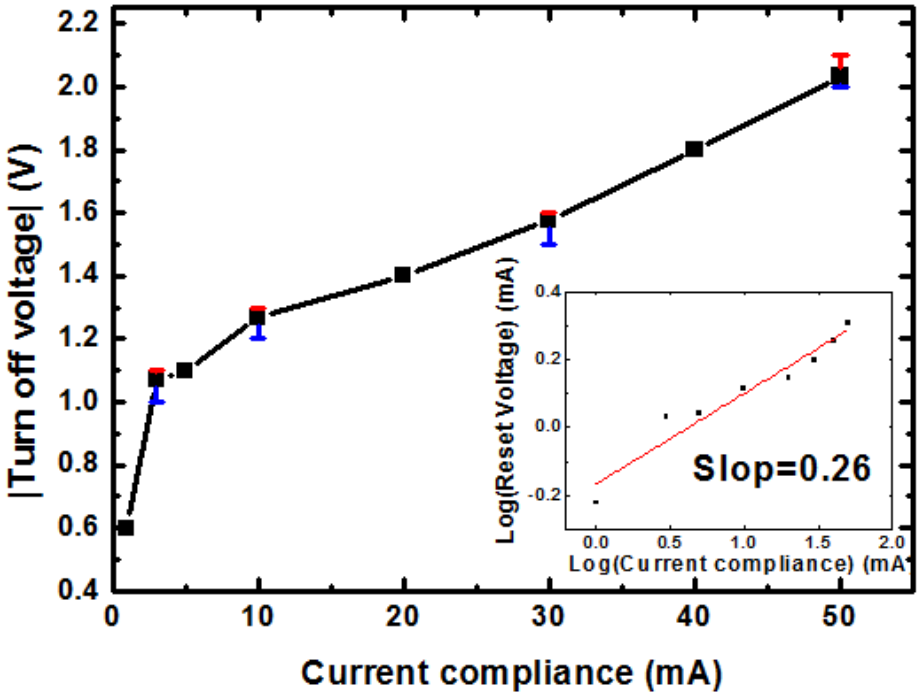


Figure 3.49. Statistics plot of turn off voltage at with different current compliance.

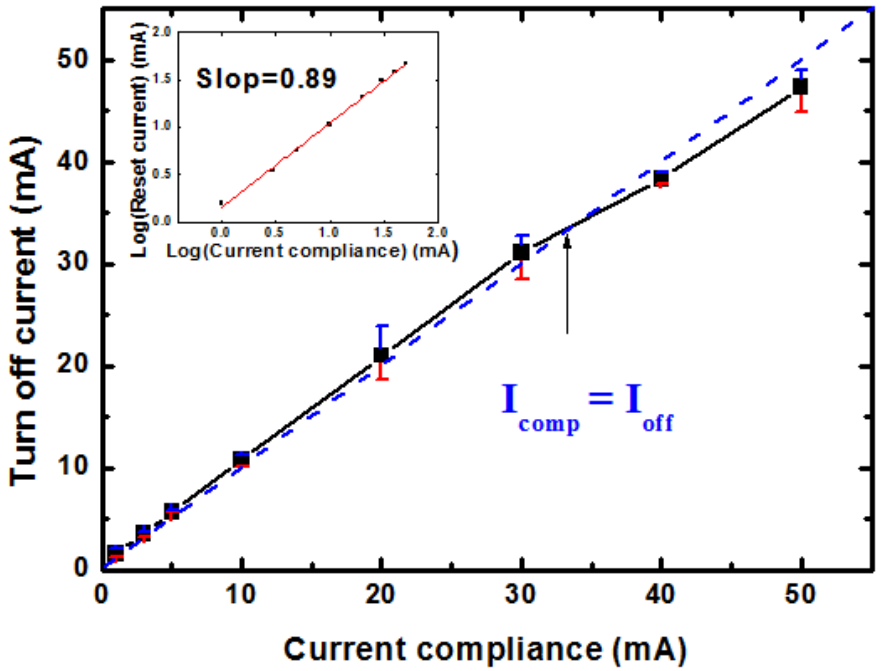


Figure 3.50. Statistics plot of turn off current with different current compliance.

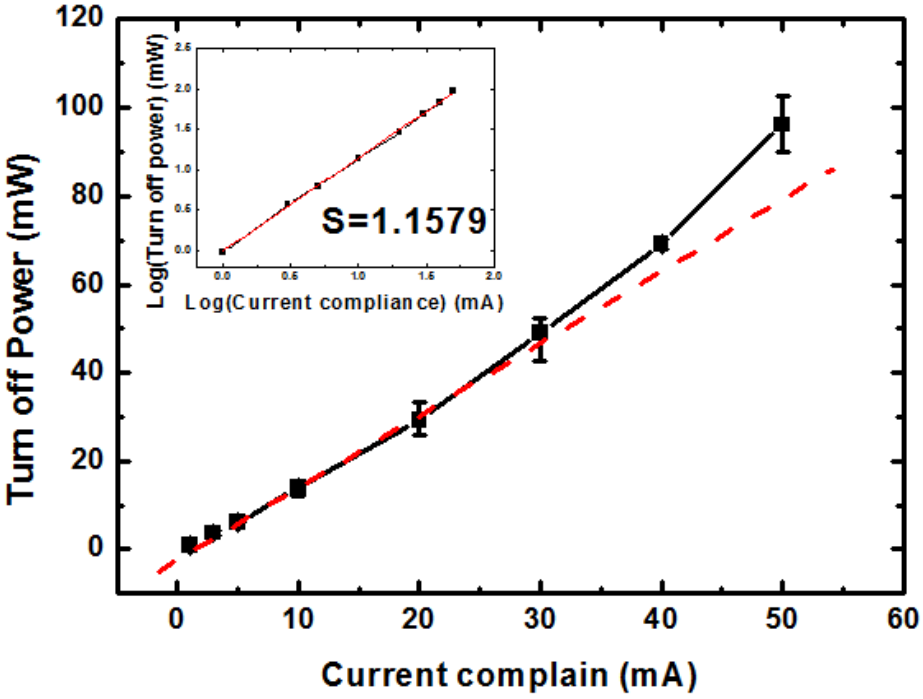


Figure 3.51. Statistics plot of turn off power at with different current compliance.

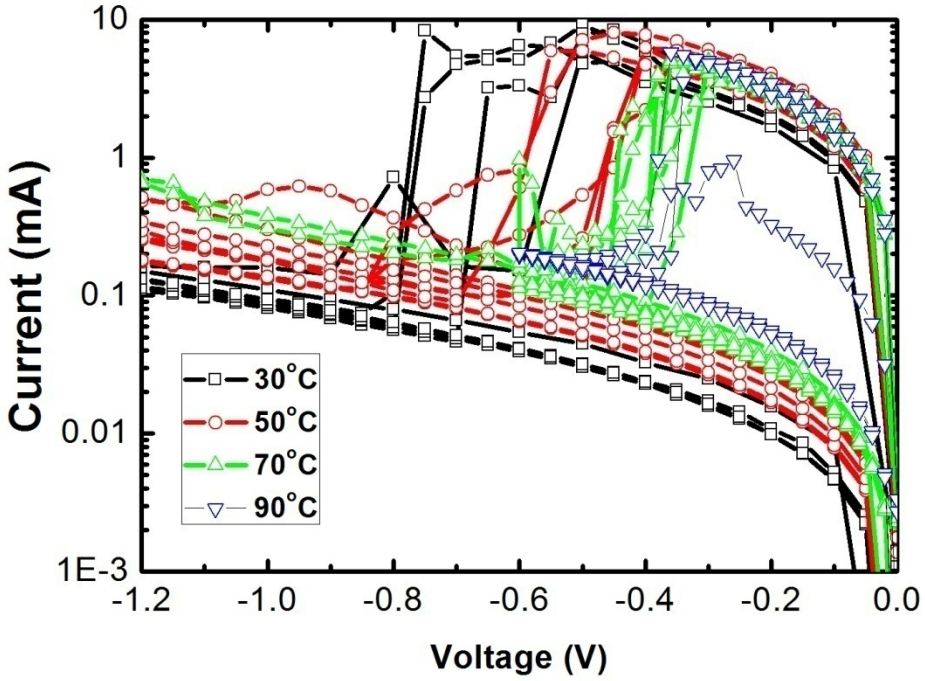


Figure 3.52. Turn off process with different temperature.

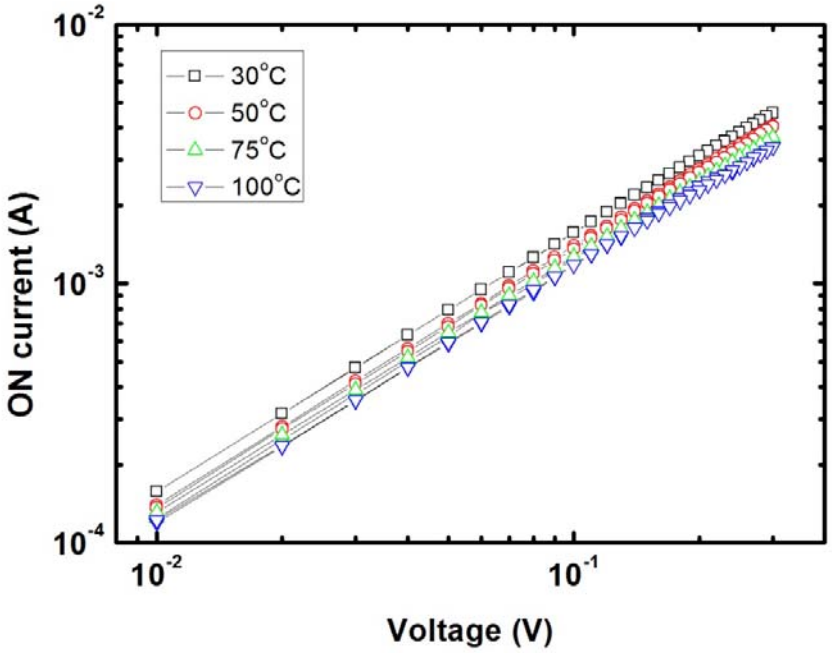


Figure 3.53. ON-state conductivity of measurement at various temperatures.

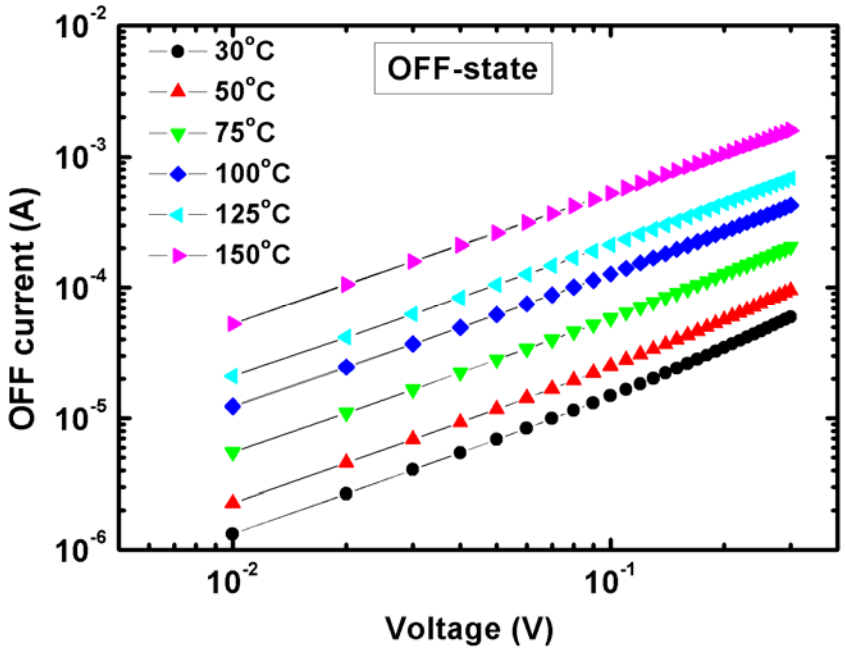


Figure 3.54. OFF-state conductivity of measurement at various temperatures.

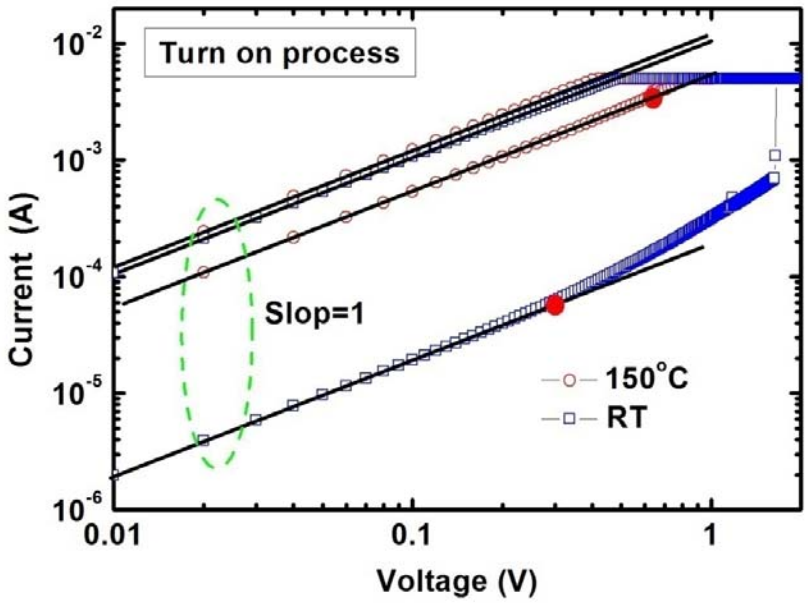


Figure 3.55. Double log *I-V* curve of turn on process at RT and 150°C.

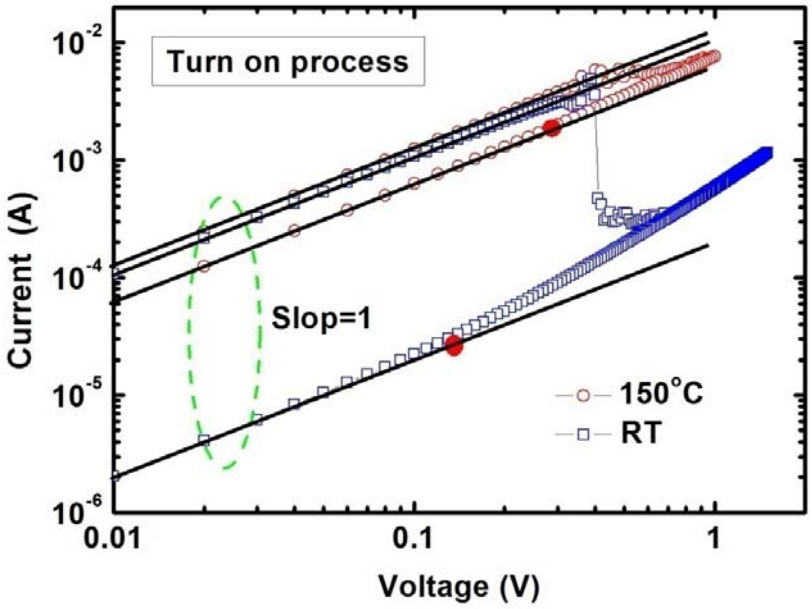


Figure 3.56. Double log *I-V* curve of turn off process at RT and 150°C.

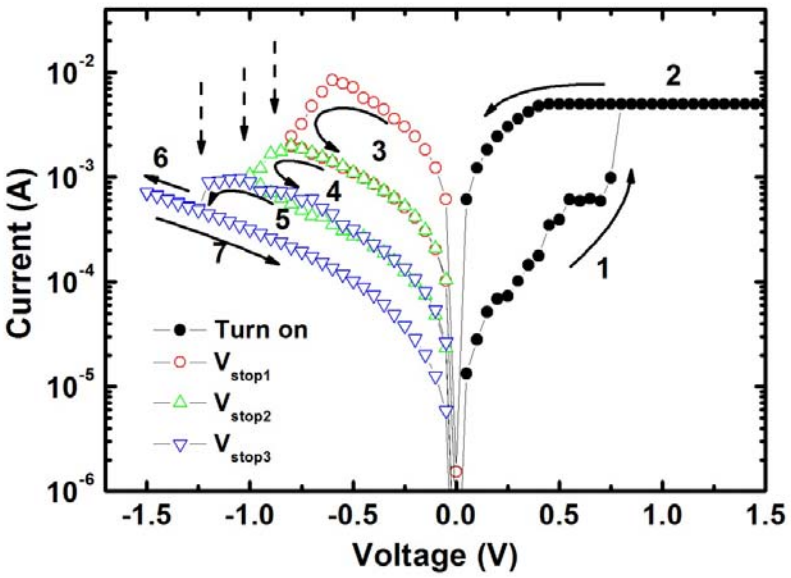


Figure 3.57. Ti/CuO/Pt structure has bipolar switching and intermediate resistance state (IRS).

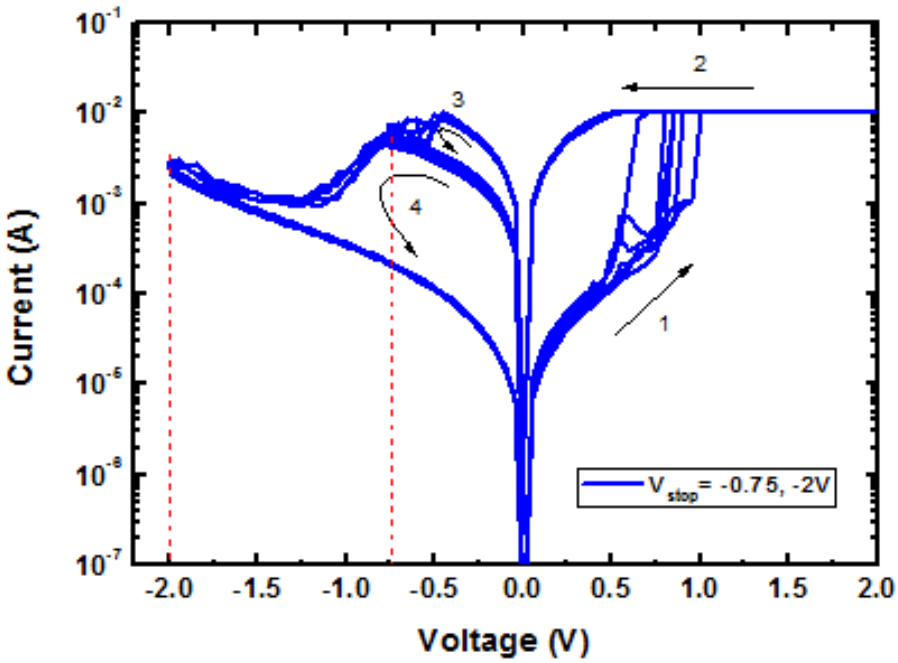


Figure 3.58. Ti/CuO/Pt device be set stop voltage at -0.75V and -2V in a switching cycle.

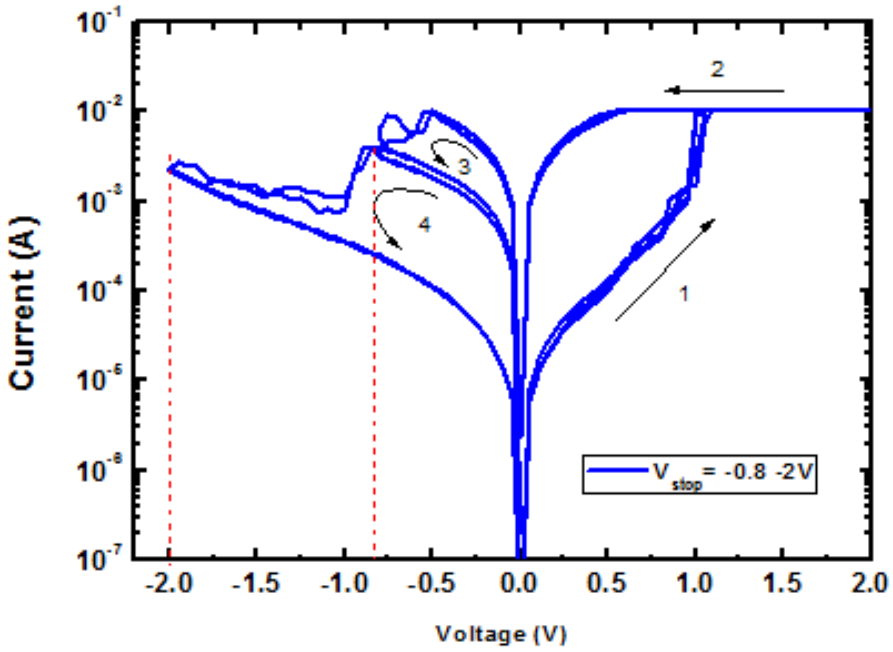


Figure 3.59. Ti/CuO/Pt device be set stop voltage at -0.8V and -2V in a switching cycle.

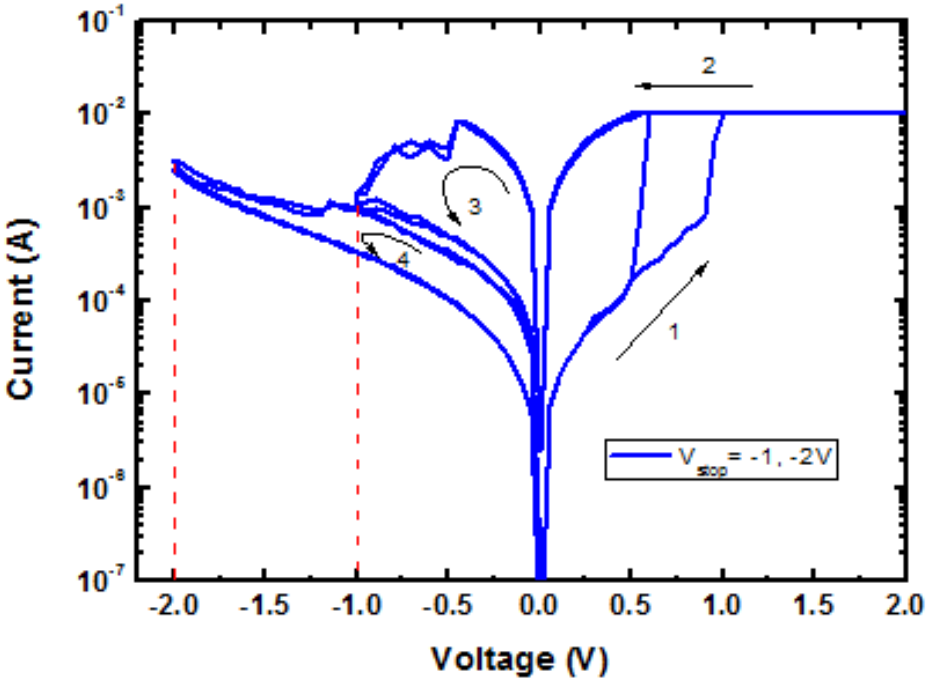


Figure 3.60. Ti/CuO/Pt device be set stop voltage at -1V and -2V in a switching cycle.

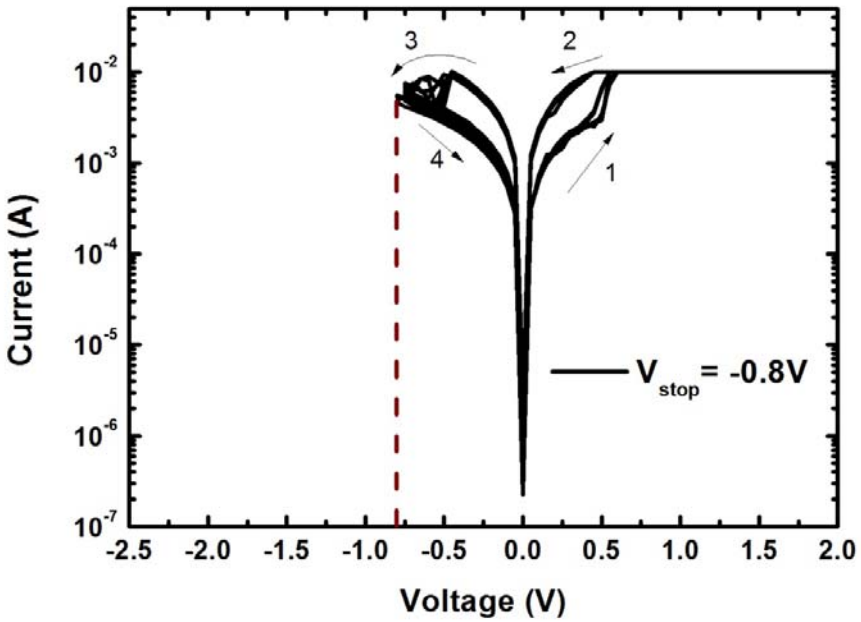


Figure 3.61. *I-V* curve of stop voltage be set at -0.8V.

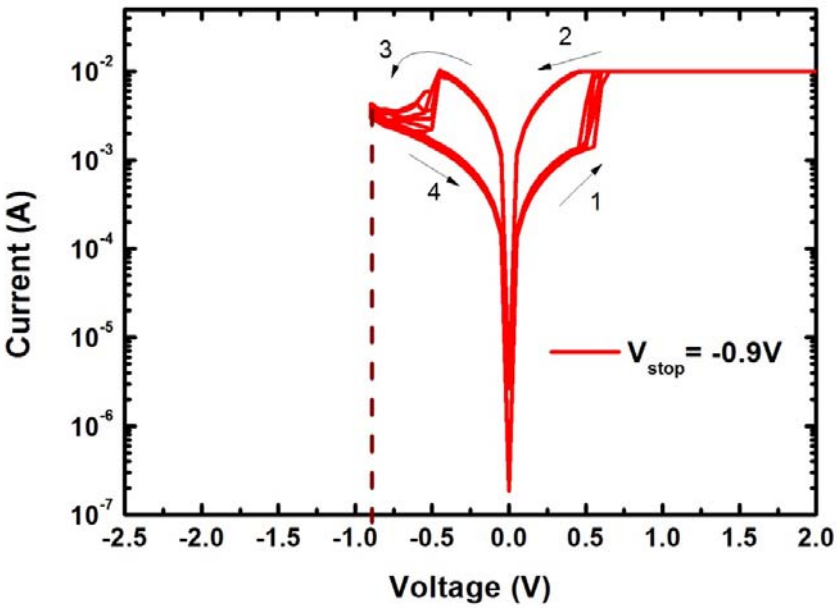


Figure 3.62. *I-V* curve of stop voltage be set at -0.9V.

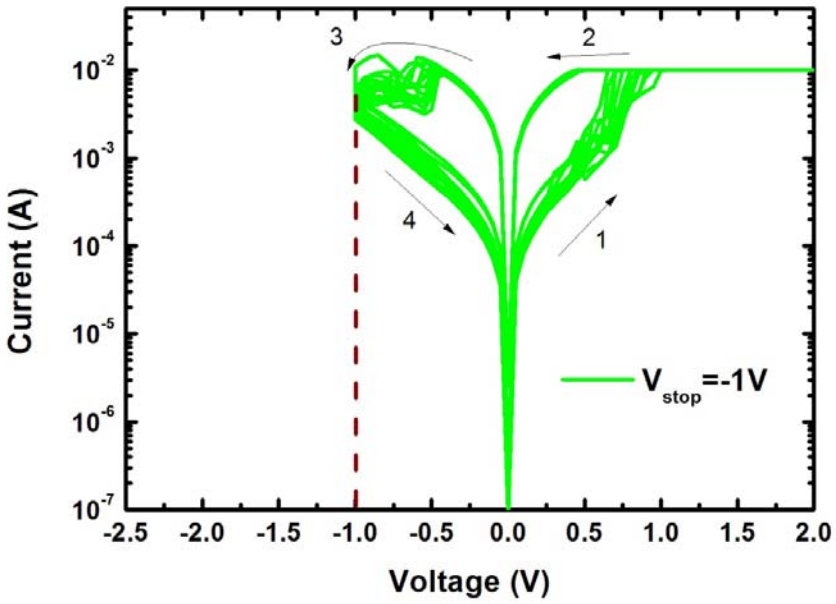


Figure 3.63. *I-V* curve of stop voltage be set at -0.1V.

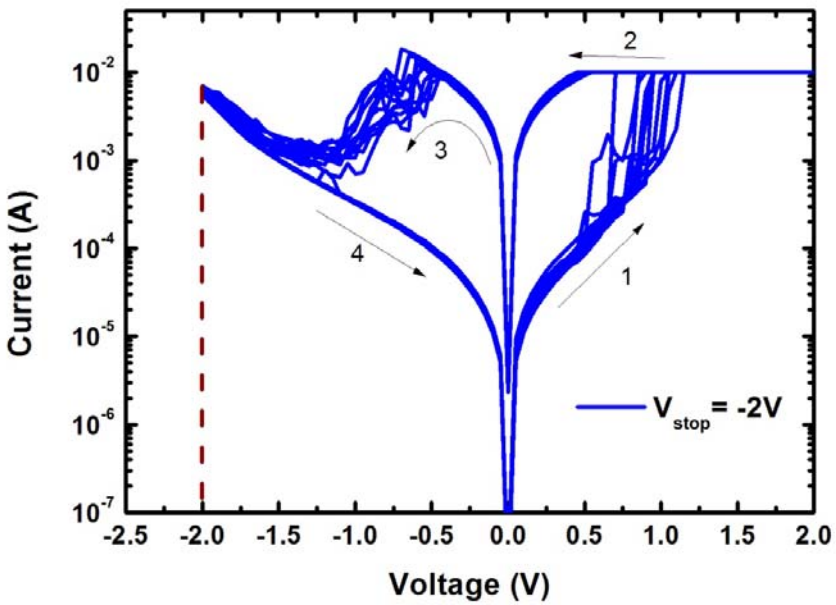


Figure 3.64. *I-V* curve of stop voltage be set at -2V.

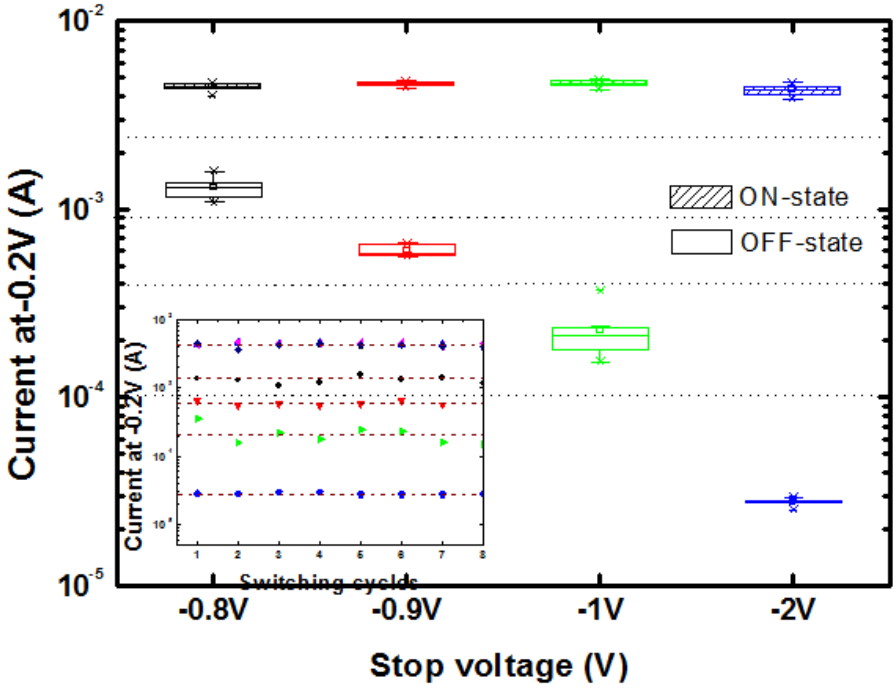


Figure 3.65. Statistics plot of current at -0.2V of ON-state and OFF-state with various stop voltage.

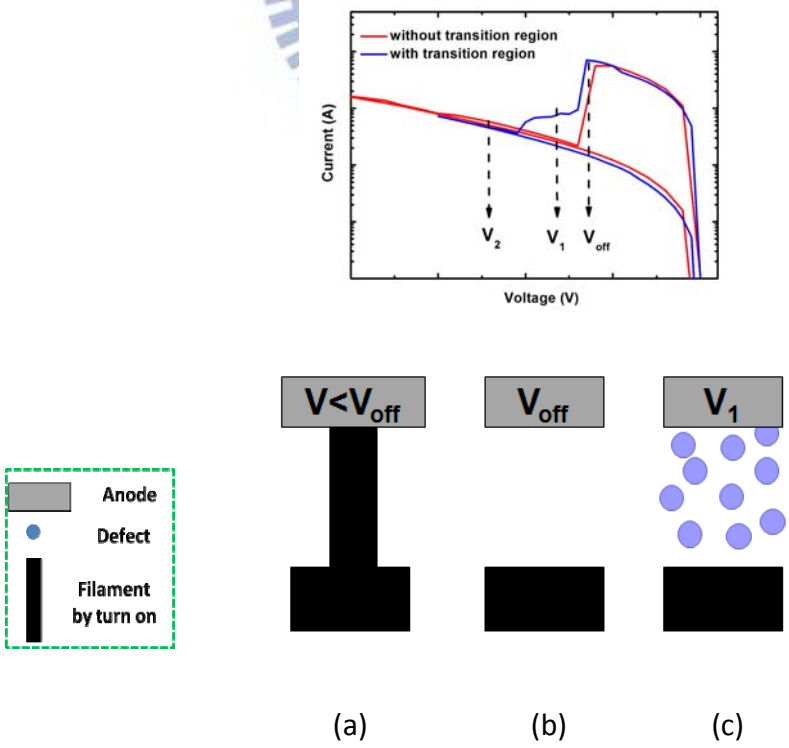
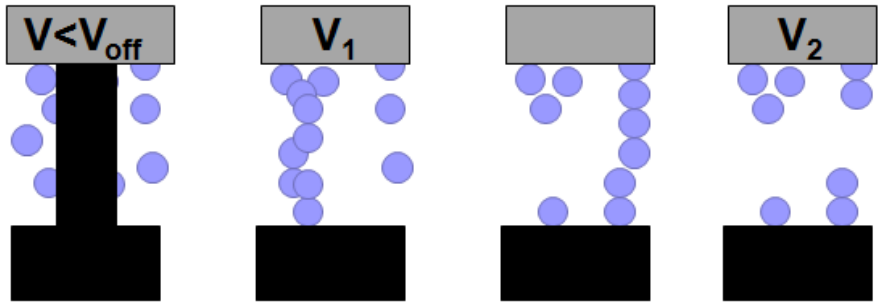
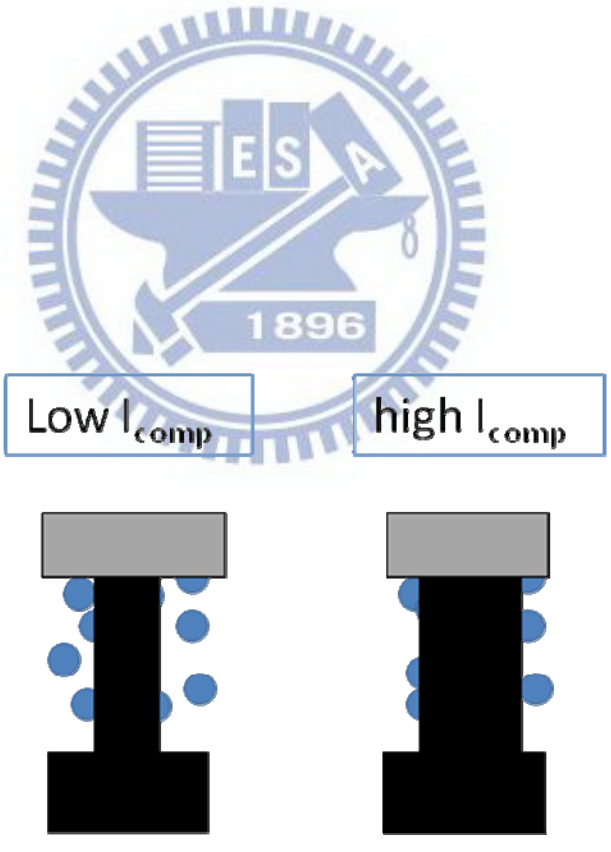


Figure 3.66. Mechanism of turn off process without transition region.



(a) (b) (c) (d)

Figure 3.67. Mechanism of turn off process with transition region.



(a) (b)

Figure 3.68. Mechanism of turn off process with transition region different current compliance.

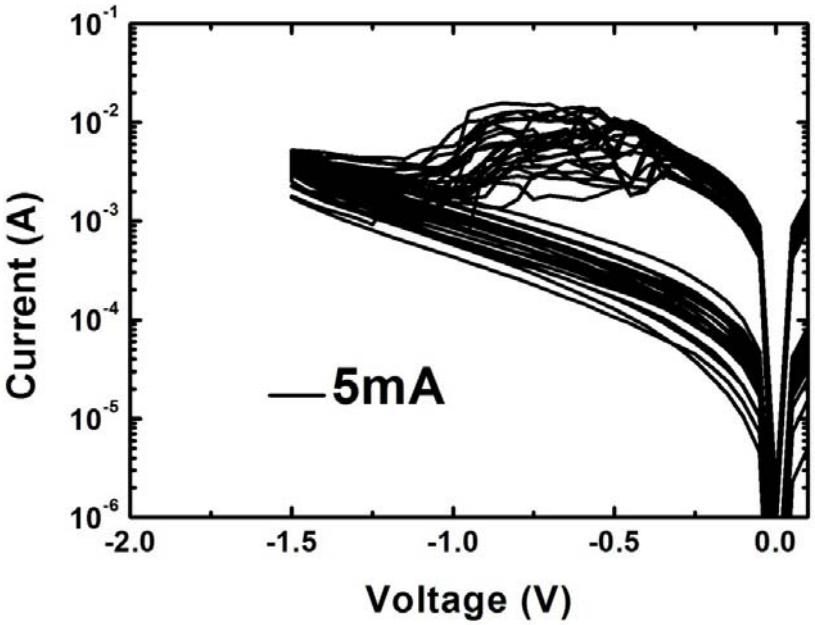


Figure 3.69. *I-V* curve in turn off process with current compliance 5mA.

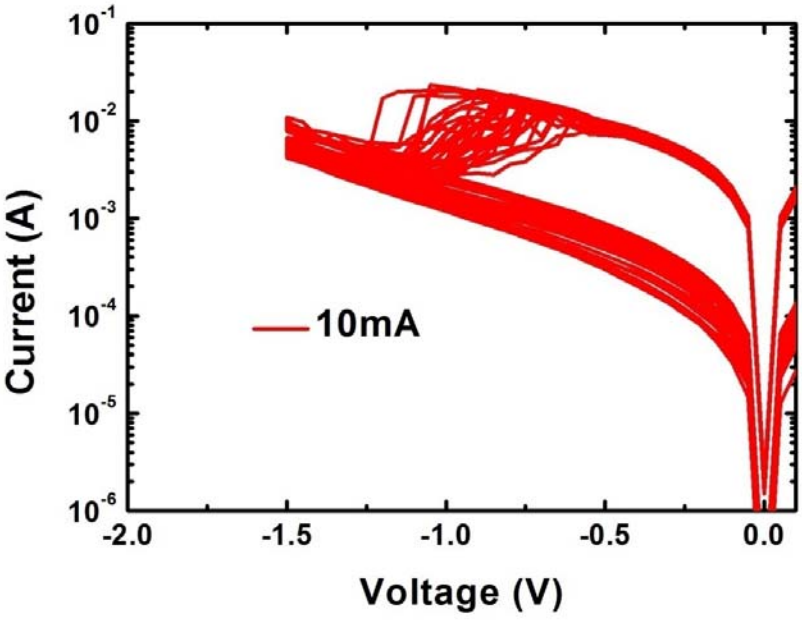


Figure 3.70. *I-V* curve in turn off process with current compliance 10mA.

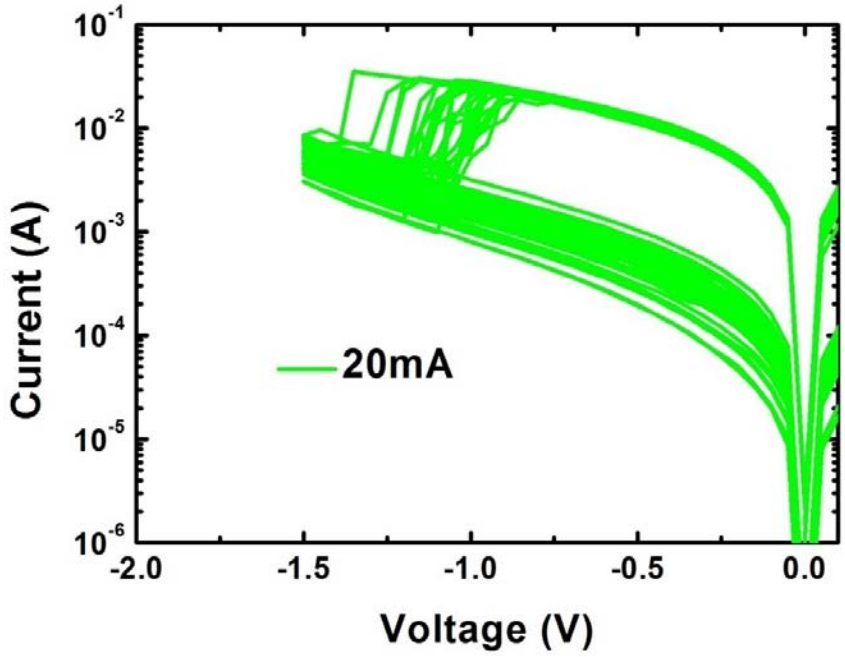


Figure 3.71. *I-V* curve in turn off process with current compliance 20mA.

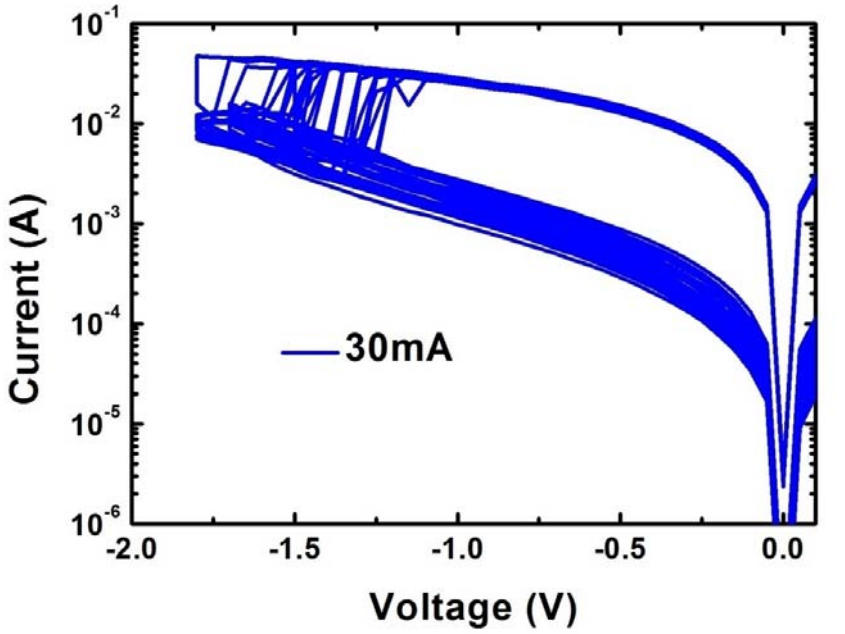


Figure 3.72. *I-V* curve in turn off process with current compliance 30mA.

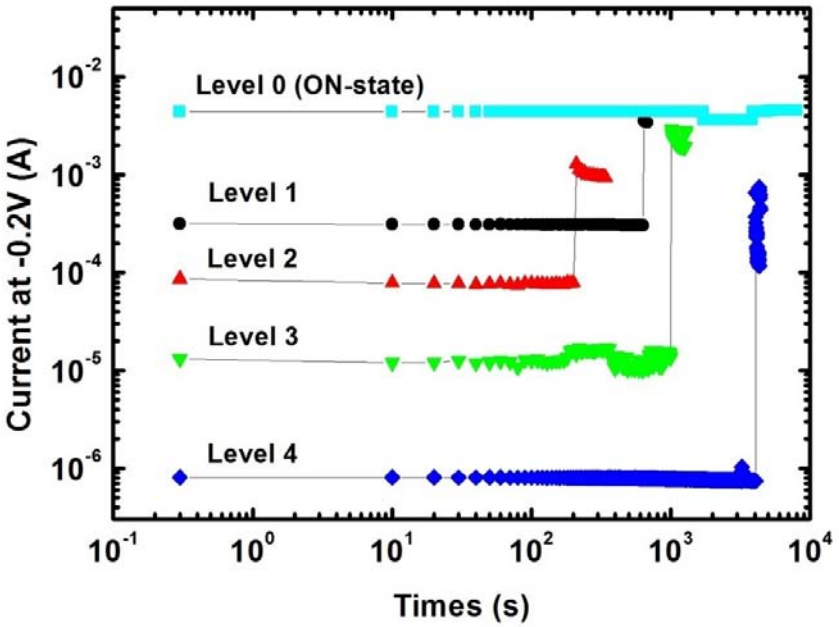


Figure 3.73. Stress characteristics of intermediate resistance state.

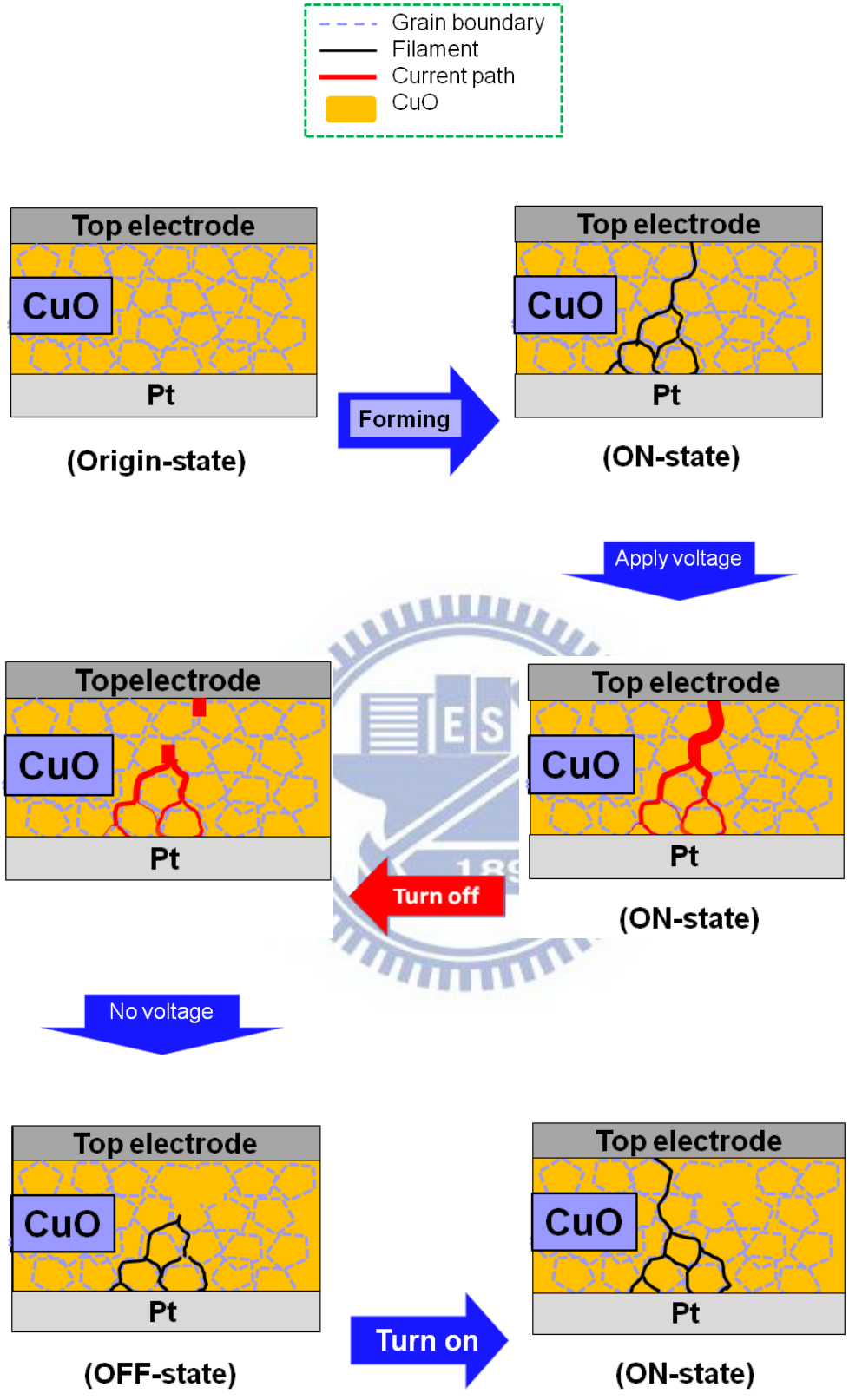


Figure 3.74. The detail resistive switching mode.

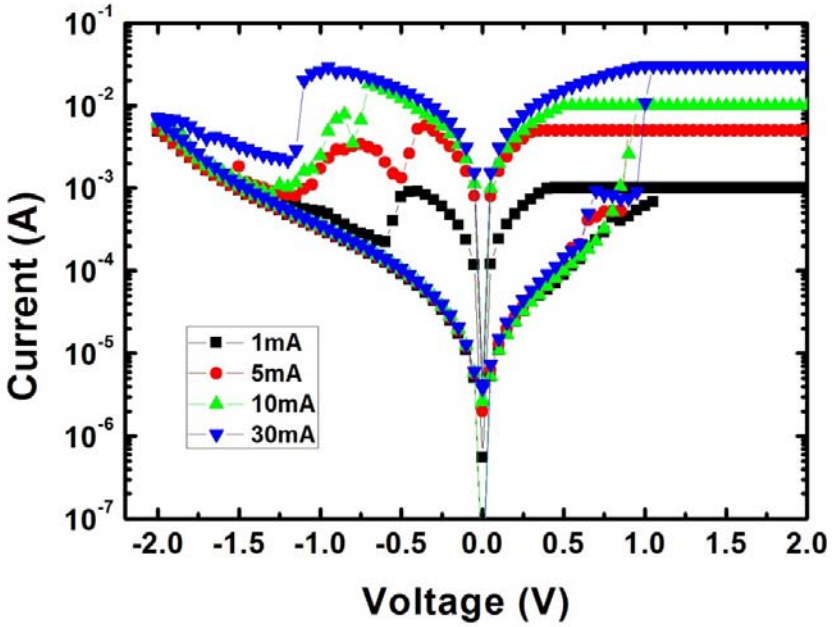


Figure 3.75. *I-V* curve of Ti/CuO/Pt device with different current compliance.

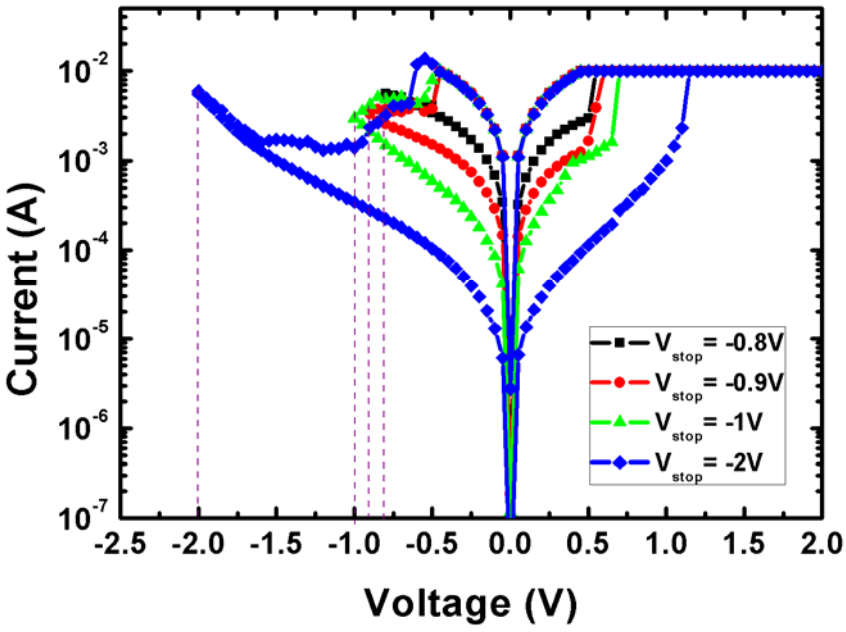


Figure 3.76. *I-V* curve of Ti/CuO/Pt device with different stop voltage.

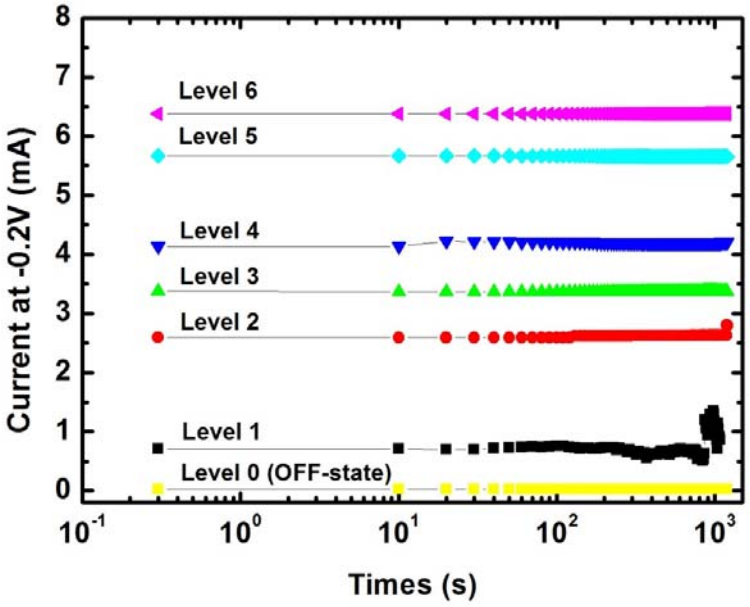


Figure 3.77. Stress characteristics of ON-state of multi-level with Ti/CuO/Pt structure.

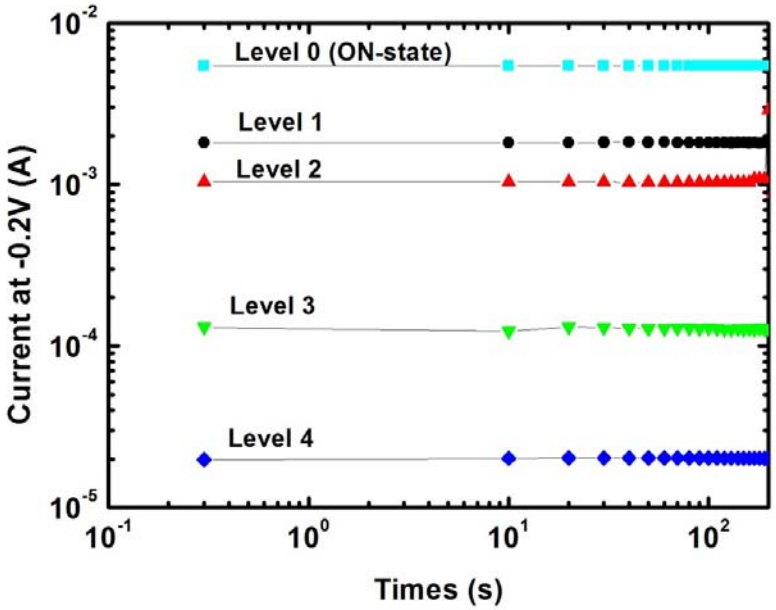


Figure 3.78. Stress characteristics of OFF-state of multi-level with Ti/CuO/Pt structure.

Chapter 4
Conclusion

4.1 Experiment conclusion

In this thesis, the oxidation condition of CuO thin film, 400 ^{o}C 60min, was investigated that provide higher yield and endurance.

The operation voltages, including V_{on} and V_{off}, are both less than 3V and suggest that the devices are appropriate for the low voltage applications, and the resistive switching occur in small region. The formation/rupture of conductive filament is preferred to explain this nonpolarity switching behavior by current fitting and size effect result.

The resistive switching of CuO thin film is nonpolar switching with Ti, Pt, W-probe top electrode, however, the bipolar switching enhance IRS switching by using Ti top electrode. We notice that this observation is very similar to the case of NiO thin films by using inert metal electrode. Nevertheless, we also notice that the metal/CuO interface effect enhance bipolar switching by using Ti electrode

The mechanism of turn-off process is Joule heating to rupture filament in nonpolar switching. However, for bipolar switching with Ti top electrode, the oxygen migration also influence turn-off process.

The Ti/CuO/Pt structure has a potential for nonvolatile multiple-valued memory device by controlling current compliance and stop voltage.

4.2 Future work

The bottom electrode and CuO thin film interface should insert a buffer layer to resist Cu atom to diffuse into bottom electrode and reduce thermal stress at high temperature. This buffer layer can choose Ta/TaN stack structure.

In oxidation CuO film, the RTA or plasma oxidation is more easy control oxidation rate. On the other hand, the oxidation atmosphere can be modulation to studying oxygen partial pressures effect resistive switching. The Cu deposition rate also controlled for origin defect concentration.

In interface engineering, there are some manners to change the property of Ti/CuO interface. One is various Ti thickness or plasma treatment before deposition Ti top electrode. On the other hand, the electrode can be using TiN.

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