國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

奈米級蕭特基金氧半場效電晶體之載子傳輸特性與通道背向散射研究

The Carrier Transport and Channel Backscattering Characteristics of Nanoscale Schottky-Barrier MOSFETs

研 究 生： 鄧安舜

指導教授： 莊紹勳 博士

中華民國 九十八 年 八 月

奈米級蕭特基金氧半場效電晶體之載子傳輸特性

與通道背向散射研究

The Carrier Transport and Channel Backscattering Characteristics of Nanoscale Schottky-Barrier MOSFETs

研　究　生：鄧安舜　　　　Student : An-Shun Teng

指導教授：莊紹勳 博士　　　　Advisor : Dr. Steve S. Chung

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master of Science

in Electronics Engineering

August 2009

Hsinchu, Taiwan, Republic of China.

中華民國 九十八 年 八 月

奈米級蕭特基金氧半場效電晶體之載子傳輸特性與通道背向散射研究

學生：鄧安舜　　　　　　　　　　指導教授：莊紹勳 博士

國立交通大學 電子工程學系 電子研究所碩士班

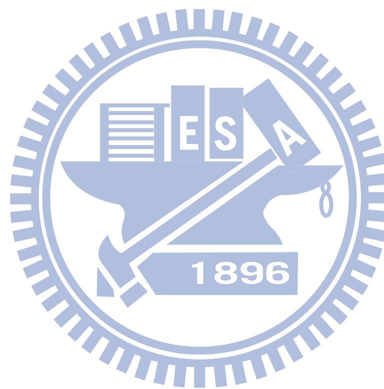
摘要

在前瞻超大型積體電路元件中，為了提升元件的效能，許多新穎的元件結構已被廣泛的提出，例如：高介電係數介電層、應變矽通道、金屬閘極與金屬源/汲極結構。當元件微縮至奈米級尺寸時，通道背向散射理論已經成功的運用在預測元件微縮極限上。而今，由於蕭特基金氧半場效電晶體製作的最佳化方法已趨可行，其在前瞻元件演進的地位已大幅的提升。因此，蕭特基金氧半場效電晶體的載子傳輸特性的研究成為主要課題。

本論文中，我們首先著眼於利用活化能(Activation Energy Method)方法求得等效的蕭特基位障勢。蕭特基場效電晶體之汲極電流傳導機制與閘極電壓的關係式可利用等效蕭特基位障勢表示。另外，我們同時發現蕭特基金氧半場效電晶體在打開狀態時，產生一個負等效蕭特基位障勢，使通道背向散射原理可運用於此。以往，溫度相依法(Temperature Dependent Method)常被用來探討通道背向散射係數。但是，在蕭特基金氧半場效電晶體中，載子主要是透過熱場發射機制由源極入射制通道內。所以對此元件來說，溫度相依法是不可行的。為了要求得載子彈道入射的機率，我們導入了等效彈道遷移率(Effective Ballistic Mobility)的觀念，此原理是建立在載子遷移率(Mobility)會隨著通道縮小而下降的因素上。因此，我們可以透過等效彈道遷移率的方法得到載子在元件線性區的彈道入射係數與載子熱入射(Thermal Injection Velocity)速度。然後，我們運用當電晶體在負等

效蕭特基位障勢發生時的載子平均傳輸速度(Carrier Average Velocity)與載子熱入射速度上，藉由這兩個速度的關係式，載子在打開狀態時的載子彈道入射機率即可求得。

由本文的研究，我們得到幾個結論：(1) 背向散射理論在蕭特基金氧半場效電機體中，因負等效位障勢的產生而再度的適用，(2) 載子由源極經通道到達汲極的背向散射機率因非局部的熱場穿遂機制而較傳統金氧半場效電晶體高，(3) 應變矽通道元件對背向散射係數影響較輕，但對載子熱入射速度影響較劇烈，(4) 遷移擴散(Drift-Diffusion)模型在quasi-ballistic區仍適用。因此，蕭特基金氧半場效電晶體加上高參雜隔離層(Dopant Segregation Implantation)與CESL(Contact-Etched Stoped Layer)技術，可達道元件高速操作的需求。



The Carrier Transport and Channel Backscattering Characteristics of Nanoscale Schottky-Barrier MOSFETs

Student：An-Shun Teng Advisor：Dr. Steve S. Chung

Department of Electrical Engineering & Institute of Electronics

National Chiao Tung University

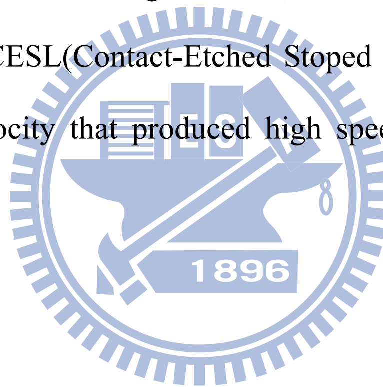
Abstract

In advanced VLSI devices, a lot of new structures have been brought up for enhancing drain current such as strained-Si channel, high-*κ* dielectric, metal gate and metal source/drain. In the nanoscale channel length, the channel backscattering theory has been applied to predict the scaling-limitations of these structures successfully. Nowadays, the Schottky-barrier MOSFETs have aroused much more attention because some optimized processes become feasible. Hence, the carrier transport mechanism of Schottky-barrier MOSFETs from source to drain becomes the most popular topic in researches.

In the thesis, first, we will focus on finding the effective Schottky-barrier height from the activation energy method. We can describe the effective Schottky-barrier height versus carrier transport mechanism relationship from this method. A negative effective Schottky-barrier height is found in the *ON-state* of the Schottky-barrier MOSFETs so that the channel backscattering theory can be used for extracting the carrier ballistic rate. In the past, the ballistic coefficient is extracted by temperature dependent method. However, the major carrier transport mechanism in the Schottky-barrier MOSFET is field emission, the temperature dependent method is failed. We practiced the effective ballistic mobility which is

from mobility degradation in short channel devices. We may directly obtain the ballistic coefficient and thermal injection velocity in the linear region. Then, we derive the carrier average velocity versus thermal injection velocity relations in *ON-state*. By the two velocity components, the ballistic probability of the Schottky-barrier MOSFET can be extracted easily.

Based on the results of this work, it was concluded that: (1) the backscattering theory is practicable from the negatively effective Schottky-barrier height, (2) the backscattering probability in the source side of Schottky-barrier is smaller than that in the conventional MOSFETs due to non-local tunneling, (3) the strained technology affects the backscattering coefficient lightly but it affects the thermal injection velocity drastically, (4) the drift-diffusion model is still workable in quasi-ballistic region. Thus, Schottky-barrier MOSFET with dopant segregation implantation and CESL(Contact-Etched Stoped Layer) can enhance the ballistic rate and thermal injection velocity that produced high speed operation in Schottky-barrier MOSFETs.



Acknowledgments

研究所生涯雖短，但經歷了這兩年的學習過程後，相信對於往後無論在生活、職場與待人處事上均有深遠的影響。首先，我把這份誠摯的感謝獻給陪伴著我兩年的研究生活，並一直是我的良師兼益友，且在國內外均享譽盛名的　莊紹勳教授，感謝您在這數百個研究日子裡，對我的諄諄教誨。

感謝博士班的易叡學長，教導我實驗室的各種規範，並給予我實驗上的實質幫助，預祝您往後的研究能突飛猛進。感謝已經畢業的學長們，家銘、小郭、有良跟文彥，除了在修課上的幫助外，感謝您們在實驗技巧與研究方向上的提點。感謝汪大暉教授門下的學長與同學們，小馬、達達、佑亮、阿標跟阿杜，對於實驗碰到的奇奇怪怪的問題，多虧有您們豐富的學識與經驗幫我一一克服。感謝一路陪伴我完成實驗的同學，振鵬，感謝您在實驗上的執著，讓我在實驗系統與實驗方法上，有更深入的了解與認識。感謝健宏，感謝您敏銳的心思，讓我在各項事務上均能盡善盡美。感謝米華，這位實驗室的精神領袖，使實驗室的氣氛活絡。感謝學弟們，士嵩、政穎、永涵跟元宏，感謝你們在我的研究與生活中的許多照應，並和我一起分擔辛勞。感謝同為前瞻元件與技術實驗室的各位，讓這個大家庭充滿歡笑與喜悅。另外還要感謝提供元件的聯華電子與在各期刊論文中給予我智慧的古聖先賢。

最後也是最值得感謝的就是我的家人們。感謝爺爺奶奶對我成長過程中無微不至的照顧，感謝爸爸媽媽對我在學生生涯中最完整的學習規劃，感謝姊姊一直擔任我學習的榜樣，讓我有今天的成就。

謹將這份榮耀獻給我的家人們。

Contents

Chinese Abstract iii
English Abstract v
Acknowledgements vii
Contents viii
Figure Captions x
Table Captions xiv

Chapter 1 Introduction 1
1.1 Motivation 1
1.2 Organization of Thesis 2

Chapter 2 Overview of Metal S/D Schottky-Barrier MOSFETs 4
2.1 Metal-Semiconductor Junctions 4
2.1.2 Energy Band Diagram 4
2.1.2 Effective of the Fermi Level Pinning 5
2.1.3 Image-Force Lowering 6
2.2 Current transport Mechanism in Metal-Semiconductor Diode 6
2.2.1 Thermoionic Emission Current 7
2.2.2 Field Emission Current 7
2.2.3 Measurement of the Schottky-Barrier Height 8
2.3 Introduction of the Schottky-Barrier MOSFET 9
2.4 The Operational Principle 10
2.5 The Challenges and New Technologies of SBMOS 11
2.5.1 Reduction of Schottky-Barrier Height 11
2.5.2 Modern Technologies for SB-CMOS 12

Chapter 3 Device Preparation and Basic Characteristics 24
3.1 Devices Preparation 24
3.2 Measuring Facility and Basic Experimental Setup 25
3.3 Basic Characteristics of the Schottky-Barrier MOSFETs 26
3.3.1 Band Diagram of DSI-SBMOS 26
3.3.2 Basic Characteristics of DSI-SBMOS 27
3.3.3 Current Flow Mechanism 27
3.3.4 Conductivity on DSI-SBMOS 29

3.5 Summary 30

Chapter 4 Carrier Ballistic Transport in Schottky-Barrier MOSFETs 48
4.1 Introduction of Ballistic Theory 48
4.1.1 To Derive the Backscattering Theory 49
4.1.2 Temperature Dependent Method to Extract Backscattering Coefficient 52
4.2 Characteristics of the Backscattering Theory 53
4.2.1 The Drain and Gate Voltage Dependences 54
4.2.2 The Mobility versus Drain Current Relationship 55
4.3 Backscattering Theory in Schottky-Barrier MOSFETs 56
4.3.1 Effective Ballistic Mobility 57
4.3.2 The Links Between Ballistic Theory, Effective Ballistic Mobility and Drift-Diffusion Model 58
4.4 The Experimental Results of Effective Ballistic Mobility 60
4.5 Summary 62

Chapter 5 Backscattering Coefficient in the Velocity Saturation Region 73
5.1 Thermal Injection Velocity 73
5.2 Carrier Average Velocity in the Saturation Region 75
5.3 The Experimental Results of the Velocity Components 77
5.4 Summary 79

Chapter 6 Conclusions 91

References 93

Figure Captions

Fig. 2.1 Energy band diagram of a Schottky contact (a) under non-equilibrium condition and (b) equilibrium condition.

Fig. 2.2 Energy band diagram of a Schottky contact (a) without and (b) with the effect of surface states. The Fermi level is pushed to ϕ_0.

Fig. 2.3 Image force induced Schottky-barrier lowering.

Fig. 2.4 Carrier transport mechanism of the Schottky contact in N-type semiconductor. (a) under forward bias (b) under reverse bias.

Fig. 2.5 Band diagram to deduce the probability of field emission (a) light doped condition (b) heavy doped (degenerate) condition (c) under reverse bias condition of a junction between n-type semiconductor and metal.

Fig. 2.6 Extracting the Schottky-barrier height by activation-energy method.

Fig. 2.7 The device structures (a) conventional MOSFET (b) Schottky- barrier MOSFET.

Fig. 2.8 Different band diagram of n-SBMOSFET (SB-NMOS). (a) *OFF-state*, $V_g<V_{fb}$ (b) *OFF-state*, $V_g=V_{fb}$ (c) $V_g>V_{fb}$.

Fig. 2.9 Current components in the source to channel interface of Schottky-barrier nMOSFETs.

Fig. 2.10 Schottky barrier height reduction technology (a) with insulator layer (b) with dopant segregation implantation.

Fig. 2.11 Drivability of Schottky barrier MOSFET as a function of Schottky barrier height for (a) N-type and (b) P-type devices.

Fig. 3.1 Process flow of Schottky-barrier MOSFETs with DSI NiPt silicide.

Fig. 3.2 (a) Device split of Schottky-barrier MOSFETs with DSI NiPt silicide and conventional MSOFET and (b) its cross-section TEM picture with the shortest length 35nm.

Fig. 3.3 (a) The I_{on}-I_{off} characteristics of Sample A, B and C. Sample B has the optimized characteristic. (b) All of them show the reduced S/D sheet resistance.

Fig. 3.4 The experimental system of current-voltage (*I-V*) for both N or PMOSFETs.

Fig. 3.5 Conduction band diagram of the (a) conventional SBMOS (b) SBMOS with dopant segregation implantation (DSI-SBMOS) when V_D is small bias.

Fig. 3.6 Short channel effect of the DSI-SBMOS.

Fig. 3.7 Some characteristics of the DSI-SBMOS (a) I_D-V_G curve (b) I_D-V_D curve.

Fig. 3.8 Drain current versus gate voltage curve (I_D-V_G) with different DSI energy when $|V_D|=0.1V$. (a) SB-PMOS (b) SB-NMOS.

Fig. 3.9 The effective Schottky-barrier height of different DSI energy in SB-PMOS.

Fig. 3.10 The conduction band edge of SBMOS with different bias condition. The dashed line is *OFF-state* and solid line is *ON-state*.

Fig. 3.11 The effective Schottky-barrier height of SB-PMOS with different bulk bias (V_B).

Fig. 3.12 The band diagram for different substrate bias of (a) $V_B=0$ (b) $V_B<0$ for Schottky-barrier pMOSFETs.

Fig. 3.13 The effective Schottky-barrier height of both N and PMOS with different channel length.

Fig. 3.14 The conduction band edge with different devices (a) Conventional SBMOS (b) DSI-SBMOS (c) Conventional MOSFET. The solid line is short channel and dash line is long channel devices.

Fig. 3.15 The band diagram of the DSI-SBMOS with different DSI energy in (a) *ON-state* (b) *OFF-state*. The DSI energy of the blue line is lower than red line. The dash line is the conventional SBMOS band diagram.

Fig. 4.1 (a) Band diagram of the conventional NMOS with the scattering matrix method for extracting the ballistic theory. (b) The simplified transmission and reflection current flow.

Fig. 4.2 The conduction band edge versus position with several bias condition (a) $V_D=50mV$, $V_G=0\sim0.6V$ (b) $V_D=0.6V$, $V_G=0\sim0.6V$ (c) $V_G=50mV$, $V_D=0\sim0.6V$ (d) $V_G=0.6V$, $V_D=0\sim0.6V$.

Fig. 4.3 The reflection coefficient versus gate voltage plot with different drain voltage. Circle is at $V_D=0.1V$, square is at $V_D=0.5V$ and triangle is at $V_D=1V$.

Fig. 4.4 The band diagram for (a) DSI-SBMOS (b) concentional MOSFETs with the same channel length and potential. υ_{inj} means the injection velocity.

Fig. 4.5 (a) The scattering components in the channel. (b) Drift velocity versus electric field plot. Solid line is experiment curve, dash line is theoretical curve. υ_s is saturation velocity, and ε_c is critical field.

Fig. 4.6 The low field mobility versus channel length plot (a) for DSI SB-PMOS with CESL (b) Conventional pMOSFET.

Fig. 4.7 The low field mobility versus channel length plot (a) for DSI SB-NMOS with CESL (b) Conventional nMOSFET.

Fig. 4.8 The linear ballistic coefficient (B_{lin}) versus channel length curve (a) for DSI SB-PMOS with CESL (b) DSI SB-NMOS with CESL compared with conventional MOSFETs.

Fig. 4.9 The thermal injection velocity in linear region of (a) SB-PMOS versus PMOS (b) SB-NMOS versus NMMOS.

Fig. 5.1 (a) Equilibrium thermal injection velocity versus inversion layer density n_s and also shown the Fermi velocity [33]. (b) Electron charge $Q_i(0)$ at the top of the barrier versus V_{DS}.

Fig. 5.2 The potential profiles from source toward drain (a) Conventional MOSFETs with doped S/D (b) Schottky-barrier MOSFETs.

Fig. 5.3 The carrier average velocity (effective velocity) of (a) Schottky-barrier pMOSFETs. (b) Conventional pMOSFETs with doped S/D.

Fig. 5.4 The carrier average velocity (effective velocity) of (a) Schottky-barrier nMOSFETs. (b) Conventional nMOSFETs with doped S/D.

Fig. 5.5 Comparison of the carrier average velocity (effective velocity) between (a) PMOS and SB-PMOS (b) NMOS and SB-NMOS.

Fig. 5.6 Comparison of the effective saturation velocity between (a) PMOS and SB-PMOS (b) NMOS and SB-NMOS.

Fig. 5.7 Comparison of the carrier average velocity (effective velocity) with different

temperature between (a) PMOS and SB-PMOS (b) NMOS and SB-NMOS.

Fig. 5.8 The inversion charge density of the Schottky-barrier MOSFET with DSI.

Fig. 5.9 The electric field of the channel potential (a) DSI SB-PMOS and conventional PMOS (b) DSI SB-NMOS and conventional NMOS.

Fig. 5.10 The saturation ballistic coefficient (B_{sat}) of (a) DSI SB-PMOS and conventional PMOS (b) DSI SB-NMOS and conventional NMOS.

Fig. 5.11 The current enhancement rate of uniaxial tensile-cap compared to conventional structure.

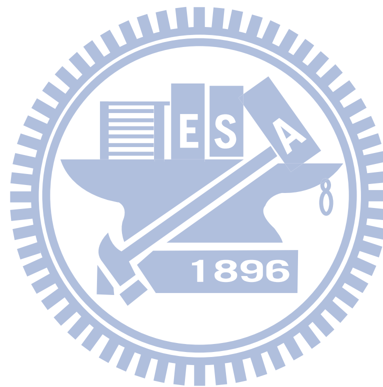
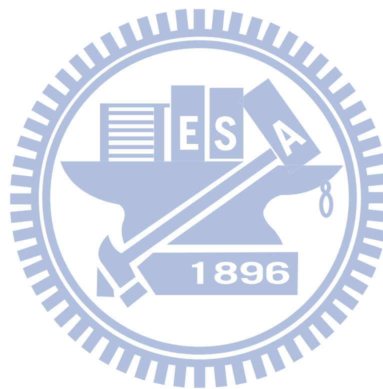


Table Captions

Tab. 3.1 Splits of SBMOS with different DSI energies. The DSI energy relation is $DSI_1 < DSI_2 < DSI_3$, and marked as samples A, B and C.



Chapter 1
Introduction

1.1 Motivation

Modern VLSI devices have entered nanoscale era for several years and continue to be scaled rapidly. By ITRS predictions, semiconductor industry will meet the scaling-limit in ten or less years. In order to understand the limitations of down-scaling, some researchers have investigated these device bahariors by the *ballistic transport theory,* such as M. Lundstrom [1-6] and M. J. Chen [7-8].

When the channel length is just a few nanometers, some transport carriers can easily emit through the channel without any collisions. As the length scales down, more carriers are easier to tunneling through the channel barrier. Hence, the drift-diffusion theory has less significant for increasing tunneling rate. Before the channel is short enough for all transport carriers to tunnel through, we call it "quasi-ballistic" region. In this region, we have two important parameters which includes backscattering coefficient (r_c) and thermal injection velocity ($\tilde{\upsilon}_T$). The former presents the carrier transmission rate in the channel barrier and the other means the limitation of carrier transport velocity. By the two parameters, we can describe how close to the limit of the devices.

In recent years, ballistic transport has investigated in various devices such as process strained-Si (PSS) devices [9-10], double-gate MOSFETs [5], Silicon nanowire transistor (SNWT) [11] etc. Besides, the significance of Schottky-barrier MOSFETs (SB-MOSFET) has risen up in recent years. In conventional Schottky-barrier MOSFETs, they performed poor performance due to the intrinsic Schottky barrier which blocks most of the transport carriers. Thus, many researchers make efforts in enhancing the performance of SBMOS. In recent years, the solutions have brought up by B. Y. Tsui, in which dopant segregation implantation

(DSI) technology [12] has been developed. The optimization methods lead to high performance which is better than conventional devices. In contrast to the conventional MOSFETs, Schottky-barrier MOSFETs have more advantages such as junction abruptness, low series resistance and low thermal budget of the process. So, the ballistic limit of SBMOS is one of the important characteristics we are interested.

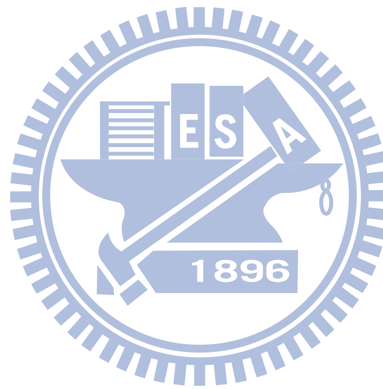
Nowadays, the temperature-dependent method is the major method to extract the ballistic transport coefficient in MOSFET devices, which is developed by M. J. Chen [7]. But in SBMOS, the carriers are transmitted by two mainly mechanisms contained field emission (tunneling) and thermal emission (thermionic emission). The major current component due to tunneling mechanism is independent of the temperature that makes the temperature-dependent method unworkable. For this reason, we investigate in some different views to understand the ballistic efficiency, which includes the effective ballistic mobility and effective saturation velocity. In this thesis, we try to explore the new observations of ballistic transport in SBMOS.

The ballistic transport theory is the simplest one to determine the limitations of the devices. Based on this theory, we can understand the correlations between carrier transport and Schottky barrier structure. We also expect to know the best method to enhance the performance of the advanced devices in the future.

1.2 Organization of Thesis

In this thesis, first, we will discuss the Schottky-barrier MOSFET technology issues and the related physical operational principle in *chapter 2*. In *chapter 3*, we will introduce our experimental setup and the basic experimental characteristics of Schottky-barrier MOSFETs. In *chapter 4*, the backscattering theory is derived in detail. Then, the effective ballistic mobility is applied for extracting the linear ballistic coefficient. The correlations between ballistic theory and effective ballistic mobility will be derived in detail. In *chapter 5*, the

effective velocity has been used for extracting the ballistic coefficient in saturation region. The thermal injection velocity presents the limit of the carrier transport velocity and the saturation ballistic coefficient can evaluate how the devices close to the transport limitation. Finally, the conclusions will be given in *chapter 6*.



Chapter 2
Overview of Metal S/D Schottky-Barrier MOSFETs

Before our experiment, it is necessary for us to understand the history and the fundamental physics of the Schottky barrier MOSFETs. In this chapter, first, we introduce the physics of metal-semiconductor junctions which is the key components of Schottky barrier MOSFETs. Then, we have an overview of the SBMOS issues such as developing history, operational principle and the process technologies.

2.1 Metal-Semiconductor Junctions

2.1.1 Energy Band Diagram

The metal-semiconductor junction was first reported by W. Schottky [13]. He reported that the metal-semiconductor junction can work as a rectifier by its statistic space charge induced potential barrier. The barrier is called Schottky Barrier. Fig. 2.1(a) is the band diagram of a Schottky junction in a non-equilibrium situation. Here, $q\phi_m$ is metal work function, $q\phi_s$ is semiconductor work function, $q\chi$ is electric affinity of semiconductor which is an intrinsic property of the crystal lattice, E_0 is vacuum free-electron energy, E_f is the Fermi level which depends on doping concentration, and E_c and E_v are conduction and valance band edge of semiconductor. Besides, the most important parameter in metal-semiconductor junction is $q\phi_B$ which indicates the difference between metal and semiconductor work function.

When the two materials are in touch with each other, a net flow of electrons or holes is induced through the junction in order to equalize the Fermi level. In non-equilibrium condition, elections in semiconductor have higher energy and attract by the metal, creating a depletion regime in the semiconductor, see Fig. 2.1(b). Under equilibrium condition, the magnitude of the energy step for *N-type* semiconductor which is called Schottky-barrier height is given by eq. (2.1), and for P-type is given by eq. (2.2).

$$q\phi_{B,n} = q\left(\phi_m - \chi\right) \tag{2.1}$$

$$q\phi_{B,p} = E_g - q\left(\phi_m - \chi\right) \tag{2.2}$$

Here, E_g is the energy gap of the semiconductor. The sum of the two barrier-heights is shown in eq. (2.3), which equals to energy gap, i.e.,

$$q\left(\phi_{B,p} + \phi_{B,n}\right) = E_g . \tag{2.3}$$

When the electrons are going from semiconductor to metal, they will see a barrier which is called build-in potential V_{bi}. Here V_n is the energy difference between conduction band edge and Fermi level.

$$V_{bi} = q\left(\phi_m - \phi_s\right) = \phi_{B,n} - V_n . \tag{2.4}$$

2.1.2 Effective of the Fermi Level Pinning

Because the lattice constant of the metal and semiconductor are different, at their junction surface, there are several surface states in the forbidden energy gap due to the presence of dangling bonds. The unpaired atom can be acceptor or donor type, which is determined by the charge neutrality condition. The neutral level ϕ_0 is usually defined as the position of the Fermi level corresponding to electrical neutrality at the surface, see Fig. 2.2. Bardeen claimed that the surface state at the metal-semiconductor junction reduce the dependency of the Schottky-barrier height and the metal work function [14]. In Fig. 2.2(a), assuming no surface state existed; the Fermi level is located below the neutral level of the surface. A positive charge is stored in the surface state and the charge in the depletion region will be reduced accordingly to the neutrality condition. The reduction of the charge in the depletion region pushes the Fermi level toward ϕ_0 and the barrier is lowered, see Fig. 2.2(b). Similarly, if the Fermi level is located above the neutral level, a negative charge is stored and increase of the positive charge in the depletion region pushes the Fermi level to ϕ_0. These phenomena are call *Fermi level pinning* and the Schottky barrier height is pinned in E_g- ϕ_0.

$$\phi_B \approx E_g - \phi_0 \tag{2.5}$$

In recent years, the Fermi level pining is also found in the high-κ metal-gate structure. The

new observations of Fermi level pining are explained by dipole effect. The details of dipole effect are complex that we do not emphasize it in this thesis.

2.1.3 Image-Force Lowering

Another phenomenon induces the Schottky-barrier lowering, which is the nature magnetic phenomenon, is the image-force lowering. This effect is the interaction between the electron and the positive image charge located in the metal. It modifies the band diagram and is according to Fig. 2.3. The magnitude of the barrier lowering is as follows:

$$\Delta\phi = \left[\frac{q^3 N|\psi_s|}{8\pi^2\varepsilon_s^3}\right]^{1/4} \tag{2.6}$$

where ψ_s is the surface potential, N is doping concentration, ε_s is the dielectric constant of semiconductor [15].

2.2 Current Transport Mechanism in Metal-Semiconductor Diode

There are several transport mechanisms in metal-semiconductor junction [16]:

1. The thermionic emission over the barrier.
2. The field emission (*tunneling*) through the barier.
3. Recombination in the depletion region.
4. Recombination in the neutral region (*hole injection*).

The first two mechanisms are the mainly mechanisms. When the metal-semiconductor junction under forward bias, as see in Fig. 2.4(a), the carriers are tunneling through the Schottky barrier or thermally emitting above the barrier. And the mechanisms are similar when in reverse bias is; see Fig. 2.4(b). Actually, most of the transport carriers have thermionic and field emission in the same time. Hence, the transport carriers have higher average energy in metal-semiconductor junction than in p-n junction.

2.2.1 Thermionic Emission Current

The thermionic emission model is first proposed by Bethe in 1942 [17]. He reported that the rate of emitted electrons from the semiconductor to the metal and from the metal to the semiconductor is proportional to the density of the state at the interface between the two materials. When the forward bias is applied, the thermionic emission current is present as:

$$I_{thermionic} = AA^{**}T^2\left(\frac{-q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right)-1\right] \tag{2.7}$$

where A is the cross section of the junction, A^{**} is the Richardson constant (for Si, $A^{**} \approx 120$ for electrons and 30 for holes), n is ideality factor (about 1~1.2), k is the Boltzmann's constant, T is the temperature by Kelvin coordinate, q is the basic charge of the electron, and ϕ_B is the effective Schottky-barrier height (contained the effect of image-force lowering).

2.2.2 Field Emission Current

In Schottky contacts, the energy of carrier is lower than the Schottky barrier. If the carrier tunnel through the barrier from metal to semiconductor or the other, we called it field emission current. It may be possible under some circumstances, degenerate semiconductor under forward bias or for relative low doped substrate under negative bias [6]. The band bending next to the interface plays a crucial role since it determines the tunneling distance that is the region where the carrier is located within the energy gap with its wave function exponential decaying, see Fig. 2.5. The WKB approximation is following. Assuming a triangular barrier shape is used. The tunneling probability for an electron at energy ΔE from the barrier top is

$$P = \exp\left[-\frac{2(\Delta E)^{1.5}}{3E_{00}V_D^{0.5}}\right] \tag{2.8a}$$

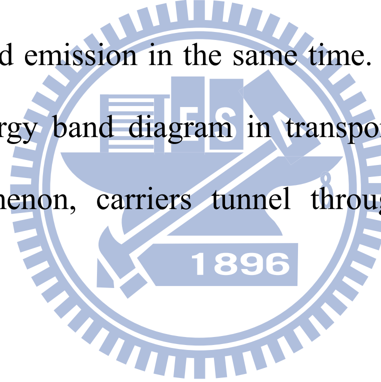
where V_D is the energy drop across the space charge region and E_{00} is

$$E_{00} = \frac{\hbar}{2}\sqrt{\frac{N_d}{m^*\varepsilon_s}}\,. \tag{2.8b}$$

We may know that the higher is E_{00}; the large is ΔE which has a non negligible tunneling probability. In lightly doped semiconductors, the depletion region width is large and the band bending is not strong enough to enable field emission, see Fig. 2.5(a). E_{00} is small and close to the conduction band edge can tunnel through the barrier. And in heavy doped semiconductor, see Fig. 2.5(b), the narrow depletion region leads to large tunneling probability, which is consistent with large E_{00}. When under reverse bias, the depletion region is narrower. It is known that tunneling probability is larger, see Fig. 2.5(c). The tunneling current through the Schottky-barrier is give by eq. (2.9) [18].

$$I_{tunneling} = A\frac{e^2\xi^2}{8\pi h\phi_B}\exp\left[-\frac{8\pi}{3he\xi}\sqrt{2m^*\left(e\phi_B\right)^3}\right] \tag{2.9}$$

where h is Plank's constant, A is the junction area, m^* is the effective mass, and ξ is the electric field of the Schottky barrier. In real Schottky diode, most carriers transport through the junction by thermionic and field emission in the same time. This means that the carrier is on the higher position of the energy band diagram in transporting than in thermal equivalent condition. Based this phenomenon, carriers tunnel through the barrier which is called *non-local tunneling*.



2.2.3 Measurement of The Schottky-Barrier Height

The simple and accurate Schottky-barrier height extraction method has been reported for a long time [15]. They are summarized as the following:

1. Current-Voltage (*I-V*) method
2. Current-Temperature (*Activation-Energy*) method
3. Capacitance-Voltage (*C-V*) method
4. Photoelectric measurement

The most appropriate method for our experiment is the activation-energy method due to the uncertain junction area of Schottky-barrier MOSFET. The method is derived from the thermionic emission current, eq. (2.7). We divided the equation by square of temperature and

applied the nature logarithm on it. Assuming the device is *N-type* and the ideality factor is one, then we have

$$\ln\left(\frac{I_F}{T^2}\right)=\ln\left(AA^{**}\right)-\frac{q\left(\phi_B-V_F\right)}{kT} \tag{2.10}$$

where the I_F is the forward bias Schottky diode current, V_F is the forward bias voltage. And $q(\phi_B - V_F)$ is considered the *activation energy*. Then, we draw the $ln(I_F/T^2)$ versus $1/T$ plot, see Fig. 2.6. The ϕ_B is calculated by eq. (2.11), and m is the slope of curve.

$$\phi_B=\frac{V_F}{n}-\frac{k}{q}\times m. \tag{2.11}$$

2.3 Introduction of the Schottky-Barrier MOSFET

In 1966, Nishi, first proposed a Japanese patent of Schottky-barrier MOSFET (SBMOS). But the first paper for SBMOS is published by Lepselter and Sze [19], who are the most important scholar in semiconductor technology. This is the first record for PtSi silicide PMOSFET. At that time, SBMOS performed poor performance so that it is concerned by nobody. Later in 1984, T. Mochizuki and K. Wise reported a n-channel MOSFET with Schottky source and drain [20]. After that the SB-CMOS have raised up their significance in the semiconductor devices., several advantages of the SBMOS had been reported gradually in the later years such as:

1. Better for devices scaling down.
2. Low parasitic source/drain resistance.
3. Low temperature processing for S/D formation.
4. Better control of short channel effect.
5. Reduced the floating body effect on SOI devices.
6. Reduced the latch-up susceptibility.

As shown in Fig. 2.7, when the conventional MOSFET is scaling down to a few nanometers, the doped S/D junctions are not abruptness so that the channel is easy to punch through. The SBMOS does not have this kind of consideration. The junction is sharp and easy to control the

MOS capacitance. Hence, Schottky-barrier MOSFET is easier to scale down than conventional MOSFET. Besides, the series resistance is becoming as large as possible due to the scaling down of the junction area. When S/D changes from silicon to metal silicide, the series resistance becomes small. For example, a 60 nm thick PtSi sheet resistance is about $6\Omega/\square$.

2.4 The Operational Principle

The typical SBMOS band diagram is shown in Fig. 2.8. In general, the carrier transport in SBMOS is so called "ambipolar". When n-SBMOS or SB-NMOS is at *OFF-state*, the electrons in the source side see a thick and high barrier so that they can only thermionic emit over the barrier instead of tunneling. Under this situation, the thermionic current by electrons is quite small that reduced the *OFF-state* drain current. But actually, the *OFF-state* drain current is quite large due to holes injection in the drain end. In the drain side, holes see a thin Schottky barrier and are easy to tunnel through the barrier. That produced a large drain leakage current, see Fig. 2.8(a). While in the *ON-state*, the electrons see a thin Schottky barrier that contributed *ON-state* drain current, see Fig. 2.8(c). Because of the two carriers transport characteristic just like bipolar junction transistor, we call it "ambipolar transport". Besides, in Fig. 2.8, the flatband voltage (V_{fb}) presents the gate voltage which makes the lateral potential from channel to source become flat. We combined the band diagram with the gate voltage and divided the operational condition in three parts. When $V_g<V_{fb}$, SB-NMOS is at OFF-state, as Fig. 2.8(a). Electrons see a thick barrier in the source side and holes see a thin barrier in the drain side that produced a large off leakage. When $V_g=V_{fb}$, both in source and drain barrier are thick, carriers can only thermionic emit over the barrier. In this state, the drain current is very small, see Fig. 2.8(b). When $V_g>V_{fb}$, SB-NMOS is at *ON-state*, as Fig. 2.8 (c). Most of electrons in the source side are easy to tunnel through the thin barrier, which produced a large on current. These transport mechanism is different from the conventional MOSFET. We note that the on current is determined by the source side barrier height. If the

barrier is short or thin, the electrons are easy to thermionic emit above the barrier or tunnel through the barrier that produces large drive current. Besides, the off current is dominated by the drain side barrier height. It is important to increase the drain side barrier height so that the *OFF-state* leakage current will be decreased.

In real Schottky-barrier MOSFETs, the *ON-state* current is contributed by both thermionic emission and field emission components. We describe the total current as eq (2.12). Some of the carriers get enough energy so that they can thermal emit over the Schottky barrier.

$$I_{channel} = I_{thermionic} + I_{tnnneling}. \tag{2.12}$$

The carrier transmission model is illustrated in Fig. 2.9. Most of carriers tunneled through the barrier. Thus, the tunneling current is larger than thermionic current, which is the major carrier transport mechanism in the Schottky-barrier MOSFET.

2.5 The Challenges and New Technologies of SBMOS

2.5.1 Reduction of Schottky-Barrier Height

In section 2.1.2, we have reported the Fermi level pining effect. This effect induces the Schottky-barrier height pinned in the same value. No mater how we change the metal, the Schottky-barrier height is unchanged. In order to reduce the barrier height, some methods have been reported [21], see Fig. 2.10. For examples, W. Saitoh reported the results of barrier height reduction. When the channel length is short and the Schottky-barrier height is as low as *0.1eV* for *N-type* and *0.2eV* for *P-type*, the performance of SBMOS is better than conventional MOSFET [18], see Fig. 2.11. Because of the Fermi level pinning, if we would to achieve an absolutely low Schottky-barrier height, we need a perfect junction interface and small work function difference between metal and semiconductor. This is nearly impossible. However, some researchers brought up some methods that we can get a low Schottky-barrier height equally. One of the methods is depositing an insulator layer between the silicon and the metal silicide [22]. The thin insulator layer becomes a tunneling barrier of the source-to- channel

junction, see Fig. 2.10 (a). The dangling bond on the silicon substrate will skip by this layer and the original Schottky barrier is lowering.

The other method is dopant segregation implantation method; see Fig. 2.10 (b) [23]. Before silicidation, a high dose of low energy dopant is implanted in the S/D region to the silicon interface. This high dose layer induces a high electric field so that the barrier will become thinner. This layer is a thin tunneling barrier which works like an insulator layer. Thus, the carriers are easy to tunnel through the barrier toward the channel. The As or S implantation has been reported to reach a very low effective barrier of $0.1eV$ [24]. Nowadays, the dopant segregation implantation technology is used widely in novel semiconductor industry.

2.5.2 Modern Technologies for SB-CMOS

In recent year, some different materials and architectures have been used for improving the performance of the integrated circuit, such as rare element silicide in S/D region, silicon on insulator and high-κ dielectric in gate stack. A lot of new materials have been published for the S/D silicide. For SB-NMOS, nickel (Ni) and platinum (Pt) is used. For SB-PMOS, erbium (Er) and ytterbium (Yb) is used. The Schottky-barrier height for SB-NMOS is about $0.15\sim0.3eV$, and $0.27\sim0.4eV$ for SB-PMOS. Because of the spike barrier blocks most of the carriers, the drain current of SBMOS is smaller than conventional MOSFET. Besides barrier reduction, someone applied the process strained silicon (PSS) technology on SBMOS. In typically, contact etch stop layers (CESL) technology is adopt by some companies [25-26].

In order to conflict the short channel effect, some structures are brought up for SBMOS, just like dual-gate structure, FinFET [27] and Vertical MOSFET. Besides, someone has reported the hot-electron generation rate in SBMOS [28]. It was concluded that the generation rate in SBMOS is better than conventional MOSFET. For this reason, we can apply metal S/D in the flash memory which will cause large hot electron injection rate.

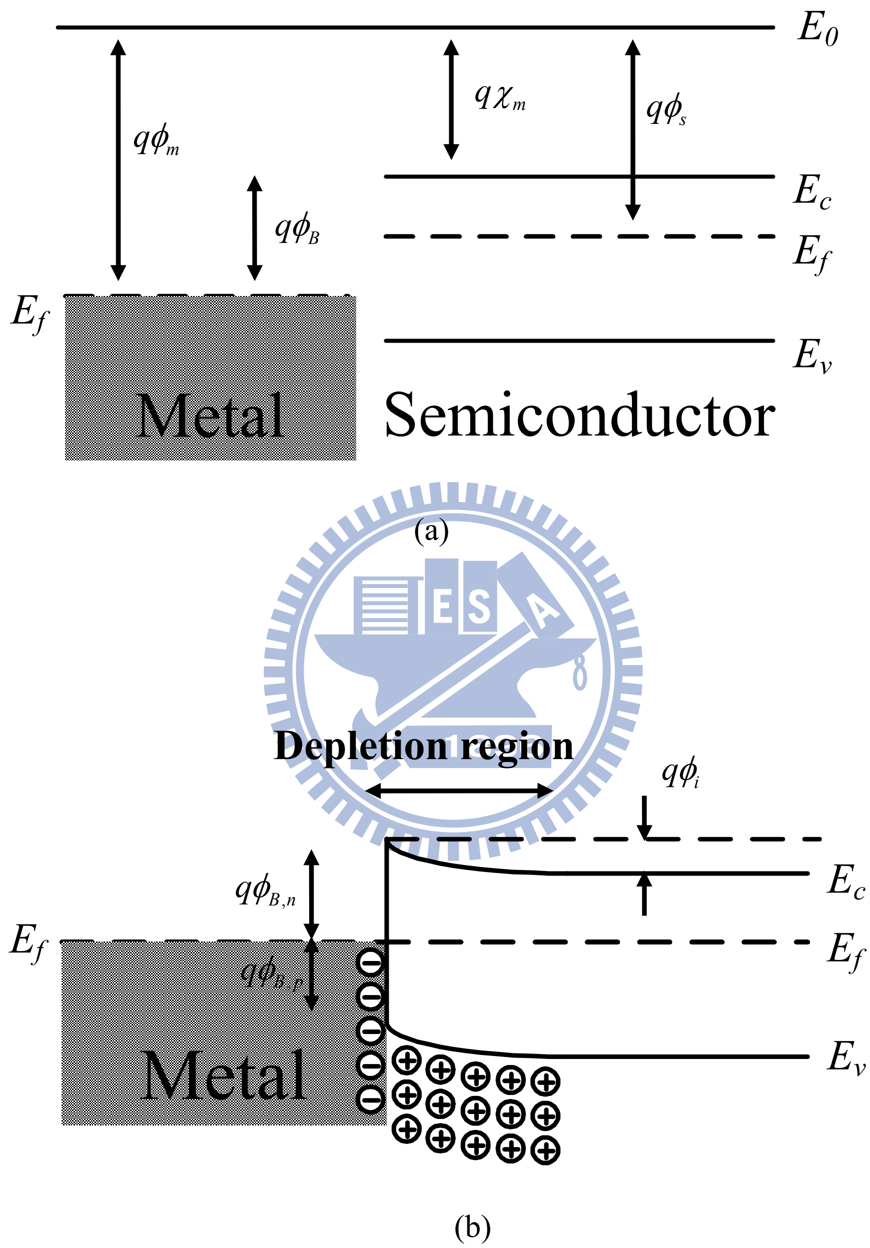
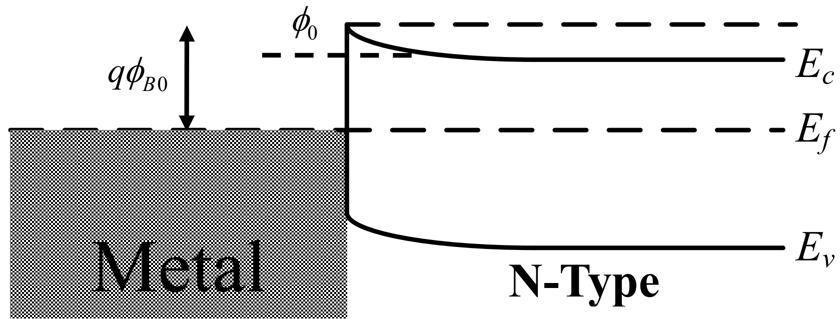
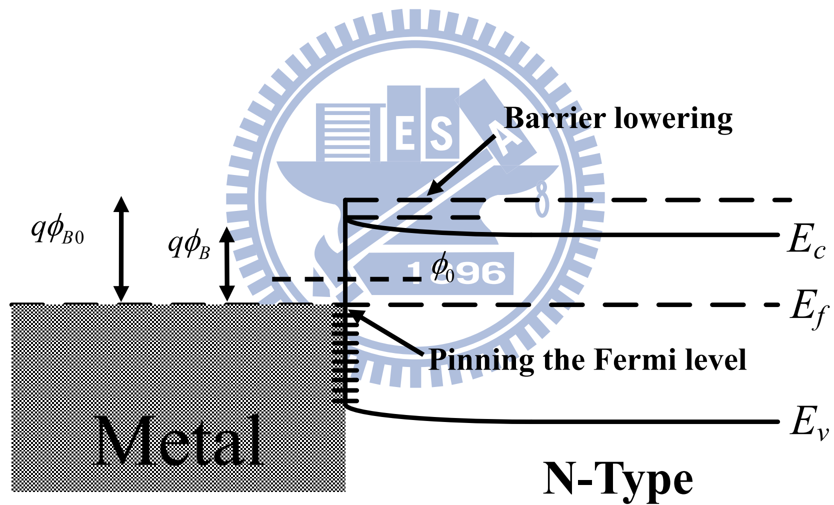


Fig. 2.1 Energy band diagram of a Schottky contact (a) under non-equilibrium condition (b) equilibrium condition.



(a)



(b)

Fig. 2.2 Energy band diagram of a Schottky contact (a) without and (b) with the effect of surface states. The Fermi level is pushed to ϕ_0.

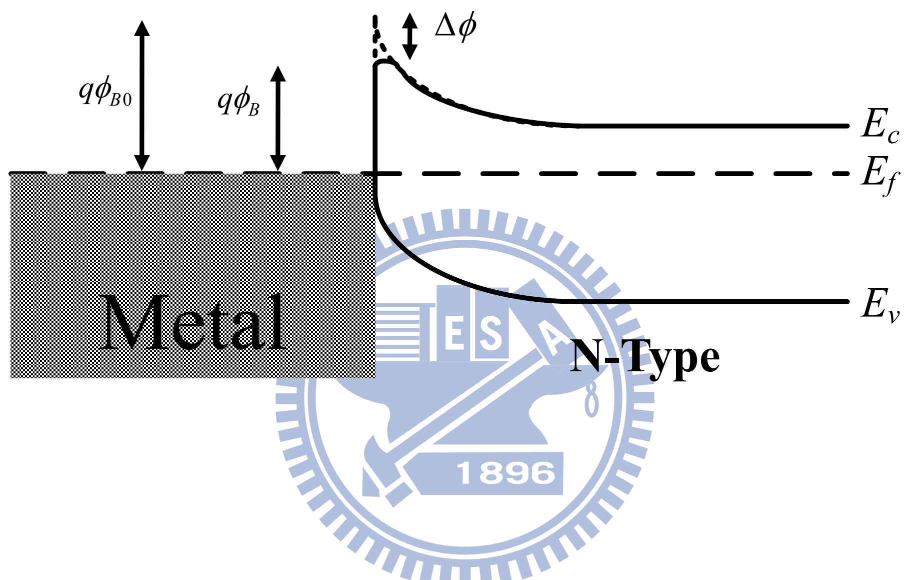


Fig. 2.3 Image force induced Schottky-barrier lowering.

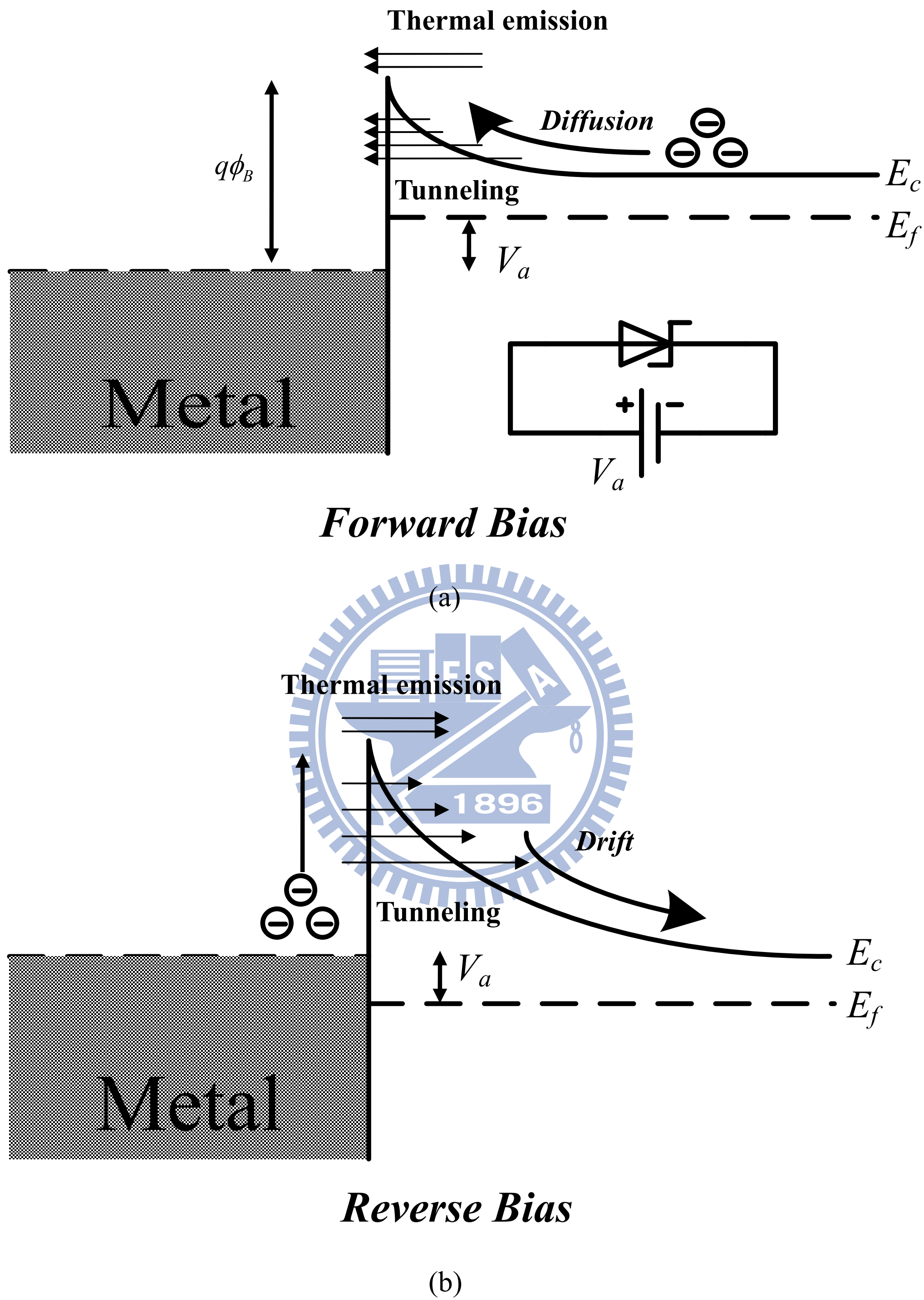


Fig. 2.4 Carrier transport mechanism of the Schottky contact in N-type semiconductor. (a) under forward bias (b) under reverse bias.

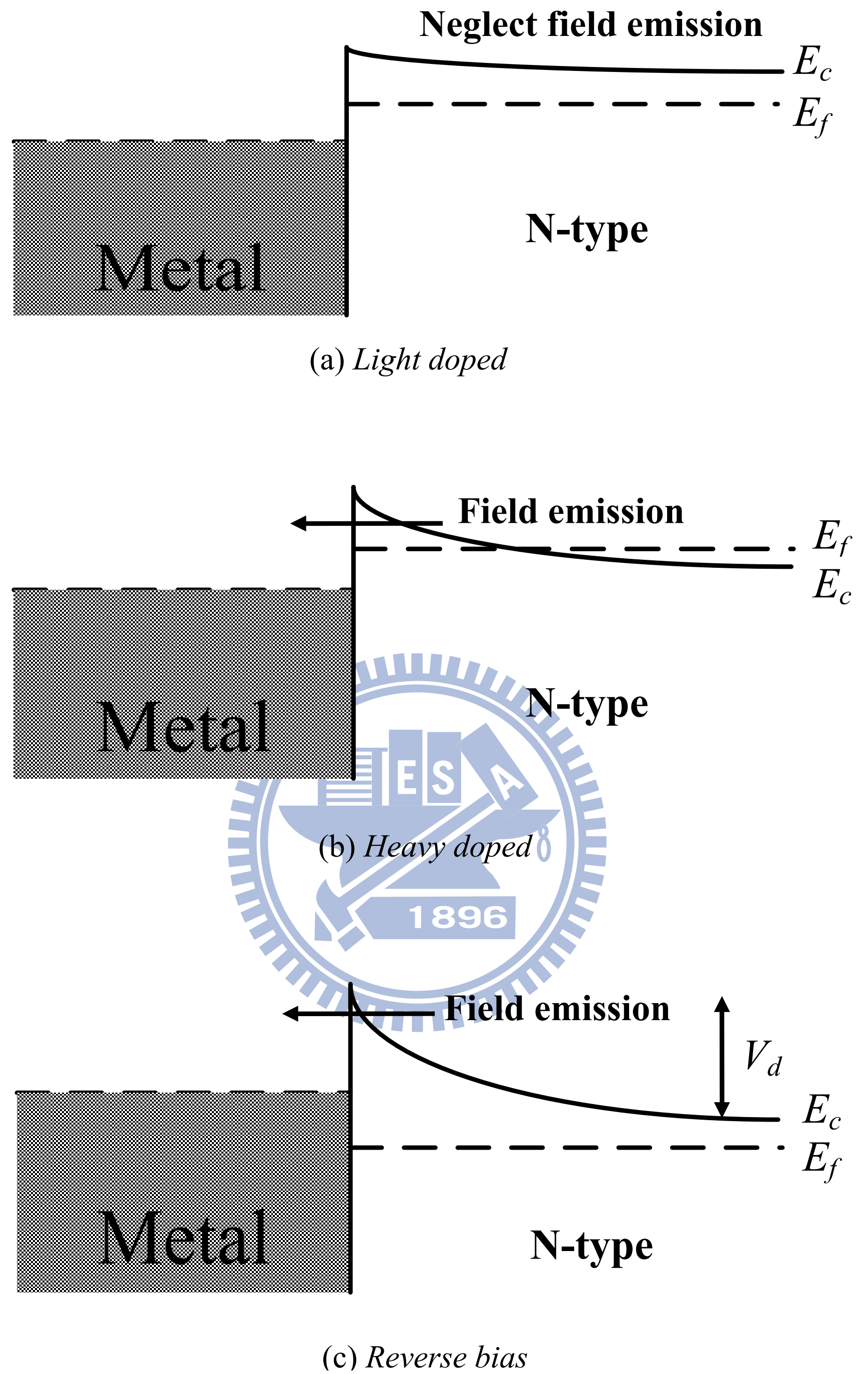


Fig. 2.5 Band diagram to deduce the probability of field emission (a) light doped condition (b) heavy doped (degenerate) condition (c) under reverse bias condition of a junction between n-type semiconductor and metal.

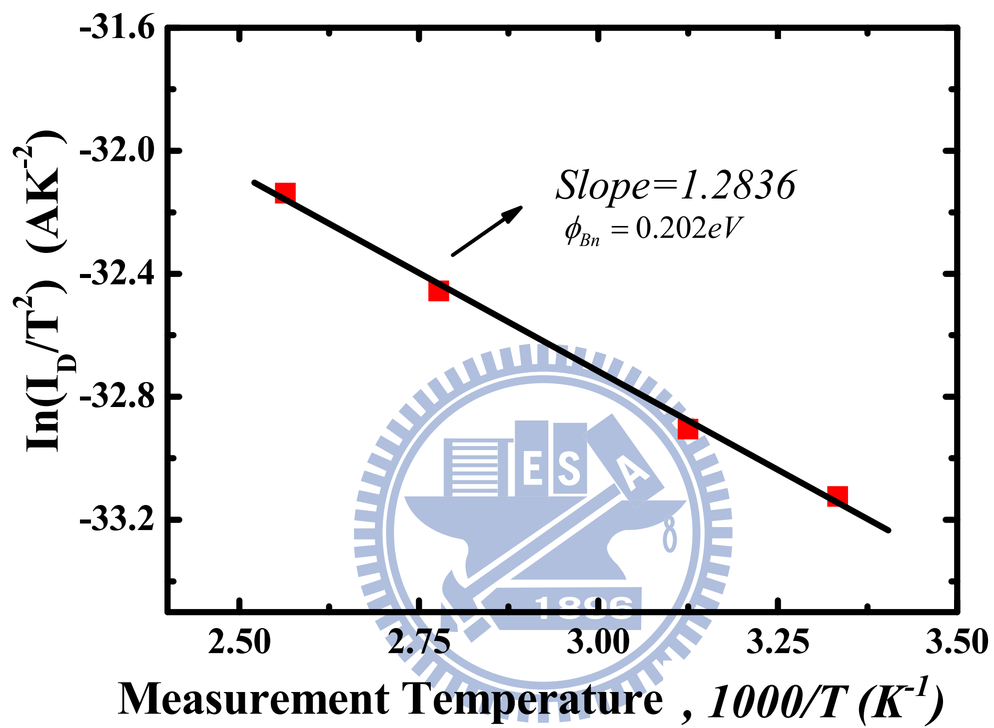
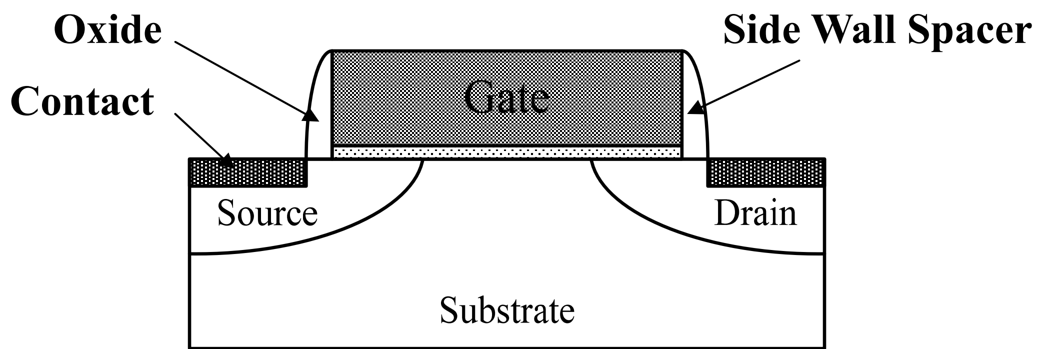
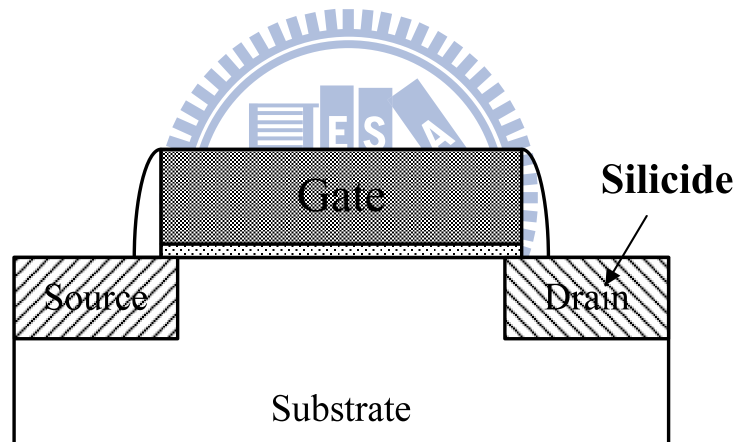


Fig. 2.6 Extracting the Schottky-barrier height by Activation-Energy method.

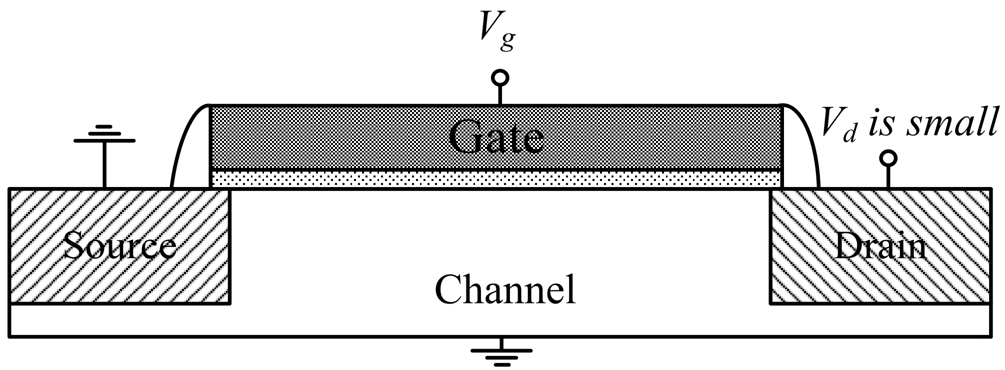


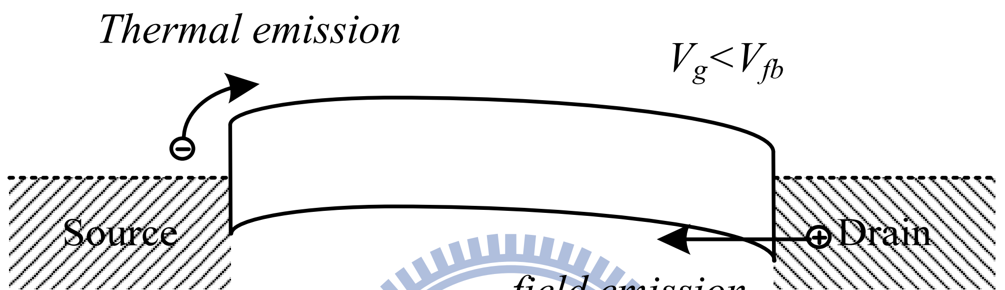
(a)



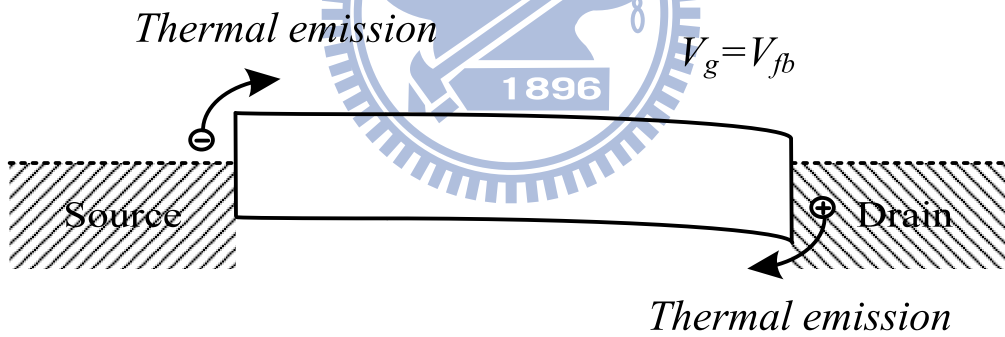
(b)

Fig. 2.7 The device structures (a) conventional MOSFET (b) Schottky-barrier MOSFET.

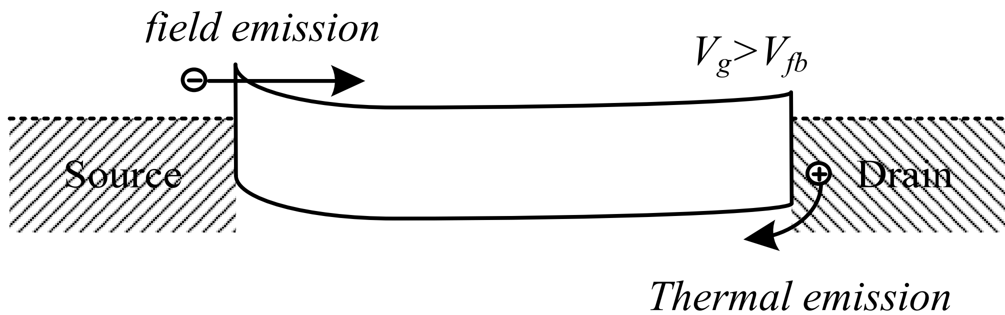




(a)



(b)



(c)

Fig. 2.8 Different band diagram of n-SBMOSFET (SB-NMOS). (a) *OFF-state*, $V_g<V_{fb}$ (b) *OFF-state*, $V_g=V_{fb}$ (c) $V_g>V_{fb}$.

1896

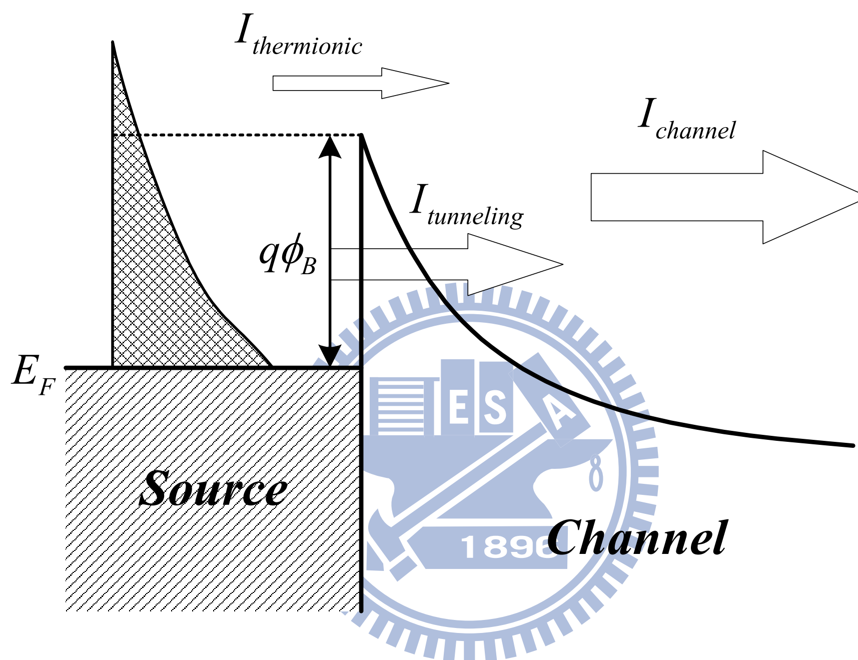
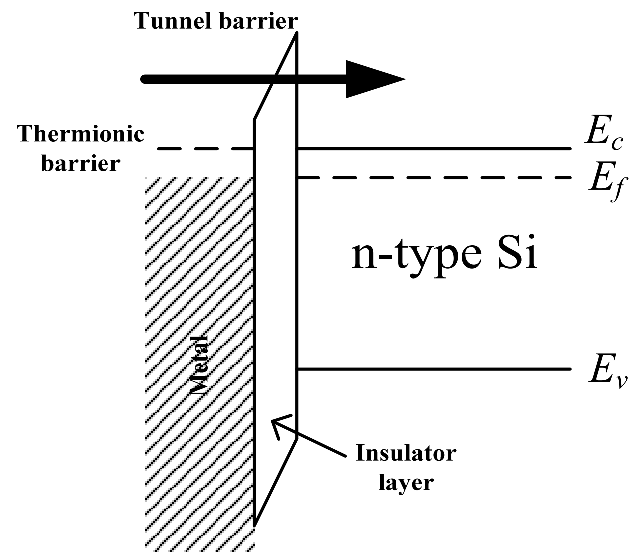
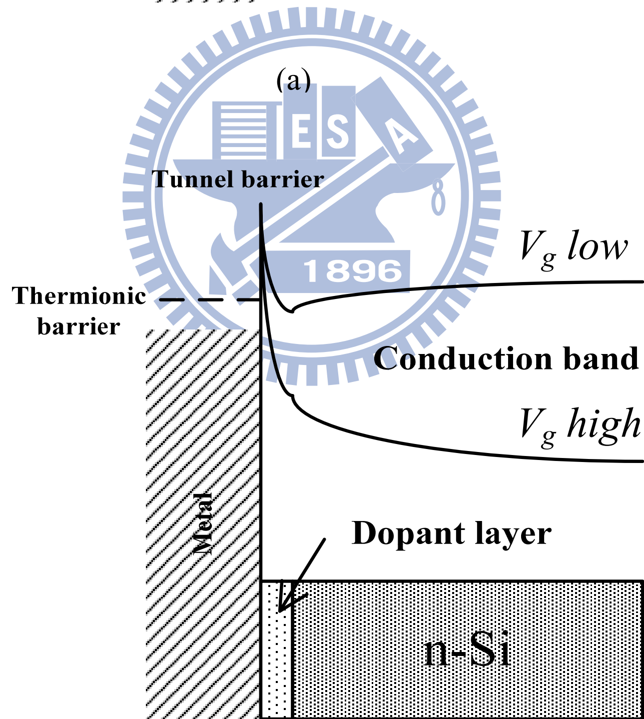


Fig. 2.9 Current components in the source to channel interface of Schottky-barrier nMOSFETs.

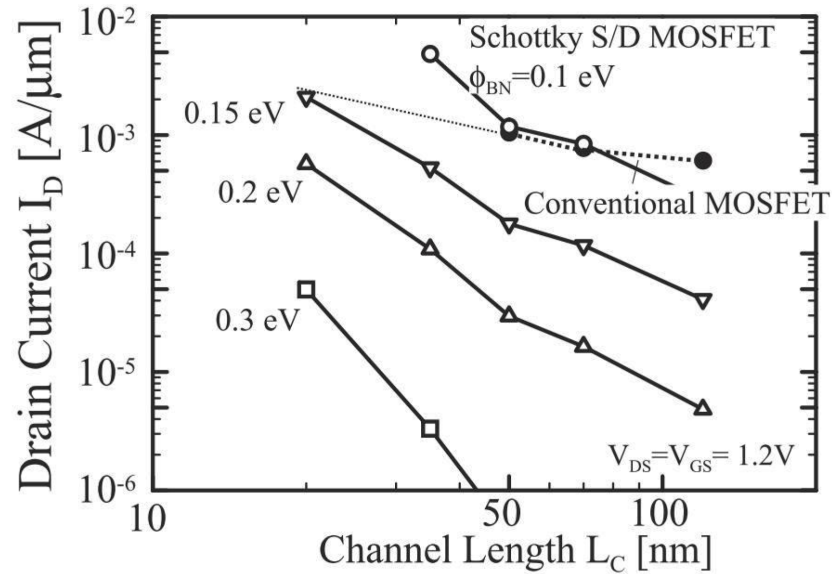


(a)

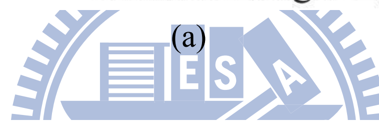


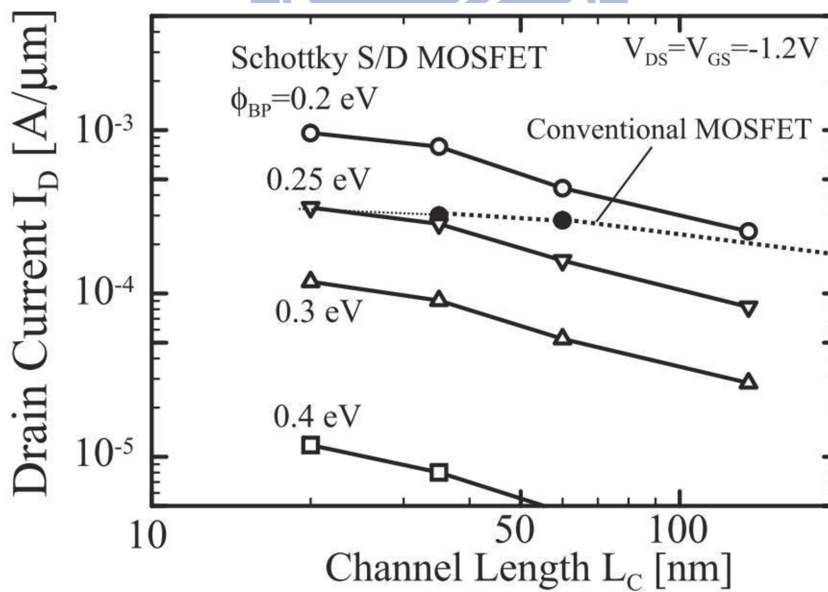
(b)

Fig. 2.10 Schottky barrier height reduction technology (a) with insulator layer (b) with dopant segregation implantation.



(a)





(b)

Fig. 2.11 Drivability of Schottky barrier MOSFET as a function of Schottky-barrier height for (a) N-type and (b) P-type devices [18].

Chapter 3
Device Preparation and Basic Characteristics

In advanced VLSI technology, the high-κ dielectric with metal gate, metal S/D SBMOS, process strained silicon and silicon-on-insulator technology are the most popular nowadays. Some of them are good for devices scaled down and conflicting short channel effect as we mentioned in the above chapter. In section 2.5.1, we demonstrated that the novel technologies for SBMOS to overcome poor performance due to high Schottky barrier height and small driving current. The most simple and popular method is dopant-segregation-implantation (DSI) technique which is developed by B.Y. Tusi [12]. On the other hand, the optimized method is first reported by A. Kinoshita [23]. In this chapter, first, we focus on how to optimize the Schottky barrier MOSFET with DSI technology and its manufacturing process. Then, we introduced our experimental setup. Finally, we demonstrate the basic characteristics of the sample devices.

3.1 Devices Preparation

In order to simplify the experiments, we controlled that the gate channel of the devices are in the same orientation of *<110>/(100)* which their gate oxide thickness are 1.4nm. The channel lengths are from *10μm* to *0.06μm*. The SBMOS with DSI fabrication process flow bases on the United Microelectronics Corporation (UMC) 65-nm technology node and is illustrated in Fig. 3.1. Following the gate stack formation, optimized offset spacer, halo and DSI implants were introduced. Then disposable spacer and deep S/D implant were performed in order to suppress the junction leakage. After disposable spacer removal, NiPt silicidation process was applied on either N or PMOSFET with DSI for its better immunity against line width effect and less silicon consumption. On the other hand, strain capping layer as high tensile SiN was performed to optimize the driving current. The split of the devices for both N and PMOS are figured in Fig. 3.2(a) and the cross-section TEM picture is shown in Fig. 3.2(b).

Besides, the conventional MOSFET were also prepared as control sample, see Fig. 3.2(a). The arsenic was implanted as a high doped layer between the S/D to substrate region and the doping concentration reached $2.5\times10^{20}cm^{-3}$. The depth of the interface between NiPt silicide and silicon is about *18nm*. The halo is implanted for suppressing the severe short channel effect and high leakage current [25]. In order to optimize the DSI energy, different implant energies are performed, see Table 1. Sample C was implanted with the highest DSI energy, and sample A was with the lowest energy. The order is

$$DSI_1 < DSI_2 < DSI_3,\ \ or\ \ A < B < C \tag{3.1}$$

The I_{on}-I_{off} characteristic and source/drain sheet resistance are shown in Fig. 3.3 [25]. Sample B has the optimized I_{on}-I_{off} characteristic. Besides, they all have the advantage of SBMOS, which is the lower source and drain sheet resistance than conventional MOSFET, is shown in Fig. 3.3(b). The sheet resistance is about 19% lower.

3.2 Experimental Setup

The experimental setup for the current-voltage measurement of devices is illustrated in Fig. 3.4. Both of the intrinsic and degradation behaviors of the devices can be achieve by this system. Each of the analyzers are connected by the co-axial or tri-axial cable, included the semiconductor parameter analyzer (HP 4156C), the low leakage switch mainframe (HP E5250A), the Cascade guarded thermal probe station, and a thermal controller. This facility provides an adequate capability for measuring the low leakage devices *I-V* characteristic. On the other hand, for precisely measuring of capacitance-voltage characteristic of the devices, LCR Meter (Agilent-HP 4284A) has been added. It provides the testing frequency from *20Hz* to *1MHz* for AC voltage. These analyzers are controlled by the corresponding software in the PC. Our group developed a control system in HT-Basic language. Through IEEE-488 (GPIB) cable, we can directly give the order to each analyzer. By the above system, the *I-V* and *C-V* characteristics of the MOSFET devices can be precisely performed.

3.3 Basic Characteristics of the Schottky-Barrier MOSFETs

In this section, we present the basic characteristics of the SBMOS, such as band diagram, short channel effect, current-voltage characteristics, and effective Schottky- barrier height. Then, we make a conjecture to the main factor of the SB-MOSFET characteristics.

3.3.1 Band Diagram of DSI-SBMOS

The band diagram of conventional Schottky barrier MOSFET is shown in the above chapter, see Fig. 2.8. However, the Schottky barrier MOSFET with dopant segregation implantation (DSI-SBMOS) is modified by the conventional SBMOS with the arsenic doped between S/D and substrate interface, see Fig. 2.10(b), and our sample devices split is shown in Fig. 3.2(a).

In order to understand the carrier transport mechanism, the band diagram of the DSI-SBMOS in the lateral direction is important. We compared the conventional SBMOS with the DSI-SBMOS as shown in Fig. 3.5 at small drain bias. The arsenic with high doping concentration induced a high electric field near the S/D to channel interface by the barrier adjustment method in [15]. Thus, the band diagram is pulled down by this high dose layer, which leads to thin down the Schottky barrier. It is called dopant segregation implantation (DSI) technique. In this optimized process, the barrier becomes the shape of the spike and leads to high tunneling current. We define that the barrier between source to channel interface and the lowest conduction band edge near the source side as Schottky barrier or tunneling barrier, and the barrier between the two lowest conduction band edges near S/D side in the channel as channel barrier, we marked them in Fig. 3.5(b). On the other hand, the holes in the valance band see a higher barrier that they are not easy to emit through it. This suppressed the *OFF-state* current and improved the current-voltage (*I-V*) characteristic.

3.3.2 Basic Characteristics of DSI-SBMOS

Figure 3.6 shows the short channel effect of our devices, and sample B is the optimized sample. In short channel region, we can see that the lager the DSI energy is, the smaller the V_{TH} is. Fig. 3.7(a) is the drain current versus gate voltage plot (I_D-V_G). The drain current versus drain voltage curve (I_D-V_D) is shown in Fig. 3.7(b). Fig. 3.8 shows the I_D-V_G plot at $|V_D|= 0.1V$ with different DSI energy, both N and PMOS, the larger the DSI energy is, the larger the *OFF-state* current (I_{off}) is.

3.3.3 Current Flow Mechanism

The carrier transport mechanism is an important issue for Schottky barrier MOSFETs. Some paper explained the current transport mechanism in the *ON-state* by operational temperature variation [29], but the analyzed process is ambiguous. In order to understand the refined current transport mechanism, we investigated the effective Schottky-barrier height profiles.

The most important parameter for Schottky barrier MOSFET is the Schottky barrier height which blocks most of the injection carriers from source to channel as we have mentioned in the above chapter. In order to measure the Schottky barrier height, we applied the "*Activation-Energy Measurement*" which is reported by SZE [15] and we have reported in section 2.2.3. In comparison with the Schottky diode, SBMOS is a four-end device. So, we define the measured barrier height as effective Schottky-barrier height, $\phi_{B,eff}$, and is measured from source to channel junction as the following:

$$\phi_{B,eff} = \phi_{B,eff}(V_G, V_D). \tag{3.2}$$

The parameter is a function of the gate and drain voltage due to the two voltages will influence the barrier height and thickness [30]. Fig. 3.9 shows the calculated effective Schottky barrier height of SB-PMOS with sample A and B. When the SB-PMOS operates in

very positive bias, by ambipolar characteristic, the transport carriers, which are electrons from drain end, transport by field emission (tunneling) mechanism and see a very thick barrier blocked some of carriers in the conduction band. That contributes to a very high effective Schottky-barrier height form difficult tunneling. If the gate bias is increasing positively for PMOS, the tunneling barrier is thinner that are easy to tunneling. Thus, the top of the effective Schottky-barrier height is decreasing as gate bias is increasing positively. As the gate voltage is increasing negatively, the SB-PMOS entered subthreshold region. In this region, the SB-PMOS with dopant segregation implantation produces a thin tunneling barrier which is easy for holes to tunnel through in the valance band. However, the carriers tunneled through the tunneling barrier, and then they see a lower channel barrier. When the gate bias increases, the channel barrier decreases. This makes the effective Schottky-barrier decrease. As in Fig. 3.9, the effective Schottky-barrier height is linear to gate voltage, which means the current is contributed by thermionic emit through the channel barrier. Hence, the subthreshold current is quite small that produces a small subthreshold swing, which is called *DIBL-like* effect. When the gate bias is larger than threshold voltage (in Fig. 3.9, $V_G - V_{TH} = 0$), a negative effective Schottky-barrier height formed. The band diagram is illustrated in Fig. 3.10. The dashed line is the *OFF-state* conduction band edge and the solid line is *ON-state* for NMOS [30]. In this region, the channel barrier is lower than flat band (V_{fb}). Most of the transport carriers tunneled through the tunneling barrier and see a negative channel barrier. Hence, the negative Schottky-barrier height is formed. Therefore, the tunneling current is the main transport method in the *ON-state*. It is worthy to be mentioned that the carriers are non-local tunneling here.

Based on the above, the external bias (V_D ,V_G) can only vary the channel barrier but Schottky barrier. This implies that the barrier pinning position is change to the interface between DSI layer and bulk effectively. Thus, the effective Schottky-barrier height presents the channel barrier variation. On the other hand, by Fig. 3.9, we concluded that the larger the DSI energy is, the lower effective Schottky barrier height is.

Another important issue for current transport mechanism is body effect. Fig 3.11 is the effective Schottky barrier height of SB-PMOS ($\phi_{B,eff}$)with different substrate bias (V_B). When V_B is decreasing toward minus region for PMOS, the threshold voltage is decreasing positively. And the channel barrier will be raised up, see Fig. 3.12. As in the above words, the top of the effective Schottky-barrier height is from the minority carrier tunneled through the barrier. For PMOS, electrons see a raised conduction band edge that makes the effective Schottky-barrier height increase. In addition, the effective Schottky barrier height is independent on channel length, see Fig. 3.13. The two devices (*0.36* and *0.5μm*) have the same threshold voltage. The comparison of conduction band diagram is shown in Fig. 3.14, including conventional MOSFET, conventional SBMOS and DSI-SBMOS. By the effective channel barrier pinning, the tunneling barrier is independent to length.

3.3.4 Conductivity on DSI-SBMOS

We have explained the process of dopant segregation implantation on Schottky-barrier MOSFET. Also, the operational carrier transport mechanism is performed by effective Schottky-barrier height. The DSI-layer will pull down the Schottky barrier that enhances the carrier tunneling probability in the source side. Some researcher had verified this phenomenon by conductivity theory [31]. By a modified one-dimensional Poisson equation:

$$\frac{d^2\phi_f}{dx^2}-\frac{\phi_f-\phi_g+\phi_{bi}}{\lambda^2}=\frac{e\left[\rho(x)+N_{seg}\right]}{\varepsilon_0\varepsilon_{si}} \tag{3.3}$$

where ϕ_f is the surface potential, ϕ_g is the gate potential and ϕ_{bi} is the build-in potential. And, λ is the relevant length scale on which potential variations are being screened, as eq. (3.4).

$$\lambda=\sqrt{\frac{\varepsilon_{si}d_{ox}d_{si}}{\varepsilon_{ox}}}\,. \tag{3.4}$$

The effect of dopant segregation implantation is accounted for by a step-function-like doping profile in [31] of spatial extension l_{seg} and doping concentration N_{seg} in the source/drain to

channel interfaces. The charge $\rho(x)$ in and current through the channel is calculated employing the non-equilibrium Green's function formalism, where the equation for the charge is solved self-consistently with eq. (3.3). After self-consistency is reached, the current is computed according to eq. (3.11).

$$I_d = W \times \frac{2e}{h} \int dE \left[T(E)(f_s - f_d) \right] \tag{3.5}$$

where $f_{s,d}$ are the Fermi distributions of source/drain and $T(E)$ is given by the Fisher-Lee relation which is the transmission function for carriers moving from source to drain [32]. The conductivity (Γ) is contributed by eq. (3.6).

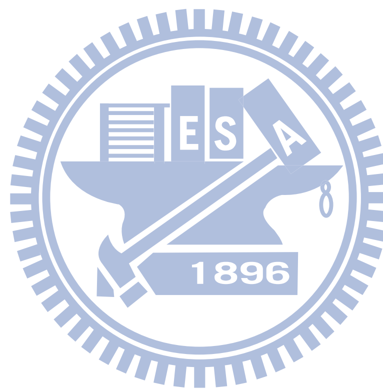
$$\Gamma = \left(\frac{e^2}{2\pi\hbar} \right) \frac{|t|^2}{|r|^2} \quad . \tag{3.6}$$

Here, t is the transmission and r is the reflection coefficient. It is assuming that the first subband contributes most to the current. So, the expressions for charge and current are averaged over the direction of W only. Besides, higher subbands are accounted for by a numerical factor that leads to higher tunneling energy [33]. Hence, ballistic transport coefficient is assumed to give an upper estimate of the possible device performance. This is the first theory on ballistic transport [32] and leads to Natori's backscattering theory that we will introduce in the next chapter.

3.5 Summary

We make a summary of the relations between DSI energy and basic characteristics which we have mentioned in the last section. When the DSI energy is increasing, the V_{TH} is decreasing, I_{off} is increasing and $\phi_{B,eff}$ becomes lower. This is due to the increasing of the DSI energy, the lowest of the conduction band edge of the channel will be far from the S/D to channel interface, see Fig. 3.15 (a), and channel barrier will be lower when drain voltage is applied. Similarly, the $\phi_{B,eff}$ is the channel barrier which influences the carrier transport in the devices. In other words, the V_{TH} and $\phi_{B,eff}$ are determined by the channel barrier. Further, the channel barrier is dominated the DSI-SBMOS current-voltage characteristics. Besides, the

holes see a lower barrier that they are easy to emit above it. As shown in Fig. 3.15 (b), the barrier is lower when DSI energy is larger. By these inferences, the channel barrier is more significant than Schottky barrier in DSI-SBMOS. Finally, it is important for us to understand the carrier injection phonemes and the backscattering probability in front of the channel barrier.



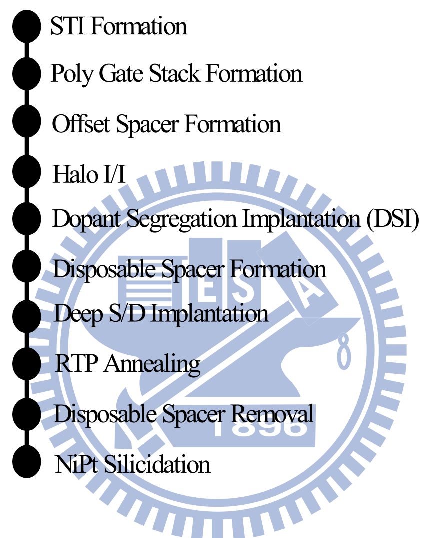
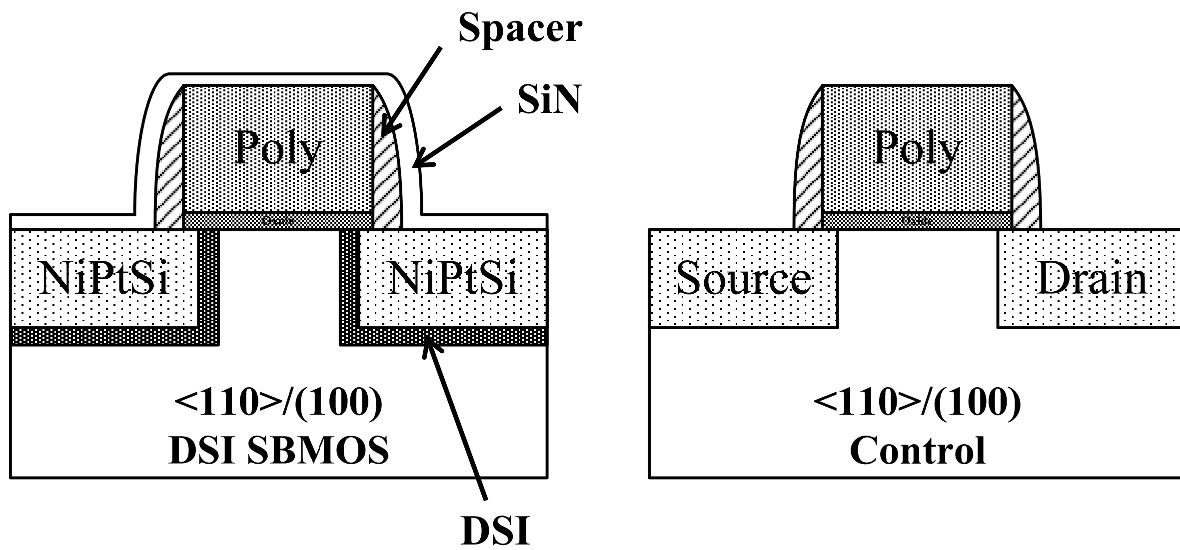
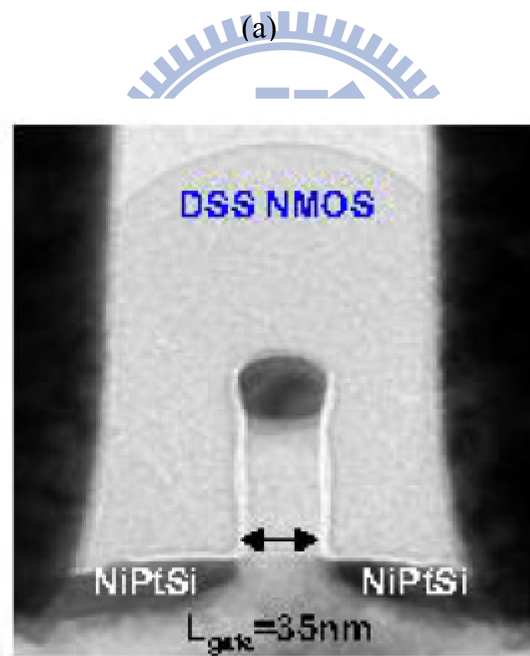


Fig. 3.1 Process flow of Schottky-barrier MOSFETs with DSI NiPt silicide.



(a)

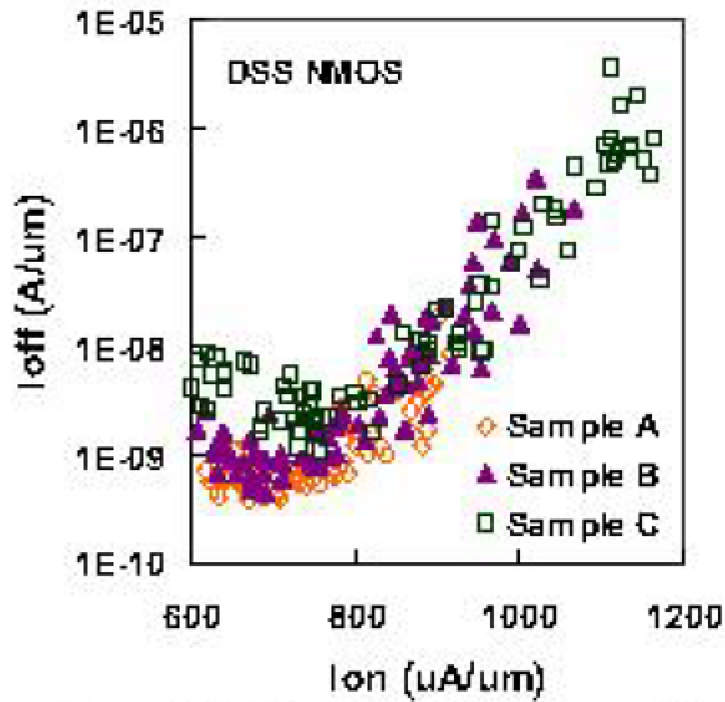


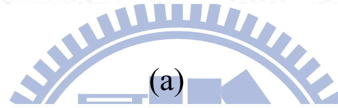
(b)

Fig. 3.2 (a) Device split of Schottky-barrier MOSFETs with DSI NiPt silicide and conventional MSOFET and (b) its crocess-section TEM picture with the shortest length 35nm [25].

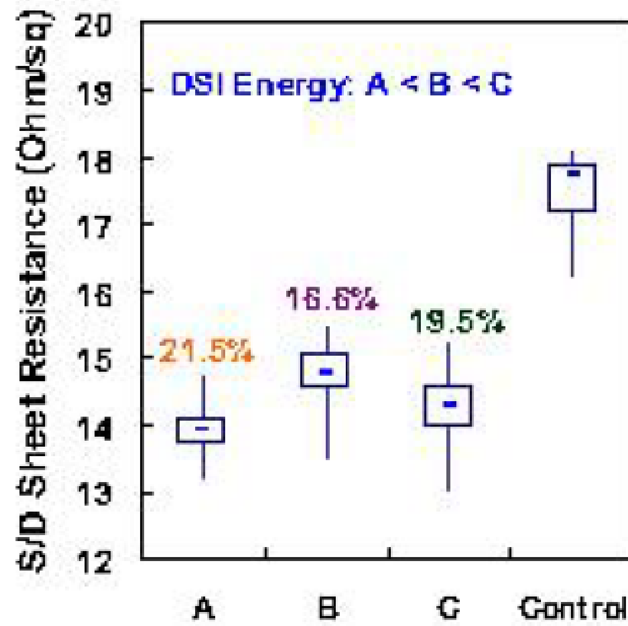
Sample		DSI Energy	w/ halo	Strain capping layer
SBMOS	A	DSI 1	Baseline	High tensile SiN
	B	DSI 2		
	C	DSI 3		
Control		L		.

Table 3.1 Splits of SBMOS with different DSI energies. The DSI energy relation is $DSI_1 < DSI_2 < DSI_3$, and marks as sample A, B and C.





(a)



(b)

Fig. 3.3 (a) The I_{on}-I_{off} characteristics of Sample A, B and C. Sample B has the optimized characteristic. (b) All of them show the reduced S/D sheet resistance [25].

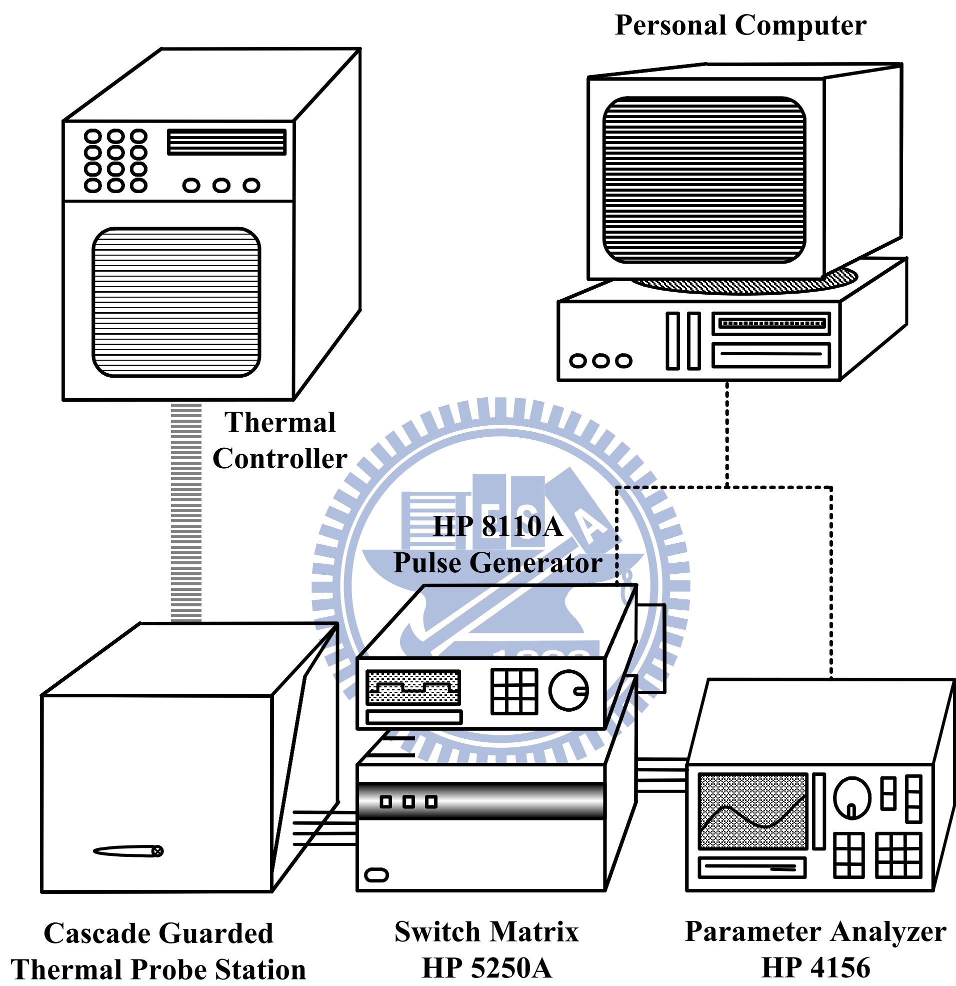


Fig. 3.4 The experimental system of current-voltage (*I*-*V*) for both N or PMOSFETs.

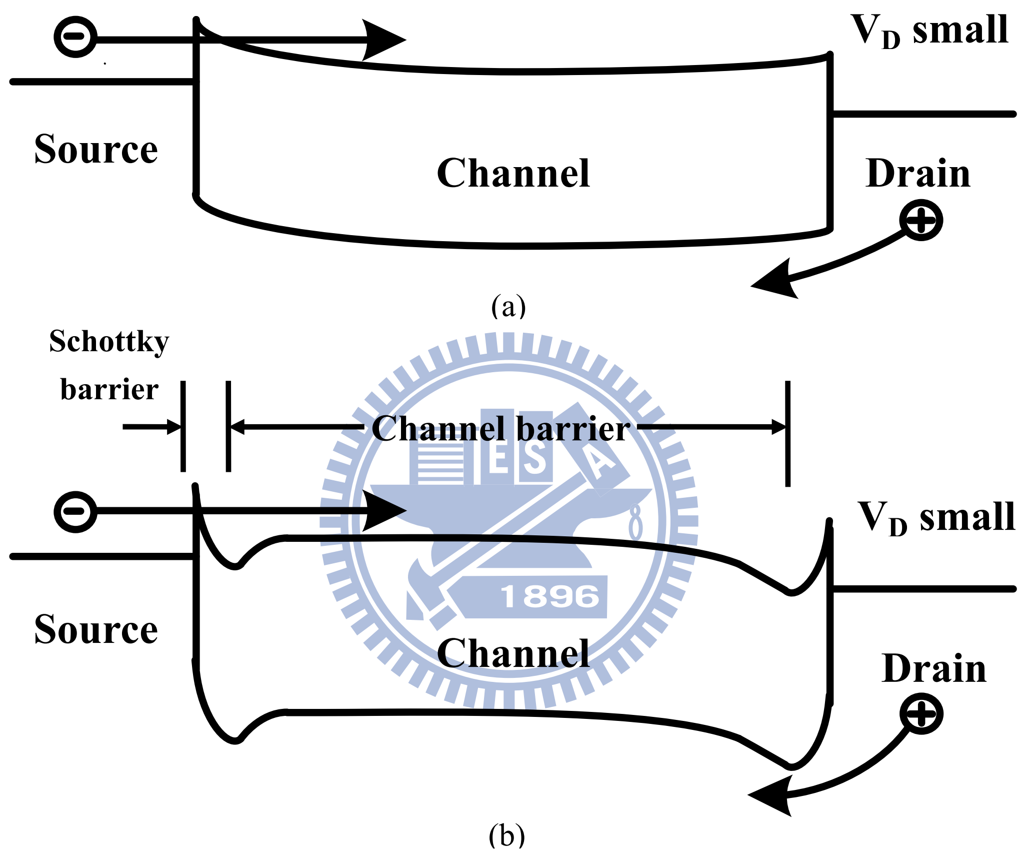


Fig. 3.5 Conduction band diagram of the (a) conventional SBMOS (b) SBMOS with dopant segregation implantation (DSI-SBMOS) when V_D is small bias.

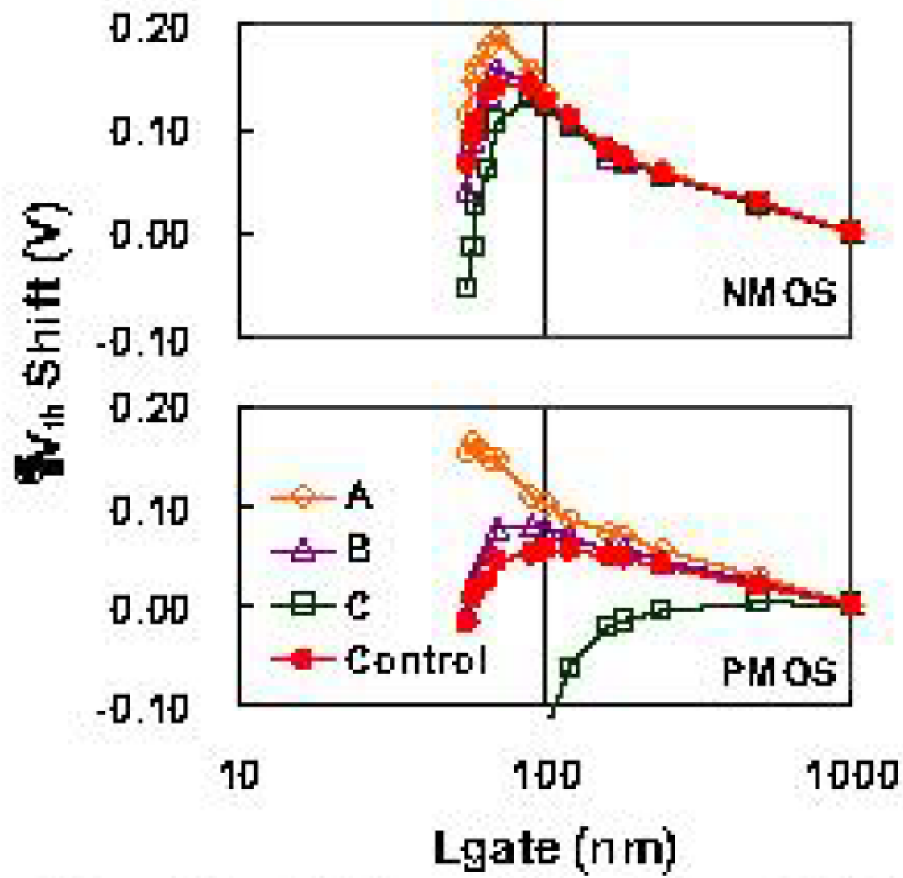
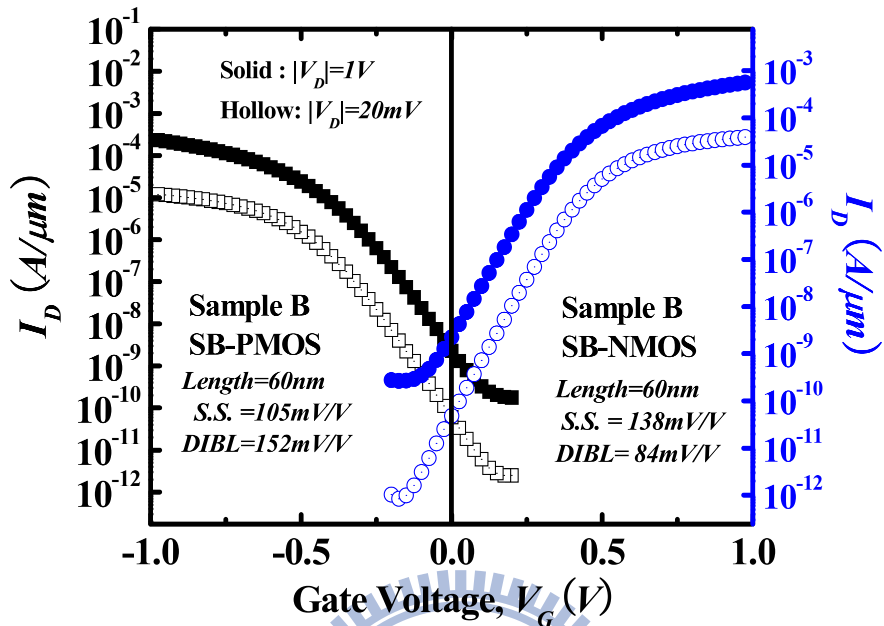
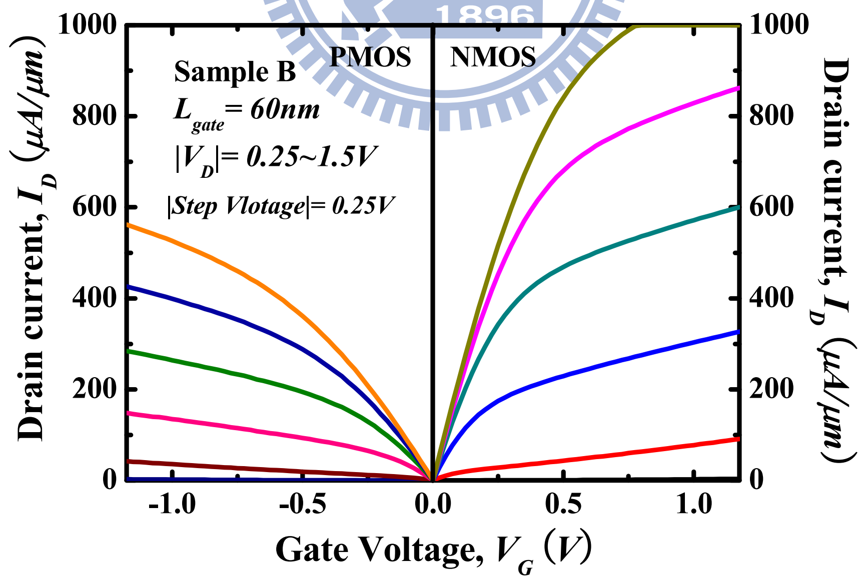


Fig. 3.6 Short channel effect of the DSI-SBMOS [25].

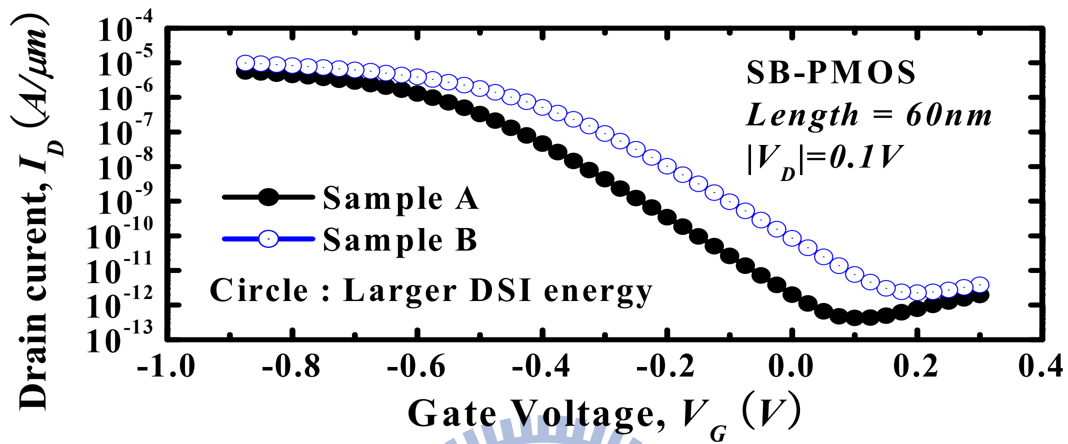


(a)

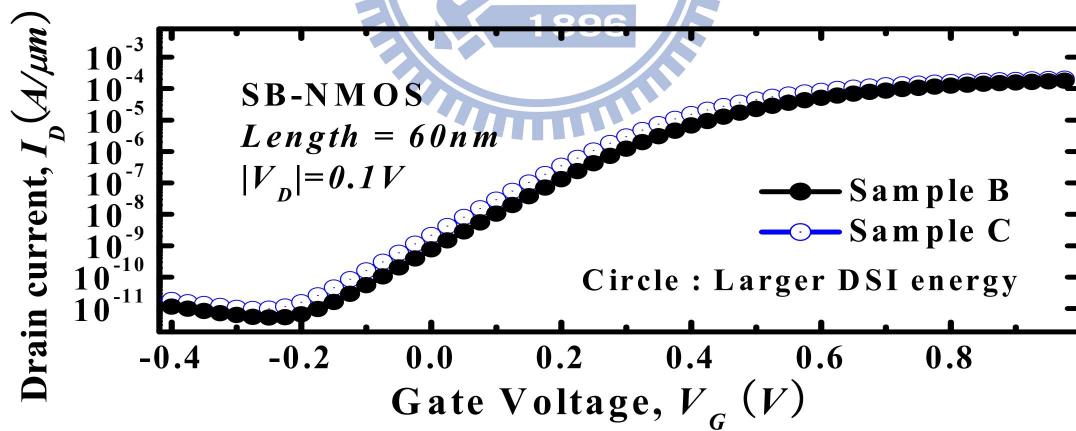


(b)

Fig. 3.7 Some characteristics of the DSI-SBMOS (a) I_D-V_G curve (b) I_D-V_D curve.



(a)



(b)

Fig. 3.8 Drain current versus gate voltage curve (I_D-V_G) with different DSI energy when $|V_D|=0.1V$. (a) SB-PMOS (b) SB-NMOS.

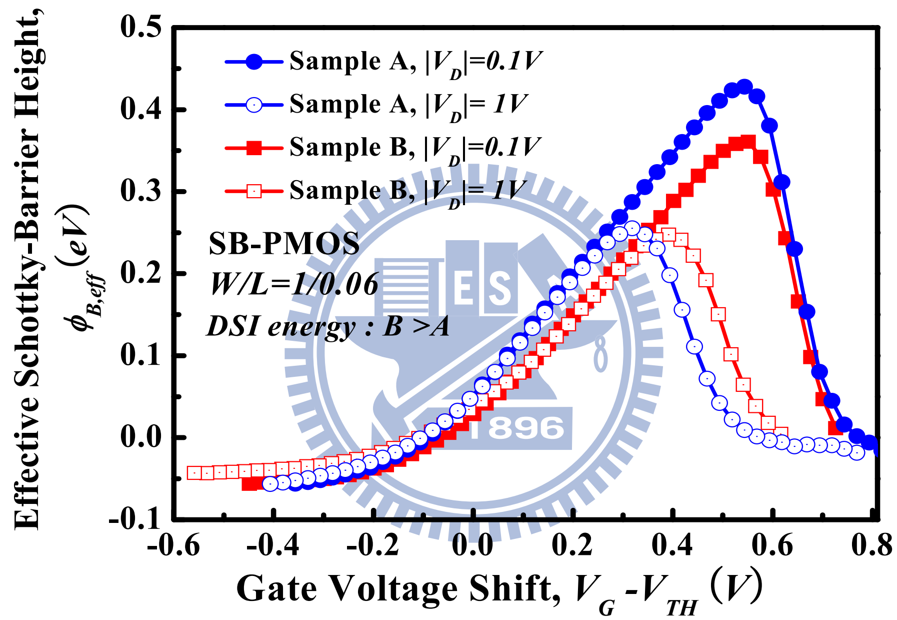


Fig. 3.9 The effective Schottky-barrier height of different DSI energy in SB-PMOS.

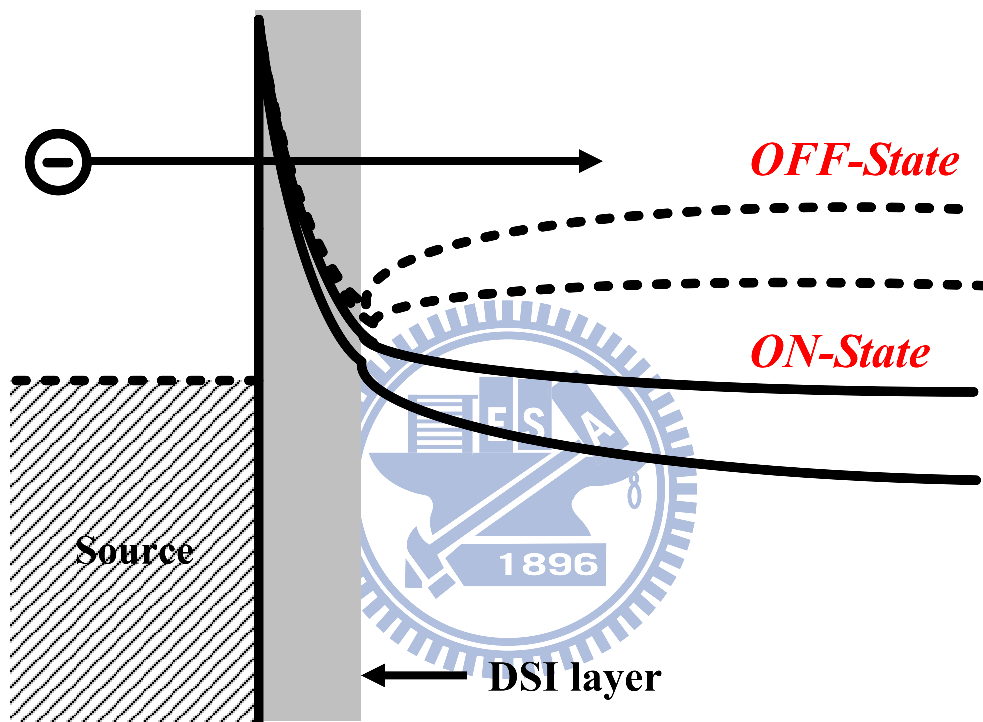


Fig. 3.10 The conduction band edge of SBMOS with different bias condition. The dash line is *OFF-state* and solid line is *ON-state*.

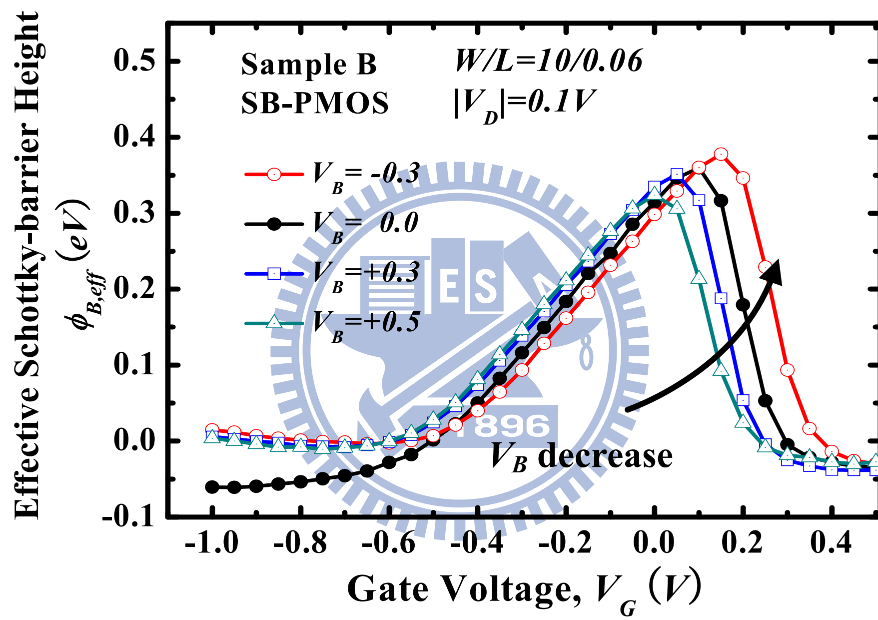


Fig. 3.11 The effective Schottky-barrier height of SB-PMOS with different bulk bias (V_B).

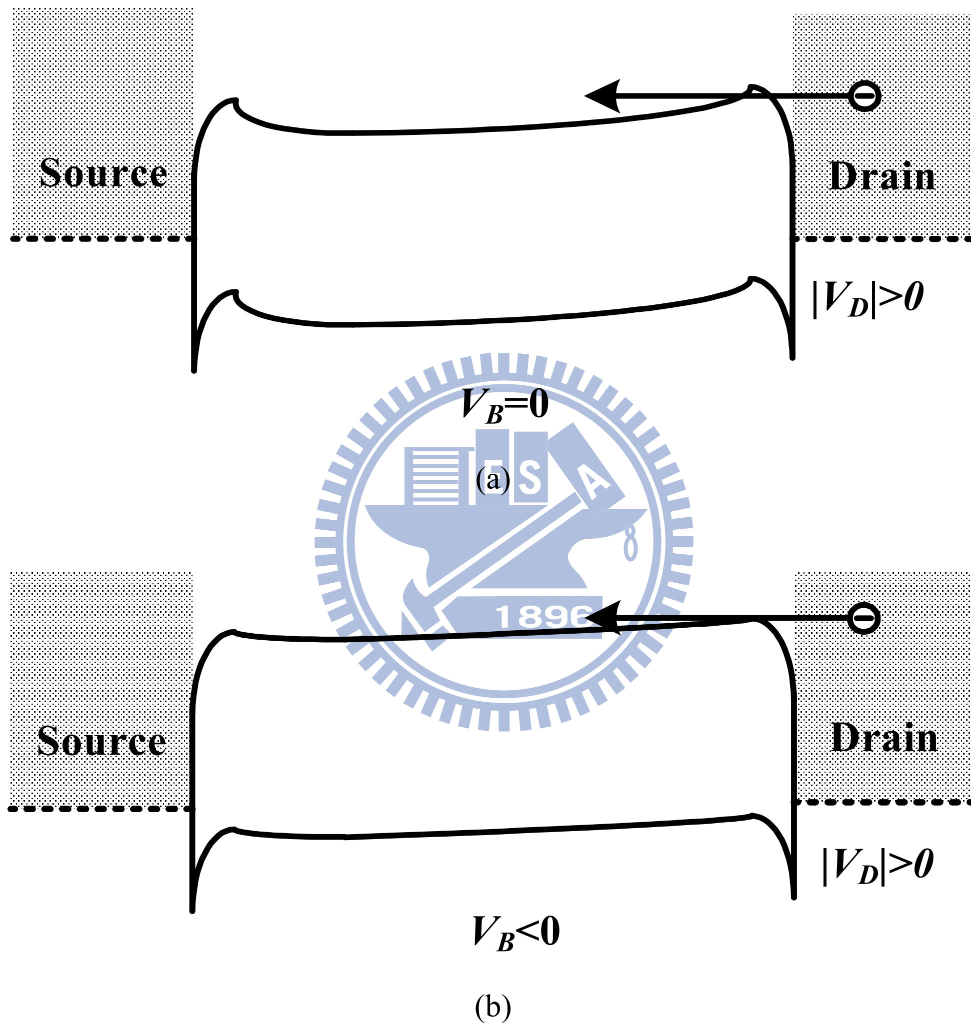


Fig. 3.12 The band diagram for different substrate bias of (a) $V_B=0$ (b) $V_B<0$ for Schottky-barrier pMOSFETs.

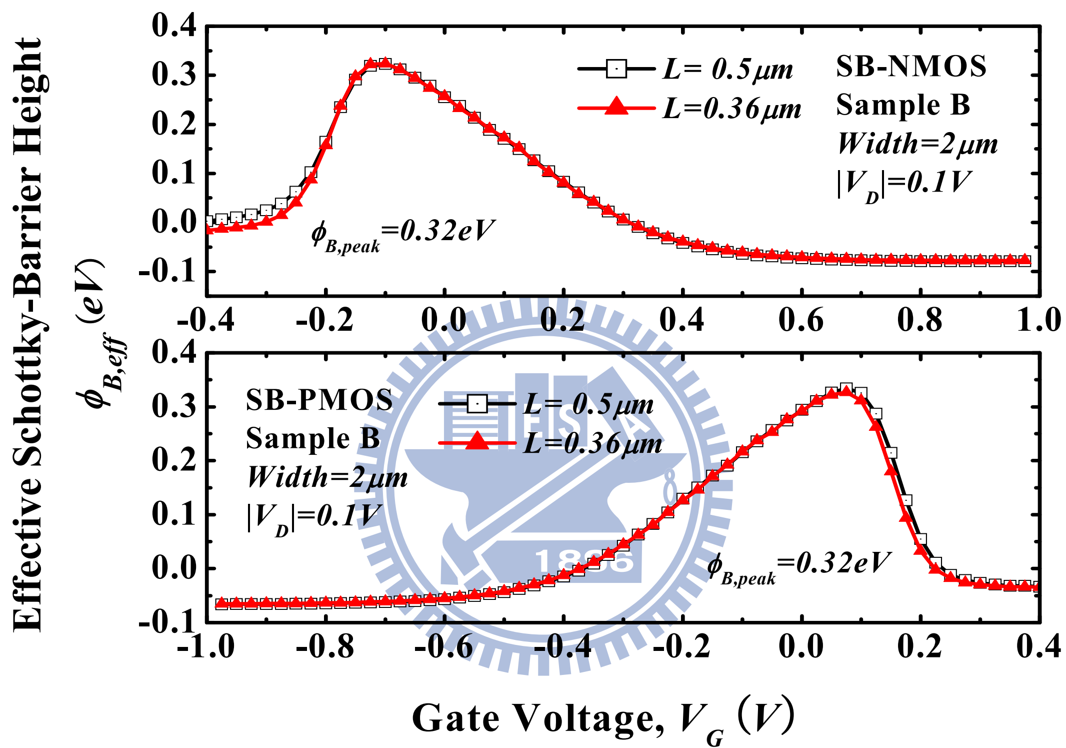


Fig. 3.13 The effective Schottky-barrier height of both N and PMOS with different channel length.

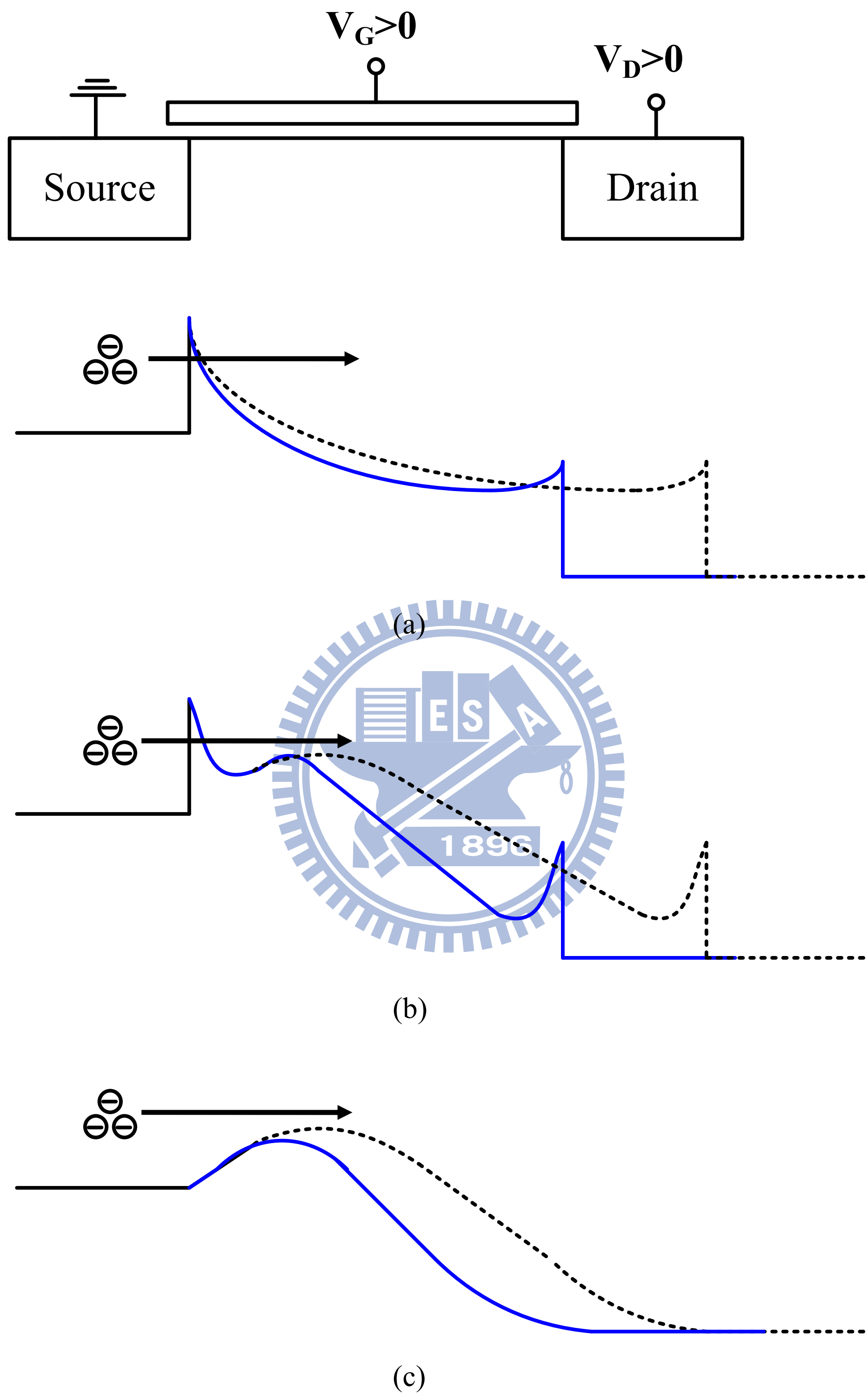


Fig. 3.14 The conduction band edge with different devices (a) Conventional SBMOS (b) DSI-SBMOS (c) Conventio-nal MOSFET. The solid line is short channel and dash line is long channel devices.

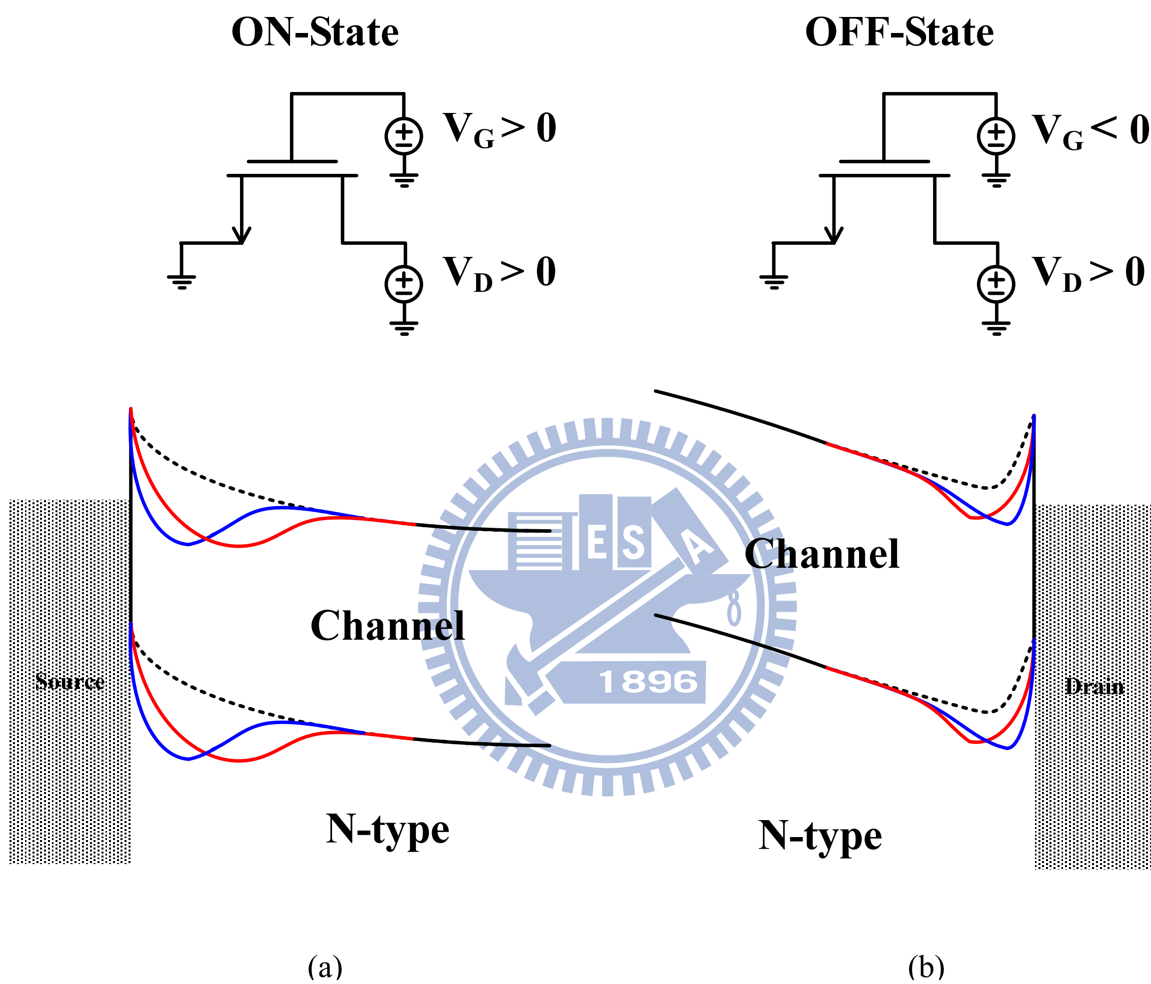


Fig. 3.15 The band diagram of the DSI-SBMOS with different DSI energy in (a) *ON-state* (b) *OFF-state*. The DSI energy of the blue line is lower than red line. The dash line is the conventional SBMOS band diagram.

Chapter 4
Carrier Ballistic Transport in Schottky-Barrier MOSFETs

Semiconductor devices have been scaled down to the nanoscale region and entered the quasi-ballistic operation mode. Because of the physical limitations of carrier transport, the drift-diffusion model for describing carrier transport becomes less significant in the nanoscale MOSFETs. From the quasi-ballistic toward ballistic region, K. Natori brought up a new insight for modeling the carrier transport phenomenon which is called ballistic theory or backscattering theory in 1994 [33]. Later in 1997, Mark S. Lundstrom developed the complete theorem for explaining the physic of ballistic and quasi-ballistic phenomenon for nanoscale MOSFETs [1]. Besides, in 2002, two experiments for extracting the backscattering coefficient have been reported. One is the current-voltage (*I-V*) fitting [2] and the other one is temperature dependent method by M. J. Chen [7].

In this decade, the ballistic coefficient of several devices such as bulk-Si, strained-Si, SOI, and etc. have been researched [9]. For SBMOS, the ballistic transport is not easy to explain due to its special carrier transport characteristics we have reported in chapter 3. In this chapter, we applied the mobility view to explain the backscattering phenomenon for SBMOS which has been the first being reported.

4.1 Introduction of Ballistic Theory

In this theory, we treat the moving carriers as the quantum wave. This kind of wave goes through channel from source to drain. When the waves move toward the channel, they bomb into an non-negligible quantum barrier which leads to transmission and reflection in quantum mechanics. In saturation region of MOSFETs, the channel barrier is like the shape of hills; see Fig. 4.1(a). The length l is called critical length or critical distance which means about the energy drops $k_B T$ from the top of the channel barrier, where k_B is Boltzmann's constant and T is the temperature in Kelvin coordinates. In the gray area of Fig. 4.1(a), which is called

k_BT-layer, carriers pass thermally through the channel barrier and get a lot of scatterings. The scattering process in the channel is due to impurity scattering, lattice vibration and surface roughness. We represent the current flow in the linear region as the following equations [3]:

$$I_{D,lin} = WC_{ox}\upsilon_{inj}\frac{1-r_{lin}}{(2k_BT/q)}(V_{GS}-V_{T,lin})V_{DS} \tag{4.1}$$

$$r_{lin} = \frac{L}{L+\lambda_0} = \frac{1}{1+\lambda_0/L} \tag{4.2}$$

where W is the device width, L is length, υ_{inj} is the thermal injection velocity from the maximum of the channel potential, C_{ox} is the oxide capacitance, r_{lin} is the backscattering coefficient in the linear region ($V_D<k_BT/q$), $V_{T,lin}$ is the threshold voltage of the linear region of the MOSFET, and λ_0 is the mean-free-path in linear region. λ_0 is about a few nanometers and is function of the length, gate and drain voltage. While, in the saturation region, we have:

$$I_{D,sat} = C_{ox}W\upsilon_{inj}\left(\frac{1-r_{sat}}{1+r_{sat}}\right)(V_G-V_{T,sat}) \tag{4.3}$$

$$r_{sat} = \frac{l}{l+\lambda} = \frac{1}{1+\lambda/l} \tag{4.4}$$

where r_{sat} is the backscattering coefficient of the MOSFET in the saturation region, which is also called r_c, $V_{T,sat}$ is the threshold voltage in the saturation region, and λ is the mean-free-path.

4.1.1 Derivation of the Backscattering Theory

As aforementioned, we treat the carriers as quantum wave. From the quantum point of view, the carriers transmit or reflect from the barrier. Backscattering rate depends on the shape of the channel barrier. Thus, we illustrate the moving carriers as a carrier flux, which is shown in Fig 4.1(b). The carriers flux incident to the barrier is F, and $(1-r_c)F$ is the transmitted flux. In this situation, r_c is a very important parameter which determines the total transmitted flux.

In Fig 4.1(a), the conduction band diagram of conventional MOSFETs is performed, E_{C1} is equilibrium condition ($V_D=0$) and E_{C2} is non-equilibrium condition ($V_D>0$). F^+ means the

injected flux from the source to drain, and F^{-} is from drain to source, respectively. We can use the scattering matrix to deduce the backscattering theory [4]. The scattering matrix can be written as

$$S=\begin{bmatrix} T & 1-T' \\ 1-T & T' \end{bmatrix} \tag{4.5}$$

where T and T' represent the fraction of the steady-state right- and left-directed fluxes that transmit across the quantum barrier which are the transmission coefficient of F^{+} and F^{-}.

In equilibrium condition ($V_D=0$), the matrix is symmetrical.

$$T=T' \tag{4.6}$$

In non-equilibrium condition ($V_D>0$), T' depends exponential on the barrier encountered lightly. We represent the T' by $Te^{-qV_D/kT}$, where T is larger than T_0 due to $DIBL$. The scattering matrix is the following matrix:

$$S=\begin{bmatrix} T & 1-Te^{-qV_D/kT} \\ 1-T & Te^{-qV_D/kT} \end{bmatrix} \tag{4.7}$$

Thus, the current flow can be described as

$$I_{DS}=W\left[J^{+}(0)-J^{-}(0)\right]=W\left[TJ^{+}(0)-T^{-}J^{-}(L)\right] \tag{4.8}$$

Also,

$$J^{-}(0)=qF^{-}(0)=q\left[F^{-}T^{-}+(1-T)F^{+}\right]=J^{-}(L)T^{-}+(1-T)J^{+}(0) \tag{4.9}$$

Then, we have

$$I_{DS}=qW\left(F^{+}T-F^{-}Te^{-qV_D/kT}\right)=qW\left[F^{+}(1-R)-F^{-}(1-R)e^{-qV_D/kT}\right] \tag{4.10}$$

where $R=1-T$. If the MOSFET operated in the linear region, the operational conditions are

$$V_D \ll {kT}/{q},\ F^{+}\approx F^{-} \text{ and } R\approx R_0 \tag{4.11}$$

We get

$$I_D \approx qW\left[F^{+}(1-R_0)-F^{-}(1-R_0)\left(1-\frac{qV_D}{kT}\right)\right]=qWF^{+}(1-R_0)\frac{qV_D}{kT} \tag{4.12}$$

In the source end of the channel, the product of total density of the carrier $n(0)$ and the thermal injection velocity $\upsilon_{inj}(0)$ is:

$$n(0)\upsilon_{inj}(0)=\frac{Q_i(0)\upsilon_{inj}(0)}{q}=\frac{C_{eff}(V_G-V_T)\upsilon_{inj}}{q}$$
$$=(1+R)F^{+}+(1-R)F^{-}=2F^{+}. \tag{4.13}$$

Here, we simplified $\upsilon_{inj}(0)$ by υ_{inj} and V_T is the threshold voltage. By eq. (4.12) and (4.13) and r_{lin} represents R which is the reflection coefficient in the linear region, we have:

$$I_{D,lin}=W\frac{\upsilon_{inj}}{2k_BT/q}C_{eff}(1-r_{lin})(V_G-V_{T,lin})V_D \tag{4.14a}$$

$$B_{lin}=1-r_{lin} \tag{4.14b}$$

Besides, by the thermal equilibrium hemi-Maxwellian, the average velocity of source to channel side (υ^+) and drain to channel side (υ^-) are

$$\upsilon^{+}=\upsilon^{-}=\upsilon_T=\sqrt{\frac{2k_BT}{\pi m^*}} \tag{4.15}$$

,which produces low drain current.

On the other hand, the MOSFET operated in the saturation region, the operational conditions are

$$V_D\gg kT/q \tag{4.16}$$

Eq. (4.10) is rewritten and combining with total density of the carrier and thermal injection velocity, i.e.,

$$I_D=qWF^{+}(1-R) \tag{4.17a}$$

$$n(0)\upsilon_{inj}(0)=F^{+}-(-F^{-}R)=F^{+}(1+R) \tag{4.17b}$$

From eq. (4.17) and r_{sat} represents R in the saturation region, we have:

$$I_{D,sat}=WC_{eff}\upsilon_{inj}\left[\frac{1-r_{sat}}{1+r_{sat}}\right](V_G-V_{T,sat}) \tag{4.18}$$

$$B_{sat}=\frac{1-r_{sat}}{1+r_{sat}} \tag{4.19}$$

B_{sat} is the index of the backscattering rate and $0<B_{sat}<1$ and r_{sat} is extracted by eq. (4.4) from [1], which means the reflection probability of the transport carriers.

In real devices, we should consider the S/D series resistance and DIBL effect. It will be explained in latter section.

4.1.2 Temperature Dependent Method to Extract Backscattering Coefficient

In the past research, M. J. Chen reported that drain current (I_D), thermal injection velocity (υ_{inj}), backscattering coefficient (r_c) and threshold voltage (V_T) are temperature dependent parameters [7]. Therefore, we can apply the devices with both linear and saturation operational condition and extract the backscattering coefficient by difference equation [8]. From eq. (4.18), we apply the log operator on it, and then we differentiate the result by temperature (T). We get

$$\begin{aligned}\frac{\partial I_{D,sat}}{\partial T} &= I_{D,sat}\left[\frac{1}{\upsilon_{inj}}\frac{\partial \upsilon_{inj}}{\partial T}+\frac{1+r_{sat}}{1-r_{sat}}\frac{\partial}{\partial T}\left(\frac{1-r_{sat}}{1+r_{sat}}\right)+\frac{1}{V_G-V_{T,sat}}\frac{\partial\left(V_G-V_{T,sat}\right)}{\partial T}\right]\\ &= I_{D,sat}\left[\frac{1}{2T}-\left(\frac{1}{1+r_{sat}}+\frac{1}{1-r_{sat}}\right)\frac{\partial r_{sat}}{\partial T}-\frac{\eta}{V_G-V_{T,sat}}\right]\\ &\triangleq I_{D,sat}\alpha\end{aligned} \quad (4.20)$$

where α and η are defined for simplifying the equation, i.e.,

$$\alpha \triangleq \frac{1}{T}\left[\frac{1}{2}-\frac{4}{2+\lambda/l}\right]-\frac{\eta}{V_G-V_{T,sat}} \quad (4.21)$$

$$\eta \triangleq \frac{\partial\left(V_G-V_{T,sat}\right)}{\partial T} \quad (4.22)$$

and λ is the mean-free-path and l is the critical length.

From eq. (4.20) to (4.22) and the experimental result, we can calculate the following parameters in difference equation.

$$\alpha = \frac{I_{D,sat1}-I_{D,sat2}}{\left(T_1-T_2\right)\times I_{D,sat2}} \quad (4.23)$$

$$\eta = \frac{V_{T,sat1}-V_{T,sat2}}{T_1-T_2} \quad (4.24)$$

The most important parameter is r_c, which comes from

$$\frac{\lambda}{l} = \frac{4}{0.5 - \left[\alpha + \frac{\eta}{V_G - V_{T,sat}}\right] \times T} - 2 \quad (4.25)$$

Thus, r_c can be calculated from eq. (4.4).

In real devices, the threshold voltage is function of drain voltage. So, we should consider the short channel effect such as V_T roll-off and Drain Induced Barrier Lowering (*DIBL*) effect. First, the threshold voltage in linear region is extract by G_m method. Then, the saturation threshold voltage is corrected by

$$V_{T,sat} = V_T\left(V_D\right) = V_{T,lin} - \sigma V_D \quad (4.26)$$

where $V_{T,lin}$ is linear region threshold voltage and σ is the DIBL parameter [15].

However, in modern VLSI devices such as our sample devices are ultra short channel devices, the inversion charge will be underestimated due to unknowing gate to channel capacitance (C_{gc}). In order to estimate the inversion layer charge density of the short channel devices, we use the large area devices such as $10\times10\ \mu m^2$ to extract the C_{gc}, and the C_{gsd} is applied for approximating C_{gc}. Then, we use the difference of the threshold voltage of long and short channel devices to compensate the inversion charge [34]. By the temperature dependent method, the backscattering coefficient can easily be extracted in the bulk-Si, strained-Si, and SOI devices.

4.2 Characteristics of the Backscattering Theory

In the last section, we examined the temperature dependent characteristics of the backscattering parameters. Besides the dependence of temperature, the drain and gate voltage dependence are also be reported. In this section, first, we perform these relations without numerical analysis. Then, the most important characteristic of the backscattering coefficient, which is the relation between effective mobility (μ_{eff}) and drain current (I_D), will be derived.

4.2.1 The Drain and Gate Voltage Dependences

Fig. 4.2 shows the conduction band diagram with different gate and drain bias voltage [2]. M. J. Chen has performed the backscattering coefficient with gate voltage variation and constant drain voltage in numerical simulation [8], see Fig. 4.3. In physical view, the conduction band diagram has also performed the same results due to the shape of the barrier top. That means the backscattering coefficient is corresponding to the shape of the channel barrier. Combining the shape of the channel barrier with the gate and drain voltages, it is simpler than making the numerical analysis.

As in section 4.1.1, we know that the backscattering coefficient (r_c) relates to the condition band edge near the source end of the channel. Now we consider the devices with the same channel length. In the saturation condition, high gate and drain bias, the larger the critical length is, the larger the backscattering coefficient is. When gate and drain voltage decrease, critical length will increase, and finally equals about the effective length in the linear region, see Fig. 4.2(a). In Fig. 4.2(a), when gate voltage changed, the critical length doesn't change drastically. So, in low V_D, r_c is almost unchanged with different V_G. It is the same as the condition that V_G is small with V_D variation; see Fig. 4.2(c). In Fig. 4.2(b), when V_G changed with constant V_D, the critical length does change drastically.

It is the same as the condition that V_G keeps constant with different V_D; see Fig. 4.2(d). Based on the above observations, we summarized that:

1. When V_D is large, r_c is decreasing by the increasing of V_G.
2. When V_D is quite small, r_c is nearly a constant.
3. No matter what the V_G is, r_c is decreasing by the increasing of V_D.

4.2.2 The Mobility versus Drain Current Relation

Assuming that the mobility is proportional to the mean-free-path (λ) and applying the mobility (μ) dependence of the drain current [3],

$$\frac{\partial I_D}{\partial \mu}=\frac{\partial I_D}{\partial \lambda}\frac{\partial \lambda}{\partial \mu} \tag{4.27}$$

We apply the eq. (4.1) and (4.2) to it, and get

$$\frac{1}{I_{D,lin}}\frac{\partial I_{D,lin}}{\partial \mu}=\frac{1}{\mu}\left(\frac{1}{1+\lambda_0/L}\right) \tag{4.28}$$

$$\frac{\Delta I_{D,lin}}{I_{D,lin}}=\frac{\Delta \mu}{\mu}\left(\frac{1}{1+\lambda_0/L}\right) \tag{4.29}$$

Finally, note that in the linear region,

$$\frac{I_{D,lin}}{I_{D,lin(ballistic)}}=B_{lin}=\frac{\lambda_0/L}{1+\lambda_0/L} \tag{4.30}$$

$$\frac{\Delta I_{D,lin}}{I_{D,lin}}=\frac{\Delta \mu}{\mu}\left(1-B_{lin}\right) \tag{4.31}$$

Where $I_{D,lin(ballistic)}$ means the absolute ballistic condition without backscattering transport ($B_{lin}\rightarrow 1$). On the other hand, we derived the eq. (4.3) and (4.4) by the same method,

$$\frac{1}{I_{D,sat}}\frac{\partial I_{D,sat}}{\partial \mu}=\frac{1}{\mu}\left(1-\frac{\lambda}{\lambda+2l}\right) \tag{4.32}$$

$$\frac{I_{D,sat}}{I_{D,sat(ballistic)}}=B_{sat}=\frac{\lambda/2l}{1+\lambda/2l} \tag{4.33}$$

The $I_{D,sat(ballistic)}$ is the absolute ballistic condition without backscattering transport ($B_{sat}\rightarrow 1$). Then, we combine the above two equations and get

$$\frac{\Delta I_{D,sat}}{I_{D,sat}}=\frac{\Delta \mu}{\mu}\left(1-B_{sat}\right) \tag{4.34}$$

Finally, the results shown that scattering theory gives simple expressions that relate the drain current to the near-equilibrium, inversion layer mobility of a corresponding long-channel device and to the ratio of the measured to ballistic current, as eq. (4.31) and (4.34).

$$\frac{\Delta I_D}{I_D}=\frac{\Delta \mu}{\mu}\left(1-B\right) \tag{4.35}$$

The result is valid for both linear and saturation region. And B means the ballistic coefficient.

4.3 Backscattering Theory in Schottky-Barrier MOSFETs

In 2002, J. Guo and Mark S. Lundstrom reported that the backscattering characteristics of SBMOS with different Schottky-barrier height [5]. The results show that the ballistic theory is failed for SBMOS, which is due to most carriers are tunneling through the channel barrier instead of emitting over the barrier. Under this argument, the backscattering theory is suitable for SBMOS just when Schottky-barrier height is negative.

In recent years, some companies demonstrated the better performance of DSI-SBMOS than conventional SBMOS and bulk-Si MOSFETs [25-26]. With dopant segregation implantation (DSI) technique, carriers are easy to tunnel through the thin Schottky barrier in the source end that induced a large drain current. The conduction band edge of the DSI-SBMOS is shown in Fig. 4.4(b), and is compared with conventional MOSFETs; see Fig. 4.4(a). When carriers inject from source to channel, most of them tunnel through the Schottky barrier, which is more than *90%* carriers tunneled the barrier in *ON-state*, and then emit over the channel barrier, as we have mentioned in chapter 3. Under this condition, the channel barrier leads to a backscattering situation for carriers. So, it is important for devices designer to re-examine in the backscattering theory of DSI-SBMOS.

A latest researches show the injection velocity of the DSI-SBMOS [35], but they do not explain the relations between injection velocity and ballistic coefficient. They describe that the injection velocity of SBMOS is larger than conventional MOSFET, where their injection velocity is the carrier average velocity in the channel instead of thermal injection velocity on the source side. In the following sections, we will demonstrate the ballistic coefficient in low field region of the channel barrier with a new observable method and the high field ballistic coefficient in the next chapter.

4.3.1 Effective Ballistic Mobility

Early in 1980s, Michael S. Shur developed the effective ballistic mobility (also called *apparent mobility*) for evaluating the limitation of high electron mobility transistor (*HEMT*) [36]. For HEMTs, in general, are composed of *AlGaAs* and *GaAs* for attaching high performance. In this structure, there is a barrier with the shape of spike between the *AlGaAs/GaAs* heterojunction. For SBMOS, there is a barrier between the S/D to channel due to metal-semiconductor junction. This barrier is like heterojunction. Therefore, we can launch the effective ballistic mobility on SBMOS. In addition, somebody used it for researching mobility degradation effect in very short devices. This target is similar to our experiment.

In MOSFETs, carriers propagate in the channel with a randomly oriented thermal velocity (υ_{th}) for non-degenerate condition or Fermi velocity (υ_F) for degenerate condition. In low electric fields, the current is proportional to the electric field and the electron concentration, just like in the collision-dominated case. We illustrate the drift velocity versus electric field plot in Fig. 4.5(b) [15]. The slope in low field region presents the constant mobility (μ). When carriers accelerate with thermal velocity by the field across the channel, the limitation time is L/υ_{th}. We defined the effective ballistic mobility as the following equation.

$$\mu_{Ballistic} \triangleq \mu_B = \frac{qL}{\pi m^* \upsilon_T} \frac{\Im_{-1/2}(\eta_F)}{\Im_0(\eta_F)} \tag{4.36a}$$

$$\Im_{1/2}(\eta_F) = \int_0^\infty \frac{\eta^{1/2}}{1+\exp(\eta-\eta_F)} d\eta, \quad \eta \triangleq \frac{E-E_C}{k_B T}, \quad \eta_F \triangleq \frac{E_F - E_C}{k_B T} \tag{4.36b}$$

For *non-degenerate* condition, the Fermi integral ($\Im$) is canceled. Then, we get

$$\mu_B = \frac{qL}{\pi m^* \upsilon_T} \tag{4.37}$$

Eq. (4.37) is also called *Shur's expression*. The unidirectional thermal velocity is

$$\upsilon_T = \sqrt{\frac{2k_B T}{\pi m^*}} \tag{4.38}$$

And, the thermal average speed is

$$\upsilon_{th} = \sqrt{\frac{8k_B T}{\pi m^*}} \tag{4.39}$$

Finally, the effective ballistic mobility is expressing as

$$\mu_B = \frac{2qL}{\pi m^* \upsilon_{th}} \tag{4.40}$$

where m^* is the effective mass, q is basic electron charge, k_B is Boltzmann's constant, T is the temperature and L is the effective length of the devices. This mobility is treated as carriers directly transmit through the channel. In quasi-ballistic situation, carriers will produce a lot of collision which results in different scattering such as impurity, phonon and surface roughness scattering. We applied the *Mathiessen's rule* for describing the carriers transport in nanoscale MOSFETs. Thus, the effective mobility is defined as

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_B} + \frac{1}{\mu_0} \tag{4.41}$$

where μ_{eff} is the effective mobility we are measured in MOSFETs in low field region and μ_0 is the effective mobility in very long channel devices which is scattering- dominate without ballistic condition and is also named μ_∞. Usually, we choose the channel length longer than $10\mu m$. However, with channel length scaled down, the effective mobility will decrease drastically. This is due to effective ballistic mobility is decreasing with down-scaling and pulling down the effective mobility. We illustrated the picture with the carriers directly overshoot the channel which contributes ballistic mobility, and other scattering mechanisms present the scattering-dominate mobility, see Fig 4.5(a). Because of easily passing through the channel without collision, the former is very small due to small length (eq. (4.40)) of the device in the nanoscale devices that decrease the mobility. Under this inference, the effective ballistic mobility (μ_B) becomes the target for predicting device's ballistic rate.

4.3.2 The Links between Ballistic Theory, Effective Ballistic Mobility and Drift-Diffusion Model

We have argued the effective ballistic mobility in low field region. In this section, first,

we expect to link the drift-diffusion model with effective ballistic mobility [6].

From eq. (4.30), and the *Einstein's relation*,

$$\mu_0 = \frac{q}{k_B T} D_n \tag{4.42}$$

Where $D_n=\upsilon_T\lambda/2$ is the diffusion coefficient and k_B is Boltzmann's constant. The long channel mobility is

$$\mu_0 = \frac{q\upsilon_T\lambda}{2k_B T} = \frac{q\lambda}{\pi m^* \upsilon_T} \tag{4.43}$$

Combining eq. (4.37) with (4.43), we have

$$\frac{\lambda}{\lambda + L} = \frac{\mu_0}{\mu_0 + \mu_B} \tag{4.44}$$

Under low drain bias, the ballistic current can be expressed in terms of ballistic mobility,

$$I_{ballistic} = WQ_i(0)\mu_B \frac{V_{DS}}{L} \tag{4.45}$$

And, from eq. (4.30),

$$I_{D,lin} = \frac{\lambda}{\lambda + L} I_{ballistic} = \frac{\mu_0 \mu_B}{\mu_0 + \mu_B} WQ_i(0)\frac{V_{DS}}{L} \tag{4.46}$$

Therefore, we treat the effective mobility as

$$\mu_{eff} = \frac{\mu_0 \mu_B}{\mu_0 + \mu_B} \tag{4.47}$$

This equation is the same as eq. (4.41). So, we derived that the effective ballistic mobility is suitable for drift-diffusion model.

Then, recalling the ballistic theory, the eq. (4.30) describes the ballistic coefficient in linear region. Thus, linking the eq. (4.30) and (4.44), the reflection coefficient can be expressed as

$$r_{lin} = \frac{\mu_B}{\mu_B + \mu_0} \tag{4.48}$$

$$B_{lin} = 1 - r_{lin} = \frac{\mu_0}{\mu_0 + \mu_B} \tag{4.49}$$

So, the relations between ballistic theory, effective ballistic mobility and drift-diffusion model are performed.

On the other hand, when the MOSFET operates in the high field, which is related to degeneracy condition, the drain current should add the Fermi integral ($\Im_n(\eta_F)$). This will complicate the extraction method [6]. In order to simplify the extracting process, we focus on the other significant parameter which is velocity component. In the high field region, the significance of saturation velocity is larger than effective mobility, especially short channel devices, which someone called mobility saturation. Thus, effective ballistic mobility is valid only in the low field region. The inferential process will be introduced in the later chapter.

Before our experiment, we have to make sure why we will try to use the effective ballistic mobility to evaluate linear backscattering coefficient. As the barrier variation in Fig. 3.16, the tunneling barrier is the same with different channel length and the channel barrier is the dominant factor of driven current in DSI-SBMOS, further, the measured mobility depends on channel barrier. Hence, the effective ballistic mobility (μ_B) can extract the channel barrier backscattering coefficient. On the other hand, we cannot use temperature dependent method we have introduced in section 4.1.2. This is due to this method is established on thermionic emission of carriers. But in DSI-SBMOS, thermionic emission is not the dominant transport method. Under these inferences, we practice the effective ballistic mobility on DSI-SBMOS in low field region.

4.4 The Experimental Results of Effective Ballistic Mobility

Further, we focus on the causes of extracting the backscattering coefficient by the effective ballistic mobility method. As in Fig. 4.5(b), carrier drift velocity will be saturation when electric field is larger than critical field (ε_c). In modern bulk-Si devices, the saturation velocity is about 1.2×10^7 *cm/s*, which is just thermal injection velocity. In 1979, K. Thornber had reported the relations between drift velocity and saturation velocity in terms of mobility and scattering rate [4]. He concluded that saturation velocity is invariant under scaling of the magnitude of the scattering rates, while alters mobility, while mobility is invariant under

scaling the magnitude of the momentum, which alters saturation velocity. In general, saturation velocity and mobility are independent. Briefly, if Γ is changed, μ is changed in the same time. If m^* is changed, υ_{sat} is changed in the same time. It is called "*Thornber's theory*". Hence, in strain-Si devices, we can investigate in saturation velocity variation but mobility variation for predicting the backscattering rate due to reduced effective mass. In bulk-Si devices, if the scattering factor is changed, to investigate in mobility variation is the route to extract the backscattering rate such as SBMOS.

In these two years, some researchers have investigated the effective ballistic mobility in some different devices such as conventional MOSFETs [38], *FDSOI*, and silicon nanowire transistor (*SNWT*) [11]. The mentioned effective ballistic mobility is so called *apparent mobility*. See Fig. 4.5(b), in low field region ($\varepsilon \ll \varepsilon_c$,or V_D is quite small), the drift velocity is proportional to the electirc field and the mobility is the ratio of the two parameters. Recalling the relations between backscattering coefficient and drain and gate voltage in section 4.2.1, the ballistic coefficient is nearly a constant in low field. This is similar to constant mobility in low field region. This proves that the low field mobility is corresponding to low field ballistic coefficient.

In our experiment, we do not expect any serious hot-carrier effect disturb in our experiment because of low operational drain and gate bias. And the effective mobility is extracted by *split C-V* method [39], and the low field mobility is the intersection of *y-component* in the μ_{eff} versus (V_{GS}-V_T) plot. In the following words, we will demonstrate the experiment which we tried to prove. Besides, the inversion charge density is corrected by the threshold voltage difference [34], see eq. (4.50).

$$Q_i(x_0) = \frac{(Q_{i0} + \Delta Q_i)}{W \times L} \tag{4.50}$$

where $Q_i(x_0)$ is the small area device's inversion charge density at the conduction-band peak at the source side, Q_{i0} is the large area device's inversion charge density corresponding to small area, and ΔQ_i is the charge density difference by ΔV_T.

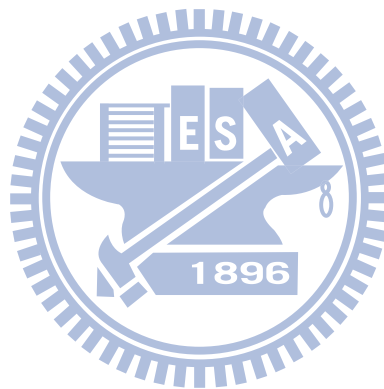
Fig. 3.8(b) shows the source to drain potential profile of DSI-SBMOS in the low-drain-bias region. The source to channel junction produces a spike-like potential barrier that blocks most of carriers, which suppresses the drain current. But, under process strained technology, the SBMOS raised up its performance, which we introduced in the chapter 2. We choose sample B to complete our experiment.

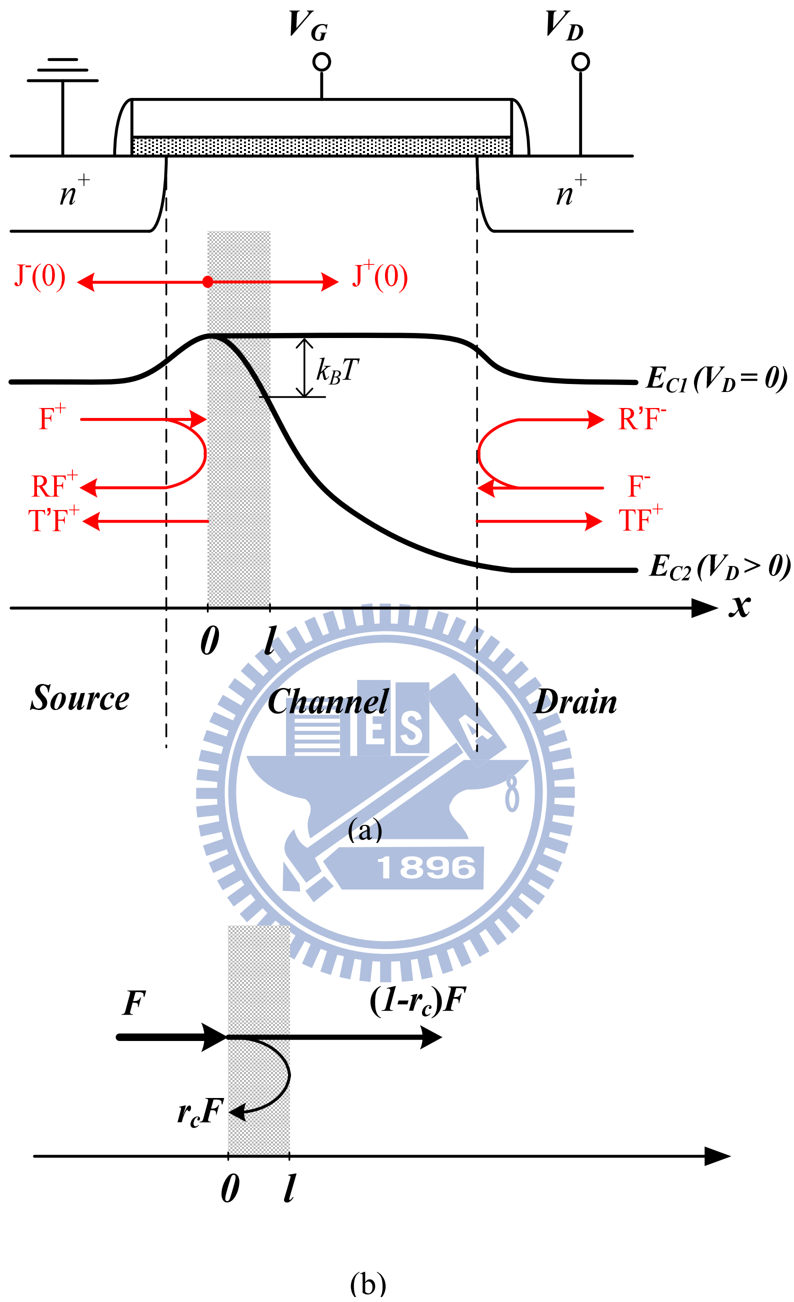
Fig. 4.6 shows the low field mobility of conventional PMOS and SB-PMOS. The effective mobility of DSI SB-PMOS is two times of the conventional MOSFET. In the long channel devices, which are larger than $1\mu m$, their low field mobility does not decrease drastically with the channel length. But the short channel devices, their low field mobility drops fast with the decreasing of the channel. In addition, the conventional NMOS and SB-NMOS show similar results as shown in Fig. 4.7. Then, we applied the effective ballistic mobility theory for extracting the linear ballistic coefficient (B_{lin}). The calculated linear ballistic coefficient is shown in Fig. 4.8 and the DSI SBMOS has poor linear ballistic coefficient. In linear region, the drain current is contributed from thermoinic emission, see Fig. 3.8. When the carriers thermionic from source to drain, they bomb into three different barriers and each of barriers provided transmission and reflection process that decreasing the carrier transfer probability from source to drain. Therefore, the reflection coefficient in the low field region of SBMOS is larger than conventional MOSFETs. Fig. 3.9 is the calculated thermal injection velocity in the linear region of SBMOS and conventional MOSFET. The Schottky-barrier MOSFET performed the better limitations of injection velocity which is contributed by CESL.

4.5 Summary

In this chapter, we have performed the basic ballistic transport theory and the relations between effective ballistic mobility, and the ballistic theory. The effective ballistic mobility has presented the limitations of channel downscaling successfully in the low field region. In

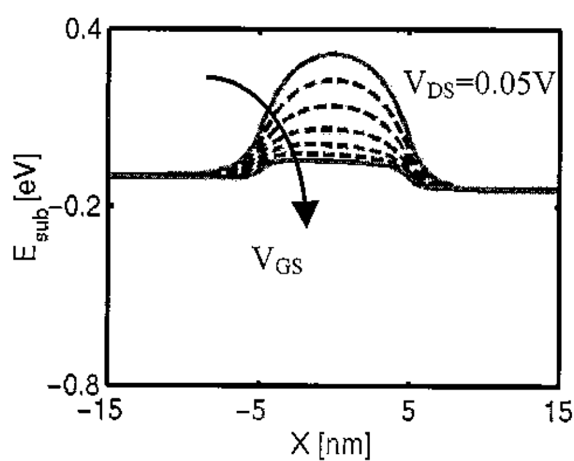
low field region, the SBMOS performed the poor ballistic characteristic due to its carrier transport mechanism. On the other hand, the high field ballistic coefficient will be discussed by carrier average velocity in the next chapter.



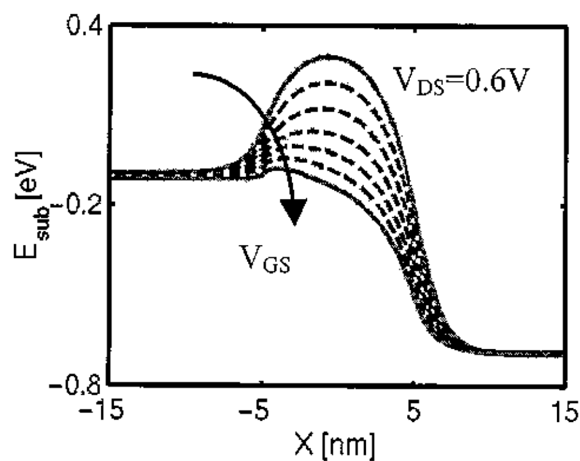


(b)

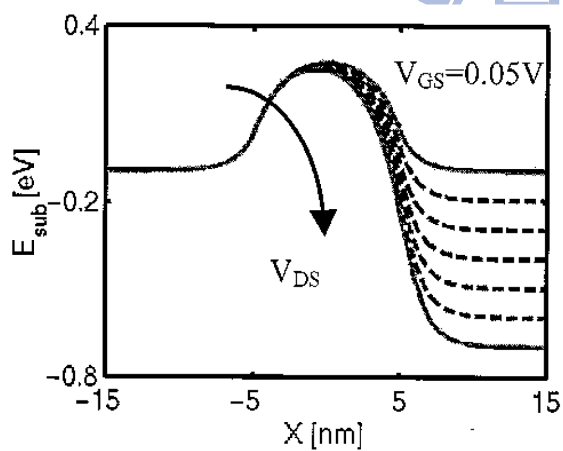
Fig. 4.1 (a) Band diagram of the conventional NMOS with the scattering matrix method for extracting the ballistic theory. (b) The simplified transmission and reflection current flow.



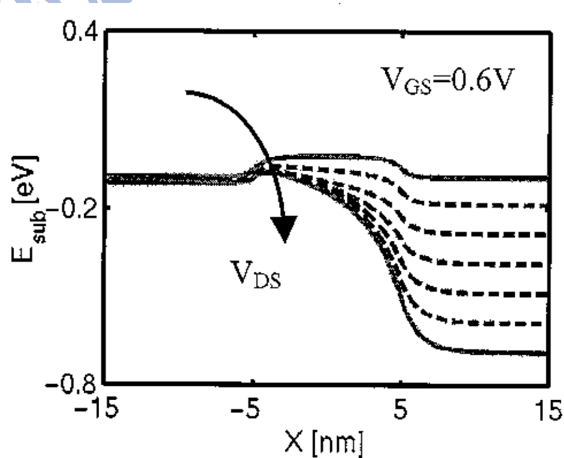
(a)



(b)



(c)



(d)

Fig. 4.2 The conduction band edge versus position with several bias condition (a) $V_D=50mV, V_G=0\sim0.6V$ (b) $V_D=0.6V, V_G=0\sim0.6V$ (c) $V_G=50mV, V_D=0\sim0.6V$ (d) $V_G=0.6V, V_D=0\sim0.6V$ [2].

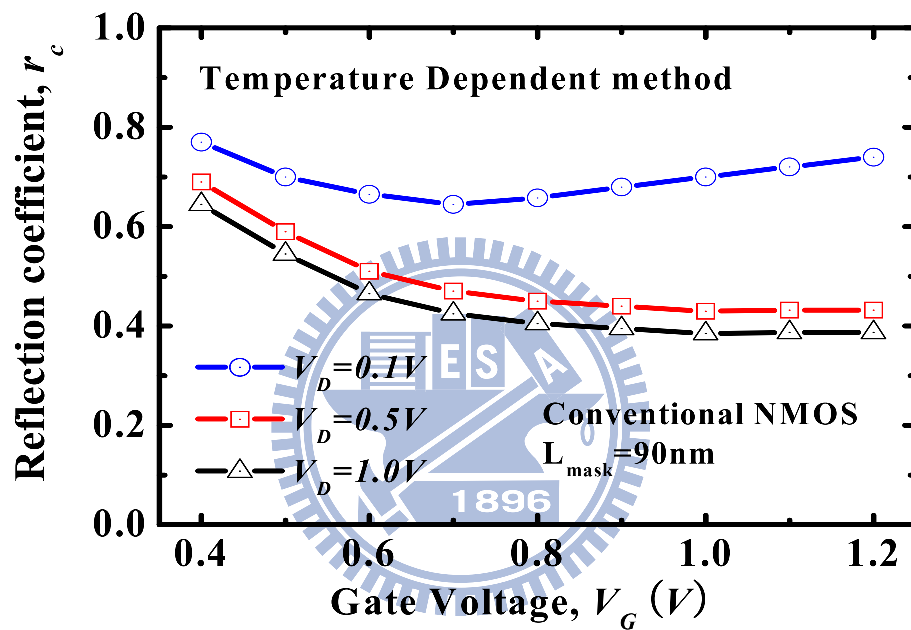
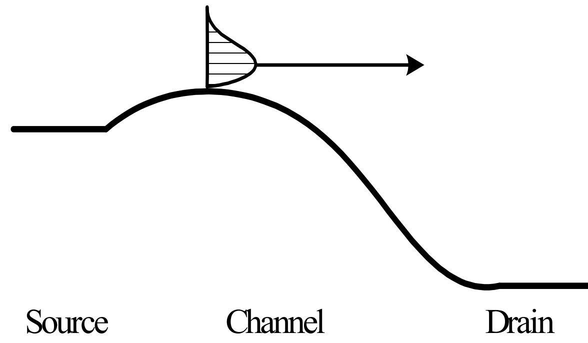
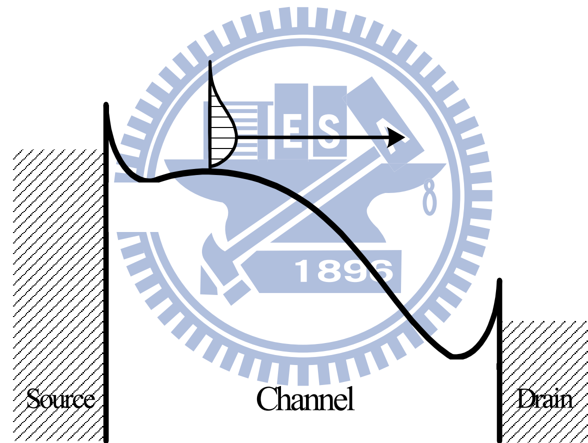


Fig. 4.3 The reflection coefficient versus gate voltage plot with different drain voltage. Circle is at $V_D=0.1V$, square is at $V_D=0.5V$ and triangle is at $V_D=1V$.

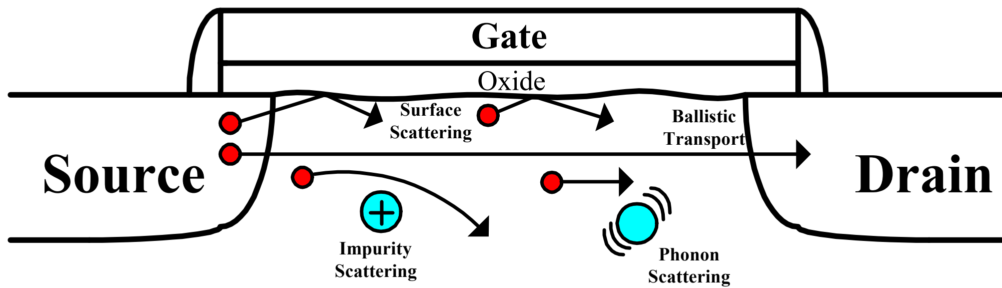


(a)

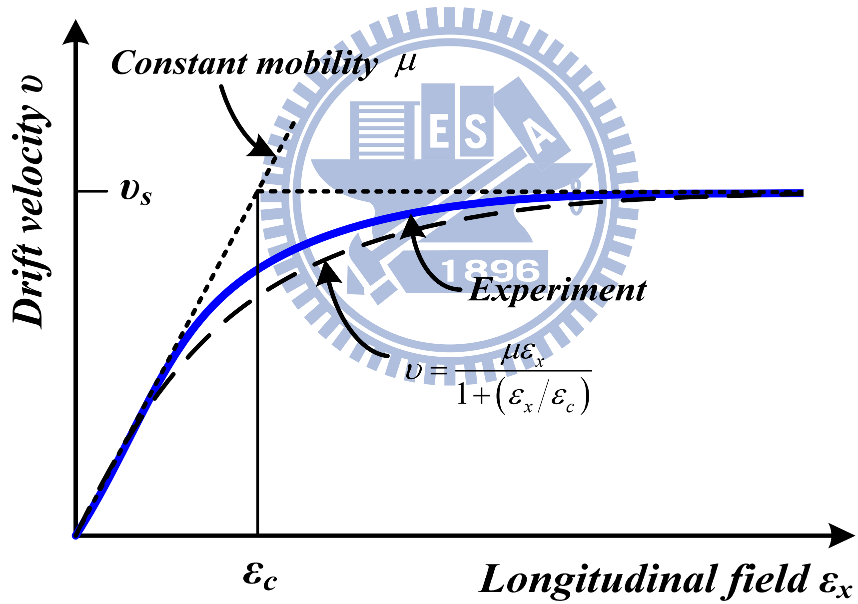


(b)

Fig. 4.4 The band diagram for (a) DSI-SBMOS (b) conventional MOSFETs with the same channel length and potential. υ_{inj} means the thermal injection velocity.

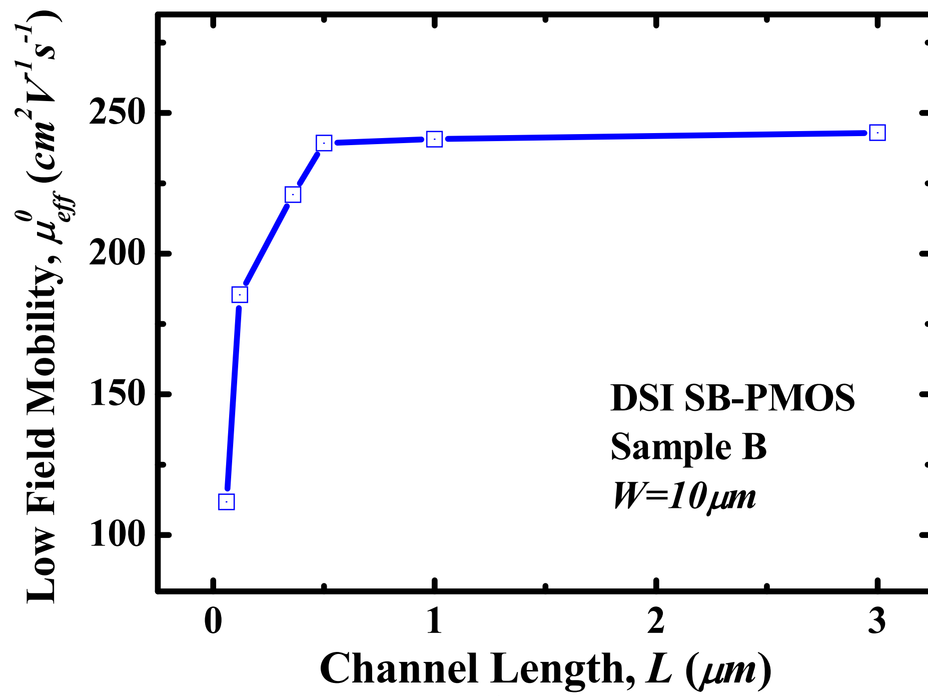


(a)

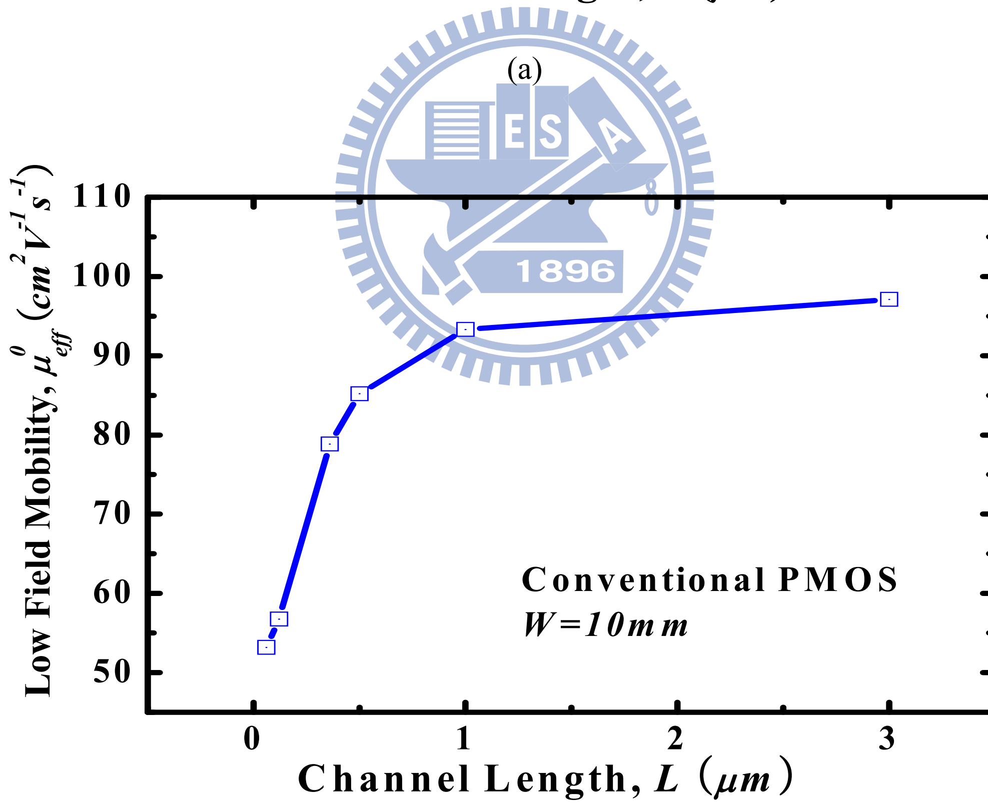


(b)

Fig. 4.5 (a) The scattering components in the channel. (b) Drift velocity versus electric field plot. Solid line is experiment curve, dash line is theoretical curve. υ_s is saturation velocity, and ε_s is critical field.

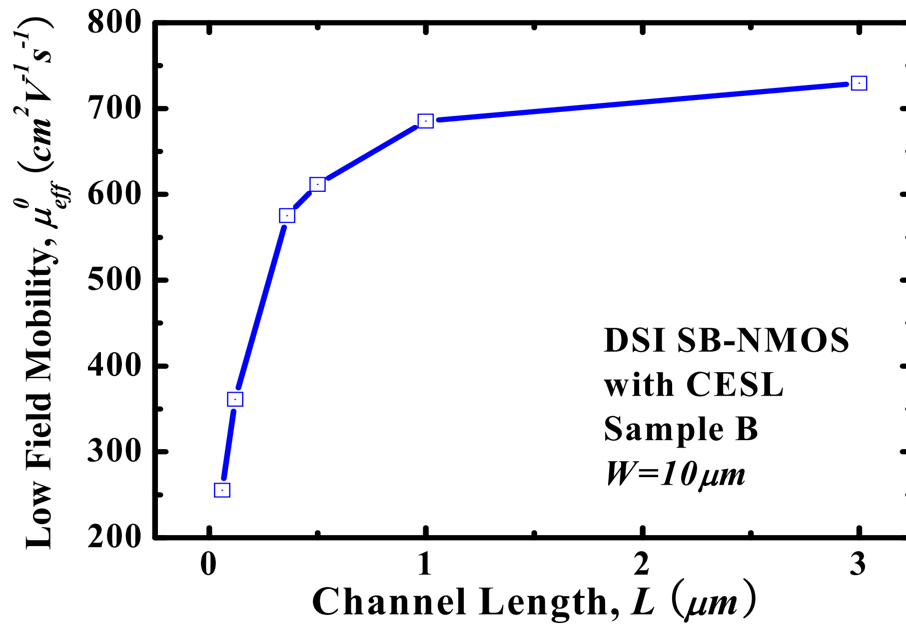


(a)

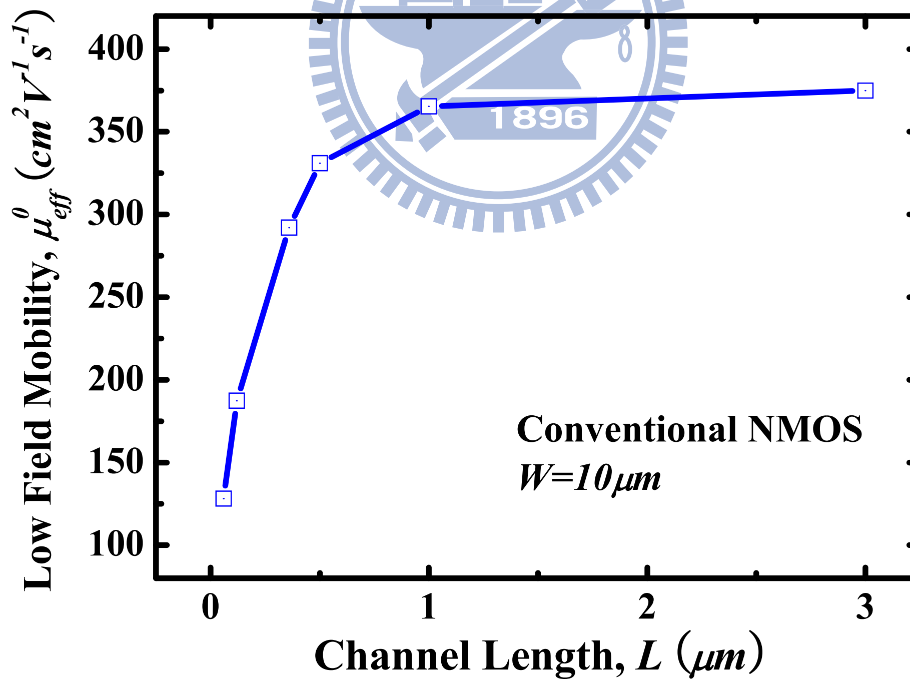


(b)

Fig. 4.6 The low field mobility versus channel length plot (a) for DSI SB-PMOS with CESL (b) Conventional pMOSFET.

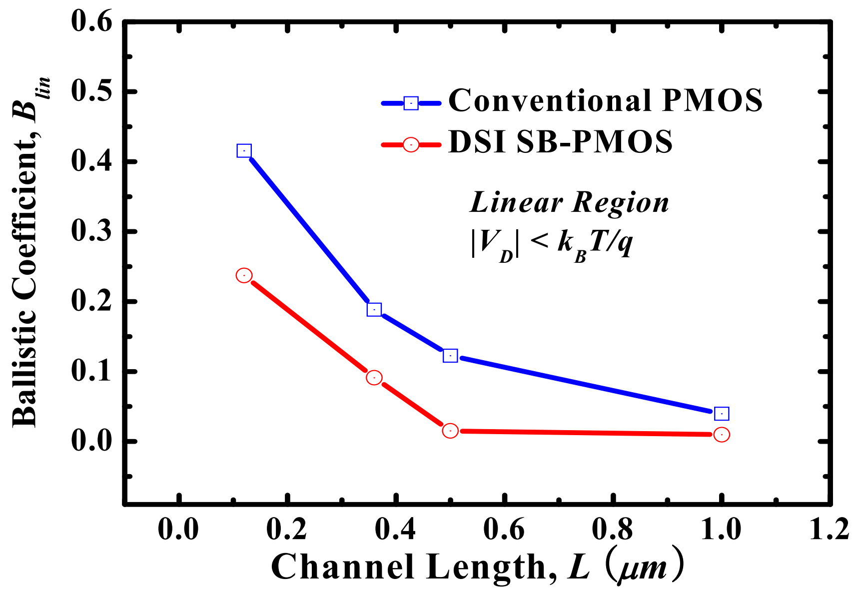


(a)

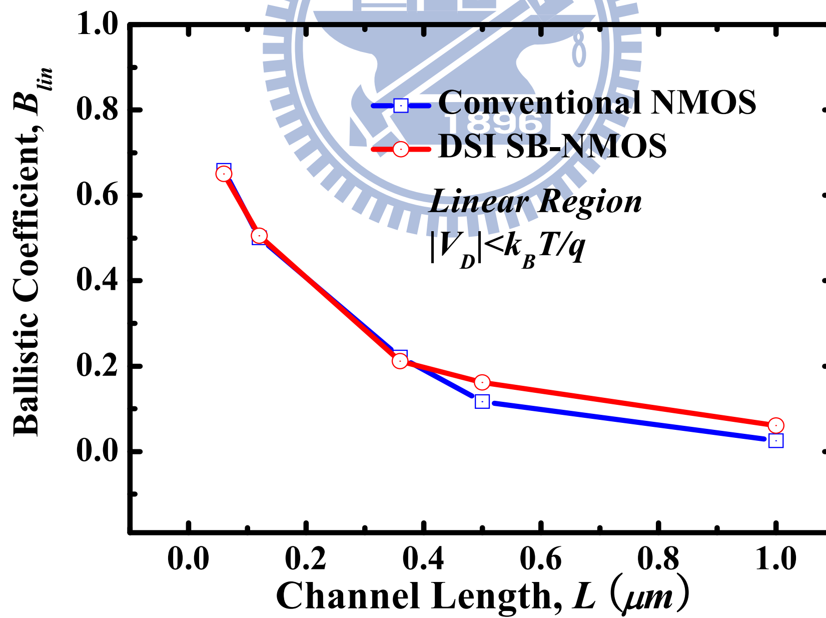


(b)

Fig. 4.7 The low field mobility versus channel length plot (a) for DSI SB-NMOS with CESL (b) Conventional nMOSFET.

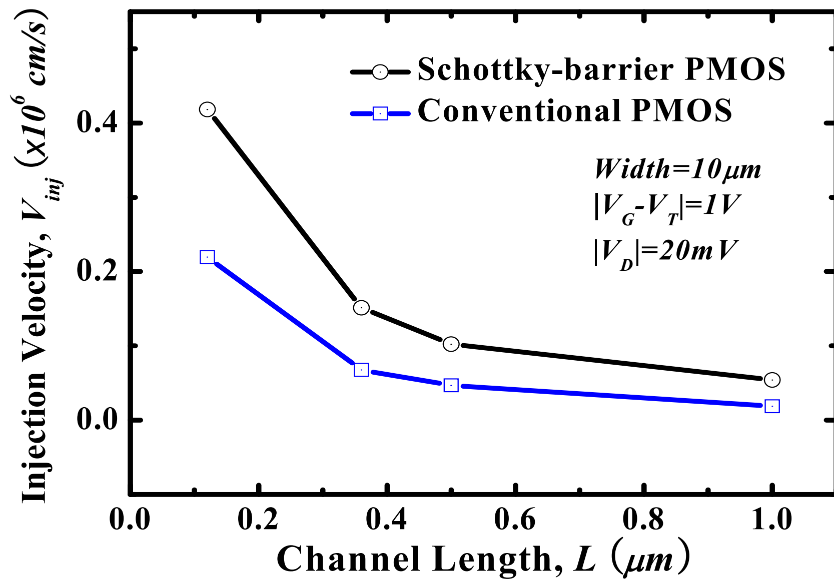


(a)

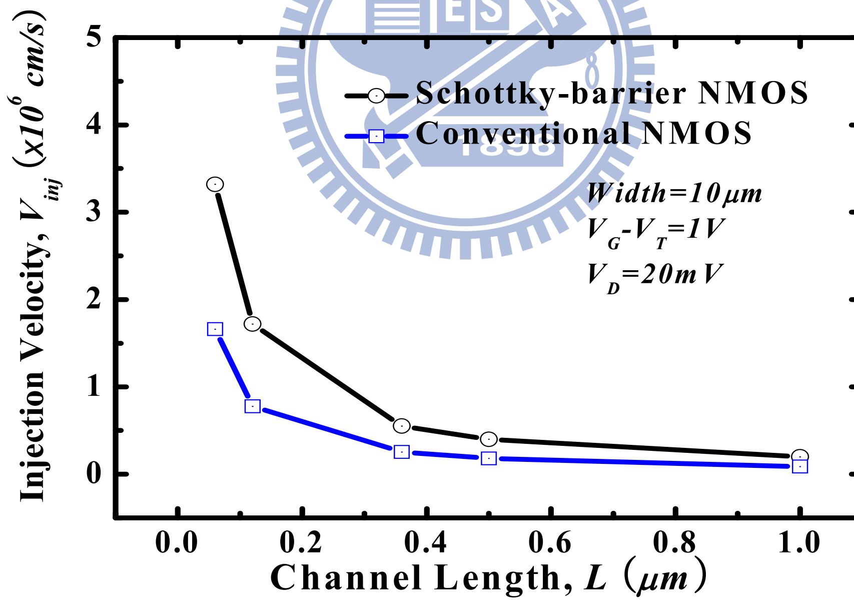


(b)

Fig. 4.8 The linear ballistic coefficient (B_{lin}) versus channel length curve (a) for DSI SB-PMOS with CESL (b) DSI SB-NMOS with CESL compared with conventional MOSFETs.



(a)



(b)

Fig. 4.9 The thermal injection velocity in linear region of (a) SB-PMOS versus PMOS (b) SB-NMOS versus NMMOS.

Chapter 5
Backscattering Coefficient in the Velocity Saturation Region

In the last chapter, we discussed the carrier ballistic transport in linear region by effective ballistic theory. But in high field region, the mobility is invalid due to velocity saturation. Hence, we should consider the saturation velocity from thermal injection velocity in degenerate situation. In this chapter, first, we focus on the theoretical characteristic of thermal injection velocity. Then, the saturation ballistic coefficient of the Schottky-barrier is characterized. Finally, we make a conclusion of our study.

5.1 Thermal Injection Velocity

The backscattering theory we derived in the last chapter did not consider the carrier degeneracy cases. When gate voltage is larger than threshold voltage, the MOSFET is in the strong inversion region that is treated as *carrier degeneracy*. From Fig. 5.1(a) [2], before threshold voltage, the inversion carrier density is lower than $10^{12}cm^{-2}$, the theoretical thermal injection velocity is about $1.2\times10^{7}cm/s$. When inversion carrier density is larger than $10^{13}cm^{-2}$, the thermal injection velocity nearly equals to Fermi velocity [2]. The inversion carrier density is described as eq. (5.1).

$$n_s = \frac{Q_{inv}}{q} \tag{5.1}$$

It means the thermal injection velocity is function of carrier density, and is also function of gate and drain voltage. Hence, the thermal injection velocity is function of Fermi energy and the quantized energy inside the potential well [33]. The thermal injection velocity is given by eq. (5.2).

$$\upsilon_{inj} = \tilde{\upsilon}_T = \sqrt{\frac{2k_B T}{\pi m^*}}\frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)} = \upsilon_{T0}\frac{\Im_{1/2}\left((E_F - E_n)/k_B T\right)}{\ln\left\{1+\exp\left[(E_F - E_n)/k_B T\right]\right\}} \tag{5.2}$$

The υ_{T0} is the non-degeneracy thermal velocity and unidirectional thermal velocity.

$$\upsilon_{T0} = \sqrt{\frac{2k_B T}{\pi m^*}} \tag{5.3}$$

where $\Im$ is the Fermi-Dirac integral, k_B is the Boltzmann's constant, m^* is the effective mass. When the channel is at non-degeneracy condition, the Fermal integral is reduced.

$$\upsilon_{inj} = \upsilon_{T0} = \sqrt{\frac{2k_B T}{\pi m^*}} \tag{5.4}$$

On the other hand, the channel is strong inversion which the inversion charge is high, the eq. (5.2) is simplified to

$$\upsilon_{inj} = \frac{8\hbar}{3m^*}\sqrt{\frac{|Q_n|}{2\pi q}} = \frac{8\hbar}{3m^*}\sqrt{\frac{C_{ox}\left(V_G - V_T\right)}{2\pi q}} \tag{5.5}$$

and is function of gate voltage. The drain current for arbitrary level of carrier degeneracy can be described as eq. (5.6) [40].

$$I_D = WQ_{inv}\left(\frac{1-r}{1+r}\right)\left[\upsilon_{T0}\frac{\Im_{1/2}\left(\eta_F\right)}{\Im_0\left(\eta_F\right)}\right]\left\{\left[1-\frac{\Im_{1/2}\left(\eta_F - U_D\right)}{\Im_{1/2}\left(\eta_F\right)}\right]\Big/\left[1+\left(\frac{1-r}{1+r}\right)\frac{\Im_0\left(\eta_F - U_D\right)}{\Im_0\left(\eta_F\right)}\right]\right\}$$

$$U_D = \frac{qV_D}{k_B T} \tag{5.6}$$

where W is the channel width, r is backscattering coefficient and Q_{inv} is the inversion charge density which is function of gate voltage and Fermi level.

$$Q_{inv} = qn_s = C_{eff}\left(V_G - V_T\right) = \frac{4\pi q m^*\left(E_F - E_n\right)}{h^2} \tag{5.7}$$

where n_s is the first subband carrier density, C_{eff} is the effective oxide capacitance. Besides, in the maximum of the barrier potential, the inversion charge is independent to drain voltage, see Fig. 5.1(b) [41]. Thus, we can use eq. (5.7) to approximate the inversion charge in the barrier top of the channel.

Now, we consider the carrier degeneracy condition. The $V_D \gg k_B T/q$ is the operational condition. The drain current can be reduced as eq. (5.8).

$$I_D = WQ_{inv}\left(\frac{1-r_{sat}}{1+r_{sat}}\right)\left[\upsilon_{T0}\frac{\Im_{1/2}\left(\eta_F\right)}{\Im_0\left(\eta_F\right)}\right] = WQ_{inv}B_{sat}\left[\upsilon_{T0}\frac{\Im_{1/2}\left(\eta_F\right)}{\Im_0\left(\eta_F\right)}\right] \tag{5.8}$$

In this situation, the backscattering theory is rewritten as

$$\lambda = \frac{\sqrt{2m^{*}\pi k_B T}}{q}\mu\frac{\left[\Im_0(\eta_F)\right]^2}{\Im_{-1}(\eta_F)\Im_{1/2}(\eta_F)} \tag{5.9a}$$

$$l = \beta\frac{k_B T}{q\varepsilon(0)} \tag{5.9b}$$

$$r_{sat} = \frac{l}{l+\lambda} = \left(1+\frac{\varepsilon(0)\mu}{\beta}\sqrt{\frac{2m^{*}\pi}{k_B T}}\frac{\left[\Im_0(\eta_F)\right]^2}{\Im_{-1}(\eta_F)\Im_{1/2}(\eta_F)}\right)^{-1} \tag{5.9c}$$

where β is numerical factor and slightly larger than one. By these equations, we can know that the ballistic coefficient is function of Fermi level which is function of gate voltage as we have mentioned in section 4.2.1.

Both in non-degeneracy or degeneracy condition, the thermal injection velocity are the limitations of carrier transport velocity in the channel. In the low field region, the limitation of carrier velocity equals to unidirectional thermal velocity. In the high field region, the thermal injection velocity is larger than thermal velocity. By the effective ballistic mobility method, we can know the thermal velocity. Combining with eq. (5.5), the thermal injection velocity in the high field region can be extracted.

5.2 Carrier Average Velocity in the Saturation Region

When the devices operate in the *ON-state*, the carrier average velocity is extracting by eq. (5.10) and (5.11) [2].

$$I_D = WQ_i(0)\langle \upsilon(0)\rangle \approx WC_{eff}(V_{GS}-V_T)\langle \upsilon(0)\rangle \tag{5.10}$$

$$Q_i(0) = qn_s(0) \approx C_{eff}(V_{GS}-V_T) \tag{5.11}$$

where $\langle \upsilon(0) \rangle$ is the average velocity of carriers at the beginning of the channel, which some people marked as υ_{eff}, and $Q_i(0)$ is the carrier density of the maximum of the channel potential. However, the maximum value of $\langle \upsilon(0) \rangle$ is approximately the thermal injection velocity υ_{inj} as the eq. (5.2). However, when the devices are under quasi-ballistic region, this average velocity

at the beginning of the channel can be related to the channel backscattering coefficient r_c as the eq. (5.12) [1].

$$\langle \upsilon(0) \rangle \approx \left(\frac{1-r_c}{1+r_c} \right) \tilde{\upsilon}_T = \left(\frac{1-r_c}{1+r_c} \right) \upsilon_{inj} \tag{5.12}$$

The inversion charge density at the maximum of channel potential is one of the other parameter on which we have to focus, see eq. (5.7). In order to determine the carrier average velocity, first, we differentiate the drain current function of eq. (5.10) by gate voltage (V_G).

$$\begin{aligned} \frac{\partial I_D}{\partial V_G} &= W \frac{\partial Q_i(0)}{\partial V_G} \langle \upsilon(0) \rangle + W Q_i(0) \frac{\partial \langle \upsilon(0) \rangle}{\partial V_G} \\ &= W C_{eff} \langle \upsilon(0) \rangle + W Q_i(0) \frac{\partial \langle \upsilon(0) \rangle}{\partial V_G} \end{aligned} \tag{5.13}$$

Note that the velocity is saturation which means the $\langle \upsilon(0) \rangle$ doesn't change with the gate voltage. So, we can ignore the second term of eq. (5.13). Then, we rewrite it in terms of υ_{sat} as

$$\frac{\partial I_D}{\partial V_G} = g_m = W C_{eff} \upsilon_{sat} \tag{5.14}$$

Hence, the υ_{sat} can be extract. Combining this equation with eq. (5.12), the ballistic coefficient can be determined.

$$B_{sat} = \frac{\upsilon_{sat}}{\tilde{\upsilon}_T} = \frac{\upsilon_{sat}}{\upsilon_{inj}} = \frac{1-r_c}{1+r_c} \tag{5.15}$$

which is the equation of ballistic theory and is also called *index of ballisticity*. On the other hand, by [1], carrier average velocity can be marked as eq. (5.16).

$$\langle \upsilon(0) \rangle = \upsilon_{eff} = \left[\frac{1}{\tilde{\upsilon}_T} + \frac{1}{\mu_n \varepsilon(0^+)} \right]^{-1} \tag{5.16}$$

Where μ_n is the effective mobility and $\varepsilon(0^+)$ is the electric field at the maximum potential in the channel which is function of both V_{GS} and V_{DS} as in eq. (4.62).

$$\varepsilon\left(0^+, V_{GS}, V_{DS} = V_{DD}\right) \cong \varepsilon\left(0^+, V_{GS}, V_{DS} = V_{DS,sat}\right) \tag{5.17}$$

In order to extract $\varepsilon(0^+)$, we referred to W. S. Lau who has explained this important parameter in detail [42]. Here we cited it simply in the following words.

$$\varepsilon\left(0^+\right) = \frac{\zeta\left(V_{GS} - V_{T,sat}\right)}{L_{eff}} = \frac{\upsilon_{sat}}{\mu_{eff}} \tag{5.18}$$

Where υ_{sat} is the effective velocity at V_D=V_{DD} with μ_{eff} is the corresponding value, $V_{T,sat}$ is the threshold voltage at V_D=V_{DD} that is extract by eq. (4.26), L_{eff} is the effective channel length, and ζ is the *correction factor* which is smaller than one. The results here are a half of which in [43].

Besides, the ballistic coefficient is express as eq. (5.15), the upper term is decreasing with increasing temperature but the lower term is opposite. This means the ballistic coefficient is decreasing with increasing temperature. Further, in eq. (5.16), the dominant term is the effective mobility that produces the inverse proportional relation of the temperature.

5.3 The Experimental Results of the Velocity Components

Fig. 5.2 shows the potential profiles of source to drain regime. Compared with the conventional MOSFET, Fig. 5.2(a), SBMOS has lower reflection coefficient due to its potential profile. Most of carriers tunnel through the barrier and they do not see any raised potential barrier that leads to small reflection coefficient. Some carriers thermionic above the barrier produced main reflection coefficient. But the thermionic carriers are less than tunneling ones. Under this condition, the reflection coefficient is smaller than conventional situation. In order to evidence these suppositions, we analyzed the velocity components to prove them. Fig. 5.3 shows the carrier average velocity of DSI SB-PMOS and conventional pMOSFET with different channel length, which are calculated by eq. (5.14). Both of their channel lengthes are from *10μm* to *0.06μm* and $|V_D|$ is *1V*. The effective velocity is saturate when the gate bias is larger than *0.8V*. In this region, the eq. (5.13) is more accurate than in the lower gate bias. Fig. 5.4 shows the results of NMOS. The effective velocity of minimum channel length is shown in Fig. 5.5. The saturation effective velocity ($\upsilon_{eff,sat}$) of SB-PMOS is three times larger than conventional PMOS, and SB-NMOS is two times larger than NMOS. The effective saturation velocity versus channel length plot is illustrated in Fig.5.6. All of the devices with different channel length of SBMOS have larger saturation velocity than doped S/D MOSFETs. As the

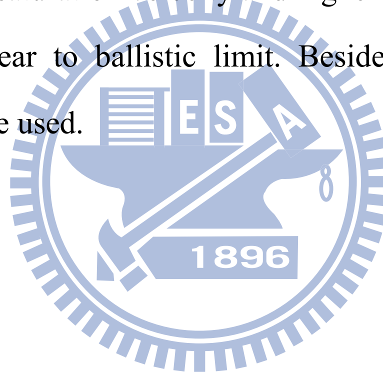
channel length down-scaling, the effective saturation velocity of SBMOS got more times than conventional MOSFETs. Fig. 5.7 shows the effective velocity with two different temperatures. When the temperature increases, the effective velocity decreases. By the eq. (5.14), the thermal velocity increases when the temperature increases. So, the saturation ballistic velocity (B_{sat}) decreases when the temperature increases. Fig. 5.8 shows the inversion charge density of the DSI-SBMOS, the density is so high that the channel is under degenerate condition. From eq. (5.18), we can carry out the electric field of the channel potential. However, the DSI SBMOS and conventional MOSFET have the same channel barrier, see Fig. 5.9, that we can evidence the potential profile in the Fig. 4.4. In order to calculate the saturation ballistic coefficient, we use the uni-direction thermal velocity in the linear region and combine with eq. (5.5). The saturation ballistic coefficient is illustrated in the Fig. 5.10. The results show that the DSI SB-MOSFETs have larger saturation ballistic coefficient than in conventional MOSFETs. Fig. 5.11 shows the drain current enhancement ratio of uniaxial tensile cap strained MOSFET versus conventional MOSFET [10]. We can know that the strained-Si structure enhanced the thermal injection velocity drastically but enhanced the backscattering coefficient lightly.

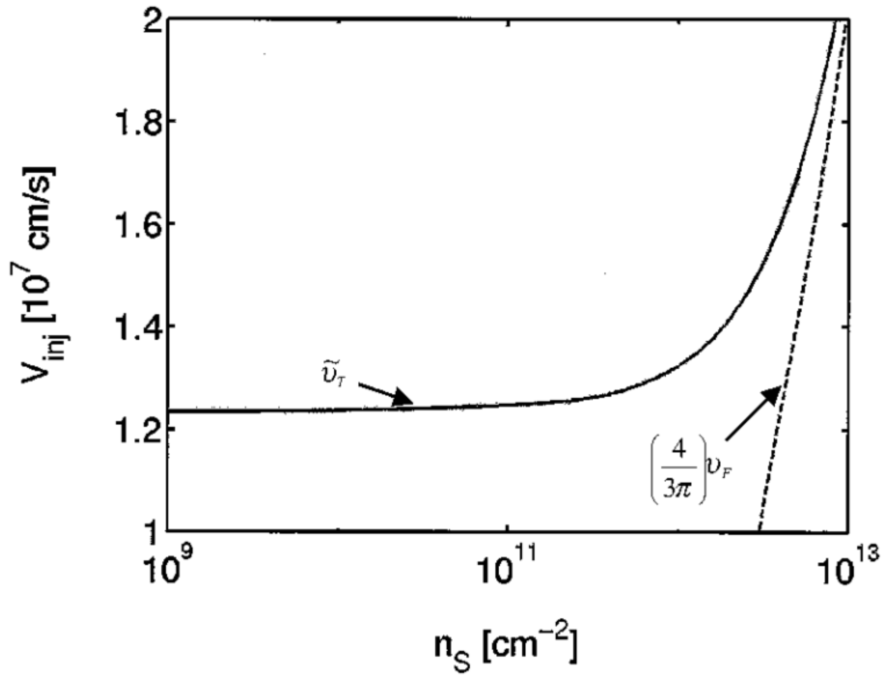
In the saturation region, we have performed the SBMOS with better ballistic characteristic than doped S/D MOSFETs. By Schottky barrier, the carriers get less backscattering in the channel. Besides, the contact etch stop layer (CESL) provided the lower effective mass that produced larger injection thermal velocity than conventional MOSFETs. By these two effects, the effective saturation velocity of SBMOS is much larger than conventional MOSFET. Compared with the ballistic theory and mobility, the lower backscattering coefficient leads to small average collision time ($<\tau>$). Besides, the process strained-Si technology reduces the effective mass that leads to larger injection thermal velocity. However, the effective mobility is proportional to $<\tau>$ and reversely proportional to m^*. By larger $<\tau>$ and small m^*, the effective mobility can be increased drastically. In order to attach higher performance of VLSI devices, besides process strain-Si technique, metal source/drain

can also makes the devices touch the ballistic limit fast.

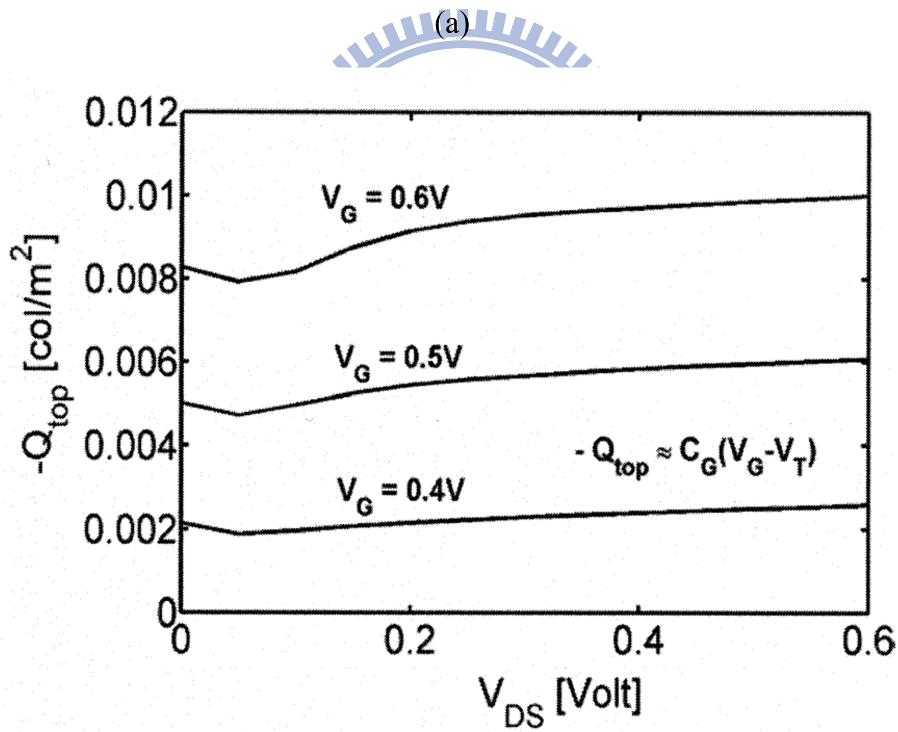
5.4 Summary

In chapters 4 and 5, we have performed the linear ballistic coefficient by effective ballistic mobility theory and the saturation ballistic coefficient by velocity components. The results show that the poor B_{lin} and better B_{sat} in DSI-SBMOS with CESL than in doped S/D MOSFETs. Because of multi-barrier structure in linear region, B_{lin} is lower. And because of the thin Schottky barrier in high electric field, B_{sat} is higher. The SBMOS provided small collision probability that enhanced ballistic coefficient and CESL provided small effective mass that enhanced the injection thermal velocity. Combining these two effects, DSI-SBMOS with CESL got larger effective saturation velocity and higher effective mobility so that we can get the higher performance near to ballistic limit. Besides, in quasi-ballistic region, the drift-diffusion theory can still be used.



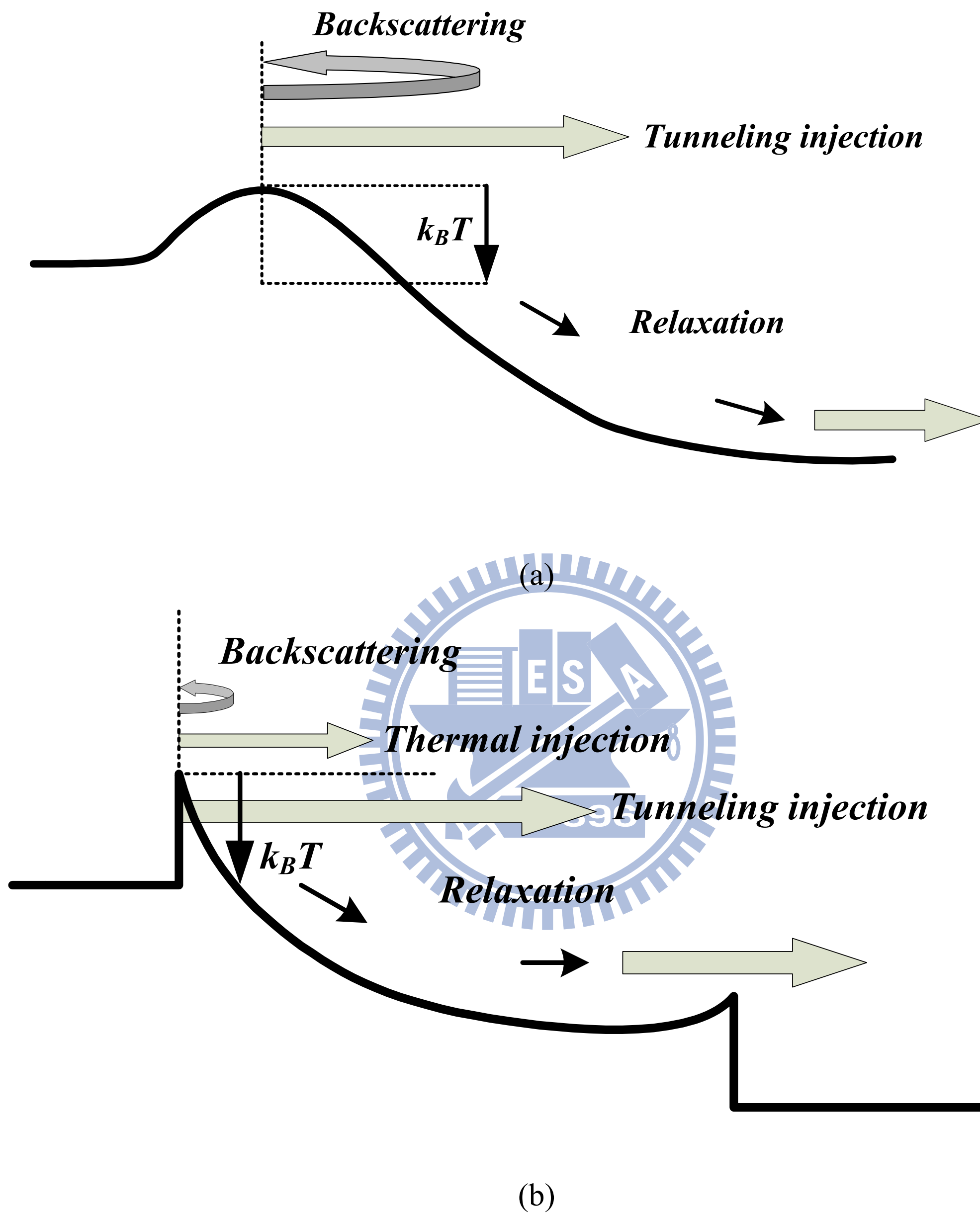


(a)



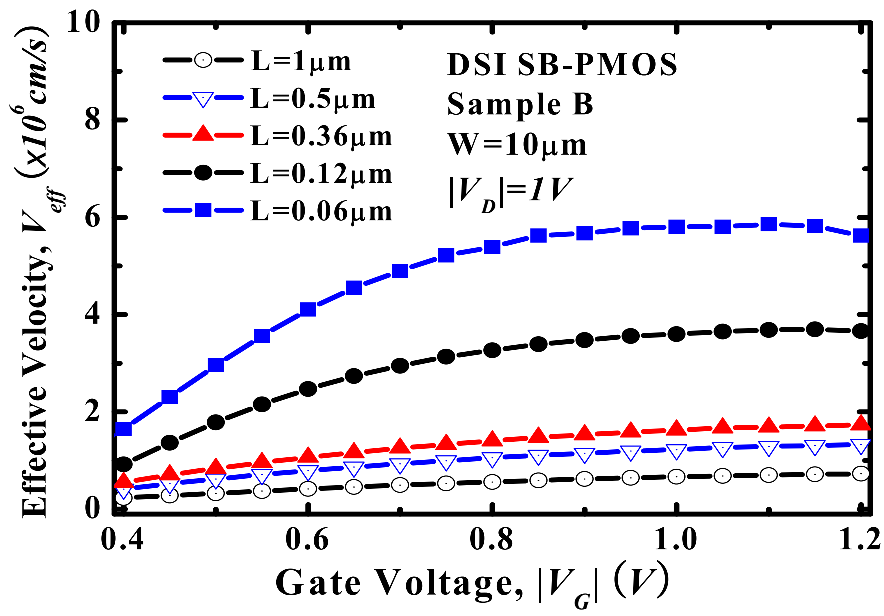
(b)

Fig. 5.1 (a) Equilibrium thermal injection velocity versus inversion layer density n_s and also shown the Fermi velocity [2]. (b) Electron charge $Q_i(0)$ at the top of the barrier versus V_{DS} [41].

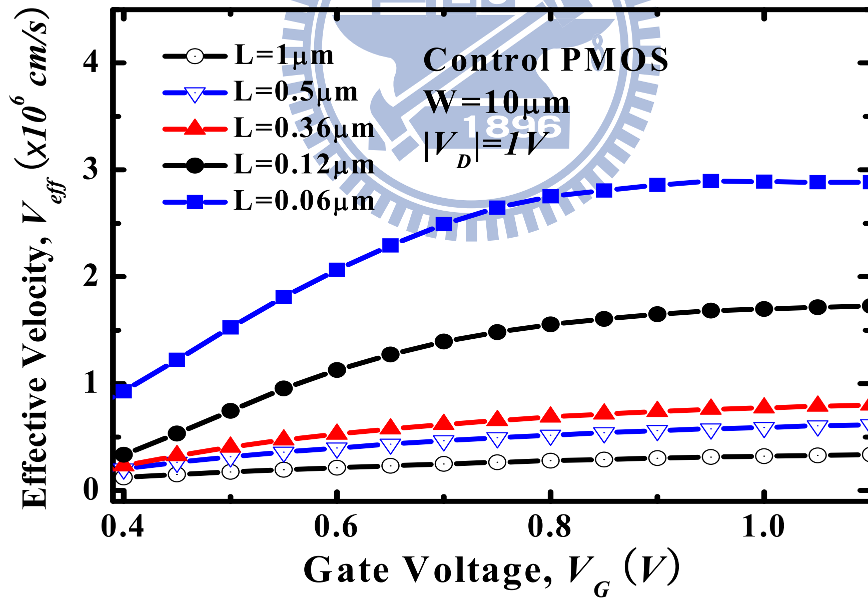


(b)

Fig. 5.2 The potential profiles from source toward drain (a) Conventional MOSFETs with doped S/D (b) Schottky-barrier MOSFETs.

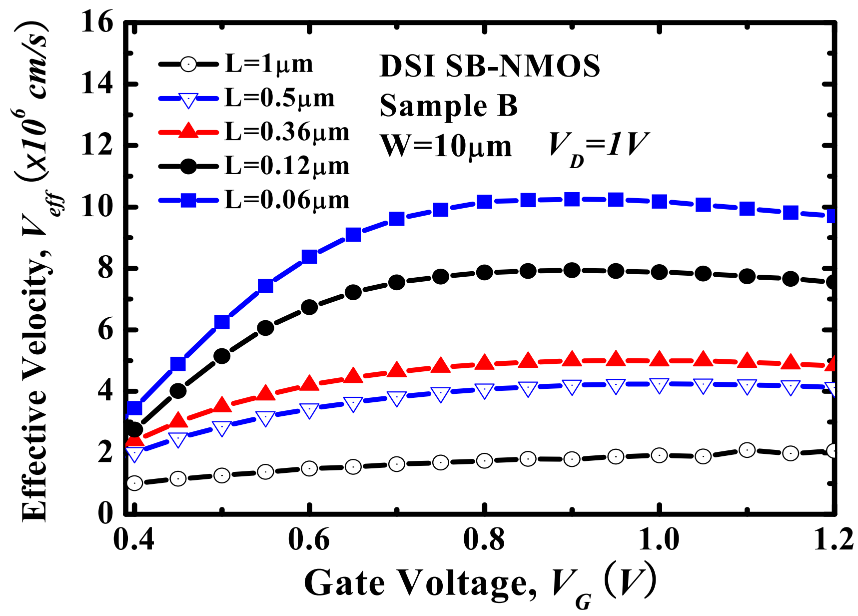


(a)

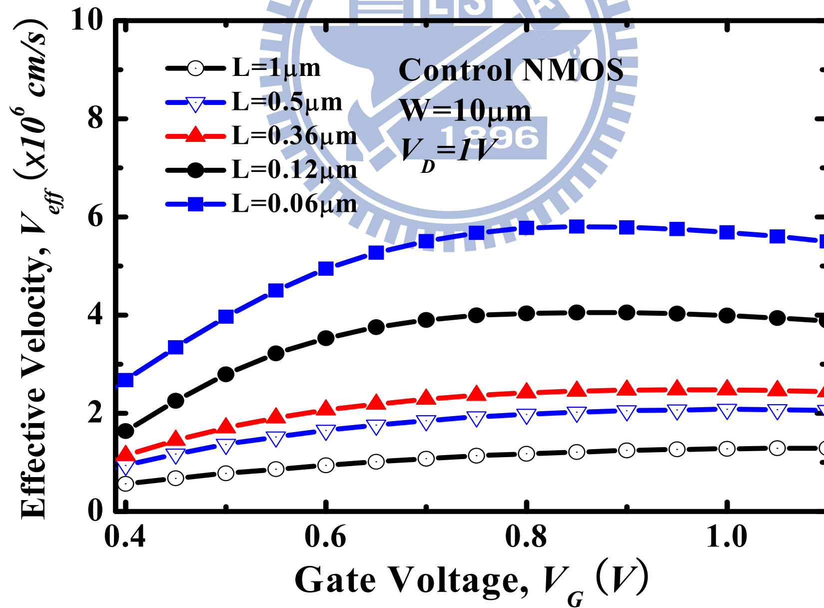


(b)

Fig. 5.3 The carrier average velocity (effective velocity) of (a) Schottky-barrier pMOSFETs. (b) Conventional pMOSFETs with doped S/D.

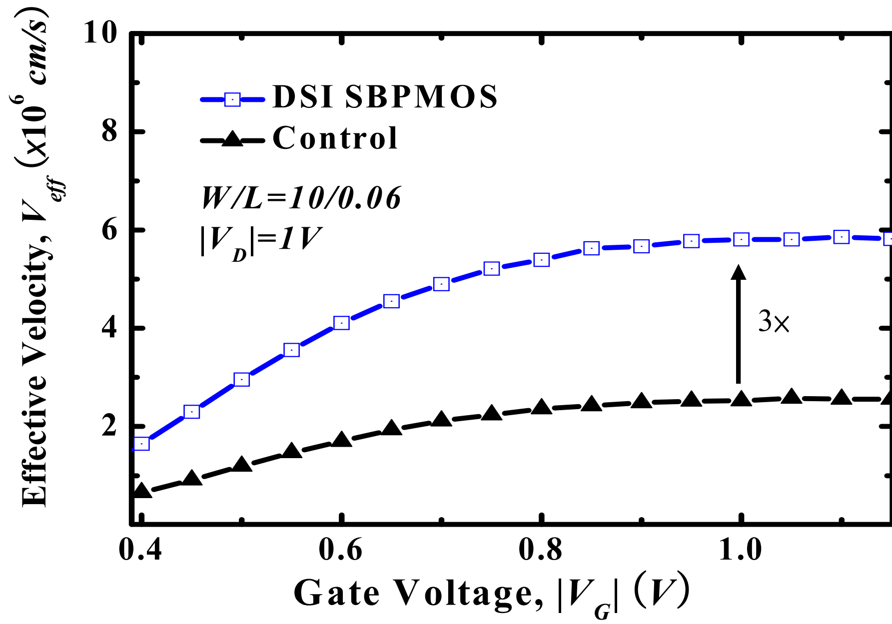


(a)

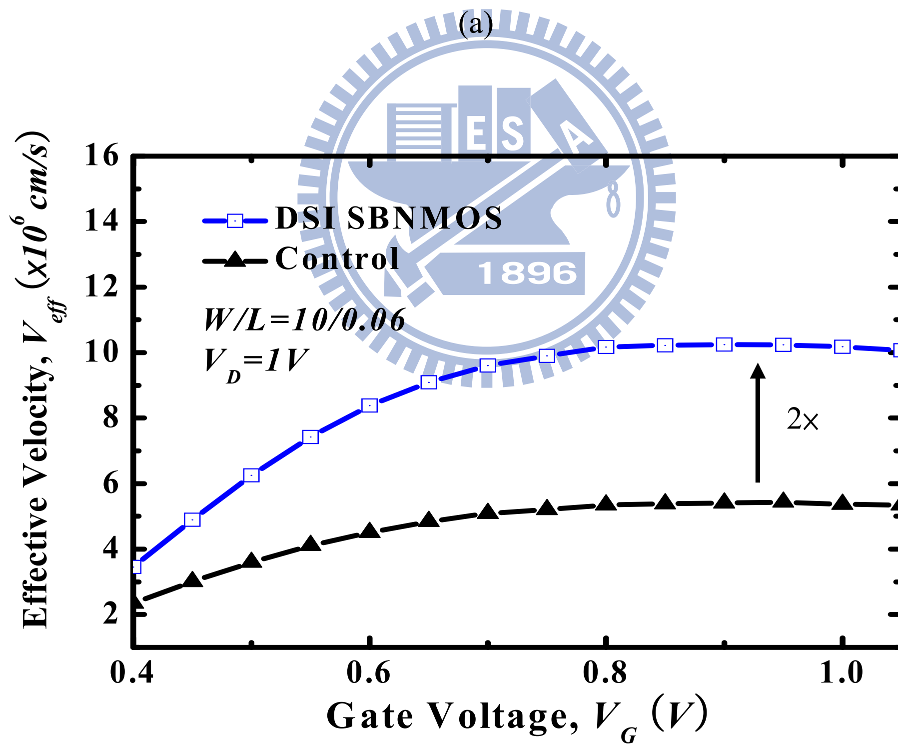


(b)

Fig. 5.4 The carrier average velocity (effective velocity) of (a) Schottky-barrier nMOSFETs. (b) Conventional nMOSFETs with doped S/D.



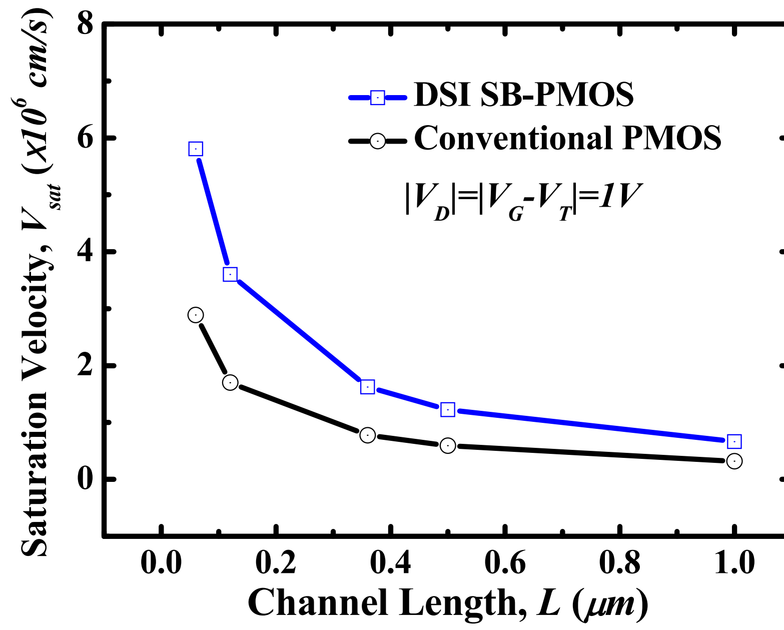
(a)



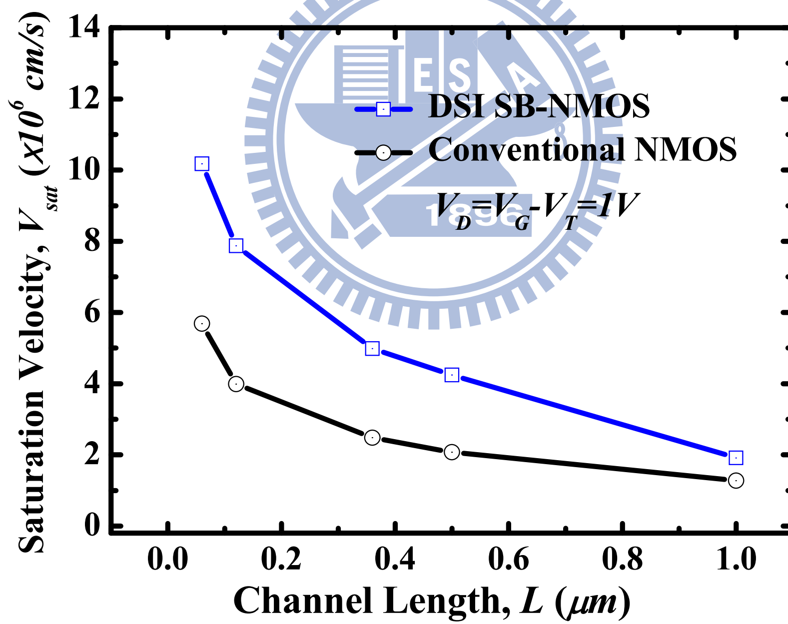
(b)

Fig. 5.5 The comparison of the carrier average velocity (effective velocity) between (a) PMOS and SB-PMOS (b) NMOS and SB-NMOS.

1896

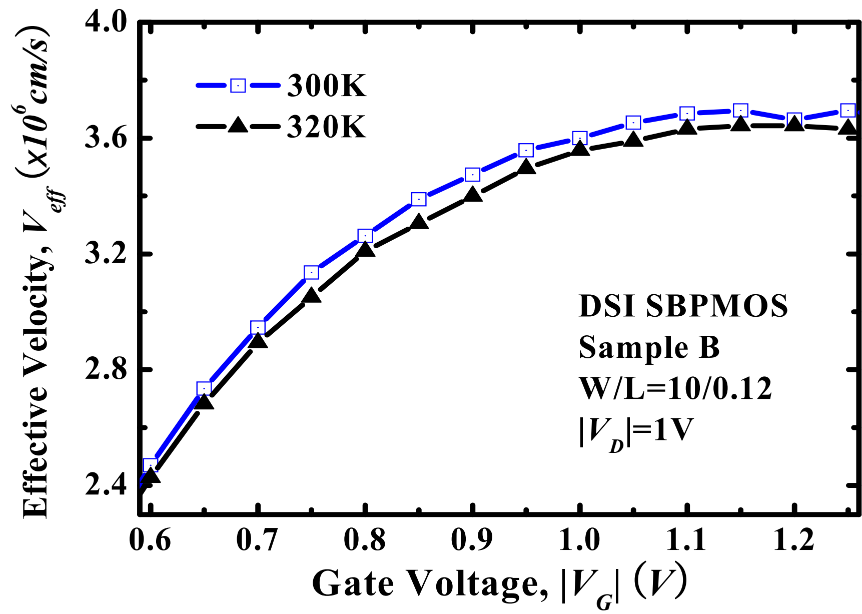


(a)

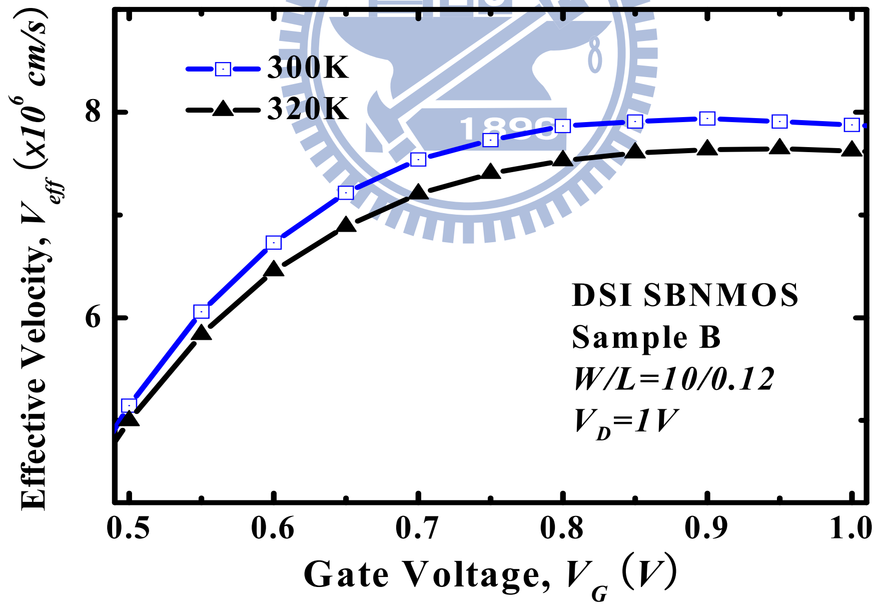


(b)

Fig. 5.6 The comparison of the effective saturation velocity between (a) PMOS and SB-PMOS (b) NMOS and SB-NMOS.



(a)



(b)

Fig. 5.7 The comparison of the carrier average velocity (effective velocity) with different temperature between (a) PMOS and SB-PMOS (b) NMOS and SB-NMOS.

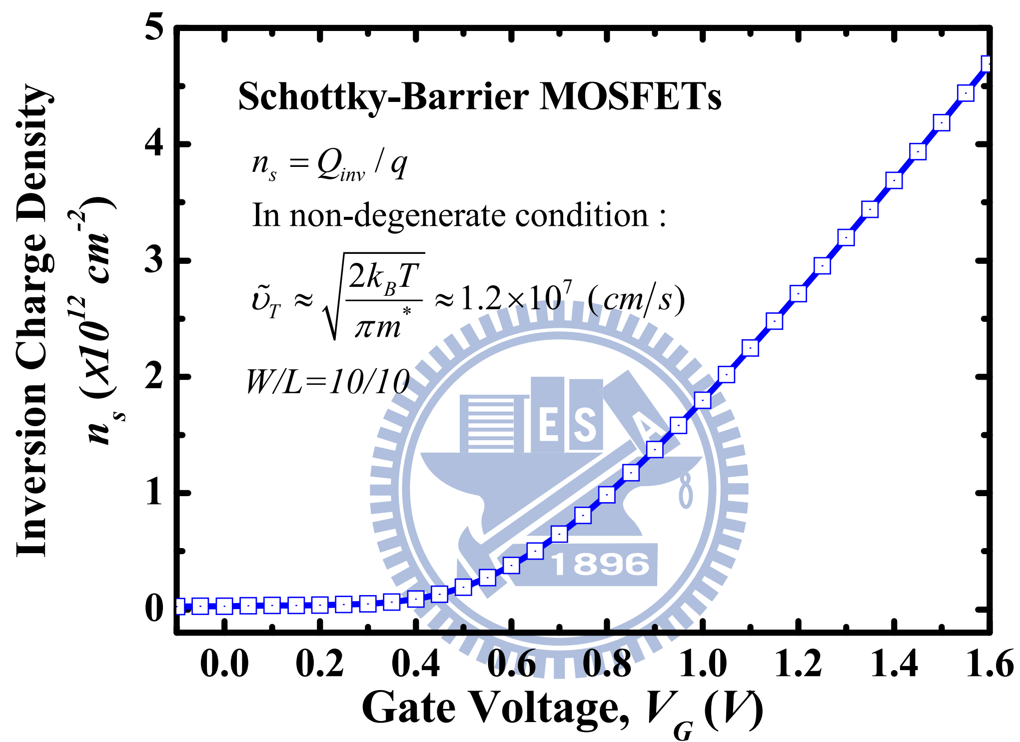
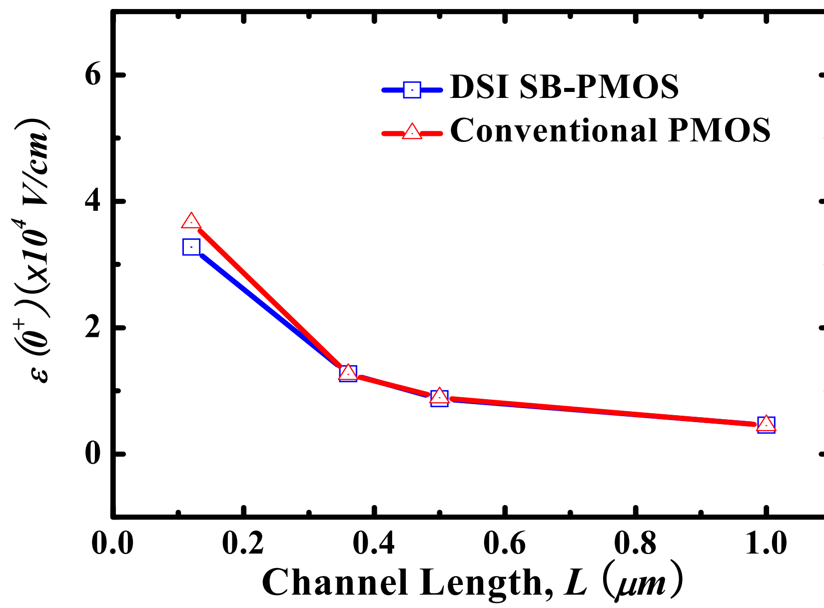
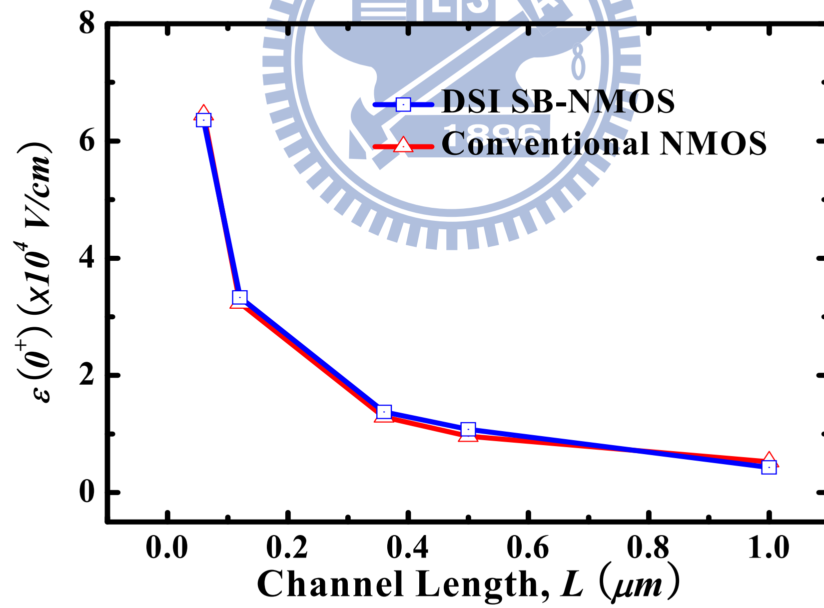


Fig. 5.8 The inversion charge density of the Schottky-barrier MOSFET with DSI.

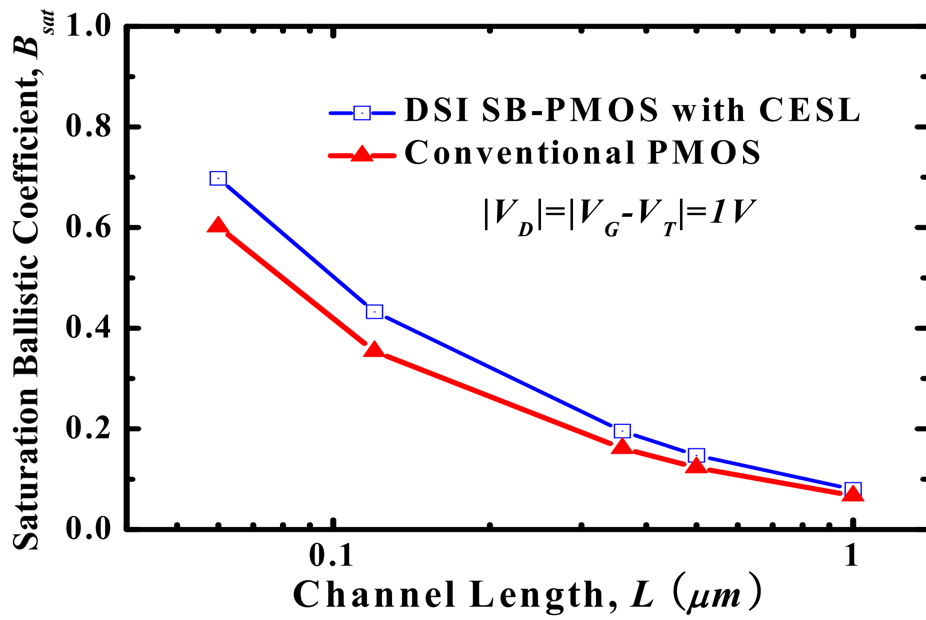


(a)

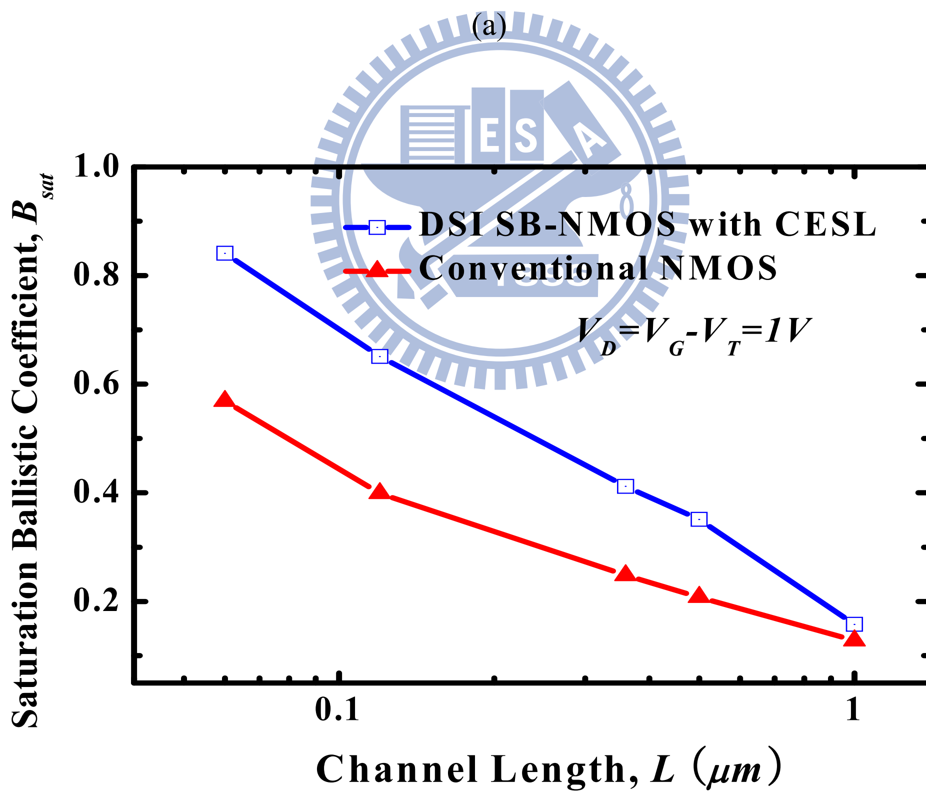


(b)

Fig. 5.9 The electric field of the channel potential (a) DSI SB-PMOS and conventional PMOS (b) DSI SB-NMOS and conventional NMOS.



(a)



(b)

Fig. 5.10 The saturation ballistic coefficient (B_{sat}) of (a) DSI SB-PMOS and conventional PMOS (b) DSI SB-NMOS and conventional NMOS.

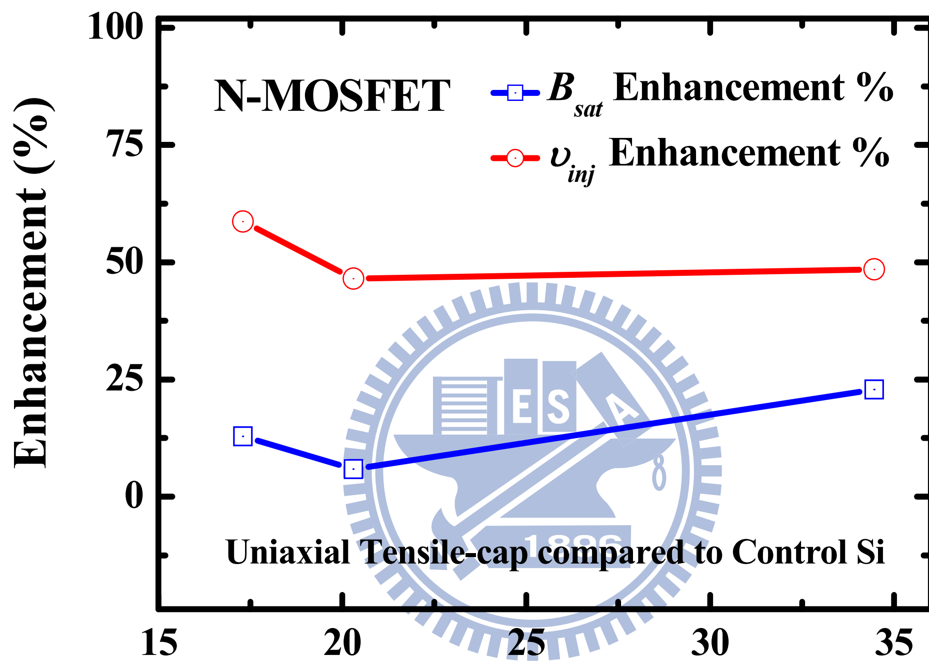


Fig. 5.11 The current enhancement rate of uniaxial tensile-cap compared to conventional structure.

Chapter 6
Conclusions

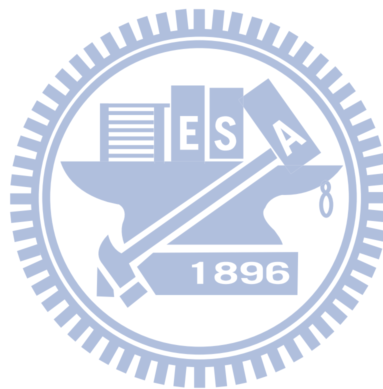
The carrier transport mechanism in the Schottky-barrier MOSFETs is a confusing issue in the past years. In recent years, we have confirmed the carrier transport mechanism by effective Schottky-barrier height variation. In this thesis, the effective Schottky-barrier height in the *DSI-SBMOS* has been investigated. When the SBMOS operates in *OFF-state*, the carriers move from source into channel by minority carriers tunneling mechanism. In the subthreshold region, the carriers thermally emit over the Schottky barrier due to its high effective Schottky-barrier height in both conduction and valance band. In *ON-state*, the most of the carriers tunnel through the Schottky barrier that leads to negative effective Schottky-barrier height.

On the other hand, some of the DSI-SBMOS with the different dopant-segregation -implantation energy have performed that the effective Schottky-barrier height is contributed by the channel barrier. Some characteristics of the DSI-SBMOS, such as threshold voltage and *OFF-state* leakage, are determined by the channel barrier. We may conclude that the Fermi-level-pining position is transferred from source-channel interface to the interface between DSI-layer and substrate.

Besides, the ballistic transport characteristic in the channel is performed by effective ballistic mobility successfully. We concluded that the carrier transport of DSI-SBMOS in the channel in low field region has larger backscattering probability than conventional MOSFET as a result of its complicated barrier which leads to large subthreshold swing. In addition, the backscattering probability in the high field region is from the ratio of the thermal injection velocity and carrier average velocity. We found that probability is smaller in SBMOS than that in the conventional device due to carrier non-local tunneling mechanism. By non-local tunneling mechanism, carriers have higher transport energy that contributed to larger transmission rate from source to channel.

In addition, we compared the backscattering characteristic in the DSI-SBMOS and

strained-Si devices. For strained-Si devices, strained-Si technology will enhance the thermal injection velocity, while it affects the backscattering coefficient lightly. For DSI-SBMOS, it enhances the backscattering coefficient instead of thermal injection velocity. If we combine these two technologies, we can get better backscattering characteristic that brings the devices close to carrier transport limitation.



References

[1] M. S. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Elec. Dev. Lett.*, vol. 18, no. 7, pp. 361-363, July 1997.

[2] M. S. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Trans. on Electron Devices*, vol. 49, no. 1, pp. 133-141, Jan. 2002.

[3] M. S. Lundstrom, "On the Mobility Versus Drain Current Relation for a Nanoscale MOSFET," *IEEE Elec. Dev. Lett.*, vol. 22, no. 6, pp. 293-295, 2001.

[4] Mark S. Lundstrom, "Fundamental of carrier transport," 2nd Edition, *West Lafayette*. Indiana, USA, Cambridge University Press, 2000.

[5] J. Guo and M. S. Lundstrom, "A Computational Study of Thin-Body, Double-Gate, Schottky Barrier MOSFETs," *IEEE Trans. on Electron Devices*, vol. 49, no. 11, pp. 1897-1902, Nov. 2002

[6] J. Wang, and M. S. Lundstrom, "Ballistic Transport in High Electron Mobility Transistors," *IEEE Trans. on Electron Devices*, vol. 50, no. 7, pp. 1604- 1609, July 2003.

[7] M. J. Chen, H. T. Huang, K. C. Huang, P. N. Chen, C. S. Chang, and C. H. Diaz, "Temperature dependent channel backscattering coefficients in nanoscale MOSFETs," in *IEDM Tech. Dig.*, pp. 39-42, 2002.

[8] M. J. Chen, H. T. Huang, Y. C. Chou, R. T. Chen, Y. T. Tseng, P. N. Chen, and C. H. Diaz, "Separation of Channel Backscattering Coefficients in Nanoscale MOSFETs," *IEEE Trans. on Electron Devices*, vol. 51, no. 9, pp. 1409-1415, Sep. 2004.

[9] E. R. Hsieh, D. W. Chang, S. S. Chung, Y. H. Lin, C. H. Tsai, C. T. Tsai, G. H. Ma, "The Ballistic Transport and Reliability of the SOI and Strained-SOI nMOSFETs with 65nm Node and Beyond Technology," *International Symp. on VLSI-TSA*, pp. 120-121, April 2008.

[10] S. S. Chung, Y. J. Tsai, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, G. H. Ma, S.

C. Chien, and S. W. Sun, "Technology Roadmaps on the Ballistic Transport in Strain Engineered Nanoscale CMOS Devices," *IEEE Conference on EDSSC*, pp. 23-26, 2007.

[11] R. Wang, H. Liu, R. Huang, J. Zhuge, L. Zhang, D. W. Kim, X. Zhang, D. Park, and Y. Wang, "Experimental Investigations on Carrier Transport in Si Nanowire Transistors: Ballistic Efficiency and Apparent Mobility," *IEEE Trans. on Electron Devices*, vol. 55, no.11, pp. 2960-2967, Nov. 2008

[12] C. K. Huang, C. K. Huang, W. E. Zhang, and C. H. Yang, "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10nm," *IEEE Trans. on Electron Devices*, vol. 45, no. 4, pp. 842-848, 1998.

[13] W. Schottky, "Semiconductor theory of the barrier film," *Naturwissenschaf-ten*, vol. 26, 1938.

[14] J. Bardeen, "Surface states and rectification at a metal semiconductor contact," *Phys. Rev.*, vol. 71, no. 10, pp. 717-727, 1947.

[15] S. M. Sze and K. K. NG, "Physics of Semiconductor Devices," 3rd Edition, *Wiley Interscience*, 2007.

[16] E. Rhoderick and R. Williams, "Metal-Semiconductor Contacts", 2nd Edition, *Oxford Science Publications*, 1988.

[17] H. A. Bethe, "Theory of the boundary layer of crystal rectifiers," *MIT Radiation Lab. Rep.*, 1942.

[18] W. Saitoh, A. Itoh, S. Yamagami, and M. Asada, "Analysis of Short-Channel Schottky Source/Drain Metal- Oxide-Semiconductor Field-Effect Transistor on Silicon-on-Insulator Substrate and Demonstration of Sub-50-nm n-type Devices with Metal Gate," Jpn. J. Appl. Phys., vol. 38, no. 11, pp. 6226-6231, Nov. 1999.

[19] M. P. Lepselter and S. M. Sze, "SB-IGFET: An insulated-gate field-effect transistor using Schottky barrier contacts for source and drain," in *Proc. of the IEEE*, vol. 56, pp. 1400-1402, 1968.

[20] T. Mochizuki and K. D. Wise, "An n-channel MOSFET with Schottky source and drain," *IEEE Elec. Dev. Lett.*, vol. EDL-5, no. 4, pp. 108-111, April 1984.

[21] D. Connelly, C. Faulkner, D. E. Grupp, and J. S. Harris, "A new route to zero-barrier metal source/drain MOSFETs," *IEEE Trans. on Nanotechnology*, vol. 3, no. 1, pp. 98-104, 2004.

[22] J. Tersoff, "Schottky barrier heights and the continuum of gap states," *Phys. Rev. Lett.*, vol. 52, pp. 465-468, 1984.

[23] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida, and J. Koga, "Solution for high-performance Schottky-source/drain MOSFETs: Schottky barrier height engineering with dopant segregation technique," in *Symp. on VLSI Tech. Dig.*, pp. 168-169, 2004.

[24] Q. T. Zhao, U. Breuer, E. Rije, St. Lenk, and S. Mantl, "Tuning of NiSi/Si Schottky barrier heights by sulfur segregation during Ni silicidation," *Appl. Phys. Lett.*, vol. 86, 062108, 2005.

[25] Y. T. Huang, P. W. Liu, W. T. Chiang, T. L. Tsai, C. H. Tsai, C. T. Tsai, and G. H. Ma, "Schottky Source/Drain CMOS Device Optimization with Dopant-Segregated NiPt Silicide," *International Symp. on VLSI-TSA*, pp. 38-39, April 2008.

[26] C. H. Ko, H. W. Chen, T. J. Wang, T. M. Kuan, J. W. Hsu, C. Y. Huang, C. H Ge, L. S. Lai, and W. C. Lee, "NiSi Schottky Barrier Process-Strained Si (SB-PSS) CMOS Technology for High Performance Applications," in *Symp. on VLSI Tech. Dig.*, pp. 80-81, 2006.

[27] B. Y. Tsui and C. P. Lin, "A novel 25-nm modified Schottky-barrierFinFET with high performance," *IEEE Elec. Dev. Lett.*, vol. 25, no. 6, pp. 430-432, 2004.

[28] K. Uchida, K. Matsuzawa, J. Koga, S. Takagi, and A. Toriumi, "Enhancement of hot-electron generation rate in Schottky source metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 76, no. 26, June 2006.

[29] B. Y. Tsui, and C. P. Lu, "Current transport mechanisms of Schottky barrier and modified Schottky barrier MOSFETs," in *ESSDERC*, pp. 307-310, 2007.

[30] J. Knoch, M. Zhang, S. Feste, S. Mantl, "Dopant segregation in SOI Schottky-barrier MOSFETs," *Microelectron. Eng.*, vol. 84, no. 11, pp. 2563-2571, 2007.

[31] J. Knoch, M. Zhang, Q. T. Zhao, St. Lenk, and S. Mantl, and J. Appenzeller, "Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation," *Appl. Phys. Lett.*, vol. 87, 263505, 2005

[32] D. S. Fisher, and P. A. Lee, "Relation between conductivity and transmission matrix," *Phys. Rev. B*, vol. 23, no. 12, pp. 6851-6854, 1981.

[33] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.*, vol. 76, no. 8, pp. 4879-4890, 1994.

[34] A. Lochtefeld, and D. A. Antoniadis, "On Experimental Determination of Carrier Velocity in Deeply Scaled NMOS: How Close to the Thermal Limit?" *IEEE Elec. Dev. Lett.*, vol. 22, no. 2, pp. 95-97, Feb. 2001.

[35] A. Kinoshita, T. Kinoshita, Y. Nishi, K. Uchida, S. Toriyama, R. Hasumi and J. Koga, "Comprehensive Study on Injection Velocity Enhancement in Dopant-Segregated Schottky MOSFETs," in *IEDM Tech. Dig.*, pp.1-4, 2006.

[36] M. S. Shur, "Low Ballistic Mobility in Submicron HEMTs," *IEEE Elec. Dev. Lett.*, vol. 23, no. 9, pp. 511-513, Sep. 2002.

[37] K. K. Thornber, "Relation of drift velocity to low-field mobility and high-field saturation velocity," *J. Appl. Phys.*, vol. 51, no. 4, pp. 2127-2136, April 1980.

[38] I. Pappas, G. Ghibaudo, C. A. Dimitriadis, C. Fenouillet-Béranger, "Backscattering coefficient and drift-diffusion mobility extraction in short channel MOS devices," *Solid State Electronics*, vol. 53, pp. 54-56, 2009.

[39] F. Lime , C. Guiducci , R. Clerc , G. Ghibaudo , C. Leroux , and T. Ernst, "Characterization of effective mobility by split *C(V)* technique in N-MOSFETs with ultra-thin gate oxides," *Solid State Electronics*, vol. 47, pp. 1147-1153,

2003.

[40] H. N. Lin, H. W. Chen, C. H. Ko, C. H. Ge, H. C. Lin, T. Y. Huang and W. C. Lee, "Characterizing the Channel Backscattering Behavior in Nanoscale Strained Complementary Metal Oxide Semiconductor Field-Effect Transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 11, pp. 8611-8617, 2006.

[41] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of Ballistic Nanotransistors," *IEEE Trans. on Electron Devices*, vol. 50, no. 9, pp. 1853-1864, Sep. 2003.

[42] W. S. Lau , P. Yang , V. Ho , L. F. Toh , Y. Liu , S. Y. Siah , and L. Chan, "An explanation of the dependence of the effective saturation velocity on gate voltage in sub-0.1 µm metal-oxide-semiconductor transistors by quasi-ballistic transport theory," *Microelectronics Reliability*, vol. 48, no. 10, pp. 1641-1648, 2008.

[43] Y. Taur, and T. H. Ning, Fundamentals of modern VLSI devices, *Cambridge University Press*, New York, USA, 1998.