國 立 交 通 大 學

電子工程學系電子研究所

碩士論文

對製程中引發應力之P-型通道金氧半電晶體的 1/f 雜訊研究

A Study of Low Frequency Noise in process Induced Stress PMOSFETs

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中華民國九十八年十月

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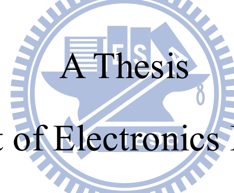

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A Study of Low Frequency Noise in process Induced Stress PMOSFETs

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Abstract

For 1.27nm thick gate oxide p-channel MOSFETs , the hole mobility booster by the means of process strained silicon (PPS) technique is applied. With the noise measurement, we can extract the trap density Nt and scattering factor α in STI compressive stress PMOSFETs. Specially, We characterize the 1/f noise power spectra density (PSD) of the drain current both in the channel width (W) and the channel length direction. In the channel length direction, the experiment results show that the STI induced stress can provide more interface trap density. However, in the channel width direction, the main decrease of the average trap density comes from the edge structure. The I-V measurement can also give us that the information the stress on narrow device is not the only reason for mobility change. With the combination of the Noise and I-V measurements, the inverse narrow channel effect may provide a appropriate interpretations to both experimental result.

對製程中引發應力之P-型通道金氧半電晶體的1/f 雜訊研究

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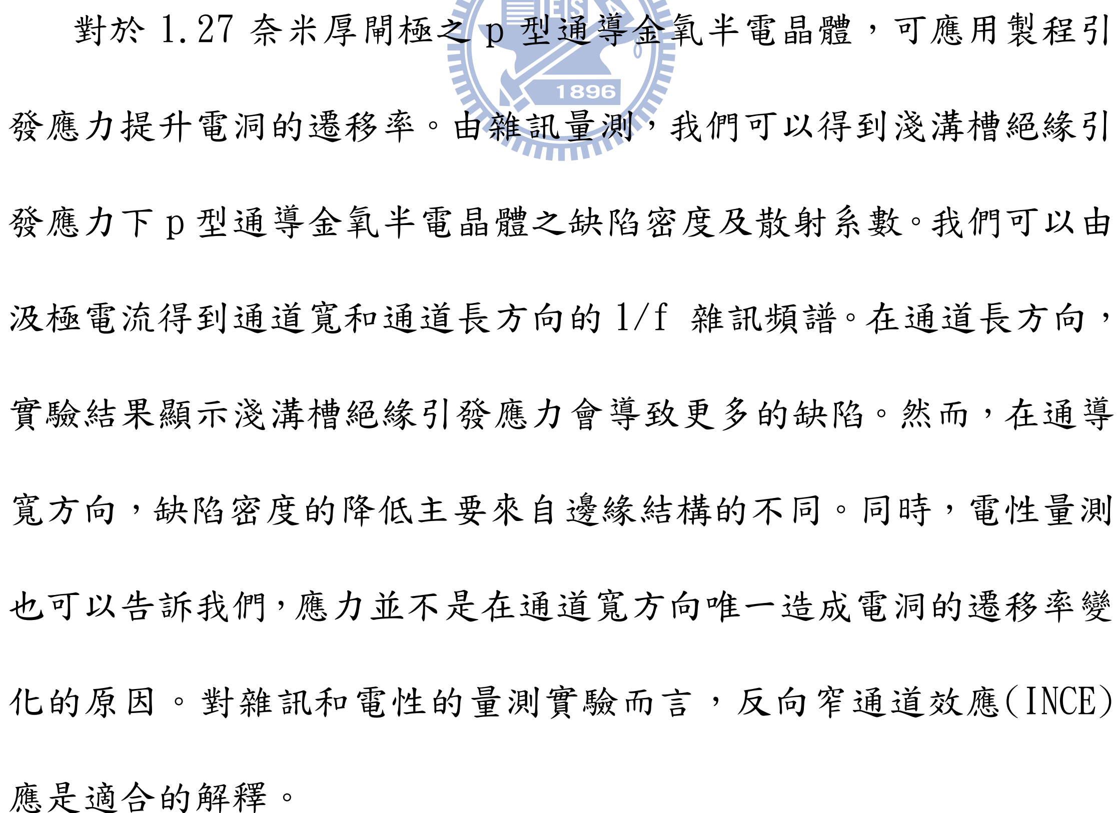
摘要



對於 1.27 奈米厚閘極之 p 型通導金氧半電晶體，可應用製程引發應力提升電洞的遷移率。由雜訊量測，我們可以得到淺溝槽絕緣引發應力下 p 型通導金氧半電晶體之缺陷密度及散射系數。我們可以由汲極電流得到通道寬和通道長方向的 1/f 雜訊頻譜。在通道長方向，實驗結果顯示淺溝槽絕緣引發應力會導致更多的缺陷。然而，在通導寬方向，缺陷密度的降低主要來自邊緣結構的不同。同時，電性量測也可以告訴我們，應力並不是在通道寬方向唯一造成電洞的遷移率變化的原因。對雜訊和電性的量測實驗而言，反向窄通道效應(INCE)應是適合的解釋。

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2009/10/4 又正寫於深夜宜蘭家中

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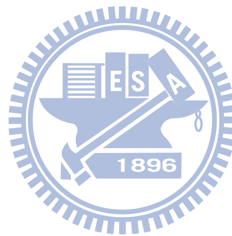
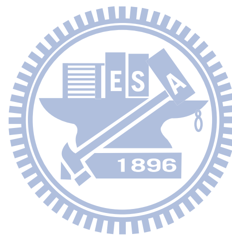


Chapter 1 Introduction

Electronic devices exhibit random fluctuations in voltage (or current) at their terminals. These fluctuations are usually referred to as noise. It originates in the random, microscopic behavior of the charge carriers in the device. It is popular in detecting the inside part of electronic devices by low frequency noise. The non-destruction investigation is the most important feature of the noise measurement. There are four typical types of noise, random telegraph signal (RTS) or low frequency (1/f noise), thermal noise, and shot noise. Each one has its physical origin. In this research, We focus on the low frequency noise on the ultra-thin gate oxide PMOSFET with STI mechanical stress to investigate the stress effect on the channel carriers.

Channel strain engineering is currently recognized as an indispensable performance booster in producing next generation metal-oxide-semiconductor field-effect transistors (MOSFETs)[1]. In order to achieve this goal, two fundamentally different methods have been proposed :(I) Strained silicon(SSi) on a relaxed SiGe buffer layer and (II)Process strained silicon (PSS) through the trench isolation, silicide, and capping layer. The un-strain low-frequency noise has been extensively examined and it has provided many interface physics [2-3]. Thus, it is challenging to examine for low-frequency noise to find further potential applications in the strain case, especially in the channel width and channel length direction.

In the investigation of ultra-thin gate oxide MOSFET device undergoing, we conduct the compressive stress on two axis directions which provide us the different direction to determine the stress induced trap density in the process strained silicon (PPS). Meanwhile, we discuss the corner edge influence on mobility shift through I-V characteristic. The TEM picture and the TCAD stress simulation in the channel width direction are also prepared. Then combined with I-V Fitting, 1/f noise, we can capture a novel picture on the stress effect affects the trap density and the mobility scattering factor.



Chapter 2 Low Frequency Noise

2.1 MOSFET Fundamentals

Current-Voltage Relations

Let we first briefly review the fundamentals of MOSFET before describing the MOSFET noise sources in next subsection. The formation of the channel allows a large current to flow between source and drain as the device is switched on. In the inversion condition, the inversion charge density can be approximated as

$$Q_i(V) = C_{eff}(V_{gs} - V_{th} - mV_c) \qquad (2\text{-}1)$$

Where Vc is the potential drop along the channel, V_{th} is the threshold voltage, m is the body-effect coefficient, and Ceff = εox/tox is the gate oxide capacitance per unit area. The gate voltage controls the charge density in the channel, thereby modulating the conductivity between drain and source. The drain current depends on the conductivity and the applied electric field in the channel. The drain current can be derived in the linear region where $V_{DS} < V_{DS,sat}$, as

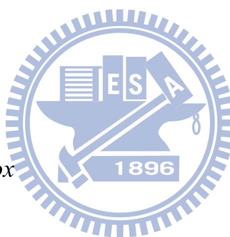
$$I_D = \frac{W}{L}\mu_{eff}C_{ox}[(Vgs - Vth)Vds - mV^2{}_{ds}/2] \qquad (2\text{-}2)$$

The threshold voltage is given by:

$$V_{th} = V_{fb} \pm 2\psi_B \pm \sqrt{\frac{4\varepsilon_{si}qN_{sub}\psi_b}{Cox}} \qquad (2\text{-}3)$$

where N_{sub} is the doping concentration in the substrate, V_{fb} the flat-band voltage, ε_{si} is the permittivity of Si and Ψ_B the energy difference between the Fermi level E_f and the intrinsic level E_i. The plus signs in Eq.(2-3) apply to NMOS and the minus signs to PMOS, respectively .

Fig.1 shows the energy band diagram of a PMOSFET biased near the threshold. Fig.2 is a schematic description of the charge distribution in the MOS structure. The flat-band voltage depends on the work function difference between the gate material and the substrate material and ϕ_{ms} the equivalent (trapped or fixed) oxide charge density at the oxide-silicon interface Q_{ox}



$$V_{fb} = \varphi_{ms} - Q_{ox} / C_{ox} \qquad (2\text{-}4)$$

For N^+ or P^+ doped poly-Si gate and p-type or n-type Si substrate, the work function difference is calculated to be

$$\varphi_{ms} = \pm 0.56 \pm kT / q \bullet \ln(N_{sub} / n_i) \qquad (2\text{-}5)$$

where the plus or minus sign in front of the first term is for p-type or n-type gate material, respectively. For the second term, the plus sign applies for n-type substrate and the minus sign for p-type.

The factor **m** in Eqs.(2-1) and (2-2), called the body effect coefficient has been inserted to account for corrections to the simple theory. The value of m is typically between 1 and 1.4. It is calculated as follows [4]: The drain current in Eq. (2-2) increases with the drain voltage until a maximum is reached and saturation occurs. The drain voltage at saturation is

$$dI_d / dV_{ds} = 0 \Rightarrow V_{ds,sat} = (V_{gs} - V_{th}) / m \qquad (2\text{-}6)$$

At this pinch-off point, the channel at the drain end vanishes. The electric field along the channel between the source end and the pinch-off point stays constant with increasing $V_{ds} > V_{ds,sat}$. By inserting Eq. (2-7) in Eq. (2-2), the drain current in the saturation region can be written as

$$I_d = \frac{W}{L} \mu_{eff} C_{ox} \frac{(V_{gs} - V_{th})^2}{2m} \qquad \textbf{(2-7)}$$

2.2 Noise and fluctuation

Metal-oxide-semiconductor field-effect transistor (MOSFETs) are finding more and more important applications in area of analog integrated circuits. There exist three models that have been invoked to account for the origin of flicker noise: **Number fluctuation model, mobility fluctuation model and unified correlated model**.

2.2.1 The McWorther model (Number fluctuation)

In the number fluctuation model, as originally proposed by McWhorter [5], flicker noise is attributed to many discrete changes, called RTS noise, in drain current resulting from trapping and detrapping into single oxide defects in the oxide by tunneling. Fig.3 shows the schematic illustration of how the oxide traps exchange carriers with the channel, causing a fluctuation in the surface potential, giving the fluctuations in the inversion charge density. The g-r noise in the oxide charge generated by one trap that randomly captures and releases channel electrons can be written as

$$S_{Qox} = S_{vgb} C^2{}_{ox} = \frac{q^2}{W^2 L^2} 4\overline{\Delta Nox}^2 \frac{\tau}{1+(2\pi f\tau)^2} \qquad (2\text{-}8)$$

The variance in △Nox due to a trap at energy E , Nox is the number of oxide charges can be calculated from the probability that the trap is occupied. The probability is given by Fermi-Dirac distribution function F(E)

$$f(E) = [1 + Exp(\frac{E - E_{f,n(p)}}{kT})]^{-1} \tag{2-9}$$

Then

$$\begin{aligned} \overline{\Delta Nox}^2 &= (1 - f(E))^2 f(E) + (0 - f(E))^2 (1 - f(E)) \\ &= f(E)(1 - f(E)) \end{aligned} \tag{2-10}$$

Now, the contribution from all traps in the gate oxide should be taken into account. The total PSD is found by summing over all traps whose noise contributions are given by Eq.(2-8). However, the individual traps are not known. It can instead assume a density of trap Nt (x,y,z,E) in volume and make an integration [6,7]

$$S_{Qox} = \frac{q^2}{W^2 L^2} \int_{Ev}^{Ec} \int_0^W \int_0^L \int_0^{tox} 4Ntf(E)(1 - f(E)) \frac{\tau}{1 + (2\pi f \tau)^2} dxdydzdE$$

(2-11)

The product f(E)(1-f(E))=-kT (df(E)/dE)is sharply peaked around the quasi-Fermi level and Nt is considered as uniform over the gate area. Thus

$$S_{Qox} = \frac{q^2 kT}{W\ L} \int_0^{tox} 4Nt \frac{\tau}{1 + (2\pi f \tau)^2} dz \tag{2-12}$$

where Nt is the density of traps in the gate dielectrics at the quasi-Fermi level (in unit of $cm^{-3}eV^{-1}$) since these traps are the only ones that contribute to the 1/f noise. Other traps are permanently filled or permanently empty. In the McWorther model, which assumes that trapping and detrapping occur through tunneling processes, the trapping time constant is given as

$$\tau = \tau_0 (E) * Exp(z / \lambda) \qquad (2\text{-}13)$$

For an electron tunneling from the interface (z = 0) to a trap located at a distance z in the gate oxide. The tunneling attenuation length λ is predicted by the Wentzel-Kramers-Brilloui (WKB) theory [7] to be

$$\lambda = [\frac{4\pi}{h}\sqrt{2m * \Phi B}]^{-1} \qquad (2\text{-}14)$$

where Φ_B is the tunneling barrier height as seen by the carriers at the interface and h is Planck's constant. Calculations using Eq.(2-14) give $\lambda \sim 1A$ for the Si/SiO_2 system. The time constant τ_0 is often taken as 10^{-10} s. This yields z =2.6nm and 0.7nm for a frequency of 0.01Hz and 1MHz. Thus, oxide traps located too close to the channel interface are too fast to give 1/f noise, those located more than ~3nm from the interface are too slow to contribute. By inserting Eq. (2-13), the integral in (2-12) can be evaluated as

$$S_{vfb} = \frac{q^2 kT\lambda N_t}{f^r WLC^2{}_{ox}} \qquad (2\text{-}15)$$

The trap density can also vary with energy, which affects the bias and frequency dependence of the noise. The band diagram in Fig.4 describes the tunneling transitions, (i) directly [7] and (ii) using interface traps as stepping stones [8] from the Si to gate oxide, and the Window (z,E) of traps seen at a particular bias point (shaded area). The interface trap density often shows a U-shaped curve as a function of energy in the bandgap with increasing values towards the conduction of valence band edges. If the oxide trap density follows the same behaviour, Nt is predicted to increase with gate bias since the quasi-Fermi level approaches Ec to Ev. Due to the band bending of the gate oxide, an energy dependent trap density should be accompanied by a frequency exponent $\gamma \neq 1$.Traps in the oxide interior are swept "faster" in energy than the traps at the channel interface. So, it is expected that $\gamma \succ 1$ and increases with gate bias in the case of a trap density that increases towards the band edges.

However, the tunneling model presented here is not the only one that can give the appropriate distribution of time constants in order to achieve the 1/f fluctuations. Another possibility is thermally activated traps with time constant exponentially depending on energy [9]:

$$\tau = \tau_{o,th} Exp[E / kT] \qquad (2\text{-}17)$$

2.2.2 The Hooge model (Mobility Fluctuation)

On the other hand, the mobility fluctuation theory [10~12] considers the flicker noise as a result of the fluctuation in the bulk mobility based on the Hooge's empirical relation for the spectral density of flicker noise in a homogenous sample.

The drain current noise generated by fluctuations in the channel carrier mobility is given according to Hooge's empirical formula

$$\frac{S_{id}}{I_d^{\,2}} = \frac{q\alpha_H}{fWLQ_i} \tag{2-18}$$

In the linear region, $Q_i(V) = C_{ox}(V_{gs} - V_{th} - mV)$,Thus the normalized drain current noise depends inversely on the gate voltage overdrive .The Hooge parameter can often be considered as a constant, but the channel position under the gate oxide and the bias dependence of different scattering mechanisms both likely affect the mobility fluctuation noise. The relation in Eq. (2-18) is only valid when the carrier density is uniform. In the saturation region, the carrier density varies parabolically along the channel and reaches zero at the drain end. Then the total channel drain current noise is evaluated by dividing the channel into small segments. Each generating a noise contribution and integrating over the channel, leading to

$$\frac{S_{id}}{Id^2} = \frac{q\alpha_H}{fWL^2}\int_0^L \frac{dx}{Qi(x)} = \{I_d = W\mu_{eff}QidV\ /\ dx\}$$
$$= \frac{q\alpha_H}{fWL^2}\int_0^{Vds} \frac{W\mu_{eff}}{I_d}dV = \frac{q\alpha_H V_{ds}}{fL^2 I_d} \tag{2-19}$$

This equation is valid for all regions of operation, but V_{DS} is replaced with $V_{DS,sat}$ for V_{DS} > $V_{DS,sat}$. Using $Vds,sat = (Vgs - Vth)/m$ and Eq.(2-7) the following expression applies to the saturation range

$$\frac{S_{id}}{Id^2} = \frac{q\alpha_H \sqrt{2\mu e_{ff}}}{f\sqrt{WL^3 C_{ox} m I_d}} \qquad (2\text{-}20)$$

In the subthreshold region, the drain current is dominated by diffusion

$$I_{d,diff} = \frac{WkT\mu_{eff}}{q}\frac{dQi(x)}{dx} \qquad (2\text{-}21)$$

Using the above expression in the integral to the left in Eq.(2-19),it is readiliy shown that the same final result can be obtained. However, the drain current and the total charge density Q_i is independent of each other for Vds>>kT/q. The mobility 1/f noise is also independent of Vds in this case and can be written as

$$\frac{S_{id}}{Id^2} = \frac{\alpha_H \mu_{eff} 2KT}{fL^2 Id} \qquad (2\text{-}20)$$

2.2.3

The Unified model (Number Fluctuation with Mobility Correlation)

A more widely accepted model, proposed by Hu's group [6, 13], is based on a theory that incorporates both the oxide-trap-induced carrier number and surface mobility fluctuation mechanism. The flat band perturbation theory shows that fluctuating oxide charge density δQox is equivalent to a variation in the flat-band voltage

$$\partial V_{fb} = \partial Q_{ox} / C_{ox} \tag{2-21}$$

The fluctuation in the drain current Id = f(V $_{fb}$,u$_{eff}$) then yields[14]

$$\partial I_d = \frac{\partial I_d}{V_{fb}} V_{fb} + \frac{\partial I_d}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \partial Q_{ox} \tag{2-22}$$

Since d(Id)/d(Vfb)= -d(Id)/d(Vgs)=-gm , (+gm for PMOS) we have

$$\partial I_d = -gmV_{fb} + \frac{I_d}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \partial Q_{ox} \tag{2-23}$$

One can define a coupling parameter or scattering parameter that reflects how a variation in the oxide charge couples to the mobility:

$$\alpha = \frac{1}{\mu^2_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \tag{2-24}$$

(valid for NMOS; a minus sign must be added for pMOS)

Inserting in Eq(2-23) gives

$$\partial I_d = -g_m \partial V_{fb} - I_d \mu_{eff} \alpha C_{ox} \partial V_{fb} \tag{2-25}$$

Calculating the power spectral density PSD, we have

$$S_{vg} = \frac{S_{id}}{gm^2} = S_{vfb} (1 + \frac{\alpha \mu_{eff} C_{ox} I_d}{g_m})^2 \tag{2-26}$$

The first term in the parentheses of Eq.(2-26) is due to fluctuating number of inversion carriers and the second term to mobility fluctuation correlated to the number fluctuations. Note that α can be negative or positive depending on the increase or decrease mobility upon trapping a charge according to Eq.(2-24):

Chapter 3 Experimental Setup

3.1 Introduction

Much of my graduate school time in I-V and noise measurement was to re-build our noise instruments. To do this work is useful for me to know lots of details about the connection in IV and Noise system. I learn the whole concept of the system and have the ability to maintain the noise system work. However, too much time in setting up the system, it let me have not enough time to research all the structure change induce by stress. That explains why I have no NMOS experiment data.

3.2 Device Structure Description

Fig.5 shows the STI induced stress in the channel width (W) and channel length direction (L). It is easy to know the compressive stress due to SiO_2 and Si lattice difference. Many of research [15] have discussed the stress induced mobility change. We can change the value of the channel width (W), channel length (L), gate to STI spacing (A) to control the stress with the reference point available.

3.3 I-V Noise Experimental Setting

The device under test was a PMOSFET fabricated using the concept of process compressive strain, main through the trench isolation. The physical gate oxide thickness was 1.3nm as determined by capacitance voltage fitting. In the channel length direction, we fixed channel length 1um and channel width 10um. By changing the gate to STI spacing A, can give the distinct stresses. On the other hand, in channel width direction, we fixed the channel length as 1um while the channel width spanned a wide range of 0.11,0.24,0.6,1, and 10um. Here a reduction in channel width means an enhancement in compressive strain in the channel width direction. Also we have the TEM picture to check the accurate dimensional in our device.

The IV measurement setting in Vd is -25 mV and -100 mV, that we can use the perturbation of flat-band theory to fit our experimental data, We set the Vg at -1~0V, to make sure our device is working at no breakdown region. The noise spectral set Vd= -50meV, with Vg is -0.3V, -0.4V,-0.5V,-0.6V and -0,7V. The scanning frequency is 1Hz to 1000Hz, The reason for using a smaller frequency is to avoid the thermal noise effect on our PSD which appears above 10KHz.

Chapter4
Experimental Results and Detail Analysis

4.1 Noise Fitting Between (Vg-Vth) and Id/gm

The **Number fluctuation with mobility correlation model** is according to flat-band theory. Ananda S. Roy and Christian C. Enz [16] have been discussed the appropriate applicability range in flat-band theory. We need to make the same assumptions that are behind the flat-band perturbation method: a long-channel MOSFET, a pure number fluctuation model, and a constant trap density over the band gap.

However, Chan, et al.'s paper [17] shows their gate to STI spacing effect on stress in noise data. Their device bias on V_d =-0.7V. The fluctuation model is not therefore suitable for their analysis. Their noise data variation is also too big to have the accurate standard deviation.

On the other hand, some research fit the noise data, which can be used to assess the trap density Nt($cm^{-3}eV^{-1}$) and scattering factor α (Vs/C) by the method of fitting $Svg^{0.5}$ and (Vg-Vth).

$$\sqrt{Svg} = \sqrt{\frac{q^2 k_b T\lambda}{C_{eff}{}^2}\frac{N_t}{WL}\frac{1}{f^{\gamma}}}\left(1+\frac{\alpha\mu_{eff}C_{ox}I_d}{g_m}\right)$$
$$\approx \sqrt{\frac{q^2 k_b T\lambda}{C_{eff}{}^2}\frac{N_t}{WL}\frac{1}{f^{\gamma}}}\times\left(1+\alpha\mu_{eff}C_{ox}(V_{gs}-V_{th})\right) \quad (4\text{-}1)$$

In the traditional analysis, one often set the id/gm= Vg-Vth .Because the mobility change by Vg is set as constant. But, in the ultra-thin gate oxide device, the mobility change with Vg need to be considered as the fact on our PMOS device. Let we discuss the relation between the two terms.

$$\frac{Id}{gm} = \frac{(Vg - Vth - Vds/2)}{\frac{1}{ueff}(\frac{\partial ueff}{\partial Vg})(Vg - Vth - Vds/2) + 1} \qquad (4\text{-}2)$$

Fig.6 shows the difference between id/gm and Vg-Vth, which means that Vg-Vth is a straight line, and id/gm is a curve. We can put the same data from our ultra-thin gate oxide device to fitting the $Svg^{0.5}$ by id/gm or Vg-Vth to discuss if mobility variation is important or not. The Fig.7 shows two different fitting results on the same sample. Obviously, id/gm is the correct choice for fitting. The NMOS device has less mobility factor α (Vs/C) influence. So, we can get in accurate but similar result with the Vg-Vth method. On the other hand, it is important for our PMOS device to use the Id/gm method.

4.2 Stress Simulation by Sentaurus TCAD Simulation and Mobility-Shift Extract Stress

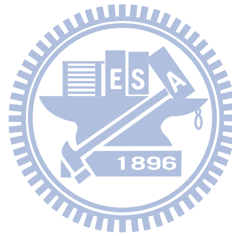
Usually, there exist two ways to determine the stress in the device. One is mobility shift approximation method, and the other is TCAD lattice simulation. In this subsection, I will demonstrate the 2D TCAD simulation result in the channel width direction, and compare with other references, the mobility shift approximation method will discussed latter.

First of all, the TCAD stress simulation follows the standard STI fabrication process to realize the device structure. It includes the substrate, pad oxide, nitride deposition, STI lithography mask, STI Etching, annealing, TEOS deposition, and fake STI CMP. Main reasons for the stress origin and the lattice mismatch induced stress. Fig.8 shows the contours of stress across the whole device. We choose the stress under the surface of 2nm, which means actual carrier transport region for our device analysis. Fig.9 demonstrates the stress distribution along the channel width. Also, Fig.10 compares our simulation result with that Shih of etal. [18], compare results can be seen similar. At the same time, by using Fig.11 we can use our simulation to separate the channel stress into the average edge stress and the average flat region stress.

In 2006, Thompson etal. [15] provides the energy level calculation relation between Stress and mobility shift. At the low strain condition, the mobility enhancement is

$$\Delta \mu / \mu \approx \left| \pi \perp \sigma \perp + \pi \parallel \sigma \parallel \right| \qquad (4\text{-}3)$$

were $\Delta \mu / \mu$ is the fractional change in mobility $\sigma \perp$ and $\sigma \parallel$ are the longitudinal and transverse stress, and the $\pi \perp$ and $\pi \parallel$ are the longitudinal and transverse piezoresistance coefficients express by Pa^{-1} respectivelyThe complete summary of the piezoresistance coefficient is shown in Table 1.



4.3 TEM Picture

In the narrow device, we have taken the cross-sectional transmission electron microscopy (TEM) (not shown in the thesis) picture of devices in the width. From the TEM results, we can take it as the reference to confirm the precise stress simulation. Unfortunately, TEM results tell us the delta width (DW) does not exist for our device.

In saturation region,

$$Id = \frac{W}{2L} Cox\mu_{eff} (Vg - Vth)^2 \qquad (4\text{-}4)$$

By fixing the channel width length, we can get the correct mobility shift from our experiment in order to extract the inner stress.

4.4 Channel Length Direction related IV and Noise Experiment

4.4.1 Vth and Mobility Shift

Fig.12 show the Vth shift for different value of gate to STI spacing (A). Fig13 shows the mobility of four devices, using calculated mobility shift by piezo-resistance coefficients. The stress extracted in Table2. Experiment shows the small spacing A gives the larger stress in our device.

4.4.2 Noise Data Analysis

Fig.14 Fig.15 Fig.16 Fig.17 is the $Svg^{0.5}$ varies Id/gm line at frequency =25Hz, Spacing A=10um, 2.4um, 0.495um, and 0.21um. Fig.18 is the fitting line for the trap density Nt ($cm^{-3}eV^{-1}$) and scattering factor α (Vs/C). Fig.19(a) and 19(b) shows the correspond Nt and α change. Although the stress change is large, and Nt has only slightly increase. The change of scattering factor is also weak.

4.5 Channel Width Direction related IV and Noise Experiment

4.5.1 Vth and Mobility shift

Fig.20 shows the Vth shift in narrow device, revealing that the more narrow width, the less change for Vth. It is well known that inverse narrow channel effect would apply especially in STI device process. △Vth~10meV was typical for edge electric field Increase, Many researches [19] suggest that the edge electrical field is more strong which makes Id current turn on more quickly.

Fig21.a is the mobility of five device (W=10,1,0.6,0.24,0.11um). If we set the x-axis as channel width, y-axis as the mobility in Vg=-0.5V, the mobility shift is very interesting. Fig.21b shows the concave up in case of narrow device, but the prediction of compressive stress effect on narrow device is presented the red line. It seems that the narrow device has different behaviors. The inverse narrow channel effect may be the suitable explanation for this phenomenon.

4.5.2 Noise Data Analysis

We have show in section 4.4 that more compressive stress renders device trap slitly increase. Fig22(a) , 23(a), 24(a), 25(a), 26(a) is the $Svg^{0.5}$ varies Id/gm line at frequency =25Hz ,for the channel width W=10um , 1um ,0.6um,0.24u,0.11um. Fig.22(b), 23(b), 24(b), 25(b), 26(b) shows the fitting lines for the trap density Nt($cm^{-3}eV^{-1}$) and scattering factor α (Vs/C).

Fig.27 (a) and (b) gives us more surprising results, the Nt in narrowest device (W=0.11um) is 1/8 of Nt(W-10um). In our further experiment, it is not reasonable, leading a simple assumption that more stress give more defects Nt. So, we think the narrow device corner has less trap density. It gives the reason why the average Nt is much more degraded in narrow device This structure difference overcomes the compressive stress effect in narrow channel case. Meanwhile, the scattering factor α is in the increasing trend, which can account for the mobility abnormal phenomenon in narrower device.

Chapter 5 Conclusion

In this thesis, we demonstrate the process strained silicon (PPS) induced stress distribution by the TCAD simulation. From stress induced energy level change, the mobility shift gives us another way to determine the stress in PMOS structure. Both of two methods tell us that the narrow device or a short gate to STI spacing (A) can provide enough evidence to make sure more increasing on the magnitude of the compressive stress.

By the Id/gm noise fitting method, we can extract the trap density and scattering factor. In the channel length direction, the experiment shows the STI induced stress can give more traps. However, in channel width direction, the large variation of the average trap density comes from the edge structure difference between the middle part. The I-V measurement also gives us the stress on narrow device is not the only reason for mobility change. Inverse narrow channel effect in Vth and mobility would be considered as the plausible origins for the narrow device. When we fabricate the narrow devices to increase the device number per area for cost-down, considering behavior of the narrow device in terms of the mobility, trap density, and Scattering factor should all be taken into account.

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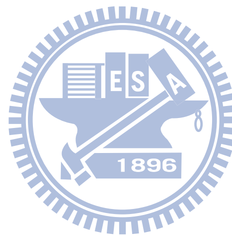


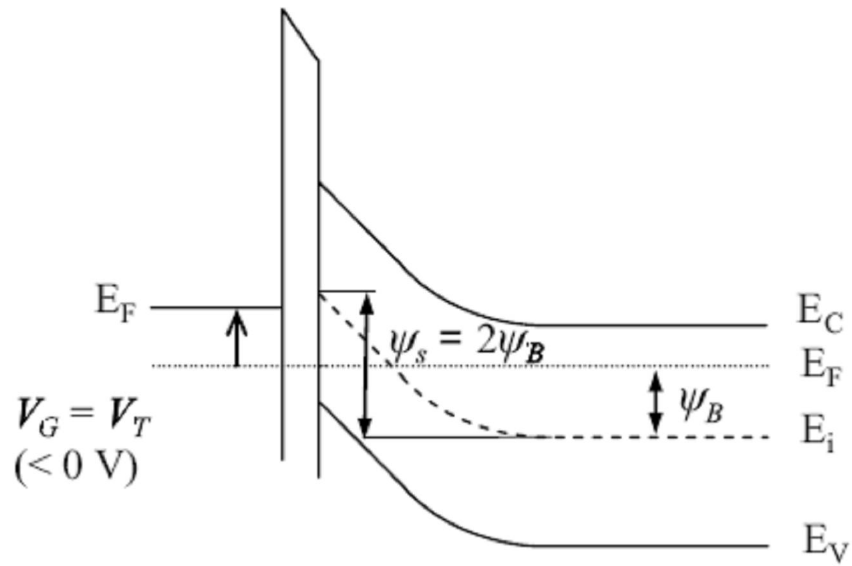


Fig.1 the Energy band diagram illustration of a PMOSFET biased near the threshold point

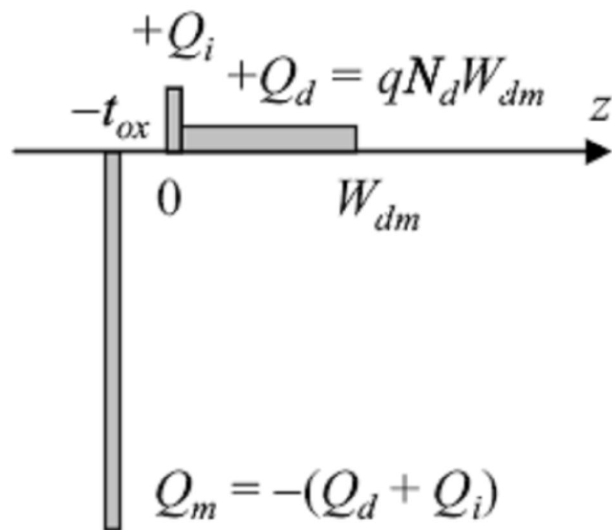


Fig2 A schematic description of the charge distribution in the MOS structure.

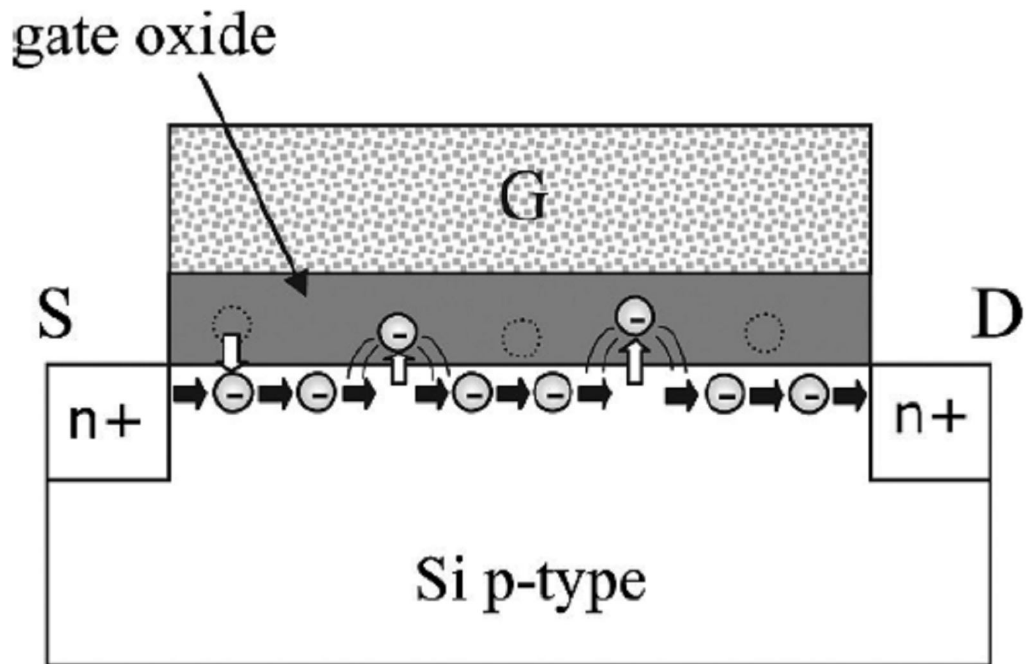


Fig.3The schematic illustration of oxide traps exchange with the channel carriers causing a fluctuation in the surface potential.

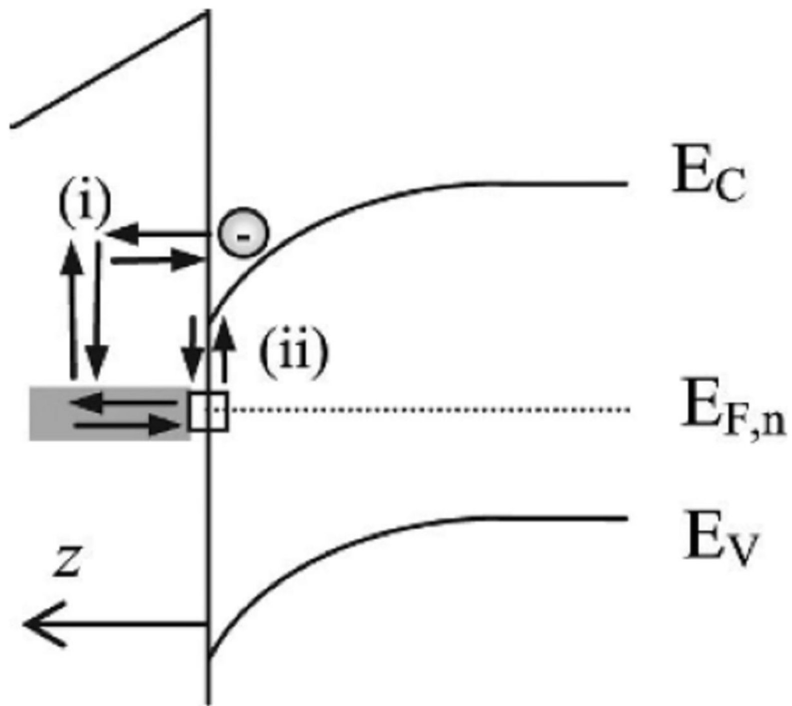


Fig4The band diagram describe the tunneling transitions, (i) directly [7] or (ii) using interface traps as stepping stones [8] from the Si to gate oxide

Device Structure

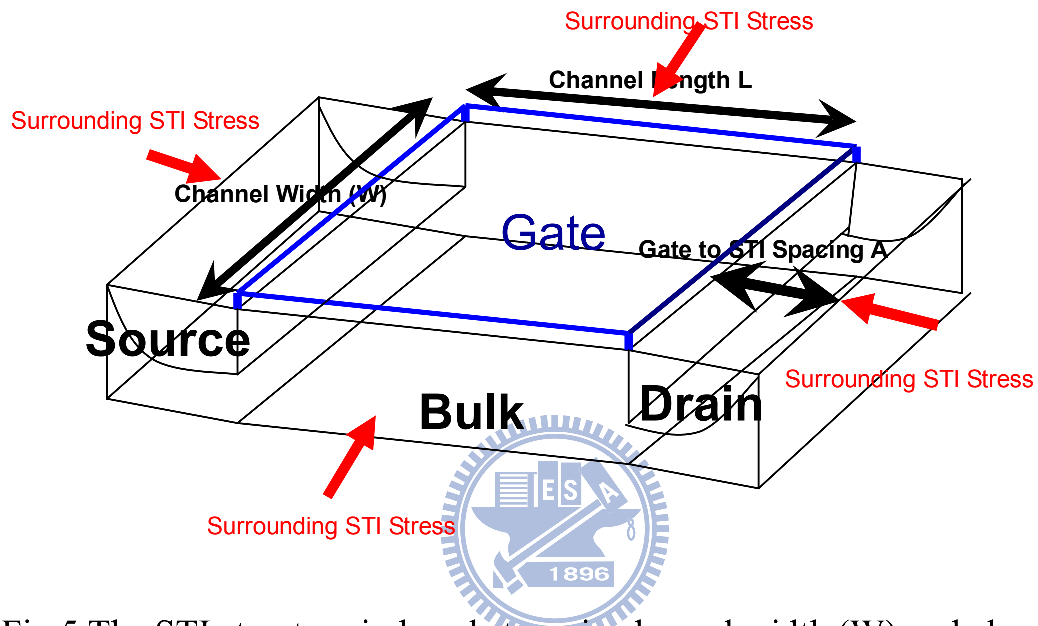


Fig.5 The STI structure induced stress in channel width (W) and channel length direction (L).

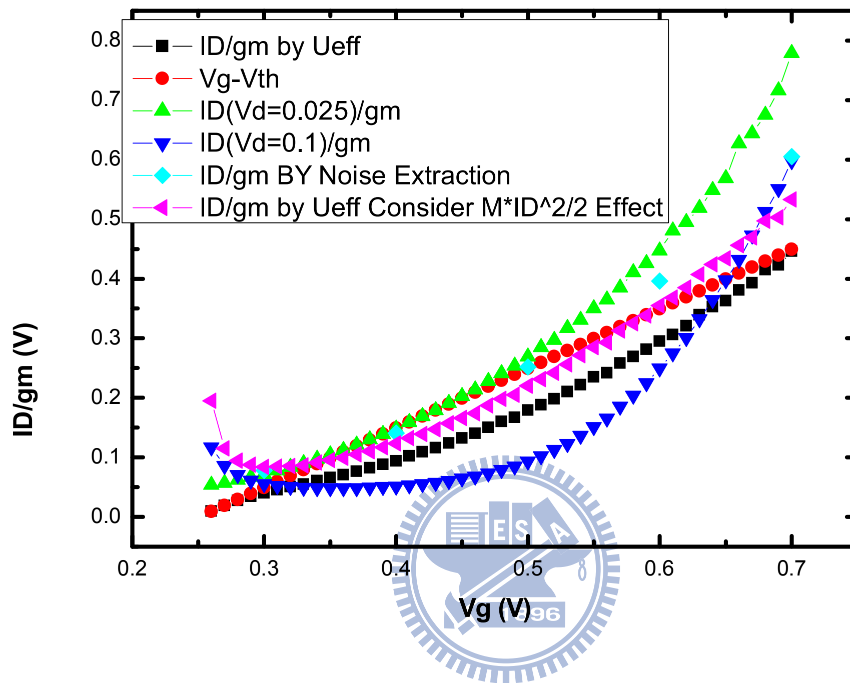


Fig.6The difference between id/gm and Vg-Vth fitting method. We can see that Vg-Vth is a straight line, instead id/gm is a curve .

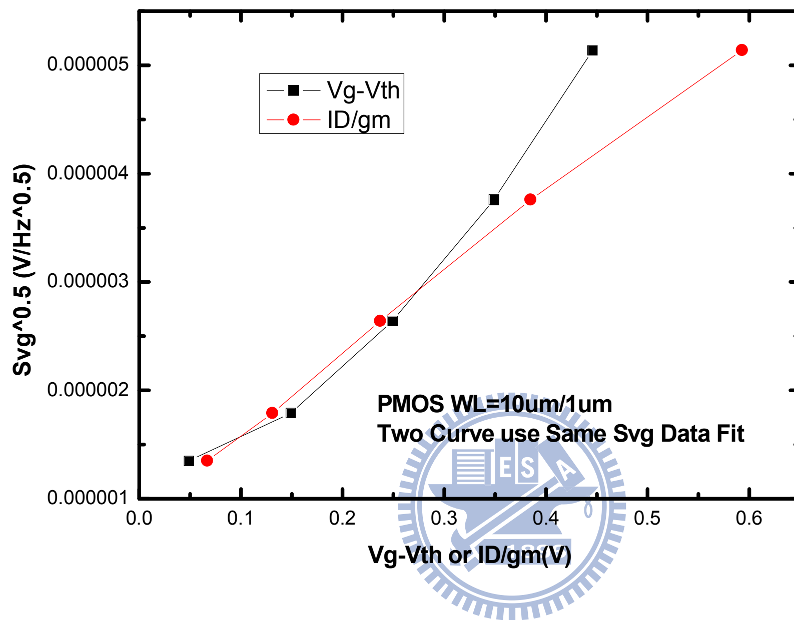


Fig.7 Two different fitting method (Vg-Vth, Id/gm) on the same sample.

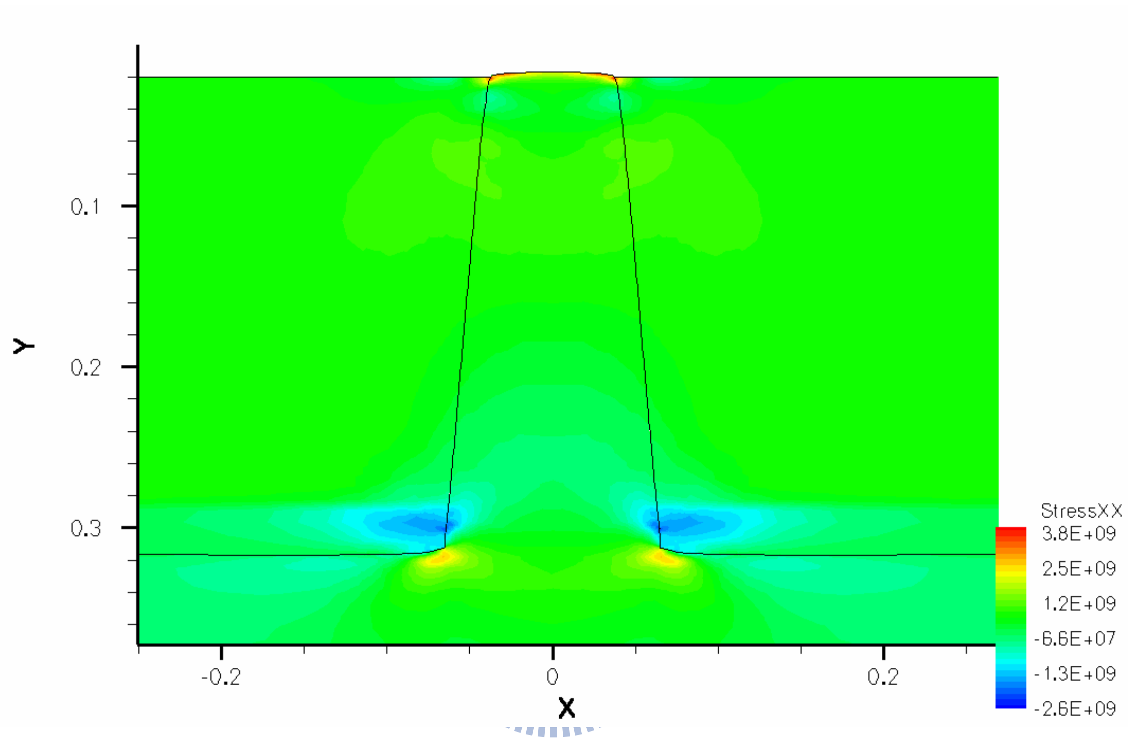


Fig8 The contours of stress distribution across the whole device.

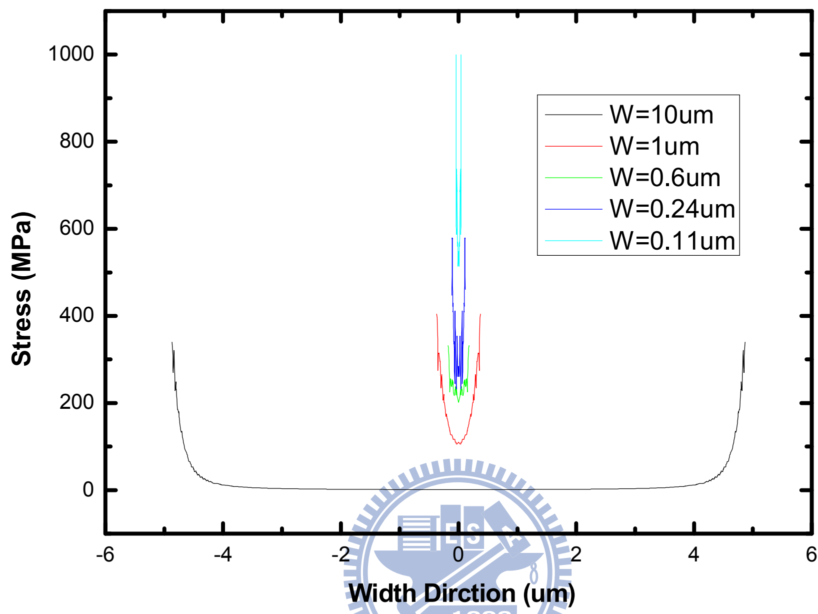


Fig.9 The stress distribution along the channel width.

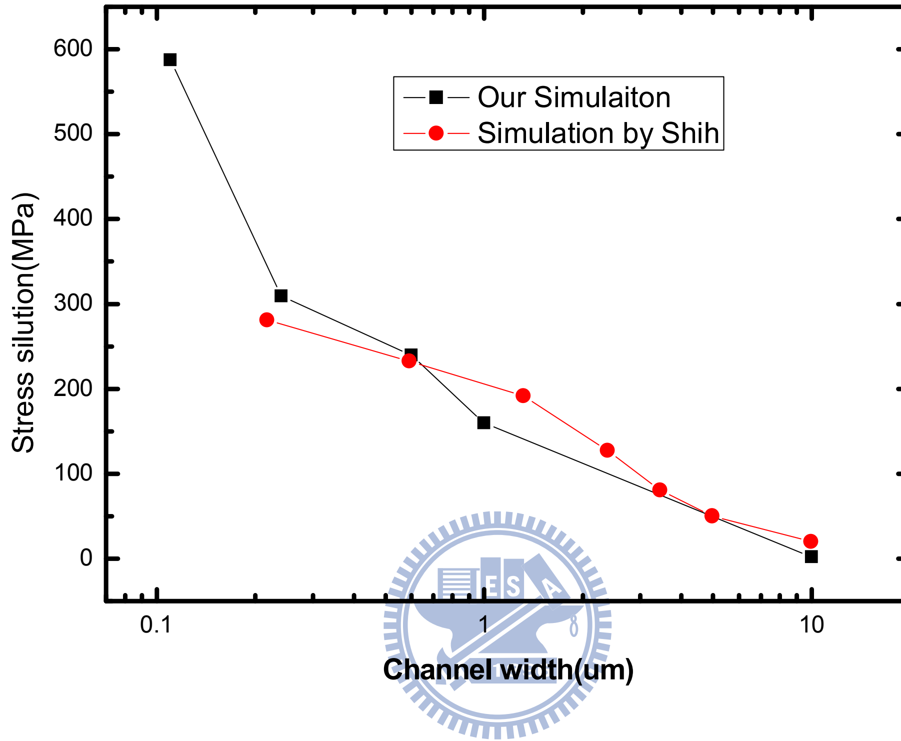


Fig.10 Comparing our simulation result with Shih[18].

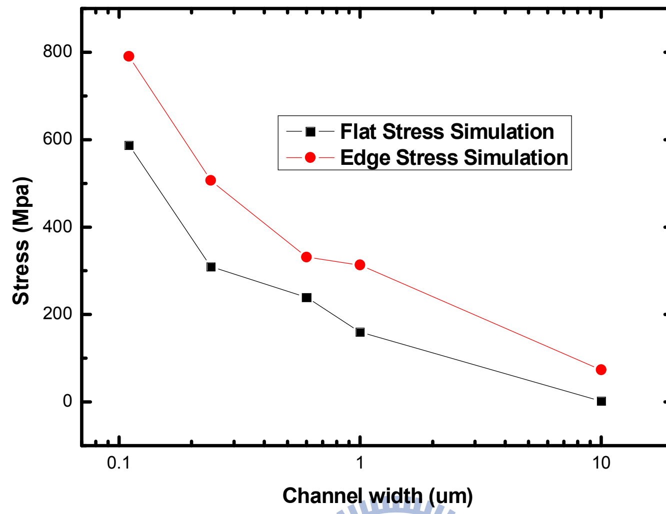


Fig11 The separated stress in terms of the average edge stress and average flat region stress.

< Unit : 10^{-12} cm^2/dyn >

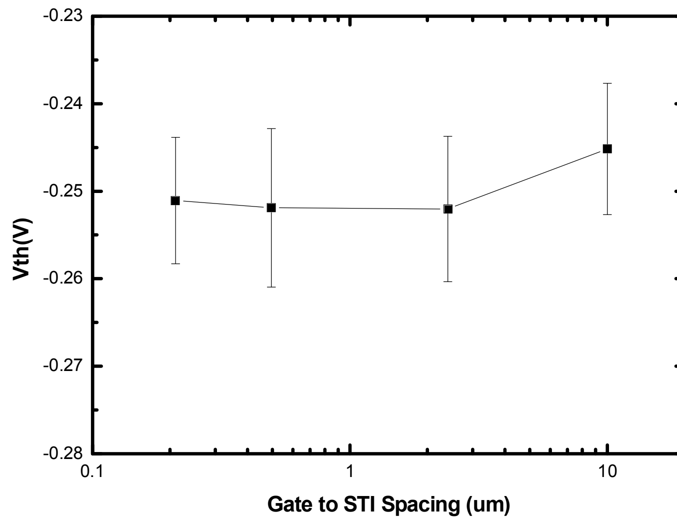
(001) wafer	<100>		<110>	
Polarity	$\pi_{\parallel}$	$\pi_{\perp}$	$\pi_{\parallel}$	$\pi_{\perp}$
	π_{11}	π_{12}	$(\pi_{11}+\pi_{12}+\pi_{44})/2$	$(\pi_{11}+\pi_{12}-\pi_{44})/2$
n - MOSFET	-42.6/ -102	-20.7/ 53.4	-35.5 / -31.6	-14.5 / -17.6
p- MOSFET	9.1/ 6.6	-6.2/-1.1	71.7/ 71.8	-33.8 / -66.3

MOSFET / bulk

(110) wafer	<110>	
Polarity	$\pi_{\parallel}$	$\pi_{\perp}$
	$\pi_{22}=(\pi_{11}+\pi_{12}+\pi_{44})/2$	π_{12}
p- MOSFET	58.0/ 71.8	38.2 / -1.1

(a)

Table1 The Measured long p- and n-channel MOSFET piezoresistance coefficients for (001) and (110) wafers compared to bulk Si piezoresistance [15]



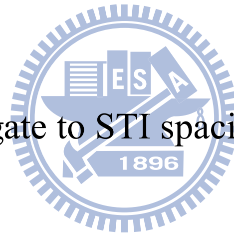


Fig.12 The Vth shfit due to gate to STI spacing (A) induced stress.

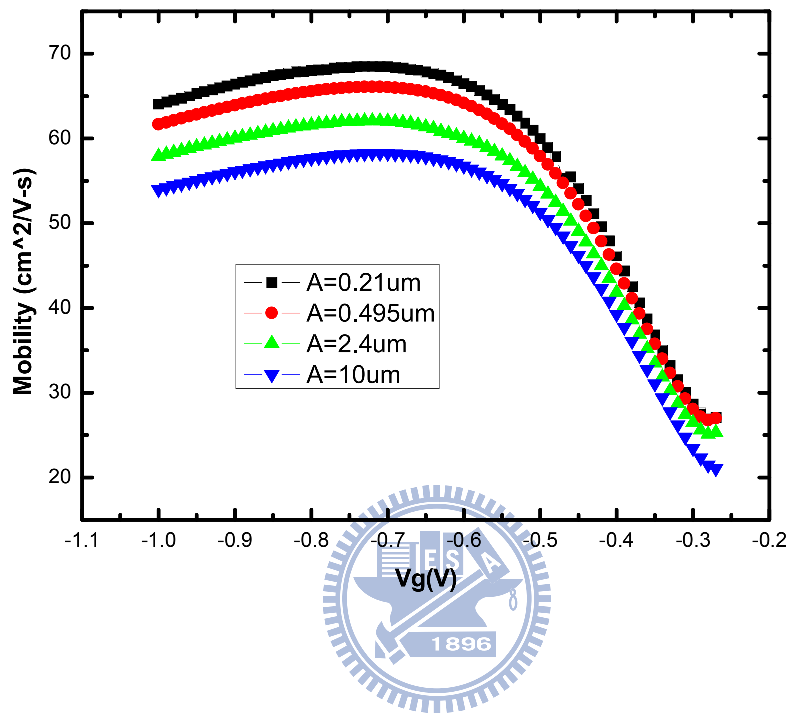


Fig.13 The mobility shift due to gate to STI spacing (A) induced stress.

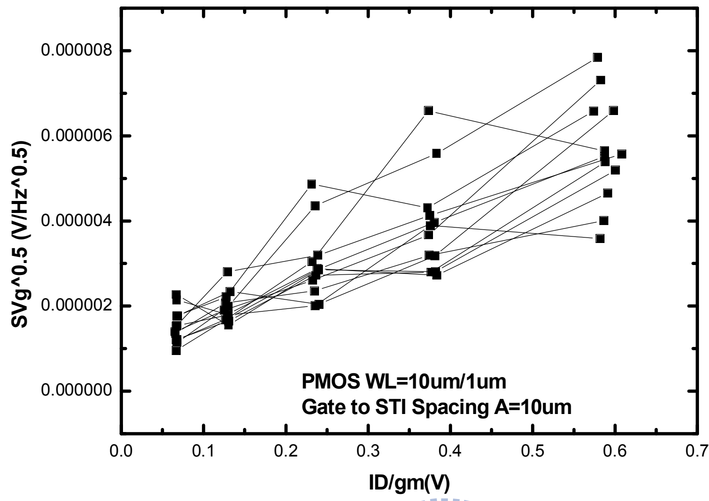


Fig .14 measured $Svg^{0.5}$ varies Id/g at 25Hz with spacing A=10um.

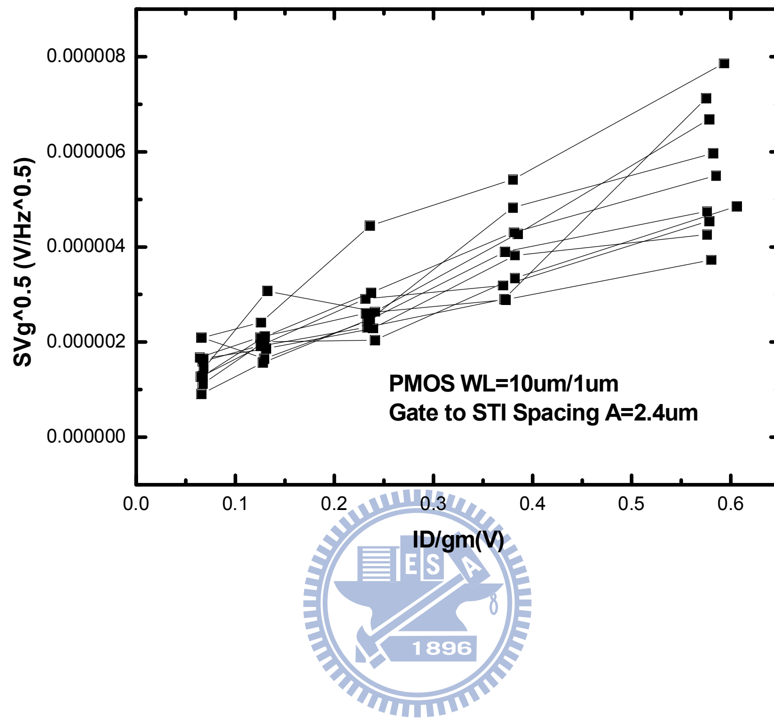


Fig .15 measured Svg$^{0.5}$ varies Id/g at 25Hz with spacing A=2.4um

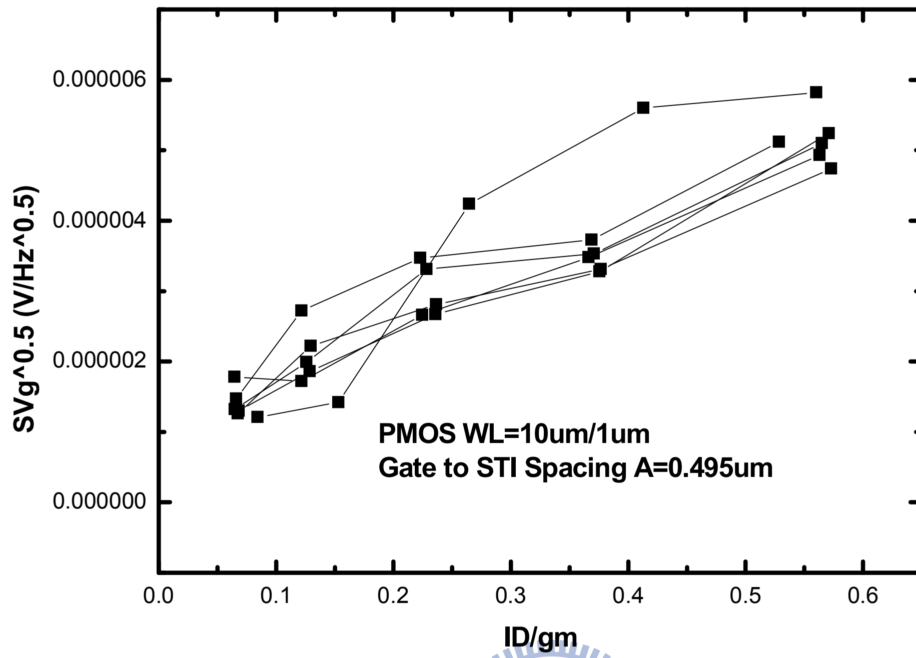
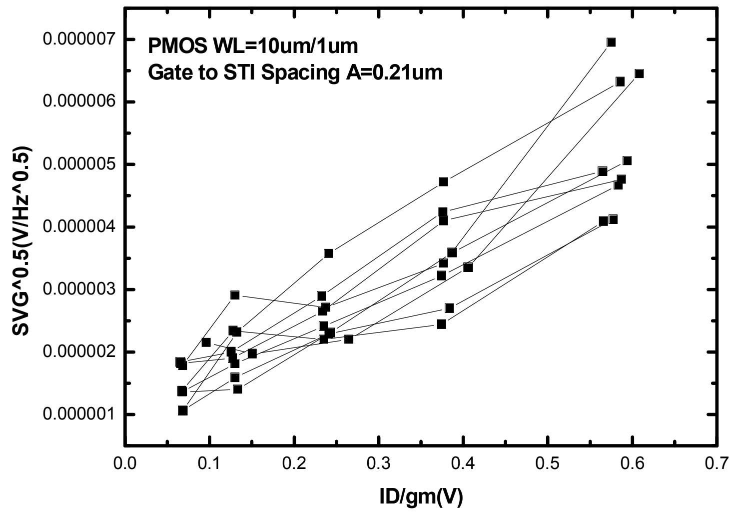


Fig .16 measured $Svg^{0.5}$ varies Id/g at 25Hz with spacing A=0.495um



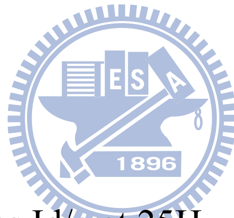


Fig .17 measured $Svg^{0.5}$ varies Id/g at 25Hz with spacing A=0.21um.

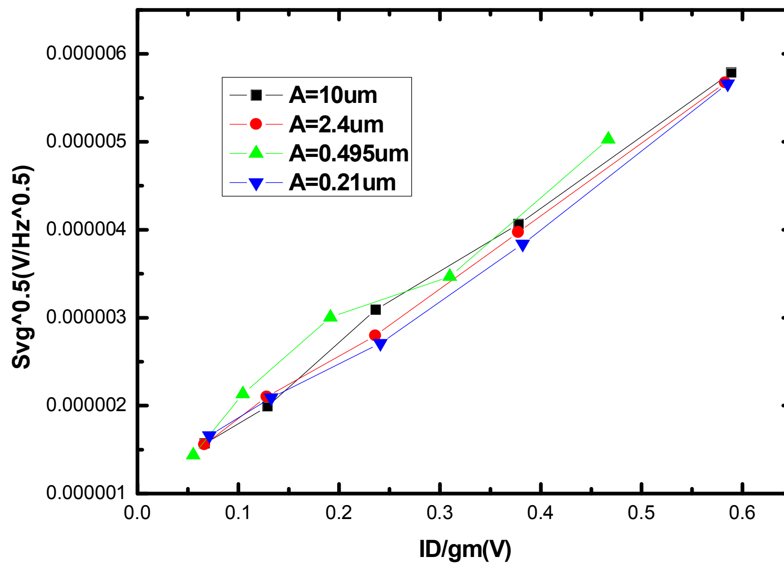


Fig.18 The fittings used line for extracting the trap density Nt ($cm^{-3}eV^{-1}$) and scattering factor α (Vs/C)

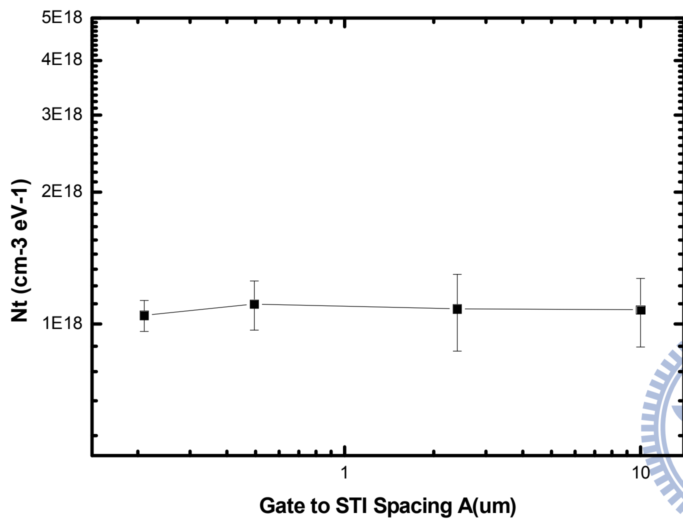


Fig.22(a)

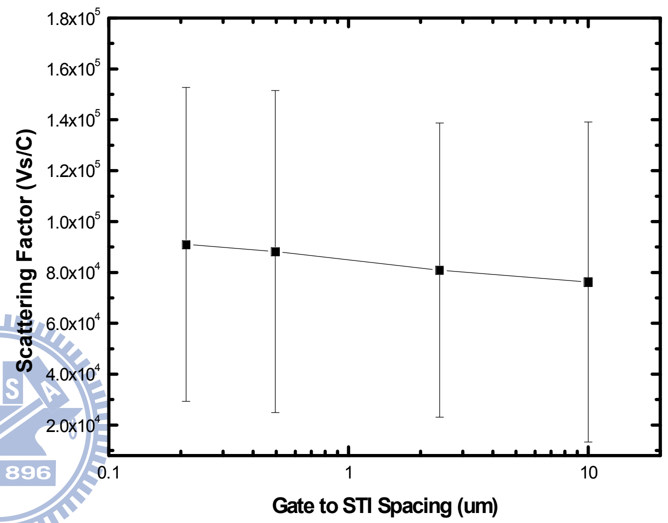


Fig.22(b)

Fig.19(a) The trap density Nt($cm^{-3}eV^{-1}$). (b) the scattering factor α variation. Varies gate to STI Spacing

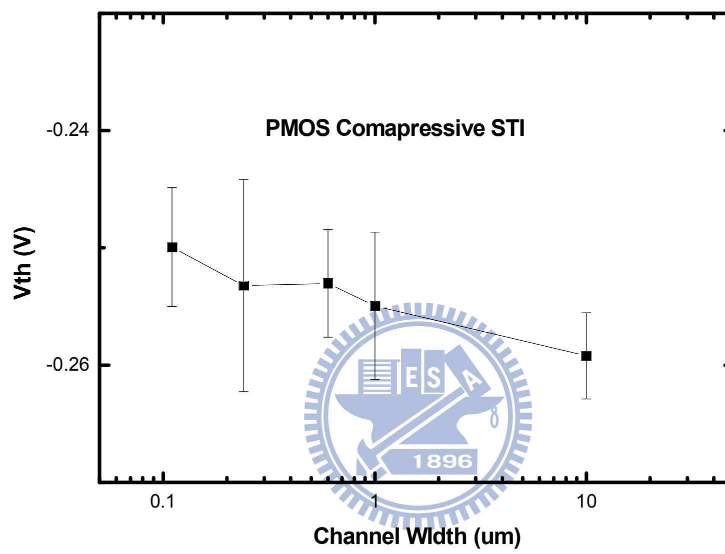


Fig 20 The Vth shift in narrow device, at L=1um,W=10,1,0.6,0.24, and 0.11um,

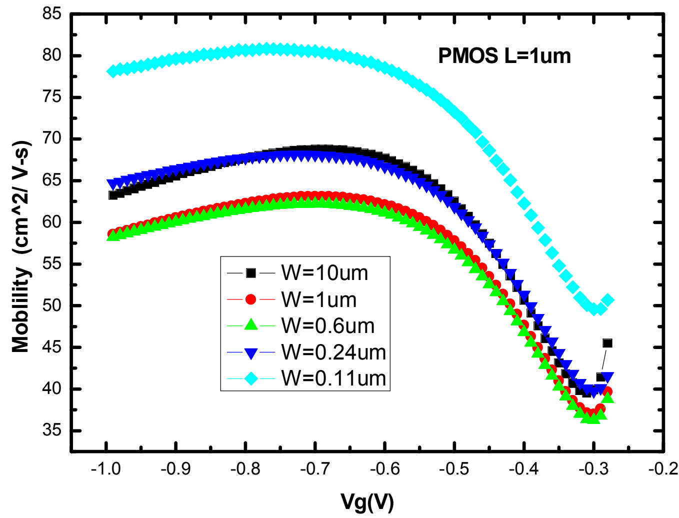


Fig.21a The mobility varies gate voltage of five device (W=10,1,0.6,0.24,0,11um), L=1um.

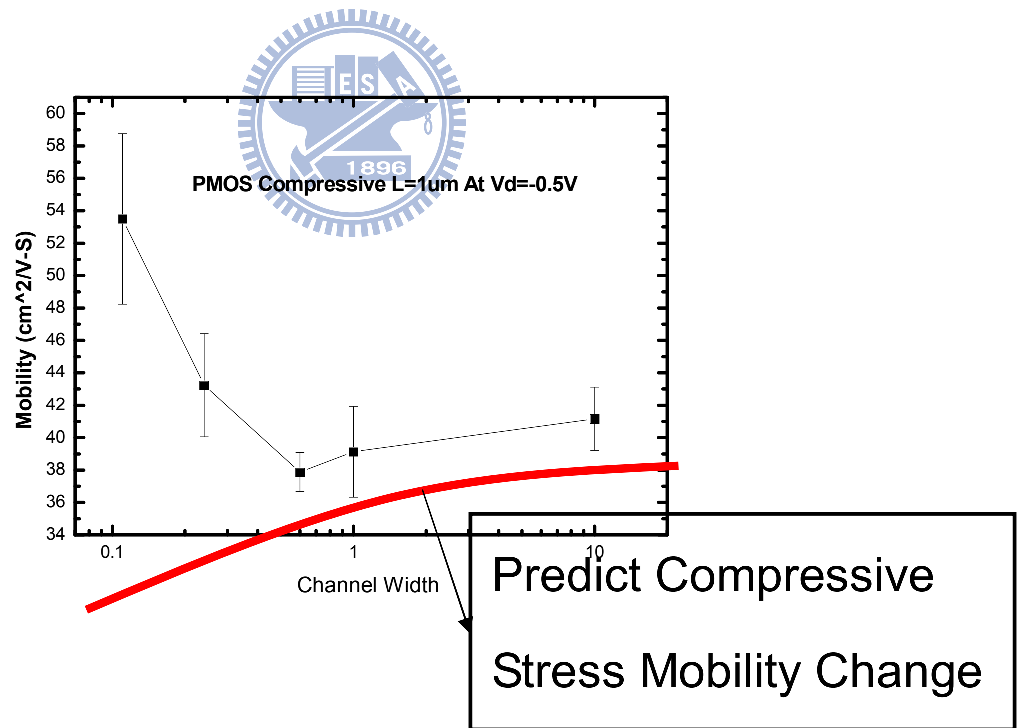


Fig.21b The anormal mobility shift in narrow devices.

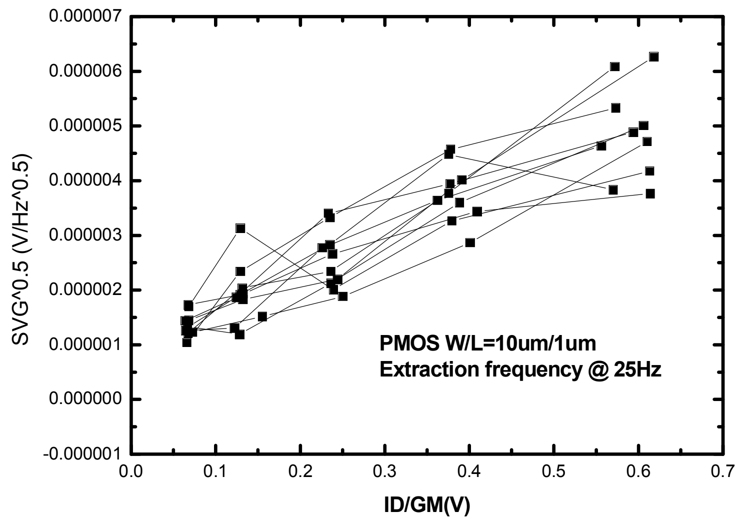


Fig 22a measured $Svg^{0.5}$ varies Id/gm at 25Hz with W=10um.

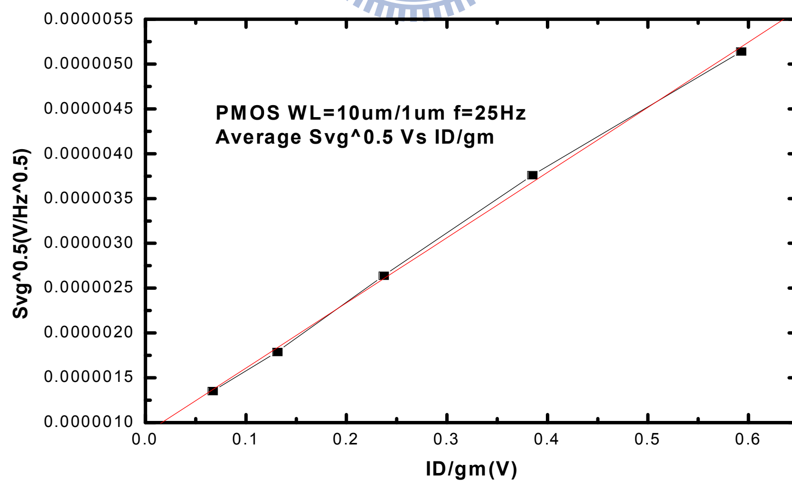


Fig 22b The fitting line at 25Hz with W=10um

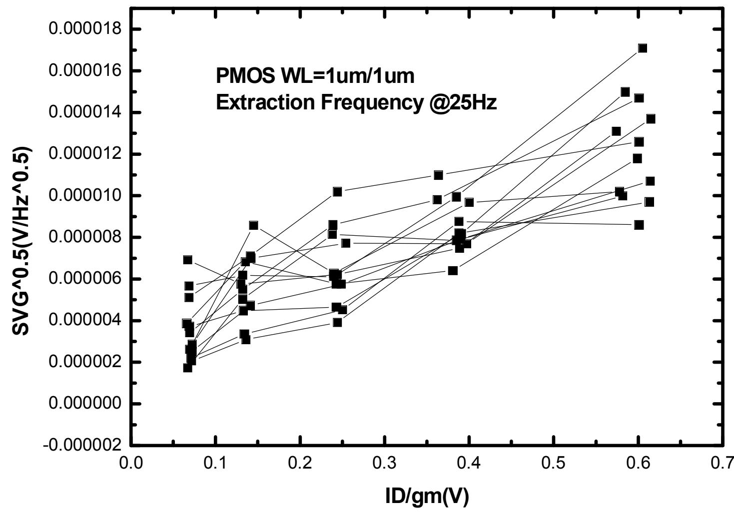


Fig 23a measured Svg$^{0.5}$ varies Id/gm line at 25Hz with W=1um.

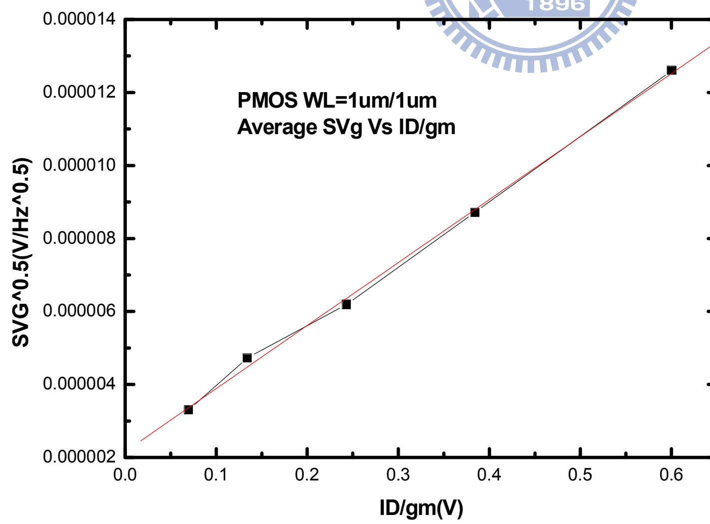


Fig 23b The fitting line at 25Hz with W=1um.

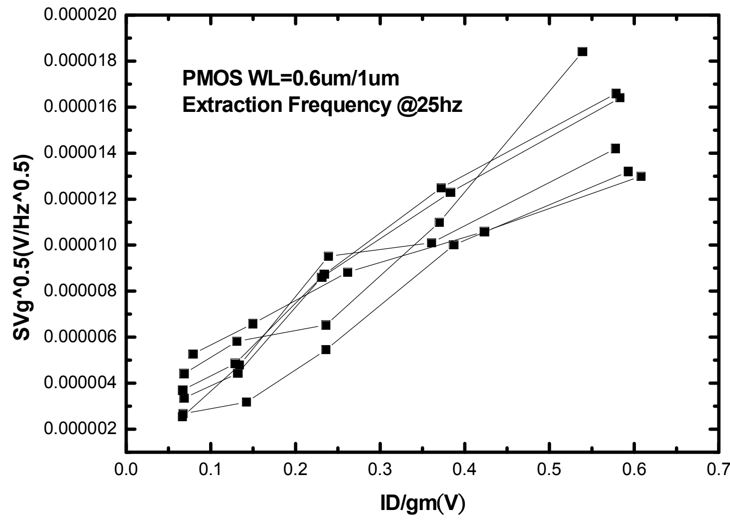
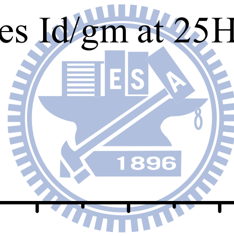


Fig 24a measured $Svg^{0.5}$ varies Id/gm at 25Hz with W=0.6um



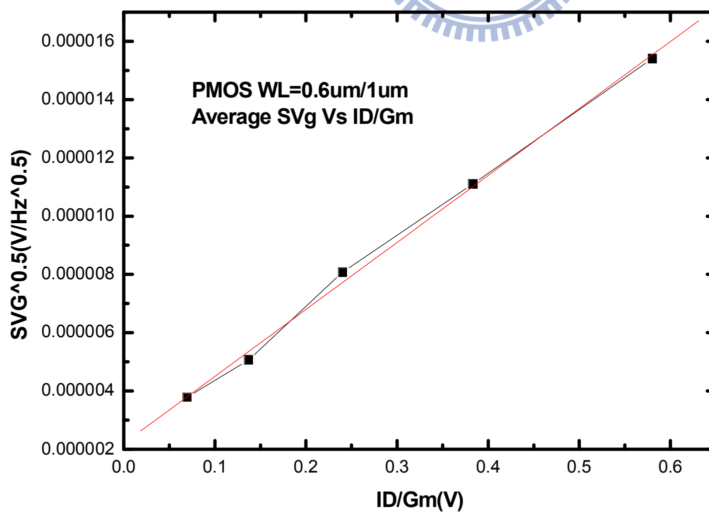


Fig 24b The fitting line at 25Hz with W=0.6um

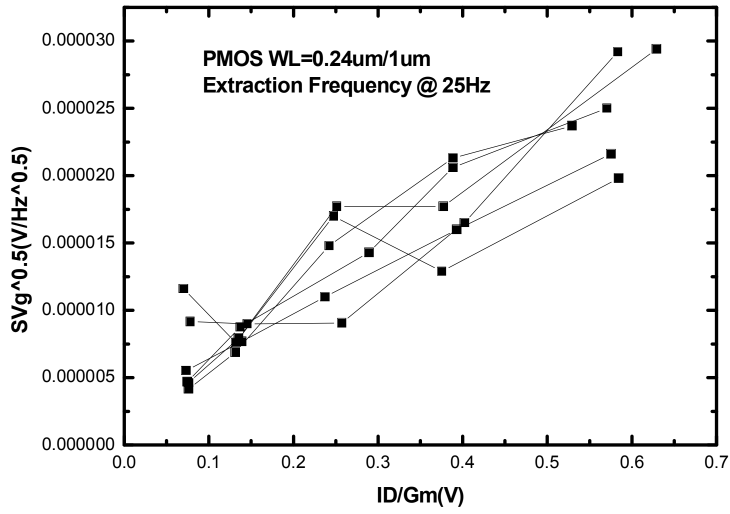


Fig 25a measured $Svg^{0.5}$ varies Id/gm line at 25Hz with W=0.24um

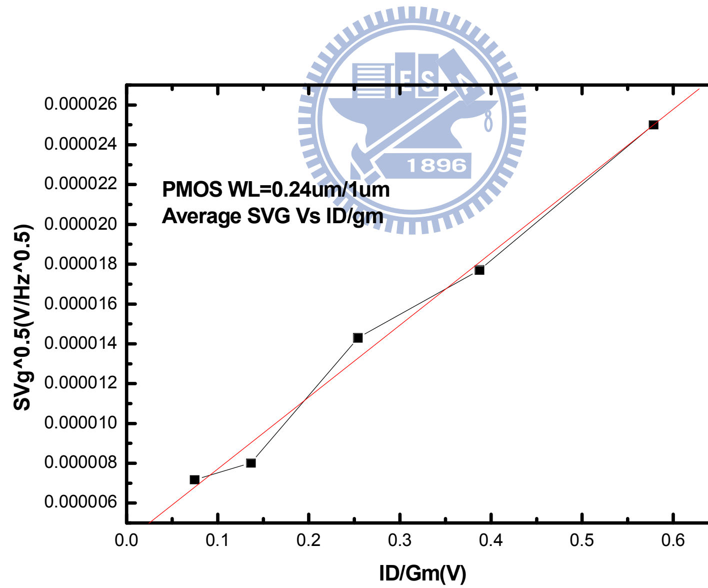


Fig 25b The fitting line at 25Hz with W=0.24um

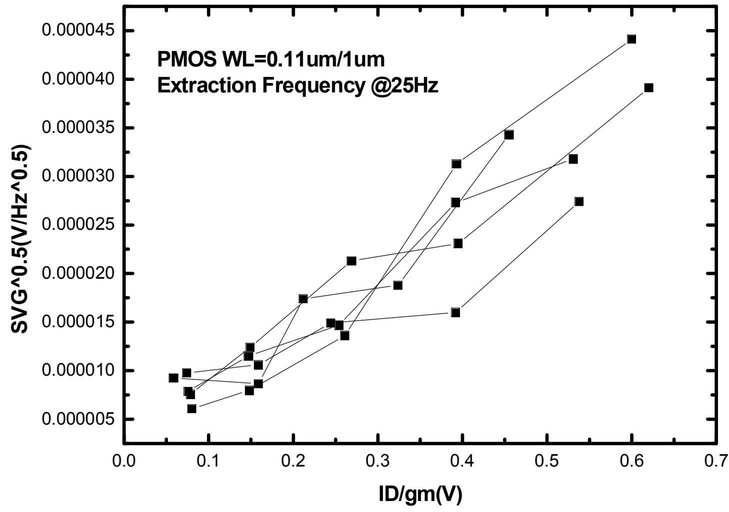


Fig. 26a measured Svg$^{0.5}$ varies Id/gm at 25Hz with W=0.11um

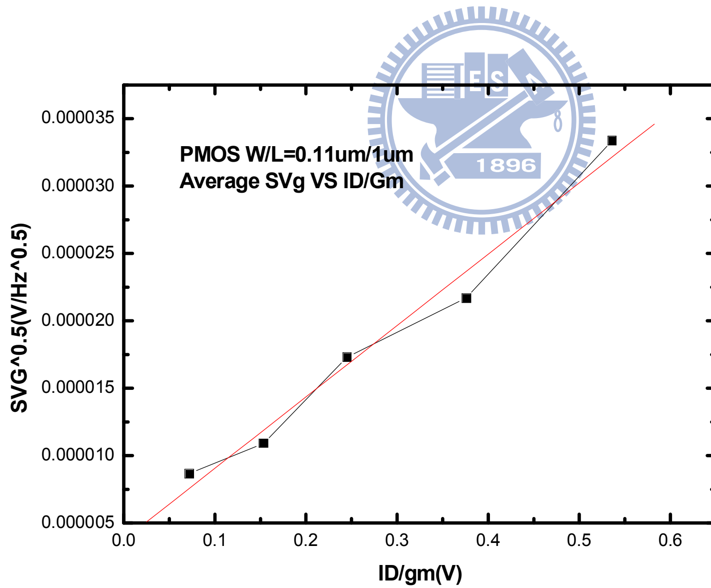


Fig. 26b The fitting line at 25Hz with W=0.11um

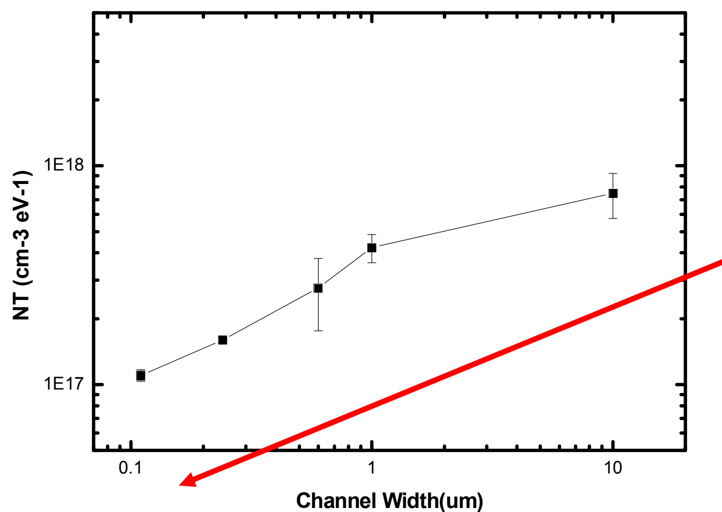


Fig.27a The Trap density Nt variation in narrowing devices.

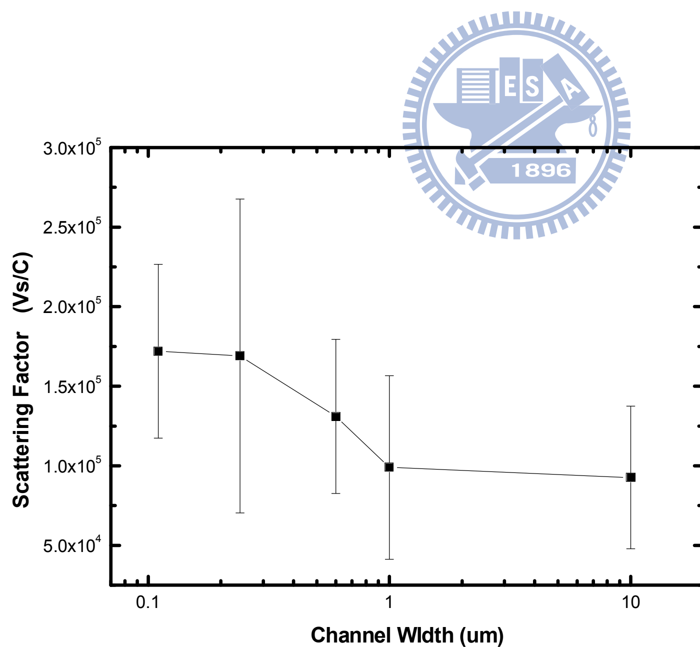


Fig.27b The scattering factor α variation in narrowing devices.