國 立 交 通 大 學

電子工程學系　　電子研究所

碩士論文

氟化製程應用於金氧半場效電晶體鈍化層之特性與研究

Characteristics and Investigation of FSG Passivation Layer on HfO_2/SiON Gate Stack MOSFETs

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摘要

根據2008 ITRS PIDS Meeting所訂出最新金氧半場效電晶體之閘極奈米尺寸的演變趨勢，因受到新穎閘極材料無法持續之前最低可容忍漏電流規範，使得高效能和低功率應用的奈米微電子元件需延緩三或五個製程世代，本文中提出與現有製程具高度匹配性的四氟化碳電漿處理(CF_4 plasma treatment)技術，利用氟化矽玻璃(FSG)當n型金氧半場效電晶體鈍化層的製程，在最後Sintering修補金屬界面斷鍵過程中，使氟原子有效擴散至高介電閘極本體和通道界面處，實驗結果顯示元件的電特性和可靠度可藉由通入適量的CF_4氣體達到明顯的改善，因此

可改善遷移率衰退以提昇驅動電流表現、較低次臨界擺幅和閘極漏電流、閘極引起汲極漏電流有明顯降低輸出等。

此外也分析可靠度劣化程度，在正偏壓-溫度應力(PBTS)和熱載子應力(HCS)可靠度特性上都有改善的效果，觀察到在電壓應力破壞下，均有較小的臨界電壓的偏移、較少的本體電子捕捉與界面狀態密度改變而引起元件的不穩定性，且在正電壓應力(PBS)與熱載子應力比較之下，熱載子應力造成的可靠度衰減相較於正電壓應力有顯著嚴重趨勢。這些元件電特性獲得改善及具有高度穩定性的可靠度呈現，造成的原因是來自於氟原子併入高介電閘極主體以及閘極層與通道界面間，不僅僅可減少界面狀態的懸空鍵結(interface dangling bond)和較低界面狀態產生，且進一步有效減少高介電閘極主體電荷捕捉情形。

最後在應力測試後再進行回復(relaxation)的行為，可分離HCS是由cold和hot載子兩個成份構成熱載子應力引起臨界電壓的偏移效應，其中cold載子具有逃逸(de-trapping)特性而hot載子會殘留在介電層形成永久傷害，不管在PBS或是HCS的回復行為，明顯觀察到氟化鈍化層元件有較少載子捕捉情形(應力下)及較高逃逸能障使得有較少逃逸現象產生(回復下)，這與先前討論Frenkel-Poole傳導機制，其比一般鈍化層有較深的載子捕捉位置有好的關連性。

Characteristics and Investigation of FSG Passivation Layer on HfO_2/SiON Gate Stack MOSFETs

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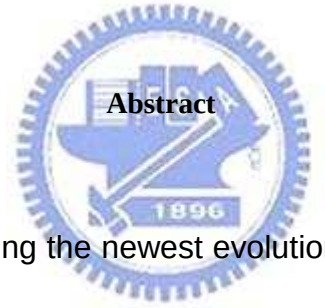

Abstract

According to establishing the newest evolutionary trend for the gate nano scale of MOSFETs from ITRS PIDS Meeting in 2008 year, the nano microelectronic devices applied high performance and low power function circuits must put off three or five process generation because the novel gate materials can be unable to sustain the criterion of the least gate leakage current tolerably previous works. A process-compatible CF_4 plasma treatment technique for fabricating fluorinated silicate oxide (FSG) as a passivation layer of n-MOSFETs is demonstrated in this work. Fluorine was effectively diffused into the high-k gate dielectric and the interface between channel and gate

dielectric during sintering step. Experimental results reveal that remarkably improved device performance and reliability can be achieved with appropriate CF_4 gas introduced. Thus, the electrical characteristics improvement exhibits driving current enhanced due to mobility improvement, good subthreshold slope, low gate leakage current, obviously reduced GIDL current and so on.

In addition, the fluorinated P.L. (the abbreviation of passivative layer) also improves the device reliability with respect to positive bias temperature stress (PBTS) and hot-carrier stress (HCS). We observe that less threshold voltage shift, less generated bulk trap density and interface state density shift during voltage stressing, which suppressing the instability characteristics due to device damage. For n-MOSFET devices with TEOS P.L. or FSG P.L., compared PBS and HCS, we find that the HCS phenomenon on reliability degradation is more serious than PBS. It shows the improvement of electrical characteristics and good stability as well as reliability in devices for FSG P.L. as a result of the fluorine atoms incorporated into high-k gate dielectric and the interface between gate dielectric and channel, which not only reducing interface dangling bonds and lower generation rates of interface states, but also effectively lowering carrier trapping in high-k dielectric further.

Finally, the relaxation behavior after hot carrier stressing test could

separate cold carrier from hot carrier, which the effect of total threshold voltage shift coming of cold and hot carriers. The cold carrier contribution is shown to be reversible while hot carrier trapping induces permanent damage of the dielectric. It is clearly noted for devices of fluorinated passivation layer that less carriers are captured in high-k bulk dielectric and interface (stress cycle) but less captured carriers take place de-trapping behavior due to higher de-trapping barrier height (relaxation cycle). As observed above, it shows a good correlation between F-P transport mechanism and de-trapping behavior that the position of carriers trapping for FSG P.L. are deeper than that for TEOS P.L..

誌　　謝

隨著實驗進度和成果一天一天的完成，也代表在交大校園的碩士生涯將慢慢地告一段落，雖然在實驗、生活和各方面上協助過我的人許多為一面之緣，但是你們的熱忱和愛心讓小弟不得不先和你們致上深深的敬意。再來，能順利完成這個學位，當然要非常地感謝我的兩位指導教授–羅正忠博士及邱碧秀博士，他們在實驗研究與論文上不但給予充分詳實的指導與鼓勵外，也讓我從他們身上學到很多寶貴知識和學問，更重要的是，學到老師處理事情的態度和方法，讓我深刻感受到在實驗研究應該朝勤奮不懈、實事求是及結合最新科技新知與技術的研究精神去努力外，還要懂得在社會上為人處事與永遠保持接受新事物和挑戰的心態去迎接未來的大小考驗。

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CHAPTER 01

Introduction to High-k Gate Dielectrics

1.1 General Background

In order to provide better performance and higher packing density on the limited space, scaling down of the channel length is essential in ULSI fabrication technologies [1-2]. One of the main scalling issues in the advanced CMOS devices in the sub-100 nm regime is the thinning of gate oxide that is required for higher drive current and to improve the gate control over the channel, which reduces the short channel effects [3-4]. When dielectric (SiO_2) thickness approaches 1 nm in CMOS devices scale, new materials such as high-k dielectrics and metal gate electrodes are required [5-6]. According to the ITRS roadmap, the SiO_2 gate dielectric film thickness should be scaled down to 1.0 nm for 35nm technology node. Such an ultra-thin SiO_2 film consists of only a few atomic layers, causing a considerably large direct-tunneling current through the film, as dictated in Equation (1-1) and in turn resulting in significant increase of power consumption. The direct tunneling current which depends on physical film thickness will cause an intolerable level of off-current, resulting in huge power dissipation and heat.

$$I_{DT} \propto [\exp - \sqrt{\frac{2mq\phi}{(h / 2\pi)^2}} T_{phys}] \qquad (1.1)$$

When it comes to leakage, it eventually degrades overall power consumption described as Equation (1-2).

$$p = ACV^2 f + VI_{leak} \quad (1.2)$$

A is the fraction of gate actively switching and C is the total capacitance load of all gate. The dynamic power component ($ACV^2 f$) and static power component (VI_{leak}) defines overall power consumption. As gate oxide is scaled down further, static power consumption will exponentially increase due to source of leakage such as gate oxide leakage and subthreshold leakage current (see Fig. 1.1). High-k materials have been shown to reduce the tunneling leakage current (i.e., suppressing gate oxide leakage and subthreshold leakage current), further reducing static power consumption, and metal electrodes are needed due to their better comparability with high-k dielectrics and absence of the depletion efffect. In order to meet the ITRS (International Technology Roadmap for Semiconductor) 2008 requirements, Table 1.1 [7], replacing polysilicon by metal gates is critical.

On the trace to the physical limit, the scaling of CMOS technology is reluctant to depart far away from the Moore's Law. The famous “Moore’s Law”, proposed by Gordon Moore in 1965, states that the number of transistors on integrated circuits doubles every 24 months. For the past four decades, the advancement in the IC industry more or less follows this intelligent foresight in its pursuing better performance with lower cost. It can be said that “Moore’s Law” is the

basis for the overwhelmingly rapid growth of the computing power. In order to keep close pace with "Moore's Law", the shrinkage of the transistor dimension is needed. Fig. 1.2 illustrates how the number of metal oxide semiconductor field effect transistors (MOSFETs) in Intel processors has increased historically [8].

According to the first order current-voltage relation in Equation (1-3) and (1-4), the driving current of a MOSFET can be given as

$$I_{D,sat} = \frac{1}{2} C_{gs} \mu_n \frac{W}{L_{eff}} (V_{GS} - V_{Th})^2 \qquad (1.3)$$

$$C_{gs} = \frac{k \varepsilon_0 A}{T_{inv}} \qquad (1.4)$$

Where V_{GS} is the applied gate to source, L_{eff} is the effective channel length, W is the channel width, V_{Th} is the threshold voltage, μ_n is the mobility for electrons, C_{gs} is the gate capacitance, k is the dielectric constant, ε_0 is the permittivity of free space and T_{inv} is the electrical film thickness. In an attempt to improve the current drivability of a MOSFET, all parameters contained in the above formula can be accordingly adjusted. With reduced threshold voltage, smaller effective channel length, and increased gate capacitance as well as gate-to-source voltage, we can achieve better current drivability and higher device density, which mean a better performance and much more transistors on the chip. However, some approaches will bring about serious drawbacks, and for instance, a large V_{GS} will degrade the reliability while too small a V_{Th} will result in statistical fluctuation

in thermal energy at a typical operation circumstance of up to 100 °C. So a bigger C_{gs} and shorter L_{eff} will be needed to maintain device performance.

In the front-end process area, there remain many technological challenges to be overcome to achieve further scaling and growth of the industry [9]:

- ◆ New gate stack processes and Materials
- ◆ Surfaces and interfaces control
- ◆ CMOS integration of new memory materials and processes
- ◆ Critical dimension and effective channel length control
- ◆ Scaled MOSFET dopant introduction and control

In this chapter, the first challenge will be discussed in detail because the challenge are the key motivation to this Thesis.

1.2 Motivation

Polysilicon gate and SiO_2 gate dielectric for the MOSFET devices have been perfect materials throughout MOSFET history till now. However, as the device dimension shrinks into deep sub-micron regime, SiO_2 as a gate oxide is facing serious challenges which seem to be almost impossible to overcome. As shown in Fig. 1.3, we can see that when the gate oxide thickness scales down to 2 nm, the leakage cureent will exceed the limit of 1A/cm^2 set by the allowable stand-by power dissipation. Further scaling of oxide thickness to below 2 nm, the direct tunneling current will increase exponentially, causing

intolerable power consumption. For easily sensing the seriousness of leakage problem: as SiO_2 thickness is reduced, leakage current increases exponentially (~10x/2Å) [10]. In addition, reliability issues become a serious concern for such a thin SiO_2 dielectric only 10-15Å thick. It points out that SiO_2 thickness uniformity across a 12 inch wafer imposes even more crucial difficulty in the growth of such a thin film, since even a mono-layer difference in thickness represents a large percentage difference and thus can result in the variation of threshold voltage (V_{Th}) across the wafer. To circumvent these problems, high-k dielectrics have been investigated extensively as possible replacement to the SiO_2 film as gate insulators.

By using gate dielectrics with higher dielectric, electrically equivalent oxide thickness (EOT) in order to maintain the same gate capacitance can be obtained with a thicker physical thickness. Therefore, the quantum direct tunneling gate leakage current can be significantly reduced, as shown in Fig. 1.4. Selecting a gate dielectric with a higher permittivity than that of SiO_2 is a clearly indispensable to extend the lifespan of the famous Moore's law. From (1.3), we can notice that the current drivability is strongly related to the electrical thickness of the gate oxide, while, from (1.2), the leakage is related to the physical thickness of the gate oxide. In order to maintain the same C_{gs} value, (1.4) can be rewritten as follows (1-5) :

$$T_{high-k} = \frac{k_{high-k}}{k_{ox}} EOT = \frac{k_{high-k}}{3.9} EOT \qquad (1.5)$$

Where the term *EOT* represents the theoretical thickness of SiO_2. So by increasing the gate dielectric constant, the same equivalent oxide thickness can be obtained with a thicker physical thickness, which in turn contributes to the reduced gate leakage current (i.e., direct tunneling), without sacrificing the performance. Also the reliability issues become a huge concern for this thin regime of SiO_2 film because the direct tunneling electrons make it more vulnerable for given conditions and eventually cause a possible threshold voltage fluctuation or even dielectric breakdowns of devices, which result in a malfunction or failure of device [11]. Therefore, searching a material with a high dielectric constant to replace SiO_2 is urgently needed.

Lately there has been increased interest in the possibility that fluorine might help protect devices against negative bias temperature instability (NBTI) [12]. It has been shown that the presence of fluorine improves the lifetime of devices under such conditions. Since NBTI has emerged as one of the main reliability issues for today's ultrathin oxides, this improvement is particularly significant. Fluorine is one of the extrinsic species that can be found in microelectronic devices. It is usually introduced through the use of a molecular precursor or by direct implantation of F ions [13-16]. The presence of fluorine in devices has been known to have certain beneficial effects on their operation, such as hot-carrier immunity [15], improved dielectric integrity [16], and reduced flicker noise [14]. In conventional, fluorine ion implantation (FII) technique is mostly adopted to introduce

fluorine atoms into the poly-Si or silicon substrate channel. However, this method may be not suitable for large-area electronics. Moreover, a subsequent high temperature process is required to activate implanted fluorine atoms and recover the damage created by implantation. It is known that excessive fluorine annealing replaces Si–O bonds with Si–F bonds, which generates reactive oxygen atoms. The oxygen atoms, which react with silicon substrate, form thick interfacial SiO_x layer [17-18]. Consequently, these processes can cause additional damage due to the high energetic ion implantation. To minimize damage, effective and process-compatible techniques to introduce fluorine atoms into high-k gate dielectric stacks are needed to be developed. In the latter chapters, we will present improvement results for the new process-compatible fluorination technique that is critical to the role of fluorine in the operation of high-k gate dielectric stacks devices.

1.3 Recent High-k Gate Dielectric

1.3.1 Criteria for High-k Gate Dielectrics

There are couples of key issue to select proper high-k dielectric material. The first one is that although the k value should be as high as possible, however, it should not be too high, otherwise it could result in degradation of the electrical properties due to increased fringing field from the gate to the source/drain of the transistor, i.e., field induced barrier lowering (FIBL) which degrade short channel

effects of MOSFETs [19]. On the same token, the k value should not be too low, otherwise it defeats the whole purpose of substituting for high k materials. Secondly, thermal stability of materials with silicon and its interface quality are important. For all thin gate dielectrics, the interface with Si substrate plays a key role, and in most cases is the dominant factor in determining the overall electrical properties. Therefore, the high-k materials require an interfacial reaction barrier to minimize the undesirable reactions with Si substrate. In addition, Figure 1.5 shows the characteristics of oxygen diffusion through high-k dielectric materials [20]. Due to the rapid oxygen diffusion, an additional interfacial layer forms between the high-k dielectric and Si substrate. But, this interfacial layer is obviously not helpful to scale down the device size because of its low permittivity. Therefore, proper capping technology might be required to avoid undesired interfacial reaction with high-k dielectric. Thirdly, the higher band offset indicates that the carriers (i.e., electron or hole) are less likely to be injected from the anode or cathode into a dielectric film. Fourthly, Gate and fabrication process compatibility need to be considered. The structural approach of conventional poly-silicon gate electrode on high-k material does not seem to be a good method any more. A poly depletion effect results in increase of EOT [21-22]. Boron diffusion through high-k dielectric degrades V_{Th} instability and reliability characteristics [22]. Moreover, Fermi level pinning characteristic affects narrow down of on-off margin in operation voltage of CMOS

[23]. Finally, the electrical reliability of new high-k dielectric must also be considered critical for application in CMOS technology. Whether or not a high-k dielectric satisfies the strict reliability criteria is still under investigation, and many areas of these studies are not well understood yet. However, a few preliminary projections for reliability such as stress induced leakage current (SILC), time-dependent dielectric breakdown (TDDB), bias temperature stress (BTS) appear to be encouraging for adopting high-k material as a future gate dielectric.

The high-k materials as advanced gate dielectric to replace conventional SiO_2 should meet following properties :

1) High dielectric constant (12~60)
2) Large energy band gap (>5eV) and barrier height ($\phi_B > V_{DD}$)
3) Low leakage current at the operating voltage ($J < 10^{-3} A / cm^2 @ V_{DD}$)
4) Thermal stability on Si at high temperature
5) High crystalline temperature due to favorable amorphous phase
6) High resistance to oxygen and impurity penetration
7) Low interface states ($D_{it} < 10^{11} / cm^2 eV^{-1}$) with Si-substrate and low bulk charge (negligible hysteresis and frequency dependence)
8) Low EOT ($T_{inv} < 1\ nm$) and gate leakage current
9) V_{FB} and Hysteresis < 20mV
10) Less mobility degradation
11) No Fermic level pinning effect for high-k film contacting with

gate electrode, i.e., tunable work function of gate electrode

12) Compatibility with gate electrode material

13) Reliability (No charge trapping, TDDB>10years)

1.3.2 Challenges to High-k Technology

Compared with the conventional SiO_2 oxide and poly-Si electrode, the high-k oxides present many challenges in the context of compatibility with the Si MOSFET technology. In addition to incompatibility with annealing temperatures used for activating poly-gates, the relatively poor quality, compared to SiO_2, of the high-k oxide materials causes charge trapping and makes the Si MOSFET gate unstable. The channel mobility degradation, and threshold voltage shift induced by high-k materials also need to be addressed. The high-k gate layer has soft optical phonons and the long-range dipole associated with the interface excitations would degrade the effective electron mobility in the inversion layer of the Si substrate [24]. Yang et al. [25] summarized the effects of all of the scattering and degradation mechanisms on the inversion channel carrier mobility, as shown in Fig. 1-6. The mobility issue is complicated by the fact that mobility values demonstrate dependence on the gate stack EOT. Therefore, different process solutions may be needed for high performance (small EOT) and low power (greater EOT) applications. Process solutions yielding ~80% universal SiO_2 mobility have been reported only for EOT ~ 15 Å [26].

The threshold voltage (V_{Th}) shift of the poly-Si/high-k stack is another challenge that must be considered. Reliability characteristics of the Hf-based dielectric such as time dependent dielectric breakdown (TDDB), bias temperature instability (BTI), and hot carrier induced degradation (HCI) have been actively investigated in connection with expected application of these materials in the high-k gate stack. One of main issues for high-k gate stack is the charge trapping characteristics during reliability test. Initial observation of instability was studied through capacitance-voltage (CV) characteristics in flat-band voltage change and current-voltage (IV) change. Since electrons can be trapped and detrapped in the high-k dielectrics with a minimal residual damage to its atomic structure [27], a threshold voltage instability associated with electron trapping/detrapping in high-k layer can significantly affect the transistor parameters and complicate the evaluation of the effects of stress-induced defect generation phenomenon on the high-k gate stacks, which typically is not an issue in the case of SiO_2 dielectrics. Since those charge trapping affect significantly on V_{Th} measurement and reliability characteristics, comprehensive study is required to detail understand.

1.4 Overview of Enhancing Robustness by Fluorine

Silicon oxide is the insulator of CMOS, and it normally has few defects. At $Si:SiO_2$ interfaces, the defect density is further lowered by

hydrogenation, with any Si dangling bonds P_b centers converted to Si–H bonds. Historically fluorine incorporation into gate dielectric is known as an effective way to passivate the interface traps in the conventional SiO_2 gate dielectric and it can improve device reliability because it was known that fluorine incorporation in the SiO_2 gate dielectrics replaces Si–H bonds with Si–F bonds, Si-F bonds rather strong than Si-H bonds. But the high-k oxides itself exist more much bulk trap charges than silicon oxide and suffer from a high density of charge traps. This causes transient instability of the gate threshold voltage, coulombic scattering of carriers in the Si channel, and possible reliability problems. Recent work indicates that the main charge trap is the oxygen vacancy V_O [28]. The high-k oxides differ from Si:H or SiO_2, that is, they all have ionic bonding. As a result of implanted fluorine that was found to have a large beneficial effect on charge trapping [29-31], F was found to substitute at the V_O site and passivates it. Thus F is one of the best passivant for defects in an ionic oxide because it is the only element that is more electronegative than oxygen and its bond length is similar. It can improve both the device performance and also reliability by way of F to passivate vacancies in ionic oxides such as HfO_2 because vacancies are more likely to be charged.

However, an excess amount of F incorporation increases oxide thickness. It is known that excessive F annealing replaces Si–O bonds with Si–F bonds, which generates reactive oxygen atoms. The oxygen

atoms, which react with silicon substrate, form thick interfacial SiO_x layer [17-18]. Moreover, another drawback after an excess amount of fluorination is a net negative charge observed at the high-k oxide and interfacial layer interface such as HfO_2/SiO_2, while also increasing the leakage current density [32]. The higher leakage current may also result in part from possible barrier height lowering for electron transport through the high-k oxide stacks. On the other hand, boron diffusion and penetration in thin gate oxide down to 17 Å with poly-Si gate have been the troublesome problem for p-type MOSFETs [33]. It shows even a moderate dose of F in SiO_2/Si with poly-Si gate such as significantly enhanced boron penetration through SiO_2 from P^+ poly-Si gate to substrate and an increase in the physical thickness of SiO_2 [34].

Therefore, tuning the F ion concentration at the HfO_2/SiO_2 interface may be an essential aspect of such a defect passivation scheme. Previous work studies suggest an insight into this problem. It was observed that the concentration of interstitial F ions was reduced by two orders of magnitude after a 400 °C FGA. Hydrogen annealings seem to be able to remove excess F ions which are not strongly bonded in the bulk region of the HfO_2 films [35].

1.5 Organization of the Thesis

This thesis consists of four chapters. The main topics are focused on the effects of fluorine incorporation into passivation dielectric of

n-MOSFETs with HfO_2/SiON gate stack, evaluated in terms of reliability and performances. We study systematically the electrical characteristics of HfO_2/SiON with FSG passivation dielectric, its reliability issues, and the behavior of charge trapping. In addition to this chapter that is dedicated to introduce the reason of the high-k dielectrics on CMOS technology and systematic discuss the effects of fluorine incorporating on MOSFETs wirh high-k gate dielectric stacks, this thesis is organized as follows :

In chapter 02, we describe the experimental procedure for fabricating n-MOSFETs test devices with HfO_2/SiON gate stack as well as FSG passivation dielectric. Fluorine profile and amount was modulated by CF_4-plasma gas flow into HfO_2 n-MOSFET. Then, show some basic electrical characteristics with and without FSG passivation dielectric, i.e., I-V and C-V characteristics, split C-V to obtain mobility, to evaluate the amount of interface states and bulk traps through charging pumping technique, and carrier separation to obtain leakage current mechanisms etc.

In chapter 03 presents the effects of FSG passivation dielectric on HfO_2 n-MOSFET reliability. Charge trapping characteristics, i.e., static PBTI and dynamic trapping analysis with stress dependent high-k film quality, threshold voltage, interface state and high-k bulk trap density shifts as indicating factors will be discussed. Besides, hot carrier reliability of the HfO_2/SiON dielectric with the FSG passivation dielectric is also investigated. Finally, the lifetime extraction based on

DC stress suggests that the high-k dielectric with FSG passivation dielectric can provide optimistic results.

In chapter 04, we conclude with summaries of the experimental results above and suggest the possible future researches in this area.

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Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
MPU Printed Gate Length (nm)	54	47	41	35	31	28	25	22	20
MPU Physical Gate Length (nm)	32	29	27	24	22	20	18	17	15
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 3E20-doped poly-Si	1.3	1.2	1.2	1	0.68	0.54	0.41		
Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for metal gate			1	0.95	0.88	0.75	0.65	0.6	0.53
Gate dielectric leakage at 100 °C (A/cm^2) bulk high-performance	180.0	450.0	650.0	830.0	900.0	1000.0	1100.0	1200.0	1330.0
Drain extension X_j (nm) for bulk MPU/ASIC	11	11	11	11	11	10	9	8.5	7.7
Allowable junction leakage for bulk MPU/ASIC (μA/μm)	0.06	0.13	0.25	0.48	0.71	0.7	0.64	0.69	0.72
Physical gate length low operating power (LOP) (nm)	38	32	29	27	24	22	18	17	15
Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for 1.5E20-doped poly-Si	1.3	1.2	1.1	0.7	0.7	0.6	0.5		
Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for metal gate			1.1	1	1	0.9	0.8		
Gate dielectric leakage at 100°C for bulk (A/cm^2) LOP	40.0	78.0	86.0	95.0	100.0	110.0	140.0		
Physical gate length low standby power (LSTP) (nm)	45	38	32	29	27	22	18	17	15.3
Equivalent physical oxide thickness for bulk low standby power T_{ox} (nm) for 1.5E20-doped poly-Si	1.9	1.2	1.1	1	0.9	0.8	0.7		
Equivalent physical oxide thickness for bulk low standby power T_{ox} (nm) for metal gate			1.5	1.4	1.3	1.2	1.1		
Gate dielectric leakage at 100°C for bulk (A/cm^2) LSTP	0.067	0.081	0.094	0.110	0.120	0.130	0.150		
Poly-Si or metal gate electrode thickness (approximate) (nm)	50	46	40	36	32	28	26	22	20

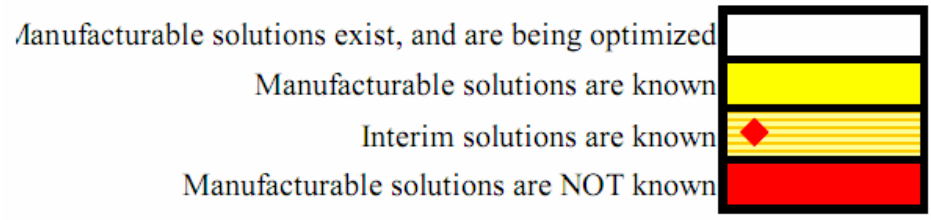

Table 1.1 2008 International Semiconductor Technology Roadmap predicts rapid reduction in the future technology trends for high performance logic, LOP, and LSTP devices.

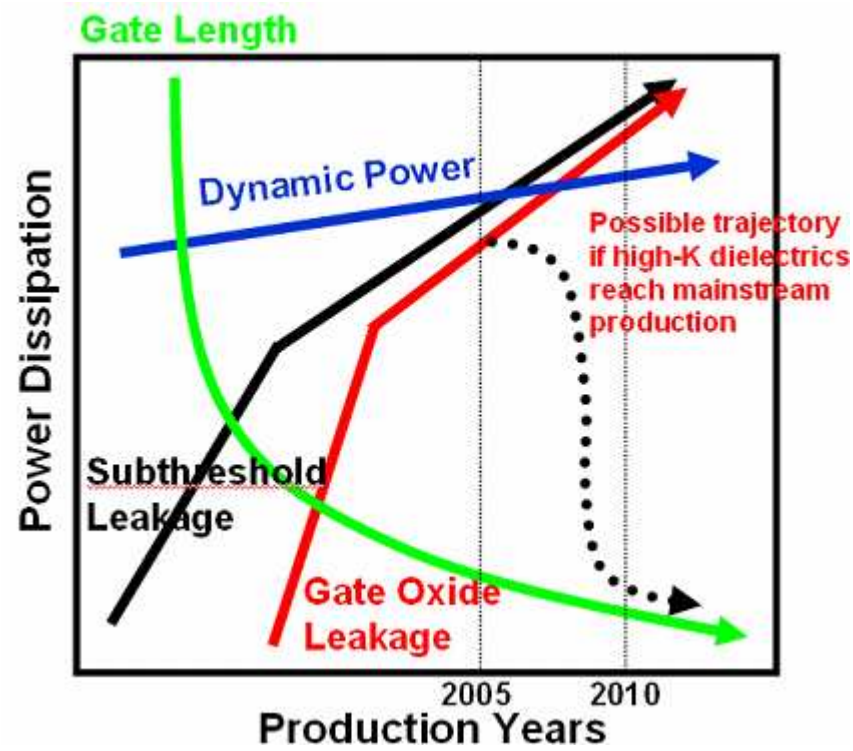

Fig. 1.1 Power dissipation (dynamic + static power) with each generation

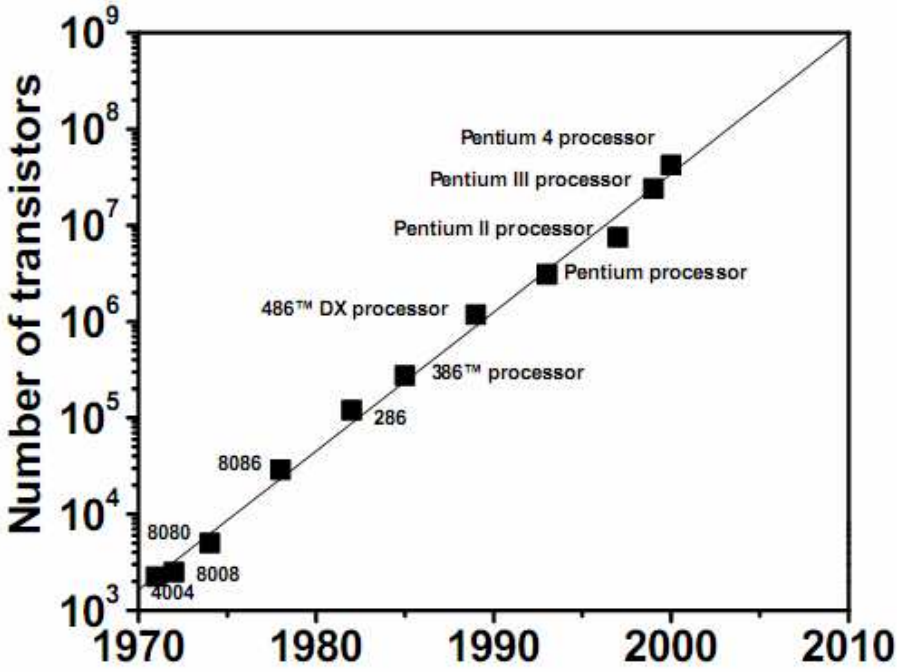

Fig. 1.2 The number of transistors in Intel processors increases exponentially over the years

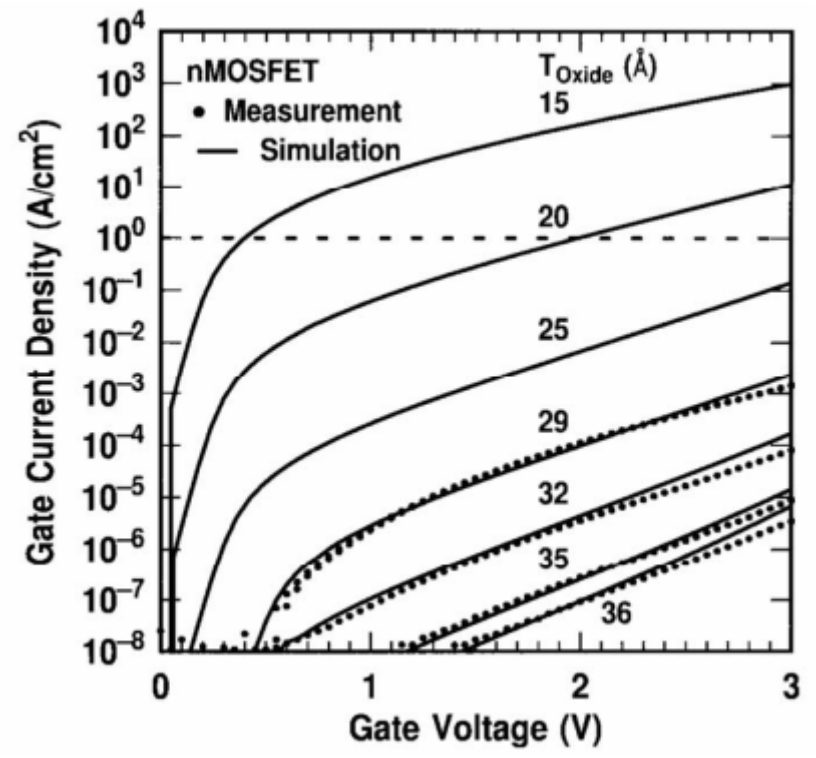

Fig. 1.3 Measured and simulated Ig-Vg characteristics under inversion conditions of SiO_2 N-MOSFET devices

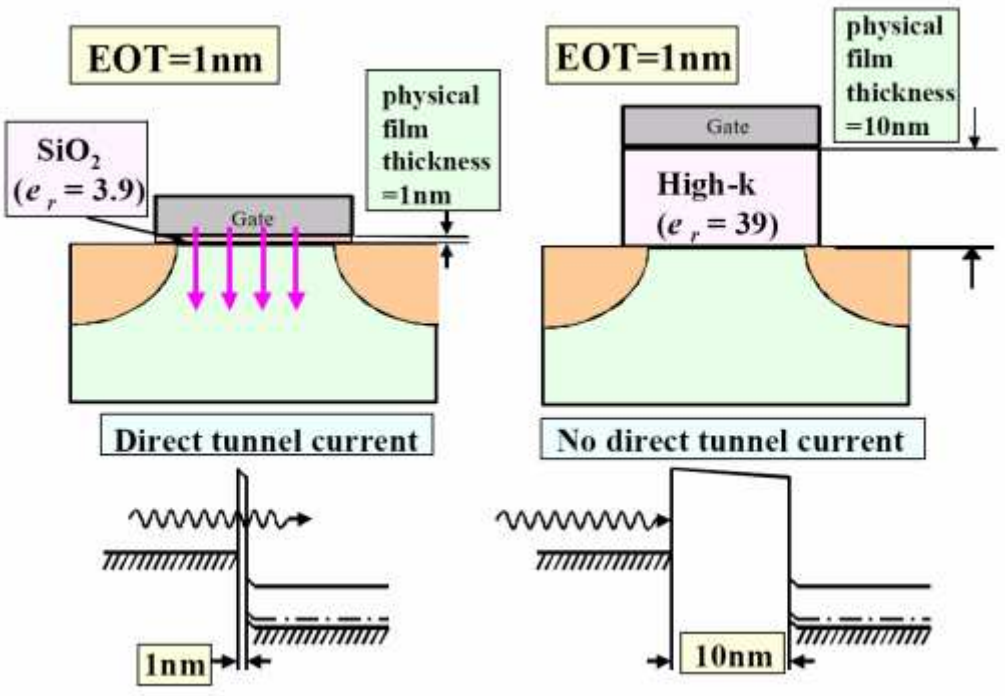

Fig. 1.4 By using high-k material to suppress gate direct-tunneling current.

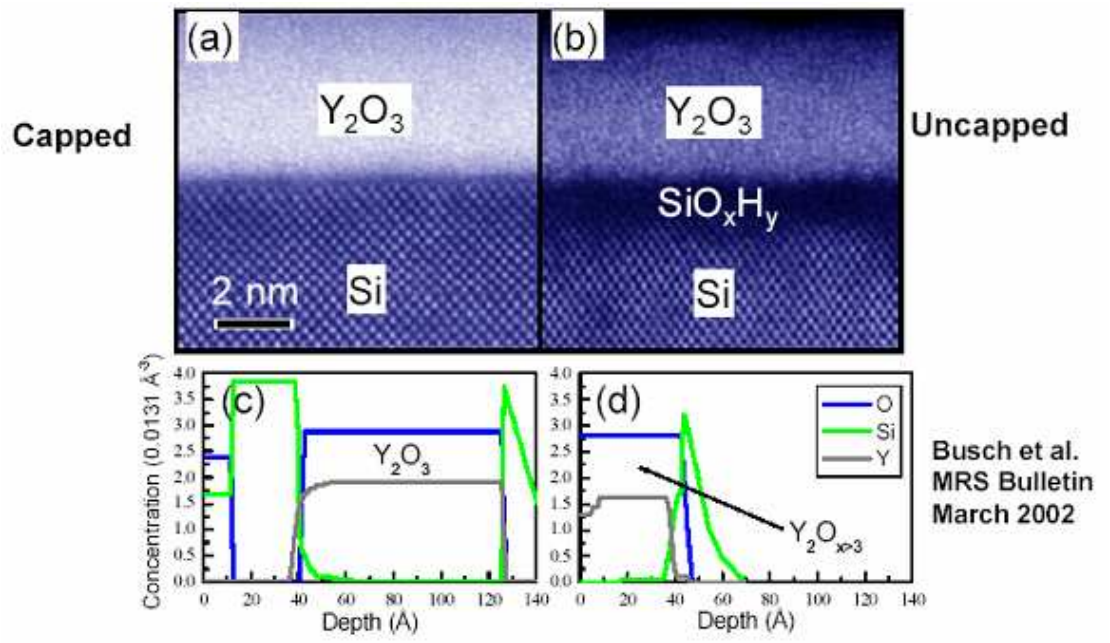

Fig. 1.5 TEM and SIMS analysis of Y_2O_3 high-k dielectric with capped and uncapped samples. Uncapped Y_2O_3 sample shows additional interfacial layer due to oxygen diffusion.

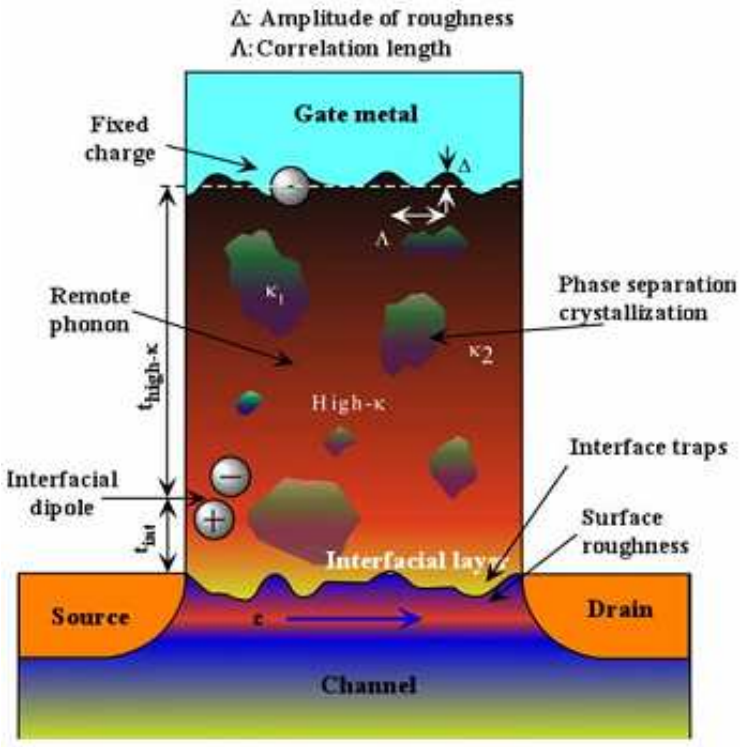

Fig. 1.6 Schematic representation of factors contributing to carrier mobility degradation in a high-k oxide layer.

CHAPTER 02

Effects of FSG Passivation from Various CF_4 Flow on the Properties of HfO_2 Thin Films

2.1 Introduction

In order to improve device performance, thinner gate insulators are required for deep sub-micron metal semiconductor field effect transistors (MOSFETs). In this situation, high-k dielectrics are effective for suppressing gate leakage current. However, a major issue in applying high-k dielectrics is that it inherently possess a high density of structural defects, both intrinsic and process/integration related. Thus, Performance degradation for high-k is a concern, particularly for the low power applications where the high-k dielectric thickness is in the range containing high defect density. High defect density in the bulk of high-k gate dielectric and the interfaces in the gate stack structure are the major causes for bias temperature instability (BTI) of V_{Th} instability (or reliability degradation) [1] as well as mobility degradation [2-3]. In order to eliminate these traps, a variety of nitridation techniques were proposed to incorporate nitrogen into the high-k films. Previous studies show that fluorine passivation is very robust and can be used to improve the reliability of high-κ dielectric MOSFETs [4-6]. Several research studies have demonstrated the application of fluorine ion implantation techniques to improve the electrical characteristics of high-k dielectric MOSFETs

by eliminating inherent bulk traps. However, it is worth pointing out that an additional thermal annealing process is required to activate the fluorine ions and cure the damage created by fluorine ion implantation, which can result in forming thicker EOT.

In this work, we studied the defect passivation with fluorine in a hafnium oxide High-K gate dielectric with poly-si gate. The novel fluorinated gate stack device exceeds the BTI targets with sufficient margin. Fluorinated silicate glass (FSG) films have also been utilized in the intermetal dielectric (IMD) layer, and in the fluorinated gate dielectric for integrated circuit (IC) manufacturing technology [7-8]. It has been demonstrated that the addition of fluorine atoms into SiO_2 can reduce the film dielectric constant to 3.2 or lower, which leads to reduced cross-talk, RC time delay, and power consumption. Using FSG film to serve as IMD can meet the requirement of multilevel interconnection in ultralarge-scale integrated circuit (ULSI) applications. Moreover, the fluorinated gate dielectric can improve the gate oxide/Si substrate interface immunity against hot-carrier impact, and exhibits better dielectric breakdown characteristics [9]. On the other hand, Kim et al. have proposed using the FSG film to serve as a diffusion source to introduce fluorine atoms into the poly-Si film [10].

2.2 Experimental Procedure

The experiment propose a simple and effective fluorine passivation technique that involves the use of a FSG passivation layer

embedded in the HfO_2/SiON gate dielectric. In the proposed fluorine passivation method, we introduce the fluorine atoms into the HfO_2 bulk material and other interfaces from the FSG passivation layer.

2.2.1 Device Fabrication Flow

First, we use local oxidation of silicon (LOCOS) process was used for device isolation. n-MOSFET device was fabricated on 6-inch p-type Si with (1 0 0)-orientation. After removing the 300Å sacrificial oxide, RCA clean was performed with HF-dip last, and immediately followed by a conventional RTA at 800 °C for 30 sec in N_2O ambient to form about 1 nm interfacial oxynitride layer (SiON). Afterwards, HfO_2 film of approximately 30Å was deposited by atomic vapor deposition (*AVD*™) in an AIXTRON Tricent® system at a substrate temperature of 500 °C, followed by 600 °C N_2 RTA for 30 sec in order to improve the film quality. The physical thickness of the SiON and HfO_2 films was measured by optical N&K analyzer. A 200 nm poly-silicon was deposited by low pressure chemical vapor deposition (LPCVD). Subsequently, gate electrode was defined by I-line lithography stepper and etched by ECR etching system. After removing sidewall spacer, S/D extension implantation was implemented by As implantation. Spacer formation was carried out by plasma-enhance chemical vapor deposition (PECVD) and then S/D implantation was executed by Arsenic implantation. Rapid thermal anneal (RTA) was performed at 950 °C for 30 sec in N_2 ambient to activate dopants.

Afterward, a 3000Å-thick FSG passivation layer (or PMD dielectric) was deposited by PECVD at 300 °C with SiH_4, N_2O, and CF_4 as precursor gases (see Fig. 2-1). To investigate the effect of various fluorine contents on the device performances, the SiH_4 and N_2O flow rates were adjusted at 4 and 60 sccm, and a variety of flow rates 10, 20, and 30 sccm were used to introduce CF_4 into the PECVD chamber and deposit various FSG passivation layers. The various CF_4 flow rates of 10, 20, and 30 sccm correspond to the FSG A, FSG B, and FSG C passivation layers, respectively. Table 2.1 lists the conditions of precursors to grow FSG passivation layers. For comparison, the control sample was deposited with a 3000Å-thick conventional PECVD-TEOS passivation layer. Since the FSG film shows poor thermal stability and the fluorine atoms may diffuse out of the FSG film during post thermal annealing, a 1000 Å-thick SiN_x capping layer on the FSG film was successively deposited by PECVD to improve the thermal stability of the FSG film and avoid the diffusion of fluorine atoms out of the FSG film [11]. After passivation layer formation and contact hole pattering. And Al-Si-Cu metallization was deposited by PVD system and then pattering. Finally, sintering process at 400 °C for 30 minutes in N_2 ambient is eventually executed to finish our novel fluorinated devices in this thesis.

The main process flow is summarized in Fig. 2-2 and schematic cross section of HfO_2/SiON n-MOSFETs with FSG passivation layer is illustrated in Fig. 2-3.

2.2.2 Suitable Measurement Setup

The experimental setup for the I-V, C-V, charge pumping and reliability measurements of MOS device is illustrated in Fig. 2-4. Based on the PC controlled instrument environment, the complicated and long-term characterization procedures for analyzing the intrinsic and degradation behavior in MOSFET's can be easily achieved.

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated by a HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The capacitance equivalent thickness (CET) of the gate dielectrics was obtained from high frequency (100 KHz) capacitance-voltage (C-V) curve at strong inversion without considering quantum effect. The interface trap density (N_{it}) was analyzed using the charging pumping method. A 1MHz for frequency and 10 ns for rising/falling time square pulse waveform provided by HP8110A with fixed amplitude level (V_A) is applied to NMOS gate. We keep V_A at 1.2V while increase V_{Base} frome -1.0V to 0.9V by step 0.1V, i.e., the base voltage varied from inversion to accumulation. The parameter analyzer HP4156A is used to measure the charge pumping current (I_{CP}). Fig. 2-5 shows the configuration of measurement setup used in our charging pumping experiment. A MOSFET with gate area A_G gives the charging pumping current as Equation (2-1) :

$$I_{CP} = qA_G fN_{it} \qquad (2\text{-}1)$$

Interface trap density could be extracted from the above equation. The total trap density increase, ΔN_T, which includes the increase of interface trap density and bulk trap density was calculated from ΔV_{Th} by assuming that the charge was trapped at the interface between the dielectric and the substrate. It expresses as follows Equation (2-2) :

$$\Delta N_T = \frac{C\Delta V_{Th}}{qA_G} \quad (2\text{-}2)$$

and bulk trap density also can be calculated as follows Equation (2-3) :

$$\Delta N_B = \Delta N_T - \Delta N_{it} \quad (2\text{-}3)$$

For mobility characterization, the electron mobility for n-MOSFETs was extracted using split C-V method .

2.3 Result and Discussions

2.3.1 Basic Device Characteristics

The C-V curves (100 KHz) of FSG A, B, C, and control samples are show in Fig. 2-6. The capacitance of the sample with CF_4 gas introduced decreases compared to that of the as-deposited sample, which no obvious difference in C-V curves in substance. When CF_4 gas flow rate is lower than 20 sccm, it indicates a slight increase of CET in FSG A and FSG B. However, the introduced CF_4 gas is much more than the allowable F concentration, residual damage for the CET after sintering step can be observed. The resultant CET increment faster may be an excess amount of F incorporation into high-k film stacks [12-13] or the absorption of moisture from the atmosphere in the

plasma-deposited FSG film is the principle root-cause, which many studies indicated that the phenomenon of moisture (H_2O) absorption in the plasma-deposited FSG film has been observed because the Si–F bonds present are highly reactive with moisture [14-15]. Fig. 2-7 was investigated with respect to CET and flat-band voltage (V_{FB}, not shown) [16] for the samples. We can see the fact that the V_{FB} has shifted to positive direction as the CF_4 flow rate increases and EOT is also affected by the presence of F atoms. This is point out that decrease of positively charged traps or increase of negatively charged traps [17-19].

Fig. 2-8 shows the gate leakage current of n-MOSFET with HfO_2/SiON gate stack under both inversion and accumulation modes. It can obviously noted that with FSG passivation layer, the leakage current is significantly suppressed for both polarities. Specially, the reduction under normal operation condition, i.e., inversion mode, is around 40% of magnitude lower. One of the reasons for the exhibited gate leakage current reduction may be a thicker CET for two splits of fluorinated devices. Hence, it extrapolates that the CF_4 gas flow rate even up to 30 sccm doesn't deteriorate gate leakage current, and on the contrary, the reduction extent of gate leakage current is dependent on the flow rate of CF_4 gas introduced into FSG passivation from measurement data of Weibull distributions shown in Fig. 2-9. Fig. 2-10 demonstrates the transconductance (G_m) as a function of gate voltage for both gate dielectrics. The G_m is normalized by CET

(Capacitance Equivalent Thickness), which is 37.9Å, 39.4Å, 42.1Å, and 38.3Å for FSG A, B, C, and control sample, respectively. The peak transconductance is 28%, 42%, and 67% for FSG passivation with respect to TEOS passivation. Fig. 2-11 shows the improved normalized linear drain–current I_D which FSG P.L. is 24% higher above than TEOS P.L. and the inset of subthreshold slope (S.S.) reduced 9.6% for the CF_4 introduced samples, indicating that fluorinated CMOS HfO_2 has better interface characterization. Previous study [20] on Zr-silicate indicates that electron transport in the channel can be degraded by the coulomb scattering of negative charges in the bulk film, and Fischetti et. al [21] also points out that electron mobility in the inversion layer is affected by remote phonon scattering due to ionic polarization in high-k films. Therefore, the peak transconductance degradation in HfO_2/SiON stack is probably due to charges or traps in the bulk film, as evidenced by the positive shift in C-V curve in Fig. 2-6, even if the interface-state densities are kept to be small. Besides, as shown Fig. 2-12, the V_{Th} distribution is less affected by the addition of F for FSG A and B wihile a increased V_{Th} can be observed for FSG C, which also corresponding with the V_{FB} trend (not shown) due to negatively charged traps.

Fig. 2-13 presents the excellent output drive current characteristics ($I_D - V_{DS}$) under various normalized gate biases ($V_{GS} - V_{Th}$), which almost 12% enhancement in magnitude of $I_{D,Sat}$

for FSG P.L. with respect to TEOS P.L.. The gate voltage has been normalized with respect to threshold voltage to minimize the effect of threshold voltage. We also understand that normalized $I_{D,Sat}$ and transconductance max peak depends on the flow rate of CF_4 gas or the amount of fluorine incorporated from Fig. 2-14. The improvements are believed to be intimately related not only to the better interface quality but also to the reduced bulk trap density. To quantify the interface state density by the CP current measurement, which the CP peak height is approximately proportional to the interface state density (N_{it}) along the channel, Fig. 2-15 can be seen that the trend is quite consistent with that in subthreshold swing, as shown in inset of Fig. 2-11. Channel mobility is dependant on the nature of gate dielectric between Si substrate and high-k gate dielectric. CF_4-introduced high-k gate dielectrics suffer from CET increased whereas mobility can be enhanced shown in Fig. 2-16. The peak mobility for FSG C device is 7% higher than the control, and the high field mobility at 0.8MV/cm is 49% higher than the control, which is correlated with the higher $G_{m,max}$ (see inset of Fig. 2-16) and higher output current characteristics. The electron mobility at 0.8MV/cm for the fluorinated device is 68% of SiO_2 universal curve. Clearly, as the amount of introduced CF_4 gas become elevated, peak mobility increasing with decreasing interface state density implying the weak and dangling bonds, associated with interface and trap states, are passivated and released strain bonds by fluorine atoms, leading to the

enhanced electrical characteristics show in Fig. 2-17.

Fig 2-18 indicates the subthreshold swing of devices with different passivation layers as a function of channel length. And we find that subthreshold swing for FSG P.L. shows the better interface states than TEOS P.L.. Thus, the FSG P.L. will improve the subthreshold swing in device. The relation between drain current and channel length for all splits of HfO_2/SiON gate stack n-MOSFET is shown in Fig. 2-19 and G_m is in Fig. 2-20. When channel length becomes shorter, the improvement is more obvious. Fig 2-21 shows the V_{Th} -roll-off characteristics with different passivation layers. When channel length is less than 1μm, V_{Th}-roll-off phenomenon is more serious for TEOS P.L. while the FSG devices effectively suppress this behaviour to the same extend with increasing the amount of CF_4 gas flow. In short, it was found that all fundamental electrical properties, including the CET, flat-band voltage, threshold voltage, drive current, interface state density (N_{it}), swing, mobility, gate leakage current, and short channel effect are almost non-degradation instead of surprise enhancement for device performance between the four splits with FSG and TEOS P.L..

2.3.2 Current Transport mechanism

Using the carrier separation method, the carrier type is investigated for the fresh devices. The carrier of gate leakage can be separated into holes and electrons. Fig 2-22 (a) and (b) are carrier

separation results for the TEOS sample under inversion and accumulation regions, respectively. It is shown that the S/D current that electrons tunnel through gate stack dominates the gate leakage for the inversion region while the substrate current that holes tunnel through gate stack dominates the gate leakage for the accumulation region. The carrier separation results for the FSG sample are shown in Fig. 2-23 (a). The case for the accumulation region is similar to the TEOS sample (see Fig. 2-23 (b)), i.e., holes from the substrate dominate the gate leakage. However, the case for the inversion region is different from the TEOS sample, where I_{SD} is obviously suppressed.

These trends can be explained by the band diagram shown in Fig. 2-24 (a) and carrier separation experiment shown in Fig. 2-24 (b). The substrate current I_{SUB} corresponds to the hole current from the gate, while the S/D current I_{SD} corresponds to the electron current from Si substrate under inversion region. Holes supply from the gate valence band in n-MOSFETs is limited by the generation rate of minority holes in n^+ gate. On the other hand, the probability of carriers from S/D that tunnel through gate stack is strongly affected by tunneling distance and barrier height of ~ 1.0 nm interfacial oxynitride layer. As a result of the asymmetry of the HfO_2/SiON band structure, it is more difficult for holes to tunnel through gate stack, as compared to electrons. Consequently, the current through the gate stack should be smaller for holes, as compared to electrons. In

n-MOSFETs, electron current from the channel is the predominant injection current under stressing. The leakage component under accumulation region could also be explained by band diagrams shown in Fig. 2-25 (a), and the current component flow in carrier separation experiment is shown in Fig. 2-25 (b). In addition, we can see that the magnitude of the leakage current in inversion is larger than that in accumulation. A plausible explanation can be understand from the asymmetric band diagram's point of view.

Fig. 2-26 (a) and (b) show gate current I_g as a function of V_g for the HfO_2/SiON gate stacks measured at several different temperatures up 100 °C in inversion and accumulation regions, respectively, for two different passivation layers. The current is temperature dependent that increases with increasing temperature. This implies that the conduction mechanism of gate current is trap-related, i.e., trap-assisted tunneling (TAT), Frenkel-Poole, etc. Base on the equation of Frenkel-Poole (F-P) :

$$I \propto V \exp\left(\frac{2a\sqrt{V}}{T} - \frac{q\phi_B}{k_B T}\right) \tag{2-4}$$

$$J = B * E_{ox} \exp\left(\frac{-q(\phi_B - \sqrt{qE_{ox} / \pi\varepsilon_H\varepsilon_0})}{k_B T}\right) \tag{2-5}$$

$$\ln\left(\frac{J}{E_{ox}}\right) = \frac{q\sqrt{q / \pi\varepsilon_H\varepsilon_0}}{k_B T}\sqrt{E_{ox}} - \frac{q\phi_B}{k_B T} \tag{2-6}$$

Where B is a constant in terms of the trapping density in the HfO_2 film, ϕ_B is the barrier height, E_{ox} is the electric field in HfO_2 film, ε_0

is the free space permittivity, ε_H is HfO_2 dielectric constant, k_B is Boltzmann constant, and T is the temperature measured in Kelvin. Fig. 2-27 shows the F-P plot for the source/drain current in inversion region. Fig. 2-28 shows the F-P plot for the substrate current in inversion region. The solid lines are fitting curves for all temperatures. In the high voltage I_{SD} and I_{SUB}, an excellent linearity for each current characteristic can be obtained, indicating that FSG and TEOS passivation layers exhibit the F-P conduction mechanism for the gate leakage current in nature. The barrier height ϕ_B and the dielectric constant ε_H of HfO_2/SiON gate stacks can be calculated from the intercept of y axis and the slope of the fitting curves according to Equation (2-6). The ε_H value is found to be around 21 for the TEOS sample and around 23 for the FSG sample. On the other hand, the fitting parameters for the hole and electron barrier heights are 1.34eV and 1.12eV, respectively, for the FSG sample, as compared to 1.27eV and 1.07eV for the TEOS sample. Note that the barrier height for electrons has changed from 1.07eV for TEOS to 1.12eV for FSG sample, and for holes has changed from 1.27eV for TEOS to 1.34eV for FSG sample. This indicates that the trap position has moved closer to the conduction and valence band of the poly-si gate after FSG P.L. process. The band diagrams are shown in Fig. 2-29 (a) and (b) for the TEOS and FSG P.L. sample, respectively. We consider the case when the injected carriers flow across HfO_2/SiON by hopping via the trap

sites with energy barrier ϕ_B, whose value depends on the fabrication process [22]. This experimental results indicate that the position of traps level in the FSG sample can be deeper than the TEOS sample, and the energy barrier ϕ_B for electrons is clearly lower than that for holes about 0.2eV in both samples.

2.4 GIDL Effect on Off-State Leakage

Gate-induced drain leakage (GIDL) is attributed to the band-to-band tunneling (BBT) process taking place in the deep-depleted drain region underneath the gate oxide. Electron-hole pairs are generated by the tunneling of valence band electrons into the conduction band and subsequently collected by the drain and substrate separately. The schematic energy band diagram of the gate-drain overlap region is shown in Fig. 2-30. The BBT (I_{BBT}) could be simplified as Equation (2-7) [23] :

$$I_{BBT} = AE_S \exp(-\frac{B}{E_S}) \qquad (2\text{-}7)$$

where A is a constant, E_S and B can be approximated as :

$$E_S = \frac{V_{DG} - 1.2}{3T_{OX}} \qquad (2\text{-}8)$$

$$B = \frac{8\pi\sqrt{2m^*}}{3qh}\sqrt[3]{E_g} \qquad (2\text{-}9)$$

where h is Plank's constant, m^* is the effective mass, and E_g is the energy bandgap. From these equations, it should be noted that

BBT current is dependent on E_g. Therefore, if E_g decreases, the band-to-band tunneling current (I_{BBT}) increases. Although Hf-based high-k dielectrics have been investigated to reduce gate leakage current, it has been observed that bulk traps significantly enhance the GIDL current in devices with high-k dielectrics [24]. Hence, bulk traps enhanced gate-induced leakage (BTE-GIDL) current will be found to improve for the devices with FSG passivation layer.

To suppress the BTE-GIDL, the role of charge trapping in high-k film should be understood in detail. As shown in Fig. 2-31, the band diagrams before and after electron trapping are denoted by the solid line and the dashed line, respectively. At low V_{DG} (TAT mechanism), the much lower electron barrier height for poly-gate/high-k than that for hole at high-k/I.L. interface, electron injected from poly-gate dominates trapping mechanism. The charges induced by injected electrons raise the bands, which decrease the tunneling distance and increase the GIDL current. The higher number of bulk traps in high-k that combines with the narrower tunneling distance give rise to higher BTE-GIDL current. At high V_{DG} (BBT mechanism), both electrons and holes are injected into the high-k dielectric, the band position is less bended due to recombination. Another possible mechanism is attributed to the trap-assisted tunneling from traps located at the remote high-k/I.L. interface [24]. Fig. 2-32 shows the $I_D - V_{GS}$ transfer characteristics of all splits at larger drain biasing (V_{DS} =3V).

We can observe that the GIDL current decreases for three splits of fluorinated devices. Especially, the GIDL improvement of FSG C samples was more obvious. The results indicate that the reduction of bulk traps in FSG C sample is more than the others due to more fluorine incorporation into HfO_2/SiON effectively passivating defect, resulting in less electron trapping in HfO_2/SiON contributing to BTE-GIDL. Therefore, the improvement of GIDL on off-state leakage current can be observed for the fluorinated devices.

2.4 Summary

In this chapter, a novel fluorinating technique method for high-k dielectric passivation, using a FSG process as n-MOSFETs passivation layer was presented. We have performaed a systematical investigation of electrical characteristics. Significant device performance improvement in devices with FSG P.L. were found, such as the excellent subthreshold swing, increased transconductance, higher current drive, improved channel electron mobility, and alleviated SCE etc., as compared to the control TEOS sample. As shown in Fig. 2-33, for FSG P.L., the number of interface states by using charge pumping method can be diminished that is attributed to the passivated interface traps by the incorporation of fluorine atoms generated from CF_4 gas in deposition process of PECVD chamber. Specially, the presence of fluorine in the FSG devices lead to a decrease in the numbers of bulk traps from intrinsic hysteresis effect

[25-26] shown in Table 2-2, which summarizing the impact of the FSG passivation layer for HfO_2/SiON gate stack n-MOSFETs. Experimental results show a good correlation between the bulk trap density and the BTE-GIDL. It was observed that incorporating fluorine into HfO_2/SiON gate stack to minimize the bulk traps could effectively reduce the BTE-GIDL.

2.5 References

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Gas / P.M.D.	CF_4	N_2O	SiH_4
Control	0	60	4
FSG A	10		
FSG B	20		
FSG C	30		

Unit : sccm

Table 2.1 Conditions of gas flow rates to deposit FSG passivation layers.

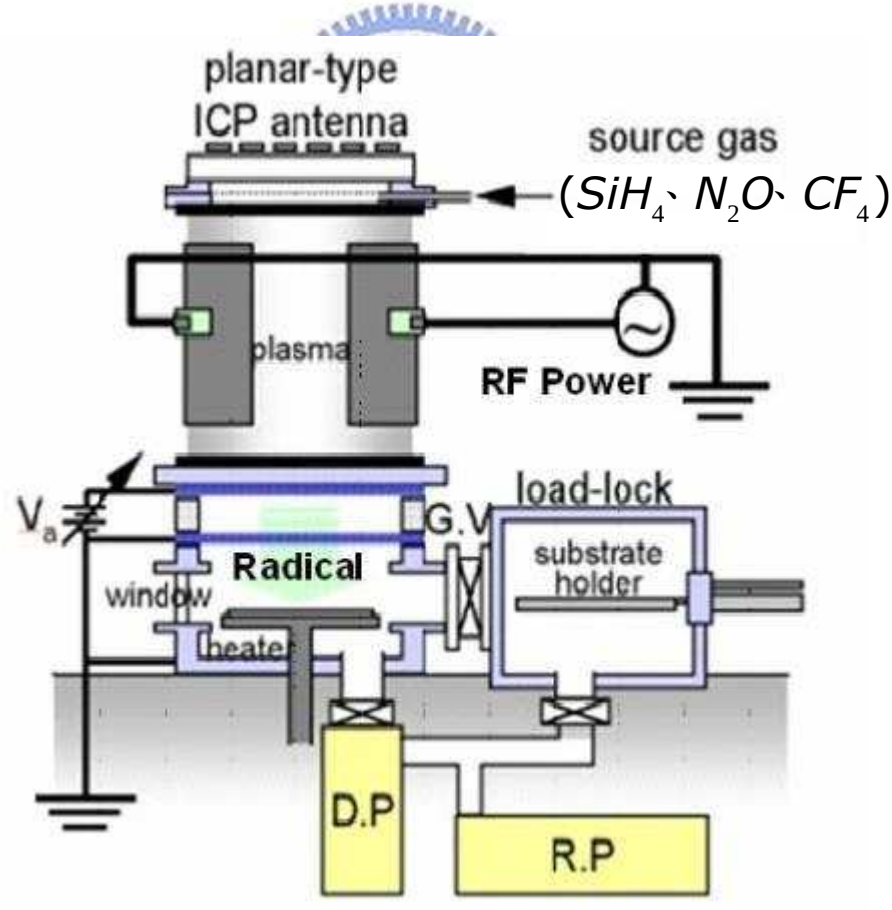


Fig. 2.1 The PECVD system used in this experiment.

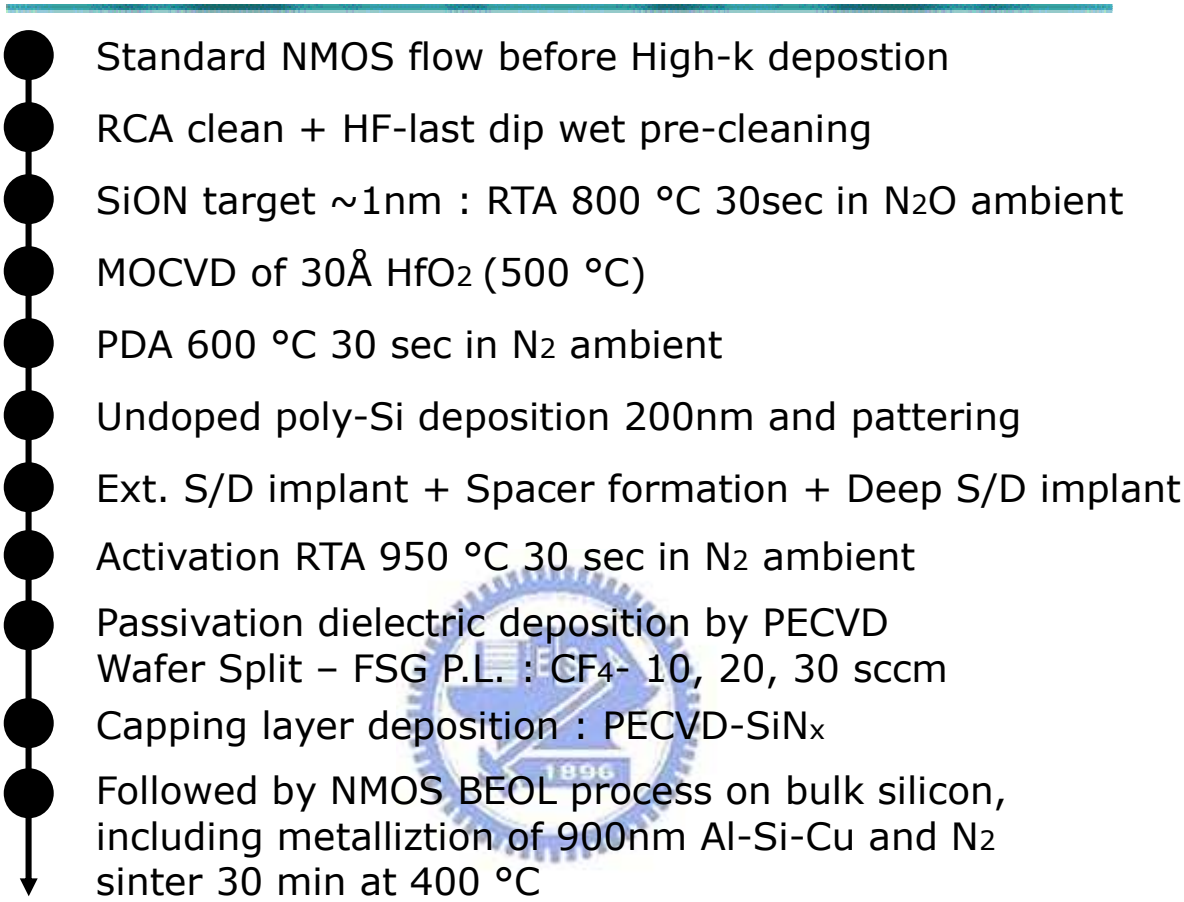


Fig. 2.2 The process flow of n-MOSFETs with FSG passivation layer.

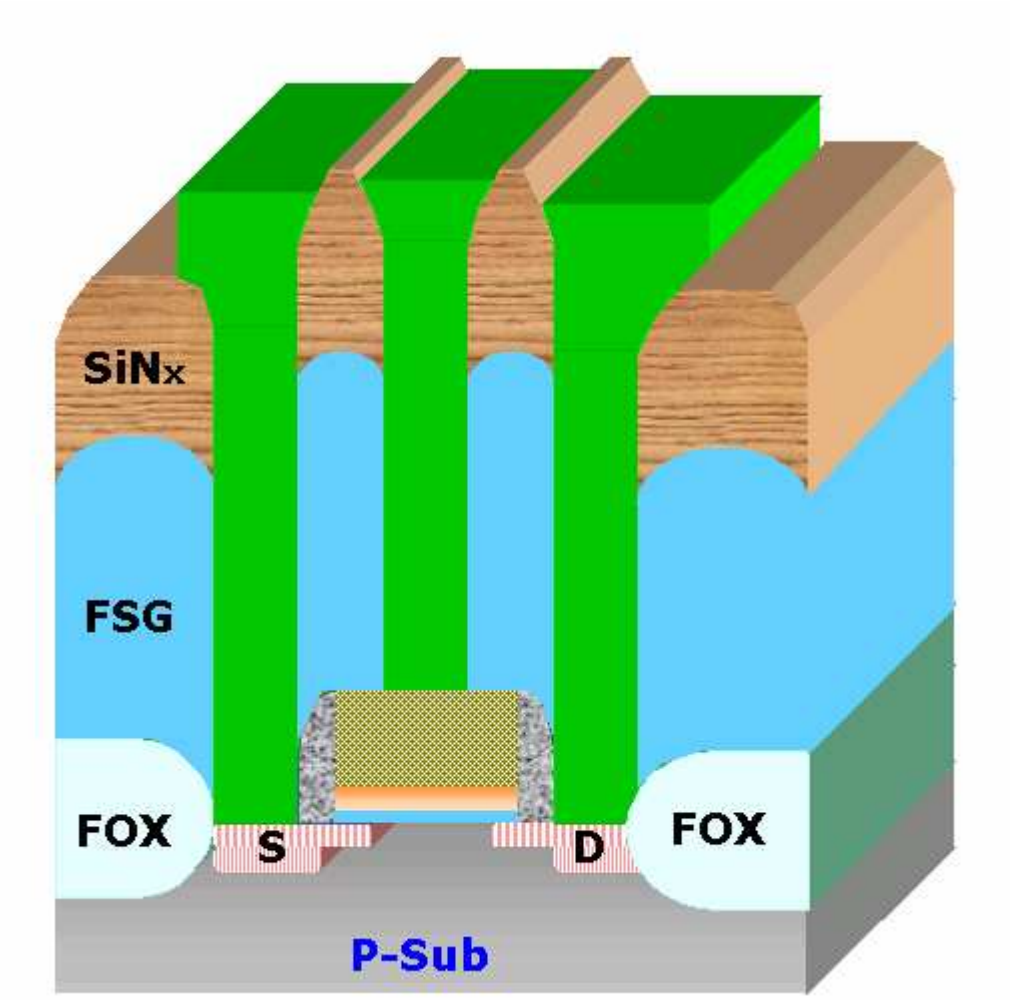


Fig. 2.3 Cross section of HfO_2/SiON n-MOSFET with FSG passivation layer.

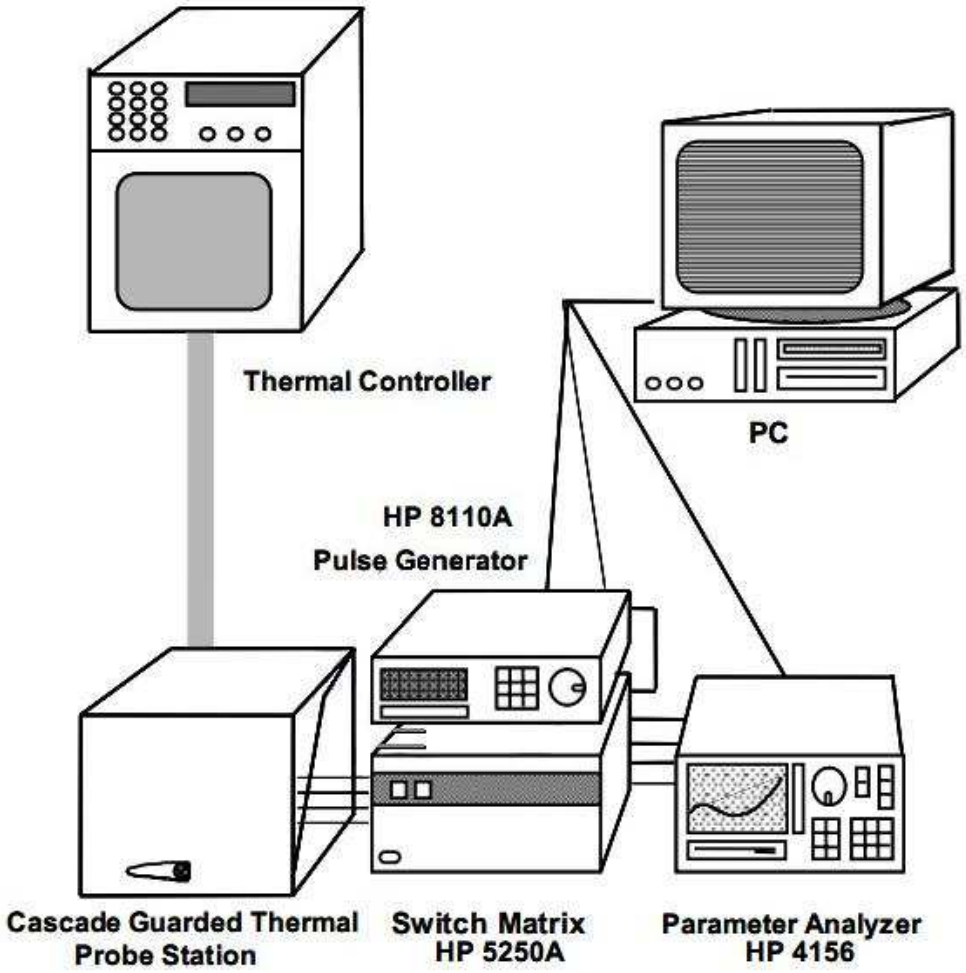


Fig. 2.4 The experimental setup for the basic electrical characteristics and long-term reliability test measurements.

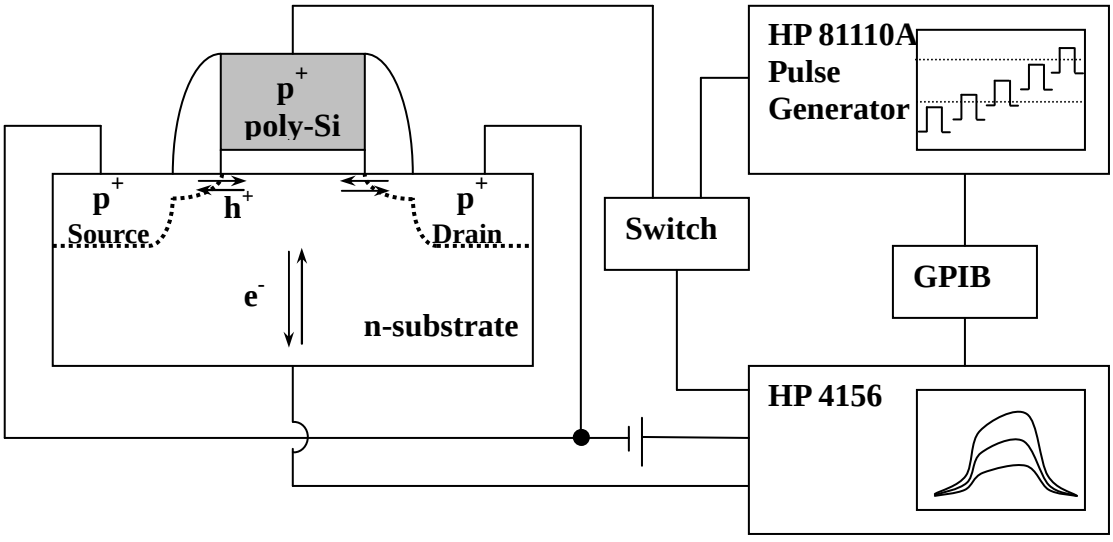


Fig. 2.5 Basic experimental setup of charging pumping measurement.

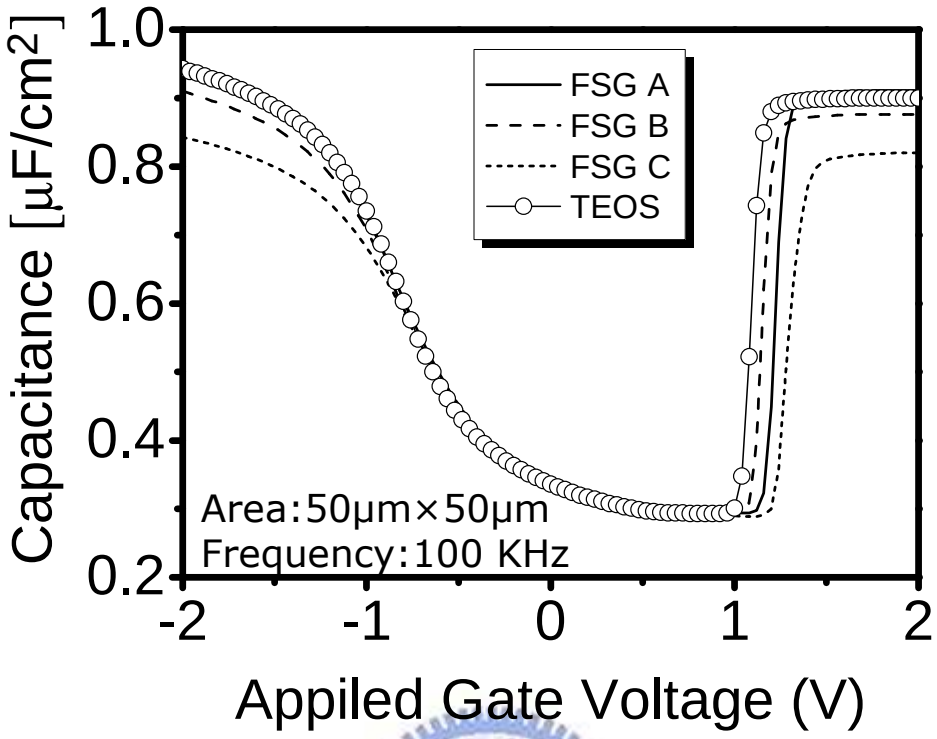


Fig. 2.6 The C-V characteristics of HfO_2 gate dielectrics with various CF_4 as precursor gas.

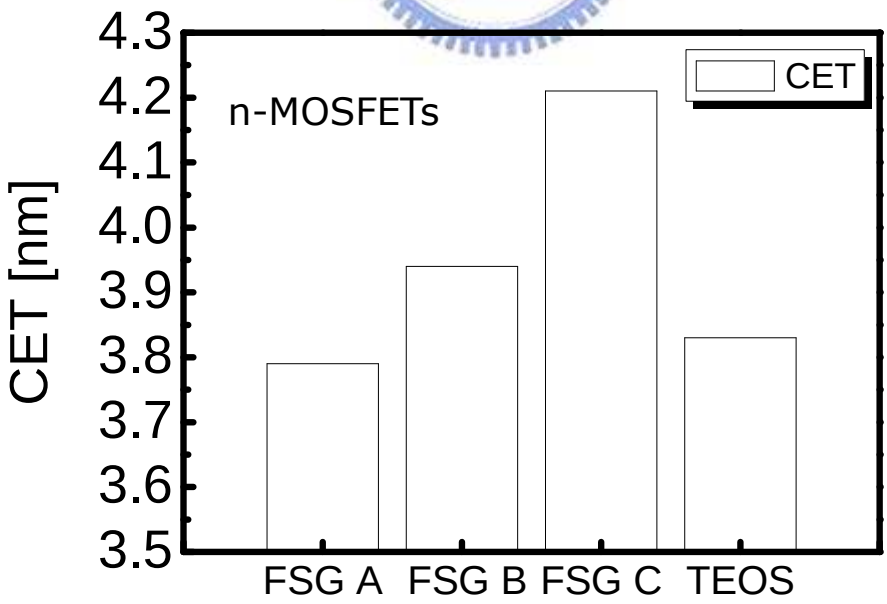


Fig. 2.7 Comparison of CET for all splits, including fluorinated and as-deposited samples.

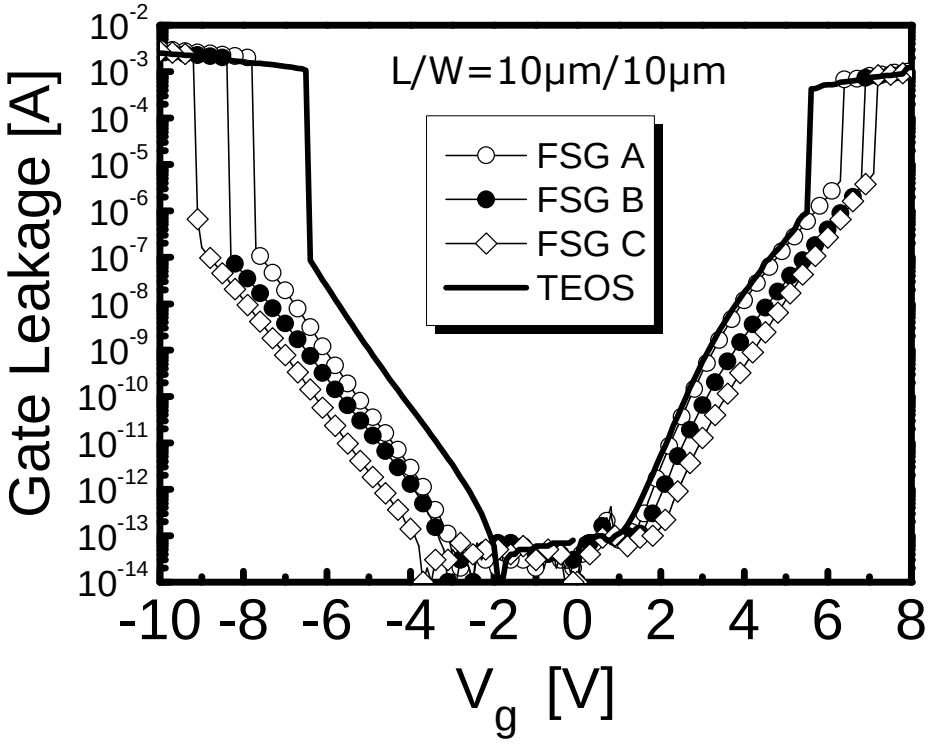


Fig. 2.8 Gate leakage current as a function of gate voltages of HfO2/SiON gate stack with (symbol line) and without (solid line) CF_4 gas incorporation both under inversion and accumulation regions

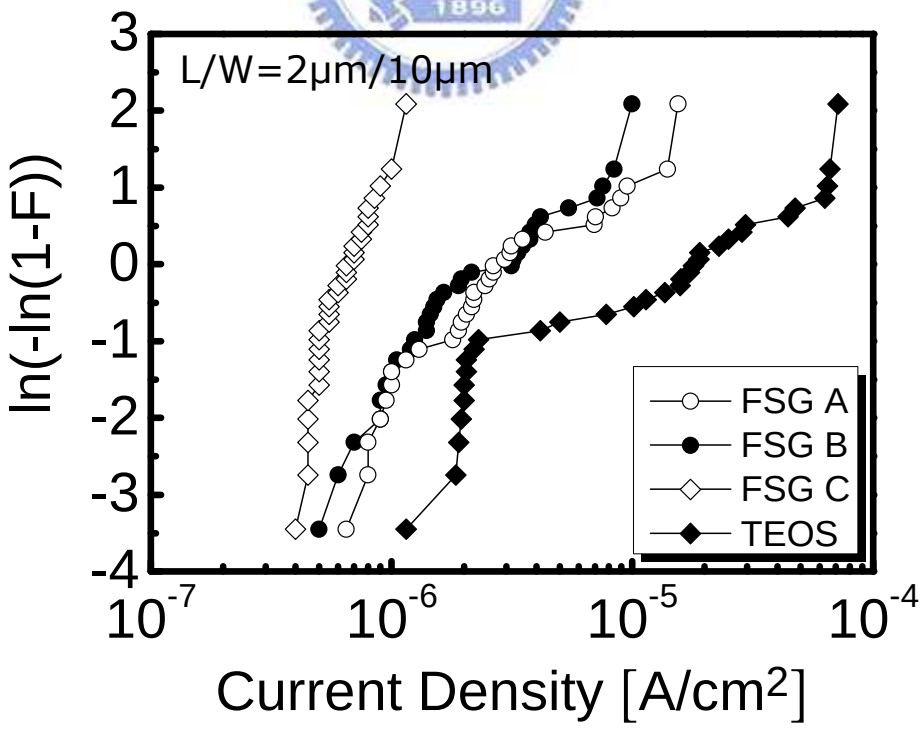


Fig. 2.9 The Weibull plot distributions at V_{GS}-V_{Th} =1.0V of J_g for all samples.

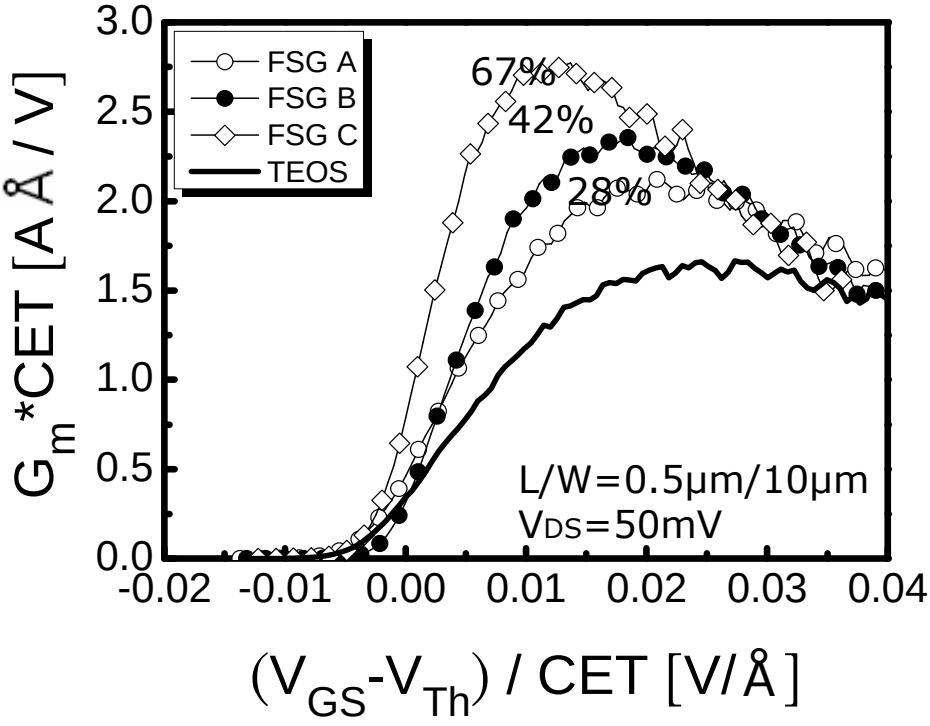


Fig. 2.10 Normalized transconductance as a function of gate voltage for TEOS and FSG passivation layer.

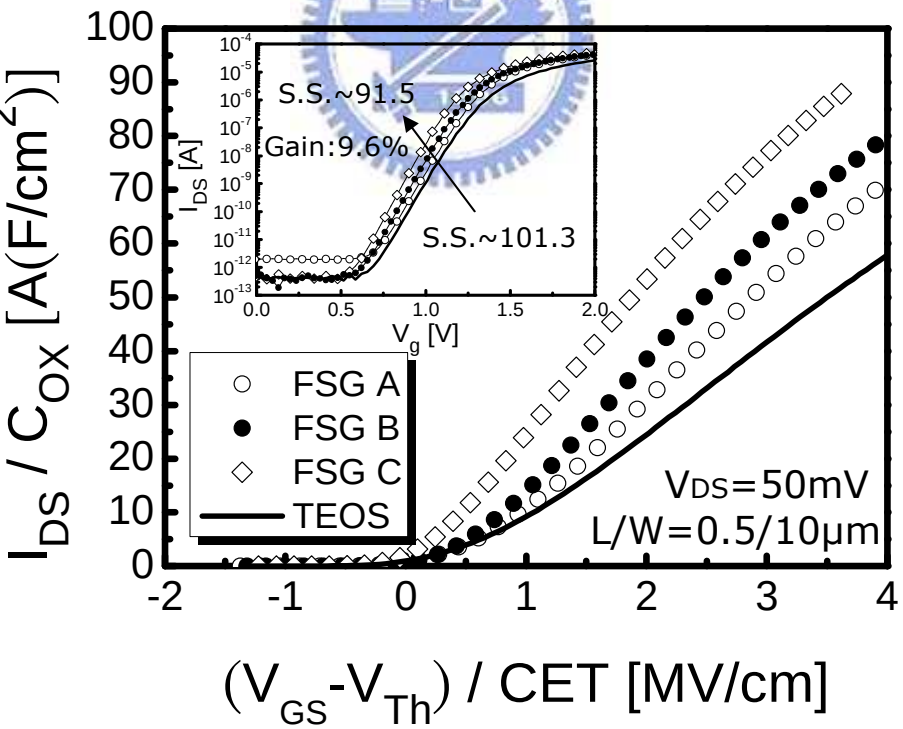


Fig. 2.11 Normalized NMOS I_{DS} of fluorinated device is 24% higher above than that for the control device, and the subthreshold properties is inset in the figure.

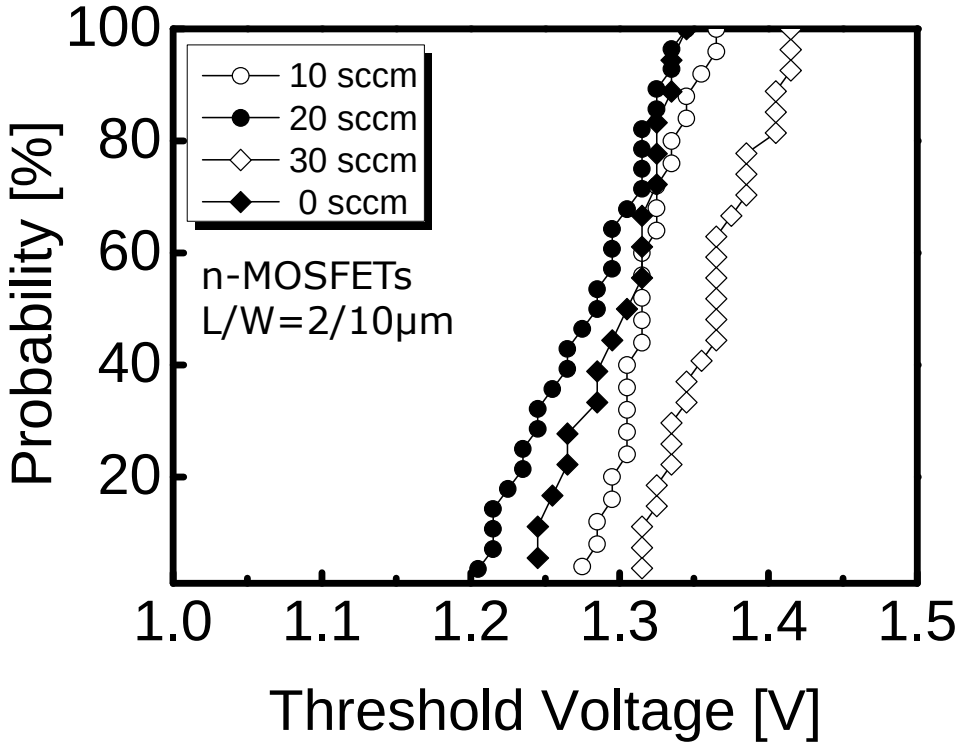


Fig. 2.12 Cumulative probability of the threshold voltage (V_{th}).

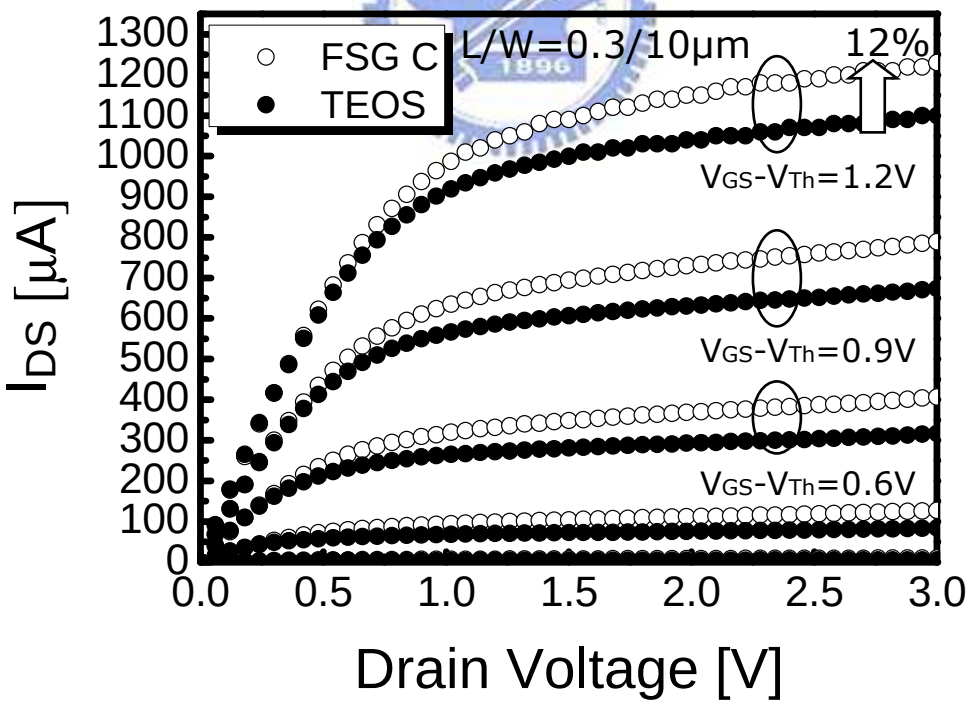


Fig. 2.13 Drain current versus drain voltage (I_D-V_D) curves of FSG C and TEOS P.L. under various normalized gate biases which 0V, 0.3V, 0.6V, 0.9V, and 1.2V, respectively.

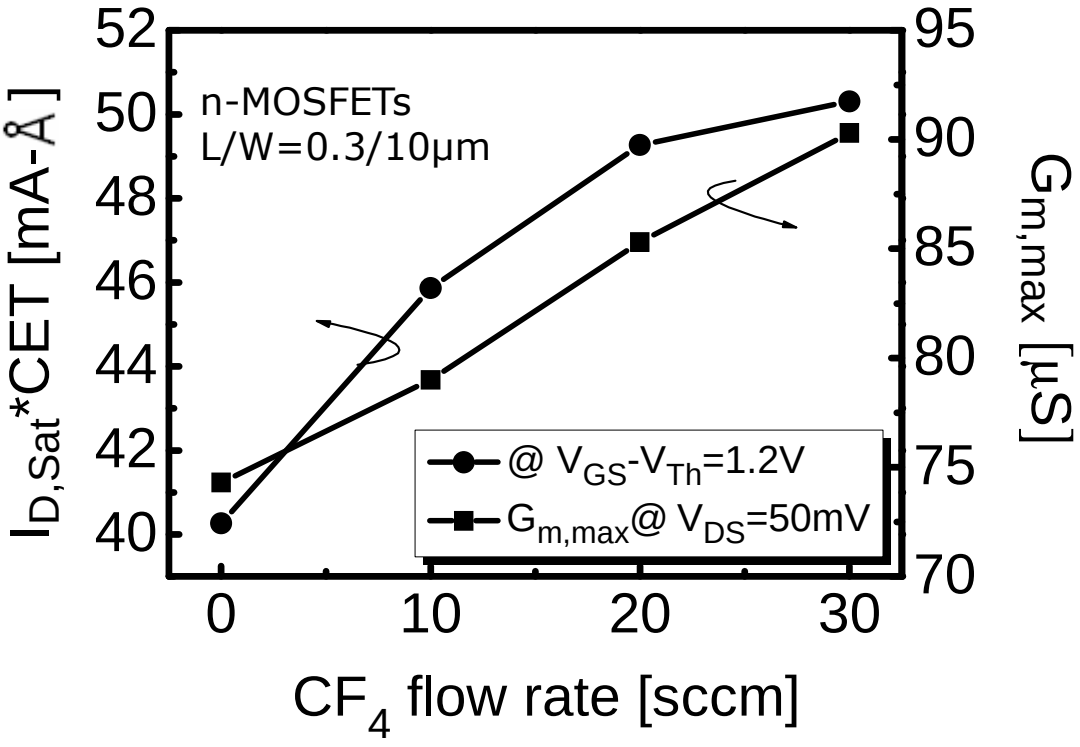


Fig. 2.14 Comparsion of normalized saturation drain current and $G_{m,max}$ for various flow of CF_4 gas introduced.

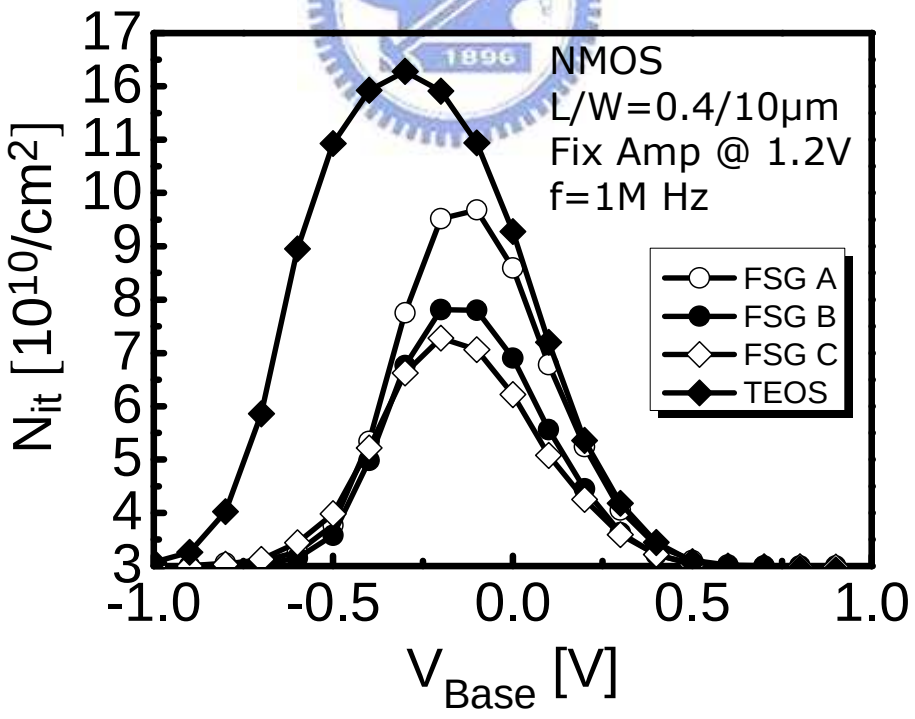


Fig. 2.15 Interface states density as a function of V_{Base} for HfO_2/SiON high-k gate stacks with FSG and TEOS P.L..

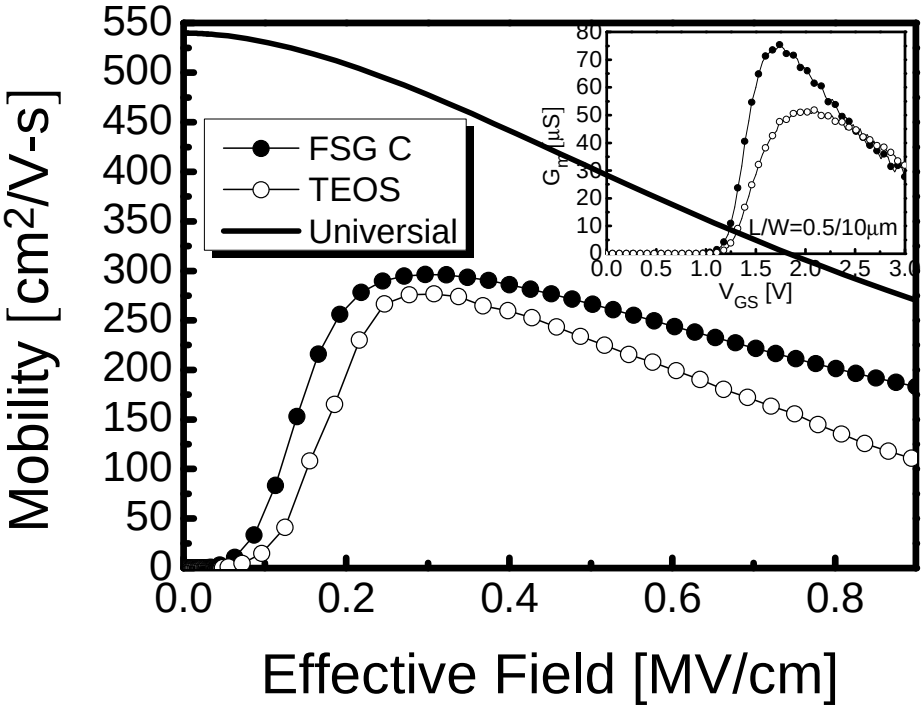


Fig. 2.16 Electron mobility for fluorinated device is enhanced as compared with the control device. Inset comparison of transconductance max peak ($G_{m,max}$).

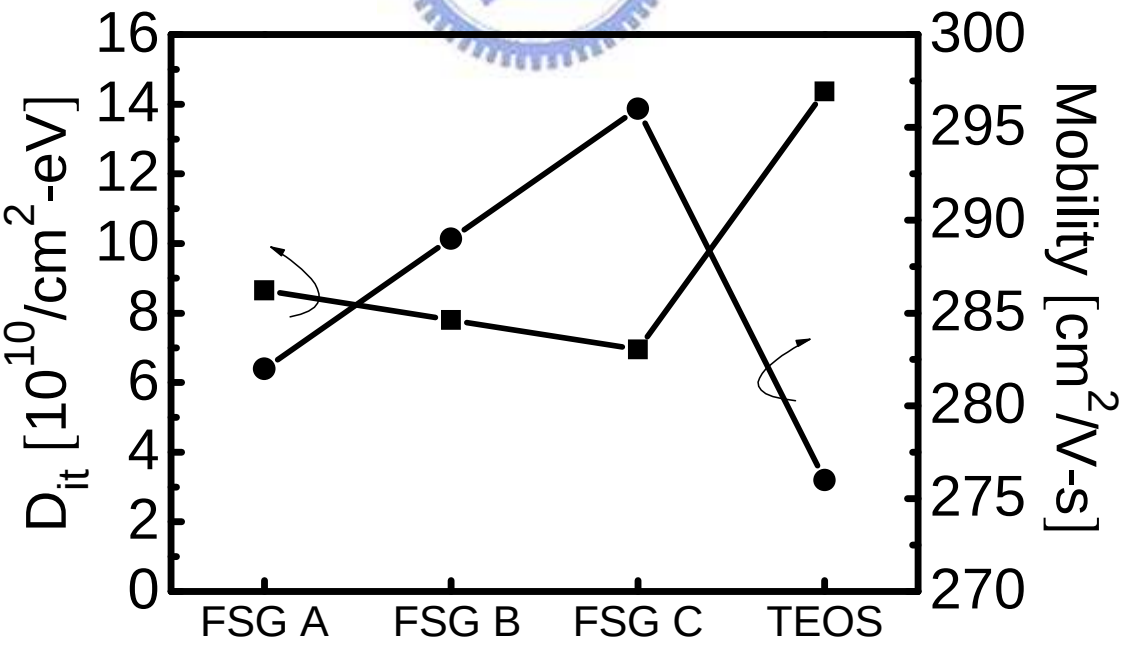


Fig. 2.17 Comparsion of interface states density correlated with electron mobility for all splits.

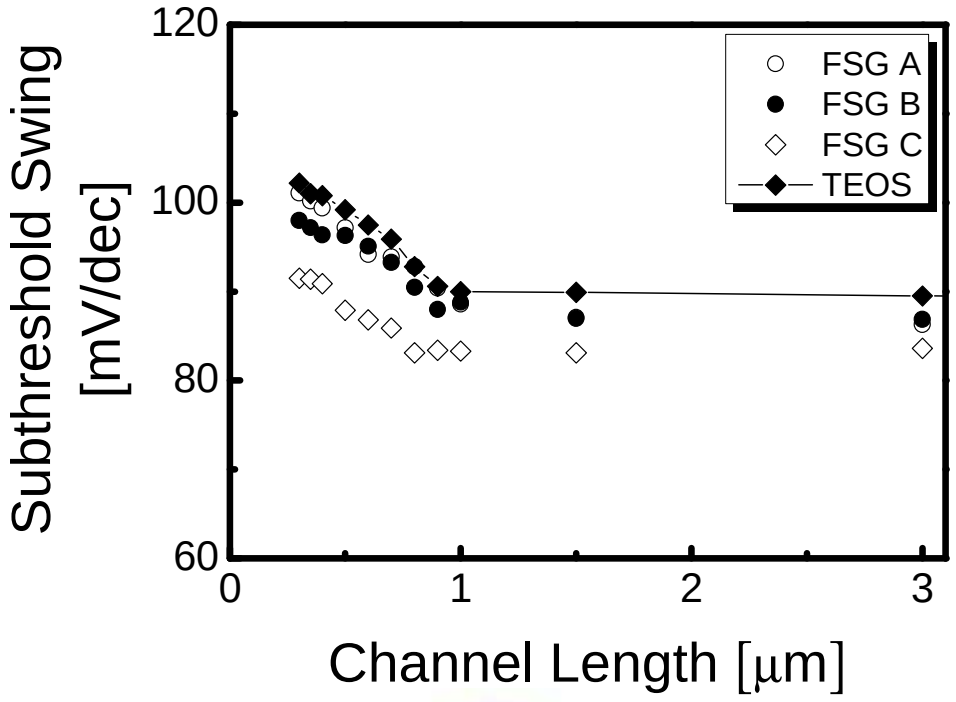


Fig. 2.18 The subthreshold swing versus channel length for all splits of HfO_2/SiON gate stack n-MOSFETs.

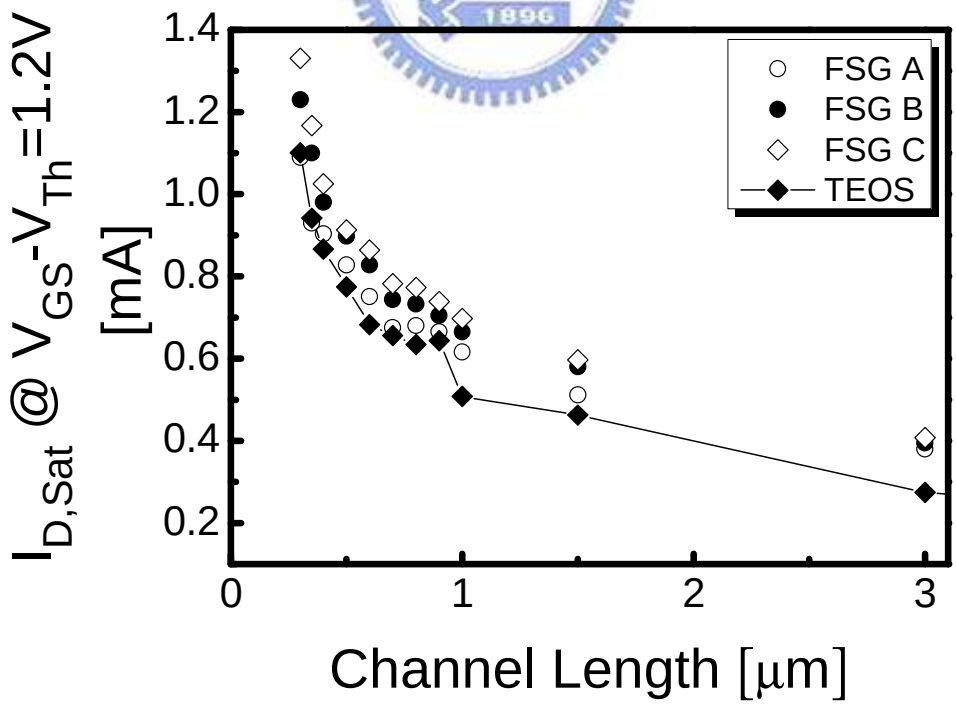


Fig. 2.19 The drain current versus channel length for all splits of HfO_2/SiON gate stack n-MOSFETs.

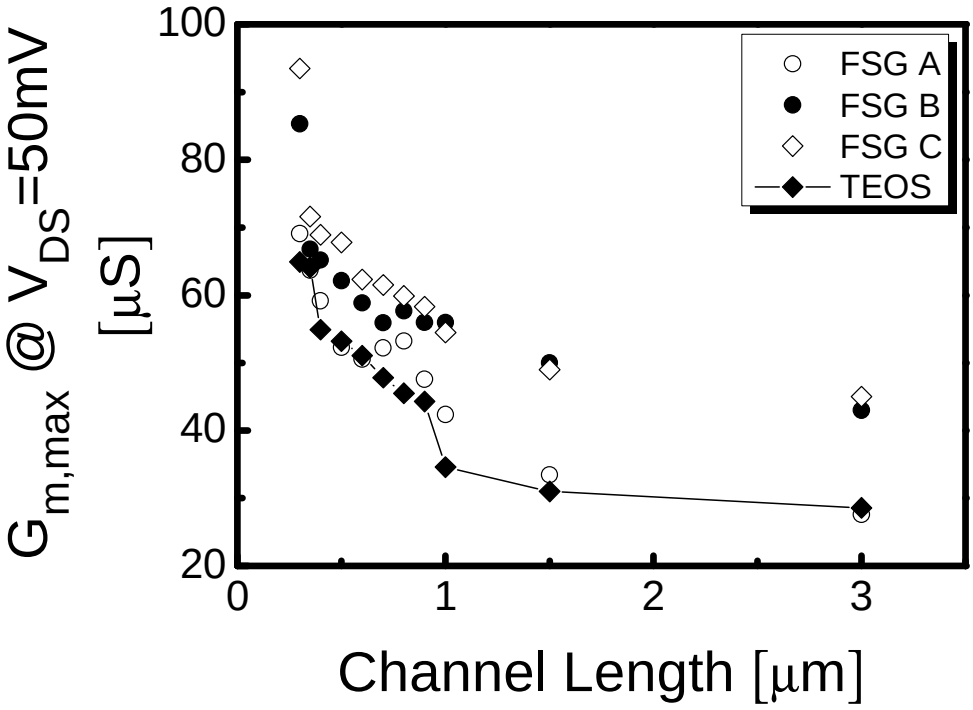


Fig. 2.20 The maximum transconductance versus channel length for all splits of HfO_2/SiON gate stack n-MOSFETs.

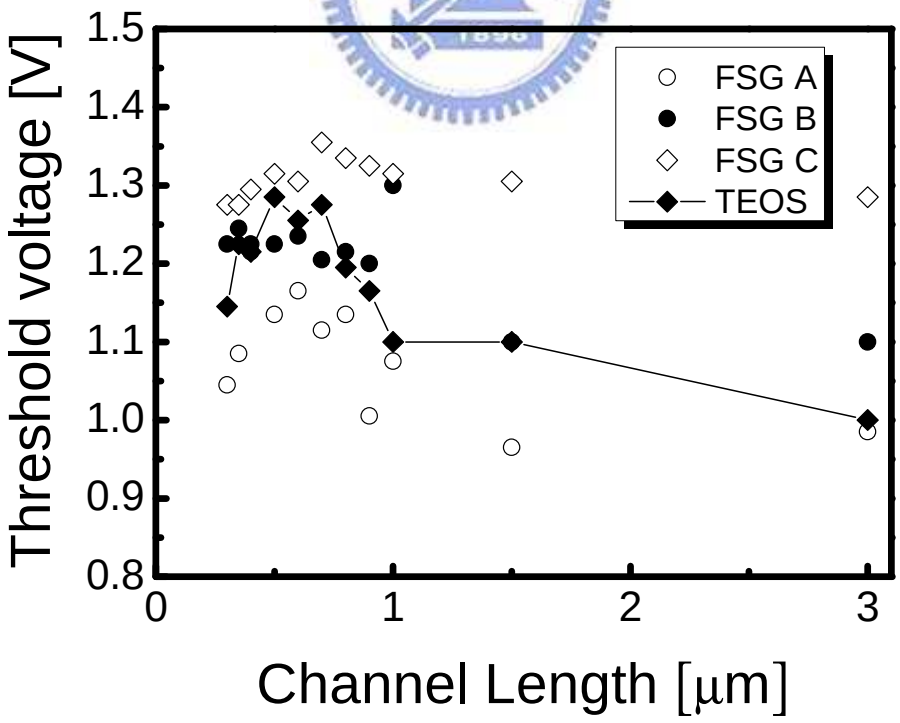
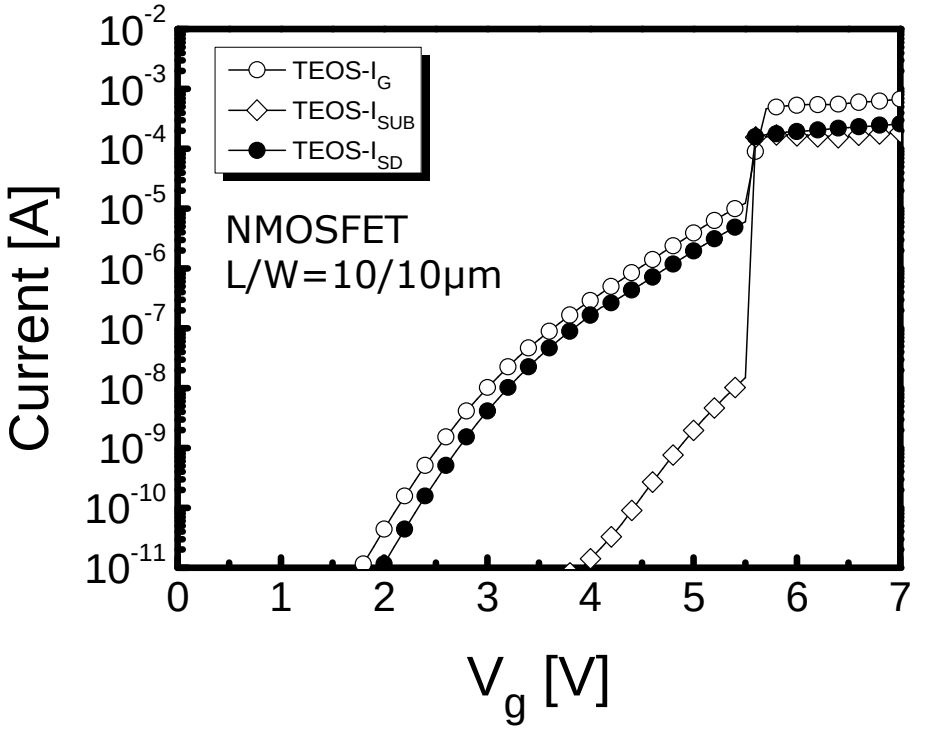
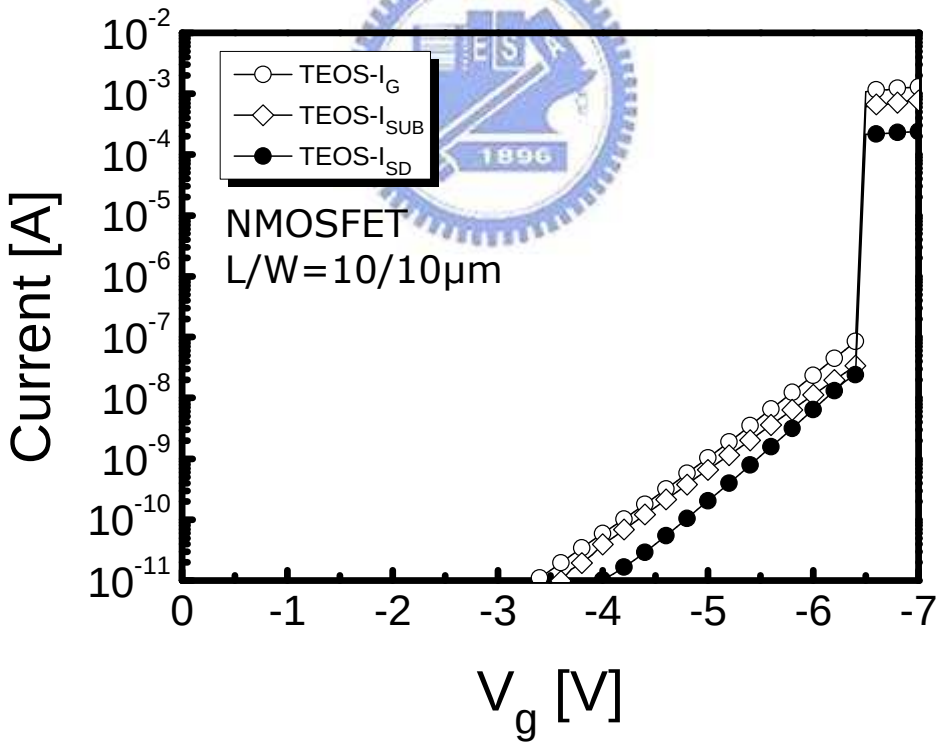


Fig. 2.21 Threshold voltage roll off characteristics for all splits of HfO_2/SiON gate stack n-MOSFETs.

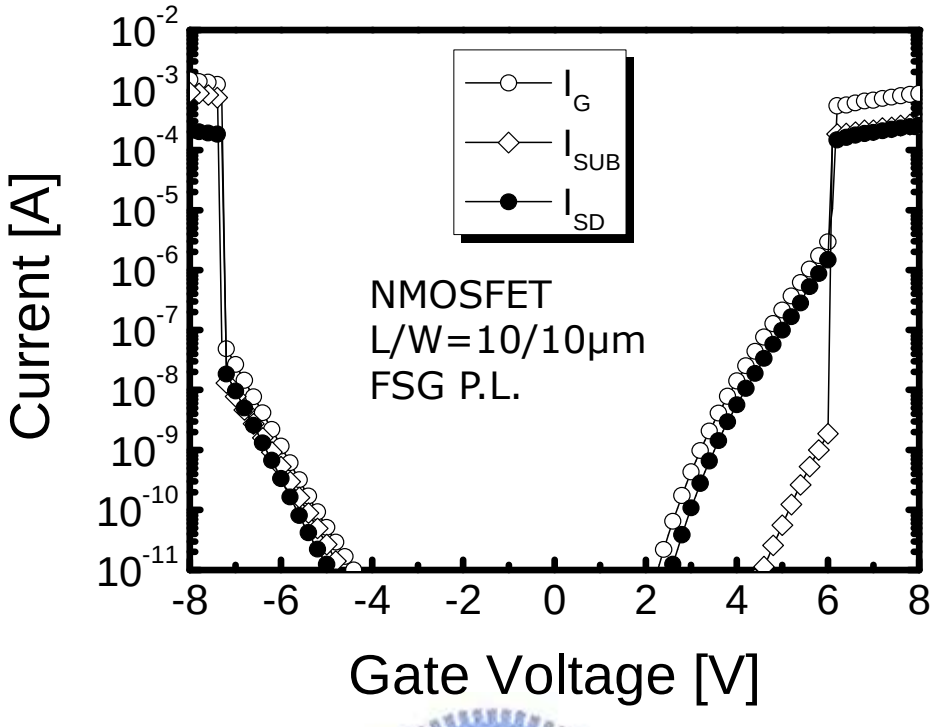


(a)

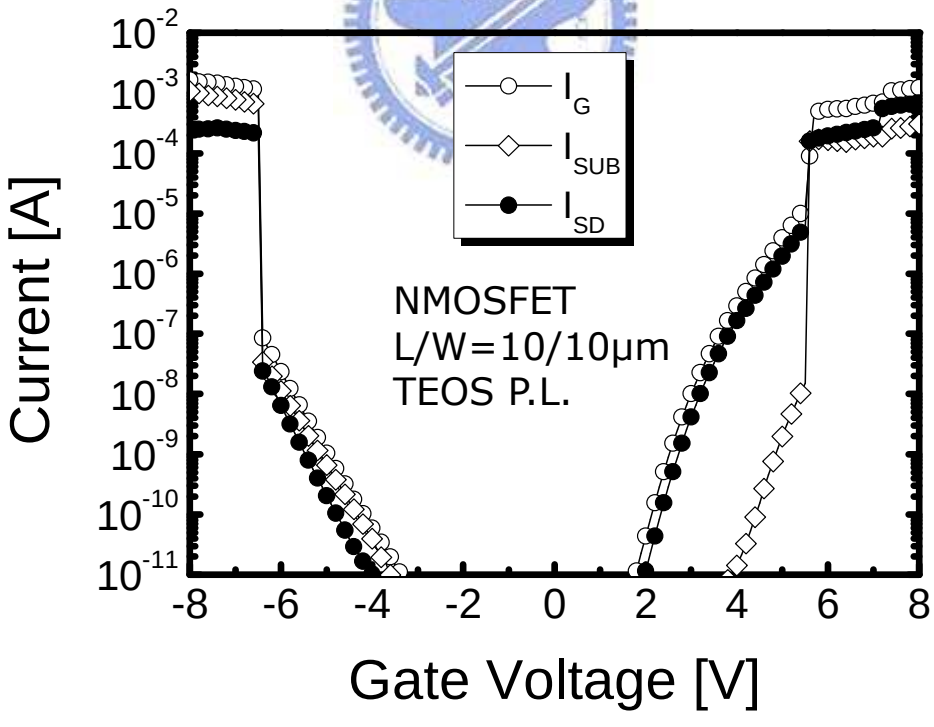


(b)

Fig. 2.22 Carrier separation under (a) inversion region and (b) accumulation region in the TEOS sample.



(a)



(b)

Fig. 2.23 Carrier separation of (a) FSG and (b) TEOS samples under both inversion and accumulation regions.

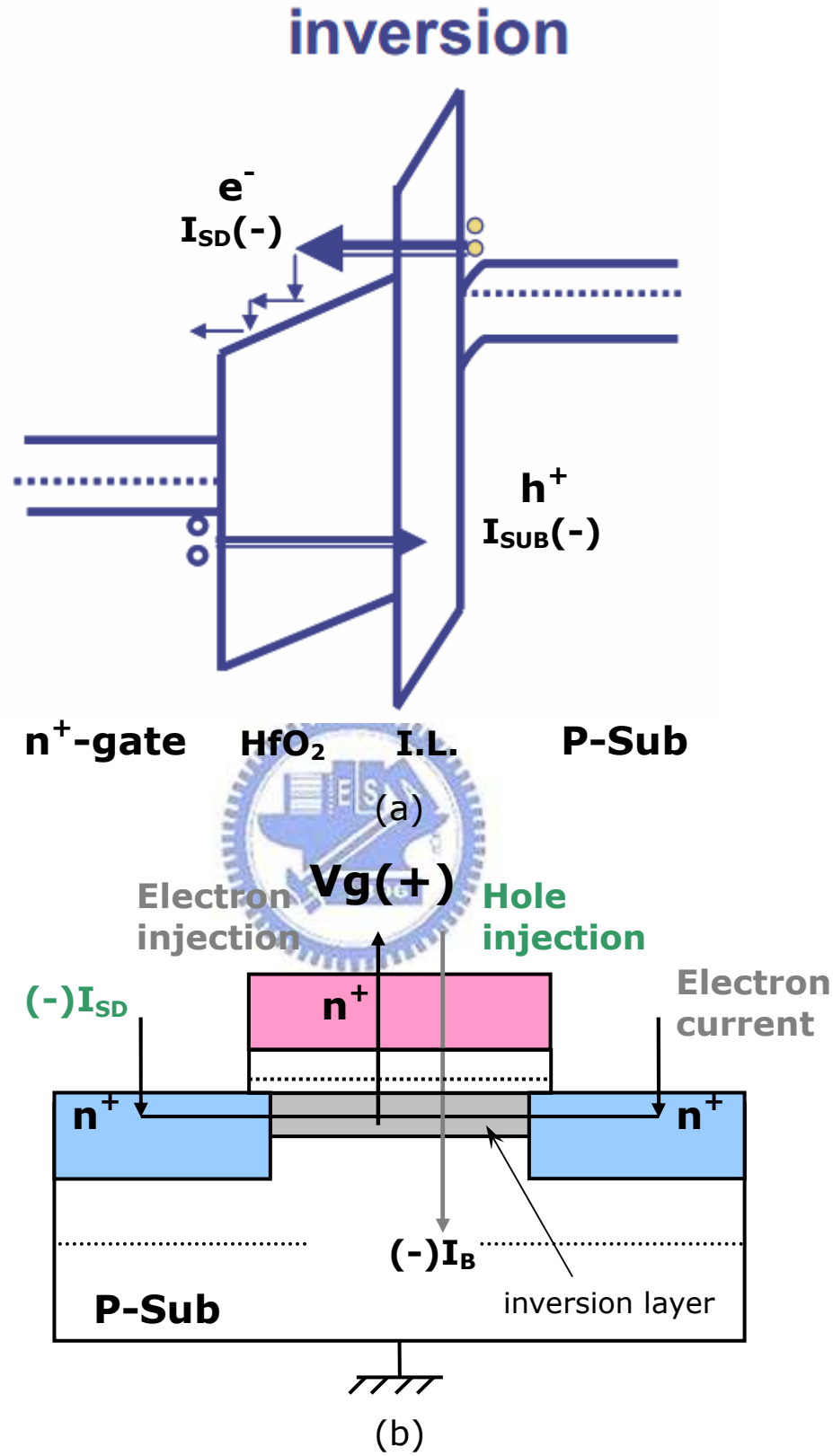


Fig. 2.24 Poly-gate n-MOSFET with HfO_2/SiON gate stack under inversion region (a) band diagrams, and (b) schematic illustration of carrier separation experiment.

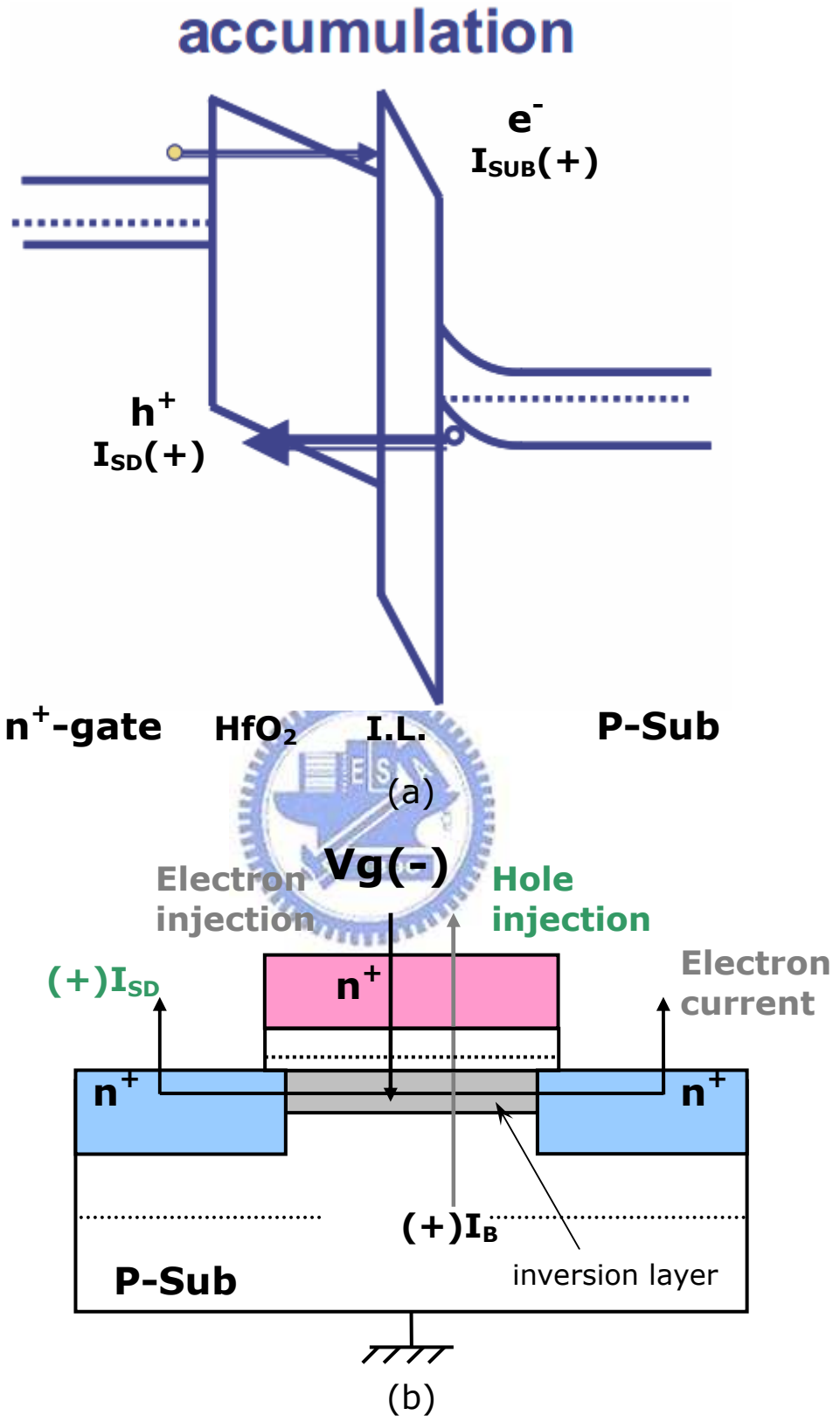
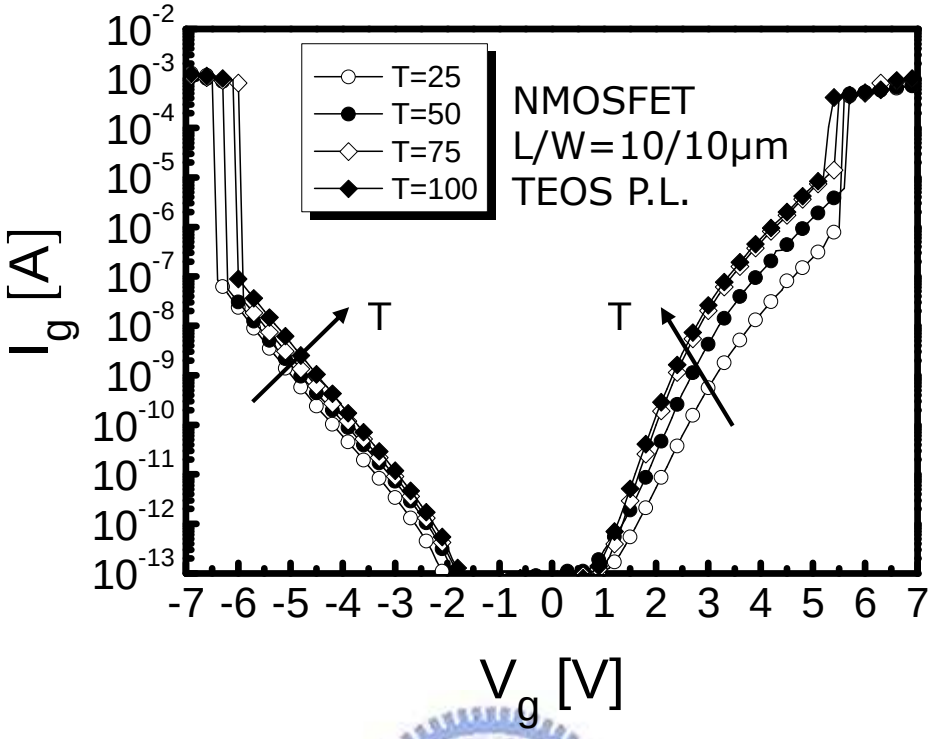
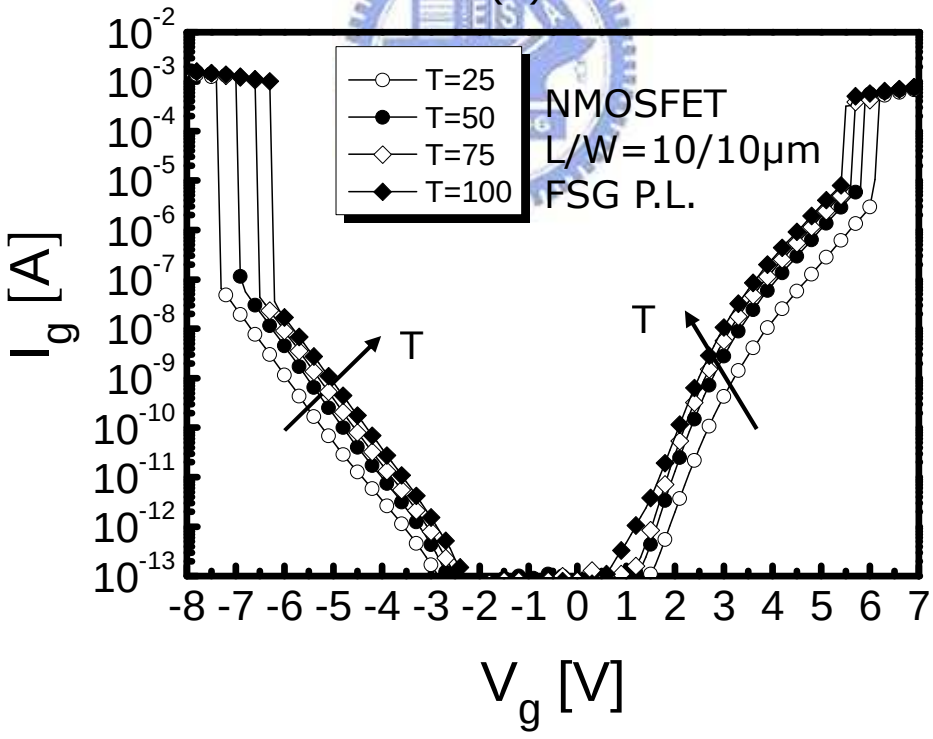


Fig. 2.25 Poly-gate n-MOSFET with HfO_2/SiON gate stack under accumulation region (a) band diagrams, and (b) schematic illustration of carrier separation experiment.

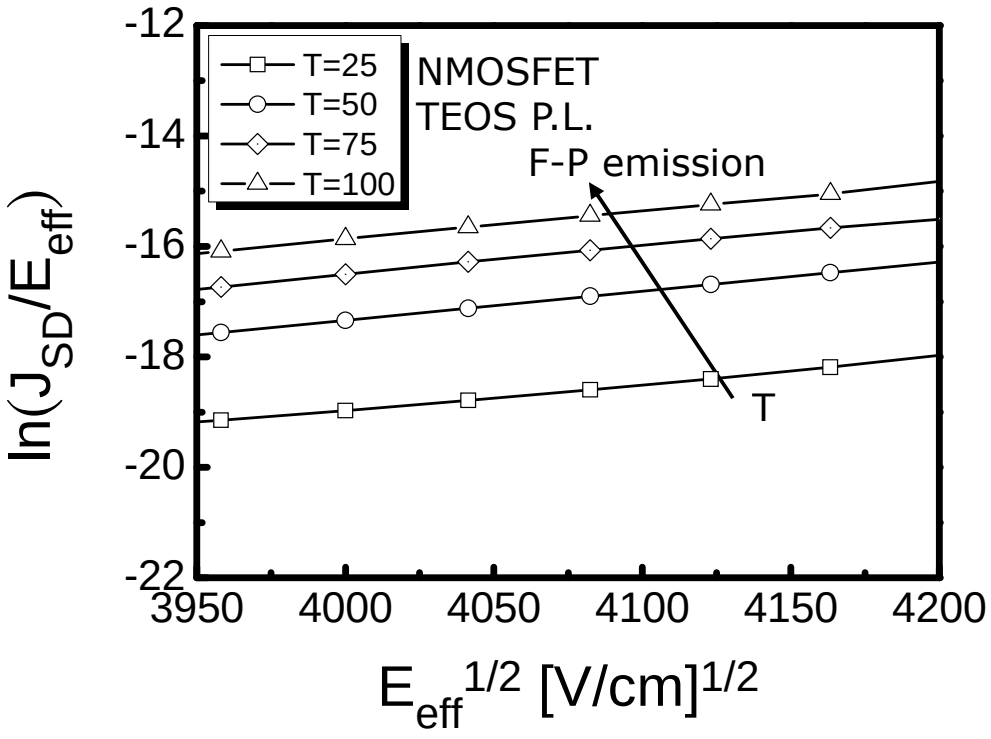


(a)

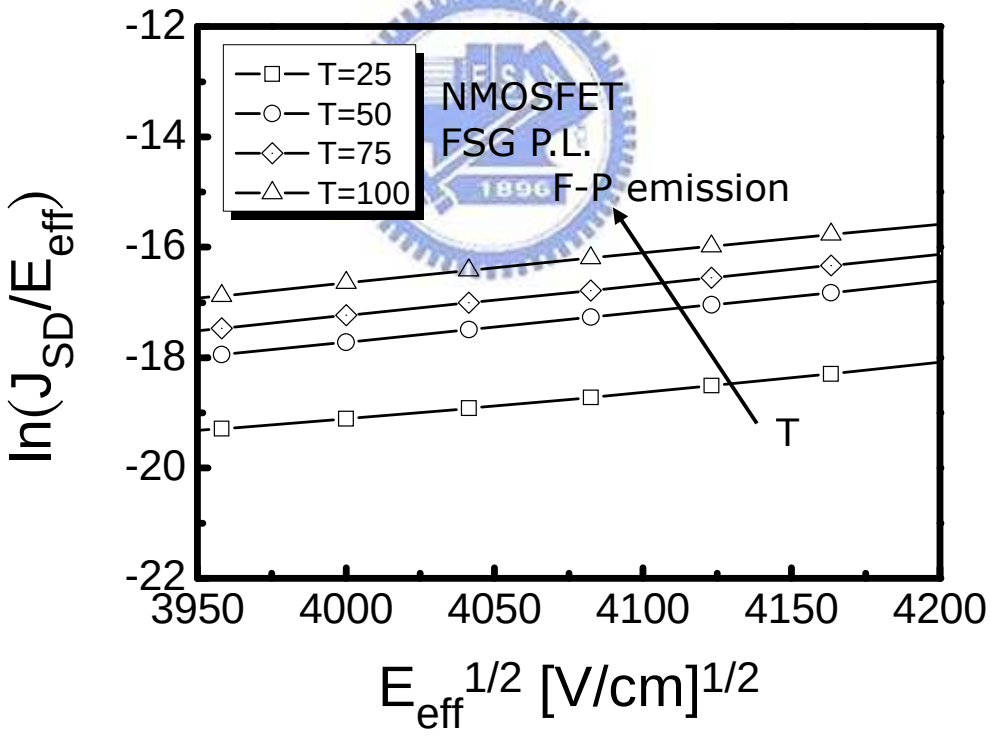


(b)

Fig. 2.26 Gate leakage current versus gate bias for fresh n-channel devices at various temperatures (a) TEOS P.L. (b) FSG P.L..

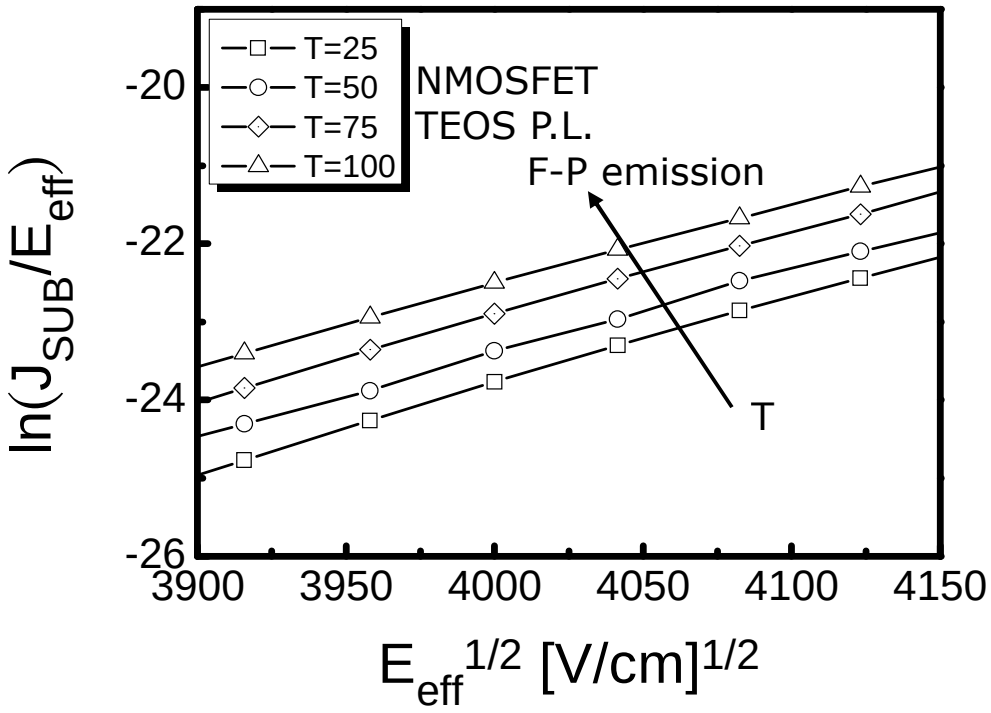


(a)

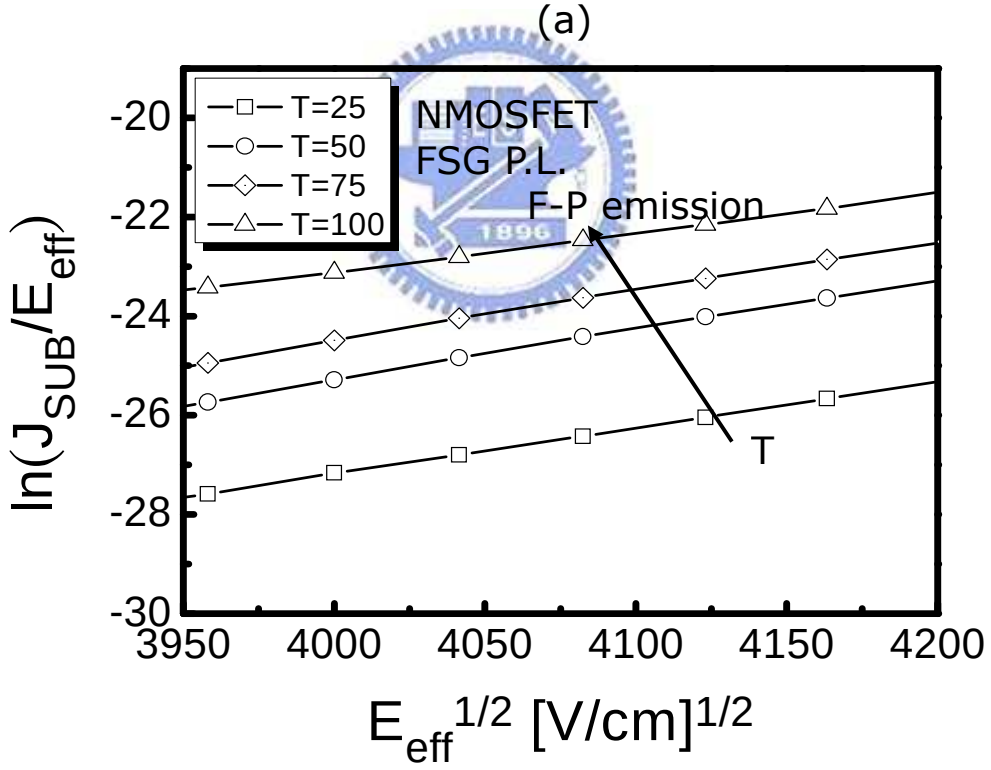


(b)

Fig. 2.27 Conduction mechanism for source/drain current fitting under inversion region (a) TEOS (b) FSG P.L..

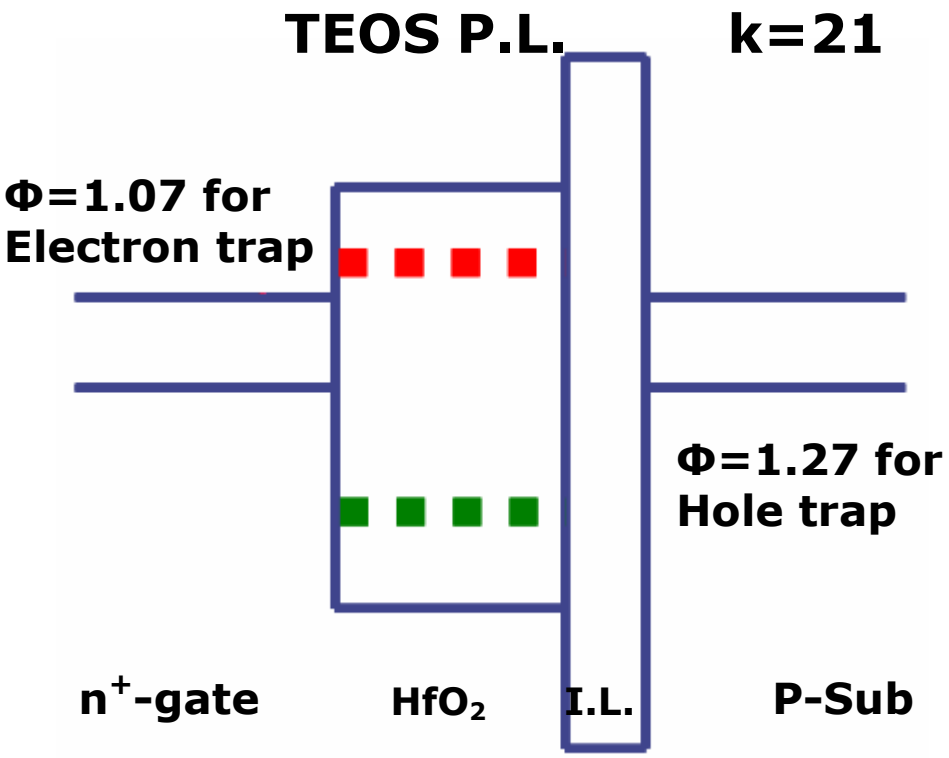


(a)

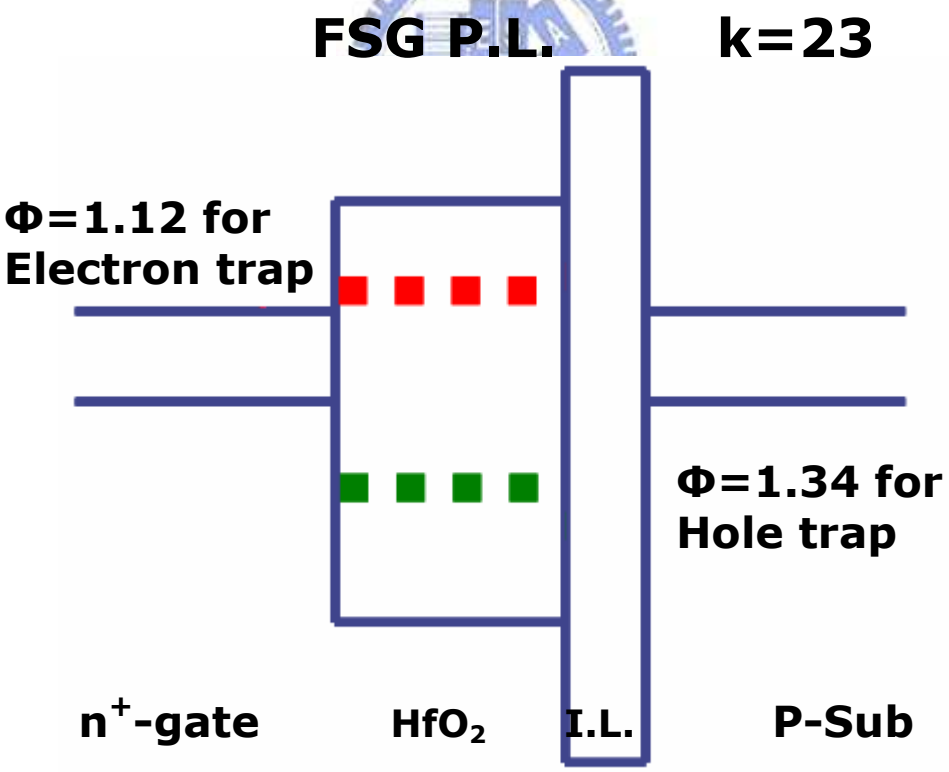


(b)

Fig. 2.28 Conduction mechanism for substrate current fitting under inversion region (a) TEOS (b) FSG P.L..



(a)



(b)

Fig. 2.29 Band diagrams for (a) TEOS and (b) FSG P.L., illustrating the conduction mechanism of Frenkel-Poole emission.

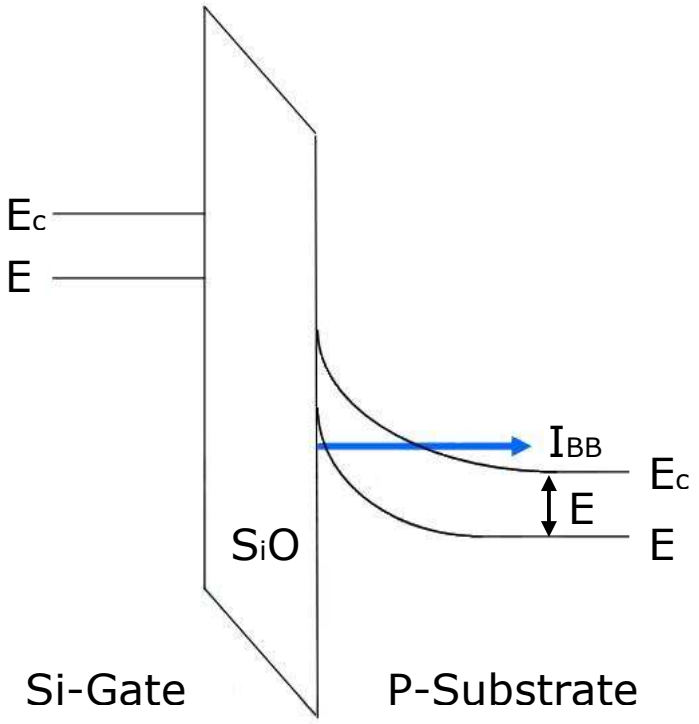


Fig. 2.30 Schematic energy band diagram of the gate-drain overlap region.

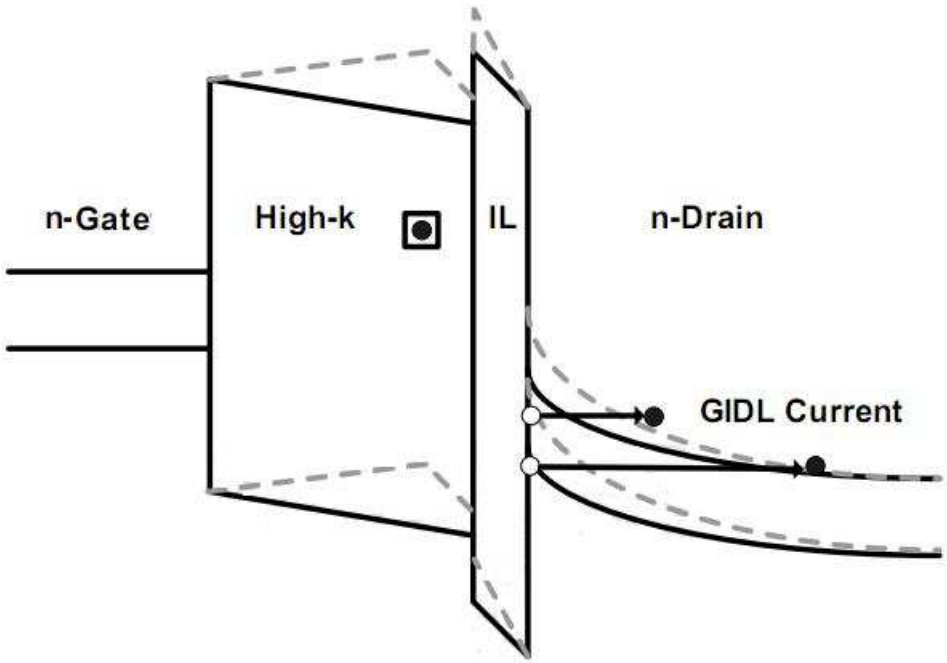


Fig. 2.31 The band diagrams before (solid line) and after (dashed line) capturing electrons by bulk traps.

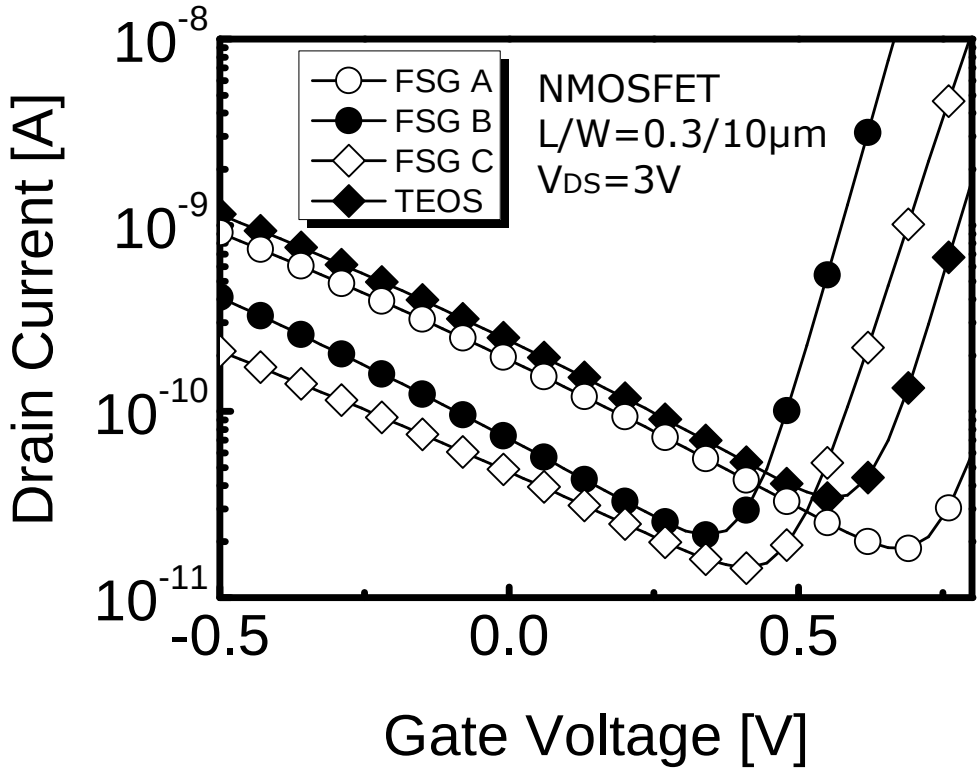


Fig. 2.32 Gate-induced leakage current characteristics of I_D-V_{GS} transfer curves for all splits of NMOSFETs.

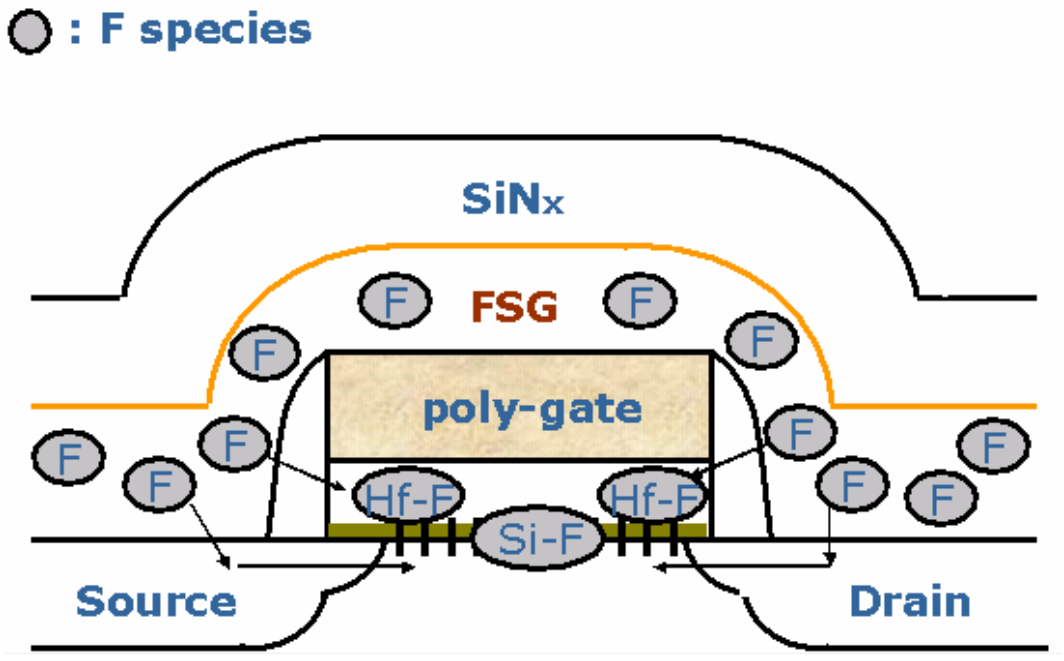


Fig. 2.33 In FSG P.L. devices, a large amount of F atoms incorporating to passivating the bulk and interface trap charges of HfO2/SiON gate stack n-MOSFET.

Critical Electrical Parameters	CET [nm]	V_{Th} [V]	S.S. [mV/dec]	μ_{eff} [cm^2/Vs]	I_{on} [μA]	J_g	N_{it} [$\#/cm^2$]	I-V Hys. [mV]
Control	3.83	1.235	101.3	276	371	--	1.58×10^{11}	150
FSG A	3.79	1.241	95.5	282	404	↓	9.52×10^{10}	120
FSG B	3.94	1.187	91.9	289	444	↓	8.58×10^{10}	100
FSG C	4.21	1.334	91.5	296	480	↓ ↓	7.65×10^{10}	50

Table 2.2 Trend of electrical properties for HfO_2/SiON gate stack n-MOSFET for all splits of different passivation layer.

CHAPTER 03

Reliability Issues of FSG Passivation on HfO_2 Gate Dielectrics

3.1 Briefly Reliability Review

Reliability characteristics of the Hf-based dielectric such as time dependent dielectric breakdown (TDDB), bias temperature instability (BTI), and hot carrier induced degradation (HCI) have been actively investigated in connection with expected application of these materials in the high-k gate stack [1-5]. Threshold voltage (V_{Th}) instability induced by charge trapping has bee recognized as one of the critical reliability issues in Hf-based high-k gate dielectrics, especially for the n-MOSFETs under substrate electron injection conditions (positive bias stress) and V_{Th} degradaion of n-MOSFET PBTI was primarily caused by charge trapping in bulk high-k rather than interfacial degradation [6]. Since the threshold voltage is directly related to the n-MOSFET's on-off characteristics and eventually determines its output power supply voltage for its own purpose. The results from several stress conditions using various voltages and temperatures enable us to evaluate the wear-out behavior of n-MOSFETs as well as the lifetime of devices.

Although one of main issues for high-k gate stack is the charge trapping characteristics during reliability test, a threshold voltage

instability associated with electron trapping/de-trapping in high-k layer [7-12] can significantly affect the transistor parameters and complicate the evaluation of the effects of stress-induced defect generation phenomenon on the high-k gate stacks, which typically is not an issue in the case of SiO_2 dielectrics because the reversible electron trapping, which is less prevalent in SiO_2, can significantly affect transistor parameters [13-14]. The electron de-trapping behavior in the high-k films has been described under specific gate bias conditions identifying charge trapping and relaxation mechanism, and we can also evaluate additional electron trapping effects on top of defect generation by a de-trapping step which has been proposed for studying generation of the electron trapping process and its impact on high-k device reliability [10-11]. As a result, in the Hf-based high-k gate dielectrics, these reversible charge trapping and de-trapping behaviors are highly related to the stress history of previously trapped charge carriers, implying these high-k traps are pre-existing bulk traps [15-16]. For further understanding as mentioned above, we will investigate trapping dynamics of carrier in HfO_2 high-k dielectric n-MOSFETs.

Finally, hot carrier reliability may be one of the major limitations for the implementation of the high-k gate dielectrics. We should consider the concurrent charging of the gate dielectric by the cold channel carriers injected into the dielectric when investigating hot carrier effects on high-k gate dielectrics [17-19]. The cause comes

from which both hot carriers near the drain region of the channel and cold carriers (channel electrons) can be injected and trapped in the high-k layer during HCS. In this chapter, we investigate the characteristics of threshold voltage (V_{Th}) shift during CVS and HCS to find a way to differentiate the contribution of cold carrier trapping and hot carrier injection.

3.2 Effects of Various P.L. on PBTI Characterization

3.2.1 Static and Dynamic Trapping Measurements Setup

To understand the positive bias temperature instability (PBTI), the generation of interface trapp charges (ΔN_{it}) and high-k bulk trap charges (ΔN_B) was extracted by the measured stress time-dependent ΔV_{Th} shifts and charge pumping current change. Fig. 3.1 (a) shows the static PBTI framework of our measurements. The gate electrode of the device was subjected to stress condition with normalized positive bias 0.5V, 1.0V, and 1.5V, respectively, varying from 25 °C to 125 °C, while the source/drain and substrate were all grounded. We measure $I_D - V_{GS}$ and charging pumping during stress intervals. $I_D - V_{GS}$ measurements are used to evaluate time evolution of threshold voltage, swing, transconductance, and charging pumping measurements are used to obtain interface density generation for certain interval time was investigated and compared. The dependence of bulk trap density on stress time has been indicated in section 2.2.2.

To investigate the relaxation chararcteristics, we can observe charge detrapping phenomenon from Fig. 3-1 (b). After changing the negative stress applied for a various duration in the range of 1 ~ 1000 sec, the V_{Th} change is continuously monitored for 1000 sec.

3.2.2 Threshold Voltage (V_{th}) Instability

Firstly, we focus on reliability characteristics of HfO_2/SiON gate stack n-MOSFETs with FSG P.L. compared to TEOS P.L. under constant DC stress condition. Fig. 3.2 and Fig. 3.3 compares the threshold voltage and $I_{D,lin}$ variations as a function of stress time for the control TEOS sample and three splits the novel of FSG n-MOSFETs, respectively. The given normalized stress was 1.0V at room temperature. In order to exclude the difference of in the threshold voltage between samples, normalized positive stress voltage of the gate terminal was used. Very noticeable difference among samples is that the FSG C P.L. shows a reduced V_{Th} degradation compared to the TEOS P.L, and this $I_{D,lin}$ degradation behavior was found to be similar to V_{Th} degradation. The high-k bulk traps (N_B) are an important factor of stress-induced degradation. To prove this degradation, the normalized gate current density during Fowler-Nordheim (FN) stress at $V_{GS} = 4.0V$ is plotted versus stress time for all splits shown in Fig. 3-4. As observed, the normalized gate leakage current density decreases with stress time for both samples, whereas TEOS P.L.

shows a higher rate of J_g decrease than three splits of FSG P.L. devices. This result indicates that there are more high-k defect traps in the high-k bulk of TEOS P.L., causing a higher number of electrons trapped than in that of FSG P.L..

To further gain insights into the degradation mechanism during voltage stressing, the interface state generation, ΔN_{it} , and the increase of the bulk trap density, ΔN_B , are shown in Fig. 3-5. Apparently, ΔN_B is significantly larger than ΔN_{it}, suggesting that the degradation under PBS is dominated by the charge trapping in the bulk of HfO_2 film, rather than the generation of interface states, irrespectively of whether CF_4 gas is introduced or not. Q_{BD} Weibull distribution of all samples stressed at 5.9V constant voltage stress is shown in Fig. 3-6. Between three samples introduced various flow rate of CF_4 gas, this bulk trap generation is correlated with the amount of the fluorine from CF_4 flow, which especially FSG C sample showed much reduced N_B shift. And it can clearly be seen that FSG C sample exhibits significant higher Q_{BD} for positive bias stress but the difference between TEOS sample and the others is small. Therefore, we regard FSG C P.L as the optimum FSG P.L. because the good correlation between trapping and breakdown results indicates that this improvement can be attributed to reduce electron trapping rate and weak bonds replacing by strong bonds in gate stack dielectric, and further we investigate also the effects of reliability between

optimum FSG P.L and TEOS P.L..

Fig. 3-7 shows the transconductance degradation ratio as a function of stress time. Basically the trends are similar to those shown in previous figure. The transconductance degradation ratio for TEOS P.L. depicts the severest degradation among all splits, reaching 28.6% after 1000 sec at $V_{GS} - V_{Th} = 1.0V$. However, the transconductance degradation is alleviated for optimum FSG P.L. device. The results clearly indicate that the use of TEOS passivation layer may aggravate PBS, while the FSG passivation layer can be helpful to mitigate the situation. Fig. 3-8 shows the time dependences of the threshold voltage degradation under various positive bias stress voltages at room temperature for optimum FSG and TEOS devices. This result indicates that quantity of electron trap sites was increased with gate bias. It is apparent that ΔV_{Th} obeys a power-law dependence on stress time, as given by Equation (3-1) :

$$\Delta V_{Th} \propto t^n \qquad (3\text{-}1)$$

where the exponent value n, which dependent relative to bulk trap generation, is found to be ~0.2 and ~0.5 at $V_{GS} - V_{Th} = 0.5V$ for optimum FSG and TEOS n-MOSFETS, respectively. For optimum FSG device, the threshold voltage degradation by PBS stress is obviously lower than that for TEOS device under various stress voltages. As an effect of F incorporation, this indicates that pre-existing defects were reduced and stress induced defects which were generated in the

high-k film could be alleviated. As shown Fig. 3-9, compared with TEOS sample, FSG sample indeed suppressed the generation of both ΔN_{it} and ΔN_B, especially ΔN_B. The improvement may be due to fluorine atoms from CF_4 gas, similar to nitrogen atoms, form complexes at the interface and dielectric, which reduce the total number of available Si-H bonds, and passivate the bulk trap, leading to less PBS degradation.

It can be seen that $I_D - V_{GS}$ curves shift toward more positive voltage at 125 °C compared to room temperature for both the FSG and TEOS P.L. devices, as shown in Fig. 3-10 (a) and (b), respectively. Further, V_{Th} shift of the TEOS sample is clearly larger. Fig. 3-11 shows the V_{Th} shift as a function of stress time at temperatures ranging from 25 °C to 125 °C. The V_{Th} shift induced by charge trapping increased exponentially with temperature. This stress induced defect generation could be observed with temperature acceleration. Since PBTI was thermally active, electron trap site generation was also accelerated by heating. Fig. 3-12 shows ΔN_{it} and ΔN_B as a function of time during PBTI for both devices measured at different temperatures. It can be seen that optimum CF_4-introduced device always show smaller both ΔN_{it} and ΔN_B than the TEOS device at all temperatures. To compare with positive bias stress at 25 °C in Fig. 3-8, PBTI-induced threshold voltage degradation, ΔN_{it} and ΔN_B as a function of stress time under various positive bias stress voltages at

100 °C for optimum FSG and TEOS n-MOSFETs are show in Fig. 3-13 and Fig. 3-14. The threshold voltage and charge trapping of bulk and interface degradation for both samples are similar to PBS at 25 °C, indicating the power-law dependence and the optimum FSG P.L. immunity to PBTI that is higher than the TEOS P.L. immunity under various stress overdrive voltages in the range from 0.5 to 1.5V. Fig. 3-15 compares the PBT-stress-time dependence of threshold voltage shift for HfO_2/SiON gate stack with optimum FSG P.L. and with TEOS P.L.. A significantly smaller V_{Th} shift is observed for the optimum FSG sample under the BT stress, $V_{GS} - V_{Th} = 0.5V$ at 25 °C and 125 °C. The exponential values of both samples at 125°C are 0.4 for TEOS sample and 0.2 for FSG sample but 0.5 for TEOS sample and 0.2 for FSG sample at 25 °C. Fig. 3-16 show ΔN_{it} and ΔN_B as a function of stress time during PBTI both devices measured at 25 °C and 100 °C. It is found that for both devices, V_{Th} degradation during PBTI stressing is primarily caused by the charge trapping in bulk HfO_2, rather than the interfacial degradation. Note that the activation energy of ΔV_{Th} in PBTI degradation for FSG P.L. is larger than for TEOS P.L. as shown in Fig. 3-17. This indicates that, thermally induced defects were increased as an effect of F incorporation. In addition, the activation energy of ΔV_{Th} is lower than that of ΔN_{it}, indicating that V_{Th} instability is not simply contributed by interface tarp generation, but mainly comes from the more significant charge trapping in the bulk of high-k dielectric as

shown in Fig. 3-18. All results are consistent with the effectiveness of fluorine incorporation from CF_4 gas in alleviating the PBT instability.

3.2.3 The Characteristics of Charge De-trapping

The threshold voltage was shifted to positive direction due to negative charges built up within the HfO_2 shown in Fig. 3-10. Parallel shift of $I_D - V_{GS}$ curve indicates that the interface qualities are not degraded significantly despite of significant electron charging. Interestingly, after relaxation voltage $V_g = -2V$, a rapid turn around of V_{Th} shift was observed in Fig. 3-19. Therefore, we can conclude that the electron trapping/de-trapping occurs on the pre-existing ("as-grown") defects due to no noticeable degradations of the interface electrical property. As shown in Fig. 3-20 shows the threshold voltage shift of the HfO_2/SiON high-k gate stack n-MOSFETs for optimum FSG P.L. and TEOS P.L. samples as a function of the static stress/relaxation time with a fixed stress voltage $V_{GS} - V_{Th} = 1.5V$ and relaxation voltage $V_{GS} = -2V$. Basically, the relaxation voltage plays a significant role to clean up the trapped charge carriers before the next stress cycle. It was also indicated that an charge de-trapping behavior can not cause an additional V_{Th} instability because the threshold voltage was still shifted above the initial V_{Th} for both samples. After relaxation, a subsequent stress-induced V_{Th} increase follows the initial pre-relaxation stress time dependence. It is clear that this

relaxation does not fully recover the V_{Th} shift caused by the positive bias stress. The residual V_{Th} shift appears to be determined by the balance between the built-in potential due to trapped charges and the barrier height for de-trapping [20].

Based on the observations above, a model explaining V_{Th} instability behavior during the stress and relaxation can be proposed as shown in Fig. 3-21. The signs of A and B in Fig. 3-22 are defined by de-trapping ratio and residual-trapping ratio, respectively. There are two factors to shift V_{Th} during the stress. One is electrons filling the existing traps and the other is the charged damages created during the stress. Portion of the former electrons was de-trapped spontaneously to reduce the instant built-in potential after the stress was removed. However still there are some amount of trapped electrons and charged damage remaining. We can observe that a lot of trapped electron is significant to be instantly pulled out from the pre-existing traps and the created traps are also obviously decreased for the TEOS sample during de-trapping bias, resulting in a few of the residual electrons ("B_T part in Fig. 3-20") and a number of reversible electrons ("A_T part in Fig. 3-20"), as shown in Fig. 3-21 (a). However, a little of trapped electron is de-trapped from the pre-existing traps even if the created traps was effective to decrease for the optimum FSG sample shown in Fig. 3-21 (b), which $B_F > B_T$ in the residual charges characteristic and $A_F < A_T$ in charge de-trapping

characteristic. It indicates that some of deep traps filled or created due to fluorine effect resulting in trapped electrons suffering from the higher barrier height of detrapping behavior during relaxation cycle for the optimum FSG P.L.. As mentioned previous, it was associated with the good correlation of the barrier height between de-trapping behavior and F-P emission results for both samples. The other possible explanation for this phenomenon is larger CET for the optimum FSG P.L than the TEOS P.L.. This CET layer could be source for charge storage, resulting in storing significant amount of trapping in addition to the existing trap for the optimum FSG P.L. shown in Fig. 3-22. The A_T (or A_F) represents charge trapping related defect level which causing threshold voltage shift, so we can understand defect generation of HfO_2/SiON gate dielectric with the optimum FSG P.L. is much less than the TEOS P.L. in operation mode.

3.3 Reliability Impact of various P.L. on HCS

3.3.1 HCS Measurement Setup

In HCS reliability measurements, devices were stressed with the drain voltage set at a highly positive voltage, and the gate terminal was biased at the voltage where maximum absolute value of I_{SUB} occurred to accelerate the degradation. To find the condition, we first measured the $I_{SUB} - V_{GS}$ characteristics with drain terminal biased at a given voltage. Besides, In order to identify the worst degradation

condition, $V_{GS} = V_{DS}$ (channel hot electron, CHE) was used to monitor the degradations of our devices for hot electron stressing. To monitor the hot electron degradation, both the $I_D - V_{GS}$ characteristics at V_{DS} = 50 mV (linear region) and charge pumping current were measured before and after the stress. The degradations in terms of threshold voltage shift (ΔV_{Th}), generation of interface trap density (ΔN_{it}), bulk trap density degradation (ΔN_B) and so on, were examined and recorded in the accelerated stress test.

3.3.2 Cold and Hot Carrier Charge Trapping Effect

Substrate current is an important factor to determine how much hot carriers are generated and injected during hot carrier stress. A hot carrier with sufficient energy can create more charge carriers through impact ionization. For n-MOSFET devices, holes generated by impact ionization are collected by the substrate. The substrate current (I_{SUB}) versus gate voltage for both samples of devices at V_{DS} of 2.5V is illustrated in Fig. 3-23. From the figure, we can clearly see the TEOS P.L. exhibits larger substrate current than the the optimum FSG P.L. in our devices. Such phenomenon is closely related to the incorporation of fluorine atoms forming stronger Si–F bonds near the source and drain sides instead of weaker Si–H and Si–Si bonds to enhance the interface hardness between HfO_2/SiON and silicon as well as the immunity against hot-carrier stress due to the inhibition of the

channel avalanche multiplication of hot carriers. Hot-carrier effects and associated performance degradation were investigated to evaluate the impacts of various passivation layer such as optimum FSG and TEOS dielectrics. Thus, we easily try two conditions $V_G = I_{SUB,Max}$ and $V_{GS} = V_{DS}$ to obtain the most serious degradation. Threshold voltage shift and captured traps density (including interface traps and bulk traps) increase as a function of stress time for both samples are shown in Figs. 3-24 and 3.25, respectively, after receiving a hot-carrier stressing at V_{DS} = 2.5 V and V_{GS} at the maximum value of substrate current. The larger degradation which happens at $V_{GS} = V_{DS}$ and also get similar case in many papers [21]. Most of high-k material devices which HCS induces aggravated degradation occur in $V_{GS} = V_{DS}$. This tells us that the degradation is caused mainly by the stress magnitude applied by gate voltage. Not to determinate by maximum substrate current. Therefore, we attain larger threshold voltage shift and huge captured traps variations with $V_{GS} = V_{DS}$ condition.

Typical results of hot-carrier stressing for the optimum FSG P.L. and TEOS P.L. devices are shown in Figs. 3.26 and 3.27, respectively, which are stressed at V_{DS} = 2.5 V and V_{GS} at maximum value of substrate current. It is expected that the TEOS P.L. will exhibit aggravated hot carrier degradation as mentioned previous, while the improvement of the hot-carrier degradation by using the FSG P.L. is

obviously seen. Since the hot carriers tend to break the Si-H bonds during the stressing, and much severe degradation will occur with the TEOS P.L. sample. The use of the optimum FSG P.L. can effectively suppress interface damage near the drain side due to the stronger Si-F bonds formation which are less easily broken than Si–Si and Si–H bonds under hot-carrier stress, therefore, and less HCS degradation in terms of threshold voltage shift, interface states, and bulk traps generation is achieved. Consequently, the aggravation is alleviated in the devices with optimum FSG passivation layer.

Besides, Fig 3-28 and 3-29 show the comparison HCS with PBS. In hot-carrier stressing at $V_{GS} = V_{DS}$, we observe that not only larger interface state and bulk trap density shift but also more serious threshold instability represent with PBS. However, HCS when V_{GS} at the maximum value of substrate current has the least interface state degradation of the others conditions, indicating the interface state degradation increases with the gate voltage. This phenomenon was observed with the formation of hot electrons resulting in much more electrons trapping in bulk traps despite $I_{SUB,Max}$ being indication of less electron trap in high-k bulk.

Finally, total threshold voltage shift during a hot carrier stress is a sum of contributions from both hot carrier and cold carrier effects. Cold carrier contribution is shown to be reversible and, therefore, it does not introduce permanent damage. The contribution from the cold carrier can be evaluated by applying a de-trapping (opposite

polarity) bias after the stress. On the other hand, since the hot carrier damage is permanent, it cannot be reverse by application of a voltage, which polarity is opposite to the one of the stress – parameter shift keeps growing with each additional stress cycle. Thus, at the same gate bias, HCS appears to induce a larger positive ΔV_{Th} shift than PBS shown in Fig. 3-30 and 3-31 for the TEOS and optimum FSG samples, respectively, pointing to the contribution from the hot electrons. From Fig. 3-30 and 3-31, cold carrier induced threshold voltage shift is repeatable during PBS and HCS, and a residual HCS V_{Th} shift increases with every cycle, indicating an increase in HCS-induced degradation. After the de-trapping cycle, amount of recovery induced by cold carrier are similar during HCS and PBS. Since total threshold voltage shift is the combination of both cold and hot carrier contribution, threshold voltage shift is greater in TEOS device than FSG device, partly due to more electron charge trapping effects, which indicates that most of the V_{Th} shift was related to the transient charge trapping within the bulk of high-k dielectrics [20,22]. Based on –2V de-trapping process, FSG device shows more residual threshold voltage shift than TEOS device, indicating FSG device has less cold carrier effects or a lower relaxation ratio but induces more hot carrier induced damage during HCS.

3.4 Summary

In this chapter, a novel CMOS compatible fluorine incorporation

into high-k technology and reliability characteristics has been successfully demonstrated. We observe that serious degradation such as interface state, bulk trap density and threshold voltage shift occurs in the TEOS P.L. sample. The CF_4-introduced silicon oxide as a FSG passivation layer showed improved reliability characteristics under the PBTI and HCS. It is believed that the HCS and PBTI degradation are related to the electron traps in gate dielectrics. PBTI was found to be mainly caused by bulk trapped generation rather than the generation of interface trapped charge. The worst-case degradation of HCS occurs at $V_{GS} = V_{DS}$ stress condition. The hot carrier contribution induces permanent damage while cold carrier contribution is shown to be reversible. Fig.3-32 shows that the longer time-to-breakdown (T_{BD}) for the FSG P.L. sample is primarily attributed to its less electron trapping to the dielectric and thus contributes to a longer dielectric lifetime. Fig. 3-33 shows the dependence of lifetime (using the E-model) from PBTI on n-MOSFETs with both samples at 25 °C and 100 °C. The PBTI lifetime (degradation criterion: 30mV V_{Th} shift) improvement for device with the FSG P.L., as compared to the TEOS P.L.. The FSG P.L. sample leading to the formation of stronger Hf-F and Si-F bonds compared to Hf-H and Si-H bonds reduced charge trap generation rate. These stronger bonds result in less interface states generation and charge trapping under PBTI and HCS, which promotes better hot-carrier and PBTI immunity against stress, as shown in Fig. 3-34.

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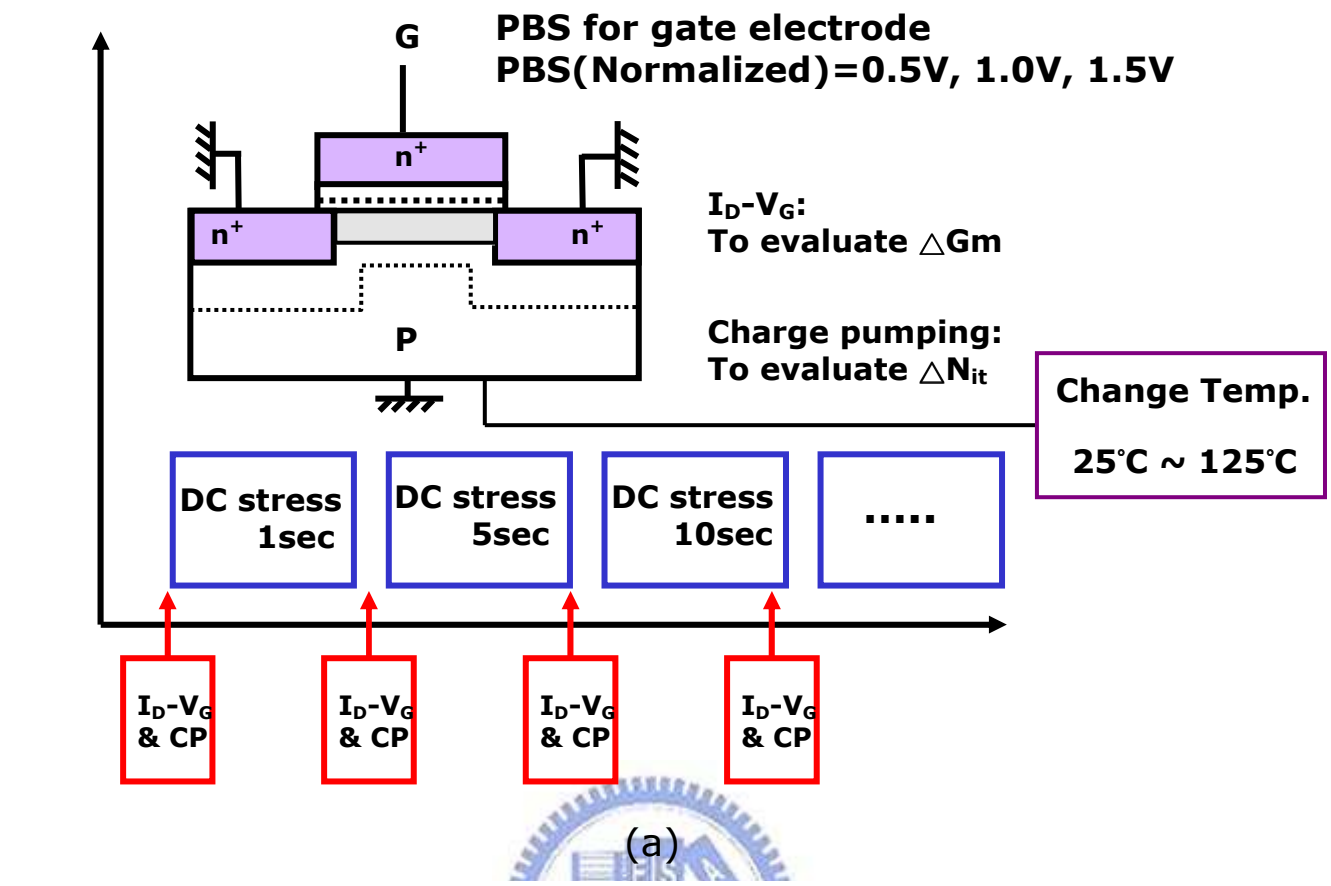
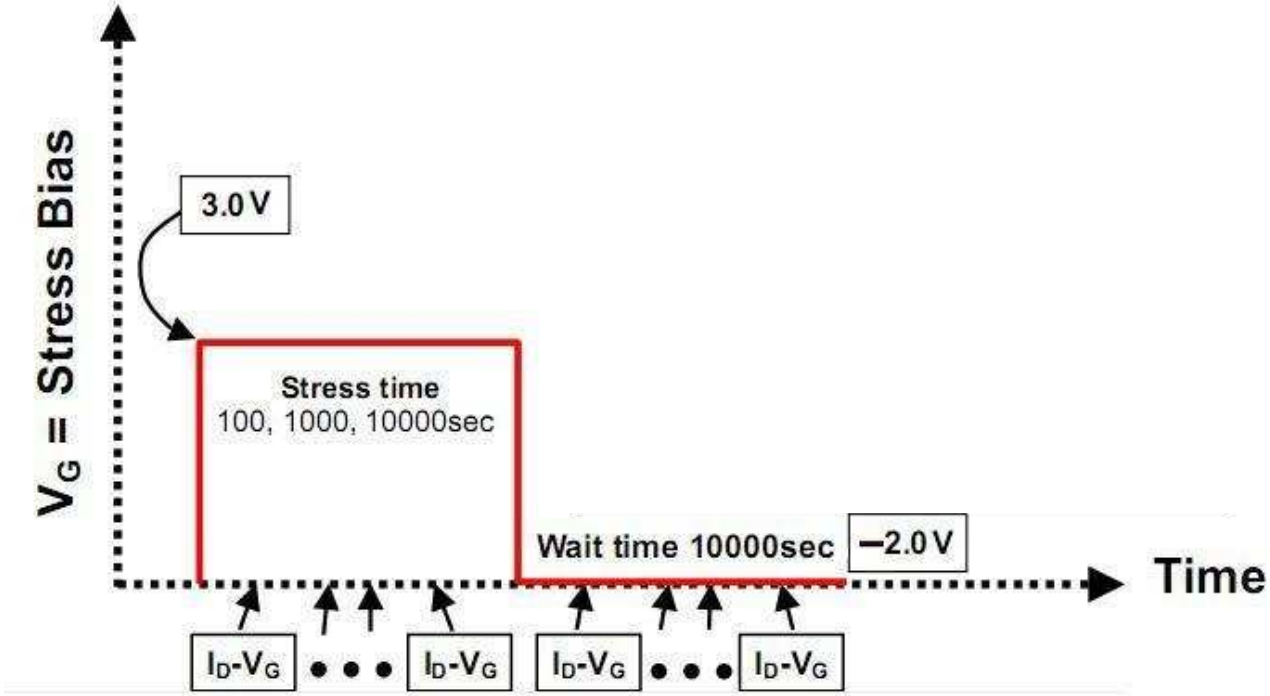


(a)



(b)

Fig. 3.1 Schematic of measurement setup for (a) static PBTS (b) dynamic trapping.

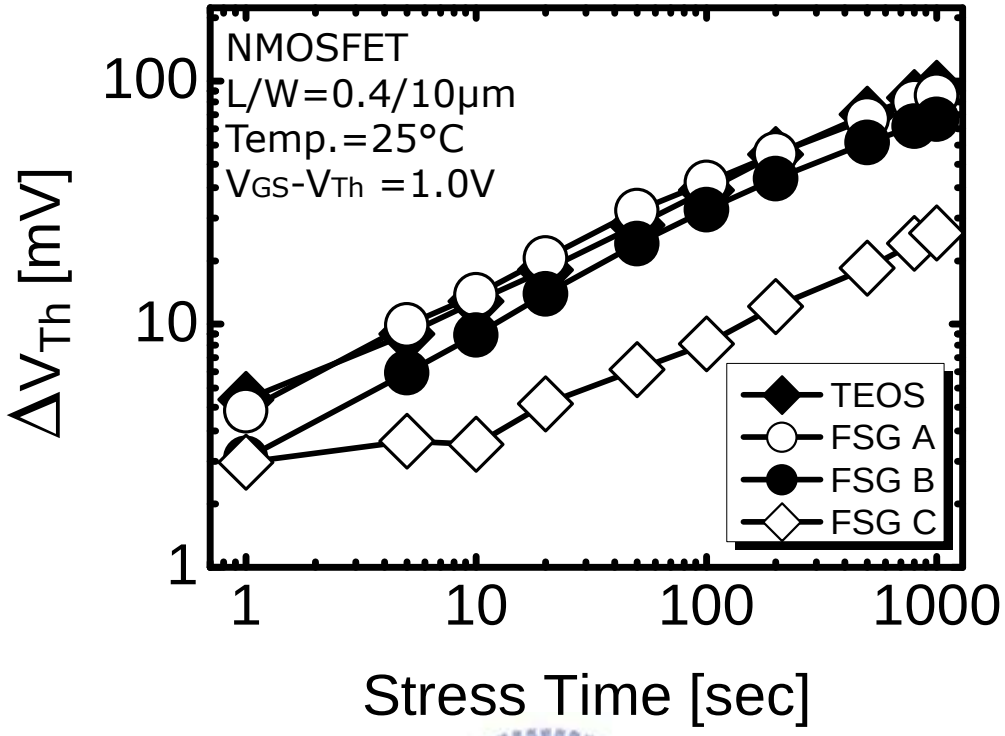


Fig. 3.2 PBT-stress-time dependence of ΔV_{th} for TEOS and FSG having different flow rate of CF_4 gas at 25°C.

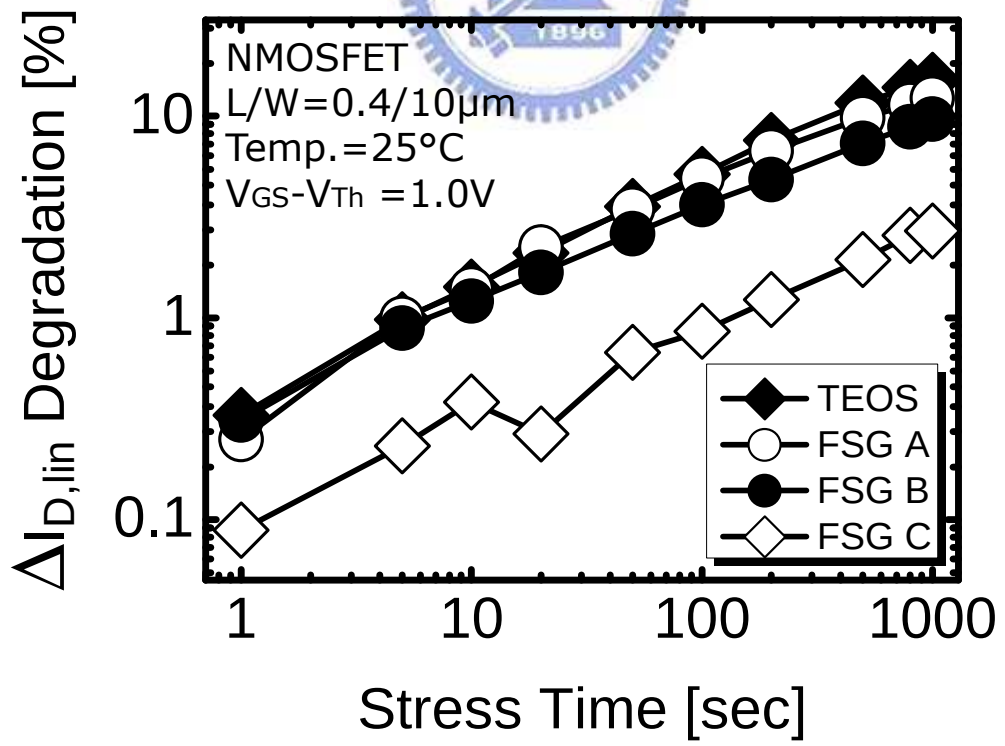


Fig. 3.3 PBT-stress-time dependence of ΔV_{th} for TEOS and FSG having different flow rate of CF_4 gas at 25°C.

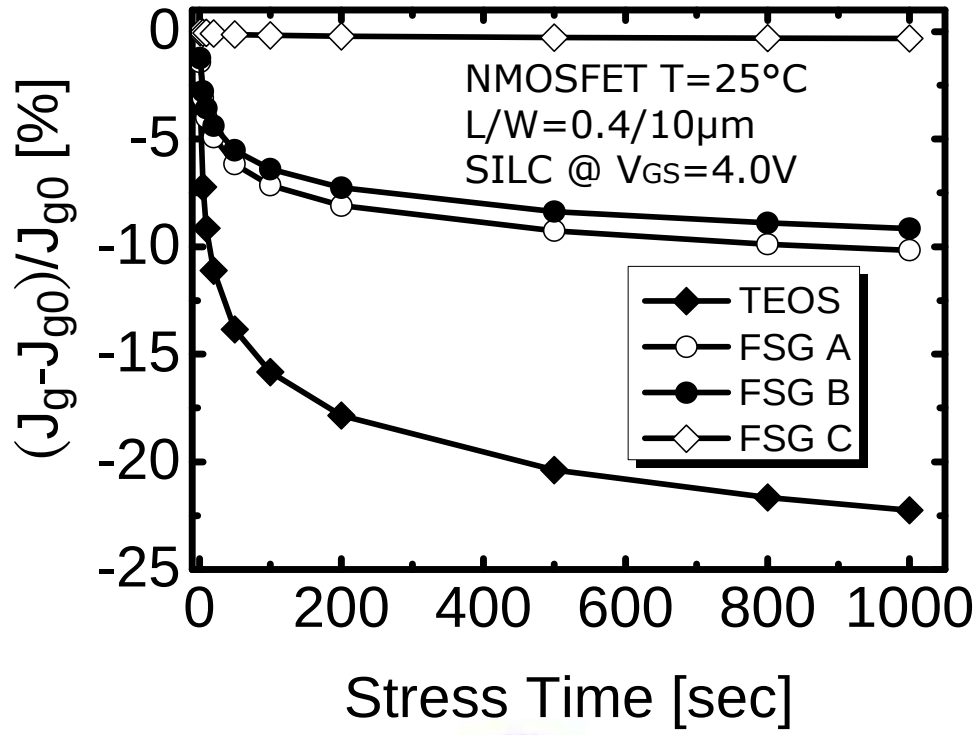


Fig. 3.4 The normalized gate current density ($(J_g-J_{g0})/J_{g0}$) at a constant gate voltage of 4.0V versus stress time of all splits.

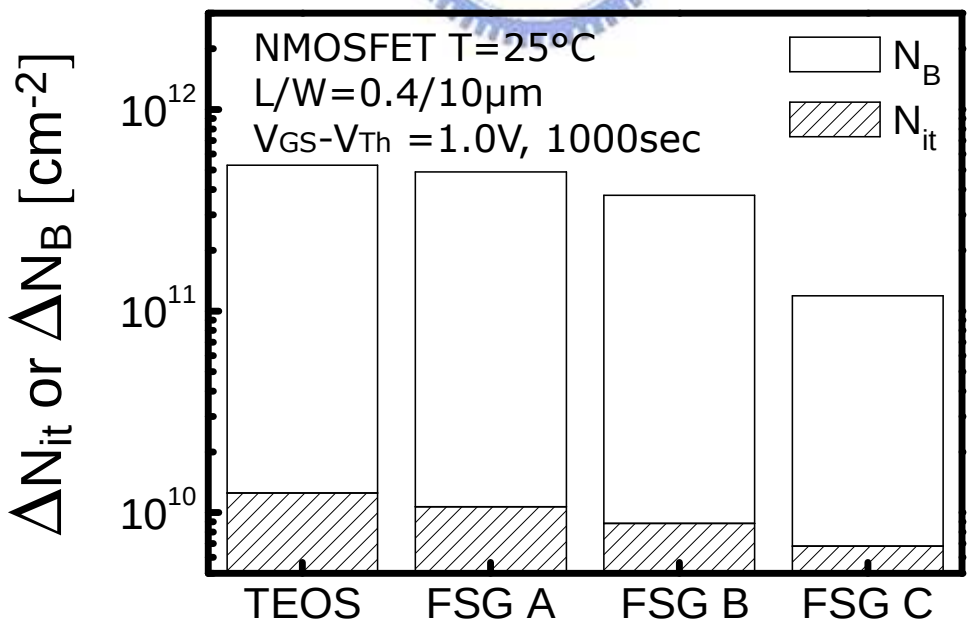


Fig. 3.5 Separation of total capatured trap density into ΔN_{it} and ΔN_B component for all splits after 1000s PBT stress.

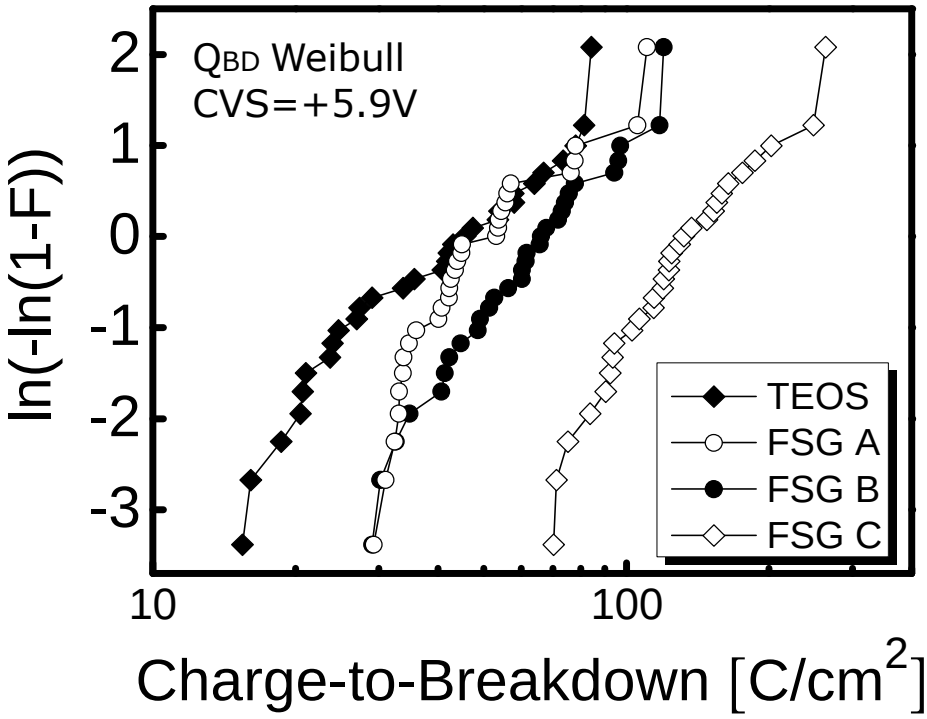


Fig. 3.6 Weibull plot of charge-to-breakdown for all samples under a constant voltage stress of 5.9V.

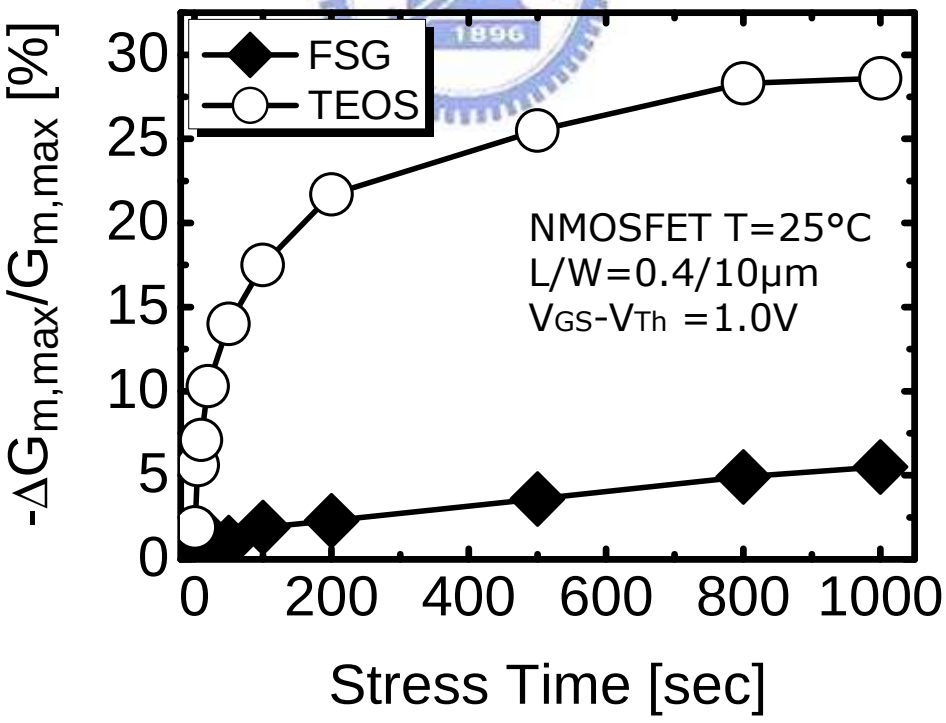


Fig. 3.7 Transconductance degradation versus stress time for both samples with V_{GS}-V_{Th}=1.0V at 25°C.

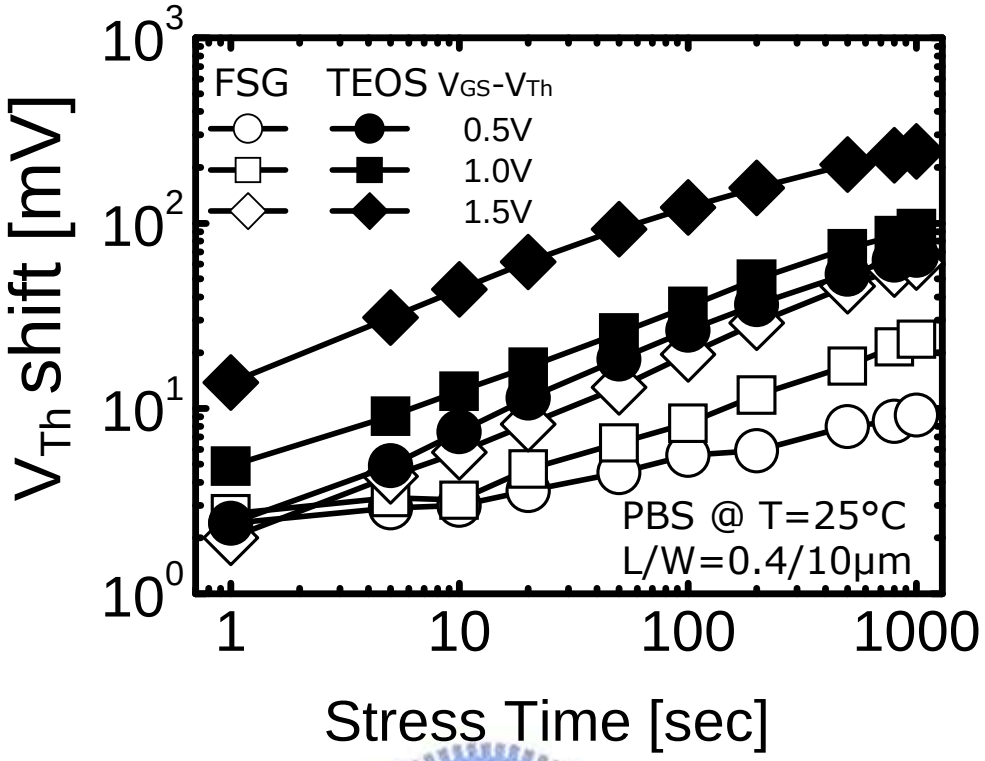


Fig. 3.8 Time dependences of PBS-induced V_{th} degradation at various normalized stress biases from 0.5 to 1.0 per steps of 0.5V at 25°C.

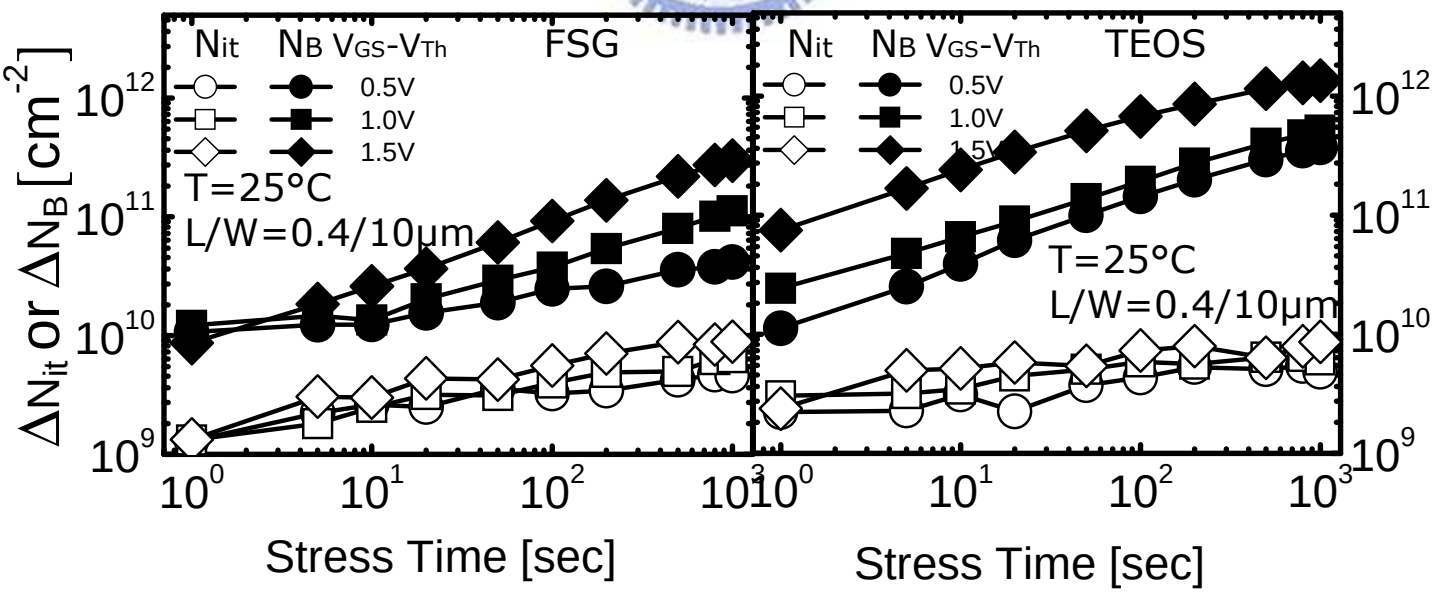
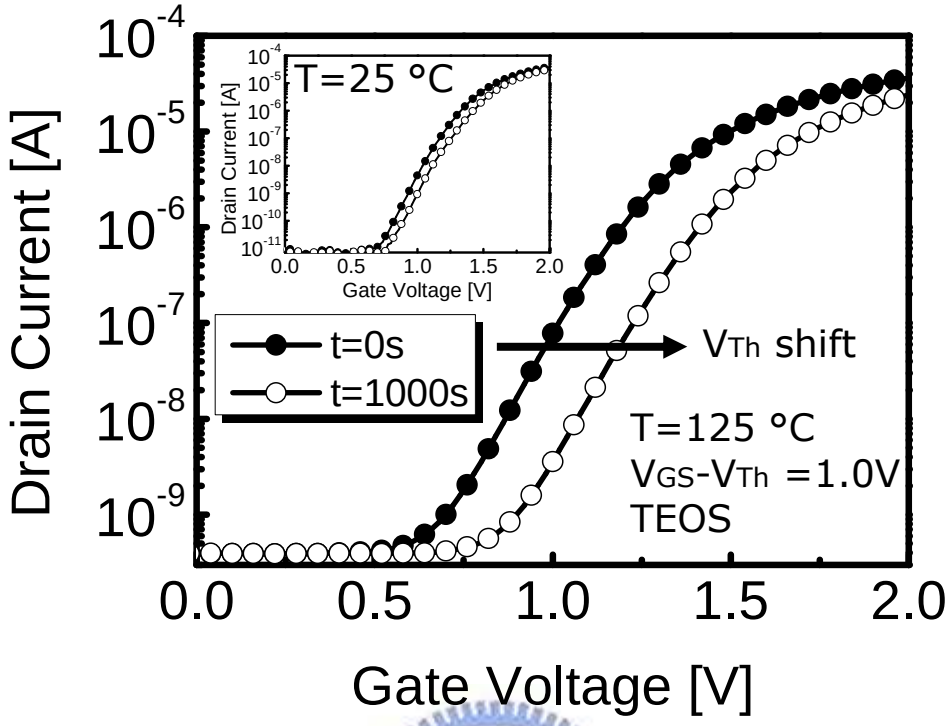
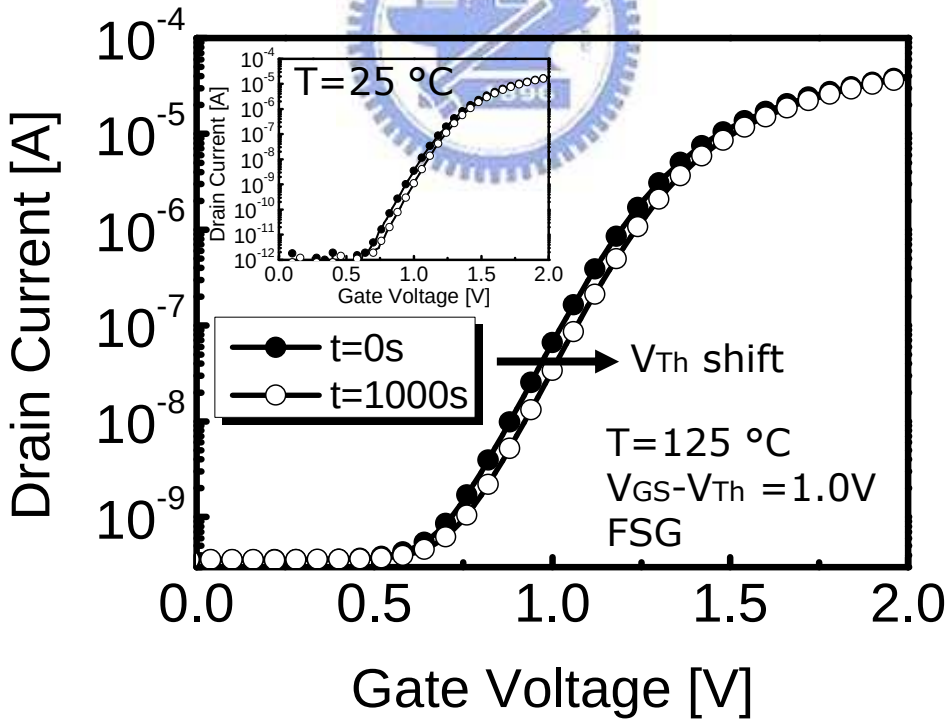


Fig. 3.9 Time dependences of PBS-induced N_{it} and N_B degradation at various normalized stress biases from 0.5 to 1.0 per steps of 0.5V at 25°C.



(a)



(b)

Fig. 3.10 I_D-V_{GS} characteristics for HfO_2/SiON n-MOSFETs before stress and after stress 1000s at 125°C (a) TEOS P.L. (b) FSG P.L. sample.

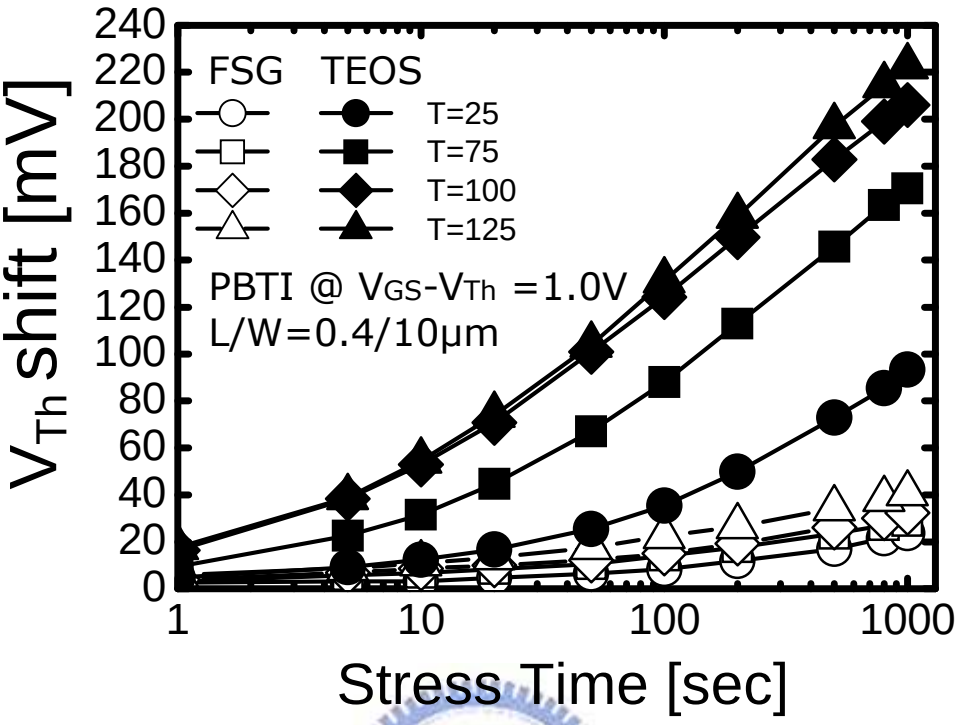


Fig. 3.11 Threshold voltage shift as a function of stress time under +1.0V normalized gate bias voltage at various temperatures.

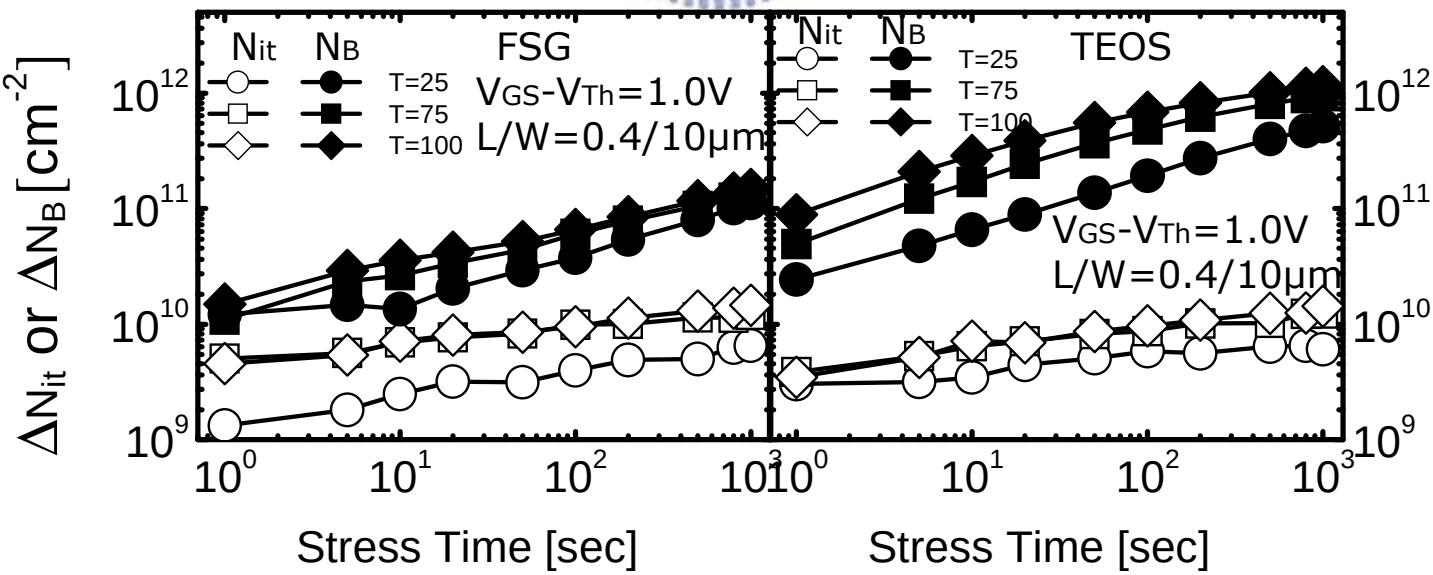


Fig. 3.12 Interface trap density and bulk trap density shift as a function of stress time under BTS at different stress temperature, V_{GS}-V_{Th}=1.0V.

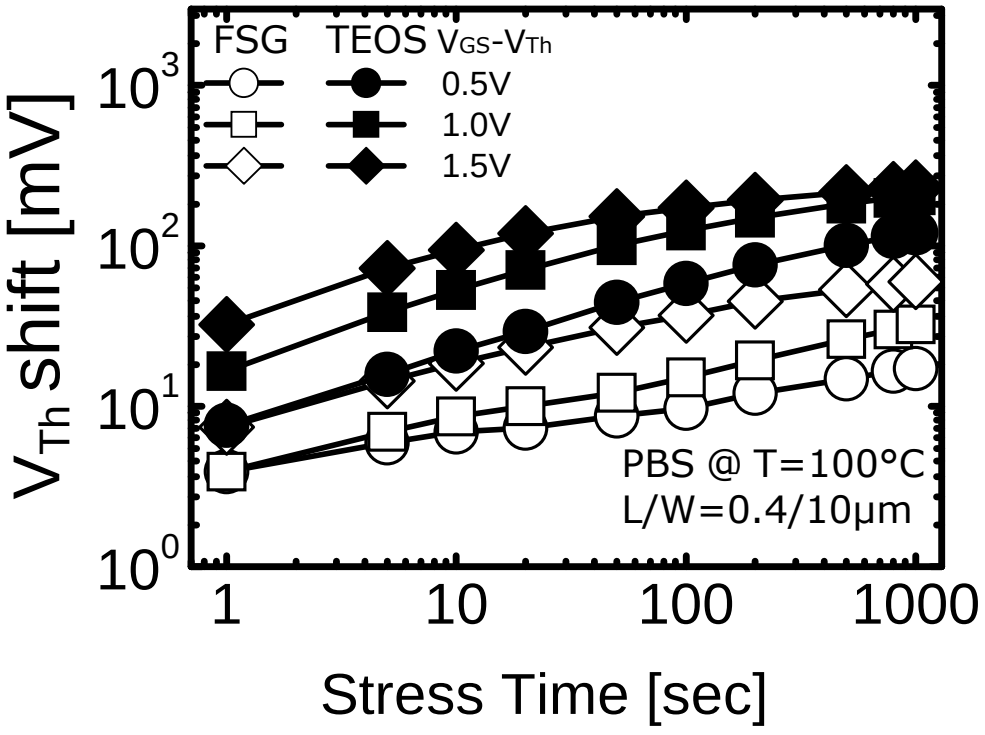


Fig. 3.13 Time dependences of PBS-induced V_{th} degradation at various normalized stress biases from 0.5 to 1.0 per steps of 0.5V at 100°C.

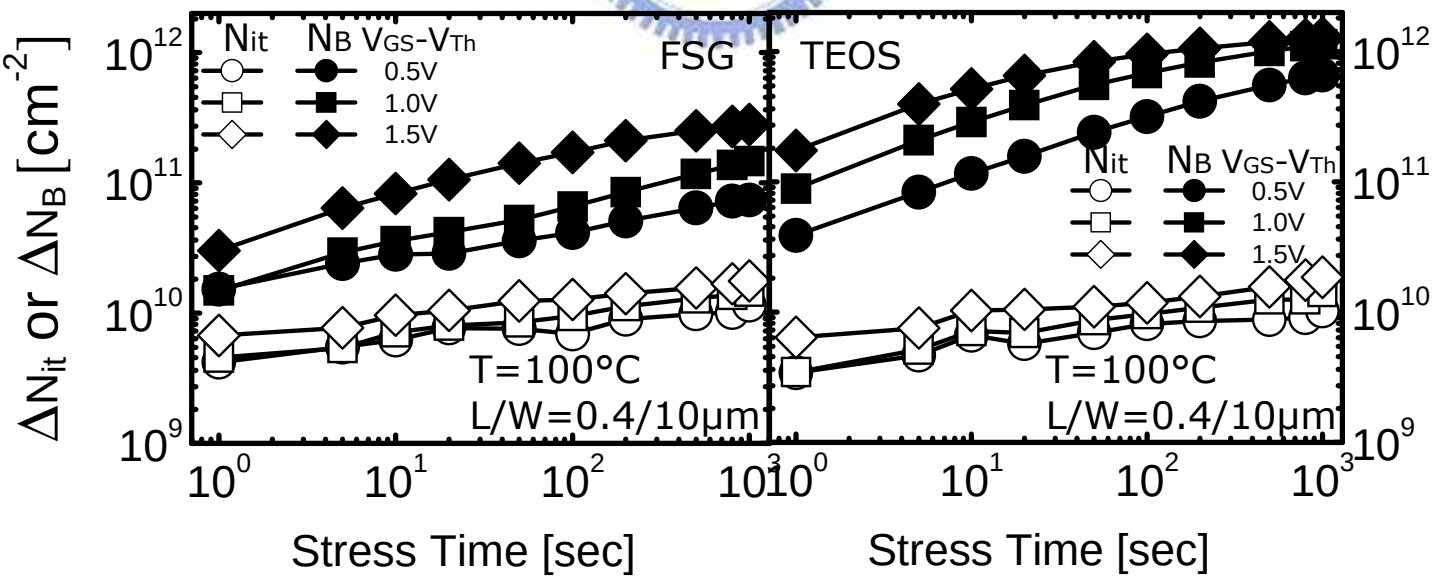


Fig. 3.14 Time dependences of PBS-induced N_{it} and N_B degradation at various normalized stress biases from 0.5 to 1.0 per steps of 0.5V at 100°C.

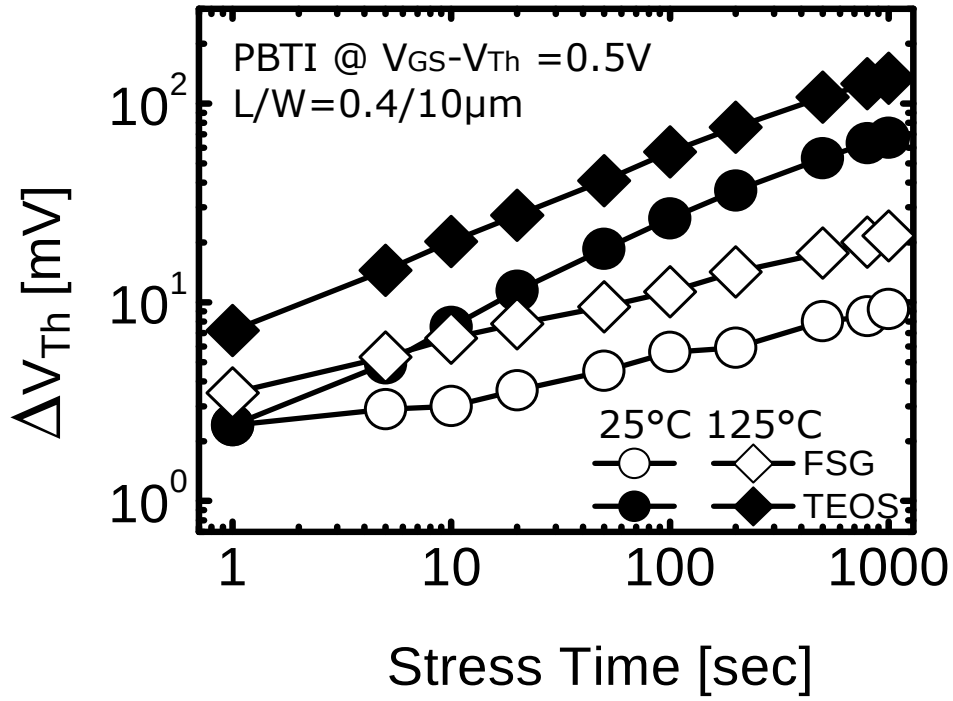


Fig. 3.15 Threshold voltage shift as a function of stress time under BTS a different stress temperature, V_{GS}-V_{Th} =0.5V for FSG and TEOS samples.

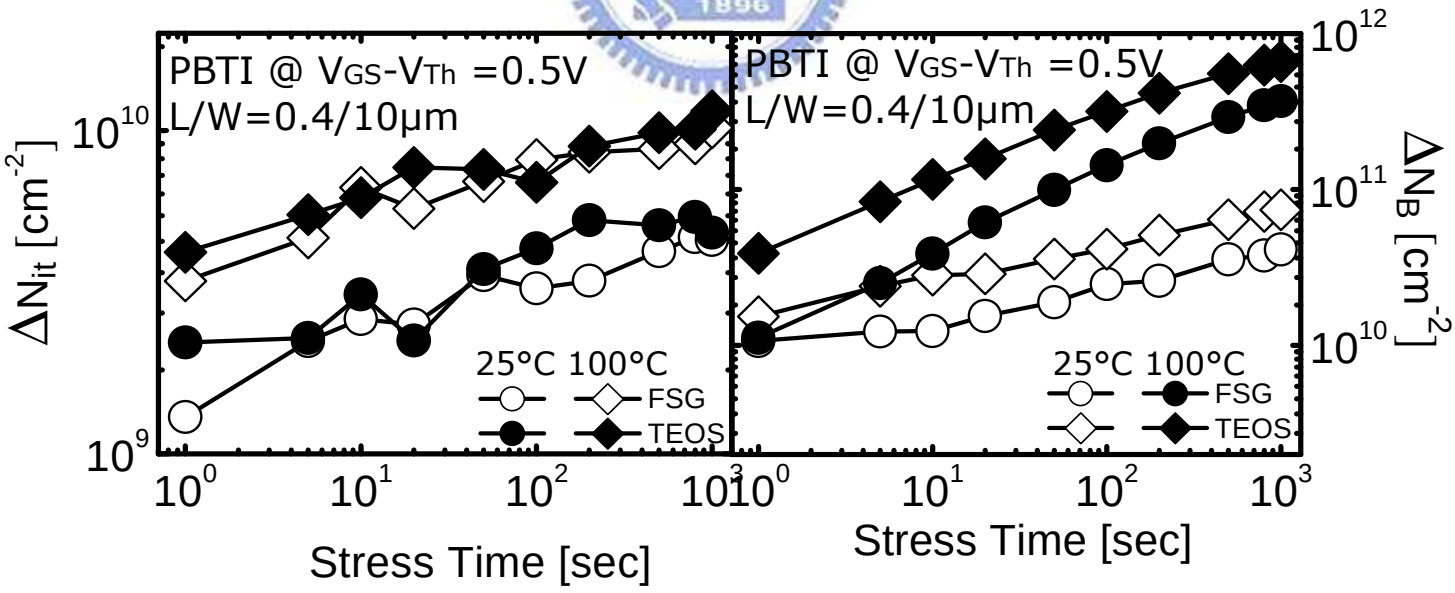


Fig. 3.16 Interface trap density and bulk trap density shift as a function of stress time under BTS a different stress temperature, V_{GS}-V_{Th} =0.5V for FSG and TEOS samples.

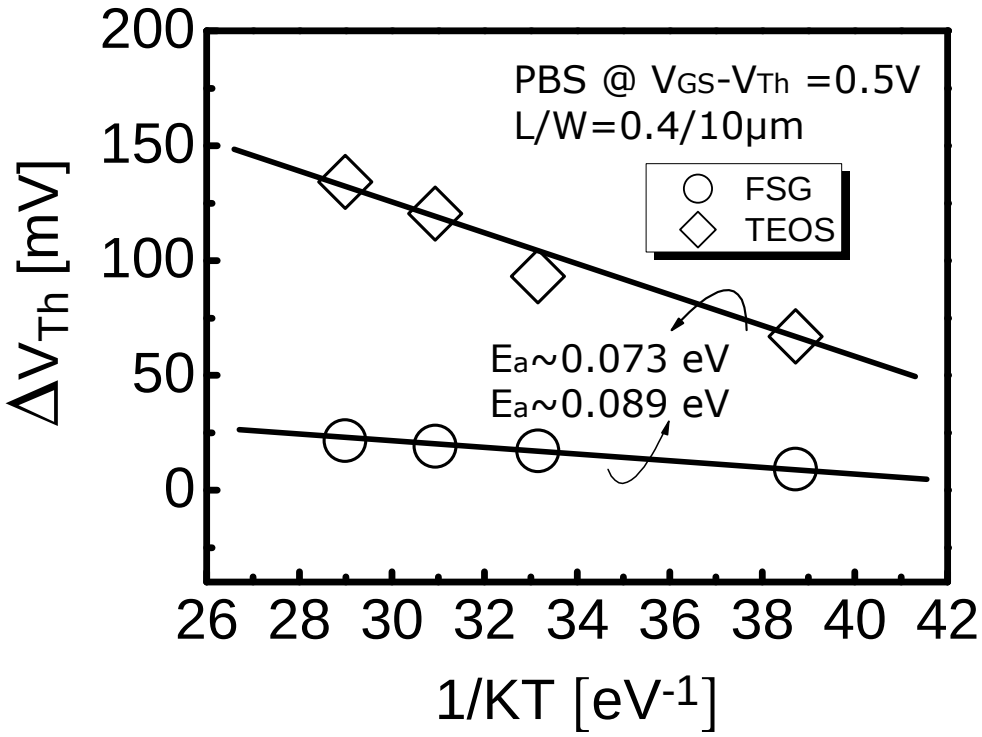


Fig. 3.17 Temperature dependence of threshold voltage shift. PBT stress was applied under V_{GS}-V_{Th}=0.5V.

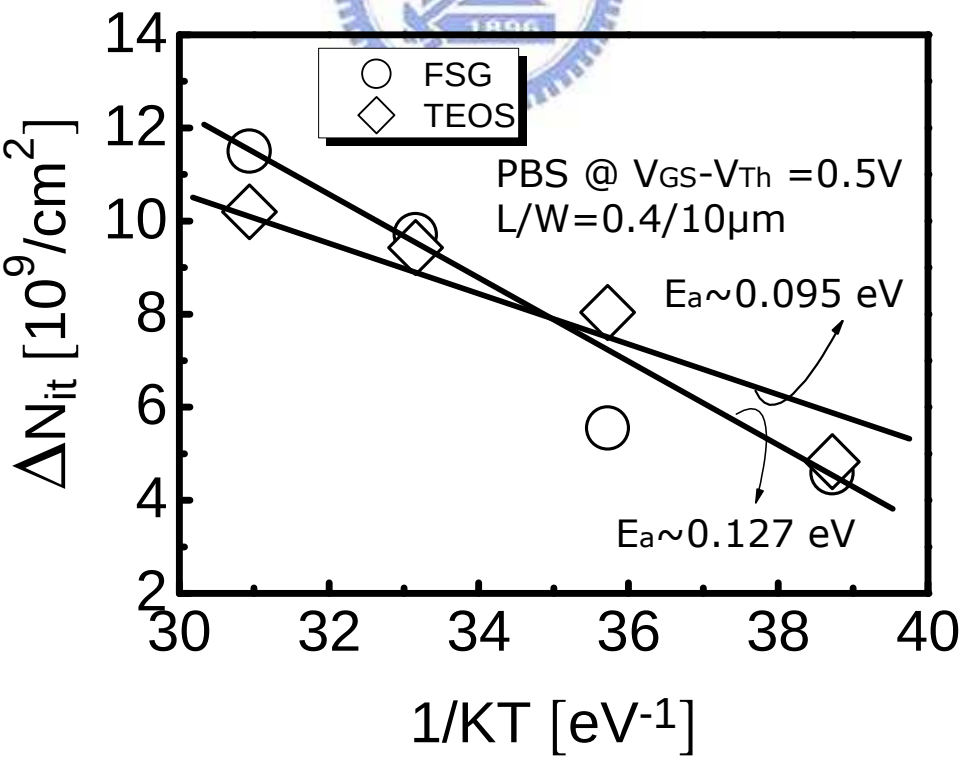


Fig. 3.18 Temperature dependence of interface traps shift. PBT stress was applied under V_{GS}-V_{Th}=0.5V.

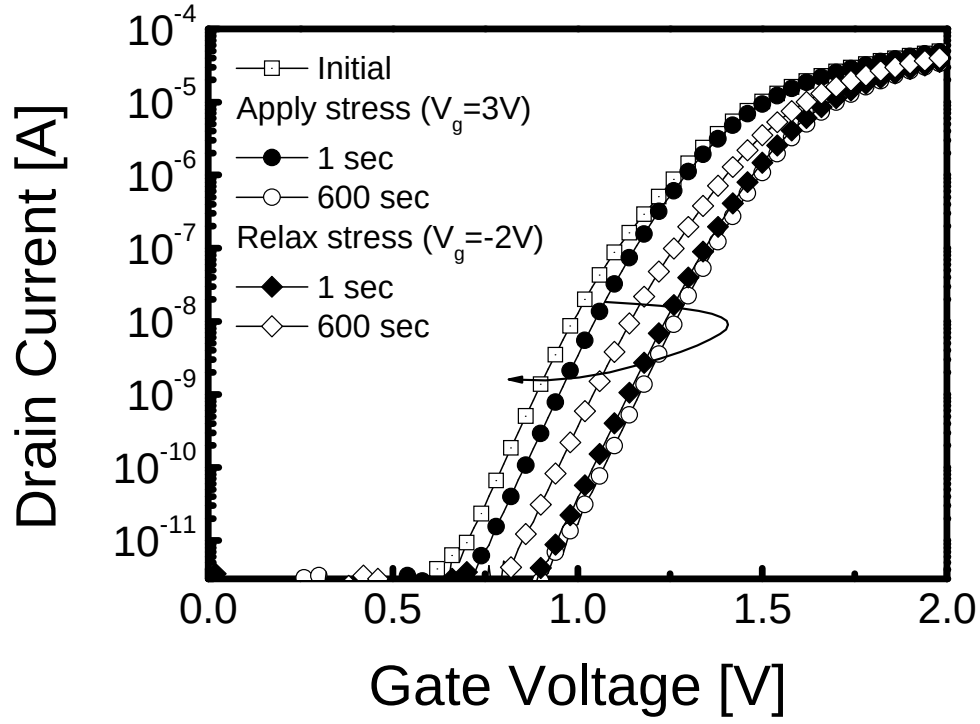


Fig. 3.19 I_D-V_{GS} characteristic during a constant voltage stress with a subsequent relaxation period.

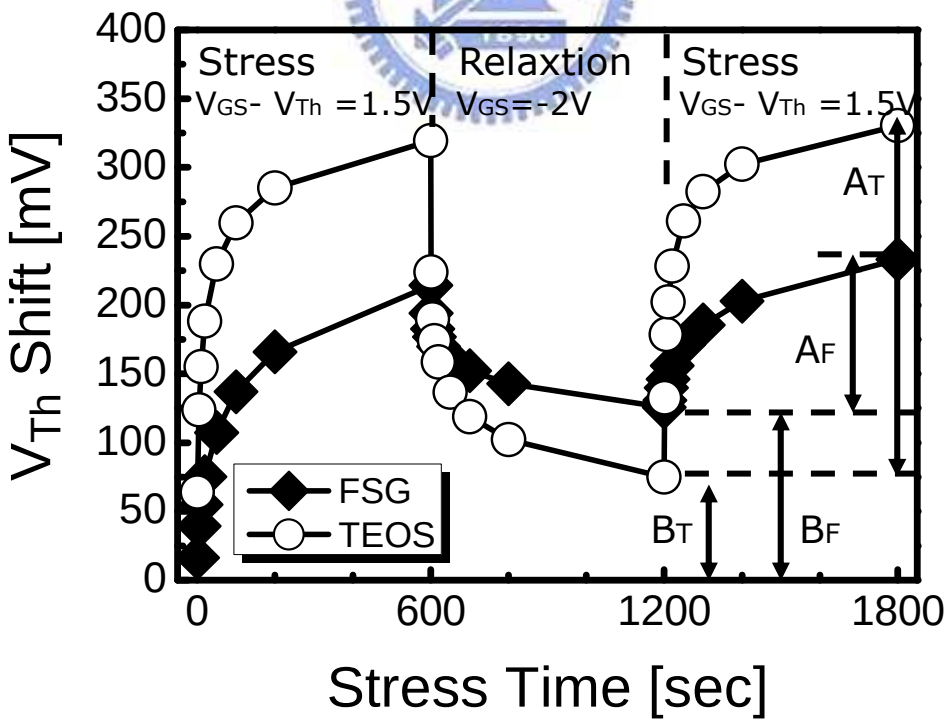


Fig. 3.20 Threshold voltage shift with de-trapping bias –2 V dependence after positive voltage stress on both samples.

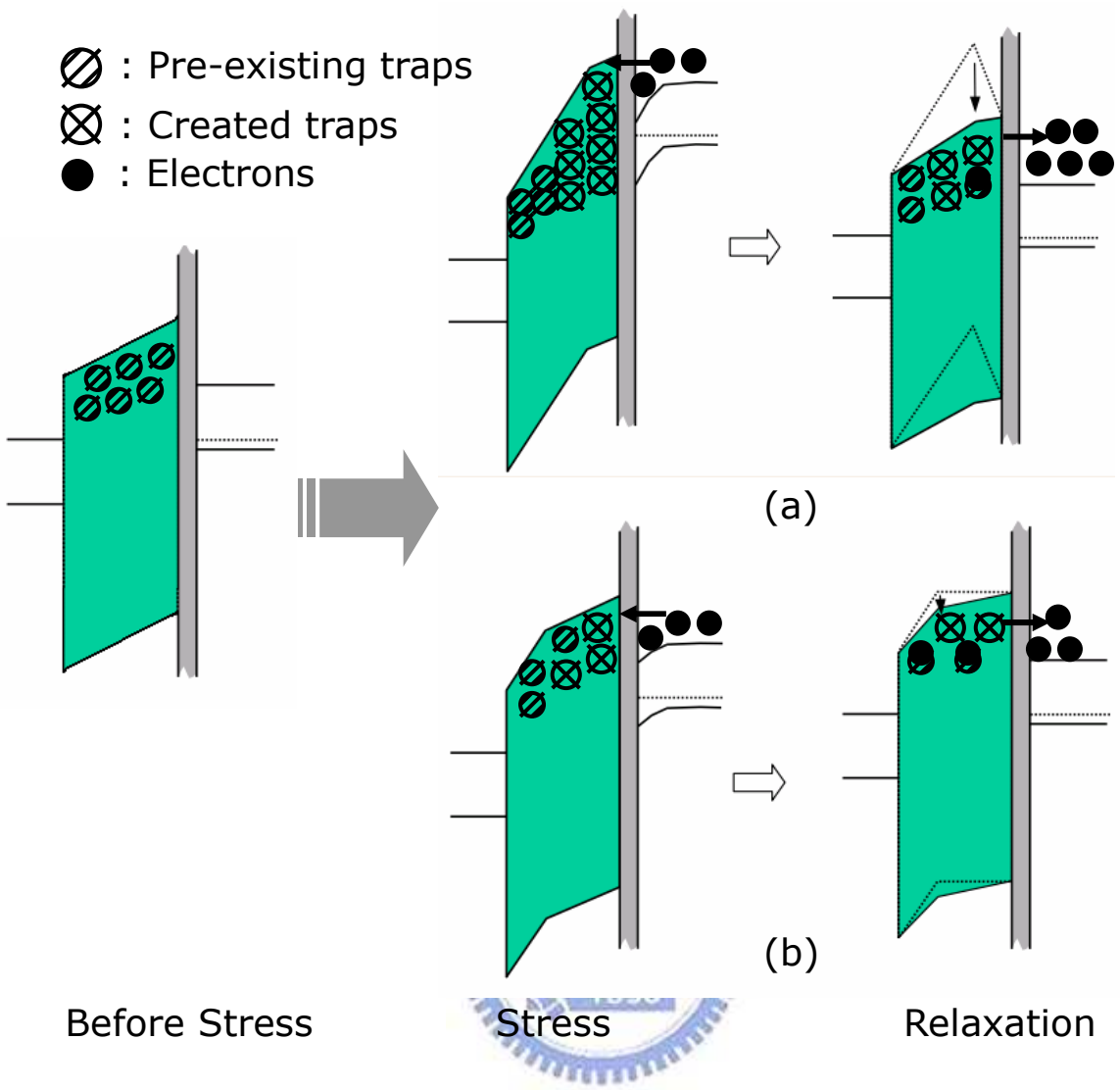


Fig. 3.21 Schematic explanation of stress and relaxation process with different bias conditions for (a) TEOS (b) FSG P.L..

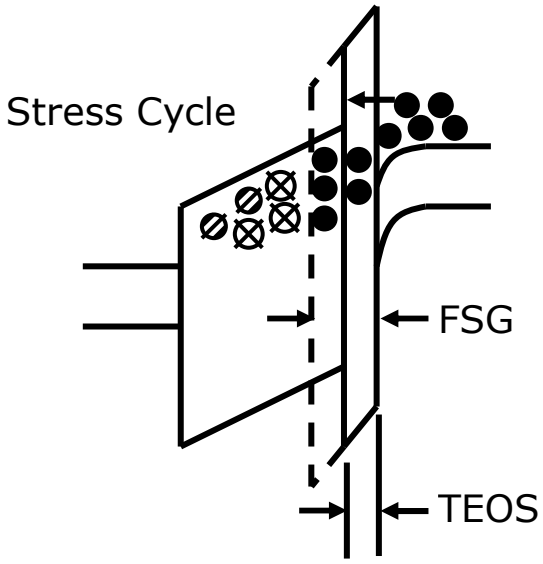


Fig. 3.22 Schematic explanation of more charge trapping stored in thicker CET during stress cycle.

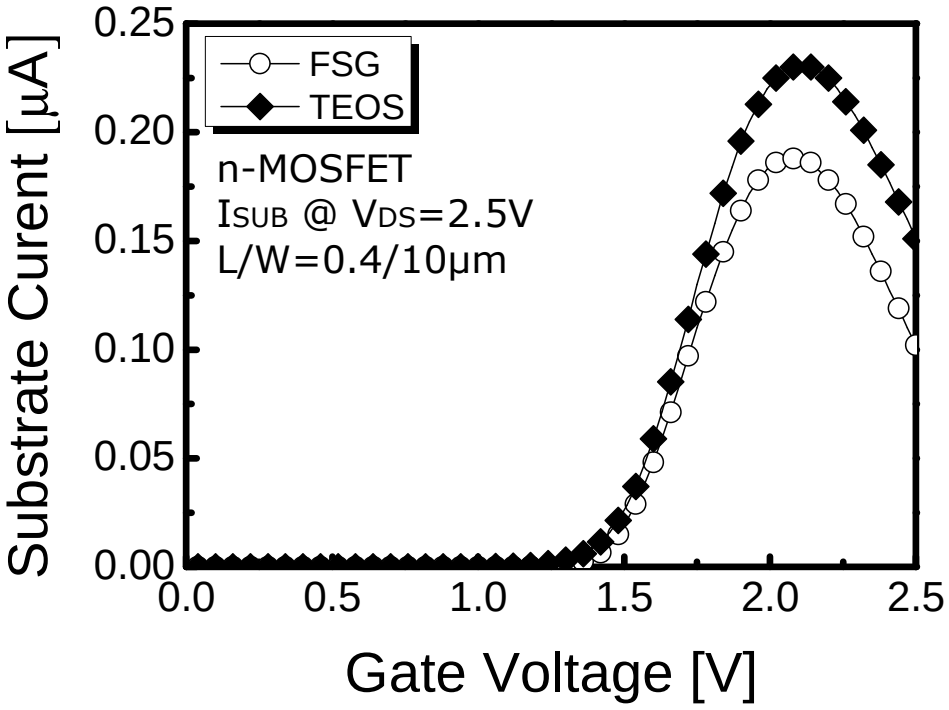


Fig. 3.23 Substrate current versus gate voltage for both samples of HfO_2/SiON gate stack n-MOSFETs.

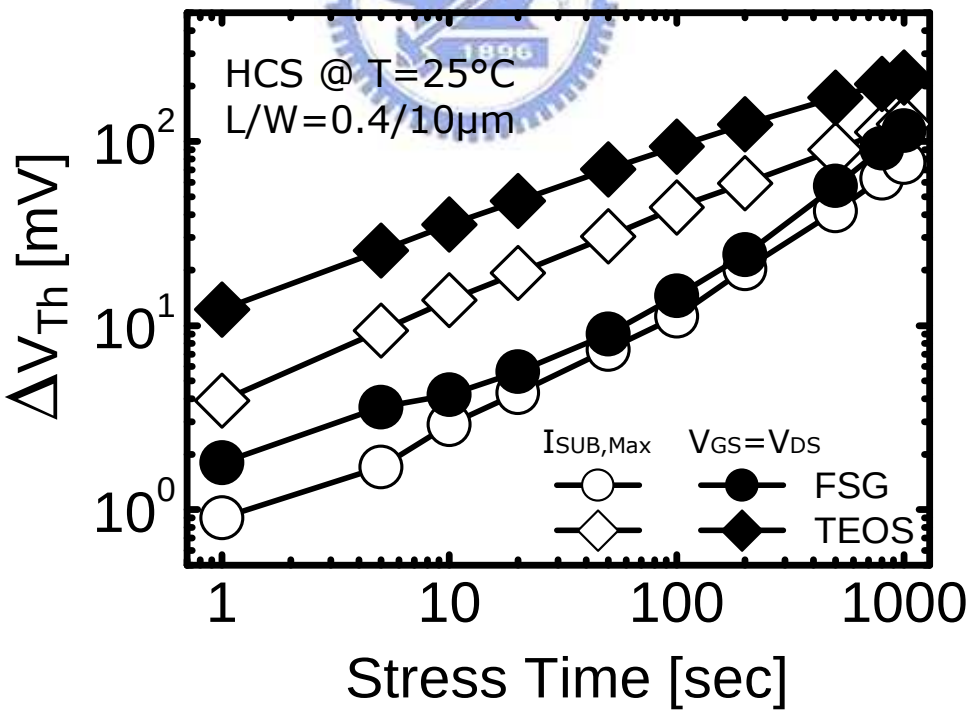


Fig. 3.24 Threshold voltage shift as a function of stress time with HCS which compares FSG P.L. with TEOS P.L..

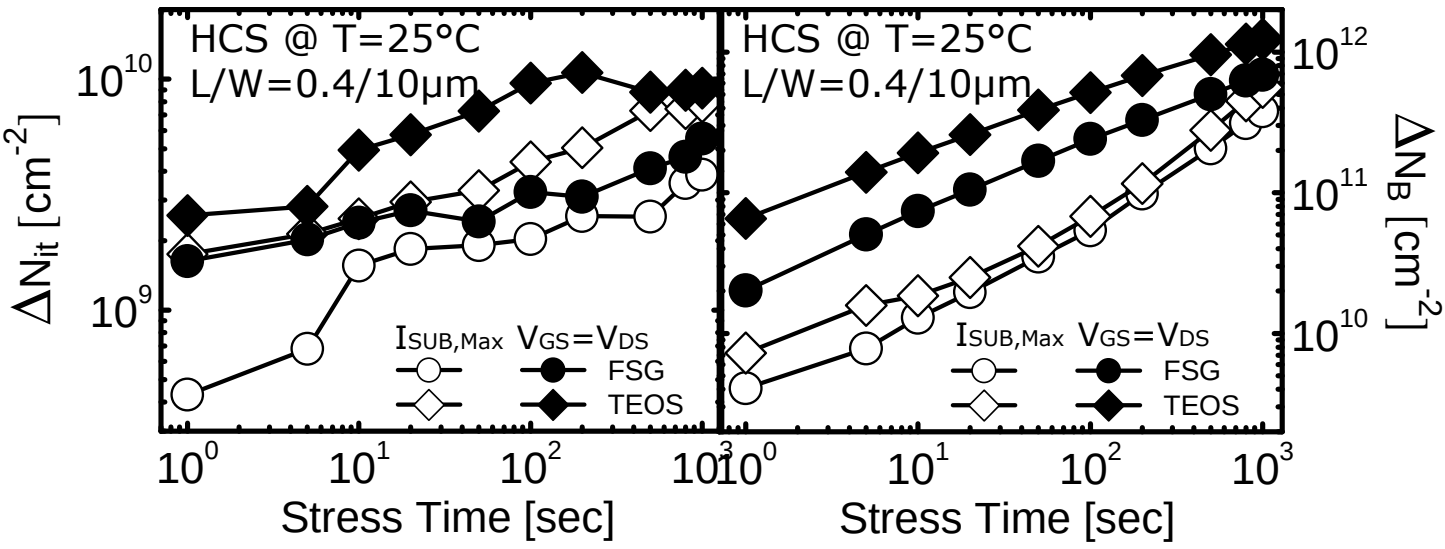


Fig. 3.25 Interface trap and bulk trap density shift as a function of stress time with HCS which compares FSG P.L. with TEOS P.L..

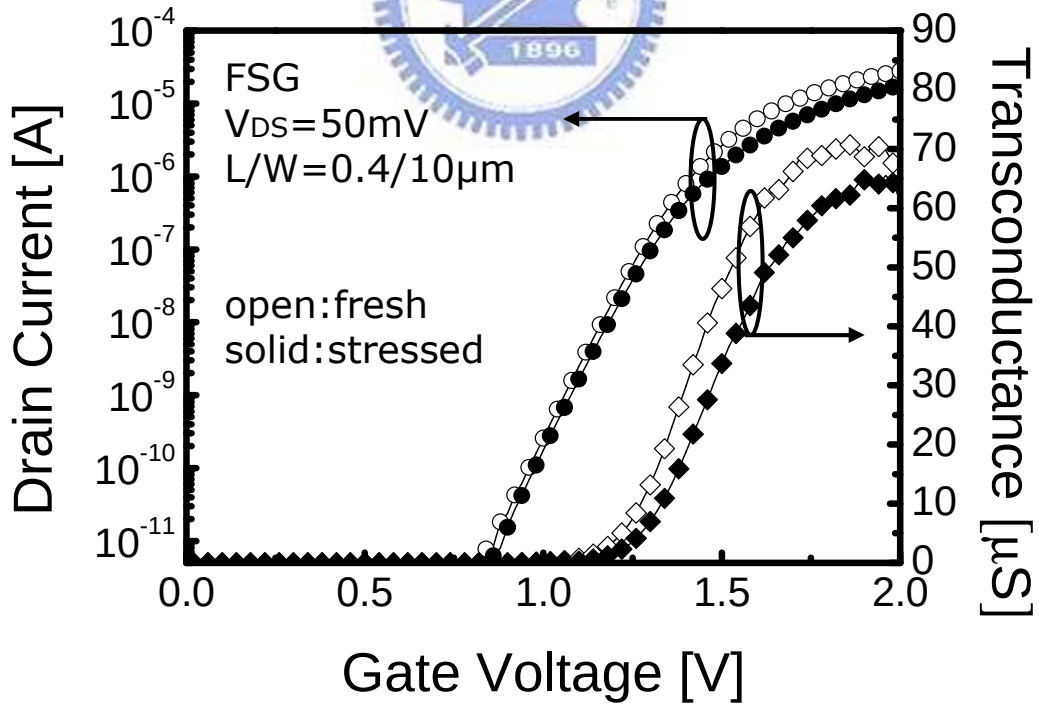


Fig. 3.26 I_D-V_{GS} characteristics and transconductance of devices with FSG P.L. before and after 1000 sec hot-electron stressing.

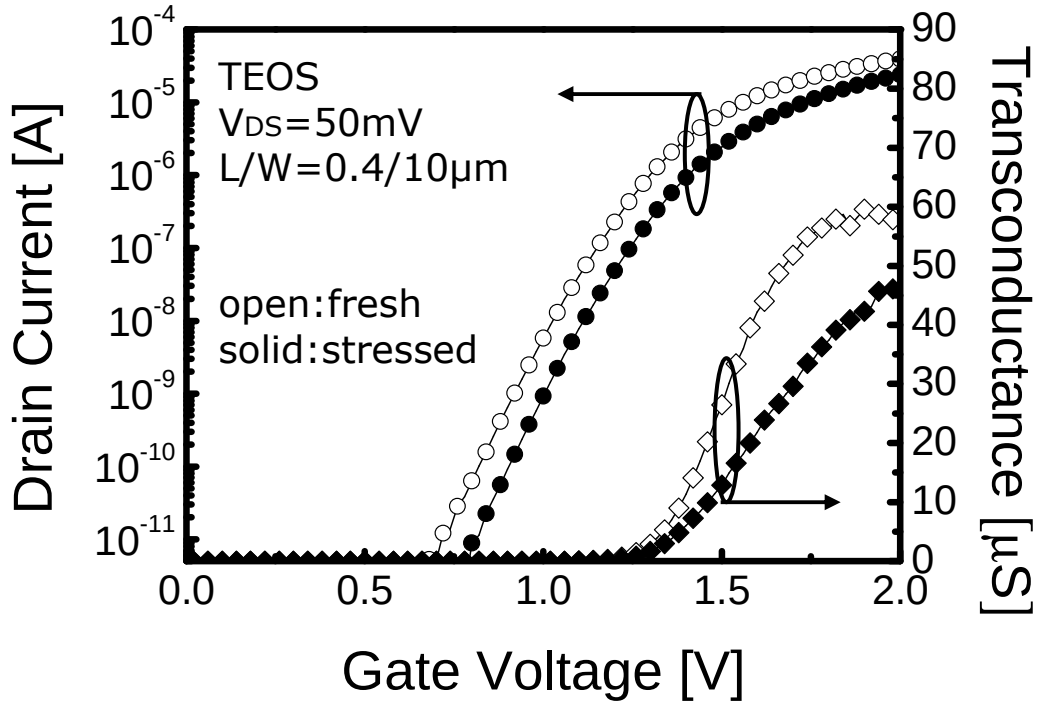


Fig. 3.27 I_D-V_{GS} characteristics and transconductance of devices with TEOS P.L. before and after 1000 sec hot-electron stressing.

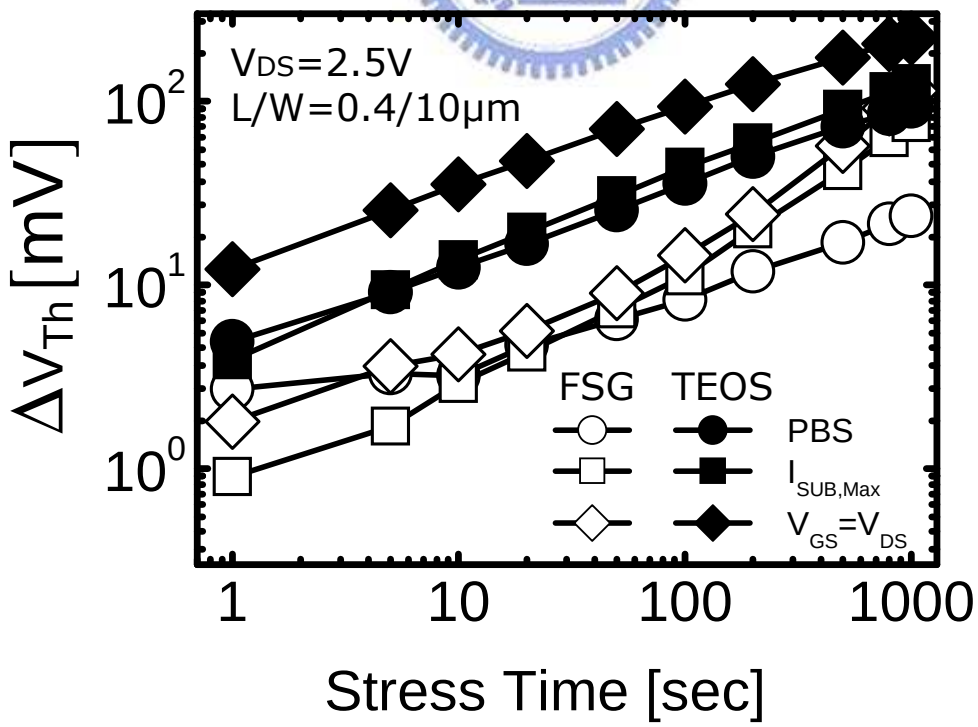


Fig. 3.28 Threshold voltage shift as a function of stress time which compares HCS with PBS.

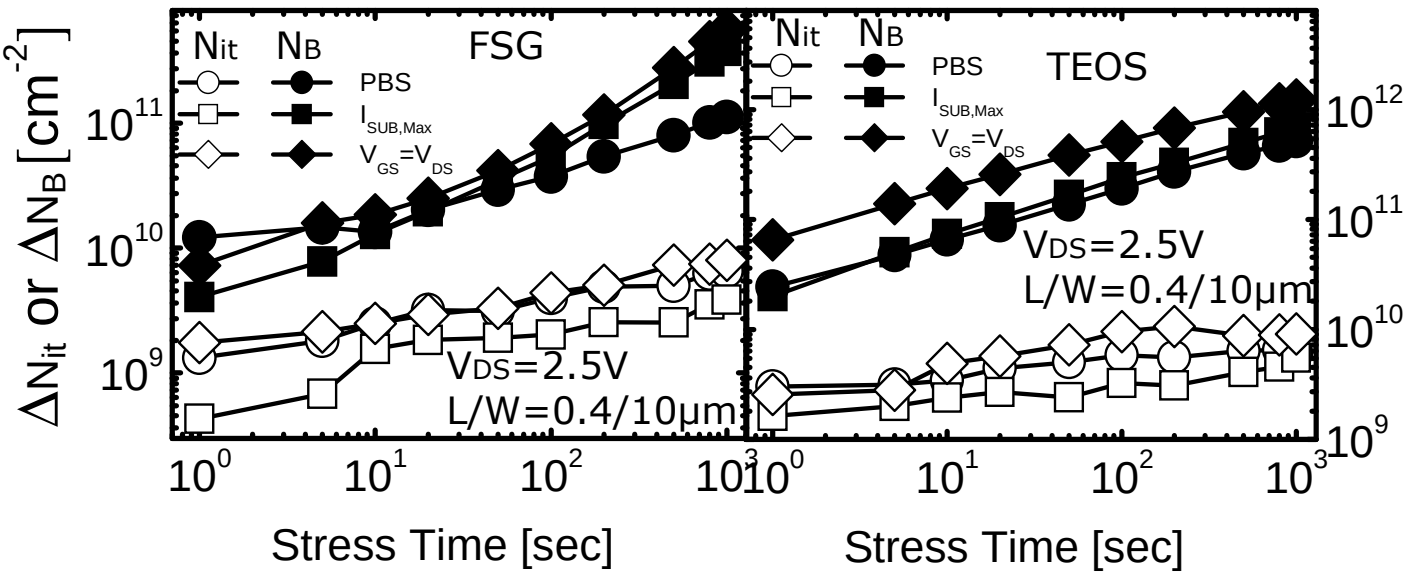


Fig. 3.29 Interface trap and bulk trap density shift as a function of stress time which compares HCS with PBS.

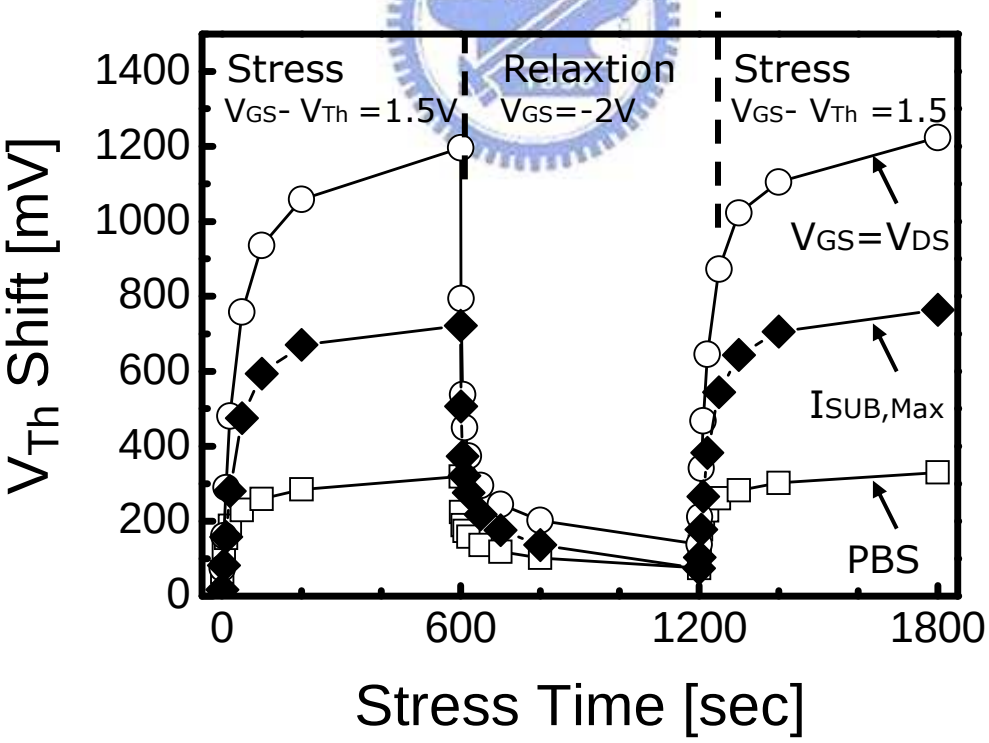


Fig. 3.30 Threshold voltage changes during HCS and PBS followed by a detrapping step (Vg=-2V) 600 sec for the TEOS sample.

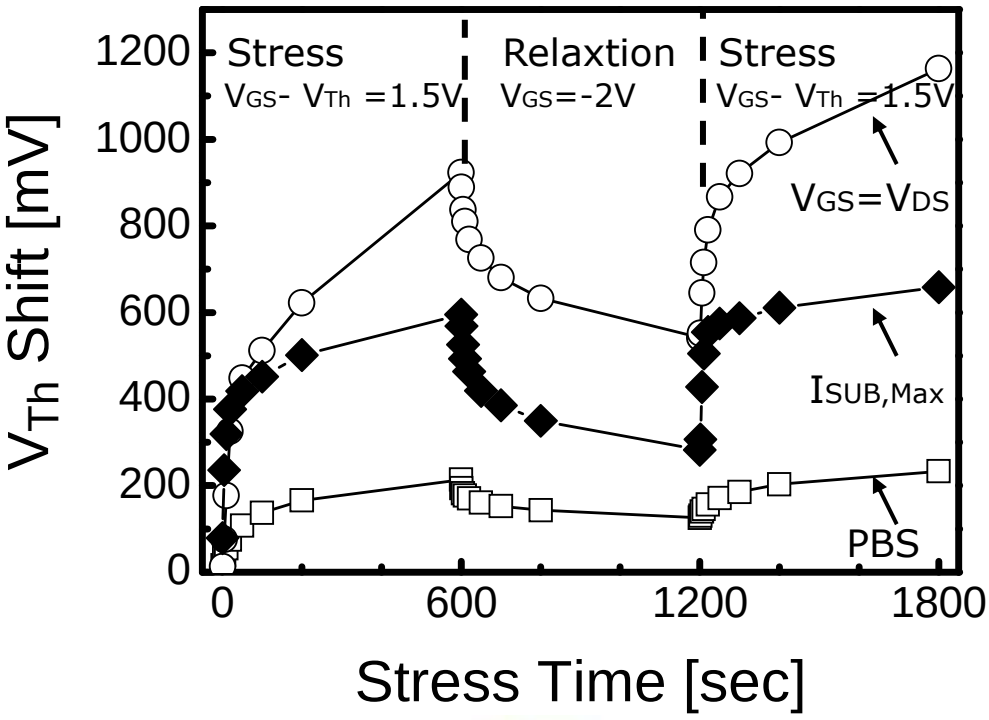


Fig. 3.31 Threshold voltage changes during HCS and PBS followed by a detrapping step (Vg=-2V) 600 sec for the FSG sample.

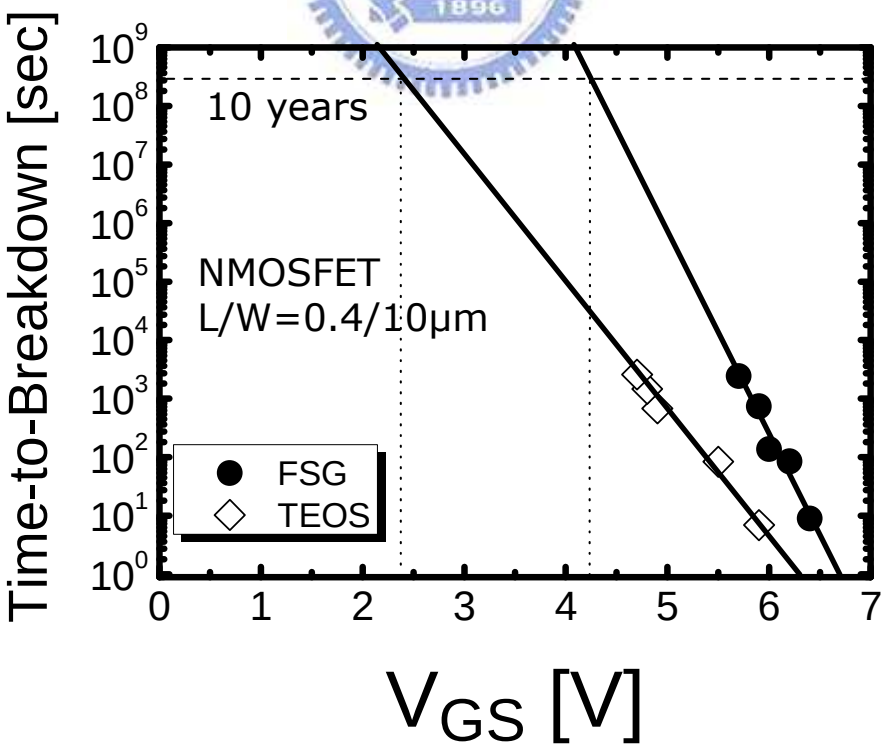


Fig. 3.32 Comparison of T_{BD} lifetime projection as a function V_{GS} of FSG P.L. larger than TEOS P.L..

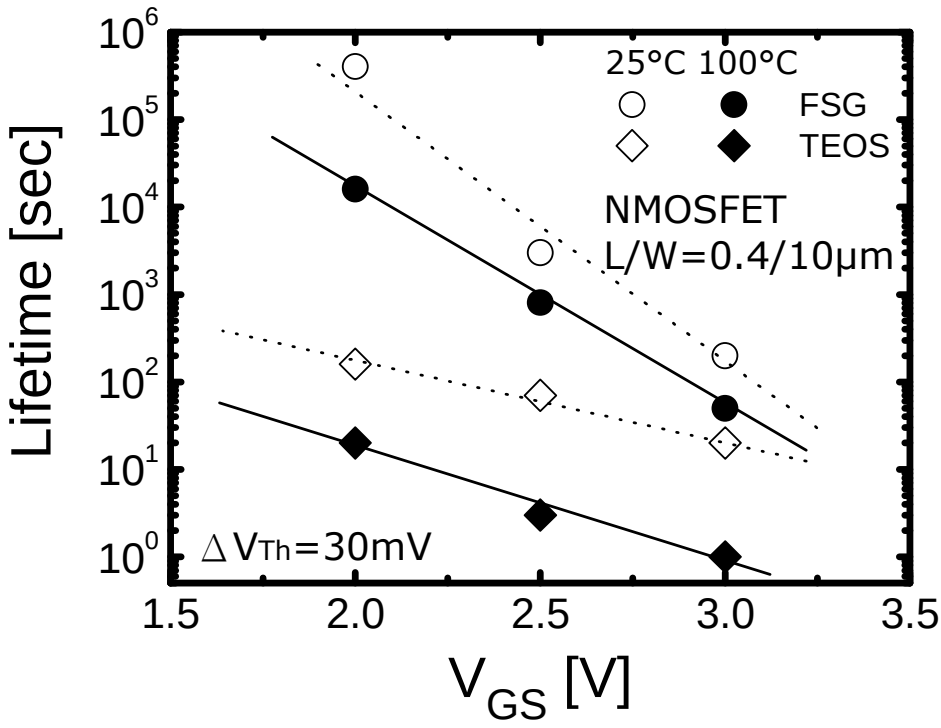


Fig. 3.33 Dependence of lifetime on stress V_{GS} for both samples.

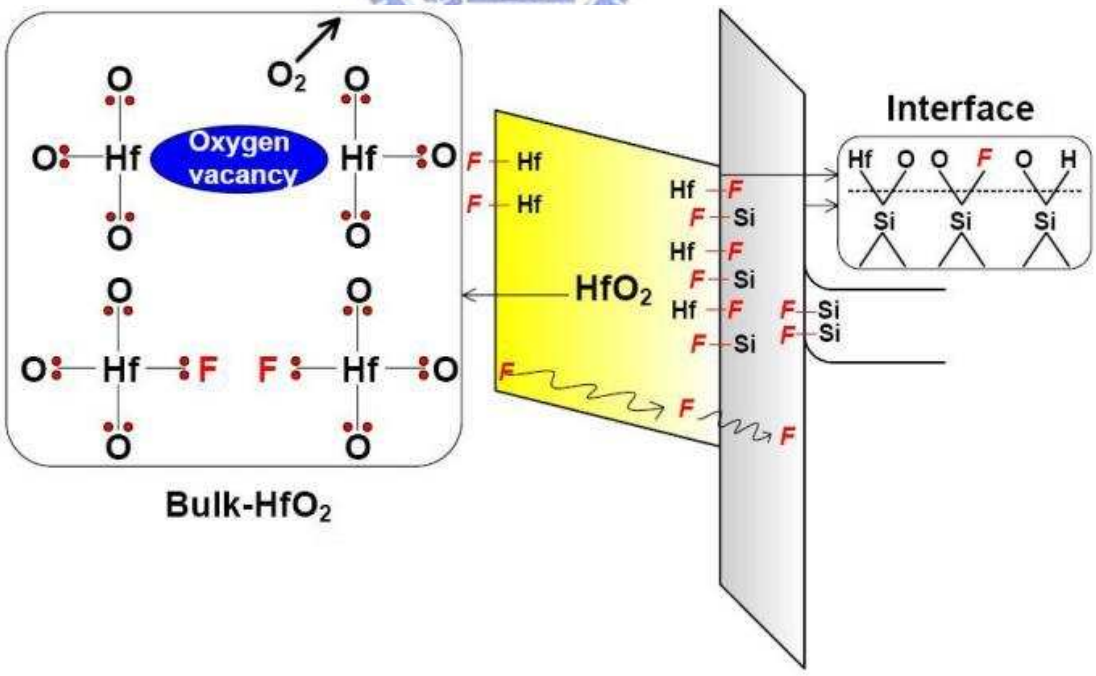


Fig. 3.34 Schematic of reliability improvement for the FSG passivation layer due to fluorine incorporation.

CHAPTER 04

Conclusions and Suggested Future Works

4.1 Conclusions

In this thesis, a novel fluorine passivation technique for HfO_2/SiON gate stack n-MOSFET is proposed. The impact of fluorine incorporation into HfO_2/SiON gate stack by introducing CF_4 gas during depositing silicon oxide as a passivation layer was investigated. Several important phenomena were observed and summarized as follows:

First of all, we have investigated its basic electrical properties. The novel high-k device with FSG film as the passivation layer to enhance the electrical characteristics due to fluorine passivation effect. We have found that improvements include many aspects, such as reduced gate leakage current, better subthreshold swing, enhanced normalized transconductance and driving current which correspond with higher mobility. This is attributed to the reduction of the interface state and bulk trap density in HfO_2/SiON gate stack as confirmed by charge pumping measurements. The gate leakage current is analyzed by the carrier separation measurement, and can be explained by the band structure of the gate stack. The S/D current I_{SD} that corresponds to the electron current dominates the leakage under inversion region, while the substrate current I_{SUB} that indicates the hole current

dominants the leakage current under accumulation region. All leakage current can be categorized by fitting to be of Frenkel-Poole type.

In the second part of the thesis, we have studied the PBTI, HCS and charge de-trapping mechanisms of poly-si gate HfO_2/SiON dielectric for various passivation layer. It is believed that the PBTI and HCS degradation are related to the electron traps in high-k dielectric, not by the interfacial degradation, resulting in threshold voltage shift. The FSG passivation layer also promotes the PBTI and HCS immunity due to the formation of the rather stronger Si-F bonds in not only the HfO_2 bulk but also the interface including near S/D sides. The results reveal that fluorine incorporation from the introduced CF_4 gas is effective in suppressing ΔN_B , thus improving threshold voltage instability. Stress induced V_{Th} shift and its relaxation characteristics under the de-trapping (negative) gate bias has been studied. The reversible electrons trapping do not generate structural damage in the dielectrics, and can be de-trapped. However, the residual electrons trapping indicate permanent damage.

Finally, we can observe that, for the FSG P.L., hot carrier induced permanent damage is significant severer than reversible cold carrier trapping. The root-cause possibly associated with the higher height barrier of de-trapping behavior and the slighter increased capacitance equivalent thickness.

4.2 Suggestions for Future Works

There are many issues that we can't discuss completely. We list some goals for future work as follows.

1. HRTEM is used to verify real thickness and estimate value of the dielectric constant for HfO_2/SiON gate stack.
2. SIMS analysis is used to prove fluorine exist in HfO_2/SiON dielectric, further in order to understand fluorine depth profile.
3. XPS analysis is used to prove if fluorine can passivate oxygen vacancy so as to lower high-k bulk traps due to the formation of Hf-F bonds.
4. In actual CMOS circuit operation, AC gate bias with specific frequency and duty cycle is usually utilized. Therefore, AC stress with dynamic AC stress application is more realistic and can provide additional insights into the trapping behavior.
5. Fast transient pulsed I_D-V_{GS} measurement is also used to evaluate charge-trapping phenomena precisely.
6. The fluorinated silicate glass as a passivation layer of strained silicon device is investigated whether channel mobility and the improvement of reliability can be effectively enhanced or not.
7. How much flow rate of CF_4 gas makes the FSG passivation layer unstable due to excess fluorine atoms, which in turn deteriorate the devices and result in the degraded performance and reliability.

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