國立交通大學

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碩 士 論 文

利用順向基極偏壓設計之低功耗低雜訊放大器

Low-Power LNA Design using Forward Body Biasing Technique

研 究 生：黃俊榮

指導教授：郭治群 博士

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利用順向基極偏壓設計之低功耗低雜訊放大器

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摘要

本論文利用 RF CMOS 製程分別設計了應用於無線接收端之超低功耗和超寬頻低雜訊放大器。內容主要實現了兩個電路晶片。一個是超寬頻低雜訊放大器，另一個是次 0.2 毫瓦低功耗低雜訊放大器。其中對於使用三階帶通濾波器的超寬頻低雜訊放大器而言，頻寬範圍為 3.1~10.6GHz，並利用順向基極偏壓技術來達成低功率消耗。輸入匹配利用三階帶通濾波器搭配源極電感來達成標準 50 歐姆寬匹配。此電路利用台積電 0.13 微米 RF CMOS 製程來實現。對於目標 3.1~10.6GHz 頻段內，量測結果顯示，當供應電壓 0.9 伏特時，整體功率消耗約 8.4 毫瓦，在 3.3～8.1GHz 頻段內，增益為 10.8～5 dB，雜訊指數為 3.9～4.1 dB，輸入端反射係數和輸出端反射係數皆分別小於 -6.7dB 和 -5.8dB，而 S12 皆小於 -27.3 dB。此超寬頻低功耗低雜訊放大器的功率消耗能有效降低主要是利用對電晶體使用順向基極偏壓技術來降低臨界電壓進一步降低 VDD 來達成。

對於超低功耗低雜訊放大計設計而言，採用 UMC90 奈米製程來實現利用順向基極偏壓設計之低功耗低雜訊放大器。此電路採用串疊式架構，並將放大級電晶體 M1 偏壓在次臨界區域搭配使用順向基極偏壓來達成次 0.2 毫瓦低功耗低雜訊放大器設計。在電感模型可信之前提下，利用順向基極偏壓可將操作電壓降低至 0.18V 時仍能提供足夠增益。由模擬結果得到，在 1.4GHz 時增益(S_{21})大小為 11dB，此時操作電壓為 0.18V，功

率消耗為 0.19 毫瓦。同時也讓雜訊指數為 2.3dB，在 1.5GHz 時有最小雜訊指數 2.1dB。在 1.4GHz 下，輸入逆向損耗(S_{11})和輸出逆向損耗(S_{22})分別為 -10.4dB 和 -10.5dB，逆向隔離(S_{12})為-15.2dB。實際量測結果由於實際電感特性太差而不如預期。若將操作電壓提升至 0.5 伏可改善這個問題。此時增益為 5.5dB 而功率消耗為 1.75 毫瓦，S_{11} 和 S_{22} 分別為 -12.1dB 和 -14.8dB，而 S_{12} 為-23.5dB。

Low-Power LNA Design using Forward Body Biasing Technique

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Department of Electronics Engineering

Institute of Electronics

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Abstract

In this thesis, low-power low noise amplifiers (LNA) design and fabrication have been realized using RF CMOS technologies for applications in ultra-low power or ultra-wide band (UWB) wireless receivers. The major achievements are composed of two circuit chips. One is UWB low-power LNA, and the other is sub-0.2mW ultra-low power (ULP) LNA. For the UWB LNA adopting three-section band-pass Chebyshev filter, the bandwidth can be extended over 3.1~10.6 GHz , and low power is achieved by using forward body bias (FBB) technique. The input matching to standard 50 Ω was realized through the three-section LC networks adopted in the MOS transistor with inductively degenerated source. This UWB LNA is fabricated in a 0.13-μm RF CMOS process. The measured performance over the targeted bandwidth of 3.1~ 10.6GHz indicates that the power gain is 10.8 ~ 5 dB, noise figure is 3.9 ~ 4.1 dB, power consumption is 8.4 mW from 0.9V, the input and output return losses, i.e. S_{11} and S_{22} are below -6.7dB and -5.8dB respectively, and the leakage S_{12} can be kept below -27.3 dB in 3.3 ~ 8.1GHz. The power consumption for this UWB LNA can be effectively

reduced by lowering the supply voltage V_{DD} attributed to substantially lower threshold voltage (V_T) under forward body biases.

As for the ultra-low power LNA design in part two, FBB scheme was implemented in this work using 90nm low leakage (LL) CMOS process. As a result, Sub-0.2mW LNA can be realized based on a cascade topology, in which the MOSFET at transconductance stage is biased under subthreshold condition and applied with FBB. Assuming the availability of on-chip inductors with performance predicted by the model, the V_{DD} can be pushed to as low as 0.18V and sufficient gain can be maintained, attributed to FBB. ADS simulation predicted that this ULP LNA can attain power gain of 11 dB at 1.4GHz and consume extremely low power of 0.19mW from 0.18V. Furthermore, the noise figure (NF_{50}) can reach the minimum of 2.1 dB at near 1.5GHz and keep around 2.3 dB at 1.4GHz. The input and output return losses (S_{11} and S_{22}) are –10.4dB and –10.5dB, respectively. The port-to-port leakage (S_{12}) is maintained as low as –15.2 dB. The power gain (S_{21}) measured from the real chips under 0.18V is abnormally low, due to poor inductors performance and the resulted severe deviation in input matching. When increasing V_{DD} to 0.5V, this problem can be solved and promisingly good results can be realized. The power gain (S_{21}) is 5.5 dB at 1.4GHz and power consumption is 1.75mW from 0.5V. S_{11} and S_{22} are –12.1dB and –14.8dB, respectively, and S_{12} is as low as –23.5 dB.

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Chapter 1

Introduction

1.1 Background and Motivation

The design of low-power wireless transceivers has gained substantial significance due to the explosion of wireless applications such as personal area networks and wireless sensor networks. These applications demand small, low-cost, and low-power wireless transceivers, which require a high level of integration with a minimal amount of off-chip components. The first active block to amplify the received signal from the antenna is the low-noise amplifier (LNA). The specifications of a LNA influence significantly the performances of the whole receiver. The LNA needs to amplify the signal without adding an inappropriately large noise and distortion while consuming minimal power. How to provide enough gain in a LNA suitable for a specific wireless communication system without consuming too much power is the main object of this thesis. The important design goal of portable wireless system is low power consumption for long battery life. In the thesis, two LNAs intended for 3.1~10.6 GHz ultra-wideband (UWB) LNA and 1.4 GHz ultra-lower power LNA are designed and fabricated.

Regarding the applications of UWB LNAs, the targeted UWB system is an emerging high-speed and low-power wireless communication domain approved by Federal Communication Commission (FCC) in 2002 for commercial applications in the frequency range from 3.1 to 10.6 GHz [1]. UWB performs excellently for short-range and high-speed uses, such as automotive collision-detection systems, through-wall imaging systems, and high-speed indoor networking, and plays an important role in wireless personal area network (WPAN) applications. This technology will be potentially a necessity in our daily life, from

wireless USB to wireless connection between DVD player and TV, and the **foreseeable** huge market attracts interest of various joint ventures in industries.

As for the ultra-low power LNAs, wireless body area network (WBAN) is identified as one of the applications of major interest . Wearable health monitoring systems integrated into a telemedicine system can facilitate a novel information technology that is able to support early detection of abnormal conditions and prevention of its serious consequences. Many patients can benefit from continuous monitoring as part of a diagnostic procedure, optimal maintenance of a chronic condition or during supervised recovery from an acute event or surgical procedure. Fig. 1.1 shows a generalized overview of multi-tier system architecture [2]. To be unobtrusive, the sensors must be lightweight with small form factor. The size and weight of sensors is predominantly determined by the size and weight of batteries. Requirements for extended battery life directly oppose the requirement for small form factor and low weight. This implies that sensors have to be extremely power efficient, as frequent battery changes for multiple WBAN sensors would likely hamper users' acceptance and increase the cost. In addition, low power consumption is very important as we move toward future generations of implantable sensors that would ideally be self-powered, using energy extracted from the environment.

In this thesis, forward body bias (FBB) scheme was implemented in the LNAs for realizing a substantial V_{DD} scaling to subthreshold region for ultra-low power and maintain sufficiently good RF performance. Note that 4-terminal (4T) multi-finger MOSFET is the fundamental device structure in which the source and body are separated in two individual pads to enable non-zero body biases, such as forward or reverse body biases (FBB and RBB). This approach is new and quite different from conventional RF CMOS circuit design, which is based on 3-terminal (3T) MOSFET with body and source tied together and body bias fixed at zero (ZBB for zero body bias). Besides the change of unit device (MOSFET) layout from

3T to 4T, the device model has been adapted and enhanced to improve the accuracy under various body biases, such as ZBB, FBB, and RBB.

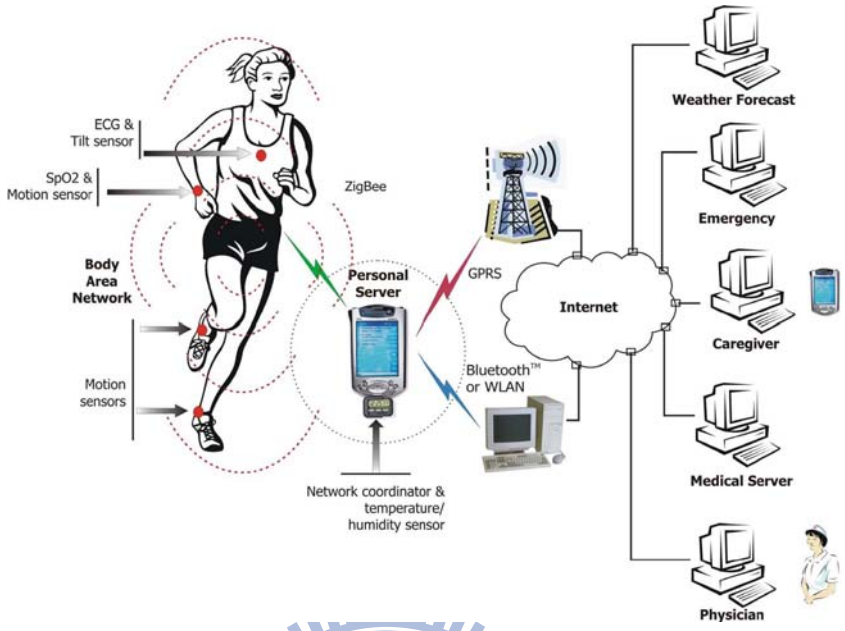


Fig. 1. 1 Wireless Body Area Network of Intelligent Sensors for Patient Monitoring [2]

1.2 Thesis Organization

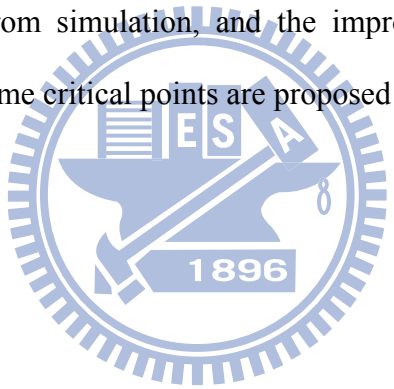
This thesis presents the work on the design and implementation of ultra-low power LNAs for receiver front-end circuits. The main objective of this thesis is to develop ultra-low power LNA design methods and certify the proposed topologies using RF CMOS processes. The contents consist of two major topics, such as “low-power UWB LNA design for 3.1~10.6 GHz wireless receivers” and “sub-0.2mW ultra-low power LNA for wireless body area network (WBAN) sensors.

In Chapter 2, we will introduce the basic concepts of LNAs design. Some conventional LNA input matching architecture will be discussed, and MOSFET noise model and the theoretical background will be addressed. Furthermore, dynamic threshold voltage CMOS technique (by using body biases) is also covered in this chapter.

In Chapter 3, we will present the design and implementation of a low-power LNA for

3.1~10.6 GHz UWB applications. We will discuss the circuit topology, the method for wideband input/output matching, and for the optimization of gain as well as noise. The test chip of LNA was fabricated by TSMC 0.13μm 1P8M CMOS Mixed Signal RF General Purpose Standard Process. The Si data measured from the test chip will be analyzed and compared with what predicted by simulation.

In Chapter 4, a narrow band LNA intended for application in 1.4 GHz WBAN is introduced. The details of circuit design and analysis method will be presented. This ultra-low power LNA chip was fabricated by UMC 90nm low leakage (logic and mixed-Mode 1P9M low-k) process. The measured results will be compared with the predicted performance from ADS simulation to verify the proposed circuit topology for ultra-low power, the root causes responsible for deviation from simulation, and the improvement solutions. In Chapter 5, conclusions are made and some critical points are proposed as the future work.



Chapter 2

Basic Concepts of Low Noise Amplifier Design

2.1 Conventional LNA Input Matching Architecture

Low noise amplifier is the first stage in the receiver front-end circuits and is used to amplify the received weak RF signal with the minimum noise figure. As it is well recognized that impedance matching is the fundamental requirement in LNA designs for achieving the target performance of both gain and noise. There are four basic 50-Ω input matching architectures that have been explored in the traditional transistor-amplifier shown in Fig. 2.1. In this section, we will have a review and discussion on the mentioned matching circuit architectures that can be used in LNA design [3, 4].

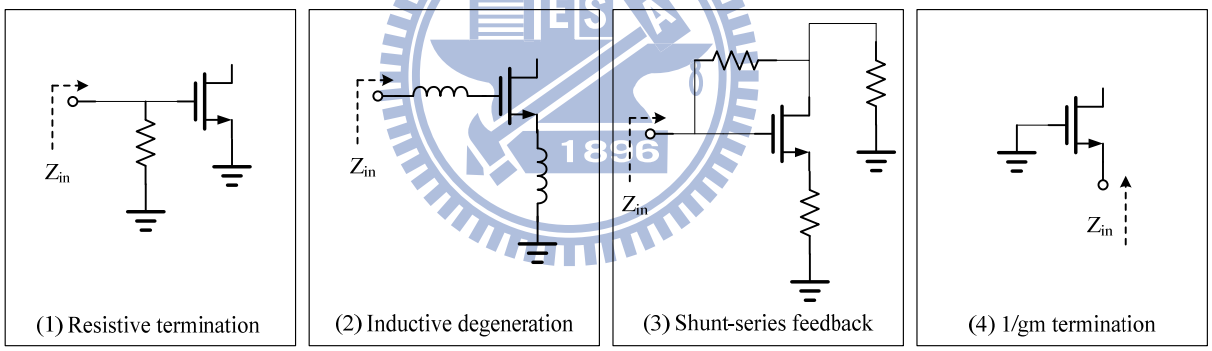


Fig. 2. 1 Traditional transistor-amplifier of input matching

2.1.1 Resistive Termination Architecture [3]

Resistive termination architecture is the most straightforward approach to providing a reasonably broadband 50-Ω termination. It is simply to put a 50-Ω resistor (R_1) across the input terminals of the LNA as shown in Fig. 2.2.

The bandwidth of this matching technique is determined by the input capacitance C_{gs} of the transistor M1 and can be very high. Unfortunately, the resistor R1 adds thermal noise of

its own and so attenuates the signal (by a factor of 2) ahead of the transistor. The combination of these two effects generally produces unacceptably high noise figures. More formally, it is straightforward to establish the lower bound on the noise figure of this circuit, given by (2-1) [3]:

$$NF \geq 2 + \frac{4\gamma}{\alpha} \cdot \frac{1}{g_m R} \tag{2-1}$$

where $\alpha \triangleq \frac{g_m}{g_{d0}}$ and γ is the coefficient of channel thermal noise, and $R_s = R_l = R$. For long-channel devices, $\gamma = \frac{2}{3}$ and $\alpha = 1$. This bound applies only in the low-frequency limit and ignores gate current noise altogether. Naturally, the noise figure is worse at higher frequencies and when gate noise is taken into account. Hence, the resistor termination technique is not practical in most application.

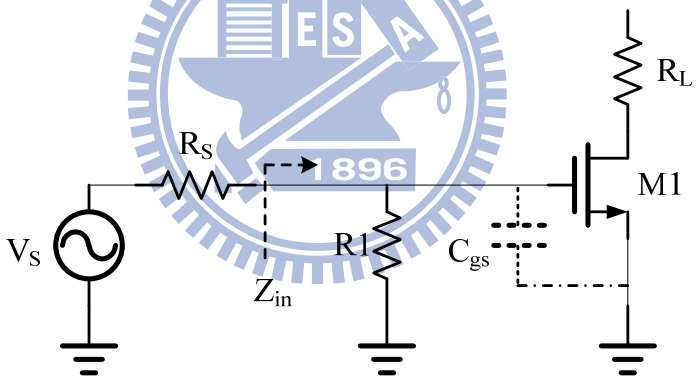


Fig. 2. 2 Resistive termination matching technique

2.1.2 Inductive Source Degeneration Architecture [3]

The inductive source degeneration architecture shown in Fig. 2.3 is popular with input matching technique of LNA. [4-18]. An important advantage of this method is that one then has control over the value of the real part of the impedance through choice of inductance, as is clear from computing the input resistance through a circuit analysis on the inductive source degeneration architecture in Fig. 2.3 and the resulted equivalent circuit in Fig. 2.4. This

method does not introduce additional noise (as in the case of using a shunt input resistor) and doesn't restrict the value of g_m (as in the case of the common-gate configuration).

To simplify the analysis, consider a device model that includes only a transconductance and a gate-source capacitance C_{gs}. The impedance looking through the gate inductor can be written as:

$$V_{in} = i_{in} \cdot (j\omega L_g + \frac{1}{j\omega C_{gs}}) + (i_{in} + g_m V_{gs}) \cdot j\omega L_s$$

$$\Rightarrow \quad Z_{in} = \frac{V_{in}}{i_{in}} = \frac{g_m L_s}{C_{gs}} + j[\omega(L_g + L_s) - \frac{1}{\omega C_{gs}}] \tag{2-2}$$

From (2-2), in order to achieve an input impedance matching, the following condition must be satisfied:

$$R_s = \frac{g_m L_s}{C_{gs}} = \omega_T L_s \tag{2-3}$$

where $\omega_T = \frac{g_m}{C_{gs}}$ is the transit frequency of the transistor M1. Once L_s is chosen based on gain, linearity and input matching requirements, L_g can then be chosen such that L_g, L_s and C_{gs} resonate at a specified frequency ω_0 in (2-4). In other words, L_g is determined according to the following condition:

$$\omega_0(L_g + L_s) = \frac{1}{\omega_0 C_{gs}}$$

$$\Rightarrow \quad \omega_0 = \frac{1}{\sqrt{C_{gs}(L_g + L_s)}} \tag{2-4}$$

At the resonance frequency where the imaginary part of impedance, i.e. the reactance contributed from the inductors (L_s and L_g) and capacitor C_{gs} are canceled out, the input impedance is left with just the first term in (2-2), i.e. the resistance representing the real part of impedance.

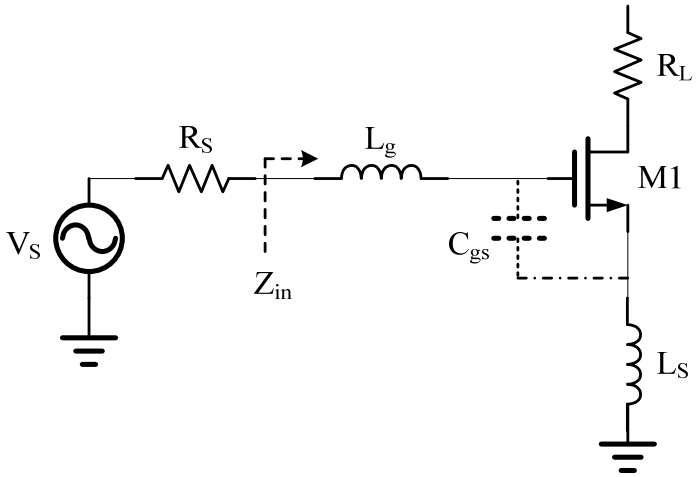


Fig. 2. 3 Inductive source degeneration matching technique

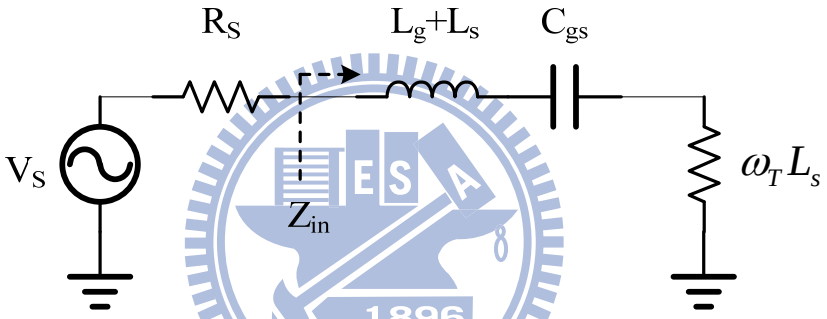


Fig. 2. 4 Equivalent circuit of inductive source degeneration matching

Note that the form of (2-2) clearly shows that the input impedance is purely resistive at only one frequency (at resonance), however, so this method can provide only a narrowband impedance matching.

2.1.3 Shunt-Series Resistor Feedback Architecture [3]

The shunt-series resistor feedback architecture as shown in Fig. 2.5 can provide good wideband matching and flat gain, but tends to suffer from poor noise figure (NF) and large power dissipation. [11, 19-23]

The impedance Z_{in} can be written as R_{FM}. The resistor $R_{FM} = \frac{R_F}{1 - A_v}$ represents the Miller equivalent input resistance of R_F, where A_v is the open-loop voltage gain ($A_v \approx g_{m1} R_L$). We design $R_{FM} = R_s = 50\Omega$ to achieve a matching to 50-Ω. The architecture as shown in Fig.

2.5 suffers from fewer problem than the architecture as shown in Fig. 2.2, yet the resistive feedback network continues to generate thermal noise of its own and also fails to present to the transistor an impedance that equals Z_{opt} at all frequencies. As a consequence, the overall amplifier's noise figure, while usually much better than that of Fig. 2.2.

In the resistive shunt-feedback amplifier, input resistance is determined by the feedback resistance (R_F) divided by the loop-gain of the feedback amplifier. Therefore, the feedback resistor tends to be a few hundred ohms in order to match the low signal source resistance of typically 50-Ω. This inappropriately large resistance generally leads to significant NF degradation. Furthermore, even with a moderate amount of voltage gain, the amplifier requires a rather large amount of current, especially in the CMOS, due to its strong dependence on the voltage gain from the transconductance of the amplifying transistor M1. [15] As a consequence, it will consume higher power dissipation and require good quality on-chip resistors for achieving a precise feedback resistance.

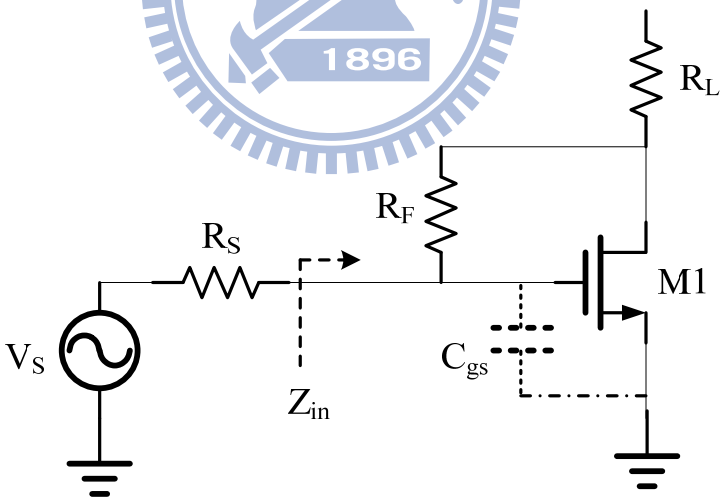


Fig. 2. 5 Shunt-series resistor feedback matching technique

2.1.4 Common-Gate Input Architecture (1/gm termination) [3]

The last input matching method for realizing resistive input impedance is to use a common-gate input architecture shown in Fig. 2.6. Since the resistance looking into the

source terminal is $1/g_m$, a proper selection of device size and bias current can provide the desired 50-Ω resistance. Using the common-gate input architecture, the minimal NF which can be achieved at low frequencies and neglecting gate current noise is $NF \approx 1 + \frac{\gamma}{\alpha} \geq 2.2\ dB$ where $\alpha \triangleq \frac{g_m}{g_{d0}}$ and γ is the coefficient of channel thermal noise. Note that for long channel devices, NF=2.2 dB corresponding to α = 1 and γ = 2/3. As for short channel devices ($\alpha \leq 1, \gamma \geq \frac{2}{3}$), NF perhaps as high as 4.8 dB ($\frac{\gamma}{\alpha} = 2$). The noise figure will become significantly worse at higher frequencies and when gate current noise is taken into account.

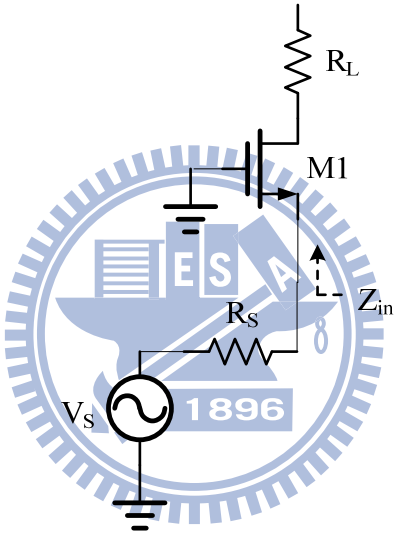


Fig. 2. 6 Common gate input matching technique

As compared to the conventionally used common-source topology, the common-gate input architecture is an efficient way to achieve a broadband matching with small chip area. Because it doesn't need many inductors to achieve wideband input matching. However, it can't provide sufficient gain and lower noise figure with low power consumption [24].

2.1.5 LNA design and Comparison of Input Matching Architecture

For LNA design, the trade-offs between the gain, noise, and power consumption are critical factors to be considered for the selection of circuit topologies, impedance matching methods, and details to the active and passive devices design. In the following, the major

requirements and trade-offs are described, tentatively as a design guideline.

1) Low power dissipation :

In general, low power RF circuit design is challenging, due to trade-off between gain, linearity, and noise, etc. For a broadband LNA design, the power dissipation becomes even worse and makes low power design more difficult in the broadband circuits.

2) Input and Output matching (return loss)

In wireless receiver, the components placed in front of LNA are usually filter and antenna with the characteristic impedance 50-Ω, so input impedance matching of LNA must realize a match to 50-Ω. Unfortunately, the architecture for an input impedance matching is always different from that for an optimum noise matching.

3) High power gain

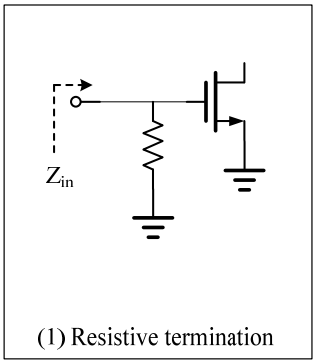
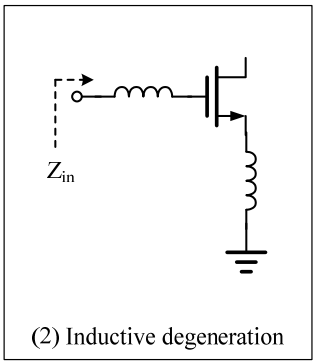
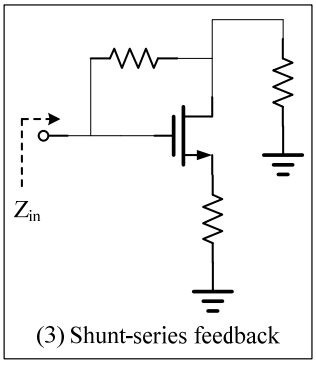
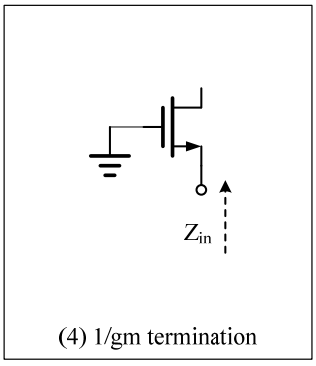
For LNA design, power gain is one of the most important performance parameters to be considered. Power gain should be sufficiently high to amplify the small RF signal from the receiver and then reduce the noise generated from the following stages. However, the larger power gain will generally degrade the linearity in LNAs.

4) Low Noise Figure (NF):

As it is well known that LNA acting as the amplifier in a receiver system, the noise generated from itself dominates the noise from all other components following the LNA. Thus, minimizing noise figure (NF) becomes the most important target in LNA design. As a matter of fact, the optimization of NF is sometime traded off with power gain and power dissipation.

The benchmark of various input matching methods as mentioned is summarized in Table 2.1.

Table 2. 1 Comparison of LNA Input matching architectures

Input matching architectures	Advantages	Drawbacks
 (1) Resistive termination	Favorable for wideband input matching. Good power gain. Good linearity.	Higher noise figure (extra thermal noise from the resistor).
 (2) Inductive degeneration	Suitable for narrow band input matching. Good noise performance. Good power gain. Good linearity.	Limited to narrow band. Large area consumed by on-chip inductors
 (3) Shunt-series feedback	Suitable for wideband input matching. Good power gain.	High power dissipation. Higher noise figure. (Feedback resistor generate thermal noise). Poor reverse isolation.
 (4) 1/gm termination	Suitable for wideband input matching. Good linearity. Good reverse isolation.	Lower power gain. Higher noise figure.

2.2 Chebyshev Filter [25, 26]

Chebyshev filters are analog or digital filters having a steeper roll-off and more passband ripple or stopband ripple than Butterworth filters. Chebyshev filters have the property that they minimize the error between the idealized filter characteristic and the actual over the range of the filter, but with ripples in the passband. This type of filter is named in honor of Pafnuty Chebyshev because their mathematical characteristics are derived from Chebyshev polynomials.

Because of the passband ripple inherent in Chebyshev filters, filters which have a smoother response in the passband but a more irregular response in the stopband are preferred for some applications.

2.2.1 Theory of Chebyshev Filter [25, 26]

The gain (or amplitude) response as a function of angular frequency ω of the *n*th order low pass filter is

$$G_n(\omega) = |H_n(j\omega)| = \frac{1}{\sqrt{1+\varepsilon^2 T_n^2(\frac{\omega}{\omega_0})}} \tag{2-5}$$

where ε is the ripple factor, ω_0 is the cutoff frequency and $T_n(\ )$ is a Chebyshev polynomial of the *n*th order.

The passband exhibits equiripple behavior, with the ripple determined by the ripple factor ε. In the passband, the Chebyshev polynomial alternates between 0 and 1 so the filter gain will alternate between maxima at $G = 1$ and minima at $G = \frac{1}{\sqrt{1+\varepsilon^2}}$. At the cutoff frequency ω_0 the gain again has the value $\frac{1}{\sqrt{1+\varepsilon^2}}$ but continues to drop into the stop band as the frequency increases. This behavior is shown in the diagram on the Fig. 2.7.

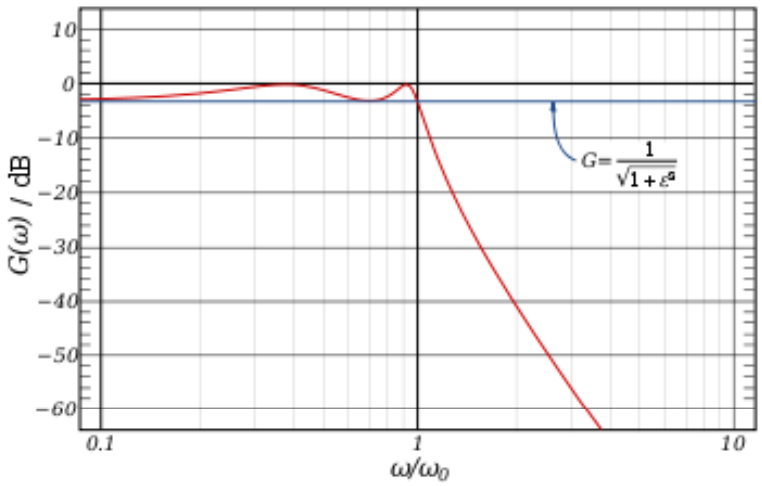


Fig. 2. 7 The frequency response of a fourth-order Chebyshev low-pass filter with $\varepsilon = 1$

The order of a Chebyshev filter is equal to the number of reactive components (for example, inductors) needed to realize the filter using analog electronics.

The ripple is often given in dB:

$$\text{Ripple in dB} = 20\log\frac{1}{\sqrt{1+\varepsilon^2}} \tag{2-6}$$

so that a ripple amplitude of 3 dB results from $\varepsilon = 1$.

a. Poles and zeroes

For simplicity, assume that the cutoff frequency is equal to unity. The poles (ω_{pm}) of the gain of the Chebyshev filter will be the zeroes of the denominator of the gain. Using the complex frequency s:

$$1 + \varepsilon^2 T_n^2(-js) = 0 \tag{2-7}$$

Defining $-js = \cos(\theta)$ and using the trigonometric definition of the Chebyshev polynomials yields:

$$1 + \varepsilon^2 T_n^2(\cos(\theta)) = 1 + \varepsilon^2 \cos^2(n\theta) = 0 \tag{2-8}$$

Solving for θ

$$\theta = \frac{1}{n}\arccos\left(\frac{\pm j}{\varepsilon}\right) + \frac{m\pi}{n} \tag{2-9}$$

where the multiple values of the arc cosine function are made explicit using the integer index

m. The poles of the Chebyshev gain function are then:

$$s_{pm} = j\cos(\theta) = j\cos(\frac{1}{n}\arccos(\frac{\pm j}{\varepsilon}) + \frac{m\pi}{n}) \quad (2\text{-}10)$$

Using the properties of the trigonometric and hyperbolic functions, this may be written in explicitly complex form:

$$s_{pm}^{\pm} = \pm\sinh(\frac{1}{n}\operatorname{ar}\sinh(\frac{1}{\varepsilon}))\sin(\theta_m) + j\cosh(\frac{1}{n}ar\sinh(\frac{1}{\varepsilon}))\cos(\theta_m)$$

(2-11)

where m = 1, 2,..., n and $\theta_m = \frac{\pi}{2}\frac{2m-1}{n}$.

This may be viewed as an equation parametric in θ_n and it demonstrates that the poles lie on an ellipse in s-space centered at $s = 0$ with a real semi-axis of length $\sinh(\frac{ar\sinh(\frac{1}{\varepsilon})}{n})$ and an imaginary semi-axis of length of $\cosh(\frac{ar\sinh(\frac{1}{\varepsilon})}{n})$.

2.2.2 Applications of Chebyshev Filter [27]

Filters are signal-processing circuits used to modify the frequency spectrum of an electrical signal. They may be used to amplify, attenuate, or reject a certain range of frequencies of their input signals. Filters are pervasive in integrated circuits because of their vast number of applications. Some applications include noise reduction in communication systems, band-limiting of signals before sampling them, conversion of sampled signals into continuous-time signals, signal demodulation, improving the sound quality of audio system components such as loudspeakers and receivers, and many others.

The Chebyshev response is a mathematical strategy for achieving a faster roll-off by allowing ripple in the frequency response. Analog and digital filters that use this approach are called Chebyshev filters. For instance, analog Chebyshev filters were used for analog-to-digital and digital-to-analog conversion.

The Chebyshev gives a much steeper roll-off, but passband ripple makes it unsuitable for audio systems. It is superior for applications in which the passband includes only one frequency of interest (e.g., the derivation of a sine wave from a square wave, by filtering out the harmonics).

2.3 linearity [28]

Linearity is one of the key requirements in LNA design to maintain linear operation in the presence of a large interfering signal and when the input is driven by a large signal. Any nonlinear transfer function can be mathematically written as **a** series expansion of power-law terms unless the system contains memory. The input V_i and output V_o of a two-port network can be related by a power series. For simplicity, we make an approximation to the third order term:

$$V_o = \alpha_1 V_i + \alpha_2 V_i^2 + \alpha_3 V_i^3 \tag{2-12}$$

where $\alpha_1, \alpha_2, \alpha_3$ are constants.

2.3.1 Harmonic Distortion [28]

If a sinusoidal waveform is applied to a nonlinear system, the output generally exhibits frequency dependent components that are integer multiples of the input frequency. In (2-12), setting $V_i(t) = A\cos(\omega t)$, then

$$V_o(t) = \alpha_1 A\cos(\omega t) + \alpha_2 A^2 \cos(\omega t)^2 + \alpha_3 A^3 \cos(\omega t)^3 \tag{2-13.1}$$

$$= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \tag{2-13.2}$$

In (2-13.1), the term with the input frequency ω is called the “fundamental” and the higher-order terms the “harmonics”. The first term in (2-13.1) is the linear term and is the ideal output if the two-port network is completely linear. Other terms in (2-13.1) are responsible for nonlinearities, and they cause a DC shift as well as distortion at frequencies

2ω, 3ω, and higher harmonics derived in (2-13.2), which result in either gain compression or gain expansion. It can be observed from (2-13.2) that distortion is present in any signal level.

2.3.2 1-dB Compression Point (P1dB) [28]

In most circuits of interest, the output is a "compressive" or "saturating" function of the input; that is, the gain approaches zero for sufficiently high input levels. In (2-13) this occurs if $\alpha_3 < 0$. Written as $\alpha_1 A + \frac{3\alpha_3 A^3}{4}$, $\alpha_1 A$ represents the fundamental amplitude and the gain is therefore a decreasing function of the third-order harmonic proportional to $\alpha_3 A^3$. In RF circuits, this effect is quantified by the "1-dB compression point", defined as the input signal level that causes the small-signal gain to drop by 1 dB. As shown in Fig. 2.8, which is plotted on a log-log scale as a function of the input level, the output level falls below its ideal value by 1 dB at the 1-dB compression point [28].

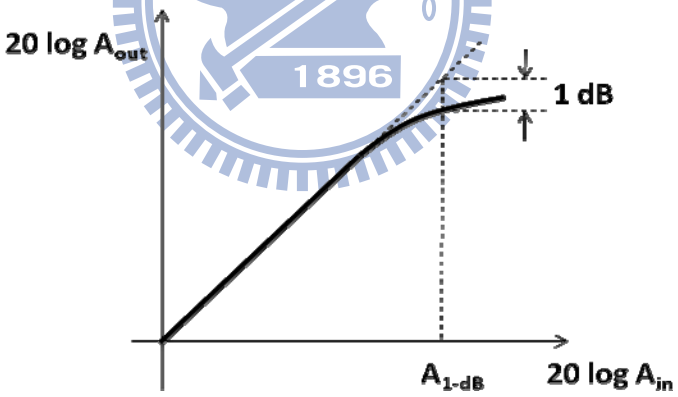


Fig. 2. 8 Definition of the 1-dB compression point

To calculate the 1-dB compression point, we can write from (2-13.3)

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{1-dB}^2\right| = 20\log|\alpha_1| - 1dB \tag{2-14}$$

That is,

$$A_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2-15}$$

2.3.3 Intermodulation [28]

Harmonic distortion that was introduced previously is the result of nonlinearities due to a single sinusoidal input. When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. Called intermodulation (IM), this phenomenon arises from "mixing" (multiplication) of the two signals when their sum is raised to a power greater than unity. To investigate the effects of both harmonic distortion and intermodulation, **we** assume that the input signal is composed of two different frequencies ω_1 and ω_2 given in (2-16)

$$V_i(t) = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t) \tag{2-16}$$

(2-16) can be substituted into (2-12). Thus, the output can be expressed as

$$\begin{aligned} V_o(t) = {} & \alpha_1[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)] + \alpha_2[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)]^2 \\ & + \alpha_3[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)]^3 \end{aligned} \tag{2-17}$$

Expanding the right-hand side and discarding the dc terms and harmonics, we obtain intermodulation products expressed in (2-18) and (2-19) for the second order and (2-20) for the third order IM products, namely IM2 and IM3.

$$\omega = \omega_1 \pm \omega_2 : \alpha_2 A_1 A_2\cos[(\omega_1 + \omega_2)t] + \alpha_2 A_1 A_2\cos[(\omega_1 - \omega_2)t] \tag{2-18}$$

$$= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4}\cos[(2\omega_1 + \omega_2)t] + \frac{3\alpha_3 A_1^2 A_2}{4}\cos[(2\omega_1 - \omega_2)t] \tag{2-19}$$

$$= 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^2 A_1}{4}\cos[(2\omega_2 + \omega_1)t] + \frac{3\alpha_3 A_2^2 A_1}{4}\cos[(2\omega_2 - \omega_1)t] \tag{2-20}$$

and the fundamental components written in (2-21)

$$\begin{aligned} \omega = \omega_1, \omega_2 : {} & (\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2)\cos(\omega_1 t) \\ & + (\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2)\cos(\omega_2 t) \end{aligned} \tag{2-21}$$

Of particular interest are the third-order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, illustrated in Fig. 2.9 in which the input RF signals are two-tone with two different frequencies such as

ω_1 and ω_2

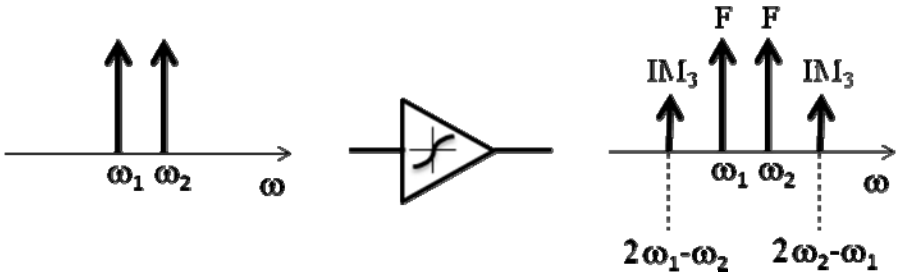


Fig. 2. 9 Intermodulation in a nonlinear system

where it is assumed that $A_1 = A_2 = A$.

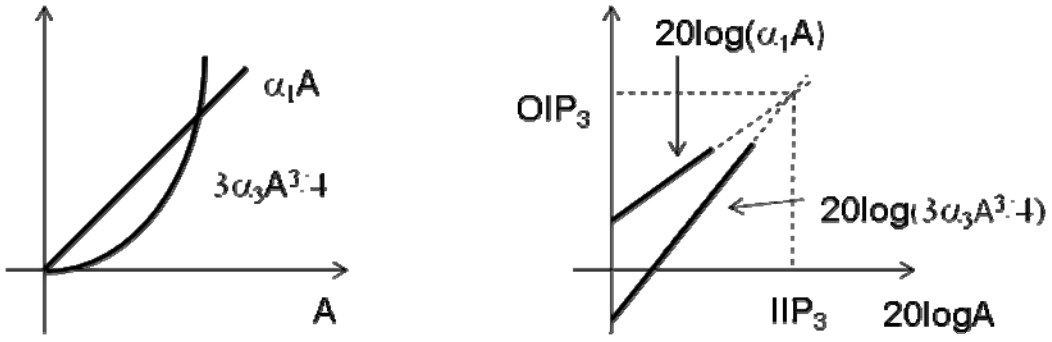
From Fig. 2.9, it is apparent that the third-order intermodulation distortion IM3 signals are close to the signals of interest F, which makes the filtering out of IM3 signals difficult when recovering the signals of interest. Therefore minimizing intermodulation distortion is a key objective in many RF circuit design.

2.3.4 Third-Order Intercept Point (IIP3) [28]

From **(2-17)~(2-21)** and let $A_1 = A_2 = A$, we can drive the expression

$$V_o(t) = (\alpha_1 + \frac{9}{4}\alpha_3 A^2)A\cos(\omega_1 t) + (\alpha_1 + \frac{9}{4}\alpha_3 A^2)A\cos(\omega_2 t) + \frac{3}{4}\alpha_3 A^3 \cos[(2\omega_1 - \omega_2)t] + \frac{3}{4}\alpha_3 A^3 \cos[(2\omega_2 - \omega_1)t] + \ldots \quad (2\text{-}22)$$

We note that as the input amplitude A is small to keep $\alpha_1 >> \frac{9}{4}|\alpha_3|A^2$, the fundamentals increase proportional to A, whereas if the input level A increases to the intercept point so that $\alpha_1 >> \frac{9}{4}|\alpha_3|A^2$ is no longer valid, the gain will drop and the third-order IM products in proportion to A^3 will take over the fundamentals, as shown in Fig. 2.10(a). Plotted on a logarithmic scale [Fig. 2.10(b)], the magnitude of the IM products grows at three times the rate at which the main components increase. The third-order intercept point, namely IP_3 is defined to be at the intersection of the two lines. The horizontal coordinate of this point is called the input IP_3 (IIP_3), and the vertical coordinate is called the output IP_3 (OIP_3).



(a) (b)

Fig. 2. 10 (a) The linear gain and the nonlinear component (b) The IIP_3 and OIP_3

If $\alpha_1 \gg \frac{9}{4}\alpha_3 A^2$, the input level for which the output components at ω_1 and ω_2 have the same amplitude as those at those at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ is given by

$$|\alpha_1| A_{IP3} = \frac{3}{4}|\alpha_3| A_{IP3}^3 \tag{2-23}$$

Thus, the input IP_3 is

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2-24}$$

2.4 Stability [29]

One more important consideration for an amplifier design like LNA is the assurance of stability. For LNAs in the form of a two-port network, the requirement for ensuring stability is that it must not produce an output with oscillatory behavior. The stability of a two-port network can be determined from the S-parameters, the matching networks, and the terminations. Simpler tests can be used to determine unconditional stability [29]. One of these is the K−△ test, where it can be shown that a device will be unconditionally stable if Rollet's condition [30], defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2-25}$$

along with the auxiliary condition that

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2-26}$$

are simultaneously satisfied. These two conditions are necessary and sufficient for unconditional stability.

While the K−△ test of (2-25)~(2-26) is a mathematically rigorous condition for unconditional stability, it cannot be used to compare the relative stability of two or more devices since it involves constraints on two separate parameters. However, a new criterion has been proposed [31] that combines the S parameters in a test involving only a single parameter, μ, defined as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21}S_{12}|} > 1 \tag{2-27}$$

Thus, if $\mu > 1$, the device is unconditionally stable. In addition, it can be said that larger values of μ implies greater stability.

2.5 Noise in Two-Port System [3]

2.5.1 Noise Factor

Noise factor (F) is defined as the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output. Considering a network with gain G and noise N_a, noise factor then can be express as (2-28) [3]

$$F \equiv \frac{S_i / N_i}{S_o / N_o} = \frac{S_i / N_i}{(GS_i)/[G(N_i + N_a)]} = \frac{N_i + N_a}{N_i} = \frac{N_o}{GN_i} = \frac{\textit{Total noise power @ output}}{\textit{Noise power @ output due to source only}}$$

(2-28)

Generally we use this measure in the unit of dB, namly noise figure (NF) written in (2-29)

$$NF = 10 \log F \tag{2-29}$$

A useful measure of the noise performance of a system is the noise factor, denoted as F

and given in (2-28). To define it and understand why it is useful, consider a noisy (but linear) two-port network driven by a source that has an impedance Z_s and an equivalent series noise voltage $\overline{e_s^2}$, illustrated in Fig. 2.11.

If we are concerned only with overall input-output behavior, it is an unnecessary complication to keep track of all of internal noise source. Fortunately, the net effect of all of those sources can be represented by just one pair of external sources like a noise voltage $\overline{e_n^2}$ and a noise current $\overline{i_n^2}$ as shown in Fig.2.12. This simplification allows a rapid evaluation of how the source impedance affects the overall noise performance. As a consequence, we can identify the criteria, which one must satisfy for optimum noise performance.

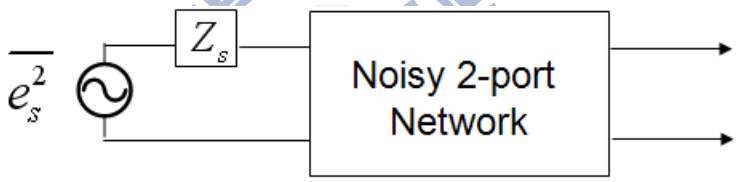


Fig. 2. 11 Noisy two-port driven by noisy source

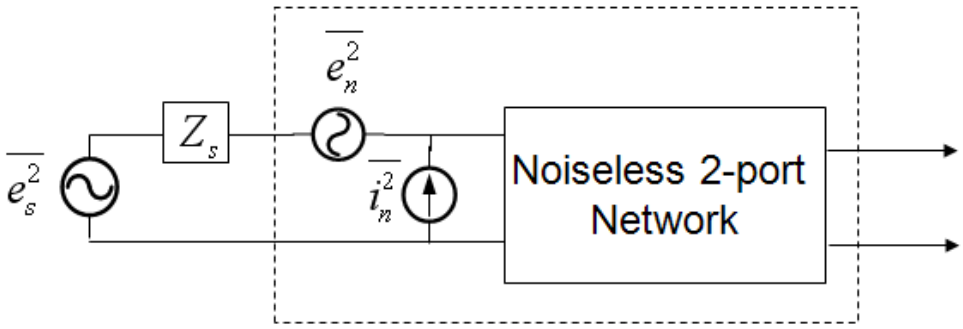


Fig. 2. 12 Equivalent circuit for two-port noise model

Carrying out the calculations based on the equivalent circuit of noisy two-port illustrated in Fig.2.12, the noise factor is written as

$$F = \frac{N_i + N_a}{N_i} = \frac{\overline{e_s^2} + \overline{|e_n + Z_s i_n|^2}}{\overline{e_s^2}} \tag{2-30}$$

In order to accommodate the possibility of correlations between e_n and i_n, express e_n as the sum of two components in (2-31) in which e_{nc}, represents the term correlated with i_n, and e_{nu}, the un-correlated term.

$$e_n = e_{nc} + e_{nu} \tag{2-31}$$

Since e_n is correlated with i_n, it may be treated as proportional to $\mathbf{i_n}$ through a constant namely Z_C whose dimensions are those of impedance:

$$e_{nc} = Z_c i_n \tag{2-32}$$

Combining (2-30), (2-31), and (2-32), the noise factor becomes

$$F = \frac{\overline{e_s^2} + \overline{|e_{nu} + (Z_c + Z_s) i_n|^2}}{\overline{e_s^2}} = 1 + \frac{\overline{e_{nu}^2} + |Z_c + Z_s|^2 \overline{i_n^2}}{\overline{e_s^2}} \tag{2-33}$$

The expression in (2-33) contains three independent noise sources, each of which may be treated as thermal noise produced by an equivalent resistance or conductance:

$$R_u \equiv \frac{\overline{e_{nu}^2}}{4kT\Delta f}, \quad R_s \equiv \frac{\overline{e_s^2}}{4kT\Delta f}, \quad G_n \equiv \frac{\overline{i_n^2}}{4kT\Delta f} \tag{2-34}$$

Using these equivalences, the expression for noise factor can be written purely in terms of impedances and admittances:

$$F = 1 + \frac{R_u + |Z_c + Z_s|^2 G_n}{R_s} = 1 + \frac{R_u + \left[(R_c + R_s)^2 + (X_c + X_s)^2 \right] G_n}{R_s} \tag{2-35}$$

where $Z_c = R_c + jX_c$ is the correlation impedance and $Z_s = R_s + jX_s$ is the source impedance.

2.5.2 Optimum Source Impedance [3]

Once a given two-port's noise has been characterized with its four noise parameters (R_c, X_c, R_u, and G_n), (2-35) allows us to identify the general conditions for minimizing

the noise factor. Taking the first derivative with respect to the source impedance and setting it equal to zero yields the optimal source reactance X_{opt} and resistance R_{opt} in (2-36) and (2-37), respectively

$$X_s = -X_c = X_{opt} \tag{2-36}$$

$$R_s = \sqrt{\frac{R_u}{G_n} + R_c^2} = R_{opt} \tag{2-37}$$

Hence, to minimize the noise factor, the source reactance X_s should be made equal to the inverse of the correlation reactance X_c, while the source resistance R_s should be set equal to the value in (2-37).

The noise factor corresponding to this optimal condition is the minimum noise factor, namely F_{min}, which is derived by direct substitution of (2-36) and (2-37) into (2-35) and expressed as (2-38):

$$F_{\min} = 1 + 2G_n\left(R_{opt} + R_c\right) = 1 + 2G_n\left(\sqrt{\frac{R_u}{G_n} + R_c^2} + R_c\right) \tag{2-38}$$

We may also express the noise factor in terms of $F_{\min}$ and the source impedance:

$$F = F_{\min} + \frac{G_n}{R_s}\left[\left(R_s - R_{opt}\right)^2 + \left(X_s - X_{opt}\right)^2\right] \tag{2-39}$$

2.6 Noise Sources in MOSFET [3]

To develop good CMOS RF circuit design skills, a fundamental understanding of noise source in a MOSFET is necessary. We will focus on the inherent noise of a MOSFET, which can be categorized into two parts: drain noise source and gate noise source.

2.6.1 Drain Noise Source

For a MOSFET under operation, the conducting channel behaves like a voltage-controlled resistor. This resistor contributes thermal noise at the drain terminal, as

illustrated in Fig.2.13. This noise can be expressed as [3]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f$$

(2-40)

Where g_{d0} is the drain-source transconductance at V_{DS}=0V. For long channel devices, γ is close to unity in its triode region and decreases to about 2/3 when in saturation

(i.e. $\frac{2}{3} \le \gamma \le 1$). In long channel case, g_{d0} is equal to the gate transconductance g_m in saturation region which leads to a familiar result

$$\overline{i_{nd}^2} = \frac{8}{3}kTg_{d0}\Delta f = \frac{8}{3}kTg_m\Delta f \qquad (2\text{-}41)$$

Due to the carrier heating driven by the large electric fields in short channel devices [3] or channel length modulation effect [3], γ may become larger than 2 or even larger.

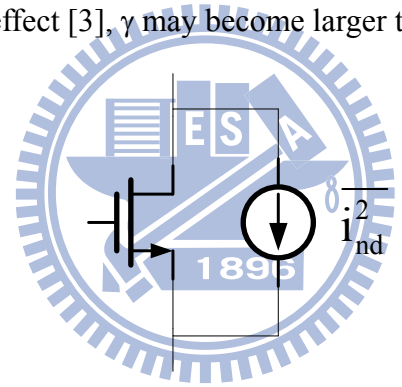


Fig. 2. 13 Drain current noise model

2.6.2 Gate Noise Source

Fig.2.14 presents the gate noise circuit model in which the gate noise can be introduced from the channel region through the capacitive coupling (C_{gs}) to the gate terminal, due to the fluctuating potential. Also, noisy gate current may be produced by thermally noisy resistive gate material, denoted as gate resistance (R_g). This component is defined as extrinsic gate noise, which is distinguished from the intrinsic (induced) gate noise originated from channel potential fluctuation and coupling through C_{gs}. As the operation frequency increases, contribution of this noise can't be neglected. This noise can be expressed as (2-42) [3]

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2-42}$$

where g_g is given by

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2-43}$$

Because the channel noise and induced gate noise have a common origin, they do have correlation. The correlation coefficient is usually expressed as c in (2-44)

$$c \equiv \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}}\sqrt{\overline{i_{nd}^2}}} \approx -0.395\, j \tag{2-44}$$

The value of -0.395j is exact for long-channel devices. The correlation can be treated by expressing the gate noise as the sum of the two components, the first of which is fully correlated with the drain noise, and the second of which is uncorrelated with the drain noise. Hence, the gate noise is re-expressed as

$$\overline{i_{ng}^2} = 4kT\delta g_g (1 - |c|^2)\Delta f + 4kT\delta g_g |c|^2 \Delta f \tag{2-45}$$

where the first term is uncorrelated and the second term is correlated to drain noise.

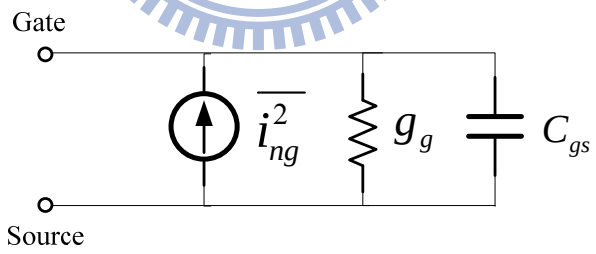


Fig. 2. 14 Gate noise circuit model

2.6.3 MOSFET Noise Model

A standard MOSFET noise model can be expressed in Fig. 2.15, where $\overline{i_{ng}^2}$ is the gate noise source, $\overline{i_{nd}^2}$ is the drain noise source.

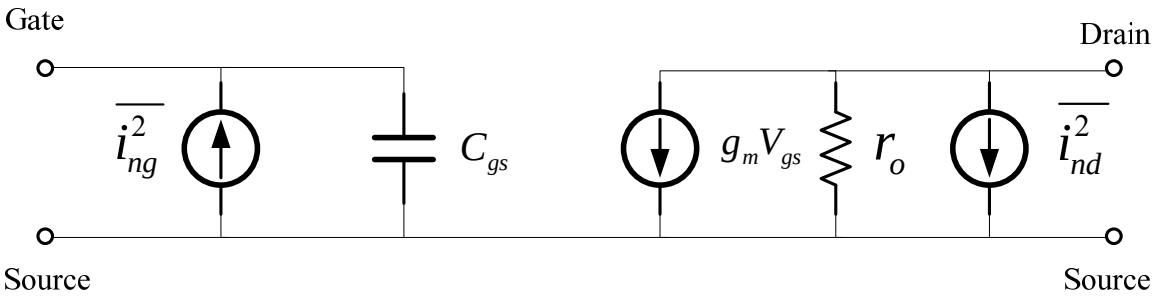


Fig. 2. 15 MOSFET noise model

2.7 Dynamic Threshold Voltage CMOS

The threshold voltage (V_{th}) of a MOSFET is expressed as

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}\right) \tag{2-46}$$

where V_{th0} is the threshold voltage when $V_{bs} = 0$, γ is the body-effect coefficient, φ_f is the bulk Fermi potential. Note that V_{bs} is the voltage between body and source. Thus, changing V_{bs} can modify V_{th}, which can achieve a dynamic threshold voltage MOSFET (DTMOS). Threshold voltage is decreased as the external bias V_{bs} is increased toward the forward direction for the substrate. Usually, the junction between body and source is zero-biased or reverse-biased. To further improve performance under continuously scaled supply voltage (V_{DD}), forward body bias (FBB) method becomes attractive for reducing V_{th}, according to (2-46). Here, we introduce this concept into low voltage LNA design. To implement forward body bias scheme in NMOSFET, a deep N-well process is needed as shown in Fig.2.16, which can provide separate body region for each NMOS transistor and allow the freedom of body biases. In addition, a deep N-well process can reduce noise cross-talk through the substrate. In this thesis, FBB method has been extensively used in low-power UWB LNA and ultra-low power narrow band LNA design.

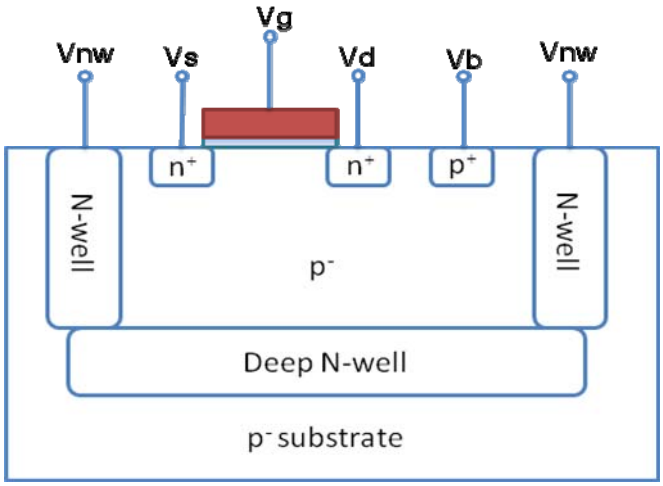


Fig. 2. 16 Cross-sectional view of the DTMOS device with deep N-well structure

Chapter 3

Low-Power UWB LNA Design using Forward Body Biasing Technique for 3.1~10.6 GHz Wireless Receivers

3.1 Introduction

Wideband systems have recently gained much attention due to their capability of high data rate transmission. The so called ultra-wide band (UWB) technology can pave the way for a wide range of applications, which use the frequency bands in 3.1 ~ 10.6 GHz and can co-exist with the already licensed spectrum users. To interface with the antenna and pre-select filter in a receiver system, the low-noise amplifier (LNA) input impedance should be close to 50-Ω across the band from 3.1 to 10.6 GHz.

There are several existing solutions for wideband amplifiers in CMOS technology. The distributed amplifier (DA) is widely used for wideband application due to its intrinsic broadband frequency response going all the way down to dc along with good input and output impedance matching. Yet, so far, high power consumption and large die area have hampered its widespread applications [32-34]. Recently, the RC feedback topology is widely used for wideband application. It can provide good wideband matching and flat gain but it can't provide sufficient gain and lower noise figure with low power consumption [35, 36]. Another efficient way to achieve a broadband matching is the common-gate input topology [24]. However, the mentioned weaknesses in terms of gain, noise, and power consumption cannot be solved. For the UWB technology to be widely employed in the hand-held wireless applications, it cannot be avoided that power consumption is one of the main challenges. In this chapter, we present a UWB LNA with broadband impedance matching, low noise figure (NF), low power consumption, and small chip-area. We focus on the design and

implementation of UWB LNA with very low power consumption in a 0.13um CMOS technology.

3.2 Circuit Architectures

Fig. 3.1 illustrates the circuit architecture of our proposed UWB LNA which is composed of an input matching network, cascode topology, shunt peaking circuit and output buffer. For a circuit analysis, this UWB LNA can be divided into three blocks – input matching stage, amplifying stage and source-follower buffer stage.

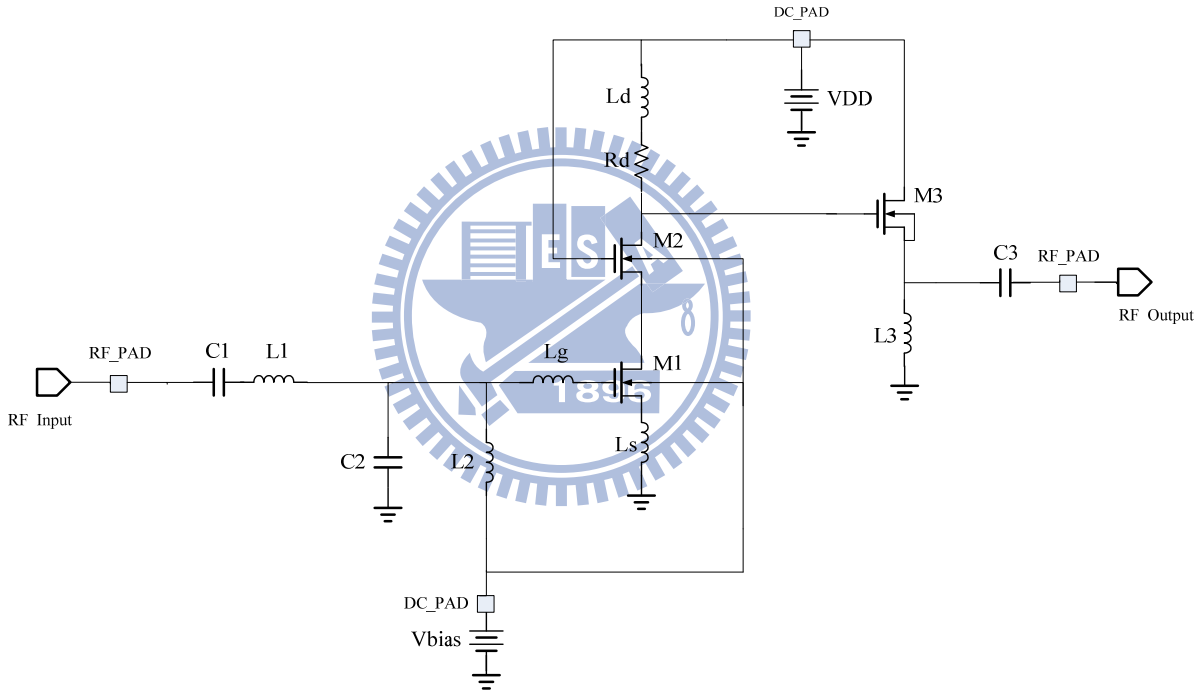


Fig. 3. 1 Circuit architecture of the UWB LNA

In the following, the function of each element in the circuit architecture will be interpreted to explain the UWB LNA design concept. First for the input matching stage, a three-section Chebyshev filter was used, combining the gate-source capacitance (C_{gs}) of M1 and the source degeneration inductance L_s. This input matching circuit is aimed at a broadband matching from 3.1 to 10.6 GHz.

Secondly for the amplifying stage, a cascode topology with forward body biasing (FBB)

scheme was adopted to reduce the supply voltage and power consumption. The cascade structure can offer the advantages, such as less Miller effect, better reverse isolation, wider frequency response, and lower noise figure [28, 29]. FBB technique can facilitate low-voltage UWB LNA design by reducing transistor's threshold voltage (V_T). Shunt peaking method can improve the gain at low frequency and extend the usable bandwidth.

Finally for source-follower buffer stage, an output matching buffer composed of M1, L3, and C3 shown in Fig.3.1 was designed to achieve flat gain over the entire bandwidth and improve the gain at high frequency. Note that the dimensions of M3, L3 and C3 will determine the high-frequency characteristic of UWB LNA and an appropriate selection of the layout dimensions is indispensable to achieve a wideband output matching from 3.1 to 10.6 GHz.

3.3 Circuit Topology Analysis

3.3.1 Input Matching Circuit and Analysis [37-39]

Fig. 3.2 illustrates an input impedance matching circuit in the form of multi-section LC networks proposed for UWB LNA in this thesis. The implemented matching network is built and operates based on the LC resonance matching technique. In the following, the theory and circuit operation principle of this matching network will be described to detail.

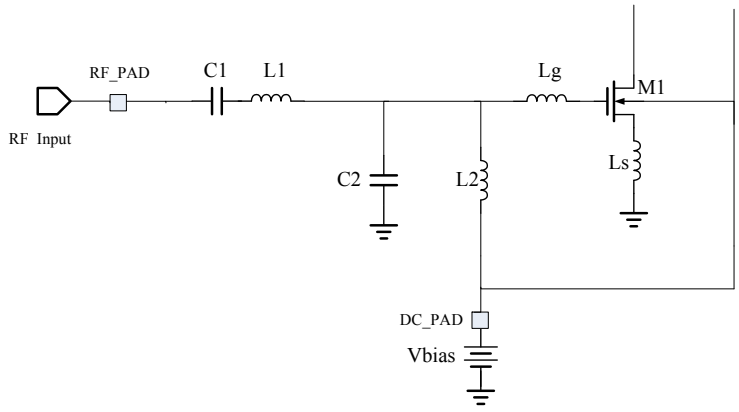


Fig. 3. 2 The circuit schematics of input matching network for UWB LNA

a. Series LC resonance method:

First, a series LC resonance network is depicted in Fig. 3.3 and the impedance corresponding to this LC network can be derived as shown in (3-1).

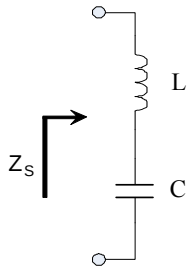


Fig. 3. 3 Series LC resonance circuit

$$Z_s = j\omega L + \frac{1}{j\omega C} = j(\omega L - \frac{1}{\omega C}) \tag{3-1}$$

$For \;\; Z_s = 0$

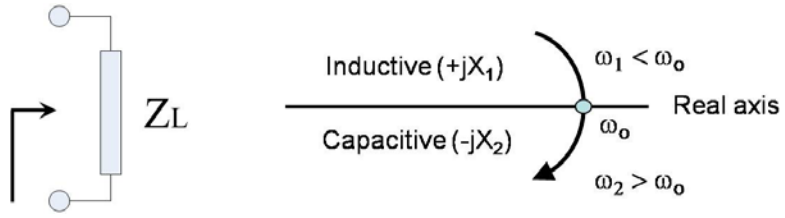
$$\omega = \omega_0 = \frac{1}{\sqrt{LC}}$$

ω_0 is the series resonance frequency

$for \;\; \omega < \omega_0 \;:\; Z_s = -jX \;:$ capacitive mode reactance

$for \;\; \omega > \omega_0 \;:\; Z_s = +jX \;:$ inductive mode reactance

Now, set a load Z_L illustrated in Fig. 3.4 (a) and the impedance of Z_L under varying frequencies is shown in the Z-Smith chart in Fig. 3.4 (b). It shows that Z_L is a kind of inductive mode impedance at lower frequency $\omega_1 < \omega_0$ and becomes a capacitive mode at higher frequency $\omega_2 > \omega_0$.



(a) (b)

Fig. 3. 4 (a) Load Z_L (b) The impedance modes of load Z_L under varying frequencies, drawn in the Z-Smith chart

Then, we can add a series LC resonance circuit to the load Z_L, as shown in Fig. 3.5.

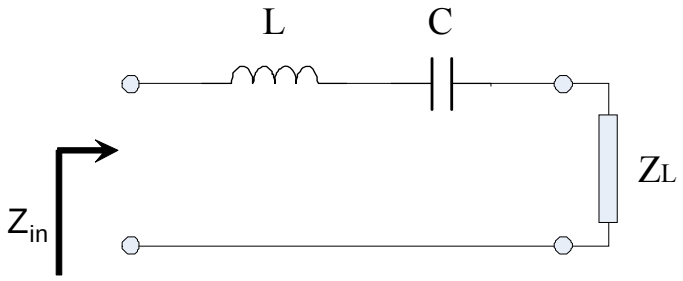


Fig. 3. 5 Add a series LC resonance circuit to the load Z_L

The above analysis provide us a guideline to select suitable L and C to generate capacitive mode impedance ($-jX_2$) at lower frequency and inductive mode impedance(jX_1) at higher frequency. In the way, the created series LC network can offer the required impedances to just cancel out that of load Z_L, i.e. the inductive mode jX_1 at lower frequency and capacitive mode $-jX_2$ at higher frequency. As a result, the equivalent impedance of the input Z_{in} can approach the real axis, shown in Fig. 3.6.

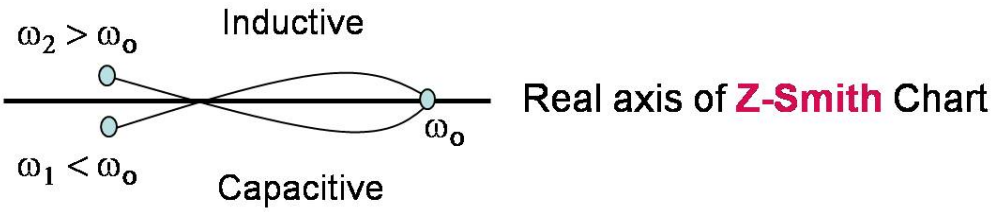


Fig. 3. 6 Effect of adding a series LC resonance circuit to the load in the Z-Smith chart

b. Parallel LC resonance method:

Fig. 3.7 illustrates a parallel LC resonance network. The admittance corresponding to this parallel LC network can be derived as shown in (3-2).

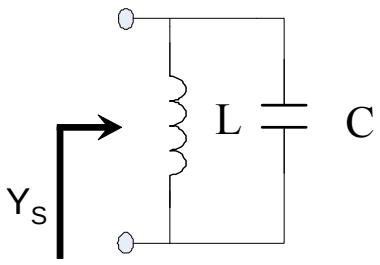


Fig. 3. 7 Parallel LC resonance circuit

$$Y_s = j\omega C + \frac{1}{j\omega L} = j(\omega C - \frac{1}{\omega L}) \tag{3-2}$$

$For \quad Y_s = 0$

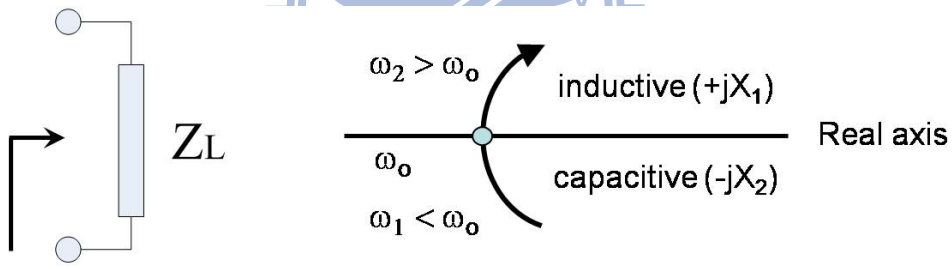
$$\omega = \omega_0 = \frac{1}{\sqrt{LC}}$$

ω_0 is the parallel resonance frequency

$for\ \omega < \omega_0 : Z_s = -jB$: inductive mode susceptance

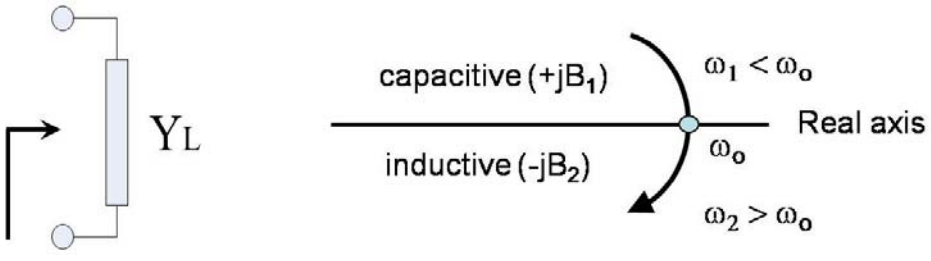
$for\ \omega > \omega_0 : Z_s = +jB$: capacitive mode susceptance

Following what has been done for series LC network, set a load Z_L illustrated in Fig. 3.8 (a) and the impedance of Z_L under varying frequencies is shown in the Z-Smith chart in Fig. 3.8 (b). It shows that Z_L is a kind of capacitive mode impedance at lower frequency $\omega_1 < \omega_0$ and becomes a inductive mode at higher frequency $\omega_2 > \omega_0$. And then, the load impedance Z_L in the Z-Smith chart was converted to a load admittance Y_L in the Y-Smith chart, as shown in Fig. 3.9.



(a) (b)

Fig. 3. 8 (a) Load impedance Z_L (b) The impedance modes of load Z_L under varying frequencies, drawn in the Z-Smith chart



(a) (b)

Fig. 3. 9 (a) Load admittance Y_L (b) The admittance modes of load Y_L under varying frequencies, drawn in the Y-Smith chart

Then, we can add a parallel LC resonance circuit to the load Y_L, as shown in Fig. 3.10.

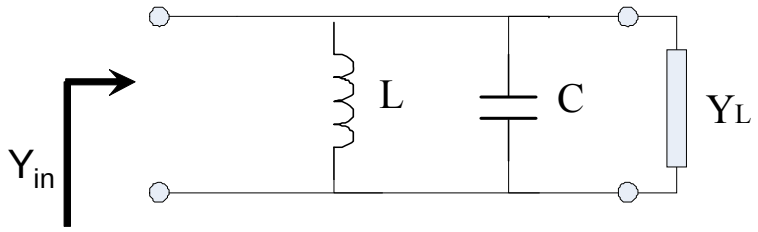


Fig. 3. 10 Add a parallel LC resonance circuit to the load

Again, the above analysis provide us a guideline to select suitable L and C to generate capacitive mode admittance (jB_1) at lower frequency and inductive mode admittance ($-jB_2$) at higher frequency. In the way, the created parallel LC network can offer the required admittance to just cancel out that of load Y_L, i.e. the capacitive mode jB_1 at lower frequency and the inductive mode $-jB_2$ at higher frequency. As a result, the equivalent admittance of the input Y_{in} can approach the real axis, shown in Fig. 3.11.

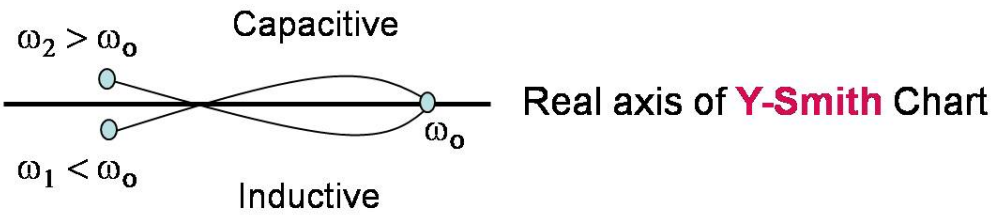


Fig. 3. 11 Effect of adding a parallel LC resonance circuit to the load in the Y-Smith chart

Based on the analysis on both series and parallel LC resonance circuits, an input matching circucit containing three-section LC networks, as shown in Fig.12 was implemented for ultra-wide band impedance matching in UWB LNA design. The first section of LC network is composed of L_g and C_{gs} appearing at the gate of MOSFET (L_s for source degeneration). As shown in Fig.13 (b), adding the first section LC network makes the S_{11} going from the lower half plane through the real axis to the upper half plane, which means an impedance shift from capacitive mode to inductive mode. Following the first series LC

network (L_g and C_{gs}), a parallel LC network consisting of L_2 and C_2 is added as the second section and the resulted S_{11} movement is shown in Fig.13(c). Finally, the third section of LC network in form of series L_1 and C_1 drives S_{11} reaching the center of Smith-chart, i.e. the targeted standard impedance 50 Ω for matching over the wide bandwidth 3.1 ~ 10.6GHz.

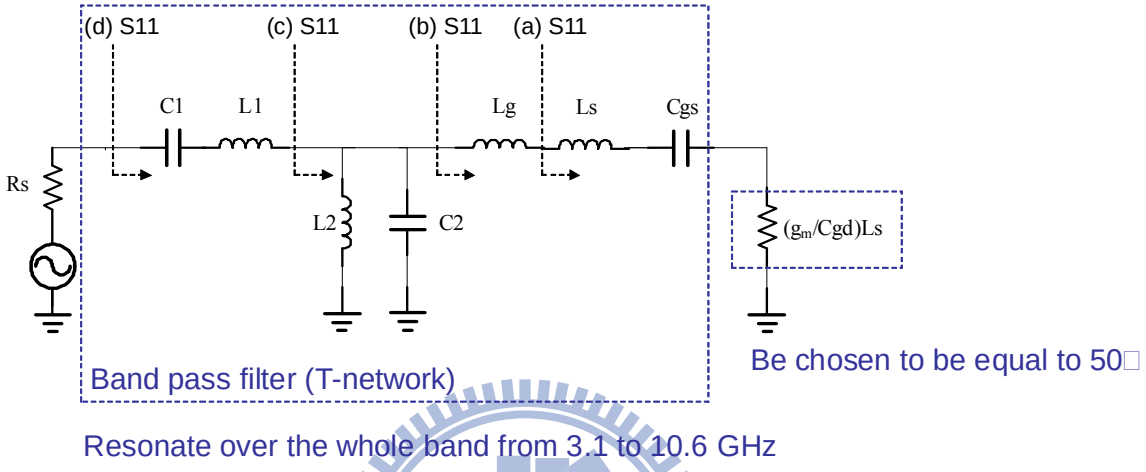


Fig. 3. 12 An input matching circuit with three-section LC networks for ultra-wide band input impedance matching

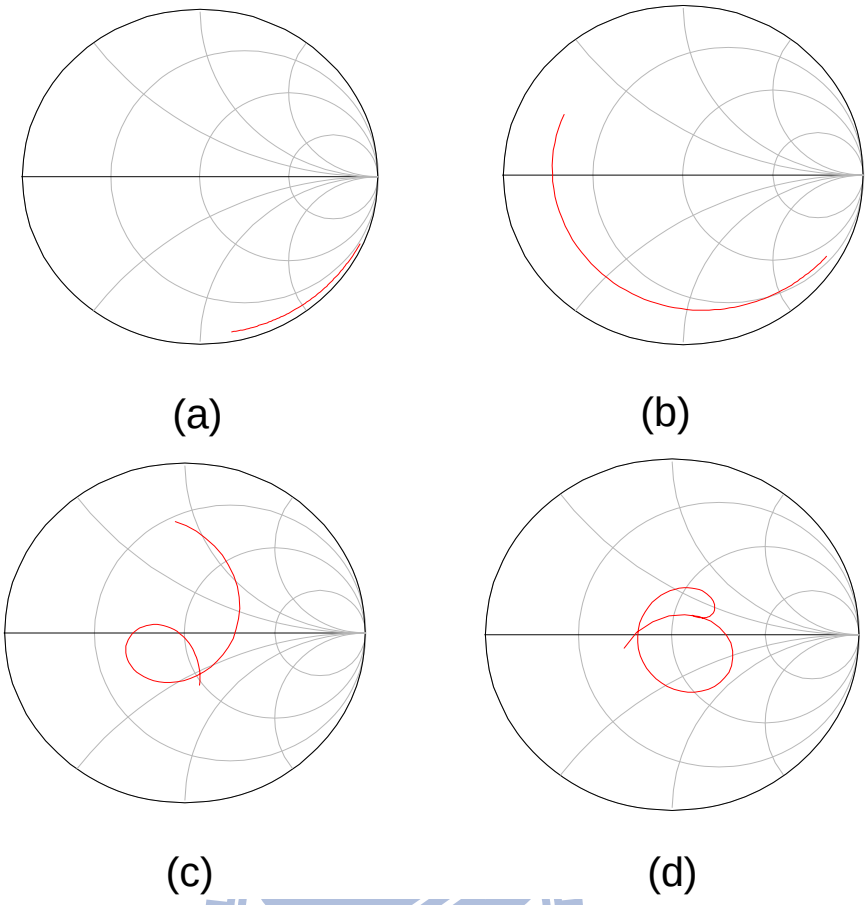


Fig. 3. 13 The input matching network effect on S_{11} (a) original nMOSFET without external LC network (b) adding the first section of LC network : L_g and C_{gs} (c) adding the second section of LC network : L_2 and C_2 (d) adding the third section of LC network :L_1 and C_1

3.3.2 Shunt Peaking Circuit and Analysis

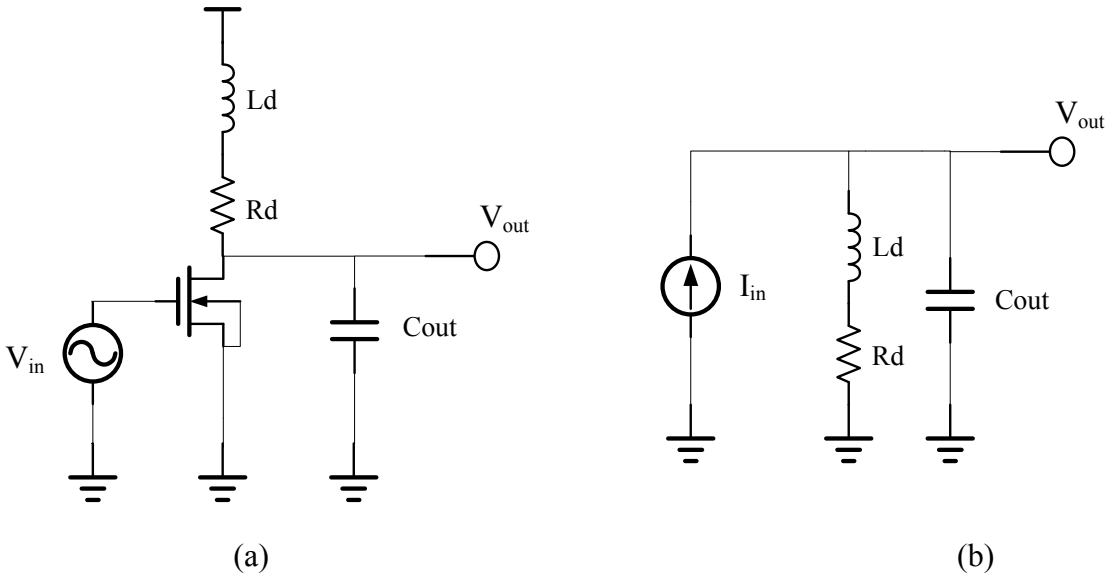


Fig. 3. 14 (a) Inductive-peaking configuration (b) Small-signal equivalent circuit

A model of shunt peaking amplifier is shown in Fig. 3.14. The capacitance C_{out} may be taken to represent all the loading on the output node, including that of a subsequent stage. The resistance R_d is the effective load resistance at that node and the inductor L_d is employed to extend the usable bandwidth. From Fig. 3.14, the transfer function H(s) without L_d is expressed in (3-3) and that with L_d is written in (3-4).

$$H(s) = g_m(R_d \,//\, \frac{1}{sC_{out}}) = g_m R_d \frac{1}{sR_d C_{out} + 1} \tag{3-3}$$

$$H(s) = g_m[(R_d + sL_d) \,//\, \frac{1}{sC_{out}}] = g_m R_d \frac{s(\frac{L_d}{R_d}) + 1}{s^2 L_d C_{out} + sR_d C_{out} + 1} \tag{3-4}$$

As shown in (3-4), the addition of an inductor L_d in series with the load resistor R_d provides an impedance component that increases with frequency, which helps offset the decreasing impedance of the capacitance, leaving net impedance that remains roughly constant over a broader frequency range than that of the original RC network. This technique, so called as shunt peaking method is suitable for broadband design. Note that L_d must be optimized in the dimensions to have large gain, and to be sufficiently small so that it can keep the resonance from L_dC_{out} out of the working band. R_d is chosen to place the zero-node frequency ($\omega_z=R_d/L_d$) as close as to the lower edge of the bandwidth to improve the power gain. Fig. 3.15 demonstrates the shunt output inductance L_d effect on the ULW LNA performance, such as power gain (S_{21}), noise figure (NF), input return loss (S_{11}), output return loss (S_{22}), calculated by ADS simulation. Note that the adoption of L_d, constituting the shunt peaking circuit can effectively improve the UWB performance with higher S_{21} and lower NF.

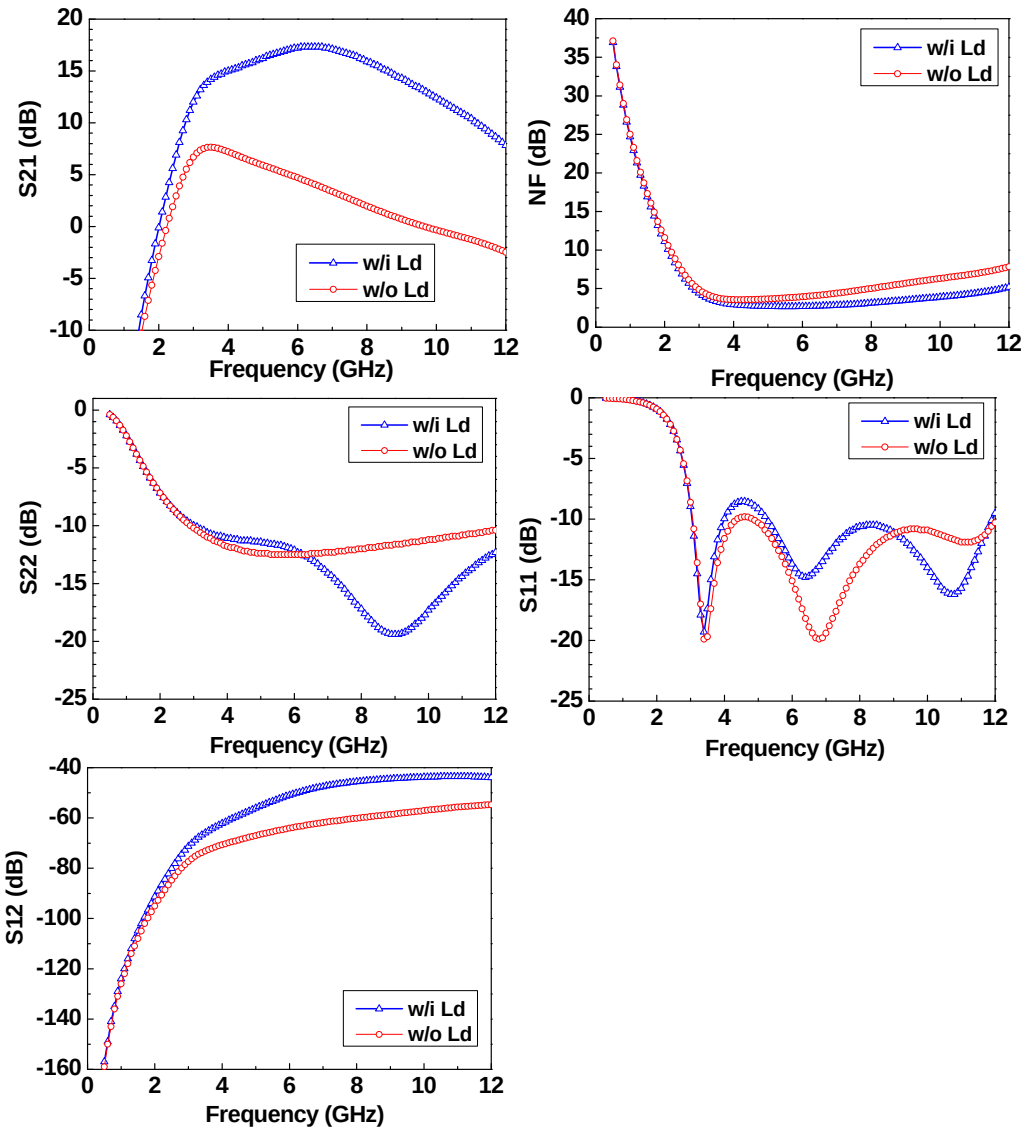


Fig. 3. 15 The output inductance L_d effect on UWB LNA performance from ADS simulation for power gain (S_{21}), noise figure (NF), input return loss (S_{11}), output return loss (S_{22}).

3.3.3 Output Matching Circuit and Analysis

For an amplifier design, output matching circuit is indispensable to drive an external load, which is generally a low impedance. Source-follower buffer illustrated in Fig. 3.16 has been widely used as a typical output matching circuit for the purpose of ensuring sufficient power gain, even with an external load of low impedance.

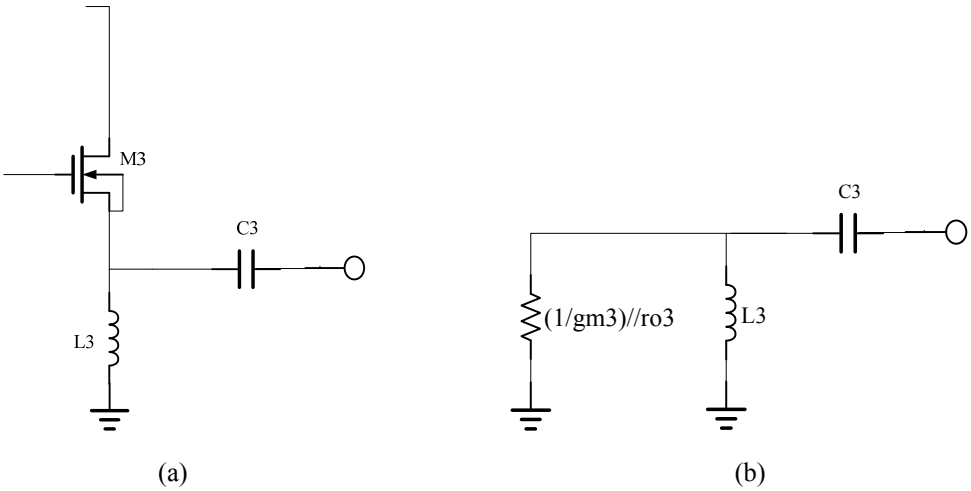


Fig. 3. 16 The output matching circuit for UWB LNA (a) the circuit schematic of a Source-follower buffer (b) the Small-signal equivalent circuit for the source-follower

In the following, an equivalent circuit analysis based on Fig. 3.16(b) was performed to derive and compare the output characteristics like the external and internal output voltages. The external output voltage V_{out}' is related to the output voltage of the amplifier by

$$\frac{V_{out}'}{V_{out}} = \frac{Z_o}{Z_o + \frac{1}{g_{m3}}} \tag{3-5}$$

where

$$Z_o = sL_3 // \frac{1}{s\left[C_{gs3}(1-\frac{1}{K})\right]} // r_{o3} \tag{3-6}$$

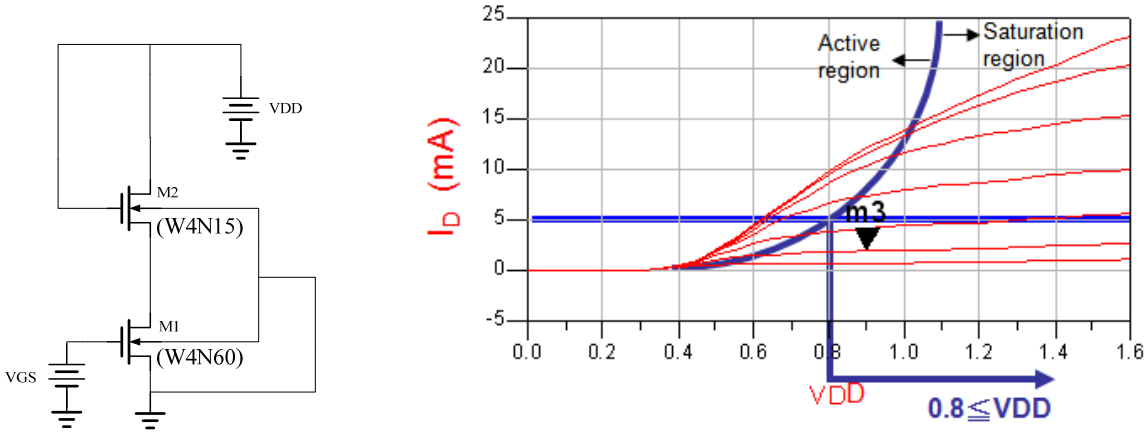
$$\frac{V_{out}'}{V_{out}} = \frac{(sL_3 // r_{o3})}{(sL_3 // r_{o3}) + \frac{1}{g_{m3}}} \triangleq K\ (low-frequency\ voltage\ gain) \tag{3-7}$$

In this work for UWB LNA implementation, the source-follower buffer is designed to improve the power gain of the amplifier at high frequency and over wide bandwidth. In order to achieve wideband output matching from 3.1 to 10.6 GHz, we made an appropriate selection on the transistor M3 dimension (width) and biasing current to achieve $(1/g_m)//r_{o3}$= 50 Ω. Furthermore, L3 and C3 were designed with a careful consideration of layout and dimensions

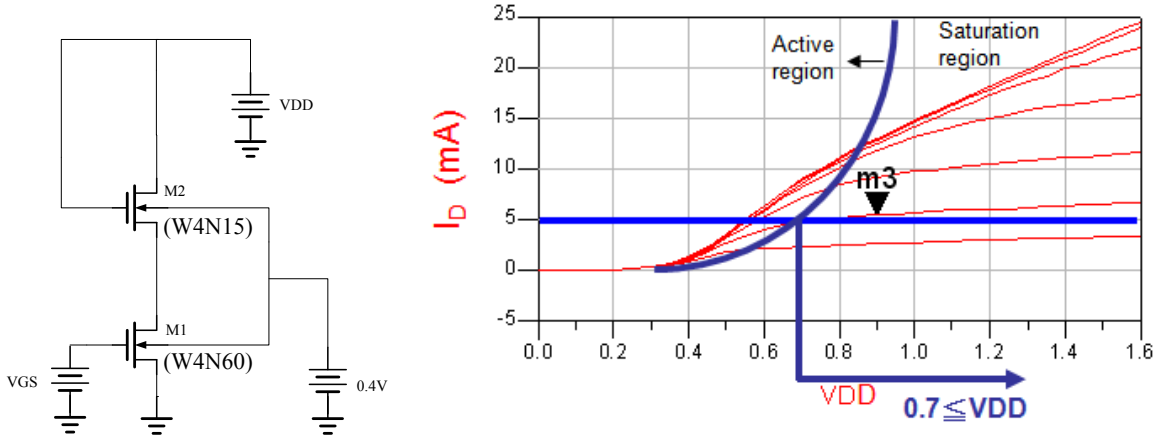
to enable an LC resonance at required high frequency. Note that the inductance L3, acts as a current source biasing the source-follower buffer, and also as a matching element for achieving high gain at the upper bound of bandwidth.

3.3.4 Forward Body Biasing Technique

The cascade topology has been widely used in amplifier design like LNA; however, the structure employing stacked transistors generally requires higher supply voltage (V_{DD}). For the stacked transistors M1 and M2 under zero body bias (V_{BS}=0V), the simulated output characteristics I_{DS} –V_{DS} shown in Fig. 3.17(a) indicates that voltage swing of 0.8V is required to make M2 operate in saturation, reaching the specified current, I_{DS} =5mA. As for the same structure operating with forward body bias (FBB), e.g. V_{BS}=0.4V applied to both M1 and M2, the I_{DS} –V_{DS} characteristics shown in Fig. 3.17(b) reveals that the required voltage swing can be reduced by 0.1V to 0.7V for the specified current in saturation region. This simulation predicts that FBB can facilitate V_{DD} scaling, attributed to lower threshold voltage (V_{th}).



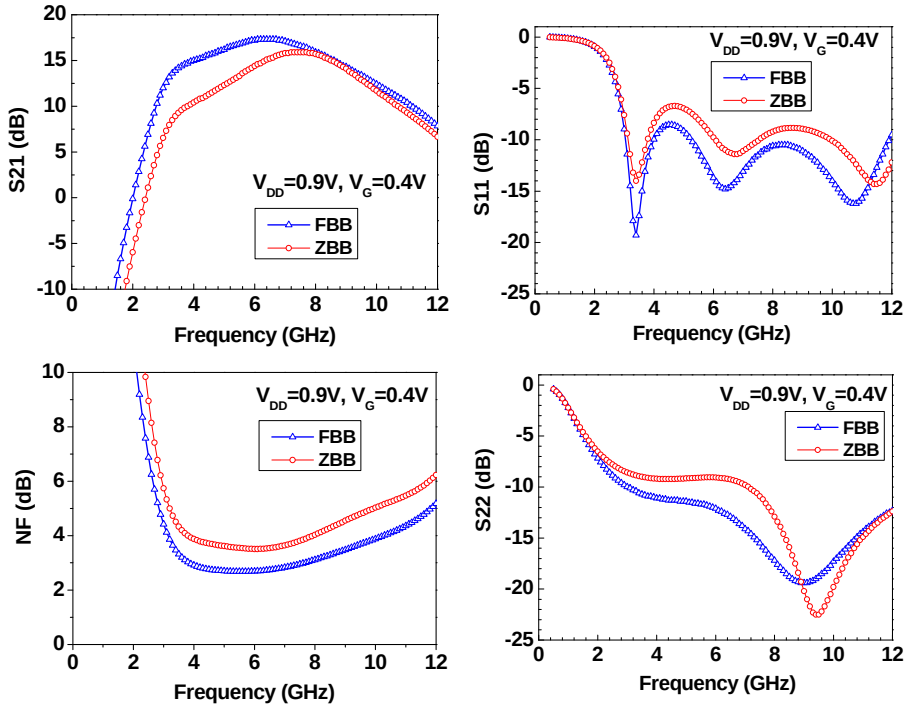
(a)



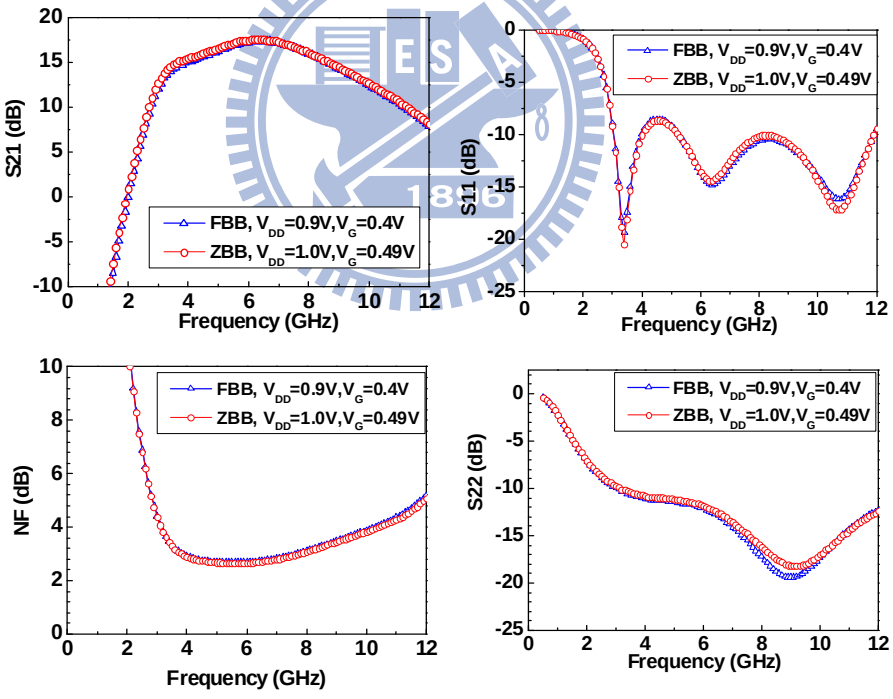
(b)

Fig. 3. 17 Simulated I_{DS} –V_{DS} characteristics for stacked transistors structure (M1 and M2), under (a) zero body bias (V_{BS}=0V) (b) forward body bias (V_{BS}=0.4V).

In the following, the FBB effect on the proposed UWB LNA performance was verified by ADS circuit simulation. Referring to circuit schematics of our UWB LNA in Fig.3.1, ZBB at V_{BS}=0V or FBB at V_{BS}=0.4V were simultaneously applied to the body node of M1 and M2 for this evaluation. First, the supply voltages to the drain and gate, such as V_{DD}=0.9V and V_G=0.4V were fixed the same for different body biases like ZBB and FBB. The simulation results shown in Fig. 3.18(a) indicate that FBB (V_{BS}=0.4V) can improve LNA performance in terms of higher power gain (S_{21}), lower noise (NF), and lower return loss in both input and output (S_{11}, S_{22}). Then, the supply voltages were increased for ZBB to verify V_{DD} and V_G required to reach the performance achieved under FBB. The simulation results shown in Fig. 3.18(b) suggest that V_{DD} increased by 0.1V to 1.0V and V_G raised by 0.09V to 0.49V can make the performance comparable with that under FBB. The results manifest the fact that FBB technique can facilitate lower power design, attributed to lower supply voltages as required. The Table 3.1 summarizes the performance under FBB and ZBB for a comparison. Note that FBB can help reduce the supply voltage V_{DD} from 1.0V (for ZBB) to 0.9V and reduce DC power consumption by 2.8 mW, from 11.1 mW (for ZBB) to 8.3 mW, that is around 34% power saving for keeping all other performance parameters the same.



(a)



(b)

Fig. 3. 18 UWB LNA performance : power gain (S_{21}), lower noise (NF), input return loss (S_{11}), and output return loss (S_{22}) from ADS simulation (a) V_{DD}=0.9V, V_G=0.4V fixed for ZBB (V_{BS}=0) and FBB (V_{BS}=0.4) (b) V_{DD}=0.9V, V_G=0.4V FBB (V_{BS}=0.4), V_{DD}=1.0V, V_G=0.45V for ZBB (V_{BS}=0).

Table 3. 1 UWB LNA performance and supply voltages V_{DD} comparison from ADS simulation, under zero body bias (ZBB) and forward body bias (FBB)

RF Corner	Unit	TT_forward body	TT_zero body
Frequency	GHz	3.1 ~ 10.6	3.1 ~ 10.6
Power (only core LNA)	mW	4.7	6.9
Power (total)	mW	8.3	11.1
Supply Volatge (V_{DD})	V	0.9	1.0
Bias current (only core LNA)	mA	5.23	6.85
Bias current (total)	mA	9.18	11.10
Gain(S_{21})max / Gain(S_{21})min	dB	17.3/11.2	17.5/11.4
NF - min / max	dB	2.7/4.1	2.7/4.1
Input Return Loss (S_{11})	dB	< -8.6	< -8.6
Output Return Loss (S_{22})	dB	< -10.1	< -10.1
IIP3	dBm	-10@4G,-11@10G	-9.75@4G,-11.36@10G
Reverse isolation (S_{12})	dB	< -43.6	< -42.5
Chip size	mm^2	0.637 x 0.892	0.637 x 0.892
FOM(Figure of Merit)	W^{-1}	53.7	40.7
FOM/Size	$(W^{-1})/(mm^2)$	94.4	71.6

3.3.5 Gain Analysis

In the following, a complete circuit schematic incorporating input matching, amplifying stage, and output buffer, for the UWB LNA is illustrated in Fig. 3.19.

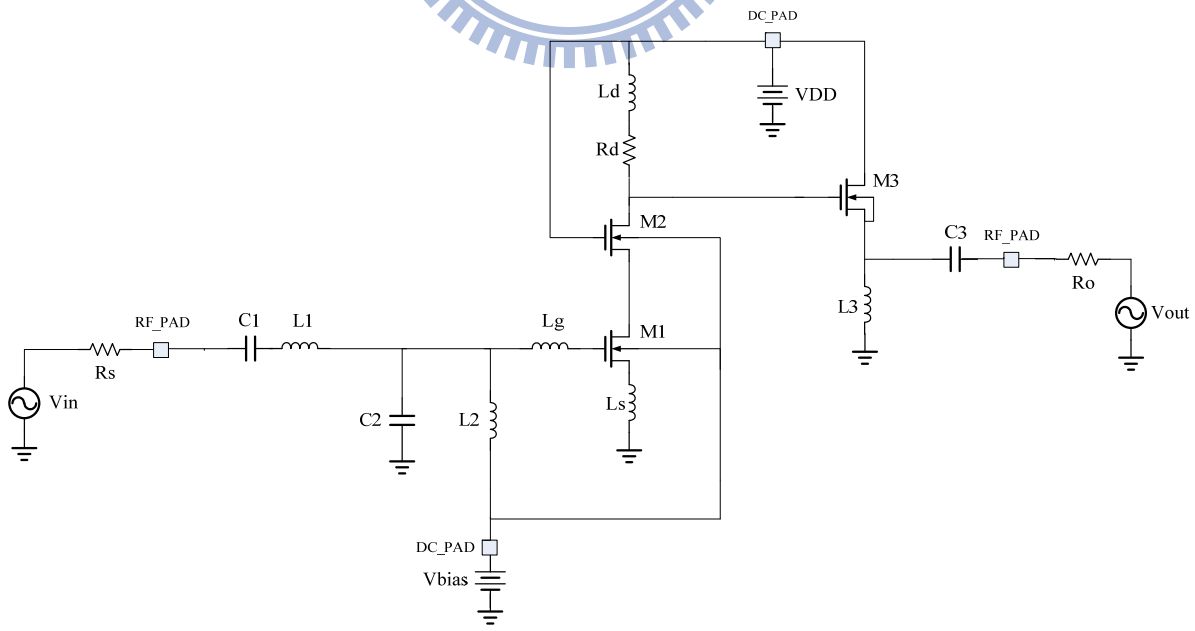


Fig. 3. 19 A complete circuit schematic of the UWB LNA

At high frequency, the MOS transistor acts as a current amplifier. The current gain is

$\beta(s) = g_m / sC_{gs}$, and the current into M1 is $V_{in} \cdot W(s) / R_s$, where W(s) is the Chebyshev filter transfer function. Note that |W(s)| in band is approximately unity and that out of band tends to be zero. The impedance looking into the amplifier is therefore equal to R_s when operating in band, and it becomes very high when working out of band. Therefore, the voltage gain can be derived as

$$\frac{I}{V_{in}} \cdot \frac{V_{out}}{I} \cdot \frac{V_{out}'}{V_{out}} = \frac{W(s)}{R_s} \frac{1}{sC_{gs}} (-g_m) \cdot R_d \frac{s(\frac{L_d}{R_d}) + 1}{s^2 L_d C_{out} + sR_d C_{out} + 1} \cdot \frac{Z_o g_{m3}}{Z_o g_{m3} + 1} \cdot \frac{R_o sC_3}{R_o sC_3 + 1} \quad (3\text{-}8)$$

where

$$\frac{V_{out}'}{V_{out}} = \frac{(sL_3 // r_{o3})}{(sL_3 // r_{o3}) + \frac{1}{g_{m3}}} \triangleq K \quad (3\text{-}9)$$

$$Z_o = sL_3 // \frac{1}{s\left[C_{gs3}(1 - \frac{1}{K})\right]} // r_{o3} // (\frac{1}{sC_3 + R_o}) \quad (3\text{-}10)$$

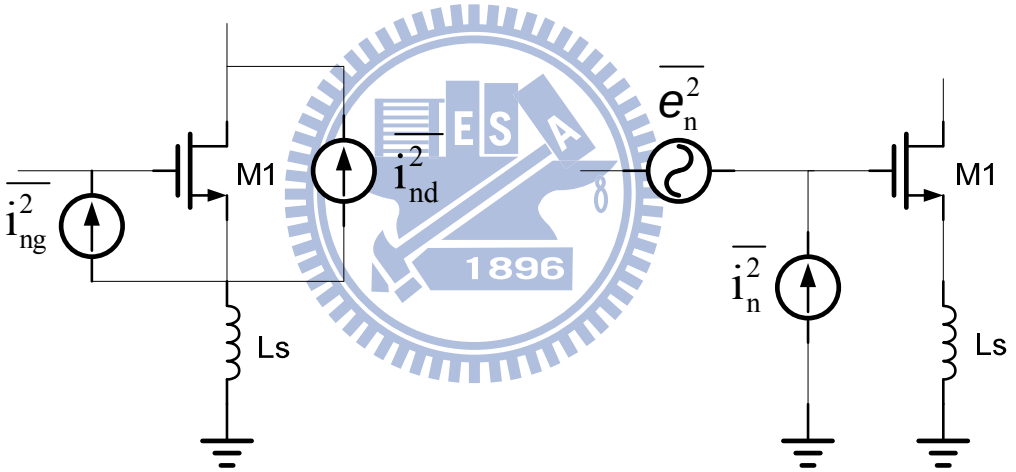
$$C_{out} = C_{db2} + C_{gd3} + C_{dg2} + C_{gs3}(1 - K) \quad (3\text{-}11)$$

C_{out} is the total capacitance between the drain of M2 and ground, where C_{db2} is the drain-bulk capacitance of M2, C_{gd3} is the gate-drain capacitance of M3, C_{dg2} is the drain-gate capacitance of M2 and C_{gs3} is the gate-source capacitance of M3.

3.3.6 Noise Analysis [5]

The noise performance of the proposed topology is determined by two main contributors [5], such as the losses of the input network and the noise of M1 in the cascade amplifier. The noise introduced from the input network is due to the limited quality factor (Q) of the inductors integrated on bulk Si chip. To overcome this penalty, extensive research works have been carried out to improve Q of on-Si-chip inductor. The higher Q realized in an inductor can help reduce the noise but may trade off with wideband performance. Regarding the thermal

noise contributed from the transistor M1, layout optimization is generally done using multi-finger structure. For a fixed total width (W_{tot}), the smaller unit finger width (W_F) and larger finger number (N) can help reduce gate resistance R_g and then suppress thermal noise, i.e. the lower NF. Again, a trade-off between the power and noise has to be considered in determining transistor dimension. The larger W_{tot} (W_F*N) can reduce noise resistance R_n, attributed to larger g_m; however, the associated higher current leads to higher power consumption. Fig. 3.20(a) presents a conventionally used thermal noise model for MOSFET, in which drain current noise ($S_{id} = \overline{i_{nd}^2} / \Delta f$) and induced gate noise ($S_{ig} = \overline{i_{ng}^2} / \Delta f$) are two primary noise sources. Fig.3.20(b) indicates an equivalent model for input referred noise generator with two correlated noise sources.



(a) (b)

Fig. 3. 20 Noise model for the amplifying transistor M1. (a) noise sources from drain and gate (b) Input-referred equivalent noise generators.

In the following, noise model equations are derived for MOSFETs based on Fig. 3.20 [5]

$$i_n = i_{ng} + \frac{j\omega C_{gs}}{g_m} i_{nd} \tag{3-12}$$

$$e_n = j\omega L_s i_{ng} + (1 - \omega^2 L_s C_{gs}) \frac{i_{nd}}{g_m} = j\omega L_s i_n + \frac{i_{nd}}{g_m} \tag{3-13}$$

where i_{nd} is the drain noise current, while i_{ng} is the induced gate noise.

The power spectral density of drain current noise and induced gate noise are expressed in (3-14) and (3-15), respectively

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{3-14}$$

$$\overline{i_{ng}^2} = 4kT\delta\frac{\omega^2 C_{gs}^2}{5g_{d0}}\Delta f \tag{3-15}$$

where $\delta \approx 1.33-4$, and $\gamma \approx 0.67-1.33$ are excess noise parameters [40], and g_{d0} is the channel conductance at $V_{DS}=0$.

$$\begin{aligned} Z_c &= \frac{\overline{e_n i_n^*}}{\overline{i_n^2}} = j\omega L_s - j\frac{(|c|\alpha\chi+1)}{\omega C_{gs}(\alpha^2\chi^2+2|c|\alpha\chi+1)} \\ Z_c &= R_c + jX_c \\ R_c &= 0 \Rightarrow Z_c = jX_c \\ X_c &= \omega L_s - \frac{(|c|\alpha\chi+1)}{\omega C_{gs}(\alpha^2\chi^2+2|c|\alpha\chi+1)} \end{aligned} \tag{3-16}$$

where

$$\overline{i_n^2} = 4kT\frac{\gamma}{\alpha^2 g_{d0}}\omega^2 C_{gs}^2(\alpha^2\chi^2+2|c|\alpha\chi+1)\Delta f \tag{3-17}$$

$$\overline{e_n i_n^*} = 4kT\frac{\gamma}{\alpha^2 g_{d0}}\omega C_{gs}(-j)[-\omega^2 L_s C_{gs}(\alpha^2\chi^2+2|c|\alpha\chi+1)+(|c|\alpha\chi+1)]\Delta f \tag{3-18}$$

$$\sqrt{\overline{i_{ng}^2}}\sqrt{\overline{i_{nd}^2}} = 4kT\omega C_{gs}\sqrt{\frac{\delta\gamma}{5}}\Delta f \tag{3-19}$$

$$\chi = \sqrt{\frac{\delta}{5\gamma}} \tag{3-20}$$

$$\alpha = \frac{g_m}{g_{d0}} \tag{3-21}$$

$$c = \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}}\sqrt{\overline{i_{nd}^2}}} \tag{3-22}$$

The two uncorrelated noise source, e_{nu} and i_n are described by means of two parameters such as G_u and R_u written in (3-23) and (3-24), respectively:

$$G_n = \frac{\overline{i_n^2}}{4kT\Delta f} = \frac{\gamma}{\alpha^2 g_{d0}} \omega^2 C_{gs}^2 (\alpha^2 \chi^2 + 2|c|\alpha\chi + 1) \tag{3-23}$$

$$R_u = \frac{\overline{e_{nu}^2}}{4kT\Delta f} = \frac{\gamma}{\alpha^2 g_{d0}} \frac{\alpha^2 \chi^2 (1 - |c|^2)}{(\alpha^2 \chi^2 + 2|c|\alpha\chi + 1)} \tag{3-24}$$

By using the introduced parameters, the noise factor F can be expressed by

$$F = 1 + \frac{R_u + |Z_c + Z_s|^2 G_n}{R_s} = 1 + \frac{R_u + \left[(R_c + R_s)^2 + (X_c + X_s)^2 \right] G_n}{R_s} \tag{3-25}$$

where $Z_s = R_s + jX_s$ is the source impedance.

According to noise optimization theory [3, 29], the minimum noise figure (NF_{min}) is achieved if the source impedance $Z_s = Z_{opt} = R_{opt} + jX_{opt}$ is chosen such that

$$R_{opt} = \sqrt{\frac{R_u}{G_n} + R_c^2} = \sqrt{\frac{R_u}{G_n}} = \frac{\alpha\chi\sqrt{1 - |c|^2}}{\omega C_{gs}(\alpha^2 \chi^2 + 2|c|\alpha\chi + 1)} \tag{3-26}$$

where, in this case $R_c = 0$, and

$$X_{opt} = -X_c \tag{3-27}$$

(3-16) and (3-27) show that the optimum source impedance X_{opt} is roughly the one that resonates the series combination of C_{gs} and L_s. As a consequence, nearly minimum NF can be achieved over the entire bandwidth by using the proposed input matching network, which produces X_{opt} over the required wide bandwidth. As a result of the foregoing discussion, the noise factor (F) of the LNA is

$$F(\omega) \approx 1 + \frac{R_u}{R_s} + G_n R_s = 1 + \frac{p(\omega)}{g_m R_s} \frac{\gamma}{\alpha} \tag{3-28}$$

where

$$p(\omega) = \frac{\alpha^2 \chi^2 (1 - |c|^2)}{(\alpha^2 \chi^2 + 2|c|\alpha\chi + 1)} + \omega^2 C_{gs}^2 R_s^2 (\alpha^2 \chi^2 + 2|c|\alpha\chi + 1) \quad (3\text{-}29)$$

(3-28) and (3-29) show that increasing the transconductance g_m or reducing C_{gs} can improve the noise performance, with all of the other parameters being the same.

The noise factor (F) described by (3-28) depends on three of the following four quantities: the drain current I_D, the over-drive voltage V_{od}, the transistor width W, and the frequency. In order to perform an optimization over the entire band of interest, we consider the average noise figure (NF). Thus, we reduce the number of independent variables by one. Fig. 3.21 shows the contour plots of the average NF as a function of I_D and W. For each value of the bias current, the device width can be chosen to minimize the NF.

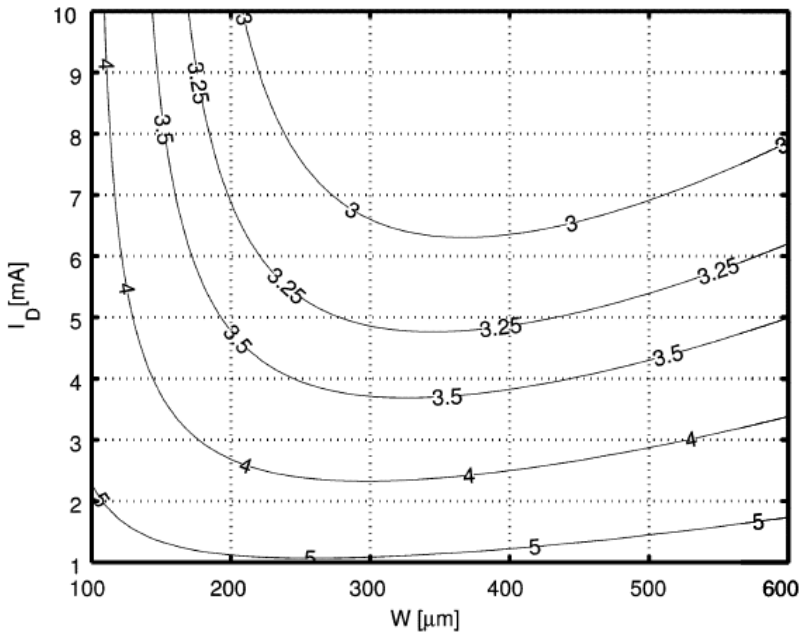


Fig. 3. 21 Contour plots of the average NF [5]

In order to minimize the average NF, the larger drain current I_D has the better NF performance, but it consumes more power. Therefore, under a specified power consumption, decreasing the supply voltage and increasing the current can improve NF performance.

Therefore, the supply voltage in this design is set a low voltage of 0.9V. In particular, for $I_D = 5mA$, the best noise performance is achieved in the region $200\mu m < W < 400\mu m$. Note that Fig. 3.21 only refer to the noise contribution of M1. In a real circuit like LNA, additional noise besides that of transistors may come from the following sources.

1. the losses of the input network, i.e., the limited quality factor of the integrated inductors;
2. the cascode device (M2) noise contribution, particularly significant at higher frequencies;
3. the load resistance (Rd) noise contribution;
4. the output buffer (M3) noise contribution.

Due to the mentioned fact, the measured NF is generally worse than what is calculated for the MOSFETs themselves.

3.4 Chip Circuit Design and Simulation

TSMC 0.13μm 1.2V RF CMOS process [41] was employed for this UWB LNA circuit simulation and design. This RF SPICE model includes passive elements such as resistors, inductors, capacitors, and RF MOSFETs as the major active devices. Also, on-chip circuit layout will be introduced.

3.4.1 Model for Circuit Simulation

In mixed signal and RF circuit design, an accurate and scalable model is strongly demanded to assure circuit simulation accuracy and facilitate the success of circuit design. For active devices, the intrinsic MOSFET model suitable for logic circuit simulation is no longer valid for RF circuit design. Parasitic and coupling effects from interconnection, substrate, and pads should be considered and taken into the model. As for passive devices, such as inductors, capacitors, and resistors, substrate lossy and conductor loss become important effects required for accurate modeling.

3.4.2 RF Circuit Simulation for UWB LNA Design

The whole circuit schematics for the proposed UWB LNA is illustrated in Fig. 3.22 in which three major blocks such as input matching network, amplifying stage (cascode), and output buffer are included and the layout dimensions for active transistors and parasitic elements (R, L, C) are remarked for simulation. Note that all the components in this design, including spiral inductors, metal-insulator-metal (MIM) capacitors and resistors, are realized on chip. Fig. 3.23 depicts the chip layout of the proposed UWB LNA. The chip area occupied by the core circuits of LNA and probing pads in peripheral region is 0.637x0.892 mm^2. The details of circuit topology analysis and operation principles have been introduced in sections 3.2~3.3. The proposed UWB LNA is simulated with Agilent ADS simulator using TSMC 0.13μm mixed-signal 1.2/2.5V RF CMOS Model. In the following, the simulation results will be presented, including pre-layout and post-layout under typical (TT) and corner conditions (FF, SS). For this UWB LNA design, the key performance parameters, such as power gain (S_{21}), input return loss (S_{11}), output return loss (S_{22}), reverse isolation (S_{12}), noise figure (NF), stability, and third-order intercept point (IIP3) have been calculated by ADS simulation. Fig. 3.24 ~ 28 show pre-layout simulation results, under the typical condition of V_{DD}=0.9V, V_G=0.4V, and a wide range of frequencies in 2~11 GHz. Note that the third-order intercept point (IIP3) shown in Fig. 3.28 is determined by two-tone test with tone space of 10MHz, and fundamental frequency at 4GHz and 10GHz. Fig. 3.29 ~ 33 indicate the pre-layout simulation for mentioned performance parameters, with a comparison under typical (TT) and corner conditions (FF, SS). The comparison is summarized in Table 3.2. As for the differences from post-layout, Fig. 3.34 ~ 38 present a comparison for all of the performance parameters, between pre-layout and post-layout simulation. Fig. 3.39 shows the Post-simulated stability. Fig. 3.40 shows the Post-simulated IIP3 at 4 GHz and 10 GHz. Table 3.3 shows the post-simulation results summary of typical and corner case. The performance of the proposed

UWB LNA is summarized in Table 3.4.

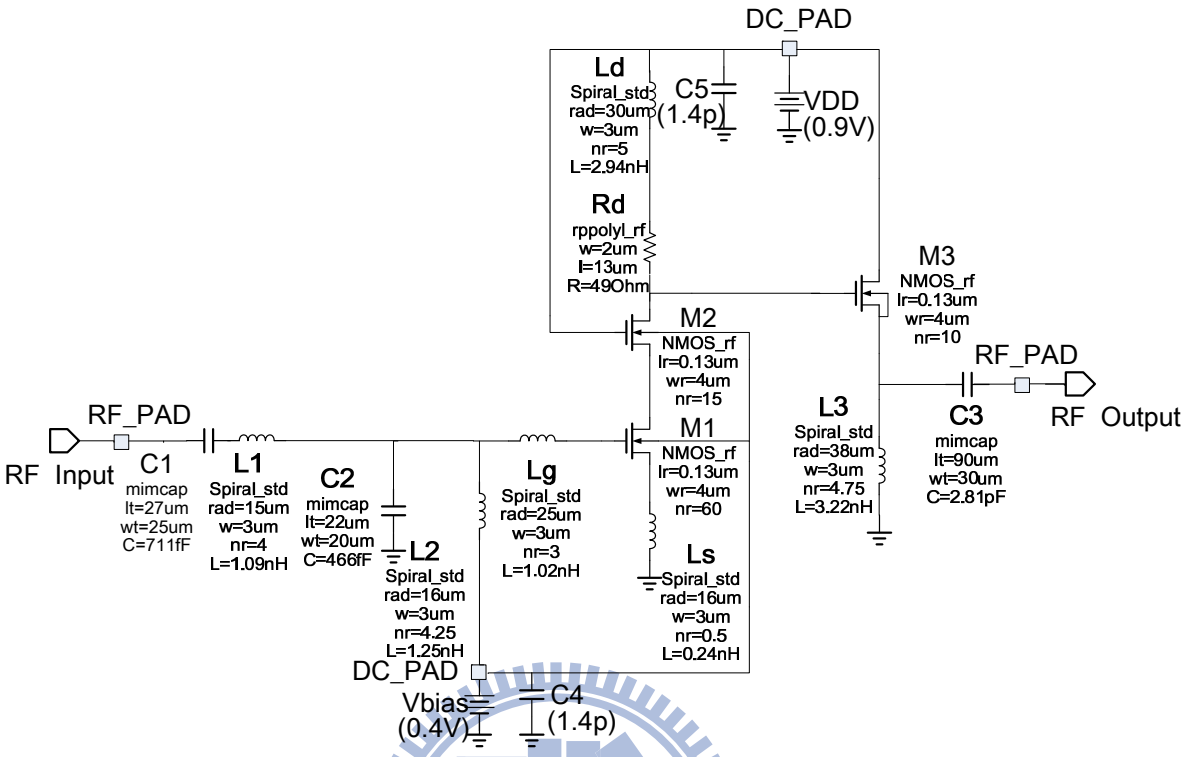


Fig. 3. 22 Circuit schematic of the UWB LNA with three core circuit blocks in which the active and passive devices dimensions are provided

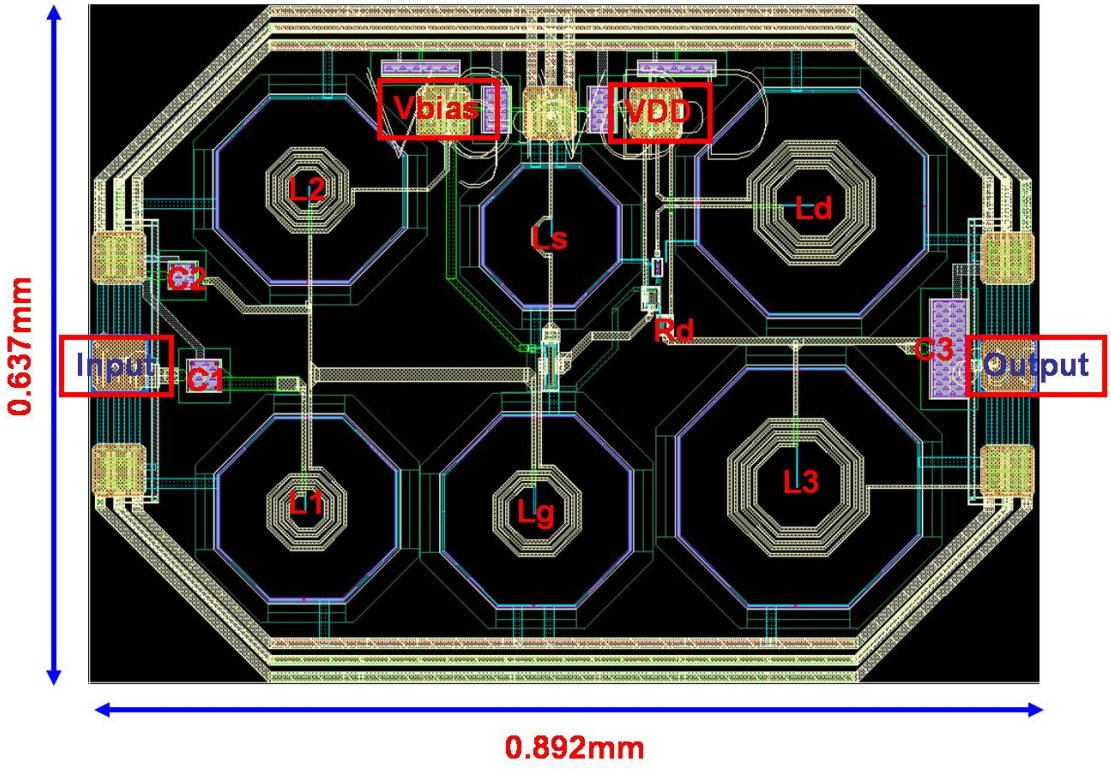


Fig. 3. 23 Chip layout of the UWB LNA

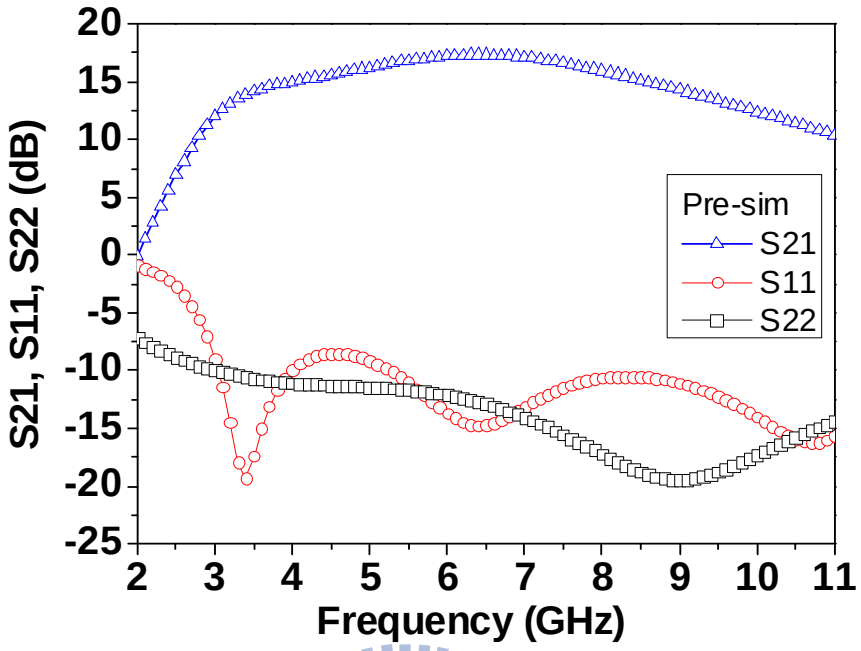


Fig. 3. 24 Pre-layout simulation for power gain (S_{21}), input return loss (S_{11}), output return loss (S_{22}). V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz.

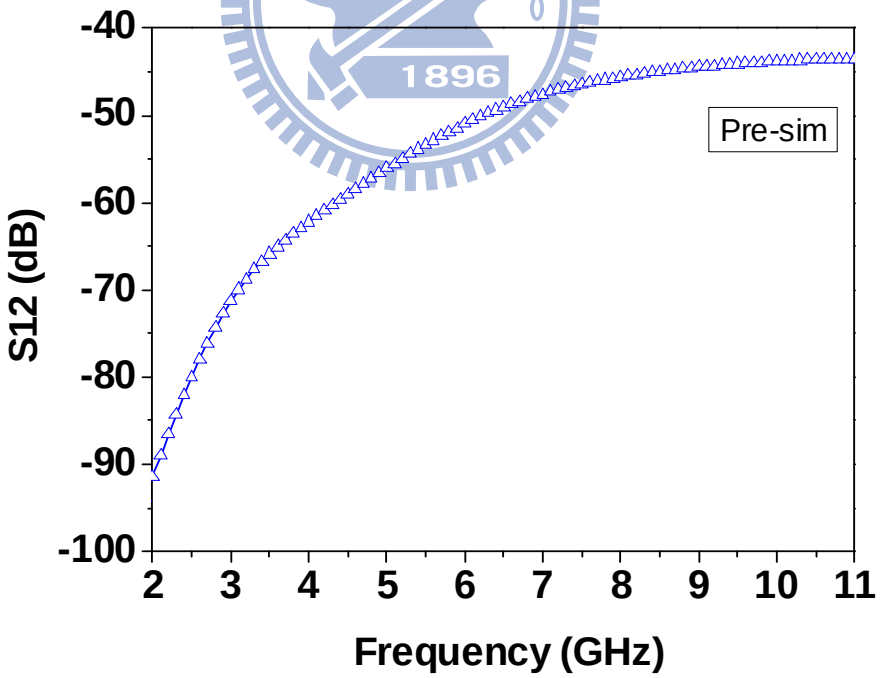


Fig. 3. 25 Pre-layout simulation for reverse isolation (S_{12}) V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz.

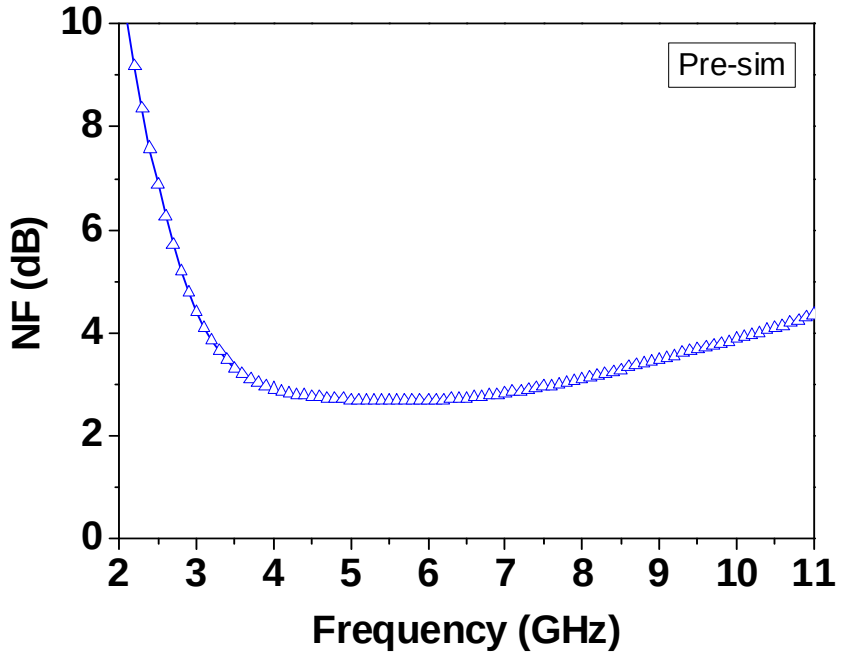


Fig. 3. 26 Pre-layout simulation for noise figure (NF). V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz.

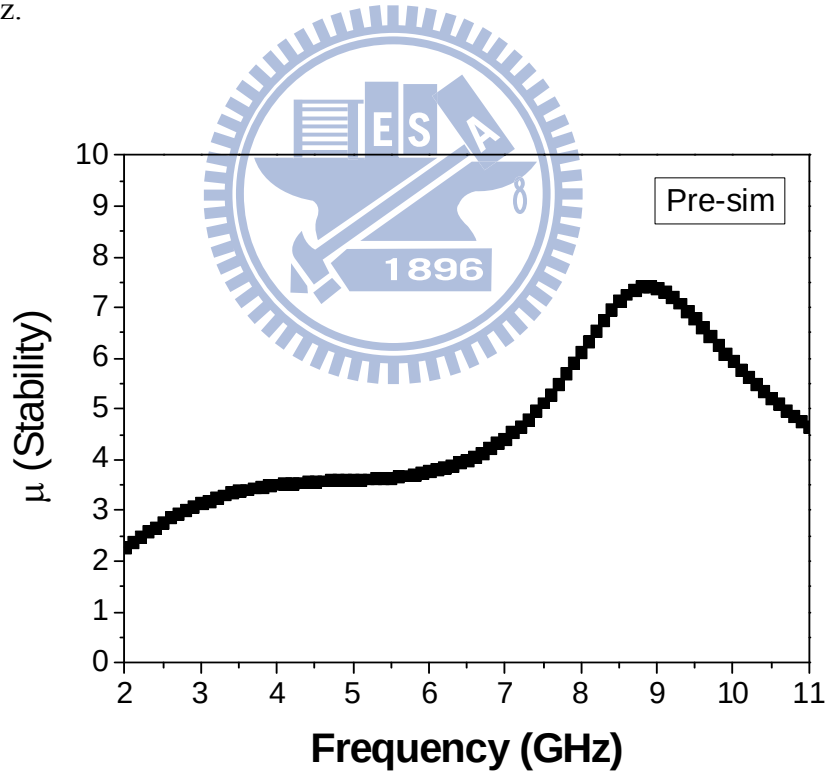
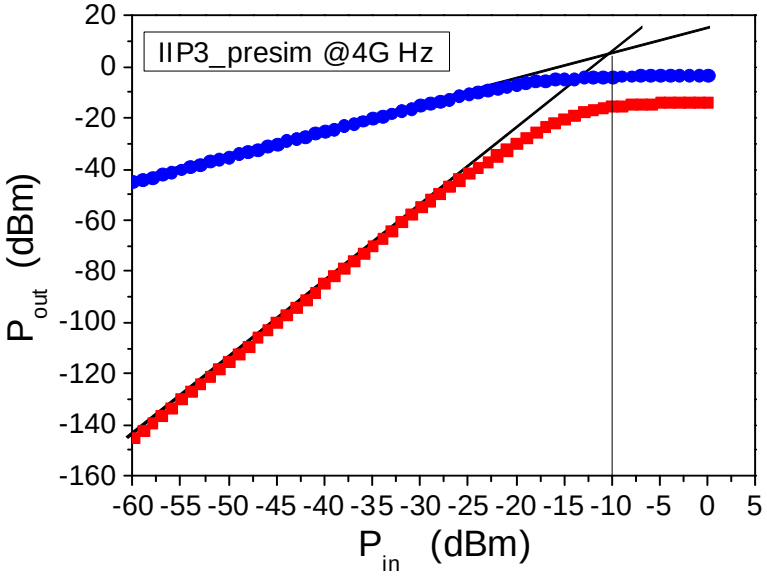
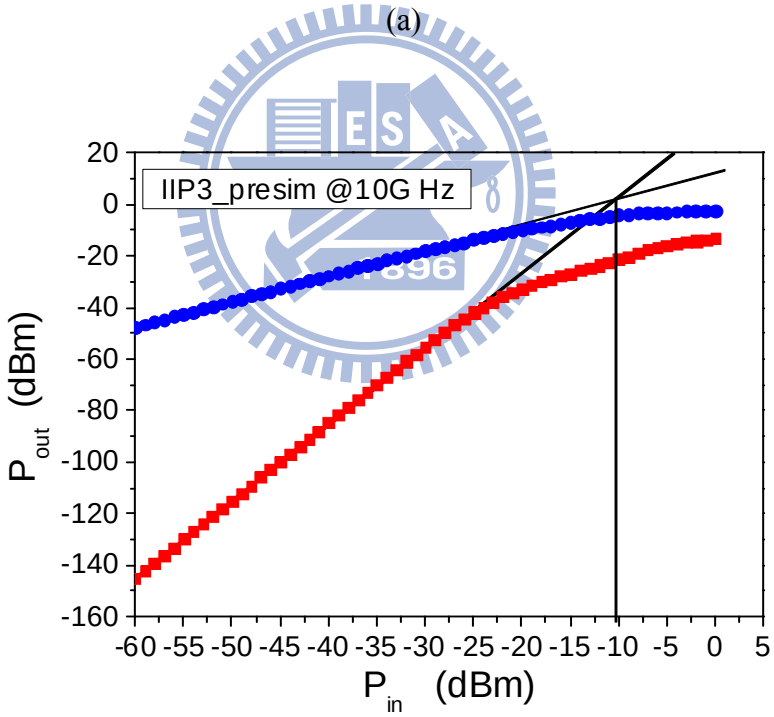


Fig. 3. 27 Pre-layout simulation for stability. V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz.



(a)



(b)

Fig. 3. 28 Pre-layout simulation for third-order intercept point (IIP3) (a) 4GHz : IIP3 =-10dBm (b) 10GHz IIP3=-11dBm. Two-tone test with tone spacing of 1MHz. V_{DD}=0.9V, V_G=0.4V.

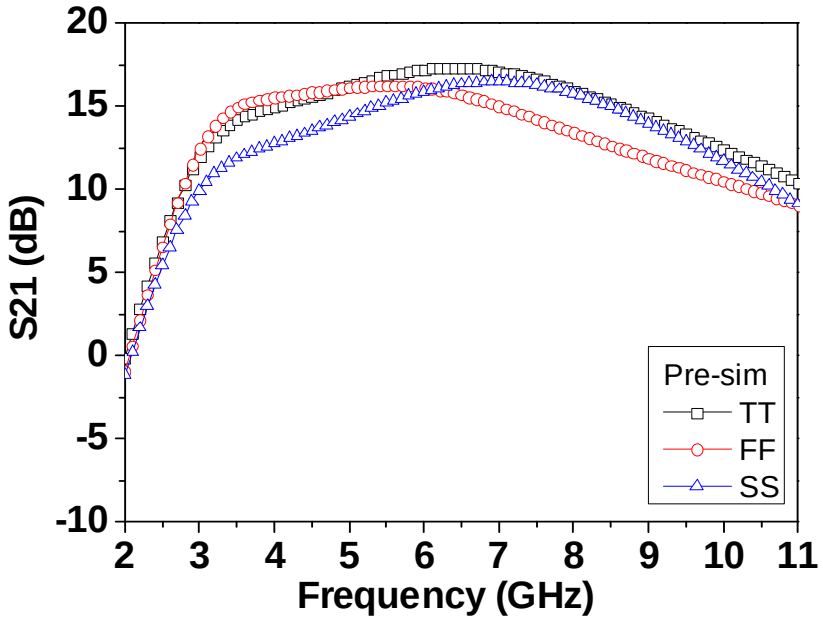


Fig. 3. 29 Pre-layout simulation for power gain (S_{21}), under typical (TT) and corner conditions (FF, SS). TT : V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz.

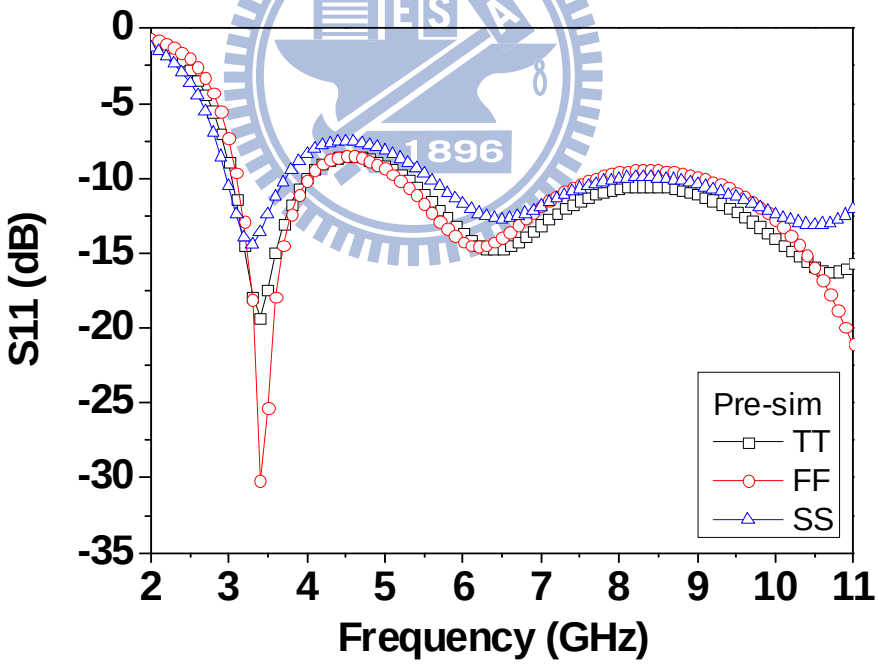


Fig. 3. 30 Pre-layout simulation for input return loss (S_{11}), under typical (TT) and corner conditions (FF, SS). TT : V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz

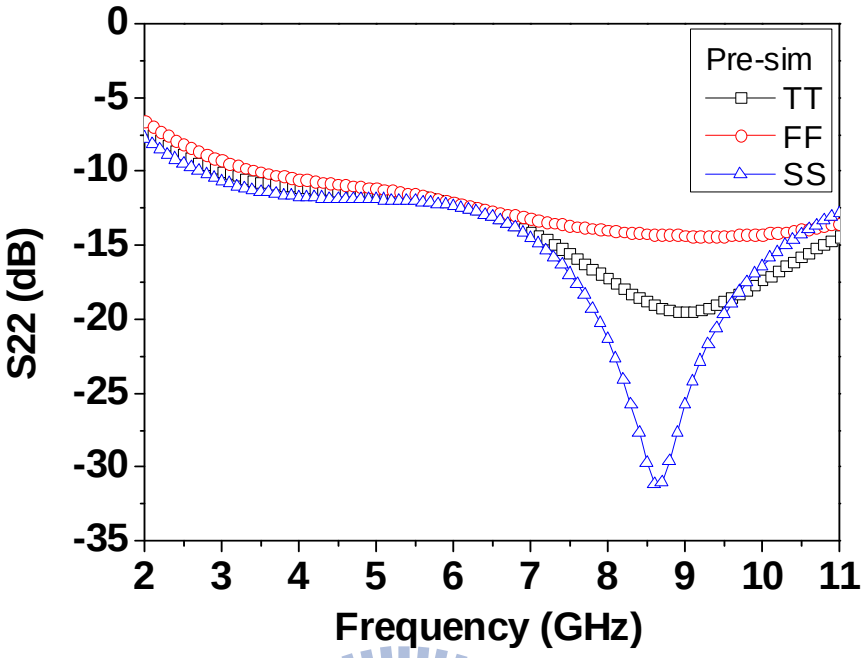


Fig. 3. 31 Pre-layout simulation for output return loss (S_{22}), under typical (TT) and corner conditions (FF, SS). TT : V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz

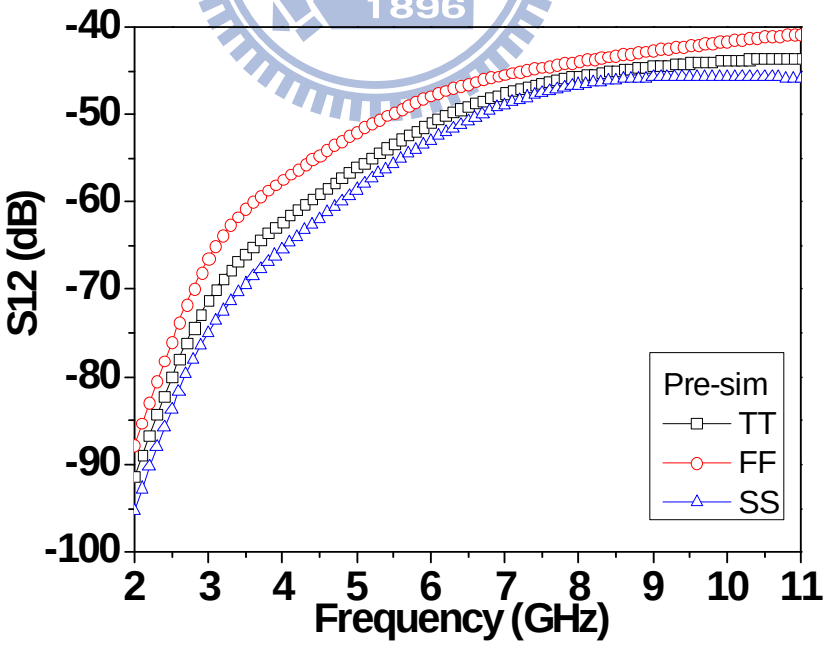


Fig. 3. 32 Pre-layout simulation for reverse isolation (S_{12}), under typical (TT) and corner conditions (FF, SS). TT : V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz

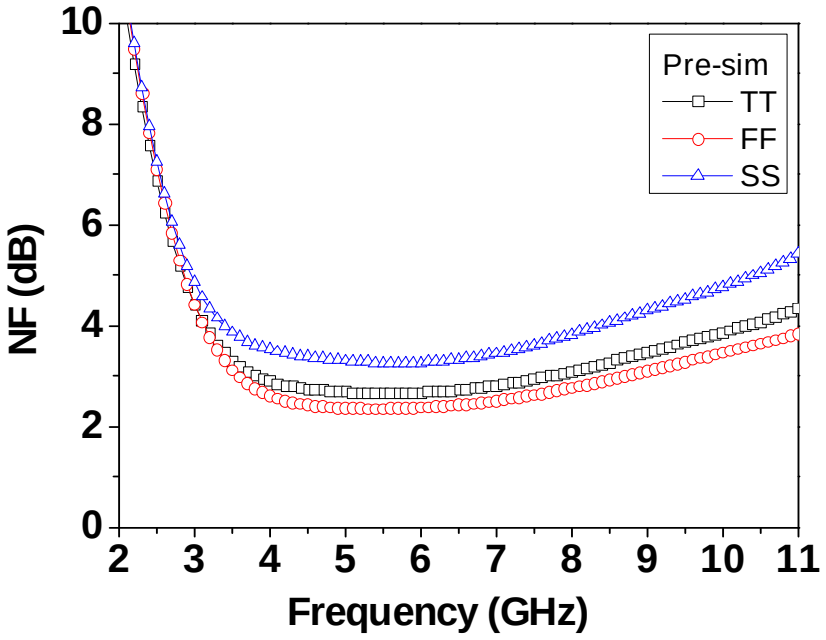


Fig. 3. 33 Pre-layout simulation for noise figure (NF), under typical (TT) and corner conditions (FF, SS). TT : V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz.

Table 3. 2 Pre-layout simulation results, under typical and corner conditions

Pre-layout simulation

RF Corner	Unit	TT	FF	SS
Frequency	GHz	3.1 ~ 10.6	3.1 ~ 10.6	3.1 ~ 10.6
Power (only core LNA)	mW	4.7	7.9	2.5
Power (total)	mW	8.3	11.1	6.6
Supply Volatge (V_{DD})	V	0.9	0.9	0.9
Bias current (only core LNA)	mA	5.23	8.75	2.80
Bias current (total)	mA	9.18	12.30	7.36
Gain(S_{21})max / Gain(S_{21})min	dB	17.3 / 11.2	16.3 / 9.6	16.5 / 10.2
NF - min / max	dB	2.7 / 4.1	2.4 / 4.0	3.3 / 5.1
Input Return Loss (S_{11})	dB	< -8.6	< -8.5	< -7.6
Output Return Loss (S_{22})	dB	< -10.1	< -9.4	< -10.8
IIP3	dBm	-10@4GHz,-11@10GHz	-11@4GHz,-11@10GHz	-7@4GHz,-6@10GHz
Reverse isolation (S_{12})	dB	< -43.6	< -41.1	< -45.8

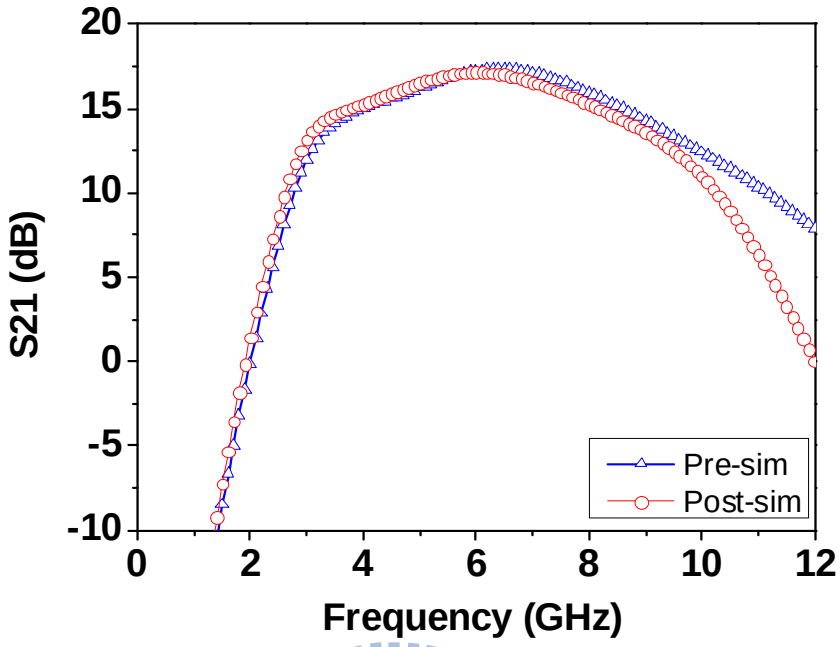


Fig. 3. 34 Comparison between pre-layout and post-layout simulation results for the power gain(S_{21}). V_{DD}=0.9V, V_G=0.4V, frequency=2~11 GHz.

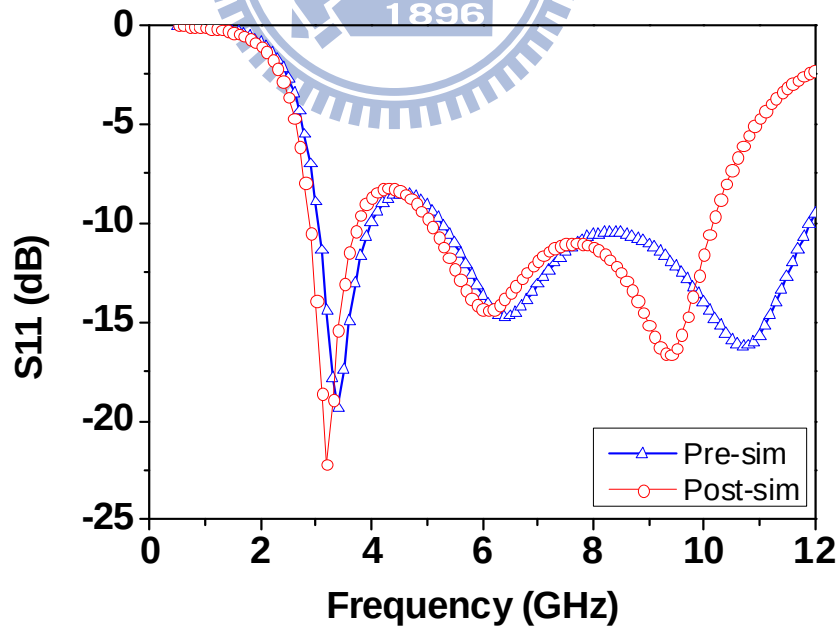


Fig. 3. 35 Comparison between pre-layout and post-layout simulation results for the input return loss (S_{11}). V_{DD}=0.9V, V_G=0.4V, frequency=0.5~12 GHz.

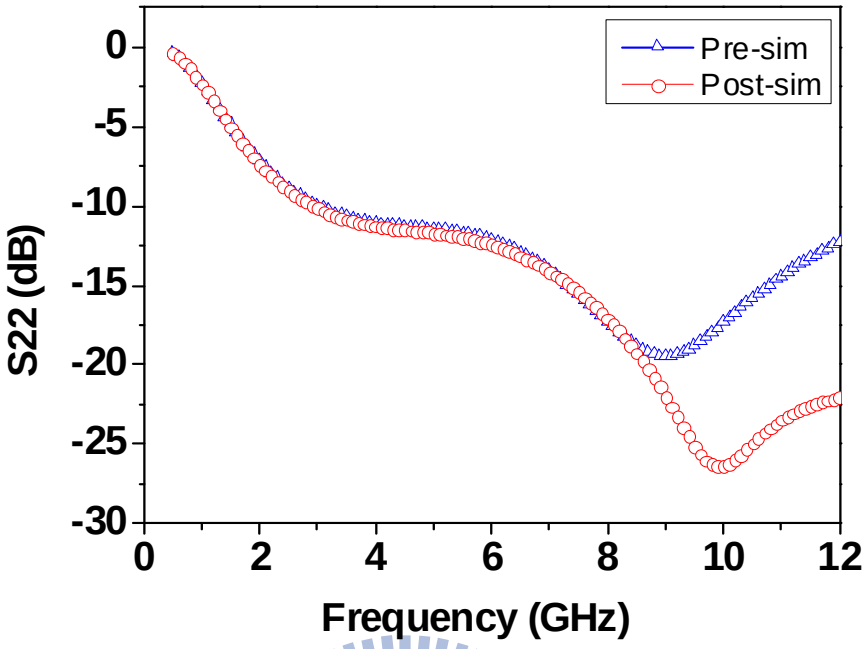


Fig. 3. 36 Comparison between pre-layout and post-layout simulation results for the output return loss (S_{22}). V_{DD}=0.9V, V_G=0.4V, frequency=0.5~12 GHz.

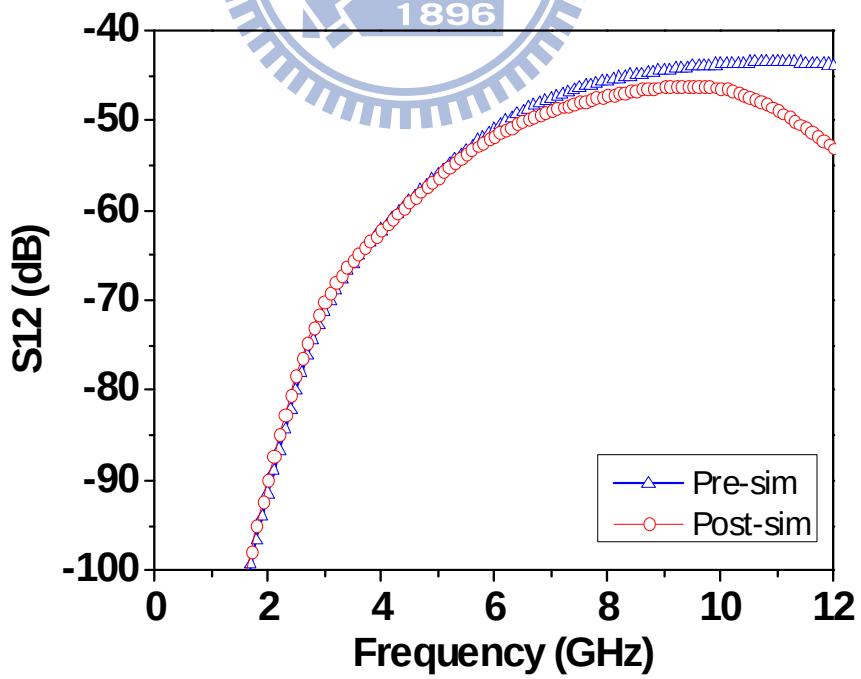


Fig. 3. 37 Comparison between pre-layout and post-layout simulation results for the reverse isolation (S_{12}). V_{DD}=0.9V, V_G=0.4V, frequency=0.5~12 GHz.

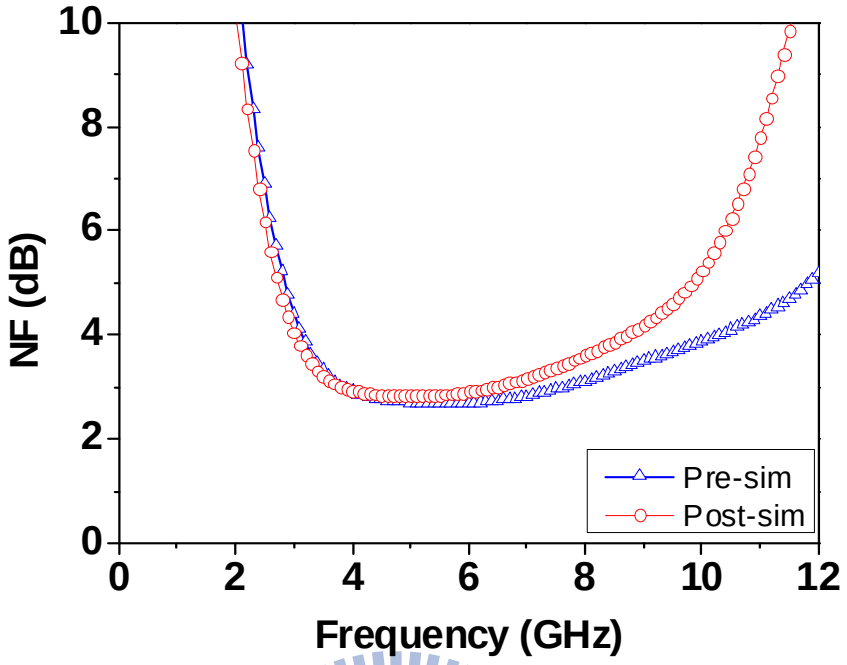


Fig. 3. 38 Comparison between pre-layout and post-layout simulation results for noise figure (NF). V_{DD}=0.9V, V_G=0.4V, frequency=0.5~12 GHz.

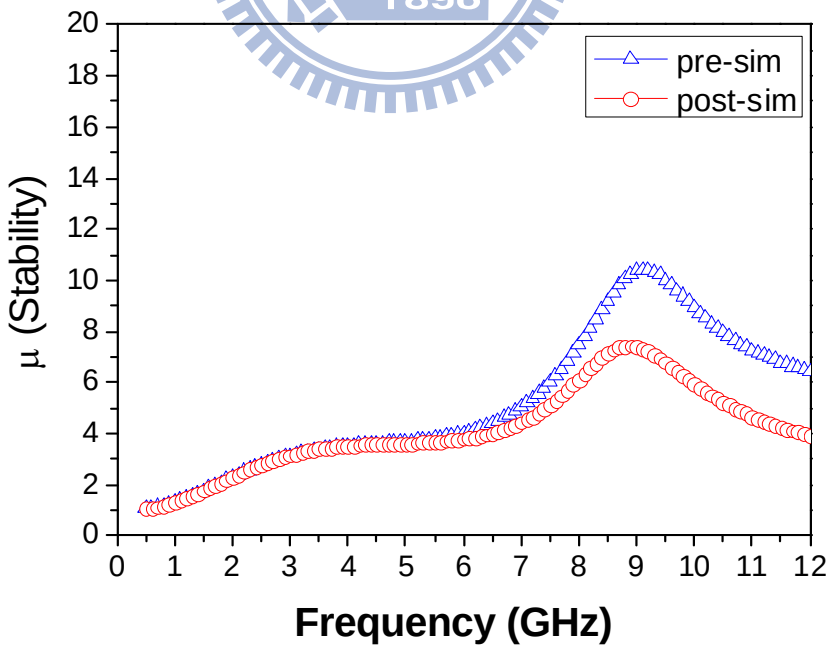
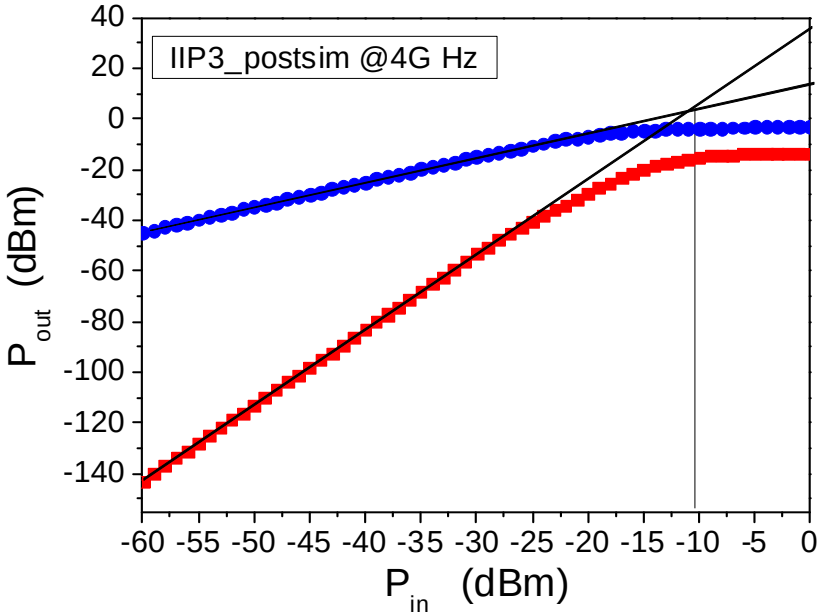
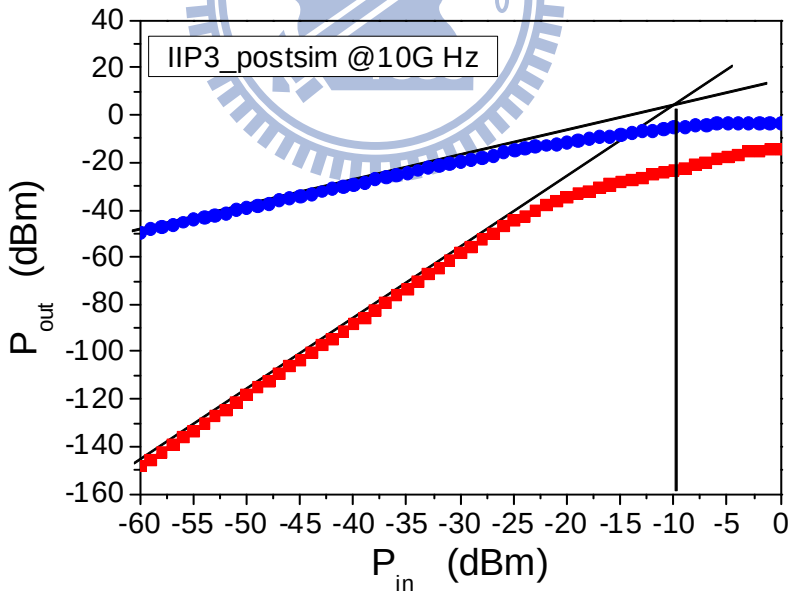


Fig. 3. 39 Comparison between pre-layout and post-layout simulation results for stability. V_{DD}=0.9V, V_G=0.4V, frequency=0.5~12 GHz.



(a)



(b)

Fig. 3. 40 Post-layout simulation for third-order intercept point (IIP3) (a) 4GHz : IIP3 = -11dBm (b) 10GHz IIP3= -10dBm. Two-tone test with tone spacing of 1MHz. V_{DD}=0.9V, V_G=0.4V.

Table 3. 3 Post-layout simulation results, under typical and corner conditions

Post-layout simulation

RF Corner	Unit	TT	FF	SS
Frequency	GHz	3.1 ~ 10.6	3.1 ~ 10.6	3.1 ~ 10.6
Power (only core LNA)	mW	4.7	7.9	2.5
Power (total)	mW	8.2	11.0	6.6
Supply Volatge (V_{DD})	V	0.9	0.9	0.9
Bias current (only core LNA)	mA	5.23	8.74	2.80
Bias current (total)	mA	9.10	12.20	7.31
Gain(S_{21})max / Gain(S_{21})min	dB	17.2 / 8.4	16.1 / 8.0	16.2 / 5.7
NF - min / max	dB	2.8 / 6.5	2.5 / 5.0	3.4 / 8.8
Input Return Loss (S_{11})	dB	< -8.3	< -8.2	< -7.5
Output Return Loss (S_{22})	dB	< -10.3	< -9.7	< -10.9
IIP3	dBm	-11@4GHz,-10@10GHz	-12@4GHz,-11@10GHz	-7@4GHz,-4@10GHz
Reverse isolation (S_{12})	dB	< -46.1	< -43.7	< -47.4

Table 3. 4 Comparison of pre-layout and post-layout simulation results (typical condition)

Specification	Unit	Pre-sim	Post-sim
Frequency	GHz	3.1 ~ 10.6	
Power (only core LNA)	mW	4.7	4.7
Power (total)	mW	8.3	8.2
Supply Volatge (V_{DD})	V	0.9	0.9
Bias current (only core LNA)	mA	5.23	5.23
Bias current (total)	mA	9.18	9.10
Gain(S_{21})max / Gain(S_{21})min	dB	17.3 / 11.2	17.2 / 8.4
NF - min / max	dB	2.7 / 4.1	2.8 / 6.5
Input Return Loss (S_{11})	dB	< -8.6	< -8.3
Output Return Loss (S_{22})	dB	< -10.1	< -10.3
IIP3	dBm	-10@4GHz,-11@10GHz	-11@4GHz,-10@10GHz
Reverse isolation (S_{12})	dB	< -43.6	< -46.1
Chip size	mm^2	0.637x0.892	

3.5 Measurement

3.5.1 Measurement Considerations

For this UWB LNA design, the test chip characterization will be performed through on-wafer measurement. To meet this purpose, the probing pads layout must follow the rule issued by NDL RF Lab. to match the RF probe station configuration. This LNA chip needs one 3-pin DC PGP probe and two RF GSG probes for on-wafer measurement. The measurement setup is shown in Fig. 3.41, where one DC PGP probe is located at the top and two RF GSG probes are place at two sides, in parallel to each other. Note that the DC PGP probe is used to provide the DC supply voltages to the drain and biasing voltage to the gate.

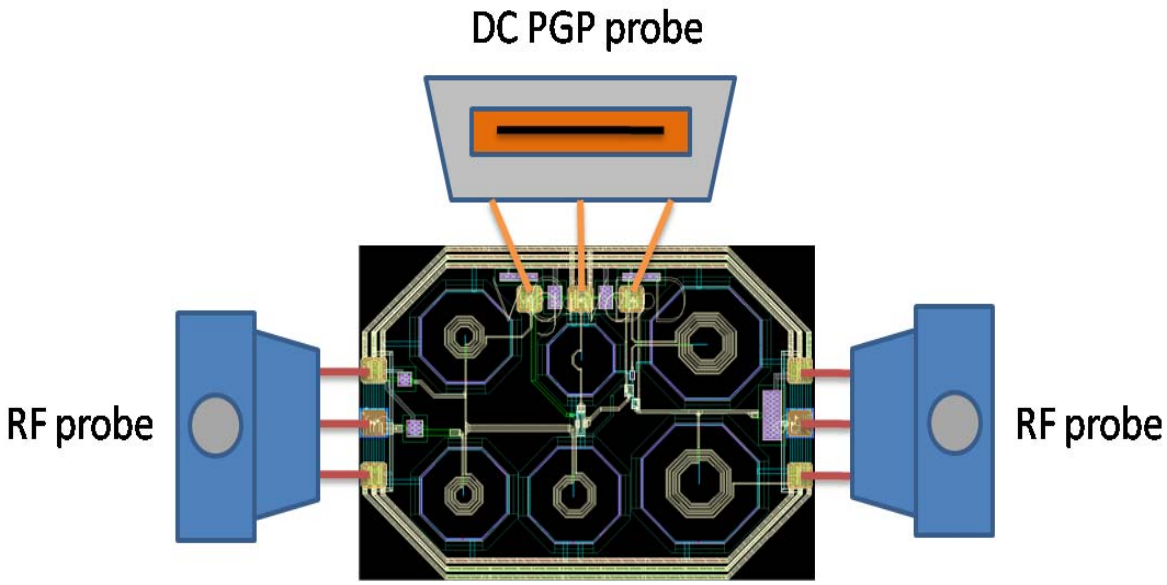
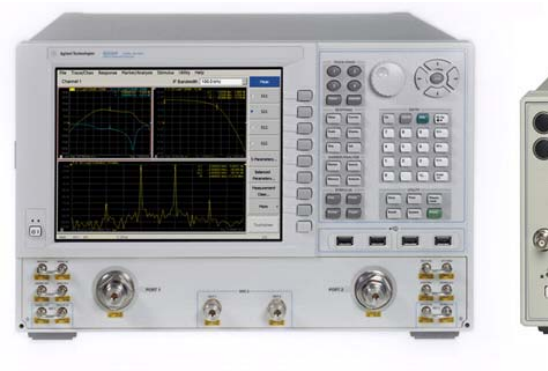


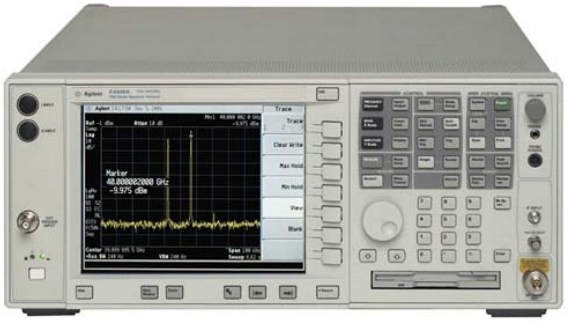
Fig. 3. 41 On-wafer measurement setup for UWB LNA chip test and characterization

The measurement equipments to support this LNA chip test include a network analyzer (Agilent PNA-X N5242A), a spectrum analyzer (Agilent E4448A) with options for NF measurement, and dc power supply (Agilent 6623A & Keithley Model 236 Source-Measure Unit). The measurement setups are shown in Fig.3.42(a) for S-parameter, IIP3, and 1-dB compression point (P1dB), and Fig.3.42(b) for noise figure. In the following, we will present

the LNA chip characterization results for all of the key performance parameters and a comparison with what predicted by post-layout simulation.



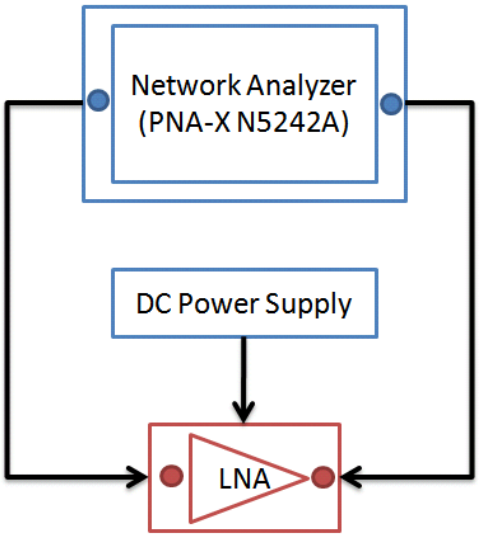
Agilent PNA-X N5242A



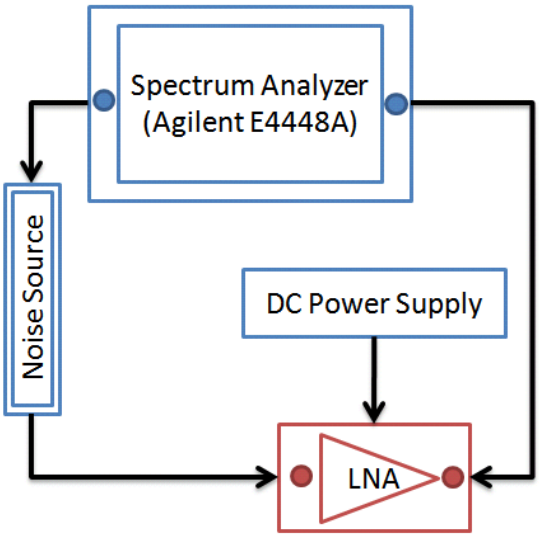
Agilent E4448A

Agilent 6623A

Keithley Model 236 Source-Measure Unit



(a)



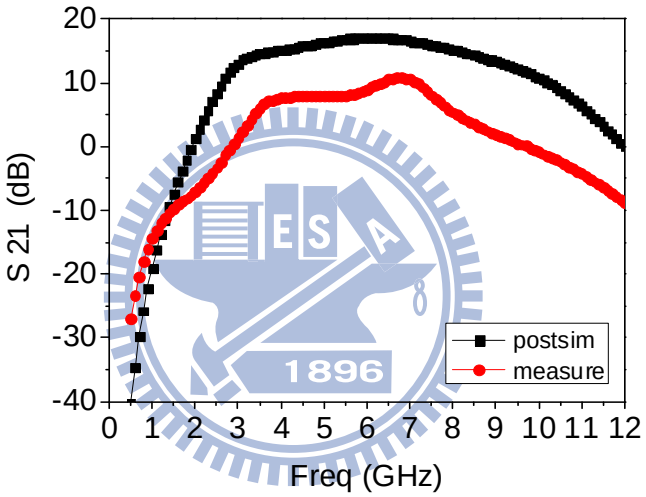
(b)

Fig. 3. 42 Measurement setups for (a) S-parameter & IIP3 & P1dB (b) noise figure

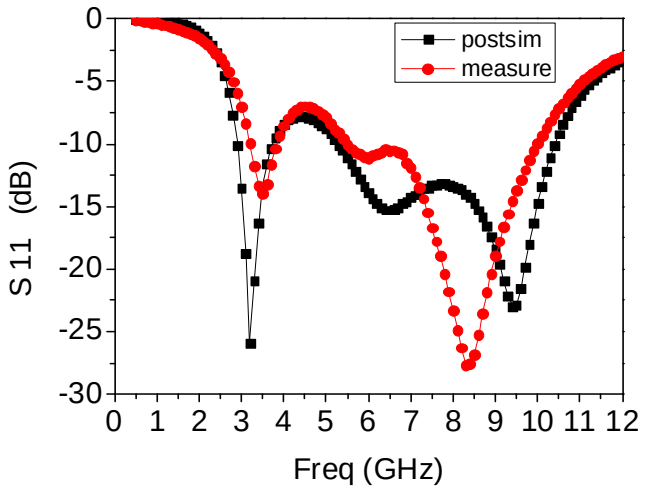
3.5.2 Measurement Results and Discussion

Fig. 3.43 presents the performance measured from this UWB LNA fabricated in 0.13μm 1.2V RF CMOS process. The comparisons between the measurement and post-layout simulation are demonstrated for power gain (S_{21}), input return loss (S_{11}), output return loss (S_{22}), reverse isolation (S_{12}), noise figure (NF) and stability, shown in Fig. 3.43(a)~(f). Fig. 3.44 indicates the measured third-order intercept point (IIP3) in which the IIP3 can reach 12dBm and 5dBm at 4GHz and 10GHz, respectively. Table 3.5 summarizes all of the performance parameters from our designed UWB LNA, and the comparison with post-layout simulation. The one-to-one comparison between measured data and simulation reveals an obvious degradation in the power gain (S_{21}) while a significant improvement on the linearity in terms of IIP3. The power gain achievable from this UWB LNA is S_{21}=5.0~10.8 dB over the bandwidth of 3.1 ~ 8.1 GHz, which are around 6/3.4 dB lower than the maximum/minimum gain predicted by simulation. As for the linearity, the measured IIP3 are as high as 12/5 dBm at 4/10 GHz, which are much better than the simulated IIP3 of –11/-10 dBm. The degradation of power gain, particularly worse in higher frequencies suggests that shunt peaking method cannot exactly meet the design target from simulation. The process variation induced shift in inductance (L_d) and resistance (R_d) is considered as one major root cause responsible for S_{21} degradation, and the power loss through the parasitic capacitance to the lossy Si substrate is proposed as the underlying mechanism. This kind of power loss generally increases dramatically when increasing frequency. Referring to (3-8), C_{out} representing the sum of junction and gate capacitances given as $C_{out} = C_{db2} + C_{gd3} + C_{dg2} + C_{gs3}(1-K)$ in (3-11) becomes a critical coupling path for power loss. Besides, Cgs of M2 (Fig.3.1) offers one more path for power loss at high frequency. The input matching circuits are justified by the acceptable match in S_{11} but somewhat more deviation is revealed in output matching in terms of S_{22}. The measured NF is close to the simulated performance over the broadband of

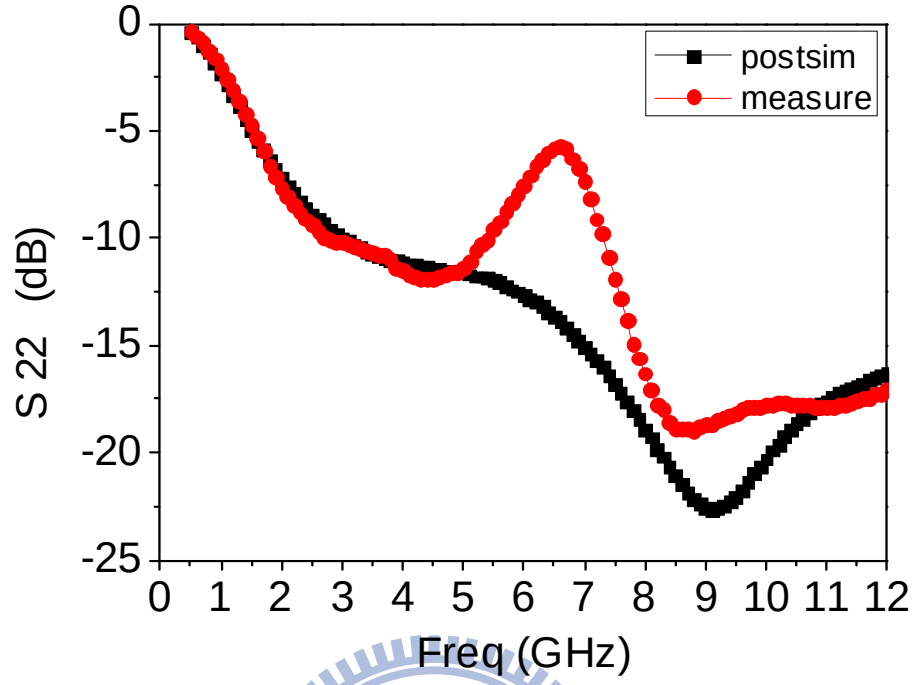
frequencies. This is an important achievement for LNA design and suggests the success of noise shielding technique using guard rings and ground shielding under the pads and transmission lines. Finally, an extensive performance benchmark with the state-of-the-art techniques in latest publications [5, 24, 35, 42, 43] has been done and summarized in Table 3.6. This benchmark indicates that our designed UWB LNA demonstrates the advantages of lower power, lower NF, and higher linearity (IIP3) under comparable gain and bandwidth. These advantages prove that the proposed UWB LNA can be realized by standard RF CMOS process and applied to UWB system applications.



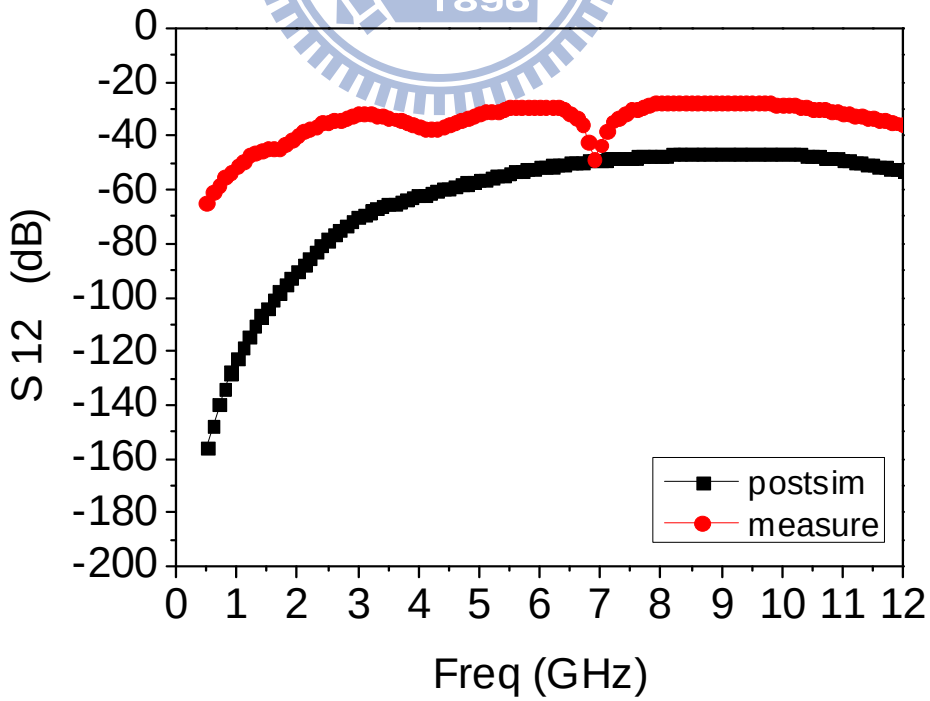
(a)



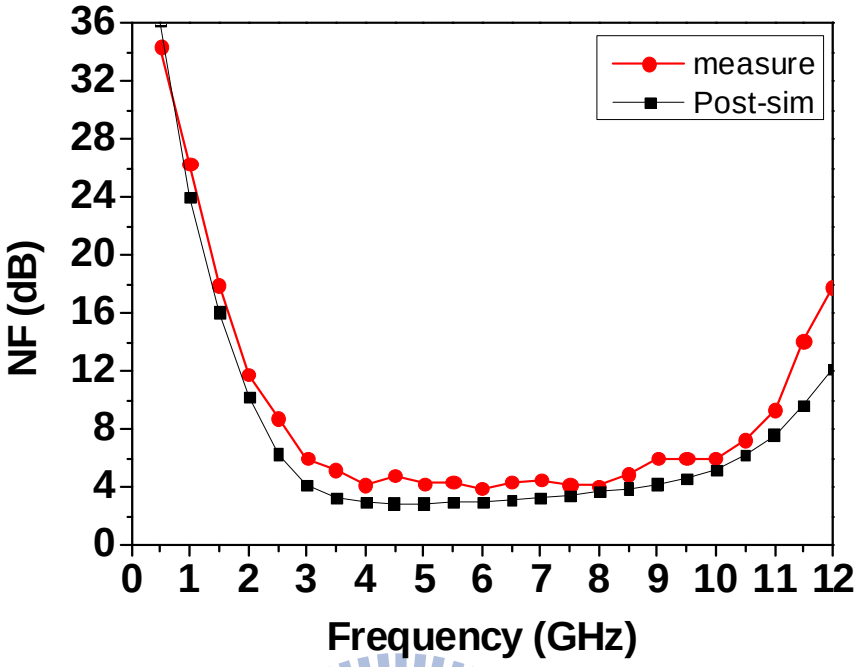
(b)


postsim
measure
S 22 (dB)
Freq (GHz)
0
-5
-10
-15
-20
-25
0 1 2 3 4 5 6 7 8 9 10 11 12

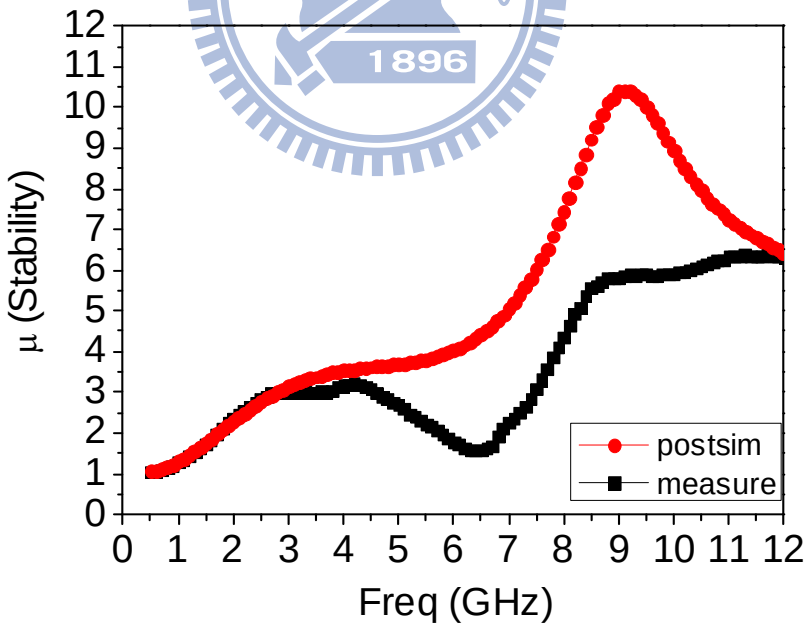
(c)


postsim
measure
S 12 (dB)
Freq (GHz)
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
-200
0 1 2 3 4 5 6 7 8 9 10 11 12

(d)

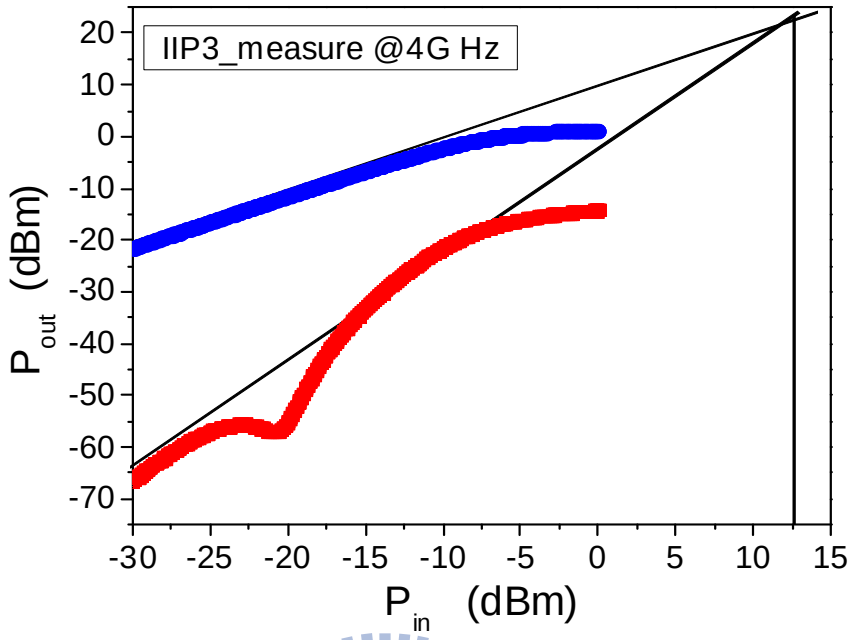


(e)

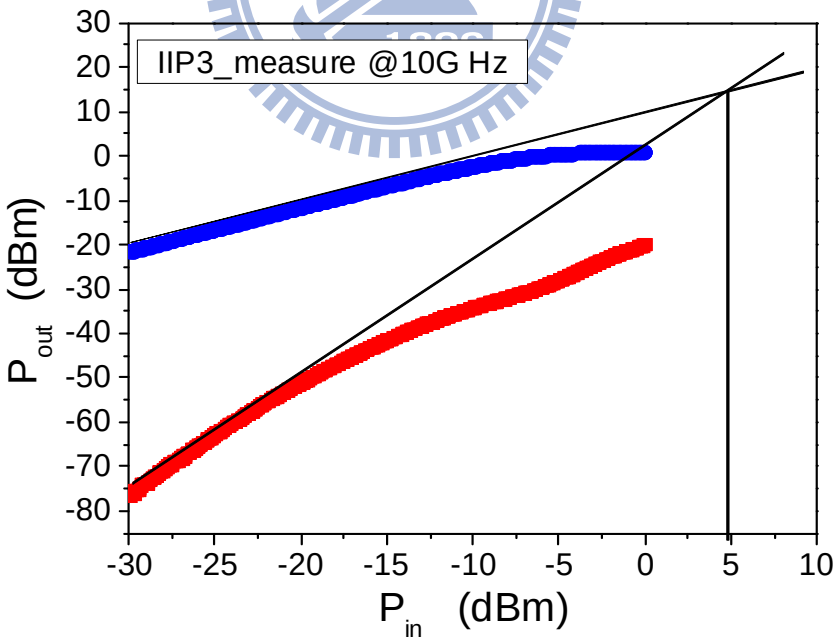


(f)

Fig. 3. 43 UWB LNA chip measured results and comparison with post-layout simulation for (a) power gain (S_{21}) (b) input return loss (S_{11}) (c) output return loss (S_{22}) (d) reverse isolation (S_{12}) (e) noise figure (NF) (f) stability



(a)



(b)

Fig. 3. 44 UWB LNA chip measured third-order intercept point (IIP3) (a) IIP3 =12dBm at 4GHz (b) IIP3= 5dBm at 10GHz

Table 3. 5 UWB LNA chip measured performance and comparison with post-layout simulation

Specification	Unit	Post-sim	measure
Frequency	GHz	3.1 ~ 10.6	3.3 ~ 8.1
Power (only core LNA)	mW	4.7	--
Power (total)	mW	8.2	8.4
Supply Volatge (V_{DD})	V	0.9	0.9
Bias current (only core LNA)	mA	5.23	--
Bias current (total)	mA	9.10	9.30
Gain(S_{21})max / Gain(S_{21})min	dB	17.2 / 8.4	10.8 / 5.0
NF- min / max	dB	2.8 / 6.5	3.9 / 4.1
Input Return Loss (S_{11})	dB	< -8.3	< -6.7
Output Return Loss (S_{22})	dB	< -10.3	< -5.8
IIP3	dBm	-11@4GHz,-10@10GHz	12@4GHz,5@10GHz
Reverse isolation (S_{12})	dB	< -46.1	< -27.3
Chip size	mm^2	0.637x0.892	

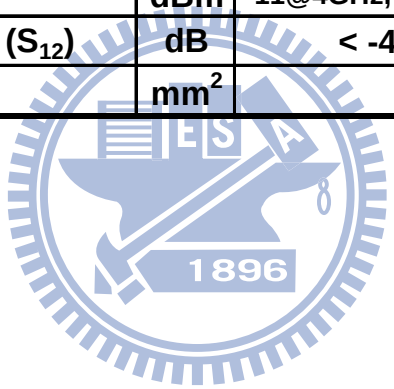


Table 3. 6 UWB LNA Performance Benchmark

RF Corner	Unit	This work	This work	This work	[43]
Frequency	GHz	3.3 ~ 8.1	3.1 ~ 10.6	3.1 ~ 10.6	3.1 ~ 10.6
Power (core LNA only)	mW	--	4.7	4.7	--
Power (total)	mW	**8.4**	**8.2**	**8.3**	**23.5**
Supply Voltage (V_{DD})	V	0.9	0.9	0.9	1.0
Bias current (only core LNA)	mA	--	5.23	5.23	--
Bias current (total)	mA	9.30	9.10	9.18	23.5
Gain(S_{21})max / Gain(S_{21})min	dB	10.8 / 5	17.2 / 8.4	17.3 / 11.2	9.2 / 7.4
NF - min / max	dB	3.9 / 4.1	2.8 / 6.5	2.7 / 4.1	4.1 / 7.0
Input Return Loss (S_{11})	dB	< -6.7	< -8.3	< -8.6	< -9.7
Output Return Loss (S_{22})	dB	< -5.8	< -10.3	< -10.1	--
IIP3	dBm	12@4G,5@10G	-11@4G,-10@10G	-10@4G,-11@10G	7.25 @6G
Reverse isolation (S_{12})	dB	< -27.3	< -46.1	< -43.6	--
Topology	--	LC-filter based + FBB	LC-filter based + FBB	LC-filter based + FBB	Feedback
Process technology	um	0.13 µm CMOS	0.13 µm CMOS	0.13 µm CMOS	0.18 µm CMOS
Year	--	2009	2008	2008	2007
measure or simulate	--	m	Post-s	Pre-s	m
Chip size	mm^2	0.637 x 0.892	0.637 x 0.892	0.637 x 0.892	0.995 x 0.780
FOM(Figure of Merit)	W^{-1}	15.6	32.1	53.7	7.3
FOM/Size	$(W^{-1})/(mm^2)$	27.5	56.4	94.4	9.4

RF Corner	Unit	[35]	[24]	[42]	[5]
Frequency	GHz	3.1 ~ 10.6	3.1 ~ 10.6	3.1 ~ 12.8	2.3 ~ 9.2
Power (only core LNA)	mW	15.6	--	18	9
Power (total)	mW	**26**	**33.2**	**--**	**18**
Supply Voltage (V_{DD})	V	1.3	1.8	1	1.8
Bias current (core LNA only)	mA	12	--	18	5
Bias current (total)	mA	20	18.4	--	10
Gain(S_{21})max / Gain(S_{21})min	dB	15.15 / 11	17.5 / 15.9	19 /--	9.3 / 4.5
NF - min / max	dB	2.18 / 2.88	3.1 / 5.7	2.8 / **9.0**	4.0 / **9.0**
Input Return Loss (S_{11})	dB	<-13	<-9	<-13	<-9.9
Output Return Loss (S_{22})	dB	<-10	<-13	--	<-10
IIP3	dBm	-5.77 @10.6G	--	--	-6.7 @6G
Reverse isolation (S_{12})	dB	<-39	<-70	--	<-43
Topology	--	Feedback	Common Gate	LC-filter based	LC-filter based
Process technology	um	0.18 µm CMOS	0.18 µm CMOS	0.13 µm CMOS	0.18 µm CMOS
Year	--	2006	2006	2005	2004
measure or simulate	--	s	s	s	m
Chip size	mm^2	1.1 x 1.2	0.74 x 0.67	0.7 x 0.8	1.0 x 1.1
FOM(Figure of Merit)	W^{-1}	30.8	13.9	--	6.0
FOM/Size	$(W^{-1})/(mm^2)$	23.3	28.0	--	5.5

Chapter 4

Sub-0.2mW Ultra-low Power LNA Design using Forward Body Biasing Technique

4.1 Introduction

In recent decade facing the stringent problems of energy sources draining and carbon emission induced global warming, clean energy and ultra-low power techniques have attracted an extensive research effort in all areas, such as materials, processes, devices, circuits, and systems. Ultra-low power wireless communication has been recognized as one of the most important domains, which match the right direction of clean energy and low emission. In the area of wireless communications, wireless sensor networks (WSN) emerges as a key component in a widely spread applications. Furthermore, the advent of WSN stimulates a strong demand for ultra-low power radio frequency integrated circuits (RFICs) to extend the battery life to reach the requirement of long time monitoring without replacement. Therefore, it is important to substantially reduce DC power consumption of CMOS RFICs with all other key performances properly maintained.

Among the published low-power techniques in CMOS platform, subthreshold region operation becomes an attractive technique in advanced CMOS processes to nanoscale regime where sufficient transconductance (g_m) can be achieved when using an optimized matching network. Theoretically, lowering the gate overdrive (V_{GS}-V_T) can improves the g_m to drain current (I_{DS}) ratio, i.e. g_m/I_{DS}. It is because that I_{DS} has an exponential dependence on the gate-source voltage (V_{GS}) in subthreshold region [44]. Adopting this comments for LNA design, its gain to power consumption ratio can be increased in subthreshold region as compared to that of strong inversion region. However, to meet the required g_m, large input

transistors are usually needed. By increasing the width of the transistors operating in subthreshold region, the gain can be maintained sufficiently high, while DC power consumption is substantially reduced [45]. Furthermore, it is feasible to keep the minimum noise figure (NF_{min}) sufficiently low in subthreshold region for the nanoscale MOS transistors provided that g_m is increased to sufficiently high by increasing the width [46]. As a result, the noise figure of the amplifier with CMOS transistors biased in subthreshold does not degrade drastically as DC power dissipation is reduced.

This chapter presents a fully monolithic micro-power LNA using subthreshold MOS devices with forward body biasing (FBB) technique and on-chip inductors at 1.4 GHz to lower the DC power dissipation. The LNA is fabricated in UMC 90nm Logic & Mixed-Mode 1P9M Low-K Process.

4.2 Circuit Architectures for ULP LNA

Fig.4.1 illustrates the circuit architecture for our proposed ultra-low power (ULP) LNA. This ULP LNA is composed of an input matching network, an amplifying stage with cascode topology, and an output matching network. The cascode amplifier consists of an input transistor M1 and a cascade transistor M2.

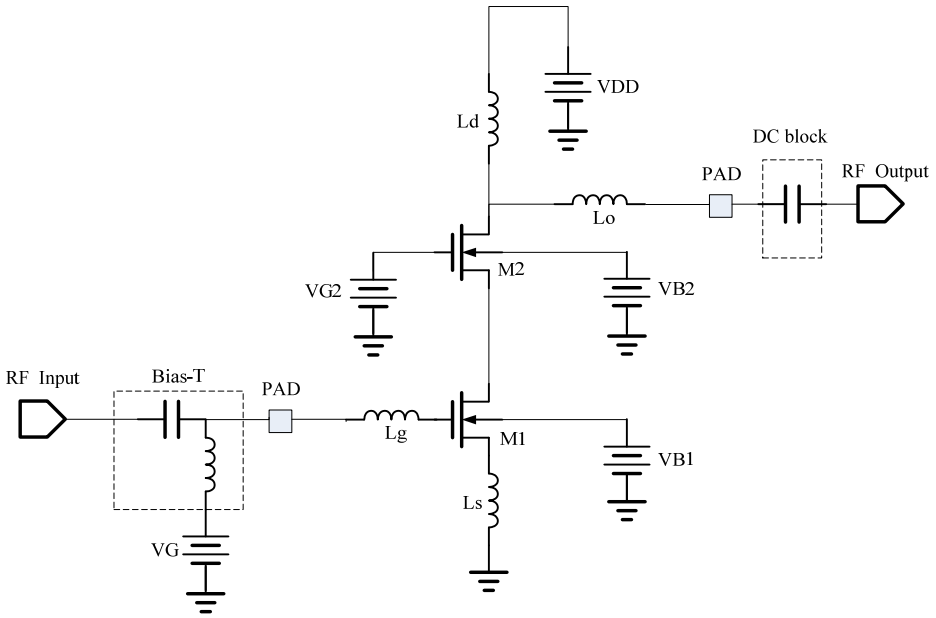


Fig. 4. 1 Circuit architecture of the proposed ultra-low power (ULP) LNA

As it is well know that cascade amplifier has the advantages of higher gain and better isolation. However, the cascade structure consisting of two stacked transistors generally leads to the penalty of higher supply voltage and then higher power. To overcome the mentioned drawbacks, forward body biasing (FBB) technique is proposed to achieve low-voltage LNA design by reducing transistor's threshold voltage (V_T). According to the mentioned argument, the input transistor M1 (NMOS) in the cascade structure is biased in subthreshold region to realize superior gain per current and achieve low power performance. Besides, the gate width over length ratio (W/L) of the two transistors (M1 and M2) have to be increased and optimized to increase the gain of the amplifier and realize an input impedance matching to 50-Ω. A source degeneration inductor (L_S) serves as another critical element to facilitate input matching to 50-Ω, and also enables good linearity and high reverse-isolation, which can facilitate amplifier stability. As for the output stage, an inductive load (L_d) as opposed to a resistive load, is preferred. An inductive load has the added benefit of boosting the gain by resonating with the capacitances associated with the output node. In this design, the output matching network is composed of L_d and L_o.

4.3 LNA Circuit Analysis

In this section, a small signal equivalent circuit analysis will be carried out for our proposed ULP LNA, with the circuit schematics illustrated in Fig. 4.2

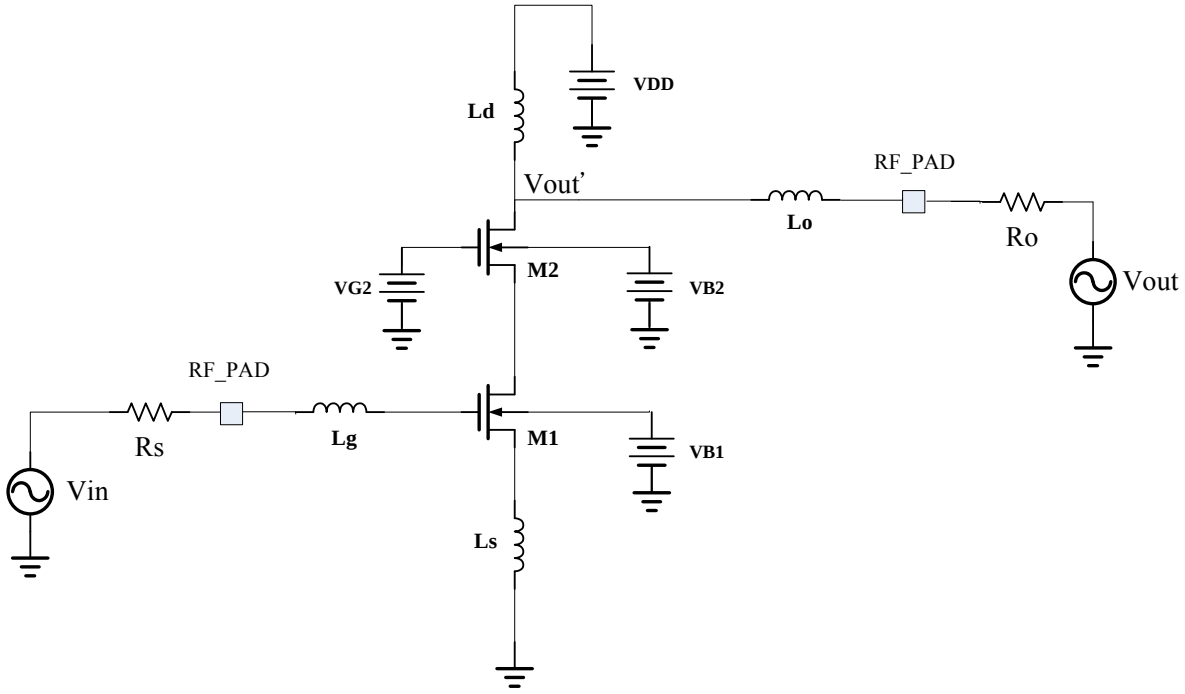


Fig. 4. 2 The circuit schematic of ULP LNA

4.3.1 Gain Analysis

As mentioned previously, a cascode topology with source inductive degeneration is used for improving the reverse isolation, frequency response, better noise figure and lower Miller effect. Input impedance matching by inductive source degeneration had been discussed previously in Chapter 2. In the following, circuit performance will be analyzed based on the small signal equivalent circuit for the proposed ULP LNA, shown in Fig.4.3. First, voltage gain is derived as follows.

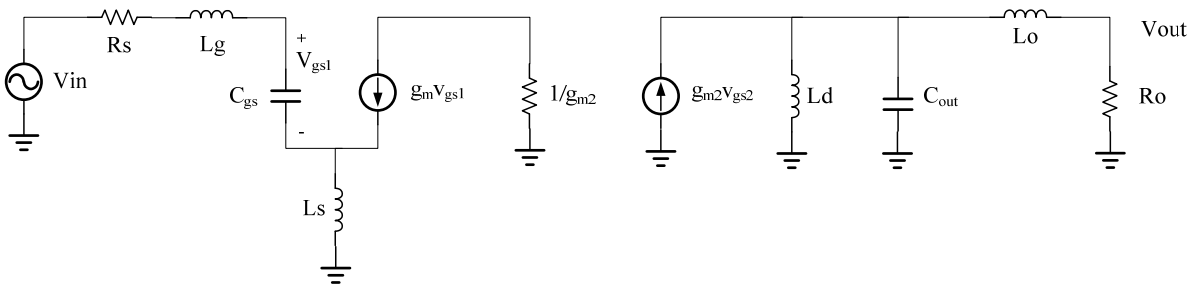


Fig. 4. 3 Small signal equivalent circuit analysis for the ULP LNA

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}^{'}}{V_{in}} \cdot \frac{V_{out}}{V_{out}^{'}}$$

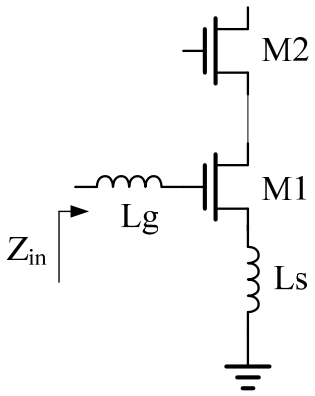
$$= \frac{-g_m}{s^2(L_g + L_s)C_{gs} + s(C_{gs}R_s + g_m L_s) + 1} \cdot \frac{s^2 L_d L_o + sL_d R_o}{s^3 L_d L_o C_{out} + s^2 L_d C_{out} R_o + s(L_o + L_d) + R_o} \cdot \frac{R_o}{sL_o + R_o}$$

(4-1)

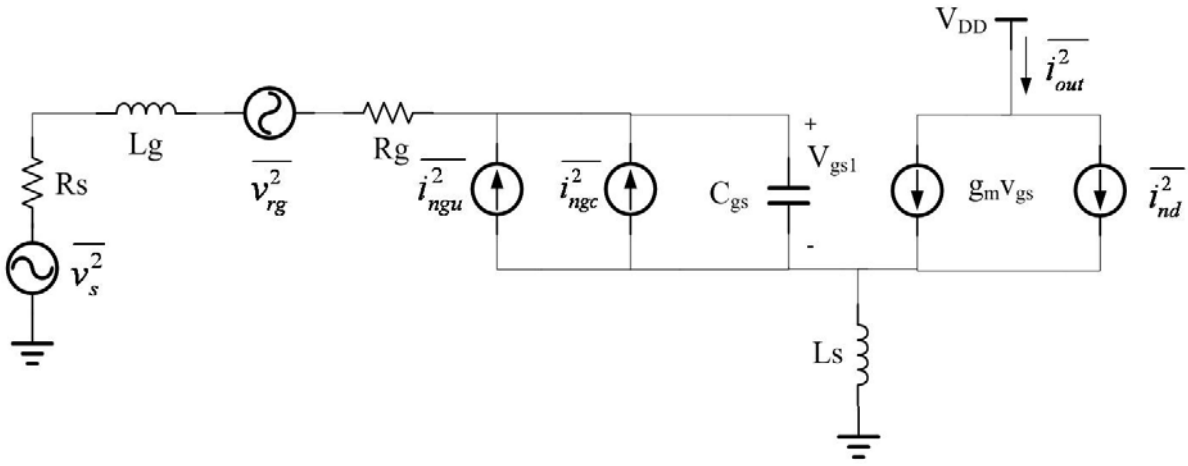
where the capacitance C_{out} may be taken to represent all the loading on the drain node of M2, C_{gs} is the gate-source capacitance of M1, R_S is the impedance of the input signal source, and R_O represent the output load impedance. The derived voltage gain in (4-1) indicates that the increase of parasitic resistances (R_S, R_O) and capacitances (C_{gs}, C_{out}) will degrade the gain available for the LNA, and the degradation becomes worse under higher frequencies.

4.3.2 Noise Analysis [4]

For LNA design, an appropriate selection of circuit topology at the first stage is critically important, not only for a good input matching but also for lower noise. Fig. 4.4(a) depicts a simple common source (CS) cascade structure, which has been adopted as a amplifying stage, i.e. the first stage in our proposed ULP LNA. An on-chip inductor L_S is employed for inductive source degeneration. Fig. 4.4(b) shows a small signal equivalent circuit for noise model of the mentioned input stage in LNA.



(a)



(b)

Fig. 4. 4 (a) a simple cascade structure used as a common source input stage of LNA (b) a small signal equivalent circuit for the noise model of input stage in LNA

According to Fig. 4.4 (a), the input impedance of the cascade amplifier is represented by

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + j[\omega(L_g + L_s) - \frac{1}{\omega C_{gs}}]$$

$$for\ \omega = \omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \qquad (4\text{-}2)$$

$$Z_{in} = \omega_T L_s,\ \omega_T = \frac{g_m}{C_{gs}}$$

The derived equation (4-2) indicates that the input impedance Z_{in} becomes purely real and proportional to Ls when operating at the resonance frequency determined by the series LC (L_g, L_S, and C_{gs}) at the input stage. By choosing Ls appropriately, this real term can be made equal to 50 Ω. In Fig. 4.4 (b), R_g represents the series resistance of the inductor as well as the gate resistance of the NMOS device (M1 in Fig.4.4(a)), and $\overline{i_{nd}^2}$ represents the channel thermal noise of M1, while the $\overline{i_{ngc}^2}$ and $\overline{i_{ngu}^2}$ are the gate noise from correlated and uncorrelated term. Here, analysis based on this equivalent circuit neglects the contribution of subsequent stages to the amplifier noise figure. This simplification is justifiable provided that the first stage possesses sufficient gain and allows us to examine in detail the salient features of this

architecture.

In order to find the output noise, we first evaluate the transconductance G_m of the input stage. With the output current proportional to the voltage on C_{gs} and nothing that the input circuit takes the form of series-resonant network, the transconductance at the resonant frequency is given by

$$|G_m| = \frac{1}{R_s + \omega_T L_s} \cdot \frac{1}{\omega_0 C_{gs}} \cdot g_m = \frac{\omega_T}{\omega_0 R_s (1 + \frac{\omega_T L_s}{R_s})} = \frac{\omega_T}{2\omega_0 R_s} \tag{4-3}$$

From this equation, the output noise power density due to the source is

$$S_{a,src}(\omega_0) = S_{src}(\omega_0) \cdot |G_m|^2 = \frac{4kT\omega_T^2}{\omega_0^2 R_s (1 + \frac{\omega_T L_s}{R_s})^2} \tag{4-4}$$

In a similar way, the output noise power density due to R_g can be expressed as

$$S_{a,R_g}(\omega_0) = S_{R_g}(\omega_0) \cdot |G_m|^2 = \frac{4kTR_g\omega_T^2}{\omega_0^2 R_s^2 (1 + \frac{\omega_T L_s}{R_s})^2} \tag{4-5}$$

Next, the noise power density associated with the correlated portion of the gate noise and drain noise can be expressed as [4]

$$S_{a,i_d,i_g,c}(\omega_0) = \kappa S_{a,i_d}(\omega_0) = \frac{4kT\gamma\kappa g_{d0}}{(1 + \frac{\omega_T L_s}{R_s})^2} \tag{4-6}$$

where

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + [1 + |c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}]^2$$

$$Q_L = \frac{1}{\omega_0 R_s C_{gs}}$$

$$\alpha = \frac{g_m}{g_{d0}}$$

The last noise term is the contribution of the uncorrelated portion of the gate noise. This contributor has the following power spectral density

$$S_{a,i_g,u}(\omega_0) = \xi S_{a,i_d}(\omega_0) = \frac{4kT\gamma\xi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{4-7}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q_L^2)$$

We observe that (4-6) and (4-7) can all proportional to the power spectral density of drain current noise, then the two equations can be combined as a simplified form:

$$S_{a,M_1}(\omega_0) = \chi S_{a,i_d}(\omega_0) = \frac{4kT\gamma\chi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{4-8}$$

where

$$\chi = \kappa + \xi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1+Q_L^2) \tag{4-9}$$

According to (4-4), (4-5) and (4-8), the noise factor at the resonant frequency can be written by the following equation:

$$\begin{aligned} F &= \frac{\textit{Total noise power @ output}}{\textit{Noise power @ output due to source only}} \\ &= 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}(\frac{\omega_0}{\omega_T}) \end{aligned} \tag{4-10}$$

To understand the implications of this new expression for the noise factor (F), we observe that χ given by (4-9) includes one term proportional to Q_L and another term proportional to Q_L^2. It follows that the noise factor in (4-10) will contain terms which are proportional to Q_L as well as inversely proportional to Q_L. Therefore, a minimum F exits for a particular Q_L. Besides, we observe that g_m is inversely proportional to F.

4.4 Chip Circuit Design and Simulation

UMC 90nm RF CMOS Spice Model was employed for this ULP LNA circuit simulation and design. This RF CMOS Spice Model includes passive elements, such as resistors,

inductors, capacitors, and RF MOSFETs as the major active devices. Also, on-chip circuit layout will be introduced.

4.4.1 Models for LNA Circuit Simulation

In RF circuits design, an accurate and scalable model is strongly demanded to assure circuit simulation accuracy and facilitate the success of circuit design. For active devices, the intrinsic MOSFET model suitable for logic circuit simulation is no longer valid for RF circuit design. Parasitic and coupling effects from interconnection, substrate, and pads should be considered and taken into the model. As for passive devices, such as inductors, capacitors, and resistors, substrate loss and conductor loss become important effects required for accurate modeling. In the following, RF device models will be introduced for active devices like MOSFETs and passive elements, such as spiral inductors and MiM capacitors.

4.4.2 ULP LNA Simulation Results

The whole circuit schematics for the proposed ULP LNA is illustrated in Fig. 4.5, in which three major blocks such as input matching network, cascade amplifying stage, and output matching network are included and the layout dimensions for active transistors and parasitic elements (R, L, C) are remarked for simulation. Note that all the components in this design, including spiral inductors and metal-insulator-metal (MIM) capacitors, are realized on a single chip. Fig. 4.6 depicts the chip layout of the proposed ULP LNA. The chip area including all of probing pads is 0.778×0.669 mm^2. This proposed ULP LNA is simulated with Agilent ADS simulator using UMC 90nm RFCMOS Spice Model. In the following, the simulation results will be presented, including pre-layout and post-layout under typical (TT) and corner conditions (FF, SS). For this ULP LNA design, the key performance parameters, such as power gain (S_{21}), input return loss (S_{11}), output return loss (S_{22}), reverse isolation (S_{12}), noise figure (NF), stability (μ), and third-order intercept point (IIP3) have been calculated by ADS simulation. Fig. 4.7 show the pre-layout simulation results, under the typical condition

of V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V, and frequencies in 0.8~2 GHz. Note that the third-order intercept point (IIP3) shown in Fig. 4.7(d) is determined by two-tone test with tone space of 10MHz, and fundamental frequency at 1.4GHz. Fig. 4.8 presents a comparison for all of the performance parameters, between pre-layout and post-layout simulation.

Table 4.1 and Table 4.2 summarizes the pre-layout and post-layout simulation for all of the performance parameters, with a comparison between typical (TT) and corner conditions (FF, SS). For mentioned simulation, the bias conditions are fixed at V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V, V_{B1}=0.4V,.and V_{B2}=0V. Note that V_{B1}=0.4V is the forward body bias (FBB) applied to amplifier transistor M1, which enables V_G scaling to 0.45V, approaching subthreshold region for ultra-low power operation. The results indicate that RF CMOS devices in 90 nm process, operating under the specified biases with FBB can achieve ultra-low power consumption to 0.19 mW for typical condition, and low NF of 2.1 dB. The performance looks very promising in both power and noise. As for the fast corner conditions (FF), the power dissipation is increased to 0.56 mW but NF can be improved to 1.8 dB. On the other hand, for slow corner condition (SS), the power consumption is pushed to extremely low to 0.05mW, but paying the penalty of significantly higher NF, up to 4.2 dB. The post-layout simulation indicates similar results with very minor difference from that of pre-layout simulation. The variations of the RF performance parameters between typical (TT) and corner models (FF, SS), under fixed biases condition can be eliminated by using tunable biases adapted to corner models. The principle of biases tuning is lowering V_G and V_{G2} for fast corner (FF) while raising those for slow corner (SS). Tables 4.3 and table 4.4 present the pre-layout and post-layout simulation results, under tunable biases exactly adapted to FF and SS. In this way, the RF performance, particularly the power dissipation and NF of major concern, can be tuned to be similar for all three conditions (TT, FF, SS). The ultra-low power to sub-0.2 mW can be realized for TT and corner models.

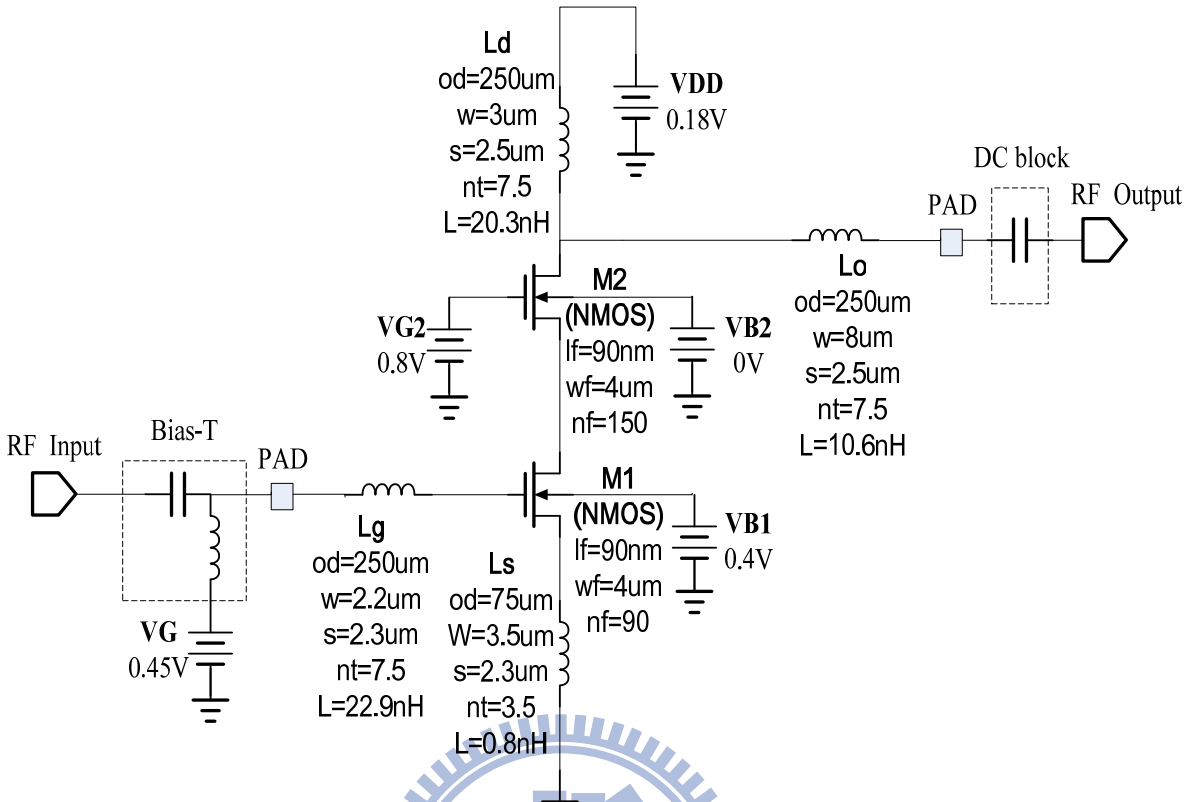


Fig. 4. 5 Circuit schematic of the ULP LNA with three core circuit blocks in which the active and passive devices dimensions are provided

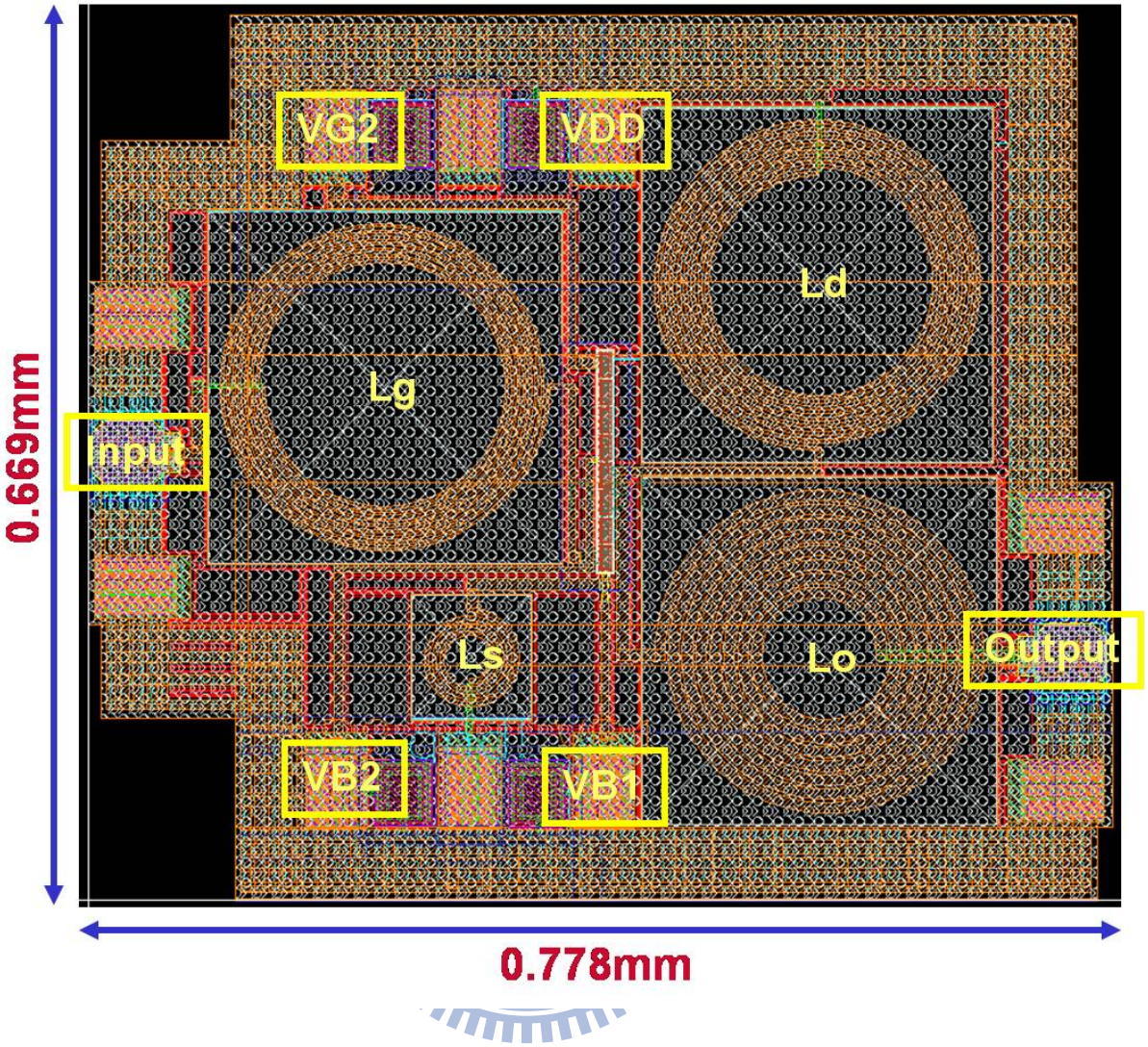
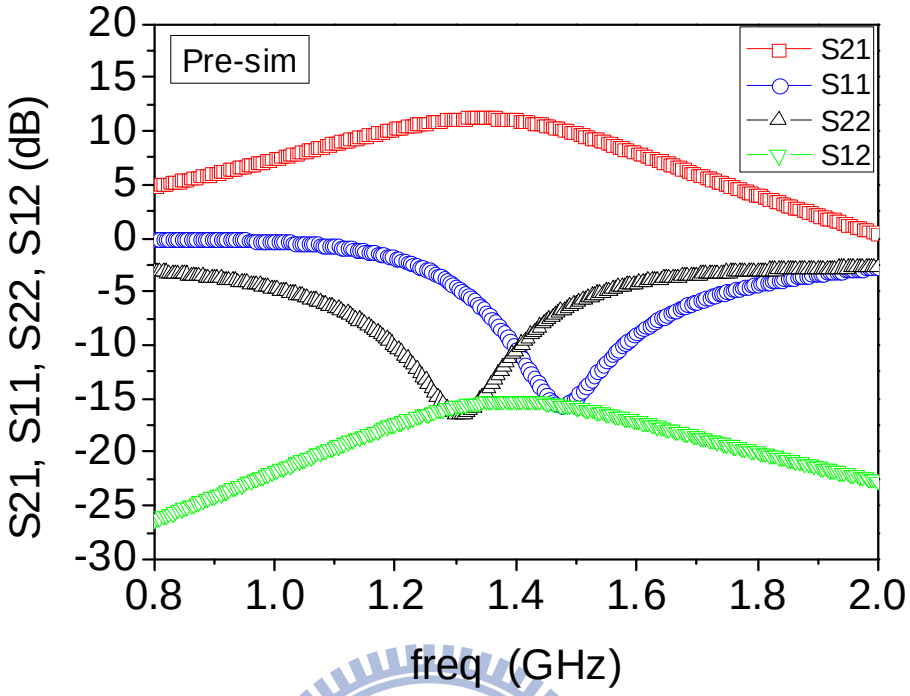
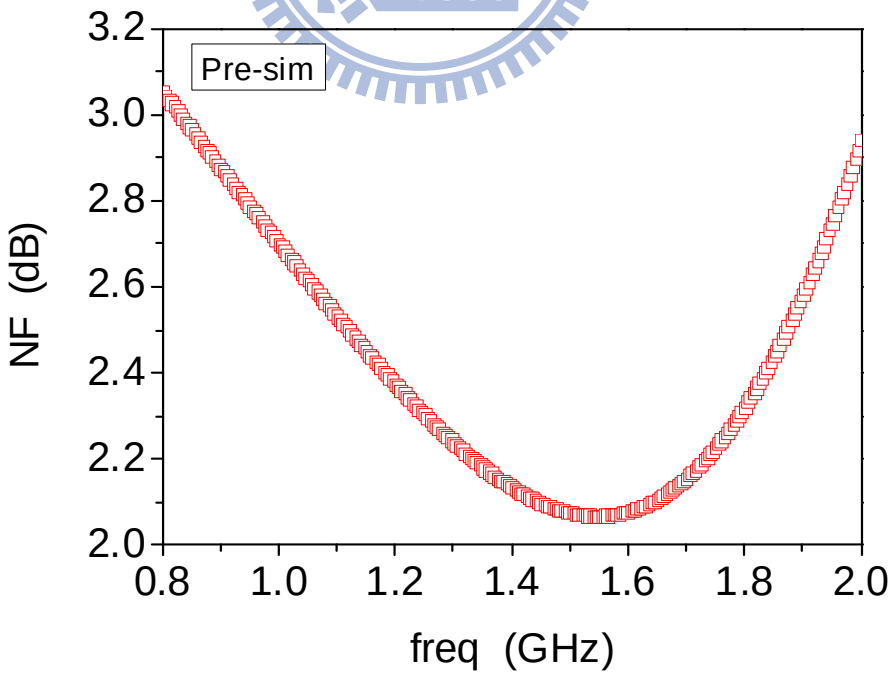


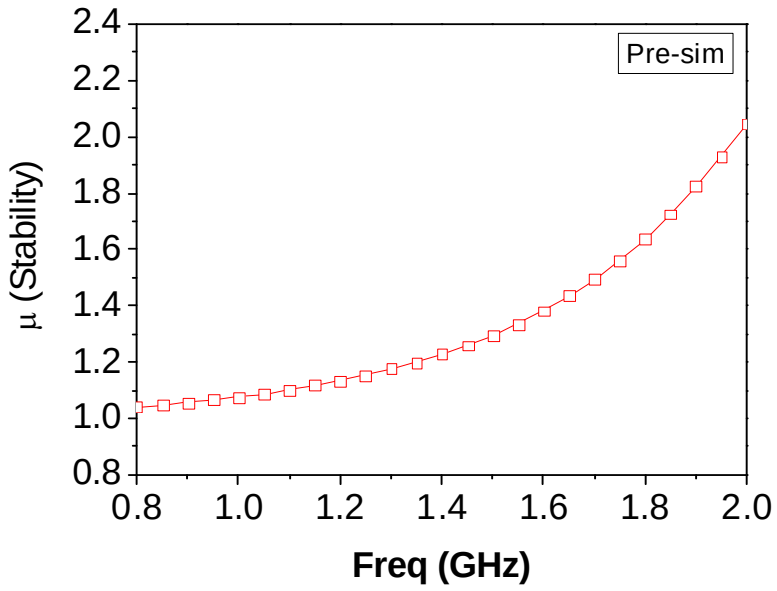
Fig. 4. 6 Chip layout of the designed ULP LNA


Pre-sim
S21
S11
S22
S12
S21, S11, S22, S12 (dB)
freq (GHz)

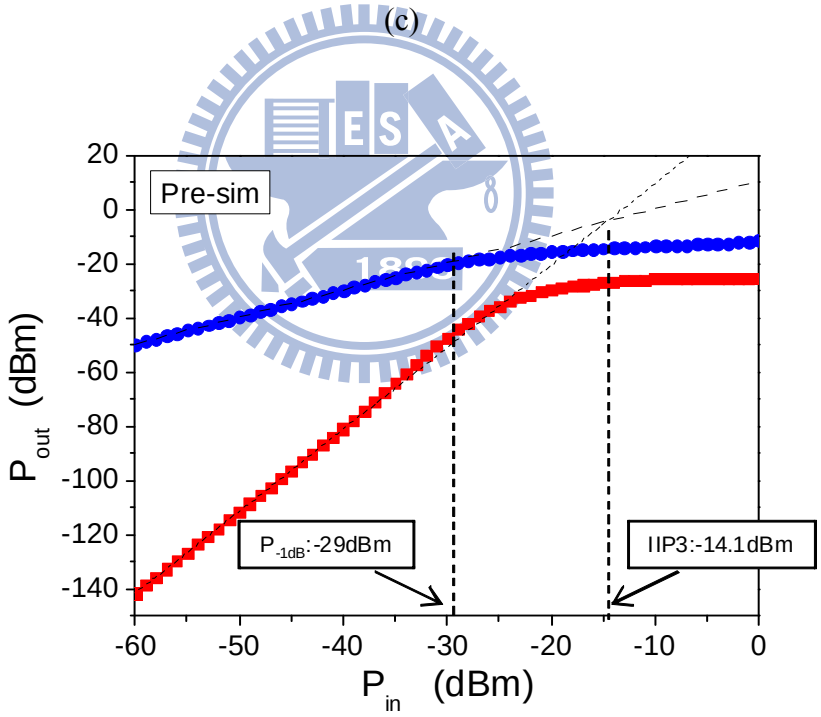
(a)


Pre-sim
NF (dB)
freq (GHz)

(b)

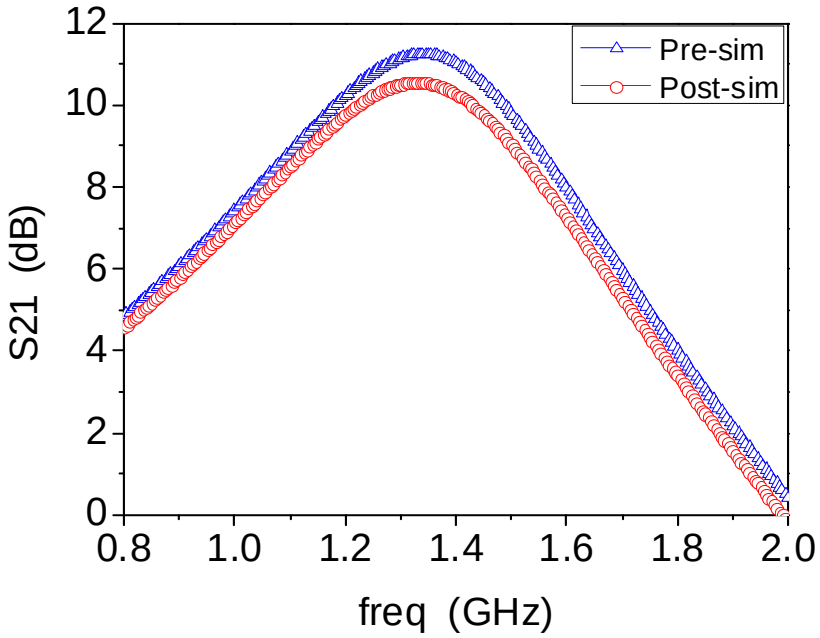


(c)

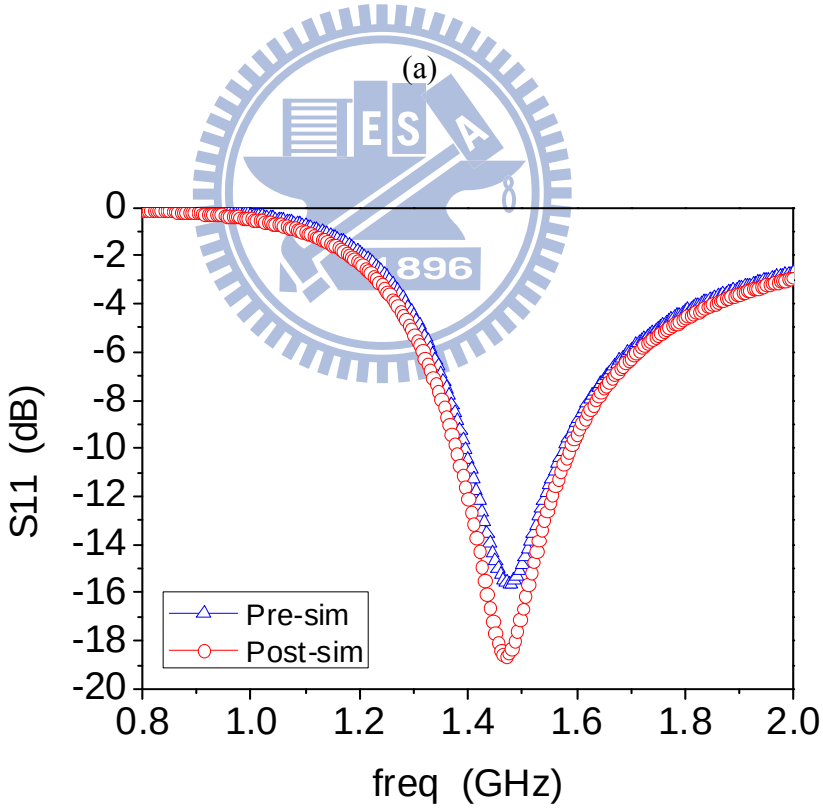


(d)

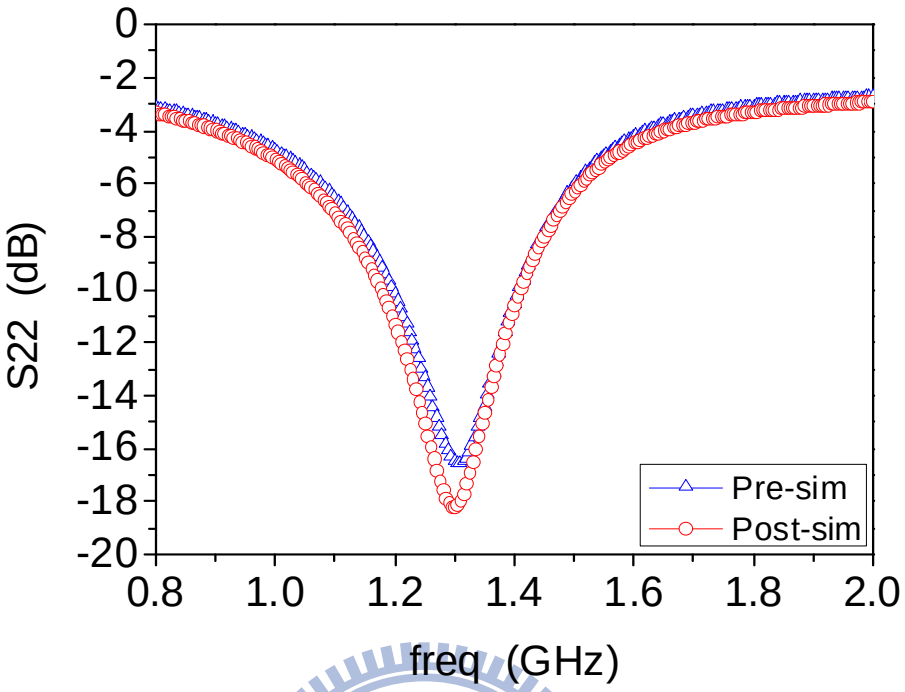
Fig. 4. 7 Pre-layout simulation for ULP LNA (a) power gain (S_{21}), input return loss (S_{11}), output return loss (S_{22}), reverse isolation (S_{22}) (b) noise figure (NF) (c) stability (d) third-order intercept point (IIP3), two tones space=10MHz, center frequency =1.4GHz. V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V, V_{B1}=0.4V, V_{B2}=0.


Pre-sim
Post-sim
S21 (dB)
freq (GHz)
0
2
4
6
8
10
12
0.8
1.0
1.2
1.4
1.6
1.8
2.0

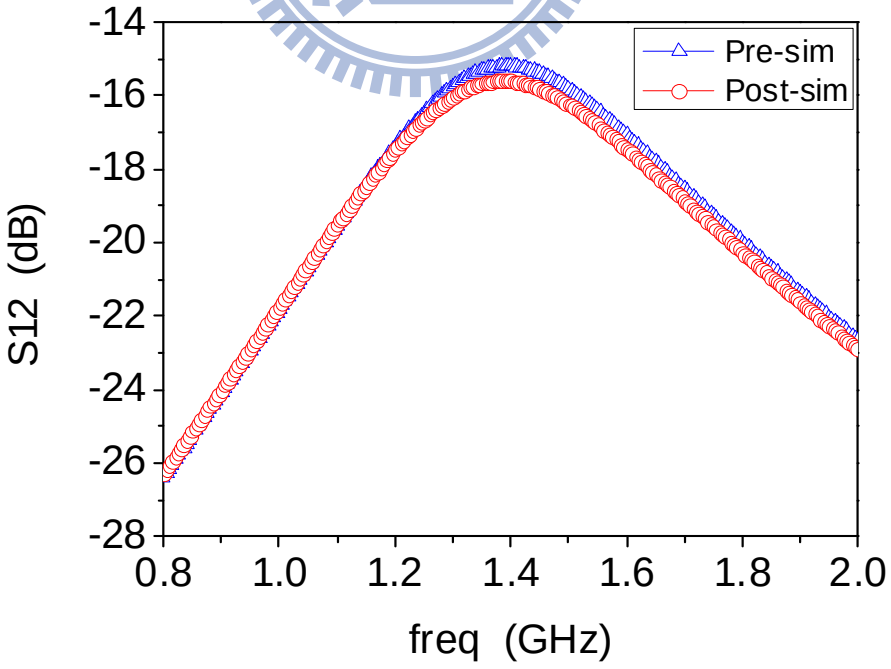
(a)


Pre-sim
Post-sim
S11 (dB)
freq (GHz)
0
-2
-4
-6
-8
-10
-12
-14
-16
-18
-20
0.8
1.0
1.2
1.4
1.6
1.8
2.0

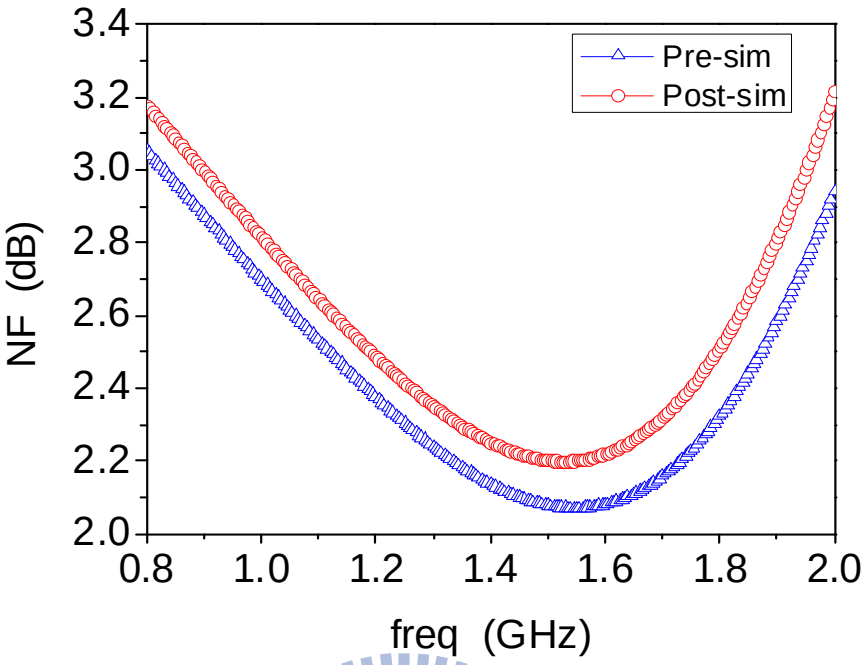
(b)


S22 (dB)
freq (GHz)
Pre-sim
Post-sim

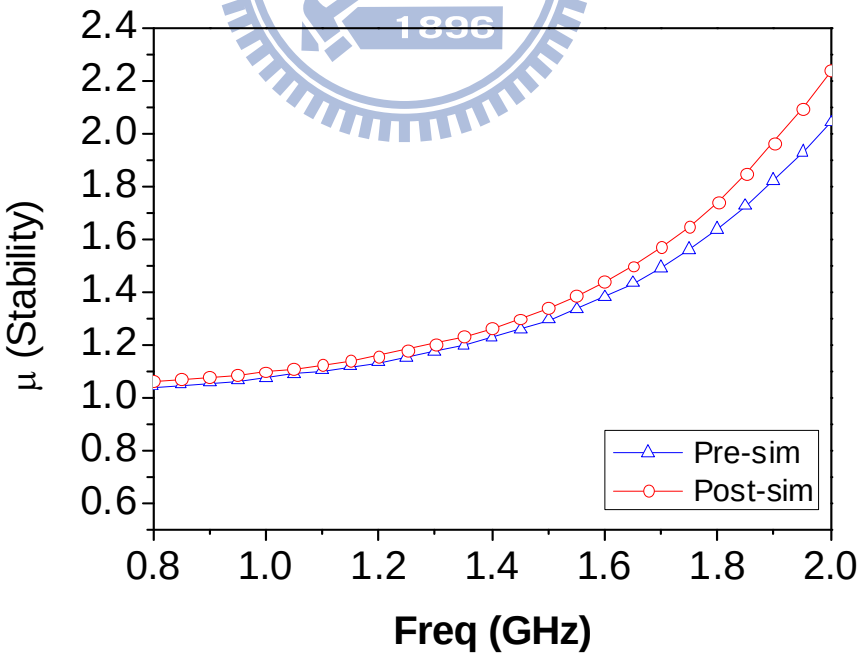
(c)


S12 (dB)
freq (GHz)
Pre-sim
Post-sim

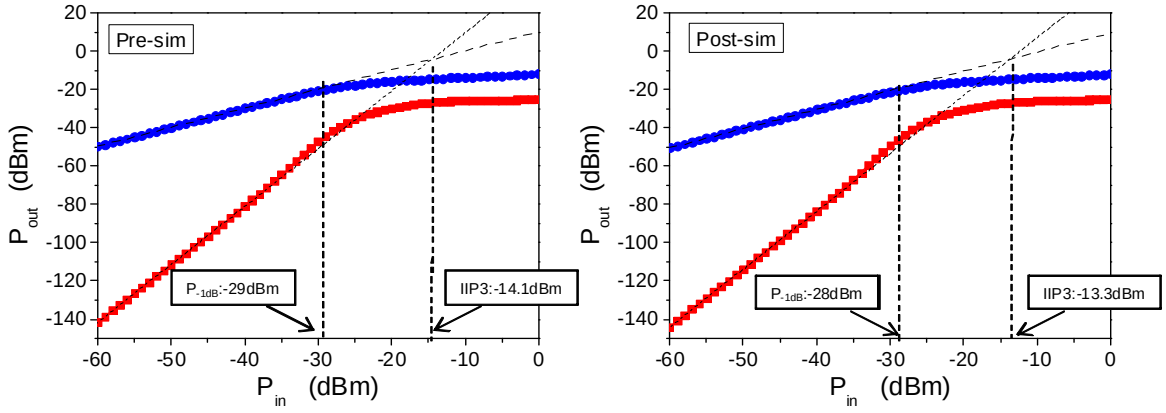
(d)


Pre-sim
Post-sim
NF (dB)
freq (GHz)
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
0.8
1.0
1.2
1.4
1.6
1.8
2.0

(e)


Pre-sim
Post-sim
μ (Stability)
Freq (GHz)
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

(f)



(g)

Fig. 4. 8 Comparison between pre-layout and post-layout simulation results for the ULP LAN (a) power gain(S_{21}) (b) input return loss (S_{11}) (c)output return loss (S_{22}) (d) reverse isolation (S_{21}) (e) noise figure (NF) (f) stability (g) third-order intercept point (IIP3). V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V, V_{B1}=0.4V, V_{B2}=0.

Table 4. 1 Pre-layout simulation for ULP LNA under fixed biases condition for typical (TT) and corner cases (FF, SS). V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V. V_{B1}=0.4V, and V_{B2}=0V.

RF CORNER	UNIT	TT	FF	SS
Process technology	nm	90	90	90
Frequency	GHz	1.4	1.4	1.4
V_{DD}	V	0.18	0.18	0.18
V_G	V	0.45	0.45	0.45
V_{G2}	V	0.80	0.80	0.80
V_{B1}	V	0.40	0.40	0.40
V_{B2}	V	0	0	0
Power dissipation	mW	**0.19**	**0.56**	**0.05**
Bias current	mA	1.06	3.11	0.26
Gain (S_{21})	dB	11.0	12.0	1.3
NF	dB	**2.1**	**1.8**	**4.2**
IIP3	dBm	-14.1	-17.8	-16.0
$P_{in,-1dB}$	dBm	-29.0	-31.0	-15.5
Input Return Loss (S_{11})	dB	-10.4	-12.9	-3.7
Output Return Loss (S_{22})	dB	-10.5	-5.3	-15.6
Reverse isolation (S_{12})	dB	-15.2	-18.5	-15.6

Table 4. 2 Post-layout simulation for ULP LNA under fixed biases condition for typical (TT) and corner cases (FF, SS). V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V. V_{B1}=0.4V, and V_{B2}=0V.

RF CORNER	UNIT	TT	FF	SS
Process technology	nm	90	90	90
Frequency	GHz	1.4	1.4	1.4
V_{DD}	V	0.18	0.18	0.18
V_G	V	0.45	0.45	0.45
V_{G2}	V	0.80	0.80	0.80
V_{B1}	V	0.40	0.40	0.40
V_{B2}	V	0	0	0
Power dissipation	mW	**0.19**	**0.54**	**0.05**
Bias current	mA	1.05	2.98	0.26
Gain (S_{21})	dB	10.3	11.3	1.1
NF	dB	**2.3**	**1.9**	**4.3**
IIP3	dBm	-13.3	-17.5	-16.0
$P_{in,-1dB}$	dBm	-28.0	-30.0	-28.0
Input Return Loss (S_{11})	dB	-12.1	-14.9	-4.2
Output Return Loss (S_{22})	dB	-10.6	-5.6	-18.1
Reverse isolation (S_{12})	dB	-15.6	-18.5	-15.7

Table 4. 3 Pre-layout simulation for ULP LNA under tunable biases condition for typical (TT) and corner cases (FF, SS).

RF CORNER	UNIT	TT	FF	SS
Process technology	nm	90	90	90
Frequency	GHz	1.4	1.4	1.4
V_{DD}	V	0.18	0.18	0.18
V_G	V	**0.45**	**0.38**	**0.52**
V_{G2}	V	**0.80**	**0.74**	**0.85**
V_{B1}	V	0.40	0.40	0.40
V_{B2}	V	0	0	0
Power dissipation	mW	**0.19**	**0.20**	**0.19**
Bias current	mA	1.06	1.09	1.03
Gain (S_{21})	dB	11.0	10.9	11.0
NF	dB	**2.1**	**2.1**	**2.1**
IIP3	dBm	-14.1	-14.2	-14.3
$P_{in,-1dB}$	dBm	-29.0	-29.0	-29.0
Input Return Loss (S_{11})	dB	-10.4	-9.3	-11.0
Output Return Loss (S_{22})	dB	-10.5	-10.8	-11.2
Reverse isolation (S_{12})	dB	-15.2	-14.3	-16.1

Table 4. 4 Post-layout simulation for ULP LNA under tunable biases condition for typical (TT) and corner cases (FF, SS).

RF CORNER	UNIT	TT	FF	SS
Process technology	nm	90	90	90
Frequency	GHz	1.4	1.4	1.4
V_{DD}	V	0.18	0.18	0.18
V_G	V	**0.45**	**0.38**	**0.52**
V_{G2}	V	**0.80**	**0.74**	**0.85**
V_{B1}	V	0.40	0.40	0.40
V_{B2}	V	0	0	0
Power dissipation	mW	**0.19**	**0.19**	**0.18**
Bias current	mA	1.05	1.07	1.01
Gain (S_{21})	dB	10.3	10.2	10.2
NF	dB	**2.3**	**2.3**	**2.3**
IIP3	dBm	-13.3	-13.4	-13.4
$P_{in,-1dB}$	dBm	-28.0	-28.0	-28.0
Input Return Loss (S_{11})	dB	-12.1	-11.0	-12.4
Output Return Loss (S_{22})	dB	-10.6	-10.9	-11.2
Reverse isolation (S_{12})	dB	-15.6	-14.8	-16.5

4.5 Measurement

4.5.1 Measurement Considerations

For this ULP LNA design, the test chip characterization will be performed through on-wafer measurement. To meet this purpose, the probing pads layout must follow the rule issued by NDL RF Lab. to match the RF probe station configuration. This LNA chip needs two 3-pin DC PGP probes and two RF GSG probes for on-wafer measurement. The measurement setup is shown in Fig. 4.9, where two DC PGP probes are located at the top and bottom, and two RF GSG probes are place at two sides, in parallel to each other. Note that the DC PGP probe is used to provide the DC supply voltages to the drain and biasing voltage to the gate.

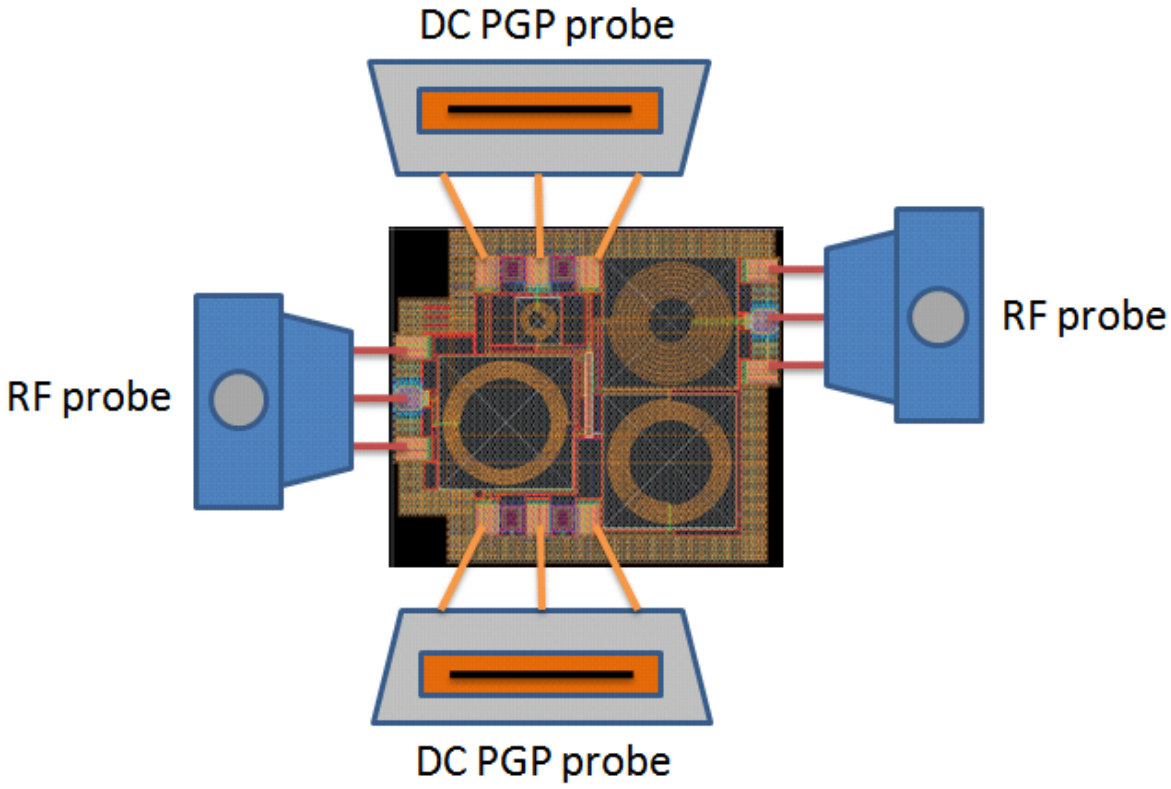
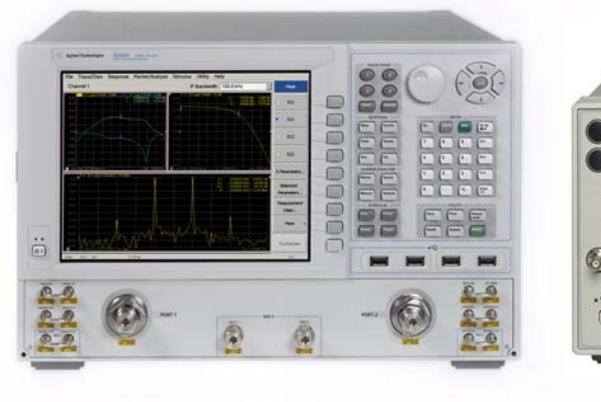
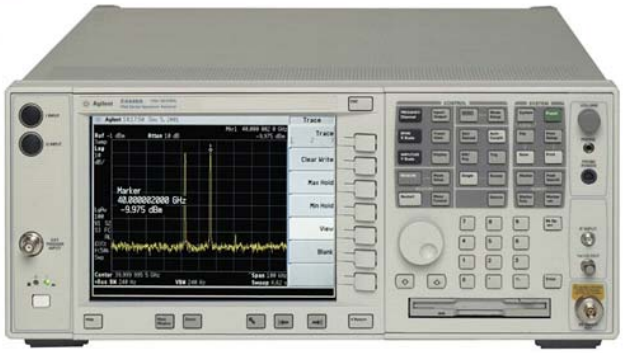


Fig. 4. 9 On-wafer measurement of LNA test diagram

The measurement equipments to support this LNA chip test include a network analyzer (Agilent PNA-X N5242A), a spectrum analyzer (Agilent E4448A) with options for NF measurement, and dc power supply (Agilent 6623A & Keithley Model 236 Source-Measure Unit). The measurement setups are shown in Fig.4.10(a) for S-parameter, IIP3, and 1-dB compression point (P1dB), and Fig.4.10(b) for noise figure. In the following, we will present the ULP LNA chip characterization results for the key performance parameters and a comparison with what predicted by post-layout simulation.



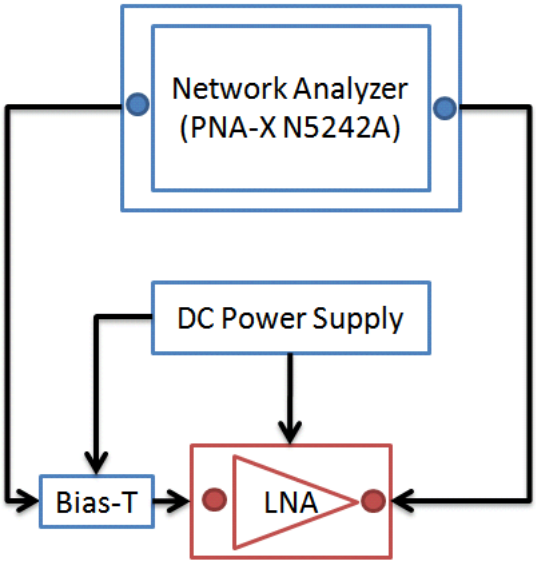
Agilent PNA-X N5242A



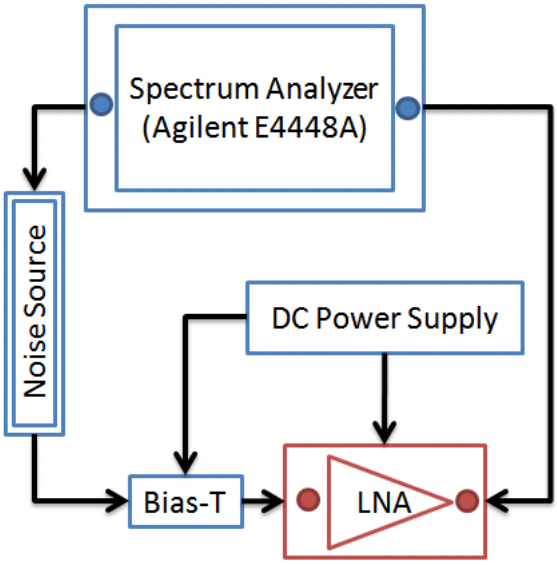
Agilent E4448A

Agilent 6623A

Keithley Model 236 Source-Measure Unit



(a)



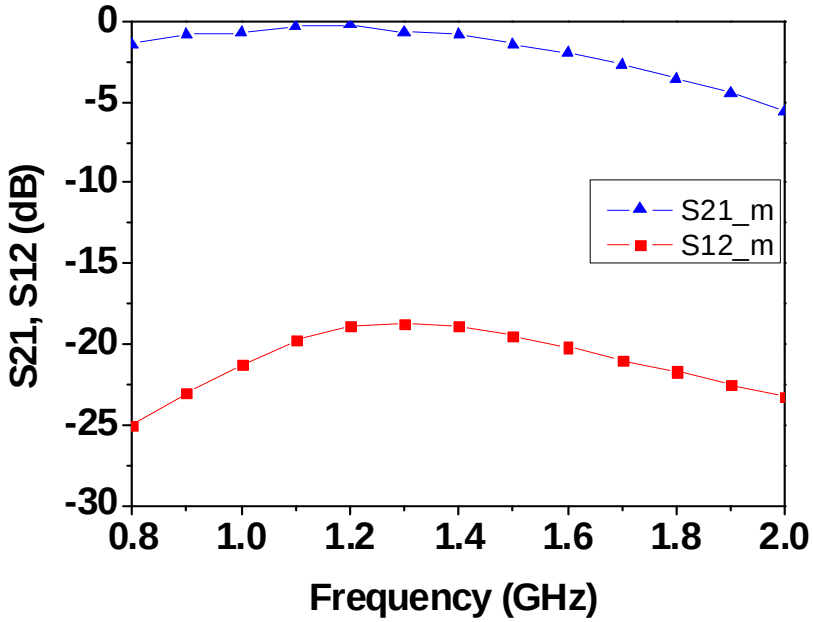
(b)

Fig. 4. 10 Measurement setups for (a) S-parameter & IIP3 & P1dB (b) noise figure

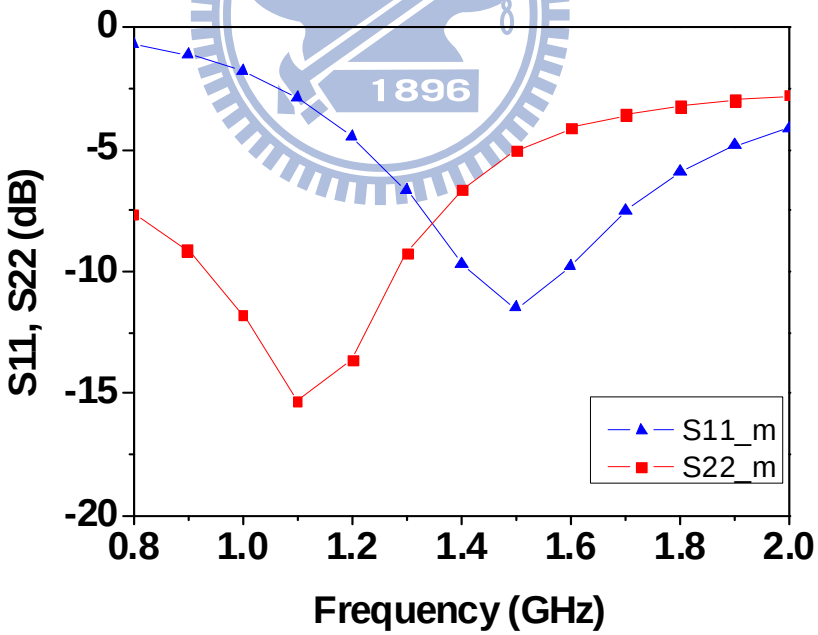
4.5.2 Measurement Results and Discussion

Fig. 4.11 presents the performance measured from this ULP LNA fabricated in 90nm 1.2V RF CMOS process. The results are demonstrated for power gain (S_{21}), input return loss (S_{11}), output return loss (S_{22}), reverse isolation (S_{12}), and noise figure (NF), shown in Fig. 4.11(a)~(c). As compared to post-layout simulation shown previously, the measured performance reveals a distinct difference from the prediction by simulation under ultra-low V_{DD} (0.18V) and V_G=0.45V to subthreshold region. The first problem is that the power gain (S_{21}) measured from the real chips under the specified biases is abnormally low. It was considered that the on-chip inductors performance may deviate from the ideal values predicted by simulation, assuming thick top metal (3.25μm). Thus, on-wafer S-parameters measurement was carried to explore the root causes responsible for this unexpected degradation. Table 4.5 makes a comparison between the measured and simulated characteristics and reveals a close match in inductance but distinct deviation in series resistance R_S=Re($1/Y_{11}$). The measured R_S is around 3~5 times larger than the simulated values for larger inductors with L=10~22 nH. The deviation becomes even worse to more than one order for the smallest inductor with L=0.8~0.9 nH. Through this analysis, it is identified that extra-ordinarily high R_S due to thin metal for the spiral conductors is the major reason responsible for inductor performance degradation like extremely low Q. To verify if the abnormal inductor performance drift is the primary reason responsible for the LNA performance degradation, the measured inductor S-parameters were imported to replace the original model for LNA simulation using ADS. The comparison as shown in Fig. 4.12 indicates a close match between the measurement and simulation using measured inductor parameters. The results match the theorectal analysis and suggest that that the power gain (S_{21}) measured from the real chips is abnormally low, due to poor inductors performance and the resulted severe deviation in input and output matching. The origin comes from the fact that

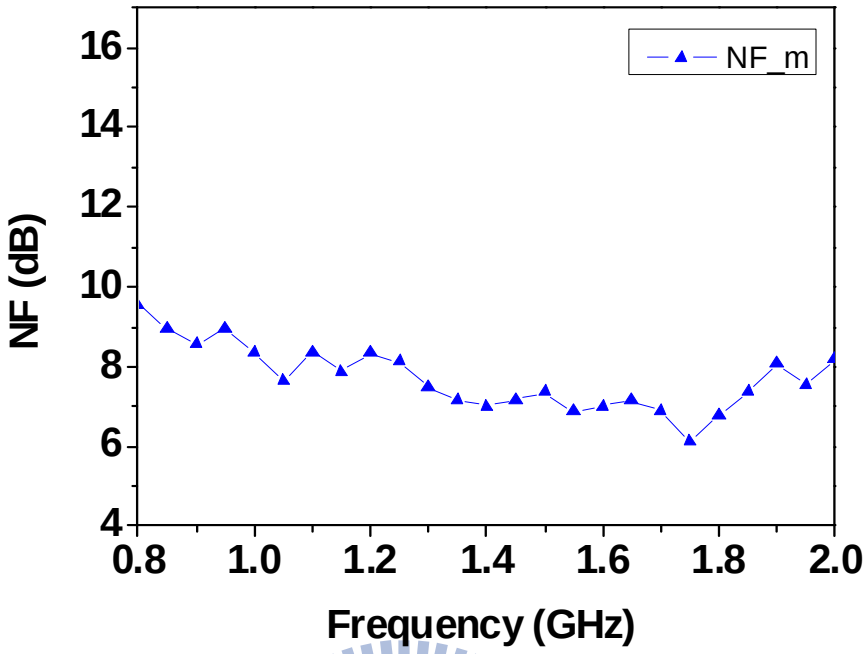
UMC 90nm Logic & Mixed-Mode 1P9M Low-K Process doesn't support the thick metal module for on-chip inductors. The thick metal required for on-chip spiral inductors is 3.25um but the thin metal supported by UMC 90nm standard logic process is 0.8um. The inappropriately thin metal is just the root cause responsible for the substantial increase of series resistance R_S and then Q degradation. A potential solution for improvement is increasing biases to modify input matching and to raise power gain. Fig. 4.13 demonstrates the LNA performance measured by increasing V_{DD} and V_G. When increasing V_{DD} to 0.5V and V_G to 0.55V, the problem of performance degradation can be solved and promisingly good results can be realized. The power gain (S_{21}) can reach 5.5 dB at 1.4GHz but power consumption increases to 1.75mW from 0.5V. S_{11} is –12.1dB, S_{22} is –14.8dB, and S_{12} is as low as –23.5 dB. Table 4.6 summarizes the measured LNA performance, under various biases. The results indicate that increasing V_{DD} and V_G can effectively improve power gain but paying the penalty of higher power dissipation. Finally, an extensive performance benchmark with the state-of-the-art techniques in latest publications [45, 47-50] has been done and summarized in Table 4.7. This benchmark indicates that our designed ULP LNA from simulation with thick metal inductors, demonstrates the advantages of lower power and lower NF under comparable gain. However, lacking thick metal inductors in current 90 nm process makes input and output matching difficult and leads to dramatic degradation of power gain. Increasing V_{DD} and V_G is can partially recover power gain but pay the penalty of increasing power consumption.


S21, S12 (dB)
0
-5
-10
-15
-20
-25
-30
0.8
1.0
1.2
1.4
1.6
1.8
2.0
Frequency (GHz)
S21_m
S12_m

(a)


S11, S22 (dB)
0
-5
-10
-15
-20
0.8
1.0
1.2
1.4
1.6
1.8
2.0
Frequency (GHz)
S11_m
S22_m

(b)

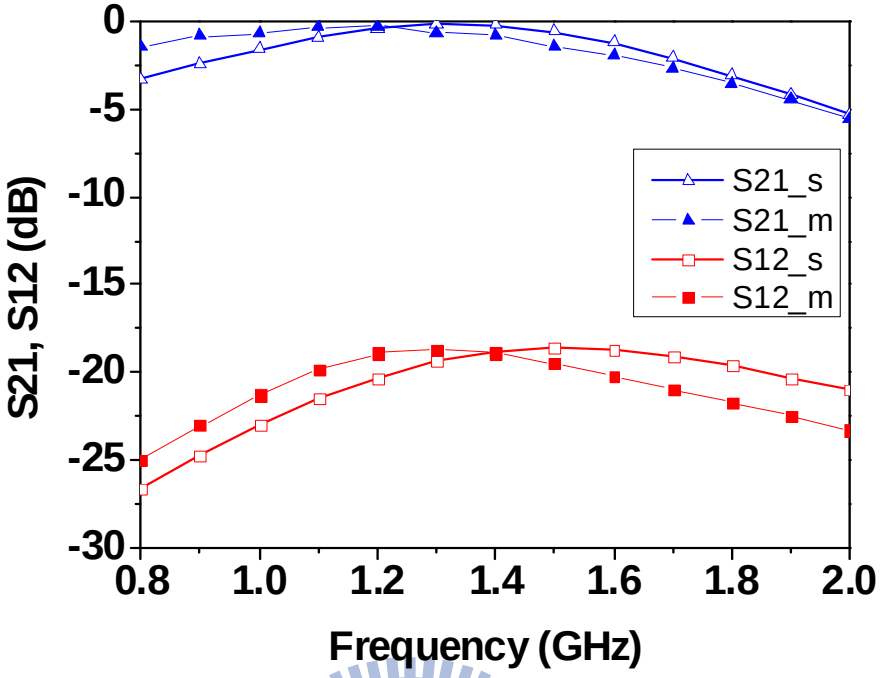


(c)

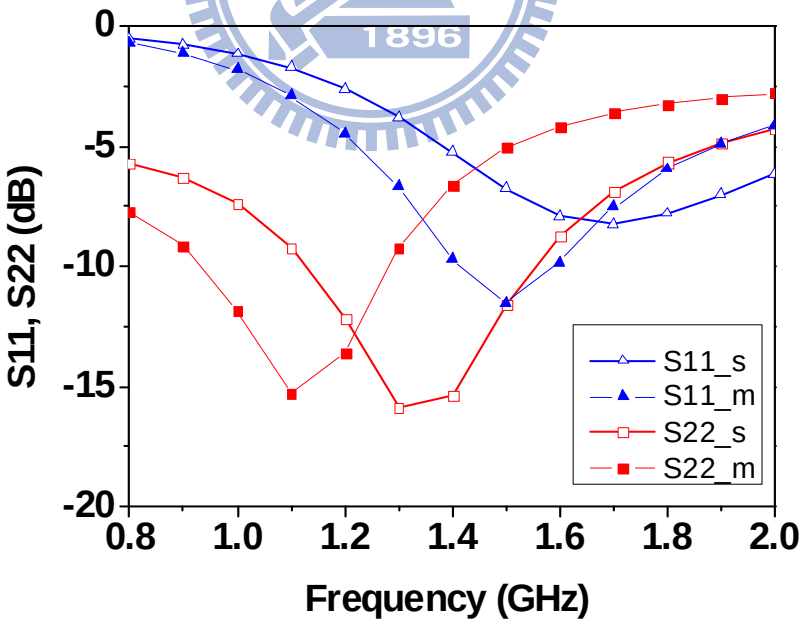
Fig. 4. 11 ULP LNA chip measured results for (a) power gain (S_{21}) and reverse isolation (S_{12}) (b) input return loss (S_{11}) and output return loss (S_{22}) (c) noise figure. V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V, V_{B1}=0.4V, and V_{B2}=0.

Table 4. 5 Spiral inductor characteristics measured from the test devices on a single chip with ULP LNA

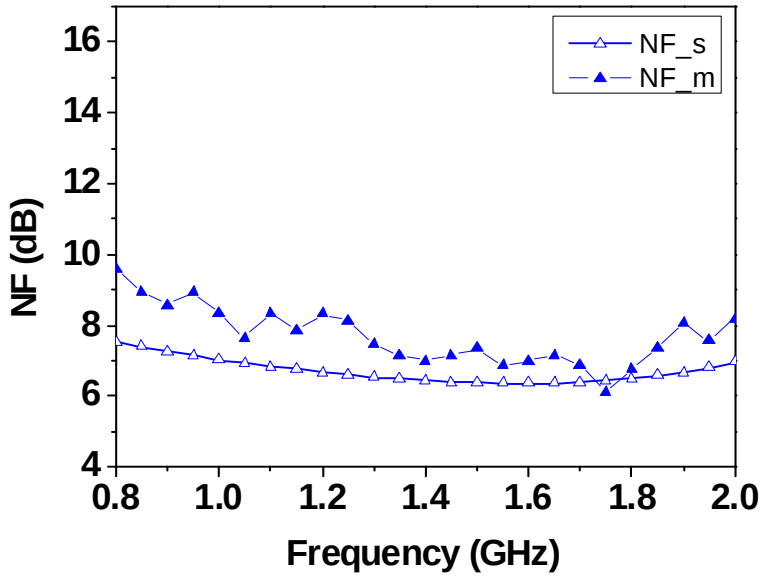
Lg		od=250um , w=2.2u , s=2.3um , nt=7.5			
	Metal thickness	L @1.4G	Q @1.4G	Qpeak	**Rs**=Re(1/Y_{11})@1.4G
Simulation	3.25um	22.6 nH	9.3	9.3	21.5
Measured	0.8um	20.8 nH	1.8	2.4	**100.7**
Ld		od=250um , w=3u , s=2.5um , nt=7.5			
	Metal thickness	L @1.4G	Q @1.4G	Qpeak	**Rs**=Re(1/Y_{11})@1.4G
Simulation	3.25um	20 nH	10.4	10.4	17
Measured	0.8um	18.6 nH	2.7	3.5	**60.4**
Lo		od=250um , w=8u , s=2.5um , nt=7.5			
	Metal thickness	L @1.4G	Q @1.4G	Qpeak	**Rs**=Re(1/Y_{11})@1.4G
Simulation	3.25um	10.5 nH	11.2	11.5	8.3
Measured	0.8um	10.2 nH	4.4	5.5	**20.2**
Ls		od=75um , w=3.5u , s=2.3um , nt=3.5			
	Metal thickness	L @1.4G	Q @1.4G	Qpeak	**Rs**=Re(1/Y_{11})@1.4G
Simulation	3.25um	0.8 nH	4.6	20.5	1.5
Measured	0.8um	0.9 nH	0.3	6.3	**24.3**


S21, S12 (dB)
Frequency (GHz)
S21_s
S21_m
S12_s
S12_m

(a)

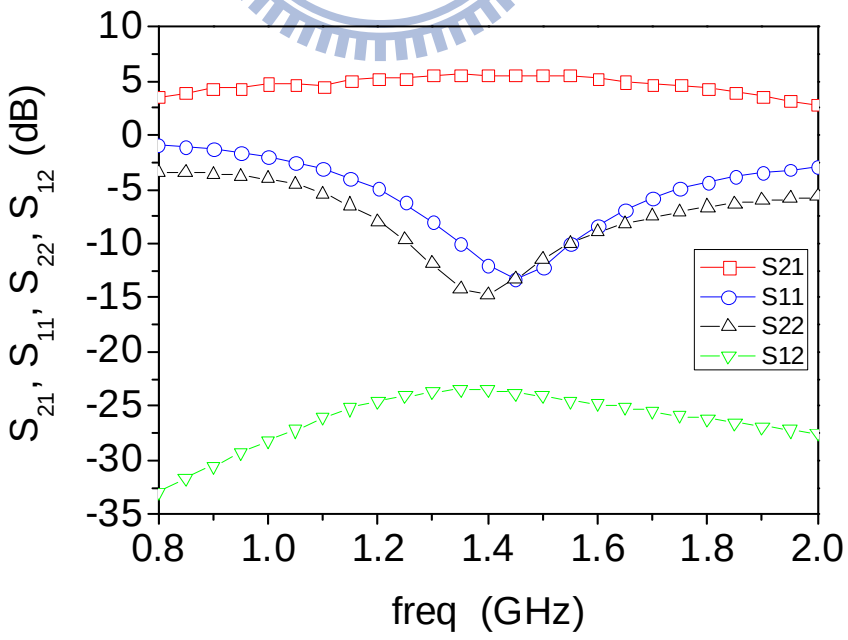

S11, S22 (dB)
Frequency (GHz)
S11_s
S11_m
S22_s
S22_m

(b)

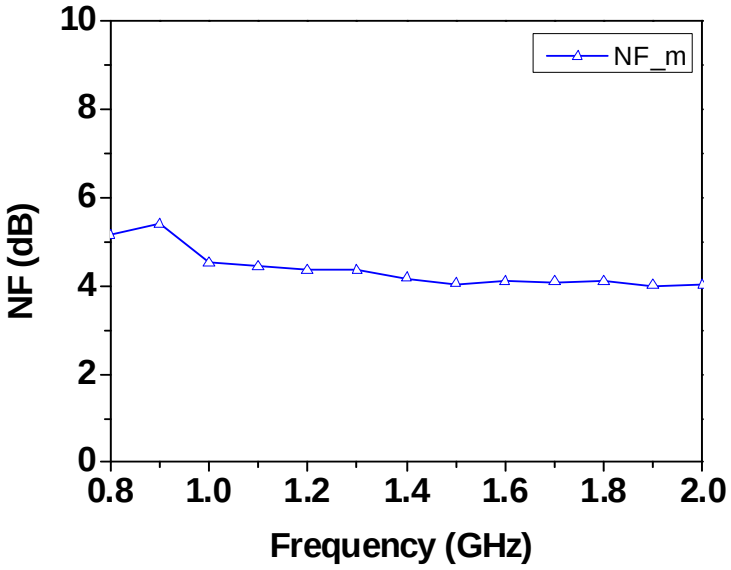


(c)

Fig. 4. 12 The comparison between measurement and ADS simulation by using measured inductor S-parameters, rather than inductor model (a) power gain (S_{21}) and reverse isolation (S_{21}) (b) input return loss (S_{11}), output return loss (S_{22}), (c) noise figure (NF). V_{DD}=0.18V, V_G=0.45V, V_{G2}=0.8V, V_{B1}=0.4V, and V_{B2}=0.



(a)



(b)

Fig. 4. 13 ULP LNA chip measured under raised V_{DD} to 0.5V (a) power gain (S_{21}) and reverse isolation (S_{12}), input return loss (S_{11}) and output return loss (S_{22}) (b) noise figure. **V_{DD}=0.5V, V_G=0.55V**, V_{G2}=0.8V.

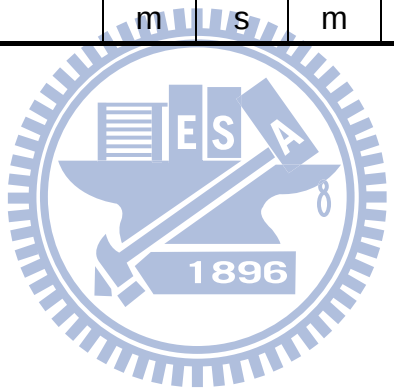
Table 4. 6 Simulated and measured performance for 1.4GHz LNA under varying V_{DD} and V_G

		Sim	Mea	Mea	Mea
VDD	V	0.18	0.18	**0.45**	**0.50**
VG	V	0.45	0.45	**0.55**	**0.55**
VG2	V	0.80	0.80	0.80	0.80
VB1	V	0.40	0.40	0.00	0.00
VB2	V	0.00	0.00	0.00	0.00

Power dissipation	mW	0.12	0.22	1.48	**1.75**
Supply Volatge (V_{DD})	V	0.18	0.18	0.45	0.50
Bias current	mA	0.66	1.2	3.28	3.50
Frequency	GHz	1.4	1.4	1.4	1.4
Gain (S_{21})	dB	-0.2	-0.8	4.7	**5.5**
NF	dB	6.4	7	4.1	4.1
Input Return Loss (S_{11})	dB	-5.2	-9.7	-12.1	-12.1
Output Return Loss (S_{22})	dB	-15.4	-6.6	-12.2	-14.8
Reverse isolation (S_{12})	dB	-18.8	-18.9	-22.6	-23.5

Table 4. 7 ULP LNA Performance Benchmark

		This LNA		Published LNAs					
Publication Ref.				[45]	[45]	[47]	[48]	[49]	[50]
Process technology	um	0.09	0.09	0.13	0.13	0.13	0.13	0.18	0.09
Power dissipation	mW	**1.75**	**0.19**	0.16	0.4	1.03	0.64	0.9	1
Supply Volatge (V_{DD})	V	0.50	0.18	0.6	0.6	0.4	0.4	0.6	0.6
Bias current	mA	3.50	1.05	0.26	0.67	2.58	1.6	1.5	1.67
Frequency	GHz	1.4	1.4	3	3	5.1	5	5	5.5
Gain (S_{21})	dB	**5.5**	**10.3**	4.5	9.1	10.3	14.3	9.2	9.2
NF	dB	4.1	**2.3**	6.3	4.7	5.3	2.93	4.5	3.6
IIP3	dBm	-8.0	-13.3	-10.5	-11	-	-16	-15	-7.25
$P_{in,-1dB}$	dBm	-17.0	-28.0	-19.5	-25	-22	-26.7	-27	-15.8
Input Return Loss (S_{11})	dB	-12.1	-12.1	-17.7	-17.7	-17.7	-20	-12	-10
Output Return Loss (S_{22})	dB	-14.8	-10.6	-11.4	-11.4	-11.4	-31	-20.9	-14
measure/simulate		m	s	m	m	m	s	m	m



Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis includes two topics. One is UWB low-power LNA, and the other is sub-0.2mW ultra-low power (ULP) LNA. The first topic have demonstrated a low-power approach for the design of UWB LNA in the 3.1~10.6GHz band. The design employs a three-section reactive input network to realize the UWB matching and FBB scheme in the cascade amplifying stage for achieving low supply voltage to V_{DD}=0.9V and gate bias to subthreshold region of V_G=0.4V. The effectiveness of our approach has been proven by experiments carried out on LNA test chip fabricated in 0.13um RF CMOS technology. The power consumption can be reduced to 8.4 mW for a whole chip operating over ultra-wide band of frequencies in 3.1~ 10.6 GHz.

The second topic presents an ultra-low power (ULP) LNA), which was fabricated using 90nm low leakage (LL) CMOS process and applied with forward body biases (FBB). The adoption of FBB scheme in the transconductance stage MOSFET enables ultra-low supply voltage to V_{DD}=0.18V and gate bias to subthreshold region, that is V_G=0.45V. The aggressive voltages scaling driven by FBB can effectively push the chip power consumption to extremely low, such as sub-0.2 mW. Unfortunately, the power gain (S_{21}) measured from the real chips under 0.18V is abnormally low, due to poor inductors performance and the resulted severe deviation in input and output matching. In Chapter 4, we have demonstrated that the abnormally large series resistance R_S appearing in the on-chip inductors lacking thick metal is the primary factor responsible the performance degradation in this LNA. The origin comes from the fact that UMC 90nm logic and mixed-Mode process doesn't support the thick top metal module for on-chip inductors. The standard top metal offered by UMC 90nm logic

process is 0.8um, which is much thinner than that required for on-chip spiral inductors, that is 3.25um. The inappropriately thin metal is just the root cause responsible for the substantial increase of R_S and then Q degradation. Thus, if we want to meet the target performance, we are forced to increase the supply voltage and then the power consumption. In this study, we learn that on-chip inductors with sufficient Q play a key role in input and output matching, and determined the LNA performance in terms of gain, power, and noise. In future work, new matching methods without resort to area consuming and cost added spiral inductors become one of interesting topics. Active inductors may be an appropriate candidate for achieving the desired performance with small chip area and without need for RF specific back-end process. In summary, the fabricated UWB and ULP LNAs proven on Si chip may become candidates for 3.1~10.6GHz wireless system applications and wireless sensor networks, respectively.

5.2 Future Work

The achievements realized in this thesis, such as low-power UWB and ULP single-chip LNA justify the proposed circuit topologies and low power RF circuit design methods. More importantly, several challenging issues arising from in this thesis become interesting topics worthy of continuous research effort in the future work.

In the following, the research topics of most critical importance are remarked for future effort. The first topic is regarding a broadband matching method with the bandwidth extended beyond the conventional UWB (3.1~10.6 GHz) to millimeter (mm) wave regime. The second topic is with a special focus on broadband matching methods for simultaneous optimization of power gain and noise. The third challenging topic is developing noise shielding methods for mm-wave chip, targeting ultra-low power and low noise. The fourth topic of interest is novel matching circuits without need of inductors for chip area saving and cost reduction, due to full compatibility with standard logic process. The final one is the extended applications of FBB

technique in RF front-end circuits like mixers and VCOs for realizing an ULP single-chip RF front-end.

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