Chapter 1
Introduction

1.1 Overview

In recent years, complementary metal-oxide-semiconductor (CMOS) memory technology which driven by the more and more increasing demand for computer, mobile phones, personal digital assistant (PDA) , and some electronic consumer products, have developed rapidly for the need in the people's life.

We could divide memory into two main categories by whether the stored data would vanish when the power supply is switched off or not. One is volatile memory, the other is nonvolatile memory. Volatile memory, like DRAM and SRAM, would lose its information once when the power is turned off. On the other hand, nonvolatile memory could still retain the data even if the power supply is been removed. Therefore, we can use nonvolatile memory with lower power and it offers a higher density of data storage.

In 1967, *D. Kahng* and *S. M. Sze* invented the first floating-gate (FG) nonvolatile semiconductor memory at Bell Labs[1]. Nonvolatile memory, such as electrically-programmable read-only-memory (EPROM)[2], electrically erasable and programmable read-only-memory (EEPROM)[3], and nonvolatile random access memory (NVRAM), has been widely used in integrated circuits. Among the types of memories mentioned above, flash memory has the advantage of good program/erase (P/E) operation, small area, low operation voltage, low power consumption, and low cost. Also, it has a byte-selectable programming operation combined with a sector erasing at the same time. Therefore, it is extensively used in memory array, NAND and NOR. Nonvolatile semiconductor memory plays an important role in memory applications for portable commercial devices.

The most popular and well-known commercial flash memory is Intel ETOX (EPROM Tunnel Oxide)[4], and its structure is shown in Figure 1.1 (a). The device is a Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) with a modified gate structure that has a control gate and a floating gate surrounded with a dielectric material such as SiO_2. The charge storage element is the isolated floating gate that disconnected from control gate to the channel. The ETOX is programmed when electrons are injected from channel to the floating gate by using Channel-Hot-Electron-Injection (CHEI) method[5], so the threshold voltage (Vt) of the device is increased. On the other hand, we erase the cell when the stored electrons have been removed from the floating gate to source by using Fowler-Nordheim (FN) tunneling or band-to-band hot hole (BTBHH) injection, and the threshold voltage of the cell is been restored to the original value. Figure 1.1 (b) depicts the mechanism of programming and erasing the ETOX cell, and Figure 1.2 shows the band diagram of P/E operations. The Vt difference between the programmed and erased states is known as “memory window”. Figure 1.3 shows the typical I-V curve for the erased ETOX cell combined with its Vt shift when the device is programmed. The memory state of the device can be determined by sensing the current when the control gate is biased in the range of the memory window.

However, the ETOX cell has several drawbacks. First, the tunnel oxide of the memory device has to be thick enough (8~10 nm) to maintain superior retention and endurance, but it also causes large operation voltage, high power consumption, slow P/E speed, and the most important, hard to be scaled. Second, since the polysilicon floating-gate is conductive, the total charges stored in the floating gate would be easily lost when the tunnel oxide has a single defect or has been damaged during P/E cycles, as illustrated in Figure 1.4. To overcome these disadvantages mentioned above, new memory structures, such as MNOS (Metal / Nitride / Oxide / Silicon)[6, 7],

SONOS (Silicon / Oxide / Nitride / Oxide / Silicon)[8, 9], and nanocrystal memory[10, 11] with discrete traps as the charge storage element, have been published as the promising candidate for the nonvolatile memory applications.

With the Semiconductor Technology shrinks to the nano scale, the quality of ultra-thin tunnel oxide (<3nm) has been extensively increased[12]. So, nitride-related discrete-traps memories, such as Metal Nitride Oxide Silicon (MNOS) and Polysilicon Oxide Nitride Oxide Silicon (SONOS), become more and more attractive in flash memory applications. However, it has been shown that in MNOS devices, some electrons stored in nitride layer would leak through the control gate. To solve the problem, someone introduces the blocking oxide between control gate and nitride layer. Therefore, the ONO (Oxide-Nitride-Oxide) gate dielectric stack has been invented to overcome the disadvantages, and SONOS memory shows greater retention and more efficient P/E operation than the MNOS devices. Figure 1.5 (a) shows the schematic of SONOS structure and its electron conduction path for P/E operations. When the control gate is biased positively, electrons in the inversion layer of the Si substrate would tunnel through the tunneling oxide to the nitride trapping layer. On the other hand, when the control gate is biased negatively, electrons trapped in the nitride layer would tunnel through the SiO_2 to the channel. However, even though the control gate has no bias, electrons trapped in the shallow trap level of the nitride layer would also tunnel to the control gate or channel even if they are blocked by the blocking oxide or tunneling oxide. The charge transport mechanism involves Fowler-Nordheim (FN) tunneling, direct tunneling, and Frenkel-Poole emissions[13], as depicted in Figure 1.5 (b). So far, SONOS memories have a huge market in the nonvolatile memory applications.

SONOS-type (Silicon-Oxide-Nitride-Oxide-Silicon) flash memory has recently been a promising candidate for the next-generation nonvolatile memory

applications[14]. High dielectric (High-k) materials could have an equal potential difference between floating gate and Si substrate for a greater physical thickness compared to SiO_2. The leakage current through the dielectric would be reduced and hence increases the scaling limit. Using high-k trapping layer could have a large memory window to distinguish the programmed state and the erased state distinctly due to the larger trap density. By using the high-k trapping layer, we could gain the advantages such as high P/E speed, low operation voltage, low power consumption, easy to fabricate, and better potential for scalability down to 70-nm node. Hafnium oxide (HfO_2) is considered to be the promising candidate for charge trapping layer for the SONOS-type flash memory instead of Si_3N_4[15]. The high-k film, HfO_2, is thought to have a better charge trapping characteristics than Si_3N_4 due to its higher density of trap states and deep trap energy level for a longer retention time[16]. Therefore, we could scale down the tunneling oxide to achieve faster P/E speed and develop multi-bit SONOS-type flash memory[17]. However, there are some obstacles for this type of memories. For SONOS-type memory, erase saturation[18] and vertical charge migration[19] are two major drawbacks. Therefore, nanocrystal memory has been invented to conquer the dilemma.

A basic structure for nanocrystal memory is shown in Figure 1.6 (a). The nanocrystals can store charge locally due to the insulator surrounded between each other and effectively prevents conduction paths between the adjacent dots, as shown in Figure 1.6 (b). Generally, nanocrystals are small clusters of atoms with size of 5 to 10 nm in diameter. We could effectively prevent charges leak from the nanocrystals to the control gate by limiting nanocrystal deposition to just one layer and adjusting the thickness of blocking oxide. Recently, Si and Ge nanocrystals have been investigated extensively. In 1995, *Tiwari et al.* first proposed a Si nanocrystal nonvolatile memory at IBM[20], and it shows fast P/E operation speed. In 2002, *W. K. Choi et al* has

published Ge nanocrystal memory[21]. Si and Ge nanocrystals can be fabricated by various techniques, including chemical vapor deposition[22], ion implantation[23], annealing of Si-rich oxide[24], thermal oxidation of SiGe[25], and aerosol nanocrystal formation[26]. Moreover, *S. Das et al* uses Ge nanocrystals embedded in HfO_2 to achieve better charge injection characteristics[27]. In 2002, Zengtao Liu et al proposed design optimization of the self-assembled metal nanocrystal memories with Au, Ag, and Pt materials[28, 29]. The nanocrystals are formed by depositing an ultra-thin metal layer on tunneling oxide and then annealing by rapid thermal annealing (RTA) system. Also, metal nanocrystals have advantages of higher density of states, stronger coupling with the channel, and great work function engineering to optimize the device performance over the semiconductor counterparts.

Flash memories (SONOS memory, SONOS-type memory, and nanocrystal memory) have a lot of applications in nonvolatile memory market due to their flexibility and high speed and density. They present single cell electrical program and block electrical erase. The low power and robust flash systems are suitable for many portable applications, such as cellular phones, digital camera, personal digital assistant, and compact smart cards. They even could replace the magnetic memory and RAMs (Random Access Memory) finally. Recently, consumer electronics evolve to higher and higher performance and multi-functional, the System-On-Chip (SOC) concept gains great attentions for ultra-large scale integration (ULSI) microelectronic devices. The concept is to integrate digital logic, memory, analog components, and signal processing on a single chip to increase system speed, density, and capability. However, many of the device modules have different materials and thermal budget, the development for a proper process recipe would have a great challenge.

1.2 Motivation

With the Semiconductor Technology goes on more and more prosperous, it is inevitably to scale down the tunneling oxide thickness in the nonvolatile memory devices. Although we could get benefits of lower power consumption and higher P/E operation, the device reliability degrades at the same time. For the ultra-thin oxide (Tox < 3 nm), the SILC becomes significant and defects generated by P/E cycles play an important role in retention of the memory devices[30]. Therefore, it is a crucial point to deal with the dilemma.

In this thesis, we utilize the properties of oxygen vacancies generated by forming gas annealing (FGA) of HfO_2 thin film and nanocrystal memory capacitors. As a result, we could get a large memory window extracted from the capacitance-voltage (CV) hysteresis. Further, we could take advantage of the capacitance's structure to realize the memory device to get a sufficiently large memory window. Moreover, in order to maintain both high program/erase speed and good retention issues of the memory device, we use the intrinsic nature of interface property of high-k material, such as HfO_2 and Al_2O_3, contacts with SiO_2 to form electric dipole in the SONOS-type nonvolatile memory. According to the band structure, we get a faster programming operation but slower erasing speed combined with a sufficiently good retention. According to the mentioned above, we solve the dilemma of performance and reliability of flash memory devices and makes the balance of it.

1.3 Thesis Organization

We propose a novel, simple, reproducible, and reliable SONOS-type nonvolatile memory structure with a thin high-k layer, called dipole layer, in between the tunneling oxide and the trapping nitride to get high speed programming operation

combined with good retention. In chapter 2, we study the forming gas annealing (FGA) temperature on theAl_2O_3, and HfO_2 thin film and nanocrystal memory capacitors to enlarge the memory window. The HfO_2 nanocrystal is formed from phase separation of HfSiOx thin film by rapid thermal annealing (RTA). In chapter 3, we use an ultra-thin Al_2O_3 layer to form a dipole layer in the SONOS-type memory capacitor. We use silicon nitride (Si_3N_4), hafnium oxide (HfO_2), and HfO_2 nanocrystal as our trapping layer. The Al_2O_3 layer is located between tunneling oxide and trapping layer, trapping layer and blocking oxide, or both of it. Moreover, we use the results of chapter 2 to subject our memory capacitor with dipole layer to forming gas anneal to get a large memory window. In chapter 4, we successfully fabricate a novel SONOS-type nonvolatile memory with a modified gate structure inserting an ultra-thin high-k layer (HfO_2 or Al_2O_3) between tunneling oxide and Si_3N_4. We get an improved performance with a faster programming speed although lower erasing speed, and good retention. Conclusions follow in chapter 5.

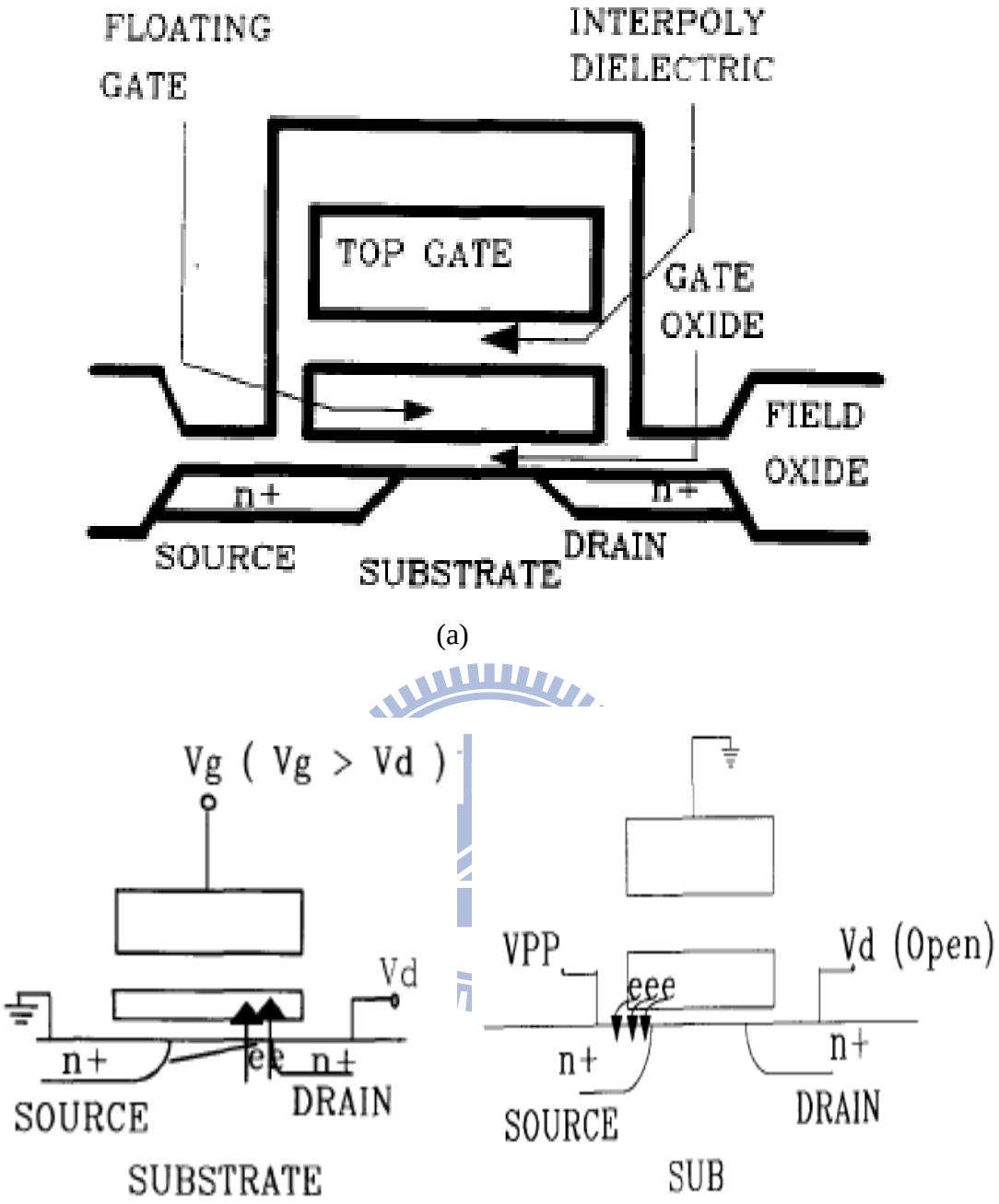


Fig. 1.1 (a)Schematic of a basic ETOX flash memory device[5]. (b) Mechanism of programming by CHE injection and erasing by FN tunneling[5].

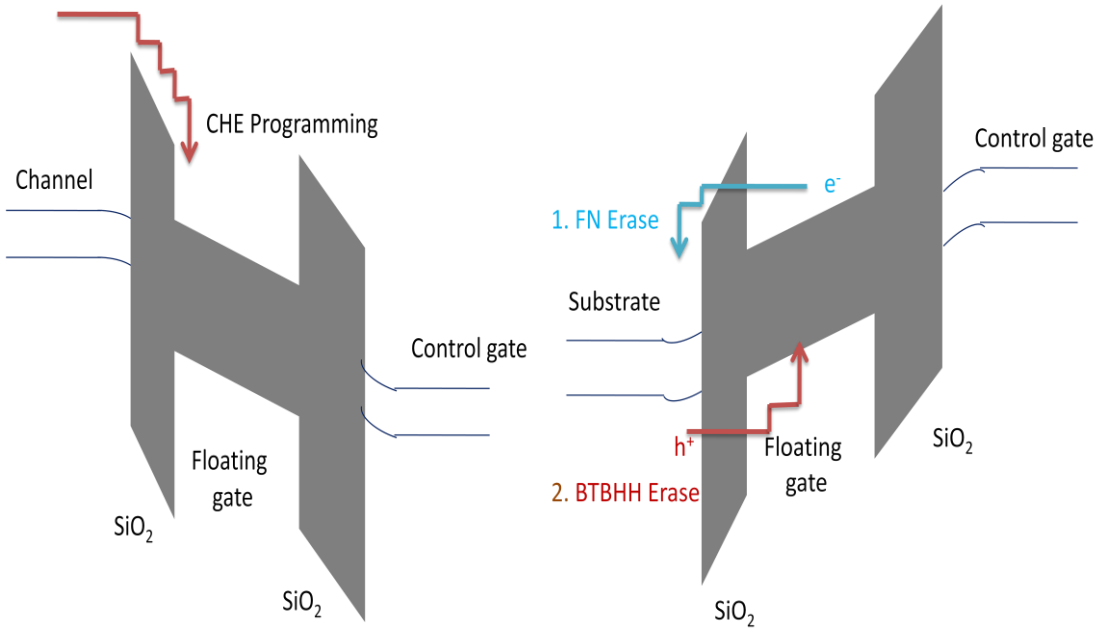


Fig. 1.2 Band diagrams of program and erase the ETOX device. Electrons flow during programming by CHE injection. Electron or hole flow during erasing by FN tunneling or BTBHH injection.

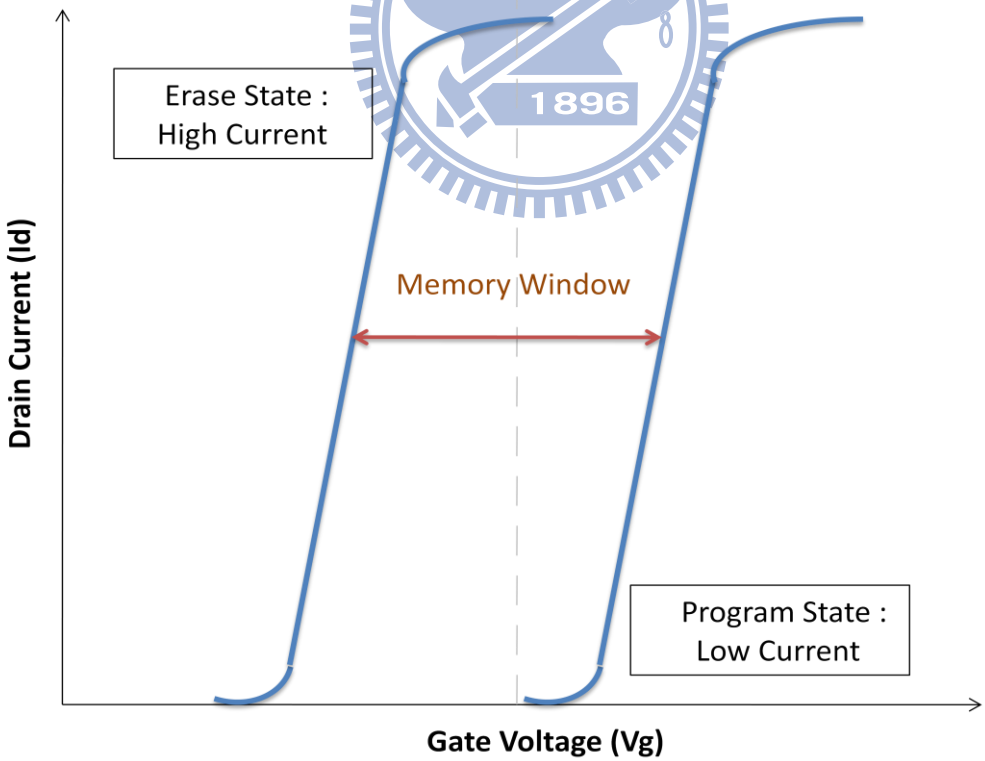
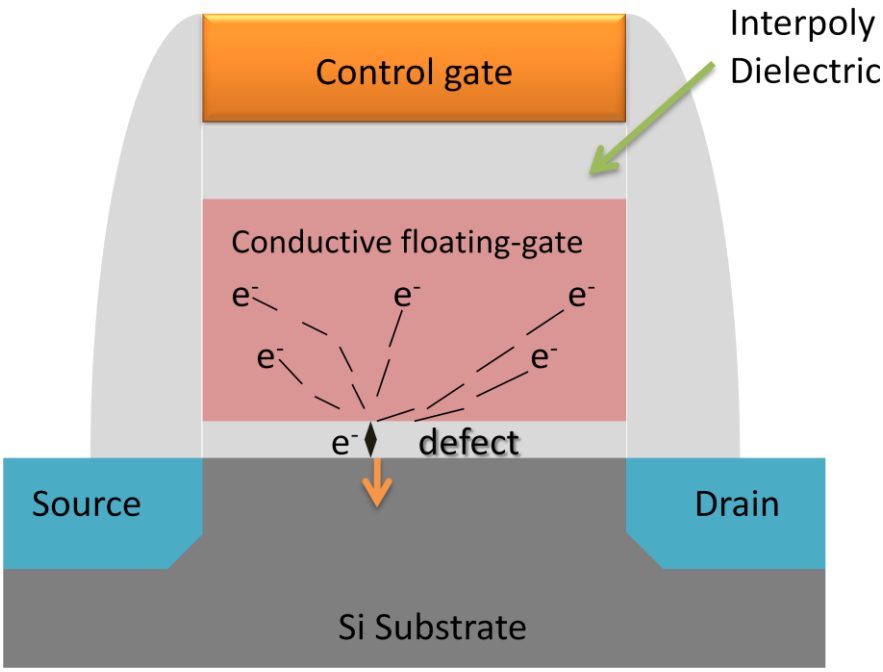
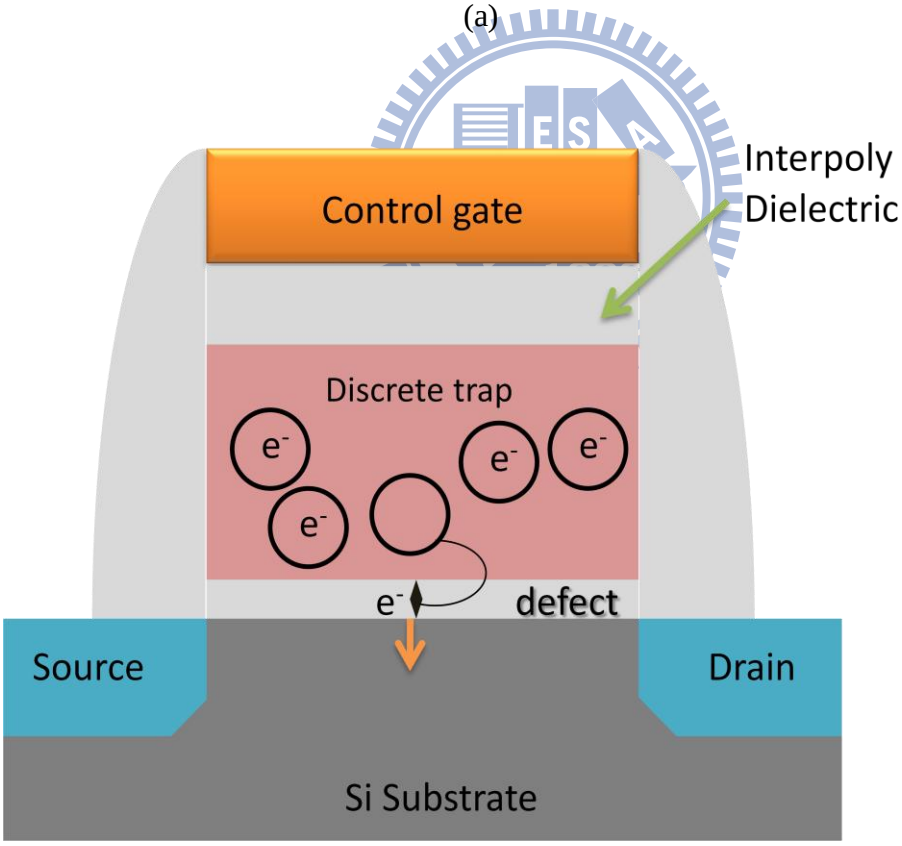


Fig. 1.3 Current-Voltage characteristics of a memory device in the programmed state and erased state display the Vth shift and memory window.

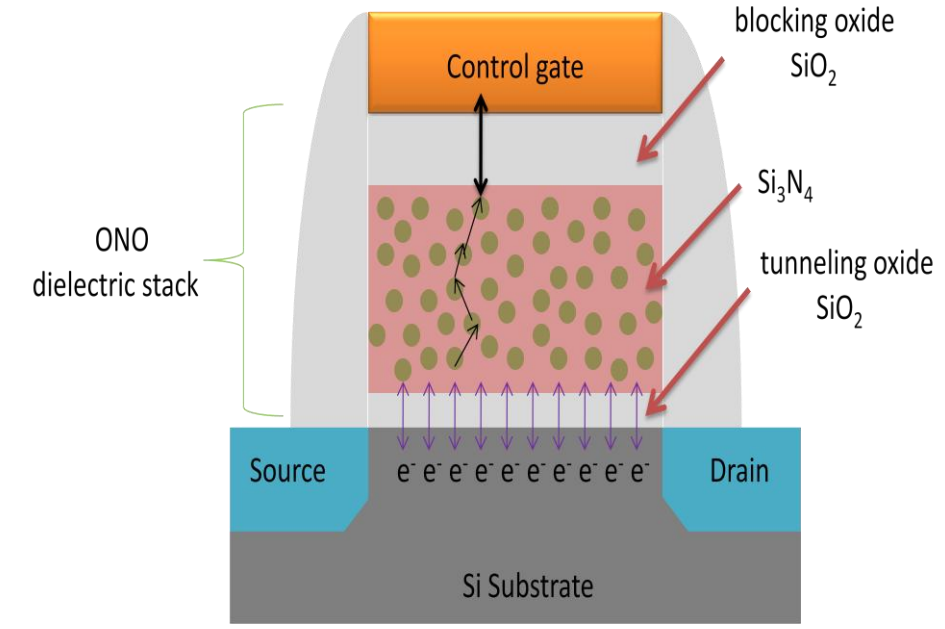


(a)

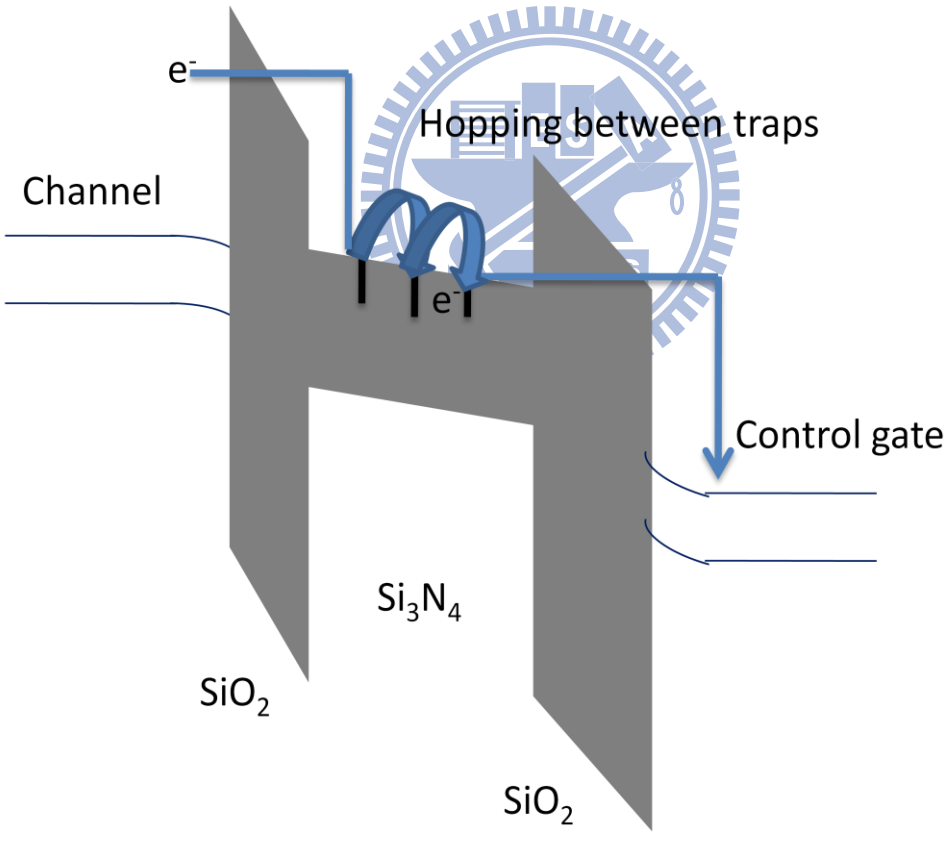


(b)

Fig. 1.4 (a)A schematic of a continuous FG structure showing that all the charges would leak through a single defect in the dielectric. (b) Charges stored in isolated storage nodes in the dielectric.

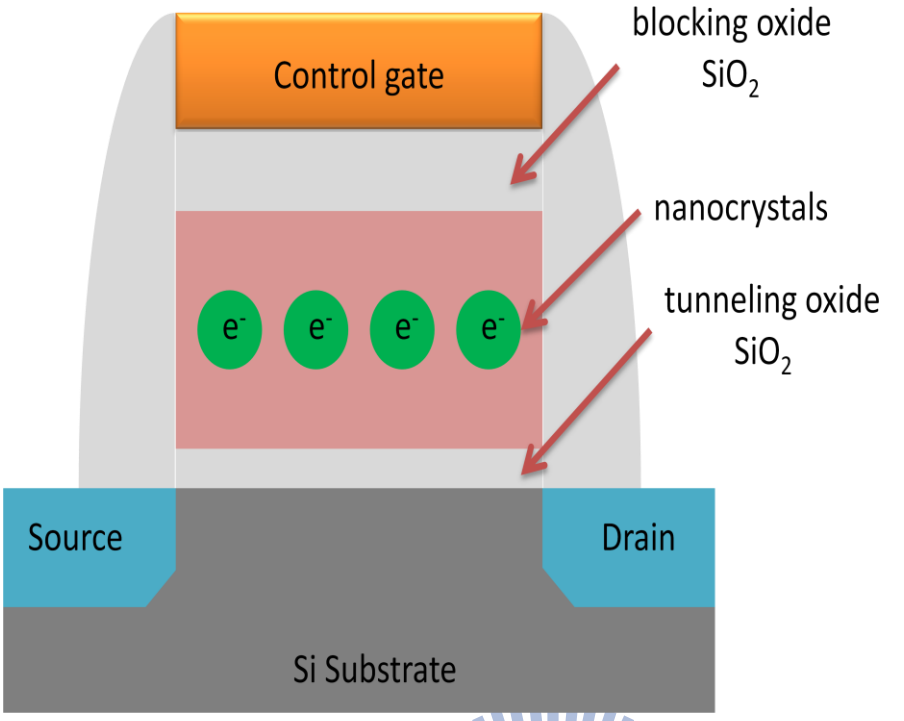


(a)



(b)

Fig 1.5 (a)Basic SONOS memory device structure. Arrows show paths of electron transport during memory operation. Electrons hop between traps. (b) Band diagram illustrating the physical process of SONOS programming operation sites within Si_3N_4 film.



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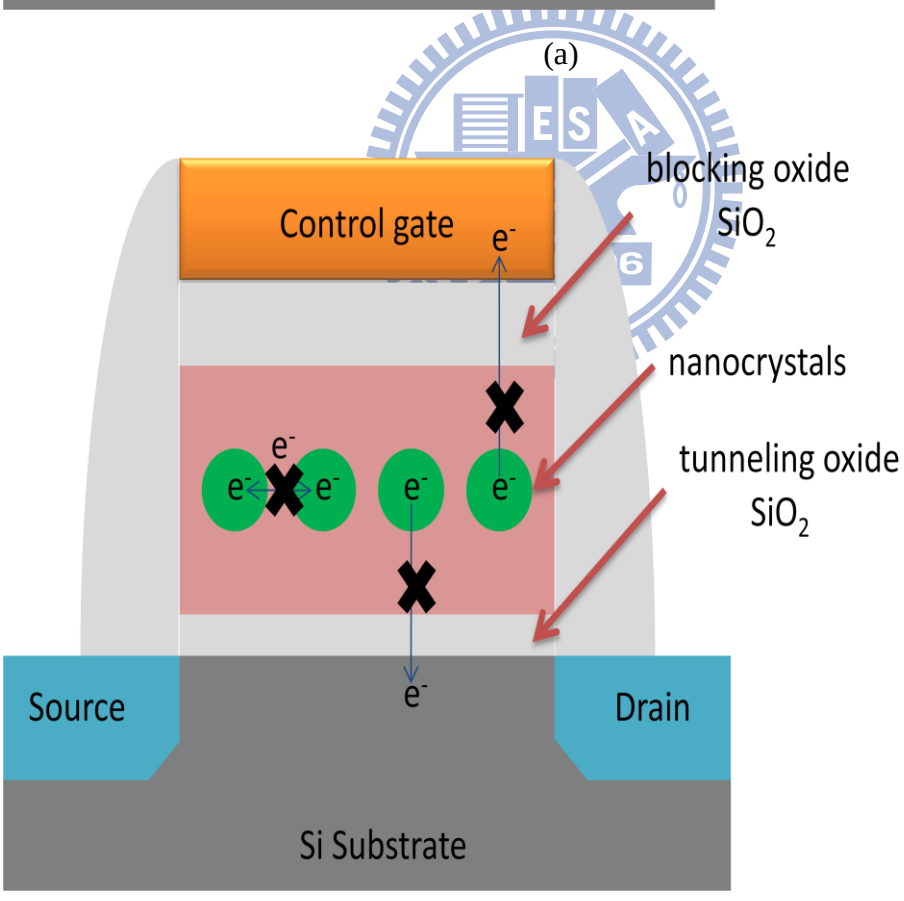


(b)

Fig. 1.6 (a)A schematic of nanocrystal memory. (b) The nanocrystal memory can store charge locally due to the well isolation of the adjacent nodes and effectively prevents the formation of conductive paths between each nanocrystals.

Chapter 2
Effects of Oxygen Vacancies on HfO_2 Thin Film and Nanocrystal Memory Capacitors

2.1 Introduction

SONOS-type (PolySi-Oxide-Nitride-Oxide-Silicon) nonvolatile flash memories, which include nitride and nanocrystal memories, have recently attracted much attention for their application in the next-generation nonvolatile memories. They exhibits many advantages, such as easy to fabricate, high program/erase speed, low programming voltage and low power consumption, better potential for scalability below the 70-nm node, according to the International Technology Roadmap for Semiconductors (ITRS)[31-40]. Hafnium oxide (HfO_2) is considered to be a promising candidate for the charge trapping layer for the SONOS-type flash memory instead of Si_3N_4 film[41]. The high-k dielectric film, HfO_2, is expected to have better charge trapping characteristics than the conventional Si_3N_4 film for its sufficient density of trap states and deep trap energy level to achieve longer retention time[42]. This feature makes HfO_2 be more helpful in scaling the tunnel oxide thickness to enhance the performance and more suitable for the development of the SONOS-type flash memory[43]. However, using HfO_2 film has a problem of lateral migration of trapped electrons and then leads to degraded retention[16].

In this chapter, we adopt forming gas annealing (FGA) on the high-k (HfO_2 and Al_2O_3) thin film and HfO_2 nanocrystal memory capacitor to generate oxygen vacancies. In 2006, *Kenji Shiraishi et al* reported that HfO_2 thin film could generate

oxygen vacancies due to the ionic nature of the Hf-O bond, and they calculate the position of the Vo (oxygen vacancy) level in the bandgap of the HfO_2, which is located at about 1.2eV below the HfO_2 conduction band edge[44, 45]. Figure 2.1 (a) an (b) shows the schematic illustration of Vo (oxygen vacancy) formation in ionic HfO_2 and covalent SiO_2. Assuming two reactions happen in the atmosphere, one reaction is the formation of Vo^0 in which two electrons are trapped, and the other is the formation of an empty Vo^{2+} and two conduction electrons:

$$\mathrm{HfO_2} \leftrightarrow \mathbf{Vo^0} + \frac{1}{2}\mathrm{O_2} - \Delta E_1 \quad \text{2-1}$$

$$\mathrm{HfO_2} \leftrightarrow \mathbf{Vo^{2+}} + 2\mathrm{e} + \frac{1}{2}\mathrm{O_2} - \Delta E_2 \quad \text{2-2}$$

ΔE_1 and ΔE_2 are the energies needed to form the oxygen vacancies in eq. (2-1) and (2-2), respectively. ΔE_2 is larger than ΔE_1 by approximately $2(\mathrm{Ec} - E(\mathbf{Vo^0}))$, where Ec is the energy level at the bottom of the HfO_2 conduction band. According to the mass action law, the Vo concentration governed by eq. (2-1) can be described by:

$$N(\mathbf{Vo^0}) \propto \exp(-\Delta E_1 / kT) \quad \text{2-3}$$

On the other hand, the relationship between Vo^{2+} and the electron concentration shown by eq. (2-2) can be expressed as:

$$N(\mathbf{Vo^{2+}}) \times N(e)^2 \propto \exp(-\Delta E_2 / kT) \quad \text{2-4}$$

Also, by taking into account the following relationships $N(e) = 2N(\mathbf{Vo^{2+}})$ and $\Delta E_2 \fallingdotseq \Delta E_1 + 2(\mathrm{Ec} - E(\mathbf{Vo^0}))$, eq. (2-4) becomes

$$N(\mathbf{Vo^{2+}}) \propto \exp\left[-\left\{\Delta E_1 + 2\left(\mathrm{Ec} - E(\mathbf{Vo^0})\right)\right\}/3kT\right] \quad \text{2-5}$$

Therefore, the effective formation energies of Vo in eq. (2-1) and (2-2) are ΔE_1 and

$\{\Delta E_1 + 2(\mathrm{Ec} - E(\mathbf{Vo}^0))\}/3$, respectively. If $\mathrm{Ec} - E(\mathbf{Vo}^0) < \Delta E_1$, eq. (2-2) dominants. On the other hand, if $\mathrm{Ec} - E(\mathbf{Vo}^0) > \Delta E_1$, eq. (2-1) is the major reaction[44].

In 2004, *W. L. Scopel et al* uses *ab initio* calculations to determine Vo^0 formation energy is about 6.4eV for HfO_2 and 5.2eV for SiO_2[46]. Also in 2004, *Hideki Takeuchi et al* utilize spectroscopic ellipsometry to show the energy level of Vo is about 1.2eV below the HfO_2 conduction band edge[45]. Thus, eq. (2-2) is the dominate reaction in the formation of Vo in HfO_2, and Vo^{2+} and two conduction electron generation occurs. The estimated effective Vo formation energy is about 2.9eV in HfO_2 and 5.2eV in SiO_2.

Actually, effects of oxygen vacancies on the performance of the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) have been widely studied in recent years[47-52]. In 2004, *Hideki Takeuchi et al* reported the impact of oxygen vacancies on the high-k film and that it causes Vth instability at UC Berkeley[53]. In 2008, *Hokyung Park et al* reported that oxygen annealing can effectively reduce gate leakage current in HfO_2 capacitor, indicating that oxygen vacancy can be a major source of the traps in HfO_2 films[54]. In 2007, *Y. Kamimuta et al* published that high-k films can generate oxygen vacancies by forming gas annealing (FGA)[55]. Since one oxygen vacancy represents one electronic state in HfO_2 bandgap, the generated oxygen vacancy seems to be beneficial to enlarge the memory window in flash memory applications. In this chapter, we fabricate high-k thin film and HfO_2 nanocrystal memory capacitor and study CV hysteresis dependence on FGA temperature.

2.2 Experiment

High-k thin film memory capacitor is realized on a p-type, 5-10 Ω cm, (100) 150-mm silicon substrate. After RCA clean, a 2.5nm tunnel oxide is grown in horizontal furnace. Next, a 12nm high-k (HfO_2 or Al_2O_3) trapping layer is deposited by MOCVD. Then, we subject the samples in FGA (95%N_2+5%H_2) for 300°C, 350°C, 400°C, 450°C, 500°C, 550°C, and 600°C, respectively. And a 7nm blocking oxide is deposited by PECVD. We use special shadow mask to define the upper electrode, and the area is about $4x10^{-4}$ cm^2. Finally, we plate Al on the back of the wafer by thermal coater for backside contact, as shown in figure 2.2 (a). For HfO_2 nanocrystal memory capacitor, after a 2.5nm tunnel oxide is grown, a 12nm amorphous HfSiOx silicate layer is deposited by MOCVD. The samples are then subjected to RTA treatment in an O_2 ambient at 950°C for 1min to convert the HfSiOx silicate film into the separated HfO_2 and SiO_2 phases. Then, 7nm PECVD oxide, and the following process is the same as the high-k thin film memory capacitors. Figure 2.2 (b) depicts the schematic of the HfO_2 nanocrystal memory capacitors.

2.3 Results and Discussions

2.3.1 High-k Thin Film Memory Capacitor

Figure 2.3 (a) and (b) shows cross-sectional transmission electron microscopy (TEM) of the HfO_2 and Al_2O_3 memory capacitors. Clearly, HfO_2 seems to be likely to crystallize due to the binding nature of the film[56]. Figure 2.4 (a) and (b) shows the Capacitance-Voltage (CV) characteristics of the HfO_2 thin film memory capacitors. Since the generated oxygen vacancy level is located at about 1.2eV below the HfO_2 conduction band edge, these near-interface traps can be detected by sweeping voltage to make capacitor be in the status of accumulation to inversion and back to

accumulation[45]. Thus we can detect CV hysteresis of the capacitor to approximately identify the trap density of the oxygen vacancies. We sweep voltages from -4V to 4V and back to -4V for the CV curve. Apparently, we can identify that FGA for 300^{o}C 30min can make the distinct hysteresis for HfO_2 memory capacitor from Figure 2.4 (a) and (b). Table 2.1 shows the CV hysteresis for HfO_2 memory capacitor extracted from the CV curve in Figure 2.4. The sample without FGA has a hysteresis of 0.66V. For FGA 300^{o}C 30min, we get largest hysteresis of 1.32V for HfO_2 memory capacitor. Also for 300^{o}C, 350^{o}C, 400^{o}C 30min FGA, the hysteresis measured is above 0.6V, which is comparably larger than the sample without FGA. When the temperature of FGA is higher than 450^{o}C, the hysteresis reduces to a value lower than the sample without FGA. We could attribute the higher hysteresis to the abundant oxygen vacancies generated by FGA[55]. However, the situation changed when we replace the trapping layer from HfO_2 to Al_2O_3. Figure 2.5 (a) and (b) shows the CV characteristics of the Al_2O_3 thin film memory capacitor. Clearly, from figure 2.5, the CV hysteresis of Al_2O_3 thin film memory capacitor for different FGA temperature from 300^{o}C to 600^{o}C is so small compared to HfO_2 memory capacitor. It seems to be related to the structure and binding characteristics of the Al_2O_3 film[57]. Table 2.2 shows CV hysteresis of Al_2O_3 memory capacitor extracted from figure. 2.5. From the table, the hysteresis of the capacitor is all below 0.1V for different FGA temperature except for 350^{o}C 30min case, which is 0.2V. Therefore, it is hard to generate oxygen vacancies by FGA in Al_2O_3 film[58]. So Al_2O_3 is more thermally stable and it is often used in blocking oxide in nonvolatile memory application to enhance programming speed[18, 59].

2.3.2 HfO_2 Nanocrystal Memory Capacitor

Figure 2.6 shows plane-view transmission electron microscopy (TEM) image of HfO_2 nanocrystal. The average nanocrystal diameter is 3-8 nm, and the density is as high as about $1.5x10^{12}$ cm^{-2}. In this image, the nanocrystal are well separated in different phases within the SiO_2, and the average distance is about 3-5nm. The isolation of nanocrystals prevents the formation of conductive paths between the adjacent nodes. The mechanism of forming HfO_2 nanocrystal is through the phase separation of hafnium silicate into a crystallized structure[60]. For hafnium silicate film, the compositions within metastable extensions of the spinodal are unstable and HfO_2 nanocrystal is formed and wrapped by SiO_2 after cooling down from RTA process. Also, we know that the ratio of hafnium and silicon must be in around 1:1 in HfSiOx film in order to form well-separated and uniform HfO_2 nanocrystals in SiO_2 matrix[11]. So we adopt different flow rate of hafnium and silicon of HfSiOx film in MOCVD, and X-ray photoelectron Spectroscopy (XPS) analysis is used to identify the ratio of elements in hafnium silicate film, as shown in figure 2.7. Table 2.3 shows the data extracted from figure. 2.7. Clearly, to get the ratio Hf:Si=1:1, the flow rate of hafnium and silicon must in between 5:1 and 10:1. We use flow rate Hf:Si=7:1 to deposit HfSiOx film in MOCVD system to make the ratio of hafnium and silicon nearly equals to 1:1 in composition. Therefore, we can generate well-separated, uniform, constant size, and high density HfO_2 nanocrystals, as shown in figure 2.6.

Figure 2.8 depicts CV characteristics of HfO_2 nanocrystal memory capacitor with different FGA temperature from 400^oC 30min to 600^oC 30min. We can see from the figure that for the case of 500^oC and 600^oC, the apparent hysteresis is shown. Table 2.4 shows the exact hysteresis of the HfO_2 nanocrystal memory capacitor. From the table, of all the different treatment, the CV hysteresis is not obvious enough to distinguish the logic “1” and logic “0” state, unless for the case of 500^oC 30min. For the 500^oC 30min case, the hysteresis is as large as 0.58V, which is mainly due to the

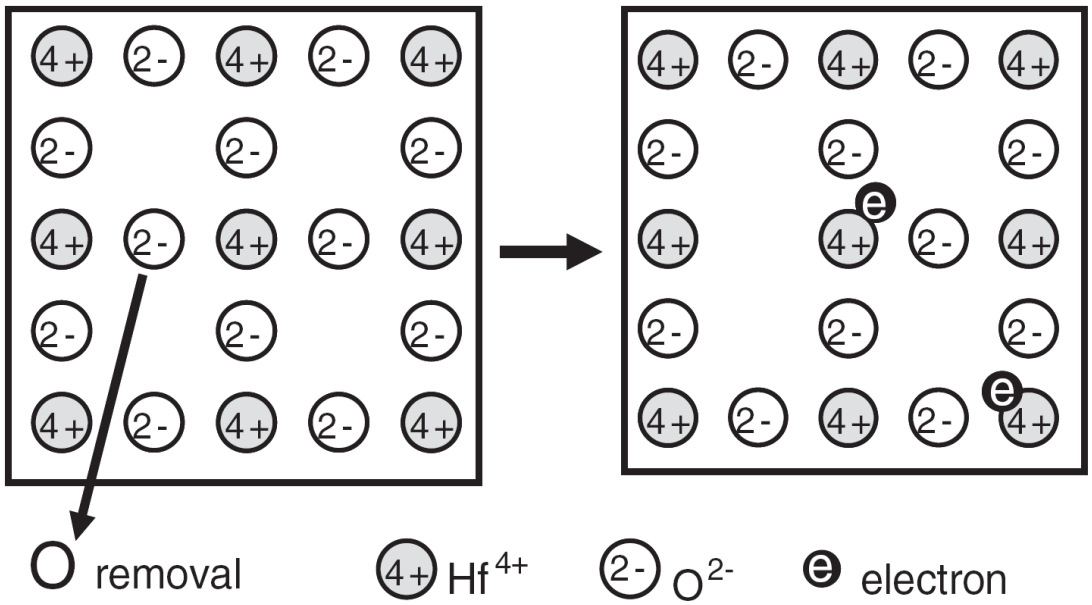
generated oxygen vacancies by FGA of 500°C 30min.

Next, in order to investigate the effect of FGA time on the performance of the capacitor, we subject the sample into FGA for a longer time. Figure 2.9 shows the XPS spectra of the HfO_2 nanocrystal memory capacitor for different FGA temperature. For 300°C, 400°C, 500°C, 600°C 1hour of FGA, the *Hf 4f* binding energy shifts towards the lower direction by 3.2eV, 3.3eV, 3.1eV, and 1.7eV, respectively. The lower binding energy indicates that after FGA, oxygen vacancy generation occurs, and a larger CV hysteresis is detected by electrical analysis. Figure 2.10 shows the CV characteristics of the HfO_2 nanocrystal memory capacitor with different FGA temperature for 1 hour. Surprisingly, the average hysteresis of all the different FGA temperature is larger than that of the 30min cases mentioned above. It would be due to the higher density of oxygen vacancies generated by a longer time of FGA. Table 2.5 lists the hysteresis extracted from the samples in figure 2.9. For 500°C 1hr case, the measured hysteresis is as high as 1.34V, which is twice of the 30 min case. Also for 400°C, 500°C, and 600°C cases, the hysteresis is at least higher than 0.65V. The ultra-high memory window is beneficial for the applications of SONOS-type nonvolatile memory.

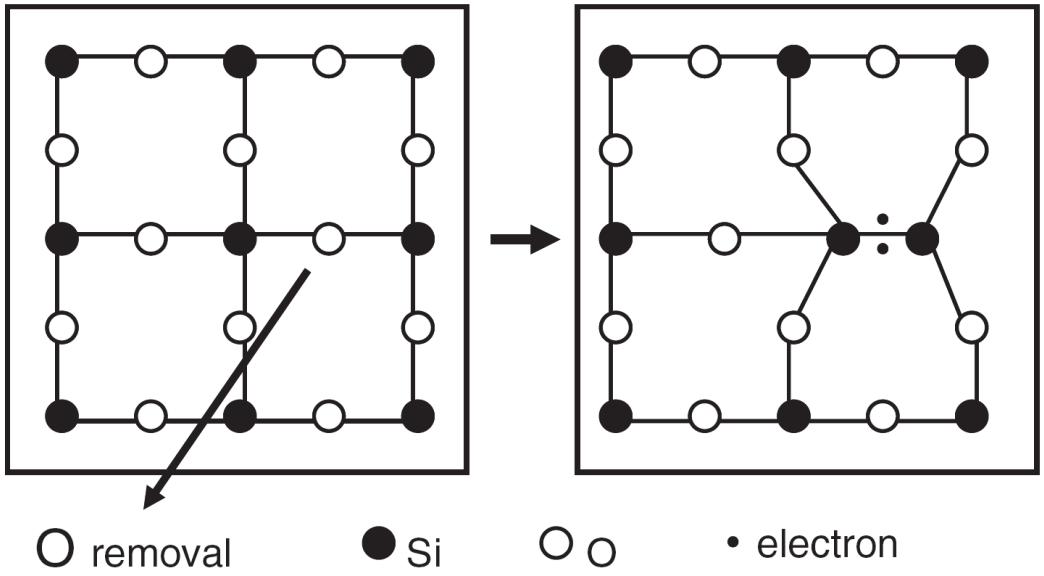
2.4 Summary

In this chapter, we demonstrate the effect of forming gas annealing (FGA) of different temperature on the CV characteristics of HfO_2 and Al_2O_3 thin film memory capacitor combined with HfO_2 nanocrystal capacitor. We identify that for FGA of 300°C 30min, HfO_2 thin film capacitor shows the largest hysteresis of 1.32V. However, for Al_2O_3 thin film capacitor, the effect of FGA is not obvious, and the higher hysteresis among different temperature is only about 0.2V in the case of 350°C

30min. Also, we use MOCVD system to deposit amorphous HfSiOx film, and we find out the most appropriate flow rate for hafnium silicate layer to convert to HfO_2 nanocrystal with uniform distributions and high density after RTA process. For the case of 500^{o}C 1hour, we get the largest CV hysteresis of 1.34V, slightly larger than HfO_2 thin film capacitor of the 300^{o}C 30min case. Therefore, utilizing HfO_2 thin film or nanocrystal trapping layer with suitable temperature of FGA, we can get a larger memory window in SONOS-type flash memory applications.

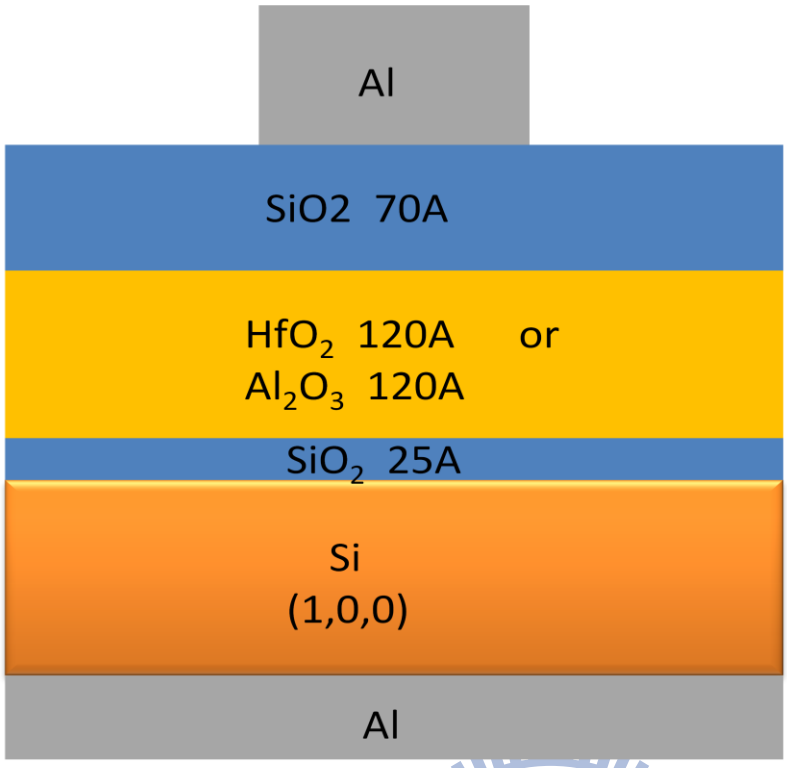


(a)

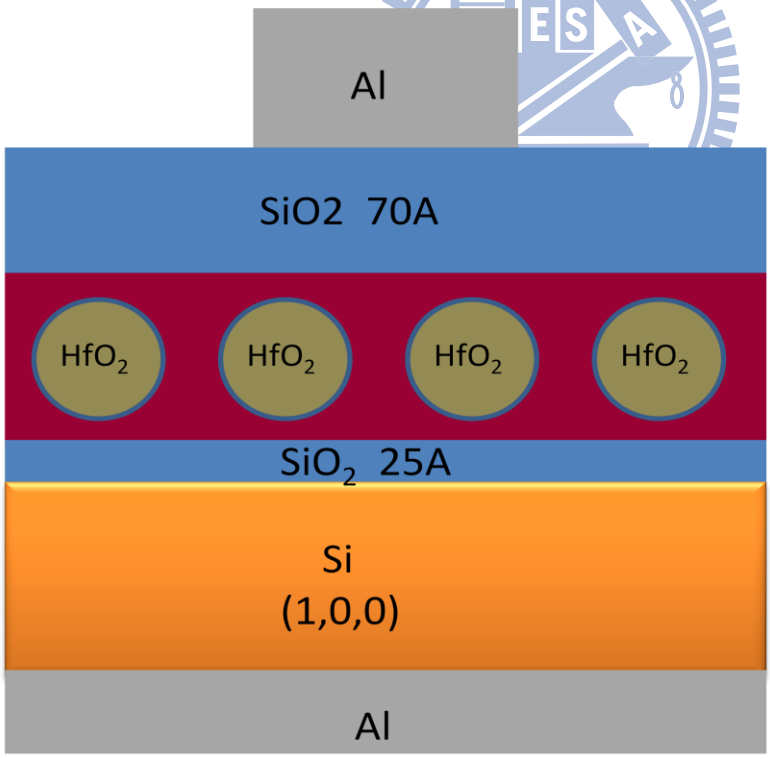


(b)

Fig. 2.1 (a)An illustration of Vo formation in ionic HfO_2. (b) A schematic of Vo formation in covalent SiO_2.

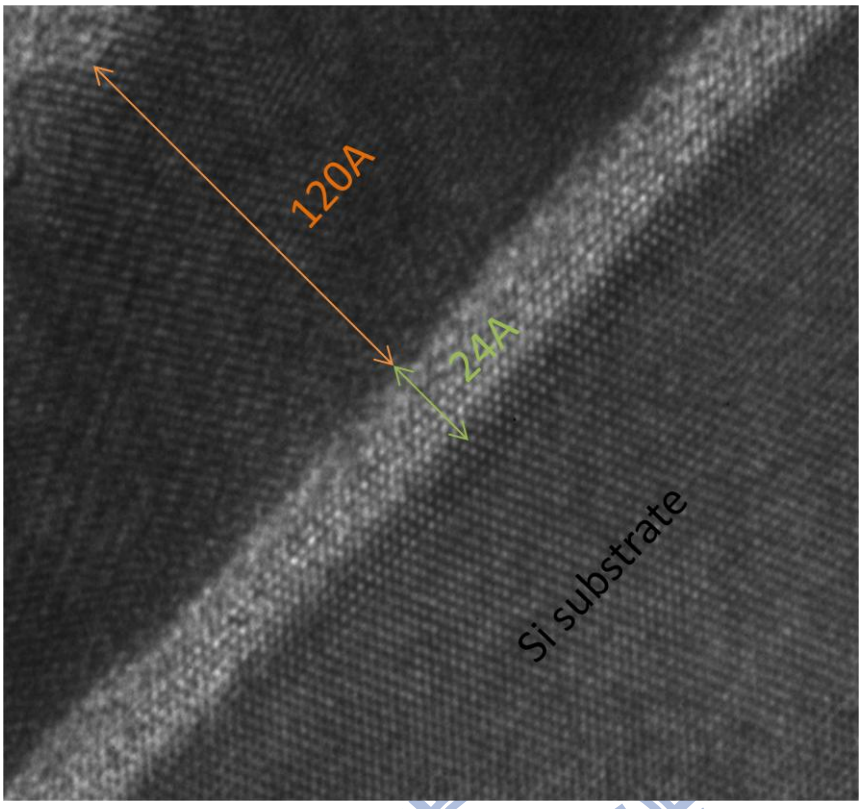


(a)

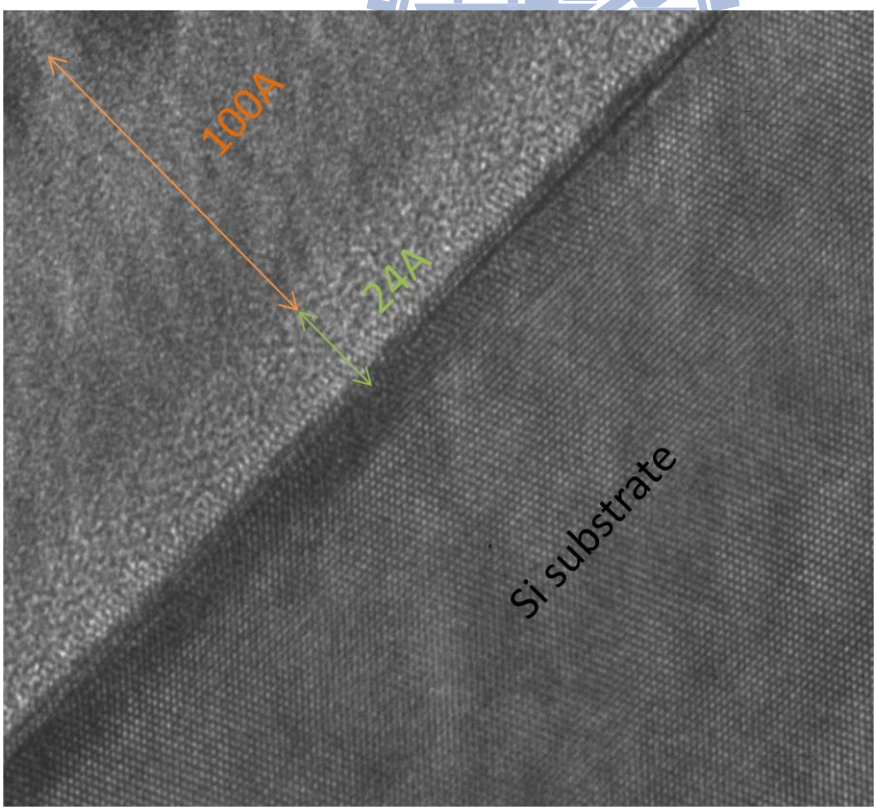


(b)

Fig. 2.2 (a)High-k thin film memory capacitor. (b) HfO_2 nanocrystal memory capacitor



(a)



(b)

Fig. 2.3 (a) Cross-sectional TEM image of HfO_2 and (b) Al_2O_3 memory capacitor.

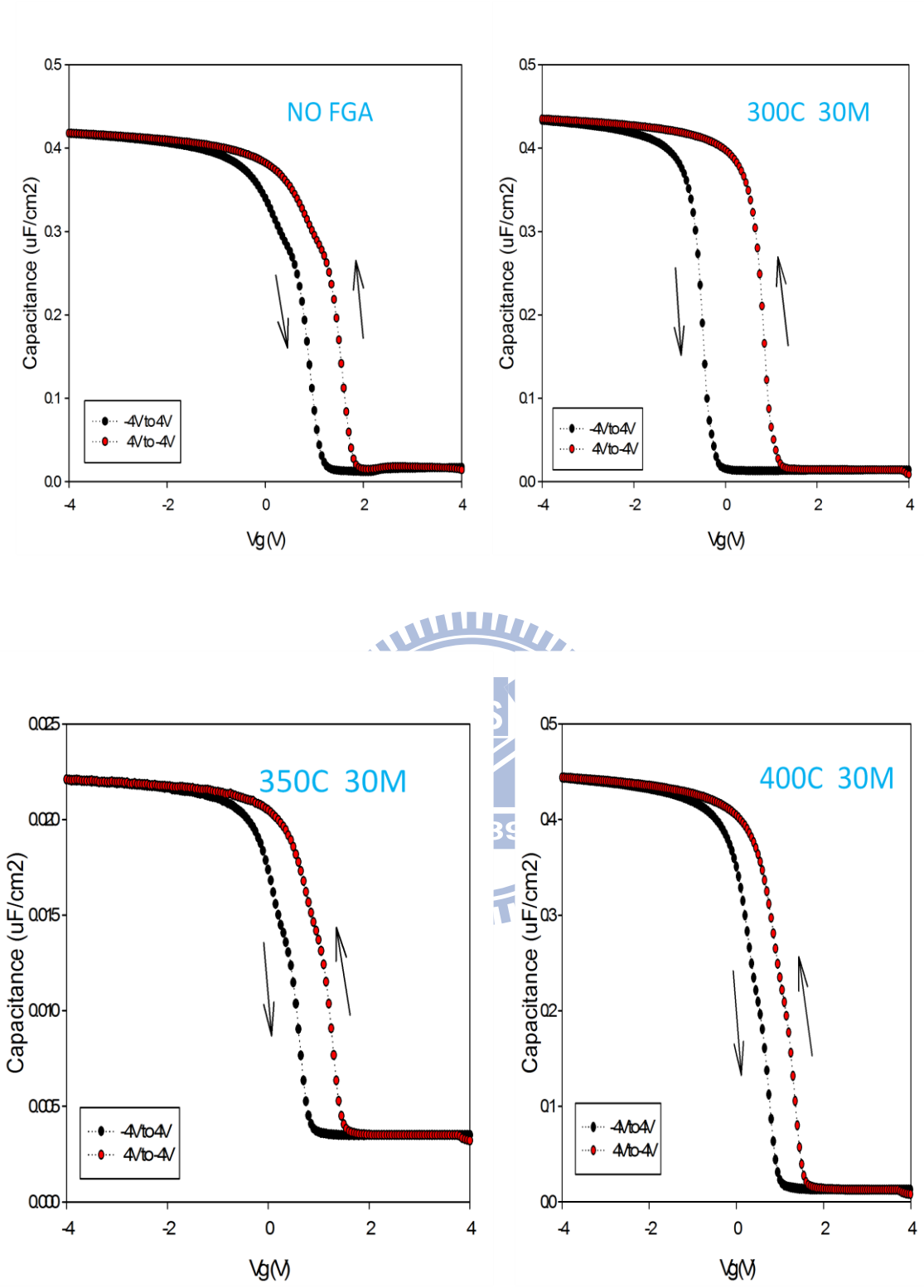


Fig. 2.4 (a) Capacitance-Voltage characteristics of HfO_2 thin film memory capacitor for no FGA sample and FGA temperature of 300°C, 350°C, and 400°C for 30min.

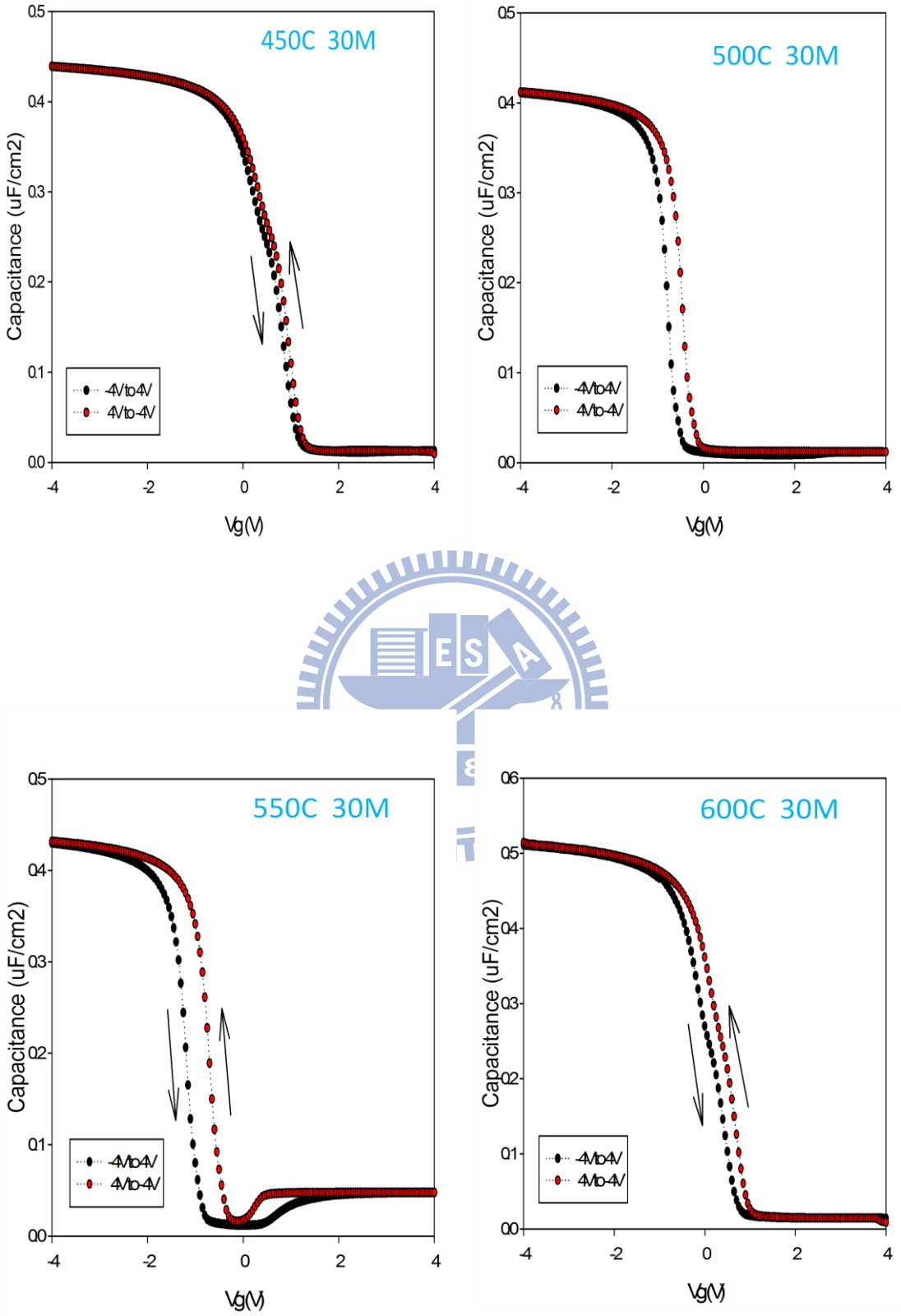


Fig. 2.4 (b)Capacitance-Voltage characteristics of HfO_2 thin film memory capacitor for FGA temperature of 450°C, 500°C, 550°C, and 600°C for 30min.

Table 2.1

HfO_2 Thin Film Memory Capacitor	
FGA Temperature	**CV Hysteresis (V)**
NO FGA	0.66
300°C 30M	1.32
350°C 30M	0.66
400°C 30M	0.60
450°C 30M	0.14
500°C 30M	0.38
550°C 30M	0.48
600°C 30M	0.29

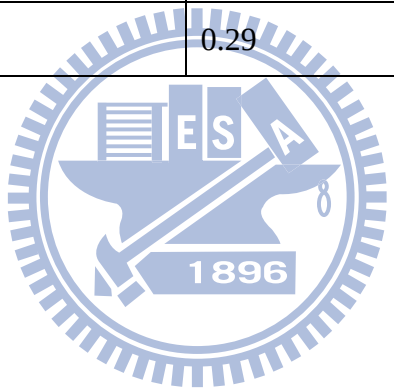


Table 2.1 Relationship between FGA temperature and CV hysteresis for HfO_2 thin film memory capacitor.

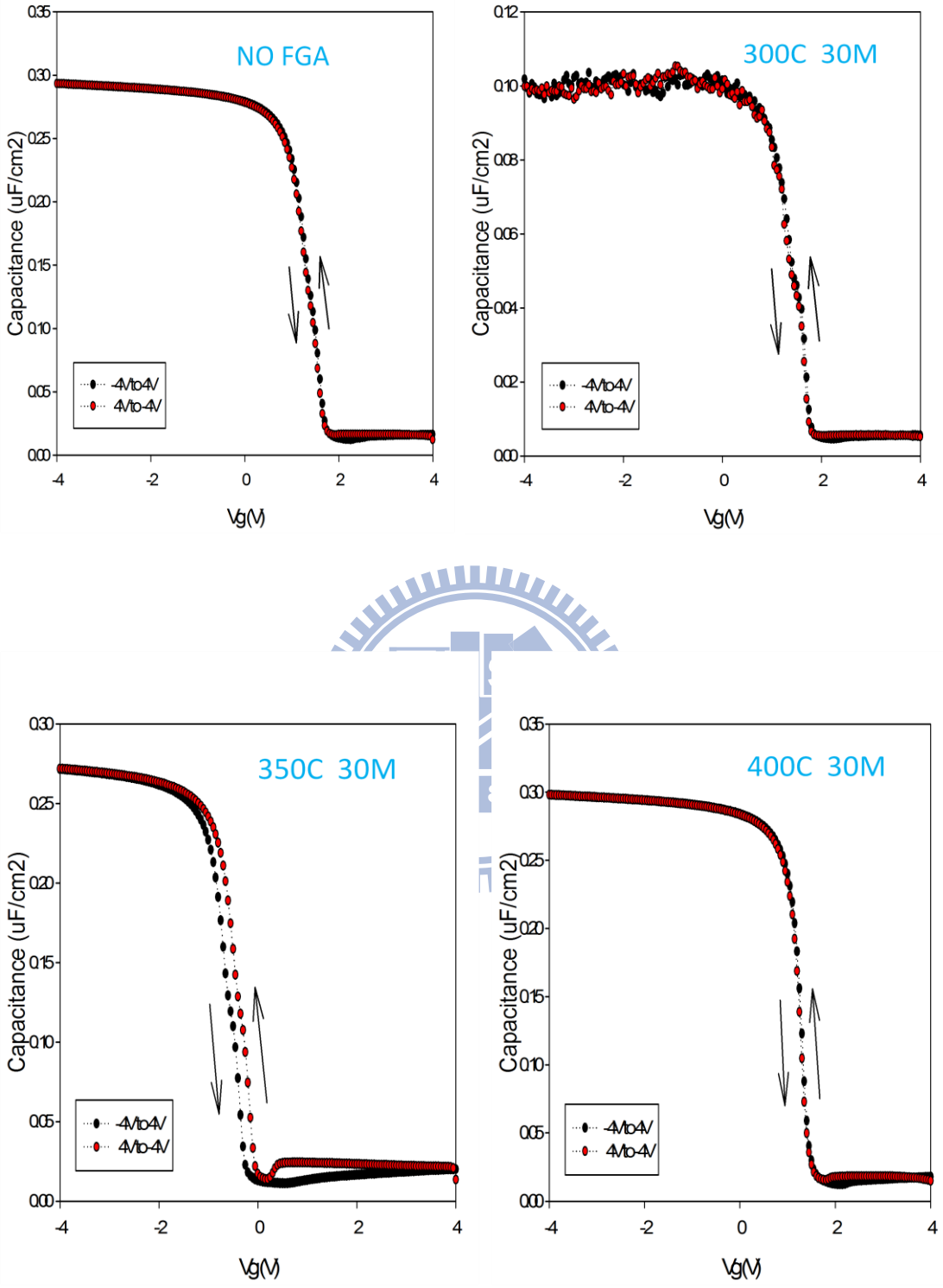


Fig. 2.5 (a)Capacitance-Voltage characteristics of Al_2O_3 thin film memory capacitor for no FGA sample and FGA temperature of 300°C, 350°C, and 400°C for 30min.

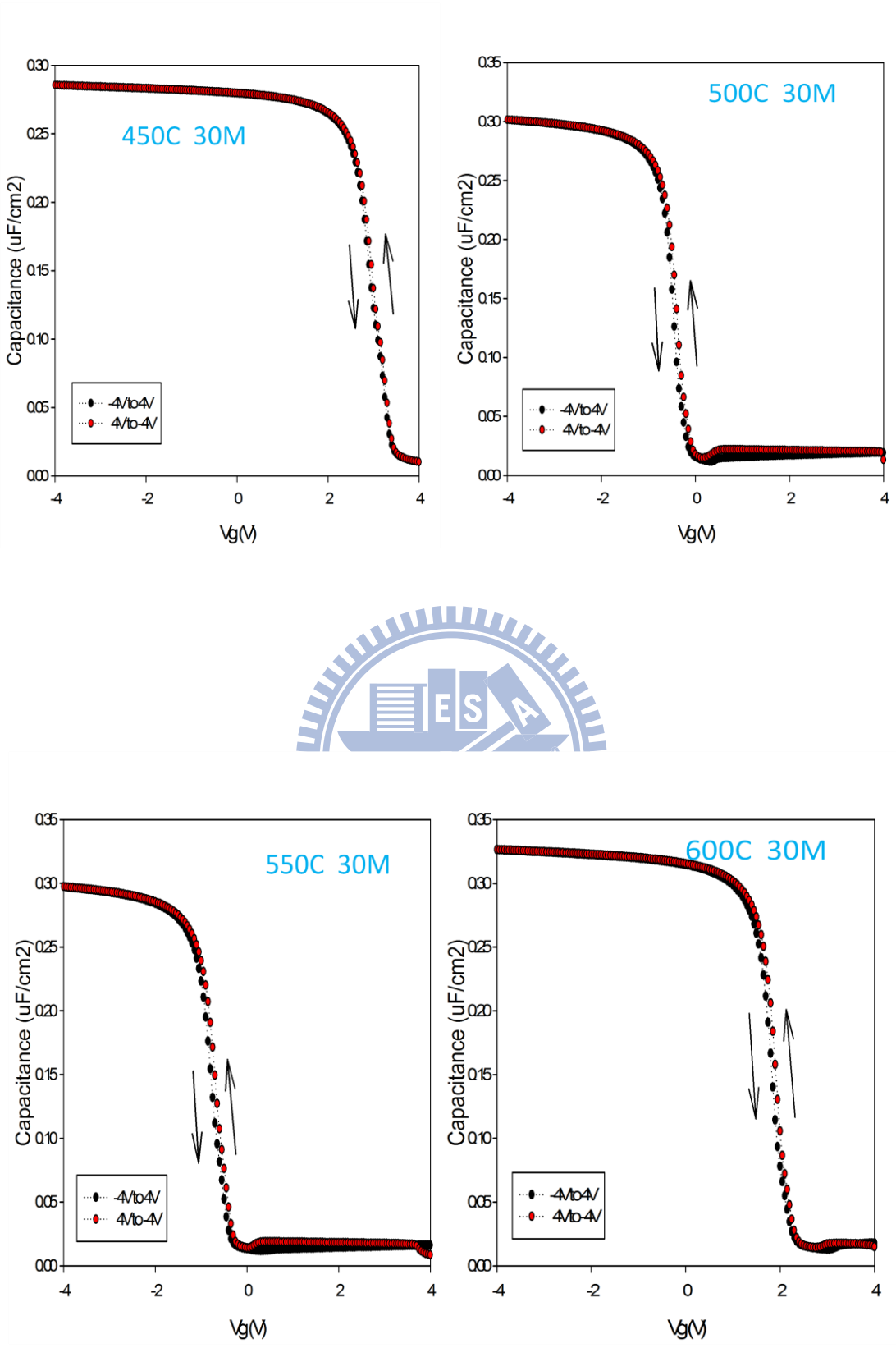


Fig. 2.5 (b)Capacitance-Voltage characteristics of Al_2O_3 thin film memory capacitor for FGA temperature of 450°C, 500°C, 550°C, and 600°C for 30min.

Table 2.2

Al_2O_3 Thin Film Memory Capacitor	
FGA Temperature	**CV Hysteresis (V)**
NO FGA	0.05
300°C 30M	0.03
350°C 30M	0.20
400°C 30M	0.03
450°C 30M	0.05
500°C 30M	0.07
550°C 30M	0.09
600°C 30M	0.08

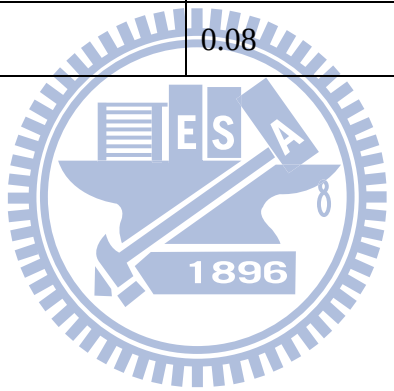


Table 2.2 Relationship between FGA temperature and CV hysteresis for Al_2O_3 thin film memory capacitor.

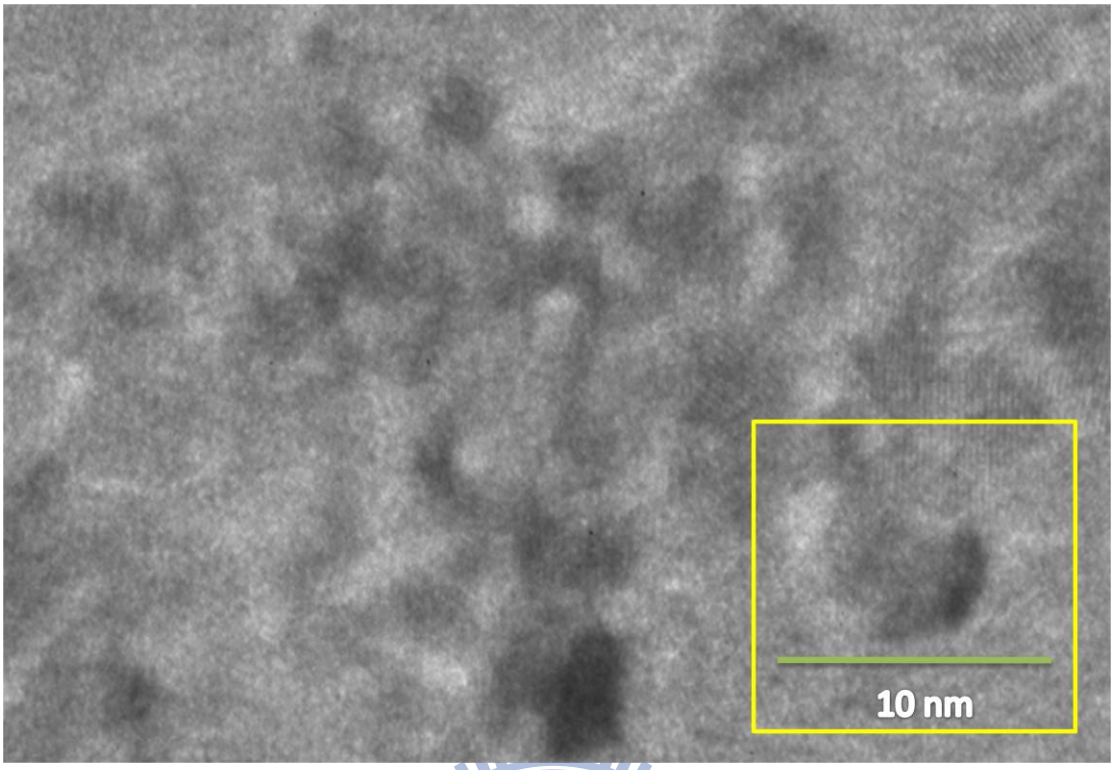


Fig. 2.6 Plane-view TEM image of the HfO_2 nanocrystal for 12nm HfSiOx layer after 950^{o}C 60sec RTA treatment. The dot size is 3-8nm and the density is about $2x10^{12}$ cm^{-2}.

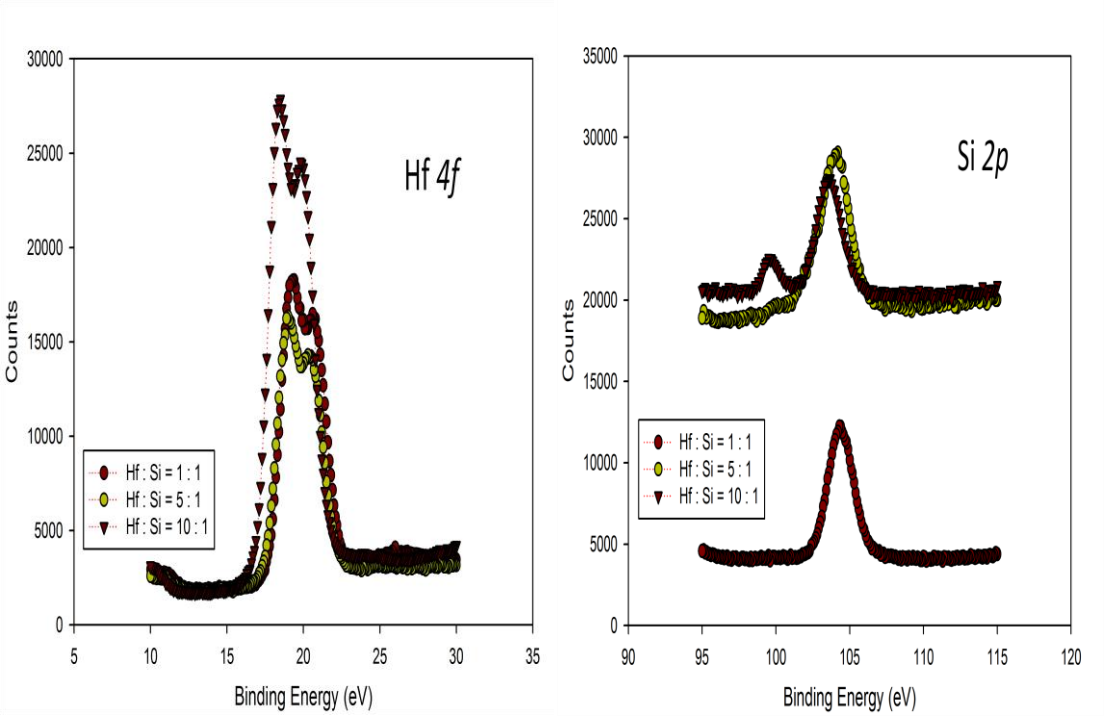


Fig. 2.7 XPS spectra of HfSiOx film for *Hf 4f* and *Si 2p*. The HfSiOx is deposited for different flow rate of Hf and Si by MOCVD system.

Table 2.3

HfSiOx Thin Film Atomic Composition		
At. %	**Hf**	**Si**
Hf : Si = 1 : 1	25.82	74.18
Hf : Si = 5 : 1	43.07	56.93
Hf : Si = 10 : 1	67.32	32.68

Table 2.3 HfSiOx atomic composition of Hf and Si for three different flow rates.

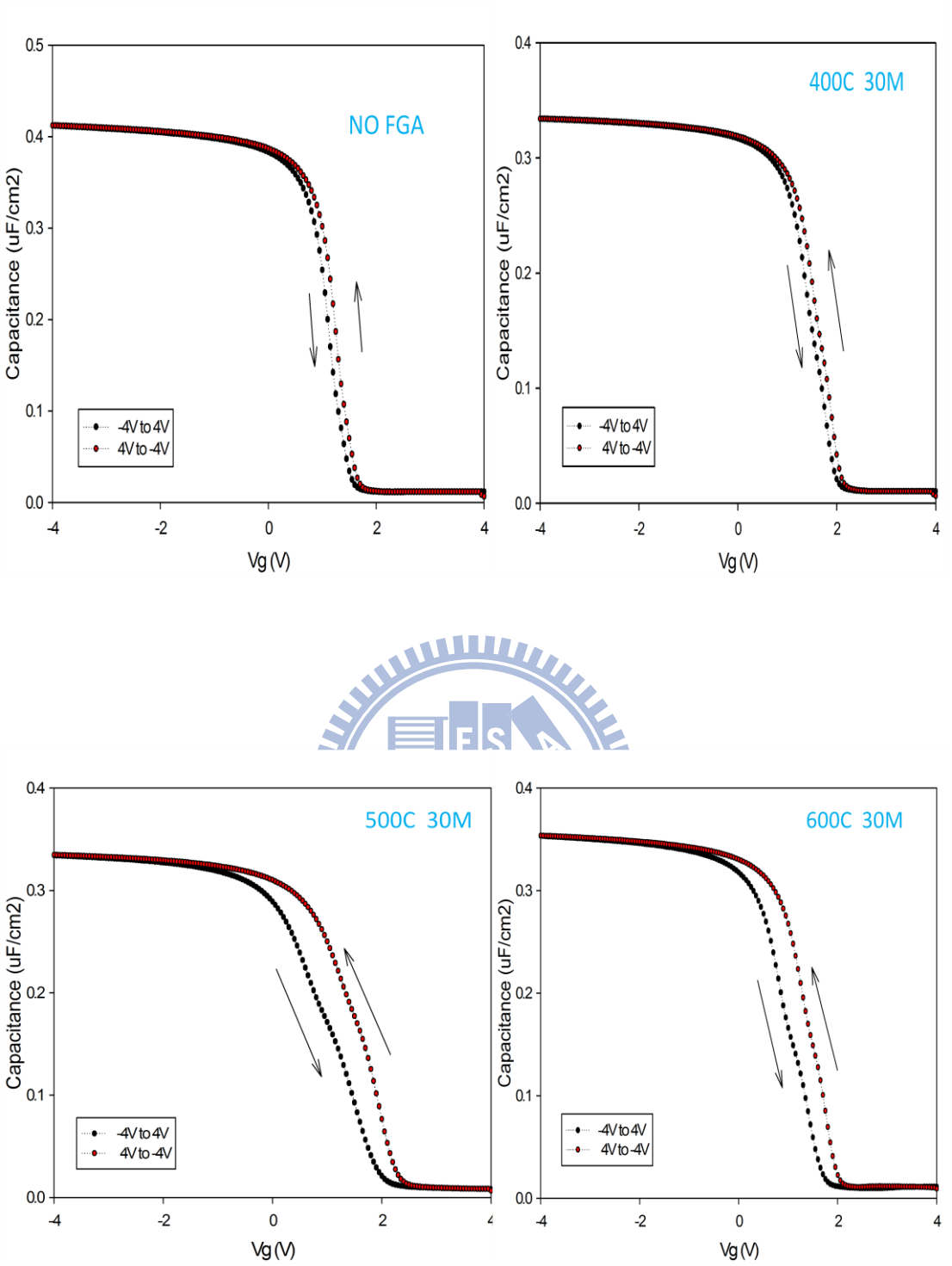


Fig. 2.8 Capacitance-Voltage characteristics of HfO_2 nanocrystal memory capacitor for no FGA sample and FGA temperature of 400°C, 500°C, and 600°C for 30min.

Table 2.4

HfO_2 Nanocrystal Memory Capacitor	
FGA Temperature	**CV Hysteresis**
NO FGA	0.13
400°C 30M	0.13
500°C 30M	0.58
600°C 30M	0.44

Table 2.4 Relationship between FGA temperature and CV hysteresis for HfO_2 nanocrystal memory capacitor.

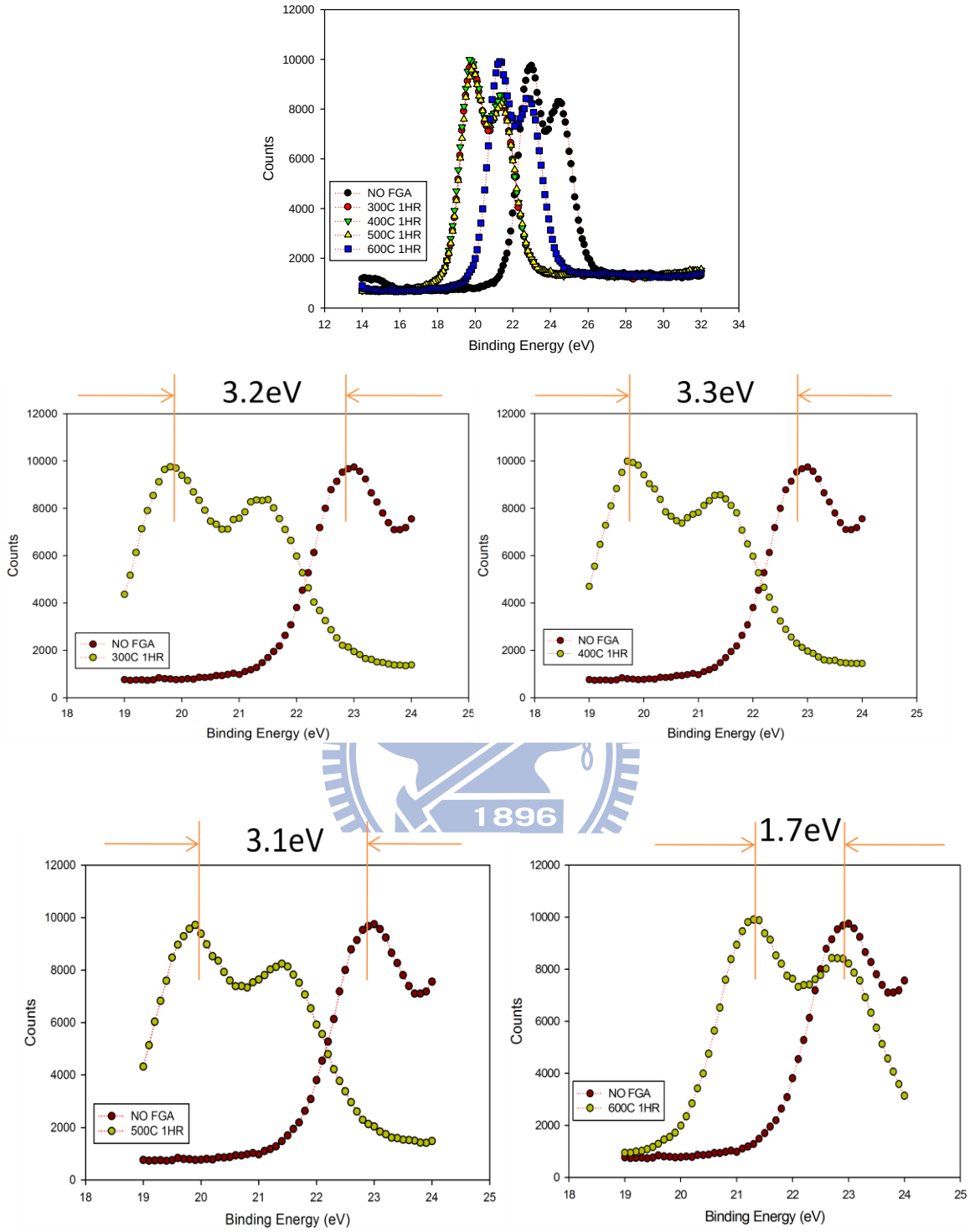


Fig. 2.9 XPS analysis for *Hf 4f* of the HfO_2 nanocrystal memory capacitor for different FGA temperature for 1hour. These spectra indicate that after FGA, a large binding energy shift toward the lower direction is seen, mainly due to the formation of oxygen vacancies.

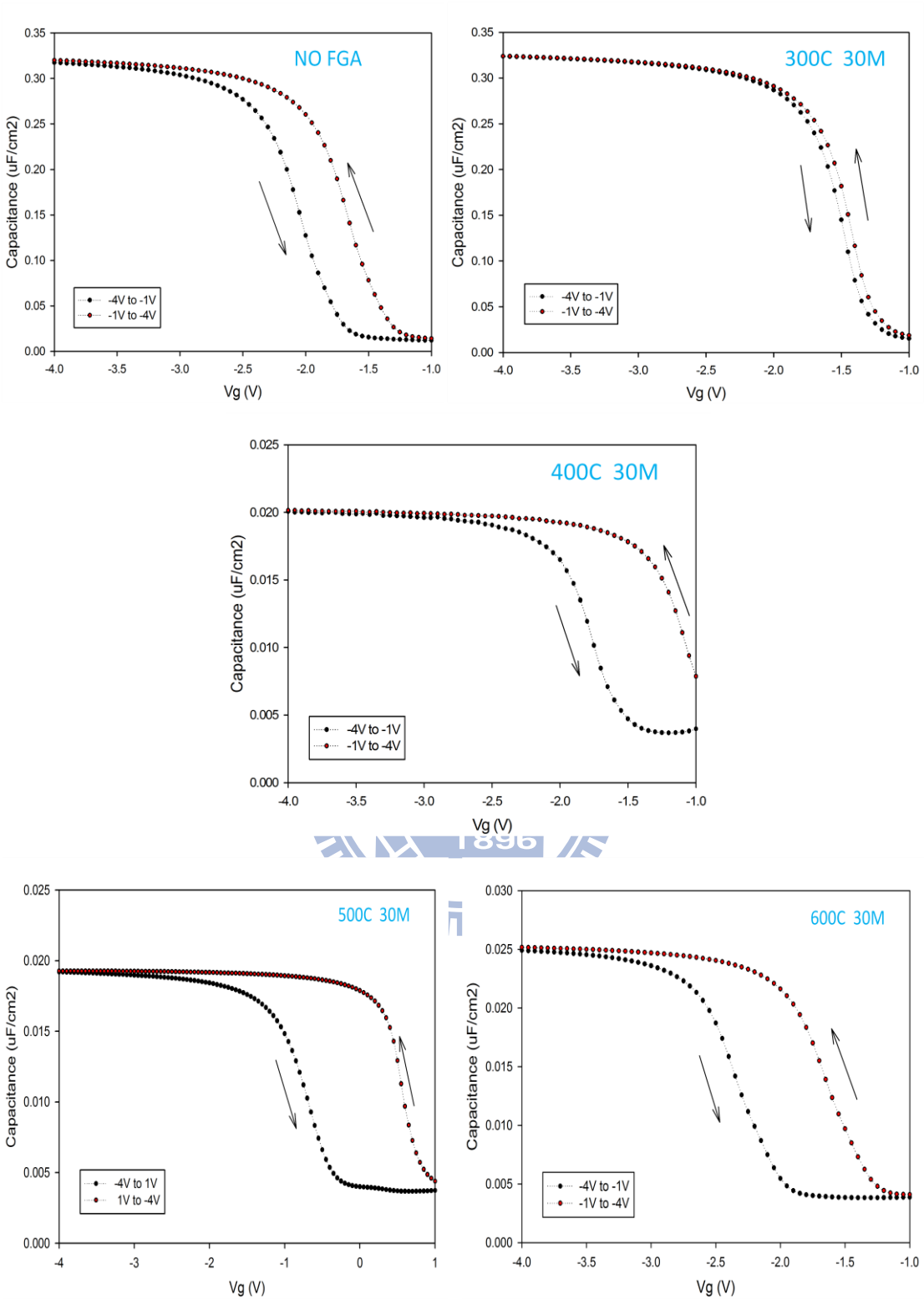


Fig. 2.10 Capacitance-Voltage characteristics of HfO_2 nanocrystal memory capacitor for no FGA sample and FGA temperature of 300°C, 400°C, 500°C, and 600°C for 1hour.

Table 2.5

HfO_2 Nanocrystal Memory Capacitor	
FGA Temperature	**CV Hysteresis**
NO FGA	0.38
300°C 1HR	0.06
400°C 1HR	0.67
500°C 1HR	1.34
600°C 1HR	0.69

Table 2.5 Relationship between FGA temperature (for 1hour) and CV hysteresis for HfO_2 nanocrystal memory capacitor.

Chapter 3
Effects of Electric Dipole on HfO_2 Thin Film and Nanocrystal Memory Capacitors

3.1 Introduction

SONOS-type (PolySi-Oxide-Nitride-Oxide-Silicon) flash memory has recently attracted much attention as a candidate for the next-generation nonvolatile memory[61]. For this discrete-trap memory, the SONOS-type flash memories have advantages of high P/E speed, low operation voltage, low power consumption, excellent retention, endurance, and disturbance characteristics[62-64]. However, with the semiconductor technology becomes more and more prosperous, designing devices with higher P/E speed while maintaining sufficiently long retention time is a major challenge.

A high-k metal gated scheme for metal-oxide-semiconductor field-effect-transistors (MOSFET) at 45nm technology is developed to replace the traditional SiON/polysilicon (poly-Si) based devices due to the poly-Si depletion effect[65]. Metal gate with two different work functions for n- and p-MOSFET is required for optimal device performance in CMOS logic circuits[66-68]. However, for nMOSFET, low work function metal gate is easy to react with the underlying high-k dielectric and causes interfacial layer growth, thus high EOT. For pMOSFET, high work function metal gate is often inert metal, so it is hard to fabricate and increase process complexity. Also, it is hard to develop metal gate with work function near Si band edges on Hf-based gate dielectrics because of Fermi-level pinning effect. So it is

becoming strongly apparent to tailor the work function of the metal gate by engineering the interface. It has been reported that La_2O_3 or LaN interfacial layer is used to get band-edge effective work function for high-k/metal gate nMOSFET[69, 70]. Also, AlOx or AlN capping layer has been shown to be effective in modulating the band-edge effective work function for pMOSFET[71-74]. The inserted layer, rare-earth (RE)-based for nMOSFET and Al-based for pMOSFET, named dipole layer, either decreases or increases the effective gate work function by creating a localized electric field in the gate stacks. In 2007, *S. Kubicek et al* adopted dipole layer in both nMOS and pMOS to successfully integrate in CMOS circuits to achieve band-edge effective work functions (EWF)[75]. Also in the year of 2007, *K. Iwamoto et al* confirm that V_{FB} is uniquely determined by the high-k film contacting with bottom SiO_2, and the high-k material/SiO_2 interface plays a significant role in Vth control for MOS devices[76]. *Y. Kamimuta et al* further indicate that the effective work function is only governed by the high-k/SiO_2 interface and metal work function, as shown in figure 3.1[55]. The energy offsets at the interface of Al_2O_3, HfO_2, and Y_2O_3 on SiO_2 are estimated to be $+0.57\pm0.05$, $+0.31\pm0.05$, and -0.23 ± 0.05eV, respectively.

In this chapter, we adopt the concept of the above understandings and combined with FGA effect mentioned in chapter 2 to our HfO_2 thin film and nanocrystal memory capacitors. It gives us a general idea of how the dipole layer affects our nonvolatile memory devices.

3.2 Experiment

Nitride-based SONOS-type memory capacitor is fabricated on a p-type, 5-10 Ω cm, (100) 150-mm silicon substrate. After RCA clean, a 2.5nm dry oxide is grown in horizontal furnace system by APCVD. Then an ultra-thin (~1nm) high-k film (HfO_2

or Al_2O_3) is deposited by MOCVD system. Next a 12nm Si_3N_4 is deposited by LPCVD followed by 7nm PECVD SiO_2. After coating Al as top and bottom electrode, the memory capacitor with dipole layer is finished (Figure 3.2). HfO_2 thin film memory capacitor with dipole layer below trapping nitride is realized by thermally grown SiO_2 on silicon substrate, ~1nm Al_2O_3 and 12nm HfO_2 is deposited by MOCVD. Then we subject the samples into FGA for 300^oC~600^oC for 1hour. And a 7nm SiO_2 by PECVD is deposited(Figure 3.3 (a)). HfO_2 thin film memory capacitor with dipole layer both upon and below the HfO_2 is fabricated by the same sequence as mentioned above except for the additional ~1nm Al_2O_3 on top of the HfO_2 (Figure 3.3 (b)). Three different samples for HfO_2 nanocrystal memory capacitors are fabricated with changing temperature of FGA for 1hour by the same manner as described in chapter 2.2 except for interlayer insertion: One for ~1nm Al_2O_3 between HfO_2 nanocrystal trapping layer and bottom SiO_2, another for ~1nm Al_2O_3 between trapping layer and top SiO_2, the other for ~1nm Al_2O_3 both upon and below the trapping layer, respectively(Figure 3.4 (a~c)).

3.3 Results and Discussions

3.3.1 Analysis of Dipole Layer Engineering

Figure 3.5 depicts CV characteristics of SONOS-type memory capacitor with dipole layer engineering. Clearly, flat band voltage increases with inserting an ultra-thin high-k layer. V_{FB} follws: SONOS-Al_2O_3 > SONOS-HfO_2 > SONOS according to figure 3.5. The EOT enhancement could be negligible due to the ultra-thin high-k layer, and the process is almost the same for these samples. Therefore, we can attribute the increase of V_{FB} to the increase of gate effective work

function. The results are well fitted to figure 3.1, which is reported by *Y. Kamimuta et al*. We confirm that modulating the gate effective work function by inserting an ultra-thin dipole layer is valid. It has been employed to the advanced high-k/metal gate devices to adjust threshold voltage appropriately (0~0.2 for nMOSFET, 0~-0.2 for pMOSFET)[71-74].

3.3.2 HfO_2 Thin Film Memory Capacitor with Dipole Layer Engineering

Figure 3.6 shows XPS spectra of HfO_2 thin film memory capacitor with ~1nm Al_2O_3 between HfO_2 and bottom SiO_2 for different FGA temperature of 300^{o}C~600^{o}C 1hour. And figure 3.7 illustrates Capacitance-Voltage characteristics of these capacitors. The CV hysteresis extracted is shown in table 3.1. For 300^{o}C and 400^{o}C cases, the core-level *Hf 4f* shifts about 0.2eV toward the higher binding energy compared to the sample without FGA. And it shows the largest CV hysteresis shown in Table 3.1, 1.46V for 300^{o}C case and 1.42V for 400^{o}C case. The larger hysteresis is caused by generated oxygen vacancies from FGA as discussed in chapter 2. For 500^{o}C case, the binding energy is exactly the same as the sample without FGA. And we discover that the hysteresis is almost the same as that of no FGA case. Furthermore, for 600^{o}C case, the binding energy decreases by about 0.1eV compared to the no FGA case. And we find out that the hysteresis even decreases to about 0.06V, which is smaller than the sample without FGA. In 2007, *Y. Kamimuta et al* reported that oxygen vacancies generated by FGA can induce an “extrinsic dipole” at high-k/SiO_2 interface, which is in opposite polarity with the “intrinsic dipole” discussed in this chapter[55]. From the above XPS analysis and CV measurement, we get some clues which are in consistent with the report.

Figure 3.8 demonstrates XPS analysis of HfO_2 thin film memory capacitor with ~1nm Al_2O_3 both below and upon HfO_2 trapping layer for FGA temperature of 300°C~600°C, 1hour. Figure 3.10 shows CV characteristics of these capacitors. The hysteresis is extracted by figure 3.9 and is shown in Table 3.2. From figure 3.9, all the cases for FGA temperature from 300°C~600°C reveals a binding energy shift of about 0.6eV toward the lower direction compared to the no FGA case. And the hysteresis is almost the same for all different samples, and the larger one is for 500°C 1hour of 0.7V. We have mentioned that the "intrinsic dipole" and the oxygen-vacancy-generated dipole ("extrinsic dipole") have opposite polarity[55]. The two dipole layers and FGA-generated oxygen vacancies represent two different situations and may possibly be the cause of similar CV hysteresis.

3.3.3 HfO_2 Nanocrystal Memory Capacitor with Dipole Layer Engineering

Figure 3.10 shows CV characteristics of HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 between trapping layer and bottom oxide for different FGA temperature from 300°C to 600°C for 1hour. Table 3.3 illustrates CV hysteresis extracted from figure 3.11. We find that for the case of FGA temperature of 500°C for 1hour, the hysteresis is as large as 1.69, which is caused by the oxygen vacancies generated by FGA. Figure 3.11 shows XPS spectra of *Hf 4f* for HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 between trapping layer and top SiO_2 for different FGA temperature from 300°C~600°C, 1hour. Figure 3.12 depicts CV characteristics of these samples. Table 3.4 shows CV hysteresis extracted from figure 3.12. For 300°C, 400°C, 500°C cases, the binding energy shifts toward the lower direction compared to the sample without FGA and results in a slightly bigger hysteresis. For 600°C case, the binding

energy is rather larger than the no FGA sample. For the 400°C, 1hour case, the hysteresis is 0.81, which is the highest among the different FGA temperature. Also for that case, the binding energy of Hf 4f shifts the most to the lower direction, which corresponds to the generated oxygen vacancies, and is responsible for the higher CV hysteresis. Figure 3.14 illustrates CV characteristics HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 both below and upon trapping layer for different FGA temperature from 300°C~600°C, 1hour. Table 3.5 shows CV hysteresis extracted from figure 3.13. For 300°C 1hour case, the hysteresis is as large as 1.73V, which can be utilized to distinguish the "1" and "0" states in logic applications.

3.4 Summary

In this chapter, we investigate the HfO_2 thin film and nanocrystal memory capacitor with dipole layer engineering for different FGA temperature from 300°C to 600°C for 1hour. At first, we incorporate an ultra-thin (~1nm) high-k (HfO_2 or Al_2O_3) layer between Si_3N_4 and tunnel oxide in SONOS-like memory capacitor. Flat-band voltage shift is observed in SONOS-type memory capacitor and Al_2O_3 is found to be the most effective to modulate gate work function. HfO_2 thin film memory capacitor with ~1nm Al_2O_3 between trapping layer and bottom oxide shows a large CV hysteresis of 1.46V and 1.42V for FGA temperature of 300°C and 400°C for 1hour. Moreover, for HfO_2 thin film capacitor with both ~1nm Al_2O_3 below and upon trapping layer, a hysteresis of 0.7V is found for 500°C 1hour case. For HfO_2 nanocrystal memory capacitor, a 1.69V hysteresis is achieved with 500°C 1hour FGA for ~1nm Al_2O_3 between trapping layer and bottom oxide. And a hysteresis of 0.81V is realized with 400°C 1hour FGA for ~1nm Al_2O_3 between trapping layer and top oxide. Also we get hysteresis of 1.73V with 300°C 1hour and 1.11V with 500°C 1hour from FGA for

both ~1nm Al_2O_3 below and upon the trapping layer.

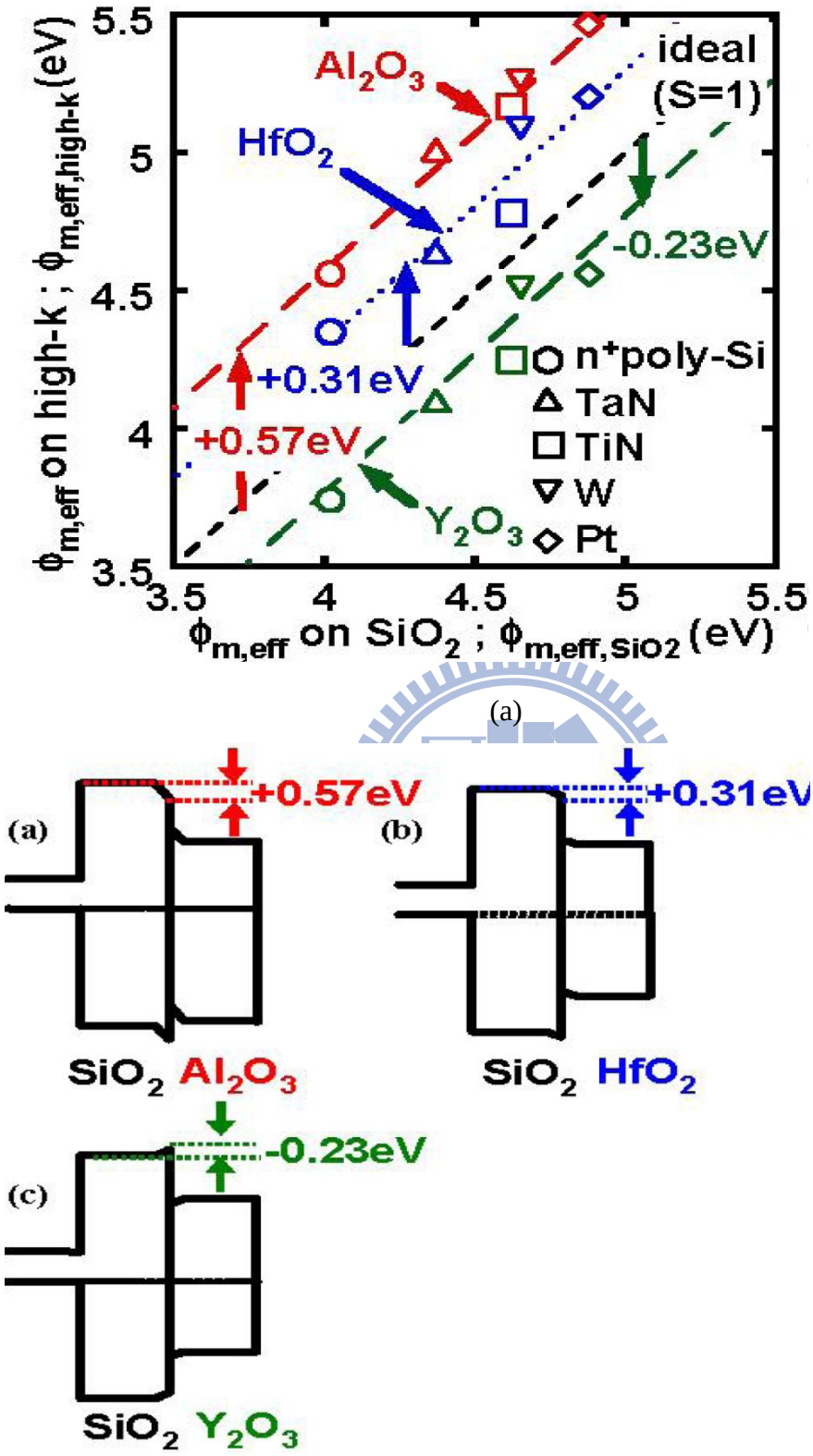


Fig. 3.1 (a)Relationship between EWF of metal gate along with n^+ poly-Si on high-k and SiO_2. (b)Schematic band diagram of Al_2O_3/SiO_2, HfO_2/SiO_2, and Y_2O_3/SiO_2 systems[55].

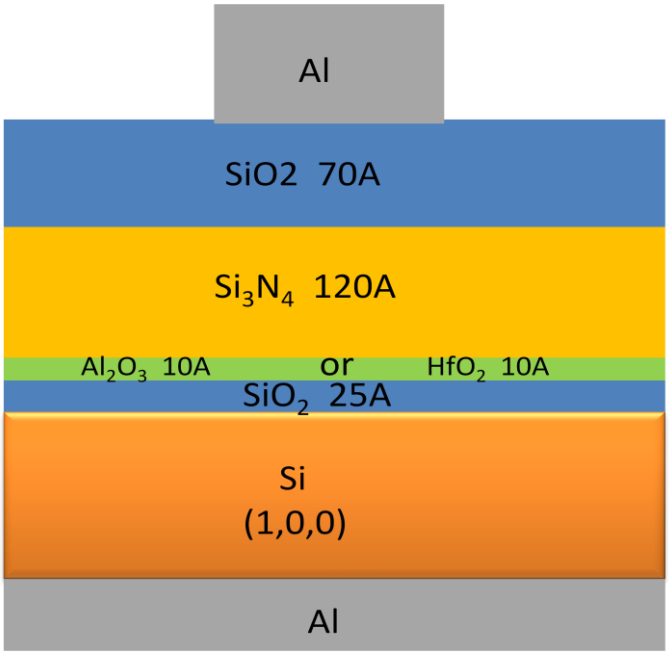


Fig. 3.2 Schematic of dipole layer engineering on SONOS-type memory capacitor.

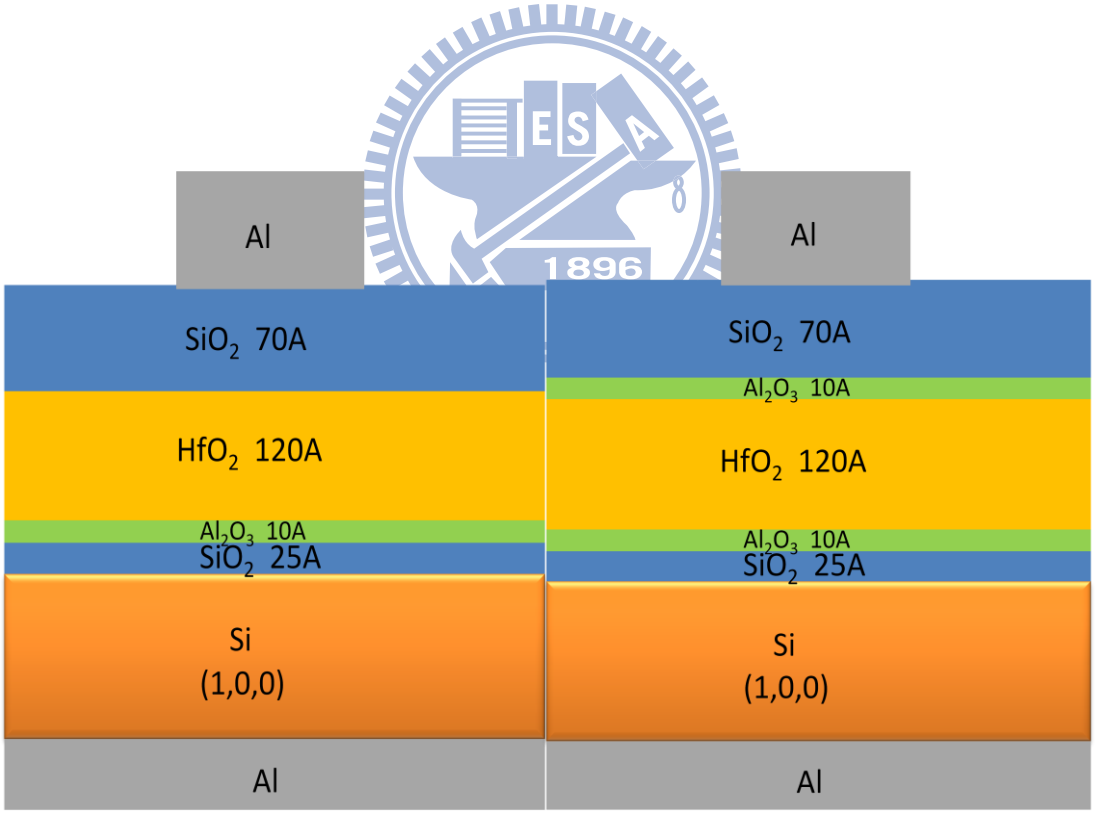
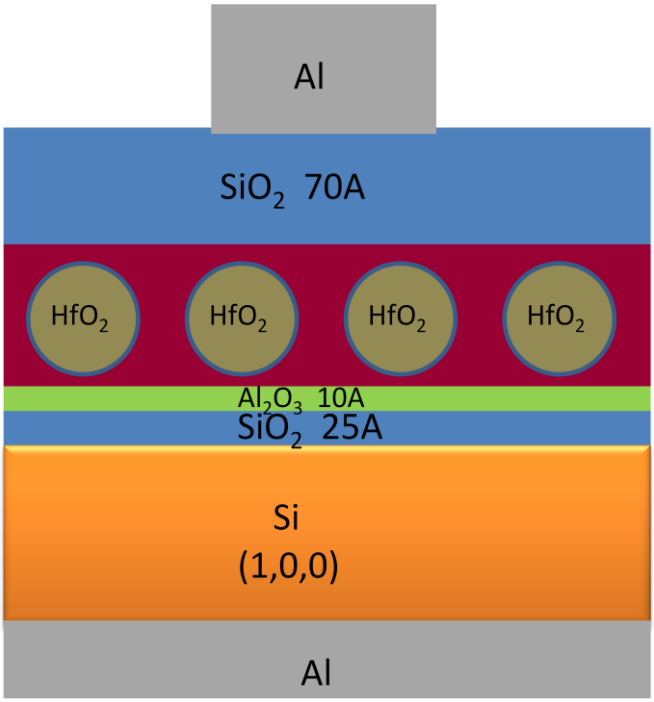
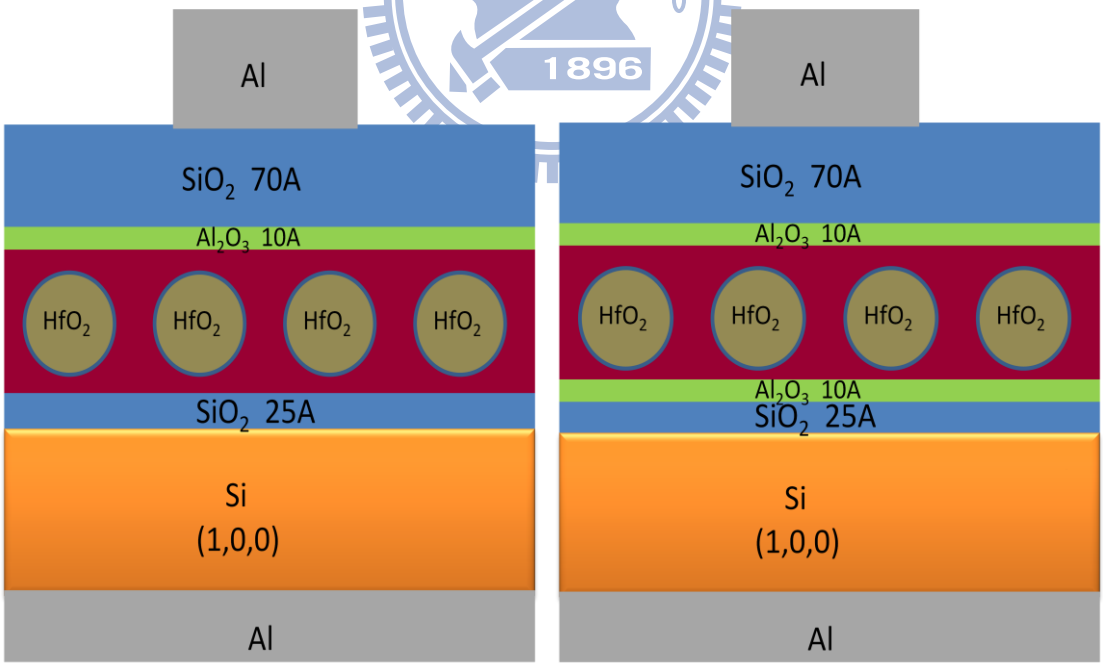


Fig. 3.3 Schematic of HfO_2 thin film memory capacitor with dipole layer engineering (a)between HfO_2 and SiO_2 (b)both below and on the top of HfO_2.



(a)



(b) (c)

Fig. 3.4 Schematic of HfO_2 nanocrystal memory capacitor with dipole layer engineering (a)below (b) on the top of (c) below and on the top of the HfO_2 nanocrystal trapping layer.

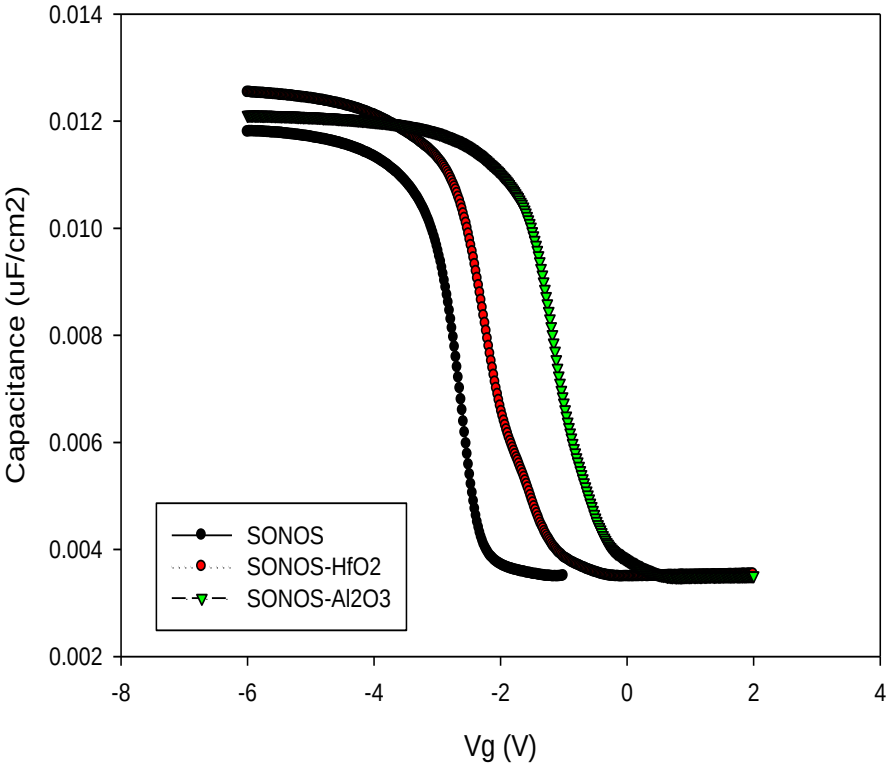


Fig. 3.5 Schematic of CV curves for SONOS-type memory capacitor without and with (HfO_2 and Al_2O_3) dipole layer engineering.

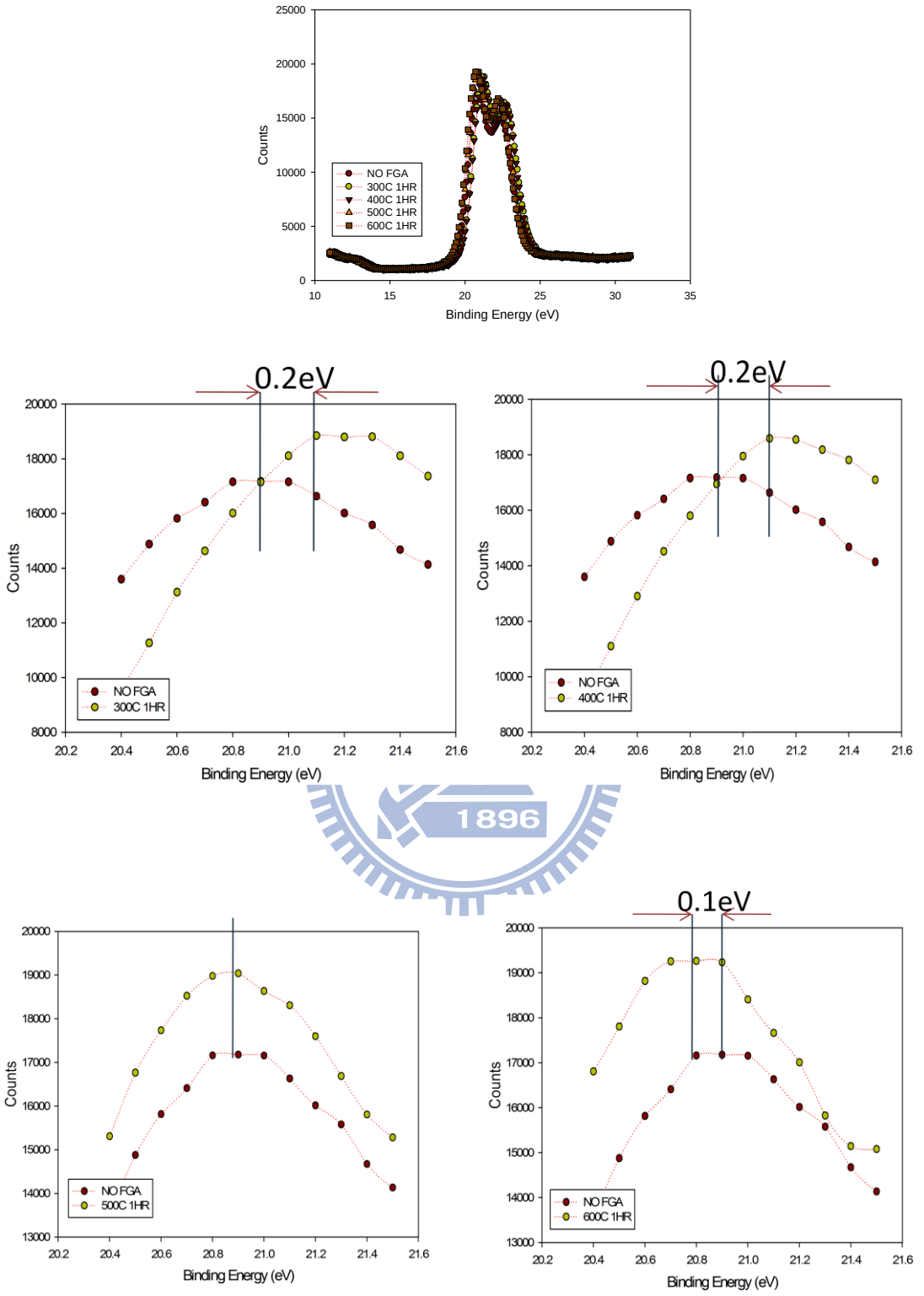


Fig. 3.6 XPS spectra of *Hf 4f* for HfO_2 thin film memory capacitor with ~1nm Al_2O_3 between HfO_2 and bottom SiO_2 for different FGA temperature from 300°C to 600°C for 1hour.

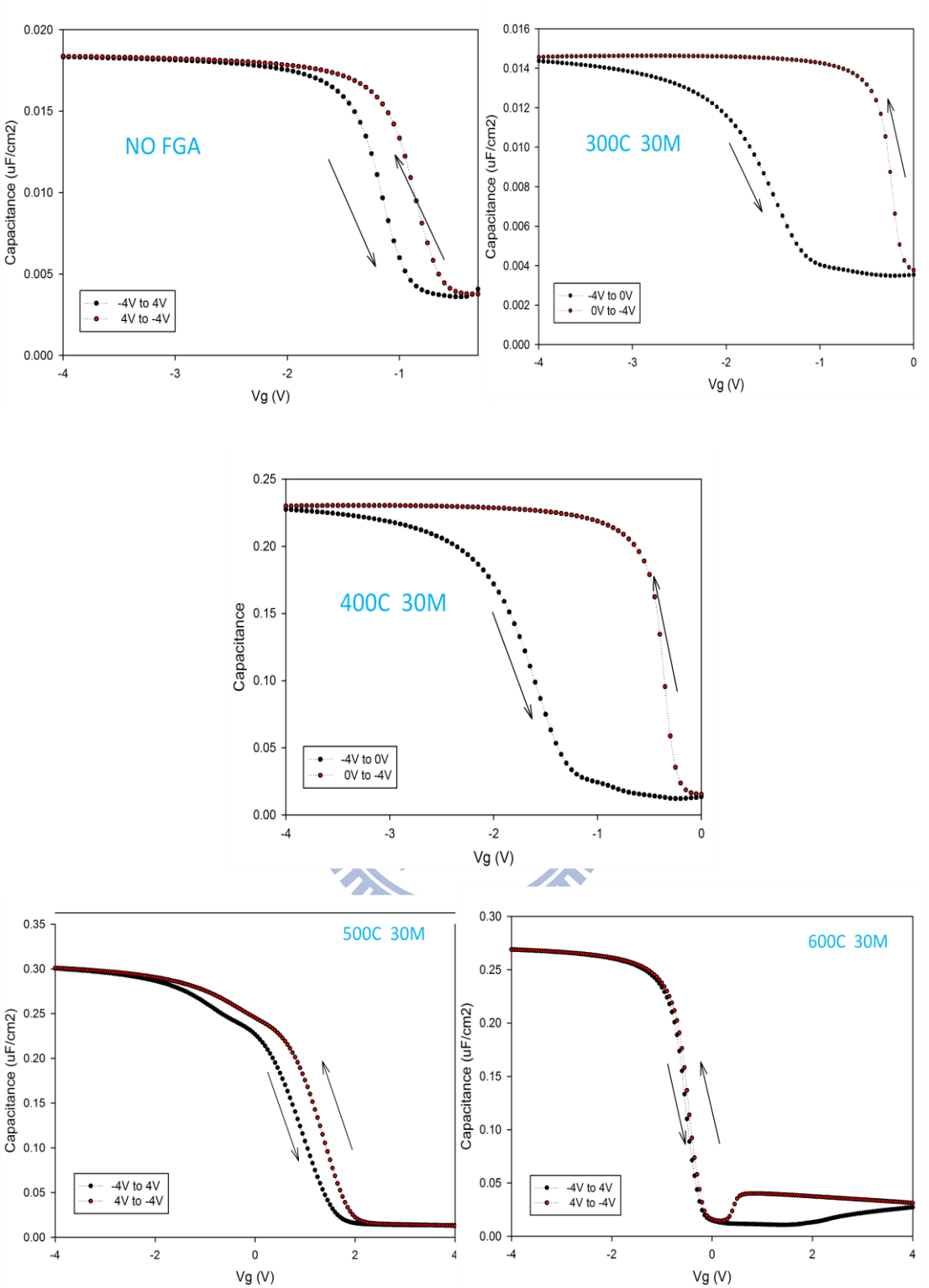


Fig. 3.7 CV characteristics of HfO_2 thin film memory capacitor with ~1nm Al_2O_3 between HfO_2 and bottom SiO_2 for different FGA temperature from 300°C to 600°C for 1hour.

Table 3.1

HfO_2 Thin Film Capacitor (with bottom Al_2O_3)	
FGA Temperature	**CV Hysteresis**
NO FGA	0.30
300°C 1HR	1.46
400°C 1HR	1.42
500°C 1HR	0.46
600°C 1HR	0.06

Table 3.1 CV hysteresis of HfO_2 thin film memory capacitor with ~1nm Al_2O_3 between HfO_2 and bottom SiO_2 for different FGA temperature from 300°C to 600°C for 1hour.

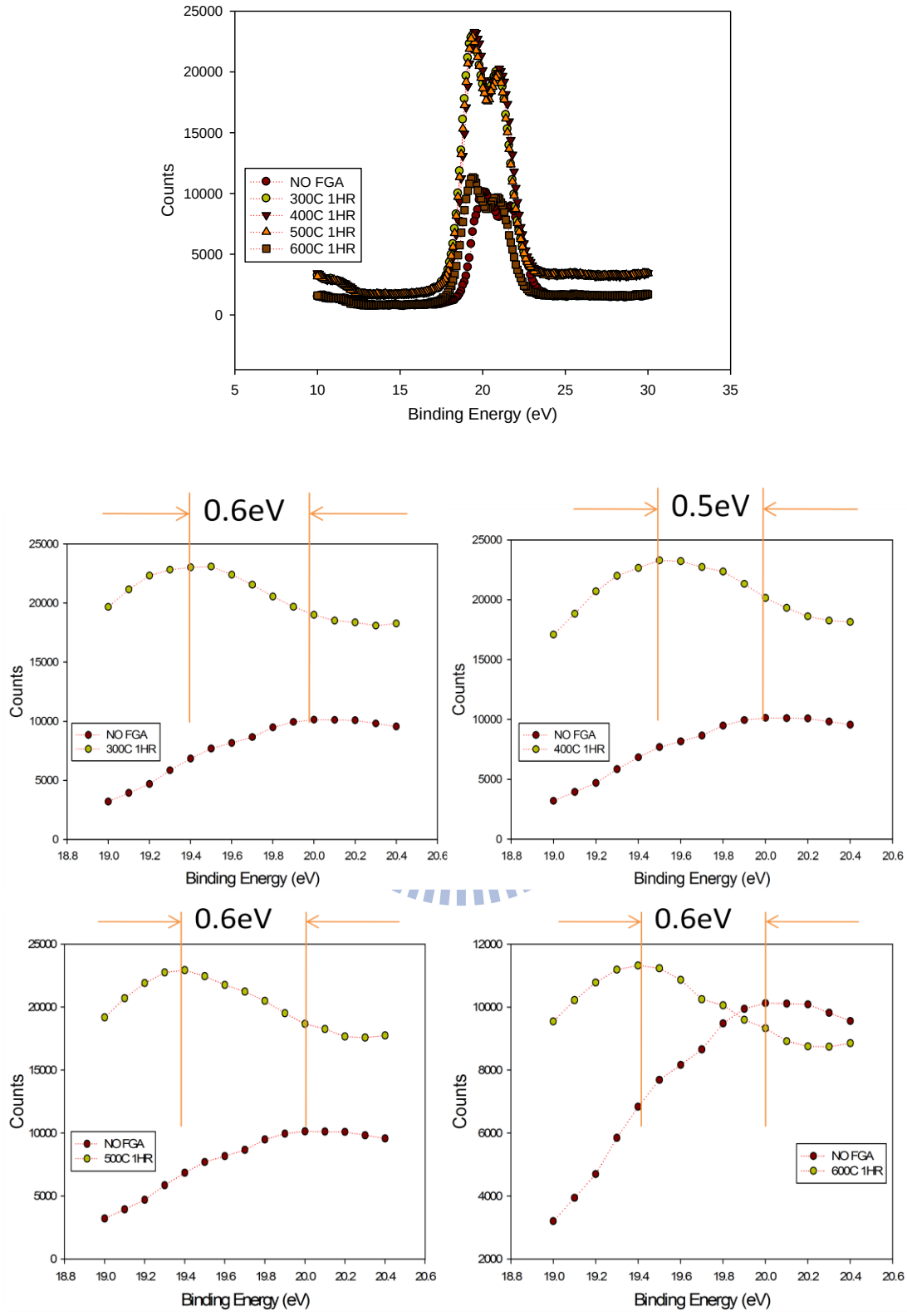


Fig. 3.8 XPS spectra of *Hf 4f* for HfO_2 thin film memory capacitor with ~1nm Al_2O_3 both below and upon HfO_2 trapping layer for different FGA temperature from 300°C to 600°C for 1hour.

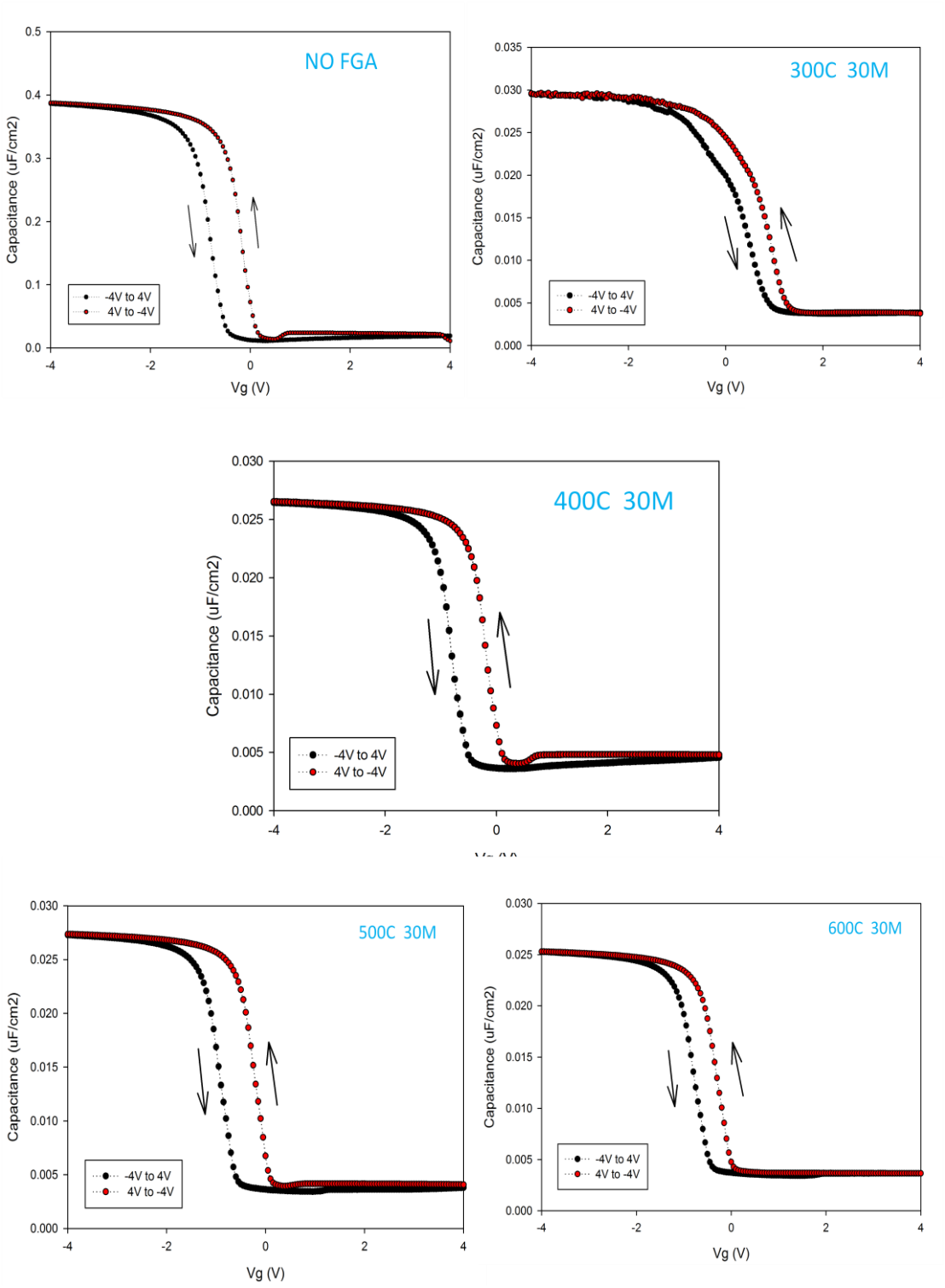


Fig. 3.9 CV characteristics of HfO_2 thin film memory capacitor with ~1nm Al_2O_3 both below and upon HfO_2 trapping layer for different FGA temperature from 300^oC to 600^oC for 1hour.

Table 3.2

HfO_2 Thin Film Capacitor (with bottom and top Al_2O_3)	
FGA Temperature	**CV Hysteresis**
NO FGA	0.62
300°C 1HR	0.52
400°C 1HR	0.62
500°C 1HR	0.70
600°C 1HR	0.48

Table 3.2 CV hysteresis of HfO_2 thin film memory capacitor with ~1nm Al_2O_3 both below and upon HfO_2 trapping layer for different FGA temperature from 300°C to 600°C for 1hour.

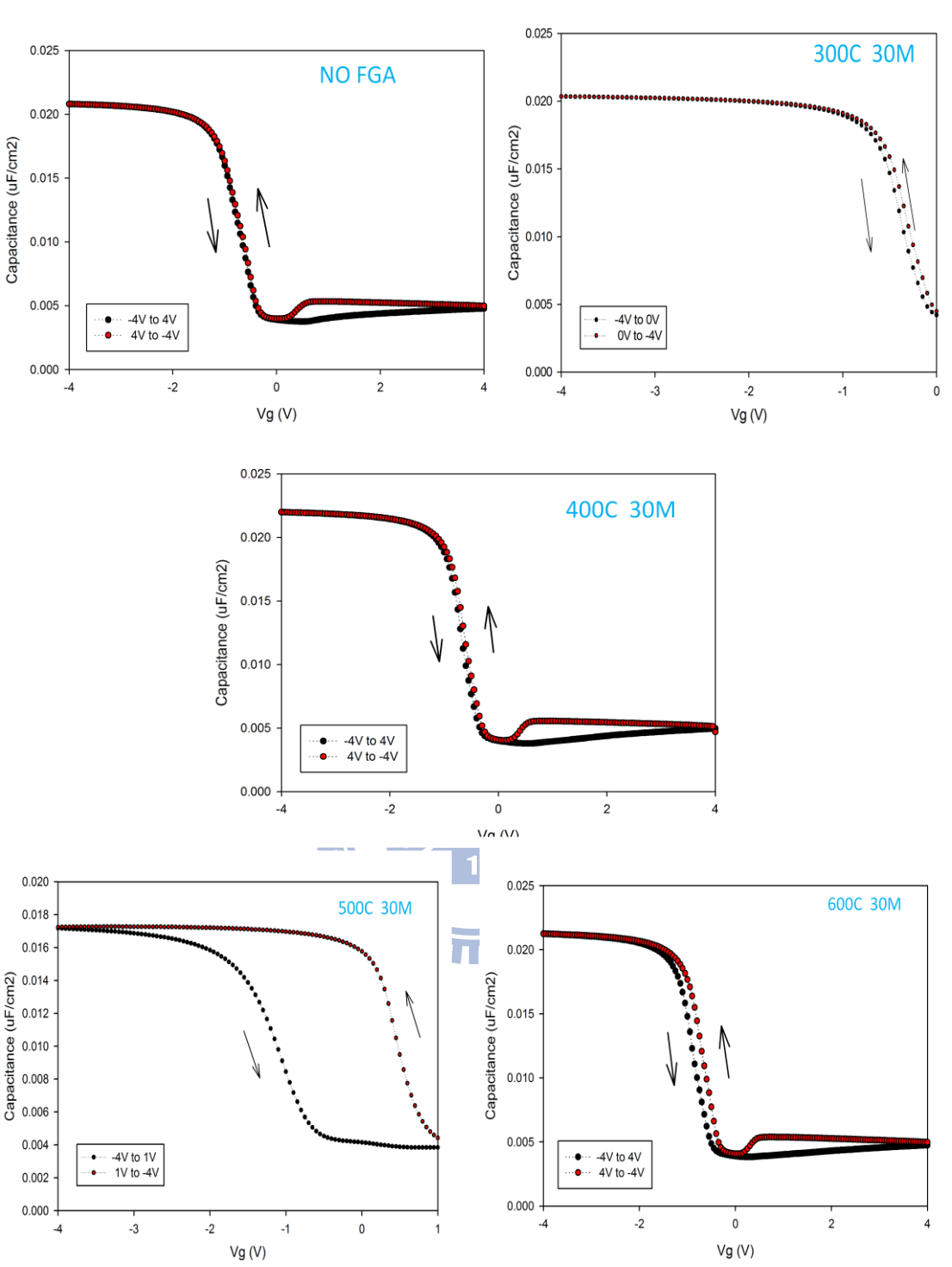


Fig. 3.10 CV characteristics of HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 between HfO_2 trapping layer and bottomSiO_2 for different FGA temperature from 300^{o}C to 600^{o}C for 1hour.

Table 3.3

HfO_2 Nanocrystal Capacitor (with bottom Al_2O_3)	
FGA Temperature	**CV hysteresis**
NO FGA	0.03
300°C 1HR	0.06
400°C 1HR	0.06
500°C 1HR	1.69
600°C 1HR	0.19

Table 3.3 CV hysteresis of HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 between HfO_2 trapping layer and bottomSiO_2 for different FGA temperature from 300°C to 600°C for 1hour.

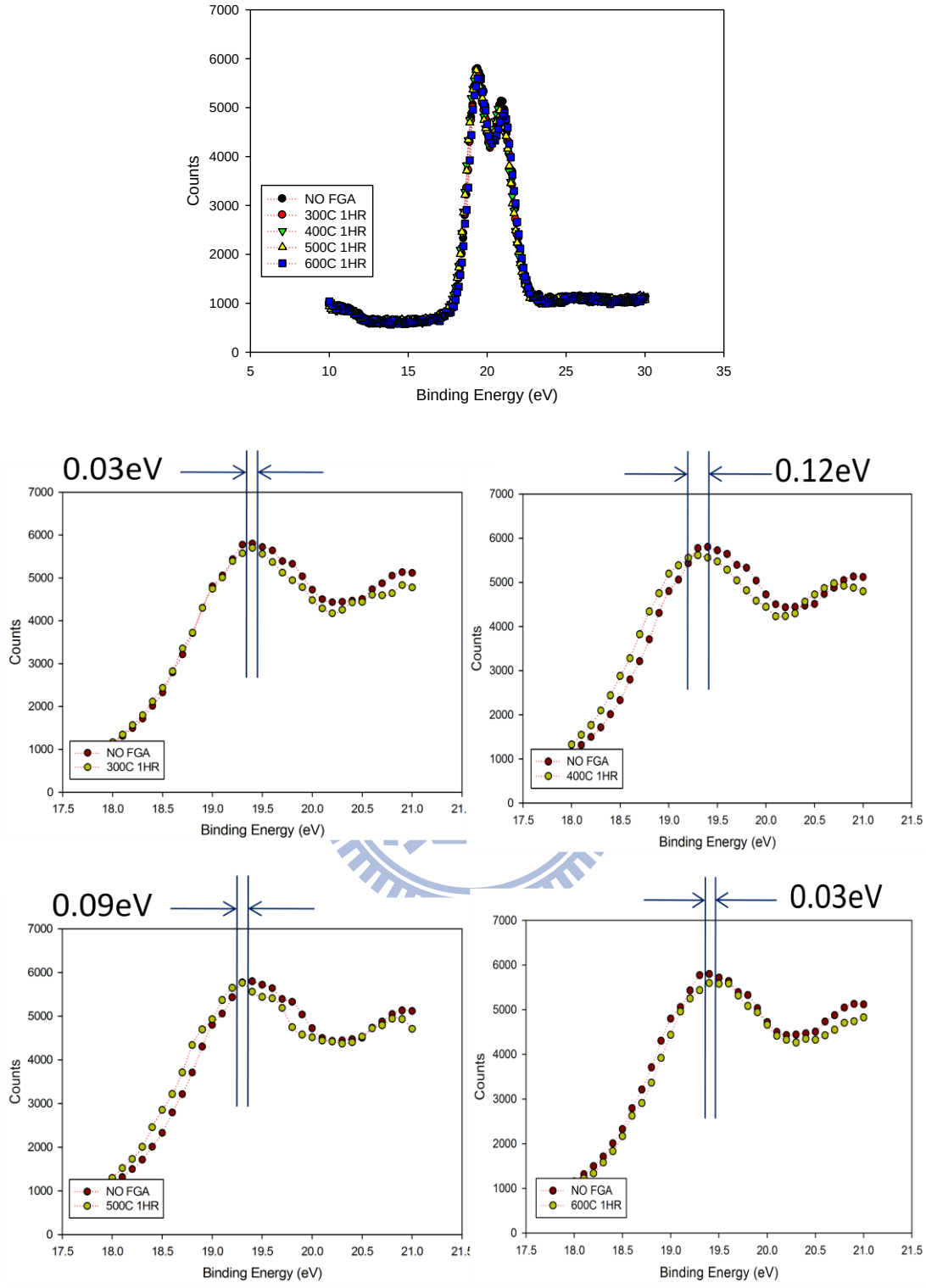


Fig. 3.11 XPS spectra of *Hf 4f* for HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 between HfO_2 trapping layer and top SiO_2 for different FGA temperature from 300°C to 600°C for 1hour.

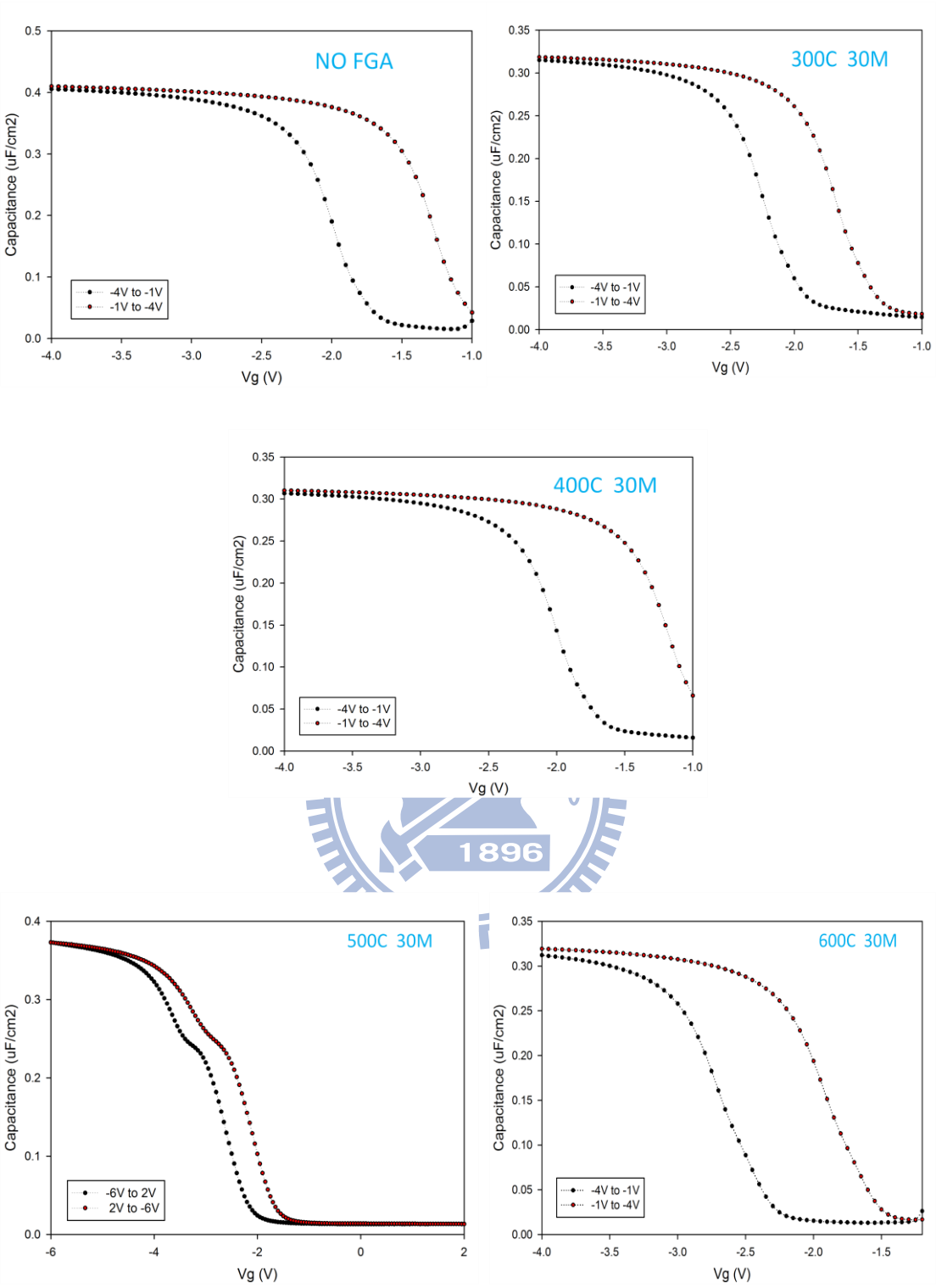


Fig. 3.12 CV characteristics of HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 between HfO_2 trapping layer and top SiO_2 for different FGA temperature from 300^{o}C to 600^{o}C for 1hour.

Table 3.4

HfO_2 Nanocrystal Capacitor (with top Al_2O_3)	
FGA Temperature	**CV Hysteresis**
NO FGA	0.71
300°C 1HR	0.52
400°C 1HR	0.81
500°C 1HR	0.49
600°C 1HR	0.78

Table 3.4 CV hysteresis of HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 between HfO_2 trapping layer and top SiO_2 for different FGA temperature from 300°C to 600°C for 1hour.

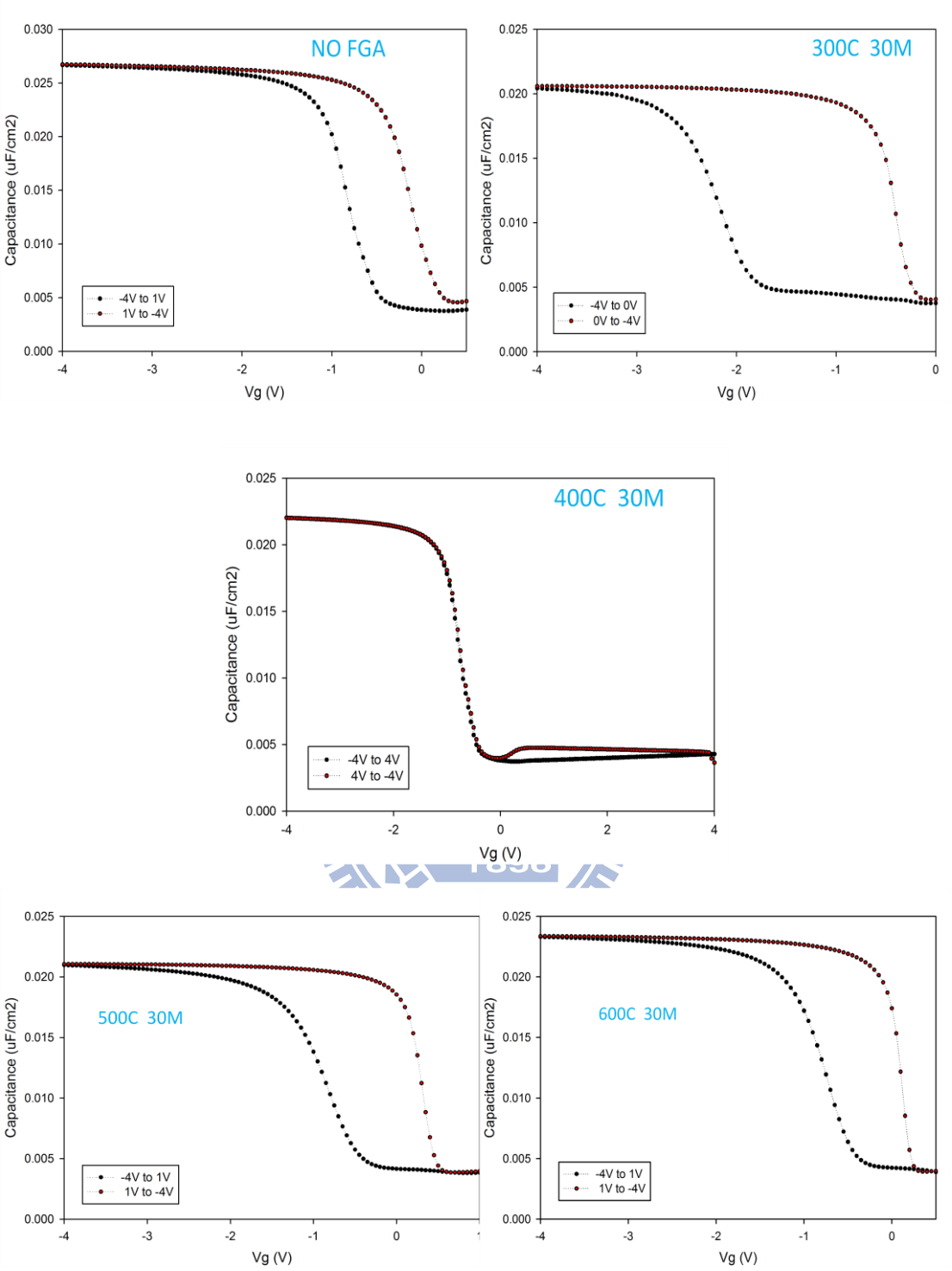


Fig. 3.13 CV characteristics of HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 both below and upon HfO_2 trapping layer for different FGA temperature from 300°C to 600°C for 1hour.

Table 3.5

HfO_2 Nanocrystal Capacitor (with bottom and top Al_2O_3)	
FGA Temperature	**CV Hysteresis**
NO FGA	0.70
300°C 1HR	1.73
400°C 1HR	0.03
500°C 1HR	1.11
600°C 1HR	0.80

Table 3.5 CV hysteresis of HfO_2 nanocrystal memory capacitor with ~1nm Al_2O_3 both below and upon HfO_2 trapping layer for different FGA temperature from 300°C to 600°C for 1hour.

Chapter 4
Dipole Layer Engineering in SONOS Nonvolatile Memory Devices

4.1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS), there are tough challenges for aggressively scaling down conventional floating-gate nonvolatile memory in sub-70nm node[77]. Therefore, SONOS-type (PolySi-Oxide-Nitride-Oxide-Silicon) flash memories, including nitride and nanocrystal memories, have recently attracted much attention in the next-generation nonvolatile memory for their capability of performing high P/E speed, low programming voltage, low power consumption, and good retention[78-84].

However, there are many concerns about these charge-trapping flash memories. As semiconductor technology becomes prosperous, pursuing high density and low cost per bit in nonvolatile memory application is inevitably important. So it is a major trend to scale down tunnel oxide thickness to improve P/E performance, and SILC happens to degenerate the reliability. Therefore, we get better operation performance at the cost of poor retention. So it's a crucial challenge to enhance P/E speed while maintaining sufficiently long retention time.

In this chapter, we demonstrate high performance SONOS nonvolatile memory devices with dipole layer engineering for high speed and good retention applications. By utilizing the concept of electric dipole discussed in chapter 3, we get higher programming speed but lower erasing speed in our novel memory structure compared to the conventional SONOS flash memory. Also, it shows retention enhancement in

SONOS-type nonvolatile memory with dipole layer engineering. The mechanism of operation is discussed in this chapter.

4.2 Experiment

A fabrication flow of the novel structure of SONOS nonvolatile memory device is demonstrated by a LOCOS isolation process on a p-type, 5~10 Ω cm, (100) 150-mm silicon substrate (Figure 4.1). First, a 2.5nm tunnel oxide is thermally grown in the horizontal furnace system. Then an ultra-thin high-k layer (HfO_2 or Al_2O_3) is deposited by MOCVD to form dipole layer. The flow rate and pulse number of precursors is carefully modulated to obtain ~1nm high-k film. Next a 12nm Si_3N_4 film is deposited by LPCVD. A 8nm blocking oxide is then deposited through TEOS precursor by LPCVD. Subsequently, poly-Si deposition, gate patterning, source/drain (S/D) implanting, and the remaining standard CMOS procedures are completed to fabricate novel SONOS-type nonvolatile memory devices.

4.3 Results and Discussions

4.3.1 Program/Erase Operation

Figure 4.2 and 4.3 illustrates cross-sectional TEM image of gate stacks of SONOS devices with ~1nm HfO_2 or Al_2O_3. Due to the challenge of forming the ultra-thin high-k layer by MOCVD system, a careful modulation of pulse number of precursors is therefore important. By both presetting the thickness of HfO_2 and Al_2O_3 to be 2nm, the actual thickness detected by TEM image is ~13A for HfO_2 and ~18A for Al_2O_3, respectively. And the thickness of the tunnel oxide, Si_3N_4 trapping layer, and blocking

oxide layer are 2nm, 12nm, and 8nm, respectively. Thus we successfully get the well-formed ultra-thin dipole layer in our SONOS-type flash memory structure. For the operation of our novel SONOS-type memory, we employ Fowler-Nordheim (FN) tunneling for programming and erasing, respectively. Figure 4.4 shows Ids-Vgs curves of the SONOS-type flash memory device with Al_2O_3 dipole layer engineering with programming time of 10us for different programming conditions. For Vg=12V and 14V, we get memory window of about 0.45V and 1.65V, respectively. A relatively large memory window of about 3V can be achieved with Vg=16V programming condition.

Figure 4.5 shows programming characteristics as a function of pulse width for different operation conditions. Source, drain, and substrate terminals are biased at 0V. The Vt shift is defined as the threshold voltage change of the device between programmed and erased states. We find out from this figure that the programming speed increases with the devices which have ultra-thin high-k layers in the gate stacks. Programming speed follows the trend: SONOS-Al_2O_3 > SONOS-HfO_2 > SONOS. With Vg=16V, relatively high speed (10us) programming performance can be achieved with a memory window of about 2.1V. Meanwhile, figure 4.6 illustrates erasing characteristics as a function of various operation conditions. Clearly, our novel SONOS-type flash memories show a slower erasing speed compared to the control SONOS device. Erasing speed follows the trend: SONOS > SONOS-HfO_2 > SONOS-Al_2O_3. Even though our proposed new structure of SONOS-type flash memory with dipole layer engineering enhances programming speed, the erasing speed decreases at the same time.

In 2008, *Y. N. Tan et al* utilizes dipole layer engineering in TANOS flash memory[85]. Dipole layer inserting at the tunnel oxide and charge trapping layer interface may induce dipole formation that shifts the bands of the nitride and blocking

oxide down relative to the tunnel oxide, as shown in the band diagram (figure 4.7)[85]. Therefore, programming speed can be enhanced at a given tunnel oxide electric field due to the lower barrier seen by the electrons for tunneling. In addition, dipole layer incorporation causes a slightly slower erasing speed because the nitride bands are shifted down relative to the tunnel oxide, as shown in figure 4.8[85]. As a result, this would increases the barrier for electrons out-tunneling from charge storage layer to p-Si substrate when erasing the cell. Also, the barrier for holes injection from Si substrate to nitride layer at a given tunnel oxide electric field is increased during erase. Thus a lower erasing speed is detected in our SONOS-type memory with dipole layer engineering.

4.3.2 Retention

The retention characteristics of our SONOS and SONOS-type memory with dipole layer engineering at room temperature (T=25^{o}C) are illustrated in figure 4.9. For SONOS device, it results in ~50% memory window loss for 10^{8} seconds retention time at room temperature. However, for SONOS-type devices with dipole layer engineering, the retention characteristics improve instead. The retention time can be up to 10^{8} seconds with ~34% window loss for SONOS-HfO_2 and ~19% loss for SONOS-Al_2O_3.

Figure 4.10 shows band diagrams of SONOS devices with dipole layer engineering during retention[85]. By introducing dipole layer into SONOS-type memory devices, the nitride band is shifted down with respect to tunnel oxide. This would lead to a higher energy barrier for electrons out-tunneling from the charge storage layer to the silicon substrate during retention. Hence a longer retention time is expected for our novel structure of SONOS-type nonvolatile memory with an ultra-thin high-k layer

(HfO_2 or Al_2O_3) inserted.

4.3.3 Endurance

Figure 4.11 shows endurance characteristics of SONOS combined with SONOS-type flash memory devices with dipole layer engineering. From this figure, the individual threshold voltage shift becomes visible after 10^4 program/erase cycles. The high enough P/E cycles make this new structure of SONOS-type memory applicable in nonvolatile memory devices.

4.4 Summary

In this chapter, we propose a novel, simple, reproducible, and reliable structure of SONOS-type flash memory with high-k (HfO_2 or Al_2O_3) layer inserting between charge storage layer and tunnel oxide. SONOS-type memory device with dipole layer engineering may induce dipole formation that shifts the bands of nitride and blocking oxide down relative to the tunnel oxide at a given tunnel oxide electric field. Hence a higher programming speed is expected but a slightly lower erasing speed is resulted due to the higher barrier seen by the electrons for out-tunneling during erase. We get a longer retention time in this type of memory owing to the higher barrier seen by the electrons in charge storage layer during retention discharge. Thus a higher programming speed is realized while maintaining sufficiently long retention time. As a result, we believe that SONOS-type flash memory with dipole layer engineering has a great potential to be a candidate for the next-generation nonvolatile memory applications.

- Thermal oxide : 2.5nm
- High-k layer (HfO_2 or Al_2O_3) : ~1nm
- Si_3N_4 : 12nm
- TEOS SiO_2 : 7nm
- Poly gate : 200nm
- n^+ Source/Drain
- Passivation
- Metallization

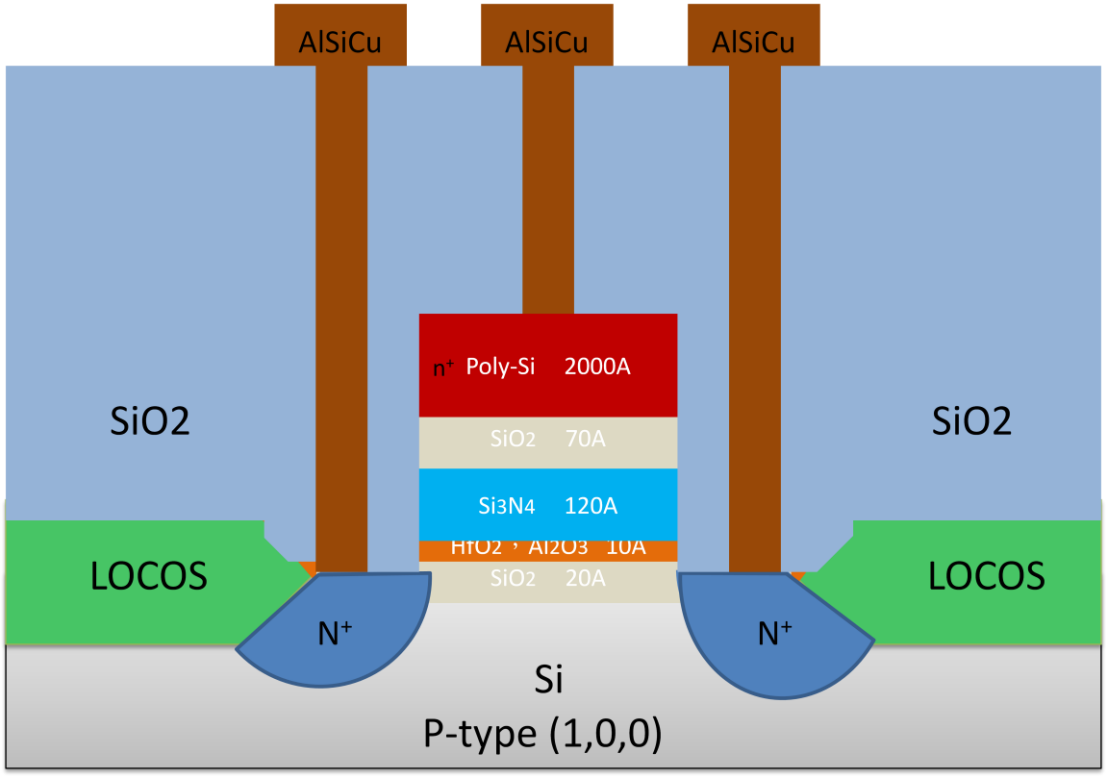


Fig. 4.1 Schematic of novel SONOS flash memory structure with dipole layer engineering.

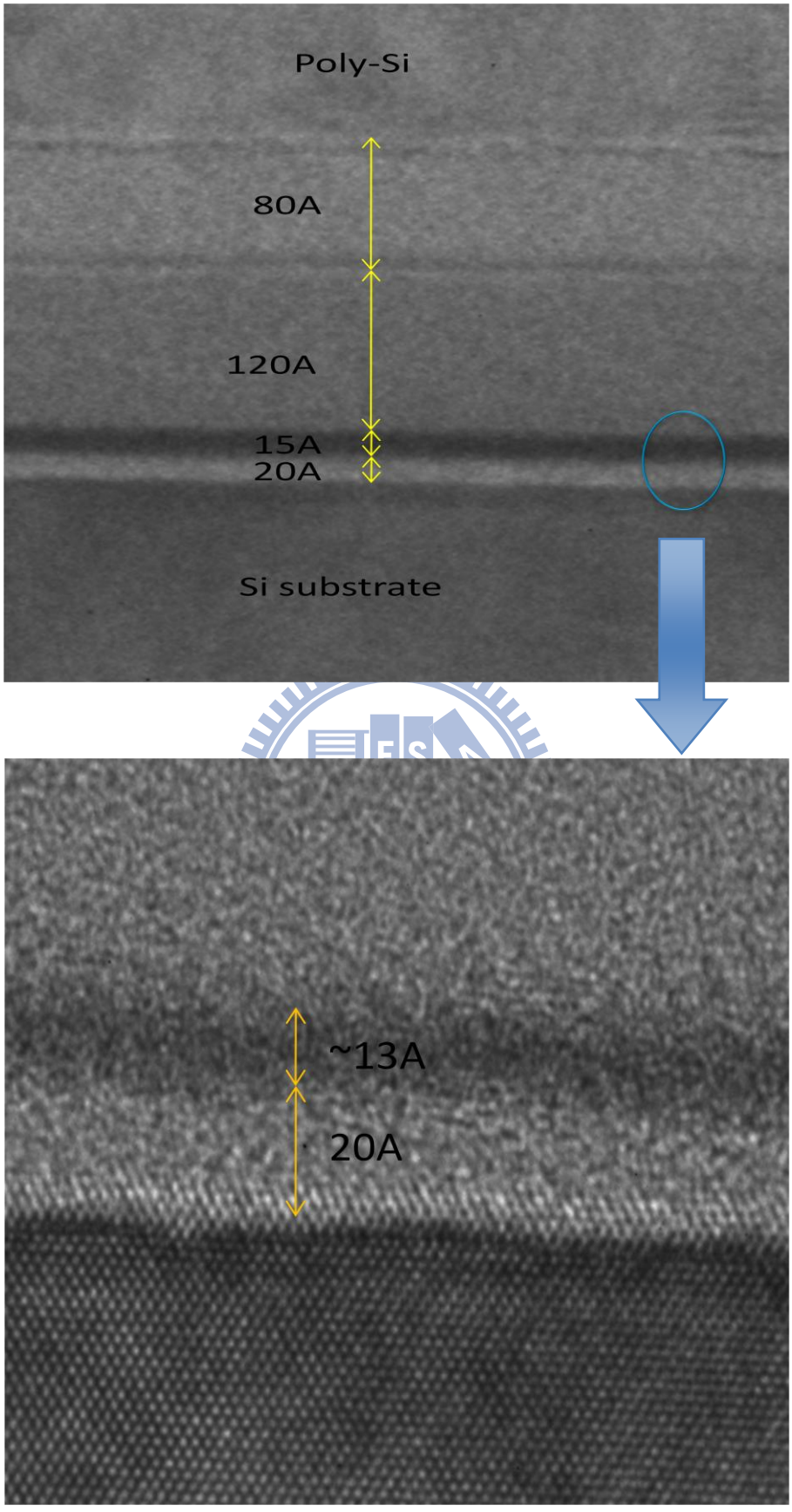


Fig. 4.2 Cross-sectional TEM image of $Si/SiO_2/HfO_2/Si_3N_4/SiO_2$/poly-Si. The ultra-thin HfO_2 layer is well formed upon the bottom SiO_2.

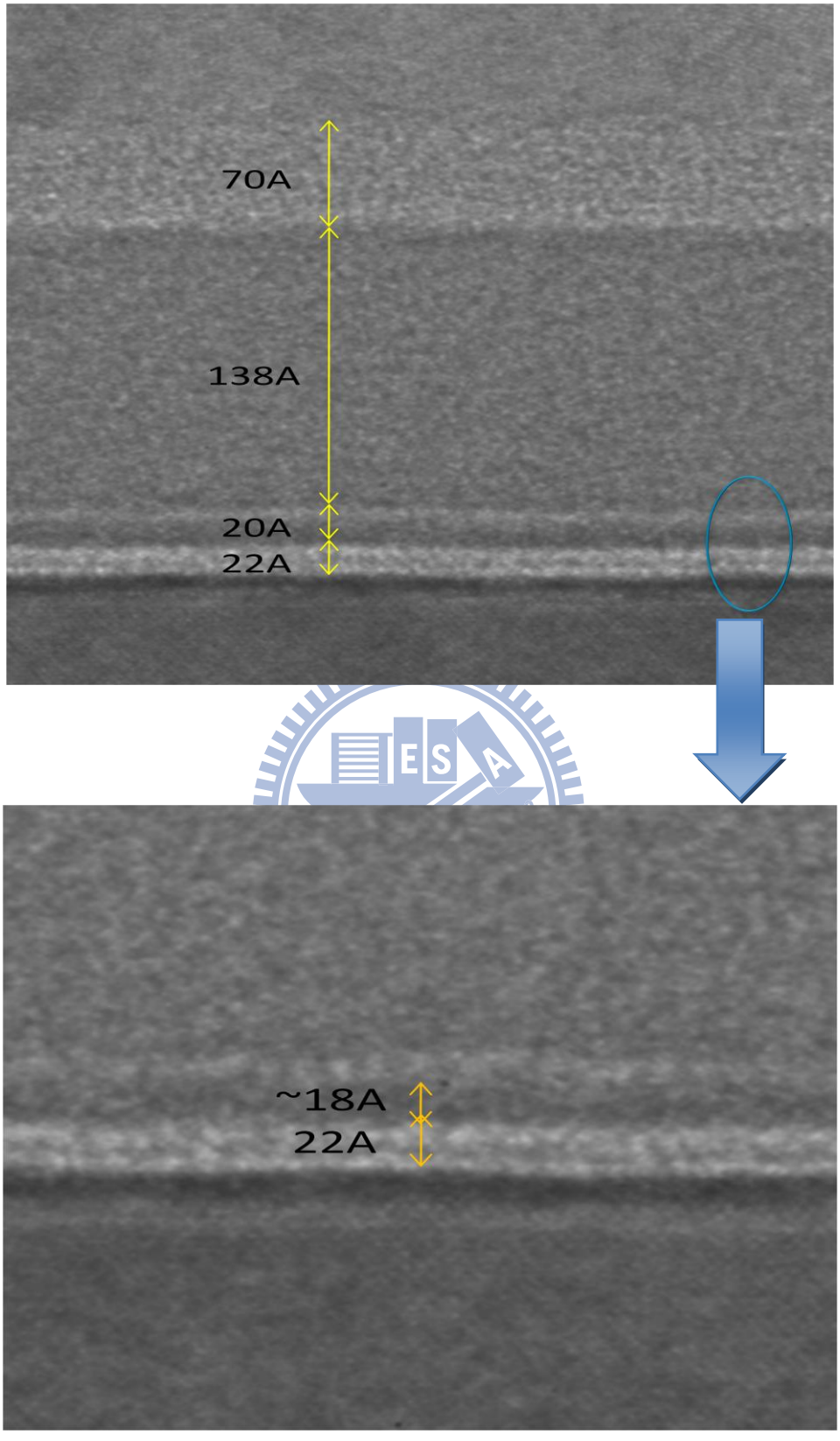


Fig. 4.3 Cross-sectional TEM image of $Si/SiO_2/Al_2O_3/Si_3N_4/SiO_2$/poly-Si. The ultra-thin Al_2O_3 layer is well formed upon the bottom SiO_2.

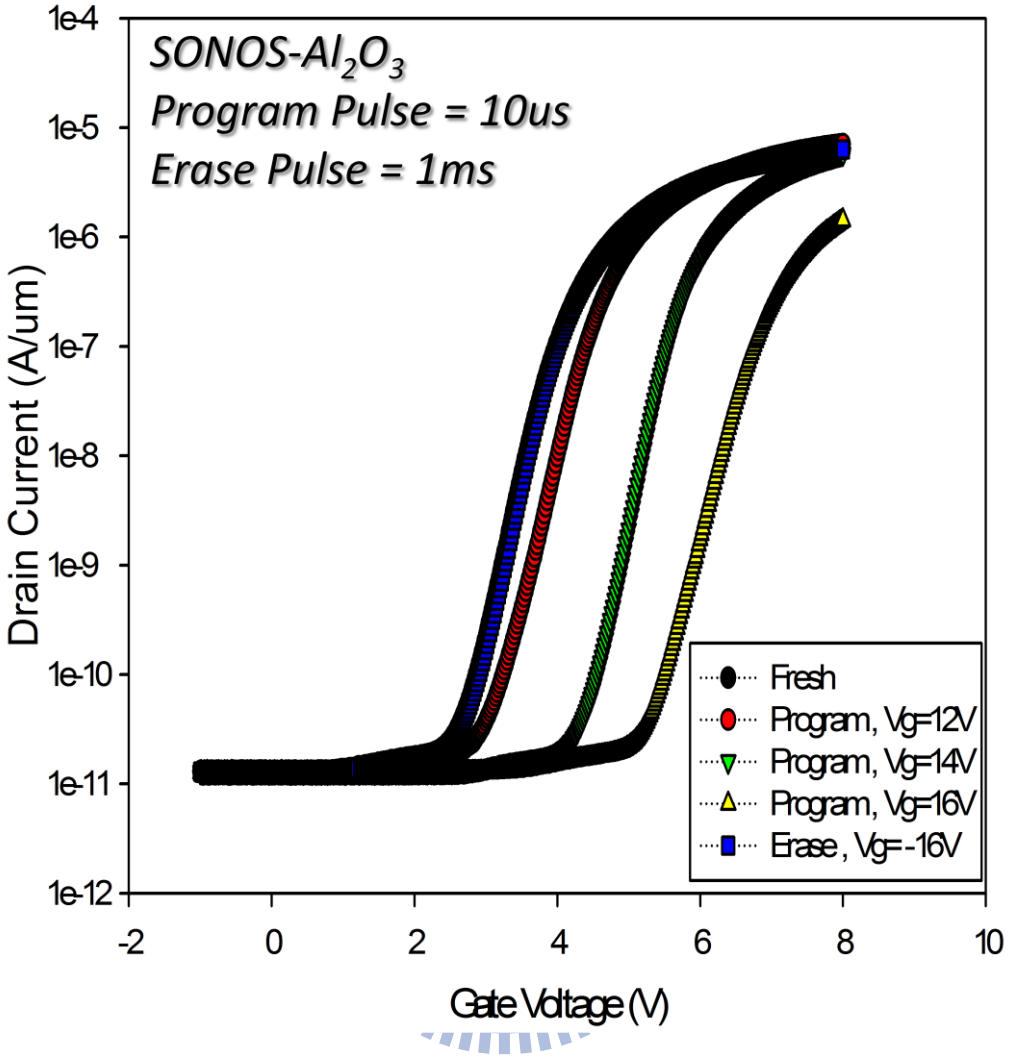


Fig. 4.4 Ids-Vgs curves for SONOS-type flash memory devices with Al_2O_3 dipole layer engineering for different programming conditions.

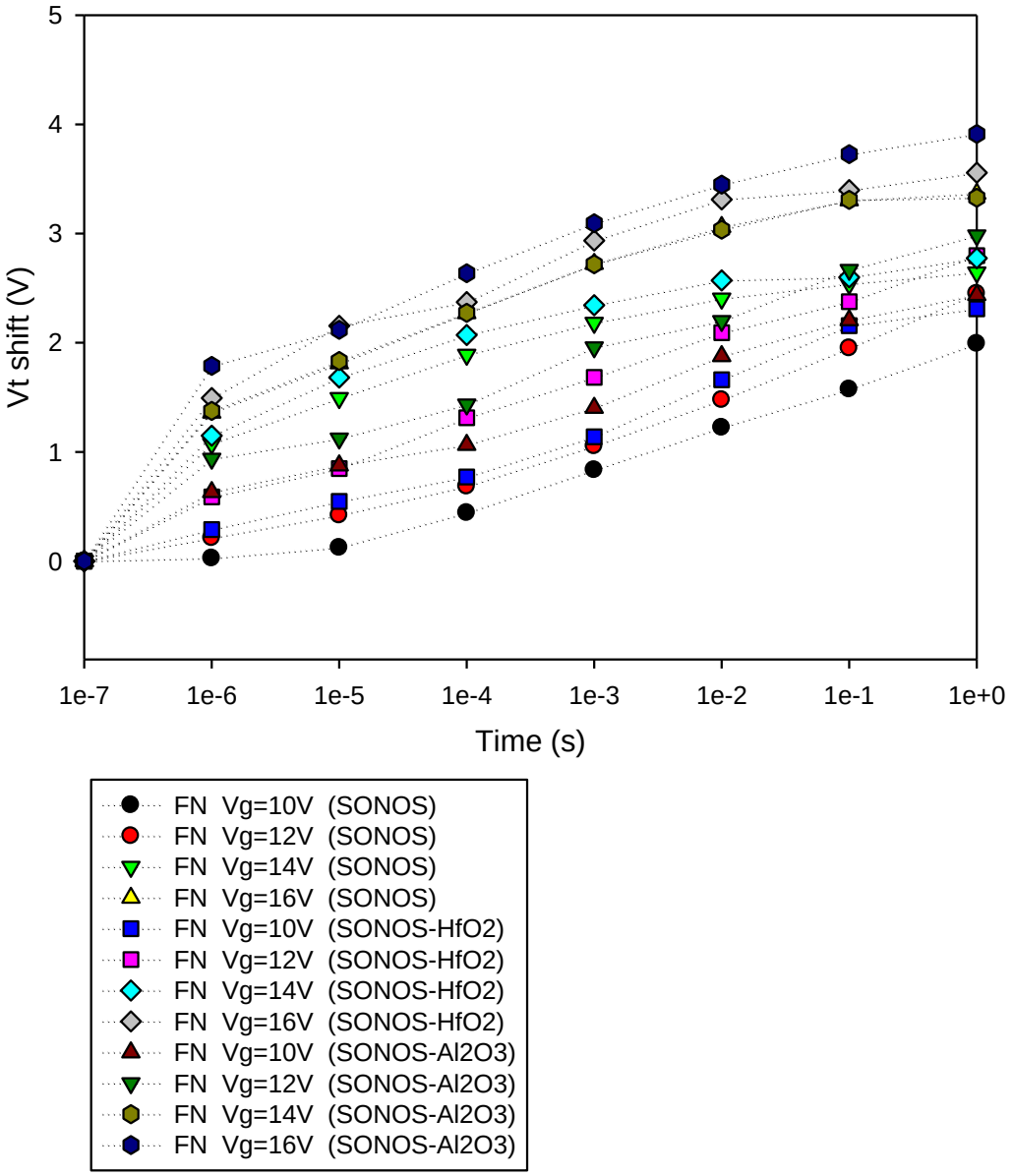


Fig. 4.5 Programming characteristics of our SONOS-type memories as a function of pulse width for different operation conditions.

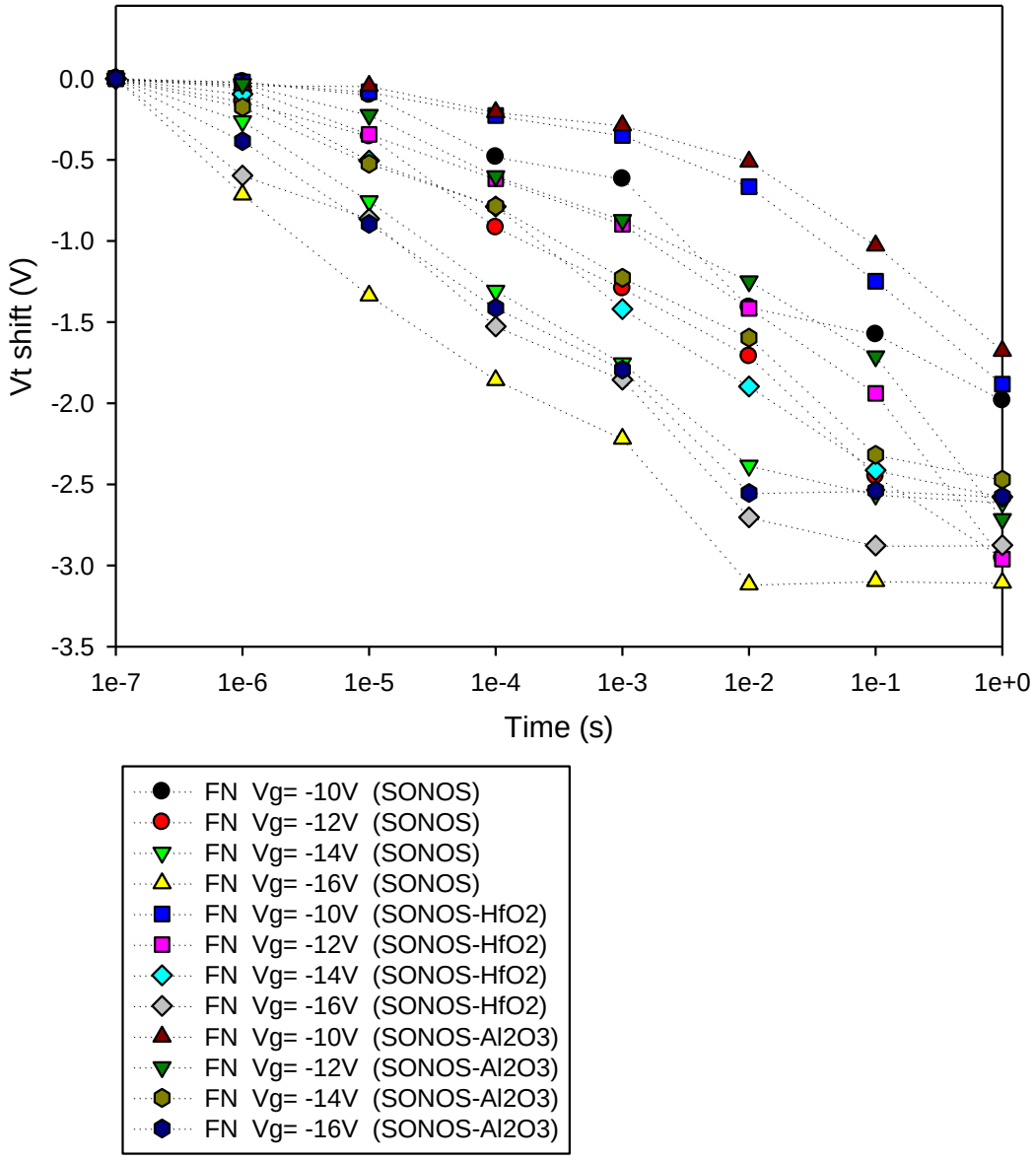


Fig. 4.6 Schematic of erasing characteristics of our novel SONOS-type flash memories with various operation conditions.

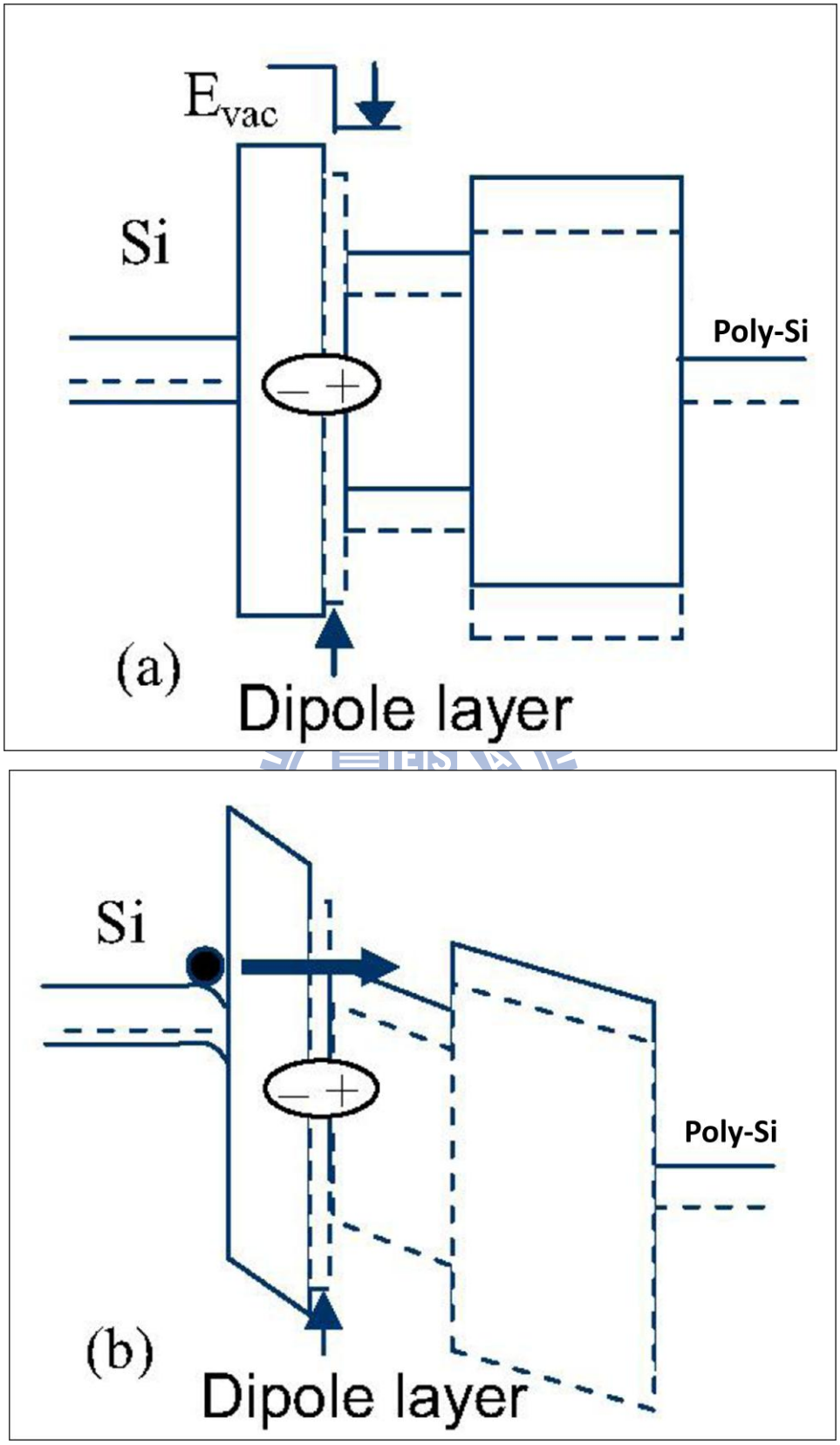


Fig. 4.7 (a)Dipole layer causes charge trapping layer bands to be shifted down with respected to tunnel oxide. (b)Using a dipole layer is expected to result in easier programming at a given tunnel oxide electric field[85].

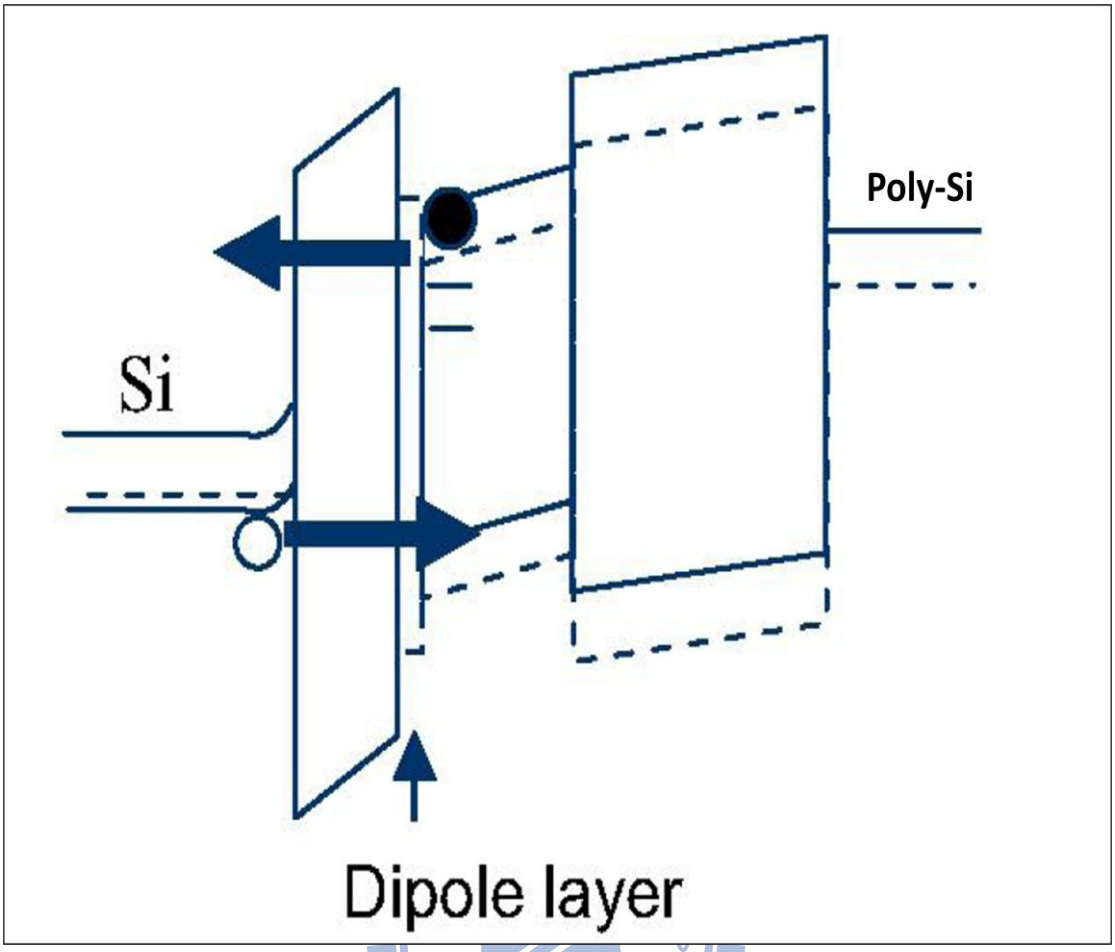


Fig. 4.8 Dipole layer incorporation causes a slightly slower erase at a given tunnel oxide electric field as the nitride bands are shifted down with respect to the tunnel oxide[85].

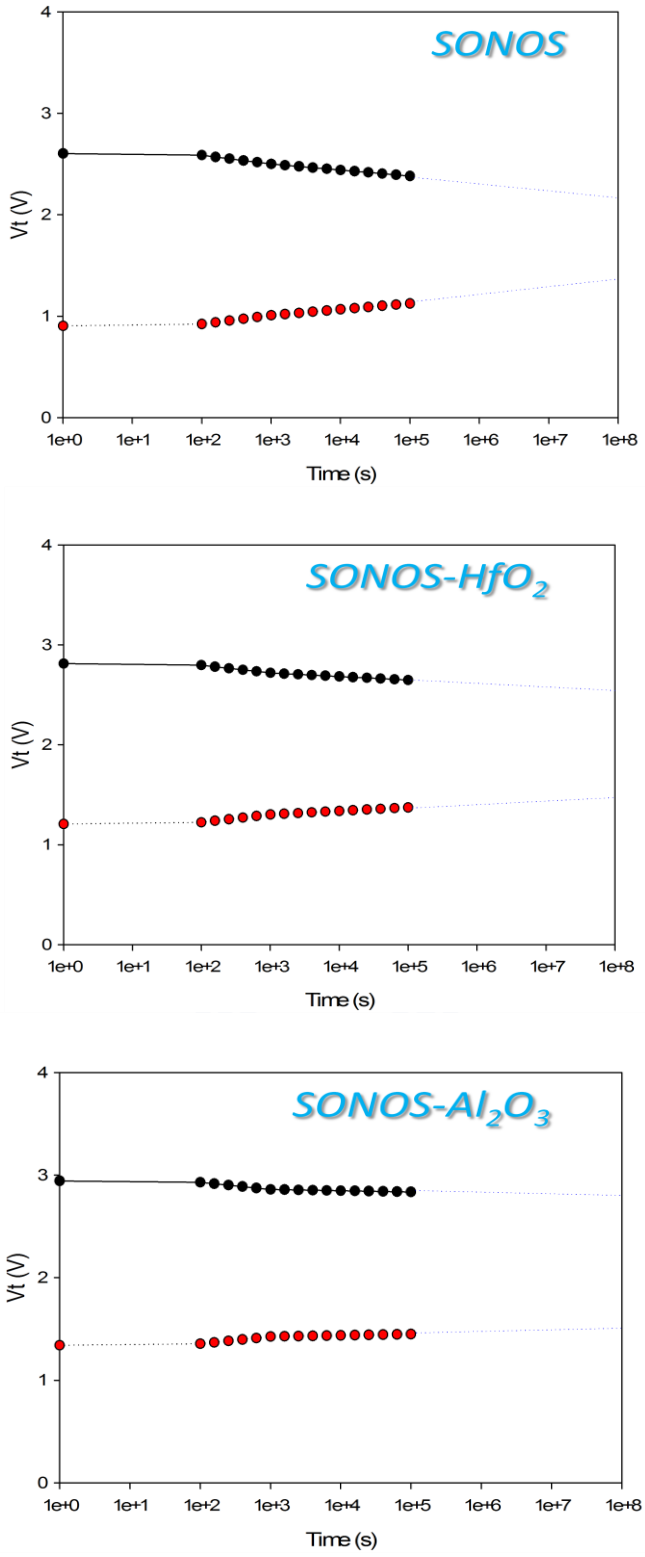


Fig. 4.9 Retention characteristics of SONOS and SONOS-type flash memory with dipole layer engineering at T=25^{o}C.

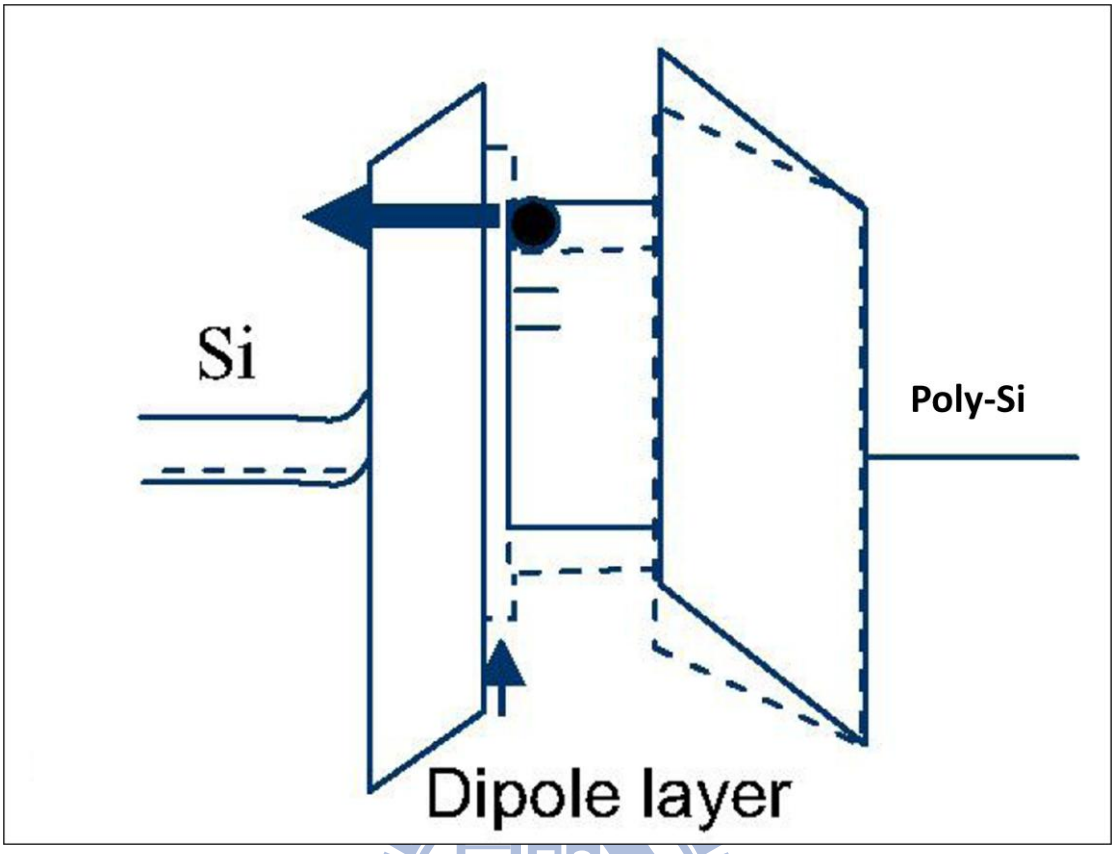


Fig. 4.10 Band diagram of SONOS-type flash memory with dipole layer engineering during retention[85].

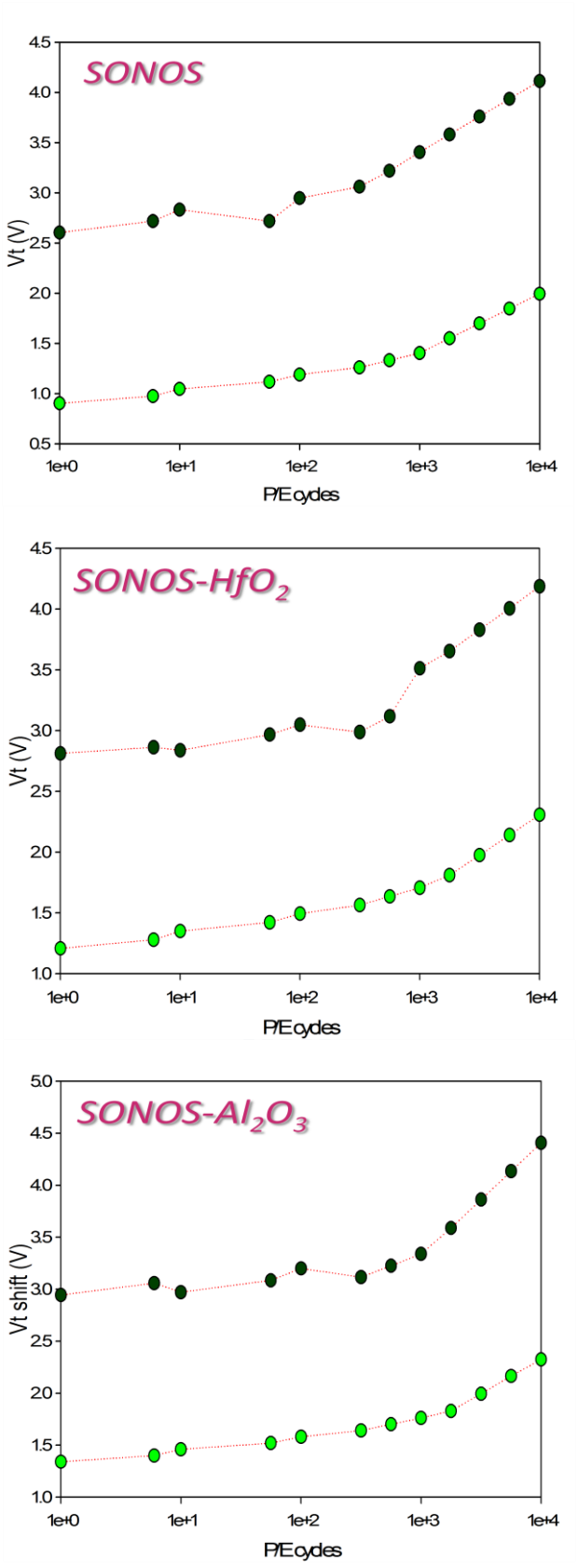


Fig. 4.11 Schematic of endurance characteristics of SONOS and SONOS-type memory with dipole layer engineering.

Chapter 5
Conclusions

In this thesis for chapter 2, we studied the effect of FGA-generated oxygen vacancies on HfO_2 thin film and nanocrystal memory capacitors. The large memory window of about 1.32V can be achieved by FGA temperature of 300^{o}C for 30min in HfO_2 thin film memory capacitor. And we also find out that oxygen vacancies are hard to generate by FGA in Al_2O_3 memory capacitors. Also we fabricate HfO_2 nanocrystal memory capacitor through the spinodal decomposition of hafnium silicate. We get the highest CV hysteresis of 1.34V by FGA of 500^{o}C for 1hour, which is slightly larger than the HfO_2 thin film capacitors for 300^{o}C, 30min case.

In chapter 3, effects of electric dipole on HfO_2 thin film and nanocrystal memory capacitors are studied. From CV characteristics of SONOS-like memory capacitor with an ultra-thin dipole layer (HfO_2 or Al_2O_3), we observe a distinct flat-band voltage shift with Al_2O_3-inserted memory capacitor. By incorporating dipole layer at different position and appropriate FGA temperature, we may get a sufficiently large CV hysteresis from both HfO_2 thin film and nanocrystal memory capacitors.

In chapter 4, we propose a novel, simple, reproducible, and reliable structure of SONOS-type flash memory devices with dipole layer engineering. A higher programming speed due to the lower barrier seen by the electrons for tunneling is achieved. However, we observe a slightly lower erasing speed owing to the higher barrier seen by the electrons at charge storage layer during erase. Also we detect a longer retention time as a result of the higher barrier for electrons to out-tunneling during retention discharge. Therefore, we achieve high programming speed while maintaining sufficiently long retention time. SONOS-type flash memory with dipole

layer engineering has a potential to be a candidate for next-generation nonvolatile memory applications.

References

[1] K. Kahng and S. M. Sze, "A floating gate and its application to memory devices," *Electron Devices, IEEE Transactions on*, vol. 14, pp. 629-629, 1967.

[2] H. B. Pein and J. D. Plummer, "Performance of the 3-D sidewall flash EPROM cell," in *Electron Devices Meeting, 1993. IEDM '93. Technical Digest., International*, 1993, pp. 11-14.

[3] F. Masuoka, M. Momodomi, Y. Iwata, and R. Shirota, "New ultra high density EPROM and flash EEPROM with NAND structure cell," in *Electron Devices Meeting, 1987 International*, 1987, pp. 552-555.

[4] A. Fazio, "A high density high performance 180 nm generation Etox™ flash memory technology," in *Electron Devices Meeting, 1999. IEDM Technical Digest. International*, 1999, pp. 267-270.

[5] G. Verma and N. Mielke, "Reliability performance of ETOX based flash memories," in *Reliability Physics Symposium 1988. 26th Annual Proceedings., International*, 1988, pp. 158-166.

[6] D. Frohman-Bentchkowsky and M. Lenzlinger, "Charge Transport and Storage in Metal-Nitride-Oxide-Silicon (MNOS) Structures," *Journal of Applied Physics*, vol. 40, pp. 3307-3319, 1969.

[7] M. H. White and J. R. Cricchi, "Characterization of thin-oxide MNOS memory transistors," *Electron Devices, IEEE Transactions on*, vol. 19, pp. 1280-1288, 1972.

[8] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *Circuits and Devices Magazine, IEEE*, vol. 16, pp. 22-31, 2000.

[9] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," *Electron Device Letters, IEEE*, vol. 21, pp. 543-545, 2000.

[10] R. Muralidhar, R. F. Steimle, M. Sadd, R. Rao, C. T. Swift, E. J. Prinz, J. Yater, L. Grieve, K. Harber, B. Hradsky, S. Straub, B. Acred, W. Paulson, W. Chen, L. Parker, S. G. H. Anderson, M. Rossow, T. Merchant, M. Paransky, T. Huynh, D. Hadad, C. Ko-Min, and B. E. White, Jr., "A 6 V embedded 90 nm silicon nanocrystal nonvolatile memory," in *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, 2003, pp. 26.2.1-26.2.4.

[11] L. Yu-Hsien, C. Chao-Hsin, L. Ching-Tzung, C. Ching-Wei, C. Chun-Yen, and L. Tan-Fu, "High performance multi-bit nonvolatile HfO_2 nanocrystal memory using spinodal phase separation of hafnium silicate," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp.

1080-1082.

[12] R. Degraeve, B. Kaczer, and G. Groeseneken, "Ultra-thin oxide reliability: searching for the thickness scaling limit," *Microelectronics Reliability*, vol. 40, pp. 697-701, 2000.

[13] W. J. Tsai, N. K. Zous, C. J. Liu, C. C. Liu, C. H. Chen, W. Tahui, S. Pan, L. Chih-Yuan, and S. H. Gu, "Data retention behavior of a SONOS type two-bit storage flash memory cell," in *Electron Devices Meeting, 2001. IEDM Technical Digest. International*, 2001, pp. 32.6.1-32.6.4.

[14] J. Bu and M. H. White, "Design considerations in scaled SONOS nonvolatile memory devices," *Solid-State Electronics*, vol. 45, pp. 113-120, 2001.

[15] J. Buckley, B. D. Salvo, G. Ghibaudo, M. Gely, J. F. Damlencourt, F. Martin, G. Nicotra, and S. Deleonibus, "Investigation of SiO2/HfO2 gate stacks for application to non-volatile memory devices," *Solid-State Electronics*, vol. 49, pp. 1833-1840, 2005.

[16] T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, "Novel multi-bit SONOS type flash memory using a high-k charge trapping layer," in *VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on*, 2003, pp. 27-28.

[17] O. Chang Woo, K. Sung Hwan, K. Na Young, C. Yong Lack, L. Kwan Heum, K. Byeong Soo, C. Nam Myun, K. Seung Beom, K. Dong-Won, P. Donggun, and R. Byung-Il, "A 4-Bit Double SONOS Memory (DSM) with 4 Storage Nodes per Cell for Ultimate Multi-Bit Operation," in *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 40-41.

[18] L. Sheng-Chih, L. Hang-Ting, Y. Ming-Jui, H. Jung-Yu, W. Szu-Yu, W. Tai-Bor, L. Guang-Li, C. Chao-Hsin, L. Erh-Kun, H. Kuang-Yeu, R. Liu, and L. Chin-Yuan, "MA BE-SONOS: A Bandgap Engineered SONOS using Metal Gate and Al2O3 Blocking Layer to Overcome Erase Saturation," in *Non-Volatile Semiconductor Memory Workshop, 2007 22nd IEEE*, 2007, pp. 88-89.

[19] W. J. Tsai, S. H. Gu, N. K. Zous, C. C. Yeh, C. C. Liu, C. H. Chen, W. Tahui, S. Pan, and L. Chih-Yuan, "Cause of data retention loss in a nitride-based localized trapping storage flash memory cell," in *Reliability Physics Symposium Proceedings, 2002. 40th Annual*, 2002, pp. 34-38.

[20] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, "Volatile and non-volatile memories in silicon with nano-crystal storage," in *Electron Devices Meeting, 1995., International*, 1995, pp. 521-524.

[21] W. K. Choi, W. K. Chim, C. L. Heng, L. W. Teo, V. Ho, V. Ng, D. A. Antoniadis, and E. A. Fitzgerald, "Observation of memory effect in

germanium nanocrystals embedded in an amorphous silicon oxide matrix of a metal--insulator-- semiconductor structure," *Applied Physics Letters*, vol. 80, pp. 2014-2016, 2002.

[22] T. Baron, B. Pelissier, L. Perniola, F. Mazen, J. M. Hartmann, and G. Rolland, "Chemical vapor deposition of Ge nanocrystals on SiO_2," *Applied Physics Letters*, vol. 83, pp. 1444-1446, 2003.

[23] C. Bonafos, M. Carrada, N. Cherkashin, H. Coffin, D. Chassaing, G. B. Assayag, A. Claverie, T. Muller, K. H. Heinig, M. Perego, M. Fanciulli, P. Dimitrakis, and P. Normand, "Manipulation of two-dimensional arrays of Si nanocrystals embedded in thin SiO_2 layers by low energy ion implantation," *Journal of Applied Physics*, vol. 95, pp. 5696-5702, 2004.

[24] S. Guha, S. B. Qadri, R. G. Musket, M. A. Wall, and T. Shimizu-Iwayama, "Characterization of Si nanocrystals grown by annealing SiO_2 films with uniform concentrations of implanted Si," *Journal of Applied Physics*, vol. 88, pp. 3954-3961, 2000.

[25] K. Ya-Chin, K. Tsu-Jae, and H. Chenming, "Charge-trap memory device fabricated by oxidation of Si_{1-x} Ge_x," *Electron Devices, IEEE Transactions on*, vol. 48, pp. 696-700, 2001.

[26] J. De Blauwe, M. Ostraat, M. L. Green, G. Weber, T. Sorsch, A. Kerber, F. Klemens, R. Cirelli, E. Ferry, J. L. Grazul, F. Baumann, Y. Kim, W. Mansfield, J. Bude, J. T. C. Lee, S. J. Hillenius, R. C. Flagan, and H. A. Atwater, "A novel, aerosol-nanocrystal floating-gate device for non-volatile memory applications," in *Electron Devices Meeting, 2000. IEDM Technical Digest. International*, 2000, pp. 683-686.

[27] S. Das, K. Das, R. K. Singha, A. Dhar, and S. K. Ray, "Improved charge injection characteristics of Ge nanocrystals embedded in hafnium oxide for floating gate devices," *Applied Physics Letters*, vol. 91, pp. 233118-3, 2007.

[28] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystal memories. I. Device design and fabrication," *Electron Devices, IEEE Transactions on*, vol. 49, pp. 1606-1613, 2002.

[29] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystal memories-part II: electrical characteristics," *Electron Devices, IEEE Transactions on*, vol. 49, pp. 1614-1622, 2002.

[30] J. de Blauwe, J. van Heudt, D. Wellekens, G. Groeseneken, and H. E. Maes, "SILC-related effects in flash E^2PROM's-Part I: A quantitative model for steady-state SILC," *Electron Devices, IEEE Transactions on*, vol. 45, pp. 1745-1750, 1998.

[31] L. Jong Jin, W. Xuguang, B. Weiping, L. Nan, and K. Dim-Lee, "Theoretical

and experimental investigation of Si nanocrystal memory device with HfO_2 high-k tunneling dielectric," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 2067-2072, 2003.

[32] L. Jong Jin and K. Dim-Lee, "Metal nanocrystal memory with high-k; tunneling barrier for improved data retention," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 507-511, 2005.

[33] L. Yu-Hsien, C. Chao-Hsin, L. Ching-Tzung, C. Chun-Yen, and L. Tan-Fu, "High-performance nonvolatile HfO_2 nanocrystal memory," *Electron Device Letters, IEEE,* vol. 26, pp. 154-156, 2005.

[34] C. Myung Kwan and D. M. Kim, "High performance SONOS memory cells free of drain turn-on and over-erase: compatibility issue with current flash technology," *Electron Device Letters, IEEE,* vol. 21, pp. 399-401, 2000.

[35] C. Jing Hao, W. Ying Qian, Y. Won Jong, Y. Yee-Chia, G. Samudra, D. S. Chan, D. An Yan, and K. Dim-Lee, "Nonvolatile flash memory device using Ge nanocrystals embedded in HfAlO high-k tunneling and control oxides: Device fabrication and electrical performance," *Electron Devices, IEEE Transactions on,* vol. 51, pp. 1840-1848, 2004.

[36] C.-H. Tu, T.-C. Chang, P.-T. Liu, H.-C. Liu, S. M. Sze, and C.-Y. Chang, "Improved memory window for Ge nanocrystals embedded in SiON layer," *Applied Physics Letters,* vol. 89, pp. 162105-3, 2006.

[37] T. Z. Lu, M. Alexe, R. Scholz, V. Talelaev, and M. Zacharias, "Multilevel charge storage in silicon nanocrystal multilayers," *Applied Physics Letters,* vol. 87, pp. 202110-3, 2005.

[38] T. Yan Ny, W. K. Chim, C. Wee Kiong, J. Moon Sig, and C. Byung Jin, "Hafnium aluminum oxide as charge storage and blocking-oxide layers in SONOS-type nonvolatile memory for high-speed operation," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 654-662, 2006.

[39] H. Choi, S.-J. Jung, H. Park, J.-M. Lee, M. Kwon, M. Chang, M. Hasan, S. Choi, and H. Hwang, "Formation of TaN nanocrystals embedded in silicon nitride by phase separation methods for nonvolatile memory applications," *Applied Physics Letters,* vol. 91, pp. 052905-3, 2007.

[40] C. Sangmoo, C. Hyejung, K. Tae-Wook, Y. Hyundeok, L. Takhee, J. Sanghun, K. Chungwoo, and H. Hyunsang, "High density silicon nanocrystal embedded in sin prepared by low energy (<500eV) SiH_4 plasma immersion ion implantation for non-volatile memory applications," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 166-169.

[41] T. Ping-Hung, C.-L. Kuei-Shu, L. Chu-Yung, W. Tien-Ko, P. J. Tzeng, L. S.

Lee, and M. J. Tsai, "Novel SONOS-Type Nonvolatile Memory Device with Suitable Band Offset in HfAlO Charge-Trapping Layer," in *VLSI Technology, Systems and Applications, 2007. VLSI-TSA 2007. International Symposium on*, 2007, pp. 1-2.

[42] W. J. Zhu, M. Tso-Ping, T. Tamagawa, J. Kim, and Y. Di, "Current transport in metal/hafnium oxide/silicon structure," *Electron Device Letters, IEEE,* vol. 23, pp. 97-99, 2002.

[43] F. Irrera, "Engineered Barriers With Hafnium Oxide for Nonvolatile Application," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 2418-2422, 2006.

[44] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyow, H. Kitajima, T. Arikado, and Y. Nara, "Oxygen-vacancy-induced threshold voltage shifts in Hf-related high-k gate stacks," *Thin Solid Films,* vol. 508, pp. 305-310, 2006.

[45] H. Takeuchi, D. Ha, and T.-J. King, "Observation of bulk HfO_2 defects by spectroscopic ellipsometry," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 22, pp. 1337-1341, 2004.

[46] W. L. Scopel, A. J. R. da Silva, W. Orellana, and A. Fazzio, "Comparative study of defect energetics in HfO_2 and SiO_2," *Applied Physics Letters,* vol. 84, pp. 1492-1494, 2004.

[47] J. Robertson, X. Ka, and T. Koon-yiu, "Importance of Oxygen Vacancies in High K Gate Dielectrics," in *Integrated Circuit Design and Technology, 2007. ICICDT '07. IEEE International Conference on*, 2007, pp. 1-4.

[48] K. Shiraishi, "Interface properties of Hf-based high-k gate dielectrics -O vacancies and interface reaction-" in *Physics of Semiconductor Devices, 2007. IWPSD 2007. International Workshop on*, 2007, pp. 37-41.

[49] G. Bersuker, J. Sim, P. Chang Seo, C. Young, S. Nadkarni, C. Rino, and L. Byoung Hun, "Mechanism of Electron Trapping and Characteristics of Traps in HfO_2 Gate Stacks," *Device and Materials Reliability, IEEE Transactions on,* vol. 7, pp. 138-145, 2007.

[50] E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, and G. Shahidi, "Role of oxygen vacancies in V_{FB}/V_t stability of pFET metals on HfO_2," in *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, 2005, pp. 230-231.

[51] Y. Ito, K. Suzuki, and H. Miura, "Quantum chemical molecular dynamics analysis of the effect of oxygen vacancies and strain on dielectric

characteristic of HfO_{2-x} films," in *Simulation of Semiconductor Processes and Devices, 2006 International Conference on*, 2006, pp. 150-153.

[52] K. Akiyama, W. Wang, W. Mizubayashi, M. Ikeda, H. Ota, T. Nabatame, and A. Toriumi, "Roles of oxygen vacancy in HfO_2/ultra-thin SiO_2 gate stacks - Comprehensive understanding of V_{FB} roll-off," in *VLSI Technology, 2008 Symposium on*, 2008, pp. 80-81.

[53] H. Takeuchi, W. Hiu Yung, H. Daewon, and K. Tsu-Jae, "Impact of oxygen vacancies on high-κ gate stack engineering," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 829-832.

[54] P. Hokyung, J. Minseok, C. Hyejung, M. Hasan, C. Rino, P. D. Kirsch, K. Chang Young, L. Byoung Hun, K. Tae-Wook, L. Takhee, and H. Hyunsang, "The Effect of Nanoscale Nonuniformity of Oxygen Vacancy on Electrical and Reliability Characteristics of HfO_2 MOSFET Devices," *Electron Device Letters, IEEE*, vol. 29, pp. 54-56, 2008.

[55] Y. Kamimuta, K. Iwamoto, Y. Nunoshige, A. Hirano, W. Mizubayashi, Y. Watanabe, S. Migita, A. Ogawa, H. Ota, T. Nabatame, and A. Toriumi, "Comprehensive Study of V_{FB} Shift in High-k CMOS - Dipole Formation, Fermi-level Pinning and Oxygen Vacancy Effect," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 341-344.

[56] B. Torsten, S. Bernd, I. Ken-ichi, G. David, B. Cedric, A. Heinz, A. Markus, and S. Clement, "Self-Assembly and Crystallization Behavior of Mesoporous, Crystalline HfO_2 Thin Films: A Model System for the Generation of Mesostructured Transition-Metal Oxides," *Small*, vol. 1, pp. 889-898, 2005.

[57] W. Swiatnicki, S. Lartigue-Korinek, and J. Y. Laval, "Grain boundary structure and intergranular segregation in Al2O3," *Acta Metallurgica et Materialia*, vol. 43, pp. 795-805, 1995.

[58] J. Carrasco, N. Lopez, and F. Illas, "First Principles Analysis of the Stability and Diffusion of Oxygen Vacancies in Metal Oxides," *Physical Review Letters*, vol. 93, p. 225502, 2004.

[59] S. Maikap, P. J. Tzeng, L. S. Lee, H. Y. Lee, C. C. Wang, P. H. Tsai, K. S. Chang-Liao, W. J. Chen, K. C. Liu, P. R. Jeng, and M. J. Tsai, "High-K Hf-based charge trapping layer with Al_2O_3 blocking oxide for high-density flash memory," in *VLSI Technology, Systems, and Applications, 2006 International Symposium on*, 2006, pp. 1-2.

[60] S. S, C. Z, L. C. G, L. P. S, F. B, G. J. A, and T. J. R, "Application of Metastable Phase Diagrams to Silicate Thin Films for Alternative Gate Dielectrics," *Jpn J Appl Phys* vol. 42, pp. 3593-3597, 2003.

[61] C. Sandhya, P. K. Singh, S. Gupta, H. Rohra, M. Shivatheja, U. Ganguly, R. Hofmann, G. Mukhopadhyay, S. Mahapatra, and J. Vasi, "Recent advances in charge trap flash memories," in *Electron Devices and Semiconductor Technology, 2009. IEDST '09. 2nd International Workshop on*, 2009, pp. 1-5.

[62] M. van Duuren, N. Akil, M. Boutchich, and D. S. Golubovic, "New writing mechanism for reliable SONOS embedded memories with thick tunnel oxide," in *Integrated Circuit Design and Technology and Tutorial, 2008. ICICDT 2008. IEEE International Conference on*, 2008, pp. 181-184.

[63] W. Szu-Yu, L. Hang-Ting, D. Pei-Ying, L. Chien-Wei, L. Erh-Kun, L. Sheng-Chi, Y. Ling-Wu, Y. Tahone, C. Kuang-Chao, G. Jeng, H. Kuang-Yeu, L. Rich, and L. Chih-Yuan, "Reliability and Processing Effects of Bandgap-Engineered SONOS (BE-SONOS) Flash Memory and Study of the Gate-Stack Scaling Capability," *Device and Materials Reliability, IEEE Transactions on*, vol. 8, pp. 416-425, 2008.

[64] P. Tung-Ming and Y. Wen-Wei, "High-Performance High-k Y_2O_3 SONOS-Type Flash Memory," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 2354-2360, 2008.

[65] Y. Tateshita, J. Wang, K. Nagano, T. Hirano, Y. Miyanami, T. Ikuta, T. Kataoka, Y. Kikuchi, S. Yamaguchi, T. Ando, K. Tai, R. Matsumoto, S. Fujita, C. Yamane, R. Yamamoto, S. Kanda, K. Kugimiya, T. Kimura, T. Ohchi, Y. Yamamoto, Y. Nagahama, Y. Hagimoto, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, S. Kadomura, and N. Nagashima, "High-Performance and Low-Power CMOS Device Technologies Featuring Metal/High-k Gate Stacks with Uniaxial Strained Silicon Channels on (100) and (110) Substrates," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1-4.

[66] Y. Yee-Chia, L. Qiang, P. Ranade, H. Takeuchi, K. J. Yang, I. Polishchuk, K. Tsu-Jae, H. Chenming, S. C. Song, H. F. Luan, and K. Dim-Lee, "Dual-metal gate CMOS technology with ultrathin silicon nitride gate dielectric," *Electron Device Letters, IEEE*, vol. 22, pp. 227-229, 2001.

[67] I. Polishchuk, P. Ranade, K. Tsu-Jae, and H. Chenming, "Dual work function metal gate CMOS technology using metal interdiffusion," *Electron Device Letters, IEEE*, vol. 22, pp. 444-446, 2001.

[68] L. Qiang, R. Lin, P. Ranade, K. Tsu-Jae, and H. Chenming, "Metal gate work function adjustment for future CMOS technology," in *VLSI Technology, 2001. Digest of Technical Papers. 2001 Symposium on*, 2001, pp. 45-46.

[69] H. N. Alshareef, M. Quevedo-Lopez, H. C. Wen, R. Harris, P. Kirsch, P. Majhi, B. H. Lee, R. Jammy, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, "Work

function engineering using lanthanum oxide interfacial layers," *Applied Physics Letters*, vol. 89, pp. 232103-3, 2006.

[70] S. Guha, V. K. Paruchuri, M. Copel, V. Narayanan, Y. Y. Wang, P. E. Batson, N. A. Bojarczuk, B. Linder, and B. Doris, "Examination of flatband and threshold voltage tuning of HfO_2/TiN field effect transistors by dielectric cap layers," *Applied Physics Letters*, vol. 90, pp. 092902-3, 2007.

[71] H. N. Alshareef, H. F. Luan, K. Choi, H. R. Harris, H. C. Wen, M. A. Quevedo-Lopez, P. Majhi, and B. H. Lee, "Metal gate work function engineering using AlN_x interfacial layers," *Applied Physics Letters*, vol. 88, pp. 112114-3, 2006.

[72] J. Hyung-Suk, H. Sung Kee, L. Hajin, K. Yun-Seok, K. Min Joo, Y. Mi Young, L. Cheol-kyu, L. Mong sub, Y. Young-sub, C. Youngsu, K. Seulgi, B. Hion Suck, L. Jong-Ho, L. Nae-In, and K. Ho-Kyu, "Dual High-k Gate Dielectric Technology Using Selective AlOx Etch (SAE) Process with Nitrogen and Fluorine Incorporation," in *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 162-163.

[73] K. L. Lee, M. M. Frank, V. Paruchuri, E. Cartier, B. Linder, N. Bojarczuk, X. Wang, J. Rubino, M. Steen, P. Kozlowski, J. Newbury, E. Sikorski, P. Flaitz, M. Gribelyuk, P. Jamison, G. Singco, V. Narayanan, S. Zafar, S. Guha, P. Oldiges, R. Jammy, and M. Ieong, "Poly-Si/AlN/HfSiO Stack for Ideal Threshold Voltage and Mobility in Sub-100 nm MOSFETs," in *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 160-161.

[74] H. C. Wen, S. C. Song, C. S. Park, C. Burham, G. Bersuker, K. Choi, M. A. Quevedo-Lopez, B. S. Ju, H. N. Alshareef, H. Niimi, H. B. Park, P. S. Lysaght, P. Majhi, B. H. Lee, and R. Jammy, "Gate First Metal-Aluminum-Nitride PMOS Electrodes for 32nm Low Standby Power Applications," in *VLSI Technology, 2007 IEEE Symposium on*, 2007, pp. 160-161.

[75] S. Kubicek, T. Schram, V. Paraschiv, R. Vos, M. Demand, C. Adelmann, T. Witters, L. Nyns, L. A. Ragnarsson, H. Yu, A. Veloso, R. Singanamalla, T. Kauerauf, E. Rohr, S. Brus, C. Vrancken, V. S. Chang, R. Mitsuhashi, A. Akheyar, H. J. Cho, J. C. Hooker, B. J. O'Sullivan, T. Chiarella, C. Kerner, A. Delabie, S. Van Elshocht, K. De Meyer, S. De Gendt, P. Absil, T. Hoffmann, and S. Biesemans, "Low V_T CMOS using doped Hf-based oxides, TaC-based Metals and Laser-only Anneal," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 49-52.

[76] K. Iwamoto, H. Ito, Y. Kamimuta, Y. Watanabe, W. Mizubayashi, S. Migita, Y. Morita, M. Takahashi, H. Ota, T. Nabatame, and A. Toriumi, "Re-examination

of Flat-Band Voltage Shift for High-k MOS Devices," in *VLSI Technology, 2007 IEEE Symposium on*, 2007, pp. 70-71.

[77] W. Arden, "Future semiconductor material requirements and innovations as projected in the ITRS 2005 roadmap," *Materials Science and Engineering: B*, vol. 134, pp. 104-108, 2006.

[78] C. Tsung-Yu, C. Tien-Sheng, W. Yi-Hong, and Y. Wen-Luh, "High-Program/Erase-Speed SONOS With *In Situ* Silicon Nanocrystals," *Electron Device Letters, IEEE*, vol. 29, pp. 1148-1151, 2008.

[79] H. Wei, D. S. H. Chan, and C. Byung-Jin, "SONOS type memory cell with ALD LaAlO blocking oxide for high speed operation," in *Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on*, 2008, pp. 835-838.

[80] A. Padilla, L. Sunyeong, D. Carlton, and L. Tsu-Jae King, "Enhanced endurance of dual-bit SONOS NVM cells using the GIDL read method," in *VLSI Technology, 2008 Symposium on*, 2008, pp. 142-143.

[81] L. Sheng-Chih, L. Hang-Ting, L. Chien-Wei, W. Tai-Bor, Y. Ming-Jui, L. Yi-Hsien, H. Jung-Yu, W. Szu-Yu, L. Guang-Li, C. Chao-Hsin, H. Kuang-Yeu, L. Rich, and L. Chih-Yuan, "Highly Reliable MA BE-SONOS (Metal-Al_2O_3 Bandgap Engineered SONOS) Using a SiO_2 Buffer Layer," in *VLSI Technology, Systems and Applications, 2008. VLSI-TSA 2008. International Symposium on*, 2008, pp. 58-59.

[82] R. Ohba, Y. Mitani, N. Sugiyama, and S. Fujita, "10 nm bulk-planar SONOS-type memory with double tunnel junction and sub-10 nm scaling utilizing source to drain direct tunnel sub-threshold," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.

[83] T. C. Chen, T. C. Chang, F. Y. Jian, S. C. Chen, C. S. Lin, M. H. Lee, J. S. Chen, and C. C. Shih, "Improvement of Memory State Misidentification Caused by Trap-Assisted GIDL Current in a SONOS-TFT Memory Device," *Electron Device Letters, IEEE*, vol. 30, pp. 834-836, 2009.

[84] Z. Gang, Y. Won Jong, and L. Chung-Ho, "Hot-Electron Capture for CHEI Programming in SONOS-Type Flash Memory Using High-*k* Trapping Layer," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 1502-1510, 2008.

[85] Y. N. Tan, H. C. Wen, C. Park, D. C. Gilmer, C. D. Young, D. Heh, P. Sivasubramani, J. Huang, P. Majhi, P. D. Kirsch, B. H. Lee, H. H. Tseng, and R. Jammy, "Tunnel Oxide Dipole Engineering in TANOS Flash Memory for Fast Programming with Good Retention and Endurance," in *VLSI Technology, Systems and Applications, 2008. VLSI-TSA 2008. International Symposium on*, 2008, pp. 54-55.

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Applications of Oxygen Vacancies and Dipole Layer Engineering on SONOS-type Nonvolatile Memory