


國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

電感耦合式電漿氮化和氟化製程對鈹系
介電質薄膜之影響



The Effect of Nitridation and Fluorination Processes by
Inductive Coupled Plasma to Hafnium-based Dielectric
Thin Films

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中華民國九十八年八月

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碩 士 論 文

A Thesis
Submitted to Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao Tung University
In Partial Fulfillment of the Requirements
for the Degree of
Master
In
Electronics Engineering
August 2009
Hsinchu, Taiwan

中華民國九十八年八月

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使用二氧化矽當作閘極介電層已經達到科技和理論的極限。在4Gbit動態隨機存取記憶體中的等效氧化層厚度，將被微縮到0.22奈米，此厚度非常接近二氧化矽的結構限制，因為二氧化矽的Si-O鍵長為0.17奈米。對於MOSFET閘極介電層而言，使用氧化鉛是目前及未來最為推廣的材料，但是high-k閘極介電層在C-V曲線中被發現有磁滯現象，此現象會導致MOS元件中平帶電壓漂移以及臨界電壓的不穩定。本研究製造了Al-Ti-HfAlO(HfO₂)-Si 金屬絕緣層矽結構之電容，作為分析的樣品。本研究藉由探討鉛系介電質薄膜在不同電漿處理的條件下C-V和J-V的特性。此外，本研究亦探討鉛系介電質薄膜在不同氮化和氟化電漿製成的條件下之可靠度問題，諸如磁滯現象、應力引致漏電流、常壓應力測試，因此，本研究發現氮化和氟化電漿能有效的消滅氧的空洞，以及改善介面限補電荷密度，來有效的降低漏電流，改善其電容值及增加其可靠度。

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ABSTRACT

Silicon oxide gate dielectric is now being pushed to both its technological and theoretical limits. The equivalent oxide thickness (EOT) in the 4-Gbit generation dynamic random access memory (DRAM) will be scaled down further to 0.22nm which is very close to the structural limit of silicon dioxide, as the Si-O bond in silicon oxide is 0.17 nm. The oxide of using Hafnium-based is a most promising material for future MOSFET gate oxide applications. Unfortunately, for high-k gate dielectrics, there is a hysteresis phenomenon in its capacitance-voltage (C-V) characteristics. This hysteresis induces a flatband voltage shift, and threshold voltage instability when it is applied to MOSFETs. In this study, we fabricated Al-Ti-HfAlO(HfO₂)-Si MIS capacitor as our analysis device. The electrical characteristics of the film under different plasma conditions were discussed by C-V and I-V curves. Moreover, the reliability of the films under different plasma treatment conditions were discussed by hysteresis effect, SILC (Stress Induced Leakage Current) profile, CVS (Constant Voltage Stress) test. Hence, the nitrogen atoms and fluorine atoms can eliminate oxygen vacancies and repair the interface trap densities to suppress the leakage current.

誌謝

首先，感謝指導教授張國明教授及桂正楣教授，在這二年來的細心指導及對學生的付出，老師對於在做學問要求謹慎，強調對於了解物理觀念大於實際的數學計算，讓我在學習方面獲益良多並且給了我許多啟發，讓我能順利的完成碩士論文。

感謝陳柏寧學長給予的指導，在實驗過程中不斷的給予建議及鼓勵，並提供我寶貴的經驗，使得本研究能有不錯的完整度。對於學長這兩年來的照顧，我將永遠銘記在心。

另外，實驗室的同学汶錦、信宇、憶雯、秉燭、仲逸、文魁、卓慶、成家、彥凱、威仁、堃豪、天佑、育彬、昆謀，以及學長、學弟，大家一起在學習道路上共同分享及互相幫助，我們彼此在逆境中成長，多年後，我將不會忘記這兩年和你們一起的點點滴滴。

最後，要感謝我的家人，你們的支持與鼓勵是背後支撐我的最大力量，讓我能勇敢無畏懼的向前邁進。

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Chapter 1

Introduction

1.1 Background

According to process progress, complementary metal–oxide–semiconductor (CMOS) integrated circuit technology has been evolved continuously since 1980, this evolution may let the semiconductor industry meet many requirements to satisfy market expansion. There are several requirements such as performance, low consumed power, and a spacious range of power supply. Developing the ability to carry out a reduction of the dimension of the basic device in the microelectronics has been realized, which is called scaling. This results in growth of technology in the fabrication.

It can be discussed that the key component enabling the scaling of the Si-based metal–oxide–semiconductor field effect transistor (MOSFET) is the material properties associated with the dielectric used to be as gate oxides. For example, Silicon dioxide is a good candidate for gate. The use of silicon dioxide as a gate dielectric has many advantages in IC technology consisting of a good stability, high-quality Si–SiO₂ interface, and outstanding isolation properties. Recently, regardless of the device dimensions, hard breakdown fields of 15 MV/cm are easily obtained, midgap interface state densities are $\sim 10^{10}/\text{cm}^2$ eV, defect charge densities are $10^{10}/\text{cm}^2$, the significant electrical properties stand for a important challenge as substitutes for gate dielectrics.

Indicated on previous results and essential notices, their materials tendency

forms at interfaces with Si, it enables the use of other high-k materials by presenting as an interfacial high-k layer. While an effort is continuous, many studies are still required, just like it is obvious that any material to replace SiO₂ as the gate dielectric meets a huge challenge. It plays an important role on process integration for investigation of candidates, so it is worthwhile to be studied.

The development of the semiconductor industry depends on the progressive improvement of integrated circuit (IC) reliability. This improvement is finished by scaling the sizes of metal oxide semiconductor field effect transistor (MOSFET). Dimension reduction of MOSFET has provided extra improvement in speed performance, circuit density, and cost per transistor over the past several decades. Therefore, the scaling of MOSFET follows the famous Moore's law, which forecasts the exponential increase in the number of transistors integrated on a chip. Gordon Moore, the Chairman Emeritus of Intel Corporation, made his famous research in 1965 [1]. He observed an exponential growth in the number of transistors per integrated circuit and predicted that this trend would continue. As shown in Fig. 1-1, through Intel's continual technology advances, "Moore's Law", the four times greater of transistor numbers every three years has been maintained, and still has been demonstrated up till now. Since the circuit density will continue to increase in the future, so device scaling is needed. As shown in Fig. 1-2, the transistor physical gate length would be expected to reduce to 15nm in 2010.

Over the past 30 years, SiO₂ has been an excellent candidate for gate dielectrics, and has been scaled down from a 100nm thickness to 1.2nm at 90nm process technology node today, in order to obtain a large C_g and a higher circuit density. Schulz in Macmillan Magazines predicted that, in order to keep up with the roadmap

goal, in 2012 the thickness of gate oxide would be scaled down to 1nm, which represents only five silicon atoms thickness (see Fig 1-3)[2]. Thus the direct tunneling current which depends heavily on film physical thickness will increase to an unpredictable level, resulting in a huge power dissipation and heat (1.1).

$$I_{DT} \propto \left[\exp - \frac{2mq\phi}{\sqrt{\left(\frac{h}{2\pi}\right)^2 T_{phys}}} \right] \quad (1.1)$$

We can see from Fig. 1-4 to find that the gate oxide can be scaled down to 2nm before exceeding the limit of 1A/cm² from the tolerant power consuming. As shown in Fig. 1-5, below 2nm the tunneling current of the gate oxide will mainly dominate large part of total current density. For easily observing the problem of the leakage: as SiO₂ thickness is reduced, leakage current increases exponentially (~10×/2Å)[3].

1.2 The problem of poly-silicon gate

For the improvement of the performance and circuit density of CMOS, scaling down gate length and insulator layer thickness is a trend for silicon process. As the dimension of CMOS is scaled down, there are several problems of the gate of poly silicon and the insulator layer of SiO₂, which is as followed : As shown in Fig. 1-6, device with such a small size will generate some problems like poly-silicon (poly-Si) gate depletion effect, high gate resistance, dopant penetration from doped poly-Si gate and high gate tunneling leakage current [4]. To release these undesired effects in CMOS transistors, there is a giant interest in the replacement of the traditional materials.

1.3 Need for high-k materials

The rapid shrinking of the transistor feature size has been focused on the channel length and gate dielectric thickness to reduce rapidly. This has been reported that the CMOS gate dielectric SiO₂ thickness can be scaled to a least 13 Å [5]. Although, SiO₂ thickness is less than 20-25 Å, large direct-tunneling current is inevitable. Therefore, as shown in Fig.1-7, it is necessarily for high dielectric constant material (high-κ) gate dielectrics to be studied as alternative candidate for gate dielectrics in order to suppress unreasonable gate leakage current and power consumption.

High-κ gate materials can sustain the same EOT with thicker physical thickness, and is therefore expected effectively reduced direct-tunneling current. From Figure 1-8, the increased physical thickness significantly reduces the probability of tunneling current across the insulator, and hence, reduces the amount of off-state leakage current [6]. The relationship between dielectrics constant and thickness is expressed as follows :

$$EOT = \frac{k_{ox} \times t_{high-k}}{k_{high-k}} \quad (1.2)$$

However, threshold voltage (V_{th}) instability and device degradation are still major concerns for MOSFETs using high-κ gate dielectrics due to high interface and bulk trap density. Although these oxides reduce the gate leakage currents, they suffer from a high density of charge traps. This causes transient instability of the gate threshold voltage, scattering of carriers in the Si channel, and possible reliability problems. Hence, hafnium based gate dielectrics are still under investigation because

of their relatively high oxygen vacancy concentration which is one of the reasons for threshold voltage hysteresis, leakage current, and flatband voltage shifting that all degrade the performance of transistors. These issues include solving mobility degradation and threshold voltage instability, as well as reducing the number of fixed charges and charge traps.

1.4 Carrier Transport in High-k Gate Dielectrics

The continuous scaling down of gate silicon dioxide thickness in metal oxide semiconductor devices realize continually improvement in integrated circuit (IC) performance. However, the accompanying high leakage current of thin silicon oxide is a serious problem for IC application. While a high-k gate dielectric has a large physical thickness, an identical equivalent oxide thickness has recently been proposed to solve this leakage issue. A survey of the literature on high-k gate dielectric shows that the leakage current densities are strongly dependent on the deposition method, pre-deposition, and post-deposition annealing treatments performed to enhance the properties of high-k gate dielectric [7]. Depending on the applied voltage and the thicknesses of the high-k films, the conduction mechanism identified in Hf-based dielectric is generally attributed to a Schottky emission (SE), the Frenkel-Poole (FP) emission, or Fowler-Nordheim tunneling (F-N). Therefore, it is important to study the various leakage mechanisms in these dielectrics with the goal of minimizing their leakage current for advanced IC devices applications.

1.4.1 Schottky Emission (SE)

The carrier transport mechanism of Schottky emission (SE) in high-k gate dielectric was shown in the Fig 1-9 (a). The SE emission is due to the transport of electrons from gate electrode over the potential barrier into the Si substrate resulting from thermionic emission. The current density (J) – field (E) relation for SE is given by the Schottky-Richardson relation as [8],

$$J_{SE} = AT^2 \exp\left[\frac{\beta_{SE} \cdot \sqrt{E}}{kT}\right] \quad (1.3)$$

where β_{SE} is given by

$$\beta_{SE} = \sqrt{\frac{q^3}{4\pi\epsilon_0\epsilon_r}} \quad (1.4)$$

and

$$A = C_{RD} \cdot \exp\left(\frac{-q\phi_B}{kT}\right) \quad (1.5)$$

with ϵ_r is the dynamic dielectric constant, ϵ_0 the permittivity of the free space, k is the Boltzmann constant and T the absolute temperature; C_{RD} is the Richardson constant and is expressed as,

$$C_{RD} = \frac{4\pi \cdot q \cdot m^* k^2}{h^3} \quad (1.6)$$

where m^* is the effective mass of electrons in dielectric.

1.4.2 Frenkel-Poole Emission (FP)

The carrier transport mechanism of Frenkel-Poole (FP) emission in high-k gate dielectric was shown in the Fig 1-9 (b). The FP emission is due to the thermal excitation of charge carriers from Coulombic traps in the bulk of a dielectric or semiconductor, enhanced by the application of an electric field. The general

expression for the FP current density is given by

$$J = C_t E \exp\left[\frac{-(q\phi_B - \beta \cdot \sqrt{E})}{\xi kT}\right] \quad (1.7)$$

where C_t is a trap density related constant; $q\phi_B$ is the ionization potential in eV, which is the amount of energy required for the trapped electron to escape from the influence of the positive nucleus of the trapping center when no field is applied; $\beta \sqrt{E}$ is the amount by which the trap barrier height is reduced by the applied electric field, E . The factor ξ in the denominator of the exponential may vary between 1 and 2, depending on the amount of acceptor compensation. Rewriting Eq. (1-7) as

$$\ln[J/E] = \frac{\beta}{\xi kT} \cdot \sqrt{E} + \left[\ln C_t - \frac{q\phi_B}{\xi kT}\right] \quad (1.8)$$

which is referred as the FP plot.

1.4.3 Fowler-Nordheim Tunneling (F-N)

The carrier transport mechanism of Fowler-Nordheim (FN) tunneling in high-k gate dielectric was shown in the Fig 1-9 (c). The FN emission is caused by field ionization of trapped electron into the conduction band or by electrons tunneling from the metal Fermi energy into insulator conduction band. The tunnel emission has the strongest dependence on the applied voltage but is essentially independent of the temperature. The general expression for the F-N current density is given by [9]

$$J_{FN} = CE^2 \exp(-E_B / E) \quad (1.9)$$

where C is a function of the electron effective mass

1.5 Use in industry

In early 2007, as shown in table 1-1, Intel announced the deployment of hafnium-based high-k dielectrics in conjunction with a metallic gate for components built on 45 nanometer technologies, expected to ship in 2007. Consequently, IBM announced plans to transition to high-k materials, also hafnium-based, for some products in 2008. While not identified, it shows that the most likely dielectrics used by these companies are some form of HfSiON. HfO₂ and HfSiO are susceptible to crystallization during dopant activation annealing. NEC Electronics has also announced the use of a HfSiON dielectric in their 55 nm Ultimate Low Power technology. However, there is no absolute guarantee that hafnium will be the basis of future high-k dielectrics. The 2006 ITRS roadmap predicts the implementation of high-k materials to be commonplace in the industry by 2010.

1.6 The choice of High-K materials

The replacement of silicon dioxide as a gate insulator in MOS devices with materials of higher dielectric permittivity ϵ_r , is motivated by the need of increasing the capacitance density without further reducing the physical thickness. Despite a considerable effort in this direction, the formation of a thin SiO₂ interlayer between silicon substrate and the high-k material appears to be unavoidable [10]. Most of high-k materials are not stable in direct contact with silicon and require a thin SiO₂ layer to stabilize the dielectric film on silicon substrate. Thin SiO₂ layer can improve interface states, surface roughness and electron mobility. The use of dielectric layers with high-k materials will give us thicker films with equivalent SiO₂ electrical thickness, and should allow us to reduce the leakage current and improve the

reliability of the gate dielectric layer. Currently many experimental efforts are to investigate for alternative gate dielectric materials. Many metal oxides such as TiO₂, Al₂O₃, Ta₂O₅, ZrO₂, HfO₂, La₂O₃, Y₂O₃, [11-17] etc. and ferroelectric materials (e.g., PZT [18], BST, etc.) are being investigated as candidate materials to replace silicon dioxide. The required material properties of alternative gate oxide can be summarized as follows.

1. Dielectric constant significantly larger than 3.9 in thin film phase.
2. Thermodynamic stability in direct contact with silicon .
3. Low diffusion constant for dopant atoms in poly-Si.
4. Large band gap with more than 1 eV tunneling barrier for both electrons and holes in order to achieve low leakage current.
5. Low interface trap defect density, $D_{it} \leq 10^{10} - 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.
6. Low defect density within oxide layer.
7. Preferably stable amorphous phase to avoid grain boundary problem.

Table 1-2 illustrates Material requirement of high-k dielectrics. For most high-k materials, the higher dielectric constant comes at the expense of narrow band gap. The lower barrier height for tunneling current tends to compensate the benefit of the higher dielectric constant. Even though there are many materials with significantly high k values, many of them are not suitable for gate dielectric applications since they do not satisfy all of these necessary conditions. For example, TiO₂ has a higher k value of 80-100 but has a small band gap of 3.5 eV and band offset of 0.05 eV. Most other ferroelectric materials such as SrTiO₃ with very high dielectric constants have the same problem of small potential barrier [19]. Table 1-3 shows material properties comparison of Al₂O₃, ZrO₂, HfO₂.

1.7 Why choose HfAlO&HfO₂

High-K materials have been studied as alternative gate dielectric materials for high performance and low consumed power CMOS. Among all high-K gate dielectric materials, HfO₂ is extensively investigated as one of the most promising candidate materials. HfO₂ appears promising due to its relatively high dielectric constant (25) as compared to SiN and Al₂O₃ [20], its relatively high free energy of reaction with Si (47.6 kcal/mole at 727 C) as compared to TiO₂ and Ta₂O₅ [21] and its relatively high band gap (5.8 eV) among its high-k competitions [22]. It is desirable for high-K materials to remain amorphous type after device fabrication. However, HfO₂ crystallizes at temperatures less than 500°C. Grain boundaries in crystallized gate dielectric can be the fast paths for oxygen or dopants diffusion into gate dielectric and even FET channel region in silicon substrate, causing uncontrolled interfacial layer growth at the interface, threshold voltage instability, and defect generation. Therefore, there have been several reports on using nitrogen or aluminum incorporation into high- materials to raise the crystallization temperature [20, 21, 23, 24].

1.8 The Roles of Nitrogen in High-k Gate Dielectric

The nitrogen-incorporated gate dielectrics have been shown to possess a higher breakdown field, better crystalline retardation, and reduced leakage current with the same EOT [25]. For electrons injected from the interface, the nitrogen-rich layer near the dielectric/Si substrate interface has the capability of lowering the leakage current tunneling through the dielectric [26].

It has been also reported that the nitrogen in the gate dielectric can reduce the

amount of detrimental species diffused from the gate electrode [27]. Moreover, the electrical property degradation of MOS devices is influenced by the concentration of nitrogen in the high-k gate dielectric [28]. In general, either bottom nitrided (BN) or top nitrided (TN) can be used to improve the electrical properties of MOS devices with HfO₂, and HfSiO gate dielectric. The BN techniques using surface nitridation has shown reduced leakage current and is effective in preventing boron penetration [29]. The TN approach using a reactive sputtering method to control the nitrogen profile in HfO₂ gate dielectric has been reported to possess thermal stability and be effective in preventing oxygen diffusion through HfO₂ [30]. In addition, excellent electrical properties of MOS devices with HfO_xN_y gate dielectric have been achieved by sputtering of HfN layer in an Ar+N₂ ambient in comparison with HfO₂ [25]. It is also reported that the nitrogen concentration in HfO_xN_y gate dielectric can significantly affect the electrical properties of MOS devices [31]. The facts mentioned above indicate that the roles of nitrogen in high-k gate dielectric are important in improving the electrical characteristics of MOS devices.

1.9 The Effects of Interface Engineering on High-k Gate Dielectric

Fig. 1-10 shows the scheme of important regions in gate stack of a field effect transistor [32]. The high-k material/silicon interfaces are regarded as unideal due to the presence of defect states [33]. The originations of these interface defects may be related to the stray metal atoms within the Si adjacent to the interface or due to surface structural defects, oxidation-induced defects, or defects caused by radiation [33-34]. Interface traps have a major impact on device lifetime and play an important role in determining the threshold voltage, inversion layer mobility and low frequency

noise of MOS devices, the surface perfection comparable to Si-epitaxial growth required for reduction of interface traps are a significant concern [35-36]. Moreover, interface trap of MOS devices is another important contributor to leakage current besides the characteristics of dielectric material itself. If the interface between dielectric/Si is rough, intensive electric field will take place at the sharp corners which may lead to a high leakage current and low breakdown voltage [37]. Various processes can influence the interface quality; dry etching is one example [37-38]. Hence, to achieve a smooth surface and to form an undamaged layer on substrate is an important task in modern metal-oxide-semiconductor field-effect-transistor (MOSFET) devices [38]. That is to say, to achieve a good dielectric/Si interface as a surface channel of MOS device, the defect density at silicon surface must be reduced.

1.10 plasma Nitridation and Fluorination

According to traditional view of improving SiO_2 device performance, we could find that nitridation is a common method to improve the interface [39]. The MOS devices have properties with the result that there is often N_{it} or D_{it} in the interface, imperfect bonding of interface usually makes the characteristic of the device deteriorate. For example, charge will be trapped by the defects of the interface, it produces flat band voltage shift and also reduces the carrier mobility. Another shortcoming is that these dangling bonds will easily bond with oxygen atoms in the following high temperature environment. The extra chemical reaction will let the interfacial oxide growth, and it will reduce the C value because of the lower dielectric constant. In addition, the quality of interfacial layer formed by oxidation is worse, and it would cause the problem of charge trapping. In order to solve these problems, nitridation treatment could let the atom of nitrogen bond with these dangling bonds

and fix it while entering the interface layer, and then improve the stability and reliability of interface. Consequently, nitridation treatment is a workable solution to improve interface quality. As we note before, the question about using high-k materials to replace SiO₂ is that there are too many defects in the interface to cause reliability degradation. Therefore, when we use high-k materials, it is consider that nitridation treatment is a more suitable way to improve reliability and thermal stability of the device. These kind of treatment have already used in some relevant references [40] [41]. Among them, someone take nitridation treatment at high temperature, others take so-called plasma nitridation . According to [42], we could understand that the effect of plasma nitridation is better than thermal nitridation. The reason is that high-k materials could not sustain high thermal stress. As long as the temperature reaches certain degree, we would see the phenomenon of crystallization. The crystallization of dielectric would increase leakage current substantially, because it offers the path of leakage current. On the other hand, the meaning of plasma nitridation is to activate the gas source first. The high activation energy of radical will provide better recovery which is better than thermal nitridation. For all these reasons, we adopt plasma nitridation to improve reliability in present experience.

For fluorination, fluorine can passivate the gap states of HfO₂ completely. It has been found that silicon incorporated HfO₂ can enlarge the band gap, improve the thermal stability performance, and suppress the crystallization. A possible explanation is that fluorine takes one electron from the oxygen vacancy and pushes the other electron away from the oxygen vacancy. This causes the oxygen to be +1 charged since fluorine can only accept one electron to fill its 2p state. In the case of HfO₂, the electron that was pushed out is shared by the three hafnium atoms nearby and is localized in their 5d states. Hence, with F passivation, V_{th} instability was improved and the stress-induced leakage current decreased greatly.

1.11 Why use plasma of nitrogen and fluorine doping

Nitrogen (N) was found to give some defect passivation [43], but a large amount of N induces band gap narrowing [44]. Fluorine (F) has a large beneficial effect on charge trapping [45–47]. The wave functions are expanded in a plane-wave basis set and sufficient convergence is achieved with a 30.25 Ry cutoff. The lattice constant of $a_0 = 5.05\text{\AA}$ is obtained for cubic fluorite HfO₂. The calculations are carried out on ($2 a_0 * 2 a_0 * 2 a_0$) supercell of cubic fluorite HfO₂ containing various dopants. We calculated the electronic structures of neutral substitutional Fs. The Fermi level of the Fs lies at the bottom of the conduction band (CB). Fs has one more valence electron than O, so that a neutral Fs has one extra electron. Hence, Fs⁺ is the most stable configuration for the Fermi energy over the entire energy gap. This means that Fs⁺ passivates the V_o and gate oxide has positively charged traps in the most stable state, and it means that N doping induces V_o. The V_o inducing mechanism is the exothermic reaction. The most stable NsVoNs complex structure is composed of one V_o and two Ns at the nearest neighbor oxygen sites to the V_o. The driving force of this reaction is total energy stabilization with charge compensation. In this charge compensation, charge transfer arises from two electrons of the induced V_o gap state falling into the two vacant N states at the top of the valence band as shown in Fig. 1-11. As a result, a large amount of N induces a large amount of V_o. The key point is the increase in V_o–V_o interactions with the increase in the amount of V_o. A large amount of N induces the deterioration of the CB offset owing to V_o–V_o interaction as shown in Fig. 1-12 [44]. If we use N doped HfO₂, the deterioration of the VB offset is inevitable. If V_o can move easily, total energy is stabilized by local crystallization around V_o owing to disturbance by the movement of V_o, because the crystal state is

lower in energy than the amorphous state. A pair of Fs and Ns can passivate the Vo with no excess charges as shown in Fig. 1-13. The main passivation energy comes from one excess electron transfer of CB bottom of Fs to VB top of Ns as shown in Fig. 1-13. The amount of N is not needed large, because Fs fills up Vo. Moreover, CB lowering owing to Vo–Vo interaction can be avoided. Defects formation in HfO₂ should be affected by its crystal structure. But the fact that the CB of HfO₂ is composed of Hf 5d states, and the VB is composed of O 2p states is not affected by its crystal structure. The stabilization mechanism by the electron transfer is not affected by its crystal structure. That is to say, fluorines can fill up oxygen vacancies in HfO₂ by exothermic reaction, but induce distribution of the positive charges in HfO₂ [48]. The most important point is that we should fill up Vo by fluorine (Fs), and Fs donates an excess electron to other acceptor type dopant. This passivation process completely eliminates Vo with no excess charges in gate oxide. The amount of N is not needed large, because Fs fills up all oxygen vacancies [48].

1.12 Thesis Organization

Following chapters in the thesis are primarily organized as follow :

In chapter 2, we make a description of experimental details. Metal Organic Deposition system is used to deposit HfAlO and HfO₂ material on silicon surface.

In chapter 3, we discuss the characteristics of HfAlO and HfO₂ insulator by Metal Insulator Semiconductor (MIS) capacitors.

In chapter 4, we discuss the reliability of HfAlO and HfO₂ insulator by Metal Insulator Semiconductor (MIS) capacitors and the effects of fluorine and nitrogen radicals.

In chapter 5, we make the conclusions for this thesis and provide some suggestions for future work.

Chapter 2

Experiments of Al/Ti/ HfAlO(HfO₂)/Si MIS Capacitor

2.1 How to deposit HfAlO(HfO₂) thin film

There are many methods to deposit high- κ gate dielectrics stack, such as physical vapor deposition (PVD) [49], atomic layer deposition chemical vapor deposition (ALCVD) [50-54], and metal-organic chemical vapor deposition (MOCVD) [55-57]. In the industrial production viewpoint, PVD is not an appropriate tool for high- κ film deposition because of both poor step coverage and bad uniformity. Nowadays, ALCVD and MOCVD have paid more efforts to be evaluated for high- κ dielectrics deposition in the industry. Table 2-1 is the comparison of deposition techniques which have been used. MOCVD has the advantages of superior step coverage, high deposition rate, good control ability of film composition, and excellent thickness uniformity on large dimension wafers. MOCVD system is therefore chosen to deposit high- κ dielectrics in this thesis.

Recently, aluminum oxide (Al₂O₃) had been demonstrated as promising candidates for the gate dielectrics of sub-0.1 μ m device due to their higher κ value, relatively high ϕ_B and superior thermal stability [55]. Due to the high dielectric constant and high thermal stability, Al₂O₃ is suitable to be integrated into trench DRAM process and is therefore chosen in this thesis. Figure 2-1 shows the detail schematic structure of the MOCVD system. The MOCVD chamber is equipped with a

turbo-molecular pump and a liquid injection system which has four independent-controlled injectors. A liquid pump is consisted of the injector and pumps the precursors through a hot nickel frit with a proper rate. The vapors are carried with a 200 sccm flow of Argon to gas distribution ring which is located at a proper distance from the substrate. On the contrary of the conventional bubbler system, the liquid injection system is with sufficient temperature window to alleviate the thermal aging of the precursor. This is because the precursor remains in liquid state at room temperature until it is pumped into the vaporizer and injected into the deposition chamber. However, the precursor should keep at long-term chemical stability in solvent and non-reactive with other precursors in solvent [58]. The components of the vaporizer, the gas ring and the connecting tube are maintained at 190°C with heating tapes and blankets, while the substrate temperature is controlled at 500°C with quartz-halogen lamps and a thermocouple. A rotating susceptor is used for uniformly heating during processing. A flow of 100 sccm N₂ is maintained throughout the deposition cycle. The base pressure of the MOCVD chamber is ~ 10⁻⁸ torr. The deposition pressure of the deposition is at the 5 mtorr where the gas-phase collisions are scarce.

2.2 MOCVD system

MOCVD (metal-organic CVD) is a widely used technology for depositing a variety of thin films, including metal oxide and metal silicate films, for high-k gate dielectric applications. The basic steps in MOCVD deposition method are as follows:

1. MO precursor in company with N₂ process gas and O₂ process gas are injected into the reactor.
2. The sources are mixed inside the reactor and transferred to the deposition process

chamber.

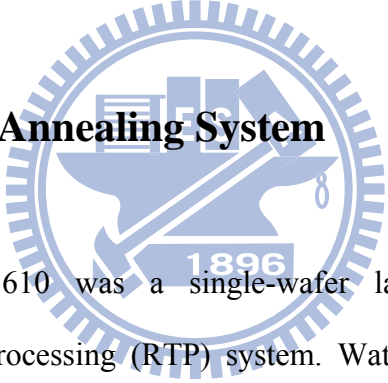
3. At the deposition process chamber, high temperature results in the decomposition of sources and other gas-phase reactions, forming the film precursors that are useful for film growth and byproducts.
4. The film precursors transport to the growth surface.
5. The film precursors are absorbed on the growth surface.
6. The film precursors diffuse to the growth site.
7. At the surface, film atoms incorporate into the growing film through surface reaction.
8. The byproducts of the surface reactions desorb from the surface.
9. The byproducts transport to the main gas flow region away from the deposition area toward the reaction. Then the wafer exits.

When a poly-Si gate is used with MOCVD HfO_2 and HfSi_xO_y , most of the devices have EOT greater than 2 nm. Unlike metal electrodes, using poly-Si electrode requires the high-k gate stack to go through a $1000^\circ\text{C}/10$ sec S/D activation anneal step. This step not only results in chemical and structural changes in the high-k film, but also affects interfaces between the high-k film/substrate and the high-k/poly-Si electrode. All devices fabricated with MOCVD ZrO_2 and ZrSiO films using poly-Si gate electrode were too leaky to give any meaningful C-V results. In general, using poly-Si gate electrode results in around 0.7 to 1 nm higher EOT for gate stacks fabricated with HfO_2 and HfSi_xO_y gate dielectric films. This additional interfacial oxide thickness is too large to be acceptable. In view of this, the MOCVD is not a good tool for high-k material deposition with poly-Si gate. However, the MOCVD has very good throughput and can process a 25-wafer lot in ~ 2 hours (roughly 4X better than ALCVD). Thus, from a throughput perspective, the MOCVD has a distinct advantage over the ALCVD [59].

2.3 Advantages of MOCVD

In our study, the depositions of TiO₂ thin films were prepared by MOCVD among the most important techniques for depositing thin, high purity epitaxial films with applications in electronics and optics [60]. MOCVD is a very attractive technique which has many advantages, such as: high deposition rate, high crystallization without post annealing, large-area deposition, high throughput, excellent uniformity, excellent step coverage on three-dimensional complex geometries, flexibility for large-scale processing, and a simple experimental system compared to physical vapor deposition which requires high-vacuum equipments. So in this study, low-pressure MOCVD technique was adopted.

2.4 Rapid Thermal Annealing System



METAL RTA-AG 610 was a single-wafer lamp-heated and computer controlled rapid thermal processing (RTP) system. Water and compressed dry air (CDA) cooling system were used to cool down the quartz chamber. High intensity visible radiation heating and cold-heating chamber walls allow fast wafer heating and cooling rate. The tungsten halogen lamps were distinguished into five groups, and the relative percentage of lamp intensity can be adjusted individually for each group to achieve uniform temperature distribution. Temperature was obtained from pyrometer and precise controlled by computer. Two gas lines were used in the system which can be switched between Ar and N₂. Before RTA process started, one minute N₂ gas purge was performed to minimize the water vapor introduced during wafer loading and also swept unwanted particles induced during process. A fast heating rate of 100°C/s was chosen in this work. When an annealing was complete, chamber

temperature was quickly cooled down from 900°C to 500°C by N₂ purge 30 seconds. Then, the chamber was slowly cooled down to 280°C without N₂ purge to avoid creaking of films. After five minutes later, wafers can be taken out from the chamber. Films' creak can be avoided by two-steps-cooling method.

2.5 Plasma treatment system

When the PDA (Post-Deposition-Annealing) was finished, some samples were subjected to an additional plasma treatment in order to improve the electrical properties of gate dielectric. There were various source gas (N₂, NH₃, N₂O, CF₄) and process time (30 sec, 60 sec, 90 sec, 120 sec) as the experiment conditions. Parallel plate high-density plasma reactor employing an ICP source was a single-wafer treated and computer-controlled system.

Fig. 2-2 illustrates ICP system that was used in this experiment. 13.56 MHz RF power was coupled to the top electrode through a matching network. After the sample load to reactor, the system was pumped down to keep the chamber clean enough. Subsequently, the source gas was become radical by the plasma system, as the chamber pressure was 100 mTorr and the substrate temperature was 300°C so that to achieve the goal of low temperature process. The power of working plasma was kept constant at 200W and the flow rate of source gas was 100 sccm. While the process of plasma treatment was finished, these samples were brought to thermal treatment to reduce plasma damage.

2.6 MIS Capacitors Fabrication Process

In this thesis, Al/Ti/HfAlO(HfO₂)/Si MIS capacitor were fabricated to study ultra thin HfAlO(HfO₂) gate dielectrics. Figure 2-3 ~ Figure 2-9 shows the fabrication flow of this experiment. The starting wafer was four inch (100) orientated p-type. It was one side polished and its resistivity was 5~10 ohm-cm.

After standard initial RCA cleaning, wafers were put into chamber and grew HfAlO(HfO₂) layer with metal organic deposition system. After the thin films were deposited, most samples were annealed after deposition (post-deposition anneal) and then subjected to an additional plasma treatment at the substrate temperature of 300°C while the pressure was 100 mTorr and the plasma power was 200W. The plasma treatment conditions were in pure N₂, NH₃ and N₂O with CF₄ gas for 30 sec, 60 sec, 90 sec, and 120 sec respectively and the flow rate were 100 sccm. After nitridation, we also annealed these samples to reduce the plasma damage. Pure titanium was deposited on the HfAlO(HfO₂) layer by dual e-gun evaporation system and aluminum films were evaporated on the top side of wafers. Mask defined the top electrode. Then, we used wet etching to etch undefined Al and Ti films. After patterning, backside native oxide was stripped with diluted HF solution, and Al was deposited as bottom electrode. The detailed fabrication process flow was listed as follows.

1. As shown in Fig.2-3

(1) Si substrate RCA clean

(2) 6 nm HfAlO(HfO₂) was deposited on the sub-Si by MOCVD.

2. As shown in Fig.2-4

(1) Post-Deposition-Annealing by RTA(800°C -60 sec for HfAlO or 600°C -30 sec for HfO₂) .

(2) Plasma treatment with N₂ , N₂O or NH₃(for optimum conditions) and CF₄ (30

sec, 60 sec, 90 sec, 120 sec) .

(3) Post-Nitridation-Annealing by RTA(600°C -60 sec for HfAlO or 600°C -30 sec for HfO₂) .

3. As shown in Fig.2-5

20 nm Ti was deposited on the HfAlO (HfO₂) layer by dual e-gun evaporation system .

4. As shown in Fig.2-6

400 nm Al was deposited on the Ti layer as top electrode by dual e-gun evaporation system.

5. As shown in Fig.2-7

Undefined Al was removed by wet etching (H₂O:CH₃COOH : H₃PO₄:HNO₃) .



6. As shown in Fig.2-8

Undefined Ti was removed by wet etching (1%HF).

7. As shown in Fig.2-9

Al was deposited on the back side of sub-Si as bottom electrode by dual e-gun evaporation system.

After the Al/Ti/HfAlO(HfO₂) /Si MIS capacitors were prepared, we used semiconductor parameter analyzer (HP4156C) and C-V measurement (HP4284) to analysis electric characteristics (i.e. I-V, C-V, EOT, leakage current density etc.). Then we tested their reliability, including stress induced leakage current (SILC),

constant voltage stress (CVS), hysteresis effect.

2.7 The theorem of MIS Capacitors measurement

As shown in Fig.2-10, the theorem which we use on capacitance measurement is: we add a constant DC bias on the metal gate and then add a small AC signal of different frequency. Due to AC signal is changing constantly so the attracted electric charges are changing constantly, too. As the result of the above-mentioned, we will get the capacitance using the changing amount of the electric charges divided by the changing amount of the voltage (2.1).

$$C = \frac{dQ}{dV} \quad (2.1)$$

We will illustrate the three different conditions of ideal MOS diode capacitance under three different bias voltages. As shown in Fig. 2-11, the first condition, we add a minus bias voltage on the metal gate and then the energy band of the interface between oxide layer and semiconductor bend upward. The interface will attract some holes to accumulate around and we name this condition: accumulation. This is real oxide capacitance.

The second condition, we add a small positive bias voltage and then the energy band bends downward. The holes of around interface will be repelled and form a depletion layer. We name this condition: depletion. Because the measurement capacitance is the oxide capacitance series connected with the depletion capacitance, so the total capacitance is smaller. The third condition, we add a large positive bias voltage on the metal gate and then the energy band bends downward drastically. The interface around will not only form depletion layer but also attract some electrons.

When the numbers of minority electrons are more than majority holes and the surface will form inversion phenomenon. We name this condition is: inversion. If the measurement frequency is high, the capacitance is constant due to the width of depletion layer up to maximum. If the measurement frequency is low, the recombination and generation rate of the minority carrier will catch up with the changing of low frequency. The carrier changing will happen at interface around totally and the capacitance is larger and larger up to oxide capacitance [61, 62]. The capacitance-voltage curves of three conditions are shown in Fig. 2-12.



Chapter 3

Electrical Characteristics of Al/Ti/HfAlO(HfO₂)/Si MIS Capacitors

3.1 Capacitance-Voltage Characteristics

In order to measure the C-V characteristics of our MIS capacitors we used HP2484C LCR meter in our experiments. We swept the gate bias from inversion region to accumulation region to obtain the curve at the frequency of 50 kHz. There are three kinds of plasma treatment with different source gas (i.e. N₂, N₂O, and NH₃) with CF₄ plasma and they were treated with CF₄ for different process time (i.e. 0 sec, 30 sec, 60sec, 90 sec,120 sec). Hence, the relationship of difference process time with CF₄ in one kinds of plasma treatment will be discussed.

Figure 3-1 reveals the capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N₂ plasma treatment for 30sec and CF₄ plasma for different process time. The capacitor treated with CF₄ for 30 sec and 60 sec shows almost the same maximum capacitance among these conditions of process time. In addition, the capacitor treated with CF₄ for 60 second shows the good C values which are larger than the capacitor with the condition of no treatment. This phenomenon indicates that the N₂ plasma treatment with CF₄ was workable to improve the capacitance. Maybe it is caused by elimination of oxygen vacancies with optimal nitrogen and fluorine doping. The growing of interfacial oxide has also been restrained. On the other hand, the capacitance treated with CF₄ for 90 sec is lower than others except for the no-treated sample. It seems that the plasma damage occur and then destroy the

structure of high-k capacitance when the duration of plasma treatment is too long. We can also find that the capacitance treated with CF_4 for 60sec is larger than only treated with N_2 plasma, so capacitance with optimal nitrogen and fluorine doping can have better performance than only with the nitrogen doping.

Figure 3-2 shows the capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with NH_3 plasma 30sec and CF_4 plasma treatment for different process time. Just like the group of N_2 plasma treatment. The improvement of capacitance and the damage cause by excessive plasma treatment both can be seen. At this condition, the capacitance treated with CF_4 plasma treatment for 60 second shows the largest value. After that, the capacitance becomes worse with the increase of the treatment time. By the way, all the other samples all have larger capacitance than the original sample. It is indicated that the optimal NH_3 and CF_4 plasma treatment is also a practicable method to improve the capacitance-voltage characteristics of HfAlO gate dielectrics.

Figure 3-3 shows the capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N_2O plasma 30sec and CF_4 plasma treatment for different process time. We can find that the capacitance with CF_4 plasma treatment for 30sec have largest value than others, it is because the optimal condition between nitrogen and fluorine causes the elimination of oxygen vacancies in Hf-based layer and has no excess charge. Also, it is shown that the capacitors treated with CF_4 for 0 sec, 60 sec, and 90 sec have larger capacitances than the origin sample. Take the view of 120 sec condition, its capacitance value is lower than the origin samples, it may be the interfacial layer growth. Besides 120 sec conditions, the other samples still remain good capacitances than origin sample. So it can be known that the long plasma time

will damage the sample and cause interfacial layer growth. It is suggested that plasma treatment with fluorine radical may cause additional etching for the dielectric layer. Because the destruction of the oxide layer, the total capacitance was be affected and become lower.

Figure 3-4 shows the capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with N₂ plasma 60 sec and CF₄ plasma treatment for different process time. The capacitor treated with CF₄ for 60 sec shows the maximum capacitance among these conditions of process time. Furthermore, the capacitor treated for 90 sec and 120 sec both show the bad capacitance values. Hence, we can suppose that there is an etched-thin film caused by Fluoridation of a long time, it would cause the distortion of the C-V curve.

Figure 3-5 shows the capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with NH₃ plasma 90sec and CF₄ plasma treatment for different process time. Just like the samples of N₂ and CF₄ plasma treatment, the improvement of capacitance could be seen at CF₄ 60sec plasma treatment. At this condition, the capacitance value shows $2.1 \times 10^{-6} \text{F/cm}^2$. By the way, the samples treated with CF₄ plasma for 120 sec has a lower capacitance than the sample without treatment. It indicates that too much CF₄ plasma treatment is also an etchant to etch thin films and degrade the capacitance-voltage characteristics of HfO₂ gate dielectrics.

Figure 3-6 shows the capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with N₂O plasma 90sec and CF₄ plasma treatment for different process time. For the condition of CF₄ plasma 30 sec, we notice the capacitance with very large value than the origin sample, but it is still a little lower than the condition

of CF_4 plasma 60 sec. This is due to no achievement of optimal condition between Nitridation and Fluorination. The best condition we thought is CF_4 60sec plasma treatment, because the leakage current is reduced (see below) and the capacitance is the largest among these conditions. The improvement of capacitance could be seen. At this condition, the capacitance treated with CF_4 plasma for 90 sec and 120 sec show the worse value when Fluorination time is raised. By the way, all the samples which use CF_4 plasma except for CF_4 120sec have larger capacitance than the sample without treatment. It is indicated that N_2O and CF_4 plasma treatment, can also be a practicable method to improve the capacitance-voltage characteristics of HfO_2 gate dielectrics. Finally, the sample treated with CF_4 plasma for 120 sec is bad due to plasma damage.

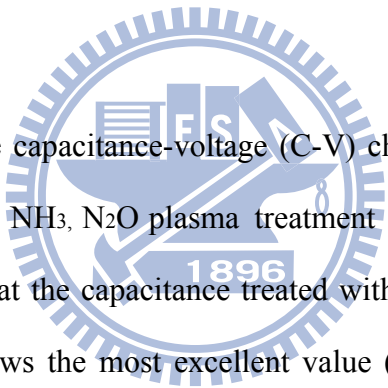


Figure 3-7 shows the capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N_2 , NH_3 , N_2O plasma treatment and CF_4 plasma at optimal condition. It is indicated that the capacitance treated with NH_3 plasma treatment and CF_4 plasma for 60 sec shows the most excellent value (i.e. 278% increasing about capacitance). Because NH_3 compose of N atoms to repair defects and dangling bonds, and fluorine also can repair interface state and let the interface have no excess charge. Among these samples, the capacitance treated with N_2O plasma treatment is worse because N_2O has oxygen atoms and the growing of interfacial oxide is unavoidable while the oxygen atoms become radical and enter the interface. But there is a good effect on capacitance by Nitridation and Fluorination, it can maintain large enough capacitance value. Thus, the capacitance improvement by interface repair was easily observed by Nitridation and Fluorination.

Figure 3-8 shows the the capacitance-voltage (C-V) characteristics of HfO_2 gate

dielectrics treated with N₂, NH₃, N₂O plasma treatment and CF₄ plasma at optimal condition. It is indicated that the capacitance treated with N₂ plasma treatment and CF₄ plasma for 60 sec shows the most excellent value (i.e. 258% increasing about capacitance). Among these samples, the reason why the sample treated with NH₃ plasma has lower capacitance than N₂O plasma treatment is complex. It may be that NH₃ has the least N atoms to repair defects and dangling bonds. NH₃ has hydrogen atoms to bond with dangling bonds but the bond is weak.

Figure 3-9 shows the capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N₂, NH₃ and N₂O plasma treatment all for 30 sec. It is indicated that the capacitance treated with N₂ plasma treatment for 30 sec shows the most excellent value. Fig.3-10 shows the capacitance-voltage (C-V) of HfO₂ gate dielectrics treated with N₂ plasma treatment for 60 sec, NH₃ plasma treatment for 90 sec and N₂O plasma treatment for 90 sec. It is indicated that the capacitance treated with NH₃ plasma treatment for 90 sec shows the most excellent value

3.2 Current-Voltage Characteristic

Figure 3-11 shows the J-V characteristics of p-type HfAlO capacitors treated with N₂ plasma 30 sec and CF₄ treatment for different process time from 0 V to -2 V. We observed that the gate leakage current density is suppressed while treatment conditions are 30sec, 60sec, 90 sec. It is indicated that N₂ plasma and CF₄ plasma treatment supply an effective barrier against the leakage current. The lower leakage shows that the weak structure of interface must be fixed by the plasma nitridation and fluorination, especially for 60 sec capacitor which both has the low leakage and largest capacitance value from Fig. 3-1. Gate leakage current density of origin insulator at V_G = -1 V is about 9.025×10⁻² A/cm². From fig.3-11, however, gate

leakage current density of the capacitor treated for 60 sec CF₄ plasma at V_G = -1 V is only about 1.52×10^{-2} A/cm². It has less gate leakage than origin insulator about 1 orders. Furthermore, we notices that the 90 sec capacitor although has lower leakage than the origin, its capacitance has become degradation. This is an interesting phenomenon. Even though the plasma damage has begun to reduce C value, the leakage current is still kept very well. It means that the capacitance value is more easily affected by plasma damage than leakage current.

Figure 3-12 shows the J-V characteristics of p-type HfAlO capacitors treated by NH₃ plasma 30sec and CF₄ plasma with different process time from 0 V to -2 V. After NH₃ plasma and CF₄ plasma treatment, we can see the reduction of leakage current in contrast of the original sample. It is worthy to be noticed that the capacitors treated by 60 sec CF₄ plasma which has the best C value also performs a low leakage current about 1.32×10^{-4} A/cm² at V_g = -1V. In addition, we find that the leakage current of 120 sec treatment are larger than the other sample, but they are all not larger than original sample. Relative to the case of N₂ plasma, we can see that the level of leakage current increase obviously due to plasma damage.

Figure 3-13 shows the J-V characteristics of p-type HfAlO capacitors treated by N₂O plasma 30sec and CF₄ plasma with different process time from 0 V to -2 V. Besides 120 sec sample, the other samples depict the presence of the reduction in leakage current. It is indicated that there are not only the effect of improving interface quality but also another effect to suppress the leakage current in the case. According to the discussion about Fig. 3-3, we know that the growth of interfacial oxide layer will decrease the C value. Now the interfacial layer introduces a hard barrier to suppress leakage current. Consequently, everythig except for that 120 sec condition,

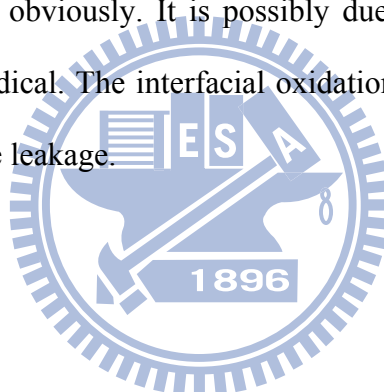
all have revealed a lower leakage current value, due to the destruction caused by the plasma.

Figure 3-14 shows the J-V characteristics of p-type HfO₂ capacitors treated by N₂ plasma 30sec and CF₄ plasma with different process time from 0 V to -2 V. We observed that the gate leakage current density is suppressed while treatment conditions are 60 sec and 90 sec. The results show that fluorine and nitrogen atoms were accumulate into the HfO₂ dielectrics to form Hf-F and Hf-N bonding by CF₄ and N₂ plasma, resulting in the reduction of gate leakage current, charge trapping. Especially for capacitor which treated with CF₄ plasma 60 sec and it also has the lower leakage and largest capacitance value from Fig. 3-4. Gate leakage current density of no treatment insulator at VG = -2 V is about 1.35 A/cm². From Fig.3-3, however, gate leakage current density of the capacitor treated for 60 sec CF₄ plasma at VG = -2 V is about 0.25 A/cm². It has less gate leakage than no treatment insulator about 1 order. Furthermore, we notices that the capacitor treated with N₂ plasma for 130 sec has high leakage current, it is might be that the CF₄ plasma is too little time to react with the film. Then, we observed that the leakage of the sample with 120 sec CF₄ plasma is also larger than the origin due to plasma damage.

Figure 3-15 shows the J-V characteristics of p-type HfO₂ capacitors treated by NH₃ plasma 90sec and CF₄ plasma with different process time from 0V to -2V. After NH₃ plasma treatment, we could see the reduction of leakage current for 90 sec sample in contrast of no treatment sample. However, the sample of plasma treated for 60 sec got the little large gate leakage current but a sharp J-V curve and good C-V curve from Fig 3-5. It is indicated that the sample with CF₄ 60sec is good for interface characteristics. Relative to the case of N₂ plus CF₄ plasma, we could see that the

level of leakage current increasing obviously. It is possibly that the time with NH_3 and CF_4 plasma too long cause etching the thin film by fluorine radicals.

Figure 3-16 shows the J-V characteristics of p-type HfO_2 capacitors treated by N_2O plasma 90sec and CF_4 plasma with different process time from 0V to -2V. After N_2O plasma treatment, we could see the reduction of leakage current in contrast of no treatment samples except the 30sec sample. It is indicated that the plasma treatment could be less for fluorine radicals to fixed interface trapped charge. However, the sample of plasma treated for 60 sec got the small gate leakage current and a good C-V curve from Fig 3-6. Relative to the case of N_2 plasma, we could see that the level of leakage current decreasing obviously. It is possibly due to the additional oxidation layer formed by oxygen radical. The interfacial oxidation layer will let the dielectric thicker to prevent from gate leakage.



3.3 Summary

By the compare of the samples which has the best capacitance in their own gas, we can realize the most suitable treatment condition which both has the best capacitance and lower leakage current. Hence, we significantly find a relative optimum condition among above discussion. It is proved that without thick oxidation layer, it can also reach the smallest leakage current when there is suitable time treatment.

If we take a look at all the samples, we find that most of the N_2 , N_2O , and NH_3 plasma treatment shows better electrical properties than original sample. Furthermore,

the N element and F element can fix the interface and promote the electrical properties include of C-V curve and J-V curve. As for the HfO₂ type of material, oxygen radical can cause growth in the interfacial layer, therefore by comparing with the N₂O plasma treatment's sample, it shows a lower C value. Just because the oxidation phenomenon, the films will become thicker so that the plasma damage will not easily affect the leakage current profile.



Chapter 4

Reliability of Al/HfAlO(HfO₂)/Si MIS Capacitors

4.1 Hysteresis

The name of Hysteresis was borrowed from electromagnetics. It means that when a ferromagnetic material is magnetized in one direction, it will not relax back to zero magnetization when the applied magnetizing field is removed. It must be driven back to zero by the additional opposite direction magnetic field. If an alternating magnetic field is applied to the material, its magnetization will trace out a loop called a hysteresis loop [34].

The hysteresis phenomenon is similar to the C-V curve in the MIS capacitor device. When we apply a voltage in reverse, it will not fit the original C-V curve measured previously. It is due to the interface traps which can trap charges to have impact on the flat band voltage and C-V curve. [23] Fig. 4-1 shows the hysteresis of p-type HfAlO gate dielectrics treated without PDA, plasma treatment and PNA and the hysteresis is 98 mV. Fig. 4-2 shows the hysteresis of p-type HfAlO gate dielectrics treated with N₂ plasma 30 sec plus CF₄ plasma treatment for 60 sec process time. Hysteresis of p-type HfAlO capacitors is changed with the plasma treatment and its value is 7mV. The hysteresis is suppressed by means of the fixing ability at the interface. This means that fluorine incorporation into the HfO₂ gate dielectrics to strengthens the HfO₂ thin film.

Figure 4-3 shows the hysteresis of p-type HfAlO gate dielectrics treated with NH₃ plasma 30sec plus CF₄ plasma treatment for 60 sec process time. The tendency of hysteresis is similar with the case of N₂ plasma treatment and it's value is 19 mV. Fig. 4-4 shows the hysteresis of p-type HfAlO gate dielectrics treated with N₂O plasma 30 sec and CF₄ plasma treatment for 60 sec process time and its value is 41 mV. It also shows a likely tendency. As a consequence, the plasma treatment can improve the reliability of hysteresis for all the different optimal plasma gas treatment. Among these samples, we can find that the hysteresis of N₂ plasma treatment for 30 sec is the smallest but the other values are larger.

Figure 4-5 shows the hysteresis of p-type HfO₂ gate dielectric without any treatment and the hysteresis is 32 mV. Fig. 4-6 shows the hysteresis of p-type HfO₂ gate dielectrics with N₂ plasma 60 sec plus CF₄ plasma treatment for 60 sec process time. The hysteresis voltage is 8mV and also small than the origin.

Figure 4-7 shows the hysteresis of p-type HfO₂ gate dielectrics (MOCVD) with NH₃ plasma 30sec plus CF₄ plasma treatment for 60 sec process time. The hysteresis voltage is 11mV. Fig. 4-8 shows the hysteresis of p-type HfO₂ gate dielectrics (MOCVD) with N₂O plasma 30 sec and CF₄ plasma treatment for 60 sec process time. The hysteresis voltage is 9mV, so nitridation and fluorination could decrease the trap density and let the thin film sustain high thermal stress.

Therefore, we can speculate that the sample without plasma treatment which is not very good at quality of interface oxide layer so that the charge was be trapped at the interface and flat band shift introduce hysteresis.

4.2 Stress Induced Leakage Current (SILC)

In order to investigate the reliability of MIS capacitor device, the stress induced leakage current is a common experiment. The mechanism about SILC is the stress induced trap density in the bulk in thin film. The trap density introduce new leakage path. Fig. 4-9 shows the SILC curve of p-type HfAlO gate dielectrics treated with N₂ plasma 30sec and CF₄ plasma treatment for different process time. After the stress of 5V constant voltage for 120 second, it is observed the leakage shift than before. The degree of leakage current degradation can be judged for the reliability of MIS capacitor. From Fig. 4-9, it displays the improvement of SILC compared with the capacitor of the original sample. Almost most samples are observed smaller increasing of leakage current after SILC than original sample. On the other hand, it is also noticed that the SILC of 90 sec treated sample become worse due to the plasma damage.

Figures 4-10 and 4-11 display the SILC curve of p-type HfAlO gate dielectrics treated with NH₃ plasma plus CF₄ treatment and N₂O plasma plus CF₄ treatment respectively. In Fig. 4-10, it is also noticed that the SILC of 120 sec treated sample become worse due to the plasma damage. In Fig. 4-11, it is observed that the SILC of 90 sec treated sample become lower due to the interfacial layer growth by plasma radicals. They all show the distinct improvement as long as they are treated with CF₄ plasma treatment for 60sec.

Figure 4-12 shows the SILC curve of p-type HfO₂ gate dielectrics treated with N₂ plasma 60sec plus CF₄ plasma for different process time. First, we use constant voltage (5V) for 120 sec to stress the thin film. After the stress of constant voltage (5V) for 120 sec, the gate leakage becomes larger or lower than before. From Fig.

4-12, it is considered that the SILC of sample (600°C-30 sec + N₂ plasma treatment 60 sec + CF₄ plasma treatment 60 sec + 600°C-30 sec) which has the better C-V curve and the lowest leakage shows a small degradation. On the other hand, it is also can be noticed that the SILC of the samples treated with CF₄ 90sec is large due to plasma damage.

Figure 4-13 display the SILC curve of p-type HfO₂ gate dielectrics treated with NH₃ plasma 90sec plus CF₄ plasma for different process time. First, we use (5V) for 120 sec to stress the samples. In Fig. 4-13, it was indicated that the SILC of the sample (600 °C - 30 sec + NH₃ plasma treatment 90sec+ CF₄ plasma treatment 60sec + 600°C-30 sec) was lower than the sample treated with CF₄ 120 sec. The reason why the SILC of the sample treated with CF₄ 120sec is larger than origin may be etching caused by too many fluorine radicals. The leakage current of other samples after stress were larger than no stress samples. So, suitable nitridation and fluorination can decrease the SILC degradation effectively.

Figure 4-14 display the SILC curve of p-type HfO₂ gate dielectrics treated with N₂O plasma 90sec plus CF₄ plasma for different process time. In Fig. 4-14, it was indicated that the SILC of the sample (600 °C - 30 sec + N₂O plasma treatment 90sec+ CF₄ plasma treatment 60sec + 600°C-30 sec) was smaller than others. The reason is the same with NH₃ sample. So the plasma treatment including of N₂, NH₃, and N₂O plus CF₄ as source gas can have the reliability of devices to suppress SILC.

4.3 Constant Voltage Stress (CVS)

To study the reliability of Hf-based film, stressing the film with a constant voltage or a constant current are two common methods. The mechanism about CVS is the charge trapping by the interfacial trap density which is caused by stress for long time. Furthermore, the amount of charges cause more interface trap density and from

new leakage path to gain in leakage. In our experiments, we use constant voltage stress (CVS) to test the reliability of Hf-based film. Fig. 4-15 shows gate current shift of p-type HfAlO gate dielectrics treated with N₂ plasma 30sec and CF₄ plasma treatment for different process time as a function of stress time during V_g = 5 V CVS stress. From the condition of 30 sec to 60 sec, the current shift is smaller than others. Then the current shift begins to become great by the plasma damage at the process time of 90 sec. Fig. 4-16 shows gate current shift of p-type HfAlO gate dielectrics treated with NH₃ plasma and CF₄ plasma treatment for different process time as a function of stress time during V_g = 5 V CVS stress. It has similar behavior about the trend compared with N₂ plus CF₄ sample. Fig. 4-17 shows gate current shift of p-type HfAlO gate dielectrics treated with N₂O plasma and CF₄ plasma treatment for different process time as a function of stress time during V_g = 5 V CVS stress. While the 60-sec treated sample presents the lowest current shift, the 120 sec treated sample become to be destroyed by the plasma damage.

Figure 4-18 shows gate current shift of p-type HfO₂ gate dielectrics treated with N₂ plasma treatment 60 sec and CF₄ plasma for different process time during CVS with V_g = 5 V. It indicated that the thin film with N₂ plasma treatment 60 sec which current shift was smaller than the original one. We can observe that the leakage shift of the sample with CF₄ plasma 90 sec is larger than others except for origin. It may be caused by etching the Hf-based thin film with many fluorine radicals.

Figure 4-19 shows gate current shift of p-type HfO₂ gate dielectrics treated with NH₃ plasma treatment 90 sec and CF₄ plasma for different process time during CVS with V_g =5 V. It indicated that the thin film with NH₃ plasma treatment plus CF₄ 60 sec which current shift was smaller than the original one. The reason is the same with the sample treated by N₂ plasma.

Figure 4-20 shows gate current shift of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment 90 sec and CF_4 plasma for different process time during CVS with $V_g = 5 \text{ V}$. It indicated that current shift of the thin film with CF_4 plasma treatment 60 sec was smaller than the original one. The samples with CF_4 plasma treatment 90 sec and 120 sec also had smaller current shift. Therefore, the growth of the interfacial layer may be caused by oxygen and fluorine radicals. The gate leakage shift level of the samples with or without nitridation and fluorination different about 2 orders, so nitridation and fluorination process could decrease the trap density effectively. Perhaps, one of the ways to improve the reliability of the gate dielectrics, is by incorporating N and F atoms in the thin film.



Chapter 5

Conclusions and Future work

5.1 Conclusions

In this thesis, we used the post-deposition annealing, plasma treatment and post-nitridation to enrich the Hf-based film quality. The plasma treatment conditions are N_2 , NH_3 , and N_2O plasma plus CF_4 plasma for 30 sec, 60 sec, 90 sec, 120 sec respectively. Several important phenomena were observed and summarized as follows. First of all, improvement in the electrical characteristics of Al/Ti/HfAlO(HfO_2)/Si MIS capacitors using plasma treatment has been demonstrated in this thesis. Most of the plasma treatment samples can promote the electrical characteristics and reliability until the plasma damage or the growth of interfacial layer happened. Among these treatments, the samples using N_2 , NH_3 and N_2O plasma plus CF_4 plasma all for 60 sec represent significantly great improvement, such as good capacitance, reduced leakage current (about 2 order reduction). It is observed that the formation of interfacial layer has been suppressed and the weak structure of interface has been repaired by N_2 , NH_3 and N_2O plasma plus CF_4 plasma respectively. Besides, the sample treated by N_2 , NH_3 , and N_2O plasma all for 60 sec also show excellent promotion about reliability issue, such as smaller hysteresis, less SILC and better CVS curve. These results were ascribed to the good interface quality. On the one hand, the N_2O plasma treatment has the lower leakage current than other plasma for HfO_2 . The reason is that the samples using N_2O plasma and CF_4 plasma treatment will introduce oxygen bonding to form

additional interfacial layer so that the capacitance will be lower. On the other hand, the thicker oxidation layer generates a good resistance against leakage current. Finally, in this thesis, the key points we focus on are both the improvement of capacitance and leakage current.

F in the oxygen vacancies of HfO_2 will cause the leakage current decrease. The results show that fluorine atoms were accumulate into the HfO_2 dielectrics to form Hf-F bonding by CF_4 plasma, resulting in the reduction of gate leakage current, charge trapping, and the hysteresis. This means that fluorine incorporation into the HfO_2 gate dielectrics to strengthens the HfO_2 thin film. After CF_4 plasma treatment, the fluorine atoms were incorporated into the interfacial layer (HfO_2 -Si interface) resulting in less charge trapping. It is indicated that fluorine atoms almost entirely distributed in the surface of the Si substrate and the interface between the Al/Ti gate and the HfO_2 thin film. The fluorine atoms would first accumulate at the surface of the HfO_2 thin film and then diffused through the HfO_2 thin film to terminate the dangling bond and accumulate at the interfacial layer between the HfO_2 thin film and the Si substrate. After the incorporation of fluorine atoms, the Hf-F bonding formation led to the reduction of charge trapping. With F passivation, V_{th} instability was improved and the stress-induced leakage current decreased greatly. They showed that F incorporation decreased the flatband voltage (V_{fb}) shift and suppressed the interface state generation.

5.2 Future work

1. The reason of leakage current mechanism :

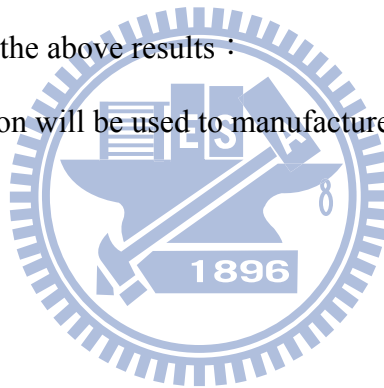
We must try to research the mechanism for leakage current with SE, FP, F-N tunneling effect in Hf-based thin film further. Therefore, we can realize the mechanism of leakage and effectively prevent leakage problem.

2. Material Analysis :

We can use some material analysis methods such as TEM, SIMS, AFM to know the thin film composition precisely and verify the phenomenon observed from C-V and J-V curve, SILC, CVS etc.

3. Devices fabrication with the above results :

The optimum condition will be used to manufacture MOS device in the future.



Table

Continuation of Moore's Law								
Intel found a solution for High-k and metal gate								
Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25 μ m	0.18 μ m	0.13 μ m	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Straine Si	Strained Si	Strained Si
Gate dielectric	SiO ₂	SiO ₂	SiO ₂	SiO ₂	SiO ₂	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal
Potential candidate for introduction						Subject to change		
Up to 22nm!								
Source: Intel 46								

Table 1-1 The time of intel corporation found a solution for high-k and metal gate to keep continuation of Moor's Law

Criteria	Requirements
EOT scalability < 10Å	Dielectric constant > 15
Negligible FIBL effect	Dielectric constant < 60
Leakage current < 1 A/cm ² @ 1V	Bandgap > 5 eV Barrier height > 1 eV
Thermal stability	No silicidation and
Hysteresis	< 20 mv
Dispersion	< 1 %/decade
Interface state density	< 10 ¹¹ /eVcm ²
Mobility	> 85 % of SiO ₂
Reliability	> 10 years

Table 1-2: Material requirements of high-k dielectrics

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

Table 1-3 Comparison of relevant properties for various high- k candidates [32].

^aCalculated by Robertson.

^bMono.=monoclinic.

^cTetrag.=tetragonal.

Physical Vapor Deposition (PVD)	Chemical Vapor Deposition (CVD)	
	MOCVD	ALCVD
Pros: 1. Convenient for new materials screening. 2. Easy to fabricate experimental data. 3. Low cost for ownership	Pros: 1. Superior step coverage. 2. High deposition rate. 3. Good controllability of composition. 4. Uniformity of film thickness.	Pros: 1. Better thin film quality. 2. Excellent coverage and conformability.
Cons: 1. Planar, line-of-sight process, damage. 2. Not likely to be used in ULSI gate process. 3. Poor conformability, especially for high aspect ratio.	Cons: 1. Hard to deposit ultra thin films 2. Carbon contamination	Cons: 1. Low throughput. 2. Mechanism-related surface sensitivity. 3. Chemistry-limited final products (only binary materials are available now).

Table 2-1 Comparison of deposition techniques: Sputter, ALCVD, and MOCVD [53].

Figure-chapter 1

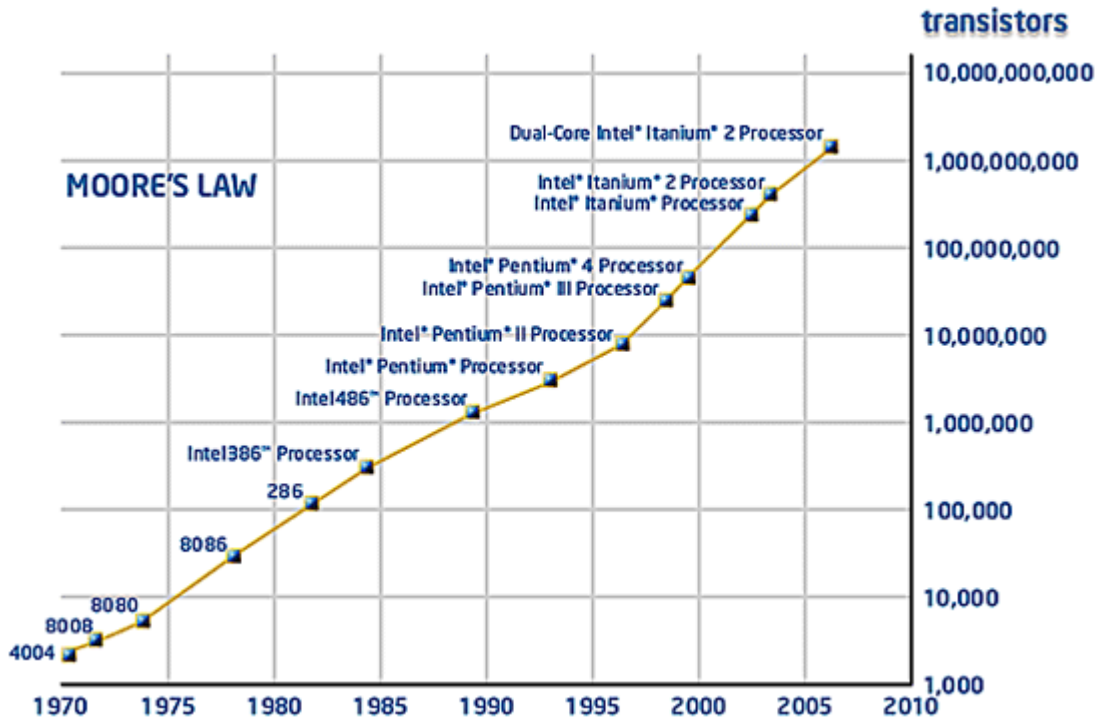


Figure 1-1 Illustration of Moore's law: number of transistors integrated in the different generations of Intel's microprocessors vs. the production year of these circuits.

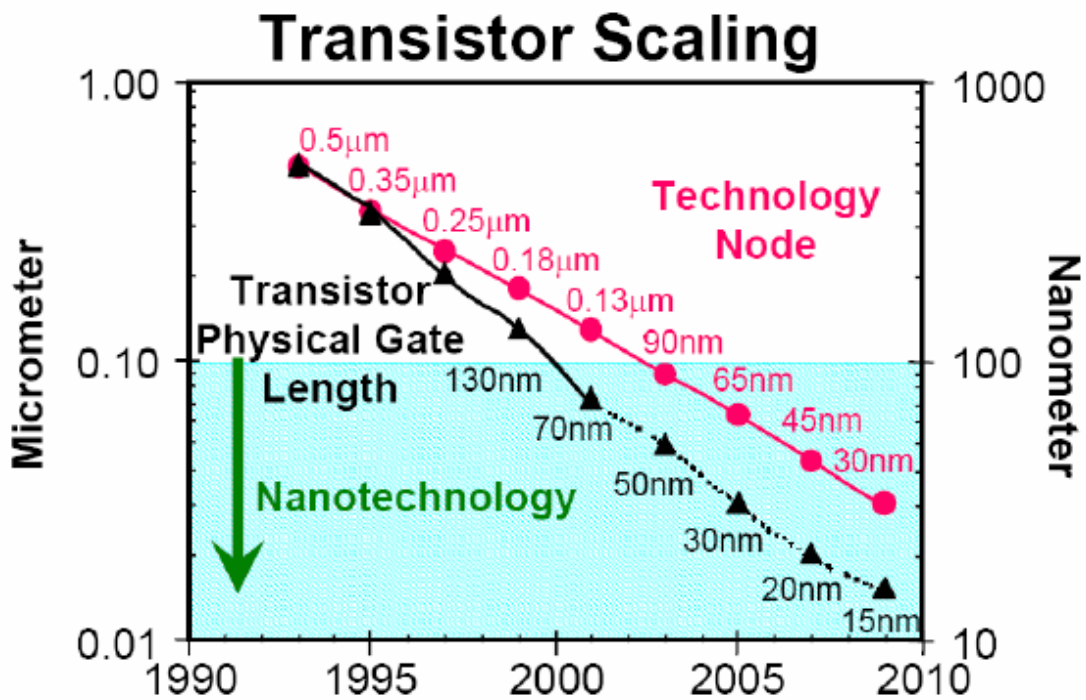


Figure 1-2 Trend of device scaling: Transistor physical gate length will reach ~ 15nm before end of this decade and ~ 10nm early next decade.

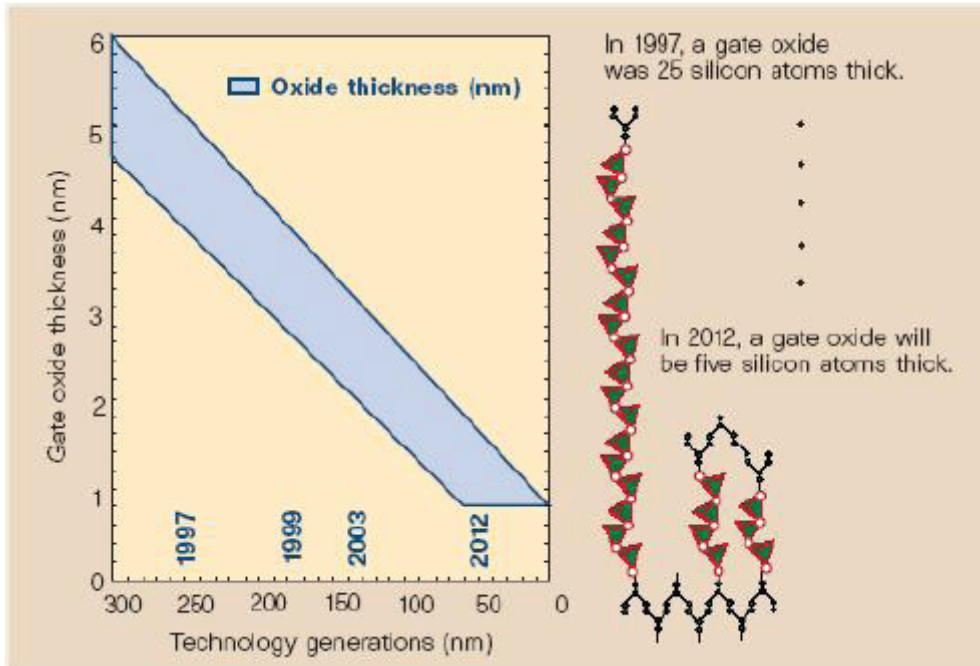


Fig. 1-3 With the marching of technology nodes, gate dielectric has to be shrunk and five silicon atoms thick of gate dielectric is predicted for 2012.[2]

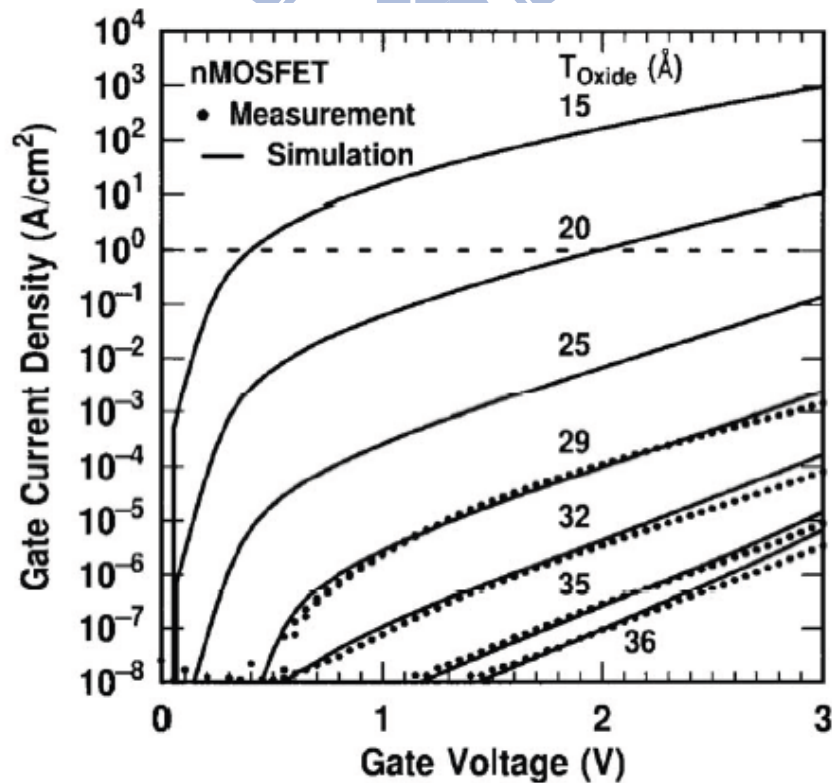


Fig. 1-4 Measured and simulated I_g - V_g characteristics under inversion condition for nMOSFETs. The dotted line indicates the $1\text{A}/\text{cm}^2$ limit for the leakage current. [3]

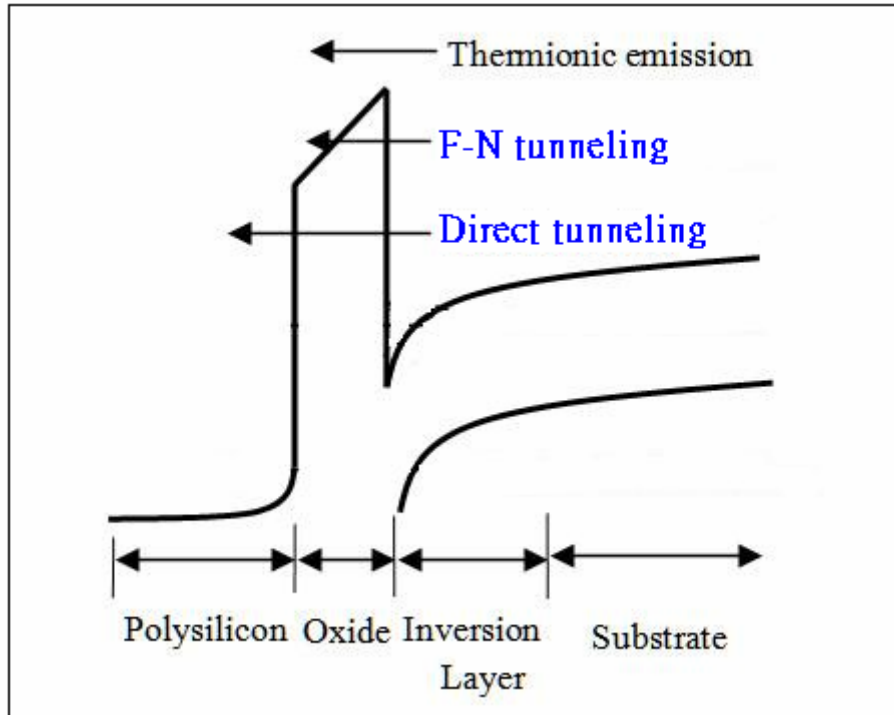


Fig. 1-5 Conduction mechanism in oxide for the MOS structure.

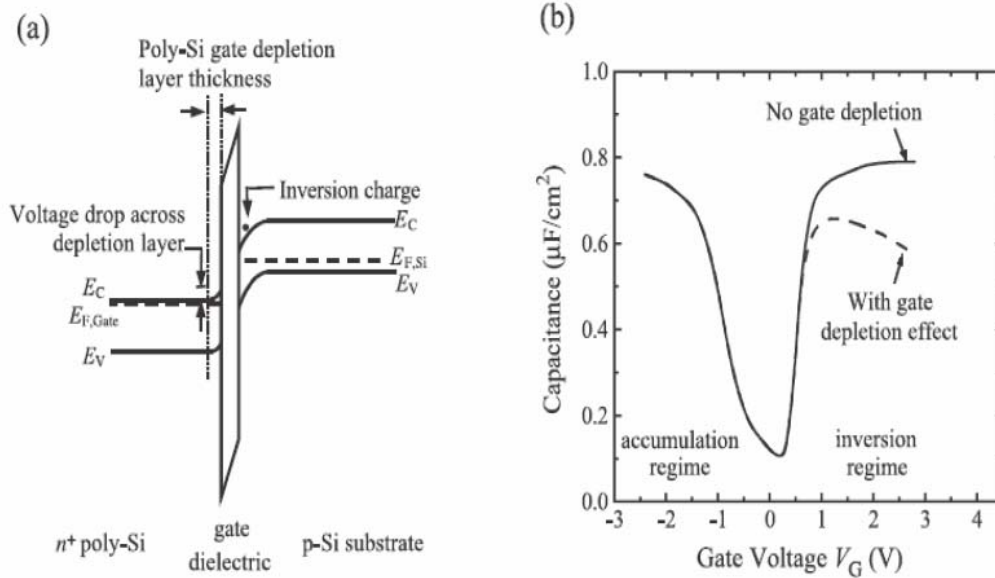


Figure 1-6 (a) Energy band chart of NMOS device (b) The influence of poly-Si depletion for capacitance density.

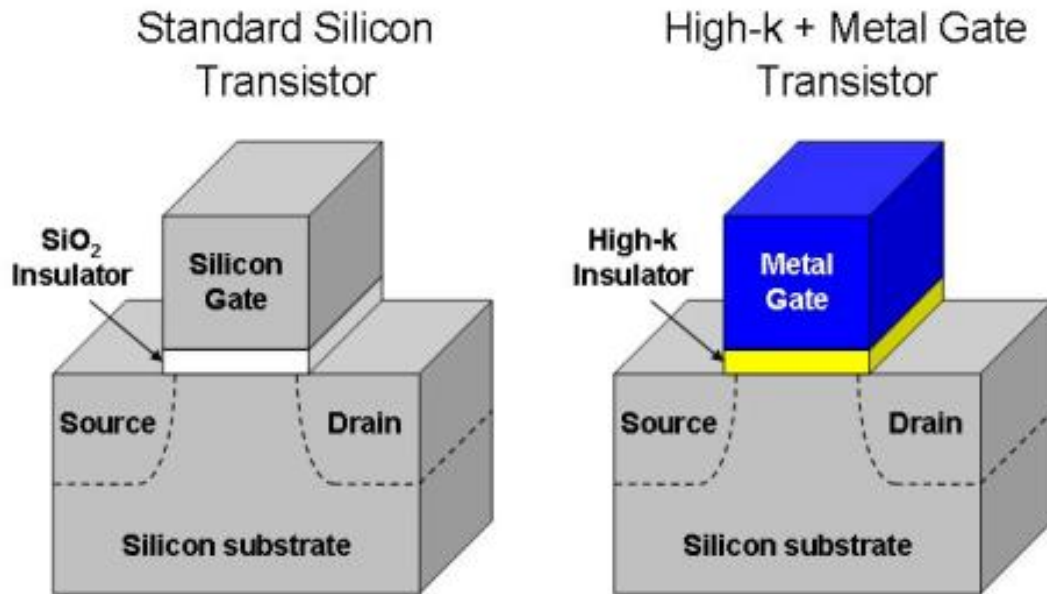


Fig. 1-7 High-k+ metal gate transistors provide significant performance increase and leakage current reduction , ensuring continuation of moor's law.

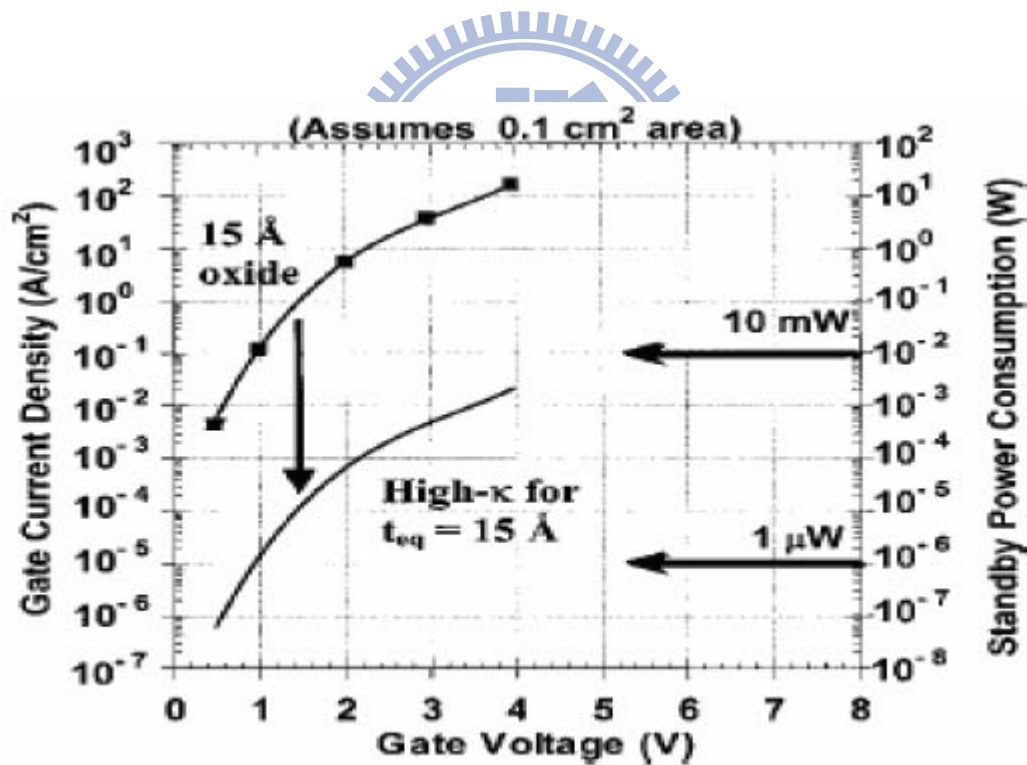
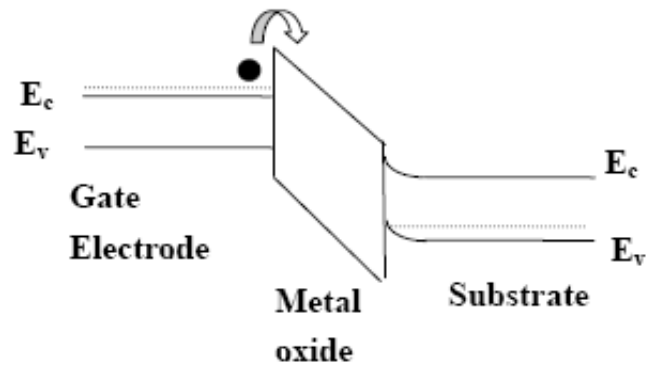
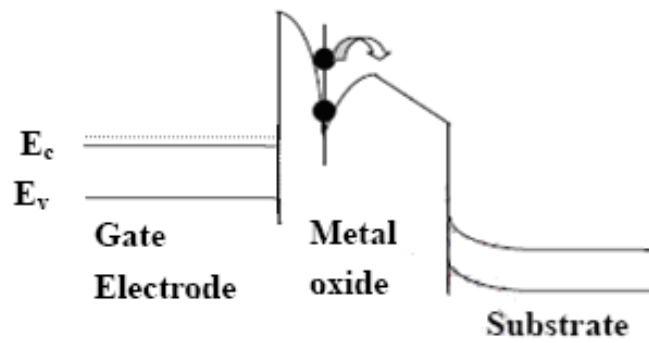


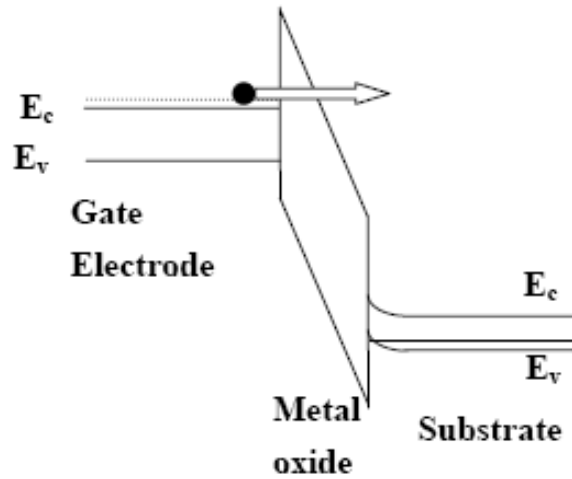
Figure 1-8 Power consumption and gate leakage current density comparing to the potential reduction in leakage current by an alternative dielectric exhibiting the same equivalent oxide thickness [5].



(a) Schottky Emission (SE)



(b) Frenkel-Poole Emission (FP)



(c) Fowler-Nordheim Tunneling (F-N)

Figure 1-9 (a) Schottky Emission (SE) (b) Frenkel-Poole Emission (FP)
(c)Fowler-Nordheim Tunneling (F-N) current transport mechanism.

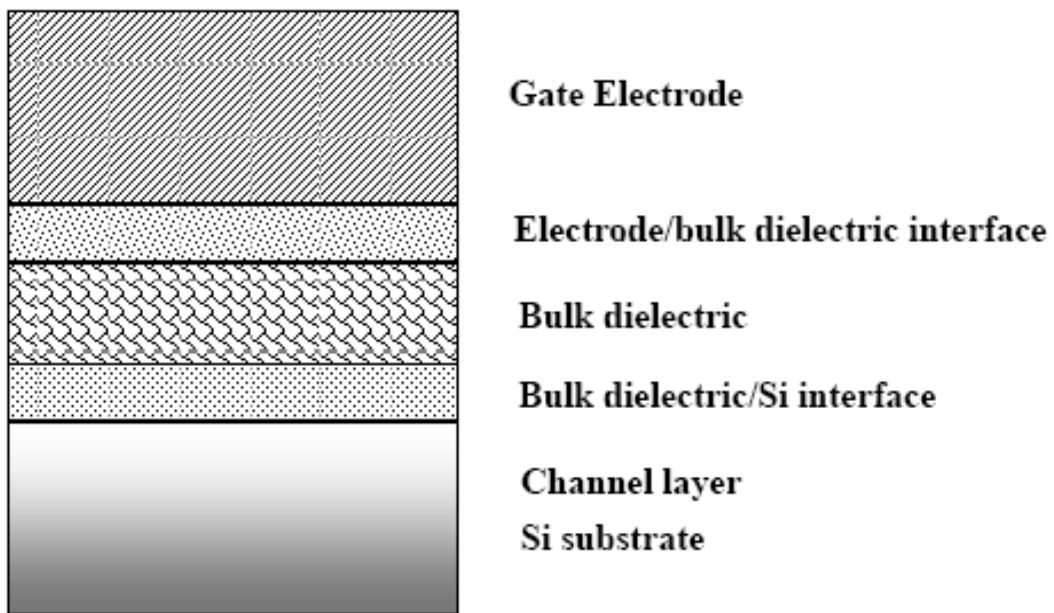


Figure 1-10 schemes of important regions in gate stack of a field effect transistor

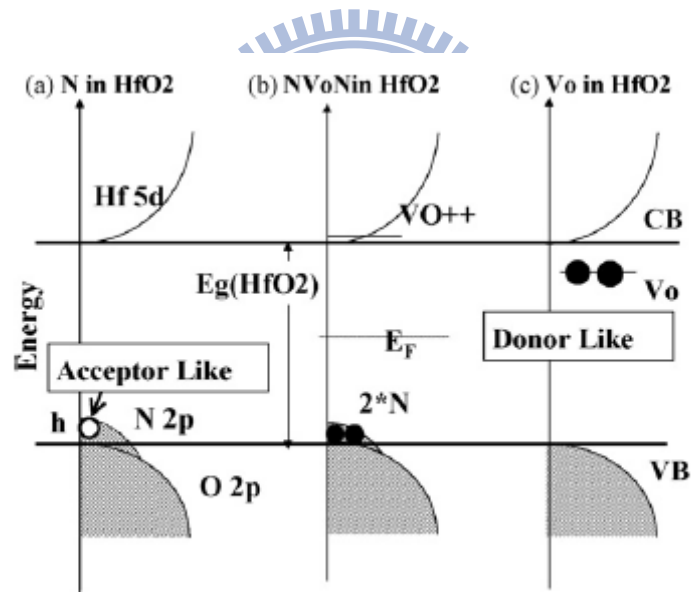


Figure 1-11 V_o induction is from charge compensation in the case of N doping in HfO_2 . (a) N-doped HfO_2 shows p-type semiconductor, if V_o does not appear. Vacant states appear at the top of VB. (b) Band gap recovery by $NsVoNs$ complex structure creation in the case of a small amount of N. (c) V_o -related gap level appears in HfO_2 . This level is occupied, and behaves as a donor to N-doped HfO_2 .

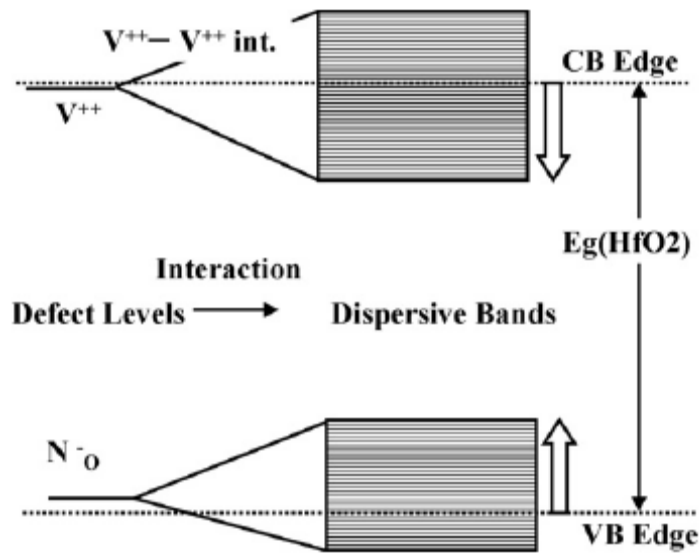


Figure 1-12 A large amount of N induces a large amount of Vo. The Vo–Vo interactions increase with the increase in amount of Vo. CB offset is deteriorated by Vo–Vo interactions. VB offset is deteriorated by Ns–Ns interactions via oxygen atoms.

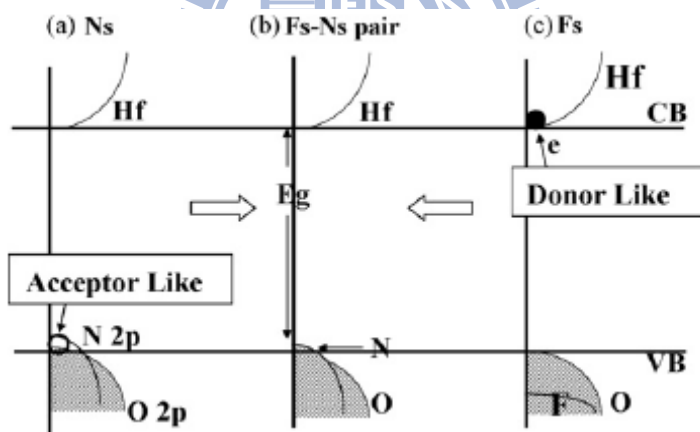


Figure 1-13 Schematic view of the density of states around the band gap of N-doped HfO₂, F- and N-doped HfO₂, and F-doped HfO₂. (a) N-doped HfO₂ shows p-type semiconductor, if Vo does not appear. Vacant states appear at top of VB. (b) Band gap recovery by Fs–Ns pair. (c) No related gap level appears in Fs in HfO₂.

Figure-chapter 2

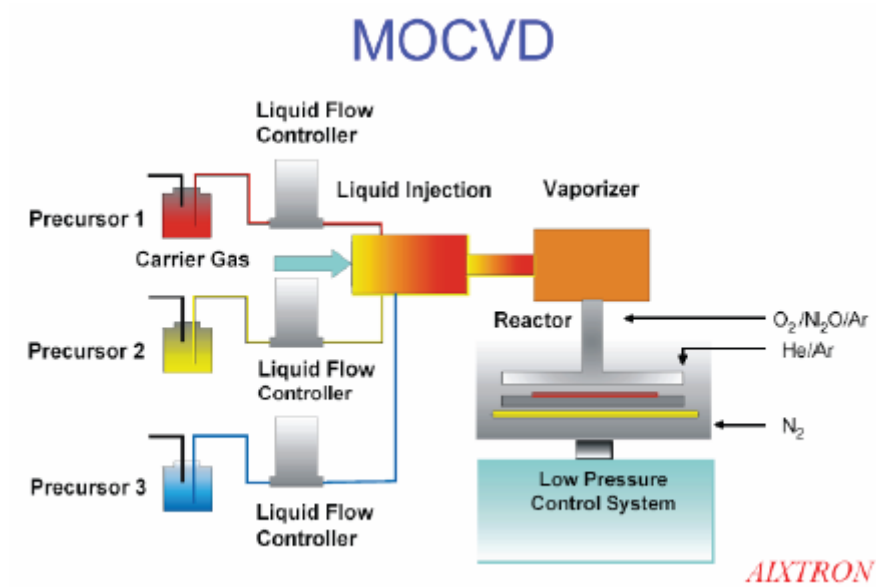


Fig. 2-1 Schematic diagram of MOCVD system structure.

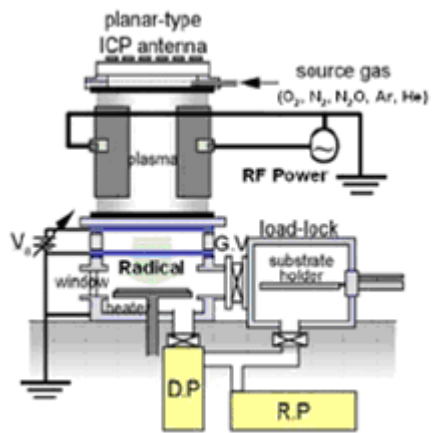


Fig. 2-2 The ICP plasma system that was used in this experiment.



Fig.2-3 (1)Si substrate RCA clean (2)3 nm HfAlO was deposited on the sub-Si by MOCVD.

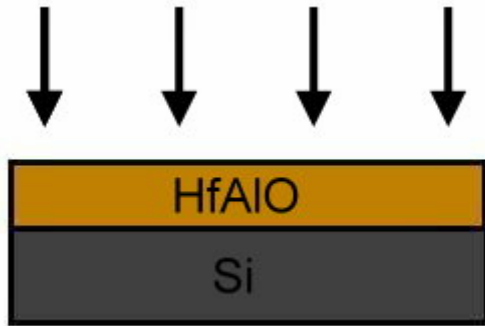


Fig.2-4 (1) PDA by RTA (2) Plasma treatment (3) PNA by RTA



Fig.2-5 20 nm Ti was deposited on the HfAlO layer by dual e-gun evaporation system .



Fig.2-6 400 nm Al was deposited on the Ti layer as top electrode by dual e-gun evaporation system.

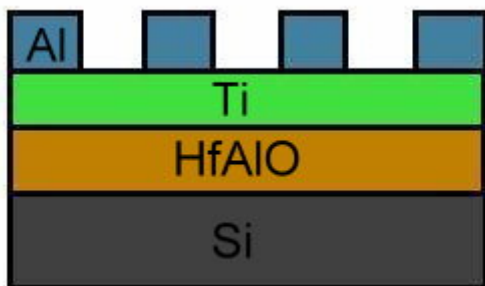


Fig.2-7 Undefined Al was removed by wet etching .

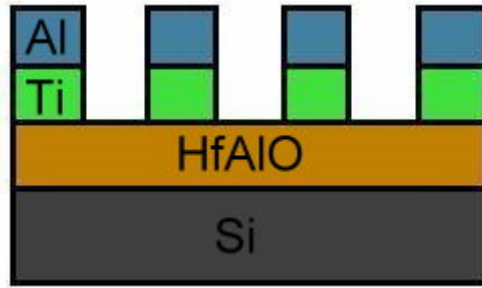


Fig.2-8 Undefined Ti was removed by wet etching (1%HF).

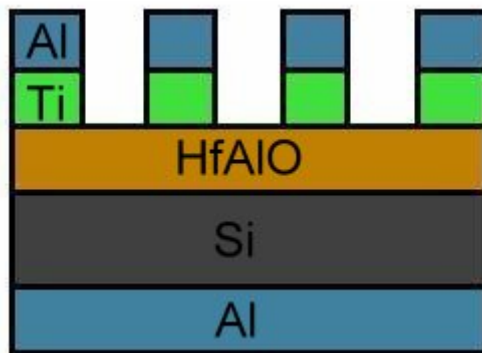


Fig.2-9 Al was deposited on the back side of sub-Si as bottom electrode by dual e-gun evaporation system.



MOS diode

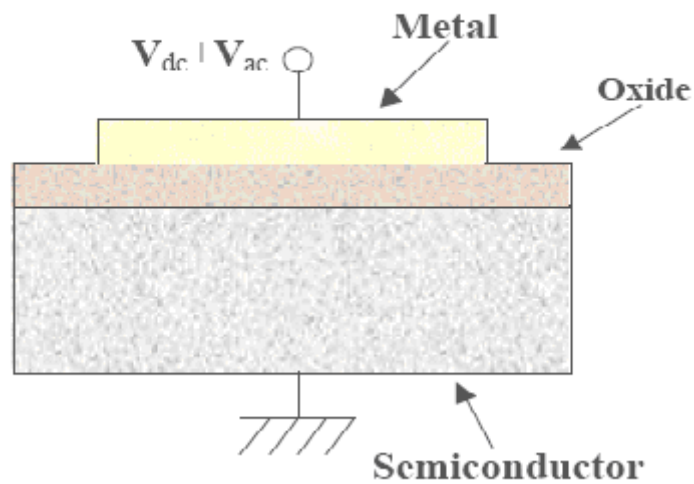


Fig. 2-10 MOS diode capacitance structure

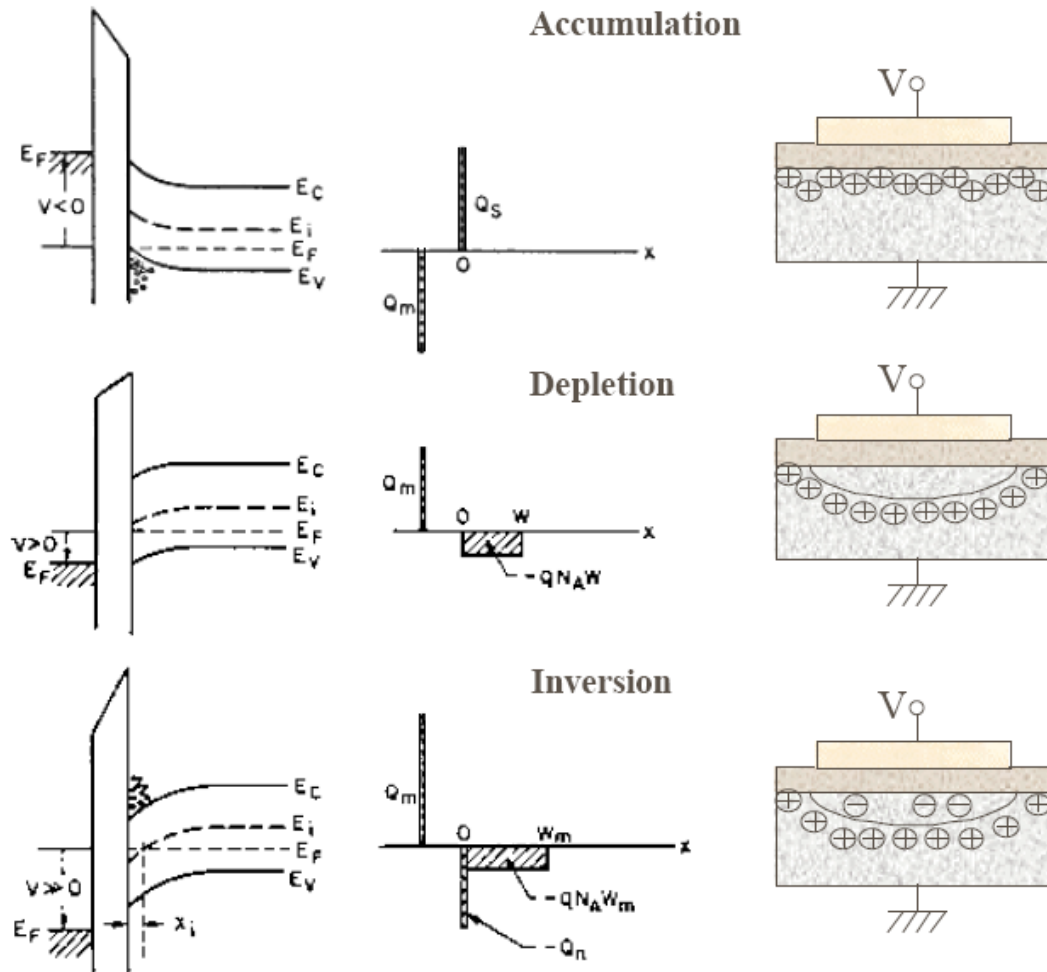


Fig. 2-11 The energy band plot and electric charges distribution of MOS diode capacitance under bias voltage.

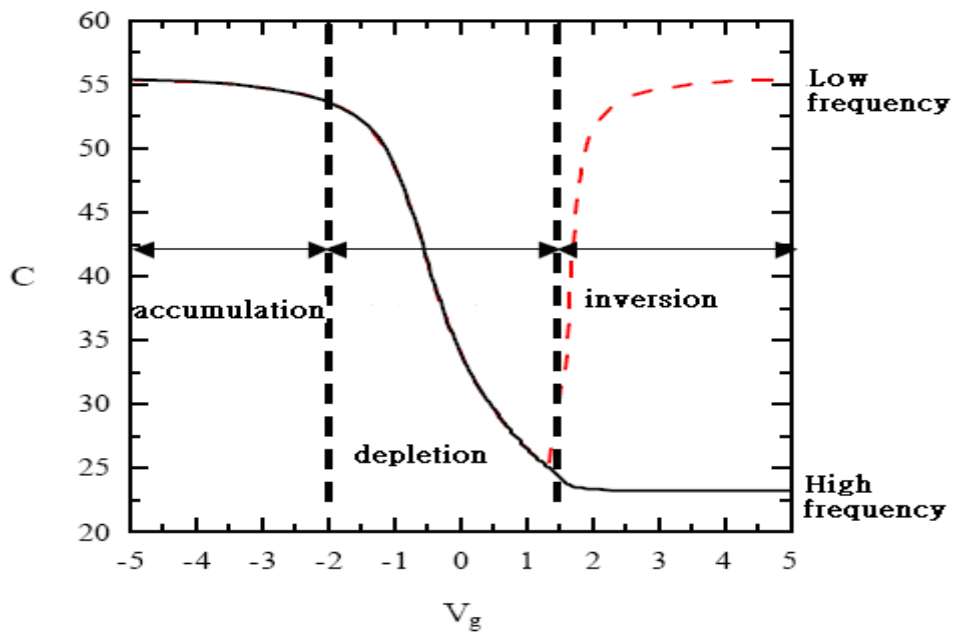


Fig. 2-12 The capacitance-voltage curve of three different conditions

Figure-chapter 3

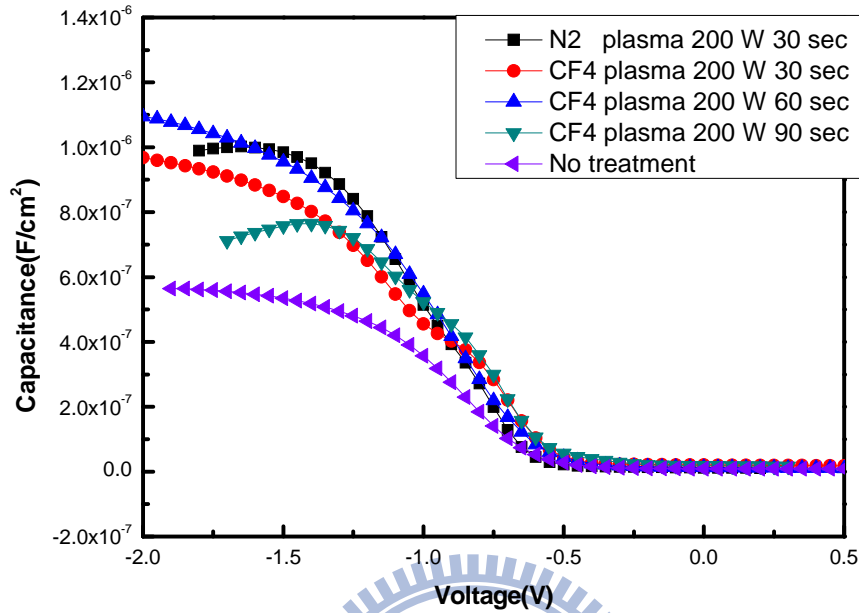


Fig.3-1 The capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N₂ plasma 30 sec and CF₄ treatment for different process time.

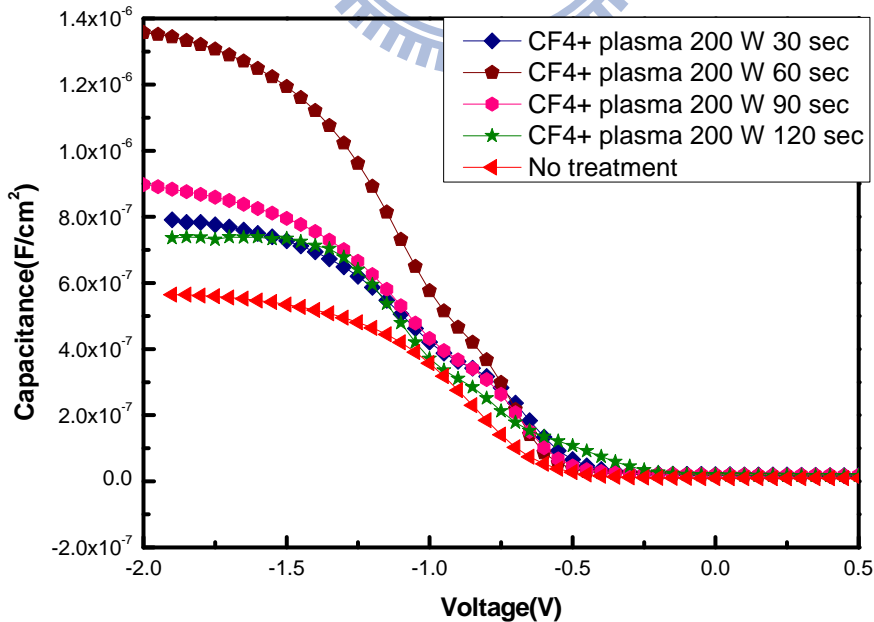


Fig.3-2 The capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with NH₃ plasma 30sec and CF₄ treatment for different process time.

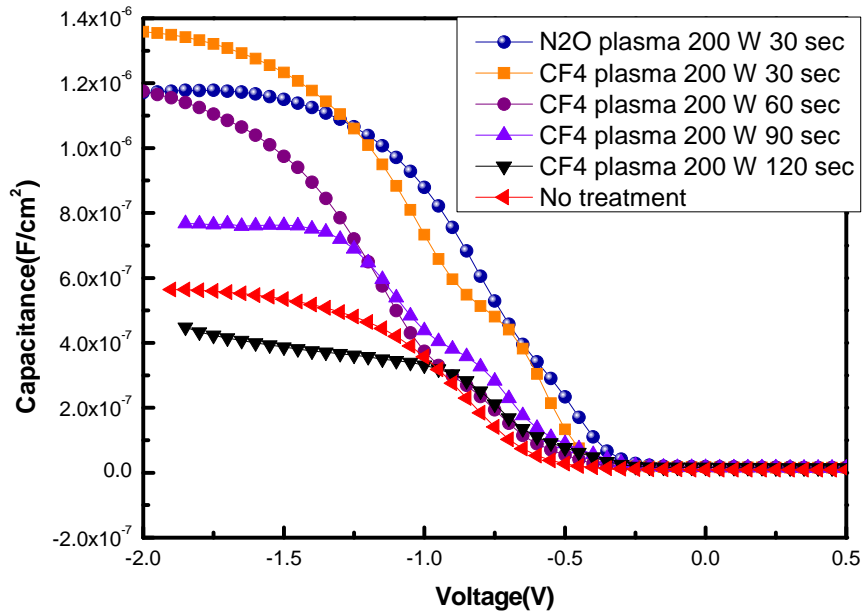


Fig.3-3 The capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N₂O plasma 30 sec and CF₄ plasma treatment for different process time.

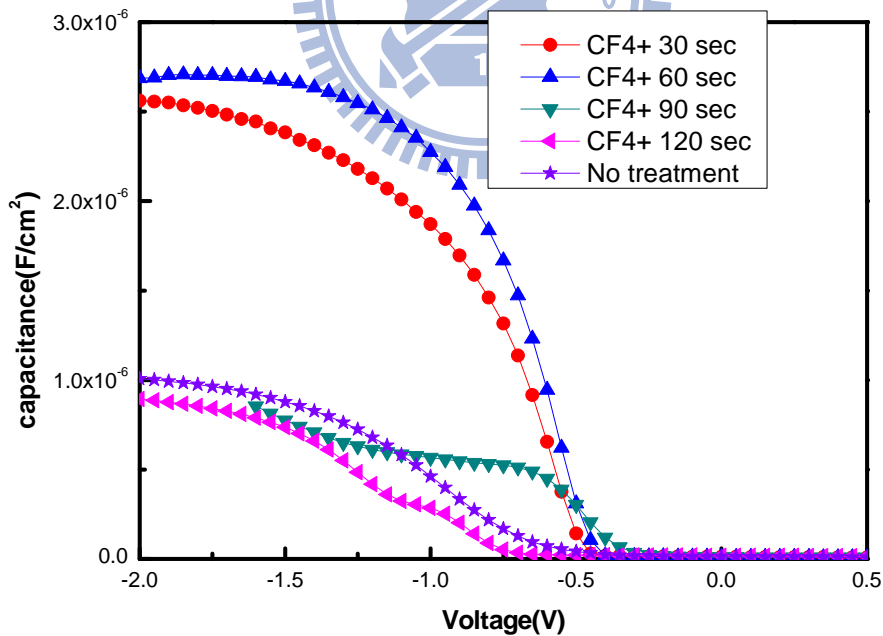


Fig.3-4 The capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with N₂ plasma 60 sec and CF₄ plasma treatment for different process time.

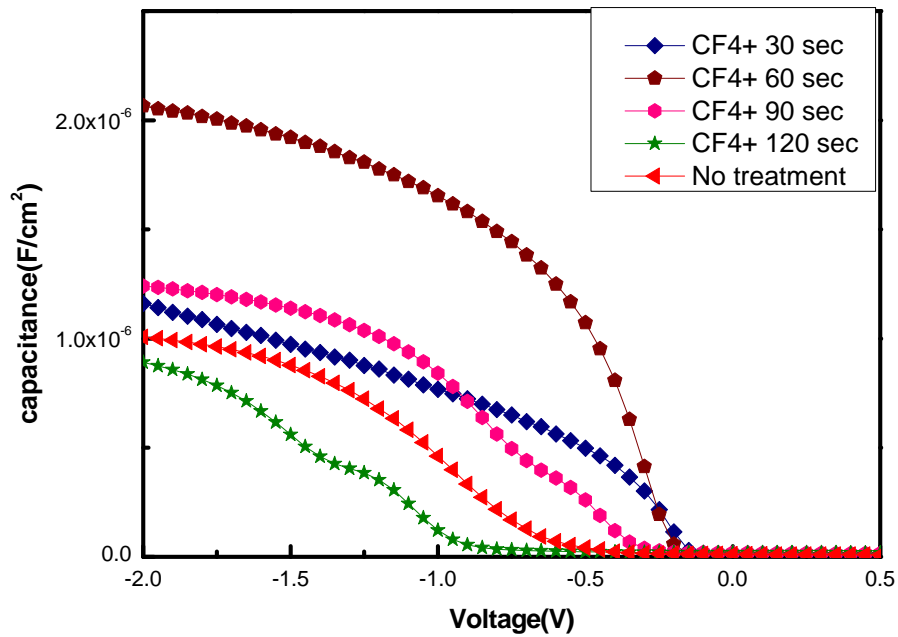


Fig.3-5 The capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with NH₃ plasma 90sec and CF₄ plasma treatment for different process time.

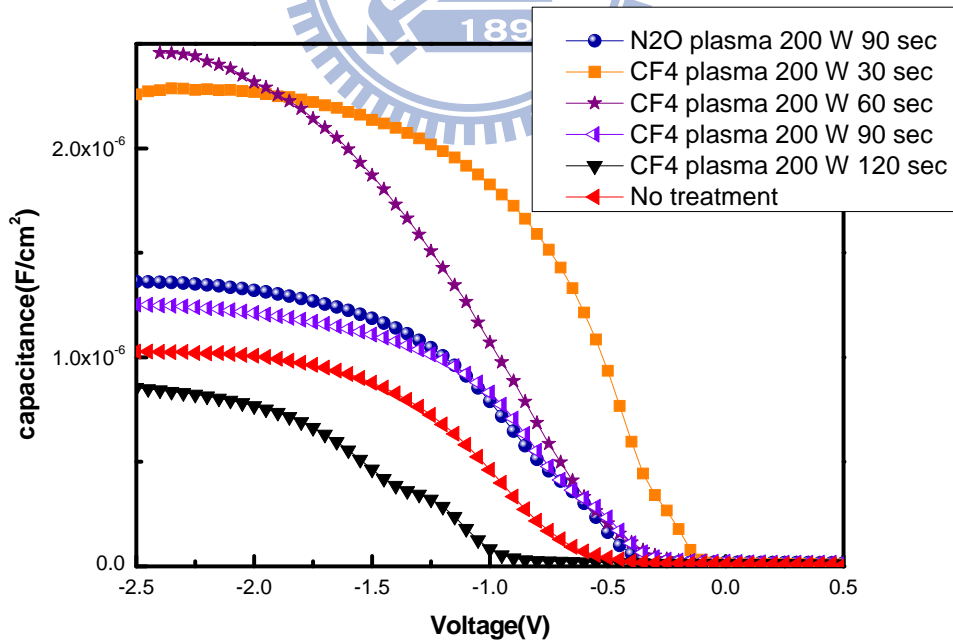


Fig.3-6 The capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with N₂O plasma 90sec and CF₄ plasma treatment for different process time.

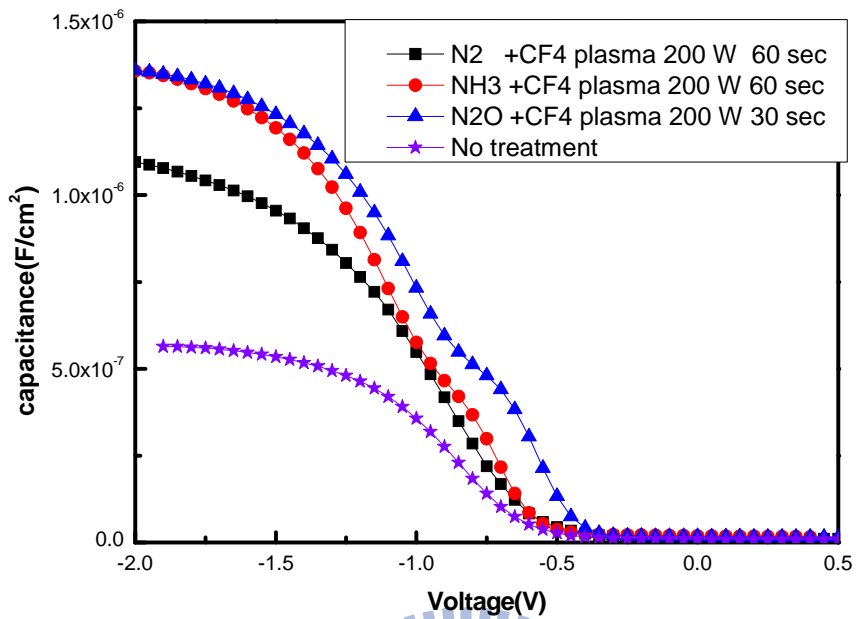


Fig.3-7 The capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N₂,NH₃,N₂O plasma treatment and CF₄ plasma at optimal condition.

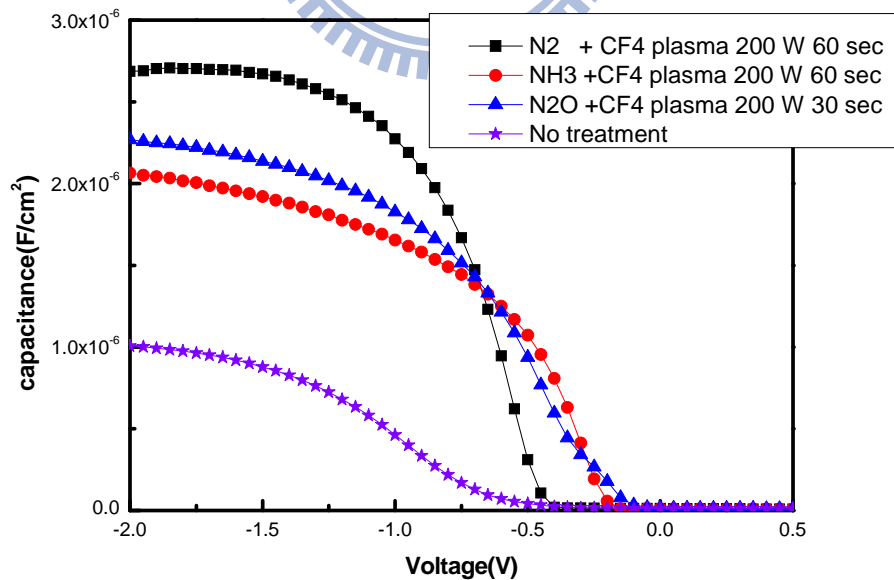


Fig.3-8 The capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with N₂,NH₃,N₂O plasma treatment and CF₄ plasma at optimal condition.

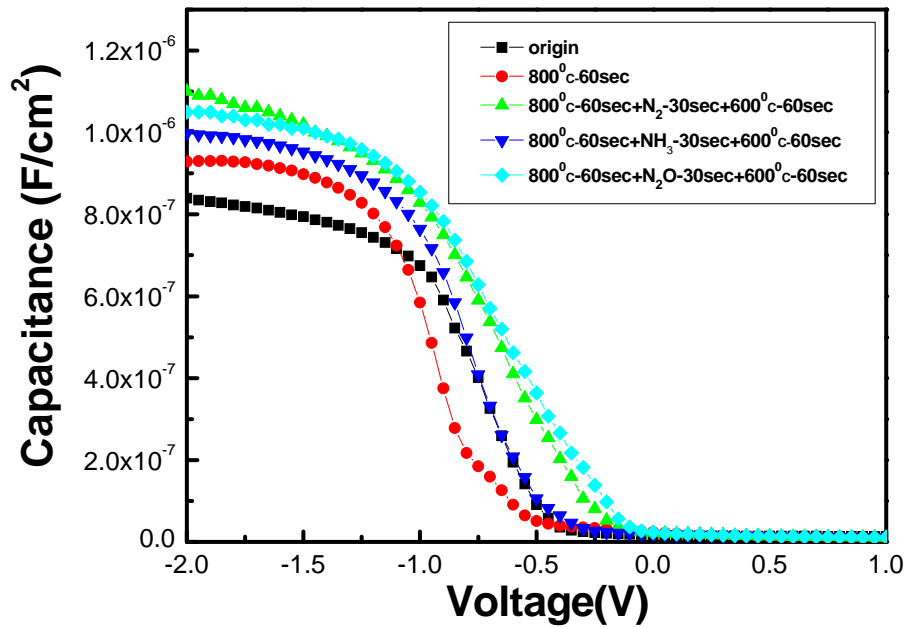


Fig.3-9 The capacitance-voltage (C-V) characteristics of HfAlO gate dielectrics treated with N₂ plasma treatment, NH₃ plasma treatment and N₂O plasma treatment all for 30 sec.

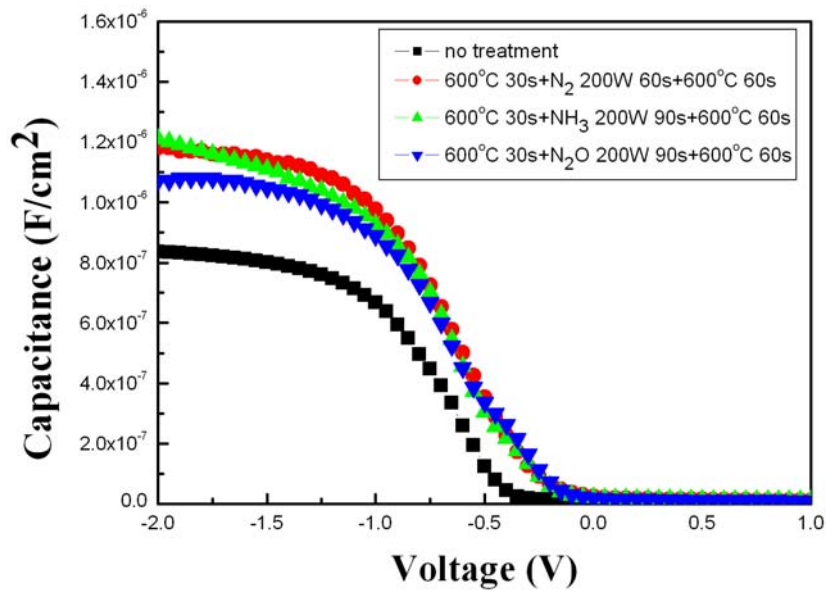


Fig.3-10 The capacitance-voltage (C-V) characteristics of HfO₂ gate dielectrics treated with N₂ plasma treatment, NH₃ plasma treatment and N₂O plasma treatment.

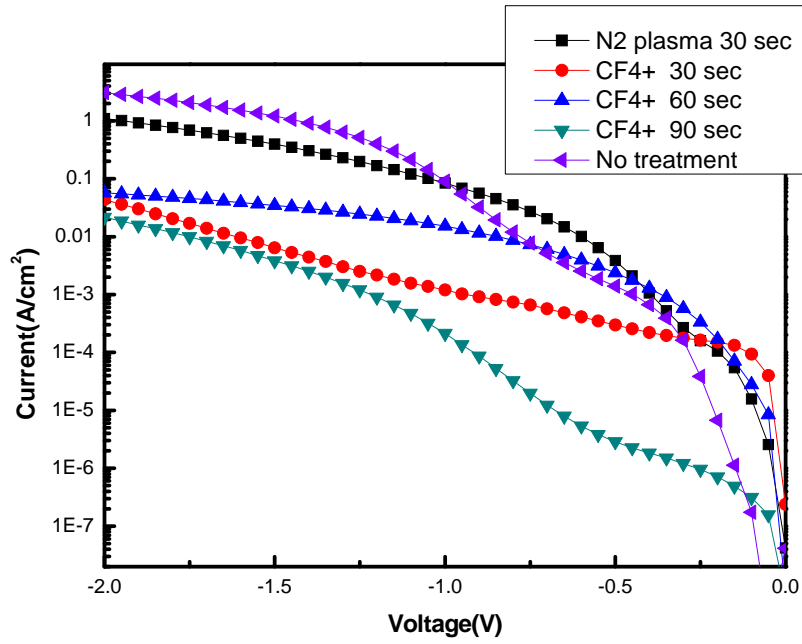


Fig.3-11 The J-V characteristics of p-type HfAlO capacitors treated with N₂ plasma 30 sec and CF₄ treatment for different process time from 0 V to -2 V.

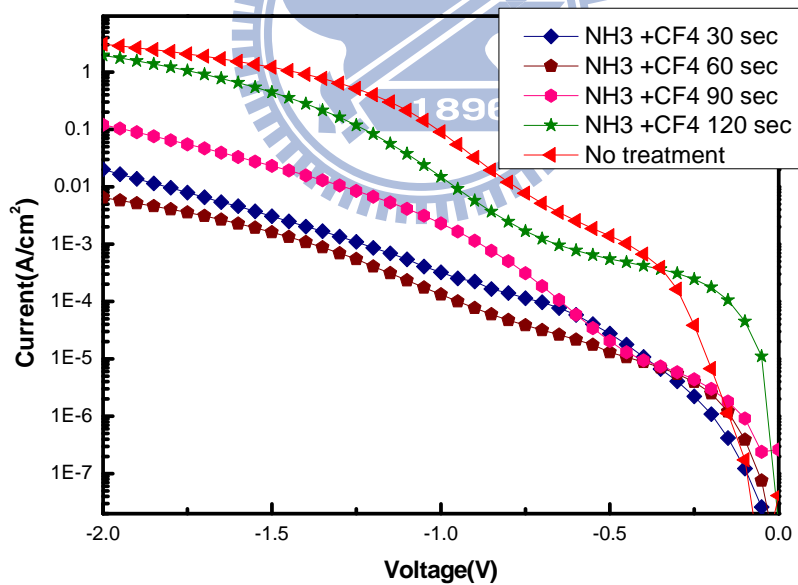


Fig.3-12 The J-V characteristics of p-type HfAlO capacitors treated by NH₃ plasma 30sec and CF₄ plasma treatment for different process time from 0 V to -2 V.

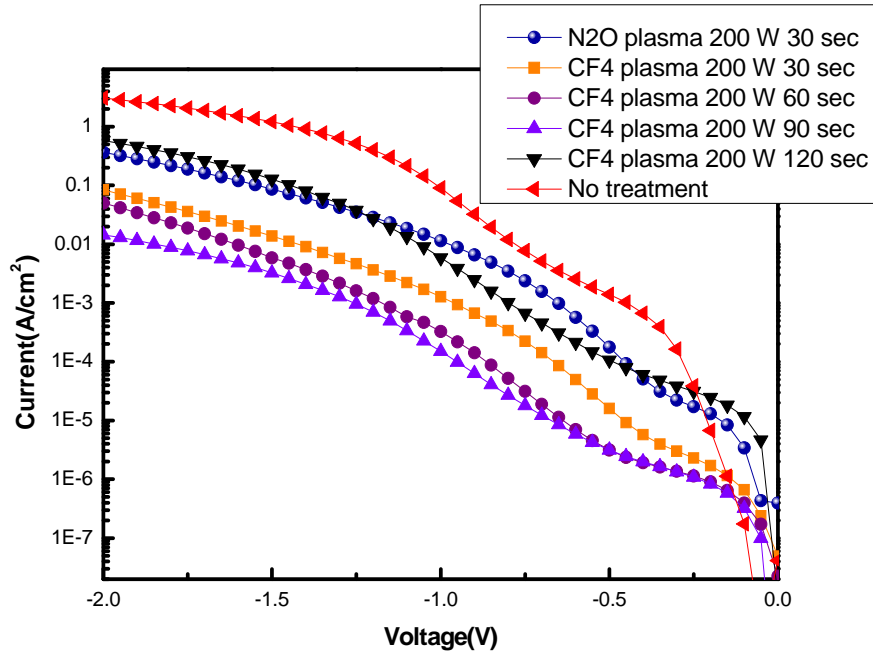


Fig.3-13 The J-V characteristics of p-type HfAlO capacitors treated by N₂O plasma 30sec and CF₄ plasma with different process time from 0 V to -2 V.

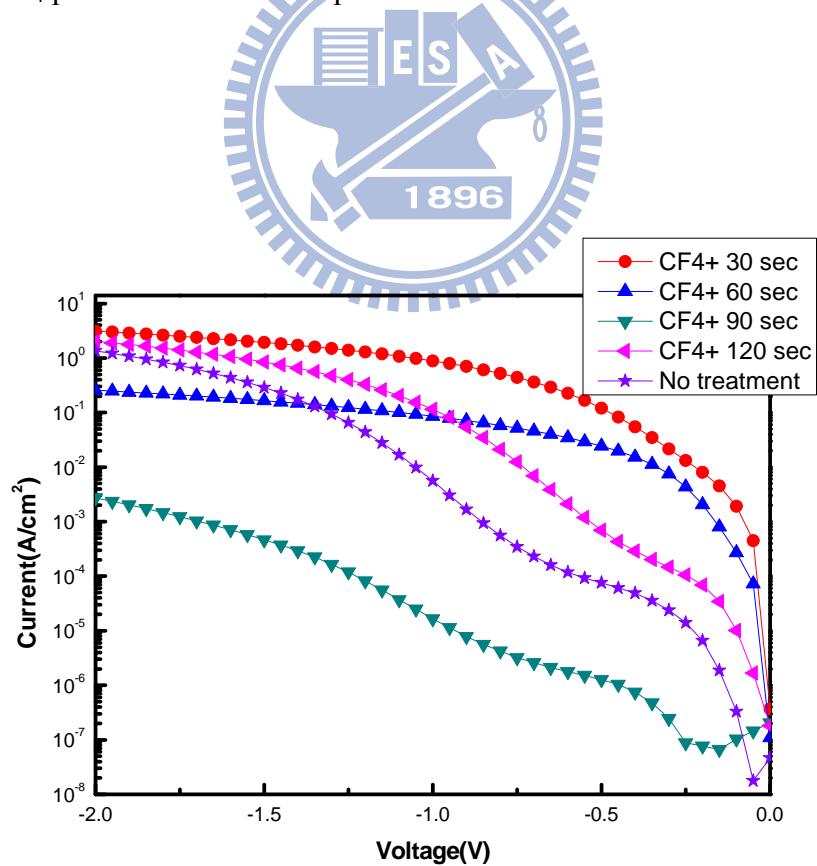


Fig.3-14 The J-V characteristics of p-type HfO₂ capacitors treated with N₂ plasma 60 sec and CF₄ plasma treatment for different process time from 0 V to -2 V.

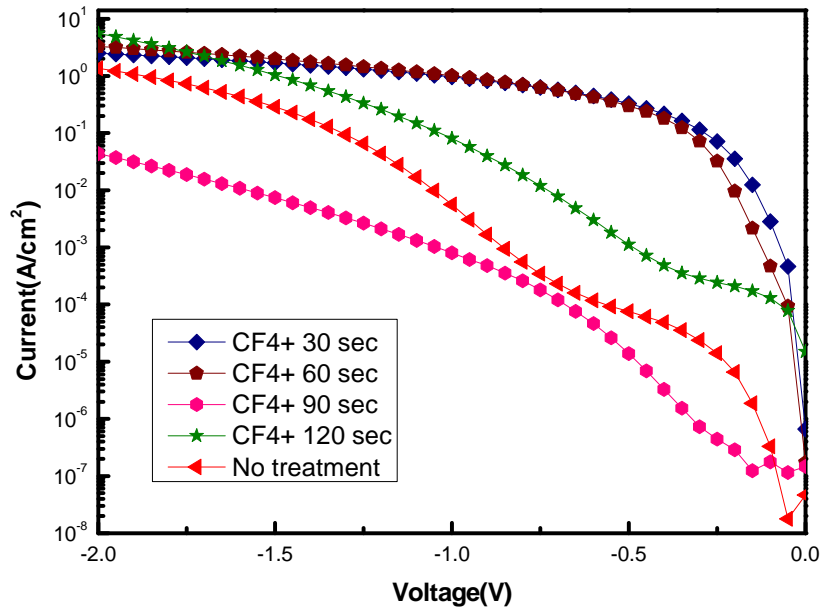


Fig.3-15 The J-V characteristics of p-type HfO₂ capacitors treated with NH₃ plasma 90 sec and CF₄ plasma treatment for different process time from 0 V to -2 V.

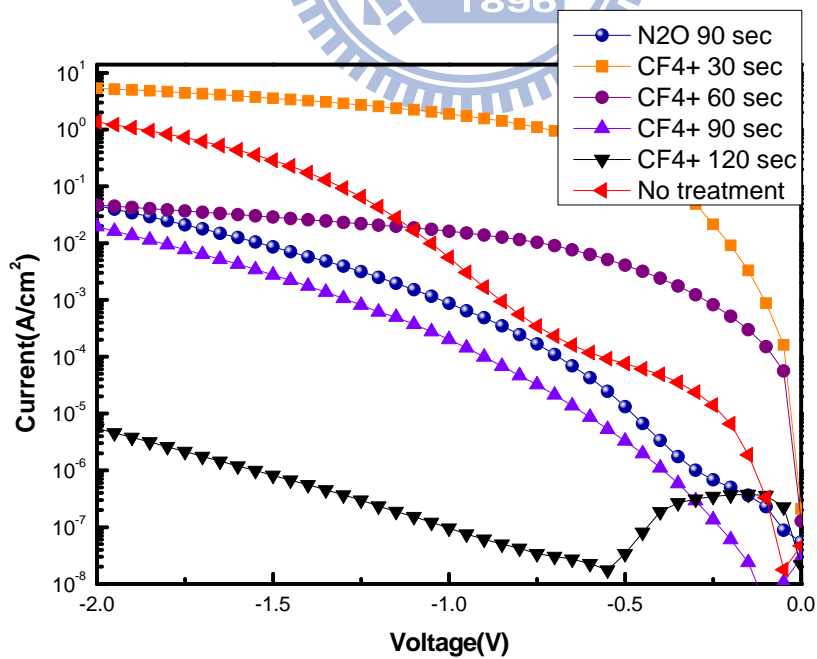


Fig.3-16 The J-V characteristics of p-type HfO₂ capacitors treated with N₂O plasma 90 sec and CF₄ plasma treatment for different process time from 0 V to -2 V.

Figure-chapter 4

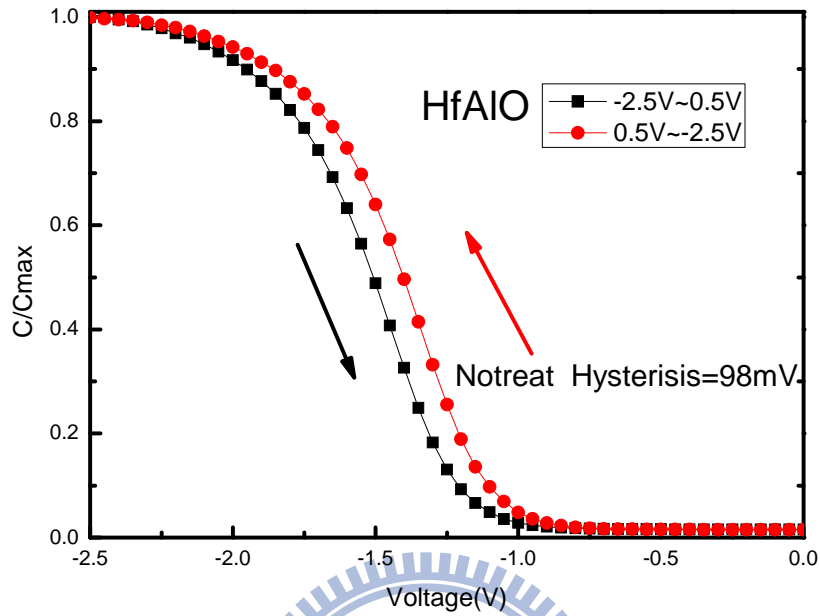


Fig. 4-1 The hysteresis of p-type HfAlO gate dielectrics treated without PDA, plasma treatment, PNA.

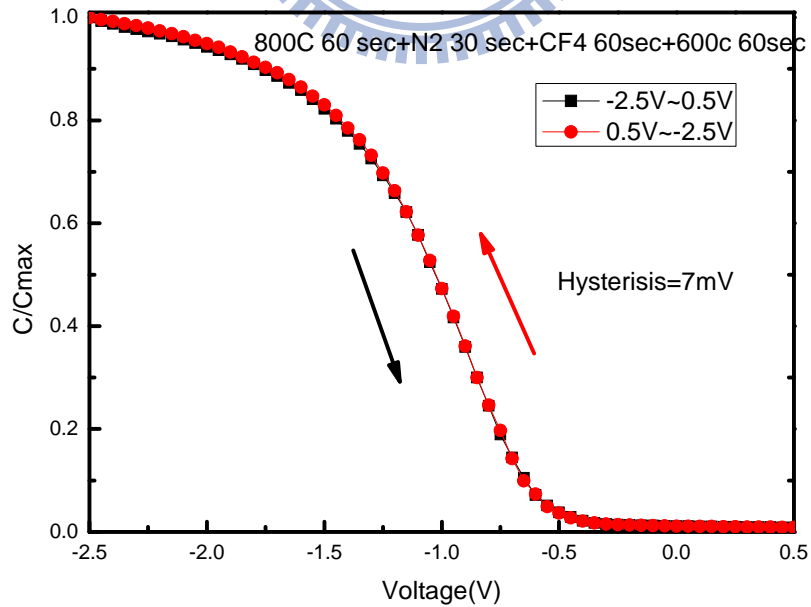


Fig. 4-2 The hysteresis of p-type HfAlO gate dielectrics treated with PDA, N₂ and CF₄ plasma treatment, PNA.

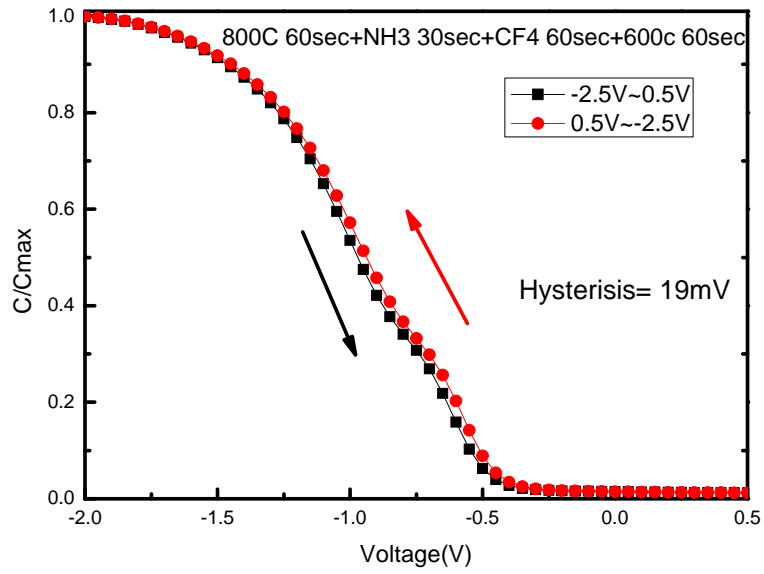


Fig. 4-3 The hysteresis of p-type HfAlO gate dielectrics treated with PDA, NH₃ and CF₄ plasma treatment, PNA.

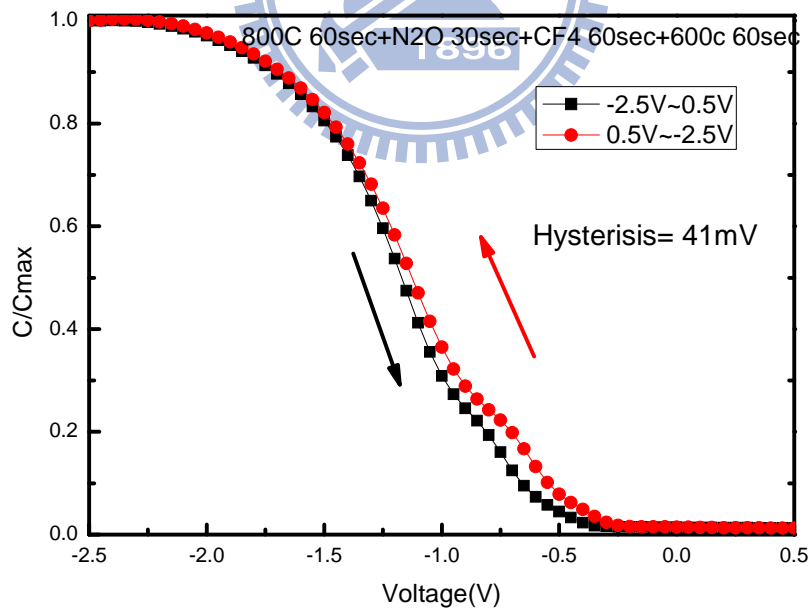


Fig. 4-4 The hysteresis of p-type HfAlO gate dielectrics treated with PDA, N₂O and CF₄ plasma treatment, PNA.

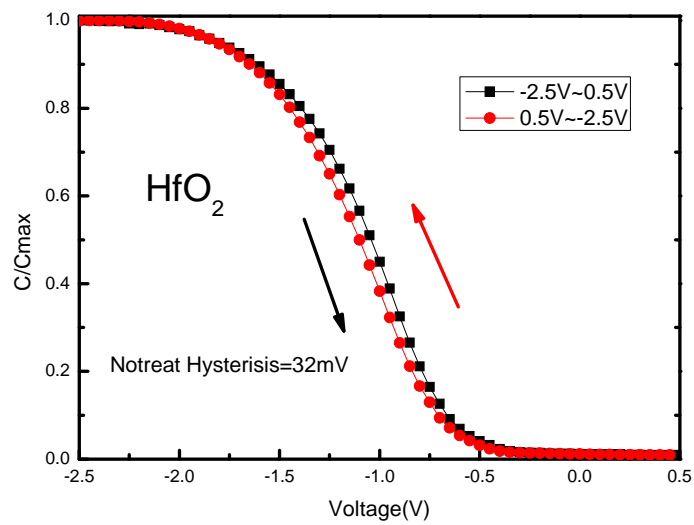


Fig. 4-5 The hysteresis of p-type HfO₂ gate dielectrics without plasma treatment.

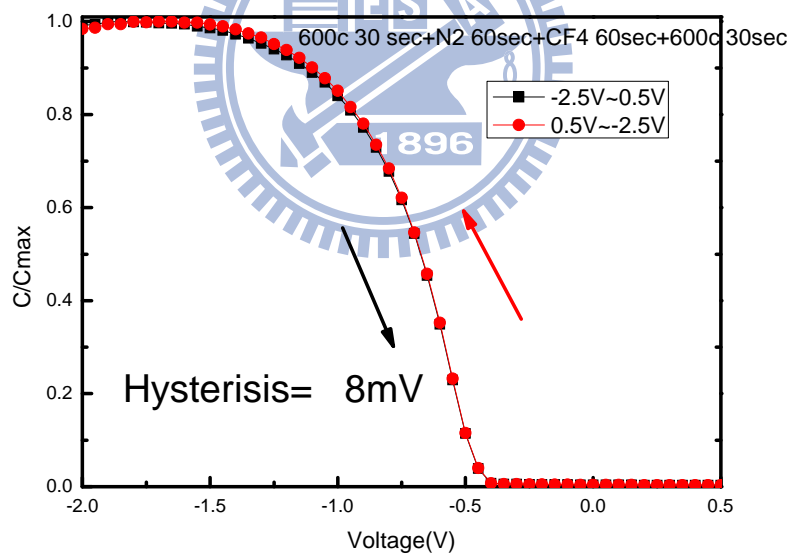


Fig. 4-6 The hysteresis of p-type HfO₂ gate dielectrics (MOCVD) with PDA
600°C-30 sec, N₂ and CF₄, PNA 600°C-30 sec.

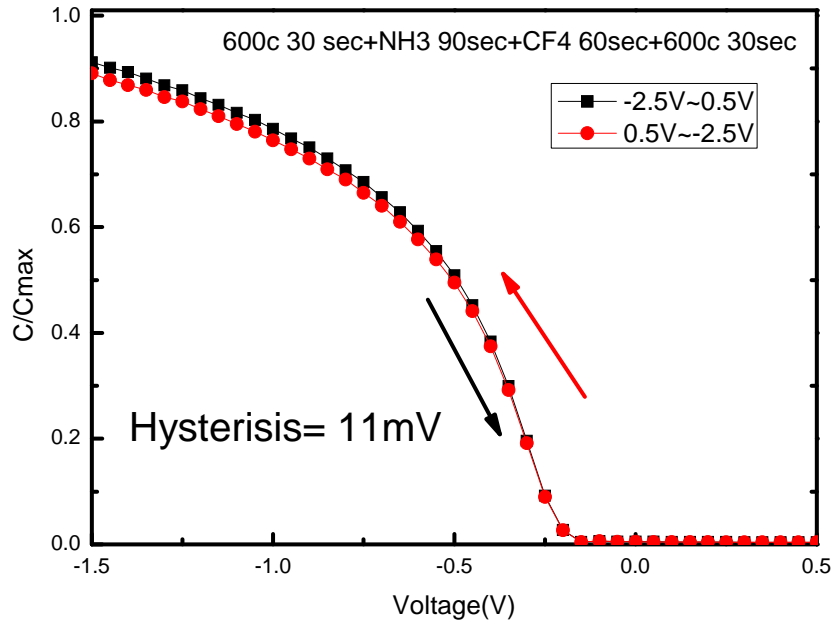


Fig. 4-7 The hysteresis of p-type HfO₂ gate dielectrics (MOCVD) with PDA
 600°C-30 sec, NH₃ and CF₄, PNA 600°C-30 sec.

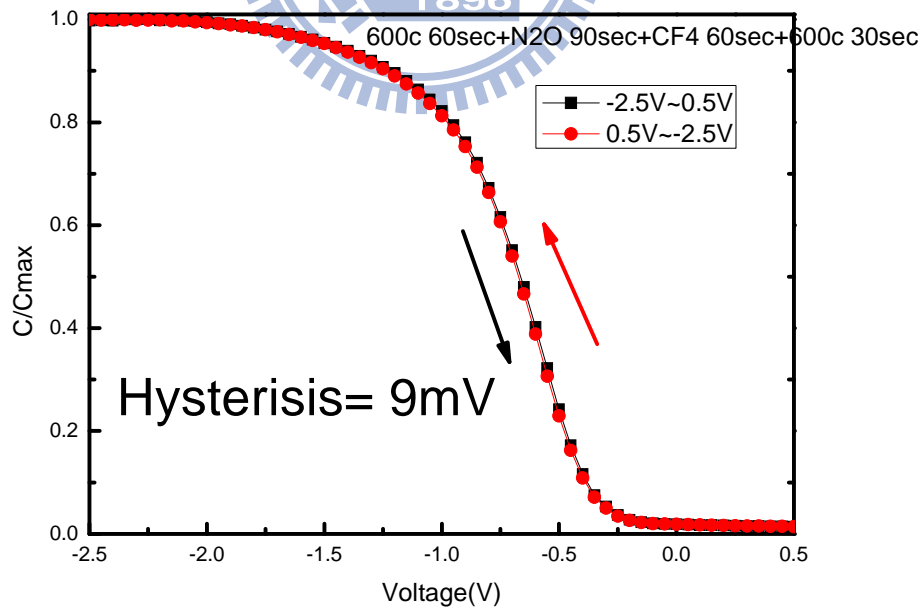


Fig. 4-8 The hysteresis of p-type HfO₂ gate dielectrics (MOCVD) with PDA
 600°C-30 sec, N₂O and CF₄, PNA 600°C-30 sec.

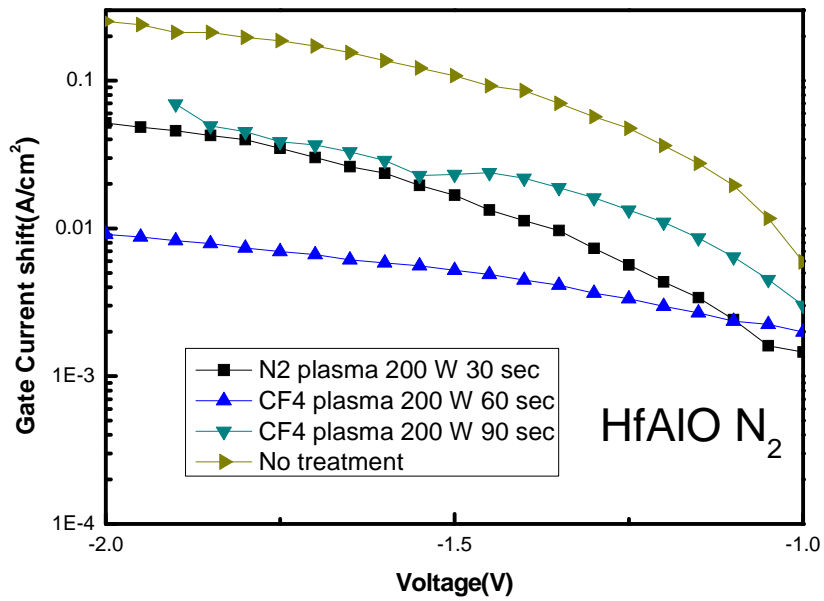


Fig. 4-9 The SILC curve of p-type HfAlO gate dielectrics treated with N₂ plasma plus CF₄ treatment for different process time.

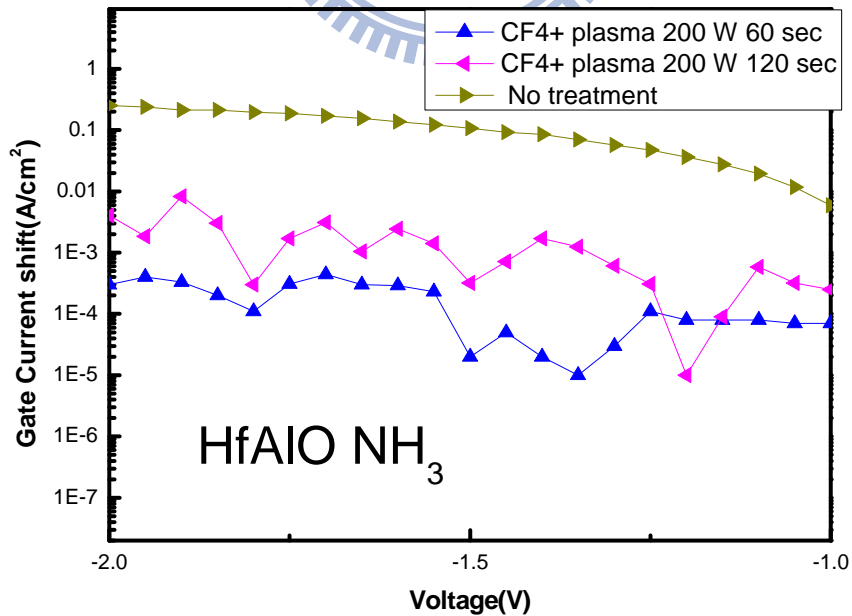


Fig. 4-10 The SILC curve of p-type HfAlO gate dielectrics treated with NH₃ plasma plus CF₄ treatment for different process time.

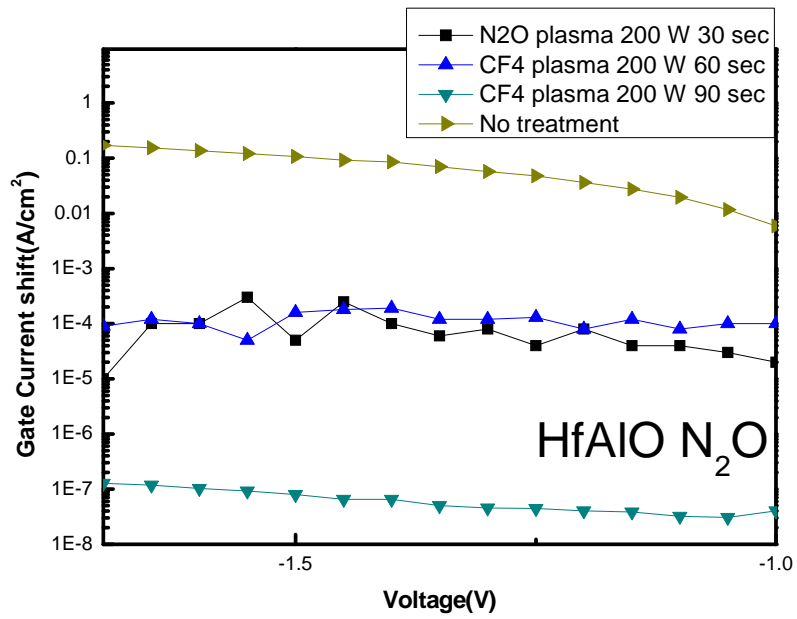


Fig. 4-11 The SILC curve of p-type HfAlO gate dielectrics treated with N₂O plasma plus CF₄ treatment for different process time.

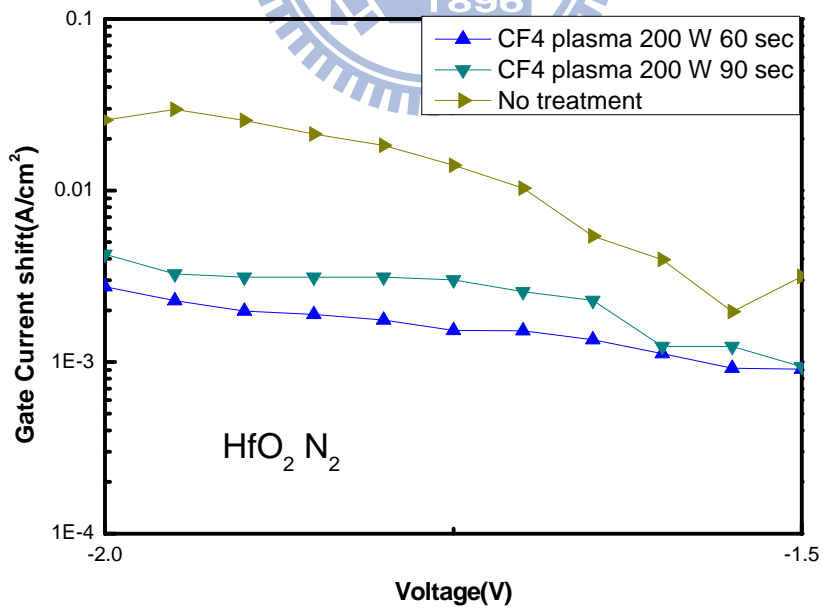


Fig. 4-12 The SILC curve of p-type HfO₂ gate dielectrics treated with N₂ plasma plus CF₄ treatment for different process time.

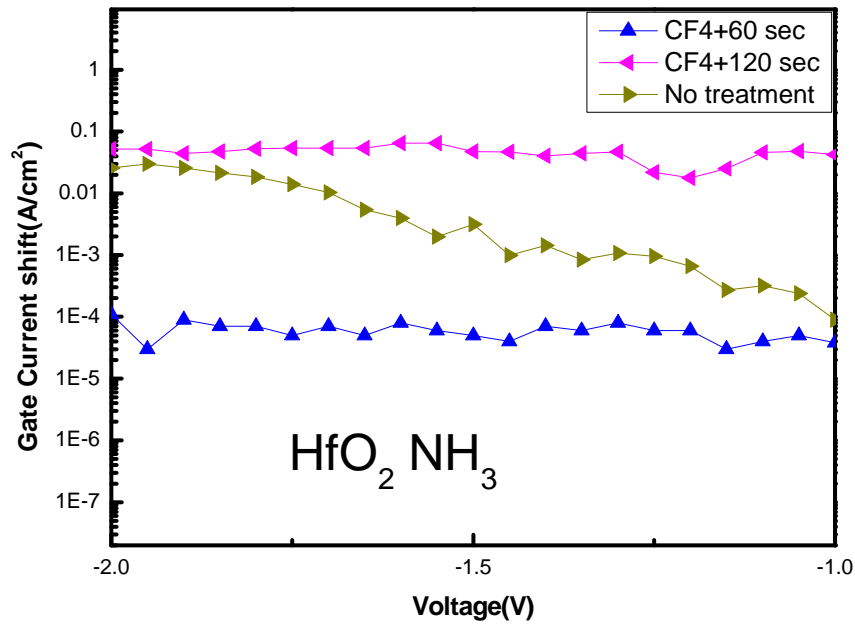


Fig. 4-13 The SILC curve of p-type HfO_2 gate dielectrics treated with NH_3 plasma plus CF_4 treatment for different process time.

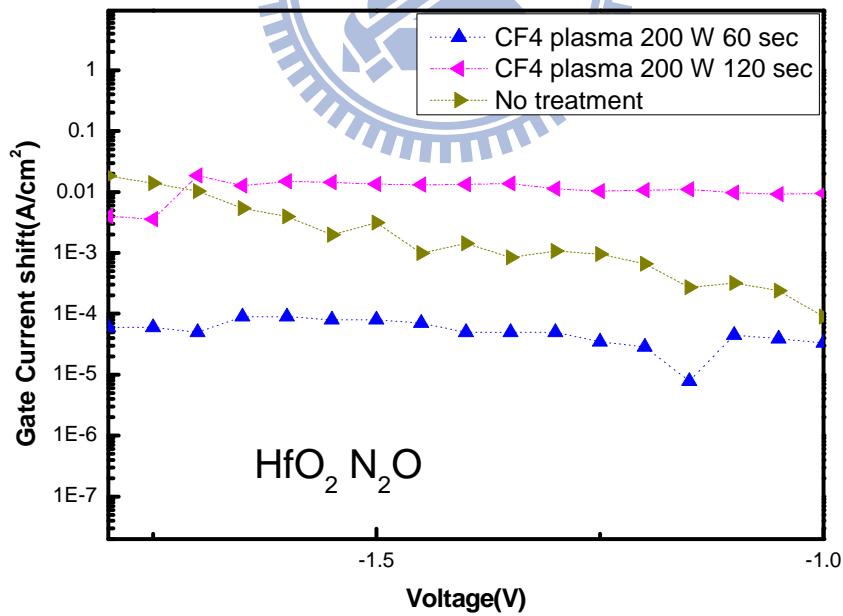


Fig. 4-14 The SILC curve of p-type HfO_2 gate dielectrics treated with N_2O plasma plus CF_4 treatment for different process time.

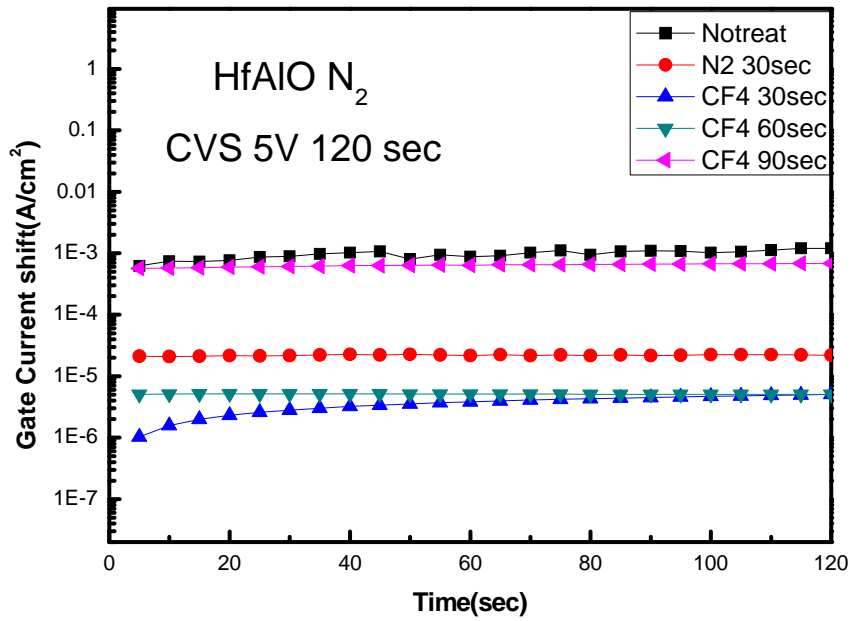


Fig. 4-15 The gate current shift of p-type HfAlO gate dielectrics treated with N₂ plasma plus CF₄ plasma treatment for different process time as a function of stress time during V_g = 5 V CVS stress.

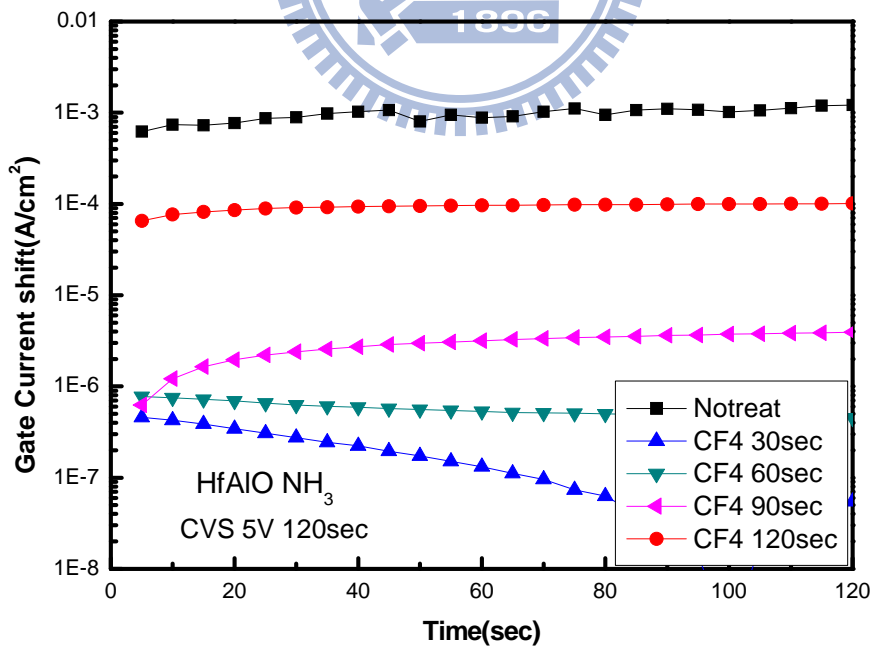


Fig. 4-16 The gate current shift of p-type HfAlO gate dielectrics treated with NH₃ plasma plus CF₄ plasma treatment for different process time as a function of stress time during V_g = 5 V CVS stress.

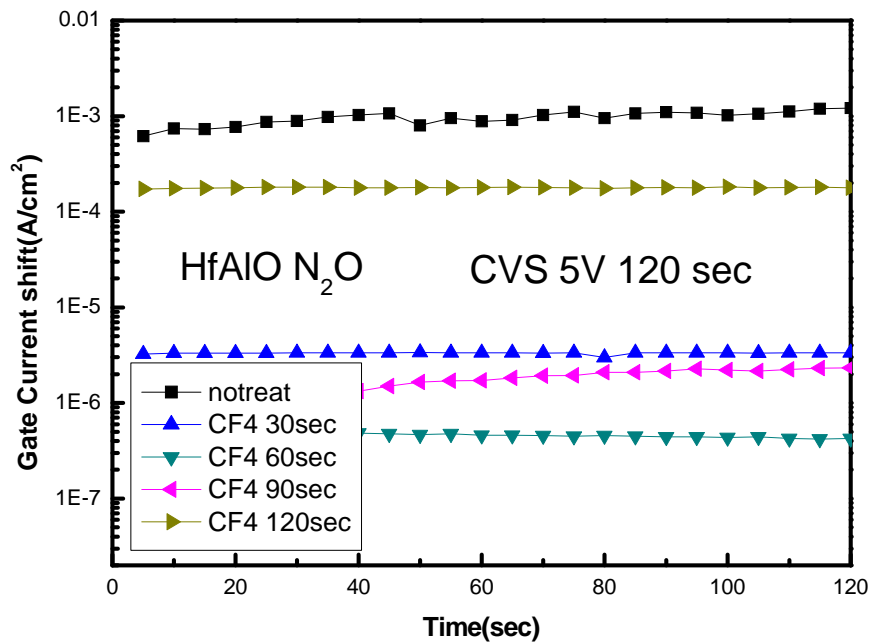


Fig. 4-17 The gate current shift of p-type HfAlO gate dielectrics treated with N₂O plasma plus CF₄ plasma treatment for different process time as a function of stress time during V_g = 5 V CVS stress.

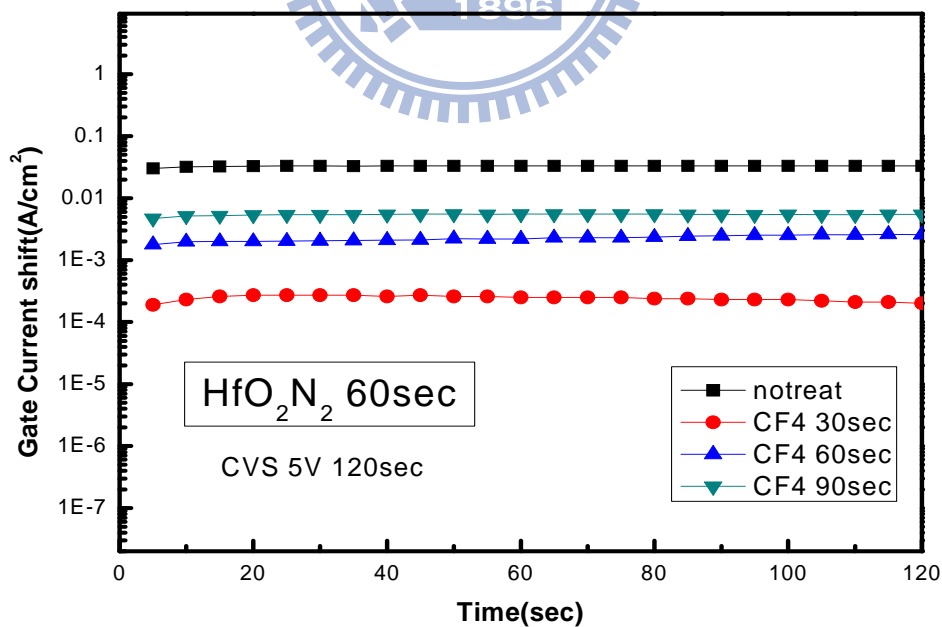


Fig. 4-18 Gate current shift of p-type HfO₂ gate dielectrics treated with N₂ plasma plus CF₄ treatment for different process time during V_g = 5V CVS for 120sec.

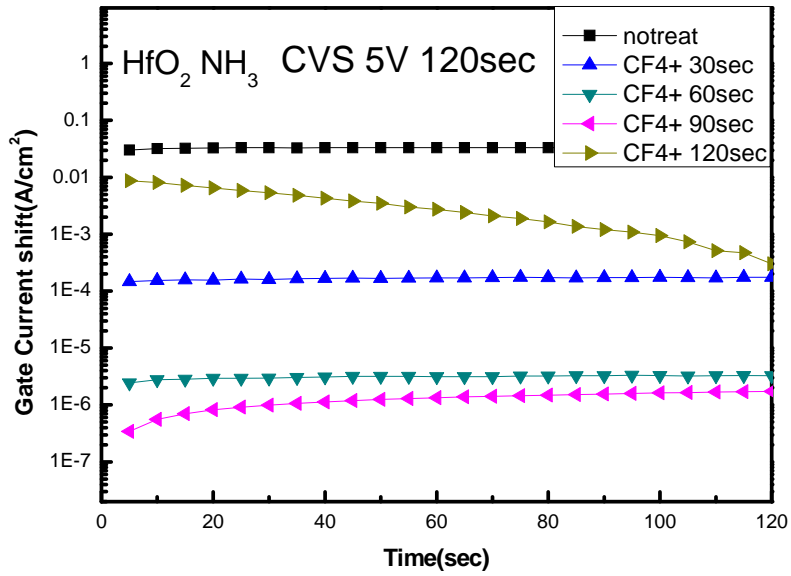


Fig. 4-19 Gate current shift of p-type HfO₂ gate dielectrics treated with NH₃ plasma plus CF₄ plasma treatment for different process time during V_g = 5V CVS for 120sec.

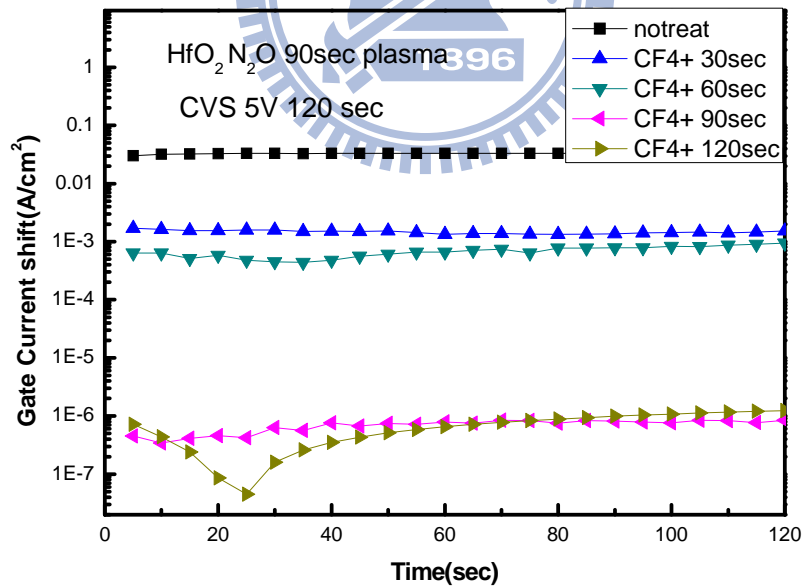


Fig. 4-20 Gate current shift of p-type HfO₂ gate dielectrics treated with N₂O plasma plus CF₄ plasma treatment for different process time during V_g = 3V CVS for 180sec.

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