國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

電感耦合式電漿氮化和氟化處理對鉿矽化合物薄膜之影響

The Effects of Nitridation and Fluorination Treatment by Inductive Coupled Plasma to Hafnium Silicate Thin Films

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摘要

隨著金氧半場效電晶體的微縮，傳統使用二氧化矽當作閘極介電層將面臨到物理和電性的限制。當電晶體的閘極通道長度微縮到 100 奈米以下時，閘極介電層厚度將縮小至 1.2 奈米以下，以二氧化矽當作氧化層將會面臨到很多的挑戰，影響最嚴重的就是太薄的二氧化矽絕緣層會使大量載子直接穿隧造成大量的漏電流，為了有效抑制此漏電流，需要使用高介電係數材料來取代二氧化矽作為閘極氧化層，高介電係數氧化層可以在維持相同的等效氧化層厚度(維持相同的電容值)的情況下，增加實際介電層厚度來抑制穿遂電流的形成。其中鉿類氧化物為主的材料被認為是目前最有可能來取代二氧化矽。本實驗以鋁-鈦-氧化矽鉿-矽之 MIS 結構為分析元件。首先，我們利用化學氣相沉積方法在矽晶片上沉積氧化矽鉿，然後進行 $500^{O}C$~$800^{O}C$ 不同溫度的沉積後退火步驟，找出最適當的退火溫度。接著再分別進行在氮氣、氨氣、氧化氮和四氟化碳等氣體環境下的表面電漿處理，然後再進行 $600^{O}C$30 秒的電漿後高溫快速熱退火，最後再沉積鈦

和鋁當電極進行量測。我們利用量測電容-電壓曲線和漏電流-電壓曲線去探討氧化層薄膜的基本特性。另外藉由磁滯效應、CVS(constant voltage stress)測試來討論經過電漿處理和沒有經過電漿處理元件的可靠度分析。我們可以發現經過電漿處理的晶片可以承受較高的溫度卻不會降低原本的電容值。這是因為電漿源中的氮原子可以抑制介電層和矽之間的氧化層成長,氟原子可以修補介面處的缺陷降低漏電流,而且電漿處理過後,電容較容易累積電荷,電容值會較高。

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ABSTRACT

The aggressive scaling of MOS devices is quickly reaching the fundamental and electric limits of convention SiO_2 as the gate insulator. When the gate length scales down below 100 nm, the gate thickness will scale down below 1.2nm, the SiO_2 gate dielectric will face severe challenges, the most critical influence is that too thin SiO_2 gate dielectric will let a lot of carriers direct tunnel to form large leakage current. Therefore, high dielectric constant gate oxide with large physical thickness while identical equivalent oxide thickness (equivalent capacity value) have been used to replace SiO_2 in order to reduce gate leakage current. Hf-based dielectric is a most suitable material for future MOSFET gate oxide applications. In this study, we analysis the Al-Ti-$HfSiO_x$-Si MOS structure. First, we deposited $HfSiO_x$ on Si wafers individually by chemistic-vapor-deposition (CVD) system. Then, the films received 500^oC~800^oC different post-deposition-annealing temperature. Find the most appropriate annealing temperature. After PDA, we had additional plasma treatment in different conditions like N_2, NH_3, N_2O and CF_4. And then received post-nitridation annealing 600^{o}C 30seconds(PNA). Final, we deposited Ti and Al as electrode to see its electrical characteristic. The electrical characteristics of the film were discussed by C-V and I-V curves. The reliability of the film with nitridation or not were discussed by hysteresis effect, CVS(Constant Voltage Stress) test. We could find that that the film with nitridation could sustain high thermal stress, and its capacitance did not decrease. It might be that nitrogen could suppress the formation of interfacial layer between the high-k/Si interface, the fluorine also can repair defects at interface to decrease the leakage current. And the films after nitridation will more easier accumulate charges, the capacity values will be more higher.

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Contents

Chapter 1 Introduction

Chapter 2 Experiments of Al/HfO_2 and $HfAlO_x$ /Si MIS capacitor

Chapter 3 Electrical characteristics of Al-Ti-$HfSiO_x$-Si MIS capacitors

Chapter 4 Reliability of Al-Ti-$HfAlO_x$-Si MIS capacitors

Chapter 5 Conclusions and future work

Table Captions

Chapter 1

Figure Captions

Figure-chapter 1

Figure-chapter 2

Figure-chapter 3

Figure-chapter 4

Chapter 1

Introduction

1.1 Background

According to the recent prediction which was made by the Semiconductor Industry Association (SIA) in International Technology Roadmap for Semiconductors (ITRS) [1]-[3], the IC technology will continue its historical rate of advancement with Moore's law for at least a couple of decades. "Moore's Law", proposed by Gordon Moore in 1965, which states that " The number of transistors and resistors on a chip doubles every 18 months ", so it is needed to pursue better performance with lower cost. In order to achieve the goal, the scaling down of the device dimension is an inevitable tendency. The IC industry has been rapidly and consistently scaling down the design rule, increasing the chip and wafer size, and cleverly improving the design of devices and circuits for over 35 years [1]-[3].

In the scaling of CMOS, reducing the thickness of gate stack with lower leakage current plays an important role. Although the leakage current of the devices with the same gate dielectric reduces with the scaling gate length and width, that leakage current density increases with the scaling of gate dielectrics exponentially, the thickness of gate oxide have to be below 10 Å after 2007. Therefore, the gate leakage current increases as the device size decreases. The larger leakage current will not only cause the higher power consumption but also degrade the reliability of the devices. [4]-[5]

In terms of the first order current-voltage relation, the driving current of a MOSFET can be given as

$$I_{dsat} = \frac{1}{2} C_g \mu_n \frac{W}{L_{eff}} (V_{GS} - V_t)^2 \tag{1.1}$$

$$C_g = \kappa \varepsilon_0 \frac{A}{t_{inv}} \tag{1.2}$$

Where V_{GS} is the applied gate to source, L_{eff} is the effective channel length, W is the channel width, V_t is the threshold voltage, μn is the mobility for electrons, Cg is the gate capacitance, κ is the dielectric constant, ε_0 is the permittivity of free space and t_{inv} is the electrical film thickness. From the formula, we know that with reduced threshold voltage, smaller effective channel length, and increased gate capacitance as well as gate-to-source voltage, the device can achieve better current driving ability. Of course, it can also have higher device density, which means a better performance and much more transistors on the chip. However, a large V_{GS} will degrade the reliability while too small V_t will result in statistical fluctuation in thermal energy at a typical operation circumstance of up to 100℃. So a bigger Cg and shorter L_{eff} will be needed to maintain device performance.

Using the material with high dielectric constant (high-k), the physical thickness of the dielectric in the devices can be increased without the reduction of capacitance density. Since the leakage current is related to the physical thickness, the increasing thickness of high-k dielectric can reduce the leakage current of the devices. Although high k dielectrics often exhibits smaller band gap, weaker bond, and higher defect density than SiO_2, the high k dielectrics with the same effective oxide thickness (EOT) with SiO_2 still shows lower leakage current than SiO_2 by several orders. [6]-[7]

That is the reason why high-k dielectrics have drawn much attention for future gate dielectrics. Recently, some high-k dielectrics have been widely studied and the characteristics and issues of those materials have also been reported. The high-k dielectrics show good performances are always accompanied by another drawbacks. Finding out the most suitable high-k dielectric for the use of device and altering the device structure or process to meet the requirement of the high-speed device are significant tasks to implant high-k dielectrics to the next VLSI generation.

1.2 Scaling down of oxide thickness

According to the SIA (Semiconductor Industry Association) roadmap, CMOS with gate length below 70 nm will need an oxide thickness of less than 1.5 nm, which corresponds to two or three layers of silicon dioxide atoms. Reducing the thickness of silicon dioxide to these dimensions would result in an exponential increase of direct tunneling current [8]. The resulting gate leakage current will increase the power dissipation and decrease the device performance and circuit stability for VLSI circuits. The Fig.1-1 shows the possible conduction mechanism of the leakage current passing through the oxide , it could see there are several kinds of conduction mechanisms of the leakage current passing through the oxide layer, which contain hot carrier injection、Fowler-Nordheim tunneling and direct tunneling. When the oxide thickness is less than 2 nm, the dominant leakage mechanism is direct tunneling. This results that the leakage current increase rapidly with the decrease of the oxide thickness. We can see the machine from (1.3)

$$I_{DT} \propto \exp-\left(\sqrt{\frac{2mq\phi}{\left(\frac{h}{2\pi}\right)^{2}}}\,T_{phys}\right) \qquad \textbf{(1.3)}$$

From Fig.1-2, when the equivalent oxide thickness (EOT) is 2 nm, the leakage current density of SiO_2 is 10^{-2} A/cm^2, which is lower than logic limit but higher than wireless limit. We could use SiON to replace SiO_2 and reduce the leakage current density about one order to make it lower than wireless limit. However, when the EOT is less than 2 nm, SiON also couldn't be used for wireless application. In addition, the leakage of SiO_2 even is larger than logic limit when the EOT is down to 1.5 nm. SiON also couldn't be used for logic application when the EOT is less than 1.3 nm. Therefore, we must use high-k materials instead of SiO_2 to be the gate dielectric. High-k dielectrics could effectively reduce the leakage current density about 4 orders. We also can see the gate leakage current of scaling down of SiO_2 from Fig.1-3.

Table 1-1 is the roadmap of 2006 (update) ITRS (International Technology Roadmap for Semiconductor) for the high performance logic technology. According to the projection of the International Technology Roadmap for Semiconductors, an equivalent oxide thickness of less than 1.0 nm is required for sub-65-nm metal–oxide–semiconductor field-effect transistor (MOSFET) devices [9]. Due to a high tunneling leakage current, the scaling of SiO_2 below 1.0 nm with an acceptable leakage current level is very difficult. Recently, high-dielectric constant (high-k) oxide thin films have attracted great interest as a replacement for nitrided SiO_2 gate oxide films [10]-[14].

(1.2) can be rewritten as follows:

$$t_{high-k} = \frac{k_{high-k}}{k_{ox}} t_{eq} = \frac{k_{high-k}}{3.9} t_{eq} \quad \textbf{(1.4)}$$

From (1.4) we can see that if we increase the gate dielectric thickness and as usual retain the same Cg value, the leakage current problem could be solved.

1.3 High-k materials

1.3.1 The advantages of high-k dielectric

High-k gate materials can maintain the same EOT with thicker physical thickness, and is therefore expected drastically reduced direct-tunneling current. From Fig1-4, the increased physical thickness significant reduces the probability of tunneling across the insulator, and hence, reduces the amount of off-state leakage current density. [15]

The relationship between dielectrics constant and thickness is followed:

$$EOT = \frac{k_{ox} \times t_{high-k}}{k_{high-k}} \qquad \textbf{(1.5)}$$

A suitable replacement gate dielectric with a high permittivity (k) must exhibit low leakage current, have the ability to be integrated into a CMOS process flow, and exhibit at least the same equivalent capacitance, performance, and reliability of SiO_2.

1.3.2 Challenges of high-k material

Although high-k material is expected to replace SiO_2 ideally, there are many problems to use high-k material practically. The issues for choosing a high-k material may include：

(1) Low dielectric constant interfacial layer between substrate and high-k material

(2) Degradation of carrier mobility

(3) Shift of threshold voltage

(4) Thermal stability

(5) Boron penetration prevention

(6) Poly interface and poly gate electrode

(7) Compatibility with traditional CMOS process.

1.3.3 The choice of high-k materials

It is important to discuss the general requirements and challenges associated with different High-k materials as possible gate dielectrics. Issues to be discussed include processing, dielectric constant, capacitance, bandgap, tunnel current, and reliability. In the past three decades, SiO_2 has served as an ideal gate dielectric, its several advantages, such as being amorphous phase through the whole integration processing, high quality interface and good thermal stability, can indeed serve as a good guide of choosing high-k material. So, an ideal gate dielectric should meet the following requirements below:

Physical properties :

a. Suitable high k value (12~60)

A suitable k value is indispensable. Those with not enough high k value could not satisfy (1.3) to lower the leakage by increasing physical thickness. While those with too high k value, in general, would suffer from thermal stability issues and larger fringing field.

b. Wide bandgap with conduction band offset > 1eV

It is found that most of the high-k materials do not have wide enough bandgap. In contact with silicon and gate electrode, the bandgap is closely related to the barrier height for carrier transport. Low bandgap will lead to intolerably high gate leakage (leakage current ~exp(-Δ Ec)).

c. Thermodynamic stability in direct contact with silicon

Preserve capacitance of gate stack after processing.

d. Film morphology (amorphous) and stable process compatibility

In the VLSI process, the thermal budget is an important issue since high temperature changes dielectric phase. Once the gate dielectric material has transformed to polycrystalline from amorphous phase, the large grain boundaries would serve as leakage path, and induce large leakage current.

e. Gate material compatibility

Materials such as metal gate, and metals have been considered for better controllability and better performance.

Electrical properties :

(a)Low interface state density (Dit< $5x10^{10}/cm^2$-eV^{-1}), and SiO2-like mobility, The interface would affect the carrier mobility in the channel, and from (1.2), mobility degradation is related to poor current drivability. In high-k, there are so many sources that would reduce mobility, such as fixed charge, remote phonon, interfacial dipoles, remote surface roughness, surface roughness and phase separation crystallization. And most of them can be avoided by improving process technology.

(b) T_{inv}<1nm,

(c) J<10^{-3}A/cm^2@ VDD,

(d) V_{FB} and hysteresis < 20mV,

(e) No C-V dispersion,

(f) Reliability issue.

To serve as a new gate dielectric, we must also take into consideration electrical reliabilities, such as stress-induced leakage current (SILC), time dependent dielectric breakdown (TDDB), hot carrier aging, bias temperature instability and charge trapping issues [16].

1.3.4 Why choose $HfSiO_x$-base

There are many kinds of high-k materials, including Al_2O_3, Y_2O_3, Ta_2O_5, TiO_2, ZrO_2 and HfO_2 etc. Table 1-2 lists basic characteristics of several high-k dielectrics. Unfortunately, many high-k materials such as Ta_2O_5, TiO_2, $SrTiO_3$ are thermally unstable when directly contacted with silicon [17] and need an additional barrier layer which may add process complexity and impose thickness scaling limit. Also, materials with too low or too high dielectric constant may not be adequate choice for alternative gate dielectric application. Ultra high-k materials such as STO or BST may cause fringing field induced barrier lowering effect [18]. Materials with relatively low dielectric constant such as $A1_2O_3$ and Y_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4 [19]. Among the medium-k materials compatible with silicon, oxides of Zr and Hf are attracting much attention recently. Especially, Hf forms the most stable oxide with the highest heat of formation ($\Delta Hf = 271$ Kcal/mol) among the elements in IVA group of the periodic table (i.e. Ti, Zr, Hf). Unlike other silicides, the silicide of Hf can be easily oxidized [20]. $HfSiO_x$ possesses a dielectric constant of up to 25 [21], a large bandgap of 5.7 eV with sufficient band offset of larger than 1.5 eV [22], and well thermal stability in contact with silicon [23]. $HfSiO_x$ is very resistive to impurity diffusion and intermixing at the interface because of its high density (9.68 g/cm^3) [24]. In addition, $HfSiO_x$ is the first high-k material showing compatibility with polysilicon gate process [25]. These properties make $HfSiO_x$ to be one of the most promising candidates for alternative gate dielectric application. Although inadequate mobility of $HfSiO_x$ MOSFETs is among the biggest concerns, various techniques have been explored to enhance the mobility. Introduction of strained silicon substrate [26], for example, drastically improved the mobility by changing the band structure of the substrate rather than changing the dielectric itself. However, the characteristics and mechanism of $HfSiO_x$ are not totally understood.

1.4 Plasma nitridation

According to traditional view of improving SiO_2 device performance, we could find that nitridation is a common method to improve the interface. [27] Property with the result that there is often N_{it} or D_{it} in the interface, imperfect bonding of interface usually makes the characteristic of the device deteriorate. Such as charge will be trapped by the defects of the interface, it produce flat band voltage shift and also reduce mobility. Another shortcoming is that these dangling bonds will easily bond with oxygen atom in the following high temperature environment. The extra chemical reaction will let the interfacial oxide growth, and it will reduce the C value because of the lower dielectric constant. In addition, the quality of interfacial layer formed by oxidation is worse, and it would cause the problem of charge trapping. In order to solve these problems, nitridation treatment could let the atom of nitrogen bond with these dangling bonds and fix it while entering the interface layer, and then improve the stability and reliability of interface. Consequently, nitridation treatment is a workable solution to improve interface quality. As we note before, the question about using high-k materials to replace SiO_2 is that there are too many defects in the interface to cause reliability degradation. Therefore, when we use high-k materials, it is consider that nitridation treatment is a more suitable way to improve reliability and thermal stability of device. These kind of treatment have already used in some relevant references. [28]-[29] Among them, someone take nitridation treatment at high temperature, others take so-called plasma nitridation . According to [30], we could understand that the effect of plasma nitridation is better than thermal nitridation. The reason is that high-k materials could not sustain high thermal stress. As long as the temperature reaches certain degree, we would see the phenomenon of crystallization. The crystallization of dielectric would increase leakage current substantially, because it offers the path of leakage current. On the other hand, the meaning of plasma nitridation is to activate the source gas first. The high activation energy of radical will provide better mend which is better than nitridation at high temperature. For all these reasons, we adopt plasma nitridation in present experience.

1.5 Thesis organization

Following chapters in the thesis are primarily organized as follow：

In chapter 2, we make a description of experimental details. Atomic Layer Deposition system is used to deposit hafnium-based materials on silicon surface.

In chapter 3, we discuss the characteristics of HfO_2 or $HfAlO_x$ insulator by Metal-Insulator-Semiconductor (MIS) capacitors.

In chapter 4, we discuss the reliability of HfO_2 or $HfAlO_x$ insulator by Metal-Insulator-Semiconductor (MIS) capacitors and the effects of Post-Metallization-Annealing.

In chapter 5, we make the conclusions for this thesis and provide some suggestions for future work.

Chapter 2

Experiments of Al-Ti-$HfSiO_x$-Si MIS capacitor

2.1 Use MOCVD to prepare high-k thin film

There are several ways to prepare high-k thin films, such as chemical vapor deposition (i.e. ALCVD, MOCVD, PECVD etc.) [30]-[32] and physical vapor deposition (i.e. Sputtering, E-gun, PLD etc.) [33]-[34]. ALCVD and MOCVD are the usual ways for preparing $HfSiO_x$ films; and E-gun is the convenience way for preparing $HfSiO_x$ films. We used the MOCVD methods below.

MOCVD (metal-organic CVD) is a widely used technology for depositing a variety of thin films, including metal oxide and metal silicate films, for high-k gate dielectric applications. The basic steps in MOCVD deposition method are as follows:

1. MO precursor in company with N_2 process gas and O_2 process gas are injected into the reactor.
2. The sources are mixed inside the reactor and transferred to the deposition process chamber.
3. At the deposition process chamber, high temperature results in the decomposition of sources and other gas-phase reactions, forming the film precursors that are useful for film growth and byproducts.
4. The film precursors transport to the growth surface.
5. The film precursors absorb on the growth surface.
6. The film precursors diffuse to the growth site.

7. At the surface, film atoms incorporate into the growing film through surface reaction.
8. The byproducts of the surface reactions desorb from the surface.
9. The byproducts transport to the main gas flow region away from the deposition area toward the reaction. Then the wafer exits.

From fig. 2-1, it is apparent that 1 nm EOT can be achieved with MOCVD metal oxide films when a metal electrode is used. However, most of the devices with MOCVD $HfSiO_x$ when a poly-Si gate is used have EOT greater than 2 nm. Unlike metal electrode, using poly-Si electrode requires the high-k gate stack to go through a 1000℃/10 second S/D activation anneal step. This step not only results in chemical and structural changes in the high-K film, but also affects interfaces between the high-k film/substrate and the high-k/poly-Si electrode. All devices fabricated with MOCVD ZrO_2 and ZrSiO films using poly-Si gate electrode were too leaky to give any meaningful C-V results. In general, using poly-Si gate electrode results in around 0.7 to 1 nm higher EOT for gate stacks fabricated with $HfSiO_x$ gate dielectric films. This additional interfacial oxide thickness is too large to be acceptable. In view of this, the MOCVD is not a good tool for high-k material deposition with poly-Si gate. However, the MOCVD has very good throughput and can process a 25-wafer lot in ~2 hours (roughly 4X better than ALCVD). Thus, from a throughput perspective, the MOCVD has a distinct advantage over the ALCVD [35].

2.2 Rapid thermal annealing system

Metal RTA-AG 610 was a single-wafer lamp-heated and computer-controlled rapid thermal processing (RTP) system. Water and compressed dry air (CDA) cooling system were used to cool down the quartz chamber. High intensity visible radiation heating and cold-heating chamber walls allow fast wafer heating and cooling rate. The tungsten halogen lamps were distinguished into five groups, and the relative percentage of lamp intensity can be adjusted individually for each group to achieve uniform temperature distribution. Temperature was obtained from pyrometer and precise controlled by computer. Two gas lines were used in the system which can be switched between Ar and N_2. Before RTA process started, one minute N2 gas purge was performed to minimize the water vapor introduced during wafer loading and also swept unwanted particles induced during process. A fast heating rate of 100℃/s was chosen in this work. When anneal was complete, chamber temperature was quickly cooled down from 900℃ to 500℃ by N_2 purge 30 seconds. Then, the chamber was slowly cooled down to 280℃ without N2 purge to avoid creaking of films. After five minutes later, wafers can be taken out from the chamber. Films' creak can be avoided by two-steps-cooling method.

2.3 Plasma treatment system

When the PDA (Post-Deposition-Annealing) was finished, some samples were subjected to an additional plasma treatment in order to improve the electrical properties of gate dielectric. There were various source gas (N_2, N_2O, NH_3, CF_3) and process time (30~120 seconds) as the experiment conditions. Parallel plate high-density plasma reactor employing an ICP source was a single-wafer treated and computer-controlled system.

Fig. 2.2 illustrates ICP system that was used in this experiment. 13.56 MHz RF power was coupled to the top electrode through a matching network. After the sample load to reactor, the system was pumped down to keep the chamber clean enough. Subsequently, the source gas was become radical by the plasma system, as the chamber pressure was 100 mTorr and the substrate temperature was 300℃ so that to achieve the goal of low temperature process. The power of working plasma was kept constant at 200W and the flow rate of source gas was 100 sccm. While the process of plasma treatment was finished, these samples were brought to thermal treatment to reduce plasma damage.

2.4 E-gun

After plasma treatment and PNA, we deposited Ti and Al as electrical by E-gun. And finished all manufacturing process, we used E-gun deposited Al as back electrical too.

Figure 2-3 shows E-gun work theorem, the system is always in vacuity, and the materials which we wanted to deposited was in the boat. We melt down the materials by heating, and using the electron-beam to bombard the materials to proceed evaporation. The chamber pressure was 10^{-6} mTorr when we deposited. After the deposited Ti and Al we could proceed lithography and etching.

2.5 MIS capacitors fabrication process

In this thesis, Al-Ti-$HfSiO_x$-Si MIS capacitors were fabricated to study ultra thin $HfSiO_x$ gate dielectrics. Figure 2-4 shows the fabrication flow of this experiment. The starting wafer was four inch (100) orientated p-type wafer. It was one side polished and its resistivity was 5~10 ohm-cm.

After standard initial RCA cleaning, wafers were put into chamber and grew $HfSiO_x$ layer with atomic layer deposition system. After the thin films were prepared, some samples were annealed after deposition (post-deposition anneal) and then subjected to an additional plasma treatment at the substrate temperature of 300℃ while the pressure was 100 mTorr and the plasma power was 200W. The plasma treatment conditions were in pure N_2, N_2O, NH_3, and CF_3 for 30~120 seconds respectively and the flow rate were 100 sccm. After nitridation, we also annealed these samples to reduce the plasma damage. Finally, pure Ti and Al films were thermally evaporated on the top side of wafers. Mask defined the top electrode. Then, we used wet etching to etch undefined Al, Ti and $HfSiO_x$ films. After patterning, backside native oxide was stripped with diluted HF solution, and Al was deposited as bottom electrode. The detailed fabrication process flow was listed as follows.

1. Initial RCA cleaning.

2. Atomic layer deposition $HfSiO_x$.

3. Post-deposition anneal with 500℃ 60 seconds for $HfSiO_x$.

4. Plasma treatment with N_2，N_2O, NH_3 and CF_3 plasma for 30~90 seconds respectively.

5. Post-nitridation annealing with 600℃ 30seconds.

6. Thermally evaporate 200 Å titanium 4000 Å aluminum as the top electrode.

7. Mask: define top electrode and then wet etch undefined Al, Ti and $HfSiO_x$ films.

8. Strip backside native oxide and coat 4000 Å aluminum as bottom electrode.

After the Al/ Ti/ HfO_2 /Si MIS capacitors were prepared, we used semiconductor parameter analyzer (HP4156A) and C-V measurement (HP4284) to analysis electric characteristics (i.e. I-V, C-V, EOT, leakage current density etc.). Then we tested their reliability, including constant voltage stress (CVS), Hysteresis effect.

Chapter 3

Electrical characteristics of Al-Ti- $HfSiO_x$-Si MIS capacitors

3.1 Electrical characteristics of capacitors with different post-deposition annealing temperature

3.1.1 Capacitance-voltage characteristics for $HfSiO_x$ with different gate electrodes

In order to measure the C-V characteristics of our MIS capacitors, we used HP 4284A precision LCR meter in our experiments. We swept the gate bias from accumulation region to inversion region to obtain the curve at the frequency of 50 kHz from -2V to 1V. Then, the effects of different post deposition annealing (PDA) temperature (i.e. 500^{o}C, 600^{o}C, 800^{o}C) and different post deposition annealing times (i.e. 30seconds, 60seconds, 90seconds, 120seconds) and different plasma treatment source (i.e. N_2, N_2O, NH_3, CF_4) will be discussed.

Fig. 3-1 shows the capacitance-voltage (C-V) characteristic of $HfSiO_x$ gate dielectrics and Al gate electrode treated with different annealing temperatures for different process time. PDA could reduce the flat-band voltage and make the thin film dense. And we could see that the suitable annealing condition is 500^{o}C 60seconds.

Fig. 3-2 shows the C-V characteristic of $HfSiO_x$ gate dielectrics and A+Til gate electrode treated with different annealing temperatures for different process time. In this case, the capacitances treated with PDA 500oC 60 seconds had the best capacitance too.

3.1.2 Leakage current-voltage characteristics for $HfSiO_x$ with different gate electrodes

The leakage current of our MIS capacitors were analyzed from the current -voltage (I-V) characteristics measured by an HP4156A semiconductor parameter analyzer.

Fig. 3-3 shows the I-V characteristics of $HfSiO_x$ gate dielectrics and Al gate electrode treated with different annealing temperatures for different process time from 0V to -2V. The gate leakage current density of these samples after PDA could be decreased, because the film became dense after PDA. And the lowest condition is PDA at 500^{o}C 30 seconds.

Fig. 3-4 shows the I-V characteristics of $HfSiO_x$ gate dielectrics and Al+Ti gate electrode treated with different annealing temperatures for different process time from 0V to -2V. The gate leakage current density of these samples after PDA could be decreased, because the film became dense after PDA. And the lowest condition is PDA at 500^{o}C 30 seconds.

We compared two gate electrodes, Ti-Al gate had larger capacitance and lower leakage current than Al gate. It is maybe Ti match $HfSiO_x$ rather Al.

3.2 Electrical characteristics capacitors with different plasma treatment for different process time

There are three kinds of plasma treatment with different source gas (i.e. N_2, N_2O, NH_3 and CF_4) and they were treated for different process time (i.e. 30 seconds, 60 seconds, 90 seconds and 120 seconds). And, the relationship of difference process time in one kind of plasma treatment will be discussed.

3.2.1 Capacitance-voltage characteristics for $HfSiO_x$

Fig 3-5 shows the capacitance-voltage (C-V) characteristics of $HfSiO_x$ gate dielectrics after PDA at 500°C 60 seconds and treated with N_2 plasma treatment of 200W for different process time. The capacitor treated for 60 seconds shows the maximum capacitance among three conditions of process time. Furthermore, the capacitor treated with N_2 plasma both show the good capacitance values which are larger than the capacitor which was not treated by N_2 plasma.

Fig. 3-6 shows the capacitance-voltage (C-V) characteristics of $HfSiO_x$ gate dielectrics after PDA at 500°C 60 seconds and treated with N_2O plasma treatment of 200W for different process time. At this condition, the capacitor treated for 90 seconds shows the maximum capacitance among four conditions of process time. But for the capacitance treated with N_2O plasma for 60 seconds shows the best C-V curve.

Fig. 3-7 shows the capacitance-voltage (C-V) characteristics of $HfSiO_x$ gate dielectrics after PDA at 500°C 60 seconds and treated with NH_3 plasma treatment of 200W for different process time. Just like the samples of N_2 plasma treatment. The improvement of capacitance could be seen. At this condition, the capacitance treated with NH_3 plasma for 30 seconds shows the largest value. By the way, all the samples which use NH_3 plasma have larger capacitance than the sample without treatment. It is indicated that NH_3 plasma treatment is also a practicable method to improve the capacitance -voltage characteristics of $HfSiO_2$ gate dielectrics.

Fig 3-8 shows the capacitance-voltage (C-V) characteristics of $HfSiO_x$ gate dielectrics after PDA at 500°C 60 seconds and treated with CF_4 plasma treatment of 200W for different process time. The capacitor treated for 60 seconds and 90 seconds all shows the maximum capacitance among three conditions of process time. Furthermore, the capacitors after post plasma annealing treated show the larger capacitance values and show the better than the capacitors which have no annealing treatment after plasma.

When the N_2 plasma process time over 90 sec, the C value will become smaller, we think that it is may be caused by the growing of interfacial oxide in the plasma process time. The same phenomenon is also found on N_2O, NH_3 and CF_4 plasma.

3.2.2 Leakage current-voltage characteristics for $HfSiO_x$

Fig. 3-9 shows the I-V characteristics of p-type $HfSiO_x$ capacitors after PDA at 500°C 60 seconds and treated by N_2 plasma of 200W with different process time from 0V to -2V. We observed that the gate leakage current density is suppressed while N_2 plasam treatment. It is indicated that N_2 plasma treatment supply an effective barrier against the leakage current. The film after N_2 plasma treatment became dense and strong, so the leakage current could be effectively decreased, especially for capacitor which treated with N_2 plasma 30 seconds has the lowest leakage. Gate leakage current density of no treatment insulator at Vg = -1V is about 7×10^{-2} A/cm^2. However, gate leakage current density of the capacitor treated for 30 sec N_2 plasma at Vg = -1V is about 5×10^{-5} A/cm^2. It has less gate leakage than no treatment insulator about 2~3 order.

Fig. 3-10 shows the I-V characteristics of p-type $HfSiO_x$ capacitors after PDA at 500^oC 60 seconds and treated by N_2O plasma of 200W with different process time from 0V to -2V. After N_2O plasma treatment, we could see the reduction of leakage current in contrast of no treatment samples. However, the sample of plasma treated for 60 seconds got the smallest gate leakage current and a good C-V curve from Fig 3-6.

Fig. 3-11 shows the I-V characteristics of p-type $HfSiO_x$ capacitors after PDA at 500^oC 60 seconds and treated by NH_3 plasma of 200W with different process time from 0V to -2V. After NH_3 plasma treatment, we could see the reduction of leakage current in contrast of no treatment samples. However, the sample of plasma treated for 90 seconds got the smallest gate leakage current. Compare with the sample which no treated by plasma, the leakage current would lower about 3 order.

Fig. 3-12 shows the I-V characteristics of p-type $HfSiO_x$ capacitors after PDA at 500^oC 60 seconds and treated by CF_4 plasma of 200W with different process time from 0 V to -2V. After CF_4 plasma treatment, we can see much reduction of leakage current in contrast of no treatment samples. It is worthy to be noticed that all the capacitors treated by CF_4 plasma have a low leakage current about 2×10^{-4} A/cm^2 at Vg = -1V. We can clearly see the F element will effectively repair defect, can let leakage current seriously decrease.

As a consequence, the N_2, N_2O, NH_3 CF_4 plasma treatment all shows better electrical properties than no treatment sample. Furthermore, the N element, O element and F element all could fix the interface and improve the electrical properties include of C-V curve and I-V curve.

3.3 Electrical characteristics of capacitors with different gate dielectric thickness

We have four kinds of plasma treatment with different source gas (i.e. N_2, N_2O, NH_3) and treated for different process time (i.e. 30 seconds, 60 seconds and 90 seconds). Then we compare the effect of different source gas with different thickness.

3.3.1 Capacitance-voltage characteristics for $HfSiO_x$

Fig. 3-13 shows C-V characteristics of 3nm $HfSiO_x$ gate dielectrics after PDA at 500^{o}C 60 seconds and treated with N_2 plasma treatment for 60 seconds, N_2O plasma treatment for 60 seconds and NH_3 plasma treatment for 30 seconds. It is indicated that the capacitances treated with N_2 plasma for 60 seconds and NH_3 plasma for 30 seconds show the most excellent value (i.e. 30% increasing about capacitance). Among these samples, the reason why the sample treated with N_2O plasma has lower capacitance than N_2 and NH_3 plasma treatment is complex. It is may be the growing of interfacial oxide made the C value smaller and this interfacial layer also made the gate leakage current smaller. But for the reason of oxidation caused by oxygen radical, the N_2O plasma treatment samples show the lower C value.

Fig. 3-14 shows C-V characteristics of 5nm $HfSiO_x$ gate dielectrics after PDA at 500^{o}C 60 seconds and treated with N_2 plasma treatment for 60 seconds, N_2O plasma treatment for 60 seconds and NH_3 plasma treatment for 30 seconds. It is indicated that the capacitance treated with NH_3 plasma for 30 seconds shows the most excellent value (i.e. 60% increasing about capacitance).

3.3.2 Leakage current-voltage characteristics for $HfSiO_x$

Fig. 3-15 and Fig. 3-16 show I-V characteristics of 3nm and 5nm $HfSiO_x$ gate dielectrics after PDA at 500°C 60 seconds and treated with N_2 plasma treatment for 60 seconds, N_2O plasma treatment for 60 seconds and NH_3 plasma treatment for 30 seconds. It is indicated that the capacitances treated with plasma show the lower leakage current. Especially for capacitor which treated with N_2 plasma 30 seconds has the lowest leakage.

3.4 Electrical characteristics of capacitors combined with two plasma treatment for different process Time

Final, we try to combined two plasma treatment for different process time to see the electrical characteristics of P-type capacitors.

3.4.1 Capacitance-voltage characteristics for $HfSiO_x$

Fig. 3-17 shows C-V characteristics of $HfSiO_x$ gate dielectrics after PDA at 500°C 60 seconds and treated with N_2 plasma treatment of 200W for 60 seconds, then treated with CF_4 plasma treatment for 30 or 120 seconds. It is indicated that the capacitance treated with CF_4 plasma for 30~60 seconds will increase effectively. And the C-V curve became better. But the capacitance treated with CF_4 plasma for 90~120 seconds will decrease, the result is maybe too long plasma treatment would cause plasma damage. It let the capacitance become lower. However, the N element and F element have a good collocation.

Fig. 3-18 shows C-V characteristics of $HfSiO_x$ gate dielectrics after PDA at 500°C 60 seconds and treated with N_2O plasma treatment of 200W for 60 seconds, then treated with CF_4 plasma treatment for 30 or 120 seconds. It is indicated that the capacitance treated with CF_4 plasma for 60 seconds will increase effectively. And the C-V curve became better. But same to N_2 plasma, the capacitance treated with CF_4 plasma for 120 seconds will decrease, the result is maybe too long plasma treatment would cause plasma damage. It let the capacitance become lower. However, the N and O element and F element have a good collocation.

Fig. 3-19 shows C-V characteristics of $HfSiO_x$ gate dielectrics after PDA at 500^{o}C 60 seconds and treated with NH_3 plasma treatment of 200W for 30 seconds, then treated with CF_4 plasma treatment for 30 or 120 seconds. It is indicated that the capacitance treated with CF_4 plasma for 60 seconds will increase effectively. And the C-V curve became better than others. However, the N element and F element have a good collocation.

3.4.2 Leakage current-voltage characteristics for $HfSiO_x$

Fig. 3-20 shows I-V characteristics of $HfSiO_x$ gate dielectrics after PDA at 500^{o}C 60 seconds and treated with N_2 plasma treatment of 200W for 60 seconds, then treated with CF_4 plasma treatment for 30 or 120 seconds. It is indicated that after N_2 plasma treatment only, the leakage current shows the lowest leakage current. But had CF_4 plasma will increase, this is maybe that the F element would etch $HfSiO_x$, causing the oxide became thinner and let the leakage current increase. The sample treated with CF_4 plasma 120 seconds was the most obvious.

Fig. 3-21 shows I-V characteristics of $HfSiO_x$ gate dielectrics after PDA at 500^{o}C 60 seconds and treated with N_2O plasma treatment of 200W for 60 seconds, then treated with CF_4 plasma treatment for 30 or 120 seconds. It is indicated that after N_2O plasma treatment only, the leakage current shows the lowest leakage current. But had CF_4 plasma will increase, this is maybe that the F element would etch $HfSiO_x$, causing the oxide became thinner and let the leakage current increase. The sample treated with CF_4 plasma 90~120 seconds was the most obvious.

Fig. 3-22 shows I-V characteristics of $HfSiO_x$ gate dielectrics after PDA at 500^{o}C 60 seconds and treated with NH_3 plasma treatment of 200W for 60 seconds, then treated with CF_4 plasma treatment for 30 or 120 seconds. It is indicated that after NH_3 plasma treatment only and with short time CF_4 plasma like 30 seconds, the leakage current shows the lowest leakage current. But had long time CF_4 plasma will increase, this is maybe that the F element would etch $HfSiO_x$, causing the oxide became thinner and let the leakage current increase. The sample treated with CF_4 plasma 90~120 seconds was the most obvious.

After plasma treatment we always did post deposition annealing and post plasma treatment annealing, the sample without nitridation can not sustain the high temperature annealing, so nitridation can improve the thermal stability of high-k film. The sample without PDA and treated by plasma treatment directly is distorted at high negative bias voltages owing to the crystallization. It might be cause by plasma damage, therefore we must add the post-nitridation anneal step to restore the plasma damage. We could see that after post deposition anneal, nitridation could effectively improve the thermal stability of the thin film. We can find the same result, the sample with nitridation after PDA can effectively decrease gate leakage current. It is good evidence to show that the thin film treated by plasma treatment after post-deposition anneal can make the thin film sustain high thermal stress.

Chapter 4

Reliability of Al-Ti-$HfSiO_x$-Si MIS capacitors

4.1 Hysteresis

When a ferromagnetic material is magnetized in one direction, it will not relax back to zero magnetization when the applied magnetizing field is removed. It must be driven back to zero by the additional opposite direction magnetic field. If an alternating magnetic field is applied to the material, its magnetization will trace out a loop called a hysteresis loop. The lack of retrace ability of the magnetization curve is the property called hysteresis and it is related to the existence of magnetic domains in the material. Once the magnetic domains are reoriented, it takes some energy to turn them back again [36]. The hysteresis phenomenon is similar in the C-V curve of the MIS capacitor device. When we apply a voltage in opposite direction, it will not fit the original C-V curve measured previously. It is due to the traps of interface which would trap charges to influence the flat band voltage and C-V curve. [37]

Fig. 4-1 shows the hysteresis of p-type $HfSiO_x$ gate dielectric which was without PDA. Fig. 4-2 shows the hysteresis of p-type HfO_2 gate dielectric which was with PDA 500^{o}C 60 seconds but without plasma treatment. We see that, the hysteresis of the thin film treated with annealing was much smaller than the thin film without annealing. It is a good way to do annealing ater deposited Hf-base dielectric, because its interfacial trap density could be removed after annealing. The hysteresis for capacitance which was with PDA is 44 mV.

Fig. 4-3 shows the hysteresis of p-type $HfSiO_x$ gate dielectrics with PDA 500^{o}C 60 seconds、N_2 plasma 60 seconds、and PNA 600^{o}C 30 seconds. The hysteresis is 32 mV. Fig. 4-4 shows the hysteresis of p-type $HfSiO_x$ gate dielectrics with PDA 500^{o}C 60 seconds、N_2O plasma 60 seconds、and PNA 600^{o}C 30 seconds. The hysteresis is 23 mV. Fig. 4-5 shows the hysteresis of p-type $HfSiO_x$ gate dielectrics with PDA 500^{o}C 60 seconds、NH_3 plasma 30 seconds、and PNA 600^{o}C 30 seconds. The hysteresis is 26 mV. So nitridation could decrease the trap density and let the thin film sustain high thermal stress.

Fig. 4-6 shows the hysteresis of p-type $HfSiO_x$ gate dielectrics with PDA 500^{o}C 60 seconds、CF_4 plasma 60 seconds、and PNA 600^{o}C 30 seconds. The hysteresis is 2 mV. Fig. 4-7 shows the hysteresis of p-type $HfSiO_x$ gate dielectrics with PDA 500^{o}C 60 seconds、N_2 plasma 60 seconds、CF_4 plasma 60 seconds、and PNA 600^{o}C 30 seconds. The hysteresis is 9 mV. Fig. 4-8 shows the hysteresis of p-type $HfSiO_x$ gate dielectrics with PDA 500^{o}C 60 seconds、N_2O plasma 60 seconds、CF_4 plasma 60 seconds、and PNA 600^{o}C 30 seconds. The hysteresis is 16 mV. Fig. 4-9 shows the hysteresis of p-type $HfSiO_x$ gate dielectrics with PDA 500^{o}C 60 seconds、NH_3 plasma 30 seconds、CF_4 plasma 60 seconds、and PNA 600^{o}C 30 seconds. The hysteresis is 12 mV. So fluorination could decrease the trap density and let the thin film sustain high thermal stress too and more clearly. As a consequence, the plasma treatment can improve the reliability of gate oxide.

4.2 Constant voltage stress (CVS)

To study the reliability of thin films, we can stress the samples with a constant voltage or a constant current, which are useful methods. The mechanism of CVS is the charge trapped by the interfacial trap density which is caused by stress for a long time. In addition, the increasing interface trap density would cause new leakage path to add leakage current. In our experiments, we use constant voltage stress (CVS) to test the reliability of the thin film.

Fig. 4-10 shows gate current shift of p-type $HfSiO_x$ gate dielectrics treated with N_2 plasma treatment and CF4 plasma treatment during CVS with V_g = 5 V. It indicated that the thin film with plasma treatment which current shift was smaller than the original one. The sample with N_2 plasma and CF_4 plasma treatment also had much smaller current shift but had large leakage current. Fig. 4-11 shows gate current shift of p-type $HfSiO_x$ gate dielectrics treated with N_2 plasma treatment and CF4 plasma treatment during CVS with V_g = 5 V. It indicated that the thin film with plasma treatment which current shift was smaller than the original one. The sample with N_2O plasma and CF_4 plasma treatment also had much smaller current shift but had large leakage current. Fig. 4-12 shows gate current shift of p-type $HfSiO_x$ gate dielectrics treated with NH_3 plasma treatment and CF4 plasma treatment during CVS with V_g = 5 V. It indicated that the thin film with plasma treatment which current shift was smaller than the original one. The sample with N_2 plasma and CF_4 plasma treatment also had much smaller current shift but had large leakage current.

The gate leakage shift level of the samples with or not nitridation differed about 3 to 4 orders, so nitridation process could decrease the trap density effectively. It might be a good way to incorporate N atoms in the thin film to improve the reliability of the gate dielectrics.

Chapter 5

Conclusions and future work

5.1 Conclusions

In this thesis, characteristics and reliability of $HfSiO_x$ gate dielectrics with the post-deposition annealing (PDA) and the post plasma treatment (PNA) have been investigated. These methods could be improved that the quality of $HfSiO_x$ thin film. The plasma treatment conditions are N_2, N_2O, NH3 and CH_4 plasma for 30 sec, 60 sec, 90 sec and 120 sec individually. After the post-deposition annealing (PDA), the plasma treatment and the post plasma treatment (PNA), our experimental data revealed low leakage current density and good thermal stability. We find several important phenomena and they would be summarized as follows.

First, improvement in the electrical characteristics of Al-Ti-$HfSiO_x$-Si MIS capacitors after post-deposition-annealing has been demonstrated in this work. The $HfSiO_x$ thin film after PDA would become dense and we could find their capacitance would increase and gate leakage current would decrease.

Second, all of the samples after plasma treatment can promote the electrical characteristics and reliability until the plasma damage happened. Among these treatments, the sample treated by N_2 plasma treatment for 60 sec, N_2O plasma treatment for 60 sec, NH_3 plasma treatment for 30 sec and CF_4 plasma treatment for 60 sec for $HfSiO_x$ represented a fairly great improvement, such as good capacitance (25~40% increasing for $HfSiO_x$), reduced leakage current (about 1~2 order reduction for all samples). It was showed that the interfacial layer could be suppressed and the weak structure of interface has been repaired by N_2 and NH_3 plasma respectively. However, N_2O plasma treatment also can provide good effects on electrical characteristics. The samples treated N_2O plasma treatment would introduce oxygen bonding to form additional interfacial layer, so the capacitance would be decreased a little. The sample treated by CF_4 plasma also showed excellence promotion about reliability issues, such as smaller hysteresis (< 15 mV) and better CVS curve.

Finally, in this thesis, it has been indicated that combined two kinds of plasma, such as N_2, NH_3 and N_2O plasma and then did the CF_4 plasma treatment could improve stress stability of $HfSiO_x$ thin film. Simultaneously, and the reliability of the film after nitridation and fluorination also represented better electronic characteristics. The most suitable way for post-deposition treatment by plasma to improve electrical characteristics on MIS structure has been observed.

5.2 Future work

In this experiment, the $HfSiO_x$ film was deposited by MOCVD system. In the future, the ALCVD (Atomic Layer CVD) system will become another important deposition technology. Further experiment and analysis are required to clarify if the same treatment condition is also suitable for ALCVD film. On the other hand, the MOSFET will be fabricated by the same treatment condition to verify the effect on device characteristics, such as mobility, subthreshold swing, and transonductance.

The interfacial layer between high-k/Si would be increased by increasing post-deposition-annealing temperature. In order to suppress the growth of the interfacial layer, we could use some pre-treatment methods to introduce a thin oxide or nitride layer by HDP-PECVD or chemical deposition. Furthermore, we might have to understand the mechanism of leakage current of thin film and thick film individually. Finally, the mechanism of the generation of the defects in the high-k bulk or interface still needs to be solved.

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Table

Table 1-1 High-performance Logic Technology Requirements Roadmap.

(ITRS：2006 updae)

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1E20-doped poly-Si [A, A1, A2]	1.1	1	1						
WAS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.2	1.1	1.1	0.5					
IS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.2	1.1	1.1	1	0.9				
WAS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 3E20-doped poly-Si [A, A1, A2]	1.3	1.2	1.2	0.71	0.54	0.41			
IS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 3E20-doped poly-Si [A, A1, A2]	1.3	1.2	1.2	1.2	1.1	0.41			
WAS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				0.9	0.75	0.65	0.5	0.5	
IS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				~~0.9~~	~~0.75~~	0.65	0.5	0.5	
WAS	Gate dielectric leakage at 100 °C (A/cm^2) bulk high-performance [B, B1, B2]	1.80E+02	5.40E+02	8.00E+02	9.10E+02	1.10E+03	1.60E+03	2.00E+03	2.40E+03	
IS	Gate dielectric leakage at 100 °C (A/cm^2) bulk high-performance [B, B1, B2]	1.80E+02	5.40E+02	8.00E+02	1.20E+03	1.10E+03	1.60E+03	2.00E+03	2.40E+03	
WAS	Metal gate work function for bulk MPU/ASIC $\|E_{c,v} - \phi_m\|$ (eV) [C]				<0.2	<0.2	<0.2	<0.2	<0.2	
IS	Metal gate work function for bulk MPU/ASIC $\|E_{c,v} - \phi_m\|$ (eV) [C]				~~<0.2~~	~~<0.2~~	<0.2	<0.2	<0.2	
WAS	Channel doping concentration (cm^{-3}), for bulk design [D]	3.70E+18	4.60E+18	5.40E+18	7.30E+18	8.60E+18	8.90E+18	8.60E+18	8.80E+18	
IS	Channel doping concentration (cm^{-3}), for bulk design [D]	3.25E+18	3.68E+18	4.19E+18	5.80E+18	7.30E+18	7.14E+18	8.08E+18	9.00E+18	
	Bulk/FDSOI/DG – Long channel electron mobility enhancement factor for MPU/ASIC [E]	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
	Drain extension X_j (nm) for bulk MPU/ASIC [F]	11	9	7.5	7.5	7	6.5	5.8	4.5	
	Maximum allowable parasitic series resistance for bulk NMOS MPU/ASIC × width ((Ω–μm) [G]	180	170	140	140	120	105	80	70	
	Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq) [G]	653	674	640	740	677	650	548	593	
	Extension lateral abruptness for bulk MPU/ASIC (nm/decade) [H]	3.5	3.1	2.8	2.5	2.2	2	1.8	1.5	
	Contact X_j (nm) for bulk MPU/ASIC [I]	35.2	30.8	27.5	25.3	22	19.8	17.6	15.4	

Table 1-2 Characteristics of various high-k materials.

Material	Dielectric Constant (k)	Band Gap E_G (eV)	ΔE_C (eV) to Si	Crystal Structure (s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8	Amorphous
Y_2O_3	15	5.6	2.3	Cubic
La_2O_3	30	4.3	2.3	Hexagonal, Cubic
Ta_2O_5	26	4.5	1-1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[b], (Rutile, Anatase)
HfO_2	25	5.7	1.5	Mono.[a], Tetrag[b]., Cubic
ZrO_2	25	7.8	1.4	Mono.[a], Tetrag.[b], Cubic

[a]Mono. = Monoclinic.
[b]Tetrag. = Tetragonal.

Figure-chapter 1

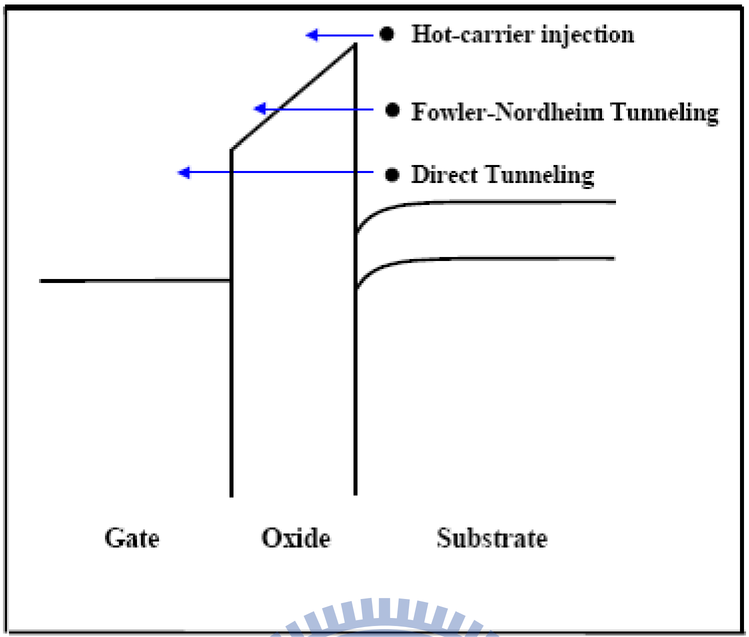


Fig. 1-1 Conduction mechanism in oxide for the MOS structure.

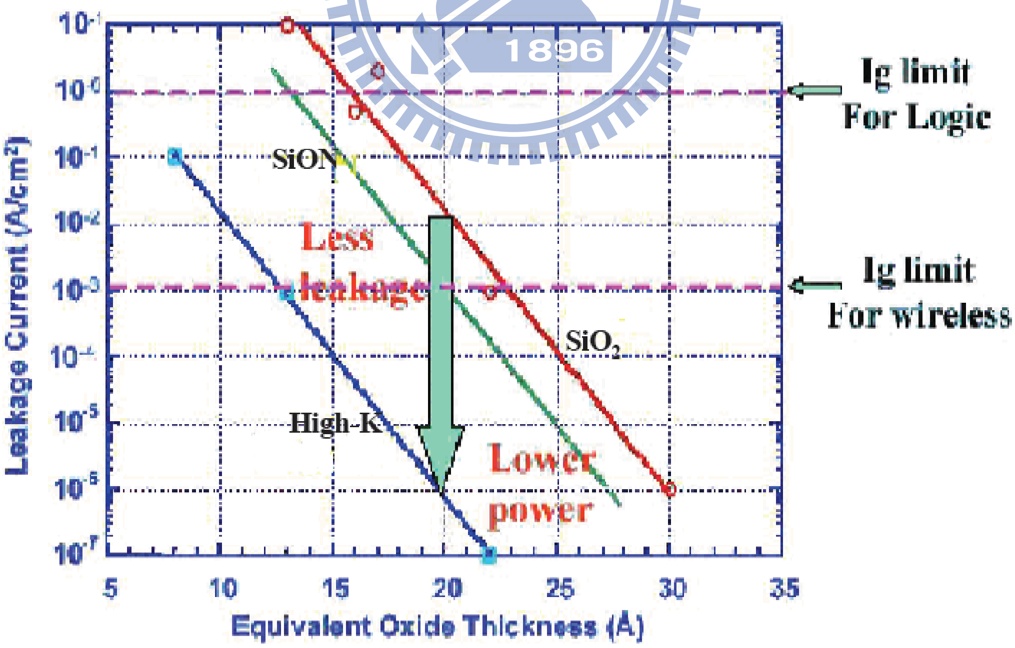


Fig1-2 Roadmap of the gate dielectric.

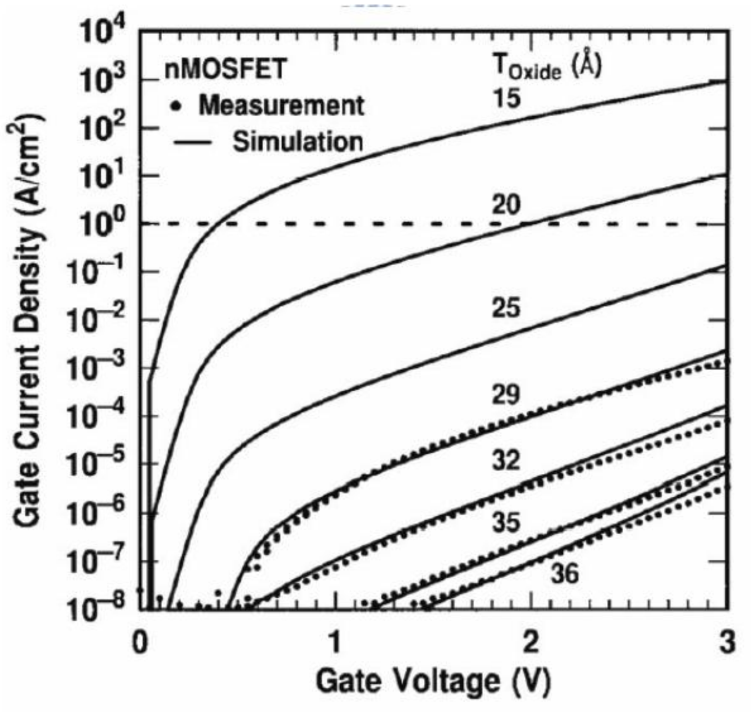


Fig. 1-3 Measured and simulated I_g-V_g characteristics under inversion condition for nMOSFETs. The dotted line indicates the 1A/cm^2 limit for the leakage current. [14]

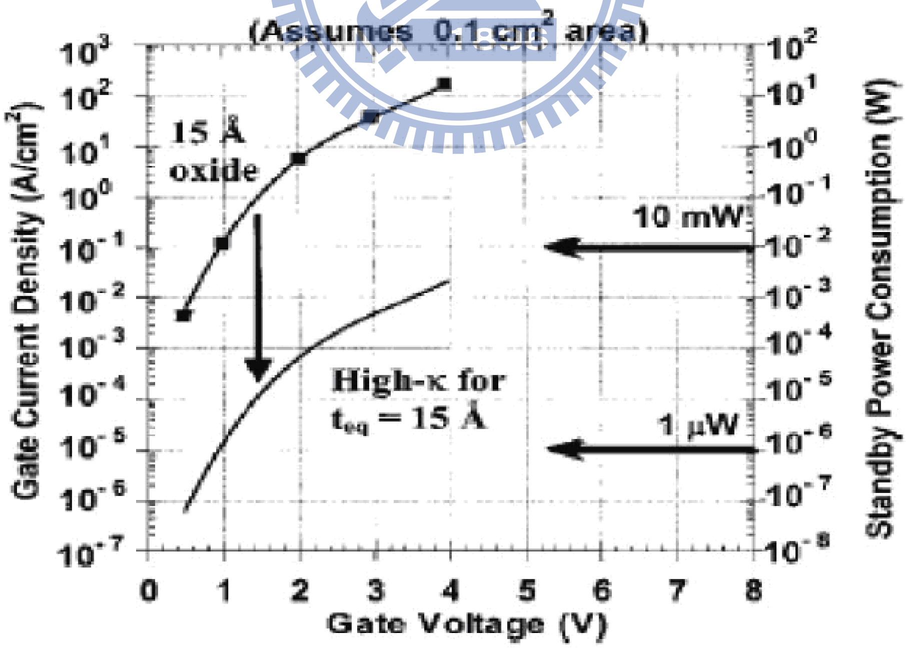


Fig. 1-4 Power consumption and gate leakage current density comparing to the potential reduction in leakage current by an alternative dielectric exhibiting the same equivalent oxide thickness [15].

Figure-chapter 2

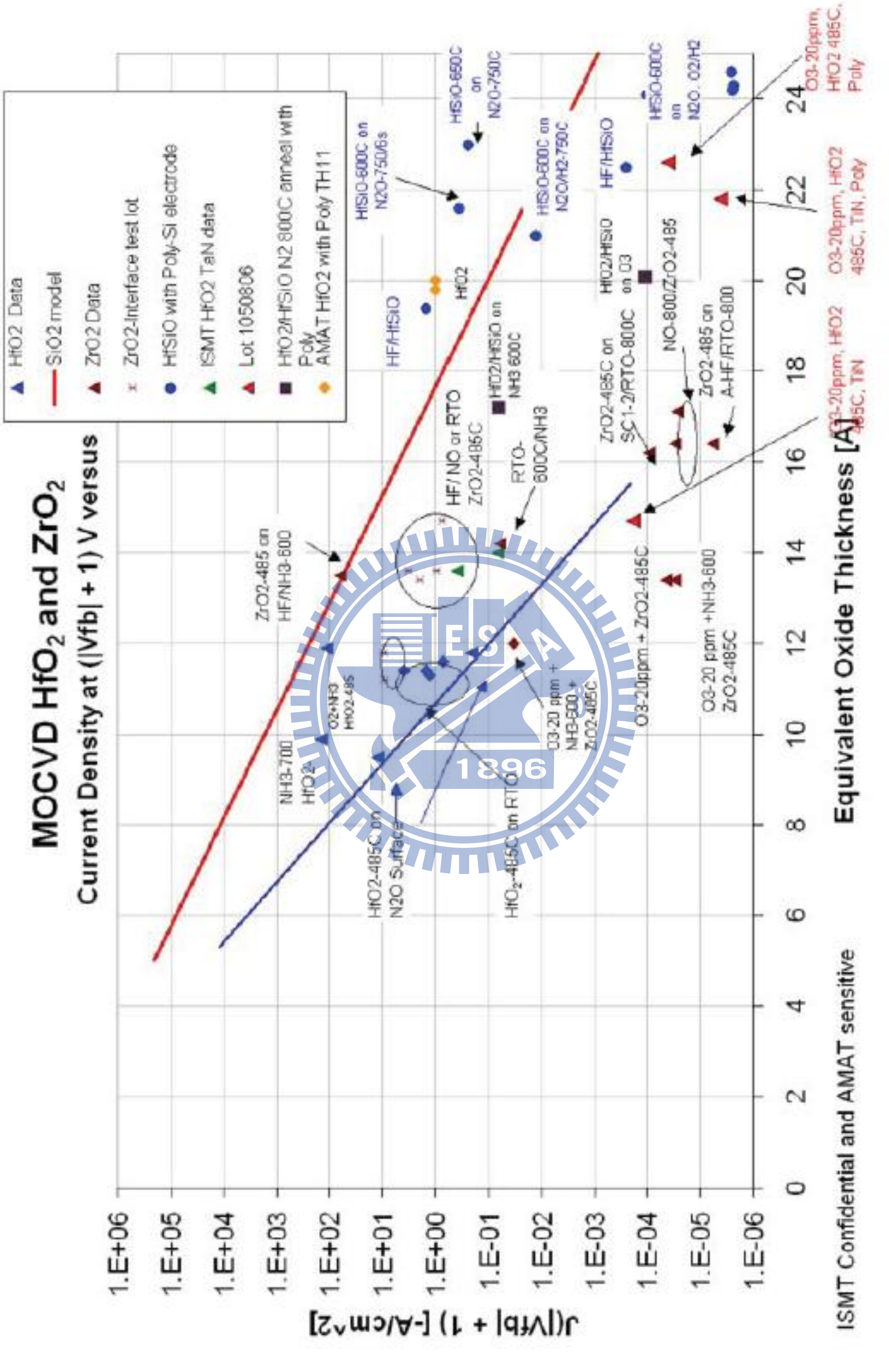


Fig. 2-1 Scaling limits of MOCVD HfO_2 and ZrO_2.
(International SEMATECH Confidential and Supplier Sensitive, 2002)

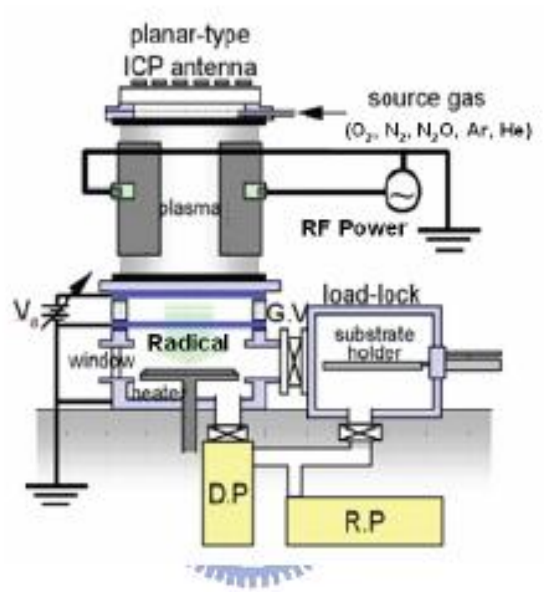


Fig 2-2 The ICP plasma system that was used in this experiment.

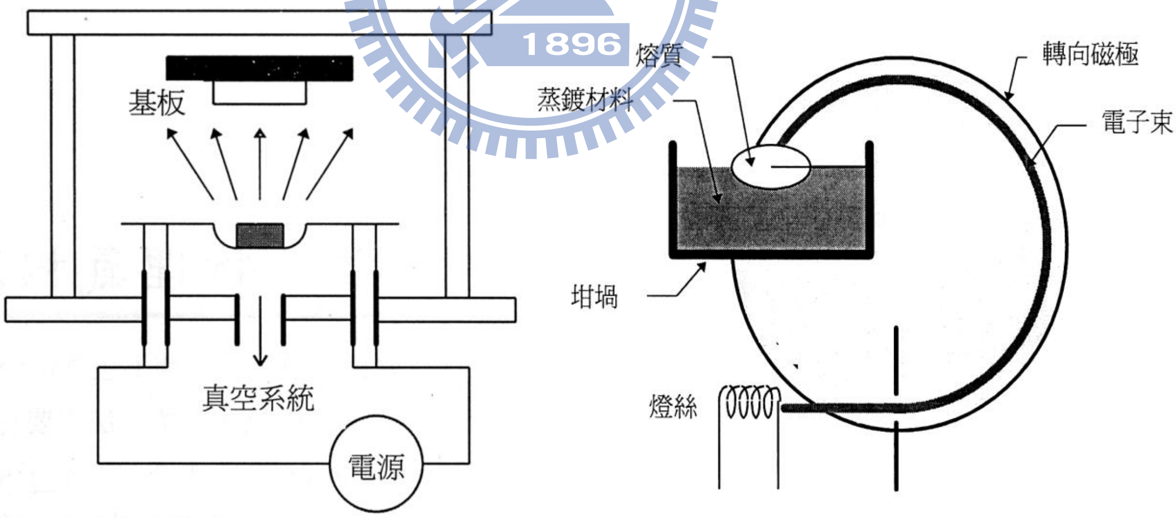
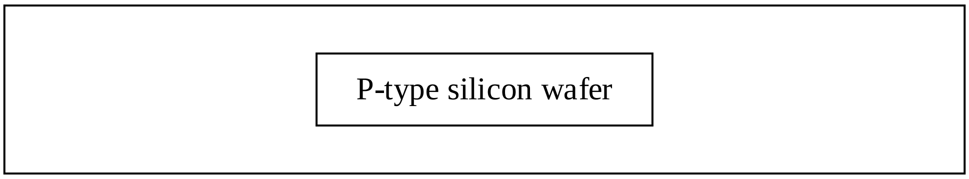
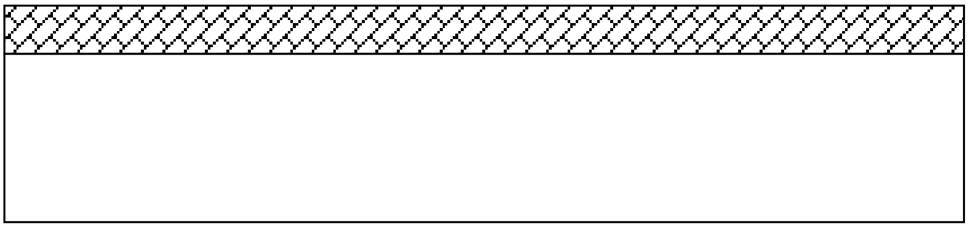


Fig 2-3 The E-gun system that was used in this experiment.

1. Standard RCA cleaning

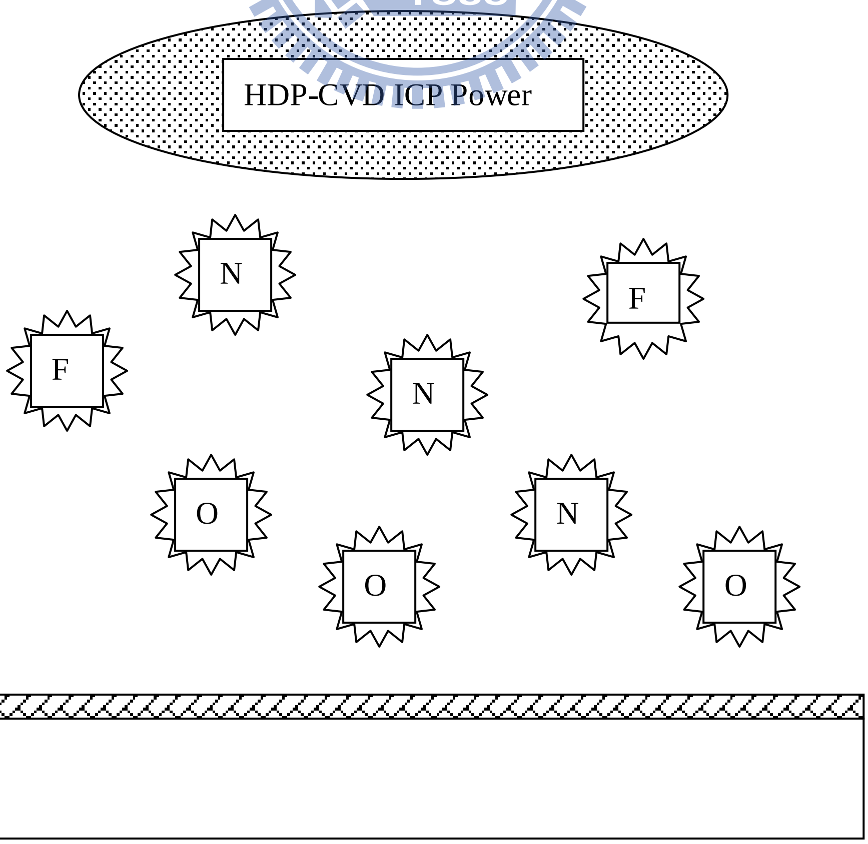


2. MOCVD deposited $HfSiO_x$ 2nm



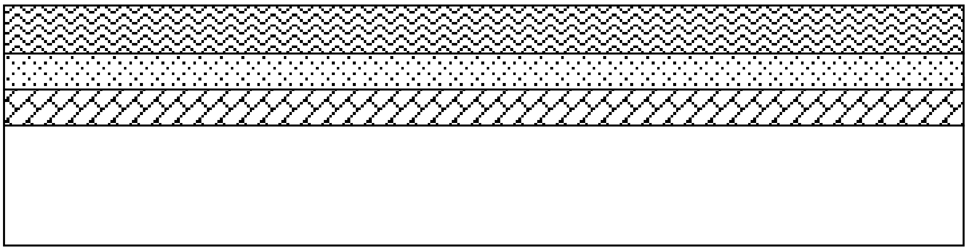
3. Post-deposition-annealing (500°C 60 seconds)

4. Plasma treatment with N_2, N_2O, NH_3 or CF_4 (30seconds, 60 seconds, 90 seconds, 120 seconds)

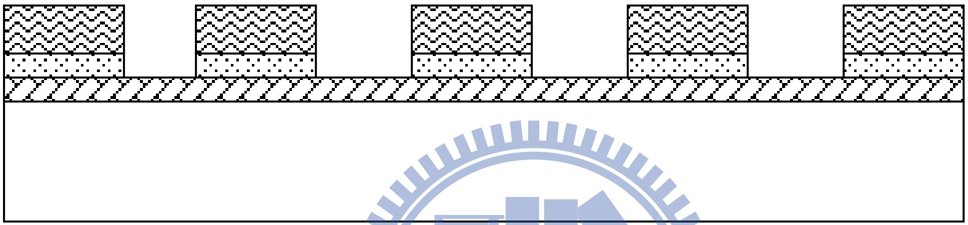


5. Post-nitridation-annealing (600^{o}C 30seconds)

6. Thermally evaporate 400nm Aluminum as top electrode



7. Lithography：Define top electrode → Wet etch undefined Ti and Al



8. Thermally evaporate 500nm Aluminum as bottom electrode

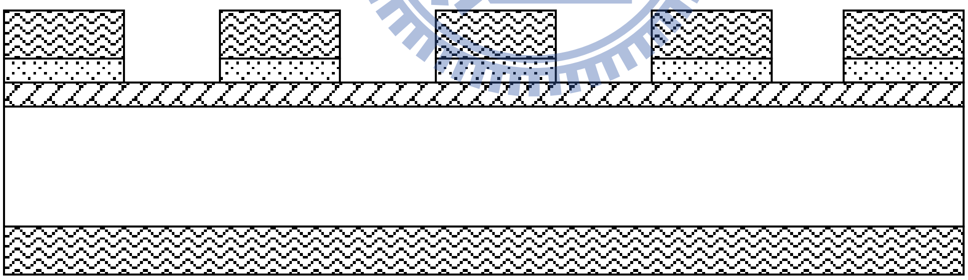


Fig. 2-4 The fabrication flow of the experiment

Figure-chapter 3

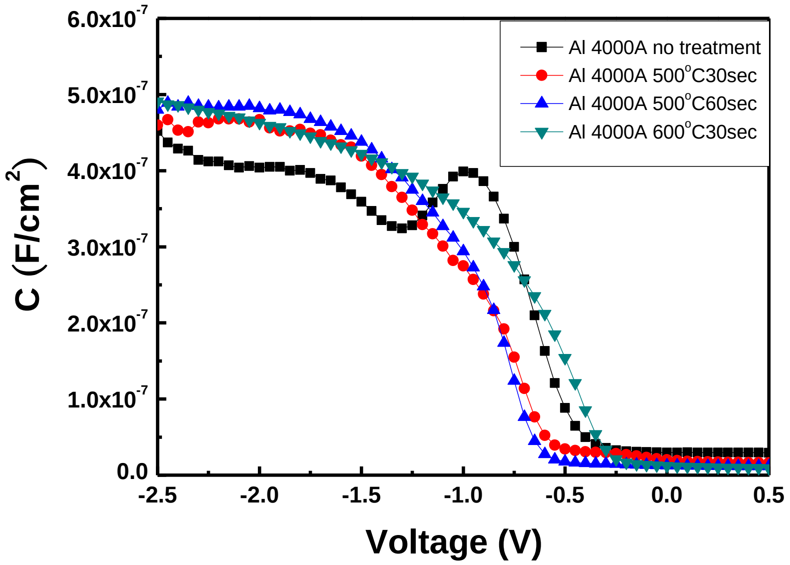


Fig. 3-1 The capacitor C-V characteristics of $HfSiO_x$ for different RTA temperatures and times with Al gate electrode

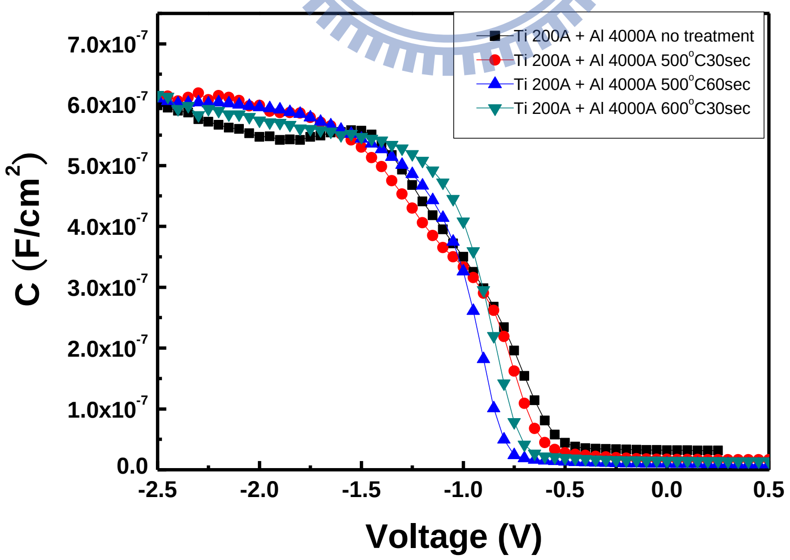


Fig. 3-2 The capacitor C-V characteristics of $HfSiO_x$ for different RTA temperatures and times with Al and Ti or Al gate electrode

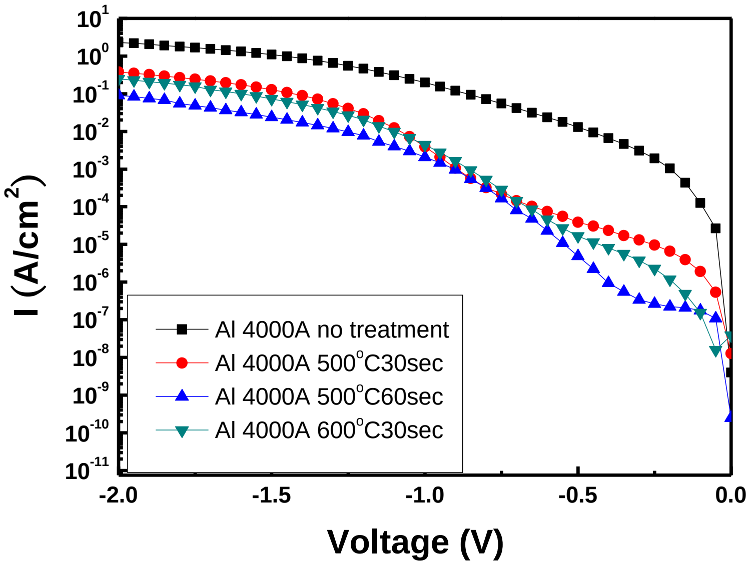


Fig. 3-3 The I-V characteristics of $HfSiO_x$ for different RTA temperatures and times with Al gate electrode

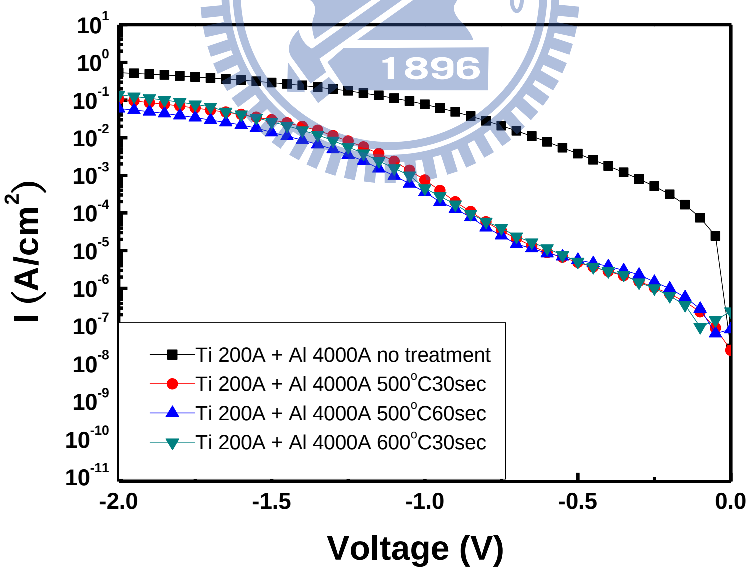


Fig. 3-4 The I-V characteristics of $HfSiO_x$ for different RTA temperatures and times with Al and Ti or Al gate electrode

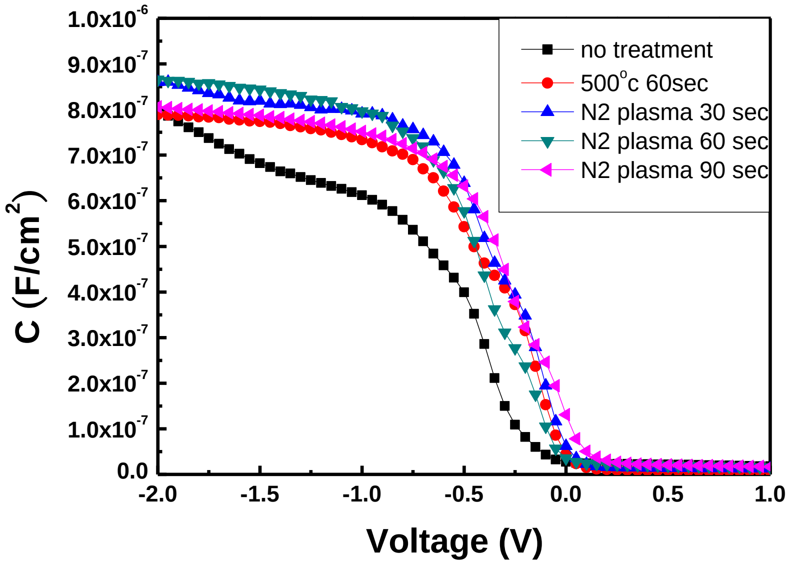


Fig. 3-5 The C-V characteristics of $HfSiO_x$ for N_2 plasma treatment compare with different times

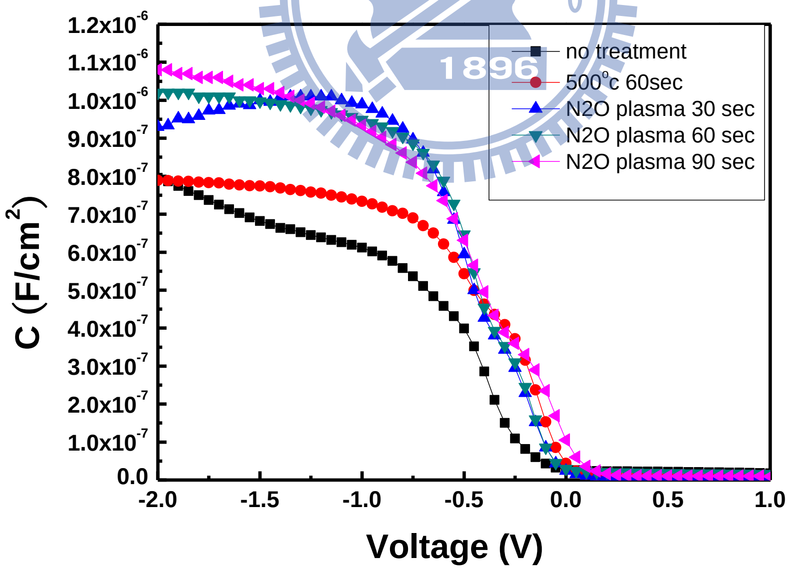


Fig. 3-6 The C-V characteristics of $HfSiO_x$ for N_2O plasma treatment compare with different times

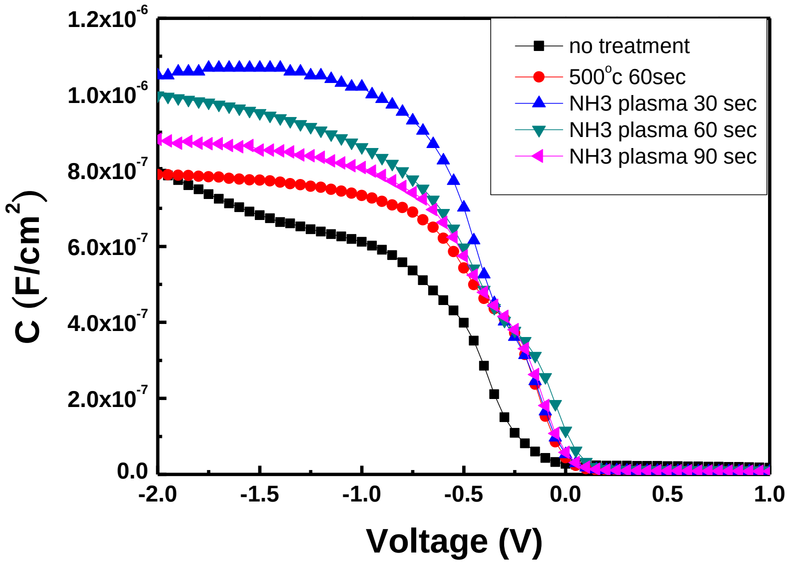


Fig. 3-7 The C-V characteristics of $HfSiO_x$ for NH_3 plasma treatment compare with different times

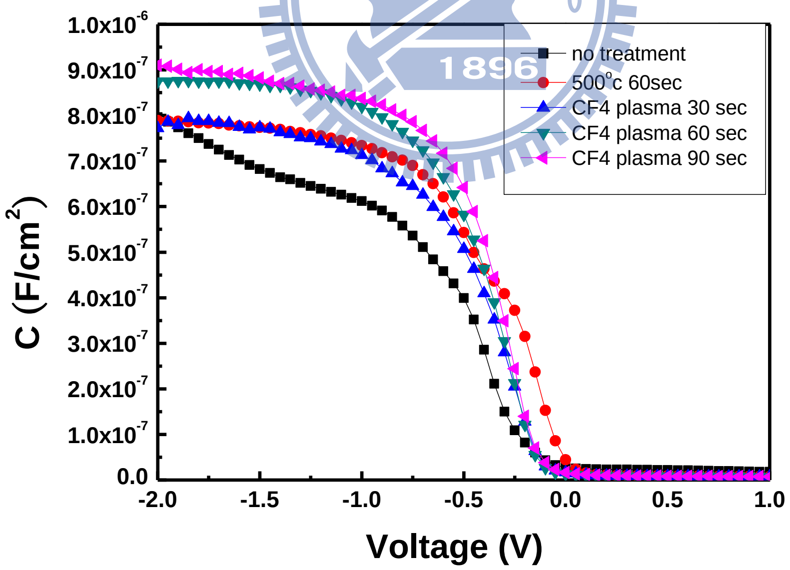


Fig. 3-8 The C-V characteristics of $HfSiO_x$ for CF_4 plasma treatment compare with different times

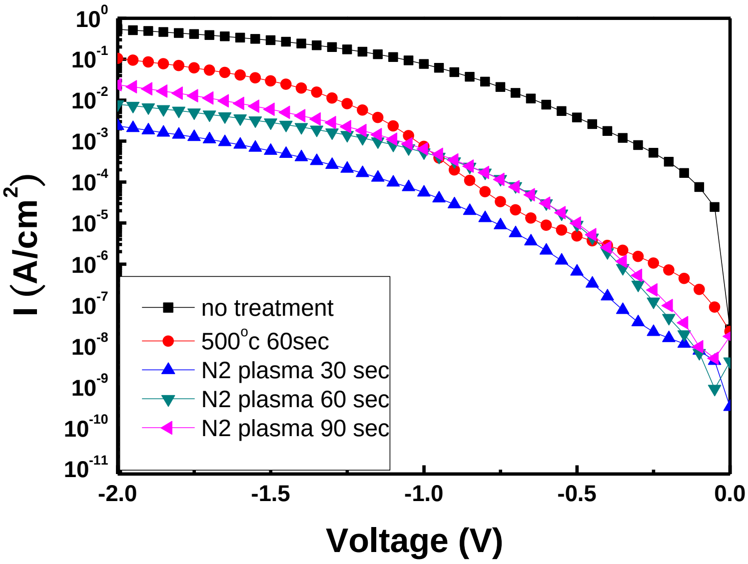


Fig. 3-9 The I-V characteristics of $HfSiO_x$ for N_2 plasma treatment compare with different times

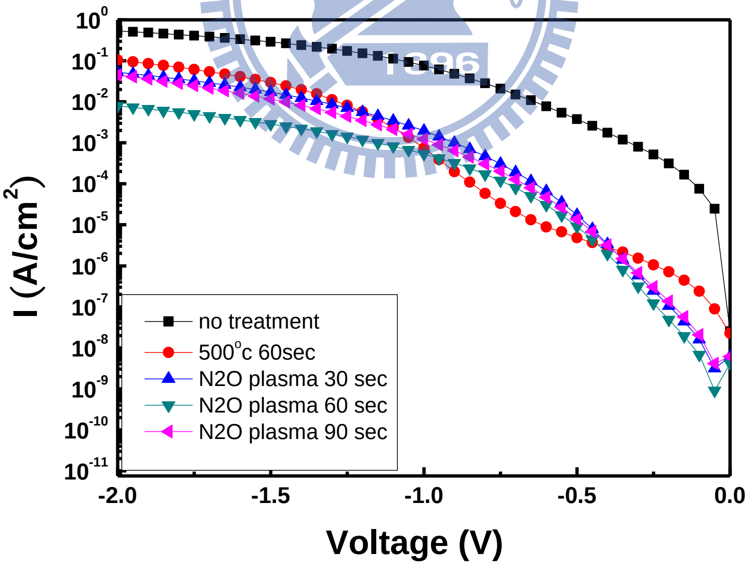


Fig. 3-10 The I-V characteristics of $HfSiO_x$ for N_2O plasma treatment compare with different times

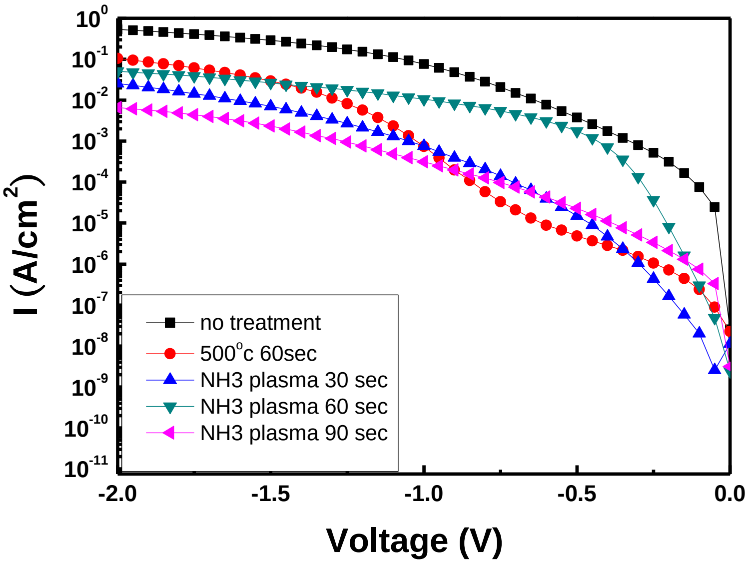


Fig. 3-11 The I-V characteristics of $HfSiO_x$ for NH_3 plasma treatment compare with different times

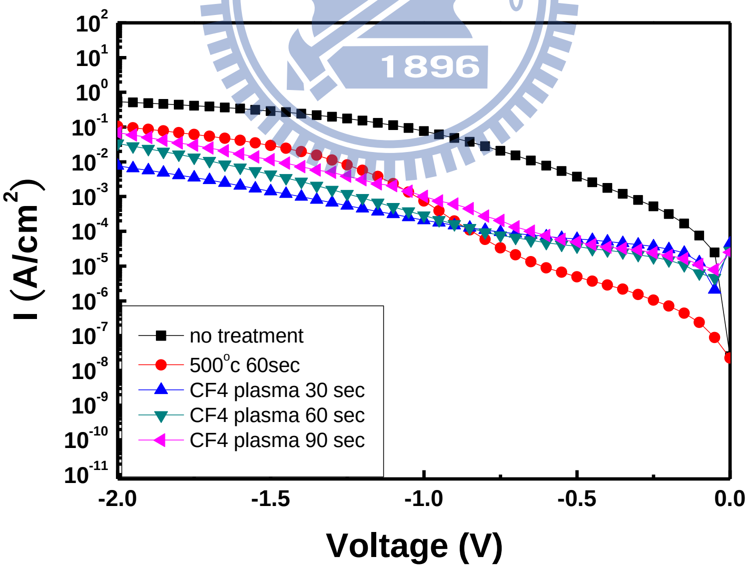


Fig. 3-12 The I-V characteristics of $HfSiO_x$ for CF_4 plasma treatment compare with different times

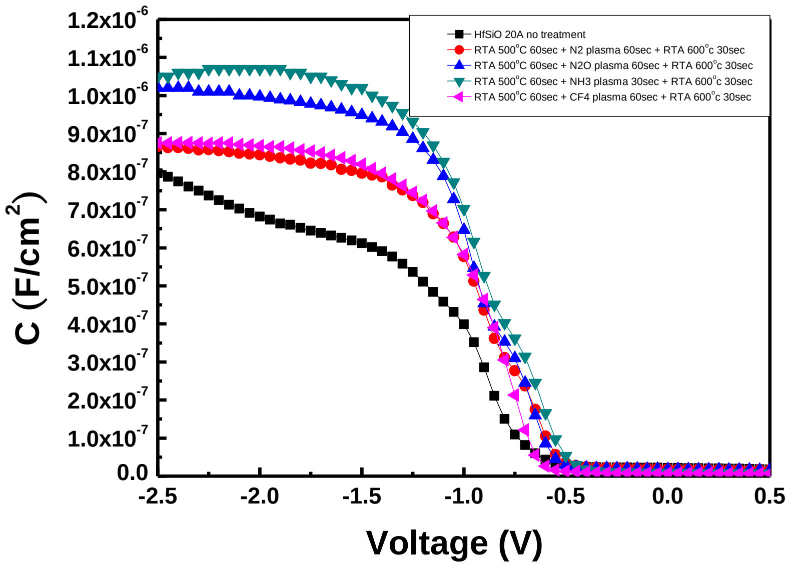


Fig. 3-13 The C-V characteristics of 3 nm $HfSiO_x$ gate dielectric Compared with different plasma treatments

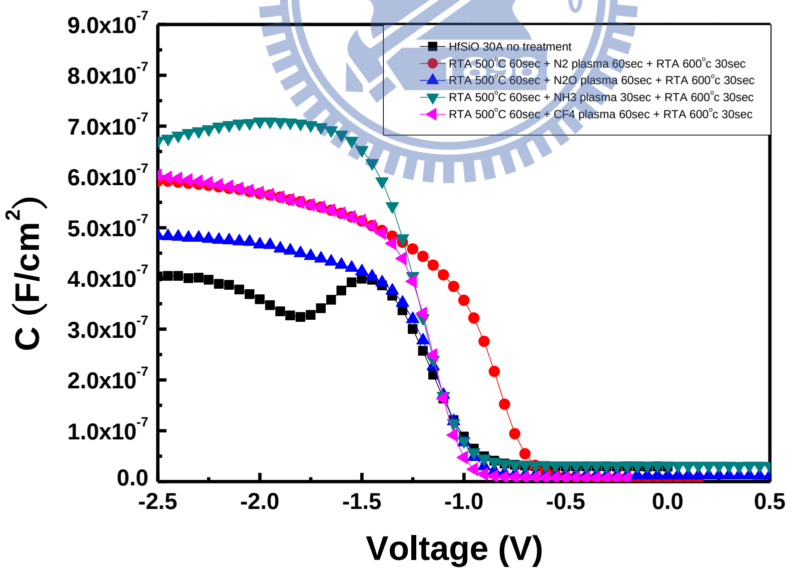


Fig. 3-14 The C-V characteristics of 5 nm $HfSiO_x$ gate dielectric Compared with different plasma treatments

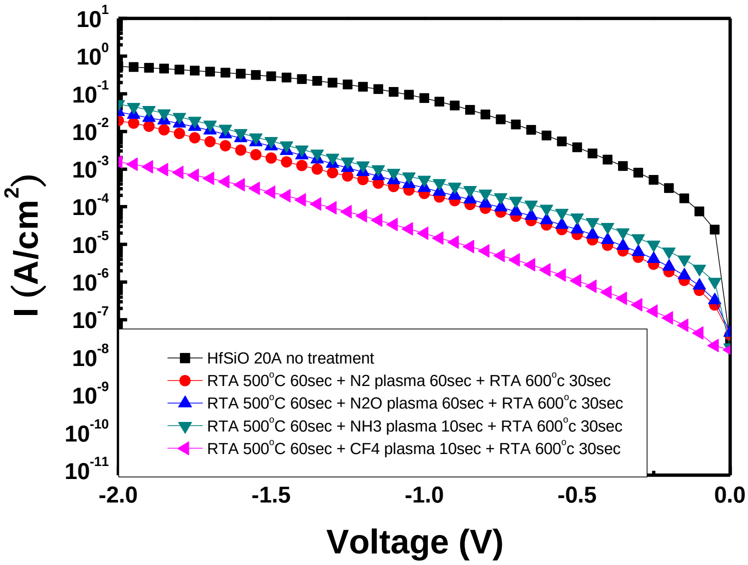


Fig. 3-15 The I-V characteristics of 3 nm $HfSiO_x$ gate dielectric Compared with different plasma treatments

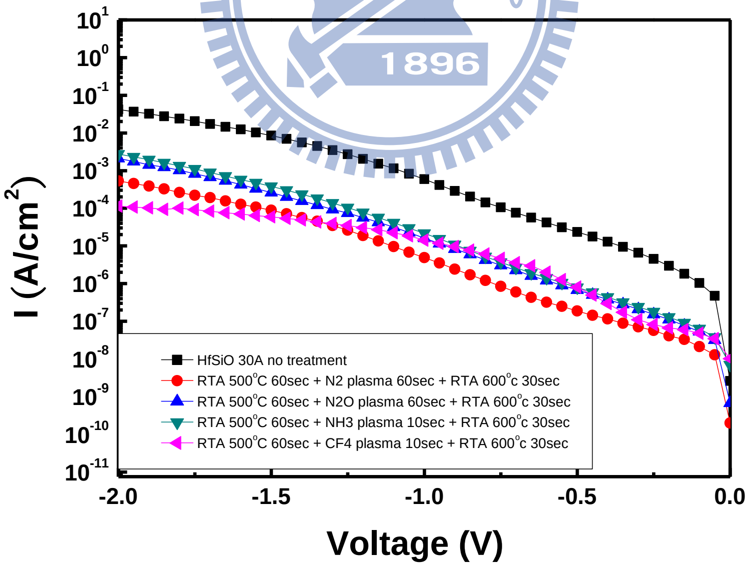


Fig. 3-16 The I-V characteristics of 5 nm $HfSiO_x$ gate dielectric Compared with different plasma treatments

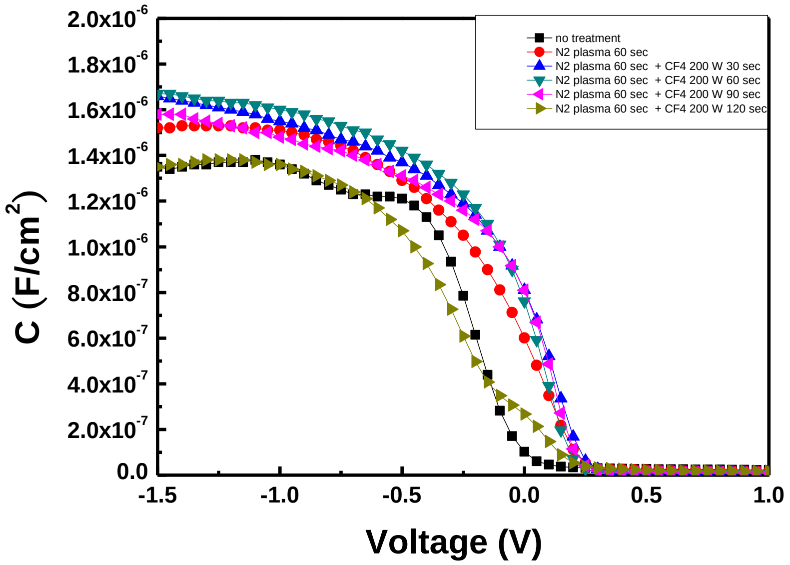


Fig. 3-17 The C-V characteristics of $HfSiO_x$ for N_2 plasma treatment then CF_4 plasma treatment

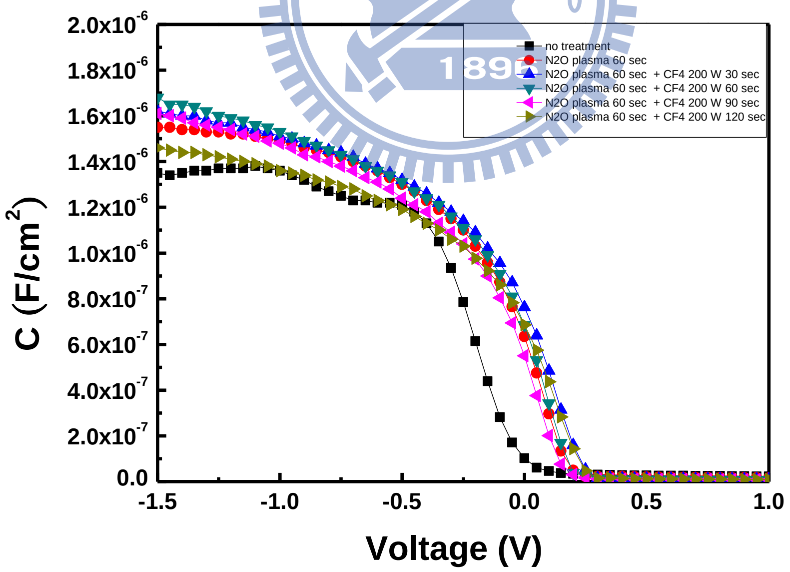


Fig. 3-18 The C-V characteristics of $HfSiO_x$ for N_2O plasma treatment then CF_4 plasma treatment

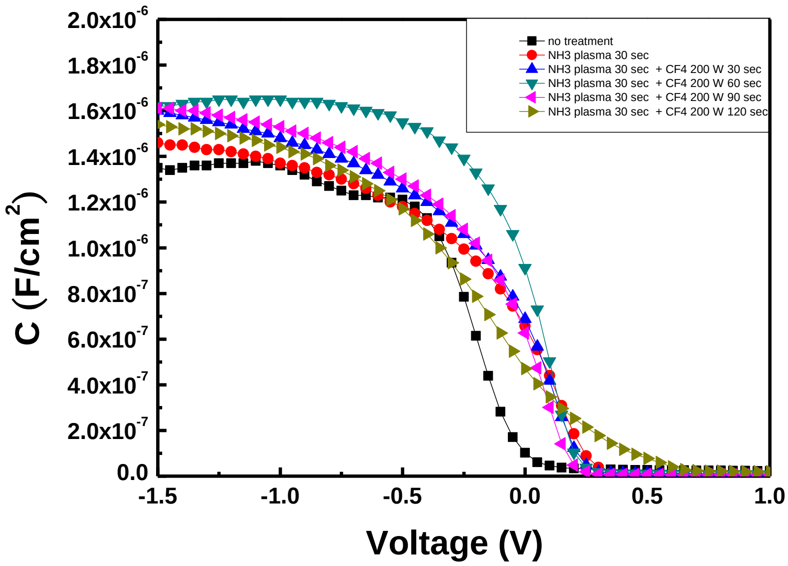


Fig. 3-19 The C-V characteristics of $HfSiO_x$ for NH_3 plasma treatment then CF_4 plasma treatment

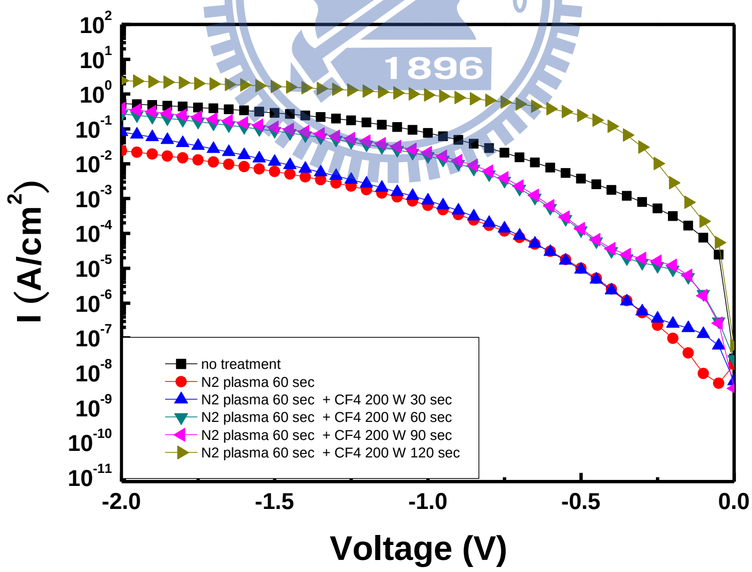


Fig. 3-20 The I-V characteristics of $HfSiO_x$ for N_2 plasma treatment then CF_4 plasma treatment

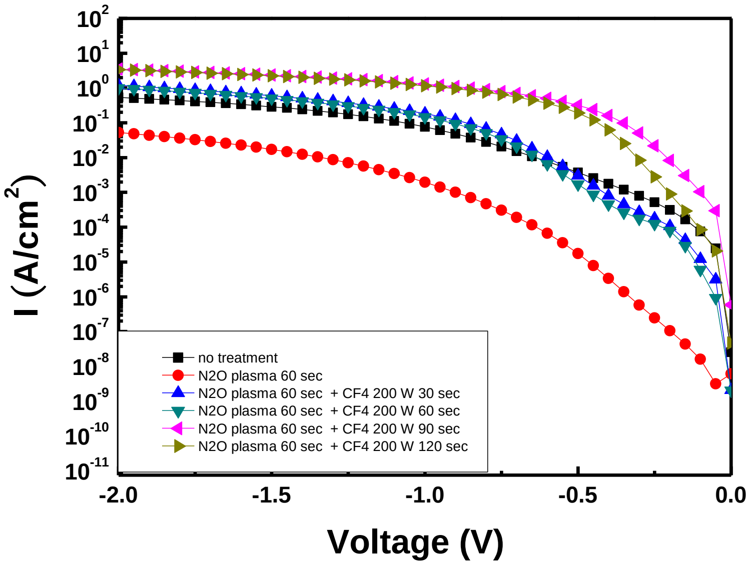


Fig. 3-21 The I-V characteristics of $HfSiO_x$ for N_2O plasma treatment then CF_4 plasma treatment

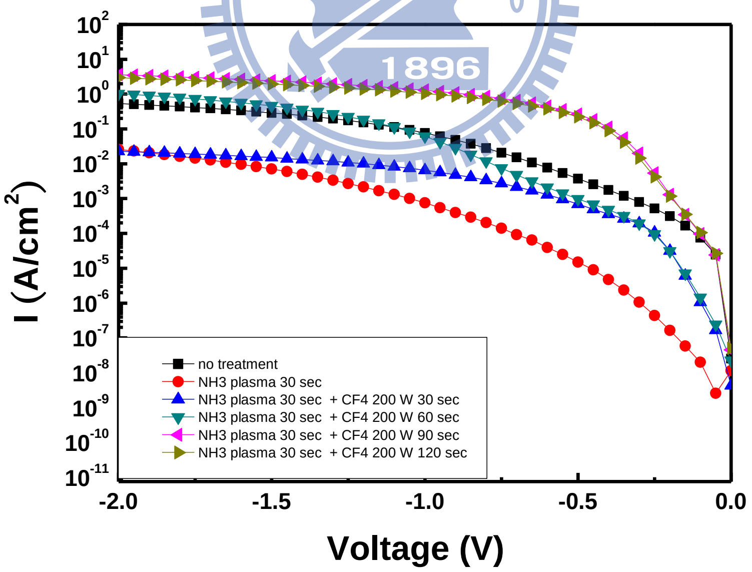


Fig. 3-22 The I-V characteristics of $HfSiO_x$ for NH_3 plasma treatment then CF_4 plasma treatment

Figure-chapter 4

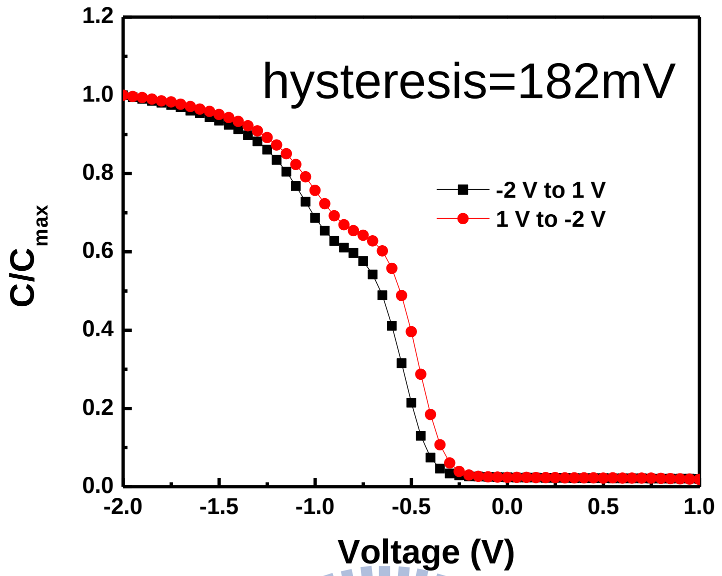


Fig. 4-1 The hysteresis of $HfSiO_x$ gate dielectrics without RTA and plasma treatment

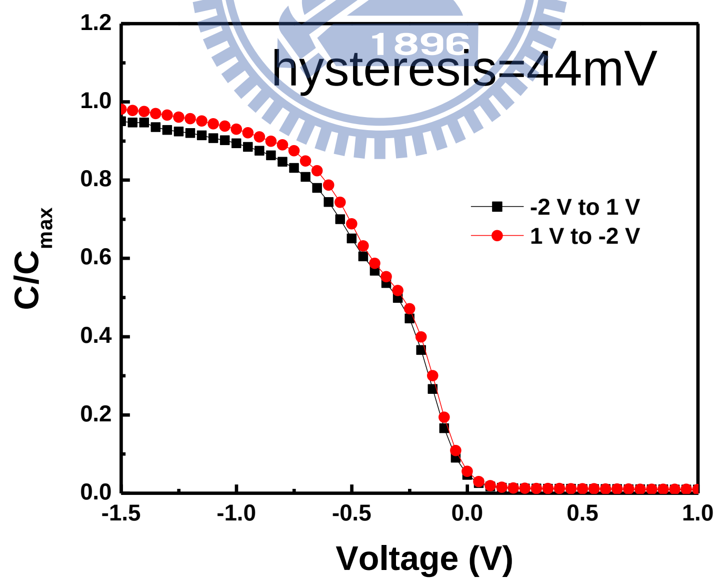


Fig. 4-2 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds

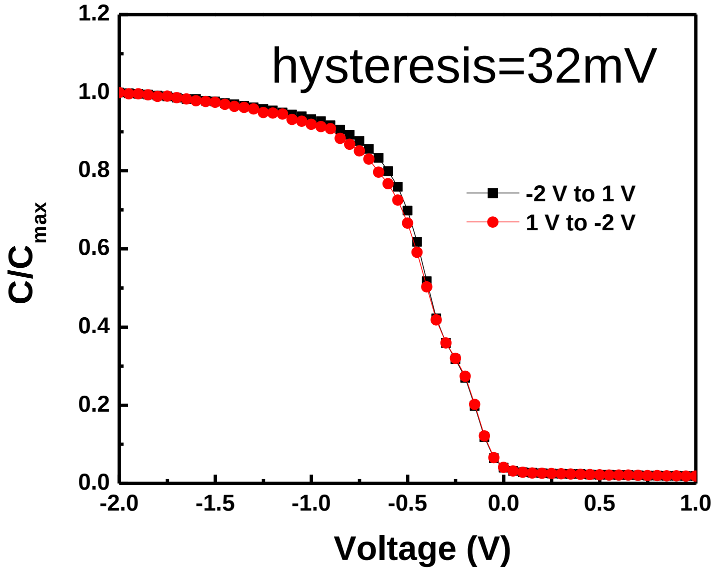


Fig. 4-3 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds and N_2 plasma 60 seconds

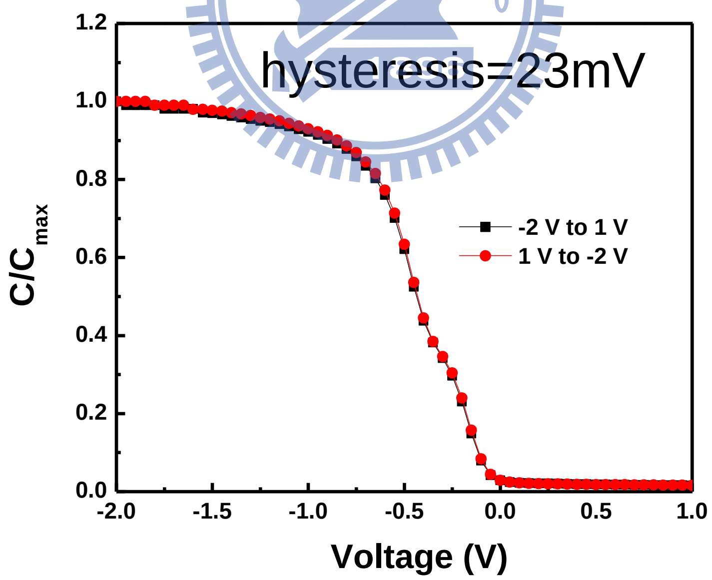


Fig. 4-4 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds and N_2O plasma 60 seconds

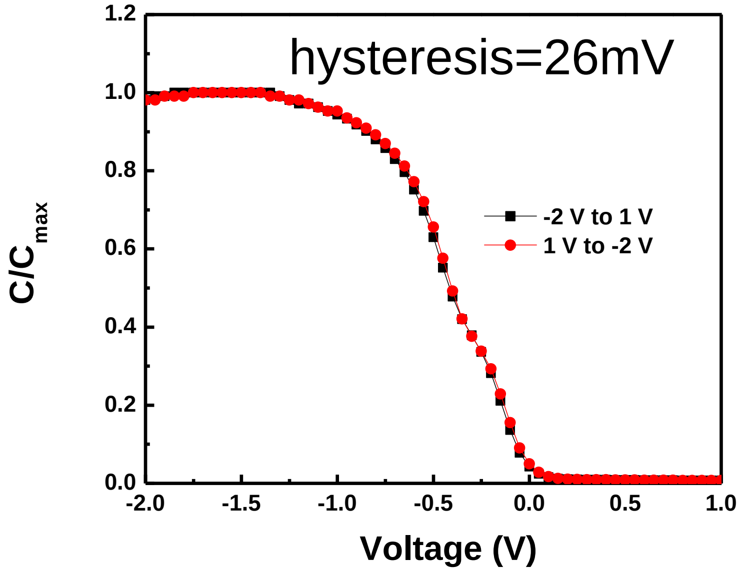


Fig. 4-5 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds and NH_3 plasma 30 seconds

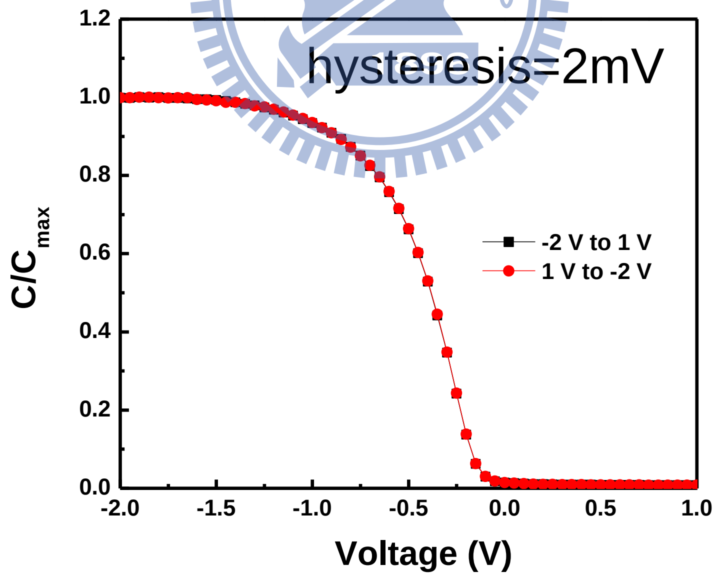


Fig. 4-6 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds and CF_4 plasma 60 seconds

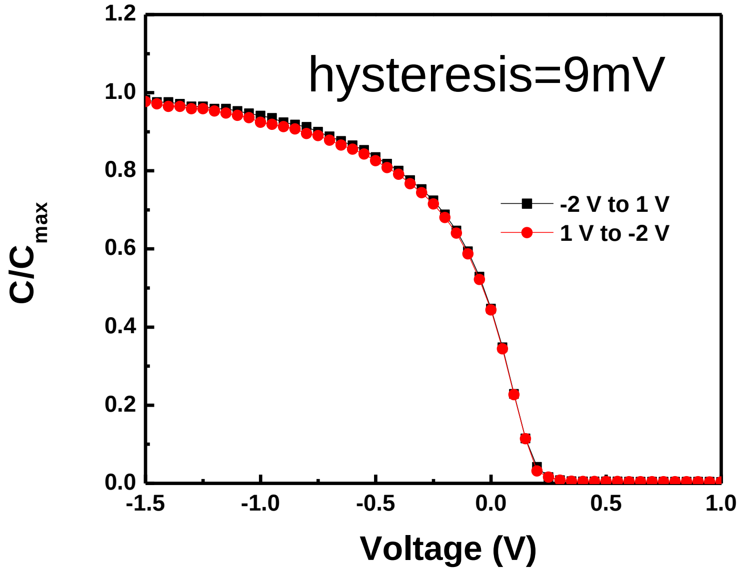


Fig. 4-7 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds and N_2 plasma 60 seconds then CF_4 plasma 60 seconds

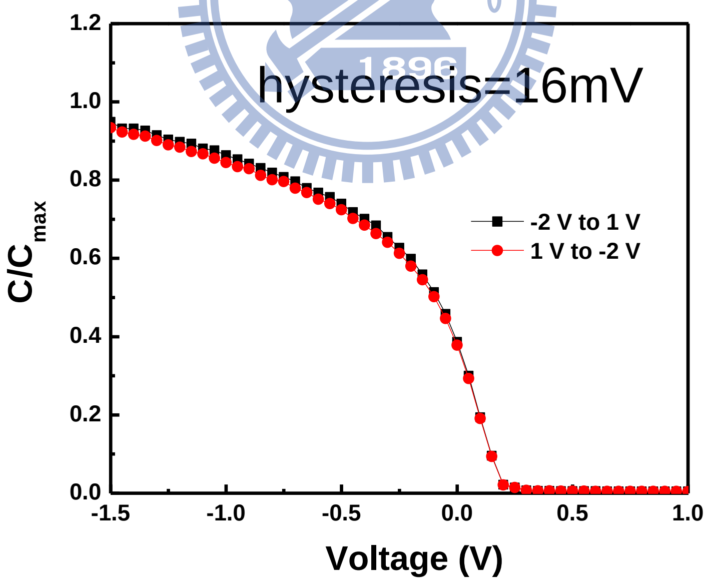


Fig. 4-8 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds and N_2O plasma 60 seconds then CF_4 plasma 60 seconds

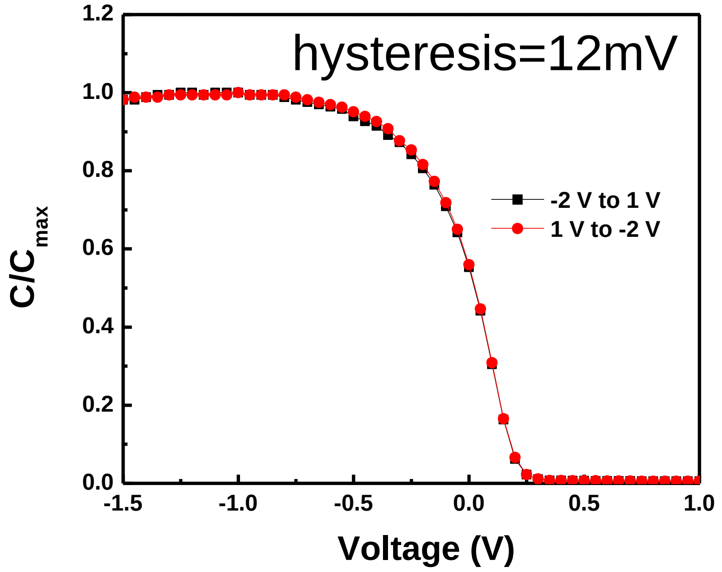


Fig. 4-9 The hysteresis of $HfSiO_x$ gate dielectrics with RTA 500°C 60 seconds and NH_3 plasma 30 seconds then CF_4 plasma 60 seconds

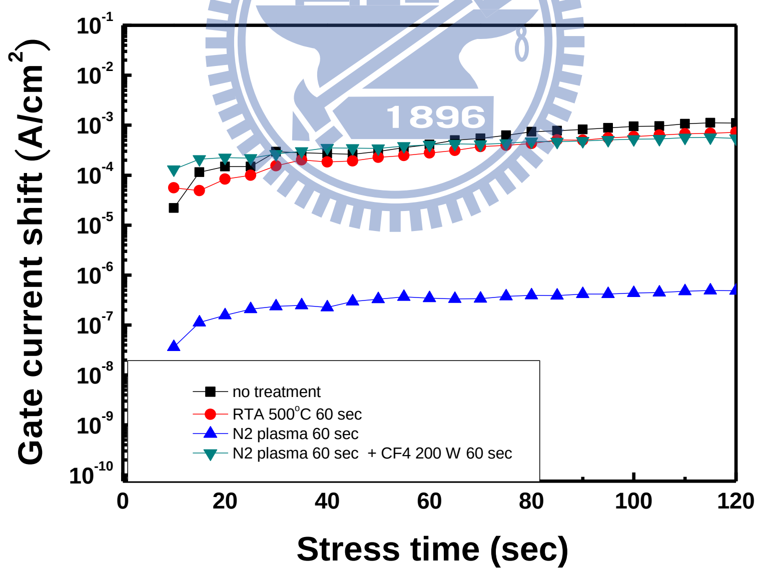


Fig. 4-10 Gate current shift of $HfSiO_x$ gate dielectrics treated with N_2 and CF_4 plasma treatment during Vg = 5V CVS

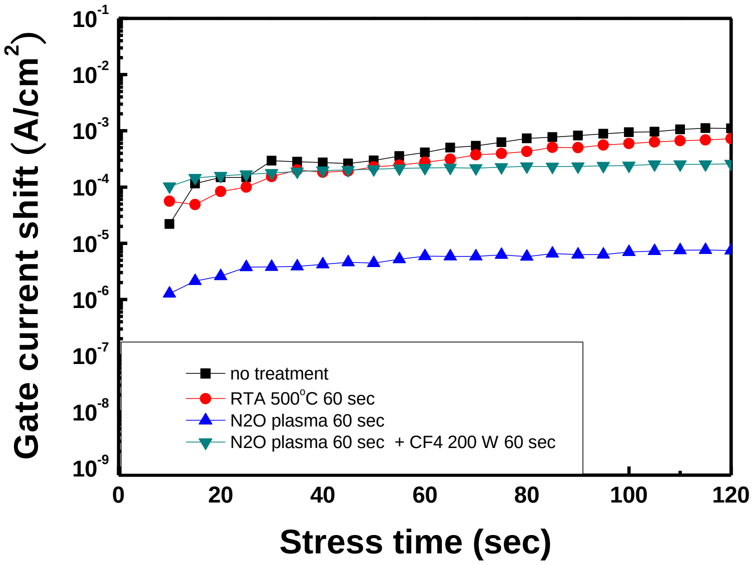


Fig. 4-11 Gate current shift of $HfSiO_x$ gate dielectrics treated with N_2O and CF_4 plasma treatment during Vg = 5V CVS

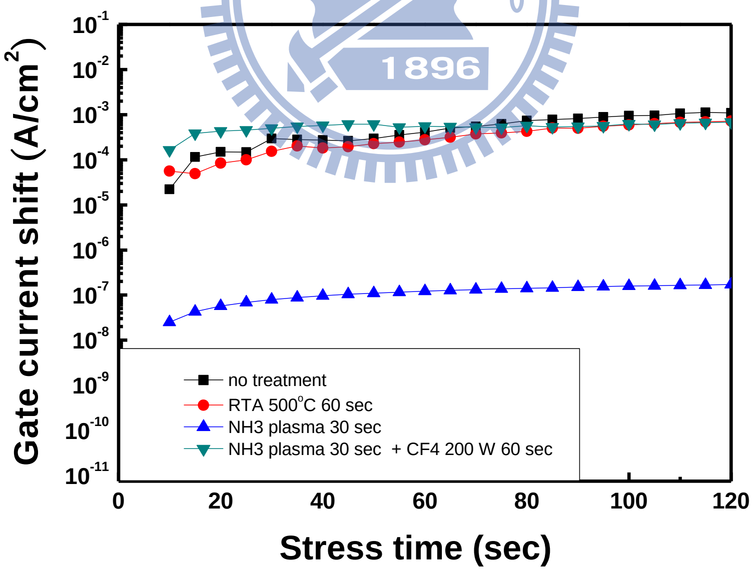


Fig. 4-12 Gate current shift of $HfSiO_x$ gate dielectrics treated with NH_3 and CF_4 plasma treatment during Vg = 5V CVS