國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

提昇多指狀靜電放電保護元件導通均勻度之設計

Design to Enhance Turn-on Uniformity of Multi-Finger ESD Protection Devices

研 究 生：溫 詠 儒 (Yong-Ru Wen)

指導教授：柯 明 道 (Ming-Dou Ker)

中華民國九十八年九月

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ABSTRACT (CHINESE)

隨著製程不斷的演進，積體電路元件的規模也從微米縮小至奈米，同時也伴隨著閘極氧化層的厚度變得越來越薄。此外，為了增加互補式金屬氧化層半導體中積體電路的操作速度，金屬矽化層已是一道非常重要且必備的光罩。而上述這些對積體電路的效能是正面的助益，但是卻對靜電放電(Electrostatic Discharge, ESD)防護耐受度造成嚴重的下降。為了能維持足夠的靜電放電耐受度，在一般積體電路上，靜電放電防護電路是需要加入的。

在靜電放電路徑產生時，為了能讓靜電放電保護元件承受更大的電流，一般會增加
元件的通道寬度，而形成一種多指狀的結構。而在 NMOS 的導通機制中，會有一個電壓突然跳回的點(snapback)，這是由於 NMOS 閘極下有一個寄生的橫向 npn 雙載子接面電晶體，其電流增益(β gain)很大的緣故。而這則會造成多指結構 NMOS 的不均勻導通，使電流集中在先導通的指頭上，因而容易造成燒灼，降低了靜電放電的耐受度。因此，在不斷的增加通道寬度，加大面積下，靜電放電保護能力並不會隨著線性提升。而在我的論文中則會對此不均勻導通的問題提出方法來解決，提出的設計將不需要任何複雜的拉線技巧，也不用外加觸發電路，只需要在元件佈局上做變化即可。第一部份提出的是折彎 N-Well 穩定電阻(bending N-Well ballast resistance)技術，而套用在閘極接地的 NMOS。這設計的概念是用一折彎 N-Well 電阻而避開使用金屬矽化層阻隔(silicide blocked

mask)這層光罩。這設計成功在 55 奈米的 CMOS 製程下實現，相較於傳統的 N-Well 穩定電阻技術，也在較好的靜電放電耐受度下得到驗証。而第二部份提出的是基板隔離(isolated-body)的技巧。因為傳統使金屬矽化層阻隔的多指結構 NMOS 仍有不均勻導通的問題，因此在本論文中對其來做改良。在此設計下，他的基板能看到一樣的基板電阻(substrate resistance)，而有均勻導通的效果。而此設計也在 55 奈米的 CMOS 製程下實現了。和傳統的多指結構 NMOS 以及使用插入源極端短路基底接觸點(source butting substrate contact)的技術相較起來，本論文新提出的基板隔離技巧在實驗結果中能有更小的導通電流，也有更好的靜電放電耐受度。

DESIGN TO ENHANCE TURN-ON UNIFORMITY OF MULTI-FINGER ESD PROTECTION DEVICES

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ABSTRACT (ENGLISH)

While the process evolution from microscale to nanoscale, the device size is continually scaled down, and so does the gate oxide thickness. The silicide process now is a common procedure to improve the operating speed of CMOS ICs. These are positive to the performance of IC chips, but negative to electrostatic discharge (ESD) robustness. To sustain a required ESD robustness in CMOS ICs, the chip should contain ESD protection circuits inside.

In order to discharge enough ESD current as the ESD event occurs, the MOSFET in ESD protection circuit should be drawn in multi-finger layout structure to maintain enough channel width for discharging ESD current. But there is a snapback breakdown phenomenon due to NMOS parasitic lateral bipolar beta gain. This will cause multi-finger non-uniform turn-on issue, degrade the ESD robustness. As a result, the ESD robustness can't increase effectively by increasing the channel width and area of device. The purpose of this thesis is to solve the non-uniform turn-on phenomenon of multi-finger NMOS. The proposed designs use only layout technique to fulfill without external triggering circuit and increase of layout area. The first proposal is bending N-Well ballast resistance technique applied to gate-grounded NMOS (GGNMOS). The design concept is using N-Well resistance without silicide blocked mask, and it has been successfully verified in a 55-nm CMOS process, and the ESD robustness of bending N-Well ballast resistance GGNMOS could be improve

than that of traditional N-Well ballast resistance GGNMOS. The second proposal is the isolated-body technique. Because there is still the non-uniform turn-on issue on traditional silicide blocked multi-finger NMOS, isolated-body is a design to achieve substrate resistance equalization of every finger, it has been realized in a 55-nm CMOS process. The experimental results show that isolated-body structure has smaller trigger current than traditional multi-finger NMOS and inner pickup structure NMOS. The HBM ESD level could also be improved through this design.

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溫　詠　儒
僅誌於竹塹交大
九十八年　九月

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Chapter 1 Introduction

1.1 MOTIVATION

With the process evolution from microscale to nanoscale, the device size is continually scaled down, and so does gate oxcide thickness. The salicided process now is a common procedure to improve the operating speed of CMOS ICs. This is positive to the performance of IC chips, but negative to electrostatic discharge (ESD) robustness. To sustain a required ESD robustness in CMOS ICs, the chip should contain ESD protection circuits inside. The typical ESD level of commercial IC products are 2kV higher in human-bpdy-modal (HBM) ESD test and 200V higher in machine-modal (MM) ESD test. To sustain the required ESD levels, ESD protection devices are often designed with large device dimensions, which are often drawn with the multi-finger layout style to reduce the total occupied silicon area. Typically, multi-finger NMOS devices are widely used as ESD protection structures owing to the effectiveness of parasitic lateral n-p-n BJT in handling high ESD current. However, it has been reported that multi-finger NMOS can not be uniformly turned on under ESD stress [1]-[2]. That is, even if a larger multi-finger NMOS is used as the ESD protection device, uniform conduction of all fingers is hard to achieve, and hence the expected ESD level can not be realized. A isolated body technique to solve the non-uniform turn-on issue of multi-finger gate-grounded NMOS (GGNMOS) is proposed in this thesis, and the design has been successfully verified in a 55-nm CMOS process.

In modern IC process, silicide is a common mask to increase the operation speed of ICs. Although this mask is good for internal IC circuit, it bad for ESD protection circuit. With silicide above diffusion region, once ESD occurs, the current will most flow in the surface, under this situation, it easily burns the oxide under poly. To avoid this phenomenon, silicide blocked is used for solving this problem, but this will cost for a lot of money due to several mask should add in process. So how to block the silicide without the mask of silicide blocked is important topic in nowadays CMOS technology. In this thesis, a bending N-Well ballast technique is proposed to enhance

the ESD robustness of GGNMOS, and the design has been fabricated and verified in a 55-nm CMOS process.

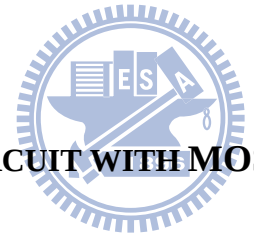
1.2 THESIS ORGANIZATION

To improve the turn-on uniformity of multi-finger ESD protection devices, two designs applied to multi-finger GGNMOS are proposed and discussed in this thesis. This thesis contains five chapters. Chapter 2 introduces the background of ESD event and the turn-on mechanism of NMOS transistors under ESD condition. Then, the mechanism that results in non-uniform turn-on phenomenon of multi-finger NMOS transistors is illustrated. In chapter 3, prior designs of ballast technique without silicide blocked are first reviewed. Then the modified design is proposed to compared with prior designs. New bending N-Well ballast technique is fabricated and verified in a 55-nm CMOS process. The measurement setup and experimental results including the dc characteristics, TLP-*IV* curves, ESD robustness are stated in detail in chapter 3. In chapter 4, the isolated body technique, a method to improve the turn-on uniformity of GGNMOS is proposed and verified in a 55-nm CMOS process. The design concept of isolated body structure is illustrated and then the measurement results including dc characteristics, TLP-*IV* curves, and ESD robustness are stated in detail. In the end of this thesis, a short conclusion and future work are given in the chapter 5.

Chapter 2 Non-Uniform Turn -on Phenomenon in Multi-Finger ESD Protection NMOS

2.1 General Introduction to ESD

The phenomenon of electrostatic discharge (ESD) occurs when an electrostatic voltage slowly develops between an object and its surrounding environment, commonly referred to as earth or ground, then spontaneously discharges as an electrical current impulse [3]. ESD can be brought about by different origins, it can be classified to human-body model (HBM), machine-model (MM), and charged-device model (CDM) according to different discharging methods and sources of electrostatic charges.



2.2 ESD Protection Circuit with MOS Transistors

MOS transistors are the most common ESD protection devices in CMOS ICs. Fig. 2.1 shows the typical design of efficient ESD protection circuits in a CMOS IC to protect the internal circuits against ESD damage [4]. For the input ESD protection circuit, the gates of Mp1/Mn1 are connected to VDD/VSS to avoid interference with the normal circuit operation. While for output ESD protection, because the device size of the output buffer is usually very large, the output PMOS/NMOS (Mp2/Mn2) could be used as self-protection device. To achieve better ESD robustness, VDD-to-VSS power clamped circuit is added between power lines. And the power clamped circuit are realized by an ESD detection circuit and the main ESD protection device (a large size NMOS, Mn3, in this case). The ESD detection circuit can provide a voltage at the gate of Mn3 to help Mn3 turn on more quickly under ESD stress condition, and bias the gate of Mn3 to ground to keep the Mn3 off under normal circuit operation condition.

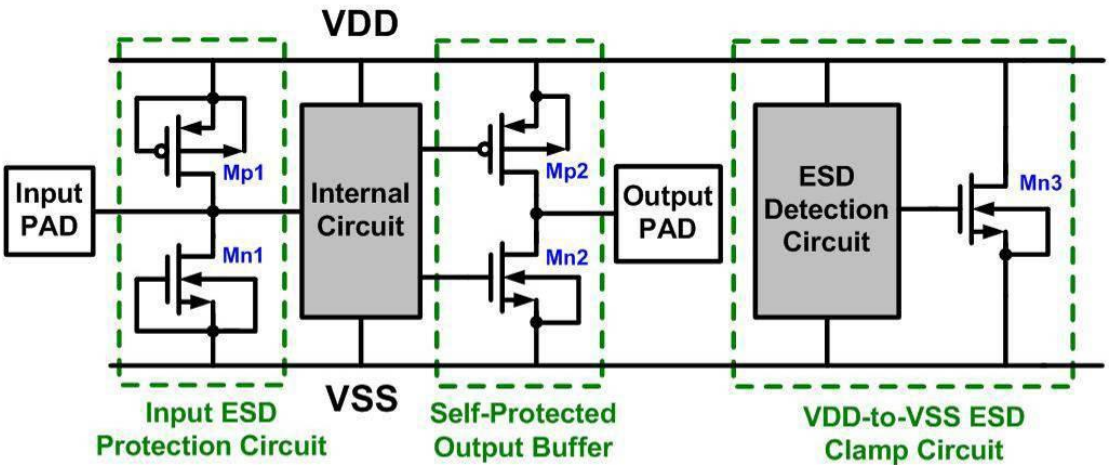


Fig. 2.1 Typical on-chip ESD protection circuit in CMOS ICs.

2.3 TURN-ON MECHANISM OF MOS TRANSISTOR UNDER ESD CONDITION

Under ESD stress conditions the MOS transistor in the ESD path is required to carry amperes of current. The inherent lateral bipolar transistor (BJT) presents in both NMOS and PMOS transistors is triggered on to snapback region to carry such high ESD current, and the mechanisms involve both avalanche breakdown and turn-on of the parasitic lateral BJT. For better comprehension, the following statements concentrate on NMOS transistor. Fig. 2.2(a) depicts the cross section of a NMOS transistor including the parasitic lateral n-p-n BJT and associated currents. The N+ drain junction, P-substrate and the N+ source junction of a NMOS device construct a parasitic lateral n-p-n bipolar transistor. When the high ESD stress voltage occurs, the parasitic n–p-n bipolar junction transistor inherent in NMOS device structure can be turned on to carry the huge ESD current and to clamp down the ESD voltage to protect gate oxide of internal circuits the ESD voltage to protect gate oxide of internal circuits. To illustrate the turn-on mechanism of MOS transistor under ESD condition, a NMOS with gate, source, and substrate at zero potential is considered. The corresponding high current *I-V* curve is shown in Fig. 2.2(b).

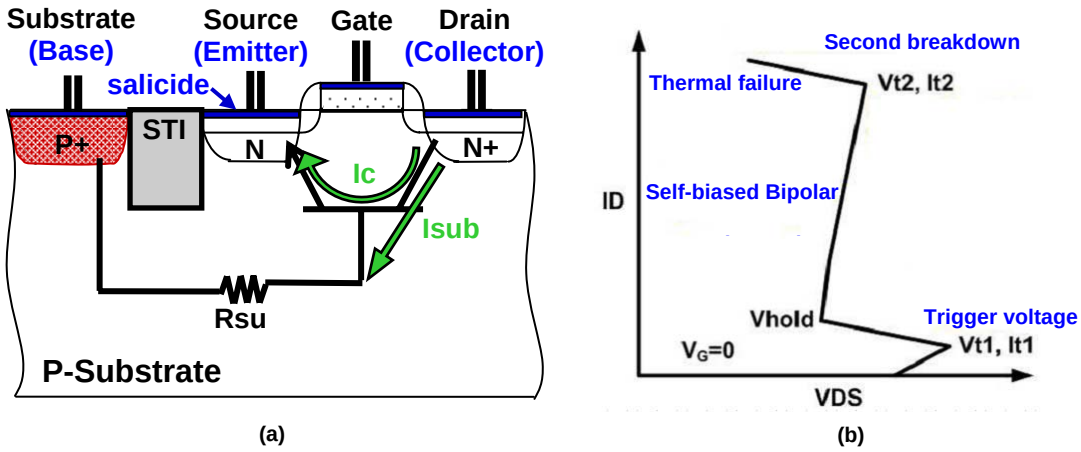


Fig. 2.2 (a) Cross section of an NMOS transistor. (b) High current I-V curve of an NMOS transistor with gate, source, and substrate at zero volts.

As the drain current is increased, the reverse-biased drain-substrate junction is initially in high impedance. The only current is the reverse current at the drain-substrate junction. Eventually the drain-substrate junction begins to avalanche due to the high voltage across it, and electron-hole pairs are generated. The electrons are swept across the drain junction towards the drain contact, adding to the drain current, while the holes drifts towards the substrate contact giving rise to a substrate current, Isub. As Isub increases, the potential at the source-substrate junction increases and forward biases this junction. Then the parasitic LBJT can be considered to be turned on. In Fig. 2.2(b), Vt1 is the trigger voltage of the parasitic BJT and the trigger current is It1. The above-mentioned is effectively self-biased bipolar operation, since the bias current is generated by the intrinsic avalanching at the drain-substrate junction. Once the parasitic lateral BJT turns on, the drain voltage decreases and a negative resistance is observed due to the availability of more carriers for multiplication until a minimum voltage, called snapback holding voltage (Vhold), is reached. The *I-V* curve now show a positive resistance as further increase in the injected current results in conductivity modulation of the substrate region that reduces the intrinsic substrate resistance. A higher Isub is required to maintain the transistor in the on-state. Finally, the parasitic BJT will be permanent damaged due to thermal failure, and the failure current/voltage level is called second breakdown current (It2)/voltage (Vt2).

2.4 SNAPBACK CHARACTERISTICS OF NMOS AND PMOS TRANSISTORS

NMOS transistor have obvious snapback characteristic, while the snapback of PMOS transistor is unobvious. Besides, the trigger current of PMOS is much larger than that of NMOS. It is because that the current gain of p-n-p bipolar junction transistor in CMOS process is much smaller than that of n-p-n bipolar junction transistor; thus the *I-V* curve of PMOS under ESD stresses usually have no, or weak, snapback phenomenon. Because the snapback holding voltage and trigger voltage of PMOS is nearly the same, any finger breakdown would not clamp the pad to a low voltage, thus multi-finger PMOS can be turned on uniformly under ESD condition. On the other hand, if any finger is turned on first in multi-finger NMOS, the pad would be clamped to the low snapback holding voltage and prevent other fingers from being turned on, and results in non-uniform turn-on issue of multi-finger NMOS. Therefore, in this thesis, the work is concentrated on improving the turn-on uniformity of multi-finger NMOS transistors.

2.5 MECHANISM OF NON-UNIFORM TURN-ON PHENOMENON IN NMOS

There are two main causes of non-uniform turn-on issue in multi-finger NMOS transistor. One is the obvious snapback characteristic of NMOS device, the other is the layout geometry effect on the distributed substrate resistance of the n-p-n bipolar transistor. Fig. 2.3 shows the layout and cross-sectional view of traditional multi-finger NMOS. In the multi-finger NMOS structure with P+ guard ring surrounding it, due to the different distances from the base regions of each parasitic lateral n-p-n BJT to the substrate guard ring, the base resistance of parasitic lateral n-p-n BJT in the central region of the multi-finger NMOS is higher than those in the side regions. Therefore, in the multi-finger NMOS structure, the center NMOS fingers are always triggered on faster than the others under ESD stress. As long as the center NMOS fingers are triggered on, the ESD overstress voltage is clamped to the snapback holding voltage of NMOS. Moreover, if the secondary breakdown voltage (Vt2) of NMOS is smaller than its trigger voltage (Vt1), the other non-turned-on NMOS fingers in the side region cannot be triggered on before the first turned-on NMOS fingers are burned out [5].

Therefore, the ESD current will be only discharged through some local regions. The current are concentrated on the central regions of multi-finger gate-grounded NMOS, indicating the occurrence of non-uniform turn-on phenomenon.

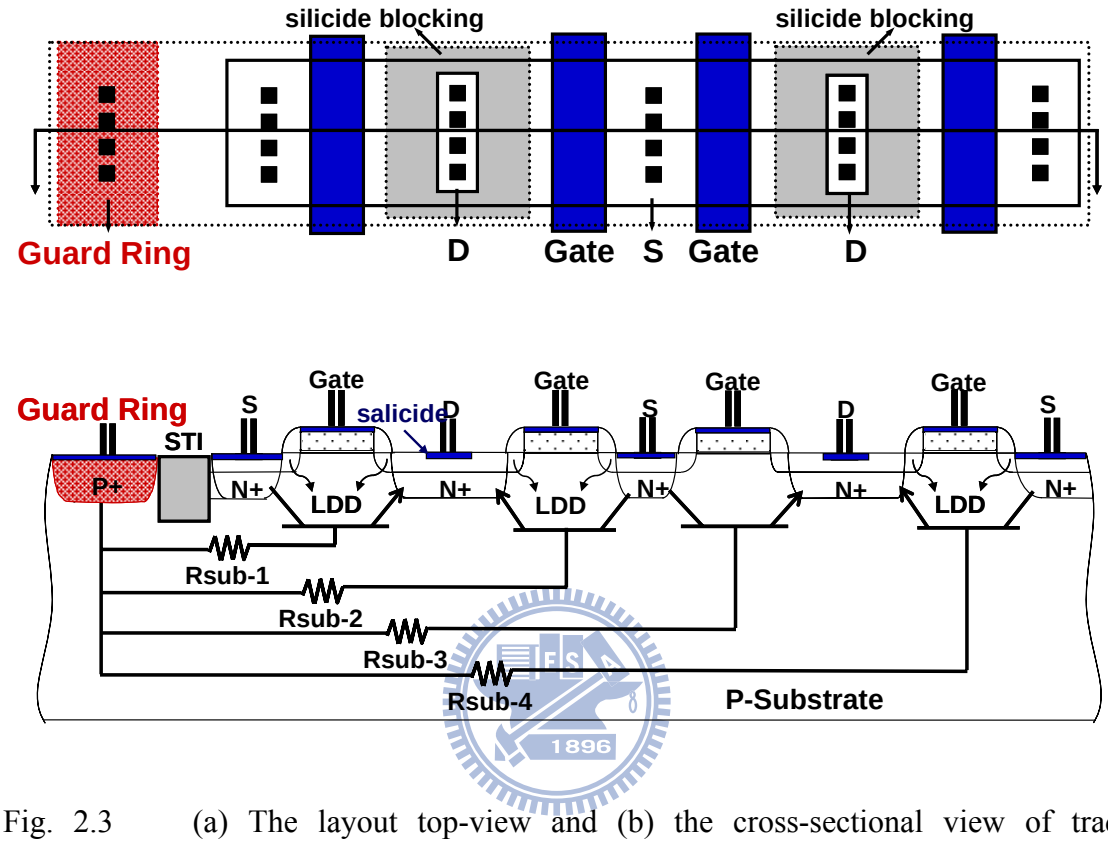


Fig. 2.3 (a) The layout top-view and (b) the cross-sectional view of traditional multi-finger gate-grounded NMOS, indicating that the central parasitic lateral BJTs have larger substrate resistance due to layout geometry.

Therefore, ESD robustness of multi-finger NMOS cannot be efficiently increased by increasing the device dimension due to non-uniform turn-on issue. To solve this problem, some circuit designs such as gate-coupled or substrate-triggered techniques have been proposed to reduce the trigger voltage (Vt1) of NMOS for improving the turn-on uniformity of multi-finger NMOS. In this thesis, the designs of isolated body technique and bending N-Well ballast technique are proposed to enhance turn-on uniformity of large-size NMOS devices.

Chapter 3
Ballast Resistance Technique to Enhance ESD Robustness of GGNMOS

3.1 PRIOR DESIGNS OF BALLAST RESISTANCE TECHNIQUE ON GGNMOS

3.1.1 Layout Skill

To sustain high ESD robustness, the ESD protection device is always drawn in multi-finger structure which possesses effective long channel length and less layout area. In the process of nowadays, salicided process is a necessary process to enhance operation speed of CMOS ICs. Unfortunately, the current will flow on surface with salicided process, this phenomenon limits the available volume for heat dissipation, results in low ESD robustness. As a result, the salicided blocked mask is essential and useful for ESD protection circuit [6], but useless for internal circuit. So the salicided blocked mask is another cost for whole process. Fig. 3.1 shows the top and the cross-section view of NMOS with salicided blocked mask [7]. (The drain, poly gate and source of the MOSFET are all covered by salicided blocked.)

ESD protection device, as implied by the name, it should discharge the sudden current to prevent damage on internal circuit. So the foundry would confine the metal width, channel length, distance from drain contact to poly gate edge of the ESD protection device in a range to guarantee enough capacity for discharging ESD current.

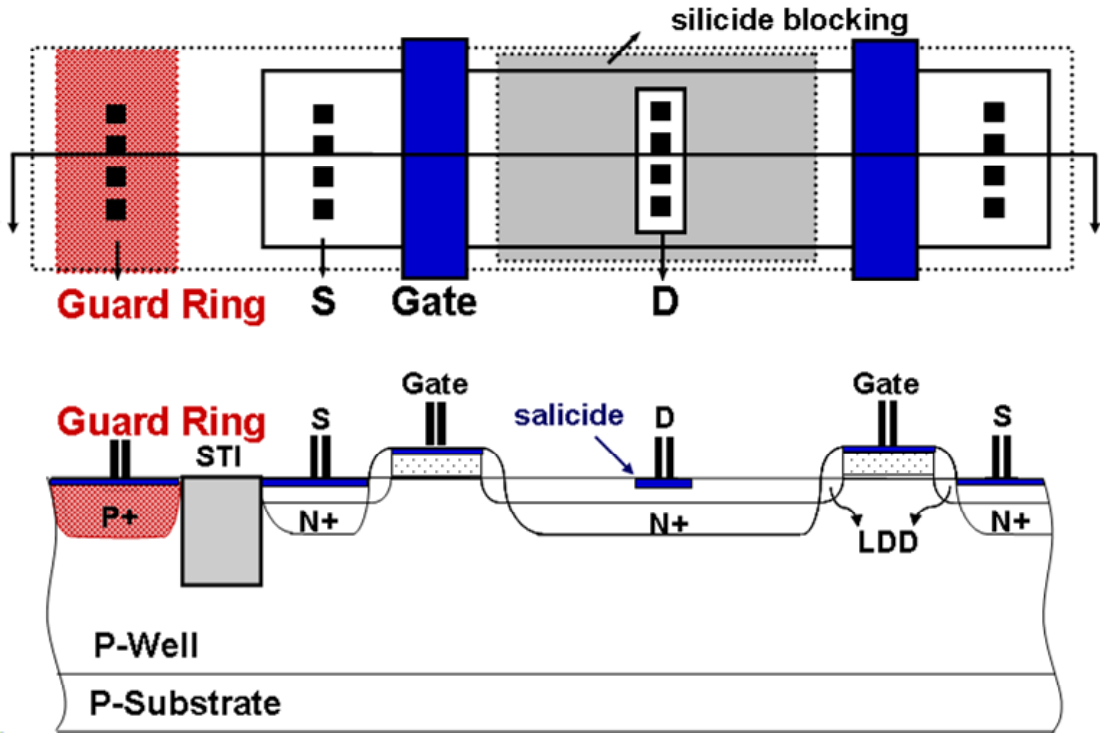


Fig. 3.1 The layout top-view and the cross-sectional view of the traditional silicide blocked NMOS.

3.1.2 Flouting Poly Array Ballast Technique

Cause salicided blocked mask is another cost for whole process, so it's better if the ESD protection device should maintain high ESD robustness and use fully salicide process without salicided blocked mask. The Fig. 3.2 shows top layout view and cross-section view of an NMOS structure with the flouting poly array (FPA) at the drain side [8]. The drain and source n+ diffusion regions are separated by the poly gates as well as the channel underneath the poly gates. As shown in Fig. 3.3, three rows of FPAs, each has a poly-silicon segment over a gate oxide layer, are distributed in the drain diffusion region. FPAs provide not only the ballast resistance for drain side region,

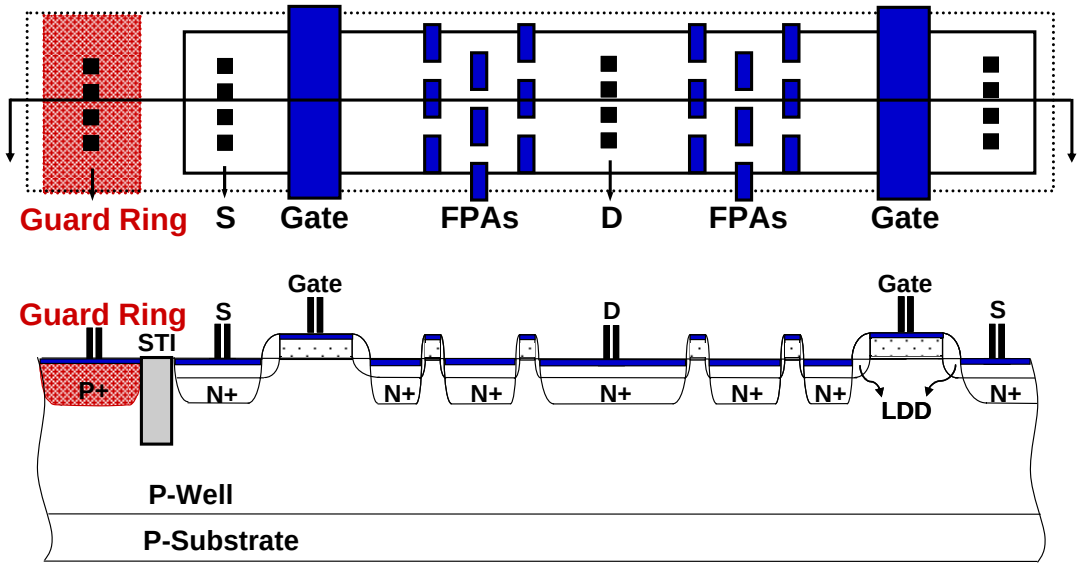


Fig. 3.2 The layout top-view and the cross-sectional view of the flouting poly arrays structure.

also the combined GIDL-related band-to-band tunneling and impact ionization mechanisms at the poly-to-drain overlapping regions near the periphery of the FPAs. And the experiment result of FPAs GGNMOS shows that the ESD level is approaching saliciede blocked GGNMOS.

This structure uses a common process, which is poly gate as ballast resistance to realize high ESD robustness under fully salicide.

3.1.3 N-Well Ballast Resistance Technique

In fully salicided CMOS technology, as compared with the flouting poly array structure, N-Well ballast resistance technique is using the N-Well resistor as ballast resistance at drain side [9], thus increasing the ESD robustness and turn-on uniformity of multi-finger. Fig. 3.3 and fig. 3.4 shows the cross-section view of the N-Well ballast resistance NMOS. It uses STI to block the salicide and n+ diffusion at drain

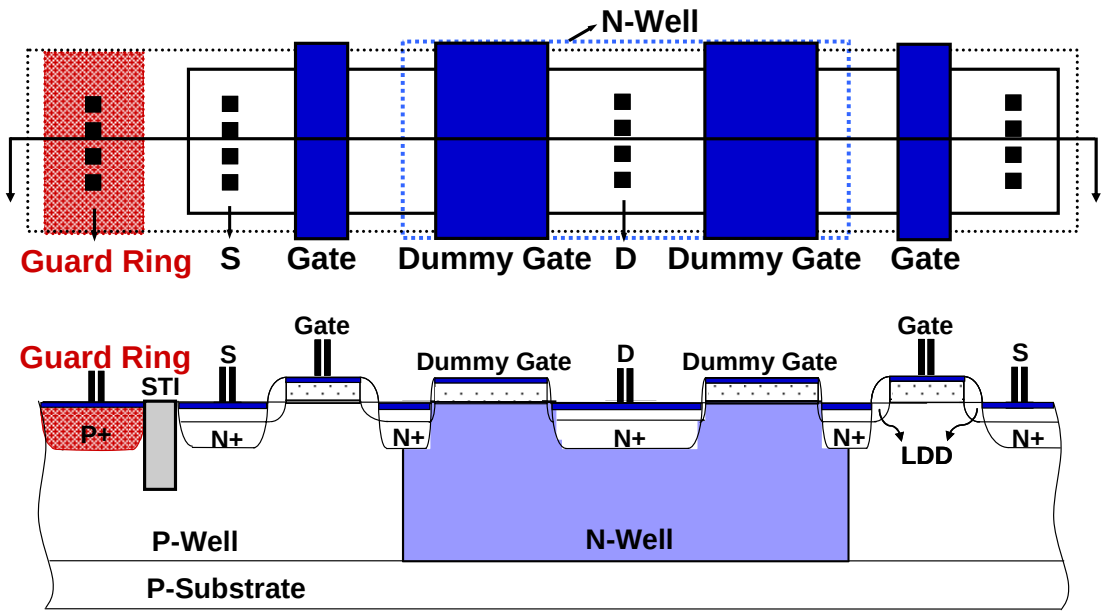


Fig. 3.3 The layout top-view and the cross-sectional view of the N-Well ballast resistance technique with dummy gate.

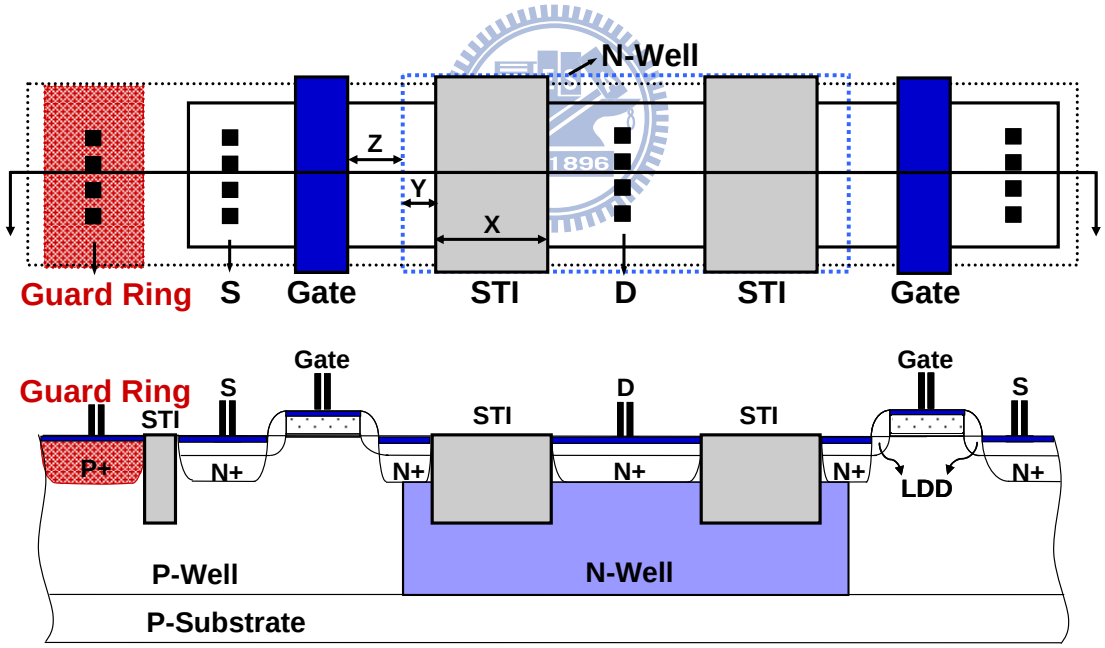


Fig. 3.4 The layout top-view and the cross-sectional view of the N-Well ballast resistance technique with STI.

side, which is enclosed by N-Well to increase ballast resistor, and fig. 3.4 uses dummy gate to take place of STI. Without extra process steps, these two structures of NMOS both could block salicide above drain side diffusion,

increase ballast resistance and sustain higher ESD robustness than traditional fully salicide NMOS.

3.1.4 Active Area Segmentation Technique

With the same purpose as the following prior designs, active area segmentation (AAS) technique [10] uses no extra ballast resistor as N-Well resistor, only segmenting the active area of drain and source regions. The idea of this structure is from the back-end-ballast (BEB) technique [11], which takes use of poly-gate as ballast resistor to enhance ESD robustness. Fig. 3.5 shows the layout view and cross-section view of BEB structure. The poly resistor and contact/via chain segment the current path between the PAD metal and the drain side active silicided area. By adding series resistance in every segment, the current uniformity within the finger is improved and at the same time the dynamic on-resistance is increased facilitating the trigger of multiple fingers through Vt2 increase above Vt1. Crucial is that this segmentation results in a current homogenizing mechanism defocusing the current at the onset of current crowding and resulting in a stable single finger ESD performance (Fig. 3.6).

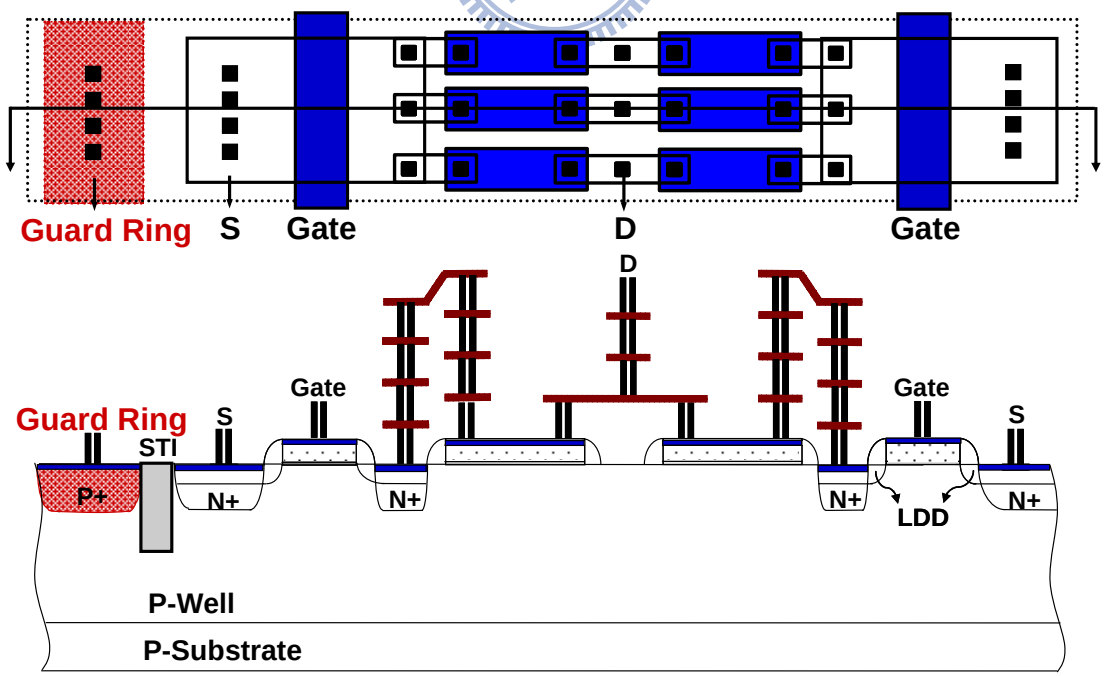


Fig. 3.5 The layout top-view and the cross-sectional view of the back-end-ballast structure.

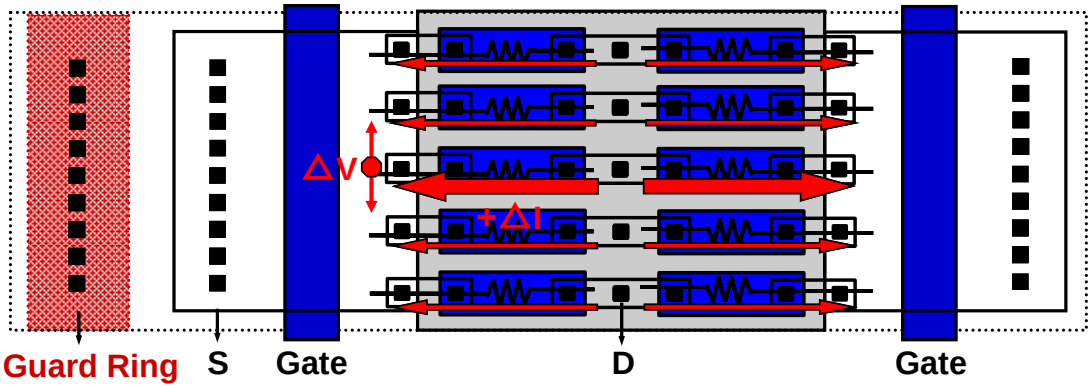


Fig. 3.6 The effect of current de-focusing.

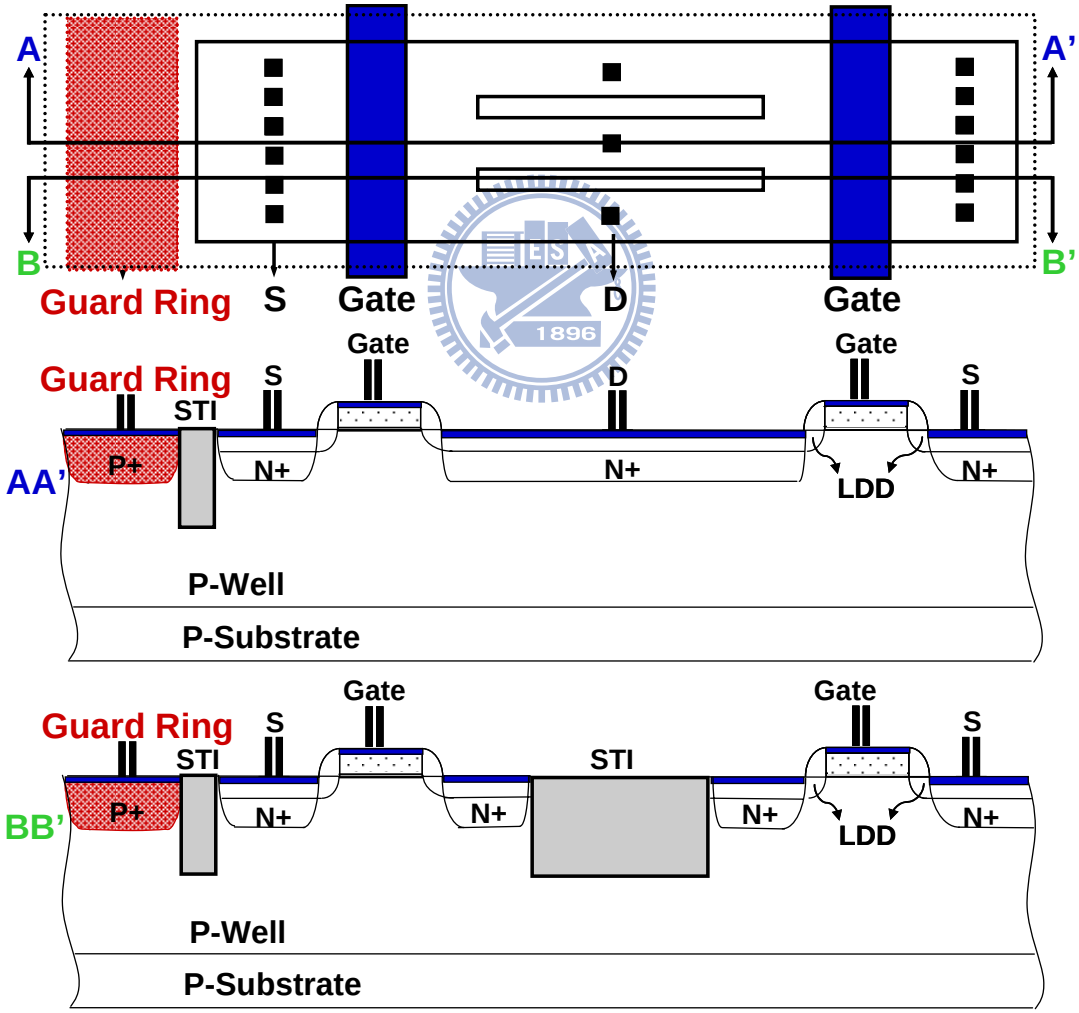


Fig. 3.7 The layout top-view and the cross-sectional view of the active area segmentation structure.

In a similar design technique with BEB technique, AAS structure applies small silicided N+ active area for ballast segmentation instead of silicided poly (Fig. 3.7). The same micro ballasting and de-focusing mechanisms works as for the BEB approach, however, for AAS mostly the contact (~10-15 Ohm) contributes to the ballasting resistance. Moreover, AAS can be implemented in an extremely compact way close to minimum feature size still maintaining functional fingers. After all, the AAS technique basically takes a standard MOSFET layout without any drain resistor and inserts slots in both the drain and source diffusions.

3.1.5 Staggered and Segmented Technique

Continually, another technique based on AAS structure named staggered and segmented (SS) technique provides ballasting with reduced layout area [12]. As shown in Fig. 3.8, different from AAS structure, diffusion segmentations are staggered on SS structure, this arrangement endure higher ESD robustness in smaller layout area. And Fig. 3.9 show the shows the layout view and cross-section view of SS structure.

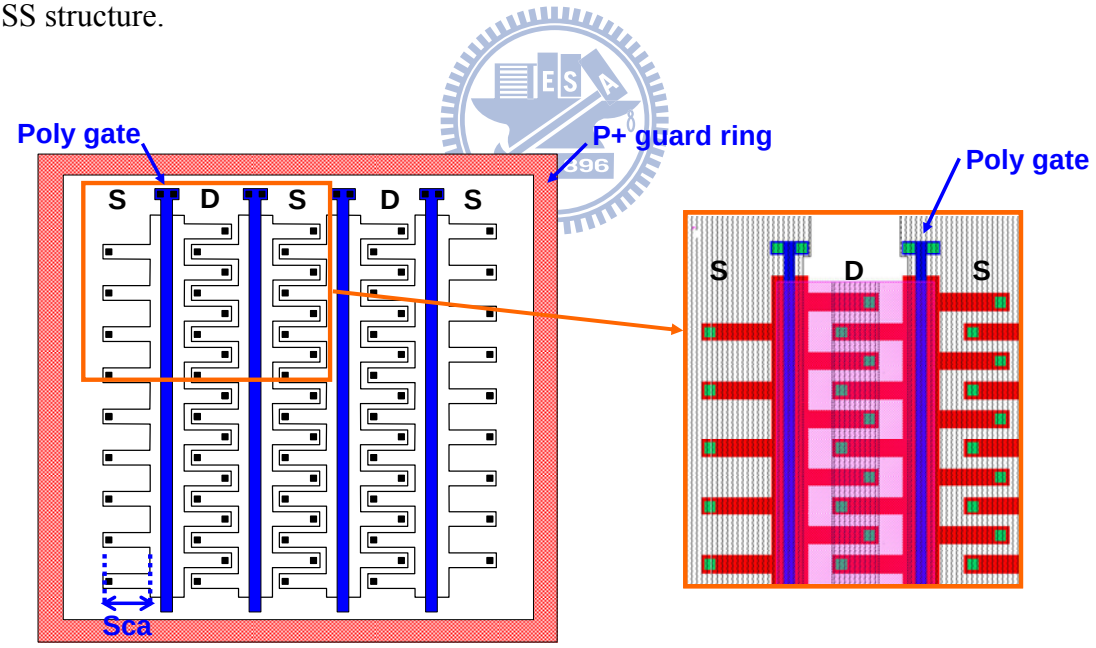


Fig. 3.8 The layout top-view and the local zoom-in view of the staggered and segmented structure.

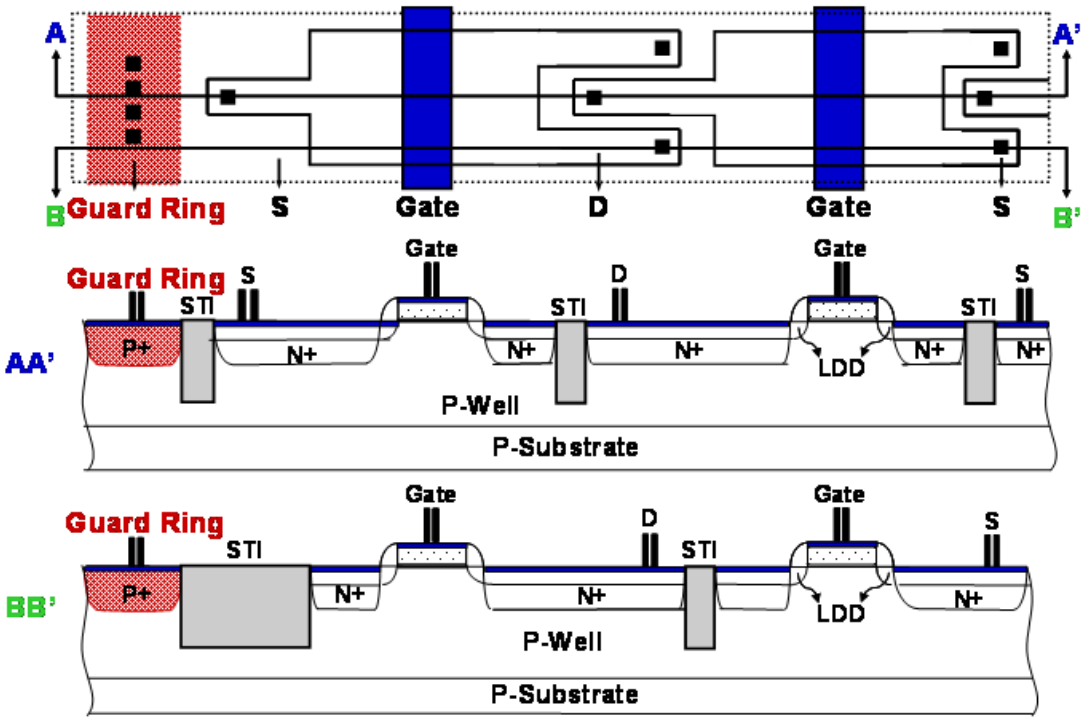


Fig. 3.9 The layout top-view and the cross-sectional view of the staggered and segmented structure.

3.2 MODIFIED DESIGN OF BALLAST RESISTANCE TECHNIQUE

At the prior design of staggered and segmented (SS) technique, the shape of diffusion region is very thin, this has no enough capacity for heat dissipation, causing serious contact spiking, and a low MM ESD level. At my modified design, there's N-Well under each drain contact to prevent contact spiking effect. At Table 3.1, compared with traditional silicide blocked NMOS, the It2 and HBM ESD level of SS structure and its modified design both have a high value, but SS structure has a low MM ESD level. In my modified design, the contact spiking effect is solved from the additional N-Well under drain side contact, and it has a high MM ESD level.

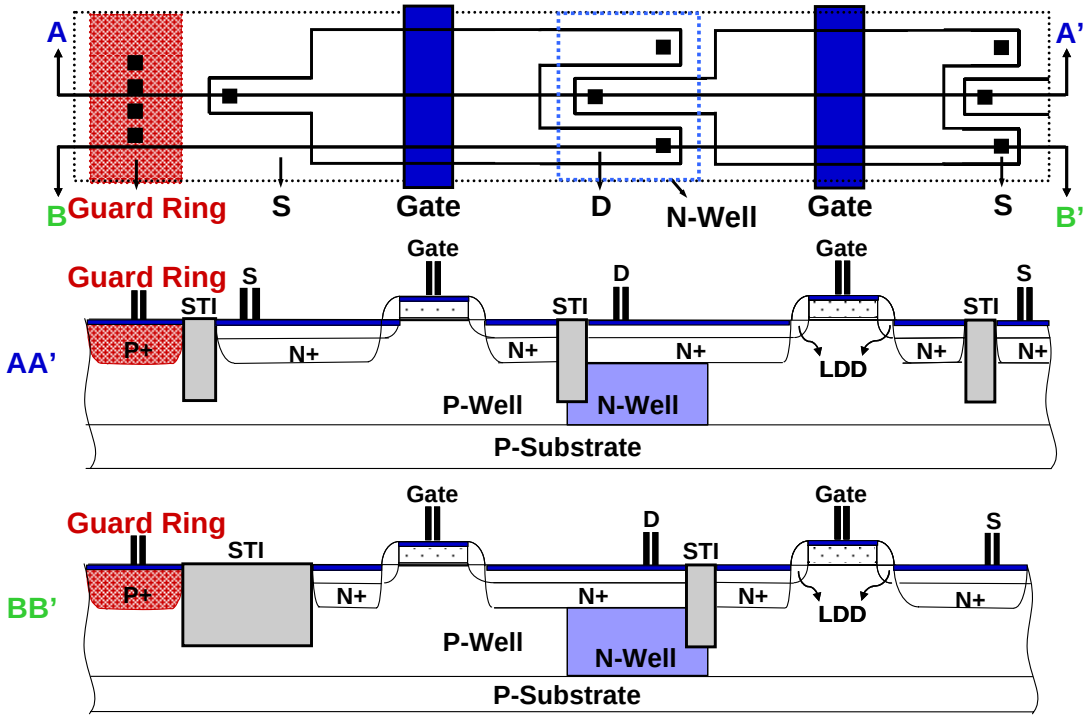


Fig. 3.10 The layout top-view and the cross-sectional view of the modified design staggered and segmented structure.

MOS type		Silicide Blocked	It2 (A)	HBM (kV)	MM (V)	W/L (μm/μm)	Area (μm^2)	It2/Area ($mA/\mu m^2$)
Traditional Silicide Blocked NMOS		Yes	1.29	2.8	125	240/0.12	1127	1.14
SSD NMOS	Scg=1.0μm	No	1.61	3.0	75	240/0.12	806	1.99
	Scg=1.5μm	No	1.45	3.0	75	240/0.12	978	1.49
	Scg=2.0μm	No	1.45	3.0	75	240/0.12	1149	1.26
SSD NMOS with N-Well	Scg=1.0μm	No	1.44	3.0	150	240/0.12	806	1.79
	Scg=1.5μm	No	1.59	3.0	150	240/0.12	978	1.62
	Scg=2.0μm	No	1.53	3.0	150	240/0.12	1149	1.33

Table 3.1 The second breakdown current, ESD level and second breakdown current per area of traditional silicide blocked NMOS, staggered and segmented structure, and its modified design.

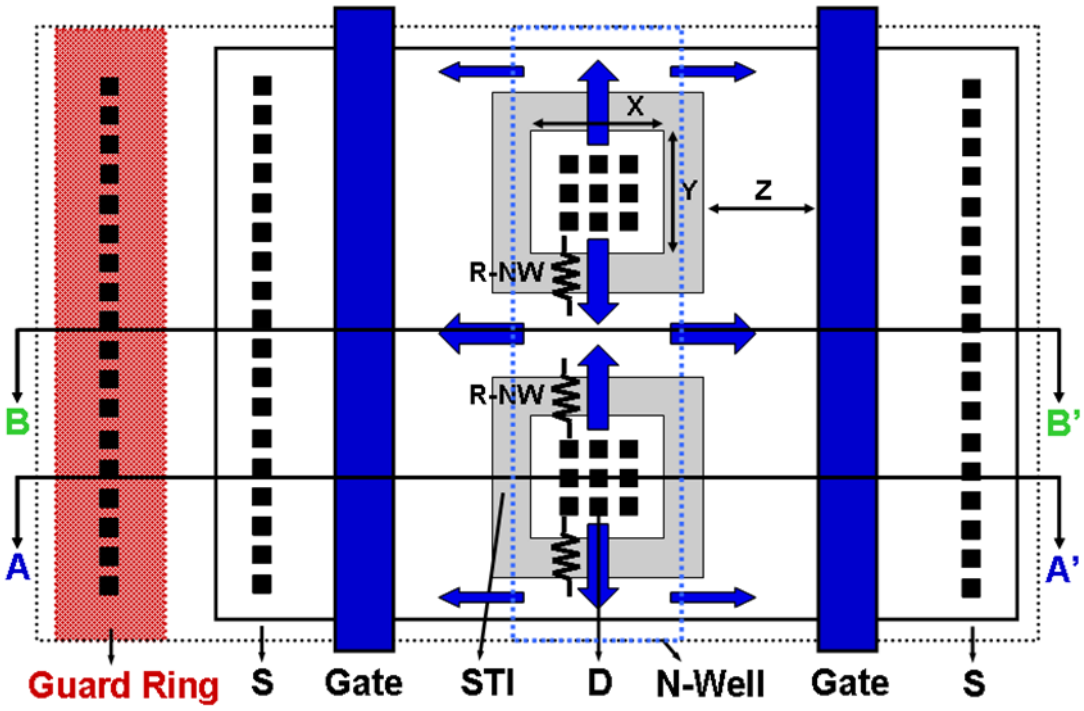
3.3 BENDING N-WELL BALLAST RESISTANCE TECHNIQUE

Under these prior designs for current ballasting of ESD protection device, a proposed design named bending N-Well ballast resistance (BNW) technique is shown in Fig. 3.11. This design is based on N-Well ballast resistance technique but drawn in a compact way. Fig. 3.11(a) and (b) show the layout top view and cross-section view of BNW_GGNMOS. At AA' cross-section, the drain side N-Well ballast resistance is perpendicular to the effective NMOS channel, and isolated from the active area which is adjacent to poly-gate. Until at BB' cross-section, the N-Well connects to active area, the collector of parasitic bipolar. Diverge from traditional contact arrangement of MOS structure, drain side contacts are arranged in array within a square and isolated active area region in BNW structure. Due to conversation of charge, the contact amount of drain and source side should be equal, so how much contacts are inside the single drain side island and how much is the area of the island must be considered.

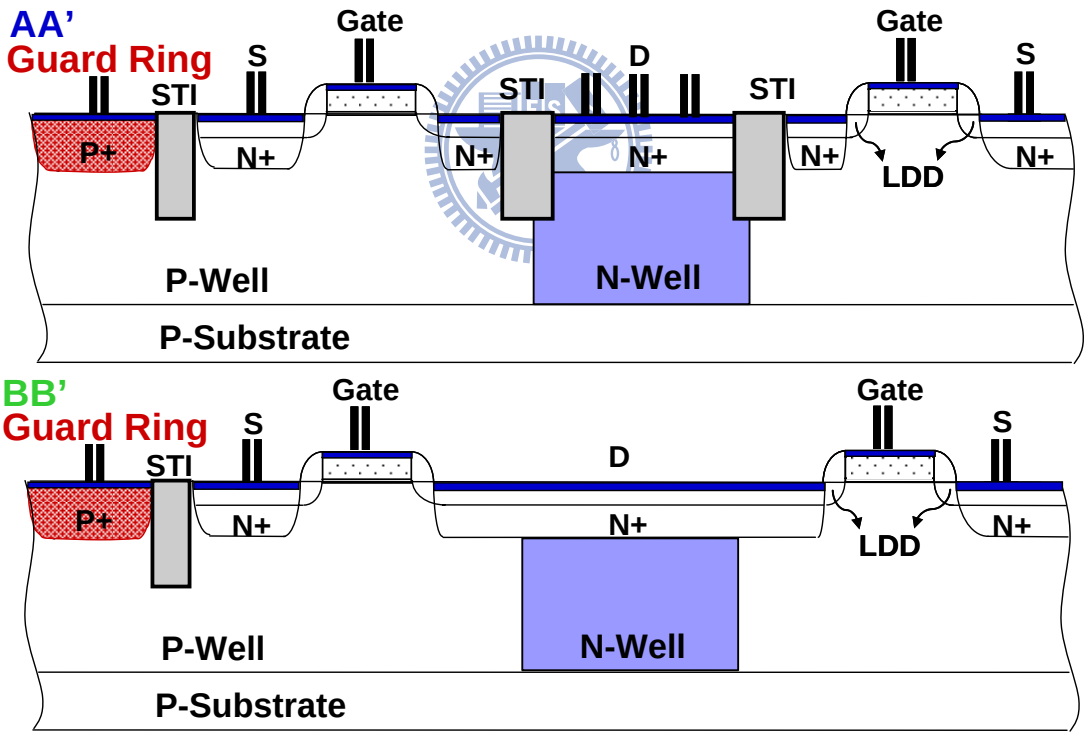
With same ballasting route as N-Well ballast resistance technique, BNW structure can be drawn in a smaller layout area, but possessions of identical mechanism as it. The distance from drain contact to poly-gate edge (Dcg) can clearly tell the difference between BNW technique and traditional N-Well ballast resistance technique. In UMC 55-nm CMOS process's minimum scale foundry rule, the Dcg of N-Well ballast resistance structure is 2.38 m, but it's only 1.91 m of BNW structure. And the layout area of N-Well ballast resistance structure is 1404 m^2, and it's 1540 m^2 of BNW structure.

Otherwise, BNW technique has de-focusing mechanism like AAS technique as well. Between two adjacent BB' cross-sections, it applies small silicided N+ active area for ballast segmentation to enhance turn-on uniformity of multi-finger NMOS.

With the same purpose of the prior designs which is compatible to fully salicide CMOS processes without any additional mask and external triggering circuits, BNW technique contains both AAS and N-Well ballast resistance technique, enhances turn-on uniformity of multi-finger NMOS and ESD robustness, and realizes on condition of no increasing layout area.



(a)



(b)

Fig. 3.11 (a) The layout top-view and the (b) cross-sectional view of the banding N-Well ballast resistance structure.

3.4 EXPERIMENTAL RESULTS AND DISCUSSION

3.4.1 TLP Measurement Results

The TLP system provides a single and continually-increasing-amplitude pulse to the device under test, the pulse width is as short as 100ns to simulate the ESD condition. By using the TLP measurement, the snapback characteristics and the secondary breakdown currents (It2) of the devices can be investigated. It2 is the index for HBM ESD robustness, which is indicated as the corresponding current when the leakage current under the voltage bias of 1.0V is above 1μA in this work. The relation between It2 and HBM ESD level (VESD) can be approximated as VESD ≅ It2×1.5kΩ, where 1.5kΩ is the equivalent resistance of human body.

Fig. 3.12 shows the TLP I-V curve of traditional N-Well GGNMOS and the bending N-Well ballast resistance GGNMOS in 55nm CMOS process. The It2 of traditional N-Well ballast resistance is only 0.443A, which is smaller than the new proposed bending N-Well ballast resistance. Different from the silicide blocked or the staggered and segmentated structure, using the N-Well resistance as ballast resistance will provide a huge drain resistance on the current path, this cause the turn-on resistance is larger than traditional silicide blocked GGNMOS. And there is a second snapback at the point about 10V, this phenomenon doesn't show up in the prior designs, it would explain in 3.4.2 characteristics of the BNW_GGNMOS.

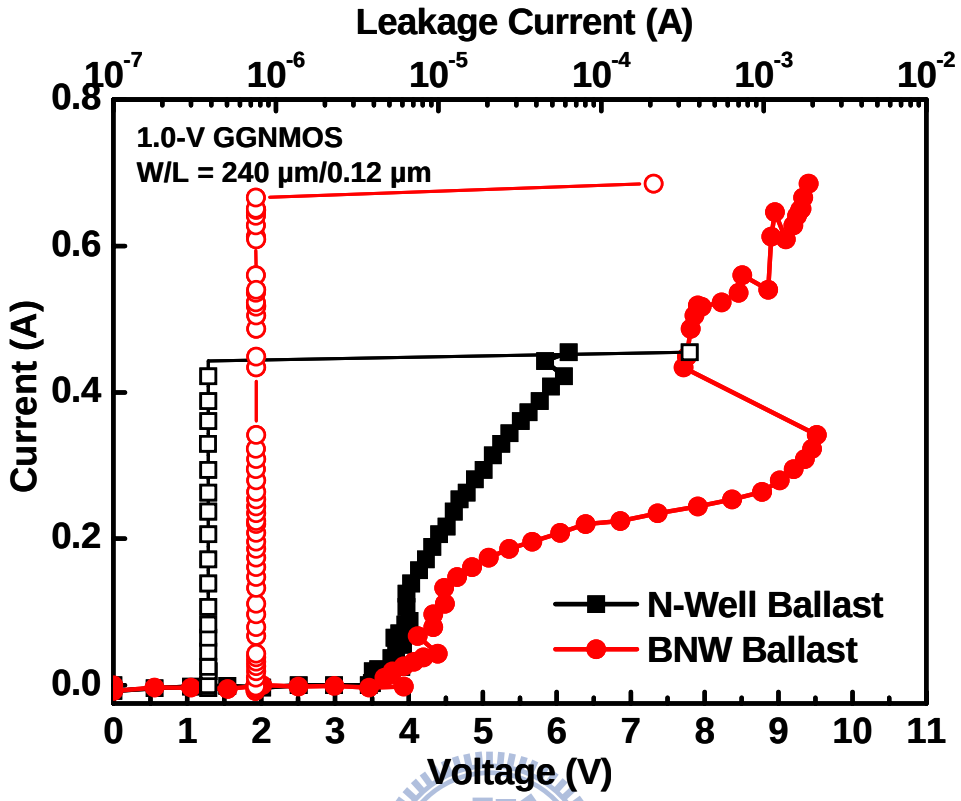


Fig. 3.12 The TLP-measured I-V curves of the traditional N-Well GGNMOS and the bending N-Well ballast resistance GGNMOS in 55nm CMOS process under the drain voltage bias of 1.0V.

3.4.2 Characteristics of the BNW_GGNMOS

N-Well to P-Well junction breakdown is the reason how SCR turn-on, and its breakdown is about 10V. The same breakdown mechanism happens in BNW structure. While the TLP pulse raise step by step, the first turn-on route is N+ to P-sub breakdown, and enter the bipolar operation region. But there is a huge N-Well resistance tied to the drain, which contributes a huge turn-on resistance on the ESD route. As voltage is large enough to supply the N-Well to P-Well junction breakdown, the second snapback happens. Fig. 3.13 shows the current route of BNW structure under ESD stress. As these two routes turned on, the turn on resistance will reduce because of series of resistances in the two routes. Therefore, BNW structure could provide better ESD robustness than traditional N-Well ballast resistance structure.

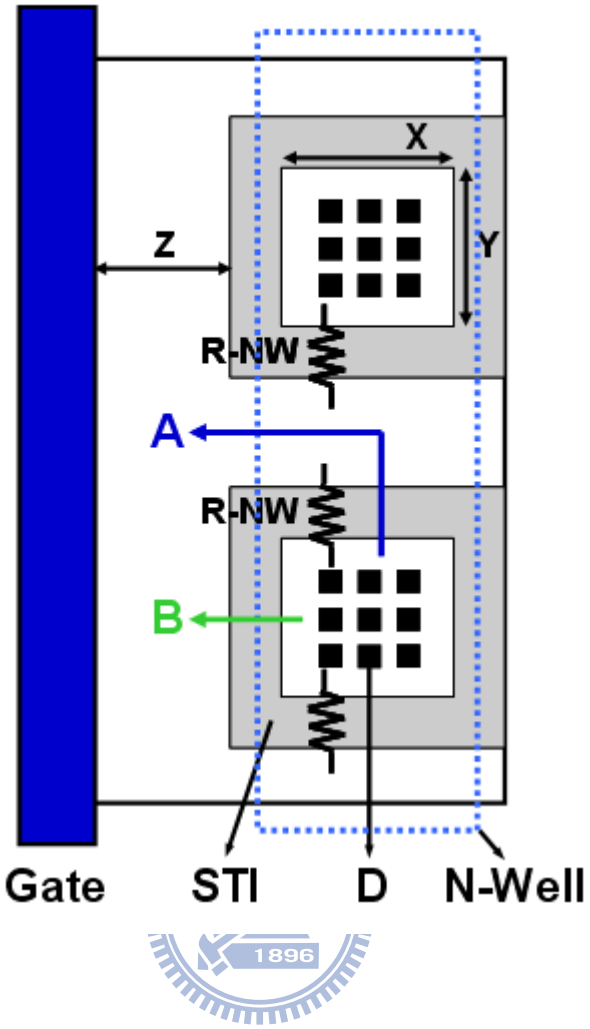


Fig. 3.13 The current route of BNW structure under ESD stress.

3.4.3 ESD Robustness

The HBM and MM ESD stresses are applied to the ESD protection devices to verify their ESD robustness. In these ESD verifications, the devices are tested under the positive-to-VSS ESD stress, and the failure criterion is defined as the measured voltage at the current level of 1μA shifted 30% from its original value. The comparison of the ESD levels between the traditional N-Well ballast resistance GGNMOS and the BNW_GGNMOS is shown in Table 3.2 The different arrangement is to optimize the drain side contact form, and the total number of drain side contact is changed with different arrangement., The number of drain side contact get more as the product of contact arrangement increase, and comes the better ESD level, too. And the parameter Z, the spacing between drain side island to poly gate, is also the crucial tern on the effect of ESD robustness.

Contact Array	X (μm)	Y (μm)	Z (μm)	It2(A)	HBM (kV)	Area (μm²)	It2/Area (mA/μm²)
N-Well Structure	0.55	1	0.3	0.44	0.8	1404	0.32
6x3	1.32	0.6	1.91	0.67	1.8	1540	0.43
6x5	1.32	1.08	1.91	0.73	2.4	1540	0.47
12x3	2.28	0.6	0.89	0.70	2.2	1540	0.46
12x3	2.28	0.6	1.61	0.93	2.8	1791	0.52
12x3	2.28	0.6	2.33	1.15	3.2	2027	0.57

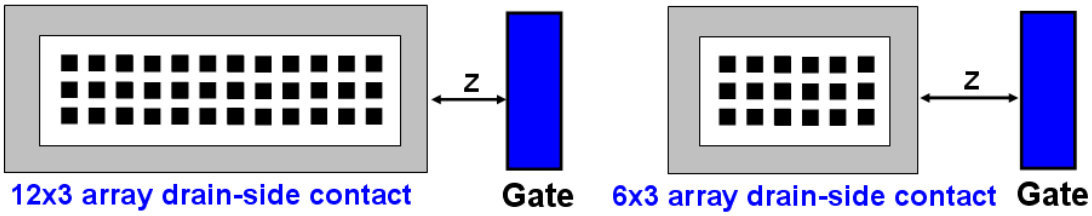


Table 3.2 The different arrangement of drain side island contact with It2, HBM ESD level, and It2 per area.

3.5 Conclusion

To improve the ESD robustness in fully-silicide, a bending N-Well ballast resistance technique has been designed and verified in a 55-nm CMOS process. The device characteristics of BNW_GGNMOS have been explained in silicon and the experimental results have confirmed that the new proposed design has a better ESD robustness than traditional N-Well ballast resistance GGNMOS. Without silicide blocked mask, BNW technique is a good device for ESD protection design in the nano-scale CMOS technology.

Chapter 4 Equal-Substrate-Potential Technique to Enhance the Turn-on Uniformity of Multi-Finger MOSFET

4.1 INTRODUCTION

Due to wider channel width of ESD protection device are needed for discharging ESD current, it should be drawn in multi-finger structure to use area effectively. From the turn-on mechanism introduced in the preceding chapter, the substrate potential elevates the base of lateral parasitic bipolar transistor, then turns on the channel of MOSFET. In chapter three, all works use ballast technique without silicied blocked to enhance ESD robustness to prevent current localization, but it doesn't solve un-uniform turn-on issue of multi-finger NMOS. Because ballast resistance only reduces the current crowding phenomenon in one single finger on the surface of diffusion region, the un-uniform turn-on issue still remains on adjacent fingers though, results in decreasing of ESD robustness.

In order to solve the un-uniform turn-on issue of multi-finger NMOS, there is a solution to equalize the substrate potential under each finger. In order to verify the design works or not, the design and the contrast both use silicide block around drain side contact to complete.

4.2 PRIOR DESIGNS TO ENHANCE TURN-ON UNIFORMITY OF GGNMOS

Fig. 4.1 shows a layout style that can make the base resistance of each parasitic lateral n-p-n BJT in the multi-finger GGNMOS approximately equal, which is implemented by inserting a P+ diffusion region (P+ pick up) adjacent to the source terminals of each finger NMOS transistor [14]. With the equal base resistance, all parasitic lateral n-p-n BJTs can be triggered on simultaneously to discharge ESD current. However, the layout area is greatly

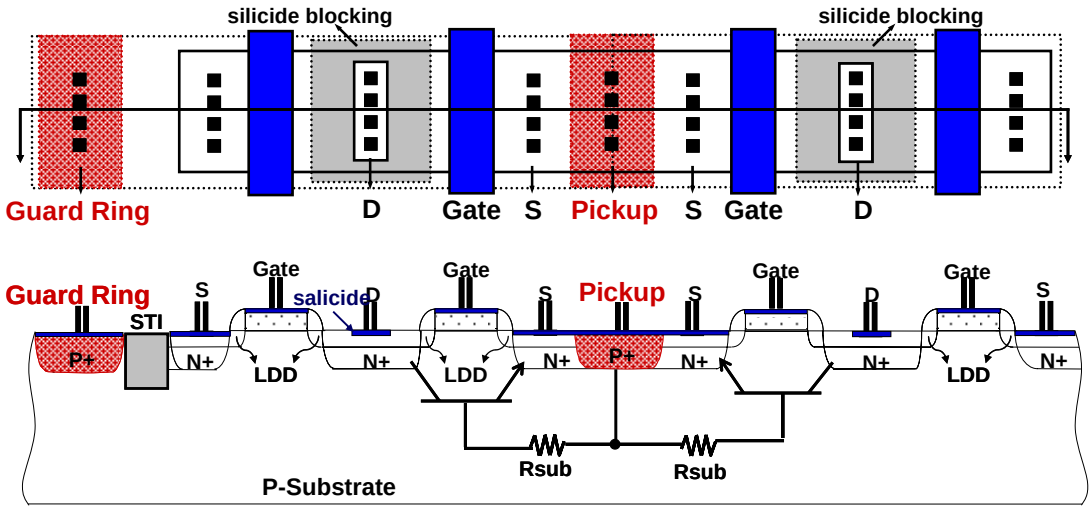


Fig. 4.1 The layout top-view and the cross-sectional view of the inner pickup structure.

increased by the insertion of P+ diffusion region into each source region. Also, such a layout style is strictly prohibited in the deep-submicron CMOS processes, because the substrate resistance of each finger NMOS drawn in this layout style becomes so small that all parasitic lateral n-p-n BJTs in the NMOS fingers are hard to be triggered on quickly to protect the thin gate-oxide of internal circuits [15].

To verify if it is still prohibited in nano-scale CMOS process, and to check the nano-scale PMOS parasitic lateral bipolar turn-on mechanism, this prior design is taped out in 90nm CMOS process to confirm the doubt.

Fig. 4.2 shows the layout scheme of inner pickup NMOS. All the device are drawn in 6 fingers shape, with every finger length is 20 mm. Fig. 4.3 shows the TLP I-V curve testing under the testing voltage of 1.0V. In Fig. 4.4, it's apparently that the second breakdown current (It2) degrades as the number of inner pickup increase. To verify the reason of degradation is the same or not, Fig. 4.5 shows the zoom-in view of little step TLP test curve. Just as expected, Fig. 4.6 verify that the trigger current and holding voltage get larger as the number of inner pickup increase. This is the main reason that the ESD degradation still remains in 90nm CMOS process.

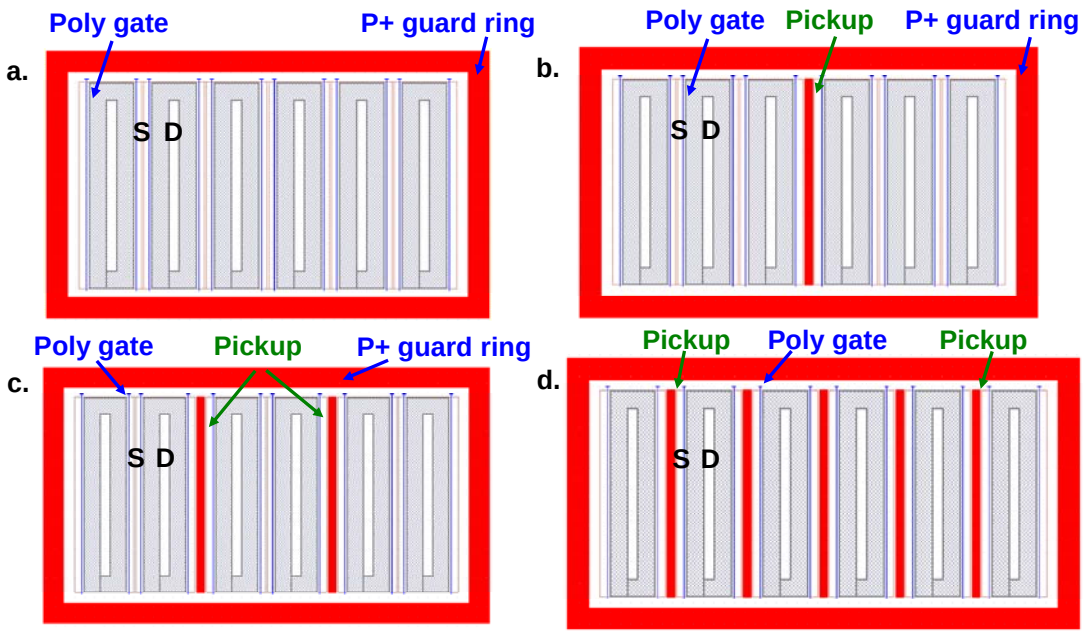


Fig. 4.2 The layout top view of the multi-finger NMOS with different number of additional pickup structures inserted into source regions, (a) pickup = 0, (b) pickup = 1, (c) pickup = 2, and (d) pickup = 5.

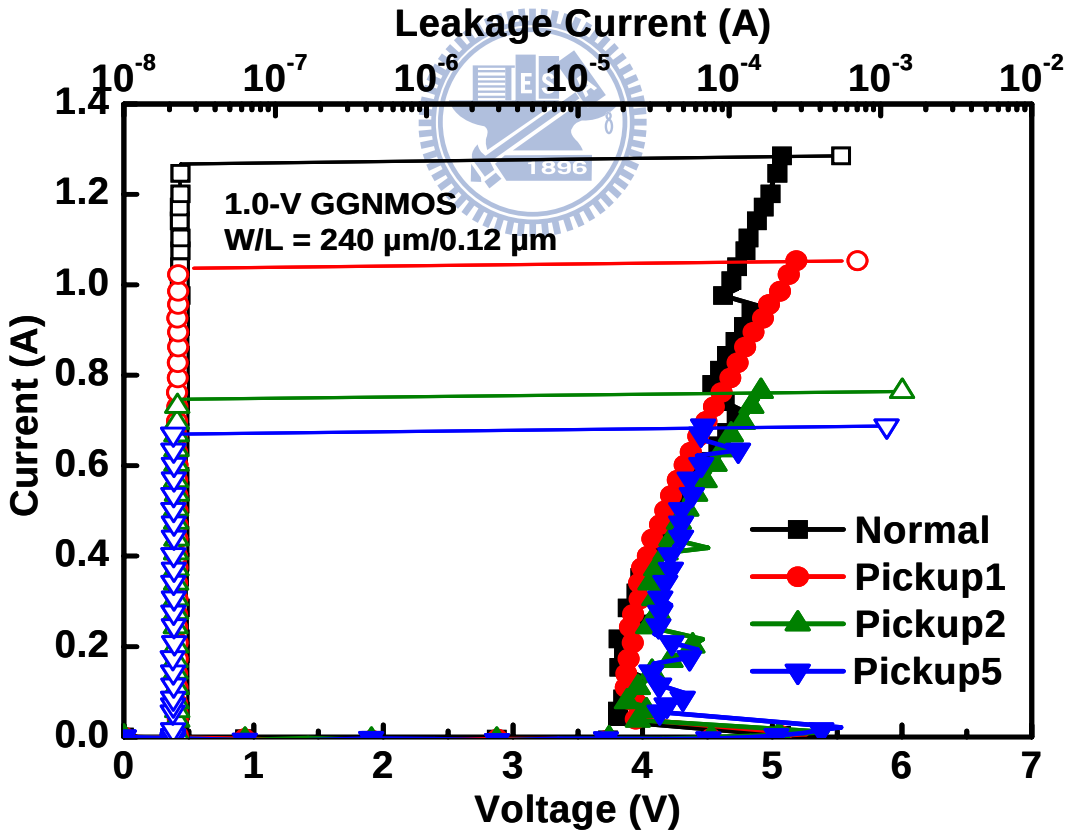


Fig. 4.3 The TLP I-V curve of 1.0V GGNMOS with inner pickup in UMC 90nm CMOS Process.

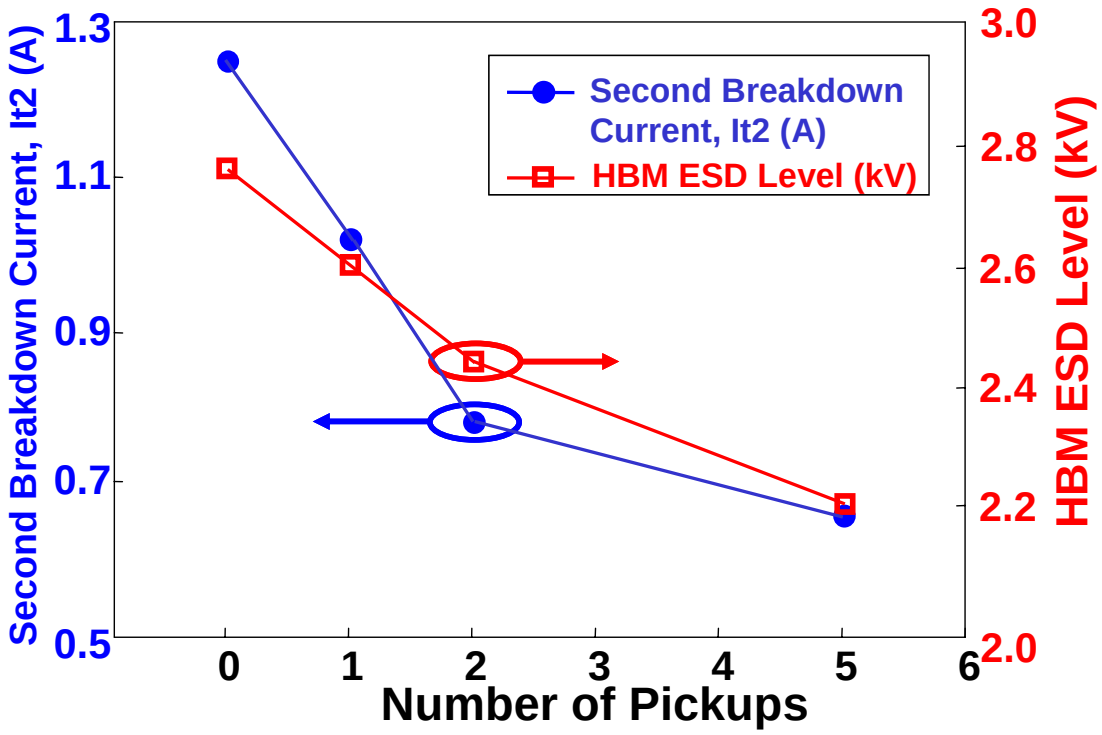


Fig. 4.4 Dependence of It2 and HBM ESD level on different number of pickup structures of 1.0V and multi-finger NMOS.

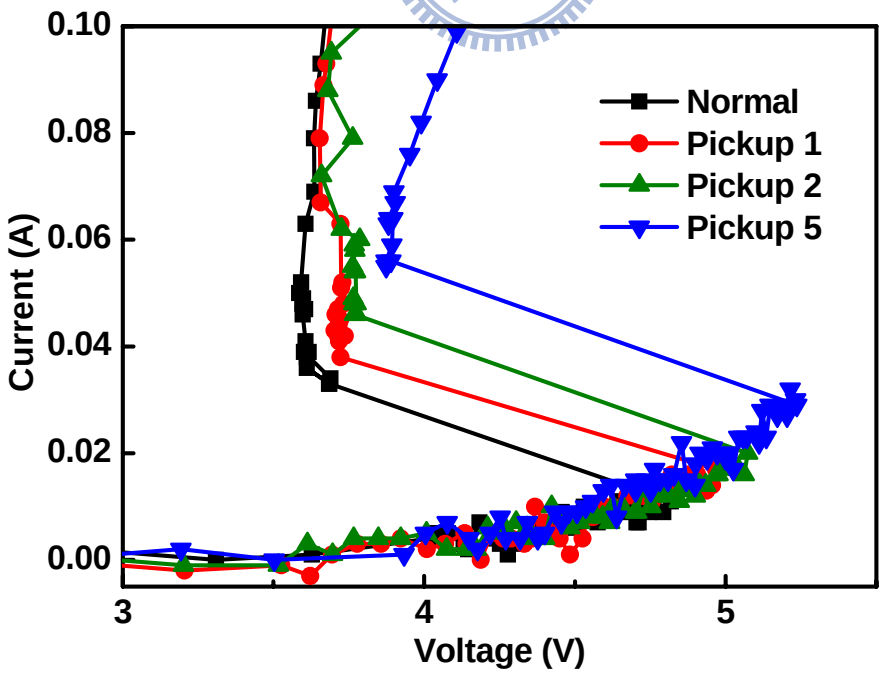


Fig. 4.5 The zoom-in view of little step TLP test curve.

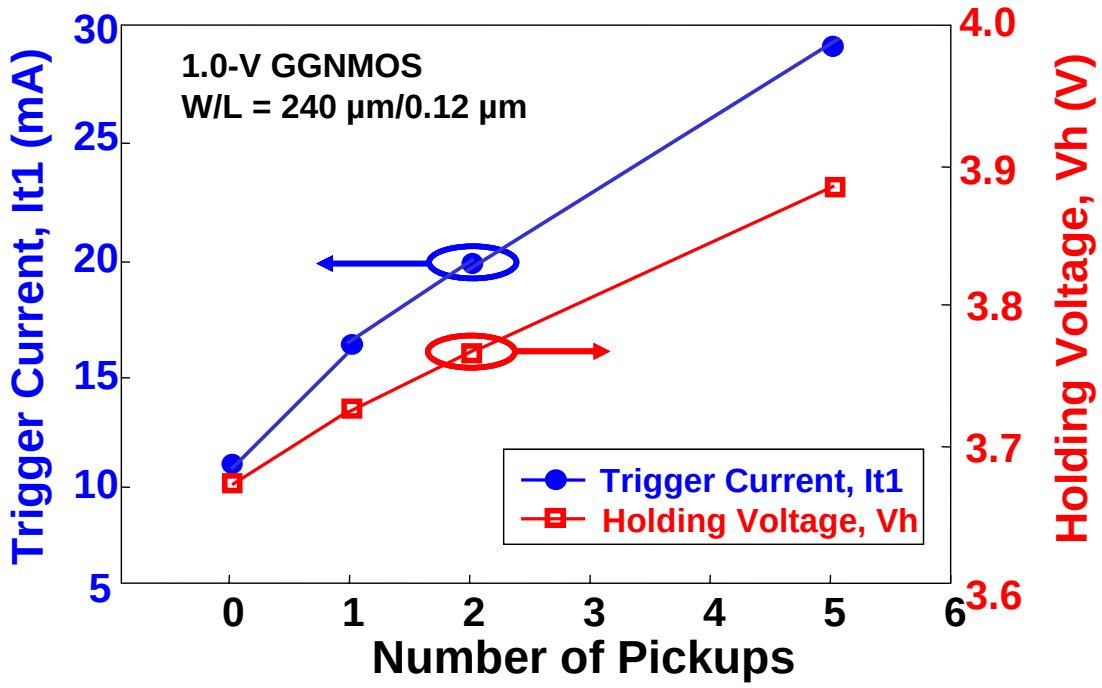


Fig. 4.6 Trigger current (It1) and Snapback Holding Voltage (Vh) of 1.0-V GGNMOS.

So as the N+ inner pickup insert to the source region of PMOS, the layout top view shows in the Fig. 4.7. Fig. 4.8 shows the TLP I-V curve of 1.0V GDPMOS with inner pickup in 90nm UMC process. Fig. 4.9 shows the second breakdown current (It2) and HBM ESD level on different number of pickup structures. Fig. 4.10 shows the zoom-in view of little step TLP test curve. and Fig. 4.11 shows the trigger voltage of different number of pickup structures. It seems there's no difference in the effect of inserting inner pickup. It's sure that the PMOS parasitic pnp bipolar beta gain is still not enough to result in the snapback of bipolar turn-on.

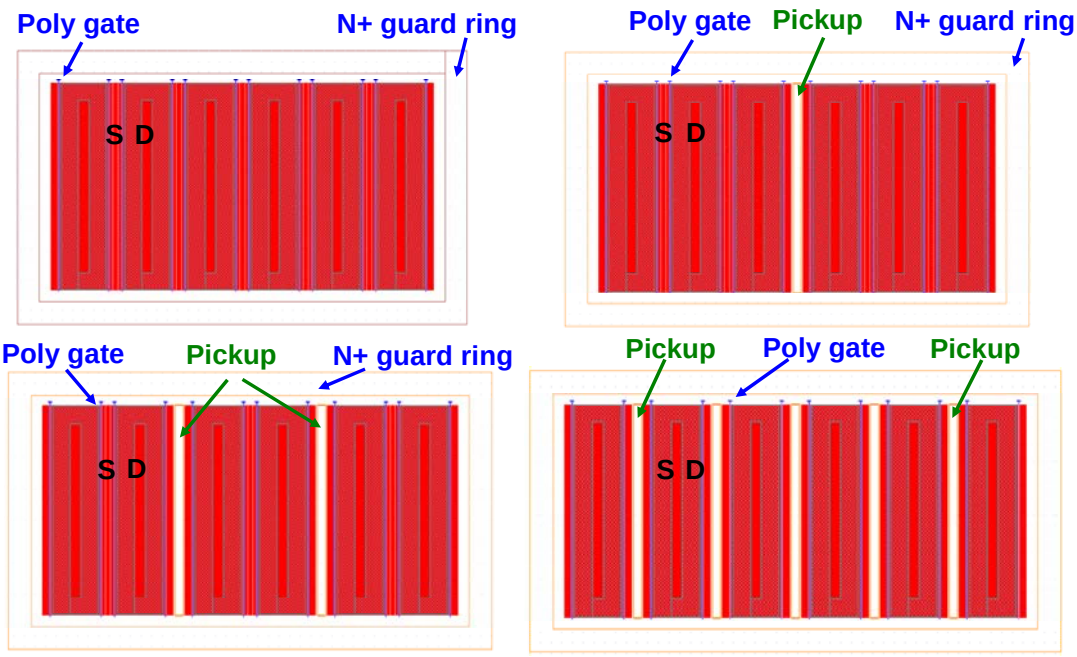


Fig. 4.7 The layout top view of the multi-finger PMOS with different number of additional pickup structures inserted into source regions, (a) pickup = 0, (b) pickup = 1, (c) pickup = 2, and (d) pickup = 5.

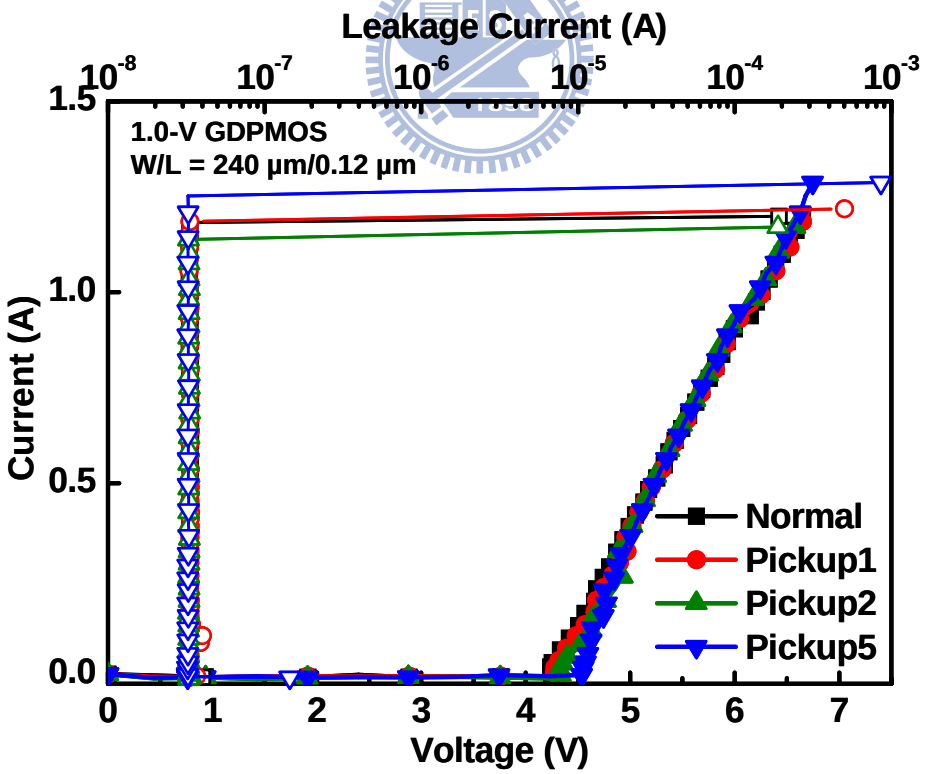


Fig. 4.8 The TLP I-V curve of 1.0V GDPMOS with inner pickup in UMC 90nm CMOS Process.

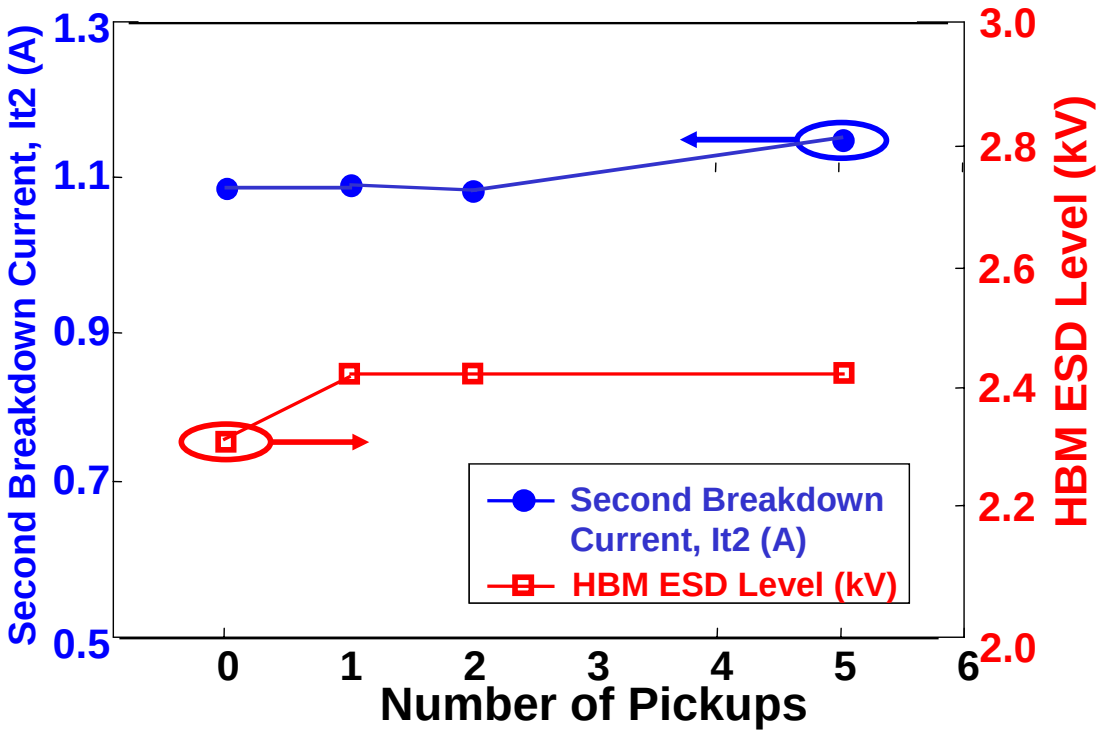


Fig. 4.9 Dependence of It2 and HBM ESD level on different number of pickup structures of 1.0V and multi-finger PMOS.

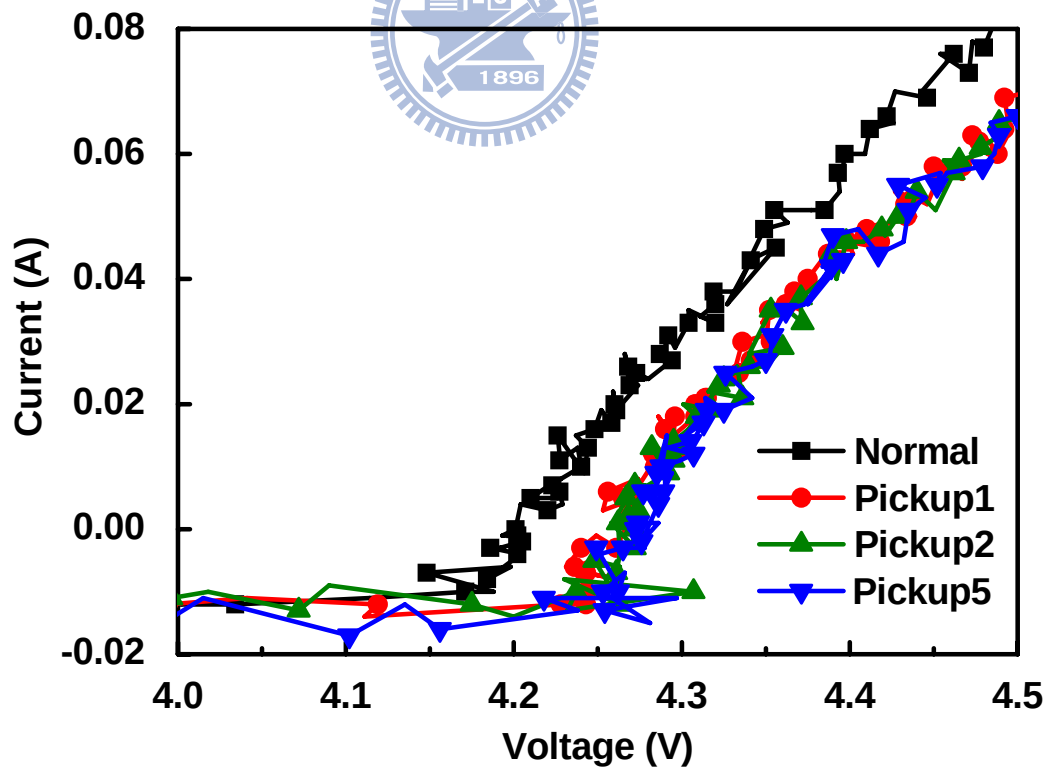


Fig. 4.10 The zoom-in view of little step TLP test curve.

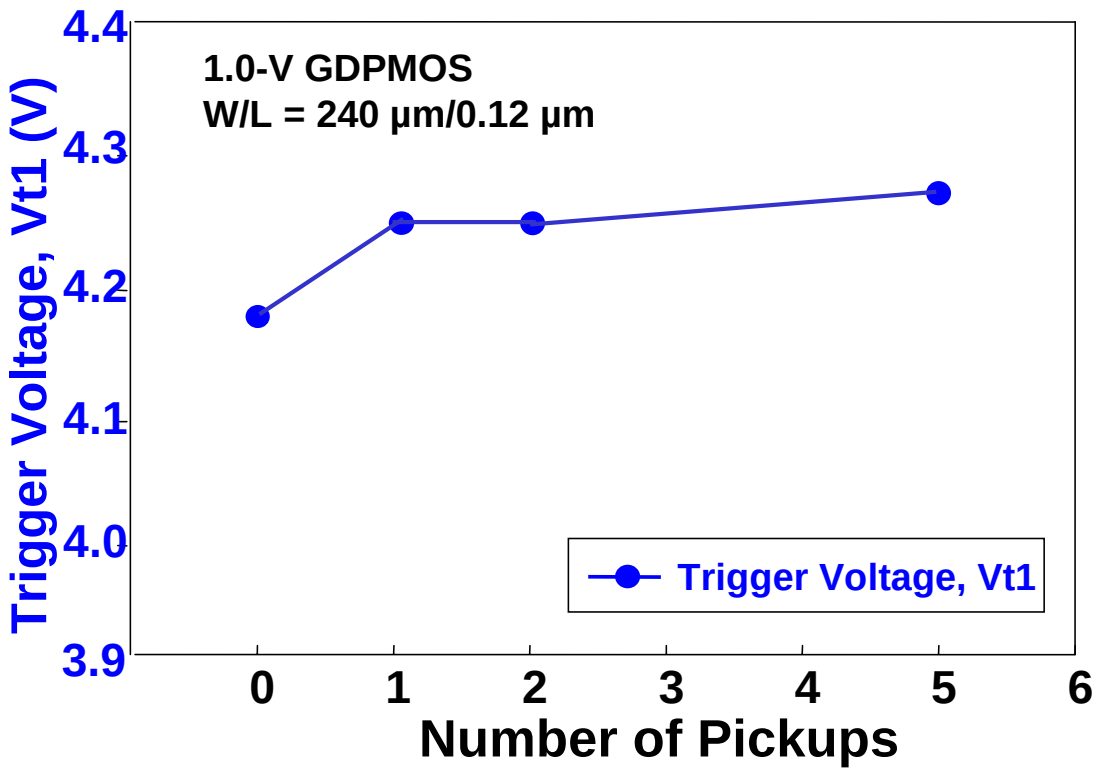


Fig. 4.11 Trigger current (It1) and Snapback Holding Voltage (Vh) of 1.0-V GDPMOS.

4.3 PARTLY-ISOLATED-BODY GGNMOS (PIB_GGNMOS)

Although the following introduced inner pickup structure could solve the non-uniform turn-on issue of multi-finger GGNMOS, but it degrades the ESD robustness due to the increase of trigger current and holding voltage. The new proposed partly-isolated-body GGNMOS could solve the non-uniform turn-on issue of multi-finger GGNMOS, and still have high ESD robustness. Fig. 4.12 shows the layout top view and cross-section view of partly-isolated-body structure. The Deep N-Well is coverd the whole N+ diffusion region, and every drain side diffusion has N-Well strip underneath, and there is also the N-Well strip beside the side edge of source, under STI. Base on this structure, the base of the parasitic lateral bipolar under gate has no any connection with the left and right side guard, it could only connect to guard ring by up and down side. And the situations under all the channel are the same.

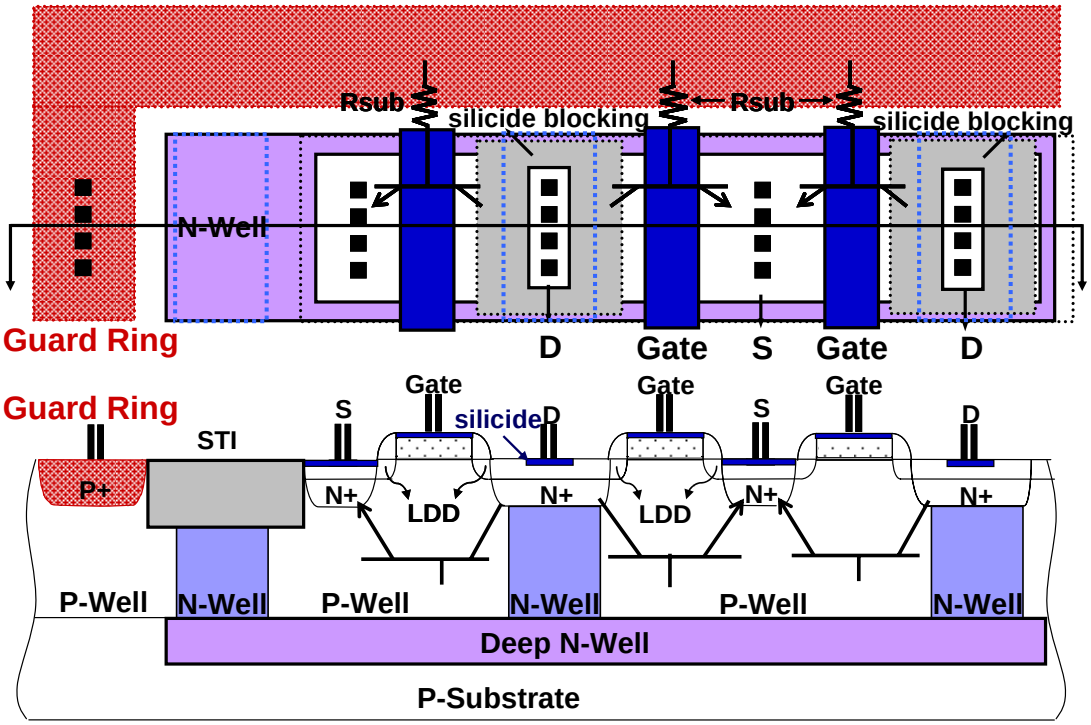


Fig. 4.12 The layout top-view and the cross-sectional view of the partly-isolated-body structure.

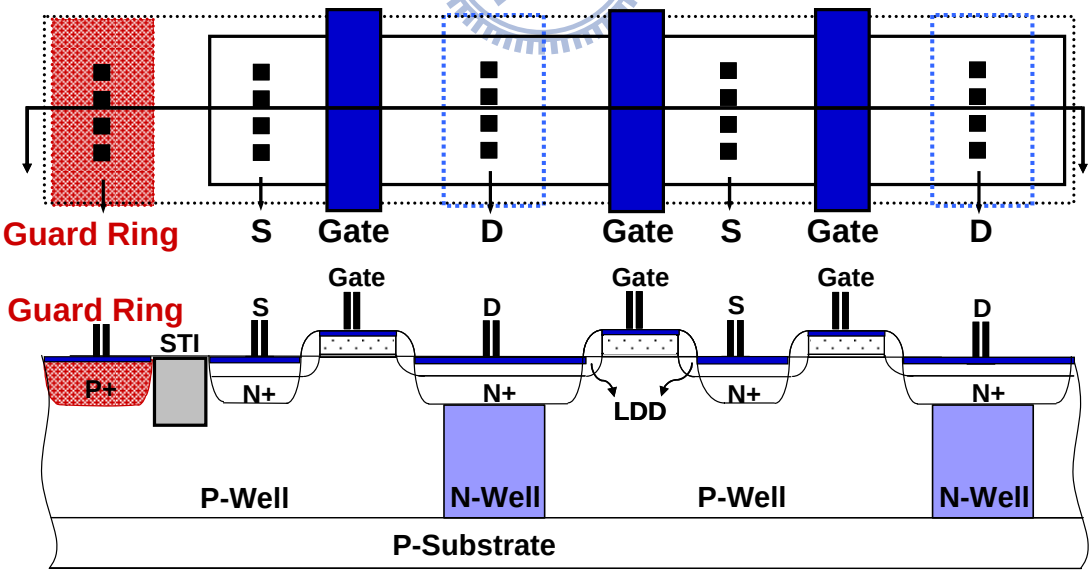
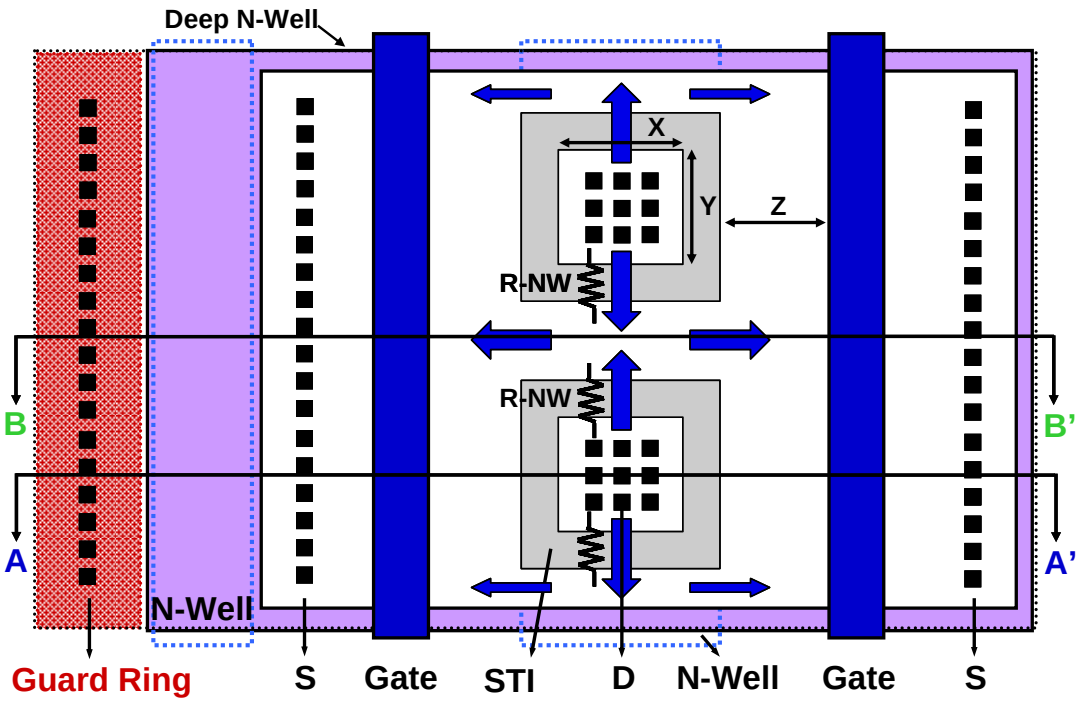


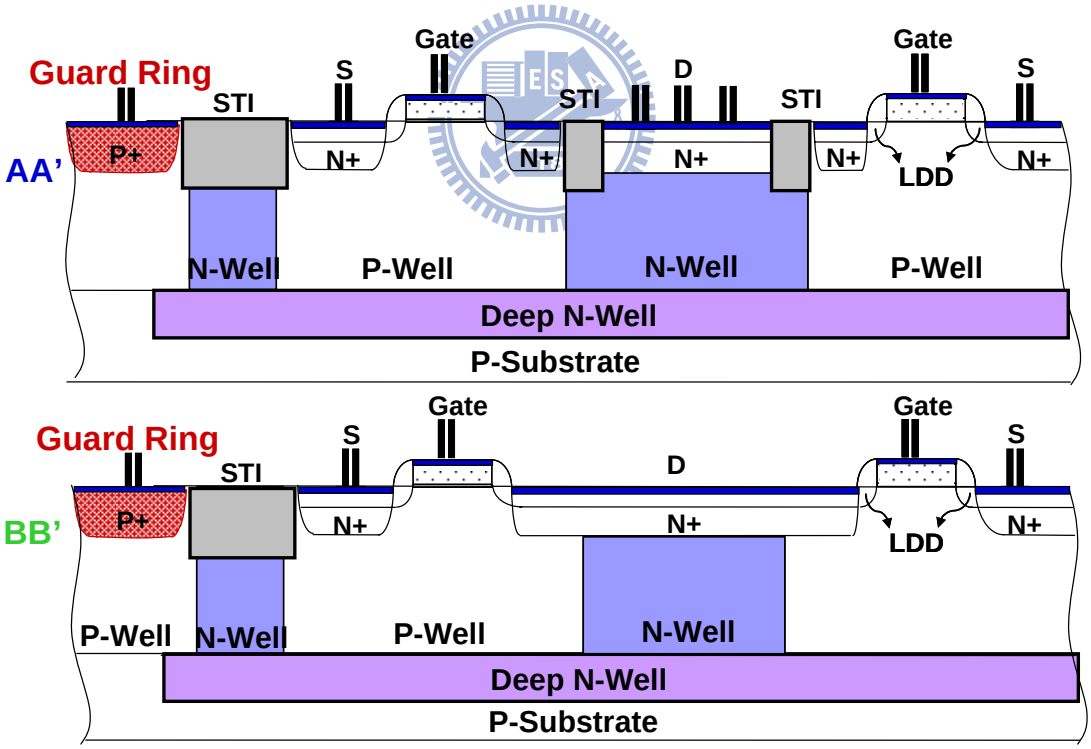
Fig. 4.13 The layout top-view and the cross-sectional view of the contract of partly-isolated-body structure.

In order to verify the effect is from isolated body, but not the reason of N-Well prevents spiking, Fig.4.13 structure is needed to be comparison with partly-isolated-body structure. The contract is based on traditional multi-finger NMOS with N-Well under drain side contact, to prevent the spiking effect and enhance reliability.

Furthermore, the partly-isolated-body structure could be used on the bending-N-Well ballast structure, it will promote the ESD robustness without silicide blocked mask. Fig. 4.14 shows the combination of these two structure. There is already N-Well strip under drain side contact in the bending N-Well structure, so it only has to add the Deep N-Well under the device and two N-Well strip beside the N+ diffusion inside guard ring.



(a)



(b)

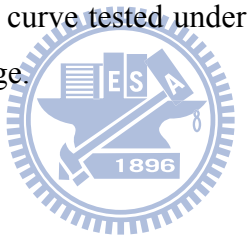
Fig. 4.14 (a) The layout top-view and (b) the cross-sectional view of the bending N-Well ballast resistance structure combined with partly-isolated-body structure.

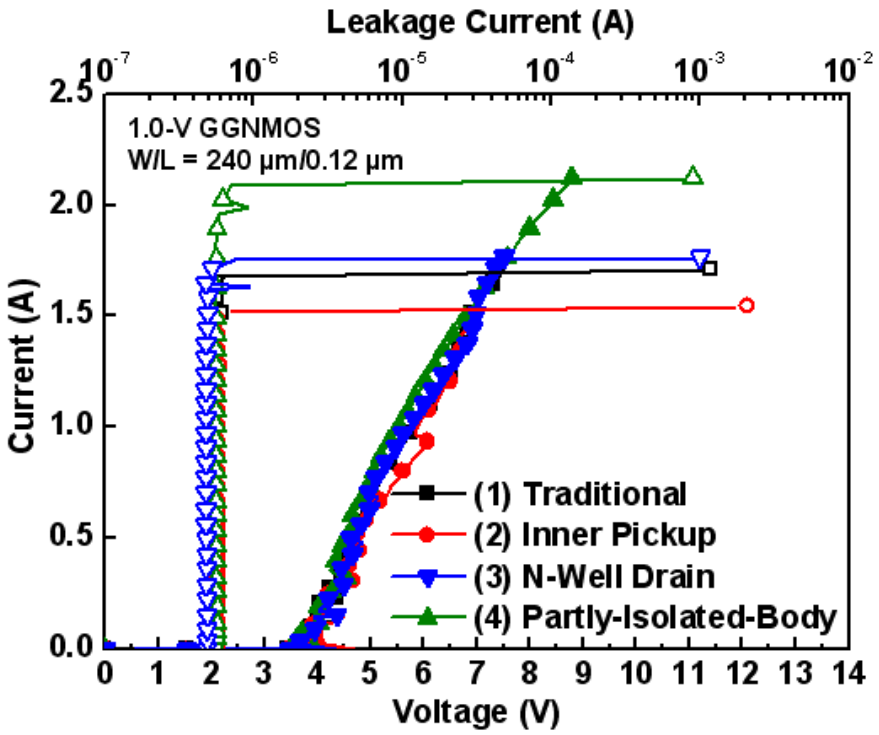
4.4 EXPERIMENTAL RESULTS AND DISCUSSION

The new proposed partly-isolated-body has realized in 55-nm CMOS process with silicide blocked. In order to verify the effect of equal substrate potential in partly-isolated-body, there are traditional multi-finger NMOS, N-Well under drain side contact multi-finger NMOS, and inner pickup multi-finger structure.

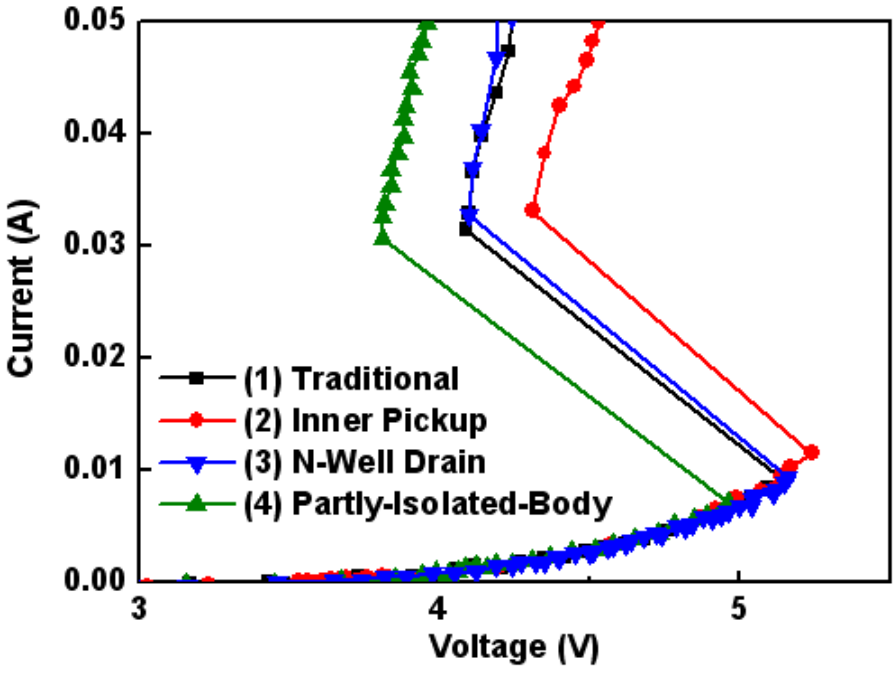
4.4.1 TLP Measurement Results

To investigate the turn-on behavior of the partly-isolated-body structure during high ESD current stress, TLP generator with a pulse width of 100ns is used to measure the second breakdown current (It2) of the device. Fig. 4.15(a) shows the TLP-measured I-V curves and the corresponding leakage currents of four types of silicide blocked multi-finger GGNMOS. All are test under 1.0V stress. And Fig. 4.15(b) is the TLP-measured I-V curve tested under low step voltage to examine the turn-on current and holding voltage.





(a)



(b)

Fig. 4.15 (a)The TLP-measured I-V curves of partly-isolated-body GGNMOS, traditional GGNMOS, GGNMOS with one inner pickup at center finger, and the contract from partly-isolated-body GGNMOS. All are drawn in channel width of 240mm, and (b) the enlarged view of the TLP-measured I-V curves under low step voltage around the trigger and snapback region.

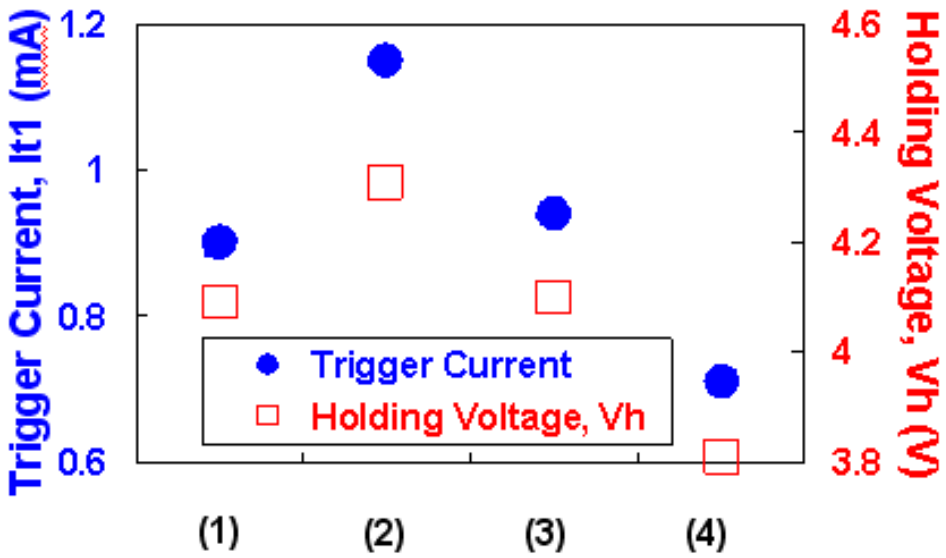


Table 4.1 The value of trigger current and holding voltage of four types of silicide blocked GGNMOS.

From the TLP I-V curve in Fig. 4.15, it's apparently that the partly-isolated-body GGNMOS has a great promotion from traditional multi-finger GGNMOS, and the contrast is no distinction with traditional multi-finger GGNMOS. Inner pickup GGNMOS, still the same, has a degradation of It2 and ESD robustness. It's because partly-isolated-body GGNMOS has a small trigger current and holding voltage as shown in Table 4.1.

Otherwise, the combination of partly-isolated-body and BNW ballast resistance structure is realized in 55-nm CMOS process, too. And Fig. 4.16 shows the TLP-measured I-V curves of traditional N-Well ballast resistance structure, BNW ballast resistance structure with or without partly-isolated-body.

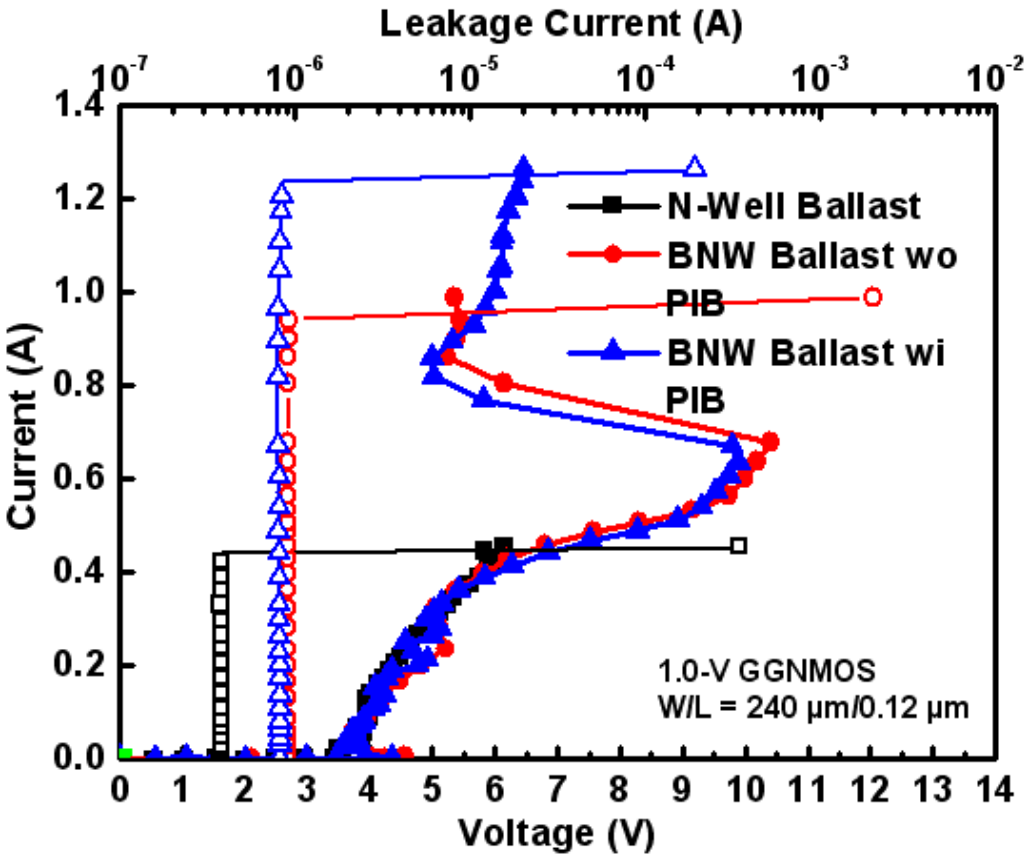


Fig. 4.16 The TLP-measured I-V curves of three GGNMOS without silicide blocked structure.

There is a obvious improve of the combination from the partly-isolated-body and the BNW ballast resistance structure, And the second snapback has explained in chapter three.

4.4.2 ESD Robustness

The ZapMaster is used to verify the HBM and MM ESD robustness of the devices. In these ESD verifications, the devices are tested under the positive-to-VSS ESD stress, and the failure criterion is defined as the measured voltage at the current level of 1μA shifted 30% from its original value. The comparison of the ESD levels between the traditional multi-finger GGNMOS and the proposed partly-isolated-body GGNMOS is shown in Table 4.2.

MOS Type	Silicide Blocked	It2 (A)	HBM (kV)	W/L (μm/μm)	Area (μm^2)	It2/Area (mA/μm^2)
Traditional Multi-Finger NMOS (TM NMOS)	yes	1.68	3.0	240/0.12	1512	1.11
	yes	0.86	2.0	120/0.12	839	1.03
Inner Pickup Structure NMOS (IP NMOS)	yes	1.55	2.6	240/0.12	1593	0.97
	yes	0.80	2.0	120/0.12	895	0.90
Traditional Multi-Finger NMOS with N-Well under Drain Side (NW NMOS)	yes	1.75	3.6	240/0.12	1512	1.16
	yes	0.90	2.2	120/0.12	839	1.07
Partly-Isolated-Body Structure NMOS (PIB NMOS)	yes	2.09	4.4	240/0.12	1624	1.29
	yes	1.03	2.8	120/0.12	941	1.10
	no	1.24	3.4	240/0.12	1791	0.69

Table 4.2 The table of It2, HBM ESD level, and It2 per area of four types of silicide blocked GGNMOS.

4.4.3 Failure Analysis

Fig. 4.17 shows the SEM analysis of traditional multi-finger GGNMOS in 55-nm CMOS process after TLP testing. It's clearly that some fingers of gate oxide are broken but some are still complete, this is the non-uniform turn-on phenomenon. Because the current mostly flows in the earlier turn-on fingers, and heat focuses on it, causing failure easily. And Fig. 4.18 and Fig. 4.19 show the SEM analysis of multi-finger GGNMOS in partly-isolated-body structure and inner pickup structure. In these two figures. The position at gate oxide are all complete, and failure happened because of the contact spiking or diffusion junction. So these two structures could both solve the non-uniform turn-on issue of multi-finger device. But in inner pickup structure, due to the higher trigger current, holding voltage, and the product of the two parameters, heat production is higher, too. So inner pickup structure has a low second breakdown current and ESD robustness compared with traditional multi-finger device. On the contrary, partly-isolated-body structure has a lower trigger current and holding voltage, so it has a higher second breakdown current and higher ESD robustness.

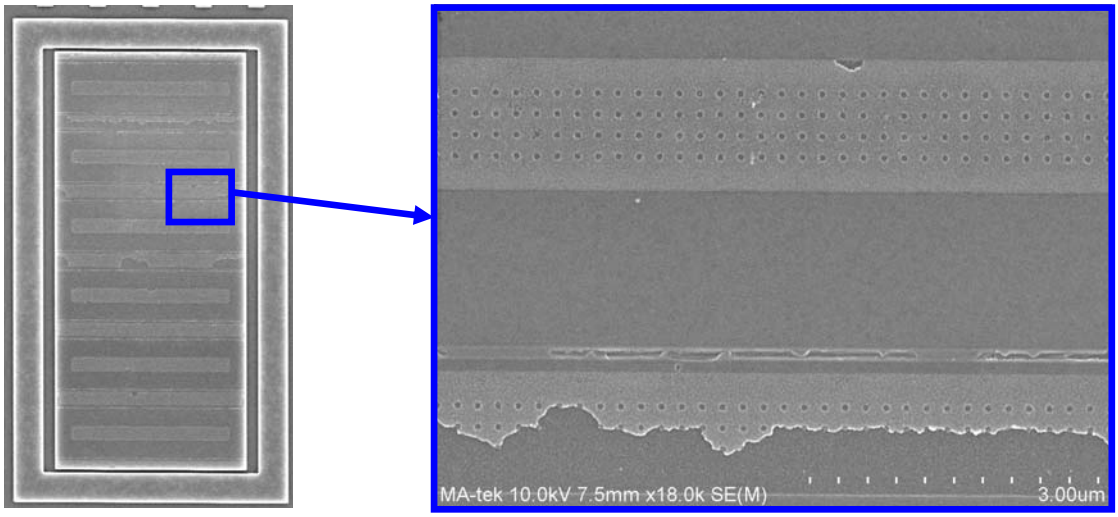


Fig. 4.17 The SEM of traditional multi-finger GGNMOS in 55-nm CMOS process after TLP testing.

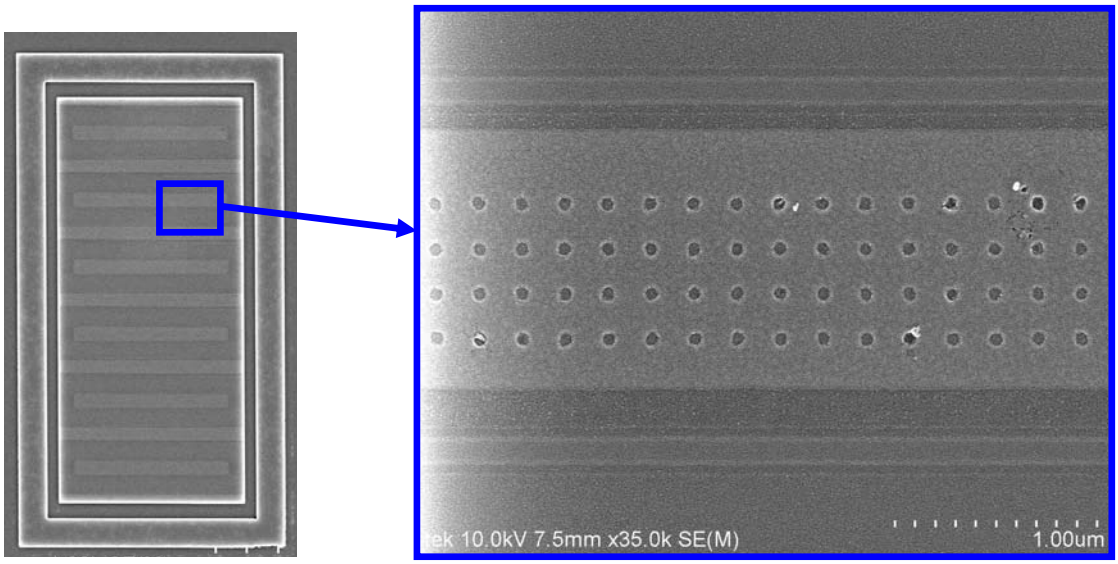


Fig. 4.18 The SEM of partly-isolated-body multi-finger GGNMOS in 55-nm CMOS process after TLP testing.

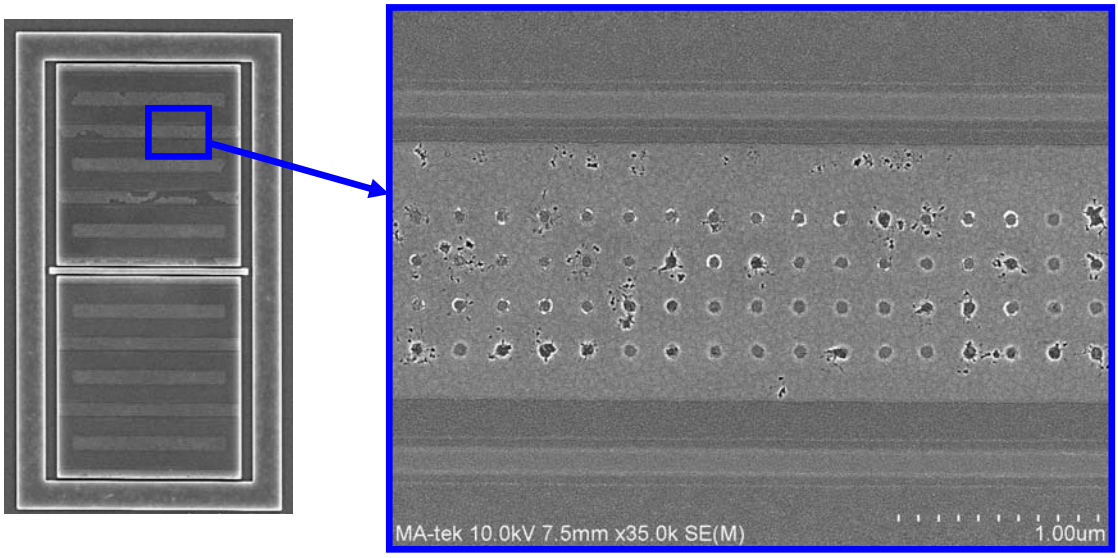


Fig. 4.19 The SEM of inner pickup multi-finger GGNMOS in 55-nm CMOS process after TLP testing.

4.5 CONCLUSION

The new proposed partly-isolated-body structure has been designed and realized in 55-nm CMOS process, effectively solved the non-uniform turn-on issue of multi-finger GGNMOS. It is still verified that the advantage of partly-isolated-body technique is no from the preventing of spiking effect. This solution uses only layout technique to complete, without complex routing. Moreover, partly-isolated-body technique could be combined with BNW ballast resistance structure in fully-silicide procedure, provide better ESD robustness without silicide blocked mask.

Chapter 5 Conclusion and Future Work

5.1 CONCLUSION

To improve the ESD robustness in fully-silicide, a bending N-Well ballast resistance technique has been designed and verified in a 55-nm CMOS process. The device characteristics of BNW_GGNMOS have been explained in silicon and the experimental results have confirmed that the new proposed design has a better ESD robustness than traditional N-Well ballast resistance GGNMOS. Without silicide blocked mask, BNW technique is a good device for ESD protection design in the nano-scale CMOS technology.

The new proposed partly-isolated-body structure has been designed and realized in 55-nm CMOS process, effectively solved the non-uniform turn-on issue of multi-finger GGNMOS. It is still verified that the advantage of partly-isolated-body technique is no from the preventing of spiking effect. This solution uses only layout technique to complete, without complex routing. Moreover, partly-isolated-body technique could be combined with BNW ballast resistance structure in fully-silicide procedure, provide better ESD robustness without silicide blocked mask.

5.2 FUTURE WORK

Without silicided blocked mask, there are already large amounts of drain side ballast resistance technique, but all these works are performed in 2-D CMOS process. That's a un-exploitative field in 3-D CMOS process. There have never developed any design of ballast technique in 3-D CMOS process.

Besides, on-chip ESD protection circuit may not be suitable in future 3-D stacked IC technology, a more flexible ESD protection should be brought up urgently.

References

[1] K.-H. Oh, C. Duvvury, K. Banerjee, and R.-W. Dutton, "Analysis of nonuniform ESD current distribution in deep submicron NMOS transistors," *IEEE Trans. Electron Devices*, vol. 49, pp. 2171-2182, Dec. 2002.

[2] T.-Y. Chen and M.-D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices," *IEEE Trans. Device and Material Reliability*, vol. 1, pp. 190-203, Dec. 2001.

[3] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd Edition, NewYork: Wiley, 2002.

[4] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, pp. 173–183, Jan. 1999.

[5] T.-Y. Chen and M.-D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices," *IEEE Trans. Device and Material Reliability*, vol. 1, pp. 190-203, Dec. 2001

[6] G. Notemans, A. Heringa, M.-V. Dort, S. Jansen, and F. Kuper "The effect of silicide on ESD performance," in *Proc IEEE Int. Reliab. Phys. Symp.*, pp. 154-158, 1999.

[7] S. Mitra, R. Gauthier, J. Li, M. Abou-Khalil, C.-S. Putnam, R. Halbach, and C. Seguin, "ESD protection using grounded gate, gate non-silicided (GG-GNS) ESD NFETs in 45nm SOI technology," in *Proc. EOS/ESD Symp.*, 2008, pp. 312-316.

[8] S.-T. Lin, W.-F. Chen, and C.-H. Lien, "A full-salicide NMOS Transistor with floating poly array for ESD improvement in a 0.18um CMOS technology," in *Proc. Taiwan ESD Conference*, pp. 23-26, 2003.

[9] H.-C. Hsu and M.-D. Ker, "Dummy-gate structure to improve ESD robustness in a fully-salicided 130-nm CMOS technology without using extra salicide-blocking mask," in *Proc. IEEE Int. Symp. on Quality Electronic Design*, 2006, pp. 503-506.

[10] B. Keppens et al., "Active-area-segmentation(AAS) technique for compact, ESD robust, fully silicided NMOS design," in *Proc. EOS/ESD Symp.*, 2003, pp. 250-258.

[11] K.-G. Verhaege and C.-C. Russ, "Wafer cost reduction through design of high performance fully silicided ESD devices," in *Proc. EOS/ESD Symp.*, 2000, pp. 18-28.

[12] E.-R. Worley, "New ballsting method for MOS output drivers and power bus clamps," in *Proc IEEE Int. Reliab. Phys. Symp.*, pp. 458-461, 2005.

[13] G. Notermans, "On the use of N-well resistors for uniform triggering of ESD protection elements," in *Proc. EOS/ESD Symp.*, 1997, pp. 221-229.

[14] J.-H. Lee, J.-R. Shih, Y.-H. Wu, B.-K. Liew and H.-L. Hwang, "An analytical model of positive H.B.M. ESD current distribution and the modified multi-finger

protection structure," in *Proc. of IPFA*, 1999, pp.162-167.
[15] M.-D. Ker, C.-H. Chuang, and W.-Y. Lo, "Layout design on multi-finger MOSFET for on-chip ESD protection circuits in a 0.18-μm salicided CMOS process," in *Proc. IEEE Int. Symp. Electronics, Circuits and Systems (ICECS)*, 2001, pp. 361-364.
[16] Ming-Dou Ker and H.-C. Hsu, "The impact of inner pickup on ESD robustness of multi-finger NMOS in nanoscale CMOS technology," in *Proc. of 2006 IEEE International Reliability Physics Symposium (IRPS)*, 2006, pp. 631-632.

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Design to Enhance Turn-on Uniformity of Multi-Finger ESD Protection Devices