國立交通大學

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碩士論文

利用雙重微影成像法製作非對稱Ｐ型金氧半場效電晶體之研究

Fabrication of Asymmetric PMOSFETs with Double-Patterning Technique

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中華民國　九 十 八　年 八 月

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摘要

在本篇論文，僅利用線形光學步進器並搭配雙重微影成像法可微影出 0.1 微米的閘極長度，這已經超越機台的微影解析度極限。利用此技巧，即使不用電子束直寫系統，仍有小於 0.1 微米的解析度，這對於學校的實驗研究，提供較便利的小線寬微影方法。在實驗中，雙重微影成像法在電子顯微鏡下的線寬觀測結果下，可對此方法的線寬控制精準度做檢查。雙重微影成像法並可應用在非對稱金氧半場效電晶體的結構設計，非對稱金氧半場效電晶體可以比傳統的對稱結構有所改善，傳統上為了考量製作成本以及製程上的便利性，都使用對稱的設計。而雙重微影成像法恰好可以滿足非對稱金氧半場效電晶體的智成考量。本研究調變了源極/汲極延伸區域的結構參數(接面深度)，來驗證其對於驅動電流、短通道效應的影響。實驗做出來的非對稱元件雖然有過度蝕刻造成的缺陷，但是在基本電性還有短通道效應上，仍可以分析出比對稱的結構有些許的改善。

Fabrication of Asymmetric PMOSFETs with Double-Patterning Technique

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Abstract

In this thesis, a double patterning method using an I-line stepper has been developed to define gate length below 0.1 μm, which is beyond the limit of I-line machines with standard lithographic procedure. Verifying by scanning electron microscopy (SEM), this double-patterning method has been shown to have the ability to push gate lengths to smaller than 0.1 μm. This allows us to fabricate nano-scale devices without using advanced and costly lithography techniques like e-beam writer or deep-UV steppers.

Apart from the capability of forming finer line-width, double-patterning method is also feasible for design and manufacturing of asymmetric MOSFETs which have many advantages over conventional symmetric ones. The concept of implementing asymmetric source/drain (S/D) extensions is conducted in this thesis on a PMOSFET structure. The ideal MOSFET prefers a shallower drain extension junction and a deeper source extension junction, rather than the same S/D extension junction depths in the conventional symmetric ones. The basic electrical characteristics of this

asymmetric PMOSFET device are examined and compared with the symmetric ones. Although an unexpected etch-induced recess phenomenon is observed, we show that many improvements are identified, especially in the enhancement of immunity to the short-channel effects.

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張格綸 誌於 新竹交大

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Chapter 1 Introduction

1-1 General Background

The evolution of CMOS technology in the past thirty years has followed the path of device scaling for achieving density, speed, and power improvements [1]. According to the report released by International Technology Roadmap of Semiconductors (ITRS), the physical gate length has scaled down to 29nm after 2008 [12]. Nevertheless, as the size of the devices is reduced down to deep sub-micron regime, some detrimental effects would degrade the performance of devices, such as the leakage issues, the ability of controlling short-channel effects, threshold voltage adjustment and variation, and parasitic effects including gate and S/D resistance and parasitic capacitance of junction.

Considerable researches have focused on the novel device structures, materials, and processes. For instance, lightly doped drain (LDD) structures [2] are used to improve hot-carrier reliability of sub-micron devices. Meanwhile, the Double Implanted LDD (DI-LDD) [3] structures added an oppositely doped "halo" implantation around source and drain to improve threshold roll-off near 0.6 μm regime. After that, the gate-over-lapped LDD (GOLD) structure [4] was developed to achieve better performance and reliability over LDD.

All the methods mentioned above and standard fabrication schemes were designed under the symmetric MOSFET structure, in other words, the source and drain are symmetric with respect to the channel. These symmetric structures are

popular mainly owing to their simplicity in device fabrication as well as low process cost. However, theoretically symmetric structures are not ideal in term of device performance since the source and drain have different requirements in this regard.

1-2 Asymmetric MOSFET

The lightly doped drain (LDD) structures were commonly used in MOSFETs since 1980's to improve hot-carrier reliability. Hence, the MOSFET could satisfy the requirement of good immunity against short-channel effects at a supply voltage of 3 ~ 5 V with sufficient hot carrier reliability. However, the transistor's drive current is reduced due to the increasing parasitic resistance in LDD region. The redcued drive current of the transistor would degrade the operation speed. Such a concern becomes more significant as MOSFETs are scaled into deep sub-micron regime. To overcome the above issue, asymmetric structures could be a useful approach.

Asymmetric LDD MOSFET not only has the merit of improving drive current without compromising the hot carrier reliability, but also has higher breakdown voltage. According to the paper by Tony Ewert in 2002, asymmetric MOSFET could be a possible approach for improving breakdown voltage while maintaining cut-off frequencies [7]. The breakdown voltage of the sub-micron MOSFET is generally just a few volts, which is not sufficient for the application in power amplifier of the transceiver. In order to generate output power density at several GHz, both the drive current and the apply voltage should be sufficiently high. Meanwhile, the cut-off frequency needs to be no less than that of the low power circuits.

Conventional MOSFET fabrication adopts symmetrical LDD processing as the standard procedure in order to take the advantage of the self-aligned process. However, several proposed asymmetrical MOSFET structures have been proved to exhibit improved performance over conventional MOSFET structure. It has been shown that asymmetric MOSFET with removal of the source side LDD could improve the drive current without degrading hot carrier reliability [5], [6]. The halo source gate-overlapped drain (HS-GOLD) structure, with a halo only in the source side and LDD only in the drain side, obtains not only high hot-carrier reliability but also high punch-through resistance [10]. As a result, designing S/D junction separately could be one feasible way in improving the performance of MOSFET.

1-3 Double Patterning Technique

MOSFET scaling was propelled by the rapid advancement of lithographic techniques for delineating fine lines of 1 μm width and below [1]. To achieve this reduction, lithographers have been finding clever ways to change the three variables of the Rayleigh criterion in order to reduce the pitch resolution:

$$HP = k_1 \times \frac{\lambda}{NA}$$

where λ = wavelength of the light

NA = numerical aperture

k_1 = process difficulty factor

HP = minimum printable half-pitch

Traditionally, reduction of the wavelength has proven very successful. Currently, 193 nm is the shortest wavelength in semiconductor production. Immersion lithography allows the increase of NA beyond 1.0 which is the physical limit imposed by the refractive index of air as described by Snell's law. Currently, immersion systems with NA of 1.30 to 1.35 could be delivered in semiconductor manufacturers since 2007 [9].

One of the options is lowering the wavelength by an order of magnitude with extreme ultra-violet (EUV) systems to reach a λ of 13.4 nm with an NA of ~0.25. The other is the use of ~1.55 NA immersion 193 nm systems requiring the 3rd generation higher index (RI > 1.8) immersion fluids, photo-resists and lens material. However, according to the experiments, neither 3rd generation lens materials nor EUV tools and infrastructure will be ready for production before 2011 [9].

Consequently, double patterning has become one of the promising candidates to bring us to the next node of the ITRS-roadmap. As an alternative in immersion lithography and EUV lithography both require considerable changes in infrastructure, instead, double patterning makes use of the existing infrastructure. Therefore, double patterning has gained considerable attention during the past few years. It has become a serious candidate to reach the 45 nm node and even the 32 nm node [10].

1-4 Motivation

In light of the above introduction, double patterning could be a feasible approach to pattern the length widths down to 0.1 μm by using the I-line stepper. Hence, in this

study we employed the technique to fabricate the MOSFET in the experiments. Furthermore, based on double patterning, designing source and drain sides separately could be realized, thus increasing the flexibility on designing MOSFETs. Therefore asymmetric LDD MOSFET could be designed with different junction depth at source and drain junctions. Based on the former reports, a deeper source junction and a shallower drain junction is preferred. To illustrate the effectiveness of separate source and drain engineering, symmetric MOSFETs are used as a benchmark for comparison.

1-5 Organization of Thesis

In Chapter 2, the process for developing double patterning is described and evaluated. Utilization of the developed double patterning technique for device fabrication is also stated. After that, the characterization scheme and measurement setup are also introduced in Chapter 2.

In Chapter 3, the experimental results on characterizing the fabricated devices, including the transfer and output current-voltage (I-V), and capacitance-voltage (C-V) characteristics, are shown and discussed. Effects of the double-patterning process on the device characteristics are explored and addressed.

Important conclusions and comments on the results of this study are stated in the final chapter of the thesis.

Chapter 2 Device Fabrication, Process Flow and Measurement Setup

2-1 Device Fabrication

All the device fabrications were carried out in National Nano Device Laboratories (NDL). PMOSFET with asymmetric source/drain (S/D) was based on, but more complicated than, the conventional MOSFET process. Fig. 2.1 shows the diagrams of the process flow for fabricating the asymmetric S/D MOSFET characterized in this study.

The devices were fabricated on 6-inch n-type wafers. N-type well was formed by P^+ implantation at 120 keV and 7.5×10^{12} cm^{-2}. Conventional local oxidation of silicon (LOCOS) was performed with channel stop implantation by As^+ implantation at 120 keV and 3×10^{12} cm^{-2}. Threshold voltage was adjusted by As^+ implantation at 80 keV and 4×10^{12} cm^{-2} and anti-punch through implantation was done by P^+ implantation at 120 keV and 4×10^{12} cm^{-2}. After the standard LOCOS process, stander RCA cleaning was performed on wafers, followed by the growth of a thermal oxide of 3 nm thick, then a 200 nm undoped poly-silicon was deposited in a vertical furnace by low-pressure chemical vapor deposition (LPCVD).

The fabrications of the control samples were carried out with conventional one-mask process to form the gate and symmetrical S/D. That is, one lithographic step and subsequent etching to form the poly-Si gate, followed by the self-aligned implant steps to form the S/D. Double patterning was executed by two masks (G1 and G2

specified in Fig. 2.2) and associated lithography/etch steps. Although fabrication cost may increase, resolution limit of the gate electrode can be reduced dramatically. In Fig. 2.1(b), the G1 mask defined the right side of the poly-Si gate, followed by the source-extension implantation. The photoresist (PR) of G1 mask was then removed. Next, G2 pattern was generated with another mask. The portion of poly-Si covered by the G2 PR represents the final gate area, and its dimensions can be much smaller than that with one-mask processing. After the second poly-Si etching, drain-extension region was implanted, followed by the removal of the G2 PR. The separated S/D extension region was implanted by BF_2^+ at 1×10^{15} cm^{-2} with different energy conditions.

Sidewall spacers were then formed with deposition of 80nm TEOS layer and subsequent anisotropic etching process. Afterwards, deep S/D regions were formed by BF_2^+ implantation at 25keV and 3×10^{15} cm^{-2}. Poly-Si gate was simultaneously doped during the above implant process. Then, substrate regions were formed and implanted with P^+ at 40 keV and 5×10^{15} cm^{-2}. The annealing process was carried out with spike rapid thermal anneal (SRTA) at 1000 ^oC to activate dopants in the preceding implantation processes.

Afterwards, a 500nm TEOS passivation dielectric layer was deposited on all wafers by OXFORD PECVD. After the contact hole etching, a 600 nm AlSiCu layer was deposited, followed by the formation of metal pads. Finally, all wafers received forming gas annealing at 400 ^oC for 30 minutes to mend the dangling bonds, reducing interface state density at the gate oxide/Si interface.

The major split conditions explored in this work are listed in Table 2.1. Different implantation conditions are employed to form the source/drain(S/D)-extension regions. Other implant conditions, including well implantation, channel stop implantation, threshold voltage adjustment implantations, and anti-punch through implantations are shown in Table 2.2.

2-2 Double Patterning

The design of the double patterning masks is shown in Fig. 2.2. The G1 mask covers mainly the right side of the active region capped with the poly-Si serving as the gate material, while the G2 mask covers mainly the left side of the active region. The overlapped region of the two masks defines the gate electrode, and the gate length could be smaller than the limitation of the I-line stepper, i.e., below 0.3 μm.

Figure 2.3 shows the after etching inspection (AEI) images with in-line scanning electron microscope (SEM). Here, L_{mask} is the designed length on the poly-Si etch mask, and L_{gate} is the practical physical length through lithography and etching processes. Figures 2.3 (a) and (b) are samples formed with conventional single patterning. From the results, it is observed that the error of gate lenth is more than 10 %. From the results shown in Fig. 2.4, it is confirmed that the double patterning can define the gate length below 0.3 μm. However, in the figures we can also see that the L_{gate} is typically shorter than the L_{mask}.In this study for device characterization, we used in-line SEM to determine the exact channel length. From the asymmetry in the signals of the secondary electron-emission presenting at the two sides of the poly-Si

gate shown in the figures, the height at the opposite side of the gate seems different. This might be due to the difference in etching rate of the two individual etching steps. In contrast, the image with the single patterning does not exhibit this feature, as shown in Fig. 2.3(a).

Since L_{gate} is dependent on the lithography and etching biases, L_{gate} can be either longer or shorter than L_{mask}. There are also process tolerances associated with L_{gate}. For the same L_{mask} design, L_{gate} may vary from die to die and wafer to wafer. Though L_{gate} can be measured with SEM, there is also an uncertainty in the precise definition of L_{gate} when the poly-Si etch profile is not vertical. In Fig. 2.3, 2.4, 2.5, and 2.6 are the measured length of conventional single patterning of different range of gate length are shown, the differences between L_{mask} and L_{gate} is defined by the following equation:

$$Error = L_{mask} - L_{gate} \qquad (2\text{-}1).$$

As shown in Figs. 2.3(a) and (b), the error of single-patterning is around 0.05 μm. Nevertheless, as shown in Fig. 2.4, the error of double-patterning is below 0.05 μm, and can be controlled under 0.02 μm for designed L_{mask} dimension in the range from 0.1 μm to 0.3 μm. The results shown in Fig. 2.5 also indicate that the error of double-patterning is small for L_{mask} >0.3 μm. Figure 2.6 shows the images of AEI patterns taken with in-line SEM for double-patterning structures with L_{mask} < 100 nm, and the error can be controlled below 0.02 μm. The above results confirm that double-patterning technique can indeed serve the purpose for producing patterned gate with length below 0.1 μm, much smaller than the limit of resolution restricted by

the exposure machine.

Based on the double-patterning technique, effects of asymmetric S/D-extension could be studied by varying the implantation energy (Table 2.1) in the device fabrication. Four types of devices with various S/D-extension shown in Fig. 2.7 were fabricated and studied in this thesis.

2-3 Electrical Measurement Setup and Basic Electrical Parameters

Current-Voltage (I-V) and capacitance-Voltage (C-V) characteristics were evaluated by using an HP 4156A precision semiconductor parameter analyzer and an HP 4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate dielectrics was obtained from high frequency (100 kHz) C-V curves. The capacitance in strong accumulation becomes independent of the fundamental device parameters; such as bulk doping N_{sub}, poly-Si gate doping N_p, oxide charges Q_{ox}, and fast interface states D_{it}. Therefore, EOT can be extracted with high confidence from one measured point from the strong accumulation region. [11].

From the Id-Vg curve measured at a drain voltage of -0.05 volt, the characteristics of PMOSFET including threshold voltage (V_{th}), subthreshold swing (SS), and transconductance (g_m) are extracted according to their definitions as follows [1]:

The threshold voltage is defined by using the constant current method, i.e., the gate voltage (V_G) needed to achieve a drain current (I_D) of ($\left(W/L\right)\times 1nA$):

$$V_{th} = V_g \Big| I_d = 1nA \times \frac{W}{L} \qquad \text{(2-2).}$$

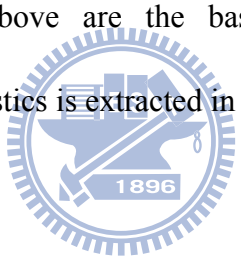
Subthreshold swing (SS) can be calculated from the subthreshold current in the weak inversion region by

$$SS = \left(\frac{\partial Vg}{\partial \log(Id)} \right) \qquad \text{(2-3).}$$

The transconductance (g_m) is extracted by the differentiation of I_d to V_g , i.e.,

$$g_m = \frac{\partial Id}{\partial Vg} \qquad \text{(2-4).}$$

The parameters shown above are the basic electrical parameters, more information of devices characteristics is extracted in the final part of Chapter 3.



Chapter 3 Results and Discussion

3-1 Issues on Double Patterning

The etched profile of the double-patterning poly-Si gates is examined by the Focus Ion Beam (FIB). Figure 3.1 shows the cross-sectional view of a gate with L_{mask} of 0.3 μm. The practical gate length from the image is around 0.2 μm to 0.25 μm. It is observed that the two sides of the poly-Si gate show different slopes and profile. Besides, the bottom of the right side is lower than that of the left, indicating the (second time) etching of poly-Si is not well controlled and results in undesired recess into the underlying gate oxide and substrate in the region adjacent to the right side of the poly-Si gate. The difference between two levels is around 50nm. For some unknown reason, the etch selectivity between the poly-Si and oxide seems to be lost, rendering such outcome.

Figure 3.2 shows the cross-sectional view of a gate with nominal gate length of 0.2 μm. The physical length of the poly-Si gate is about 0.1 μm. The mismatch of the etched profile between two sides of poly-Si gate is more obvious than the result shown in Fig. 3.1. The shape of the poly-Si gate looks more like trapezoidal rather than rectangular as that shown in Fig. 3.1 and Fig. 3.2 in which the nominal gate length is 0.5 μm. The inaccuracy due to the mismatch of the etched profile becomes more profound as the gate length decreases, especially for length below 0.3 μm. In contrast, the conventional single-patterning poly-Si gate shown in Fig. 3.4 is far more symmetric and the inaccuracy of the gate length is reduced.

Figure 3.5 is the schematic diagram of the ideal etched profile of poly-Si gate. However, in this work, the double patterning causes the asymmetric etched profile as shown in Fig. 3.6. Obviously the second etching step needs to be improved. The recessed Si substrate in active region destructs the planar structure of MOSFET and may cause dramatic degradation on the device. Certainly an increase in gate oxide can help address the issue, but this violates the scaling trend and is not appropriate for practical applications.

The above phenomenon is postulated to be related to the plasma properties of the transformer coupled plasma (TCP) poly-Si etcher. Owing to the mask design, the percentage of wafer area exposed to the plasma is high and allows us to end the first etching step with end point detection (EPD) mode. Therefore the etching procedure would finish promptly as the underlying thermal oxide layer is exposed. However, in the second etching step the etched (poly-Si) area is much reduced so the optical signal related to etching product becomes too weak to be detected signal and thus only time mode is available for controlling the etching procedure. This is believed to be the main reason for the occurrence of the above phenomenon. Understanding this issue, modified mask design to enhance the optical signal by increasing the etch area in the 2^{nd} etching step will be adopted to address the problem.

3-2 Basic Electrical Characteristics

Two modes of biasing the asymmetrical PMOSFET structure are shown in Fig. 3.7. According to the standard test configuration for PMOSFET, the source is

grounded while the drain is biased with a negative voltage. [1] So, in the forward mode shown in the Fig. 3.7 the side with a shallower extension serves as the drain, and in the reverse mode the drain is switched to the side with deeper extension.

Figure 3.8 (a) shows the transfer characteristics of an asymmetric PMOSFET of Type C. The channel length is 0.3 μm. In the figure the solid lines represents the forward mode while the dashed lines represents the reverse mode. We can observe that the forward mode has slightly better characteristics in terms of higher drive current and transconductance. The sub-threshold swing (*SS*) is about 86 mV/decade. The drain induced barrier lowering (DIBL) of forward mode is about 58 mV/V while the reverse mode is 65 mV/V. DIBL is also better with the forward mode. However, the differences mentioned above are not significant as expected. Dependences of DIBL and transconductance versus channel lengths are discussed later in Sec. 3-3. Fig. 3.8 (b) shows the transfer characteristics of a Type-D device with channel length the same as the device characterized in Fig. 3-8(a). In the figure we can see that the forward mode and reverse mode have more appreciable difference in DIBL. As described in last chapter, Type-D device has deeper source extension than Type-C under forward mode of operation. This explains the more profound DIBL difference between the two modes in Fig. 3-8(b).

As can be seen in Fig. 3.8 (c), the transfer characteristics of channel length below 0.3 μm show significantly punch-through behavior. The gate loses effective control of the channel, especially as a high drain bias is applied. The etch-induced recession mentioned above is certainly one of the factors responsible for the damage.

Additional techniques for suppressing the short-channel effects should be introduced to reach the short channel below 0.1 μm.

Figure 3.9(a) shows the output characteristics of a nominal symmetrical PMOSFET, which uses double-patterning technique to define the gate length and the extensions at two sides are designed with the same depth. However, difference in drive current between the two modes is observed and the reverse mode shows degraded drive current as much as 9%. Figure 3.9 (b) shows the output characteristics of an asymmetric Type-C PMOSFET with identical channel length. As mentioned in Chapter 2, the drain extension of this device was formed with a relatively low implantation energy of 10 keV. In this case the reverse mode further degrades the drive current by the maximum value of 24 %.

The degradation of the drive current is resulted from the increase in the source-drain series resistance. In the discussion of long channel MOSFET current, usually the effect of S/D resistance can be ignored. However, in a short-channel device, the source-drain resistance can be an appreciable fraction of the total series resistance. Theoretically the nominal symmetrical device characterized in Fig. 3.9(a) should not exhibit asymmetrical I-V characteristics shown in the figure. From the SEM analysis given in last section, obviously the degradation in reverse mode is caused by the asymmetrical etched profiles of the double patterning technique. The asymmetrical extension profile would further worsen the situation, as evidenced in Fig. 3.9(b).

The effect of source-drain resistance can be understood with the equivalent

circuit shown in Fig. 3.10. A source resistance R_s and a drain resistance R_d are assumed to connect an intrinsic MOSFET to the external terminals where V_{ds} and V_g are applied. The internal voltage are V_{ds}' and V_{gs}' for the intrinsic MOSFET. One can write the following relations:

$$V_{ds}' = V_{ds} - (R_s + R_d) I_{ds} \quad (3.1),$$

$$V_{gs}' = V_g - I_{ds} R_s \quad (3.2).$$

According to the above equations, when a MOSFET is operated, the decrease in the overdrive voltage V_{gs}' is mainly affected by the source resistance. While operating in saturation region, the drive current is correlated with overdrive voltage (V_{gs}'-V_{th}) rather than the drain voltage. In other words, the drive current is affected more seriously by the source resistance. In Fig. 3.9(a), the degradation under reverse mode indicates the recessed side contributes more resistance than the other side. This is reasonable, since the recessed junction has a longer distance (along the sidewall of the recess region) to reach the channel edge, as shown in Fig. 3.6. Additional degradation is observed in Fig. 3.9(b) for the asymmetrical device due to the shallower extension depth in the recessed side.

Figure 3.11 (a) and (b) is the output characteristics of the devices with nominal symmetrical S/D and Type-C devices, respectively, measured with a relatively wide drain bias range to illustrate the breakdown behavior. The channel length is 0.3 μm. As can be seen from the figures, breakdown occurs in the short-channel MOSFET when the drain voltage exceeds a certain value. For the nominal symmetric PMOSFET, difference between the breakdown voltage of forward mode and reverse

modes is small. For the asymmetric MOSFET, though the difference of breakdown voltage between the two modes is also small, the breakdown current of reverse mode is appreciably higher than that of the forward mode. This implies that forward mode has better hot carrier reliability than the reverse mode. Although in this work the unexpected etch-induced recessed phenomenon occurred, it is still confirmed that a reduction in the depth of drain extension junction region during operation can improve the hot carrier reliability. Substrate current can be another indicator for the hot carrier effect. From Fig. 3.12, substrate current of reverse mode is higher than that of forward mode for the asymmetrical device characterized in Fig. 3.11(b). The breakdown process in a PMOSFET is shown in Fig. 3.13. In the process the holes gain energy from the field as they move forward along the channel. Before losing energy through collisions, a number of the holes posses high kinetic energy and are capable of generating secondary electrons and holes by impact ionization. The generated holes are attracted to the drain, adding to the drain current, while the electrons are collected by the substrate contact, resulting in a substrate current. The substrate current in turn can produce a voltage drop from the spreading resistance in the bulk, which tends to forward-bias the source junction. This lowers the threshold voltage of the MOSFET and triggers a positive feedback effect, which further enhances the channel current. The results shown in Fig. 3.11(b) and 3.12 confirm that a shallower drain extension can indeed reduce the field strength in the channel and suppress the associated hot-carrier effects.

Typical capacitance-voltage characteristics of the devices are shown in Fig. 3.14.

Serious poly-Si gate depletion effect is observed. The capacitance in the inversion region does not return to the maximum oxide capacitance recorded in the accumulation region. Instead, the inversion capacitance exhibits a local maximum value, C_{max}, at Vg of around -1.5V. This is a feature of poly depletion effect [1], and the local maximum capacitance is dependent on the effective doping concentration of the poly-Si gate. The higher the doping concentration, the less profound the gate depletion effect is and the local maximum capacitance becomes closer to the oxide capacitance. Based on the analysis of poly-Si depletion effect [1], the relationship between C_{max} and the doping concentration of the poly-Si gate, N_p, can be extracted from the following equation:

$$\frac{1}{C_{\max}} = \frac{1}{C_{ox}} + \sqrt{\frac{8kT}{\varepsilon_{Si} q^2 N_p}}, \qquad (3.3).$$

From the equation, the active doping concentration is about $2\times10^{18}\ cm^{-3}$, which is far less than the typical value ($\sim10^{20}cm^{-3}$) in the poly-Si gate. This might be related to the activation step which was carried out with spike-RTA anneal with maximum temperature of 1000 ℃. Further optimization in the activation step is needed to suppress such effect.

3-3 Short Channel Effects

Figure 3.15 shows the threshold voltage (V_{th}) roll-off of the three types of asymmetric PMOSFETs. V_{th} is extracted at a drain voltage of -0.05 V. From the figures we can see that, no matter which type of asymmetric structures, there's no

appreciable difference in threshold voltage between the forward mode and reverse mode. This implies that changing the depth of S/D extension junctions causes no effects on the Vth roll-off control. This is probably due to the fact that the minimum channel length (0.3 μm) is not short enough to distinguish the effect of junction depth. Moreover, the recess phenomenon occurs in the second etching step may also affect. However, the DIBL effect characterized at a high drain bias could resolve the effect of junction depth, which is shown later.

Figure 3.16 shows the V_{th} roll-off of Type-A devices fabricated with either single patterning or double patterning. As can be seen in the figure, the single patterning split shows reverse short-channel effect which is not observed in the double patterning devices. Note that the double patterning split is nominal symmetrical, although in fact they are asymmetrical due to the occurrence of etch-induced recess phenomenon induced at the drain side. This could be the reason why the reverse short-channel effect is not observed in the split, since the practical drain junction depth is deepened with the recess.

Figure 3.17 compares the delta V_{th} roll-off of Types A~D fabricated with double patterning, together with the single-patterned symmetric MOSFET. Obviously the V_{th} roll-off trends for all the asymmetrical devices fabricated by double-patterning process are similar and worse than the Type-A splits, it is convinced that the recess of right side edge in the vicinity of poly-Si gate draws impact on the short-channel effect control. Figure 3.6 is the schematic diagram of double-patterning poly-Si gate. The over-etched active region circled by red dashed line may expose the

Si sidewall near the poly-Si edge. The un-gated region may degrade the effective control region from the point of views of charge-sharing model.

Transconductance is also extracted from the transfer $I_d - V_g$ curve measured in the linear region, and the results are shown as a function of channel length in Fig. 3.19. In the figure, the transconductance of Type C is slightly lower than the other types, owing to their most shallow source and drain extension depth among all splits (see Fig.2.4). DIBL versus channel lengths for the Type C devices is also characterized and shown in Fig. 3.20. It is seen that the forward mode shows better DIBL than reverse mode as channel length is below 0.5 μm, an indication demonstrating the effect of the asymmetrical S/D structure.

Chapter 4 Conclusion and Future Works

4-1 Conclusion

In this study, the double-patterning technique has been proved to be a feasible method for generation of gate patterns with length below 0.1 μm using a conventional I-line stepper. In comparison with the conventional single patterning, double-patterning technique needs one more mask to pattern the gate length, but the inherent asymmetrical S/D formation process makes the fabrication more flexible and more freedoms for device optimization. However, the etch-induced recess at one side of the gate during the second gate-etch step remains to be addressed. This phenomenon results in additional resistance in the drain side leading to asymmetric output characteristics. Besides, the recess etched substrate degrades the short-channel control.

Note the endpoint signal of TCP in the second gate-etch step is not detectable and thus the etching step can not be promptly stopped. Such issue can be overcome by modifying the mask design to increase the etched area and therefore the end pint signal during etching. Otherwise, the control of the gate length and etched profile could be the main issue for the double patterning technique.

In case the above issue is solved, with the double patterning technique, the MOSFET with optimized asymmetrical S/D design could be feasible. Different requirements for source and drain junctions could be realized by the added mask.

Improved device performance in terms of higher immunity to short-channel effects and better current drive is expected.

4-2 Future works

In this work, the PMOSFETs with asymmetric S/D extensions and channel length of 0.3 μm .have been fabricated and characterized. Nevertheless, to fabricate the short channel devices with gate length below 0.1 μm, some practical suggestions are listed as follows:

(1) Add halo implantation to suppress the punch-through effect. From this work, devices with channel length below 0.3 μm suffer from punch-through effect, a tilt angle implantation could be introduced to prevent it. And single side halo implantation could also be introduced. Theoretically, only drain side needs halo implantation.

(2) Mask modification. Since with the present design the second etching cannot detect the end point signal, the control of poly-Si gate etch process is not satisfactory. With mask modification, the area of poly-Si to be etched in the second gate-etch step would be significantly increased and thus the EPD mode could be executed to improve the process control.

Fig. 2.1 (a) Deposition of 200 nm un-doped poly-Si layer after forming the 3 nm gate oxide with thermal oxidation.

Fig. 2.1 (b) The G1 lithographic step to generate the PR patterns and the subsequent etching step to transfer the patterns into the polysilicon.

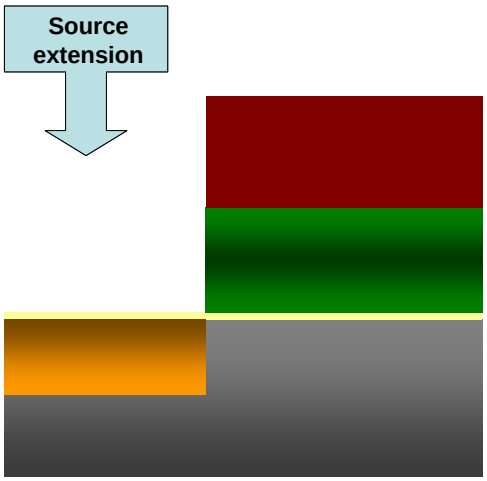


Fig. 2.1 (c) Source-side extension implant. The PR is removed after source-extension implantation.

Fig. 2.1(d) The G2 lithographic step to generate the PR patterns.

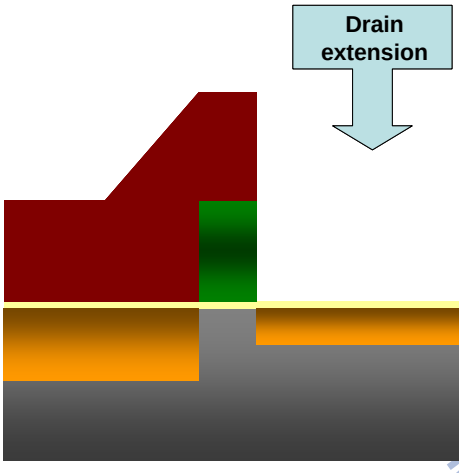


Fig. 2.1 (e) The etching step to define the polysilicon gate. Drain-side extension implant is subsequently performed.

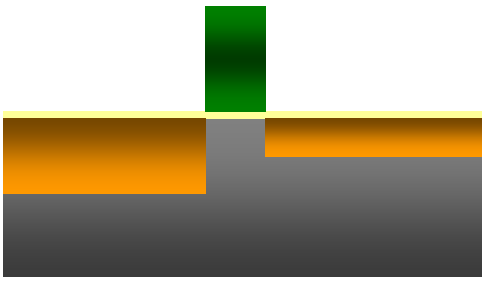


Fig. 2.1 (f) The PR is removed after drain-extension implantation.

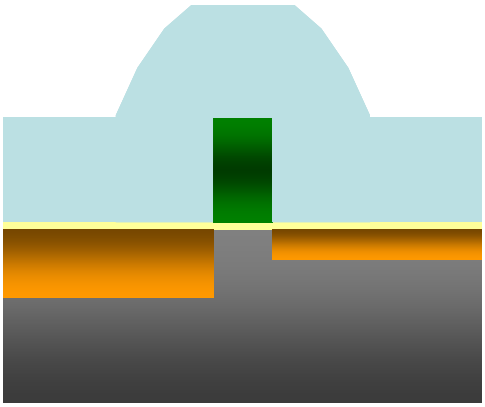


Fig. 2.1 (g) Deposition of a 80 nm TEOS layer.

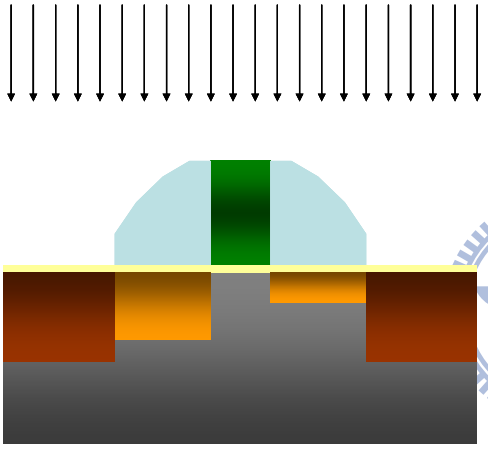


Fig. 2.1 (h) Spacer formation and subsequent deep S/D implant.

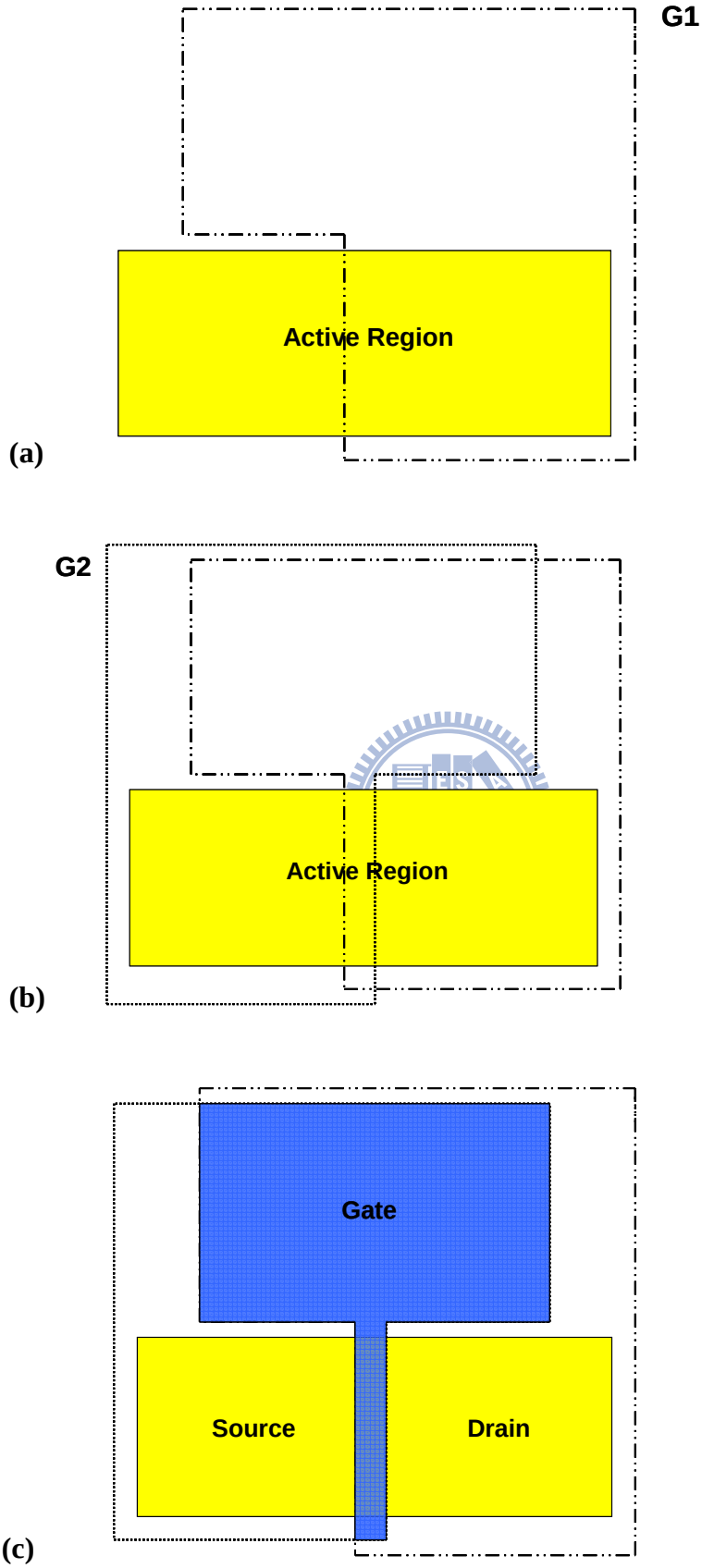


Fig. 2.2 Design of the double-patterning masks.

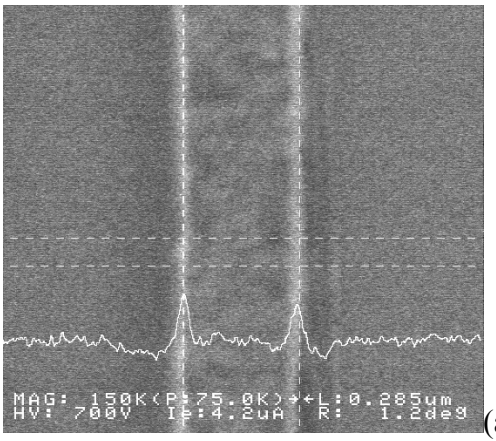
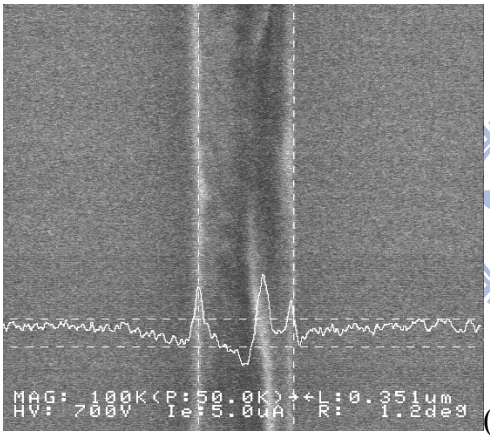
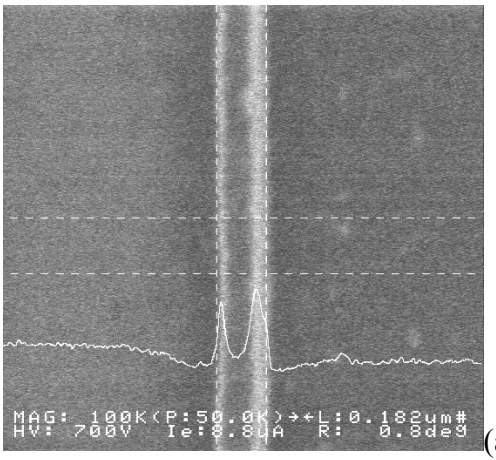
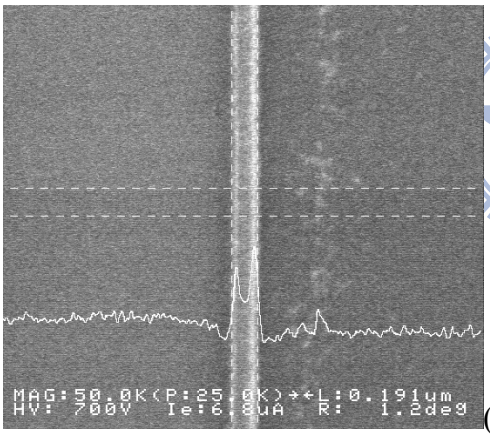
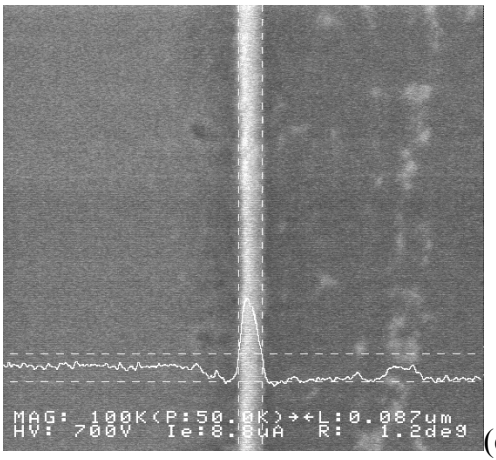
Single Patterning	Measured Length
 (a)	L_{mask} = 0.35 μm L_{gate} = 0.285 μm $Error$ = 0.065 μm
 (b)	L_{mask} = 0.4 μm L_{gate} = 0.351 μm $Error$ = 0.049 μm

Fig. 2.3 In-line SEM images and measured length for patterns formed with single patterning proces

Double Patterning ($0.1\ \mu m \leqq L_{mask} < 0.3\ \mu m$)	Measured Length
 (a)	$L_{mask} = 0.2\ \mu m$ $L_{gate} = 0.182\ \mu m$ $Error = 0.018\ \mu m$
 (b)	$L_{mask} = 0.2\ \mu m$ $L_{gate} = 0.19\ \mu m$ $Error = 0.01\ \mu m$
 (c)	$L_{mask} = 0.1\ \mu m$ $L_{gate} = 0.087\ \mu m$ $Error = 0.02\ \mu m$

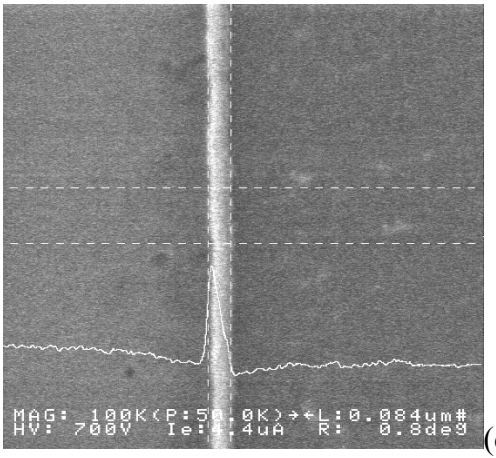
 (d)	$L_{mask} = 0.1\ \mu m$ $L_{gate} = 0.084\ \mu m$ $Error = 0.016\ \mu m$

Fig. 2.4 In-line SEM images and measured length for patterns formed with double patterning process (0.1 μm ≦ L_{mask} < 0.3 μm).

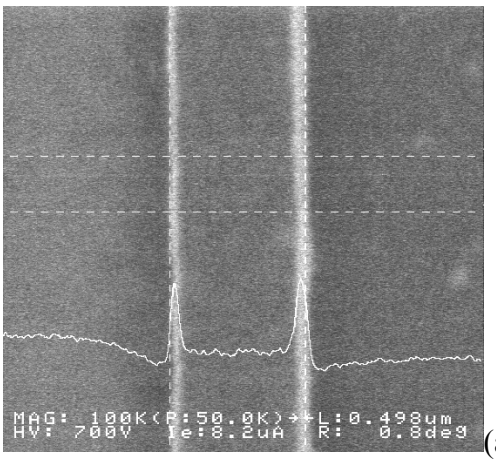
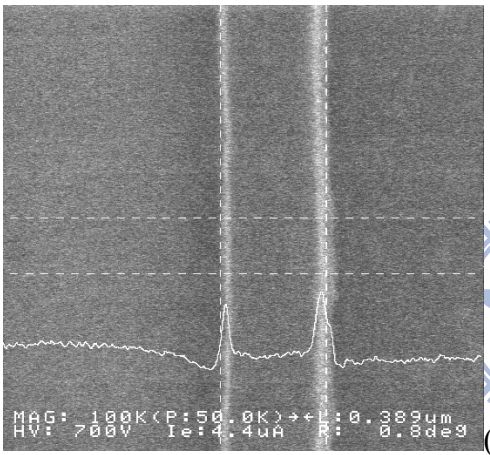
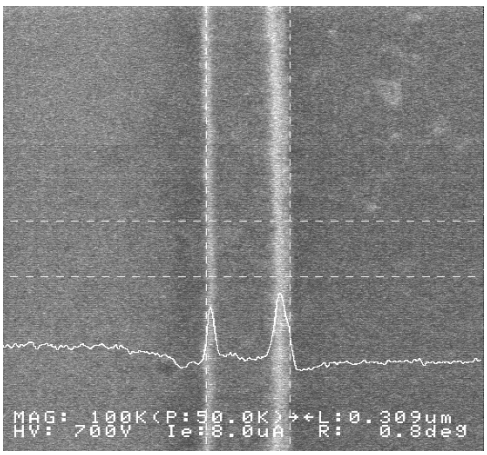
Double Patterning($L_{mask} > 0.3\ \mu m$)	Measured Length
 (a)	$L_{mask} = 0.5\ \mu m$ $L_{gate} = 0.498\ \mu m$ $Error = 0.002\ \mu m$
 (b)	$L_{mask} = 0.4\ \mu m$ $L_{gate} = 0.389\ \mu m$ $Error = 0.011\ \mu m$
 (c)	$L_{mask} = 0.3\ \mu m$ $L_{gate} = 0.309\ \mu m$ $Error = -0.009\ \mu m$

Fig. 2.5 In-line SEM images and measured length for patterns formed with double patterning process ($L_{mask} \geqq 0.3\ \mu m$).

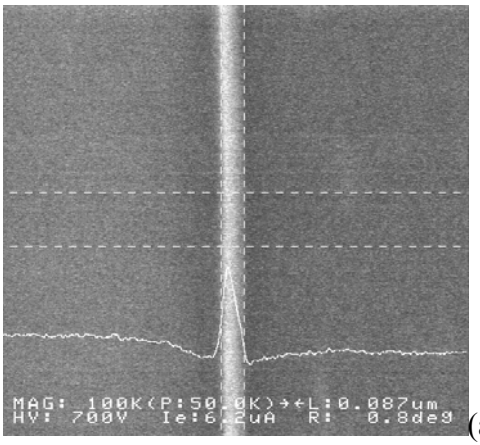
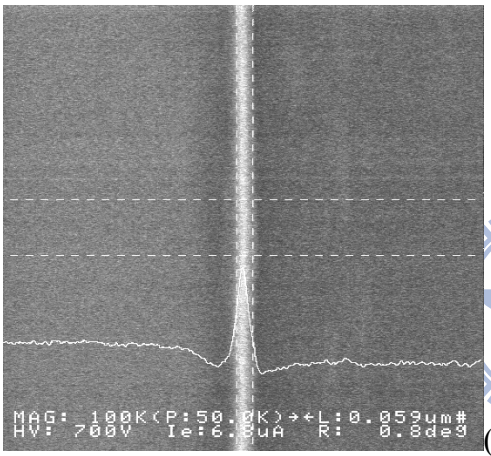
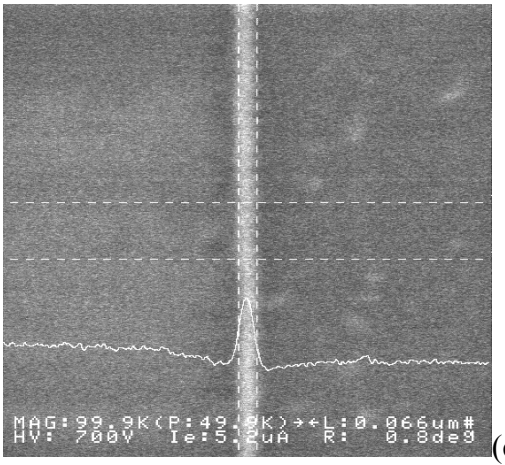
Double Patterning($L_{mask} < 0.1\,\mu m$)	Measured Length
 (a)	$L_{mask} = 0.08\,\mu m$ $L_{gate} = 0.087\,\mu m$ $Error = -0.007\,\mu m$
 (b)	$L_{mask} = 0.05\,\mu m$ $L_{gate} = 0.059\,\mu m$ $Error = -0.009\,\mu m$
 (c)	$L_{mask} = 0.03\,\mu m$ $L_{gate} = 0.066\,\mu m$ $Error = -0.036\,\mu m$

Fig. 2.6 In-line SEM images and measured length o for patterns formed with double patterning process ($L_{mask} < 0.1$ μm).

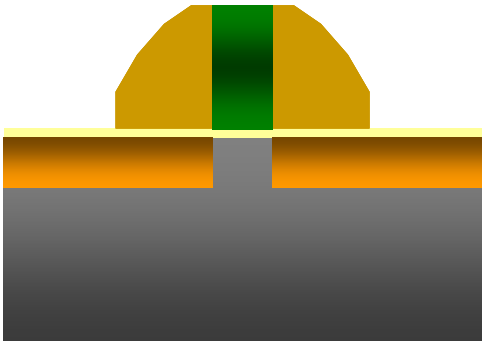


Fig. 2.7 (a) Device Type A as the control samples with symmetric S/D.

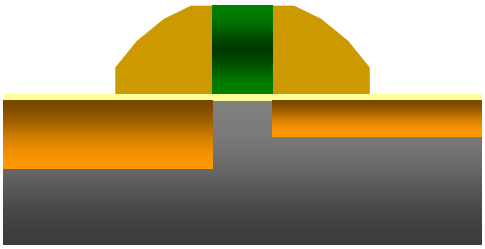


Fig. 2.7 (b) Device Type B with deep source- extension.

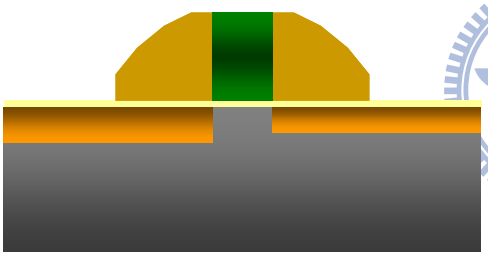


Fig. 2.7 (c) Device Type C with shallow drain-extension.

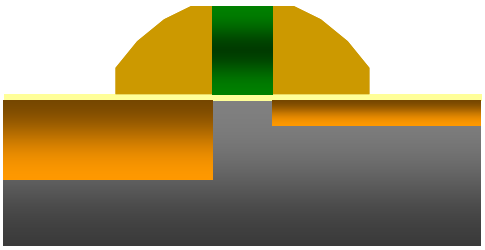


Fig. 2.7 (d) Device Type D with deep source- and shallow drain-extension.

		01	02	03	04	05
S-extension	**BF2,15k,1e15**	●	●		●	
	BF2,20k,1e15			●		●
D- extension	**BF2,15k,1e15**	●	●	●		
	BF2,10k,1e15				●	●
Deep S/D	**BF2,25k,3e15**	●	●	●	●	●

Table 2.1 Split conditions of the PMOSFETs fabricated with double-patterning process. Wafer No. 01 and 02 are Type A (or control samples), 03 is Type B, 04 is Type C, and 05 is Type D shown in Fig. 2.8.

	Ion	**Energy (eV)**	**Dose (cm^{-2})**
N-Well	P^+	120K	7.5e12
Channel Stop	As^+	120K	3e12
Vth	As^+	80K	1e13
APT	P^+	120K	4e12

Table 2.2 Other major implantation conditions used in the PMOSFET fabrication.

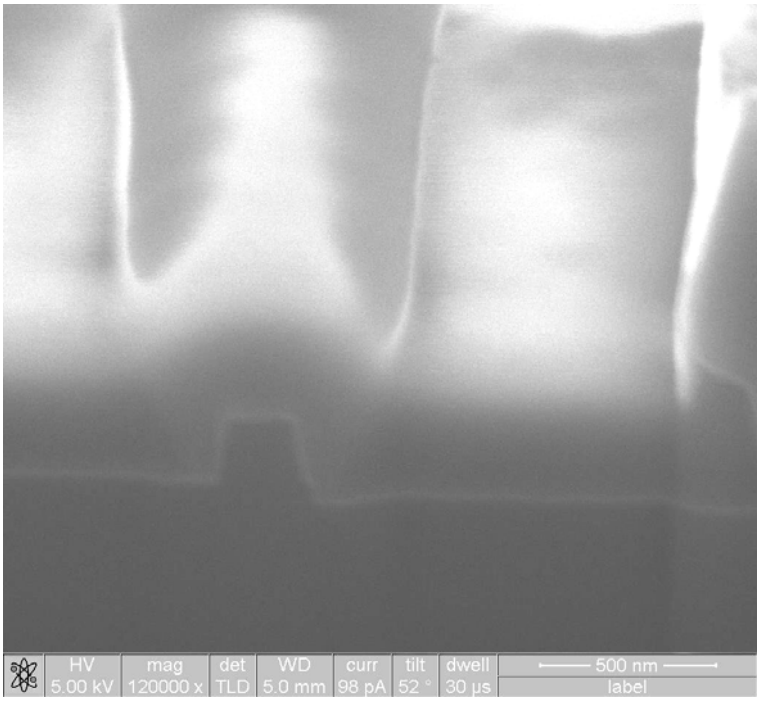


Fig. 3.1 FIB image of a double patterning gate with nominal length $L_{mask} = 0.3\ \mu m$.

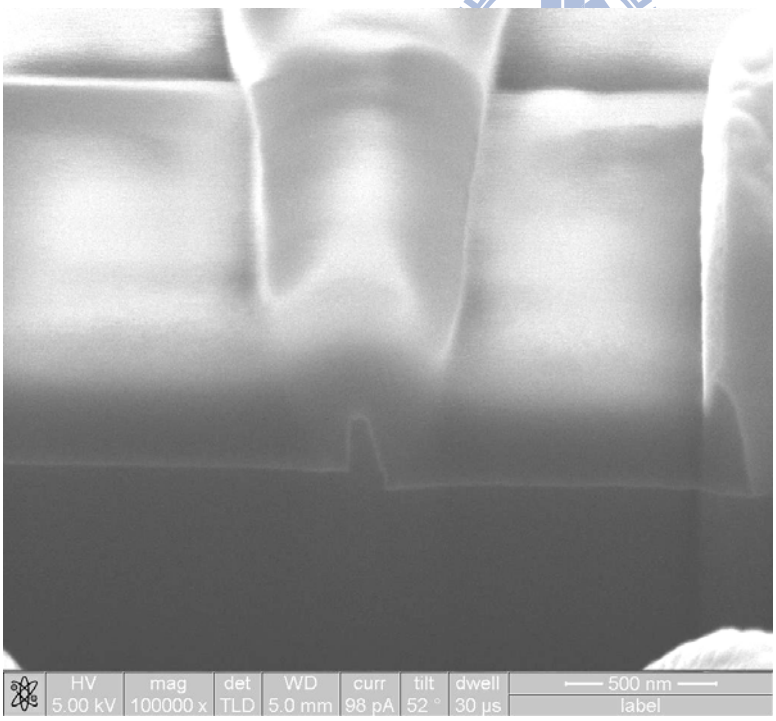


Fig. 3.2 FIB image of a double patterning gate with nominal length $L_{mask} = 0.2\ \mu m$.

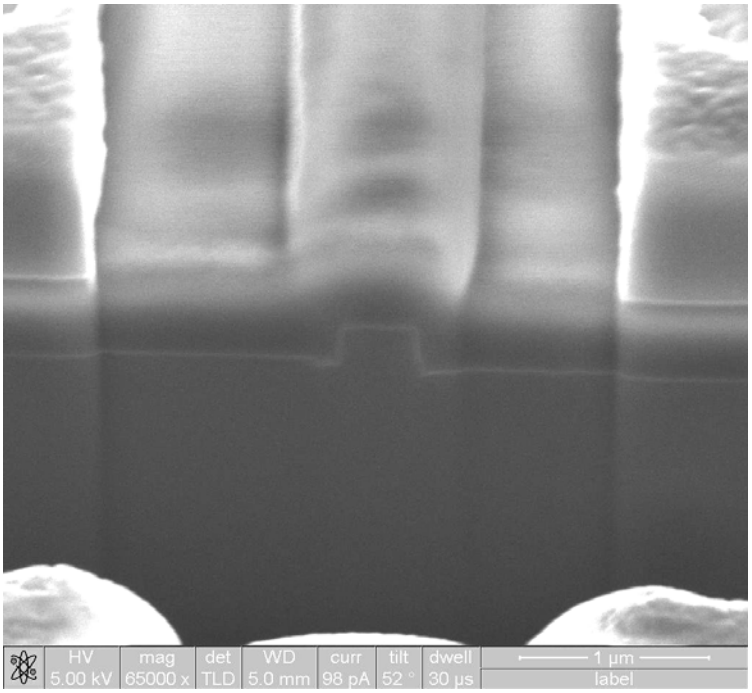


Fig. 3.3 FIB image of a double patterning gate with nominal length L_{mask} = 0.5 μm

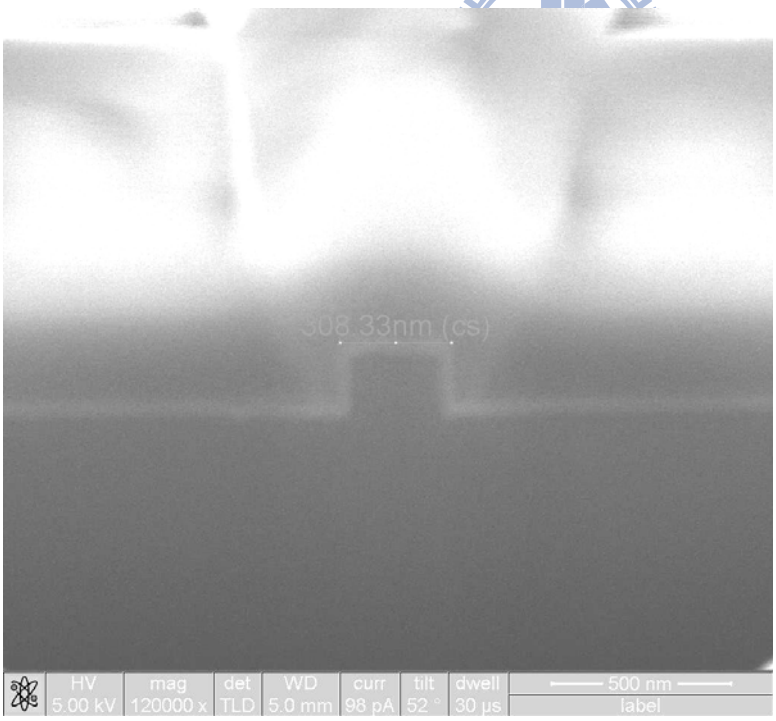


Fig. 3.4 FIB image of a single patterning gate with nominal length L_{mask} = 0.35 μm.

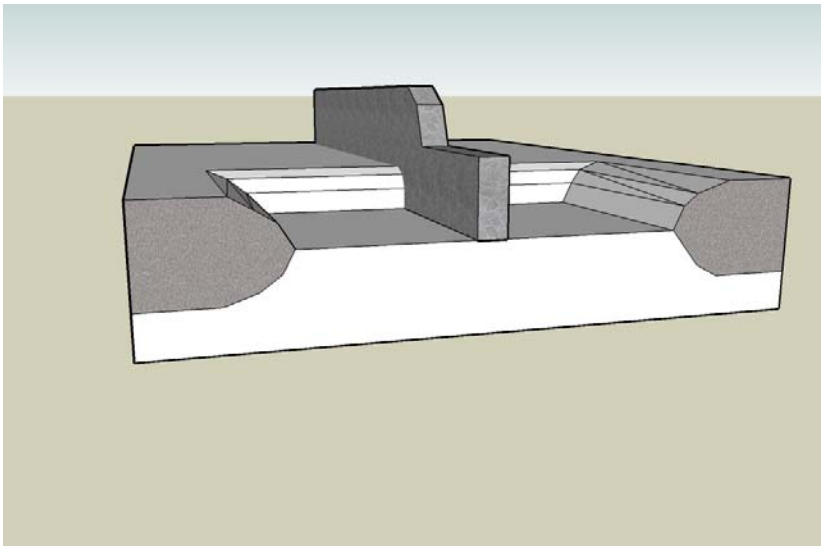


Fig. 3.5 The schematic diagram of a conventional MOSFET adopting single -patterning.

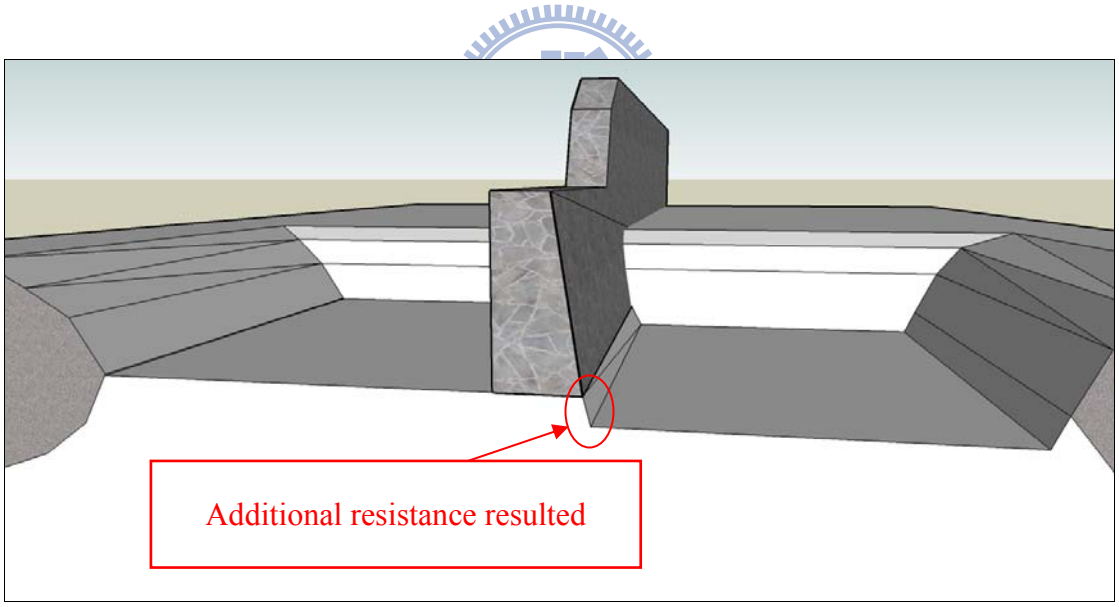


Fig. 3.6 The schematic diagram of the double-patterning MOSFET.

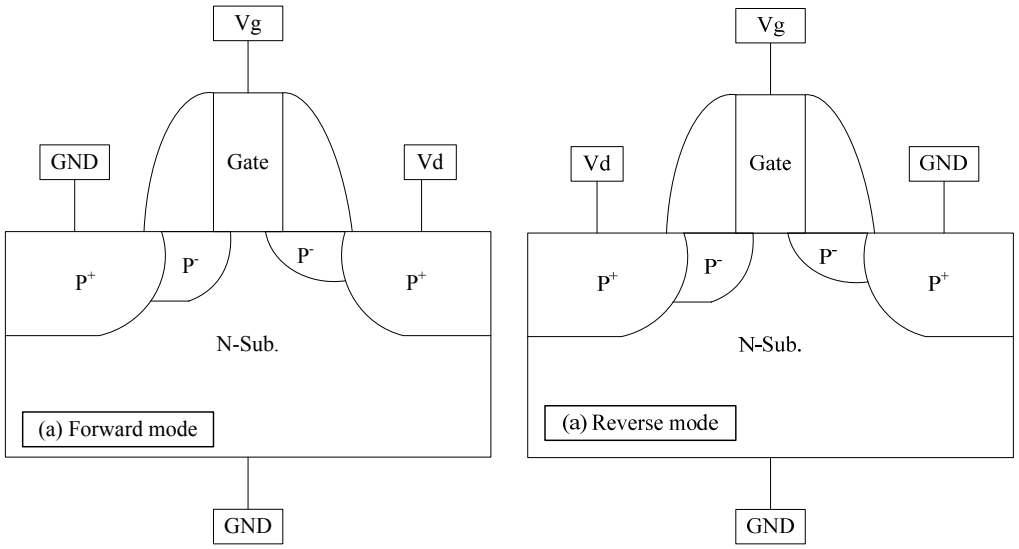
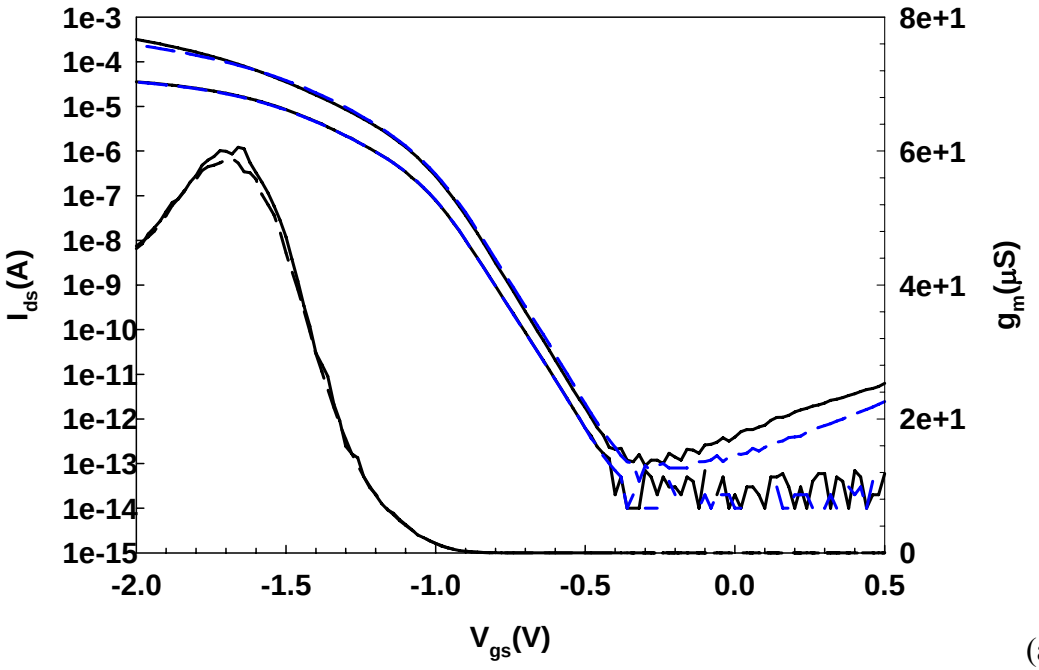
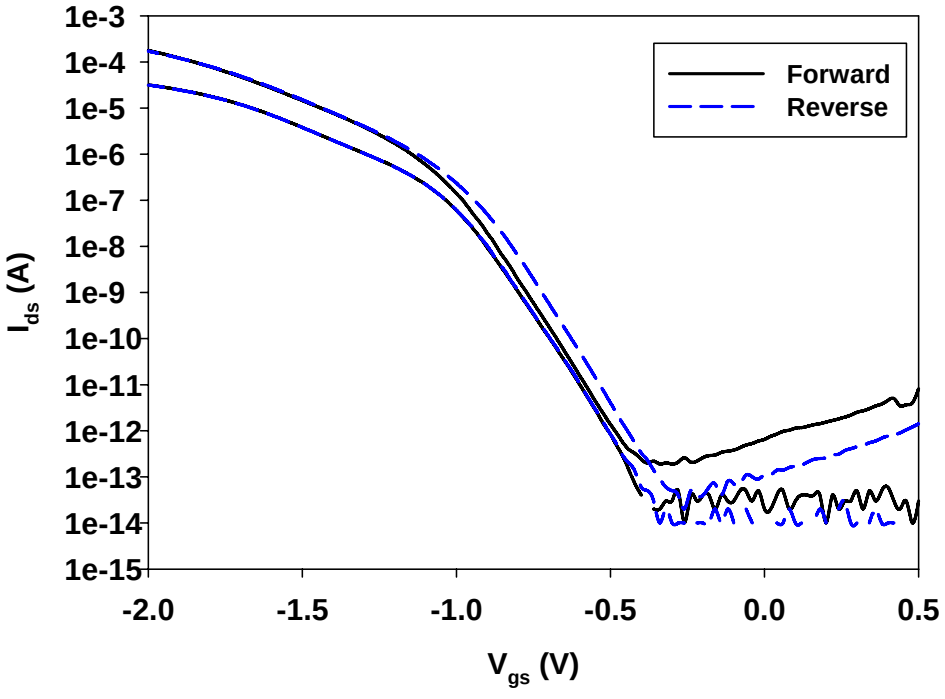


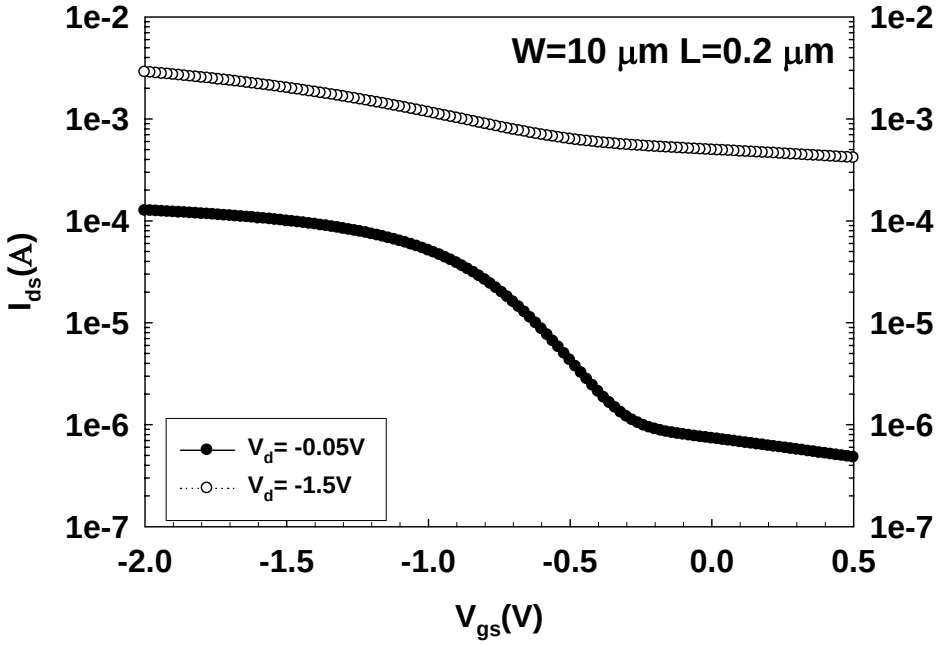
Fig. 3.7 Forward and reverse modes of bias configuration for device characterization.


1e-3
1e-4
1e-5
1e-6
1e-7
1e-8
1e-9
1e-10
1e-11
1e-12
1e-13
1e-14
1e-15
I_ds(A)
8e+1
6e+1
4e+1
2e+1
0
g_m(μS)
-2.0
-1.5
-1.0
-0.5
0.0
0.5
V_gs(V)

(a)

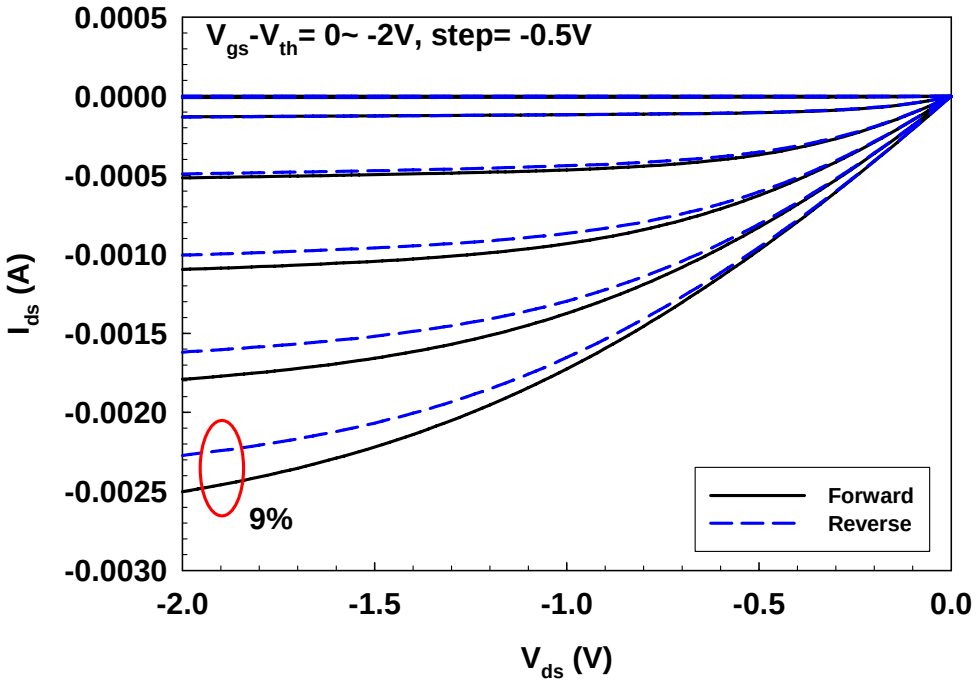

1e-3
1e-4
1e-5
1e-6
1e-7
1e-8
1e-9
1e-10
1e-11
1e-12
1e-13
1e-14
1e-15
I_ds (A)
Forward
Reverse
-2.0
-1.5
-1.0
-0.5
0.0
0.5
V_gs (V)

(b)

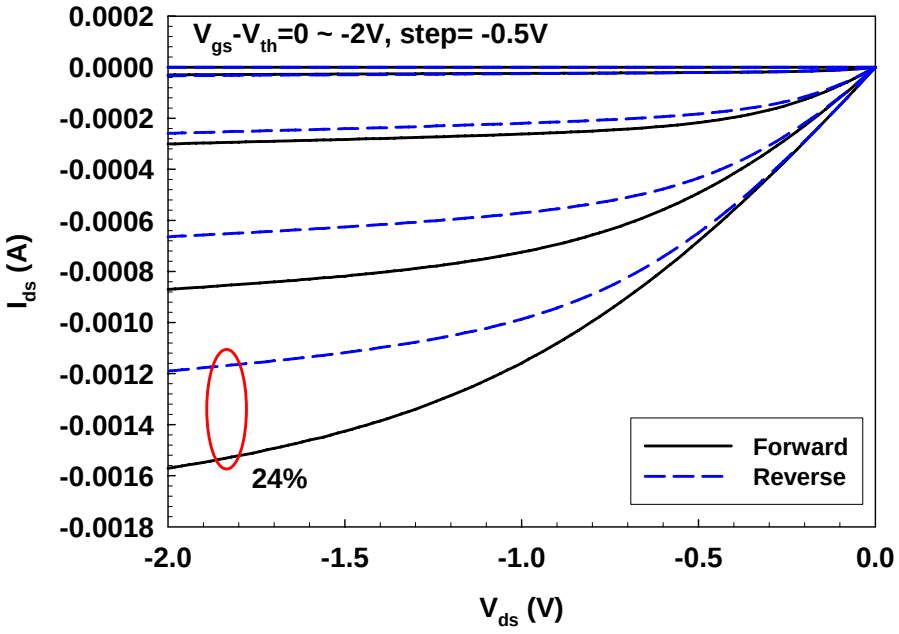


(c)

Fig. 3.8 (a) Sub-threshold characteristics and transconductance of type C and (b) type D PMOSFET under forward and reverse modes of operation. L = 0.3 μ m, W= 10 μ m. (c) Sub-threshold characteristics of a short-channel PMOSFET. L= 0.2 μ m, W=10 μ m



(a)



(b)

Fig. 3.9 $I_d - V_d$ characteristics of (a) a nominal symmetric and (b) an asymmetrical PMOSFET fabricated with double patterning technique under forward and reverse modes of operation. L= 0.3 μm, W = 10 μm.

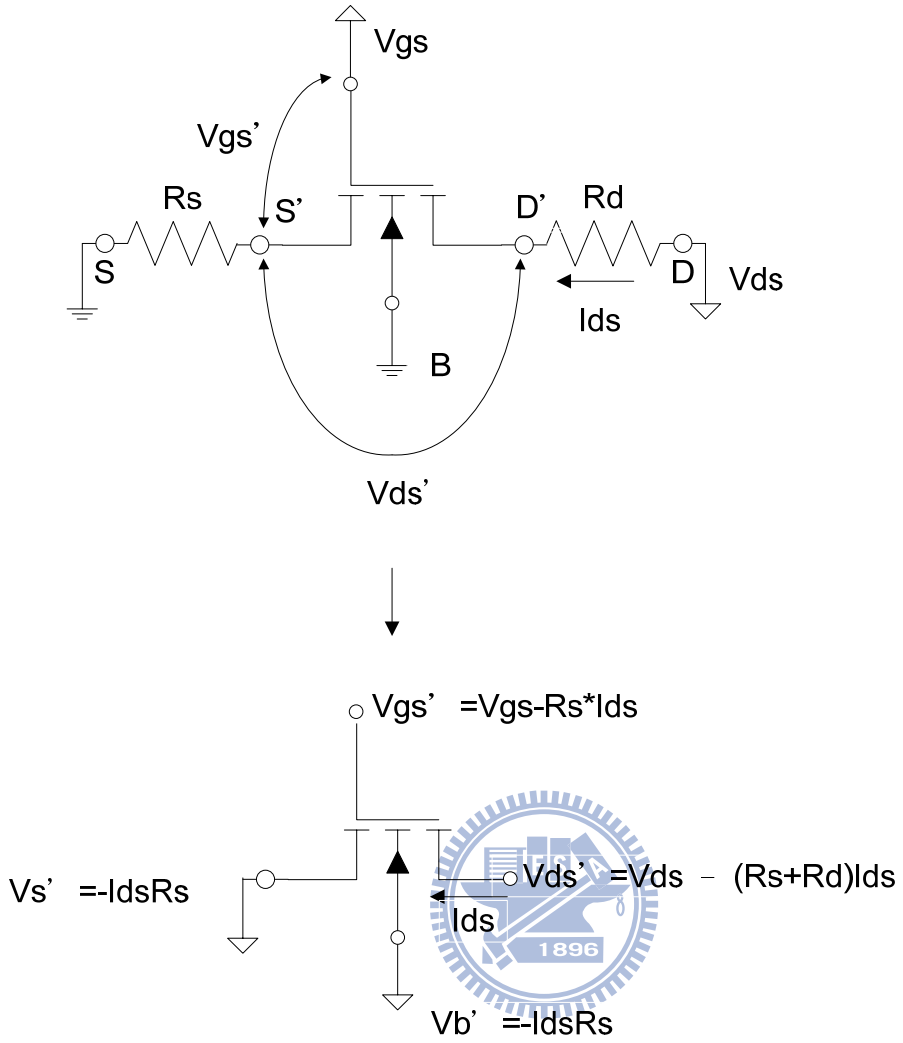
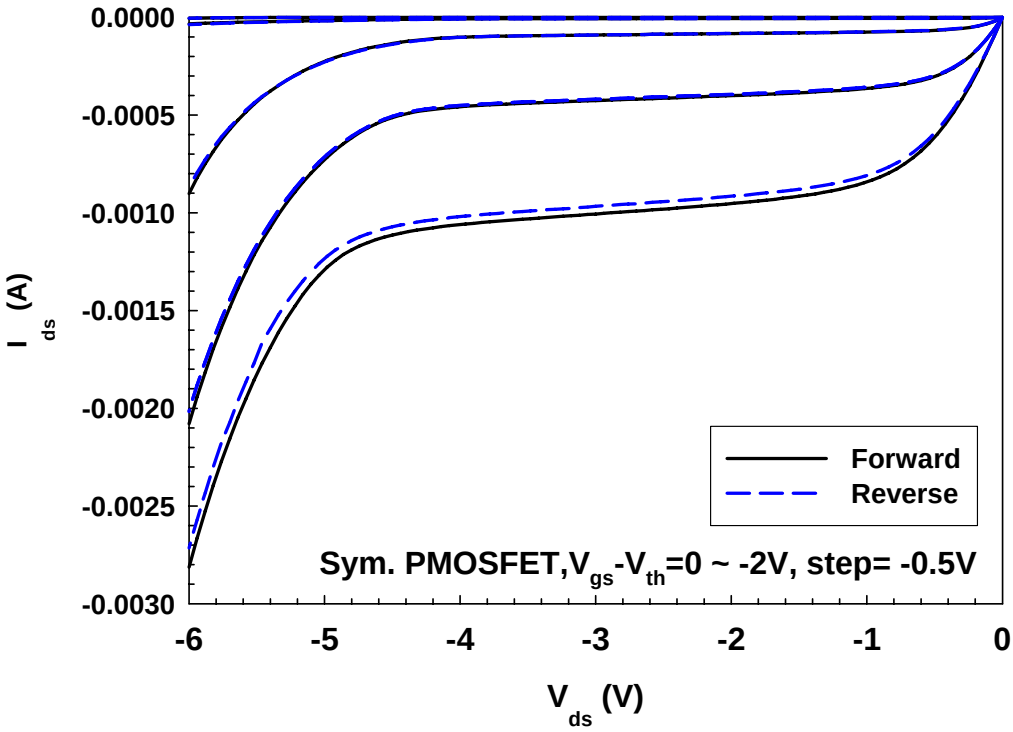
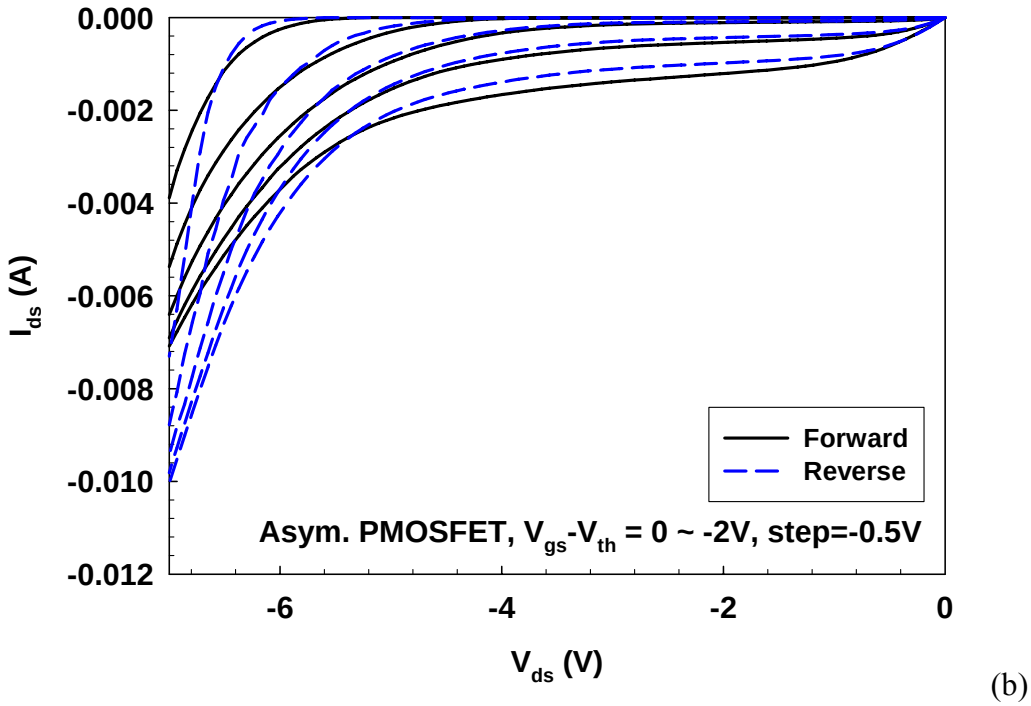


Fig. 3.10 Equivalent circuit of MOSFET with source and drain series resistance [1].



(a)



(b)

Fig. 3.11 $I_d - V_d$ characteristics of (a) a nominal symmetric and (b) an asymmetrical PMOSFET operated under forward and reverse modes. L = 0.3 μm, W = 10 μm.

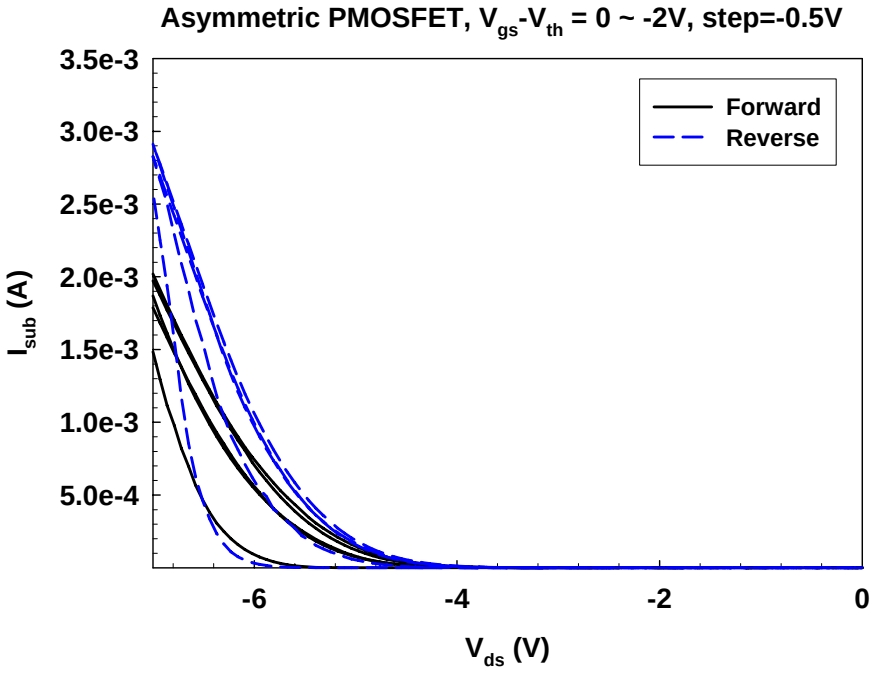


Fig. 3.12 $I_{sub} - V_d$ characteristics of the asymmetric PMOSFET characterized in Fig. 3.11(b) under forward and reverse modes of operation.

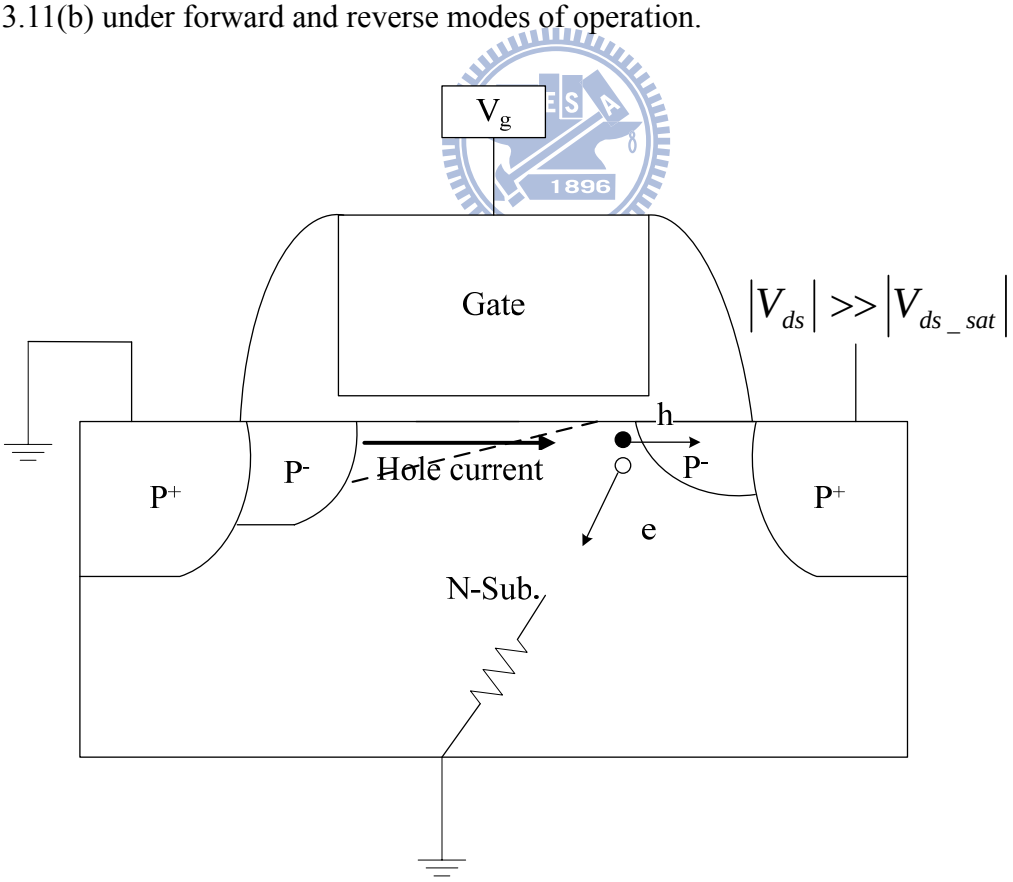


Fig. 3.13 Schematic diagram of impact ionization induced at drain.

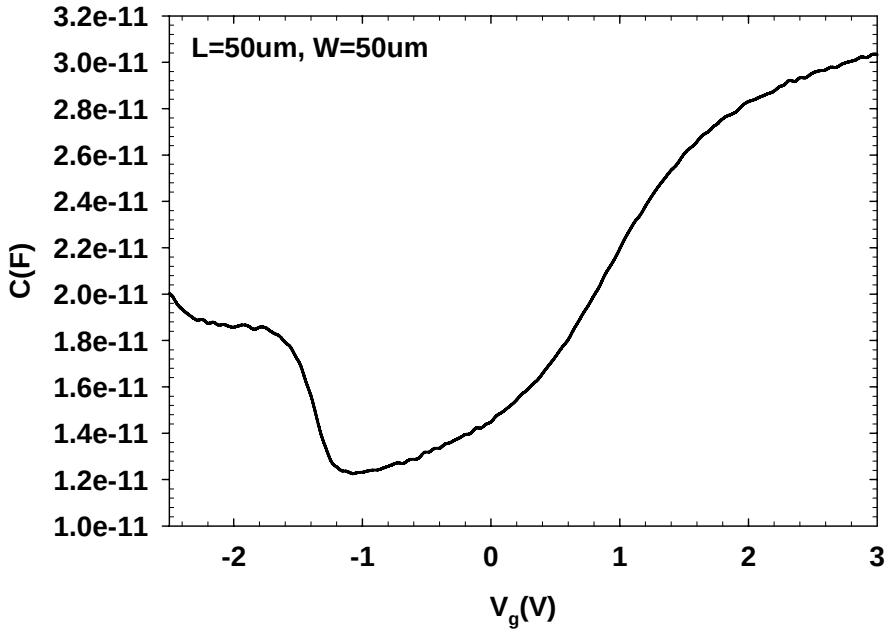
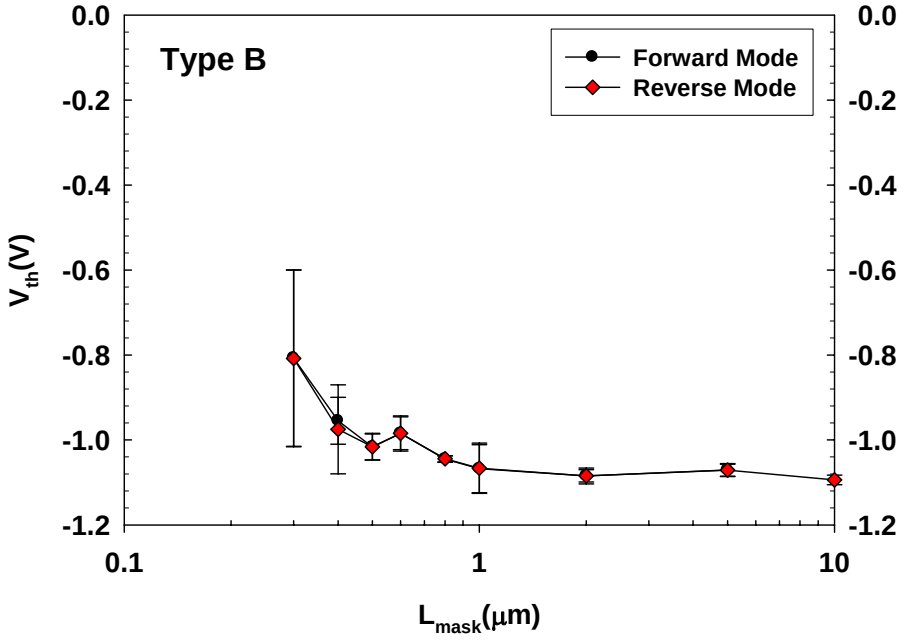
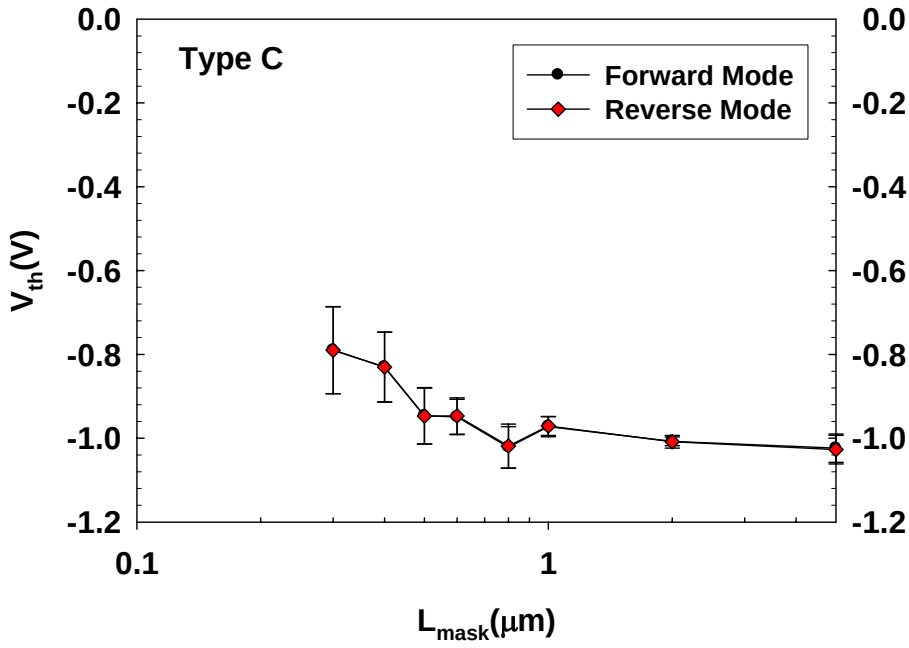


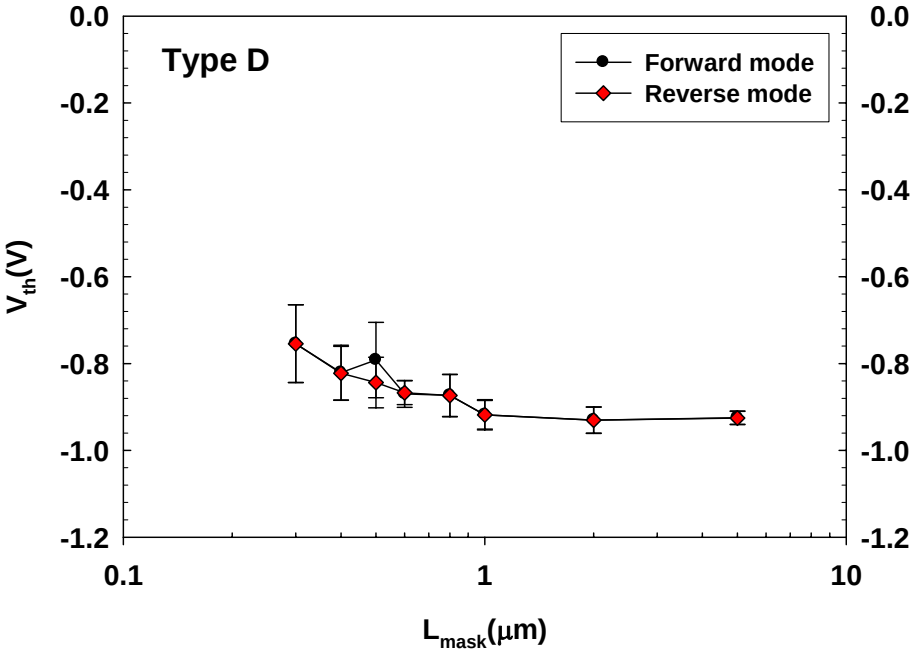
Fig. 3.14 Measured capacitance-voltage (C-V) characteristics of an asymmetric PMOSFET. The measurement frequency is 100 kHz


Type B
Forward Mode
Reverse Mode
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
0.1
1
10
V_{th}(V)
L_{mask}(μm)

(a)


Type C
Forward Mode
Reverse Mode
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
0.1
1
V_{th}(V)
L_{mask}(μm)

(b)



(c)

Fig. 3.15 Threshold-voltage (V_{th}) roll-off of (a) Type B, (b) Type C, and (c) Type D devices. V_{th} is extracted at V_d of -0.05 V under forward mode and reverse mode, respectively.

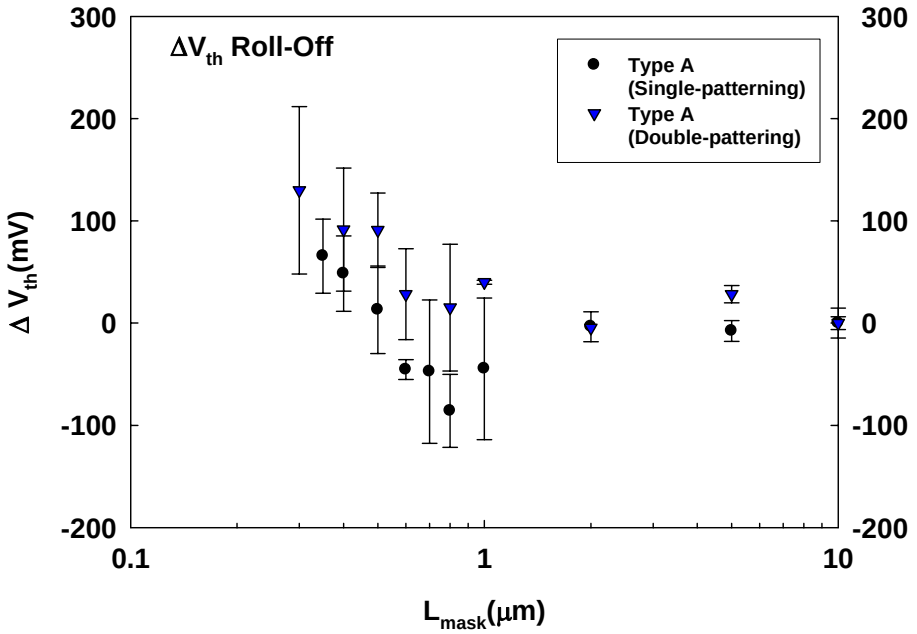


Fig. 3.16 Short-channel effects of Type-A devices fabricated with single-patterning and double patterning.

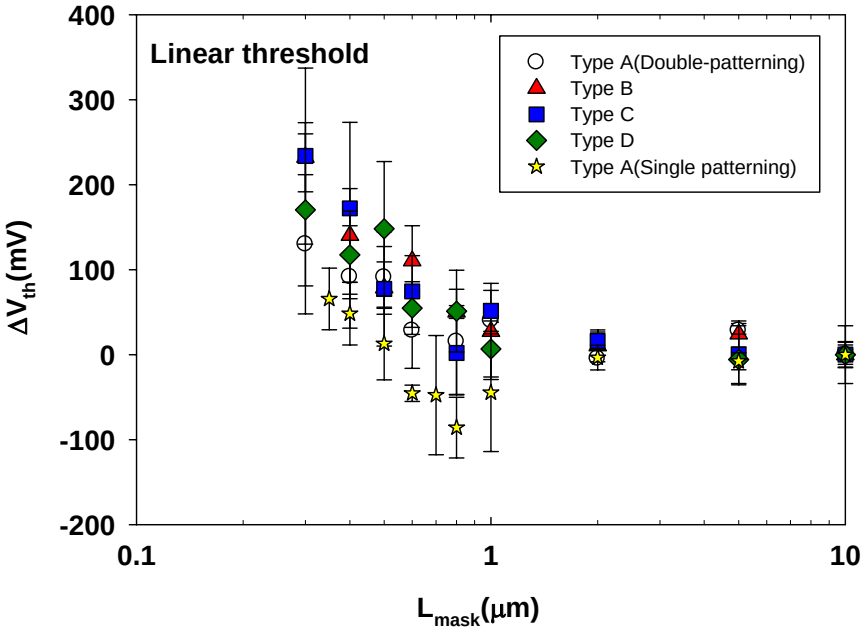


Fig. 3.17 Short-channel threshold voltage roll-off effects for all types of structures. Threshold voltages are measured at low drain voltage. Type A with double-patterning (open circle symbols), Type B with double-patterning (triangle symbols), Type C with double-patterning (rectangular symbols), Type D with double-patterning (diamond symbols), Type A with single-patterning (star symbols) are also shown.

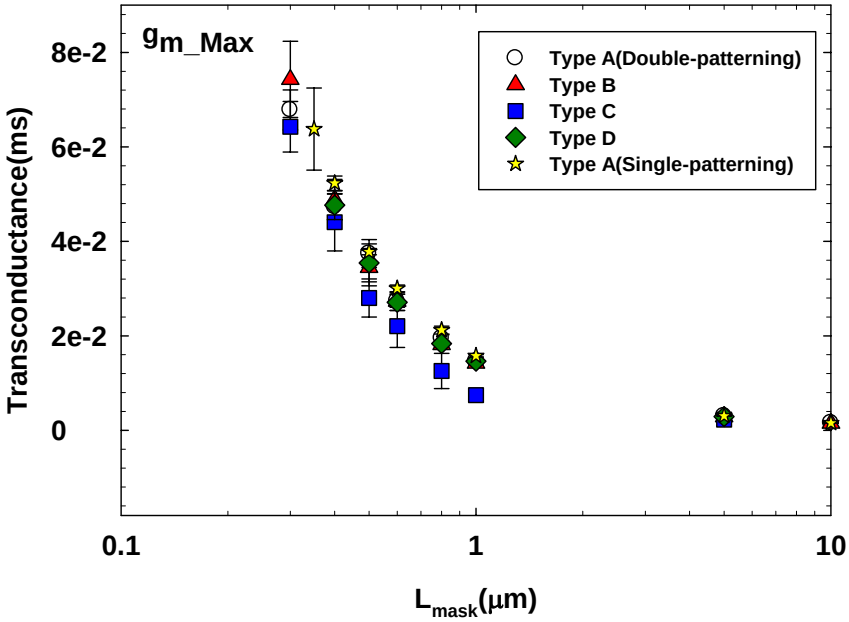
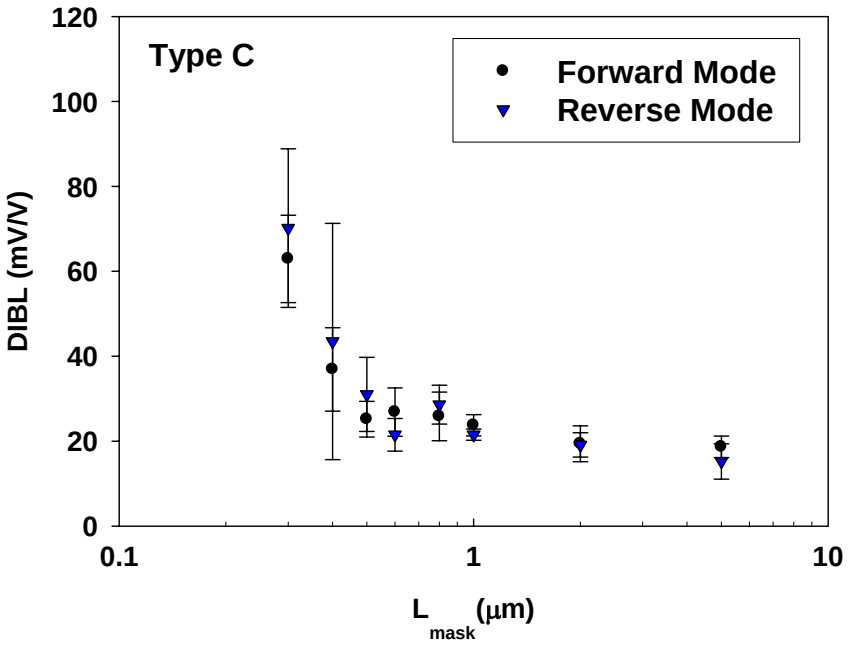


Fig. 3.18 Measured transconductance versus channel length for all splits of devices.



le (circle symbols) and reverse mode (triangle symbols) for Type C devices.

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論文題目：利用雙重微影成像法製作非對稱 P 型金氧半場效電晶體之研究

Fabrication of Asymmetric PMOSFETs with Double-Patterning Technique