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應用於射頻/類比電路的三氧化二鑭
金屬−絕緣層−金屬電容之特性研究

Study on Lanthanum Oxide Metal-Insulator-Metal
Capacitor for Radio-Frequency/Analog Applications

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摘 要

在本篇論文中，我們使用高介電常數的三氧化二鑭絕緣層，來製作應用於高頻或類比電路的低溫金屬-絕緣層-金屬(金氧金)電容。然後深入探究其操作原理，和實際應用面上所產生的問題，包含漏電流和其傳導機制、類比特性和其訊號失真機制、受電應力行為和劣化過程，以及介電絕緣層崩潰和可靠度特性探討等。

首先，就三氧化二鑭絕緣層電流的傳導機制而言，它不像傳統二氧化矽絕緣層般，有這麼明確的載子傳輸行為。因為此三氧化二鑭介電質屬於低溫製備，擁有許多的缺陷密度和介面態在能隙中，致使其傳導機制較複雜且需要被修正。第二，此三氧化二鑭金氧金電容的電容密度與外加電壓、溫度和頻率之間的關係亦在此論文中詳加探討。有鑑於過往研究對描述這些關係之背後成因的論點分歧，我們從高介電常數絕緣層最根本的介電行為：極化與鬆弛的角度來切入。於是歸結出，電容的電壓係數主要受空間電荷的極化與鬆弛影響，而電容的溫度係數則最主要受控於電偶極的極化和鬆弛行為。而此電容在定電壓應力測試中，因為電應力會造成缺陷的產生，進而降低空間電荷的遷移率，導致其電容的電壓係數降低。反之，缺陷引發的電偶極極化效應則促使電容的溫度係數增加。由此可進一步證實，這兩種機制主宰了高介電常數金氧金電容之類比特性的精確度。

接下來，我們討論此三氧化二鑭金氧金電容之電應力行為及其時間依存性可靠度的分析。由實驗結果可歸納得，三氧化二鑭金氧金電容在定電壓應力下的劣化機制是缺陷

產生與電荷補捉，這可借由量測低電場中的應力誘生漏電流及偵測出應力貢獻的電容密度變化來分別確定。我們也觀察到三氧化二鑭金氧金電容在定電壓應力下的二階段時間依存性崩潰現象，這歸因於金屬與介電質間的界面層先崩潰並導致劇烈的電荷補捉與釋放效應，爾後介電質本體也隨之崩潰。這層不可避免的界面層是因高介電常數介電薄膜直接沉積在金屬表面上所形成，由於它原本就具有較高的缺陷密度而易於崩潰，於是當介電層微縮時因它的不可微縮性就變成一個可靠度的問題。是故，界面層較高的初始缺陷密度不僅影響金氧金電容的漏電流和類比特性，在元件失效上亦佔有舉足輕重的地位。

最後，本實驗所製作的低溫十奈米三氧化二鑭金氧金電容，其具有低漏電流（在外加電壓−1 V時為 9.4 nA/cm^2），很高的崩潰電場（在 25 °C時大於 7 MV/cm)，低的電容電壓係數(頻率在 100 kHz時為 671 ppm/V^2)，足夠高之電容密度(11.4 fF/μm^2)，以及高度穩定性和良好的可靠度等眾多優良特性。因此，鑭系高介電常數絕緣層金氧金電容是超大型積體電路技術中後段的射頻和類比電路裡最具潛力的被動元件。

Study on Lanthanum Oxide Metal-Insulator-Metal Capacitor for Radio-Frequency/Analog Applications

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Abstract

In this study, the low-temperature metal-insulator-metal (MIM) capacitor with the high dielectric constant (high-k) lanthanum oxide (La_2O_3) film deposited by electron beam (e-beam) evaporation was fabricated and characterized for radio frequency (RF) and analog applications. The operational principles and the implementation issues of the high-k La_2O_3 MIM capacitor are discussed, including leakage current and conduction mechanisms, analog properties and distortion mechanisms, stress behaviors and degradation processes, as well as dielectric breakdown and reliability characteristics.

To begin with, we evaluate the conduction mechanisms for high-k La_2O_3 MIM capacitors. Unlike the conventional SiO_2 MIM capacitor where the quantum-mechanical tunneling is pronounced, the trap-related mechanisms are important for high-k MIM capacitors with low temperature fabrication, due to the high trap and interface state density in the high-k dielectric. Secondly, the effects of voltage, temperature, and frequency on the capacitance of high-k La_2O_3 MIM capacitors are investigated in detail on the basis of fundamental high-k dielectric behaviors: polarization and relaxation. The space charge polarization and relaxation are principally responsible for the positive voltage coefficient of capacitance (VCC). However, the dipolar polarization and relaxation dominate the positive

temperature coefficient of capacitance (TCC). Interplay of these two effects on analog characteristics is crucial for developing the precise MIM capacitors with high-k dielectrics. The changes in VCC and TCC caused by the constant voltage stress (CVS) also verify the above inferences. VCC decreases since the space charge mobility reduced by stress induced traps, but TCC increases because the quantity of trap induced dipoles grows during stress.

Furthermore, the stress behaviors and the reliability issues of high-k La_2O_3 MIM capacitors under various CVS conditions are also studied. The wear-out mechanisms of La_2O_3 MIM capacitors during electrical stress are trap generation and charge trapping. This could be identified by measuring the stress induced leakage current (SILC) at low field and by detecting the capacitance variation under electrical stress, respectively. Moreover, the very distinct two-step time-dependent dielectric breakdown caused by CVS testing could be observed. It is ascribed to firstly the interfacial layer (IL) breakdown leading to the severe charge trapping/detrapping, followed by the breakdown of the bulk high-k layer. Therefore, the high intrinsic defect density in the IL not only affects the leakage current and analog characteristics of MIM capacitors, but also plays an important role on the device failure rate.

In summary, a highly stable and reliable 10-nm La_2O_3 MIM capacitor with low leakage current (9.4 nA/cm^2 at −1 V), high breakdown strength (> 7 MV/cm at 25 °C), small VCC (671 ppm/V^2 at 100 kHz), low thermal budget (≤ 400 °C), and sufficient high capacitance density (11.4 fF/μm^2) has been successfully demonstrated. The results highlight the promise of the La-based high-k MIM capacitors as the next-generation passive component in RF/analog circuits.

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CHAPTER 1

INTRODUCTION

Recently, metal-insulator-metal (MIM) capacitors integrated into the backend metal interconnect level as passive components have been generated great interest for radio frequency (RF) and analog applications within Si integrated circuits (ICs) [1], [2]. For example, MIM capacitors are widely used for RF bypass and decoupling capacitors [3]-[5] or for digital-to-analog (D/A) and analog-to-digital (A/D) converters [6] due to their high conductive electrodes and low parasitic capacitance [7], [8]. Because the metal-oxide-semiconductor (MOS) capacitor usually consumes a large fraction of the whole chip area, the MIM capacitor with high capacitance density have been eagerly anticipated to reduce chip size and system cost [9]. However, since the leakage and reliability issues limit the aggressive thickness scaling, the higher capacitance density of MIM capacitors cannot be achieved by further thinning the conventional silicon dioxide (SiO_2) or silicon nitride (SiN) films [10]. Therefore, the only one choice is adopting high dielectric constant (high-k) materials as dielectrics of MIM capacitors.

In the last few years, many high-k dielectrics, such as Ta_2O_5 [11], HfO_2 [12], Al_2O_3 [13], TiO_2 [14], various compound of these materials [15]-[17], and combinations of these dielectrics as sandwich or laminate structures [18]-[20], have been investigated for MIM capacitors. Unfortunately, in spite of possessing higher capacitance density, many obvious drawbacks become the challenges for developing the high-k MIM capacitors, as described below. Fig. 1-1 shows that the trend of dielectric bandgap declines with the increase of dielectric constant [21]. Besides, the empirical data about the dielectric constant (k), the energy bandgap (E_g), and the conduction band offset with respect to the Si (E_{CB}) of various high-k dielectrics are summarized in Table 1-1 [22]. The low energy bandgap and the small

conduction band offset of high-k dielectric with respecting to the metal electrode result in larger leakage current and higher power dissipation, compared to conventional SiO_2 MIM capacitors. Secondly, it has been reported that the capacitance of the MIM capacitor with high-k dielectric would sensitively vary with the operational voltage, the temperature, and the frequency leading to distortion in analog signals for RF/analog applications [11]-[13], [15]-[20], which ultimately limit the performance of circuits. Although several studies have made efforts to discuss these phenomena [6], [23]-[25], the physical mechanisms of these influences on capacitance are still unclear. Accordingly, the large dependence of capacitance on voltage, temperature, and frequency is remaining a question for high-k MIM capacitors, and it is necessary to investigate and solve. Thirdly, earlier researches stated that the electric breakdown strength of MIM capacitors reduces sharply with the increase of dielectric constant [26], [27]. Besides, unlike the SiO_2 which is an almost ideal insulating oxide, the high-k dielectrics usually have high trap density in themselves and they have lots of interface states with electrode to cause the instability and unreliability of devices during operation [28]-[31]. Hence, from the view point of practical use, the electrical stress induced degradation and the breakdown strength of high-k MIM capacitors are serious concerns. However, a few researches have evaluated the wear-out behaviors and the statistical reliability results of high-k MIM capacitors, especially for high capacitance density (> 10 fF/μm^2) MIM capacitors. Therefore, the points mentioned above have to further study to improve the performance of high-k MIM capacitors.

According to the International Technology Roadmap for Semiconductor (ITRS) [32], as shown in Table 1-2, the RF MIM capacitors have to meet the following main demands: (1) high capacitance density (> 5 fF/μm^2), (2) low leakage current ($< 10^{-8}$ A/cm^2), (3) high breakdown electric field (holding at least a voltage bias of 5 V), (4) very small voltage linearity (< 100 ppm/V^2), and (5) low dielectric loss [$\tan\delta < 0.05$, i.e., Q factor ($=1/\tan\delta$) >20]. Moreover, since the high-k MIM capacitor for RF/analog applications is located in the

interconnection levels and above the active integrated circuit layers, the maximum fabrication process temperature is limited to 400 °C to fulfill the low thermal budget requirement of the very large scale integrated circuits (VLSI) backend process.

To replace conventional SiO_2 and SiN dielectric materials, a new suitable dielectric can be selected in terms of energy bandgap and dielectric constant, which are usually trade-off for high-k materials, as depicted in Fig. 1-1 and Table 1-2. A considerable number of studies have been conducted on hafnium (Hf) or zirconium (Zr) based oxide, but Hf or Zr based oxide does not meet the requirement of next generation where the equivalent oxide thickness (EOT) of dielectric needs less than 1 nm. Therefore, the other alternative dielectrics, rear-earth metal oxides (REOs), are being focused. And, the energy bandgaps of REOs are also revealed in Fig. 1-2 [33].

Among the REOs, lanthanum oxide (La_2O_3), or named as Lanthana, has the highest potential to achieve less than 1-nm equivalent oxide thickness (EOT) [34]. In addition, various superior characteristics of thin La_2O_3 film have been reported, including a large bandgap (> 5 eV) [34], [35], a relatively high dielectric constant (20-30) [34], [36], [37], a high breakdown electric field [27], [38], a low interface state density [34], [36], a low leakage current with small EOT [34], and a good oxide reliability [39]. As a result, the La-based oxide is the most promising candidate for the next technology node. However, up to present, the investigation on La_2O_3 MIM capacitors is very little [3], [40], and the characteristics of La_2O_3 MIM capacitors, such as stress behaviors, breakdown, and reliability issues, are unclear and essential to demonstrate. Consequently, we adopt the La_2O_3 as the dielectric of MIM capacitors to study in detail in this work, and we could establish a base to develop and really carry out the high performance La-based high-k MIM capacitors for RF/analog applications in the future.

The objective of this thesis is to achieve a fundamental understanding of the working principles and the implementation issues of the La_2O_3 high-k MIM capacitors for VLSI

backend applications. The innovation and major topics of this research are addressed as following. For one thing, although there are several reports on the electrical properties of La_2O_3 thin films on the basis of MOS structure [37], [41], [42], the conduction mechanisms of the lanthanum oxide are not fully understood, and the conduction behaviors of La_2O_3 high-k MIM capacitors have not been evaluated yet. Thus, we measure the leakage current of 10-nm La_2O_3 MIM capacitors and analysis the conduction mechanisms at various temperatures. What is more, the capacitance of high-k MIM capacitors sensitively varies with applied voltage, temperature, and frequency, which could be depicted by quadratic voltage coefficient of capacitance (α), temperature coefficient of capacitance (TCC), and frequency coefficient of capacitance (FCC). However, the opinions about origins of these phenomena are widely divided and unclear. Therefore, we study it in detail and discuss physical mechanisms, according to the high-k dielectric behaviors, for instance, dielectric polarization and relaxation. In terms of factors that induce α, TCC, and FCC, we suggest the possible solutions to improve the analog distortion events for high-k La_2O_3 MIM capacitors.

Additionally, despite the trap-rich nature for high-k dielectrics would cause the instability and unreliability of devices during operation, the study on degradation and reliability characteristics for La_2O_3 MIM capacitors under electrical stress is still an undeveloped field. As a result, we demonstrate the long-term evolution of the leakage current and the capacitance for 10-nm La_2O_3 MIM capacitors under constant voltage stress (CVS). We also observe the variation in α and TCC under CVS, which further clarify the physical origins of it. Finally, we inquire the time-dependent dielectric breakdown (TDDB) and the time-zero dielectric breakdown (TZDB) of La_2O_3 MIM capacitors to verify the lifetime and the breakdown strength of the dielectrics of fabricated MIM capacitors.

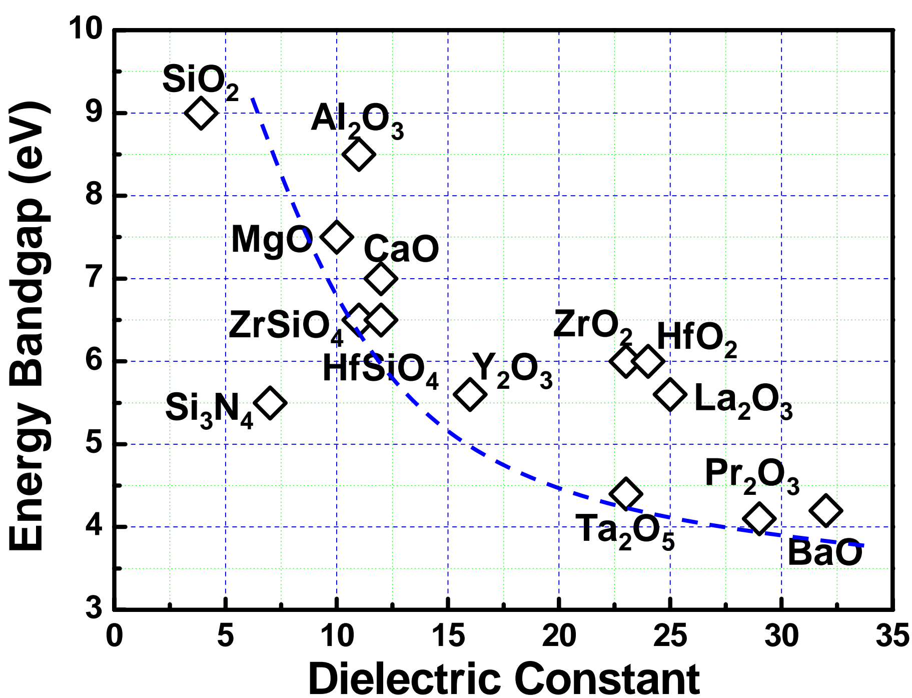


Fig. 1-1. The bandgap as a function of dielectric constant for various candidate oxides [21].

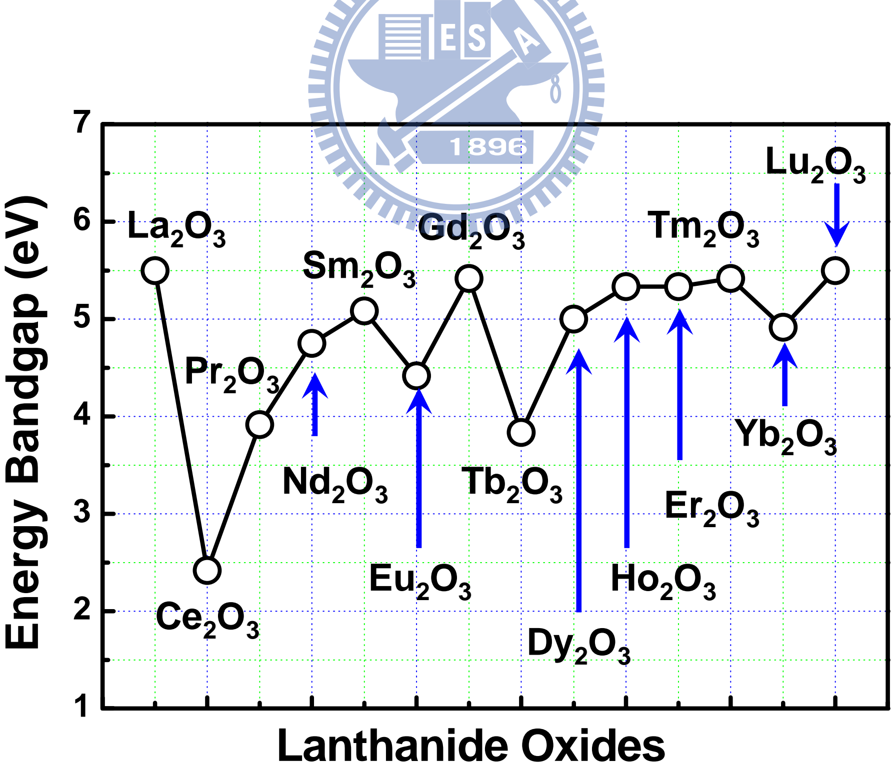


Fig. 1-2. Energy bandgap versus various rear-earth metal oxides (REOs) [33].

Table. 1-1. The empirical data about dielectric constant, energy bandgap, and conduction band offset with respect to the Si of various high-k dielectrics [22].

Dielectric	Dielectric Constant	Bandgap (eV)	Conduction band offset
SiO_2	3.9	9	3.5
Si_3N_4	7	5.3	2.4
Al_2O_3	~10	8.8	2.8
Ta_2O_5	25	4.4	0.36
La_2O_3	~21	6	2.3
Gd_2O_3	~12	---	---
Y_2O_3	~15	6	2.3
HfO_2	~20	6	1.5
ZrO_2	~23	5.8	1.4
$SrTiO_3$	---	3.3	~0.1

Table. 1-2. Requirements for RF MIM capacitors according to ITRS [32].

Metal-Insulator-Metal Capacitor						
Year of Production	2008	2010	2012	2014	2016	2018
C (fF/μm^2)	4	5	5	7	10	10
VCC (ppm/V^2)	<100	<100	<100	<100	<100	<100
Leakage (A/cm^2)	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$	$<10^{-8}$
Matching (%-μm)	0.5	0.4	0.4	0.3	0.2	0.2
Q (5GHz for 1pF)	>50	>50	>50	>50	>50	>50

CHAPTER 2

GENERAL BACKGROUNDS AND LITERATURES REVIEW

In this chapter, we first give a introduction on high-k dielectric conduction mechanisms, including Schottky emission (SE), Poole-Frenkel (PF) emission, space-charge-limited current (SCLC), and the conductions related to high trap density insulator. Secondly, section 2.2 describes dielectric behaviors comprise dielectric polarization and dielectric relaxation in high-k MIM capacitors. Subsequently, section 2.3 reviews several literatures regarding stress induced variations in properties of MIM capacitors. Finally, section 2.4 states a concise history on reliability improvement of silicon-based devices and then indicates the most interesting reliability issues on MIM capacitors for RF/analog application.

2.1 CONDUCTION MECHANISMS IN HIGH-K DIELECTRICS

Two types of electrons exist and transport in the insulator of MIM capacitor: intrinsic electrons and extrinsic electrons [43]. Intrinsic electrons natively exist in insulator, and extrinsic electrons inject from the nearby electrode to insulator. Because the carrier density of intrinsic electrons inside the insulator is low, the conduction mechanism of intrinsic electrons is like the ohmic type with a large resistivity. However, there are two possible cases in extrinsic electrons. First, the current is only limited by the bulk of insulator due to the unlimited electron sources of the electrodes. Second, if the electrodes restrict the carrier injection, the injection electrons would travel free inside the insulator. According to these two viewpoints, the conduction mechanism in insulator could be classified into bulk-limited and electrode-limited (bulk-free) ones for extrinsic electrons. Tables 2.1 and 2.2 summarize

various bulk-limited and electrode-limited conduction mechanisms, respectively, which are used to investigate the leakage conduction [39], [43]-[53] of our MIM capacitor in this work. Following, the conduction mechanisms of Schottky emission (SE), Poole-Frenkel (PF) emission, space-charge-limited current (SCLC), and some other high trap density related conductions are further described in below subsection.

2.1-1 Schottky Emission

The Schottky effect describes the image-force-induced barrier lowering for charge carrier emission [39]. Fig. 2-1 shows the energy-band diagram between a metal surface and a vacuum level while electron movies close to electrode. The maximum barrier height of vacuum level would be reduced due to the image force at interface of metal Fermi level and vacuum level. The Schottky emission (SE) is analogous to thermionic emission except for the barrier height lowing due to the external field applying. However, this barrier height lowing could help the thermally activated carriers emit from the metal electrode, called Schottky emission. Metal-vacuum system, as shown in Fig. 2-1, is also equivalent to metal-insulator system, except for the dielectric constant of the vacuum part and the insulator part. The main feature of SE is Schottky barrier lowering (or image force lowering) [39].

$$\Delta\phi_B = \sqrt{\frac{qE}{4\pi\varepsilon}} \tag{2-1}$$

Here, permittivity ε should be replaced by an appropriate permittivity characterized by the inserted medium. The tunneling current could be written by [43], [54]-[56]

$$J = \frac{4\pi m^* q}{h^3}\int_{E_m}^{\infty}[f_n(E) - f_n(E+V)]\times[\int_{E_m}^{E} D_t(E_x)\bullet dE_x]\bullet dE\,. \tag{2-2}$$

Here, h is Planck constant, f is Fermi distribution function, D_t is tunneling probability, E_m is barrier height, and V is applied voltage. Since carrier emission occurs at much higher energy level than Fermi level of the injecting electrode, the tunneling probability (D_t) could be

regarded as 1. Then, the integration in Eq. (2-2) yields

$$J = \frac{4\pi m^* q}{h^3}(k_B T)^2 \exp(-\frac{E_m - E_F}{k_B T})[1-\exp(-\frac{V}{k_B T})]. \quad (2\text{-}3)$$

Here, the Schottky barrier lowering modified from Eq. (2-1) could be written as

$$E_m - E_F = \phi_0 - \Delta\phi_B = \phi_0 - \sqrt{\frac{qE}{4\pi\varepsilon_0\varepsilon_i}}. \quad (2\text{-}4)$$

Therefore, the Eq. 2-3 under $V >> k_B T$ condition could be simplified as

$$J = \frac{4\pi m^* q}{h^3}(k_B T)^2 \exp(-\frac{\phi_B}{k_B T})\exp(\frac{\beta_S}{k_B T}E^{1/2}) \quad (2\text{-}5)$$

, where $\beta_S = (\frac{q}{4\pi\varepsilon_0\varepsilon_i})^{1/2}$. Eq. (2-5) is also called Richardson-Schottky equation [72].

The Schottky current is thermally activated process with the activation energy characterized by Eq. (2-4). The activation energy could be modulated by the applied bias with Schottky barrier height lowering effect. One notices that the barrier deformation decreases as the dielectric constant increases, indicating that SE in high-k oxide films seems to be less probable than that in conventional SiO_2 film due to higher lower dielectric constant and much defect density in their self.

2.1-2 Poole-Frenkel Emission

The potential barrier lowering also affects the Poole-Frenkel (PF) emission current while applying an external field. However, the SE is associated with the insulator barrier near to the injection side of the electrode, but the PF effect is associated with barrier at the trap site in the bulk of insulator film. Thus, neutral donor traps, which are neutral when filled but positive when empty, do not experience the PF effect owing to the absence of the Coulomb potential. Fig. 2-2 shows the thermionic emission of trapped carriers occurs at the trap site in the bulk film. Internal thermionic emission is called PF emission, while external one is called Schottky emission. The other way for electron emission is hopping process, which is a kind of tunneling process in a short range. The difference between the SE emission and the PF

emission are summarized in Table 2.3. Here, it should be noted that PF emission is closely related to the oxide film thickness but Schottky emission is not, as far as the equal electric field on dielectric is concerned. Fig. 2-3 illustrates that the restoring force in both Schottky and PF effects comes from Coulomb interaction between the escaping electron and the image charge (positive) [57]. The restoring force due to electrostatic potential makes electron move back to its equilibrium position. Although the restoring force is the same for the escaping electron and the image charge, these charges differ in the positive image charge fixed for PF barriers but mobile fixed with SE. It results in a barrier lowering twice as great for the PF effect, as shown in Eqs. (2-7) and (2-8).

$$\Delta\phi_{PF} = \left(\frac{q^3 E}{\pi\varepsilon\varepsilon_0}\right)^{1/2} = \beta_{PF} E^{1/2} \quad (2\text{-}7)$$

$$\Delta\phi_{S} = \left(\frac{q^3 E}{4\pi\varepsilon\varepsilon_0}\right)^{1/2} = \beta_{S} E^{1/2} \quad (2\text{-}8)$$

In that the electrons have enough energy to go over the energy barrier and travel in the conduction band with a mobility μ dependent on the scattering with the lattice, the general expression of the bulk current is expressed by [43]

$$J = qn(x)\mu E\ . \quad (2\text{-}9)$$

The concentration of free carriers in the insulator is

$$n = N_C \exp\left[-\frac{q}{kT}(E_C - E_F)\right]. \quad (2\text{-}10)$$

Since E_C–E_F is equal to the effective trap barrier height, including the barrier lowering effect described by Eq. (2-7), the effective barrier height and the current governed by the PF emission are written by Eqs. (2-11) and (2-12), respectively.

$$E_C - E_F = \phi_S - \Delta\phi_{PF} = \phi_S - \beta_{PF} E^{1/2} \quad (2\text{-}11)$$

$$J = qN_C \exp\left(-\frac{\phi_S}{kT}\right)\exp\left(\frac{q\beta_{PF}}{k_B T} E^{1/2}\right)\mu E \quad (2\text{-}12)$$

On the other hand, the PF emission will lower the barrier height of dielectric film when the dropping field is higher than the critical field [58] as

$$E_{crit} = (\frac{\phi_i}{\beta_{PF}})^2 \quad (2\text{-}13)$$

, where ϕ_i is the trap barrier height at zero oxide field. At electric field higher than $E_{crit.}$, the emission process, instead of bulk-process, begins to play a dominant role.

2.1-3 Space-Charged-Limited Current

Space-charge-limited current (SCLC) model has been developed and used continuously over four decades. Until now numerous attempts have been reported to interpret the current behavior of thin films within the frame of SCLC. Such films are porous SiO_2 [59]-[61], TiO_2 [62], organic materials [63], porous silicon [64], [65], SiO_2/Nitride [66], Si_3N_4 [67], [68], $SrTiO_3$ [69]-[72], Ta_2O_5 [59], [73], Al_2O_3 [74]-[76], Nb_2O_5 [77], and Nd_2O_3 [78], Gd-In-oxide [79], Dy_2O_3 [80], [81], and La_2O_3 [82] in rare-earth metal oxides.

Fig. 2-4 shows the thermal equilibrium and the quasi-thermal equilibrium (i.e., steady-state) of electrons in the conduction band and in the trap levels of the dielectric film, respectively [83]. Electron carrier concentrations for both cases are related to electrons in trap levels. If the leakage current through the dielectric is bulk-limited, the magnitude of the current is determined by the electrons in the conduction band. The concentrations of electron carriers at the thermal and quasi-thermal equilibrium in the conduction band are strongly affected by the trap level density trap levels, and injection electrons to the trap levels. It implies that, with the help of equilibrium approximation, the leakage current could be described as electrons in energy and space, causing accumulation of charges due to injected electrons, so called the space charges.

The space-charge-limited current at room temperature or below is efficient on the electrical properties of dielectric insulators because they normally have a low density of free carriers, and the charge unbalance could be easily produced by the external applied voltage. The character and the magnitude of space-charge-limited effect are largely determined by the

presence of localized states which could trap and store charges in equilibrium with the free carriers. When the charges effectively inject from the conduction (or valence) band into insulator, the net transport is limited by the actual transport, drift and diffusion, of charges in the bend of the insulator. Regarding the electron injection into the oxide film, it seems difficult for electrons to jump into the conduction band by thermal transition or tunneling process. However, if the dielectric has a large trap density or a large tail density of state (DOS) near the electrode, as shown in Fig. 2-5, electrons are able to excite into the conduction band with a small activation energy [84]-[86].

Fig. 2-6 shows the oxide band structure distorted by the injection electrons. In order to satisfy the thermal equilibrium, electrons inject from the cathode into the insulator, resulting in a negative space-charge density adjacent to the cathode. Because an equal amount of positive charges remain on the cathode, the charges distribution consists of positive charge sheet near a region with negative space charges. The same condition is also on the anode side. As the voltage bias increases, the net positive charges on the cathode would be increased and that on the cathode would be decreased. Total charge Q in the insulator could be expressed by the sum of the cathode positive charge Q_1 and the anode positive charge Q_2 [87] as

$$Q = Q_1 + Q_2 = \int_0^{\lambda_m} \rho(x)dx + \int_{\lambda_m}^{s} \rho(x)dx . \qquad (2\text{-}14)$$

The positive charges on either contact are neutralized by an equal amount of negative charges contained between the contact and the plane at $x=\lambda_m$. Since the internal field caused by Q_1 and Q_2 is zero at $x=\lambda_m$, the net field there must be zero. For this reason, the place at $x=\lambda_m$ is termed the virtual cathode. Eventually, when $Q_1=0$, the virtual cathode coincides with the physical cathode-insulator interface. Under this condition, the anode region extends throughout the whole of the insulator, and the ohmic contact no longer exists at the cathode-insulator interface. Thus, due to further increasing voltage bias, the conduction process is no longer space-charge limitation, but it belongs to emission limitation.

Space charges have an effect to distort the oxide dielectric band shape. In electron carriers case, the tunneling distance and the barrier height are increased by accumulation space charges so that the tunneling current is depressed [45]. The space-charge-limited flow is known to be effective at room temperature or below, since the low density of free carriers easily cause charge unbalance [45]. This is also valid on high-k materials with a considerable charge trap density at high temperature. Fig. 2-7 shows that the typical J-V behavior obeys the SCLC theory with the combination of exponential and the localized trap level distributions. In the logarithmic scale of J-V curve as shown in Fig. 2-7 (a), it could be easily found a linear relationship according to the SCLC theory. On the other hand, in the semi-logarithmic scale as shown in Fig. 2-7(b), it is difficult to realize the exacted J-V relationship.

The space-charge-limited current with localized trap levels in the oxide band is given by

$$J = \frac{9}{8}\varepsilon_0\varepsilon_{ox}\mu\frac{V^2}{L^3}. \qquad (2\text{-}15)$$

Here, ε_0 and ε_{ox} are dielectric constants of vacuum and oxide film, respectively. μ is carrier mobility, V is applied voltage, and L is film thickness. The mobility μ is often found to be strong dependence on electric field, particularly in the high field region [88]. The space-charge-limited current with exponential trap levels is given by

$$J = N_c\mu q^{(1-l)}\left[\frac{\varepsilon l}{N_t(1+l)}\right]^l\left(\frac{2l+1}{l+1}\right)^{(l+1)}\frac{V^{(l+1)}}{L^{(2l+1)}}. \qquad (2\text{-}16)$$

Here, N_c is density of states at conduction band, q is electronic charge, and N_t is total trap density. $l=T_t/T$, where T_t is described as trap level distribution and T is absolute temperature.

As seen in Fig. 2-6, the accumulation charges near to the cathode leads to virtual cathode in the oxide film. This means that the carrier transport is caused by the drift field between the virtual cathode and anode, with a continuous supply of charges from the accumulation region between the virtual cathode and the real cathode. So, we could expect that the electric field near the cathode is small and that in the drift current flow region is large. This point can be realized by the oxide electric field as a function of position, which is given by

$$E(x) = \left(\frac{2l+1}{l+1}\right)\left(\frac{x}{L}\right)^{\frac{l}{l+1}}\frac{V}{L}. \qquad (2\text{-}17)$$

The effective field in oxide film near the cathode is nearly zero and it is higher than the applied field. This higher electric field may result in the larger current, especially in the thin dielectric. Fig. 2-8 shows the typical trap levels with the exponential energy distribution and with the maximum trap density distribution. As regard to the spatial distribution of trap levels, uniform or non-uniform type of distribution does not alter the results of J-V relation, because the spatial trap distribution is only affected by the film thickness [46], [89]. In addition, the energetic trap distribution in the energy bandgap of oxide determines the J-V relation, such as J~V, J~V^2, or J~$V^{(n+1)}$. The oxide film thickness in SCLC with a uniform trap distribution is equal to the physical film thickness (d), while the film thickness with spatially distributed traps is effective film thickness (d_{eff}). The effective film thickness describes the trap distribution inside the film. The J-V relation remains unchanged and it is independent of how the trap is distributed spatially.

2.1-4 High Trap Density Related Conduction

Excepting for the PF emission and SCLC, there are also several conduction mechanisms related with high trap density in dielectric, such as Poole conduction, trap-assisted tunneling (TAT), junction-like conduction, and variable range hopping (VRH), as noted in Tables 2.1 and 2.2. And, we briefly describe them as following.

Poole conduction and P-F conduction assume paired trap sites and isolated trap sites, respectively [90], depending on the oxide trap density. The transition between two models has been reported in [91]. As the applied field becomes lower, the current density following P-F conduction could be described by Poole conduction because the barrier height reduction by the electric field becomes smaller, and then the trap level is comparable to that of the Poole [91]. In Poole conduction, traps are enough close to perturb the Coulombic potential of the

neighbor trap, so that the decrease of the barrier height between two traps is determined by distance between traps and applied field but not by Coulombic field. It leads to leakage current independent of the dielectric constant of the insulator.

Variable range hopping (VRH) conduction involves thermally activated hopping conduction in localized electronic states near the Fermi energy. VRH conduction dominates the conduction mechanism at low applied voltage and high temperature [92]. Besides, TAT conduction requires shallow and/or deep trap levels and it usually occurs at the oxide field greater than 4 MV/cm [93], [94]. Fleming *et al.* suggested that leakage current could flow through the defect band formed by localized large trap levels, and then its behavior is similar to the junction-like conduction due to the difference in energy level between the defect band and the Fermi level at both electrodes [95].

As regard to the relation between oxide trap density and leakage current, the traps enhance the leakage current for the case of Poole, VRH, TAT, and junction-like conductions, while they hinder it in SCLC case. This is the uniqueness of SCLC contrast to the others. Fig. 2-9 conceptually illustrates the relationship between the leakage current and the trap density of the dielectric film. If the gate current is explained by the SCLC theory, the gate current could be reduced by increasing the dielectric trap density.

2.2 Dielectric Polarization and Relaxation of High-k MIM Capacitors

2.2-1 Dielectric Polarization

In an MIM capacitor system composed of two parallel metallic plates with an insulator thickness d (in meter, m), the capacitance C_{MIM} (in farad, F) is calculated by using

$$C_{MIM} = \frac{Q}{V} = \frac{\varepsilon \times S}{d} \tag{2-18}$$

, where V (in volt) is the applied voltage of the capacitor, Q (coulomb, C) is the amount of storage charges of the capacitor, ε (in F/m) is the permittivity of the insulator, and S (in m^2) is the area of the plate. The capacitance is proportional to the permittivity which signifies the charge storage capability of the capacitor, and the large permittivity of the high-k dielectric contributes from the lattice structure and the polarizability under the external bias. The lattice structure of the dielectric determined by the crystal phase has been formed as the dielectric film deposited or grown during the fabrication process. Therefore, the changes in permittivity of high-k MIM capacitor during measurement could be contributed to the changes in polarization behaviors.

In general, the total polarizability of a dielectric could be divided into four kinds of possible compositions, as sketched in Fig. 2-10 and denoted below [96].

(1) The electronic polarizability, p_e, is caused by the slight displacement of the negatively charged electron cloud in an atom relative to the positively charged nucleus. Electronic polarizability occurs in all solids and in some, such as diamond, and it is the only contributor to the dielectric constant since ionic, dipolar, and space charge polarizabilities are absent.

(2) The ionic polarizability, p_i, arises from a slight relative displacement or a separation of anions and cautions in a solid.

(3) The dipolar polarizability, p_d, arises in materials, such as HCl and H_2O, which contain permanent electric dipoles or are induced by the defects and polar molecules in the dielectric. These dipoles may change their orientation and they tend to align themselves with an applied electric field. The effect of dipolar polarizability has large temperature dependence since the dipoles may be “frozen” at low temperature.

(4) The space charge polarizability, p_s, occurs in unperfected dielectric with a long range charge migration.

Consequently, the total polarization (p) of dielectric is the sum of all contributions and

expresses as follows:

$$p = p_e + p_i + p_d + p_s \tag{2-19}$$

2.2-2 Dielectric Relaxation

As described above, the total polarizability in dielectric composed of electronic polarizability, ionic polarizability, dipolar polarizability, and space charge polarizability can contribute to the permittivity. However, as the polarity of external force changes, all the polarization species, like electrons, ions, dipoles, and space charges, need a period of time to displace from the original site or rotate from the earlier orientation to the new equilibrium state, resulting in the other polarization status. This lag response process of the dielectric is the dielectric relaxation, and the period of time when the polarization specie needs to follow the alternating force is the relaxation time. Moreover, four kinds of polarization species have various response times, and Fig. 2-11 reveals the relation between the polarization mechanism and the alternating frequency of external force that the polarization can follow [97]. We can recognize from this diagram that the space charges have the longest relaxation time than any other polarization species, and their polarized phenomenon could be neglected as the alternating frequency of external force is higher than 1 MHz. But, the electrons can rapidly response the changes of external force to result in the shortest relaxation time, and hence such rapidly response of electrons can contribute to the polarization even at very high frequency. In a trap-rich dielectric, such as many high-k materials, the dipolar relaxation and the space charge relaxation are emphasized at our testing frequencies in the range from 10 kHz to 500 kHz. Thus, we give a brief description about these two types relaxation behaviors as following.

Space charges in dielectric of the high-k MIM capacitor are made of free carriers that inject from the biased electrode, and then they become the excess mobile charges moving in the dielectric film [98]. The excess mobile charge in the insulator is expected to follow the

alternating signal with a relaxation time τ_s depending on the mobility μ, the mobile charge concentration n(E), and the permittivity ε. According to Coelho [99], the complex permittivity ε^* is given by

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = \varepsilon \times \frac{1 + i\omega\tau_s}{i\omega\tau_s + \frac{\tanh(A)}{A}} \tag{2-20}$$

, where ε' is the real part of the complex permittivity and ε'' is the imaginary part of the complex permittivity. And, A is given by

$$A = \sqrt{\frac{1 + i\omega\tau_s}{D_E\tau_s}} \times \frac{d}{2} \tag{2-21}$$

, where d is the thickness of the dielectric, ω is angular frequency, and D_E is the diffusion coefficient according to Einstein's law ($D_E = \mu kT/e$). The relaxation time (τ_s) is given by

$$\tau_s = \frac{\varepsilon}{\mu e n(E)}. \tag{2-22}$$

Here, n(E) is mobile charge concentration dependant on the electric field E. A higher relaxation time means the mobile charges are more difficult to follow the alternating signals. The frequencies that space charge can follow are low, we would observe the tail of the space charge relaxation at the test frequencies (10 kHz to 500 kHz). If the conduction of the MIM capacitor is given by Schottky effect, the n(E) could be expressed as the following formula

$$n(E) = n_0 \exp(-\frac{e\phi_B}{k_B T}) \exp(\frac{\beta_S}{2k_B T} E^{1/2}) \tag{2-23}$$

, where n_0 is uniform concentration of mobile charges without any applied voltage. Accordingly, the amount of excess mobile charges in the insulator could be affected by the electric field, the temperature, and the barrier height at the metal/dielectric interface.

The dipole relaxation effect can be observed even at infrared frequency while the free carrier effects become negligible. The dipolar relaxation time (τ_d) shows a wide distribution range of 10^{-10} sec to 10^3 sec, which results in a broad frequency range where the dipole can contribute to the dielectric relaxation. It has been reported that the defect dipole relaxation

dominates the lower frequency part or the longer relaxation time region of the total dipolar relaxation behaviors [100]. Besides, as the temperature increases, the τ_d decreases to manifest a faster response for alternating signals.

2.3 STRESS BEHAVIORS OF MIM CAPACITORS

In terms of the precision performance of long-term use, it is a key issue that the stability of MIM capacitors under electrical stress. C. Besset *et al.* [101] first depicted the variation of the SiO_2 MIM capacitance under electrical stress, and they also observed that the relative-capacitance variation is dependent on the injection charges but independent of the stress current. Additionally, it was also found that the capacitance-voltage curve shifts toward the negative voltage side and the capacitance density significantly increases. And, it concluded that both phenomena on the C-V shift and the capacitance increase are strongly correlated and they had the same origin of the trapped charges, which could generate new dipoles in the dielectric and modulate the dielectric permittivity.

C. C. Hung *et al.* [102] investigated the degradation of SiO_2 MIM capacitors under a wide voltage range of stress conditions. It was found that the capacitance is gradually degraded during stress, but the degradation behavior strongly depends on the stress-current density. At high stress voltage level, the capacitance is increased logarithmically as the injection charges increase until the dielectric breakdown occurs. At lower voltage stress conditions, the degradation rate is proportional to the stress current and it is reversal after a certain period of time. The reversal phenomenon of the degradation rate begins in earlier at higher temperature. Initially, the oxide-trapped charges would increase the local permittivity of dielectric, thus leading to the capacitance increasing. On the other hand, a reversal in the degradation, after stressing for a certain period of time, may arise from a growth in the interlayer between the metal electrode and the dielectric.

C. Zhu *et al.* [103] and S. J. Ding *et al.* [104] demonstrated the stress induced leakage current and the stressed induced variation in voltage coefficient of capacitance (VCC) of high-k HfO_2 and HfO_2-Al_2O_3 MIM capacitors, respectively. It was argued that carrier mobility could be modulated and become smaller by the stress generated traps, and further lead to a higher relaxation time and a smaller VCC. Later, C.-H. Cheng *et al.* [105] demonstrated the effects of the constant voltage stress (CVS) on the VCC, the leakage current, and the temperature coefficient of capacitance (TCC) of HfTiO MIM capacitors. They suggested that the elevated barrier height of the dielectric caused by the trapped electrons might suppress the leakage current under CVS condition. On the other hand, the stress induced variations in both VCC and TCC could be attributed to the electron-trap generation and/or ion displacement in dielectric. They also pointed out employing the metal electrode with higher workfunction could reduce these variations during stressing.

K. Takeda *et al.* [29] discussed the stress behaviors of high-k HfAlO MIM capacitors. In this research, it was discovered that the relative dielectric constant (k), the dielectric loss (D), the temperature coefficient of capacitance (TCC), and the frequency coefficient of capacitance (FCC), would gradually increase with the voltage stress time while the VCC decreases. It was also found that nearly linear relationships existed between k and D, between TCC and D, and between FCC and D are increased. These results indicated that the increases in k-value, in FCC, and in TCC during CVS conditions, are basically explained by the increase in D. Therefore, it is suggested that the voltage stress would cause the increase of dielectric-loss, and then increases k, FCC, and TCC. Increase in stress-time dependence of dielectric-loss was well described by power dependence, and that is, the power exponent of the dependence linearly increases with stress voltage. The power exponent could be lowered by increasing the aluminum concentration in HfAlO dielectric. This indicates that adding aluminum into the HfAlO dielectric can improve the characteristic stabilities of a MIM capacitor under voltage stress.

Former two studies imply that the high-k dielectrics have more obvious charge-trapping properties so that their stress induced degradation may be an issue on high-precision analog applications. However, the correlation between the injection charges and the capacitance variation of high-k MIM capacitor due to the electrical stress has not been well characterized. Besides, the relationship between VCC and D of high-k MIM capacitor under electrical stress still remains a question and needs to be clarified. Moreover, it is well-known that the high-k MIM capacitor has distinct conduction mechanisms under various bias conditions, which leads to diverse stress effects on leakage current. Therefore, the stress induced changes in leakage current in various bias ranges should be separately discussed.

2.4 RELIABILITY CHARACTERISTICS OF MIM CAPACITORS

2.4-1 A Brief History on Reliability Improvement of Silicon-Related Device

Prior to 1985, the reliability improvements on silicon devices had already begun, and those efforts had already passed through two eras [106]. In the first era of the improvement of silicon reliability, from 1975 to 1980, the introduction of new VLSI materials was at the forefront. Everyone learned about material properties, such as Si, Al, and SiO_2, and their various interactions. In the second era, from 1980 to 1985, the major reliability problems for silicon technologies were identified: mobile ions, electro-migration, stress migration, time-dependent dielectric breakdown (TDDB), cracked die, broken bond wires, purple plague, and soft errors.

In the third era, from 1985 to 1990, the reliability physics was the focus on the silicon folks. The researchers developed various degradation models for the previously identified mechanisms and they also derived acceleration factors for the special environmental stresses of temperature cycling and corrosion. In the fourth era, from 1990 to 1995, the silicon folks adopted a new phrase, building-in reliability. It was a period of reliability engineering

emphasized on the wafer-level reliability. In the fifth era, from 1995 to 2000, the silicon folks complete their 20-year cycle by merging the metrics of reliability and quality with focus on a major defect-reduction effort. From 2000 to 2005, the silicon folks restart their cycle by reverting back to the first era, with the introduction of new materials in ULSI technology. The main work is on new copper metallization, low-k interlayer dielectrics, high-k gate dielectrics, new metal gate materials, and getting feature smaller than 100 nm.

2.4-2 Reliability Issues on MIM Capacitors

In the case of MIM capacitors, the ultimate breakdown strength of a dielectric material and their time-dependent dielectric breakdown (TDDB) characteristics have been attracted great reliability interest [107]. During electrical breakdown measurement, the ramping voltage (electrical field) is used to record an abrupt rise in leakage current through the dielectric of MIM capacitor. A rapid rise in current density could result in the severe localized joule-heating in the dielectric, the localized melting of the dielectric, and the melt-filament formation to short the dielectric between two electrodes.

TDDB properties depend on the intrinsic dielectric materials, the processing method, and the electrode materials. The MIM capacitor with thin dielectric film usually exhibits higher failure rate, thus it is a permanent challenge to improve of its TDDB properties. TDDB measurements are normally done by recording the times-to-failure when a collection of identically processed capacitors are stored under a constant electric field which is less than breakdown strength of the dielectric. The time-to-failure statistics are assumed to follow a Weibull distribution with appropriate "Weibull area scaling" for capacitors that differ only by their area [108]. The time-dependence of the TDDB process is derived from the fact that a critical amount of dielectric damage must be accumulated before the electrical breakdown and the thermal breakdown occur. From a microscopic point of view of the TDDB process, molecular bonds tend to break with time during TDDB testing, eventually reaching a

localized density of broken bonds sufficiently high to cause a conductive percolation-path to be formed between two electrodes. These conductive paths can result in electrical/thermal-breakdown of the dielectric.

Since high-k materials are aggressively developed to replace SiO_2 as dielectrics film of MIM capacitors, it is important to know whether high-k dielectrics provide superior reliability. In recent years, a number of studies have demonstrated the reliability characteristics of backend high-k MIM capacitors [29], [109]-[115]. However, most of them focus on the silicon nitride (SiNx) MIM capacitors [109]-[112], and other minorities investigate the reliability issues of Ta_2O_5, Nb_2O_5, Hf-based, and Zr-based MIM capacitors [29], [113]-[115]. As regard to La-based high-k MIM capacitors, there is no empirical research of statistical TDDB properties up to this point.

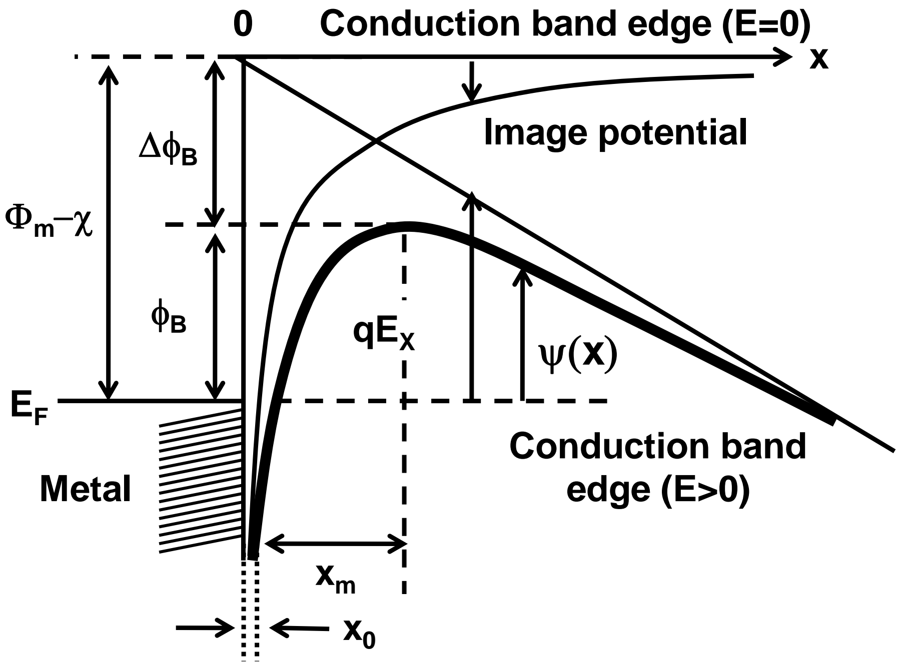


Fig. 2-1. Energy-band diagram between a metal surface and a vacuum. Conduction band edge means the vacuum energy level which is zero in electron energy. x_0 is introduced due to the singular point of image potential at x=0 [39].

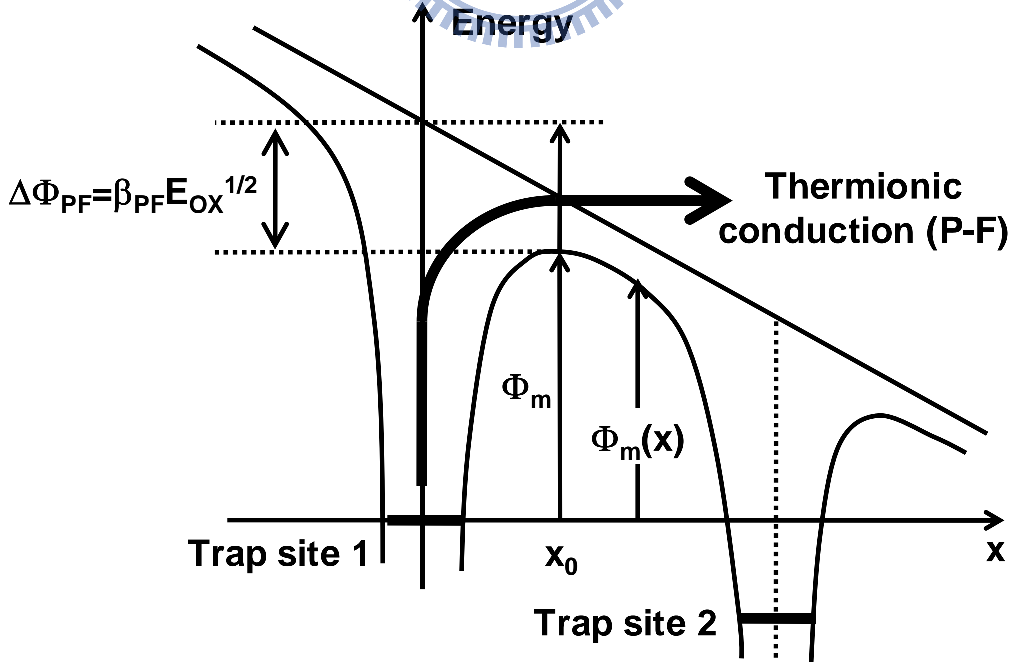


Fig. 2-2. Thermionic conduction (Poole-Frenkel conduction) [39].

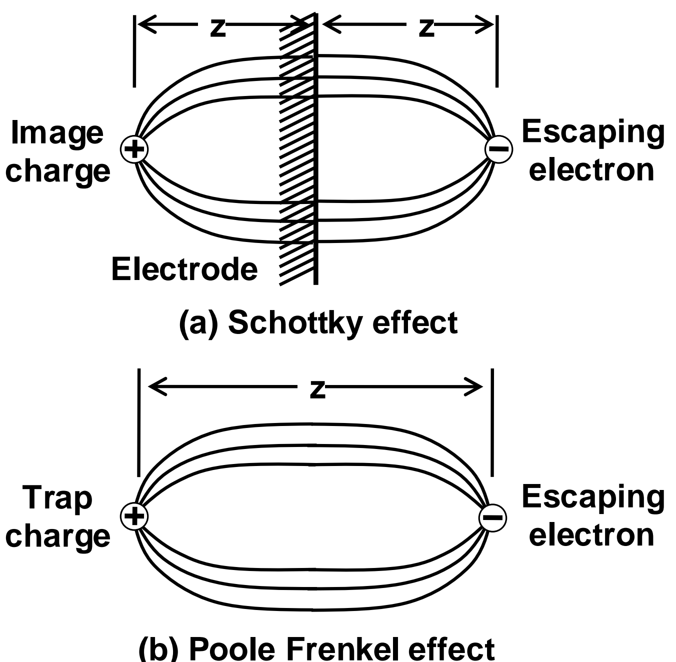


Fig. 2-3. Restoring force on escaping electron. (a) The Schottky effect. (b) The Poole-Frenkel effect [39].

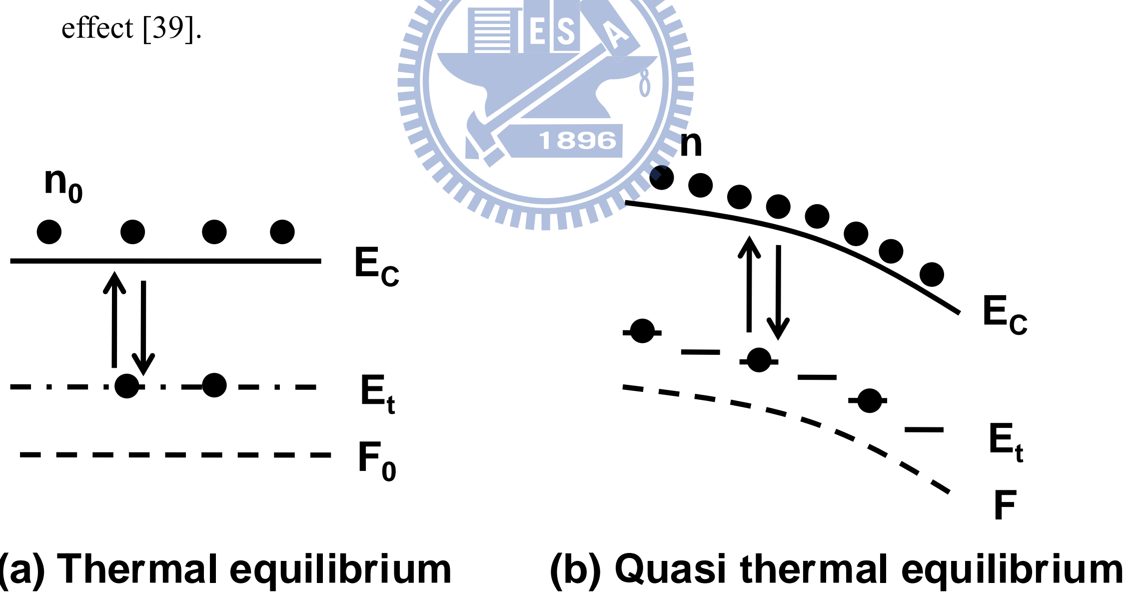


Fig. 2-4. Thermal and quasi-thermal equilibrium (steady-state) of electrons in conduction band E_c and trap level E_t. F denotes quasi-Fermi level and the subscript 0 means the thermal equilibrium [83]. The equilibrium states can be achieved by low injection and low internal emission.

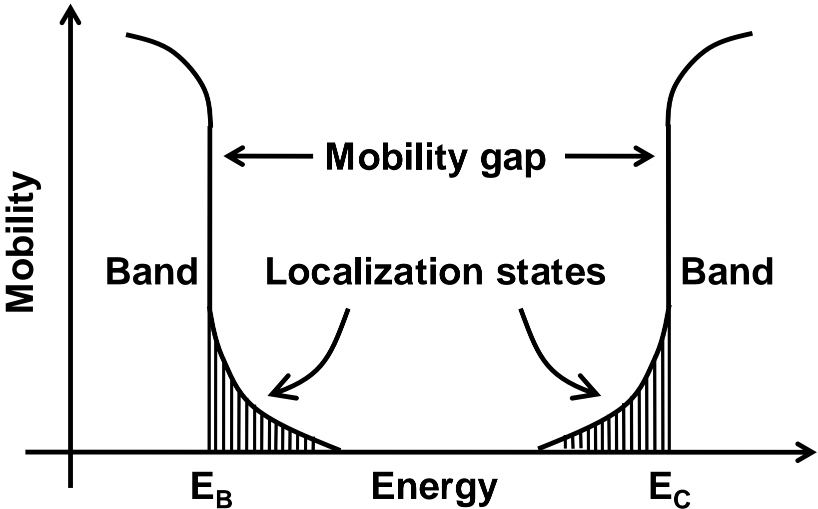


Fig. 2-5. Mobility of electrons as a function of energy showing mobility gap (amorphous stste) [84]-[86].

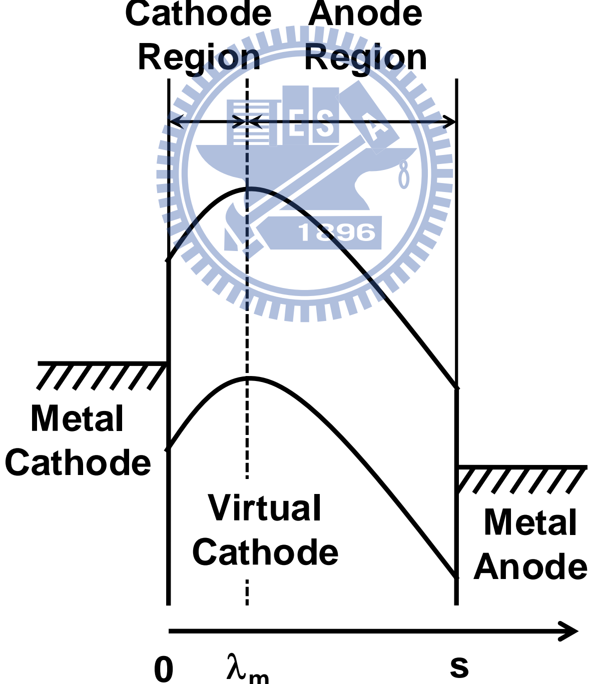


Fig. 2-6. Energy diagram illustrating virtual cathode, cathode region, and anode region under space-charge-limited conduction [83]. λ_m denotes the position of virtual cathode in the insulator. The insulator is assumed to be free of surface states and ohmic contacts.

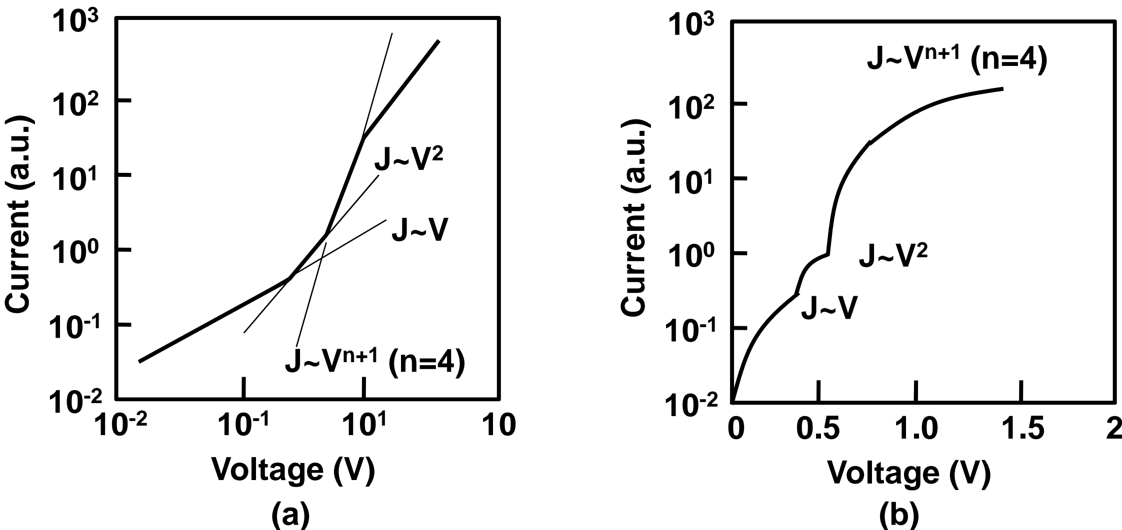


Fig. 2-7. Energy diagram illustrating virtual cathode, cathode region, and anode region under space-charge-limited conduction. λ_m denotes the position of virtual cathode in the insulator. The insulator is assumed to be free of surface states and ohmic contacts [88].

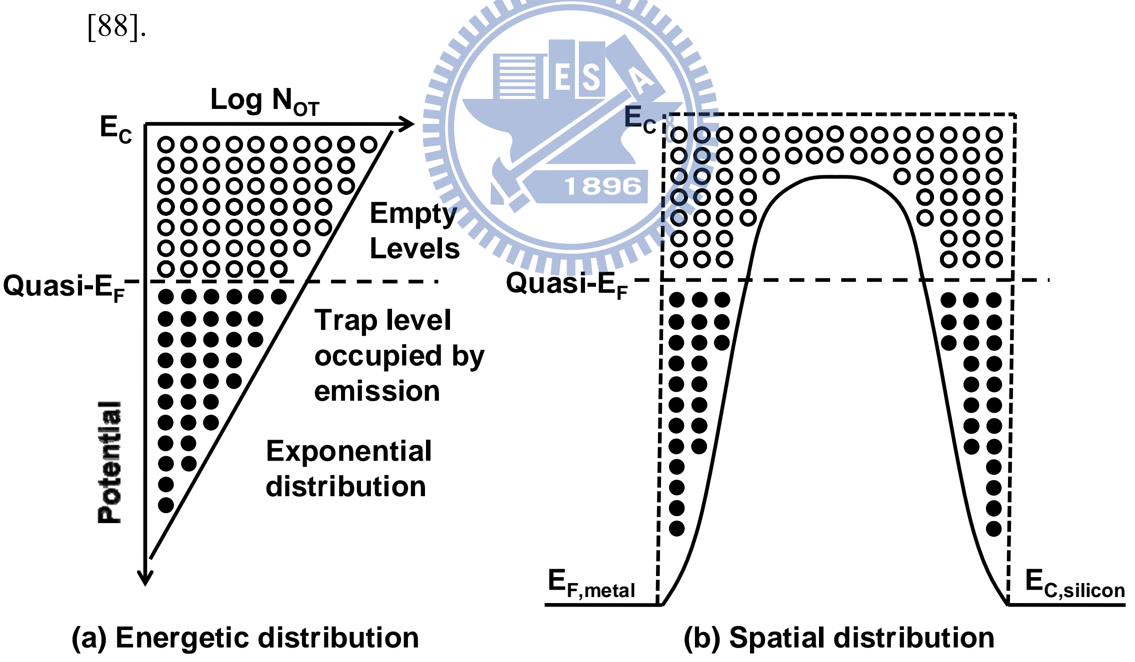


Fig. 2-8. Schematic trap level distribution at 0^ok, in the oxide (a) energetically and (b) spatially. Exponential trap distribution is assumed in (a). Trap levels filled with electrons are apparently separated from the unfilled trap levels on account of zero Kelvin degree consideration. Solid and hollow circles correspond to the trap sites with electrons and without electrons, respectively [90].

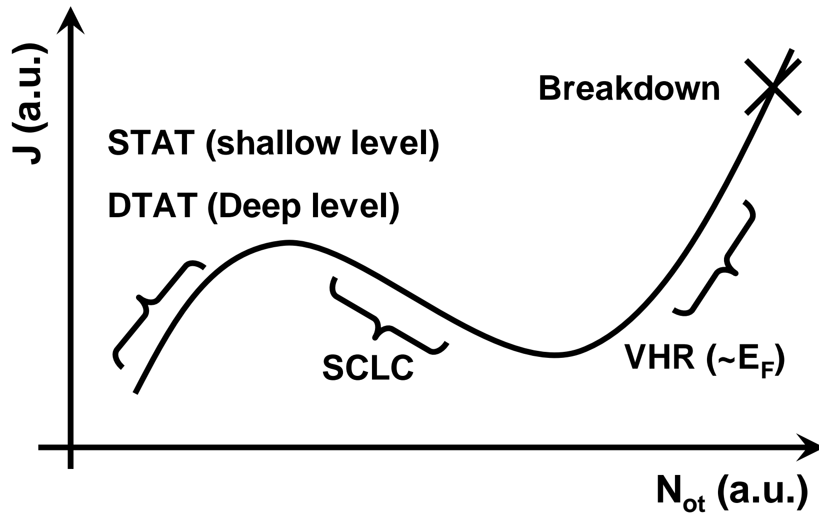


Fig. 2-9. Gate current as a function of oxide trap density N_{ot} in arbitrary scale [93].

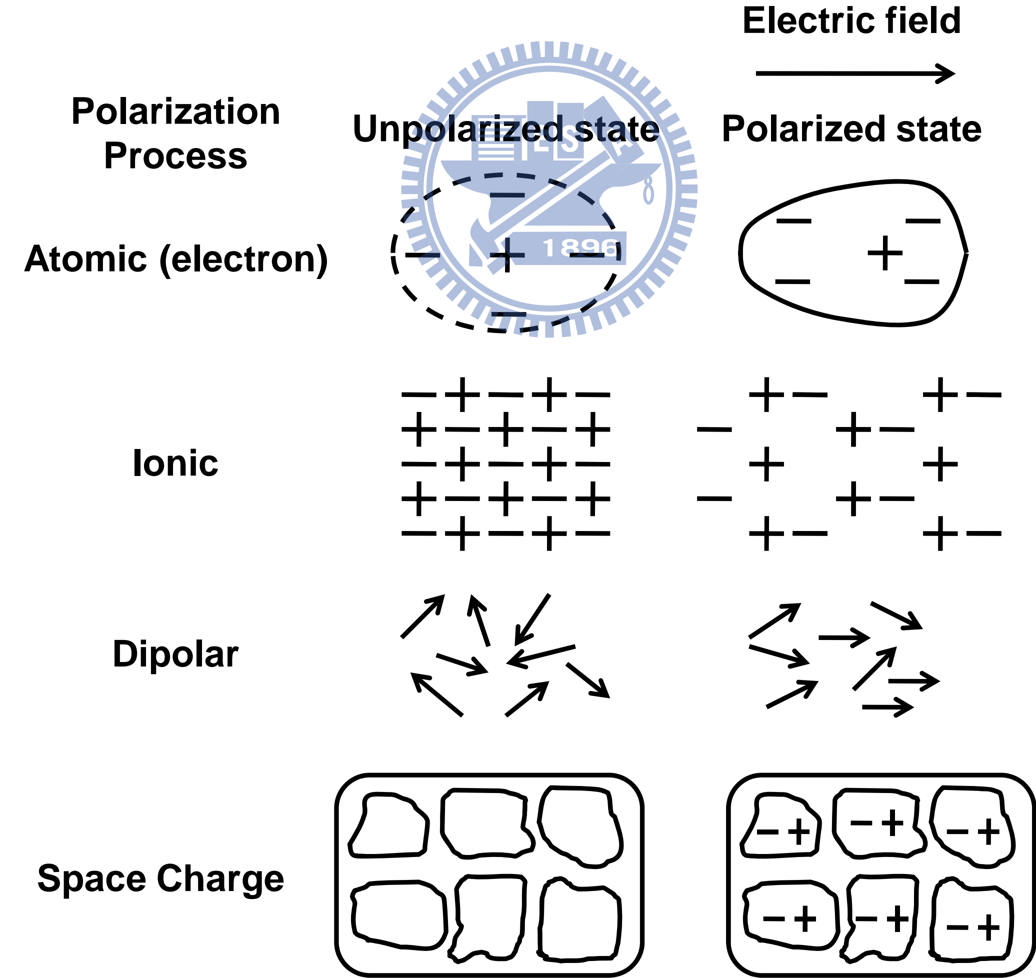


Fig. 2-10. Four kinds of polarization mechanisms [96].

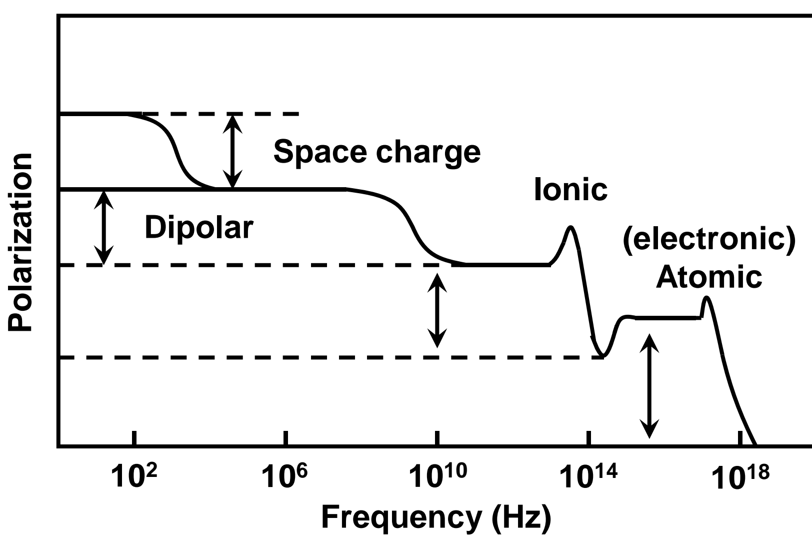


Fig. 2-11. The relation of the response frequency and polarization mechanisms [97].

Table 2-1. Theoretical expressions of the bulk-limited conduction processes [44]-[50].

	Mechanisms		Expressions	
Bulk-Limited	Ω		(1) $J = qn\mu \frac{V}{s} = qN_C \exp\left[-\frac{q}{kT}(F - E_C)\right]\mu \frac{V}{s}$	
	Poole		(2) $J = A\exp\left(-\frac{S_P E}{k_B T}\right) = A\exp\left(-\frac{qd}{2}\frac{E}{k_B T}\right)$	$S_P = \frac{1}{2}qd$
	Poole-Frenkel		(3) $J = qN_C \mu(T)\exp\left(-\frac{\phi_0}{k_B T}\right)\exp\left(\frac{\beta_{PF}}{k_B T}E^{1/2}\right)E$	$\beta_{PF} = 2\beta_S$
	Hopping		(4) $J = \frac{q^2}{k_B T}\frac{d^2}{\tau_0}n^*(T)E\exp\left(-\frac{4\pi m^*}{h}\phi_m d\right)$	$\beta_{PF} = \left(\frac{q}{\pi\varepsilon_0\varepsilon_i}\right)^{1/2}$
	VRH(a)		(5) $J = J_0 \sinh\left(\frac{qRE}{kT}\right)$	
	SCLC(b)	shallow	(6) $J_{shallow} = \frac{9}{8}\mu\varepsilon_i\varepsilon_0\theta(T)\frac{V^2}{s^3}$	
		uniform	(7) $J_{uniform} = 2qn_0\mu\frac{V}{s}\exp\left(\frac{2\varepsilon_0\varepsilon_i V}{N_t kTqs^2}\right)$	
		exponential	(8) $J_{exponential} = N_c\mu\, q^{(1-l)}\left[\frac{\varepsilon\, l}{N_t(l+1)}\right]\left(\frac{2l+1}{l+1}\right)^{(l+1)}\frac{V^{(l+1)}}{s^{(2l+1)}}$	$l = T_c/T$

(a) Variable range hopping, (b) space-charge-limited current: shallow, uniform, and exponential/ Gaussian distributions. Here, m^* denotes the electron effective mass, q the electronic charge, h the Planck's constant, k_B the Boltzman's constant, T absolute temperature, φ_0 the metal-insulator barrier height, ε_0 the vacuum permittivity, ε_i the relative permittivity of the insulator, s the insulator thickness, V the voltage of the insulator, E the electric field of the insulator.

Table 2-2. Theoretical expressions of the electrode-limited conduction processes in oxides [46], [48]-[51].

	Mechanisms		Expressions	
Bulk-Free (Electrode-Limited)	Schottky[a]	(1)	$J=\frac{4\pi m^{*}q}{h^{3}}k_B^{2}T^{2}\exp\left(-\frac{\phi_0}{k_BT}\right)\exp\left(\frac{\beta_S}{k_BT}E^{1/2}\right)$	$\beta_S=\left(\frac{q}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2}$
	D-T[b]	(2)	$J=\frac{q^{2}}{\pi h}\frac{\phi_0}{s^{2}}\exp\left(-\alpha^{*}s\phi_0^{1/2}\right)\sinh\left(\frac{\alpha^{*}sV}{4\phi_0^{1/2}}\right)$	$\alpha^{*}=\alpha\left(\frac{m^{*}}{m_0}\right)^{1/2}$
	Fowler-Nordheim	(3)	$J=\frac{q^{2}}{8\pi h}\frac{E^{2}}{\phi_0}\exp\left(-\frac{2}{3}\frac{\alpha^{*}\phi_0^{3/2}}{E}\right)$	$\alpha=\frac{4\pi(2m_0q)^{1/2}}{h}=\frac{10.25}{nm\sqrt{eV}}$
	TAT[c] deep trap	(4)	$J_{dt}=\frac{2C_tN_tq\Phi_t}{3E_{ox}}\exp\left(-\frac{8\pi\sqrt{2qm_{ox}}}{3h}\frac{\Phi_t^{3/2}}{E}\right)$	
	shallow trap	(5)	$J_{sht}=qR_0v\left(\frac{s}{E}-\frac{\Phi_t}{E^{2}}\right)$	
	Junction-like	(6)	$I=\frac{\eta V_t}{R_s}W\left\{\frac{I_0R_sR_{p1}}{\frac{\eta V_t}{R_s}(R_{p1}+R_s)}\exp\left(\frac{R_{p1}(V+I_0R_s)}{\eta V_t(R_{p1}+R_s)}\right)\right\}+\frac{V-I_0R_{p1}}{R_{p1}+R_s}+\frac{V}{R_{p2}}$	

(a) Thermionic Current, (b) Direct Tunneling Current, (c) Trap-Assisted Tunneling: deep and shallow traps. Here, C_t denotes a slowly varying function of electron energy, N_t the trap density, φ_t the trap energy, m_{ox} the effective electron mass in the insulator, R_0 tunneling rate of an electron from the silicon conduction band into a shallow trap, ν hopping frequency of an electron between shallow traps, η the junction ideality factor, V_t the thermal voltage (= kT/q), W the Lambert function [22,23] defined by the solutions of W(x)exp(W(x))=x, R_s the parasitic series resistance, R_{p1} the shunt loss resistance at the device, R_{p2} the shunt loss resistance at the device periphery, I_0 the junction reverse current, d the distance between the trap centers, F the quasi-Fermi potential of the insulator, E_C the conduction band edge of the insulator, N_C the effective density of states in the insulator conduction band, m the carrier mobility, τ_0 the time constant, n^* the density of free electrons in the insulator, φ_m the energy corresponding to the maximum of the barrier, R the hopping distance, J_0 the temperature dependent factor related to electron-phonon interactions, θ the trapping factor defined by the ration of the free electron density and the density of filled trapping sites.

Table 2-3. Comparison of Schottky-emission and Poole-Frenkel emission.

Item	Schottky Emission	Poole-Frenkel Emission
Conduction	Bulk-free	Bulk-limited
J-E_{film} or T_{film}	Uncorrelated	Correlated
Location	Interface	Bulk
Origin	Image force	Coulomb interaction
J-V polarity	Asymmetric	Symmetric

CHAPTER 3

Fabrication and Characterization Methods

In this chapter, the detail fabrication procedures of the metal-Insulator-metal (MIM) capacitors with a high dielectric constant (high-k) of a lanthanum oxide (La_2O_3) insulator are described. The physical analyses techniques and electrical measurement methods used to characterize MIM capacitors are also included and presented in this chapter.

3.1 FABRICATION OF La_2O_3 MIM CAPACITOR

The schematic layout and its cross section along the A-A' line of the fabricated La_2O_3 MIM capacitors are shown in Figs. 3-1(a) and 3-1(b), respectively. The main fabrication steps were summarized below, and the process steps corresponding to their used lithographic masks were shown in Fig. 3-2. After performing the standard RCA clean process to remove the native oxide and any contamination [1], the 1-μm thermal oxide was grown on 6-inch Si wafer as an isolation buffer layer by using wet oxidation. And then, the 200-nm tantalum (Ta) layer and the 50-nm tantalum nitride (TaN) layer were subsequently deposited on buffer oxide layer as the bottom electrode by a reactive sputtering system. Ta layer and TaN layer were used to reduce the parasitic resistance and to serve as a diffusion barrier layer [104], [107], respectively. Before defining the bottom electrode of the MIM capacitor, the surface of TaN was treated by ammonia (NH_3) plasma nitridation at 300 mtorr with the RF power of 100 watts for 10 minutes to reduce the interfacial layer [118]-[119] during the following high-k annealing processes. Besides, the metal layer TaN with NH_3 treatment has more flat surface roughness so that the leakage current of the MIM capacitor could be reduced under bottom injection condition [120].

The bottom electrode TaN/Ta was lithographically patterned and defined by employing a transformer-coupled-plasma (TCP) etcher with chlorine-based gas. Subsequently, as displayed in Fig. 3-2(b), the 200-nm tetraethoxylsilane (TEOS) oxide film used as the first inter-layer dielectric (ILD) isolation was deposited by utilizing a plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C. The capacitor region and the bottom contact region were etched by buffered oxide etchant (BOE) solution after being opened by optical lithography process. Afterwards, the lanthanum oxide (La_2O_3) was deposited by using electron beam evaporation, as illustrated in Fig. 3-2(c). The high-k dielectric La_2O_3 film on bottom electrode was annealed at 400 °C in O_2 ambient to improve its quality via fully oxidation and defects elimination. After lithography process to define the top electrode region, the 60-nm nickel (Ni) and the 30-nm TaN were subsequently deposited by electron beam evaporation and reactively sputtering, respectively. And then, the top electrode with Ni/TaN bi-layer metal was formed by using lift-off technique, as indicated in Fig. 3-2(d).

Next, the 300-nm TEOS oxide film served as the second ILD passivation layer was deposited by using a PECVD system at 300 °C. Because the La_2O_3 high-k dielectric film and the TaN metal were hardly etched by BOE solution, the contact holes were patterned by two-step etching process for interconnection, as presented in Fig. 3-2(e) and 3-2(f). Firstly, the 300-nm ILD passivation on contact hole region was removed by BOE solution and its could be etched, and the etching process could be stopped on the top of the TaN electrode and the La_2O_3 film. Secondly, the mixed solution of H_3PO_4: HNO_3: CH_3COOH: H_2O = 50: 2: 10: 9 heated to 60 °C was used to dissolve La_2O_3 film with high etching selectivity to the ILD passivation layer and the TaN electrodes. After the contact holes were opened by two-step wet etching process, the aluminum (Al) film of 500 nm was deposited by using a thermal evaporation system. Finally, the aluminum pads were lithographically patterned and also etched by the mixed solution of H_3PO_4: HNO_3: CH_3COOH: H_2O = 50: 2: 10: 9 at 60 °C. Ultimately, the MIM capacitors with La_2O_3 high-k dielectrics were accomplished, as depicted

in Fig. 3-2(g). It was noteworthy that the maximum temperature during MIM capacitors fabrication was 400 °C, which was compatible with VLSI backend process. Besides, the optimized fabrication condition for La_2O_3 is 10-nm with 10-minute annealing, and hence we measured and discussed the MIM capacitors with high-k layer of this optimized condition in this thesis.

3.2 MEASUREMENT AND PARAMETERS EXTRACTION

An automatic measurement system consisted of a person computer (PC), Agilent-4156C, Agilent-4284A, Agilent switch, and a probe station is used for DC and low-frequency measurement of the fabricated devices. The properties of the La_2O_3 MIM capacitor are measured by the temperature-controlled chuck of the probe station, such as leakage current, capacitance density, breakdown biased voltage, and reliability characteristics. For all of electrical measurements, the voltage and the altering signal are applied to the top electrode while the bottom electrode was grounded.

The leakage current-voltage (*J-V*) measurements are preformed on the Agilent-4156C semiconductor parameter analyzer in the temperature range from 25 °C to 125 °C to evaluate the conduction mechanisms of the La_2O_3 MIM capacitors. After taking about 30 minutes to stabilize the temperature of wafer and chuck, the measurement starts at 0 V and sweeps towards the high electric field region with a 0.1 V voltage step. Afterwards, the numerical fitting of the measured J-V data is carried out according to the theories and the equations stated in chapter 2.

The capacitance-voltage (*C-V*) curves are measured by the Agilent 4284A precision impedance meter, and the dielectric loss-voltage (*D-V*) curves could also be observed at the same time. The biased voltage on the top electrode of the La_2O_3 MIM capacitor sweeps from −2 V to 2 V at frequencies varying from 10 kHz to 500 kHz by applying an ac signal with

25-mV amplitude. The thermal stress on this MIM capacitor is also carried on with measurement temperatures varying from 25 °C to 125 °C. Together with the La_2O_3 physical thickness obtained from transmission electron microscope (TEM), the dielectric constant of the deposited La_2O_3 film (k_{La2O3}) could be determined as

$$k_{La2O3} = C \times \frac{d}{\varepsilon_0} \times \frac{1}{S} \quad (3\text{-}1)$$

, where ε_0 is the permittivity of free space, S is the capacitor area, d is the physical thickness of the La_2O_3 film, and C is the capacitance at zero bias, at 100 kHz, and at 25 °C. Consequently, the equivalent oxide thickness (EOT) of the deposited La_2O_3 film could be calculated by

$$EOT = \frac{k_{SiO2}}{k_{La2O3}} \times d \quad (3\text{-}2)$$

, where k_{SiO2} is the dielectric constant of the silicon dioxide.

As for the accuracy of analog functions performed by the MIM capacitors, the dependence of capacitance on the biased voltage (V), the temperature (T), and the frequency (F) are investigated. For one thing, *C-V* curves in the voltage range from −1.5 V to 1.5 V are fitted by the following second order polynomial equation as

$$C(V) = C(V=0) \times \left(\alpha \times V^2 + \beta \times V + 1\right) \quad (3\text{-}3)$$

, where C(V=0) is the capacitance at zero bias, α (ppm/V^2) is the quadratic voltage coefficient of capacitance, and β (ppm/V) is the linear voltage coefficient of capacitance. The parameter β could be cancelled by circuit design [121], but the parameter α could not. Therefore, only the parameter of α under various measurement frequencies and various temperatures are discussed in this thesis. What is more, for the discussion of the thermal stability of the MIM capacitors, the temperature coefficient of capacitance (TCC) is extracted as the slope of a capacitance-temperature (*C-T*) plot in the temperature range of 25 °C to 125 °C, as shown in Eq. 3-4.

$$TCC = \frac{1}{C(T = 25°C)} \times \frac{\partial C(T)}{\partial T} \tag{3-4}$$

As a result, the TCC (ppm/°C) for a certain bias and a certain frequency condition could be obtained. In this work, the temperature coefficients of capacitance (TCC) at zero bias are fitted to exhibit the temperature dependency of capacitance.

Concerning the frequency dispersion in MIM capacitors, the frequency coefficient of capacitance (FCC) could be defined as the slope of a C-$\log_{10}$F plot in the frequency range from 10 kHz to 500 kHz by

$$FCC = \frac{-1}{C(F = 10kHz)} \times \frac{\partial C(F)}{\partial \log_{10} F} \tag{3-5}$$

, where C(F = 10 kHz) is the capacitance at 10 kHz, the minimum frequency we measure. In this study, the frequency coefficients of capacitance at zero bias are derived as the indicators of the frequency dependency of capacitance.

Moreover, from the viewpoint of practical use, it is very important to clarify the stability of MIM capacitor properties during long-term voltage stress. Therefore, the constant voltage stress (CVS) in the range of −4 V to −5 V at the temperature of 25°C is conducted by utilizing the Agilent-4156C semiconductor parameter analyzer. The *C-V* and *J-V* characteristics of La_2O_3 MIM capacitors are also measured at various time intervals during CVS testing. To inspect the stress induced instability of La_2O_3 MIM capacitor, the relative leakage current variation and the relative capacitance variation during stressing compared to fresh conditions are observed as

$$\frac{\Delta J}{J(t=0)} = \frac{J(t) - J(t=0)}{J(t=0)} \tag{3-6}$$

$$\frac{\Delta C}{C(t=0)} = \frac{C(t=0) - C(0)}{C(t=0)} \tag{3-7}$$

, where J(t=0) and C(t=0) are the initial leakage current density and the initial capacitance

density, respectively. The leakage current and the capacitance measured at various time intervals during CVS testing are extracted at the applied voltage at −1 V and 0 V, respectively. In the same way, the relative variation in dielectric loss, in quadratic voltage coefficient of capacitance, and in temperature coefficient of capacitance caused by CVS with respect to its initial values are acquired as following

$$\frac{\Delta D}{D(t=0)}=\frac{D(t)-D(t=0)}{D(t=0)}, \tag{3-8}$$

$$\alpha \quad ratio=\frac{\alpha(t)}{\alpha(t=0)} \tag{3-9}$$

$$TCC \quad ratio=\frac{TCC(t)}{TCC(t=0)}. \tag{3-10}$$

Here, D(t=0) and D(t) are the dielectric loss at V=0 before and during stressing monitored by the Agilent 4284A precision impedance meter. α(t=0) and α(t) are the extracted quadratic voltage coefficients of capacitance before and during stressing. TCC(t=0) and TCC(t) are the deduced temperature coefficients of capacitance before and during stressing.

Additionally, the charge injecting into the dielectric film of the MIM capacitor during stressing could be determined by Q_{inj} (C/cm^2) from the integration formula

$$Q_{inj}=\int_0^t J_{stress}(t)\cdot dt \tag{3-10}$$

, where $J_{stress}(t)$ is the current density as a function of time flowing through the La_2O_3 film and the term “t” also refers to the stress time. More specifically, the Q_{inj} is the area under the curve of the J_{stress} versus stressing time, as schematically described in Fig. 3-3.

On the other hand, the reliability issues include time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) are discussed to demonstrate the lifetime and integrity of the dielectrics of fabricated MIM capacitors. In the first place, the TZDB measurement method was a J-V measurement with increasing applied voltage until the

dielectric breakdown, and then the cumulative results of the breakdown field (E_{BD}, MV/cm) are obtained because of the wide range of E_{BD} data. In the second place, the TDDB measurements are carried out by means of the CVS at 75°C with appreciable current flow (J_{stress}) through the dielectric, and the evolution of the J_{stress} with time during the CVS could be monitored. When a sudden jump in J_{stress} occurrs, the time of this event is called as the time to breakdown (t_{BD}) point. The charge to breakdown (Q_{BD}) of MIM capacitor defined by the necessary charge density injection until the dielectric breakdown could be computed from the following equation

$$Q_{BD} = \int_{0}^{t_{BD}} J_{stress}(t) \cdot dt \ . \tag{3-11}$$

Hence, the t_{BD} and Q_{BD} could be estimated in this work. The statistics of TDDB are described by the Weibull distribution [30]

$$F_C(t) = 1 - \exp\left(-\frac{t^{\beta_C}}{\alpha_C}\right) \tag{3-12}$$

, where $F_C(t)$ is the cumulative probability of the t_{BD}, α_C is the scale factor, and β_C is called the shape factor or Weibull slope, as depicted in Fig. 3-4. By extrapolating all the α_C data with respect to applied voltages, the lifetime projection of La_2O_3 MIM capacitors to operational voltages could be realized, as schematized in Fig. 3-5. Furthermore, β_C is also useful in predicting lifetime distribution for various capacitor areas. For example, the relationship between the scale factor ratio (α_C/α_{C0}) and the area ratio (S/S_0) could be described as the following equation [30]

$$\frac{\alpha_C}{\alpha_{C0}} = \left(\frac{S_0}{S}\right)^{\frac{1}{\beta_C}} \tag{3-13}$$

, where the S_0 and the α_{C0} are the initial area and the scale factor of capacitor, respectively.

3.3 MATERIAL ANALYSES

The physical characterization of deposited La_2O_3 films consisted of the transmission electron microscopy (TEM) image for physical thickness determination, and the X-ray photoelectron microscopy (XPS) measurements for the composition scrutiny. And all of these material analysis techniques were briefly stated behind.

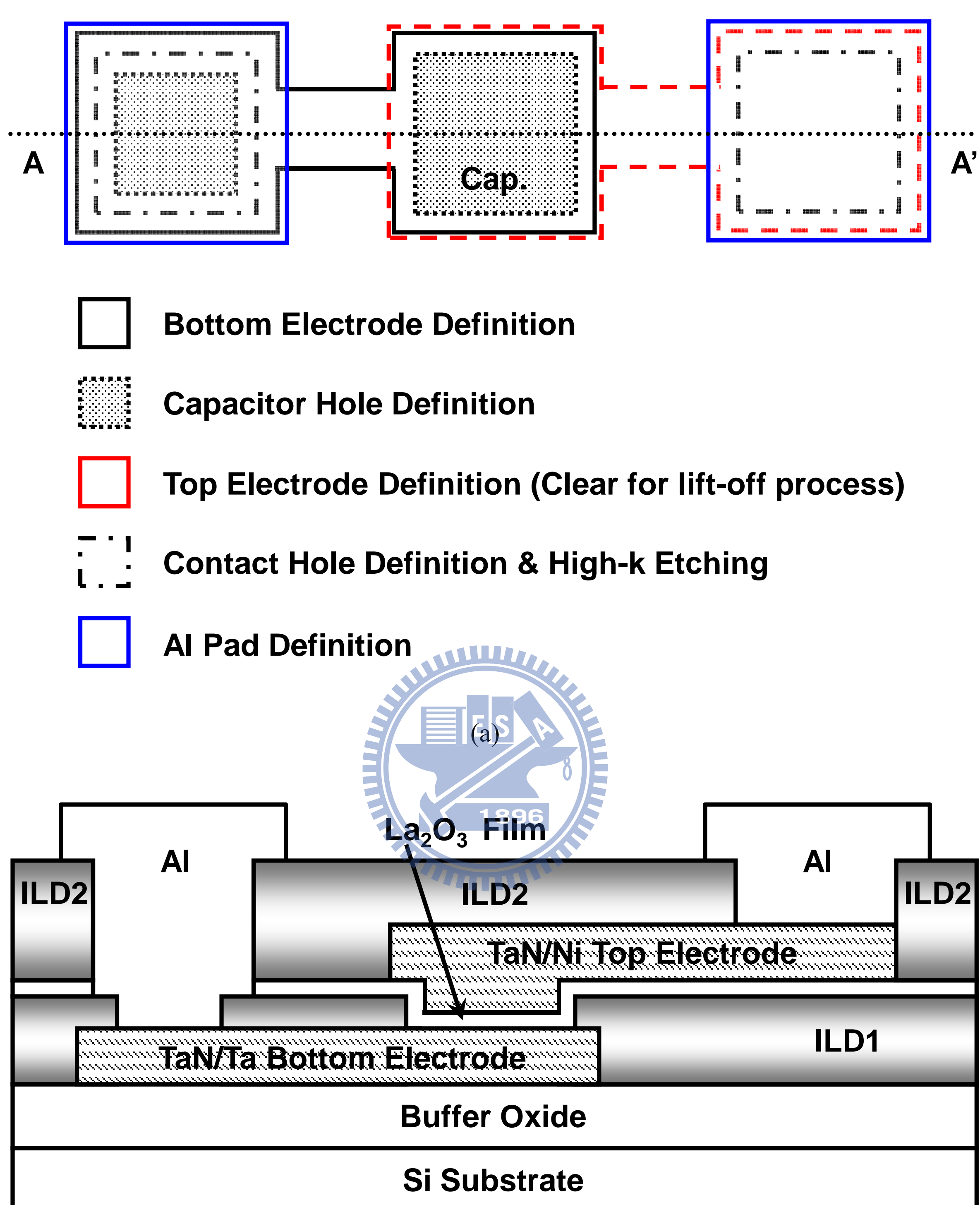
To begin with, the La_2O_3 physical thickness (cross section) of the fabricated samples was determined by the TEM image. In TEM, observation is made in ultrahigh vacuum, where an electron beam is focused onto the sample by electromagnetic lenses. Because the electron beam's wavelength is less than that of visible spectra, the resolution of TEM is higher than that of the conventional optical type microscope. In this work, the deposited high-κ dielectric is prepared by using a focus ion beam (FIB) system with the model Nova 200 of FEI Company, and then it is transferred to JEOL JME-3000F TEM system for observing its thickness.

Next, the XPS system (Microlab 350, Thermal VG Scientific Company, England) was used to detect the composition of our deposited high-k dielectrics after annealing. The XPS, also known as the electron spectroscopy for chemical analysis (ESCA), is a quantitative spectroscopic technique to measure elemental composition, empirical formula, chemical state, and electronic state of elements existed within a material. Samples would irradiate with X-ray, and their emitted photoelectrons with kinetic energy (KE) are detected. The measured kinetic energy (KE) is given by

$$KE = hv - BE - \phi_S \tag{3-14}$$

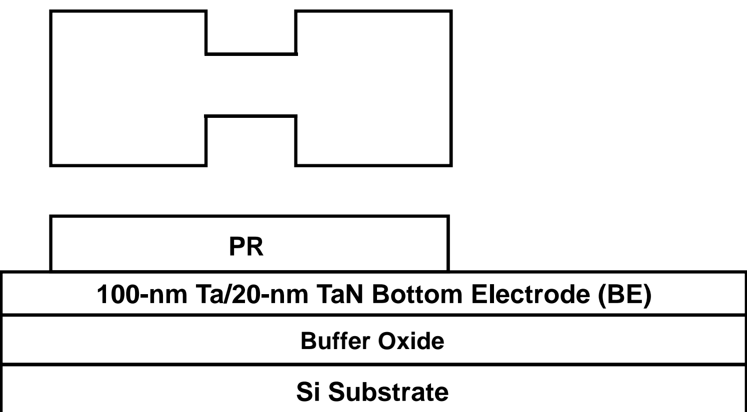
, where hv is the photon energy, BE is the binding energy of the atomic orbital where electron generates, and ϕ_S is the spectrometer work function. The binding energy is the minimum energy to break the chemical bond inherent in each bond of the measured molecule.

Thus, the binding states could be identified by the positions of the binding energies where the peaks appear. In the case that the peak position is different from the expected positions, the chemical bond states are discussed the amount of shifting to the higher or the lower energy side.

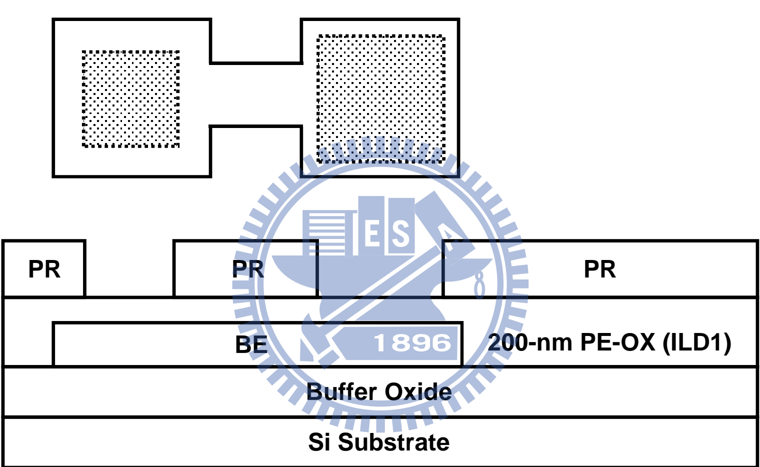


(b)

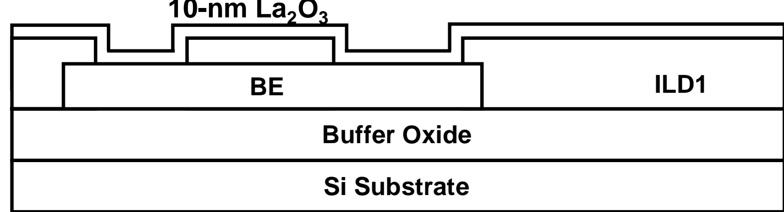
Fig. 3-1. (a) The schematic layout of the La_2O_3 high-k MIM capacitors. (b) The cross-sectional structure along the A-A' dashed line in the layout shown in (a).



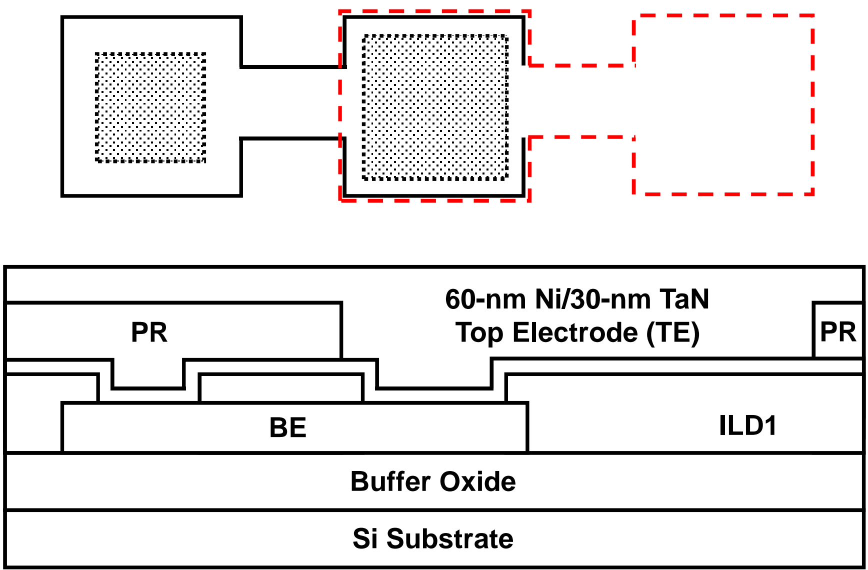
(a) Bottom electrode deposition and patterning



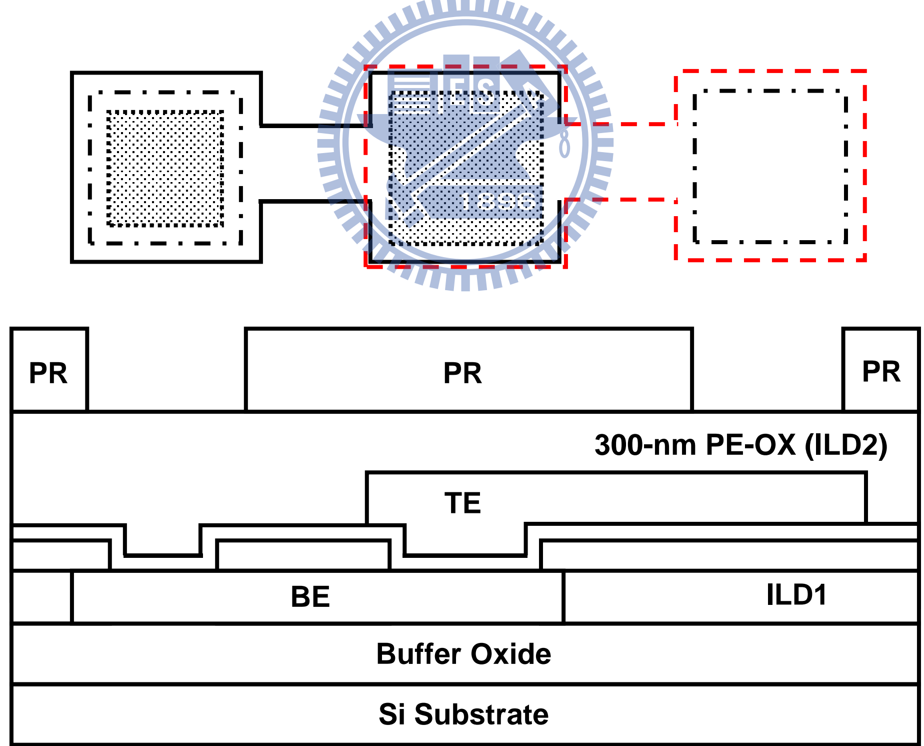
(b) ILD1 deposition and capacitor hole region opening.



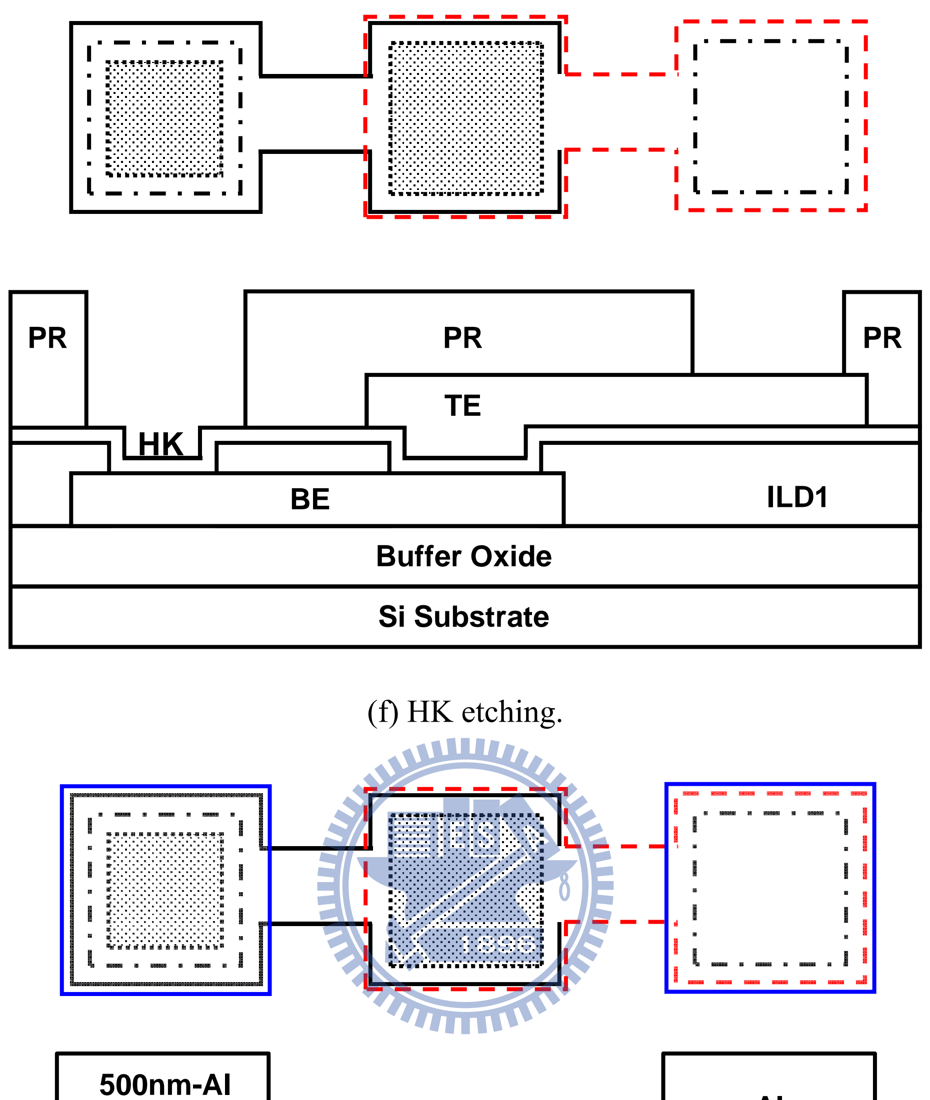
(c) High-k dielectric (HK) deposition and furnace annealing.



(d) Top electrode deposition and patterning by using the lift-off technique.



(e) ILD2 deposition and contact hole opening.



(f) HK etching.

(g) Al deposition and patterning.

Fig. 3-2. The main fabrication steps of the MIM capacitor with the La_2O_3 high-k dielectric and the process steps corresponding to their used photo masks.

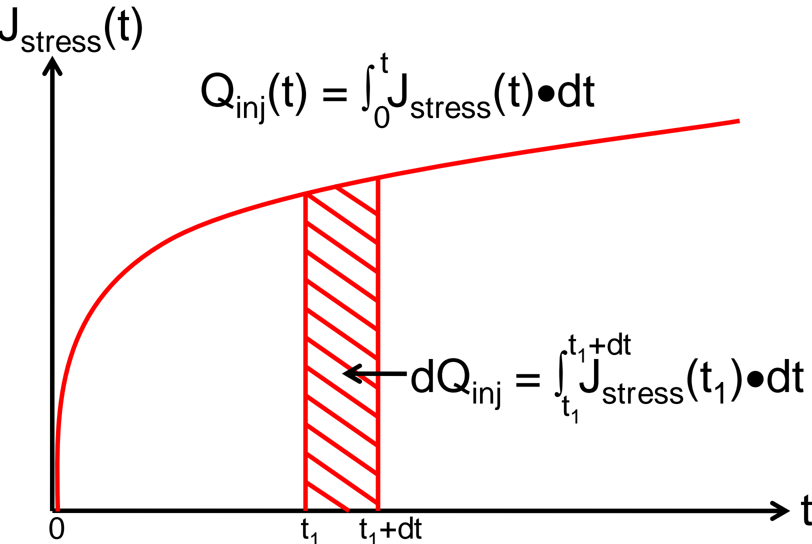


Fig. 3-3. The total injection charges density (Q_{inj}) of MIM capacitor extracted from the area under the curve of the stress current density (J_{stress}) versus stressing time.

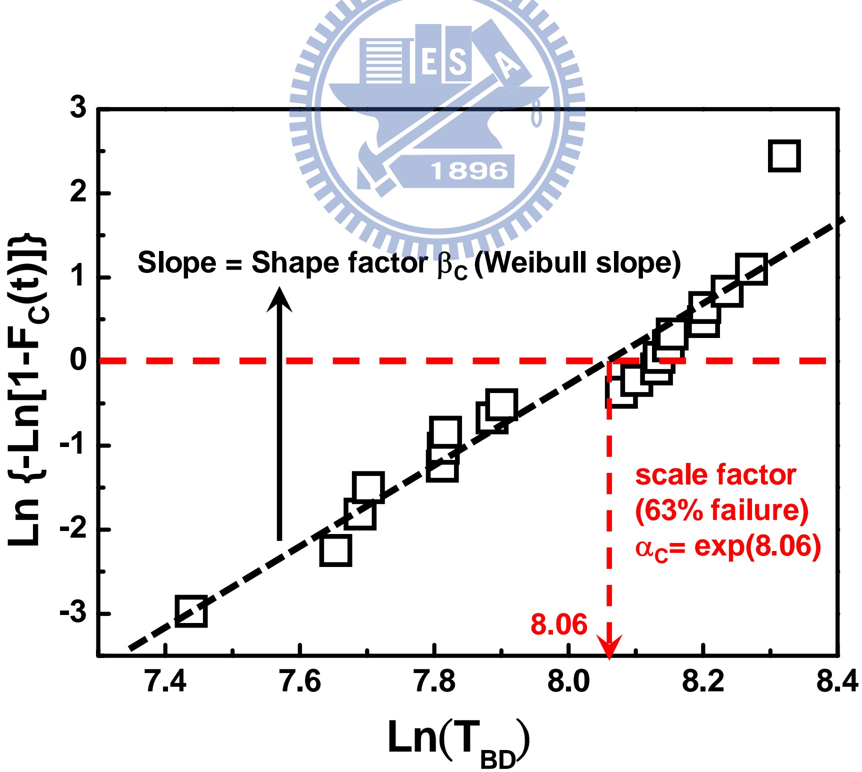


Fig. 3-4. The shape factor β_C (Weibull slope) and the scale factor α_C extracted from the TDDB plot.

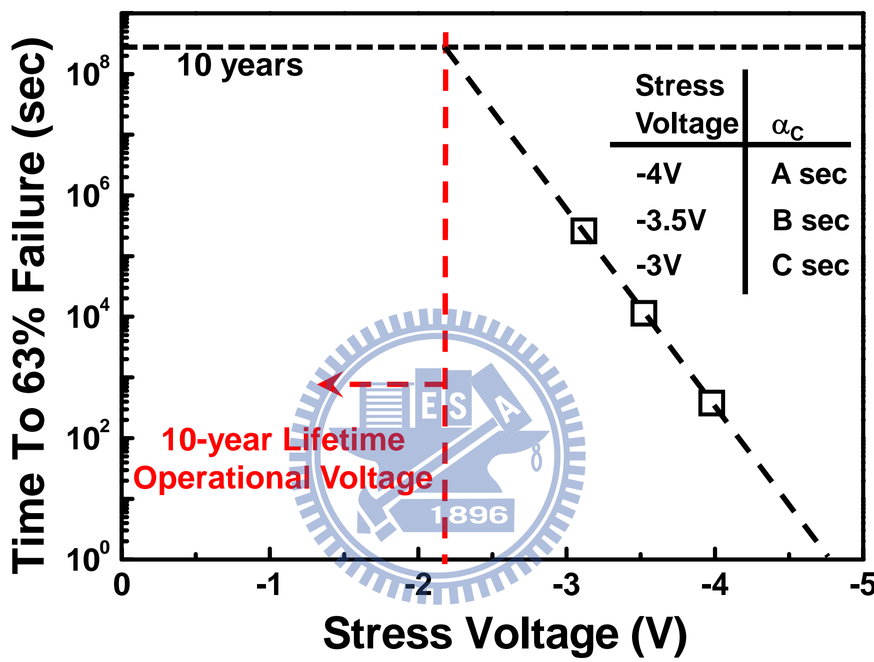


Fig. 3-5. The lifetime projection of MIM capacitors obtained from the failure plot with various stress voltages.

CHAPTER 4

Results and Discussion

This chapter falls into four main categories. Section 4.1 describes the basic properties and various physical analyses of La_2O_3 films, including the X-ray photoelectron spectroscopy (XPS) and the transmission electron microscopy (TEM). Secondly, section 4.2 studies the leakage current and the conduction mechanisms of the La_2O_3 MIM capacitor. Thirdly, considering for the accuracy of analog functions performed by the MIM capacitors, the relationships among the applied voltage, the temperature, and frequency on the capacitance of the La_2O_3 MIM capacitor are observed, corresponding to the quadratic voltage coefficient of capacitance (α), temperature coefficient of capacitance (TCC), and the frequency coefficient of capacitance (FCC), respectively. Next, as for the stability on the La_2O_3 MIM capacitors in practical use, section 4.4 investigates the stress induced variation on the capacitance density, the quadratic voltage coefficient of capacitance (α), the temperature coefficient of capacitance (TCC), and the leakage current density. Finally, the inquiries into breakdown and reliability characteristics of the La_2O_3 MIM capacitor are stated in section 4.5, such as the time-zero dielectric breakdown (TZDB) and the time-dependent dielectric breakdown (TDDB), respectively.

4.1 BASIC PROPERTIES OF THE E-BEAM EVAPORATED La_2O_3 DIELECTRIC FILMS OF MIM CAPACITORS

The chemical composition of the e-beam evaporated La_2O_3 film after 400-°C furnace annealing in O_2 ambient for 10 minutes is determined by X-ray photoelectron spectroscopy (XPS) analysis. The La 3d and O 1s core level spectral regions are detected and shown in Figs. 4-1(b) and 4-1(c), respectively. Considering the area integrated from the peak spectral to the binging energy, the atomic concentration ratio of lanthanum atom to oxygen atom could be determined about 2: 3. The La 3d signals of the La_2O_3 film consisted of the energy splitting of the $3d_{3/2}$ and the $3d_{5/2}$ spin-orbit doublets. The main La 3d XPS peak is centered at 856.7 eV, and its spin-orbit component is separated at 836.1 eV. The binding energy and the spin-orbit component associated with the present La_2O_3 features are in agreement with the XPS reference book [122]. Besides, the XPS peak of O 1s core level spectral, as presented in the Fig. 4-2(c), at binding energy of 533.1 eV could be regarded as the La-O bonding. A broad signal existed at lower binding energy of 530 eV due to the overlap of various components is associated with oxide and hydroxide on the La_2O_3 film surface.

The thickness of the deposited La_2O_3 film on the bottom electrode is decided by the cross-sectional transmission electron microscope (TEM) image of the fabricated MIM structure, as indicated in the bottom inset of Fig. 4-2. It could be found that the physical thickness of the La_2O_3 film is about 10 nm after being annealed in oxygen ambient. Fig. 4-2 shows the typical capacitance-voltage (C-V) characteristic of the La_2O_3 MIM capacitor at 100 kHz from −2 V to 2 V. The capacitance density of the 10-nm La_2O_3 MIM capacitor measured at the zero bias is 11.4 fF/μm^2. As a result, the effective dielectric constant (k_{La2O3}) value and the equivalent-oxide thickness (EOT) derived by the Eq.3-1 and Eq. 3-2 are 12.9 and 3 nm, respectively. Besides, an obvious interfacial layer (IL) between dielectric and bottom electrode is observed. This unavoidable IL might be formed as the high-k layer directly

contacts the metal electrode.

The calculated k_{La2O3} value is 12.9 in this work, which is smaller than that in the other reports [22], [34], [36], [37]. The main reason for this low k_{La2O3} value might be the low-temperature post deposition annealing [40], [123]. As the paper reported in [40], the dielectric constant of the La_2O_3 film deposited by the atomic layer deposition (ALD) at 300 °C is 9. When as-grown ALD La_2O_3 film is subjected to anneal from 400 °C to 500 °C, its dielectric constant could be raised from 12.5 to 17.3 since the improvement in its crystallinity and densification. In this study, the La_2O_3 MIM capacitor for RF/analog applications is located in the interconnection levels and above the active integrated circuit layers. Although the increase in annealing temperature could raise the dielectric constant of the La_2O_3 film, the maximum process temperature is limited to 400 °C to fulfill the thermal budget requirement of the backend process. Despite that the dielectric constant of La_2O_3 film in this research is 12.9 annealed in a low temperature of 400 °C, the capacitance density with the magnitude of 11.4-fF/μm^2 is sufficient for RF applications until 2018, as mentioned in chapter 1.

4.2 Leakage Current and Conduction Mechanisms of La_2O_3 MIM Capacitors

In spite of possessing higher capacitance density in the same physical thickness, the lager leakage current of the high-k La_2O_3 MIM capacitor is higher than that of the SiO_2 one, which could be ascribed to the smaller conduction band gap offset (ΔE_{CB}) of La_2O_3 dielectric. Since the leakage current issue limits the aggressive scaling of dielectric thickness which has an impact on the capacitance as depicted in Eq. 3-1, the technological evolution of high-k MIM capacitors requires a lower leakage current to enhance the capacitance density and reduce the power consumption. The capacitor fabricated by dielectric material with a large energy band gap and a high dielectric constant value could obtain a low leakage current and a large

capacitance density, respectively. However, the dielectric constant and bandgap for high-κ dielectric materials are usually trade-off. Hence, we choose the La_2O_3 dielectric with the largest ΔE_{CB} of 2 eV, compared to the other reports, as our insulator in MIM capacitor. In this section the leakage currents at measurement temperatures varied from 25 °C to 125 °C were obtained and current transport mechanisms of the La_2O_3 MIM capacitor were studied.

Fig. 4-3 sketches the energy band diagram of the Ni/La_2O_3/TaN MIM capacitor. The ideal work-functions of the top electrode (Ni) and the bottom electrode (TaN) are about 5 eV and 4.6 eV, respectively, and the electron affinity of La_2O_3 dielectric is 1.7 eV. The top electrode is applied voltage and the bottom electrode is grounded during measurement. When the positive voltage is applied on the top electrode, the electron carriers inject from the bottom electrode to the insulator named as the bottom injection, whereas the top injection condition is when negative voltage is applied. Fig. 4-4 illustrates the leakage current density of the 10-nm La_2O_3 MIM capacitor measured at 25 °C, where the leakage current at −1V and +1 V were 9.4 and 45 nA/cm^2, respectively, even if the biased voltage is −6 V that the corresponding electrical field applied on the MIM capacitor is up to 6 MV/cm, the leakage current density is still below 10^{-5} A/cm^2, and the features are superior to any other reported data of the MIM capacitors with La_2O_3 high-k dielectrics.

Fig 4-5 shows the leakage current of 10-nm La_2O_3 MIM capacitor measured at a negative bias on nickel electrode from 25 °C to 125 °C. It could be found that every curve has two transition regions, where the leakage current density with the increase of the temperature. The leakage current density is kept below 100 nA/cm^2 in the first region, whereas it is hugely increased in the second region. These phenomena represent various conduction mechanisms of carriers (electrons) depending on the electric field and the temperature. Therefore, we use the Poole-Frenkle emission and the Schottky emission to verify the conduction mechanisms of La_2O_3 MIM capacitor in the high field region and in the low field region, respectively. Fig. 4-6 plots the natural logarithm of the leakage current density divided by electric field ln(J/E)

versus the square root of electric field $E^{1/2}$ in the high field region according to the Eq. 2-5. Regarding to various measurement temperatures, a well linear correlation between ln(J/E) and $E^{1/2}$ could be obtained in the high field region. On account of the slopes of these fitted straight lines, the extracted ε_r value is largely increased with the increasing temperature. The reason for large increase of the extracted ε_r value can be contributed to unsuitable fitting region. The straight line could explain this conduction mechanism belongs to Poole-Frenkle emission, but the extracted ε_r value and the effective trapping level energy are not good agreement. Next, we take the other method to extract ε_r value. The extracted slope in Fig, 4-7 is chosen to re-plot the slope versus $(qE/\pi)^{1/2}$ curve, as shown in the Figs. 4-7(a) and 4-7(b). The best fitting region on applied voltage could be determined by negative slope in these plots. Therefore, the ε_r value and the effective trapping level energy could be extracted as 3.77~3.53 and 1.15~1.50 eV, respectively. The extracted ε_r value is close to the dynamic dielectric constant of La_2O_3 at optical frequencies, i.e., the square of its refractive index (~1.87~1.93).

To study the leakage mechanism in low field region, the ln(J) is arbitrarily plotted as a function of $E^{1/2}$ to verified whether Schottky emission or not. Fig. 4-8 shows the typical plotting of ln(J) versus $E^{1/2}$, and the fitted straight lines with various temperatures. The extracted ε_r value is increased with the increasing temperature and these curves appear the linearity in the low electric field. Further, a linear relationship between $\ln(J/T^2)$ and q/kT also should be displayed in terms of Schottky emission. Therefore, we also plot this linear relationship from the applied voltage from −0.6V to −1.6V in Fig. 4-9. It indicates the data could be fitted well by a straight line at various electric fields, which many research conclude this leakage mechanism is the Schottky emission, but it seems not always true. As the same method in the PF emission extraction, we also plot the extracted slope versus the $E^{1/2}$ in the inset of Fig. 4-9. According to this inset, however, the slope in the inset is negative, not compatible with the positive square root term in the extracted slope from Fig. 4-9. Therefore, the Schottky emission mechanism for this 10-nm La_2O_3 MIM capacitor in low electric field is

not valid. In fact, the Schottky emission mechanism is electrode limitation and contributed by the carriers that overcome the barrier between the electrode and the insulator. It has been verified in many researches for metal-insulator-silicon (MIS) capacitor with ultra-thin high-k dielectric without considering defects inside the bulk film. If there are more defects in the thick high-k dielectric, especially on processing at low temperature of 400 °C in this work, the traps assisted tunneling at high temperature would become more obvious and complex in low field region. As mentioned in chapter 1, the high-k dielectrics have high trap density in themselves and they have lots of interface states in their bandgap. Moreover, the deposited films have huge amounts of defects compared to the thermally grown films, especially for the e-beam evaporated films. Therefore, we may reasonably suppose that a trap-related conduction also affect the leakage current of high-k La_2O_3 MIM capacitors in the low field region.

In summary, it could be concluded that the conduction mechanism of 10-nm La_2O_3 MIM capacitors is dominated by the Poole-Frenkel emission at high applied voltage region. On the other hand, at low field region, the Schottky emission is not a unique conduction mechanism, another trap-related conduction also influences the conduction behavior of MIM capacitors at low bias, due to the trap-rich characteristic of La_2O_3 films.

4.3 EFFECTS OF VOLTAGE, TEMPERATURE, AND FREQUENCY ON THE CAPACITANCE OF LA_2O_3 MIM CAPACITORS

The performance of RF circuit would be ultimately limited by the accuracy of its passive components. It is also known that the capacitance of the MIM capacitor with high-k dielectric would vary with the operational voltage, the temperature, and the frequency to lead to distortion in analog signals for RF application [6]. However, the physical mechanisms of these influences upon capacitance are still unclear and they are necessary to investigate. In

this section, accordingly, we evaluate the relationships among the applied voltage, the temperature, and the frequency on the capacitance of the La_2O_3 MIM capacitor, corresponding to the quadratic voltage coefficient of capacitance (α), temperature coefficient of capacitance (TCC), and the frequency coefficient of capacitance (FCC), respectively.

4.3-1 Characteristics of Voltage Coefficient of Capacitance

Fig. 4-10 shows the C-V curves of the 10-nm La_2O_3 MIM capacitor measured at frequencies varied from 10 kHz to 500 kHz and at the temperature of 25 °C. As can be seen, the capacitance density rises with the increase of applied voltage and it expresses a parabolic curve with a positive curvature. This reason on the increase of capacitance might be attributed to the high degree of electric field polarization and carrier injection [6], [23], [103]. When the voltage applied on the electrode sweeps from zero to a high voltage level, some of injection carriers would be captured by interface trap states existing in the dielectric near the injection electrode. Then, these trapped charges could induce internal dipoles to follow the alternating signals with a dipole relaxation time. Besides, the other excess mobile charges in the insulator also follow the small ac signals with a space charge relaxation time. Consequently, both dipole relaxation and space charge relaxation behaviors could modulate the capacitance, resulting in the capacitance fluctuation ($\Delta C = C(V) - C(V=0)$) with the varied applied voltages. This phenomenon, named as voltage nonlinearity or voltage dispersion of capacitance, could be depicted by the voltage coefficient of capacitance (VCC).

The VCC fitting curves and the extracted α values according to the Eq. 3-3 are indicated in Fig. 4-11(a), under the top injection condition from 10 kHz to 500 kHz at 25 °C. The quadratic voltage coefficient of capacitance (α) decreases from 775 to 595 ppm/V^2 as the frequency increases from 10 kHz to 500 kHz. The reason for the lower VCC with the frequency increasing is that the trapped charges induced dipoles and the excess mobile

charges hardly follow the ac signal with higher frequency, corresponding to the higher relaxation times of these dipoles and mobile charges [24], [103], [124]. On the other hand, in Fig 4-11(b), the α value under the top injection is significant smaller than that under the bottom injection with the same measurement frequency. This asymmetry on the quadratic voltage coefficient of capacitance (α) of the top injection and bottom injection results from the difference in workfunction between top (Ni, 5 eV) and bottom (TaN, 4.6 eV) electrodes. Since the top electrode (Ni) with high workfunction has a larger barrier height to suppress the charges injection, the amount of trapped charge induced dipoles and excess mobile carriers in the La_2O_3 dielectric could be reduction to improve the voltage linearity. This experimental result further confirms that the charge injection effect at metal/dielectric interface dominates the voltage dispersion of capacitance rather than the bulk effect, such as a field dependent polarization, which is consistent with observations in other works.

In addition, the α value increases with the rise in temperature, as illustrated in Fig. 4-12. As the temperature elevates, more energetic carriers could easier inject from the electrode into the dielectric, and further the field enhanced electron hopping process in the dielectric is more remarkable. It could be expected that the higher charge in trapping/detrapping rate of dielectric would increase the quantity of mobile charges to affect the voltage coefficient of capacitance (VCC) at high temperature. As a result, the variation in capacitance becomes more sensitive to alternating voltages at high temperature and then causes the degradation in voltage linearity, especially in the lower frequency measurement condition. Moreover, the magnified distinction in α among various frequencies at elevating temperature might be attributed to the reduction in mobility of injection carriers [103]. The injection charges caused the VCC variation are classified two types, trapped charges induced dipoles and excess mobile charges. However, the trapped charges induced dipoles are more energetic and easier to follow high frequency alternating signals at high temperature. Therefore, these dipoles are

not the main reason to cause the magnified distinction in α. Although the larger amount of excess mobile charges would be generated inside the insulator to cause large α value at high temperature, the fraction of total excess mobile charges with enough high mobility, which could follow high frequency signal at higher temperature, is less than that at low temperature. Accordingly, the deviation in α measured at various frequencies at high temperature is larger than that at low temperature. This result clarifies the significance of interface charge injection on voltage dependency of capacitance for La_2O_3 MIM capacitors again.

4.3-2 Characteristics of Temperature Coefficient of Capacitance

Fig. 4-13 manifests the capacitance-temperature relationships at frequencies range from 10 kHz to 500 kHz for 10-nm La_2O_3 MIM capacitors. For instance, the capacitance density of the 10-nm La_2O_3 high-k MIM capacitor rises from 11.4 to 11.78 fF/μm^2 as the temperature increases from 25 to 125°C at 100 kHz. When the temperature elevates, the number of excess mobile charges inside the insulator would be increased and the electron hopping behaviors could easily occur as abovementioned, which has a positive impact on capacitance density. In addition, the polar molecular dipoles in insulator and the trapped charge induced dipoles at interface are also more energetic to follow the ac signals, leading to the higher capacitance. This thermal excited capacitance variation, the temperature dependency of capacitance, could be interpreted by the temperature coefficient of capacitance (TCC), as signified in previous chapter.

Fig. 4-14 exhibits the normalized capacitance as a function of temperature and the corresponding extracted TCC parameters based on Eq. 3-4. The TCC declines from 388 to 306 ppm/°C as the measurement frequency rises from 10 kHz to 500 kHz, which is similar to the trend of VCC data. However, the divergence in TCC seems small between low and high frequency. These properties imply that the charge injection effect at metal/insulator interface

is not the only one participator which dominates the temperature dependency on capacitance of La_2O_3 MIM capacitors.

Afterwards, the evaluated TCC data under various frequencies and biased conditions are depicted in Fig. 4-15. As the applied voltage increases from zero to 1.5 V and to −1.5 V, the TCC value at 200 kHz increases from 308 ppm/°C to 365 ppm/°C and to 358 ppm/°C, respectively. The external applied field on the MIM capacitor is evidently able to raise the TCC value. Unlike the VCC characteristic with a large dependence on the polarity of applied voltage, the top injection shows slightly lower TCC value than the bottom injection under the same measured frequency. Therefore, except for the interface charge injection, the other critical factor independent on the barrier height at metal/insulator interface would dominate the changes in TCC. The earlier research [125] has been pointed out that the temperature prompted capacitance variation of the high-k MIM capacitor originates from the bulk characteristic of the insulator but neglects the interfacial polarization. Consequently, we suggest that the bulk effect principally governs the temperature dependence of capacitance of the La_2O_3 MIM capacitor, such as the field dependent polarization generated by polar molecular or bulk traps induced dipoles in the insulator.

4.3-3 Characteristics of Frequency Coefficient of Capacitance

Fig 4-16 presents the relationship between capacitance and operational frequency at the temperature in the range of 25 °C to 125 °C. When the measurement frequency grows from 10 kHz to 500 kHz, the capacitance density of the La_2O_3 high-k MIM capacitor declines from 11.43 to 11.37 fF/μm^2 at 25 °C. As the frequency increases, dipoles and mobile carriers in the dielectric are more difficult to follow to alternating small signals that leads to the higher relaxation time and thus, the capacitance density of the La_2O_3 high-k MIM capacitor decreases. These characteristics, denoted as frequency dependence or frequency dispersion of

capacitance, are expressed by the frequency coefficient of capacitance (FCC) which has been stated in chapter 3.

The normalized capacitance as a function of frequency and the related FCC values calculated based on Eq. 3-5 are exhibited in Fig. 4-17. The obtained FCC rises from 0.0037 per decade to 0.0091 per decade at the temperature varied from 25 to 125°C, this apparent temperature dependency phenomenon is similar to the trend of VCC data. At elevated temperature, even though the higher concentration of mobile charges would influence the capacitance, the mobility of carriers becomes smaller and the larger relaxation time is achieved, which results in the less fraction of total excess charge in dielectric could follow the higher frequency alternating signals. Therefore, the reduction of capacitance with the increase in frequency is enlarged at high temperature, which leads to the far distinction in FCC between low and high measurement temperature. More specifically, the fluctuation in capacitance caused by varied operation frequency might be arise from the excess mobile charges in insulator, which has much in common with the VCC characteristic. This result is consistent with statements presented in chapter 2 that the space charge relaxation dominates the dielectric frequency dispersion at frequencies varied from 10 kHz to 500 kHz, as schematized in Fig. 2-11.

4.3-4 Summary

In this section, we demonstrate the analog properties of the 10-nm La_2O_3 MIM capacitor. The capacitance rises with the increase of applied voltage or measurement temperature to result in the positive VCC and TCC, while it decreases with the raise of operational frequency and leads to the positive FCC. The VCC characteristic of the La_2O_3 MIM capacitor is dominated by the space charge polarization and relaxation, which could be drastically decreased by measuring under higher frequency or on the electrode of high workfunction but could be increased at high temperature. The TCC property of the La_2O_3 MIM capacitor is

principally governed by the dipolar polarization and relaxation, which could be decreased by increasing the measurement frequency and could be largely increased by the applied voltage. Besides, the space charge relaxation is mainly responsible for the FCC characteristic of La_2O_3 MIM capacitors under the measurement frequency ranges from 10 kHz to 500 kHz, which could be increased by elevating measurement temperature.

4.4 Behaviors of La_2O_3 MIM Capacitors Under Constant Voltage Stress

In terms of the precision performance of long-term use, the stability of MIM capacitors under electrical stress is a key issue. Some studies [101], [102] have discussed the capacitance variation of SiO_2 MIM capacitors under electrical stress. However, the degradation of the high-k MIM capacitor due to the electrical stress has not been well characterized. In this section, the behaviors of 10-nm La_2O_3 MIM capacitors with the 11.4-fF/μm^2 capacitance density under constant voltage stress (CVS) are demonstrated. For one thing, the variations in leakage current [$\Delta J/J(t=0)$] under the CVS testing are evaluated. What is more, the relationship between the injected charges (Q_{inj}) and the capacitance change [$\Delta C/C(t=0)$] under stress is demonstrated. Finally, correlations among the quadratic voltage coefficient of capacitance (α), the temperature coefficient of capacitance (TCC), and the dielectric loss (D) of the La_2O_3 MIM capacitor under CVS are also studied.

4.4-1 The Variation in Leakage Current

Fig. 4-18(a) expresses the evolution of J-V curves of the La_2O_3 MIM capacitor stressed at −5 V in the case of top injection, and Fig. 4-18(b) illustrates the absolute magnitude of [J(t)-J(t=0)] as a function of applied voltage with different stress time obtained from Fig.

4-18(a). At low applied voltage region, where the conduction mechanism is dominated by Schottky emission like conduction, the J-V curve of the MIM capacitor during stressing dramatically increases and then decreases compared to the fresh condition. As the voltage applied, the trap filling and trap-assisted conduction dramatically increase the leakage current of the MIM capacitor referred to as stress induced leakage current (SILC). The SILC can be best explained by the generation of neutral electron traps in the dielectric [126] which allows more current to flow through the oxide layer by these traps. These traps act as "stepping stones" for tunneling carriers which is known as trap-assisted tunneling. The generation of these neutral sites is caused mainly by the "trap creation" phenomenon related to energy released by energetic electrons caused by negative CVS. After the traps near the metal/insulator interface are all filled due to the sufficient electrons supplied by the applied voltage, these trapped electrons would increase the interface barrier height that suppresses the further injection charges from the top electrode, and then the leakage current decreases. As the stress time increases, greater damages are caused and more traps are generated both at metal/dielectric interface and in the bulk of dielectric under a specified CVS, which enhances the SILC and allows more electrons to inject that delays the decrease of leakage current. At high applied voltage region, where the conduction is dominated by Poole-Frenkel emission, the leakage current gradually increases compared to the initial condition, and the onset of PE emission becomes earlier as the stress time increases. Since the greater damages are caused and more traps are generated under a specified CVS as the stress time increases, more trapped electrons could move into the conduction band by field-enhanced excitation, and therefore the leakage current of the La_2O_3 MIM capacitor converts early from the bulk-limited to the electrode-limited conduction behavior and leads to the increase in leakage current.

Figs. 4-19(a) and 4-19(b) illustrate the correlations among the relative leakage variation $\Delta J/J(t=0)$ at −1V, the stress time (t), and the injection charges (Q_{inj}) at various CVS voltages from −4.6 to −5 V. The $\Delta J/J(t=0)$ at −1V is an indicator for the quantity of traps generated by

the CVS. As the stress time increases, the amount of traps generated by CVS under a certain stress voltage increases, which confirms the argument before. Additionally, the $\Delta J/J(t=0)$ increases linearly with a logarithmic increase in Q_{inj}. The increase of $\Delta J/J(t=0)$ not only depends on the number of injection charges, but also depends on the magnitude of the stress voltage. More specifically, the higher stress voltage not only increases the amount of injection charges but also supplies the injection charges with higher energy, which induces more traps and performs greater impacts on SILC. Fig 4-20 illustrates trap generation probability per injected charge (P_{gen}) under the CVS of −4.6 V, −4.8 V, and −5 V as a function of stress time, which is extracted from results of SILC measurement at the applied voltage of -1V. It could be found that the trap generation probability for an injection charge decreases with the increasing of stress time.

In considering the long-term stress behaviors of leakage current, Fig. 4-21(a) depicts the time dependence of relative variation in the leakage current at −1 V under −4.6 V and −4.8 V of CVS, and Fig. 4-21(b) reveals the relative change in the leakage current at −1 V as a function of injection charge (Q_{inj}). At the initial stage, the leakage current at −1 V increases rapidly following the increase of stress time, and the relative change in leakage current linearly increases with a logarithmic increase in Q_{inj}. This is ascribed to the new traps generation and trap-assisted electron tunneling discussed in the previous paragraph. After a period of stress time, the relative variation in leakage tends to saturate and then it gradually decreases as the Q_{inj} increases. This reverse changes in leakage current during long-term stressing are attributed to the hole-trap creation. Once the tunneling electrons reach the bottom electrode and have sufficient high energy, holes are generated and tunnel into the dielectric and then trapped by the neutral traps to cause severe damages on the dielectric. Subsequently, the traps occupied with holes become positively charged and could capture the electrons that reduce the current [109].

4.4-2 The Variation in Capacitance

Figs. 4-22(a) and 4-22(b) illustrate the correlations among the relative capacitance variation $\Delta C/C(t=0)$, the stress time (t), and the injection charges (Q_{inj}) at various CVS voltages from −4.6 to −5 V. As shown in the Fig. 4-22(b), the relative-capacitance variation increases with a logarithmic increase in Q_{inj} regardless of the stress biases, which implies charge trapping in dielectric films [127]. When the carriers inject into the La_2O_3 dielectric film during CVS stress, the trapped charges could generate dipoles to increase the local permittivity and then contribute to the degradation of the capacitance [101], [102]. Besides, as shown in Fig. 4-22(a), after the [$\Delta C/C(t=0)$] rapidly increases in the initial stress, it tends to saturate after the 1000-s stressing. This saturation could be attributed to the trapped charges near the top electrodes. After the trap states at metal/insulator interface are rapidly filled by injection charges to increase the capacitance, the trapped charges would lift the barrier height near the injection electrode and result in a saturation phenomenon [28].

In considering the long-term stress behaviors of capacitance, Fig. 4-23(a) expresses the time dependence of relative capacitance variation at various CVS voltages from −4.2 to −4.6 V. The 10-year degradations of 10-nm La_2O_3 MIM capacitors with an 11.4-fF/μm^2 capacitance are 6.32 %, 4.09 %, and 2.61 % under −4.6 V, −4.4 V, and −4.2 V, respectively. No reversal phenomenon of changes in relative capacitance is observed, which differs from the relative variation in leakage current under long-term stress described earlier. Fig. 4-23(b) depicts the 10-year stability extraction of a fabricated 10-nm La_2O_3 MIM capacitor estimated by the relative-capacitance variation. It could be obtained from the extrapolated [$\Delta C/C(t=0)$] versus stress time to 10 years, as shown in Fig. 4-23(a). The safety 10-year operation voltage with below 1-% degradation could be extrapolated by around −4 V. This long-term stability is useful for the sub-65 nm technology node, whose operating voltage is smaller than 1.5 V.

4.4-3 The Variation in α and in TCC

Time dependence of α(t) normalized to its initial value α(t=0) under CVS biases from −4.6 V to −5 V is plotted in Fig. 4-24(a). The 4-24(b) presents the dependence of α(t)/α(t=0) on the relative variation in dielectric loss ΔD/D(t=0) during stressing, where D(t=0) is the fresh dielectric loss at zero bias. It can be found that α(t)/α(t=0) decreases with the increasing stress time for a certain stress bias. The reason for the decrease in the voltage dependence of capacitance is that the carrier mobility is reduced by the stress-induced trap states, and then hardly follows the alternating signal with a higher relaxation time [7]. Furthermore, higher stress voltage causes greater damages and more traps, and hence brings about the larger changes in α compared to that of lower stress voltage condition. Besides, α(t)/α(t=0) linearly decreases with a logarithmic increase in relative dielectric loss, but it still maintains almost the same slope under various stress voltages. It further verifies the change in voltage dispersion of capacitance is ascribed to the stress induced traps. Dependence of α(t)/α(t=0) on stress time under CVS of −4.8V with various measurement frequencies is exhibited in Fig. 4-25(a), and Fig. 4-25(b) presents the dependence of α(t)/α(t=0) on the relative variation in dielectric loss ΔD/D(t=0). As the measurement frequency increases, the changes in α(t)/α(t=0) become smaller, and the correlation between α(t)/α(t=0) and the relative variation in D has been confirmed again.

Fig. 4-26(a) draws the time dependence of TCC(t) normalized to its initial value TCC(t=0) under CVS biases from −3.8 V to −4.2 V, and The 4-26(b) presents the dependence of TCC(t)/TCC(t=0) on the relative variation in dielectric loss ΔD/D(t=0) during stressing. It can be found that TCC(t)/TCC(t=0) increases with the increasing stress time for a certain stress bias, which is contrary to the trend of α(t)/α(t=0) during stressing. The reason for the increase in the temperature dependence of capacitance is that the increase in quantity of stress-induced trap states of the dielectric. The number of trap induced dipoles rises under CVS, and the dipoles become more capable to follow alternating signal at higher temperature that leads to a shorter dipolar relaxation time, and consequently results in the increase in TCC.

In further, higher stress voltage causes greater damages and more traps, and hence brings about the larger changes in TCC compared to that of lower stress voltage condition. Besides, as shown in 4-26(b), TCC(t)/TCC(t=0) increases with the increase in relative dielectric loss, and it is also contradictory to the relation between α and D under CVS. The distinct evolution between α and TCC under CVS manifests the main reasons that induce α and TCC are different, which agrees well with the viewpoints declared in the previous section, and that is, the space charge relaxation dominates the voltage dependence of capacitance while the dipolar relaxation is principally responsible for the temperature dependence of capacitance.

4.4-4 Summary

The stabilities of MIM capacitors with La_2O_3 dielectrics under CVS are investigated in this section. The wear-out mechanisms of the high-k MIM capacitors are trap generation and charge trapping, which could be identified by detecting the SILC and the relative capacitance variation during stressing, respectively. The correlation among the ΔJ/J(t=0), the ΔC/C(t=0), and the Q_{inj} under CVS is evaluated. The changes in ΔJ/J(t=0) not only depend on the Q_{inj} but also depend on the stress voltage, whereas the variation in ΔC/C(t=0) strongly depends on the Q_{inj}. Both of the decrease in α and the increase in TCC of La_2O_3 MIM capacitors during CVS testing could be attributed to the stress induced traps in dielectrics. Additionally, high stability of 10-year lifetime is achieved for a 10-nm La_2O_3 MIM capacitor with an 11.4-fF/μm^2 capacitance density.

4.5 BREAKDOWN AND RELIABILITY CHARACTERISTICS OF La_2O_3 MIM CAPACITORS

Dielectric integrity and reliability are requirements for the development and manufacture of VLSI semiconductor devices. Reliability is the probability of a product that will not suffer

breakdown under specified operating conditions for the defined lifetime. The time-zero dielectric breakdown (TZDB) and the time-dependent dielectric breakdown (TDDB) are the most important issues of MIM capacitors in reliability because they could verify the dielectric integrity and device lifetime. However, these two characteristics for La_2O_3 MIM capacitors are still an undeveloped field. Therefore, both cumulative TZDB and statistical TDDB characteristics of high-k MIM capacitors with e-beam evaporated La_2O_3 dielectrics are discussed in this section.

4.5-1 Characteristics of Time-Zero Dielectric Breakdown

Fig. 4-27 exhibits the cumulative results of TZDB for the 10-nm La_2O_3 MIM capacitors at the measurement temperature varied from 25 to 125°C in the case of top injection, the breakdown field (E_{BD}) of 50% failure probability declines from 7.35 to 5.66 MV/cm as the temperature rises from 25 to 125°C. Besides, from the Fig. 4-27, it can be noted that as the measurement temperature raises, the distribution of the E_{BD} data becomes narrower. This temperature dependence of TZDB is related to the damage created in the oxide during the measurement. When carrying out the measurement, a rapid increase in applied voltage results in a rapid rise in local current density of the dielectric to generate energetic carriers that could release the energy and distort or weaken the local molecular bonds of the dielectric film. The weakened molecular bonds become very susceptible to be broken by the further injection carriers, and then a localized defective (percolation) site forms. As a conductive percolation path develops shorting the two electrodes, the breakdown occurs [27]. For the high temperature measurement, more energetic injection carriers are available to create damage leading to lower breakdown voltage than that of low temperature measurement. The effective defect forming process at elevated temperature not only reduces the E_{BD} magnitude, but also causes the dielectrics of different MIM capacitors break down at almost the same applied

voltage.

4.5-2 Characteristics of Time-Dependent Dielectric Breakdown

As discussed before, the time-dependent degradation of the La_2O_3 high-k MIM capacitors are attributed to trap generation and charge trapping, which could be identified by detecting the SILC phenomenon and the relative capacitance variation under CVS testing, respectively. During stressing, the degradation events (SILC, trapping-detrapping processes) continue to take place randomly and accumulatively. Once the trap density of the dielectric reaches the critical defect density that can form a connection of these defects throughout the entire dielectric film, leading to a conductive or percolation path from the top electrode to the bottom electrode and huge amounts of leakage current through it that shortens the whole MIM capacitor and ultimately, the time-dependent breakdown occurs [76], [128].

Fig. 4-28(a) depicts the Weibull distribution of TDDB data with a −4.2 constant stress voltage at 75°C as a function of Ln(T_{BD}). From this diagram, it can be obtained that the corresponding shape factor β_C and scale factor α_C are 5.674 and 2317.4 sec, respectively. The scale factor, α_C, signifies the time to 63% breakdown percentage of all devices under specified TDDB testing. The shape factor, β_C, also named as Weibull slope, is an important parameter when evaluating gate oxide reliability and is useful in predicting lifetime distribution for various capacitor areas. Fig. 4-28(b) reveals the Weibull distribution as a function of T_{BD} under the CVS of −4.1 V, −4.15 V, and −4.2 V at 75°C, and the related α_C and β_C are also summarized in it. As can been seen from this plot, as the stress voltage increases, the failure time decreases and the distribution of T_{BD} data becomes narrowing. The rise in β_C with the increasing of stress voltage means the less area dependence of lifetime with higher stressing voltage according to the Eq. 3-13. In terms of the earlier discussion, the higher stress voltage applied on the MIM capacitor would introduce more energetic injection carriers that

could generate more traps in the dielectric, which accelerates the time to reach the critical defect density under CVS and results in the shorter time to breakdown, as indicated in Fig. 4-28(b). Subsequently, Fig. 4-29 realizes the 10-year lifetime projection of a fabricated 10-nm La_2O_3 MIM capacitor with 11.4-fF/μm^2 capacitance density to the normal operational voltage by extrapolating all the α_C data with respect to applied stress voltages. As estimated in Fig. 4-29, the safety 10-year operation voltage at 75°C with below 63% failure percentage could be extrapolated by around −2.85 V. This long-term reliability is useful for the sub-65 nm technology node, whose operating voltage is smaller than 1.5 V.

Besides, before the final breakdown happening, a drastic fluctuation phenomenon of J_{stress} stands for a long time without breakdown is discovered during stressing, as presented in Fig. 4-30(a), which appears to like the soft breakdown (SBD) in SiO_2 of the MOS structure [128]-[130]. However, it has been reported that the SBD of SiO_2 due to a weak percolation path between substrate and gate electrode only occurs in ultra thin oxide. Thus, the SBD mechanism of the MIM capacitor with the La_2O_3 dielectric as thick as 10 nm is unclear and essential to further study. In order to distinguish definitely, the previous final breakdown is named as hard breakdown (HBD). Fig. 4-30(b) illustrates the Weibull distribution of HBD and SBD as a function of T_{BD} under CVS of −4.1 V at 75°C, and the related α_C and β_C are also summarized in it. The β_C of SBD is different from that of HBD under the same stress voltage, which is dissimilar to the soft breakdown in ultra thin SiO_2. It has been reported that a two-step breakdown of high-k MOS capacitor is interpreted as breakdown of the interfacial layer first, followed by the breakdown of the high-k layer itself [30], [131]-[133]. Besides, since the deposition of La_2O_3 directly on metal surfaces leads to an unavoidable interfacial layer (IL) formation, we suggest that the SBD of La_2O_3 MIM capacitors may be attributed to the IL breakdown. During electrical stressing, the generation of new traps and electron trapping-detrapping processes both takes place in the bulk of La_2O_3 dielectric layer and in the IL at insulator/metal interface. However, the IL has more pre-existing traps than the bulk

high-k layer, which needs a shorter time to reach the critical defect density and results in a shorter time to breakdown. Once the breakdown of IL or the SBD occurs during stressing, the breakdown paths formed in the IL by the connection of percolation sites. Hence, all of the stress voltage applies on the bulk high-k layer, and a severe trapping-detrapping process causes the drastic fluctuation in J_{stress}. Then, until the bulk layer also reaches the critical defect density, the entire layer breaks down and the HBD of the high-k MIM capacitor happens.

4.5-4 Summary

In this section, we demonstrate the TZDB and TDDB of the 10-nm La_2O_3 MIM capacitor with the 11.4-fF/μm^2 capacitance density. So far as the TZDB is concerned, the E_{BD} decreases and the distribution of E_{BD} data becomes narrowing as the measurement temperature increases, which attributed to the amount of injection energetic carriers and the efficiency of defects created. As to the TDDB, a two step breakdown is observed because of the bi-layer nature of La_2O_3 high-k system, the IL breaks down first and the SBD occurs, followed by the breakdown of the bulk high-k layer and the HBD takes place. Higher stress voltage accelerates the breakdown event due to the higher degradation rate. Moreover, highly reliable of 10-year lifetime is achieved for the fabricated high-k La_2O_3 MIM capacitors.

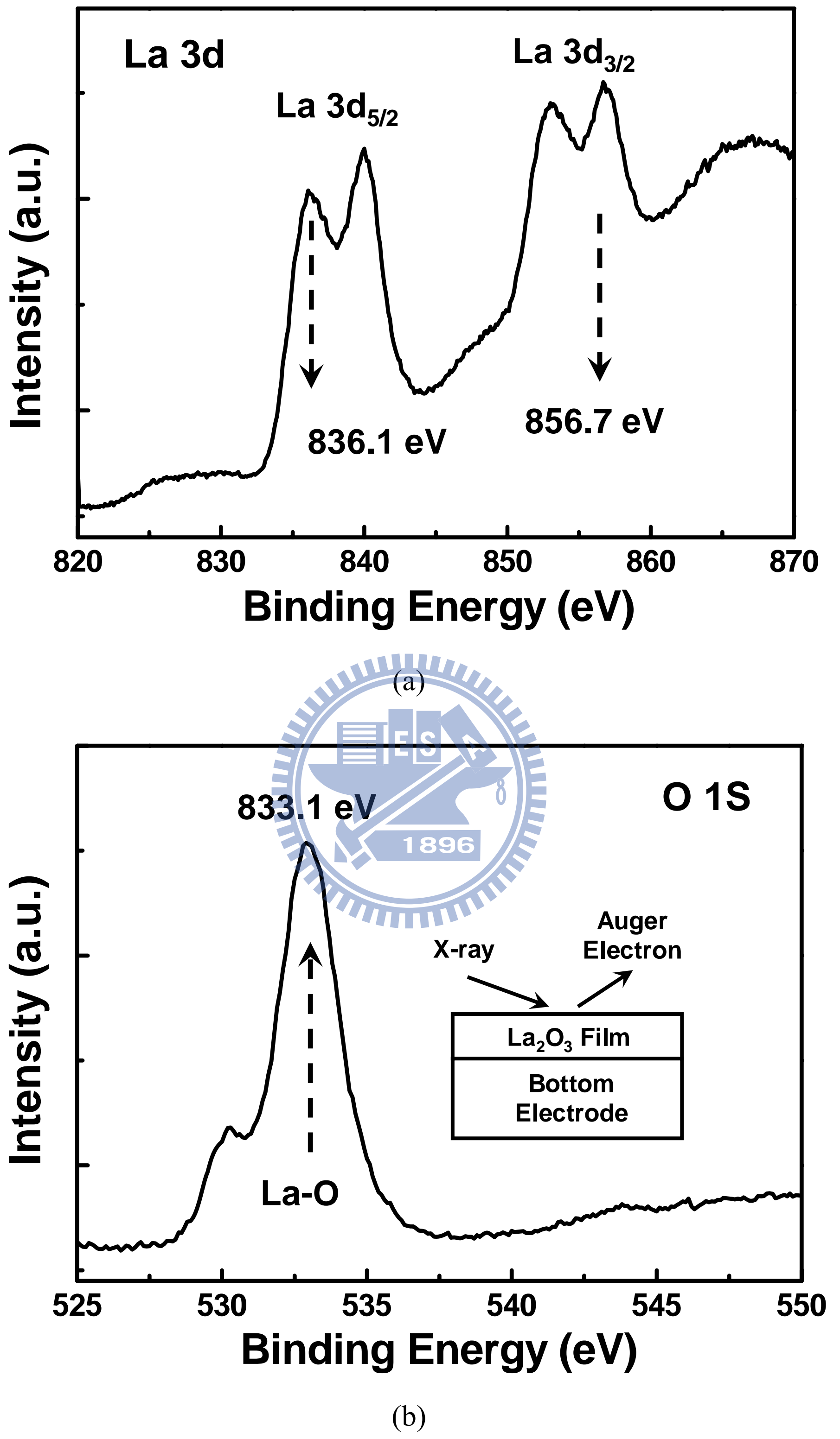


Fig. 4-1. The XPS spectra of the deposited La_2O_3 film. (a) The La 3d core level spectra, and (b) the O 1s core level spectra for the La_2O_3 film on bottom electrode.

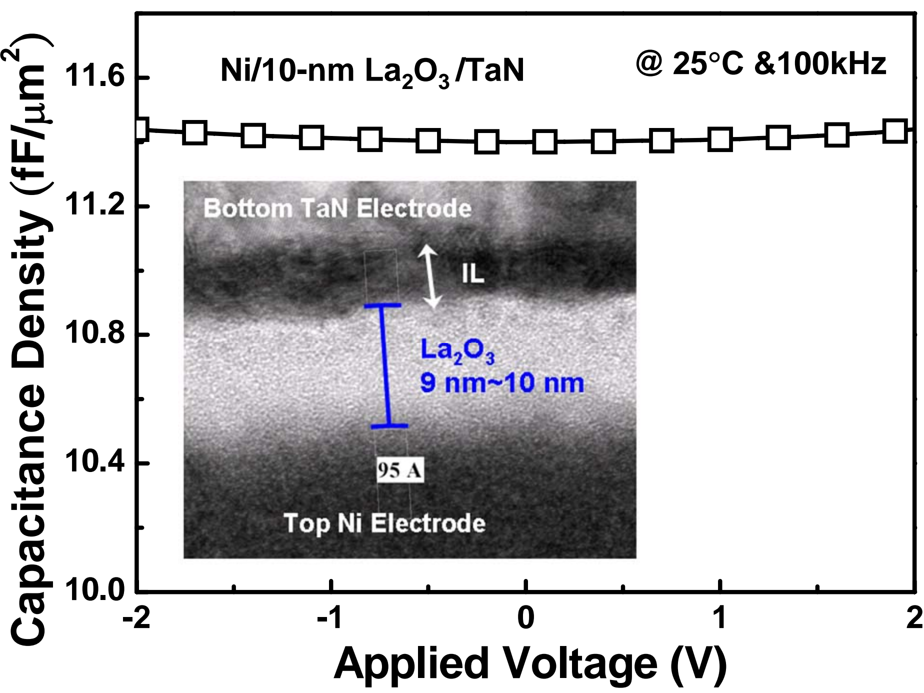


Fig. 4-2. The C-V characteristic of the La_2O_3 MIM capacitor at 100 kHz and at 25ºC. The inset is the cross-sectional TEM image of the proposed La_2O_3 MIM capacitor.

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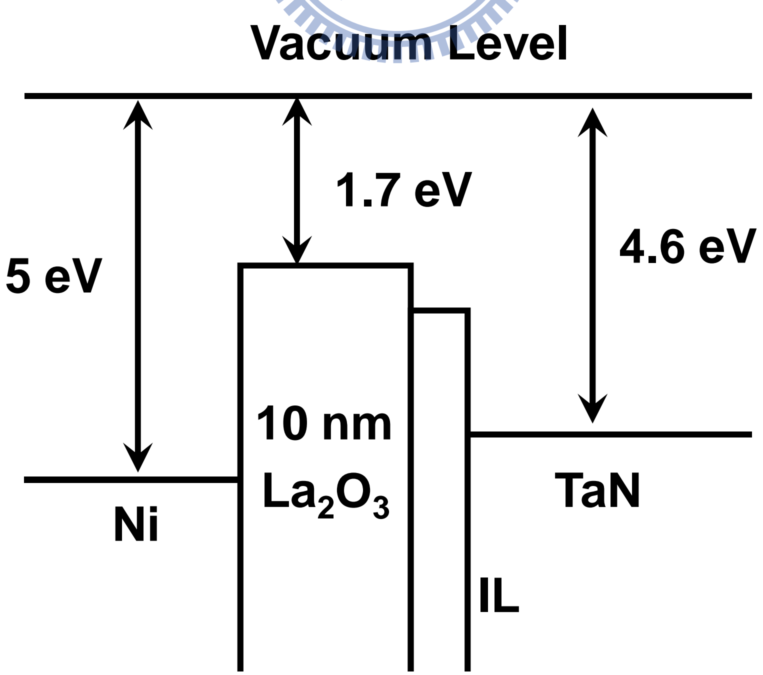


Fig. 4-3. The energy band diagram of the $Ni/La_2O_3/TaN$ MIM capacitor.

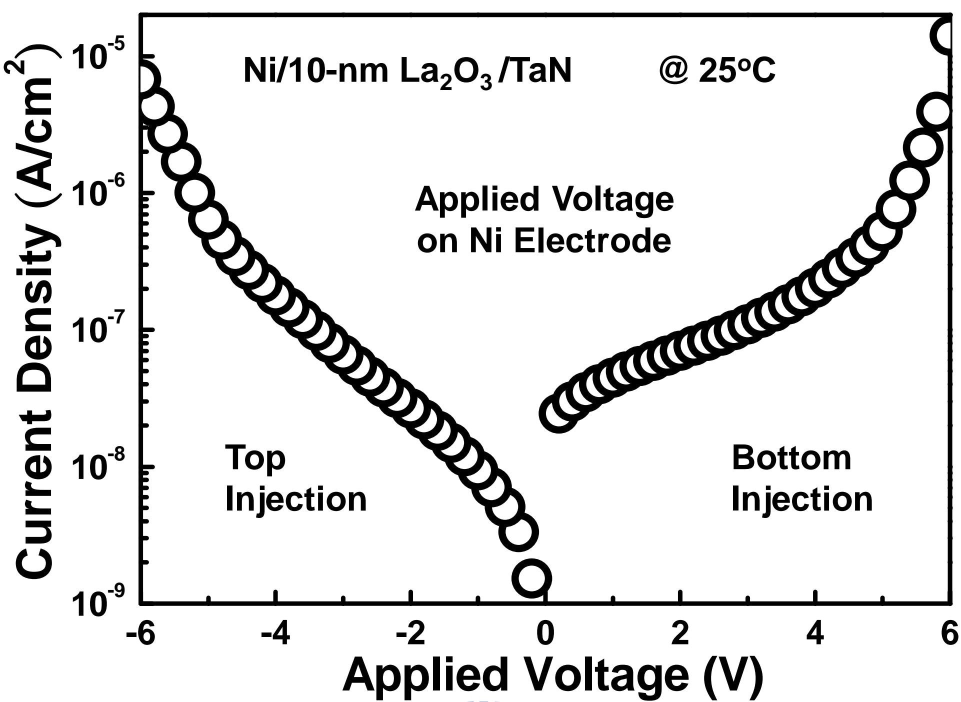


Fig. 4-4. The J-V curve of the 10-nm La_2O_3 MIM capacitor measured at 25 °C.

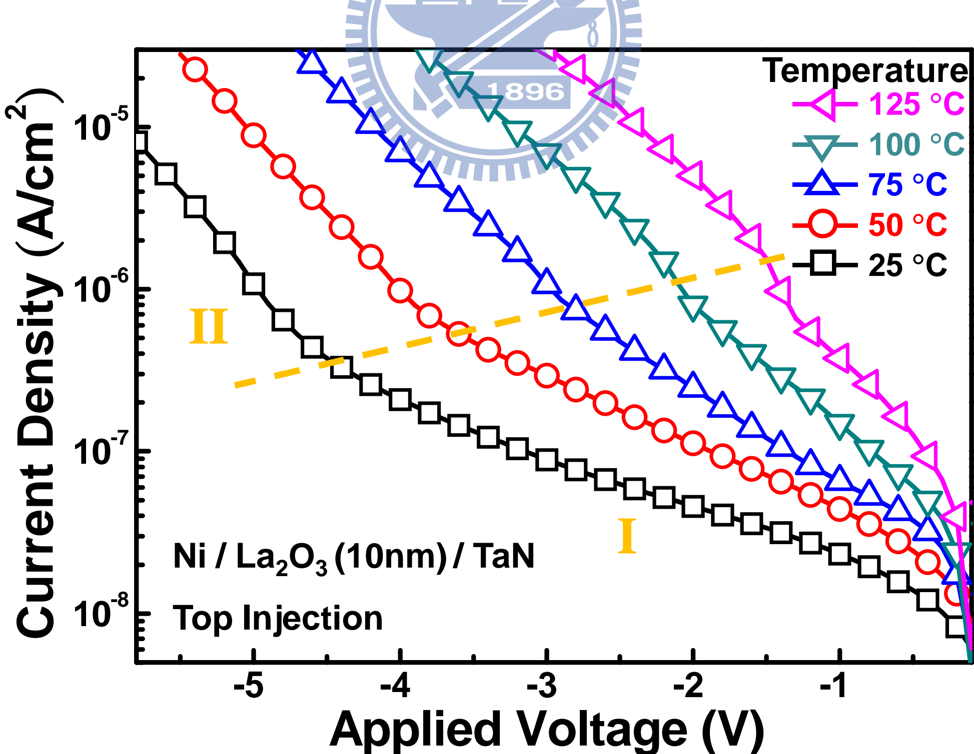


Fig. 4-5. J-V curves of the La_2O_3 MIM capacitor in the case of top injection at measurement temperatures in the range from 25 °C to 125 °C.

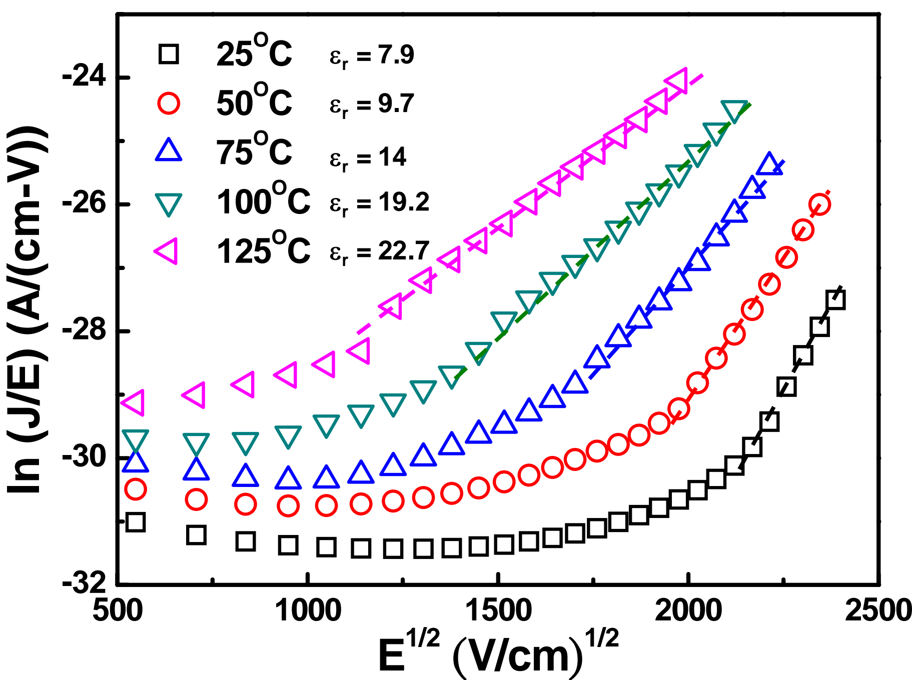
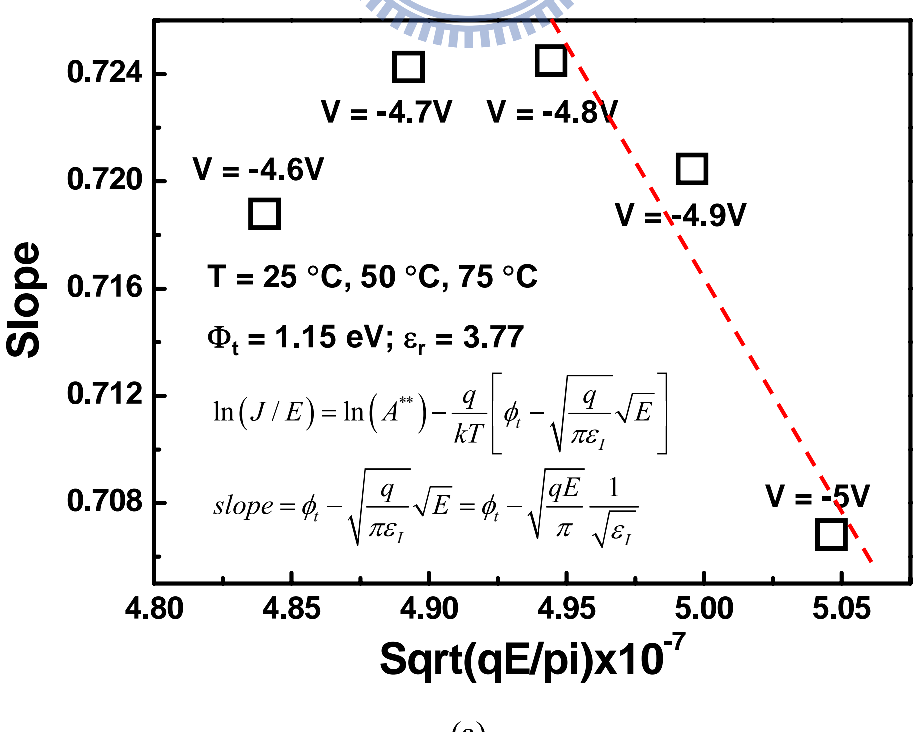
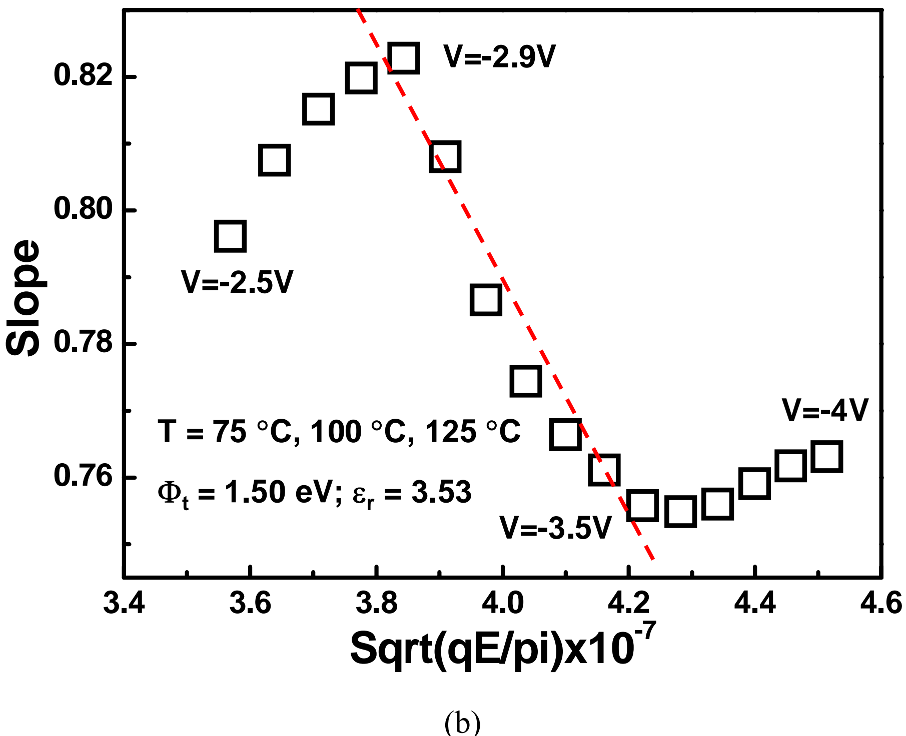


Fig. 4-6. The plot of ln(J/E) versus $E^{1/2}$ in the high field region according the Poole-Frenkel emission and the deduced static dielectric constant at various temperatures are also presented.



(a)



(b)

Fig. 4-7. The plot of the slope versus $(qE/\pi)^{1/2}$ by various applied voltages fitting (a) from 25 °C to 75 °C, and (b) from 75 °C to 125 °C.

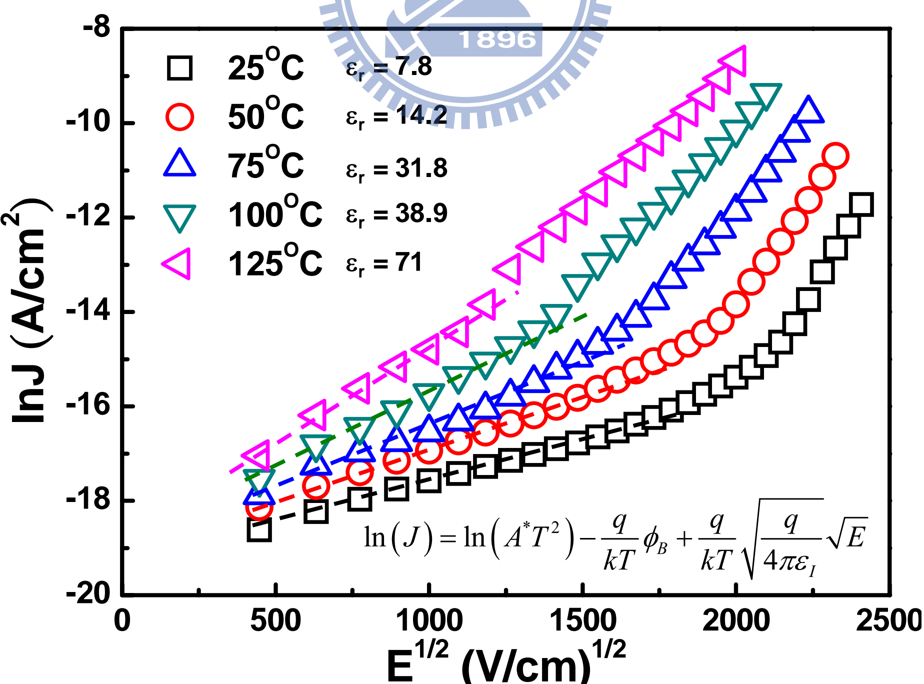


Fig. 4-8. Typical plot of lnJ versus $E^{1/2}$ in the low field region according the Schottky emission and the deduced static dielectric constant at various temperatures are also presented.

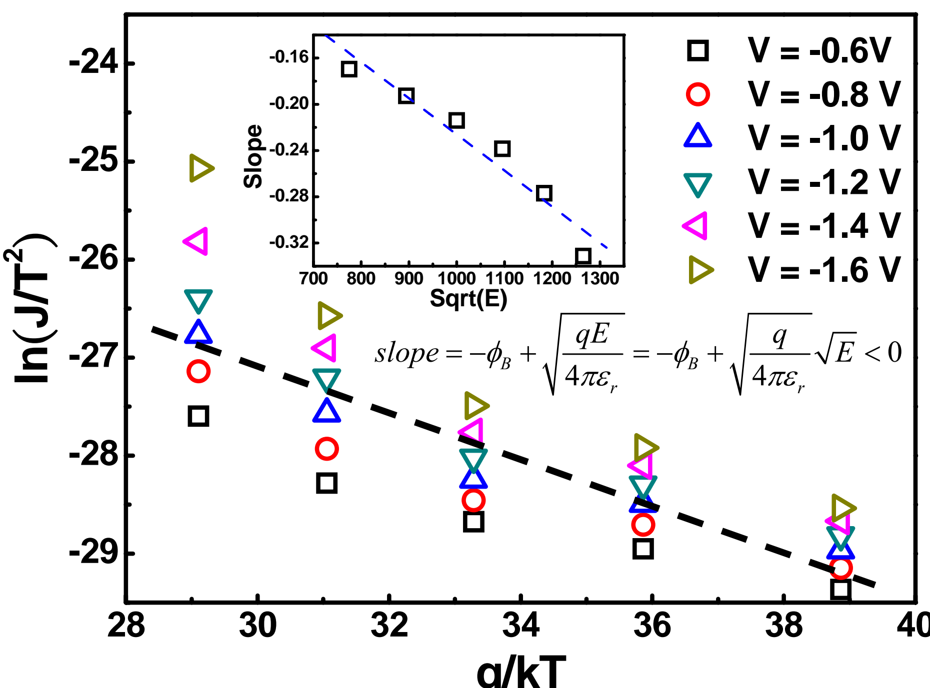


Fig. 4-9. The plot of $\ln(J/T^2)$ versus q/kT in the applied voltage from −0.6 V to −1.6V. The inset is the plot of the extracted slope versus $E^{1/2}$ to obtain the extracted ε_r value.

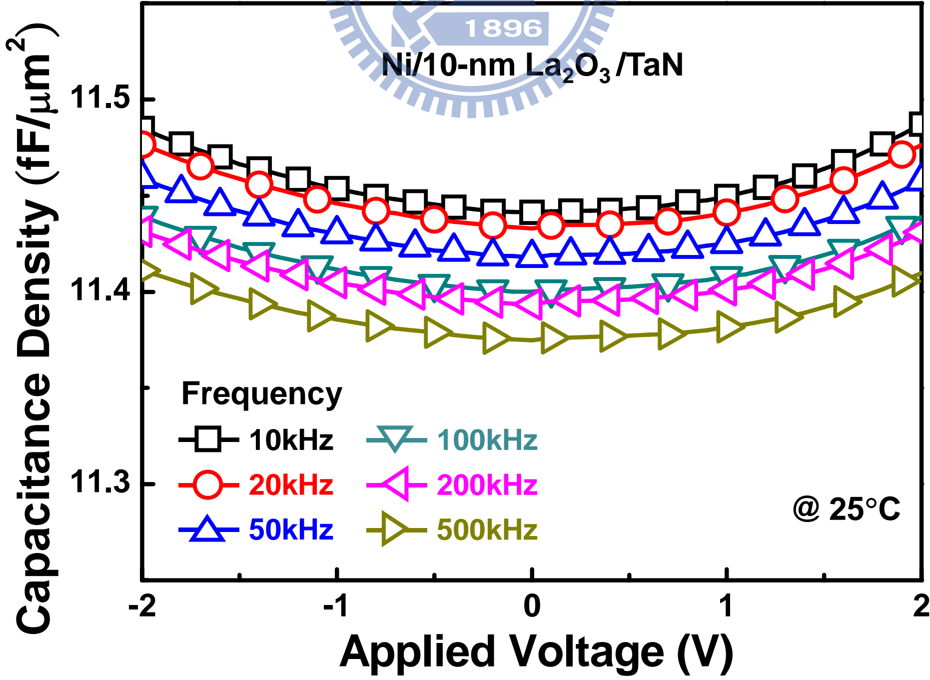


Fig. 4-10. C-V curves of the 10-nm La_2O_3 MIM capacitor measured under the frequencies varied from 10 kHz to 500 kHz and at the temperature of 25 °C.

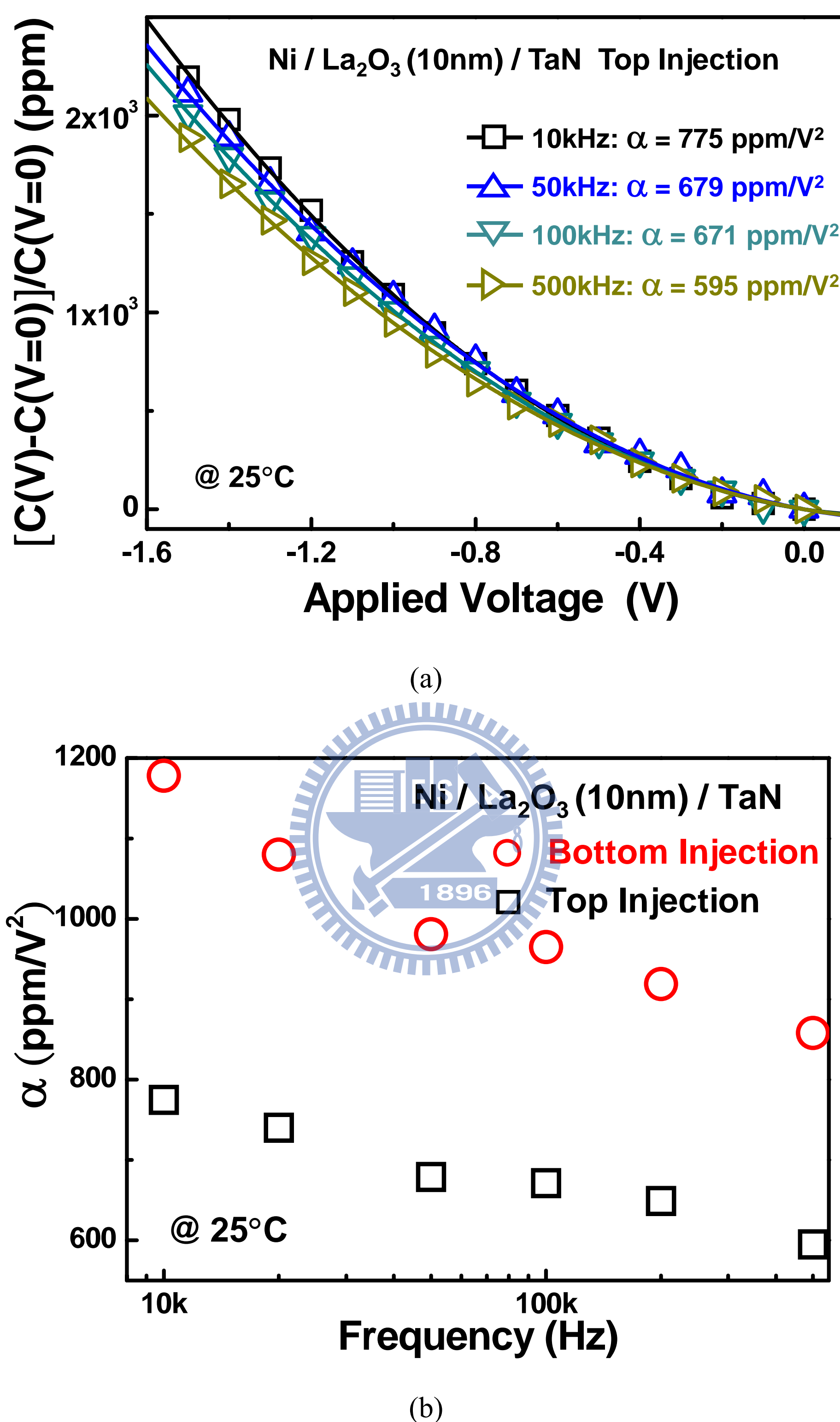


Fig. 4-11. (a) The VCC fitting curves and the extracted α values at the frequency ranges from 10 kHz to 500 kHz at 25 °C in the case of top injection, and (b) the comparison in α between top and bottom injection condition at 25 °C.

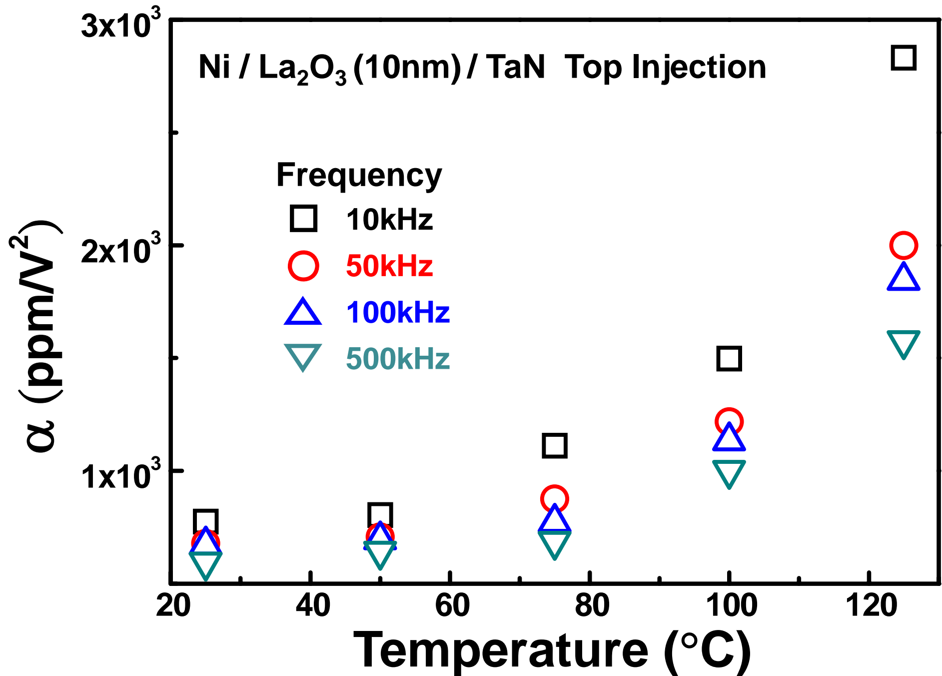


Fig. 4-12. The extracted α values under various frequencies and different temperature conditions of the La_2O_3 MIM capacitors in the case of top injection.

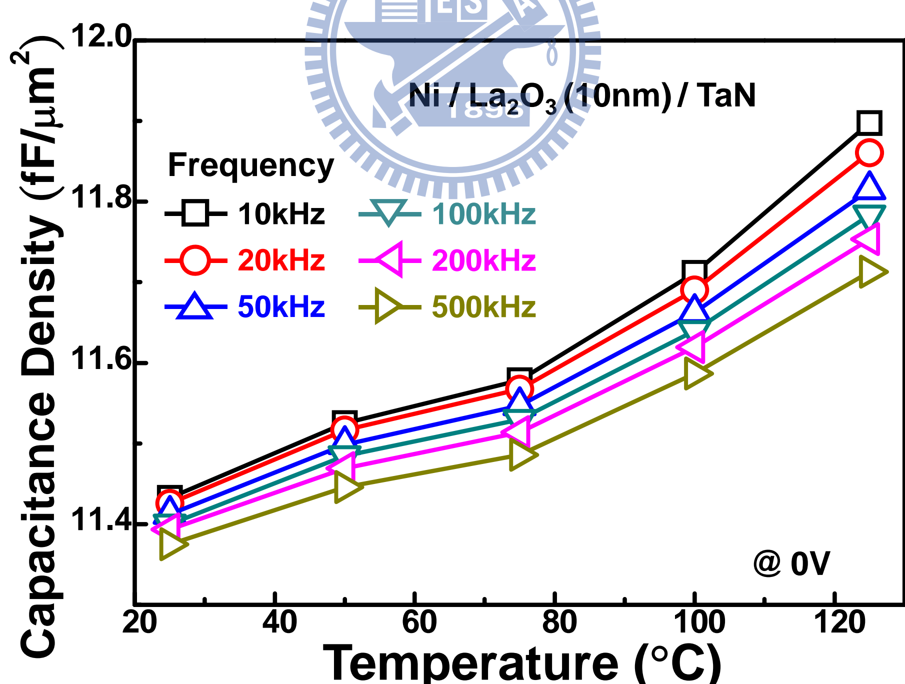


Fig. 4-13. The capacitance-temperature relationships at frequencies range from 10 kHz to 500 kHz for 10-nm La_2O_3 MIM capacitors.

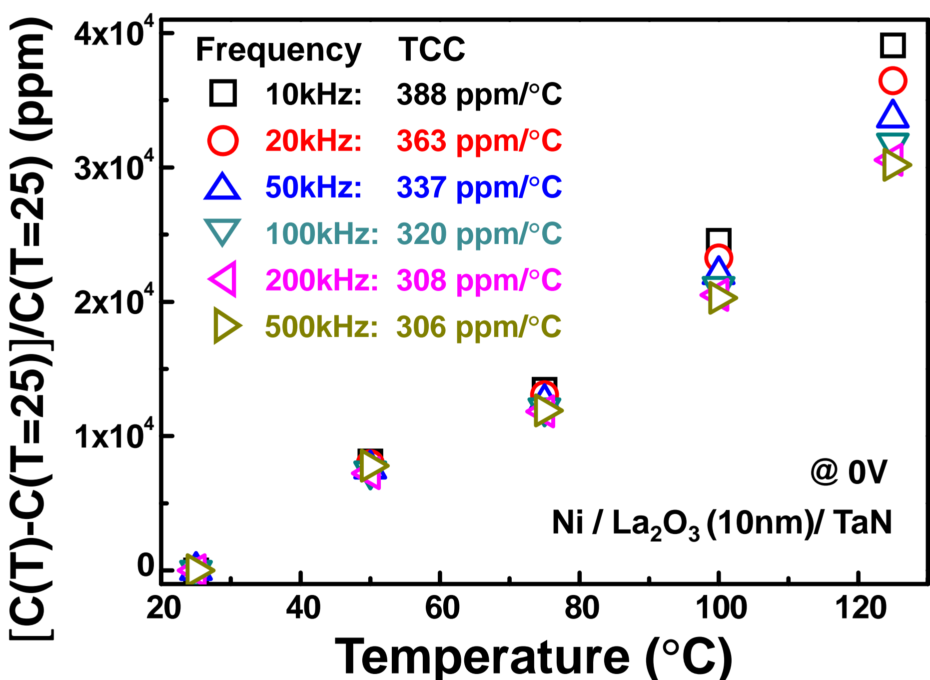


Fig. 4-14. The normalized capacitance as a function of temperature and the corresponding extracted TCC parameters at frequencies varied from 10 kHz to 500 kHz.

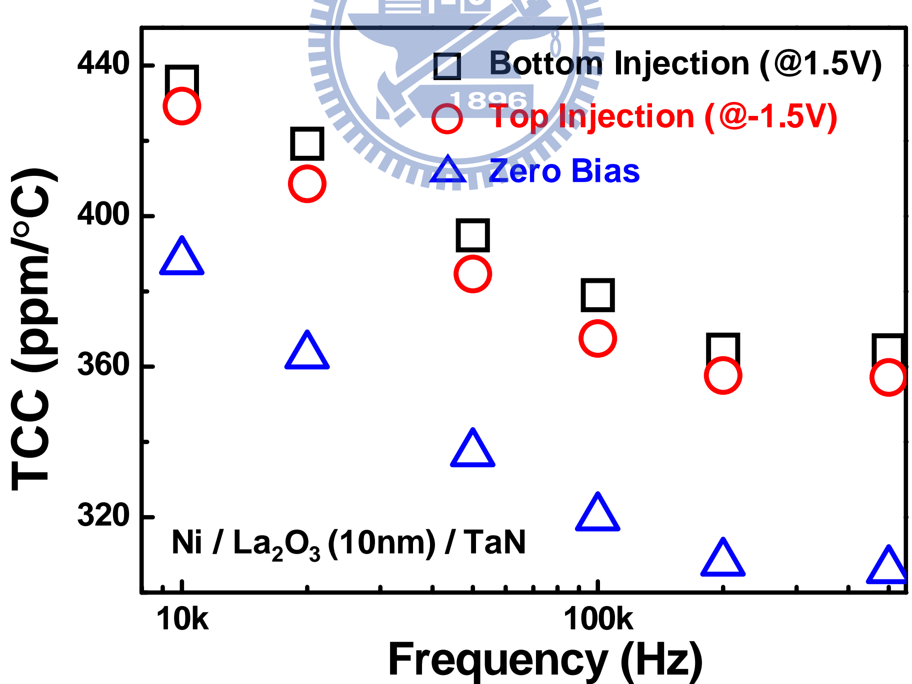


Fig. 4-15. The TCC values measured under zero bias, −1.5 V, and 1.5 V at frequencies varied from 10 kHz to 500 kHz.

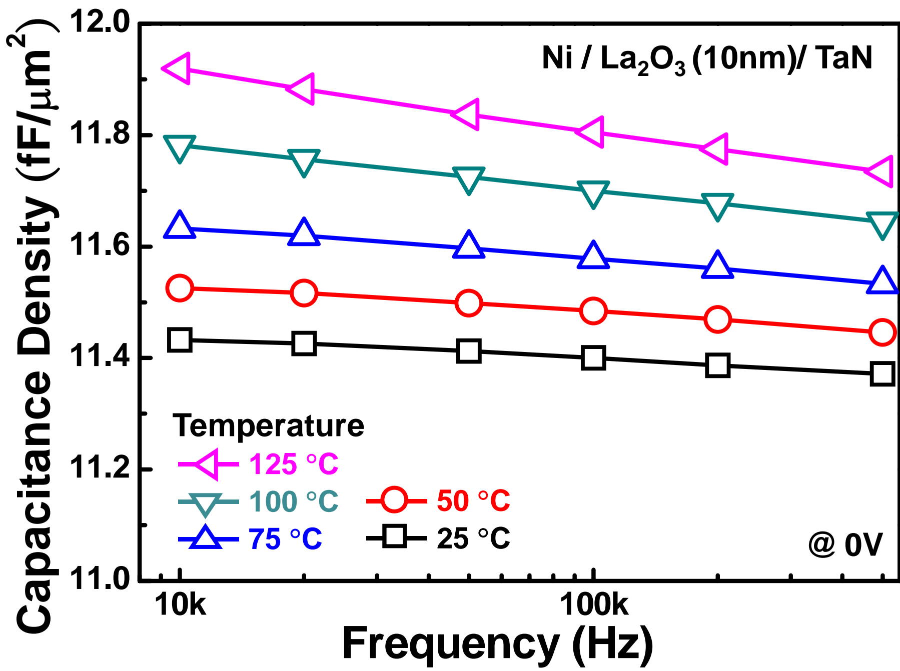


Fig. 4-16. The relationship between capacitance and operational frequency at the temperature in the range from 25 °C to 125 °C.

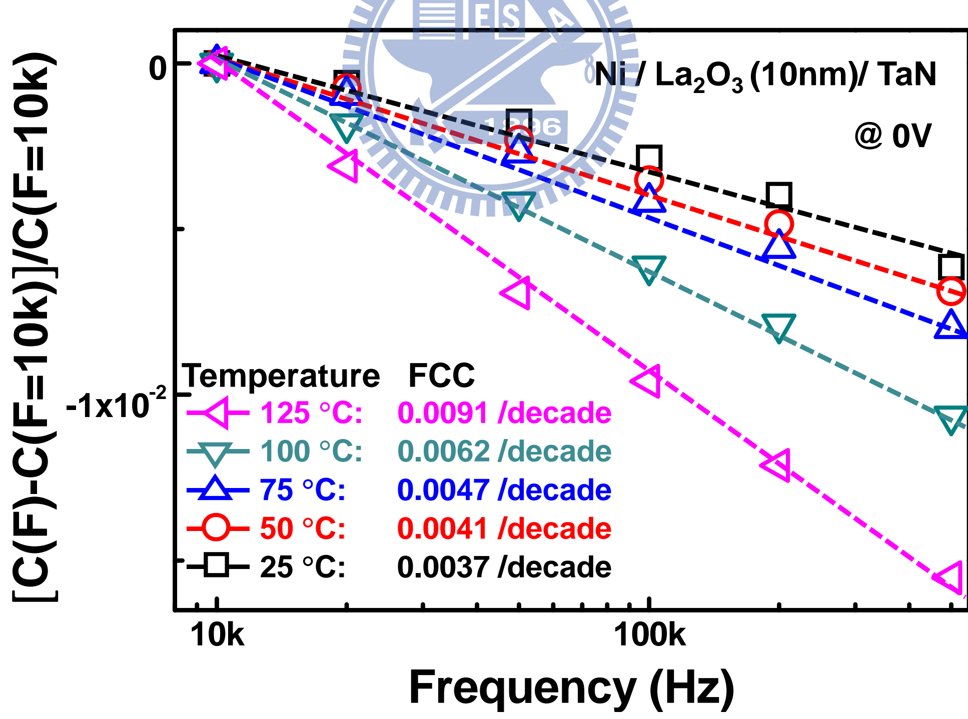


Fig. 4-17. The normalized capacitance as a function of frequency and the corresponding extracted FCC parameters at the temperature in the range from 25 °C to 125 °C.

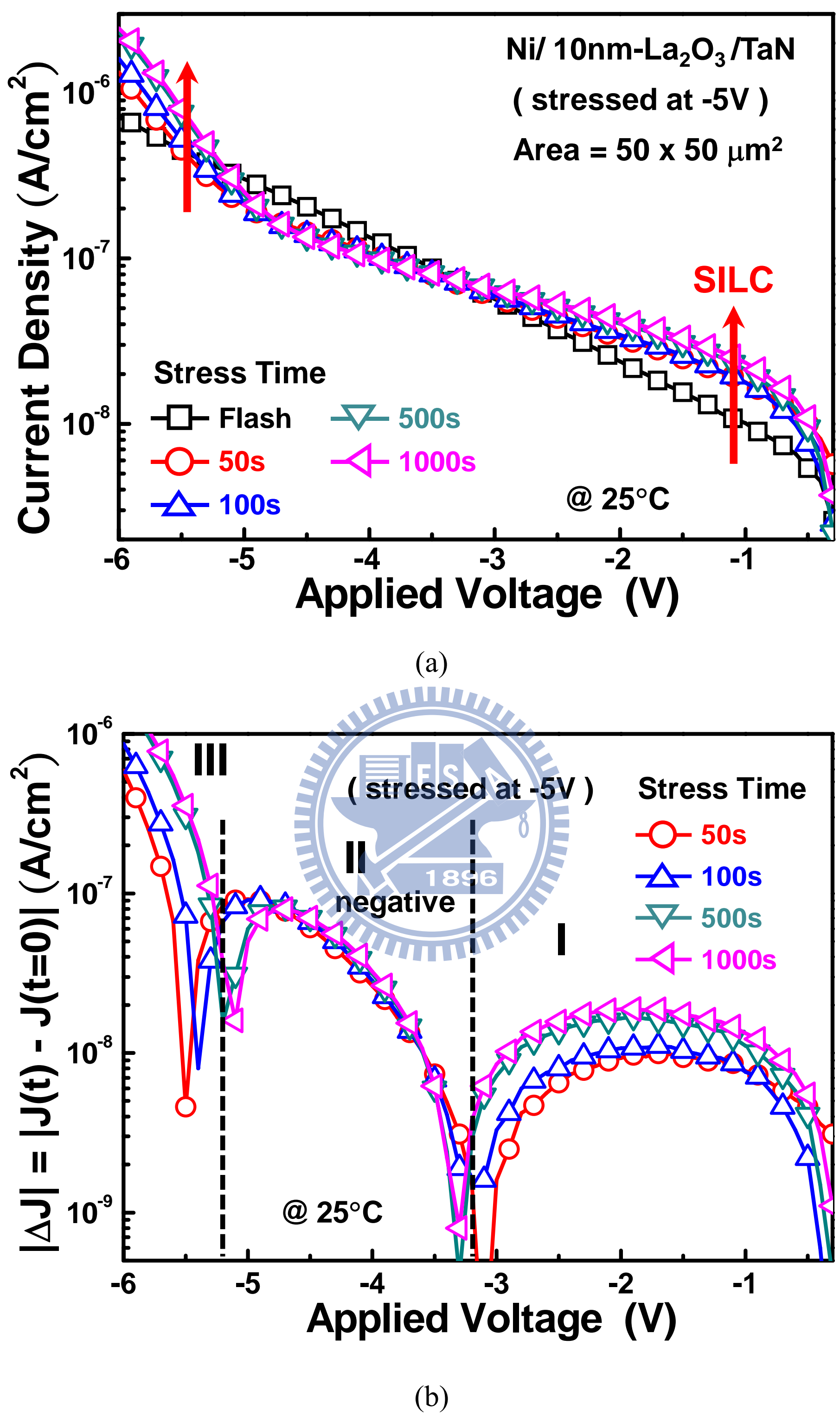
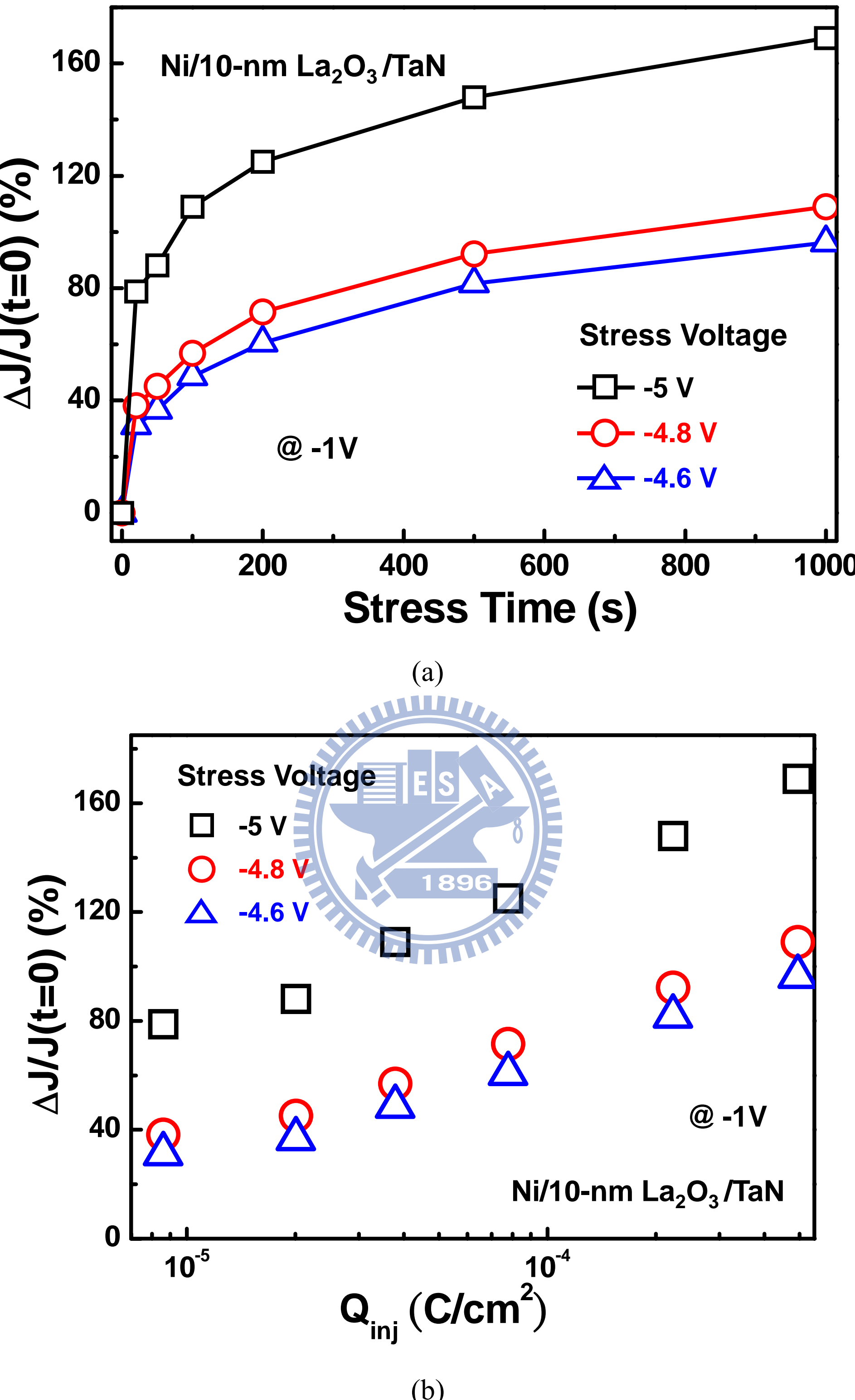


Fig. 4-18. (a) The evolution of J-V curves of the La_2O_3 MIM capacitor stressed at −5 V in the case of top injection, and (b) illustrates the absolute magnitude of [J(t)-J(t=0)] as a function of applied voltage with different stress time obtained from (a).



(a)

(b)

Fig. 4-19. The relative leakage variation ΔJ/J(t=0) measured at the applied voltage of −1 V as a function of (a) stress time, and (b) injection charges (Q_{ing}) under t under the stress voltage of −4.6 V, −4.8 V, and −5 V.

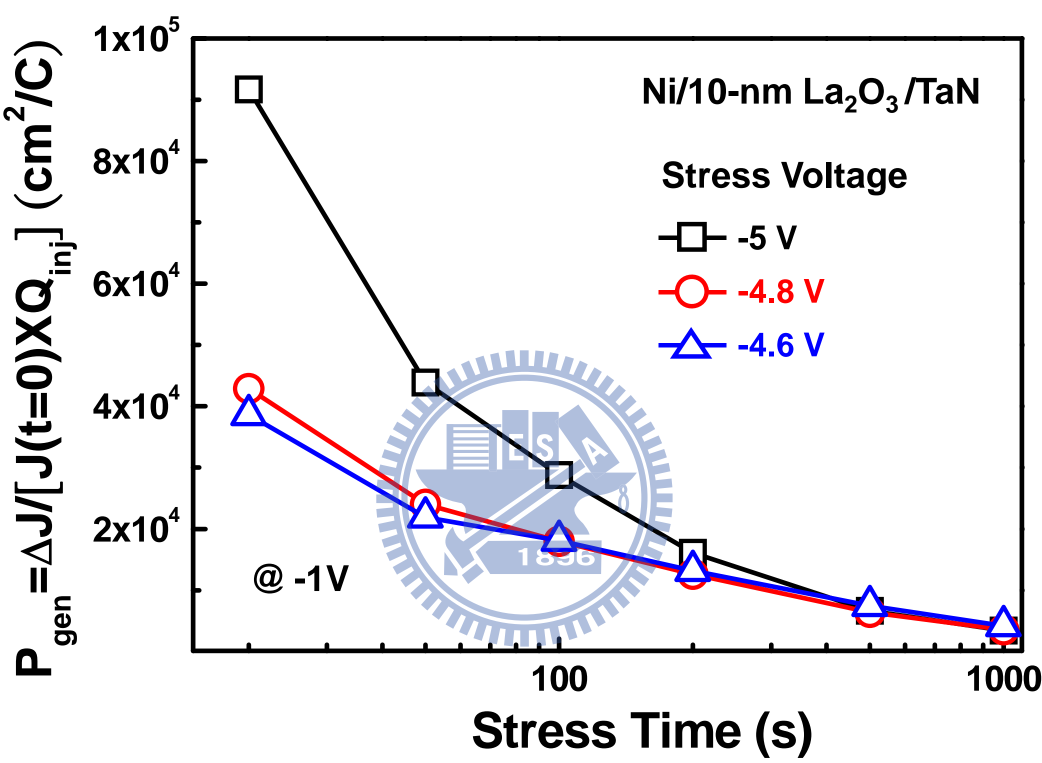
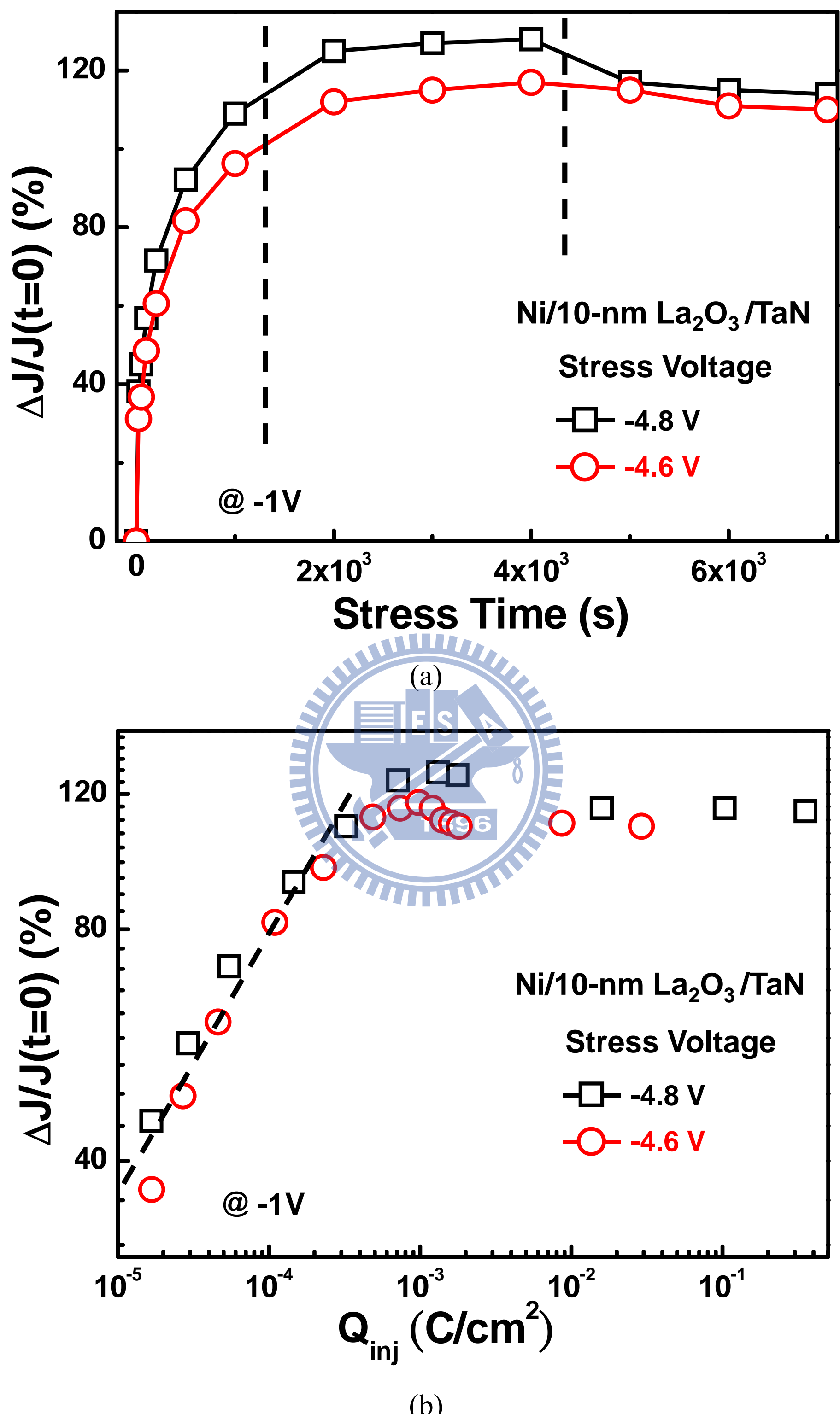


Fig. 4-20. The trap generation probability per injected charge (P_{gen}) under the stress voltage of –4.6 V, –4.8 V, and –5 V as a function of stress time.



(a)

(b)

Fig. 4-21. The long-term evolution of ΔJ/J(t=0) at −1V with the increase in (a) stress time, and (b) injection charges (Q_{inj}) under the stress voltage of −4.6 V, −4.8 V, and −5 V.

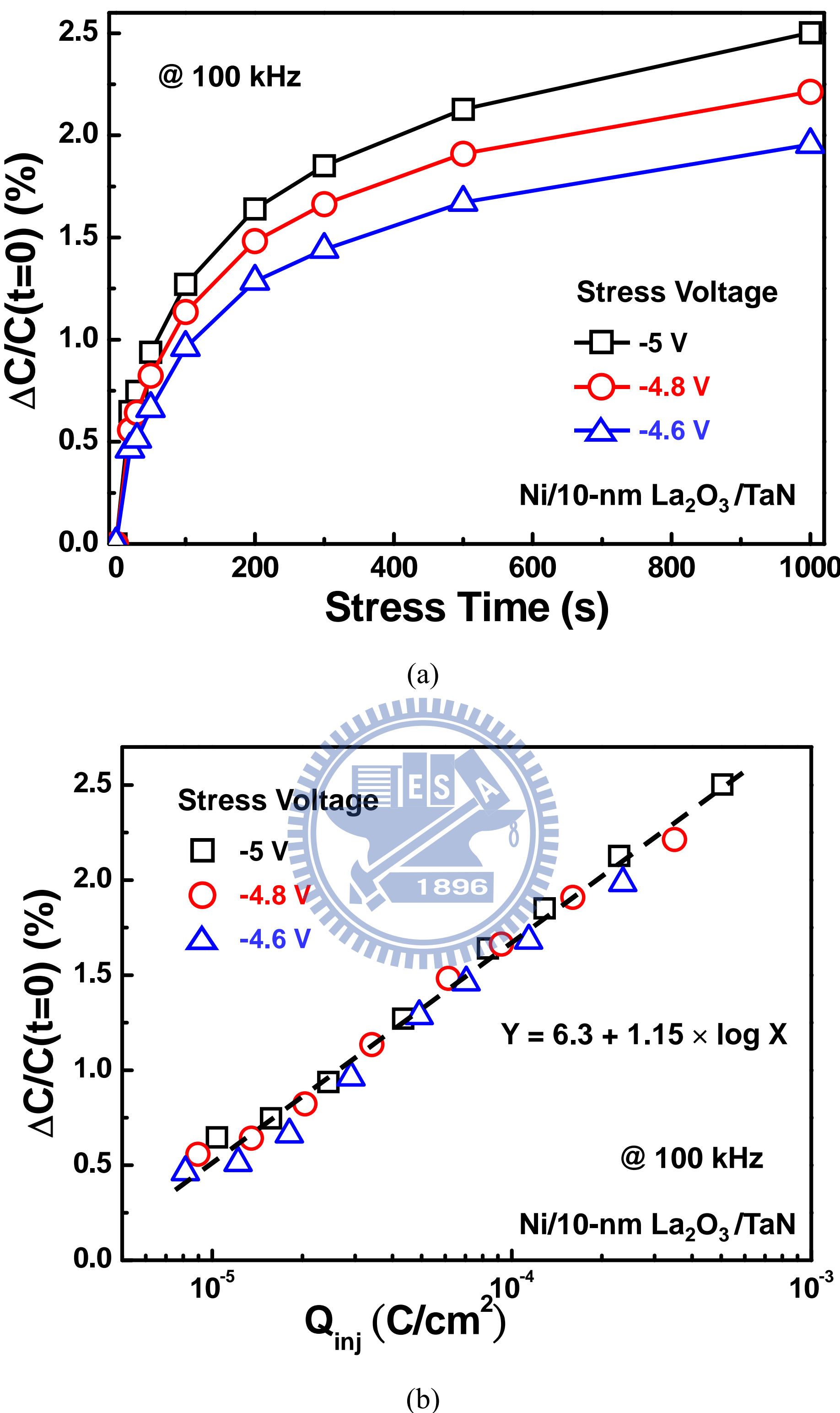


Fig. 4-22. Relative-capacitance variation [C(t)-C(t=0)]/C(t=0) at 100 kHz as a function of (a) stress time, and (b) injection charges (Q_{inj}) at various CVS voltages from −4.6 V to −5 V.

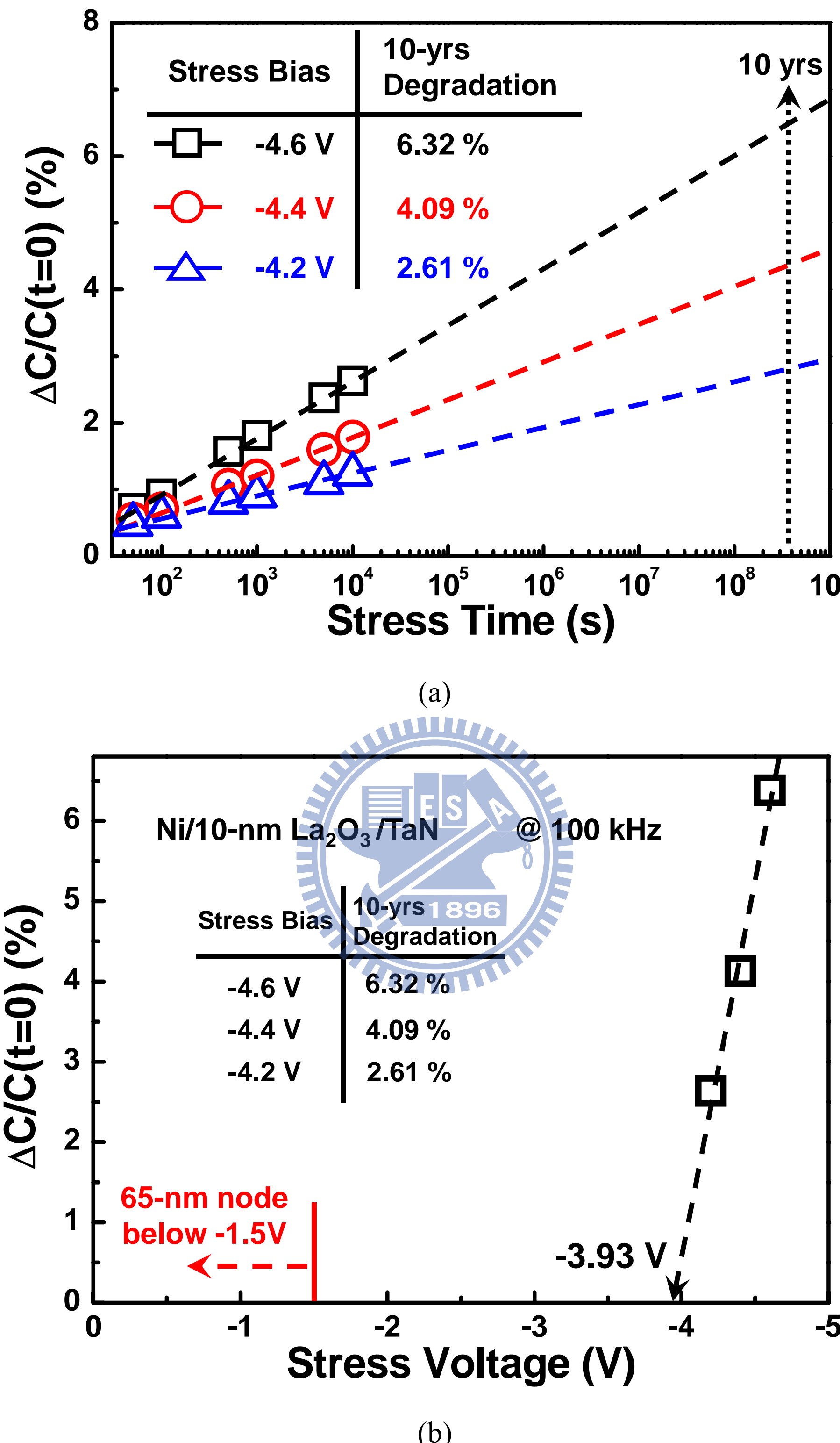


Fig. 4-23. (a) The time dependence of relative capacitance variation at various CVS voltages from –4.2 to –4.6 V and the 10-year degradations. (b) The 10-year stability extraction of 10-nm La_2O_3 MIM capacitors estimated by the relative-capacitance variation indicated in (a).

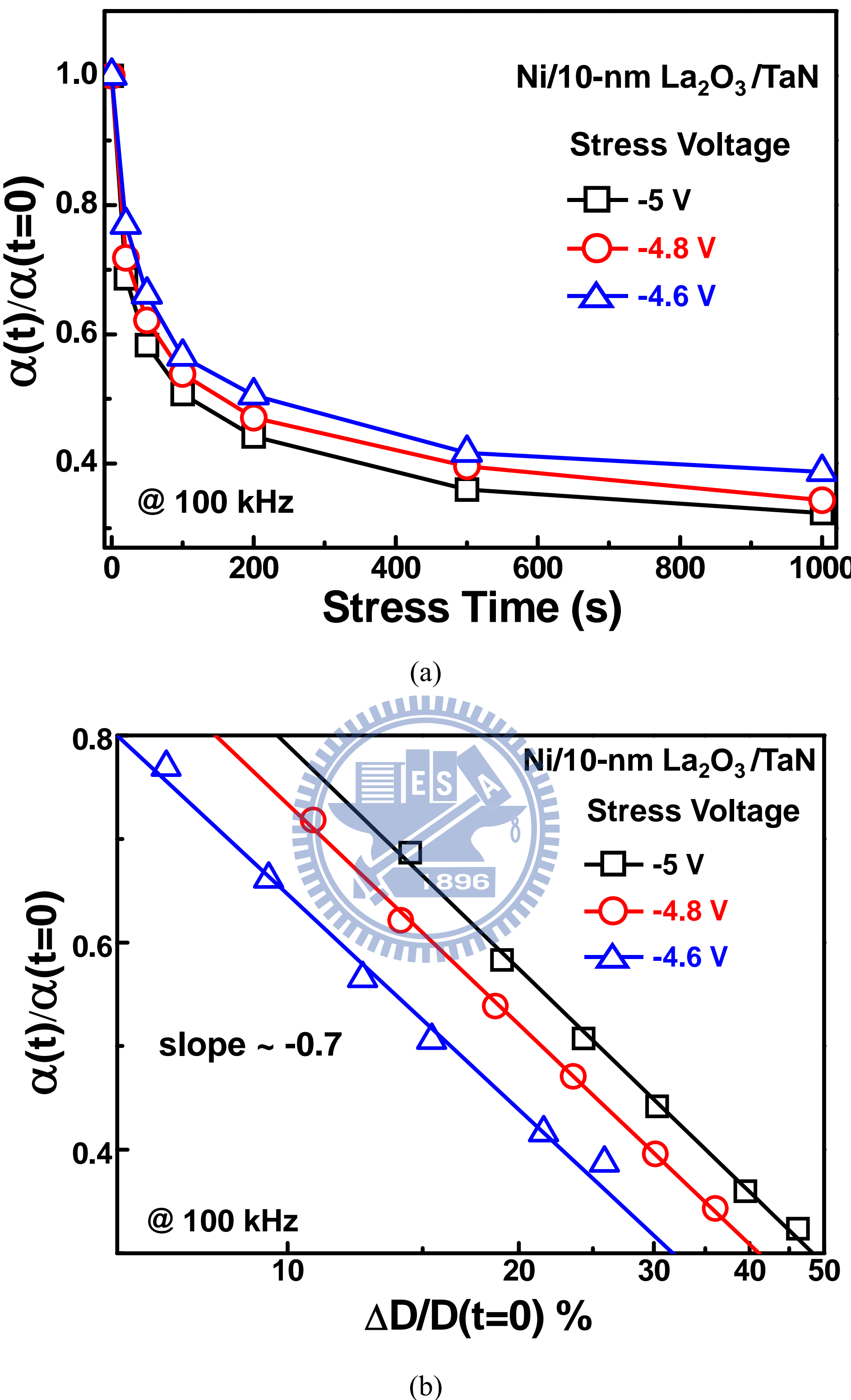


Fig. 4-24. The relative quadratic voltage coefficient of capacitance α(t)/α(t=0) under CVS from −4.6 V to −5 V as a function of (a) stress time, and (b) relative variation in dielectric loss D.

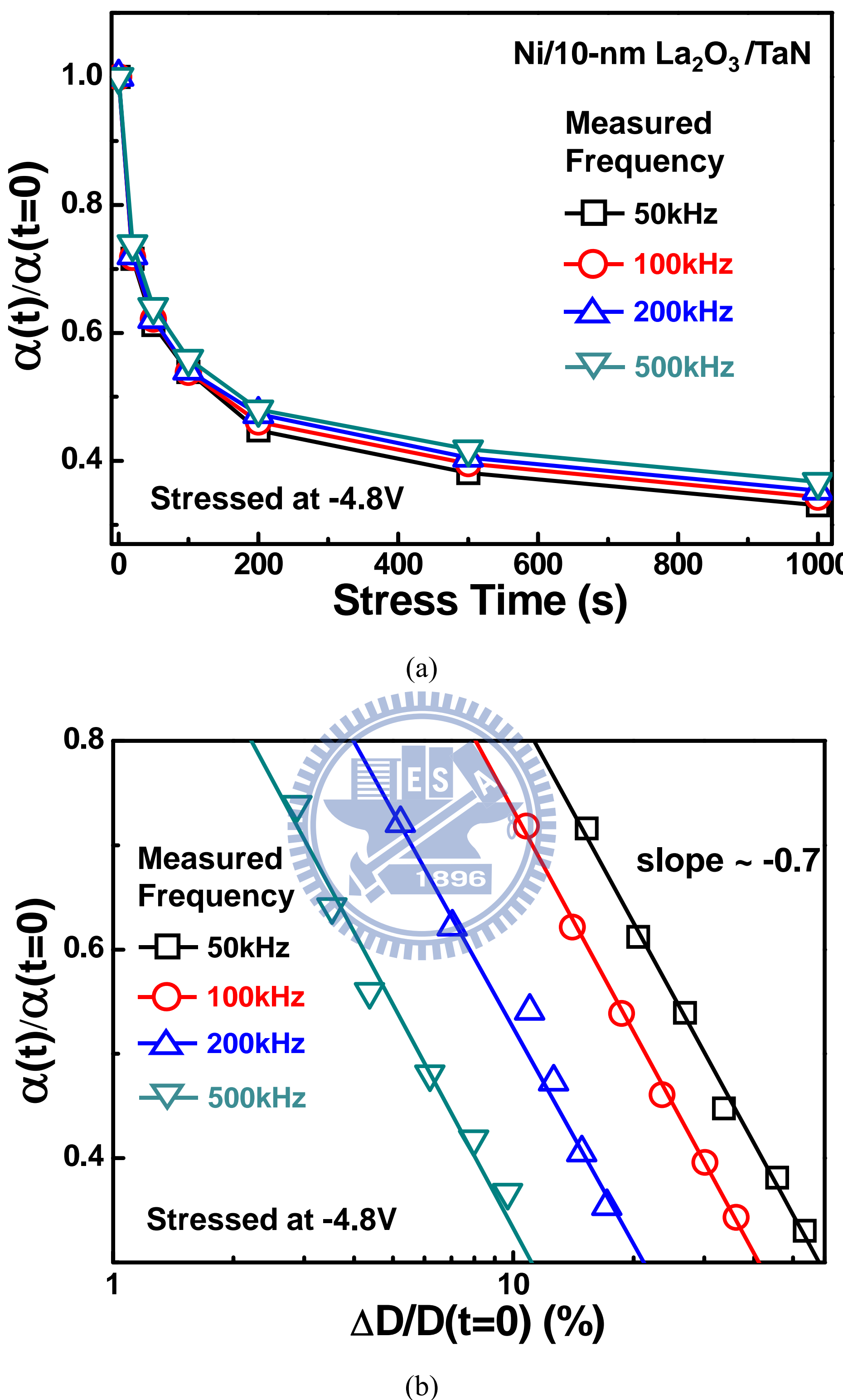


Fig. 4-25. The relative quadratic voltage coefficient of capacitance $\alpha(t)/\alpha(t=0)$ under a CVS voltage of –4.8 V with various measurement frequencies as a function of (a) stress time, and (b) relative variation in dielectric loss D.

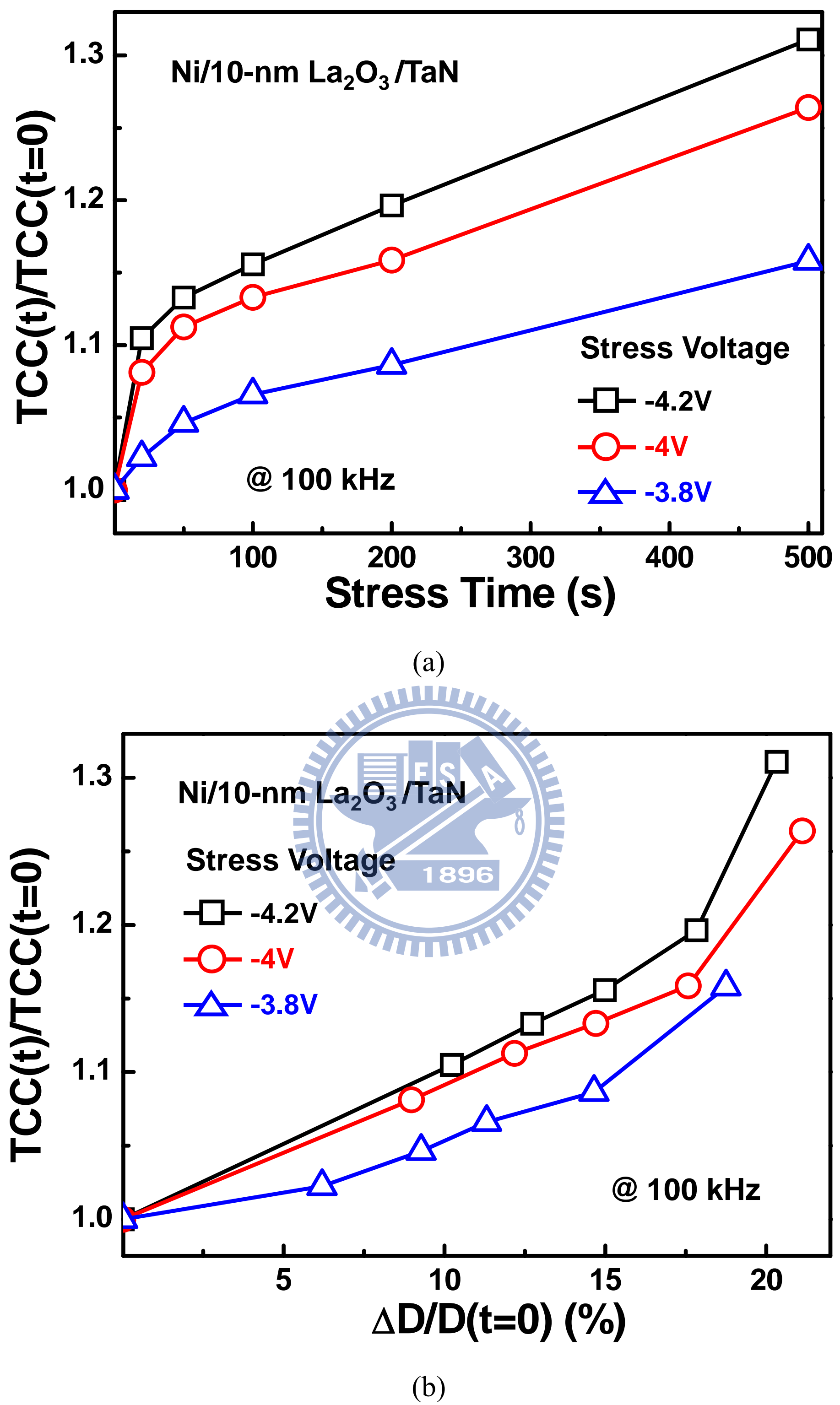


Fig. 4-26. The relative temperature coefficient of capacitance TCC(t)/TCC(t=0) under CVS from −3.8 V to −4.2 V as a function of (a) stress time, and (b) relative variation in dielectric loss D.

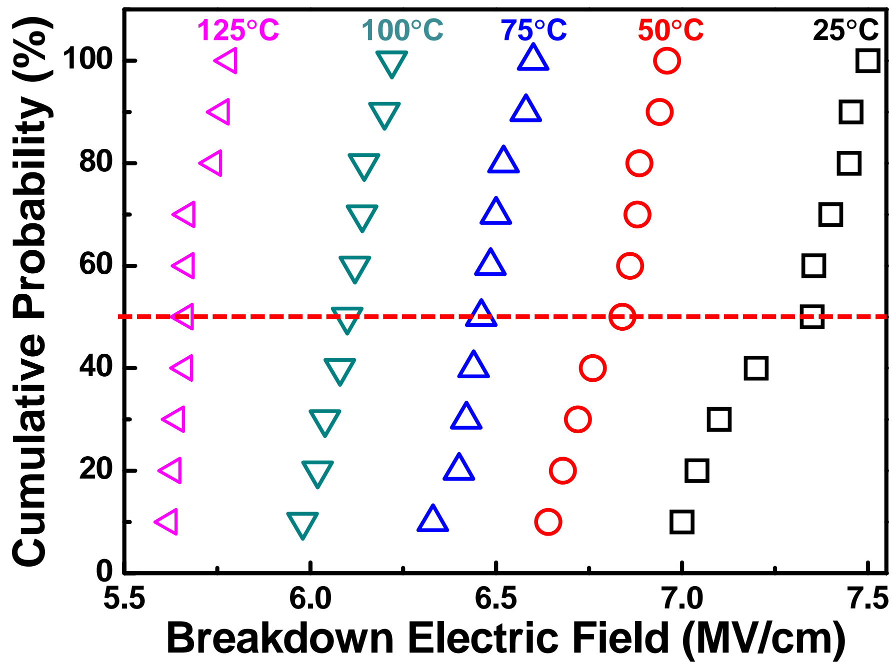


Fig. 4-27. The cumulative results of TZDB for the 10-nm La_2O_3 MIM capacitors at the measurement temperature varied from 25 °C to 125 °C.

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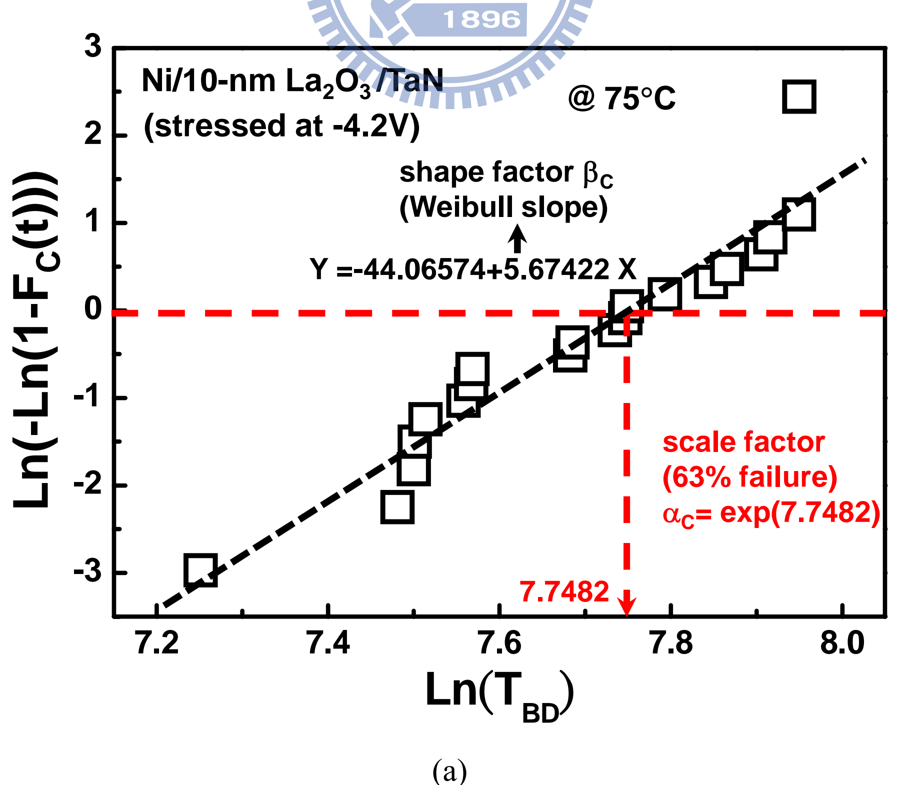
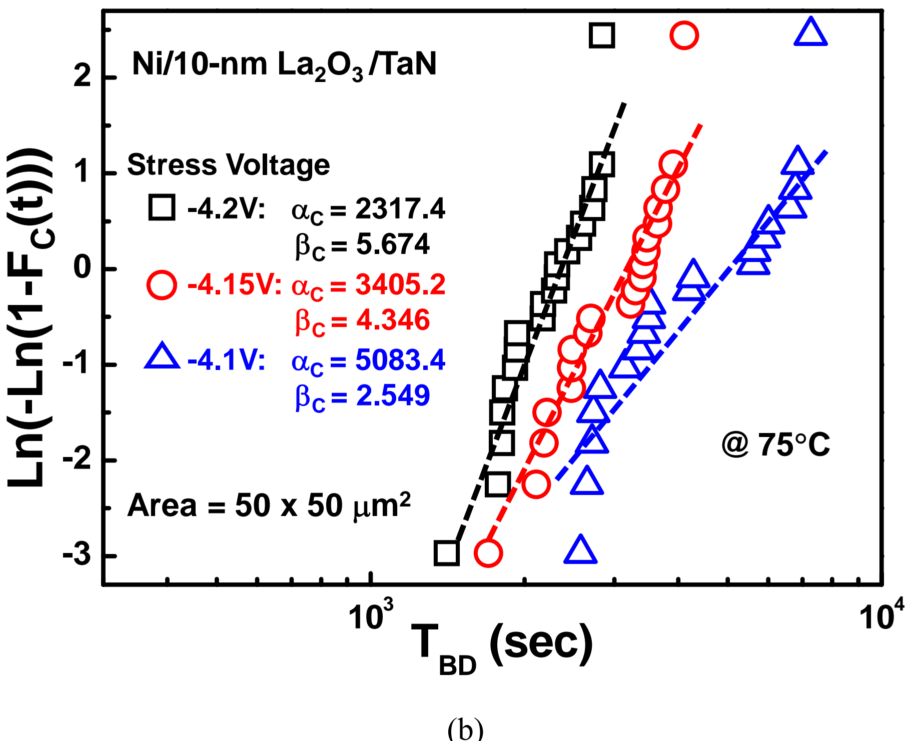


(a)



(b)

Fig. 4-28. (a) The Weibull distribution of TDDB as a function $\ln(T_{BD})$ and the extracted α_c and β_c with a –4.2-V CVS at 75 °C. (b) The Weibull distribution of TDDB as a function of T_{BD} and the extracted α_c and β_c values under a CVS of –4.1 V to –4.2 V at 75 °C.

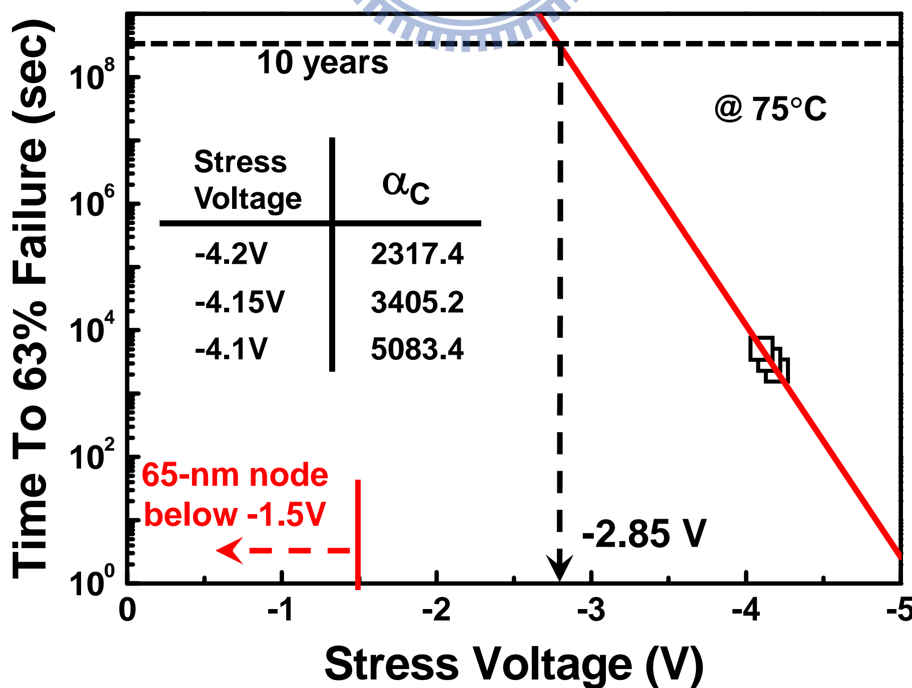


Fig. 4-29. The 10-year lifetime projection to the normal operational voltage by extrapolating all the α_C data obtained from Fig. 4-28(b).

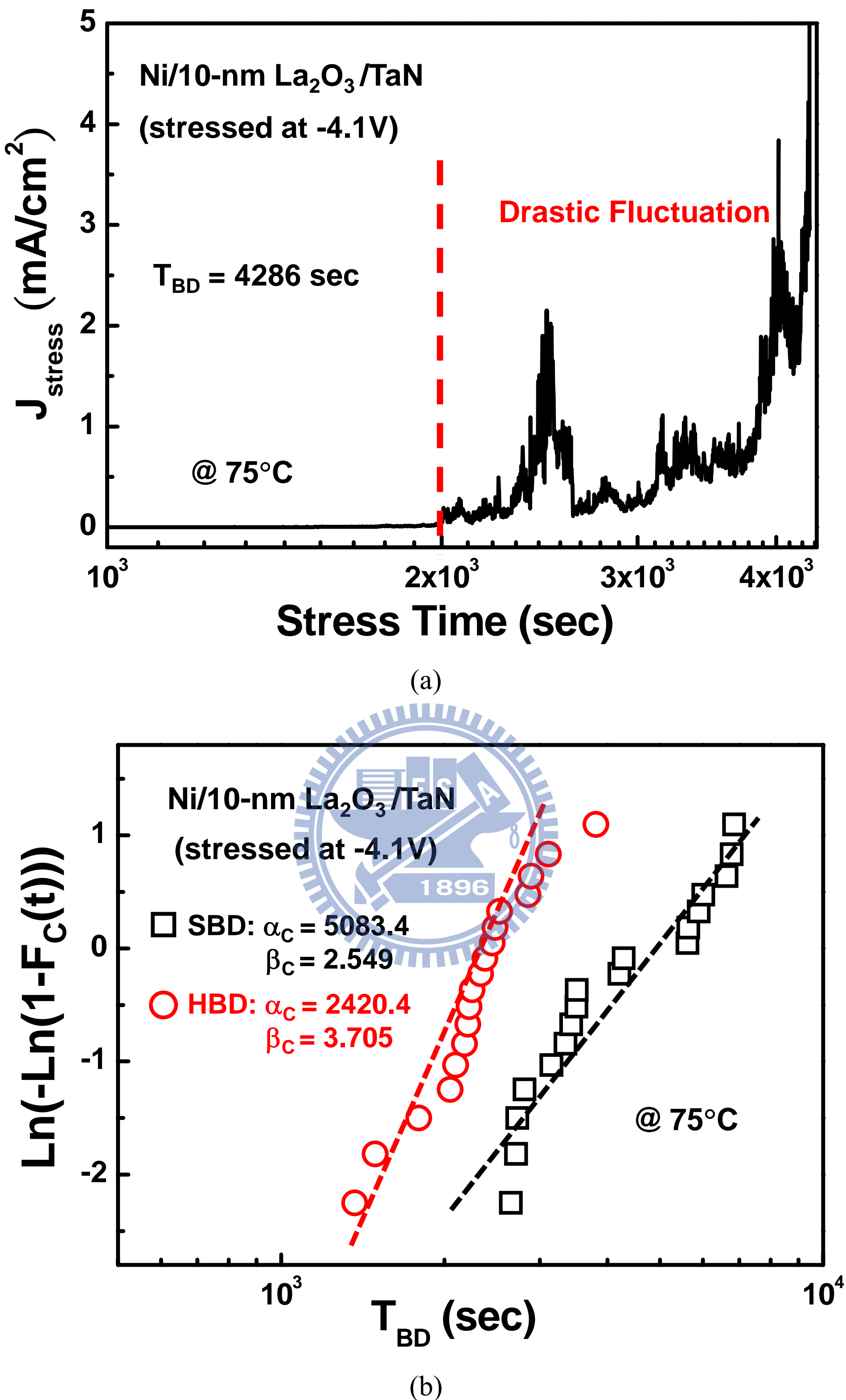


Fig. 4-30. (a) Time-dependent of J_{stress} under a –4.1-V CVS at 75 °C. (a) The Weibull plot of time-dependent soft breakdown (SBD) and hard breakdown (HBD) under a –4.1-V CVS at 75 °C.

CHAPTER 5

CONCLUSIONS AND FUTURE PROSPECTS

5.1 CONCLUSIONS

In this thesis, we demonstrate the operational principles and the implementation issues of the La_2O_3 high-k MIM capacitors integrated into the VLSI backend for RF/analog applications, including leakage current and conduction mechanisms, analog properties and distortion mechanisms, stress behaviors and degradation processes, dielectric breakdown and reliability characteristics. The innovation and major points of this research are concluded as the following.

To begin with, we evaluate the conduction mechanism of the La_2O_3 MIM capacitors for the first time. The Poole-Frenkel emission dominates the leakage current at high field region, while the Schottky emission is not a unique mechanism to govern the conduction behavior at low field region. The definite carrier transportation in conventional SiO_2 MIM capacitors is no longer validity and necessary to modify for high-k MIM capacitors due to the high trap density in it and lots of interface states in the bandgap of the dielectric. The very low leakage of the 10-nm La_2O_3 MIM capacitor could be achieved in this work, and the current density at −1 V is still below 400 nA/cm^2 even though at the temperature as high as 125 °C.

Next, the effects of voltage, temperature, and frequency on capacitance of La_2O_3 high-k MIM capacitors are investigated, since passive components in RF/analog circuits require high precision analog properties to avoid the signal distortion. As discussed in section 4-3, the space charge polarization and relaxation are principally responsible for the VCC characteristics, but the dipolar polarization and relaxation dominate the TCC characteristic. Actions of these two mechanisms on analog characteristics are demonstrated clearly, which is

crucial for developing the precise MIM capacitors with high-k dielectrics. Under CVS, VCC decreases since the space charge mobility reduced by stress induced traps, but TCC increases because the quantity of trap induced dipoles grows during stress. As a result, methods to improve the VCC of high-k MIM capacitors are reducing the amounts of charges injecting into the dielectric and then further retarding the motion of space charges to follow the external alternating voltages. On the other hand, reducing the defect density in the dielectric and at metal/insulator interface to decline the numbers of trap induced dipoles would likely ameliorate the TCC of high-k MIM capacitors. Consequently, some recommendations for improving VCC and TCC without reducing the capacitance density are noted in Table 5-1.

Subsequently, the stress behaviors and reliability issues of La_2O_3 high-k MIM capacitors under various CVS conditions are studied in this research, too. The wear-out mechanisms of La_2O_3 MIM capacitors during electrical stressing are trap generation and charge trapping, which could be identified by measuring the SILC ($\Delta J/J(t=0)$ at low field) and the relative variation in capacitance, respectively. Under CVS testing, degradation events (SILC, trapping/detrapping processes) continue to take place randomly and accumulatively. When the trap density of the dielectric reaches the critical defect density that can form a connection of these defects throughout the entire dielectric film, the time-dependent dielectric breakdown occurs. However, two-step time-dependent breakdown, soft breakdown (SBD) and hard breakdown (HBD), could be observed, which ascribed to the bi-layer nature of the high-k dielectric with an unavoidable interfacial layer (IL) and the high-k layer itself as it directly contacts the metal electrode. Differing from the SBD of ultra thin SiO_2, the SBD of the La_2O_3 high-k MIM capacitor caused by the IL breakdown due to its higher pre-existing trap density that easily reaches the critical defect density. After SBD occurs, a severe trapping-detrapping phenomenon takes place and ultimately, the bulk high-k layer breaks down and the HBD happens. Fig. 5-1 summarizes the wear out to final breakdown evolution of the MIM capacitors under CVS testing. The IL is apparently the reliability problem for MIM capacitors

with 10-nm e-beam evaporated La_2O_3 films. As the film thickness scaling down, the impact of IL becomes more significant because of its non-scaling feature, and the transition time between SBD and HBD is shortened to accelerate the final breakdown of high-k MIM capacitors. Thus, higher intrinsic defect density of IL not only affects the leakage current and analog characteristics of MIM capacitors, but also plays an important role on the device failure rate.

Finally, Table 5-2 represents electrical characteristics of fabricated devices in comparison with other reported RF/analog MIM capacitors, and it also lists requirements for RF MIM capacitors in 2018 as mentioned in chapter 1. In a word, a highly stable and reliable 10-nm La_2O_3 MIM capacitor with low leakage current (9.4 nA/cm^2 at −1 V), high breakdown strength (> 7 MV/cm at 25 °C), small VCC (671 ppm/V^2 at 100 kHz), low thermal budget (≤ 400 °C), and sufficient high capacitance density (11.4 fF/μm^2) is achieved. In conclusion, the La-based dielectrics are the most promising high-k insulators of MIM capacitors for the RF/analog applications integrated into the VLSI backend, and this research could establish a good foundation to develop and carry out excellent performance La-based high-k MIM capacitors in the future.

5.2 FUTURE PROSPECTS

In this work, we investigate the 10-nm La_2O_3 MIM capacitors with an 11.4-fF/μm^2 capacitance density and an area of 2500-μm^2 (50 μm × 50 μm). As stated in chapters 2 and 3, the scale factor α_C and the Weibull slope β_C extracted from the Weibull distribution of TDDB could be used to predict the lifetime distribution for various capacitor areas. However, the time-dependent soft breakdown process of the high-k La_2O_3 MIM capacitors is different from the traditional SiO_2 related device. Hence, the "Weibull area scaling" principle as noted in Eq. 3-13 should be further verified by studying the 10-nm La_2O_3 MIM capacitors with various

areas. Moreover, the evolutions of J-V and C-V curves after SBD are essential to study, too.

On the other hand, the La_2O_3 MIM capacitor has been proved by low frequency measurement in this thesis that it is suitable for analog applications. Therefore, the characteristics of La_2O_3 MIM capacitors at radio frequency (RF) region could be further demonstrated. When circuits or devices work at high frequencies, many parasitic effects will occur, and it is hard to obtain the accurate electrical properties of a device. As a result, using the scattering (S) parameters is the most appropriate way to characterize high-frequency performance. For S parameters measurement in RF regime, La_2O_3 MIM capacitors with ground-signal-ground (GSG) configuration should be adopted, and the dummy device should also be fabricated at the same time for calibration.

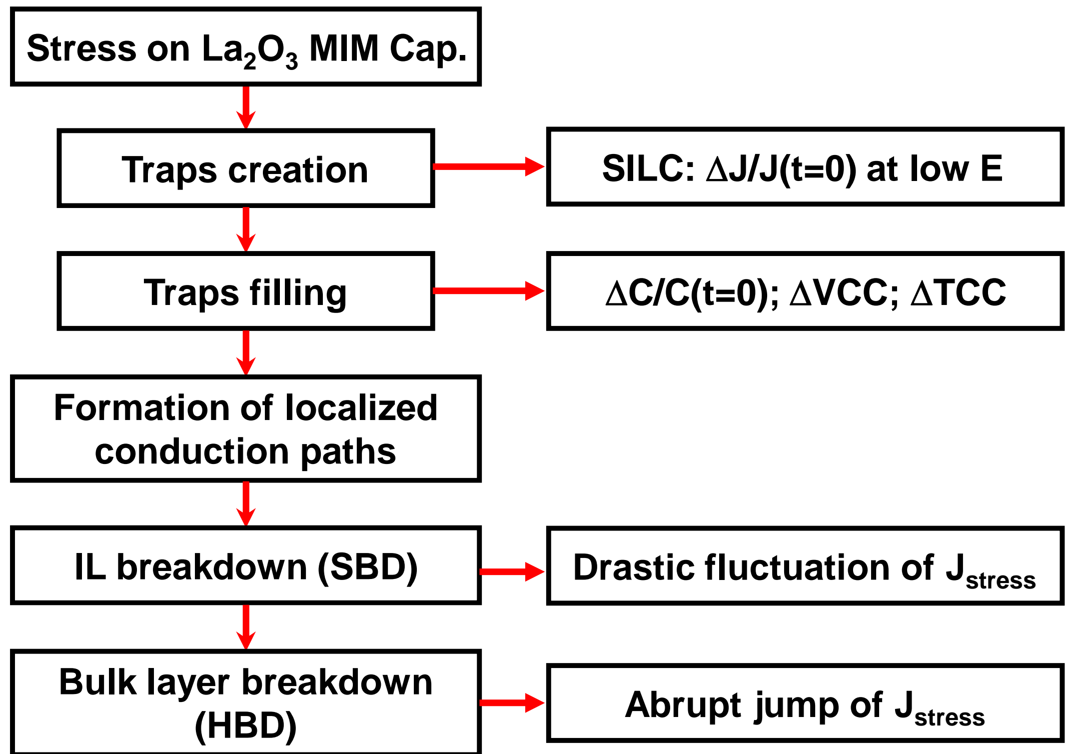


Fig. 5-1. The wear out to final breakdown evolution of the La_2O_3 MIM capacitors under the constant voltage stress.

Table 5-1. Some recommendations for improving VCC and TCC without reducing the capacitance density.

External Variable	Distortion Mechanism	Improvement Method
Voltage (VCC)	space charge polarization & relaxation	**Suppressing injection charges** (1) High workfunction metal electrode (2) Plasma treatment on electrode surface: decreasing surface roughness and interface states (3) Eliminating the IL
Temperature (TCC)	dipolar polarization & relaxation	**Decreasing defect dipoles** (1) Sufficient annealing for dielectrics (2) Plasma treatment on electrode surface (3) Adequate doping for dielectrics (4) Eliminating the IL

Table 5-2 Comparison on electrical characteristics of MIM capacitors with various high-k dielectrics.

	Deposition Method	T_{MAX} (°C)	*Thickness (nm)*	*C* (fF/μm²)	*J*** (A/cm²)	*α*** (ppm/V²)	*TCC* (ppm/°C)	E_{BD} (MV/cm)	$V_{stability}$ (V)	$V_{reliability}$ (V)
La_2O_3 [This Work]	E-beam Evaporation	400	10	11.4	9.4×10^{-9} (Ni)	671	320	> 7	3.93	2.85 @ 75°C
La_2O_3 [3]	E-beam Evaporation	400	22	9.2	> 1×10^{-6} (Pt)	> 3000	347	2	N.A.	N.A.
TiO2 [14]	E-beam Evaporation	300	20	28	3×10^{-8} (Ir)	5010	353	N.A.	N.A.	N.A.
HfAlO [29]	ALD	450	17	9.36	< 4×10^{-10} (TiN)	1456	252	N.A.	3.3	N.A.
HfO_2/Al_2O_3 [103]	ALD	420	13	12.8	1×10^{-8} (TaN)	1990	N.A.	5.85	N.A.	3.3 @ 25°C
TiHfO [105]	Sputtering	400	30	14.3	8.4×10^{-8} (Ni)	3392	123	N.A.	< 1.5	N.A.
BST [134]	Sputtering	800	300	13.4	1×10^{-6} (Pt)	5930	1000	N.A.	N.A.	N.A.
BST/Cr/BST [134]	Sputtering	800	302	11.5	> 1×10^{-7} (Pt)	1780	504	N.A.	N.A.	N.A.
ITRS @2018	–	400	–	10	1×10^{-8} @1V	100	–	–	–	–

** This data increases largely with the thickness decreasing. $V_{stability}$: the estimated 10-year operational voltage with approximate 0% variation in capacitance. $V_{reliability}$: the estimated 10-year operational voltage with 63% failure rate. Workfunction: TaN(4.6), Ni(5.1), Ir(5.27), Pt(5.6)

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