國　立　交　通　大　學

電子工程學系　　電子研究所碩士班

碩 士 論 文

二氧化鉿經四氟化碳電漿處理後應用於有機薄膜電晶體之研究

The Study of HfO_2 dielectric by CF_4 plasma treatment for OTFT application

研 究 生：曾 憶 雯

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二氧化鉿經四氟化碳電漿處理後應用於有機薄膜電晶體之研究

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摘 要

電子束蒸鍍系統的優點是可以將製程溫度控制在 200℃以下，適合應用於軟性電子製程，但若無經過高溫熱退火，長出的薄膜較鬆散且缺陷多，故用 CF_4 電漿來處理此薄膜。在這次研究中，採用的介電層是 $Hf0_2$，我們成功的利用”氟”的修補降低了介電層的漏電。因 $Hf0_2$ 屬於高介電係數(k~24)材料，我們可以提高電容值進而降低臨界電壓，使薄膜電晶體的操作電壓降到~-2 伏特。相比於只用爐管通氮氣 150℃一小時，CF_4 電漿處理的電性較好，而經過 CF_4 電漿處理再加上沉積 HMDS 2 分鐘的電性比沒有沉積 HMDS 的好。

The Study of HfO_2 dielectric by CF_4 plasma treatment for OTFT application

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ABSTRACT

The advantage of E-Gun Evaporation System is that we can control the process temperature to be under 200 ℃, and that is suitable for the application of flexible electronic process. The thin films are loose and defective if they are not annealing with high temperature, so usually we use CF_4 plasma display panel to process the thin film. In the research, we use HfO_2 as the dielectric layer and successfully reduce the electric leakage by using fluorine to mend the dielectric layer. Because HfO_2 is a high dielectric material (k~24), we can advance the capacitor value to level down the threshold voltage and lower the operation voltage of thin-film transistor to -2V. In comparison with processing with furnace and add N_2 in it for one hour, the electronic characteristic of thin film through CF_4 plasma treatment is better. The electronic characteristic of thin film through CF_4 plasma treatment deposits HMDS for 2 minutes is better than not depositing HMDS.

誌　謝

首先，我要感謝指導老師張國明教授在碩士兩年研究中給予我熱心的指導。老師對於學問中強調嚴謹的探討數據及探究其理論機制，讓我在實驗方法和實驗態度上有很大的成長。在此獻上最深的謝意。

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另外，實驗室的同學，給予我碩士班許多的歡笑。無論是在修課或實驗，大家都一起努力、一起檢討、一起排解實驗地苦悶，這種同甘共苦的日子，我會永遠珍藏。

謝謝交大奈米中心和國家奈米實驗室提供各種的機台設備，讓我可以順利進行我的實驗。

最後，我要感謝我的父母對我從小到大的栽培，還有我姐姐總在我心情低落或感到迷惘時給予我鼓勵和開導，讓我能順利完成學業。

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Chapter 1

Introduction

1-1 Introduction of organic thin film transistor

The first OTFT invented by Tsumura. A, at 1986. [1] Comparing with traditional Si semiconductor, OTFT had the possibility of avoiding expensive systems of high vacuum, high temperature; low cost process, ability of large area application, and flexibility, etc.. The inorganic semiconductors' molecule-molecule are bonded by covalent bond, however the organic semiconductors are almost bonded by Van der Waals forces and coulomb force, and the interaction of them are weak, so the mobilities are apparently lower than inorganic semiconductor a few orders(Si crystal was 300~900 cm^2/V-S and pentacene was ~1 cm^2/V-S). Furthermore, the thin films consist of organic molecules which are solid, but they still can be seen as the extremely low temperature liquid. So, the stable of devices are bad.

Due to the characters of organic semiconductor, the OTFT have been used in various applications in displays and flexible electronic devices, such as biochemical sensors, liquid-crystal flat panel displays, radio-frequency identification (RFID), etc.

Although OTFT had been studied for many years, but there're still space we can devote to, such as improving the mobility, output current, operation speed, and lowering the operation voltage.

1-2 Organic semiconductor material

Compared with traditional thin film transistor, the OTFT using organic materials instead of inorganic materials. In the past, we described electrical characteristics of the materials through energy band diagram theory. And energy band theory emphasized the periodicity and directivity of substances. Because of the characters between conductor and insulator, inorganic semiconductor can be applied widespread. In energy band theory, the vanlance band of semiconductor filled, but it has a smaller energy band gap (~1ev). In the room temperature, electrons thermal inject into conduction band, and obtain the character of electric conduction. Nevertheless, organic semiconductors can conduct electricity because the conjugate structures of molecule main chains have resonance phenomenon, which cause reciprocal overlapping, and resulted in a continuous molecular orbit, and made π-electrons moving free. Therefore, when analysing the charges transmission, we should consider the characters of molecule, lattice structure, and solid state. [2] In order to explain the conductor phenomenon of the organic semiconductors, we borrowed the polaron and bipolaron theory from physics, since 1980.

On solid state, the polarons are formed by a charge carrier appeared on ionic lattices. Figure 1-1[3] shows the hole carrier would attract the negative ion and repulse the positive one, which makes some positive ions delocalize on some molecule chains[3]. When the main chains of the conjugate molecules are cut off on structure defect, and then produced a new energy state that higher than vanlance band. It just like, an electron moved from a filled band bonded molecule orbit would improve the energy state. Generally speaking, polaron is not the main electric conduction mode. Namely, the polarons cannot let electrons transmit from band to band.

When an electron move from an oxidative molecule which contains polaron, two conditions may happen. One is this electron moves from another chemical bond of

molecule chain and then produces a polaron, the other is the electron moves from the previous polaron's energy band and then creates a more stable bication, which is called bipoaron. The bipolaron then was might only transmit the electrons from band to band.

Generally speaking, conjugate molecules produced polarons on low doping concentration, and produced bipolarons on high doping concentration. If there are more bipolarons, the energy would overlap on energy band edge, and produced a narrower bipolaron energy band between the energy bands. [4]. The Figure 1-4 is the field effect mobility of organic semiconductors from 1986 to 2000.

1-2-1 Classified the organic semiconductor materials

Organic semiconductors, considered the forms, we can divide them into small molecules and macro-molecules; considered the majority-carriers types, we can divide them into p-type and n-type. P-type materials are transmitting holes, usually include pentacene, 6T (sexithiophene), P3HT (regioregular poly [3-hexylthiophene], F8T2 (poly [9,9' dioctyl-fluorene-co-bithiophene]), PTAA (polytriarylamine), PVT (poly [2,5-thienylene vinylene]), DH-5T (α,ω -dihexylquinquethiophene), DH-6T (α,ω-dihexylsexithiophene), etc, which are shown in Figure 1-2[5] . Among them, pentacene and 6T are small molecules. For small molecules we adopt evaporative method to deposit because they're hard to dissolve. Besides small molecules, the rest of them are macro-molecules. For the macro-molecules materials we usually use spin coater to deposit, in order to make them easier to dissolve, we add some substituents on these macro-molecules' main chain. For example, we spin P3HT by adding chloroform(CCl_4).

N-type materials are transmitting electrons, include BBB (poly

[bisbenzimidazobenzophenanthroline]), QM3T (3', 4'-dibutyl-5, 5"-bis (dicyanomethylene)-5, 5"-dihydro-2, 2': 5',-2"-terthiophene), NTCDI (naphthalene tetracarboxylic diimide) etc, which are shown in Figure 1-3[5]. QM3T, NTCDI are small molecules.

Presently, most of organic semiconductors' LUMO(lowest unoccupied molecular orbital) are higher, which keeps electrons injected from electrode, and makes the mobility of holes larger than electrons'. As a result, the OTFT now are almost p-type. Fig.1-4 showing the field effect mobilities of organic semiconductors.

1-2-2 Characters of pentacene

Pentacene ($C_{22}H_{14}$) is a polycyclic aromatic hydrocarbon that contains five benzene rings. It's molecular weight is 278.3, and the length of its C-H bonds is calculated as~1.096 Å, and the length of its C-C bonds vary from 1.35 to 1.44 Å[6], As mentioned in the introduction, the structure contains conjugate double bonds (π-bonds) because of the benzene rings, so the band gap is 1.85eV[7], which is very close to semiconductor. Therefore, pentacene possess the ability of transmit carriers. The pentacene, with single-crystal phase, it's hole mobility is $3.2\,cm^2/V-S$, and electron mobility is $2.0\,cm^2/V-S$ in room temperature (RT). However, with the thin-film phase(polycrystal structure), it's hole mobility is $0.3\sim1\,cm^2/V-S$.

In Figure 1-5[8], the growing form of pentacene depends on temperature very much. By growing amorphous films of pentacene, which keeps the substrate temperature close to -196℃ during deposit, and the film is practically insulated because of its the disorder characters in the solid. When substrate temperature is keeping in RT during the deposit, a very high ordered film is deposited and then we

got high mobility of $0.6\,cm^2/V-S$. When the mixture of the thin film phase and the single-crystal phase is grown, the mobility is very low, and that possibly may because the coexistence of two phases causes high defective concentration.[8][9][10] The thickness of pentacene also affects the field effect mobility. The OTFT with thinner pentacene layers display higher hole mobilities probably because thinner channel forms shorter source-drain transport path for holes. The optimum thickness is about 30nm, or it will cause high leakage current. [11]

Now, many researchers try to improve the field-effect mobility of pentacene-based thin film transistors: chemical treatment on dielectric film surfaces, modification of the TFT structures, and manipulation of the pentacene deposit processes, etc.[11]

1-3 Gate dielectrics[12]

In fact, the mobility of the carriers of organic semiconductors now have approached or surpassed the amorphous Si (mobility of amorphous Si ~0.1 $cm^2/V-S$). To achieve that, we need very large operation voltage, even if lager than 30-50V. The large operation voltage will lead to excessive power consumption. A large capacitance of dielectric layer can drive the device with a lower bias. Therefore, there are many researches in dielectric layer of the OTFT. We describe dielectric layer into four classes, that is high k inorganic, polymer, self-assembled small molecules and inorganic/polymer stacked.

1-3-1 High-k inorganic

SiO_2 has relatively low dielectric constant (k=3.9) and substantial tunneling currents when extremely thin films are employed. The use of suitable high-k materials

can obtain greater capacitance values. That means the interface of semiconductor/ dielectric has a greater surface charge density. Under the same capacitance values, larger insulator thickness has lower leakage currents. As $V_{th} = \phi_{ms} - Q_{tot}/C_{ox} - Q_{dep}/C_{ox} + 2\phi_F$. We can get low V_{th}, when the oxide capacitance density($C_{ox}=\varepsilon_0 k/t_{ox}$) increased.

As the $S(V/dec) = \left[\frac{\partial \log_{10}(I_D)}{\partial V_G}\right]^{-1} = \frac{mkT}{q} \times \ln(10) = \frac{kT}{q}\left(1 + \frac{C_{dep} + C_{it}}{C_{OX}}\right) \times \ln(10)$

when we have greater capacitance values, we get lower subthreshold swing (SS). The Al_2O_3 [12], TiO_2 [13], HfO_2 [14], TaO_2 [15] are common dielectric materials for OTFT to reduce the operation voltage.

1-3-2 Polymer

Gate dielectrics which are solution-processable materials are often formed simply by spin-coating, casting, or printing in room temperature and under ambient conditions. The organic semiconductor materials deposit on polymer dielectric layer easier. The polymer materials can also add the adhesion to organic active layer. But the leakage current of polymer dielectric may large because it is not easy to deposit uniform. So, the polymer dielectric layer deposit thicker and the V_{th} is large. Figure 1-3 shows common polymeric dielectric materials such as PVP (polyvinylphenol), PS (polystyrene), PMMA (polymethylmethacrylate), PVA (polyvinylalcohol), PVC (polyvinylchloride).

1-3-3 Self-assembled small molecules

Self-assembled monolayer(SAM) is an ultrathin dielectric layer, which can

smaller than 3nm. The reason for being an efficient insulting barrier is its high tunneling barrier height. The values were found to be independent of the film thickness. Tunneling barrier height of a densely packed SAM of n-alkyltrichlorosilanes (thickness range 1.9-2.6) is 4.5eV for charge carrier[16], which is greater than 3nm SiO2(~3.2eV). The SAM is usually use to passivant on dielectric layer.

1-3-4 Inorganic/polymer stacked

The high k dielectric layers are thicker, (compared with SiO_2 at the same capacitance) to avoid serious gate leakage current. However, it has highly hydrophilic surface which is not compatible with the growth of organic semiconductors, because that may cause undesirable interactions with organic semiconductor. On the other hand, the major selling point of ultrathin organic gate dielectric is the hydrophobic and smooth surface which is suitable for stacking organic semiconductor. But it also has a demerit. During the deposit, there're pinholes in organic film because of the imperfections in the structure. Now we can stack the organic layer on the high k layer to circumvent the drawbacks and use the benefits of both gate materials.[17]

1-3-5 Characters of hafnium dioxide

In the future, HfO_2 thin films were widely investigated as a potential high-k oxide in replace of SiO_2 in silicon microelectronics. It can not only reduce the threshold voltage to near zero for pentacene-based TFTs, but also the thickness of the gate insulator to nanometer. The pentacene grown on the HfO_2. The grain size of pentacene increases significantly compared with those grown on SiO_2,which may

improve the field effect mobility of OTFT.[18] It has high dielectric constant (k=22~25 for high temperature process) and high band gap (E_g =5.7 eV) [14]

The interface states of high-k dielectric are similar to those of SiO_2 gate dielectric. Oxygen vacancies in the HfO_2 are formed in the deposit itself or oxygen redistribution during high-temperature processes, which lead to shallow defect sites with single- or double-charged states and traps the electrons.[19] Fluorine may be the best passivant for defects in ionic oxide because it is the only element that is more electronenegative than "O" and for its bond length is similar. That means metal-F states will always tend to lie outside of the oxide band gap.[20]

1-4 Device structure

Usually, test structures of OTFT are fabricated in several modes. Ordinarily, we could divide into two kinds, such as horizontal and vertical, which showing as Figure 1-7. The advantages of top contact are fine source/drain resolution, more planar surface to deposit pentacene and good contact resistance, and the disadvantage is contaminated pentacene by patterned source/drain. The bottom is contrary to top contact.

1-5 Organic thin film transistor operation mode

1-5-1 Source/Drain contact

Ideally, the electrodes of source/drain should be ohmic contact with majority-carriers of organic semiconductors. There are two methods to produce an

ohmic contact. First, we can increase the doping concentration of semiconductors. Second, find an appropriate mental to match. For example, in Figure 1-8, n-type semiconductors need a low work function metal and p-type semiconductors need a high work function metal. That make majority carriers "see" a lower barrier height, and than improve the mobility.

We chose pentance, which was p-type, to be our organic semiconductor, so higher work function metal was our priority selection to treat as source/drain electrodes. According to Figure 1-9, we considered over Au (work function~5.47eV) to be the source/drain electrodes.[21][22]

1-5-2 Operation mode

Organic semiconductors usually operate on accumulation mode. Take p-type pentacene –based as the example. In Figure 1-10 $V_D = V_S = V_G = 0$, If we increase the negative voltage of V_G gradually, and the negative voltage will go across the dielectric layer and will be close to the interface of dielectric and semiconductor. Positive charges accumulate on the interface of dielectric and semiconductor which causes the semiconductor energy band bending and forms a positive charges channel. The channel is an accumulation region. The positive charges come from ohmic contact of source and drain. On the contrary, when negative charges increase on interface of dielectric and semiconductor, positive charges deplete which makes the band bending inversely. After the accumulation region was formed, we add a negative V_D and make V_S=0, $V_G < V_D < 0$. The positive charges which approach drain reduce. The loss of voltage on the channel verse the position in the channel is a function. When the negative voltage in V_D is higher than V_G. As in Figure 1-11, the

positive charges will be depleted in drain and create a depletion region. The OTFT is on saturation state.

Organic semiconductors have less choices to form an inversion mode. That is because an organic semiconductor has a larger band gap in comparison with Si, the velocity of thermal induce carriers is lower than Si. Also, Carries injection in source/ drain is not ohim contact.

1-5-3 Important parameters

Organic thin film transistor usually discusses several parameters, such as mobility, threshold voltage, I_{ON}/I_{OFF} ratio and subthreshold swing.

1-5-3-1 Field effect mobility

On the influence of electric field, the transmission ability of electron or hole in the semiconductor is mobility. Theoretically, there are two methods to calculate it.

First, lower drain voltage on the linear region, drain current is add linear with the drain voltage. We can use the:

$$I_d = \frac{WC_i}{L}\mu\left(V_G - V_{th} - \frac{V_D}{2}\right)V_D \qquad (1\text{-}1)$$

If we calculate $\partial I_D/\partial V_G$, we can get a transconductance g_m:

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D=\text{const.}} = \frac{WC_i}{L}\mu V_D \qquad (1\text{-}2)$$

We measurement the low drain voltage of I_D versus V_G graph, and the slope of the curve is g_m. Substitute the W, L, C_i, and V_D, and than get the mobility.

Second, when V_D bigger than V_G which on saturation region, the accumulation layer in the drain will generate pin-off. The current satisfied

$$I_D = \frac{WC_i}{2L}\mu(V_G - V_{th})^2 \quad (1\text{-}3)$$

We drafting the $|I_D|^{\frac{1}{2}}$ versus V_G graph, the slope is $\sqrt{\frac{WC_i}{2L}\mu}$. Substitute the W, L, and C_i , and than get the mobility.

1-5-3-2 Threshold voltage

The gate voltage higher than threshold voltage is the base condition to driver device. The interface state between semiconductor and dielectric may trap the charges, when the charges transmitting and thick dielectric layer both need larger threshold voltage to drive device.

Two methods to obtain the V_{th} .

First, when operator on linear region, which based on equation (1-1), measure I_D versus V_G curve with V_S =0, low V_D , and than get a maximum gm. Make a tangent at V_G , which at maximum g_m . The tangent line cut the V_G axis, and the intersection point is $V_G = V_{th} + \frac{V_D}{2}$. Substitute the, V_D and than get the V_{th} .

Second, when on saturation region, which made square root on equation (1-3). And obtain

$$\sqrt{I_D} = \sqrt{\frac{WC_i}{2L}\mu}(V_G - V_{th}) \quad (1\text{-}4)$$

We can find the curve cut the V_G axis is the V_{th} .

1-5-3-3 I_{ON}/I_{OFF} ratio

I_{ON} express the channel current when transistor on the accumulation region, and the I_{OFF} express on the depletion region. The larger ratio shows that the device easier to control and the performance is better. Measure I_D versus V_G curve, I_{ON}/I_{OFF} ratio is the maximum I_D / minimum I_D ratio.

1-5-3-4 Subthreshold swing

Subthreshold swing always indicates the quality of the interface between dielectric and semiconductor. To subthreshold swing, the smaller value is better. Define the subthreshold swing which is

$$S(V/dec) = \left[\frac{\partial \log_{10}(I_D)}{\partial V_G}\right]^{-1} = \frac{mkT}{q} \times \ln(10) = \frac{kT}{q}\left(1 + \frac{C_{dep} + C_{it}}{C_{OX}}\right) \times \ln(10) \qquad (1\text{-}5)$$

Draft I_D versus V_G curve. Make the $\log(I_D)$ versus V_G plot, there is a linear region. The inversion of slope is the subthreshold swing.

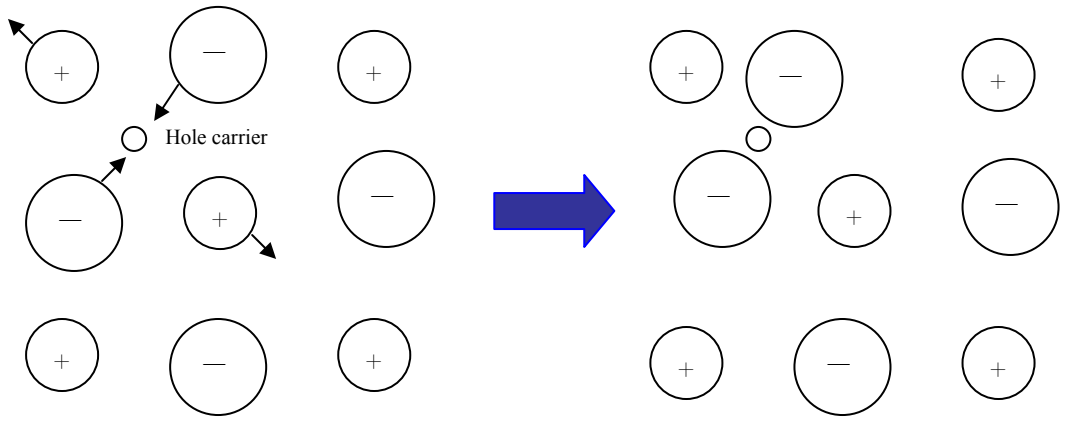


Fig. 1-1 Formation of polaron[3]

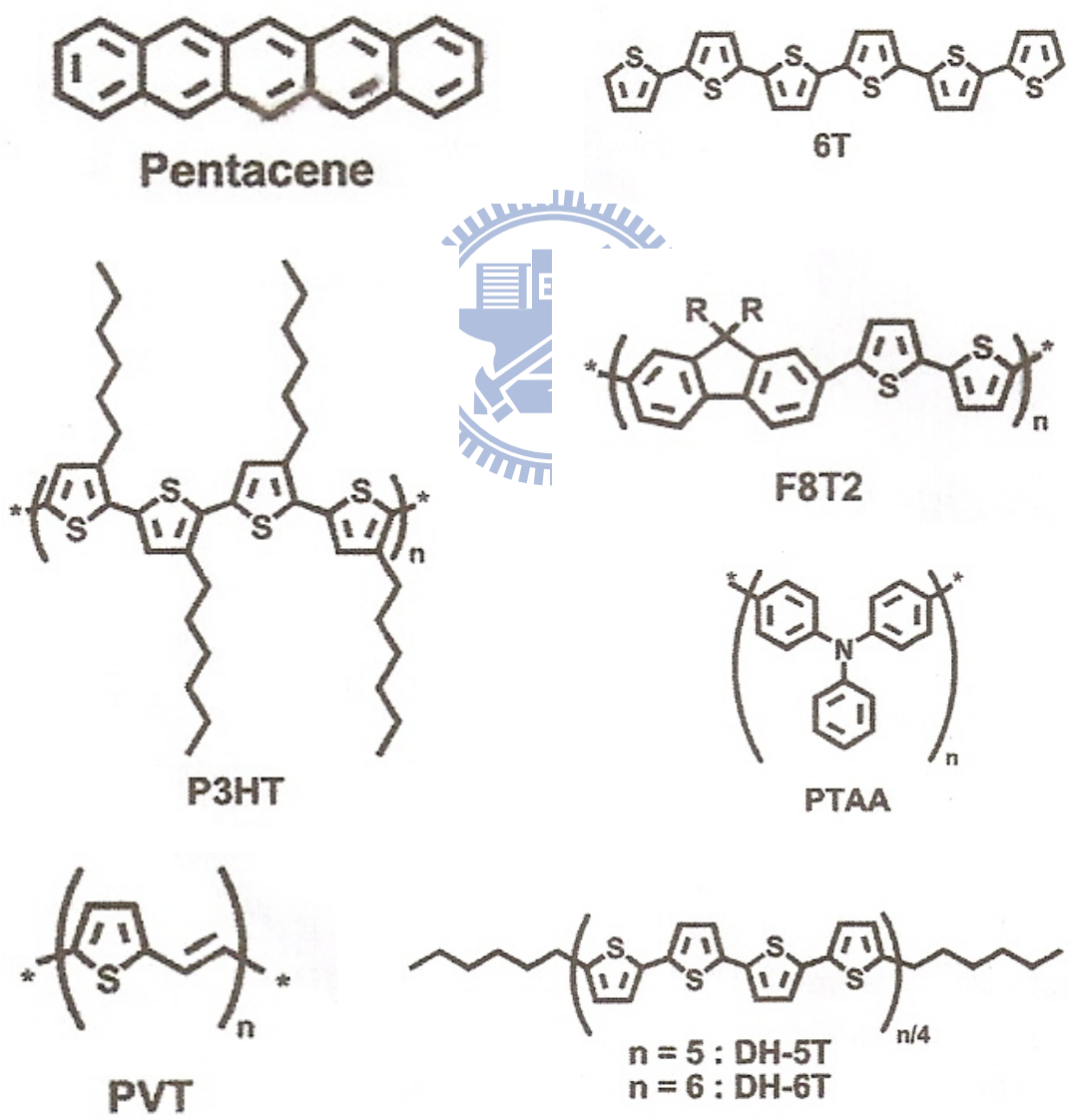
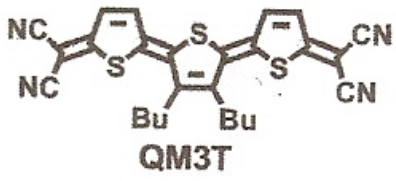


Fig. 1-2 Chemical structure of some p-type organic semiconductors pentacene, 6T, P3HT, F8T2, PTAA, PVT, DH-5T, DH-6T.[12]



NTCDI

Fig. 1-3 Chemical structure of some n-type organic semiconductors BBB, QM3T, NTCDI.[12]

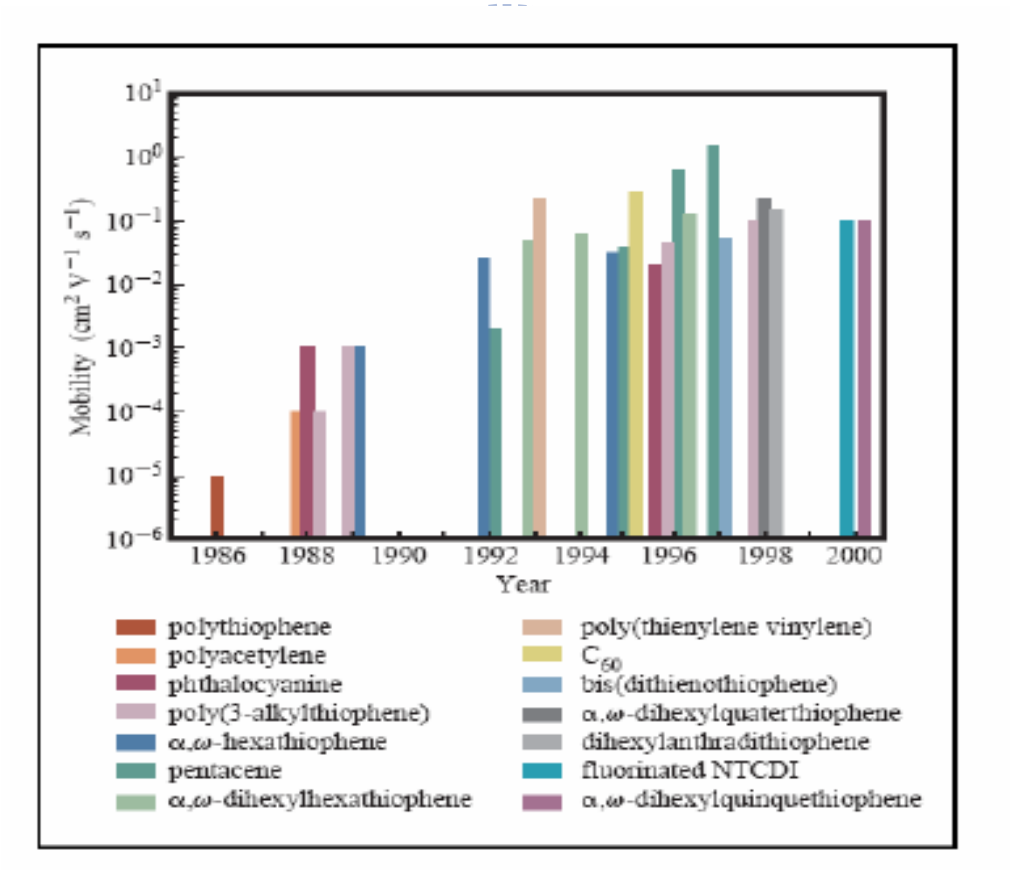


Fig.1-4 Semilogarithmic plot of the highest field-effect mobilities(μ) reported for OTFTs fabricated from the most promising polymeric and oligomeric semiconductors versus year from 1986 to 2000.[24]

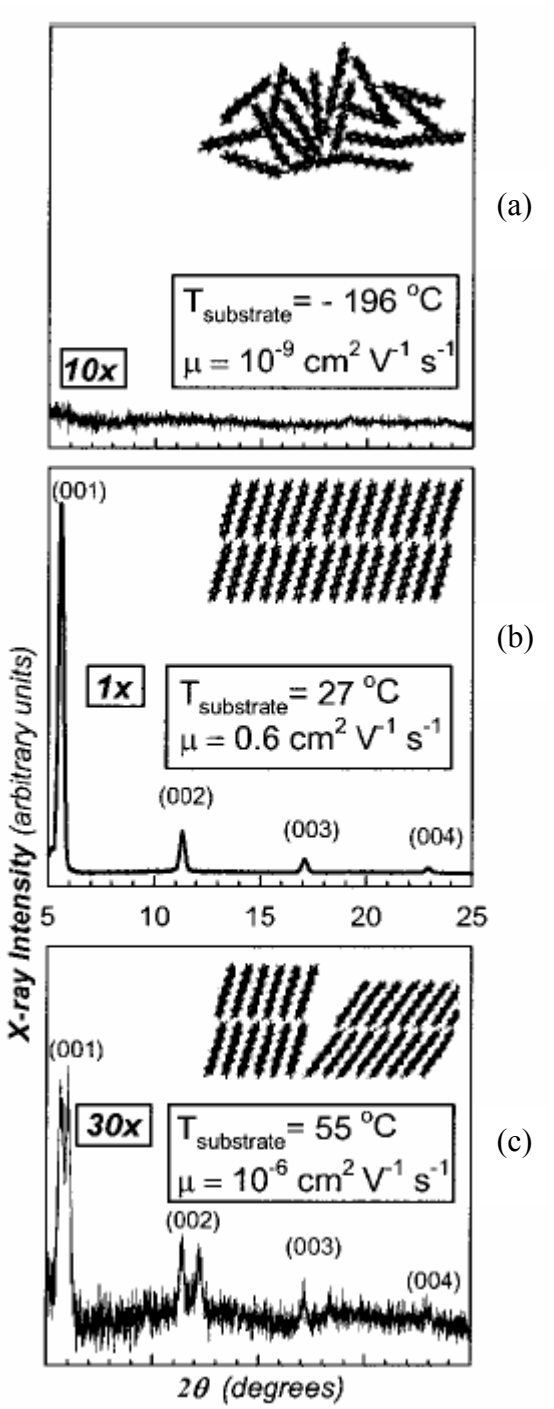


Fig.1-5 X-ray diffractograms schematic representatios of structural order, and field-effect mobilities corresponding to three different thin film pentacenes. (a) An amorphous phase is achieved using a substrate temperature. T_{sub} = -196℃ and a deposition rate. (b) A single "thin film phase" resulted for T_{sub} = 27℃ (c) Setting T_{sub} = 55℃ yielded a film consisting of two phases the "thin film phase" and the "single crystal phase" [8]

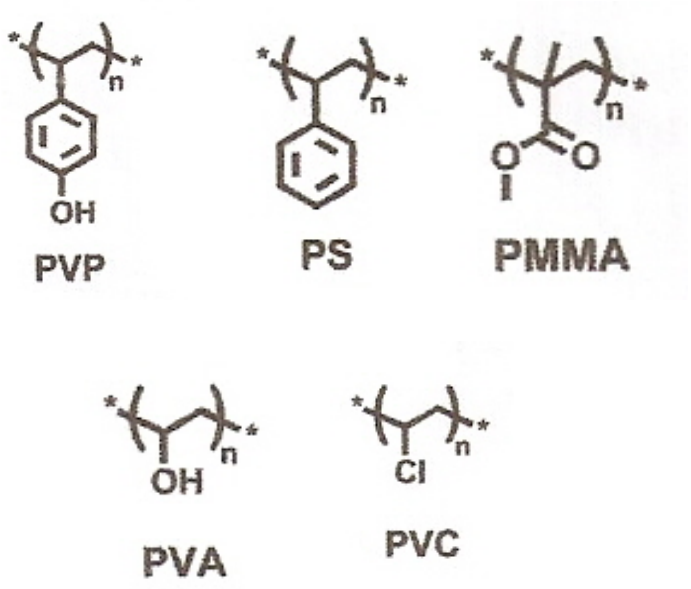


Fig.1-6 Chemical structure of some polymers used as OTFT dielectrics PVP, PS, PMMA, PVA, PVC.[12]

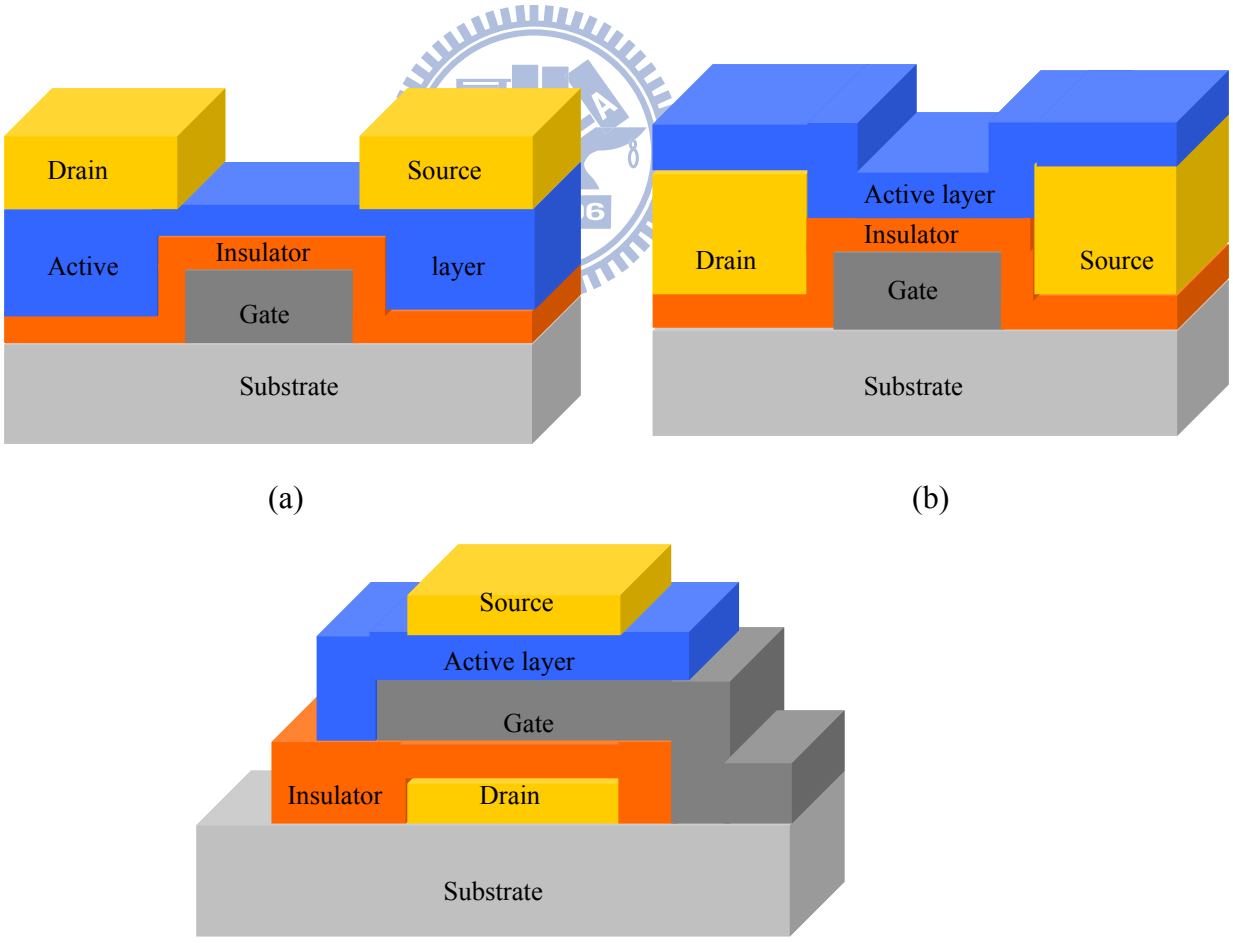
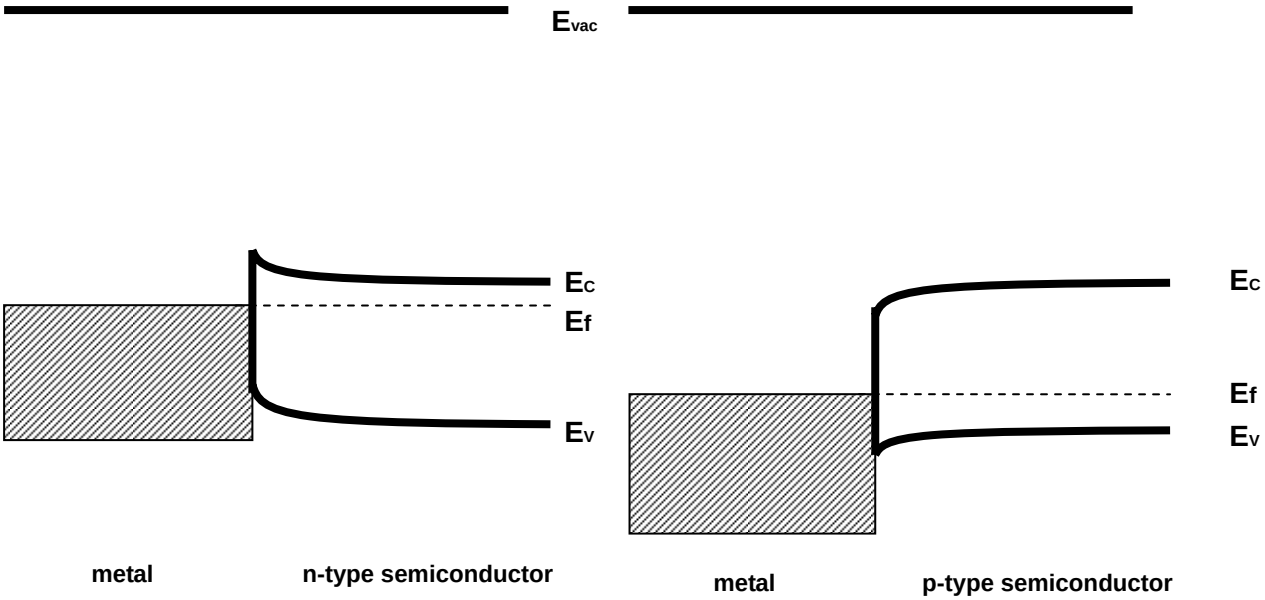


Fig. 1-7 Schematic of organic thin film transistors (OTFTs) with horizontal of (a) top contact structure (b) bottom contact structure (c) vertical structure.



(a) (b)

Fig. 1-8 Band diagram of semiconductor and metal. (a) n-type semiconductor and low work function metal (b) p-type semiconductor and high work function.

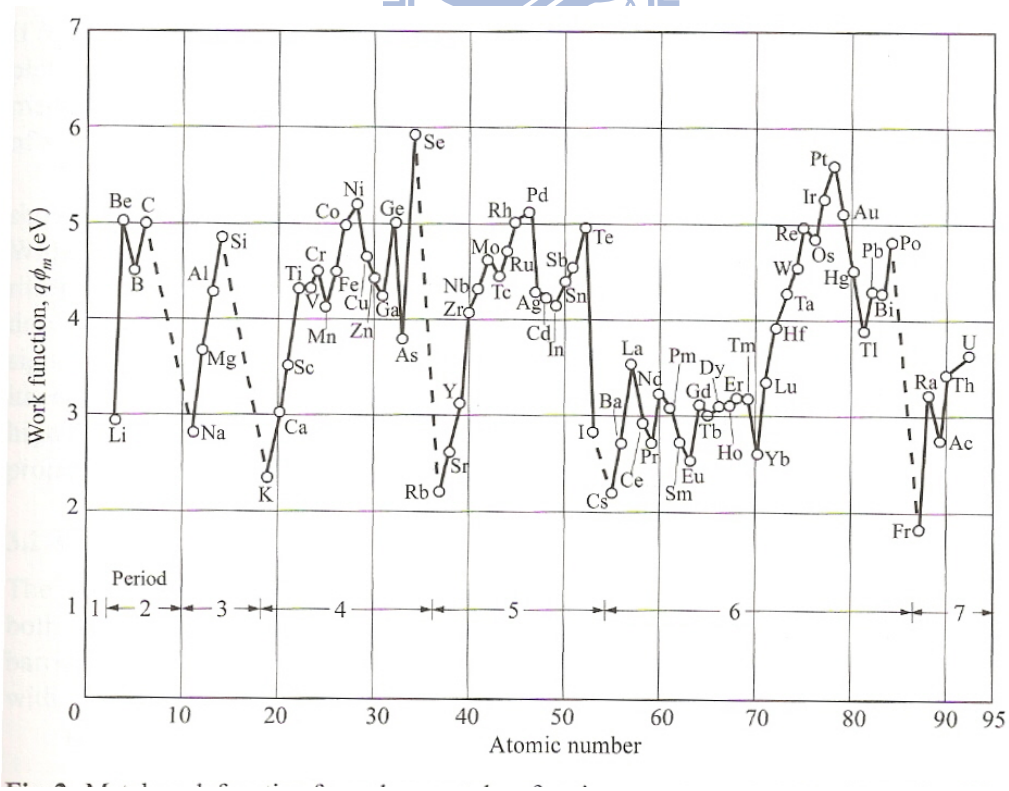


Fig. 1-9 Metal work function for a clean metal surface in a vacuum versus atomic number.[21][22]

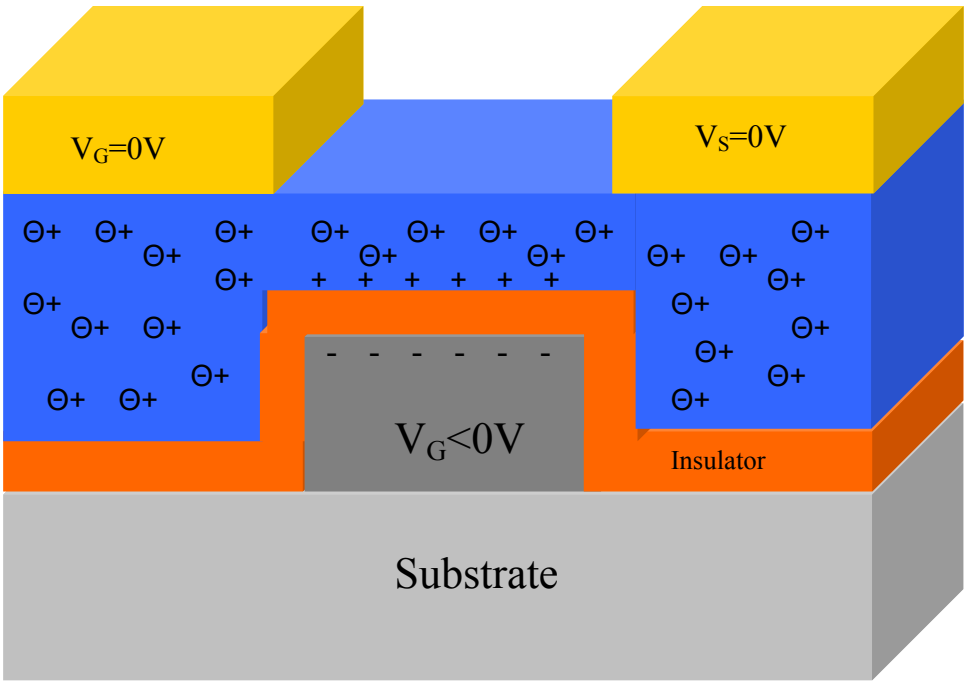


Fig. 1-10 Schematic of organic thin film transistors (OTFTs) forms accumulation region.

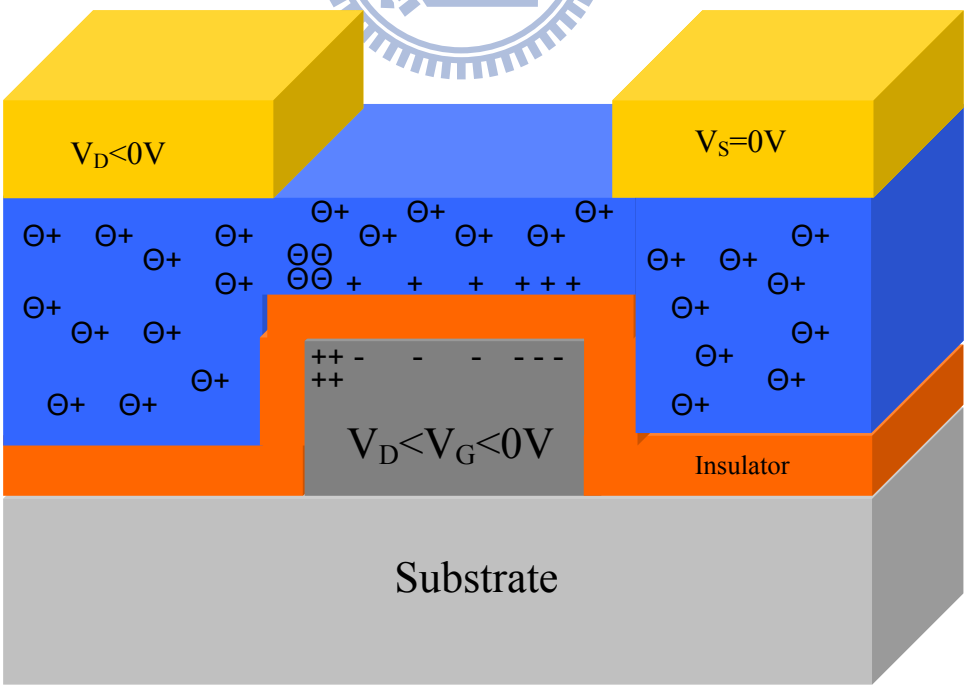


Fig. 1-11 Schematic of organic thin film transistors (OTFTs) on saturation state of accumulation mode.

Chapter 2

Experiment

2-1 Hafnium dioxide deposited with E-gun and CF_4 plasma treatment on the metal insulator metal (MIM) structure

In this scenario, we purpose to deposit hafnium dioxide dielectric on the bottom el ectrode metal by E-gun technology. In order to conform with flexible substrate, all the process, except the thermal oxide, need low temperature (< 200 ℃).

First, the n-Si (or p-Si) wafer was used as the substrate, and was rinsed in the deionization water (DI water), and then dipped in dilute HF solution (HF:DI water =1:100) , that to remove the native oxide. The wafer was accomplished the RCA clean procedure after, and use furnace at 1000 ℃, one hour to deposit silicon dioxide 500nm thick on the top of n-Si (or p-Si) substrate for isolation purpose. And the next step we choice three conditions to discuss:

2-1-1 Different bottom electrode

As shown in Figure 2-1, used E-gun to deposit 50 nm nickel (Ni), 50 nm palladium (Pd), and used sputter to deposit 50 nm tantalumnitride (TaN), 300 nm aluminum(Al) on 500 nm SiO_2 individually. And then we used E-gun to deposit the hafnium dioxide(HfO_2) 30 nm as the dielectric layer on the bottom contact at 150 ℃. The next step was using HDPCVD to add CF_4 plasma treatment in order to improve the electrical properties of dielectric. The deposition source CF_4 flow rate was 100

sccm, ICP power was 500 W, bias was 0 W, process pressure was 100 mTorr, and process time was 90 sec, temperature was150 ℃.

Finally, all top contact electrodes were deposited 50 nm thick Ni layer defined as shadow mask by E-gun. The active region pad of etch capacitors' area was $4\times10^{-4}/cm^2$.

2-1-2 Different bias of HDPCVD system

As shown in Figure 2-2, we used E-gun to deposit 50 nm Ni on 500 nm SiO_2. And then we used E-gun to deposit the HfO_2 30 nm as the dielectric layer on the bottom contact at 150 ℃. The next step was using HDPCVD to add CF_4 plasma treatment in order to improve the electrical properties of dielectric. The deposition source CF_4 flow rate was 100 sccm, ICP power was 500 W, process pressure was 100 mTorr, process time was 90 sec, temperature was 150 ℃ and bias was 0 W, 10 W, 20 W individually. Finally, all top contact electrodes were deposited 50nm thick Ni layer defined as shadow mask by E-gun. The active region pad of etch capacitors' area was $4\times10^{-4}/cm^2$.

2-1-3 Different process time

As shown in Figure 2-3, we used E-gun to deposit 50 nm Ni on 500 nm SiO_2. And then we used E-gun to deposit the HfO_2 30 nm as the dielectric layer on the bottom contact at 150 ℃. The next step was using HDPCVD to add CF_4 plasma treatment in order to improve the electrical properties of dielectric. The deposition source CF_4 flow rate was 100 sccm, ICP power was 500 W, process pressure was 100 sccm, ICP power was 500 W, bias was 0 W, process pressure was 100 mTorr,

temperature was 150 ℃ and process time was 30, 90, 150 sec individually. Finally, all top contact electrodes were deposited 50 nm thick Ni layer defined as shadow mask by E-gun. The active region pad of etch capacitors' area was $4\times10^{-4}/cm^2$.

2-2 Fabricated processes of organic thin film transistor

In this scenario, we chose the better CF_4 plasma condition to treatment on the HfO_2 30 nm insulator as gate dielectric layer on the organic thin film transistor structure.

As shown in Figure 2-4, the n-Si (or p-Si) wafer was used as the substrate, and was rinsed in the deionization water (DI water), and then dipped in dilute HF solution (HF:DI water =1:100), that to remove the native oxide, the wafer was accomplished the RCA Clean procedure after, The wafer was accomplished the RCA clean procedure after, and use furnace at 1000 ℃, one hour to deposit SiO_2 500 nm thick on the top of n-Si (or p-Si) substrate for isolation purpose. The bottom contact structure was adopted to fabricate organic thin film transistor.

And we deposited 50 nm thick Ni layer as the gate electrode by lift-off method. The Ni layer was deposited by E-gun and HfO_2 30nm deposited by E-gun. In order to compare the electronic characteristics of OTFT, we adopted three treatments on dielectric layer:

As shown in Figure 2-5, we loaded the sample into the furnace and then surrounded by N_2 one hour.

As shown in Figure 2-6, we adopted CF_4 flow rate was100 sccm, plasma ICP was 500 W, bais was 0 W, temperature was 150 ℃, process time was 90 sec, process pressure was 100 mTorr parameters to treatment on hafnium dioxide.

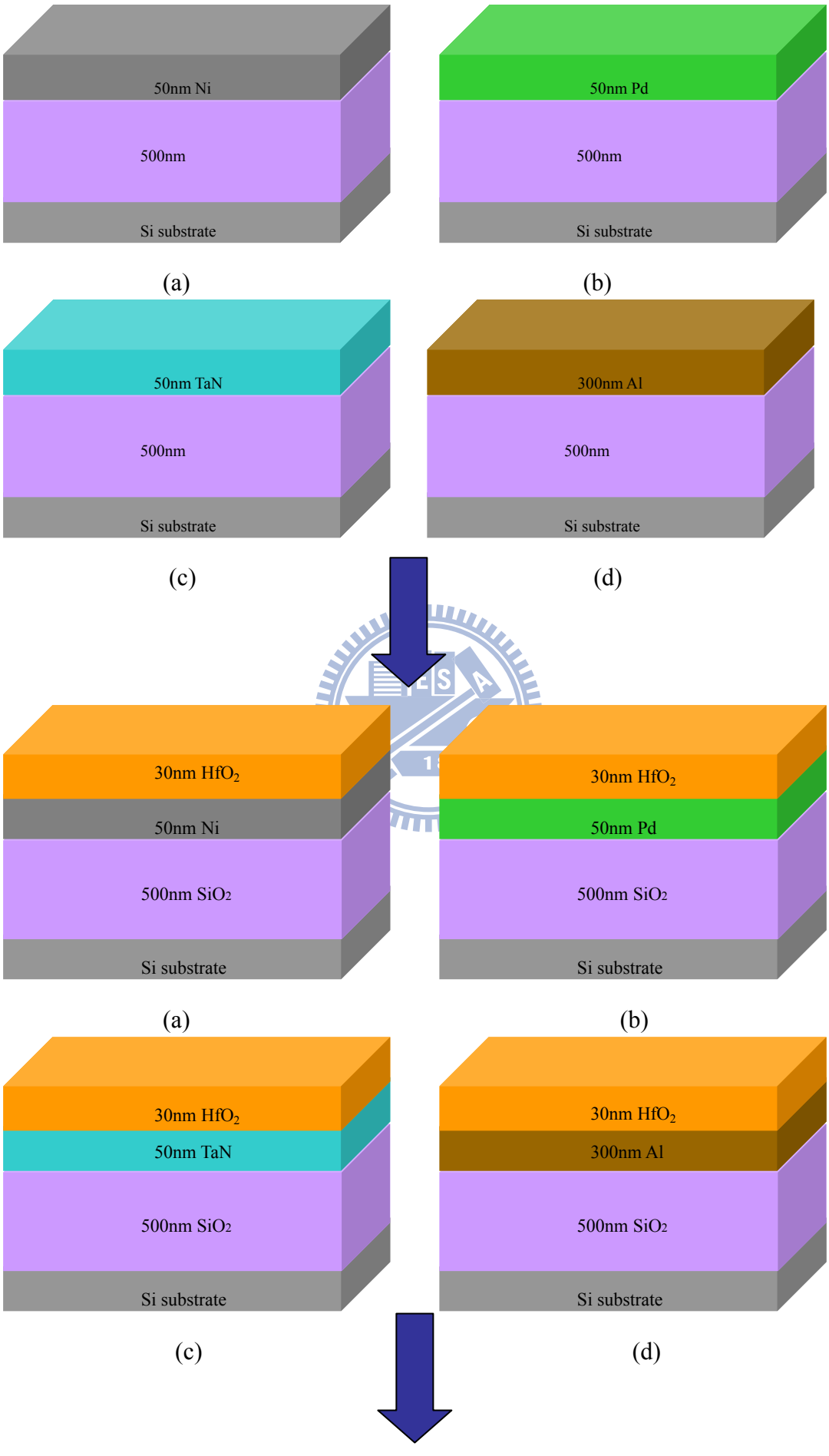
As shown in Figure 2-7, we adopted CF_4 flow rate was100 sccm, plasma ICP was 500 W, bais was 0W, temperature=150 ℃, process time was 90 sec, process pressure was 100 mTorr to treatment on hafnium dioxide, and then HMDS treatment 2min.

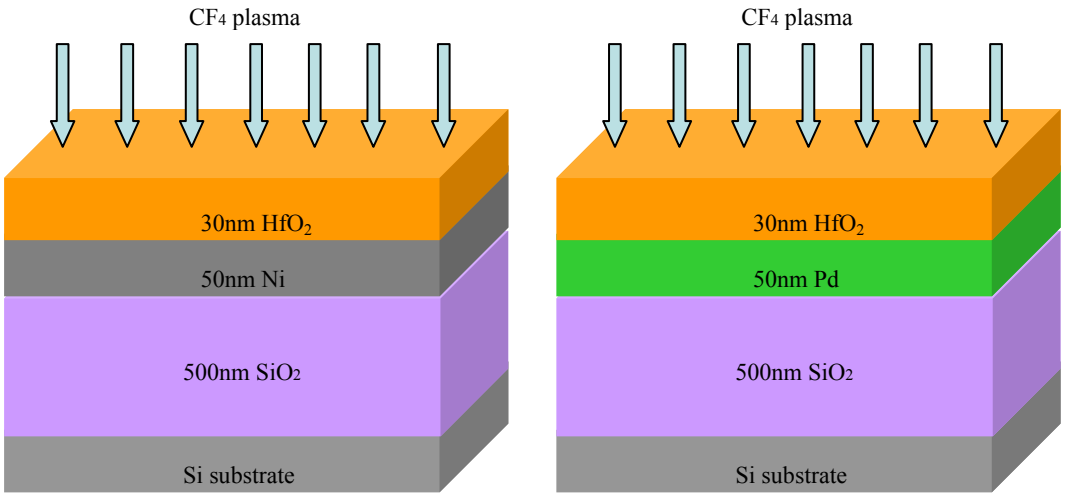
When we finished above three treatments, as shown in Figure 2-8, the next step was evaporating the pentacene active layer by thermal coater and patterned by shadow mask. During deposition of pentacene 80nm thickness, the substrate was heated to 70℃ at 17W in a pressure chamber of around 1×10^{-6} Torr.

As shown in Figure 2-9, finial step was deposited the gold (Au) as source/drain, which patterned by shadow mask. W/L=500μm/50μm.

2-3 ICP system

The high-density plasma source of HDPCVD is come from inductively coupled plasma(ICP) system. The inductive coils shown in Figure 2-10 serve just like the initial coils of a transformer. When an RF current flows in the coils, it generates a changing magnetic field. The inductively coupled electric field accelerates electrons and causes ionization collisions. Since the electric field is in the angular direction, electrons are accelerated in the angular direction, which allows electrons to travel a long distance without collisions with the chamber wall or electrode.[23]

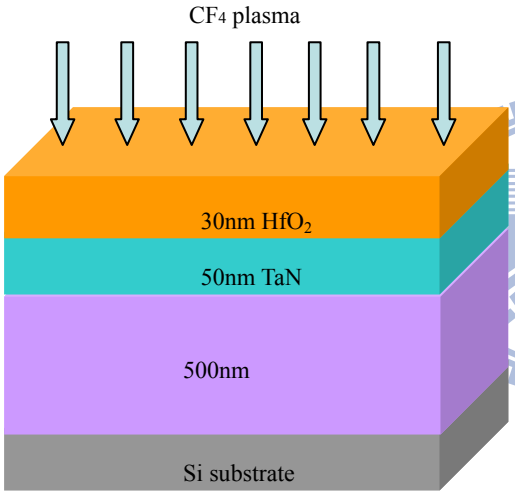

50nm Ni
500nm
Si substrate
(a)
50nm Pd
500nm
Si substrate
(b)
50nm TaN
500nm
Si substrate
(c)
300nm Al
500nm
Si substrate
(d)
30nm HfO2
50nm Ni
500nm SiO2
Si substrate
(a)
30nm HfO2
50nm Pd
500nm SiO2
Si substrate
(b)
30nm HfO2
50nm TaN
500nm SiO2
Si substrate
(c)
30nm HfO2
300nm Al
500nm SiO2
Si substrate
(d)


CF4 plasma
30nm HfO2
50nm Ni
500nm SiO2
Si substrate

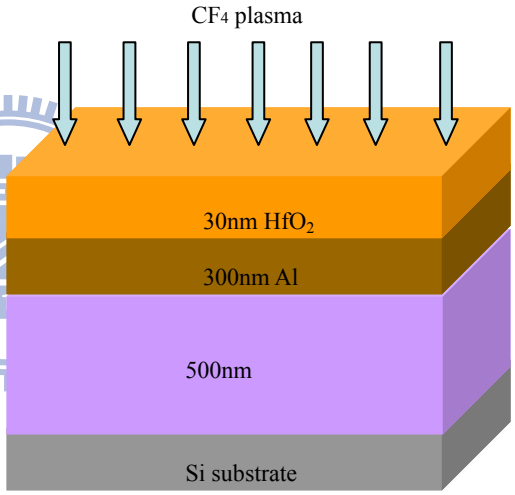
(a)

CF4 plasma
30nm HfO2
50nm Pd
500nm SiO2
Si substrate

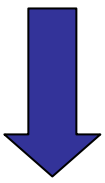
(b)


CF4 plasma
30nm HfO2
50nm TaN
500nm
Si substrate

(c)


CF4 plasma
30nm HfO2
300nm Al
500nm
Si substrate

(d)



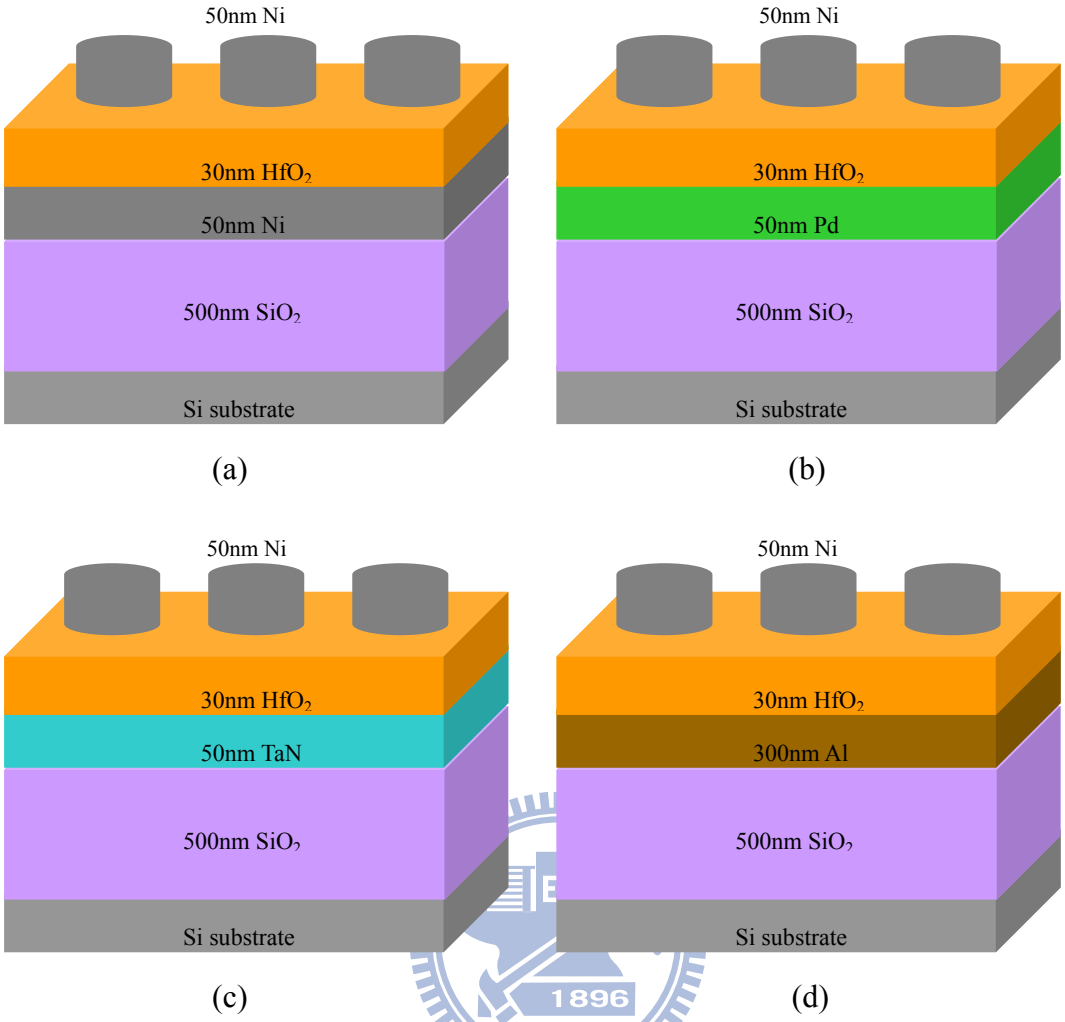
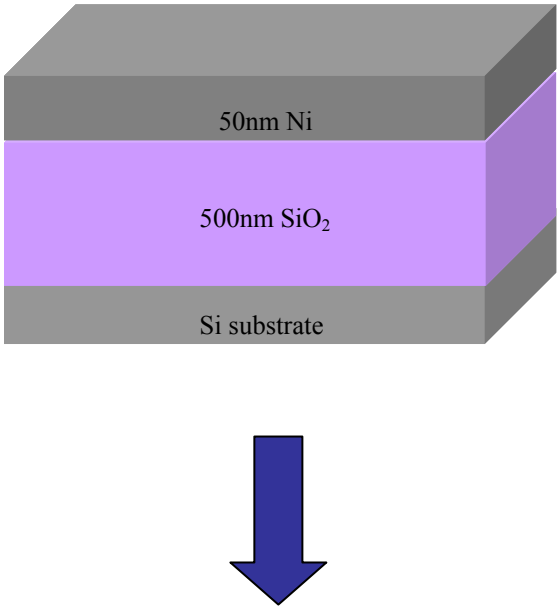


Fig. 2-1 Fabrication flow of different bottom electrode MIM structure (a) Ni bottom electrode (b) Pd bottom electrode (c) TaN bottom electrode d) Al bottom electrode.



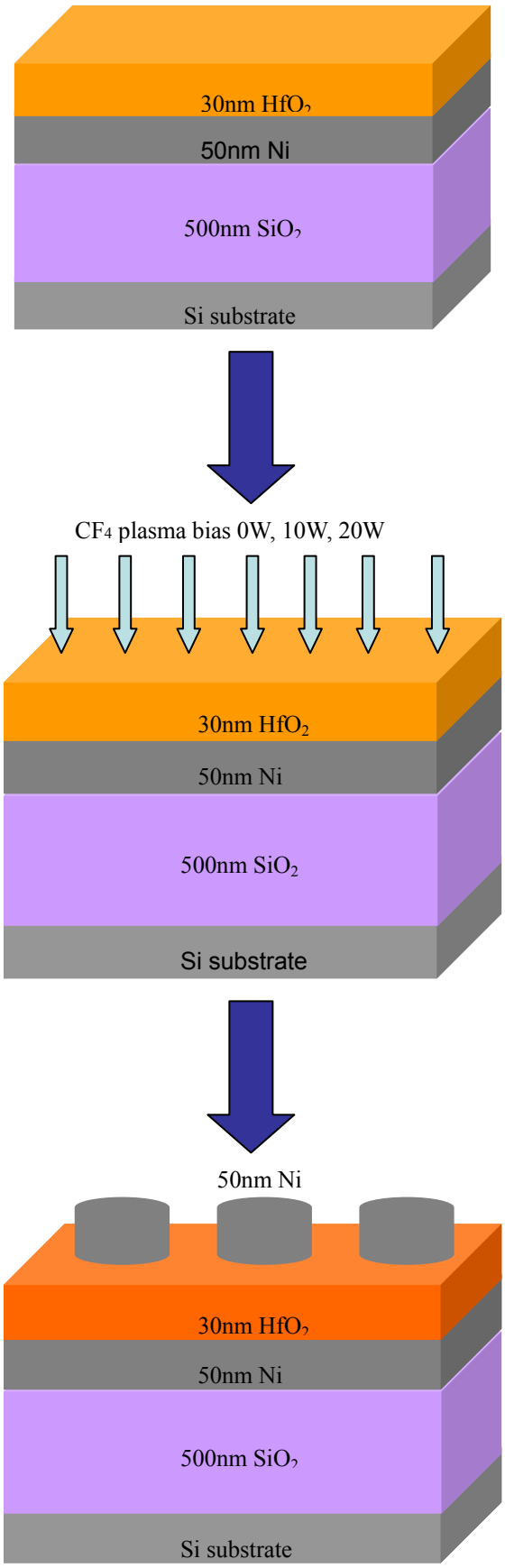
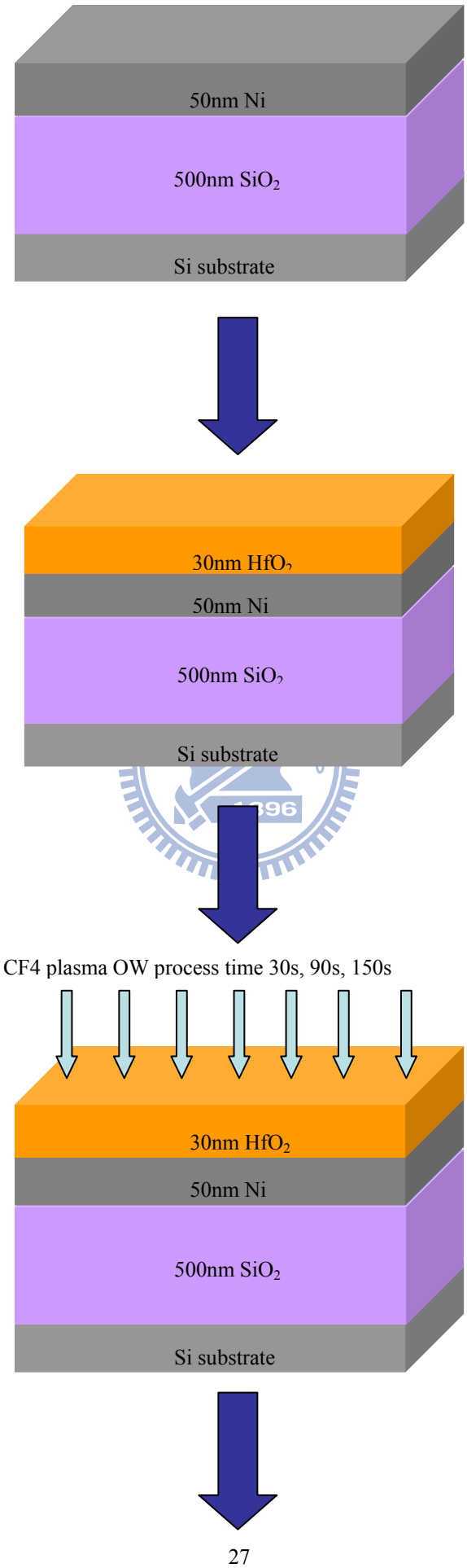


Fig. 2-2 Fabrication flow of different bias MIM structure.


50nm Ni
500nm SiO2
Si substrate
30nm HfO2
50nm Ni
500nm SiO2
Si substrate
CF4 plasma OW process time 30s, 90s, 150s
30nm HfO2
50nm Ni
500nm SiO2
Si substrate

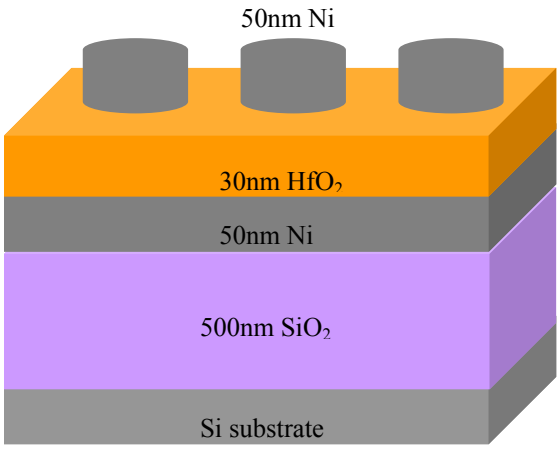


Fig. 2-3 Fabrication flow of different process time MIM structure.

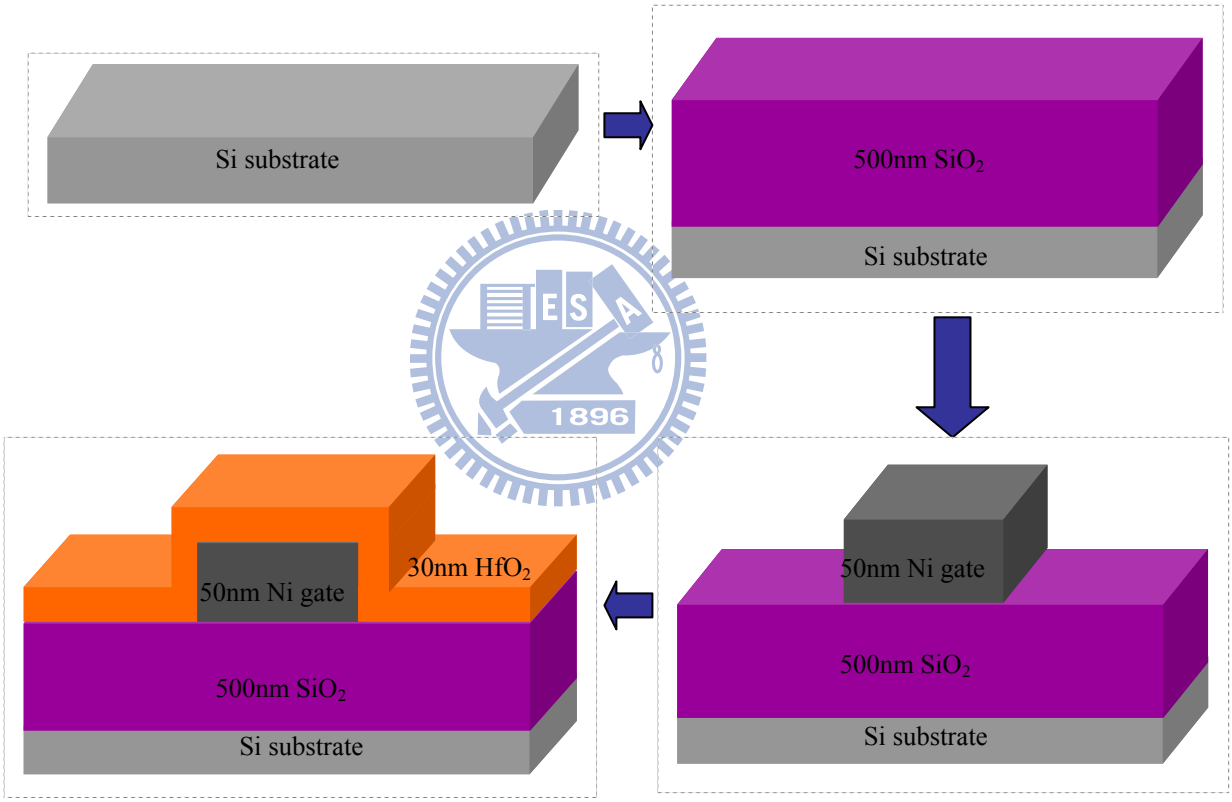


Fig. 2-4 Fabrication flow of organic thin film transistor (OTFT) before the surface treatment.

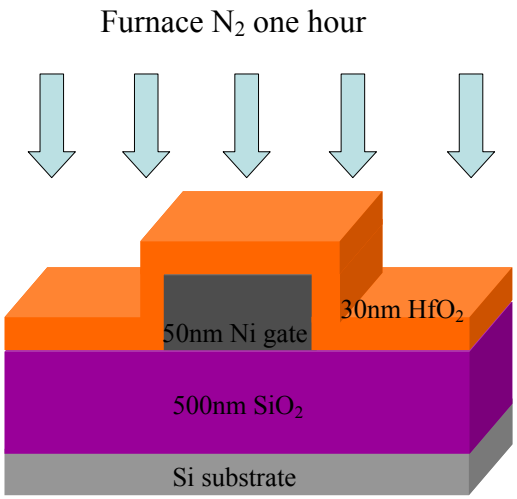


Fig. 2-5 HfO_2 treated with N_2 one hour by furnace.

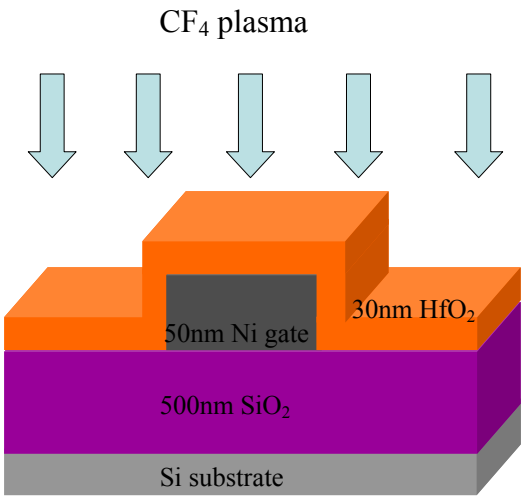


Fig. 2-6 HfO_2 treated with CF_4 plasma ICP=500W, bias=10W, time=90s, temperature=150℃, pressure=100mTorr.

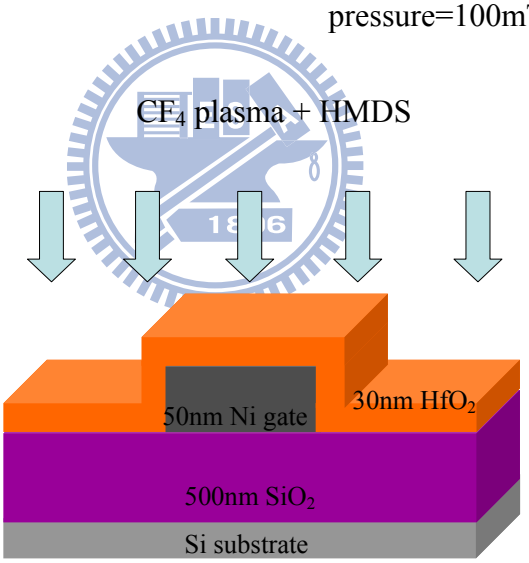


Fig. 2-7 HfO_2 treated with CF_4 plasma ICP=500W, bias=10W, time=90s, temperature=150℃, pressure=100mTorr and then added HMDS 2 min.

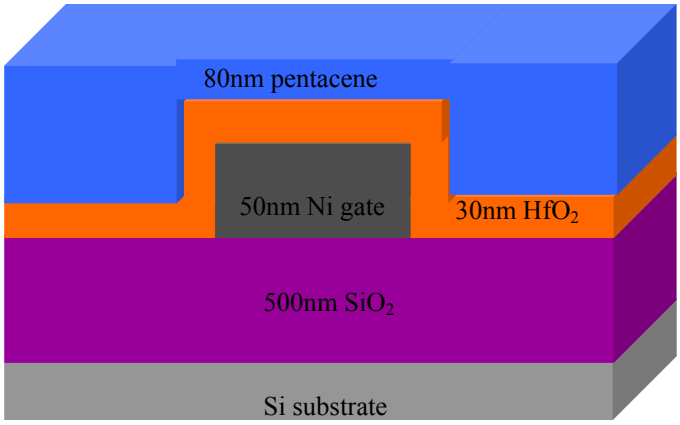


Fig. 2-8 Deposited pentacene on OTFT's HfO_2 dielectric layer.

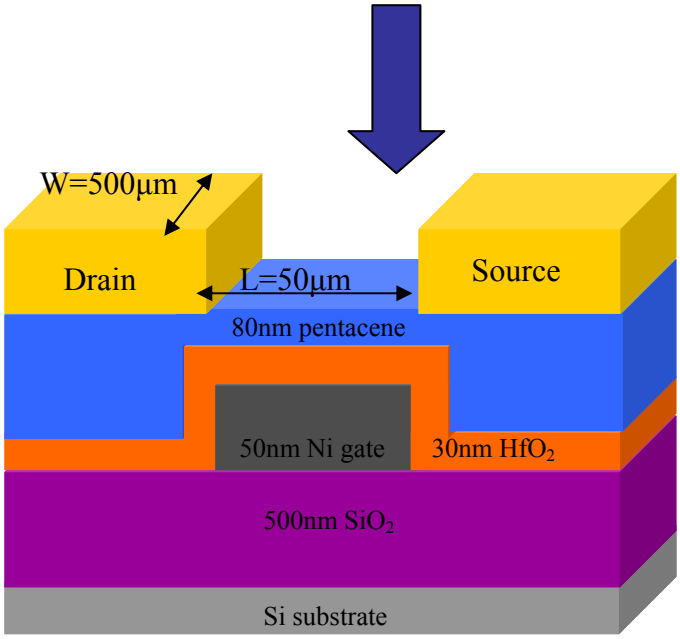


Fig. 2-9 Source/ drain patterned on pentacene.

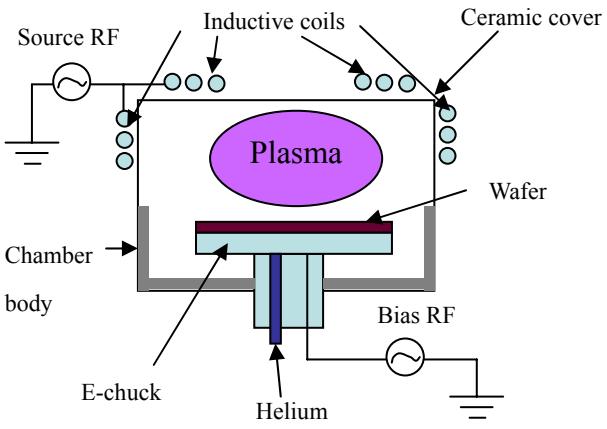


Fig. 2-10 Schematics of the ICP high density plasma system.[24]

Chapter 3

Results and Discussion

3-1 Hafnium dioxide dielectric layer quality analysis on MIM structure

In the past, when we discussed about the leakage of dielectric films, we adopted EOT parameter. Because there were many kinds of dielectric constant materials, EOT can be a standard for a comparison of gate insulator. Different conditions of CF_4 plasma treatment may change the dielectric constant of HfO_2. Because the degree how much fluorine incorporation get into the HfO_2 film might be different, and it caused different dielectric constant. CF_4 plasma treatment may also cause the C-F bonds on the surface of HfO_2. We should try to make the comparison under the same electric field obtained from the voltage divided by the EOT (Effective electric field= Bias voltage / EOT).

$$\mathrm{EOT(cm)} = \frac{3.9 \times 8.85 \times 10^{-14}\,(\mathrm{F/cm}) \times \mathrm{A(cm^2)}}{\mathrm{C(F)}}$$

"A" is capacitance area, "C" is capacitance.

In our OTFTs and testing MIM capaciators, the characteristics of all current-voltage (I-V) were measured with a semiconductor parameter analyzer (HP4156C), and C-V measurements were made with an HP4284 capacitance meter (100 kHz) in the dark in RT.

Figure 3-1 showed the SEM graph of the physical thickness of CONTROL sample and the sample after CF_4 plasma treatment. We observed the thickness of HfO_2 layer without CF_4 treatment was 40nm and with the CF_4 treatment was 40nm. The k values were 17.35 and 13.68 respectively.

3-1-1 Different bottom electrode

We must Choose one metal that a high resistance to CF_4 plasma, and the lower leakage current. We chose several metals which were more stable and cheaper to be the bottom electrode, such as Ni, Pd, TaN, and Al. After CF_4 plasma treatment on the HfO_2 dielectric layer based on different bottom electrodes, we discarded the TaN to be the metal gate. Although TaN is more thermal stable, but it has poorer resistance for CF_4 plasma. And our process temperature was smaller than 200 ℃ for flexible electronics, so we discarded the TaN to be the metal gate. Even if the TaN was still measured, it was difficult to integrate. Figure 3-2 showed the J-E characteristics of HfO_2 capacitors treated by CF_4 plasma with different bottom metal from 0 MV/cm to 4 MV/cm. We could see the different leakage current densities, which were $J_{Al} > J_{Pd} > J_{TaN} > J_{Ni}$. That may because the different metals have different work functions. In Figure 1-9, we compared the three metals (Ni, Pd and Al), the work function of Al is lower than the other two. Because the high work function may result in high barrier to the same HfO_2 dielectric layer, the electrons would be hard to "climb over", and the leakage current density would smaller. So, the maximum of leakage current was Al-based (current density was 1.18×10^{-6} A/cm^2 at 3 MV/cm), and the minimum was Ni-based (current density was 1.20×10^{-7} A/cm^2 at 3 MV/cm).

3-1-2 Different bias of HDPCVD system

Figure 3-3 showed the J-E characteristics of HfO_2 capacitors treated by CF_4 plasma with different bias of HDPCVD system from 4 MV/cm to -4 MV/cm. We

observed that the leakage current density was suppressed under all treatment conditions (bias was 0w, 10w, 20w), especially the 0W bias (current density was 4.34×10^{-8} A/cm^2 at 3V) was less than control insulator about 3 orders. Figure 3-4 is the x-ray photoemission spectroscopy (XPS) spectra, and indicates that fluorine bonded on the HfO_2 film about 0.5 nm to 7.5 nm depth. The peak located at ~685 eV corresponded to the F bonds in bulk HfO_2 [13]. Figure 3-5 is the graph of XPS analysis of "C 1s" of HfO_2/Ni bottom electrode. (a) is the HfO_2 without CF_4 plasma treatment and (b) is the HfO_2 with CF_4 plasma treatment. Compare Figure 3-5(a) with Figure 3-5(b), and we can observe that Figure 3-5(b) had a peak located at ~288 eV corresponded to C-F bonds on the surface of the HfO_2 layer.[25] So, we can infer that the C-F bonds may make the k value reduced, which reflected the Figure 3-1. Figure 3-6 is the graph of XPS analysis of "Hf 4f" of HfO_2/Ni bottom electrode. (a) is the HfO_2 without CF_4 plasma treatment and (b) is the HfO_2 with CF_4 plasma treatment. The Figure 3-6(a) showed two peaks which are Hf-O bonds. Obviously, the two peaks disappeared and the curve shifted to a large binding energy in Figure 3-6(b). Because fluorine has a larger electronegativity than oxygen, so the binding energy of HF-F bond was larger than Hf-O bond. We can infer that the fluorine bonded with hafnium after CF_4 plasma treatment. However, physical thickness of our samples was 40 nm, so we adopted another analysis. Figure 3-7 showed the secondary ion mass spectroscopy (SIMS) for sample with CF_4 plasma treatment. The fluorine concentration peaked at the top of the HfO_2 and fluorine incorporated the entire HfO_2 layer. This was because HfO_2 layer which deposited by E-gun without any high temperature thermal annealing was very loose and has high density defective bonds and trapping states. Therefore the fluorine could effectively passivate them, and the leakage current density was reduced. Furthermore, the breakdown voltage also improved from 8.6 V to 11.4 V. It might because the fluorine incorporated into HfO_2

layer and strengthened it.

In Figure 3-3, we also observed that when the bias increased, the leakage current density increased ($J_{20W} > J_{10W} > J_{0W}$). Because the bias would add the vertical bombarding energy of fluorine radical and that would damage the surface of HfO_2 layer and result in higher leakage current. Figure 3-8 showed capacitance increases with bias increases, because two reasons. First, the fluorine etched the surface of HfO_2 films and made it thinner. Second, the fluorine bombarded the C-F bond which on the surface of HfO_2 films. Moreover, pentacene thin film must deposit on a planar plane to obtain a higher mobility, we needed the fluorine radical "diffusing" into the HfO_2 layer rather than "hitting" into HfO_2. Figure 3-9 showed the atomic force microscopy (AFM) of sample：(a) without CF_4 plasma treatment which roughness was 0.596 nm, and (b) with CF_4 plasma at ICP=500 W, bias=0 W, process time=90 sec, temperature=150 ℃ which roughness was 0.515 nm. We ensure the sample at 0 W bias, so that would not cause the serious roughness.

3-1-3 Different process time

Figure 3-10 showed the J-E characteristics of HfO_2 capacitors treated by CF_4 plasma with different process time at ICP=500 W, bias=0 W, temperature=150 ℃ from 4 MV/cm to -4 MV/cm. In order to ensure a good process condition, we selected three process times such as 30 sec, 90 sec and 150 sec. We observed that the sample of 150 sec(current density was 9.60×10^{-8} A/cm^2 at 3 MV/cm) had worse leakage current density of three. Because it took too long for fluorine radical to damage the surface of the HfO_2 layer. Moreover, the sample of 30 sec (current density was 5.26×10^{-8} A/cm^2 at 3 MV/cm) had insufficient fluorine radical to fully incorporate into HfO_2 layer.

3-2 OTFT electric characteristics analysis and discussion

In this part, the parameters of the gate insulator of OTFT was CF_4 flow rate = 100 sccm, ICP = 500 W, process bias=0 W, process time = 90 sec, temperature =150 ℃. In order to compare the OTFT device without CF_4 plasma treatment, we made the HfO_2 annealing by N_2 through one hour to be the control sample. On the another hand, after CF_4 plasma treated on HfO_2, we evaporated HMDS for 2 min to improve the interface between dielectric layer and pentacene.

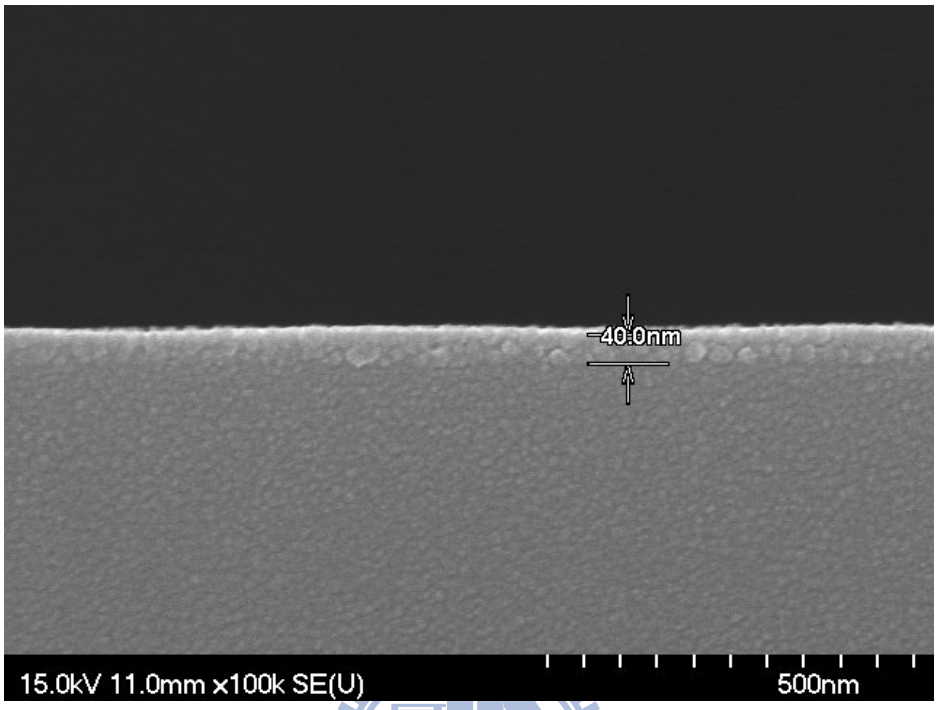
Figure 3-11 showed the AFM surface images of the HfO_2 treated with (a) N_2 annealing at 150℃ 1 hour, (b) HfO_2 treated with CF_4 plasma, and (c) HfO_2 treated with CF_4 plasma +HMDS and then deposited pentacene which the areas are $5\mu m \times 5\mu m$ and $1\mu m \times 1\mu m$. It is obvious that the grain size in pentacene of Figure 3-11(a) is smaller than Figure 3-11(b) and Figure 3-11(c). In other words, the density of grain boundary of Figure 3-11(a) is higher than Figure 3-11(b) and Figure 3-11(c). The higher density of grain boundary will cause more leakage current paths. So we supposed that the HfO_2 with CF_4 had better electric characteristics than treated with N_2 annealing.

Figure 3-12 (a), (b), (c) showed the drain-current voltage curves($(I_D - V_D)$ which obtained from pentacene-based TFTs, were respectively fabricated on N_2 annealing gate dielectric, CF_4 plasma treated gate dielectric and CF_4 plasma+HMDS treated gate dielectric. These three types of devices successfully demonstrated the characteristics of OTFT that the operation voltage is lower than -2 V. The maximum saturation current ~ -0.025 μA, achieved under a gate bias (V_G) of -4 V from the OTFT with the N_2 annealing gate dielectric while about ~ -0.75 μA was achieved from the OTFT with CF_4 plasma +HMDS treated gate dielectric. Although after

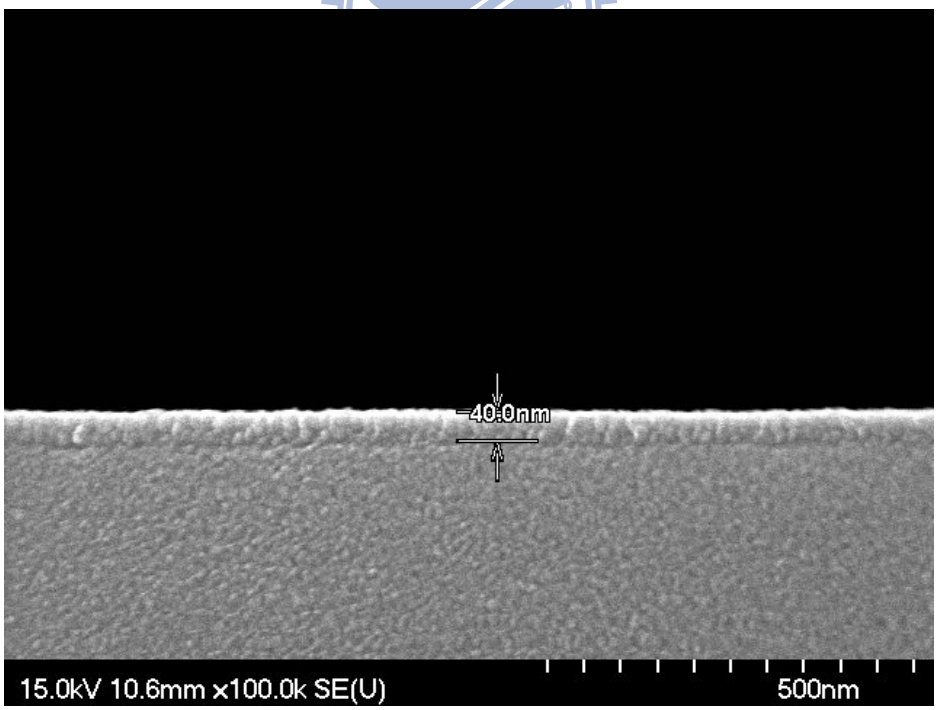
CF_4 plasma treatment, the capacitances of MIM structure because smaller, larger drain current was obtained due to high quality pentacene films on CF_4 plasma. Because the HMDS improves the interface between gate dielectric and pentacene, so CF_4 plasma +HMDS treated on gate dielectrics.

Field effect mobilities were determined from $\sqrt{|I_D|}$ vs V_G curves as shown in Figure 3-13. The field effect mobilities for the device with N_2 annealing, CF_4 plasma and CF_4 plasma +HMDS treated gate dielectric were 1.16×10^{-3}, 1.82×10^{-2}, 2.87×10^{-2} $cm^2/V-S$ respectively. These mobilities are increased after gate dielectric was CF_4 plasma treated. Due to the improvement of carrier transport behavior on pentacene interface of channel/dielectric. Because the fluorine radical repaired the oxygen vacancies and interface states, the electrons would not be trapped easily. The threshold voltage (V_{th}) of pentacene TFTs moved toward a more positive bias with CF_4 plasma +HMDS. Figure 3-14 showed the $\log_{10}(I_D)$- V_G curves, the on/off current ratios for each devices with N_2 annealing, CF_4 plasma and CF_4 plasma +HMDS treated gate dielectric were 1.36×10^3, 1.69×10^4, 4.03×10^4 respectively, which reflected the leakage current results of Figure 3-11. The subthreshold swing (SS) were -353, -286, -266 mV/decade, respectively. The lower has SS the better interface states.

Figure 3-15 showed the contact angle of the HfO_2 treated with (a) N_2 annealing at 150 ℃ for 1 hour, (b) HfO_2 treated with CF_4 plasma, and (c) HfO_2 treated with CF_4 plasma +HMDS. We observed that the HfO_2 treated with CF_4 plasma has smallest contact angle among the three condition. But it still has larger grain size of petacene after pentacene deposit, and has larger field effect mobility. From these result, we can make a conclusion that the grain size of pentacene is not fully dependent on the surface contact angle of gate dielectric.



(a)



(b)

Fig. 3-1 SEM image of HfO_2 (a) without treatment, (b) with CF_4 plasma treatment.

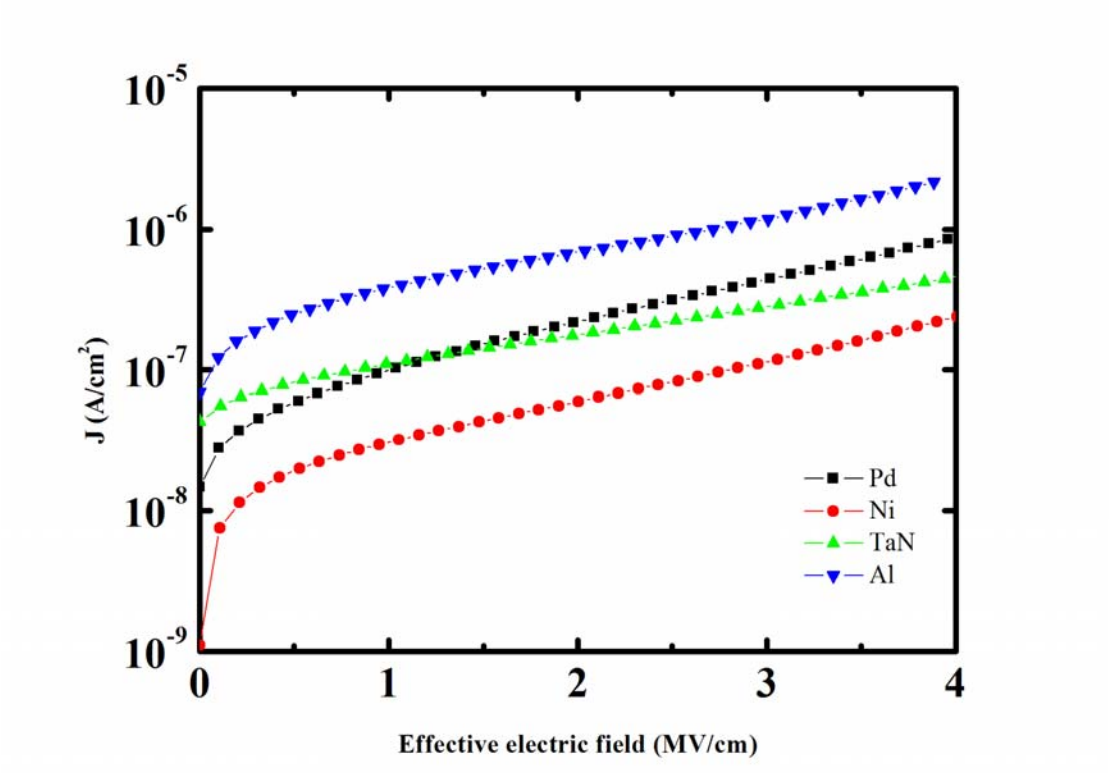


Fig. 3-2 The electronic leakage current characterization of Ni/HfO_2/different bottom electrode MIM with CF_4 plasma treatment.

	Pd	Ni	TaN	Al
C_i (F/cm^2)	3.60×10^{-7}	3.64×10^{-7}	3.78×10^{-7}	3.34×10^{-7}
EOT (nm)	9.59	9.48	9.13	10.3

Table 3-1 The capacitance density and EOT of Ni/HfO_2/different bottom electrode MIM.

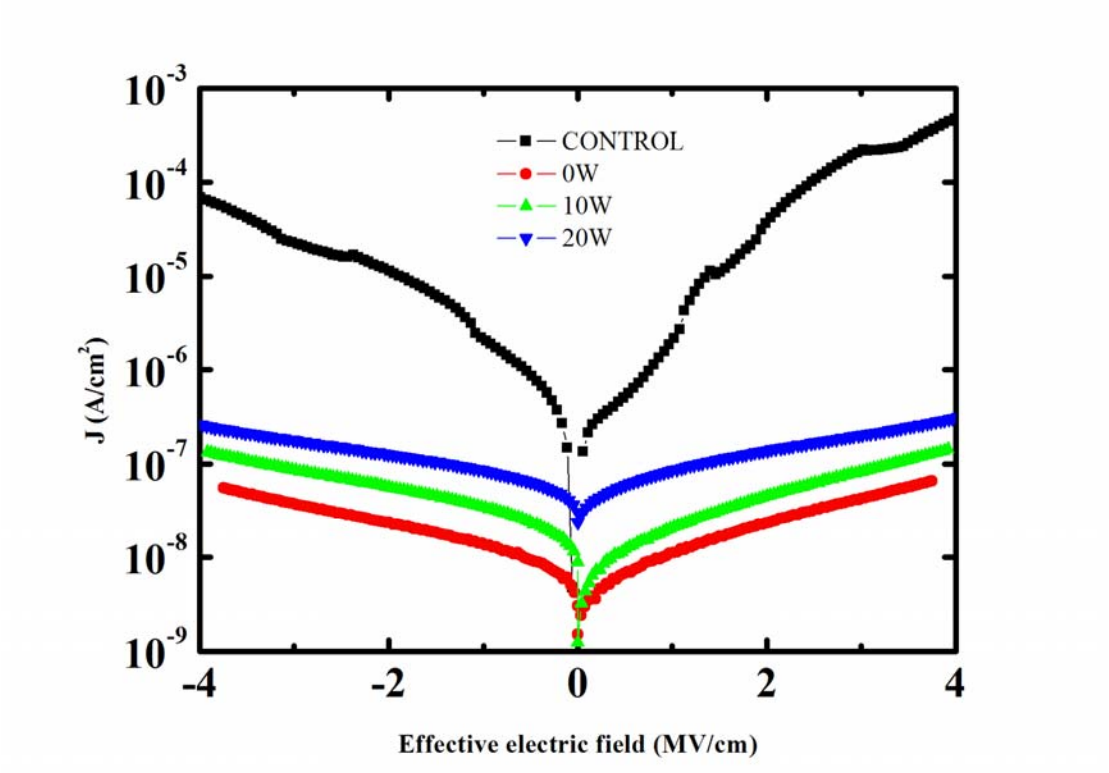


Fig. 3-3 The electronic leakage current characterization of Ni/HfO_2/Ni bottom electrode MIM with different bias of CF_4 plasma treatment.

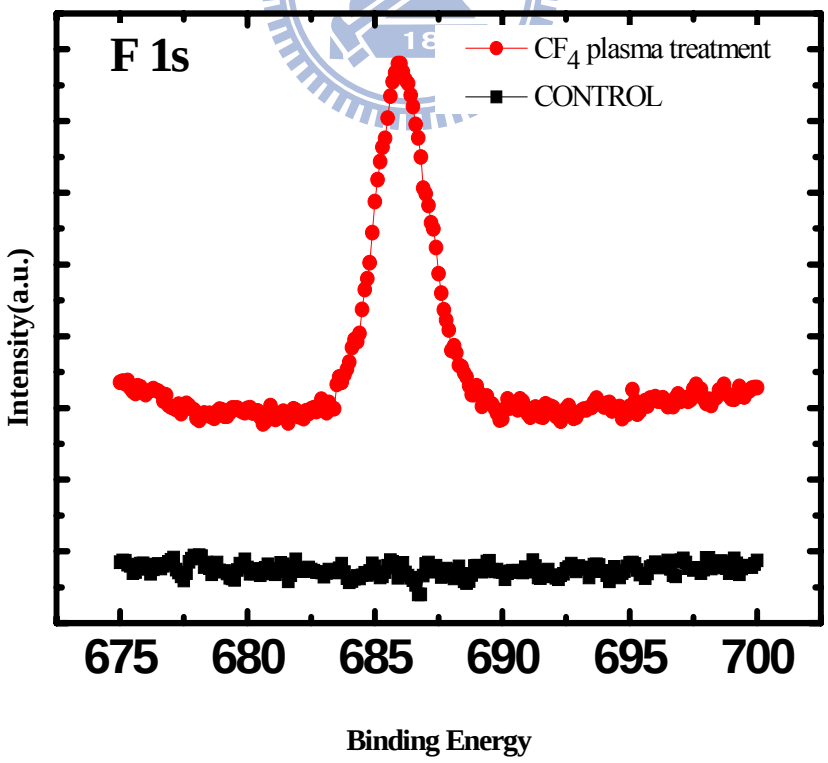
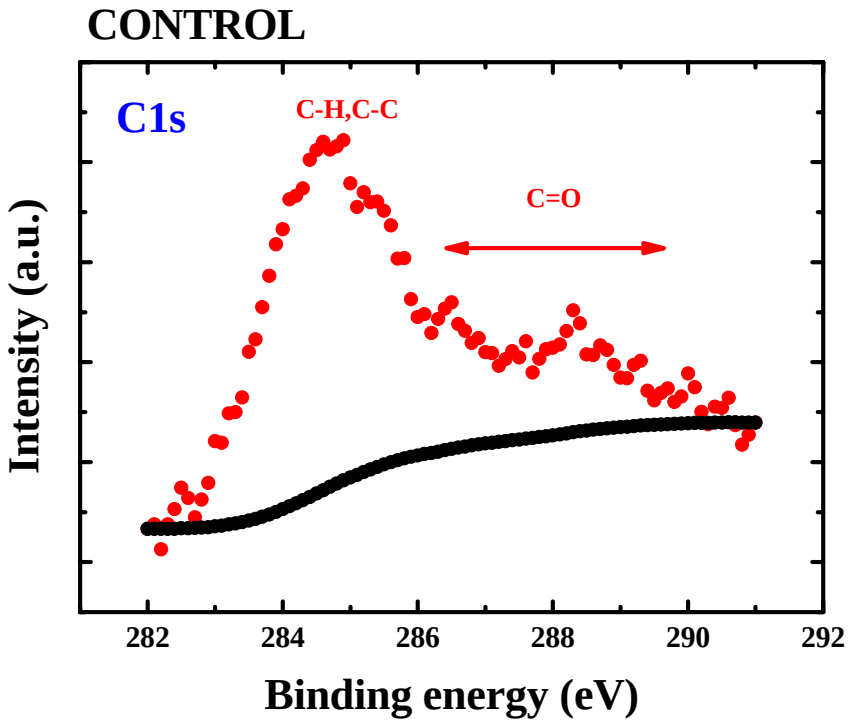
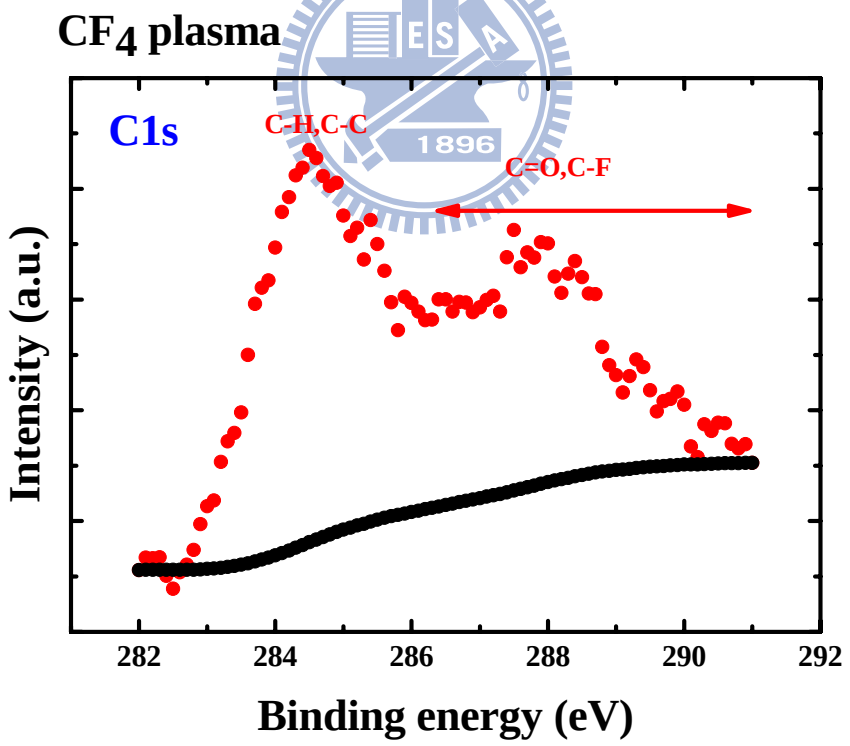


Fig. 3-4 Graph of XPS analysis of "F 1s" of HfO_2/Ni bottom electrode.



(a)



(b)

Fig. 3-5 Graph of XPS analysis of "C 1s" of HfO_2/Ni bottom electrode.

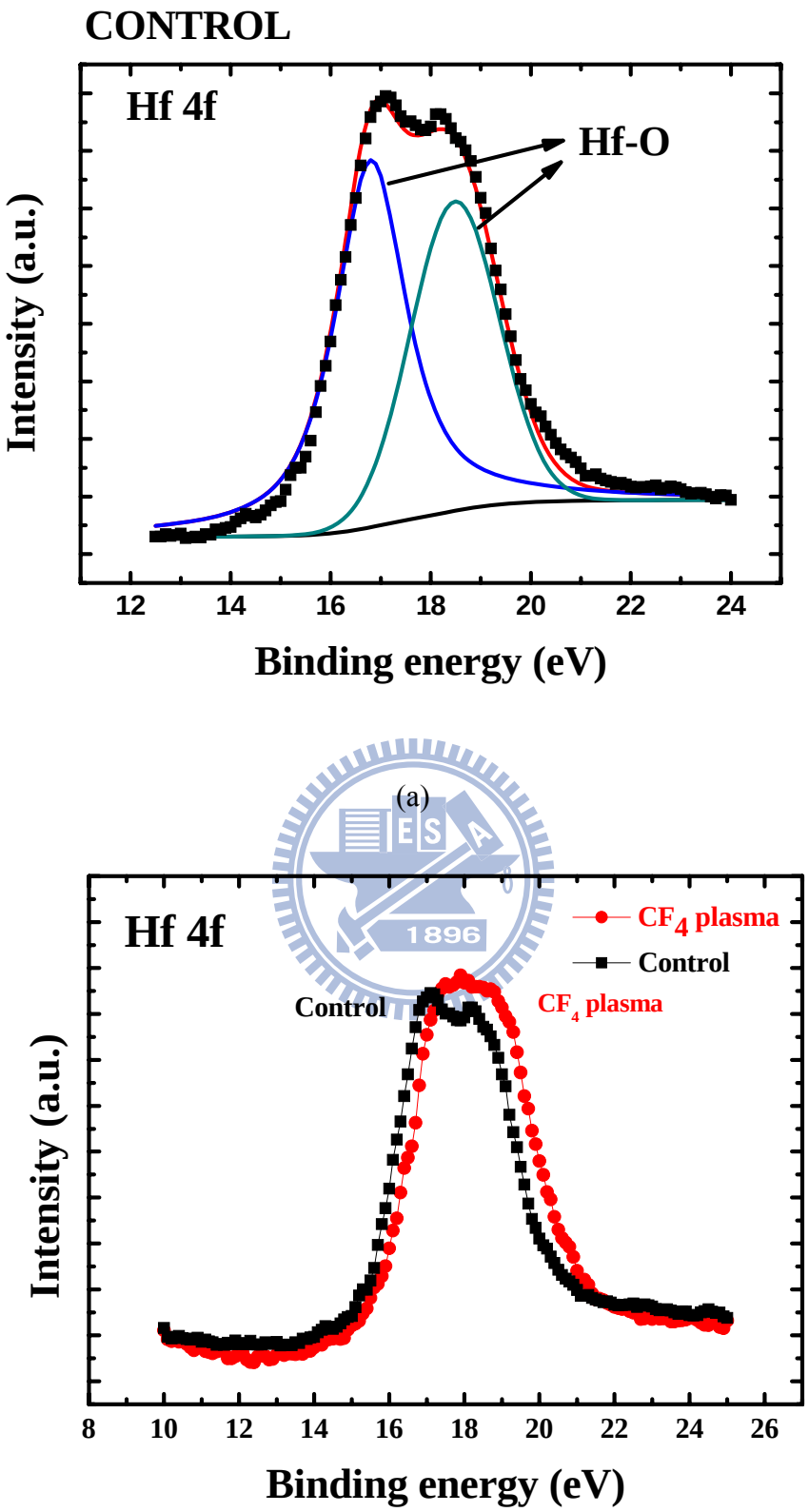


Fig. 3-6 Graph of XPS analysis of "Hf 4f" of HfO_2/Ni bottom electrode.

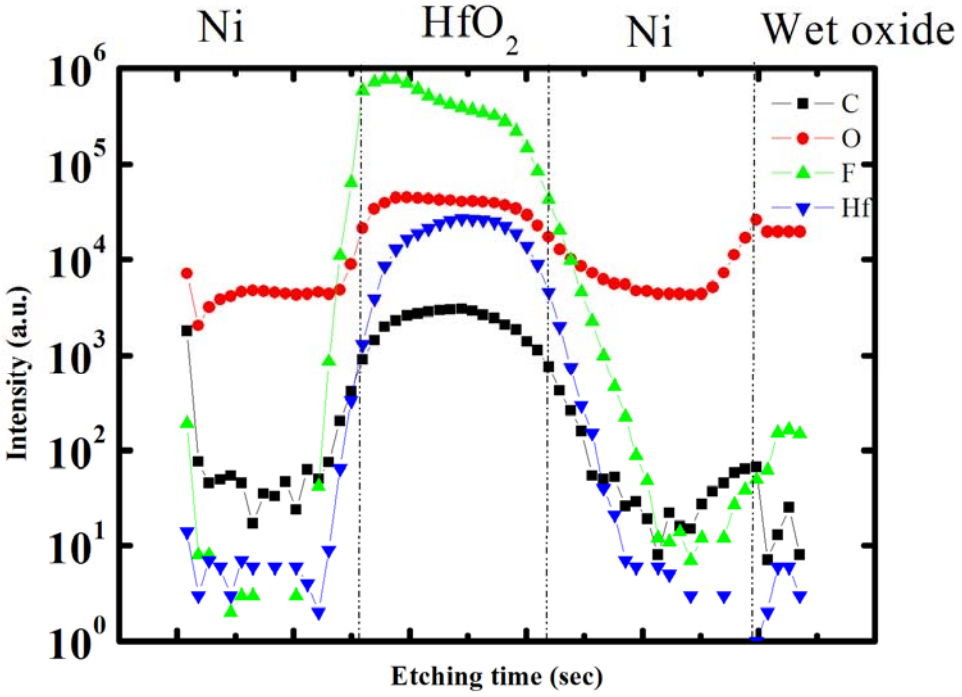


Fig. 3-7 Graph of SIMS analysis of Ni/HfO_2/Ni bottom electrode.

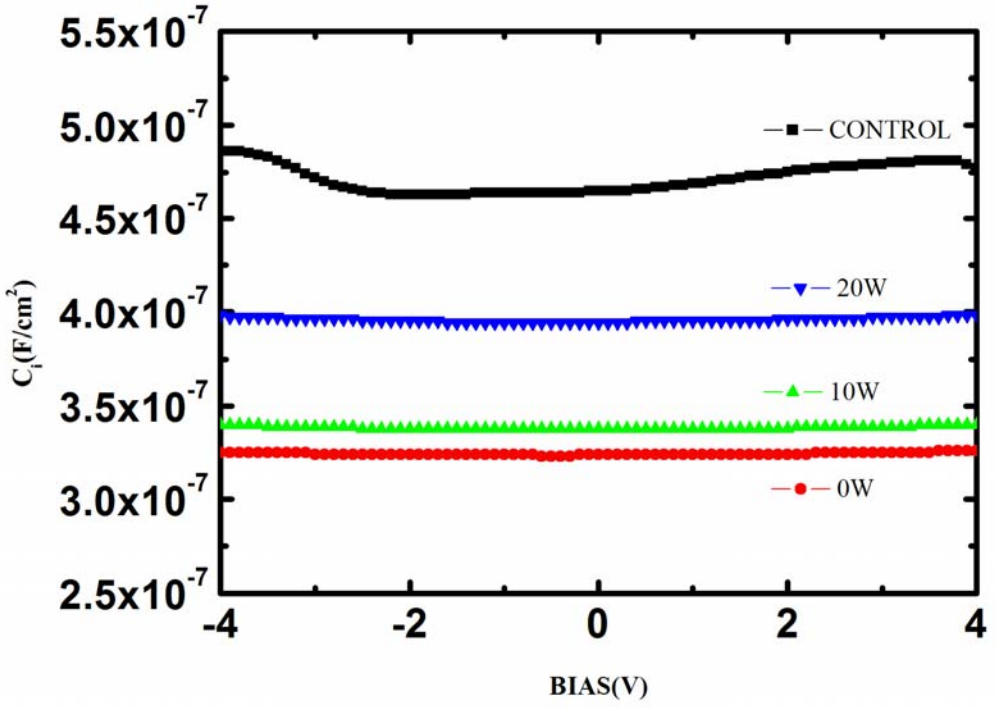
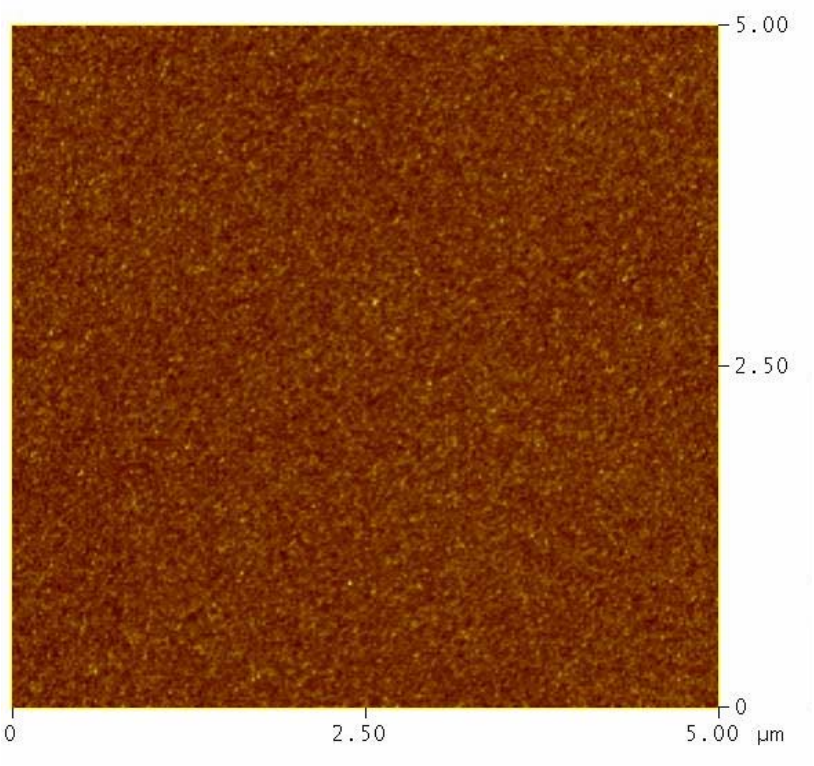
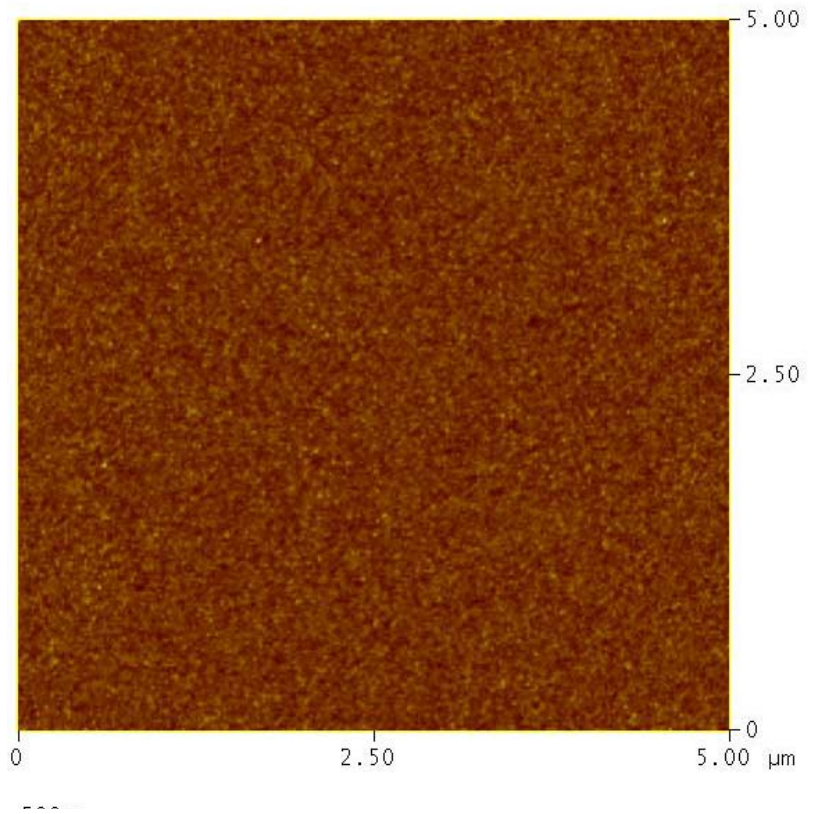


Fig. 3-8 The electronic characterization of Ni/HfO_2/Ni bottom electrode MIM with different bias of CF_4 plasma treatment for C-V.



(a)



(b)

Fig. 3-9 AFM surface image of HfO_2 (a) without treatment which roughness is 0.596nm, (b) with CF_4 plasma treatment which roughness is 0.515nm.

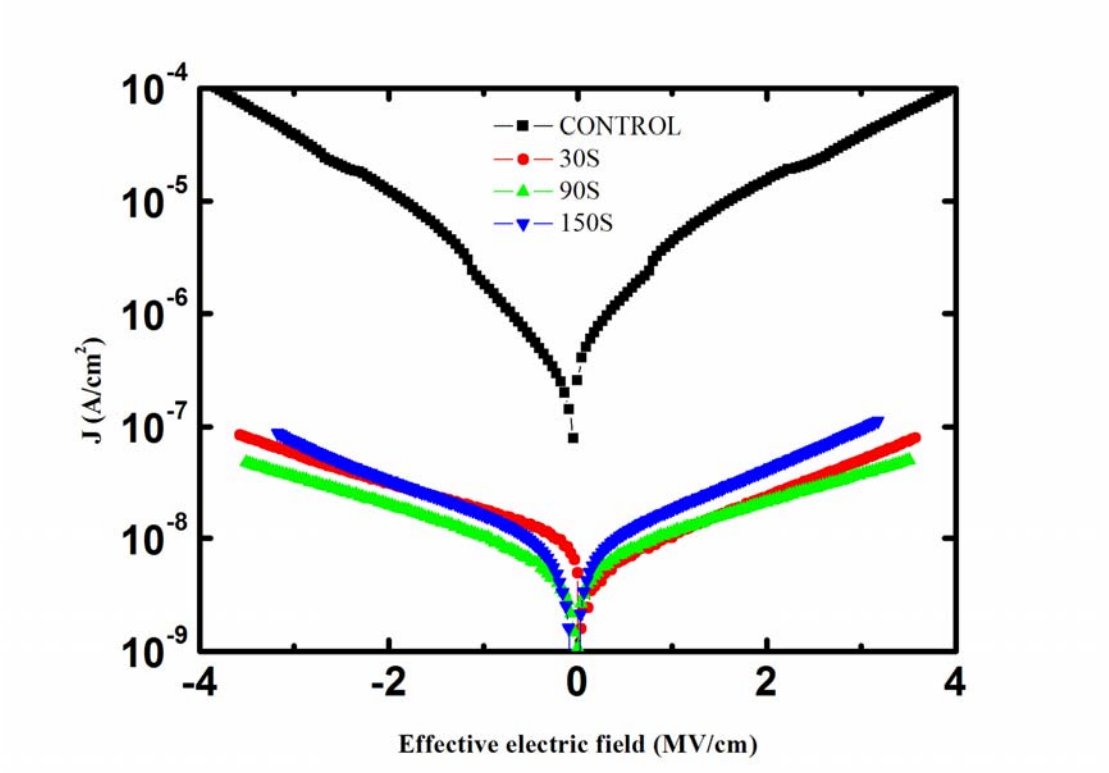


Fig. 3-10 The electronic leakage current characterization of Ni/HfO_2/Ni bottom electrode MIM with different process time of CF_4 plasma treatment.

	CONTROL	30 s	90 s	150 s
C_i (F/cm^2)	3.84×10^{-7}	3.07×10^{-7}	3.03×10^{-7}	2.75×10^{-7}
EOT (nm)	8.99	11.2	11.4	12.6

Table 3-2 The capacitance density and EOT of of Ni/HfO_2/Ni bottom electrode MIM with different process time of CF_4 plasma treatment.

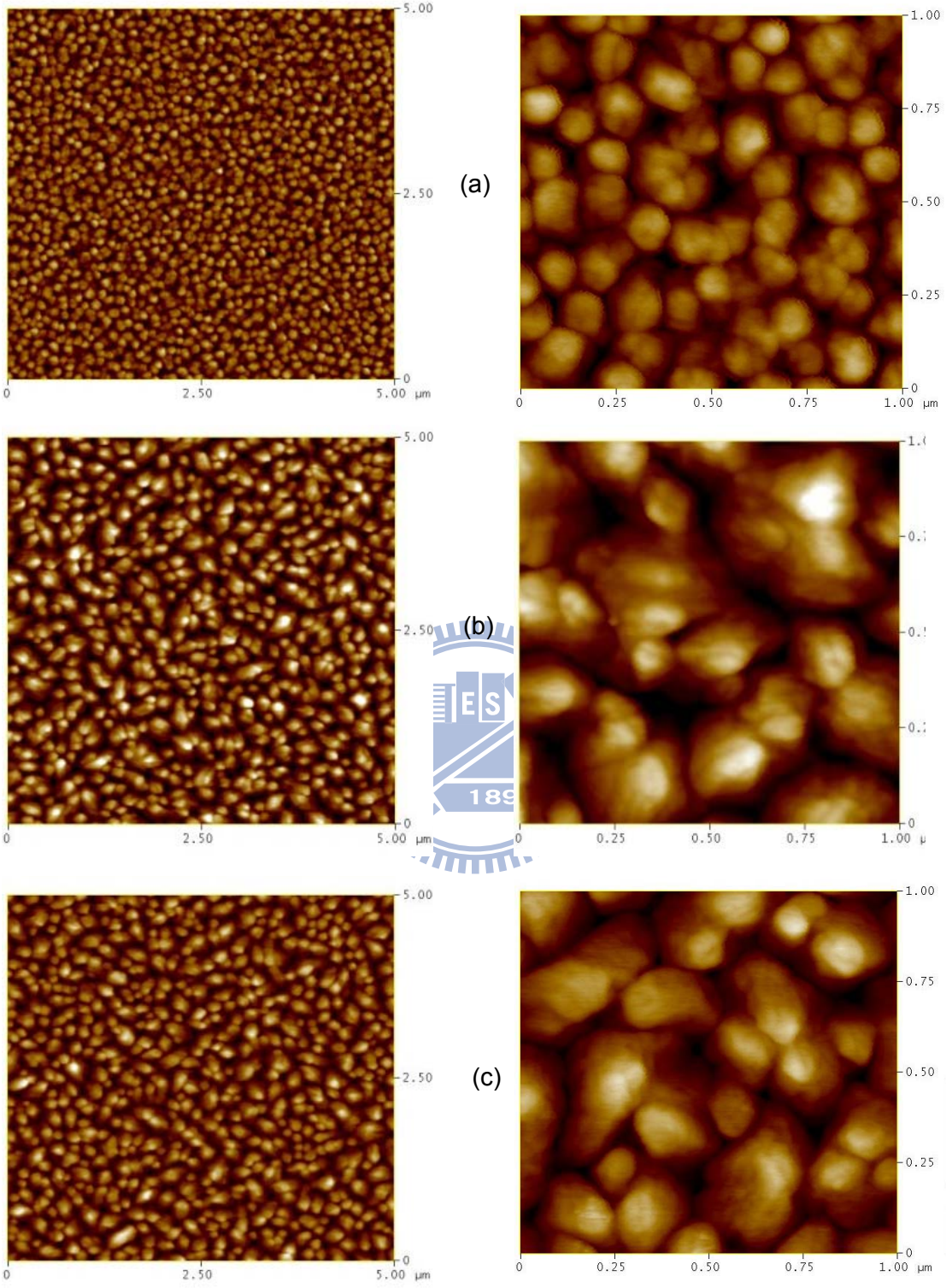
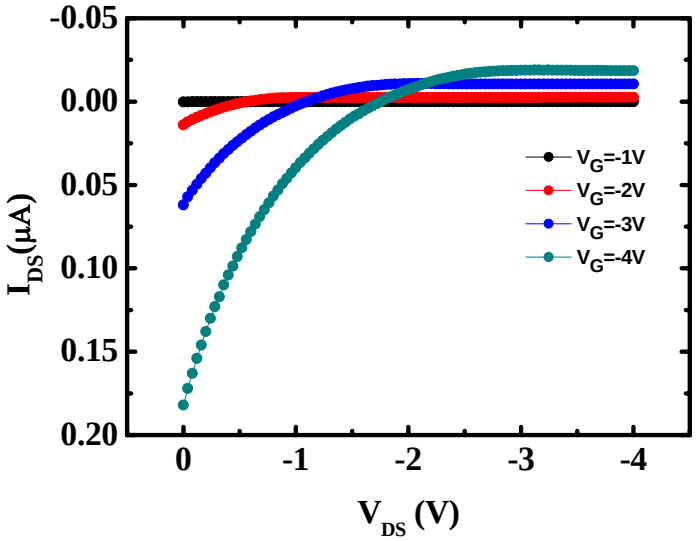
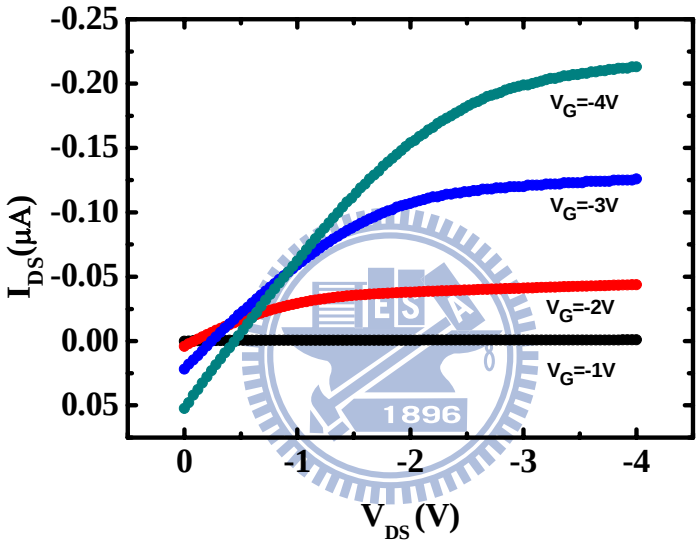


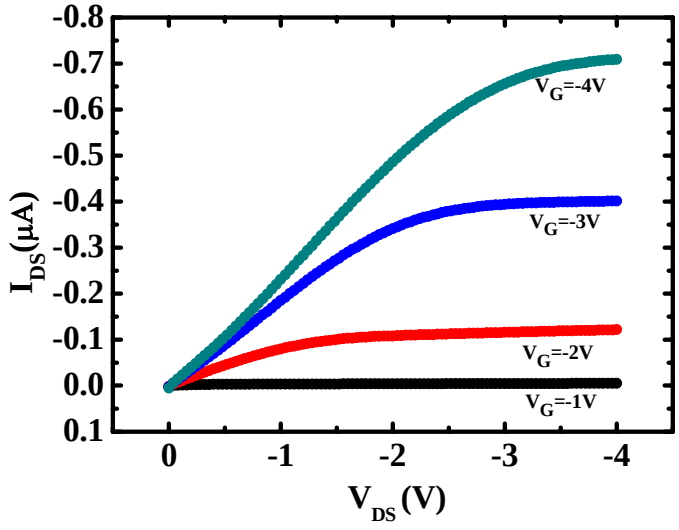
Fig. 3-11 AFM surface images of the HfO_2 treated with (a) N_2 annealing at 150℃ 1 hour , (b) HfO_2 treated with CF_4 plasma , and (c) HfO_2 treated with CF_4 plasma +HMDS and then deposited pentacene which areas are $5\mu m \times 5\mu m$ and $1\mu m \times 1\mu m$.



(a)



(b)



(c)

Fig. 3-12 The electronic characterization of OTFT for I_D - V_D (a) N_2 annealing 1 hour (b) CF_4 plasma treated (c) CF_4 plasma +HMDS treated gate dielectric.

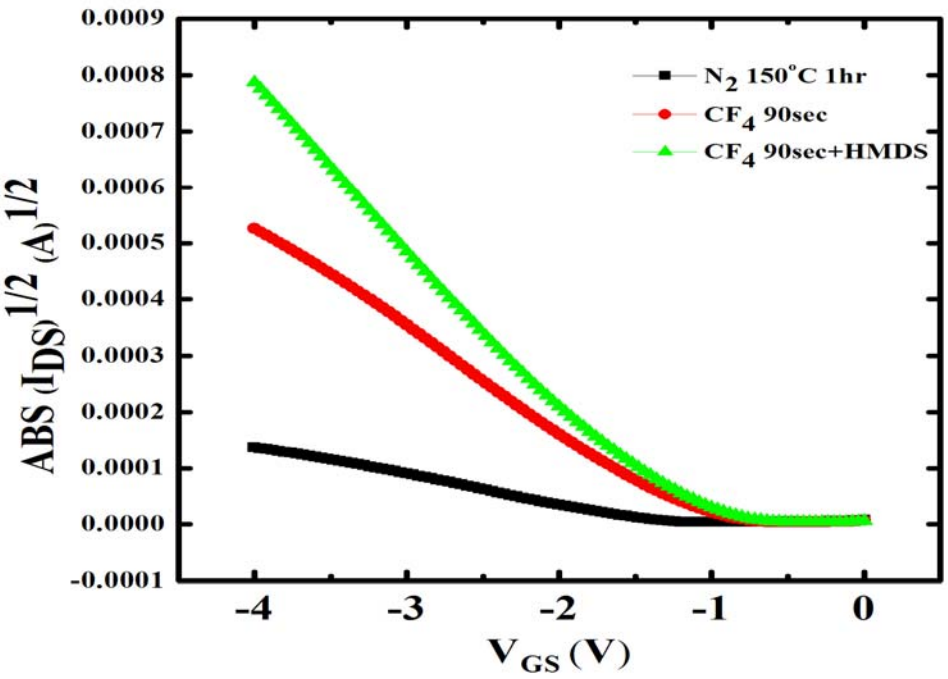


Fig. 3-13 The electronic characterization of OTFT for $\sqrt{|I_D|}$ vs V_G

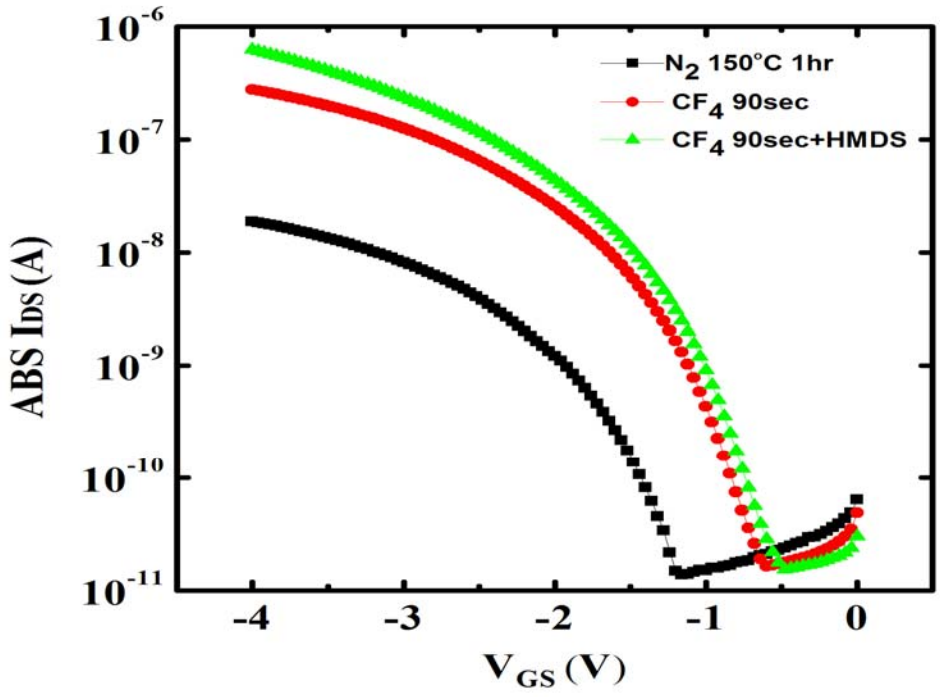
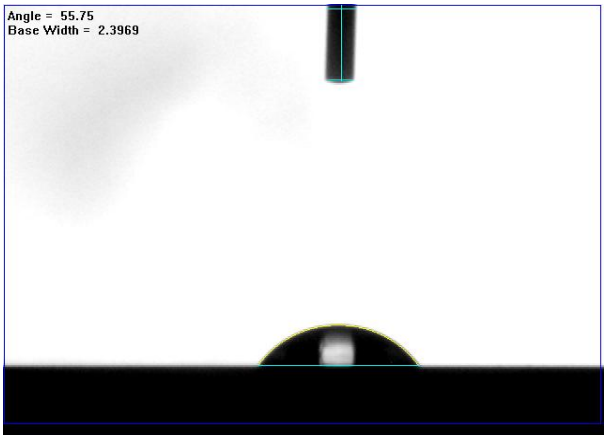


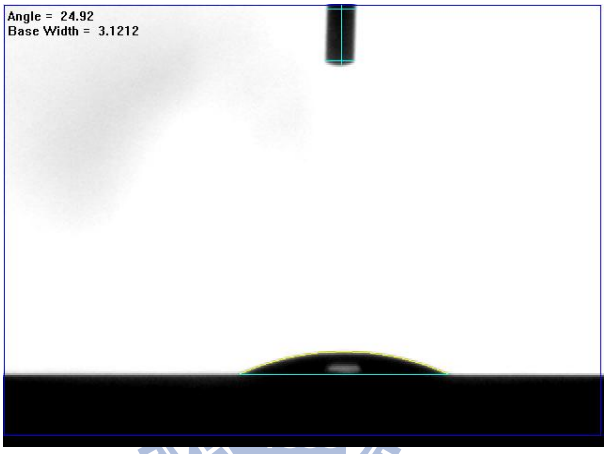
Fig. 3-14 The electronic characterization of OTFT for $\log_{10}(I_D)$- V_G .

Table 3-3 The electronic characteristics of OTFT

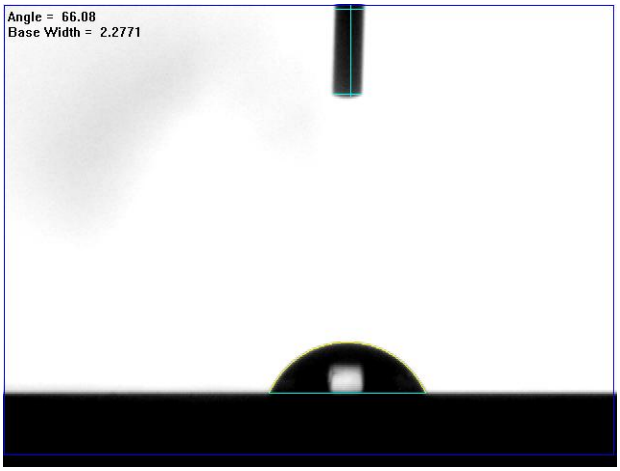
Gate dielectric	Mobility($cm^2/V-S$)	Ion/Ioff	Vth(volt)	SS(mV/decade)
N_2 annealing 1hr	1.16×10^{-3}	1.36×10^{3}	-1.35	-353
CF_4	1.82×10^{-2}	1.69×10^{4}	-1.18	-286
CF_4 +HMDS	2.87×10^{-2}	4.03×10^{4}	-1.12	-266



(a)



(b)



(c)

Fig. 3-15 Contact angle of the HfO_2 treated with (a) N_2 annealing at 150℃ 1 hour was 55.75°, (b) HfO_2 treated with CF_4 plasma was 24.92°, and (c) HfO_2 treated with CF_4 plasma +HMDS was 66.08°.

Chapter 4

Conclusion and Future work

4-1 Conclusion

From the experiment 3-1, we know that the best CF_4 plasma parameters on HfO_2 dielectric layer is CF_4 flow rate = 100 sccm, ICP = 500W, process bias=0W, process time = 90sec, temperature =150℃. The leakage current of HfO_2 based MIM capacitor is $\sim 10^{-7}$ A/cm^2 at $\pm$4MV/cm which is lower than we discussed before. Because it has a good insulator property, we chose to fabricate OTFT device. The pentacene-based OTFTs with HfO_2 gate dielectrics by CF_4 plasma +HMDS treatment has very good device performance such as field effect mobility (maximum of 2.78×10^{-2} cm^2/V-S), a low V_{th} of -1.12V, and on/off current ratios of 4.03×10^4 at -4V gate bias. The results show that fluorine repaires the HfO_2 layer which fabricated with low temperature and the HMDS improves the interface of HfO_2 layer/ pentacene.

4-2 Future work

We can find the suitable polymer which has benzene ring and not reaction with dielectric layer to deposit on HfO_2. And use another gas plasma which such as N_2, NH_3, O_2, etc. to treat the HfO_2 dielectric layer. We also can use the high temperature annealing to find that whether the temperature affect the k-value of HfO_2 layer with CF_4 plasma.

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