## Correspondence

## Probabilistic Modeling and Fault Analysis in Sequential Logic Using Computer Simulation

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#### Abstract

The problem of detecting permanent faults in sequential circuits by random testing is analyzed utilizing a continuous paraneter Markov model. Given a sequential circuit with certain stuck faults specified, the original state table and its error version can be readily derived from an analysis of the circuit under fault-free and faulty conditions, respectively. By simulation of these two tables on a computer, the parameters of the desired Markov model can be obtained. The present approach does not require formulation of a product state table corresponding to the fault-free state table and its faulty version, which is rather difficult while dealing with large circuits. For a specified confidence degree, it is easy to derive the parameters of the model and to calculate either the required lengths of random test patterns or the maximum testing time. A complete mathematical analysis of the model is given that provides some useful insights into the nature of faults in relation to random testing and the associated confidence degree.


## I. Introduction

The increasing complexity of today's digital devices has rendered the problem of fault detection, fault analysis, and test generation [1]-[29] not only an important and indispensable part of the manufacturing and maintenance process but at the same time extremely difficult. The test generation of both combinational and sequential logic circuits can be broadly classified as either deterministic or probabilistic. There are two distinctly different approaches to the problem of fault detection and deterministic test generation in sequential circuits [3]-[10], [22]. The first approach is called the circuit testing approach, which requires an exact knowledge of the circuit realization, and also the faults that can possibly occur. The second approach is called the transition checking approach, which assumes no knowledge whatsoever of the circuit realization, but does assume knowledge of the desired state transitions. In this approach, the investigator just considers the given circuit as a black box, and takes recourse to terminal experimentation based on external observations.
The random test generation techniques that come under the category of probabilistic test generation can reduce computation time and costs, and can be effectively used for fault detection in relatively complex digital systems. Conventionally, in random

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testing, the effect of a failure in a logic network is propagated to the network output by applying random patterns to the primary inputs of the network. By using a simulator, the outputs of the fault-free and faulty networks are then compared. If the comparison fails, the applied random input pattern is retained as a test. For complete fault detection, the experiment is continued until every network fault has been detected by at least one input pattern. The accuracy of the random testing method depends on the length of the applied bit stream; thus it is important to investigate the relationship between the random test length and the associated confidence degree.

The use of probabilistic models to characterize the behavior of digital circuits in the presence of faults was discussed in the literature. Some of these models were introduced for the detection of intermittent faults, while some others were proposed for the detection of permanent or nontransient faults by random patterns. For describing the behavior of circuits with intermittent faults, Breuer [11] introduced a discrete parameter Markov model of first order, whereas Kamal and Page [12] presented a discrete parameter Markov model of zero order, which was subsequently used by Savir [17], and also by Koren and Kohavi [18]. Su et al. [21] proposed a continuous parameter Markov model with two states to characterize the behavior of digital systems in the presence of intermittent faults.
A fault in a digital circuit need not cause an immediate error in the circuit output; there is typically a delay between the occurrence of a fault and the first error to appear in the circuit output. The delay is the error latency of the fault. The error latency is an attribute of the fault; it depends on the circuit, the fault, and the input pattern applied to the circuit. Shedletsky and McCluskey [15] analyzed random testing of digital circuits using the errorlatency model (ELM). This model proved very useful for the analysis of random testing procedures in sequential circuits. In earlier works [13] it was shown that the error latency in combinational circuits in certain cases may be comparable to the mean time between failures (MTBFs): Such a large error latency basically indicates the presence of correct output sequences long after a fault has occurred in a circuit.
When random inputs generated by a stationary multinomial process are applied to a sequential circuit, the probability of the circuit of being in a given state at time $n$ depends only on the state of the circuit at time $n-1$, and the probabilities of the input vectors at time $n-1$. The operation of the circuit under these conditions may be described by a finite, first order Markov process [2], [30], [31]. The Markov process is also ergodic and stationary if the circuit is strongly connected, and the input probabilities do not change with time [15].
A fault occurring in a sequential circuit transforms the state table from the correct version into a faulty version. Any model to determine the error latency of a particular fault must take into consideration the correct behavior of the fault-free circuit as well as the actual behavior of the faulty circuit. A normal procedure is to form a product state table, called ELM state table, using the state tables of the fault-free and faulty circuits. The state diagram corresponding to the ELM state table is next transformed into a Markov chain by assigning probabilities to the different state transitions. An additional absorbing state $S_{+}$is added for the detection of the fault. By calculating the probability distribution function of the error latency of the fault, the relation between the desired quality of test and necessary length of the random test
pattern can be obtained. The ELM is obviously very efficient for small or medium size digital circuits; however, for large digital circuits the ELM approach may prove somewhat difficult because of the complexity involved in generating the product state tables, and forming their corresponding transition matrices.

In this paper the problem of detecting permanent faults in sequential logic circuits by random testing is analyzed utilizing a continuous parameter Markov model with three states. The sequential circuits considered here are deterministic and synchronous, and can be represented by state diagrams with transition assigned outputs, or by equivalent state tables (i.e., Mealy model circuits). The circuits are also assumed to be strongly connected such that there exists a path, not necessarily of length 1 , from any state to any other state.

Given a sequential circuit with certain faults specified, the original state table and its error version can be readily derived from an analysis of the circuit under fault-free and faulty conditions, respectively. By simulation of these two tables on a computer, the parameters of the desired Markov model can be obtained. For a specified confidence degree, it is fairly straightforward to derive the model, and to calculate the lengths of the test-input patterns required for fault detection. Using the model, it is also possible to determine the maximum testing time needed so that the probability of a wrong conclusion is smaller than or equal to some prespecified value $\alpha$. A complete mathematical analysis of the model is given that provides some use, . 1 insights into the nature of faults in relation to random testing and the associated confidence degree. Unlike the ELM approach, the present approach does not require formation of a product state table corresponding to the fault-free state table and its faulty version, which may be rather difficult while dealing with large circuits. The approach is valid for any sequential circuit with faults that result in a deterministic state table. Incidentally, all logical stuck faults in synchronous sequential circuits and certain internal stuck faults in flip-flops that are commonly used as memory devices have this property.

## II. Continuous Parameter Markov Model of a Faulty Sequential Circuit

In order to describe the behavior of a sequential circuit in the presence of a fault while subjected to random inputs, we propose a continuous parameter Markov model with three states designated as: state 0 , state 1, and state 2, as shown in Fig. 1. The state transition probabilities depend linearly on the infinitesimal time step $\Delta t ; \lambda_{i} s$ and $\mu_{j} s$ are the constants of proportionalities. Clearly, these probabilities should increase as the time step $\Delta t$ increases. Once a random pattern is applied, the circuit may stay in any of the aforementioned three states. We assume that the circuit is in state 0 , if the fault exists, but causes no error in the output and state; the circuit is in state 1 , if the fault causes an error output at the output terminals; and the circuit is in state 2 , if the fault causes only error state transition, but no error output results at the output terminals.

To represent the interactions among the three states 0,1 , and 2 for the infinitesimal time step $\Delta t$ in the circuit, we can now define the different state transition probabilities. Let $\operatorname{pr}[(S=x$, $T=t+\Delta t) \mid(S=y, T=t)]$ denote the probability of the circuit staying in state $y$ at time $t$, but going to state $x$ at time $t+\Delta t$. Then we have the following.
$\left.\lambda_{0} \Delta t: \operatorname{pr}[(S=1, T=t+\Delta t)](S=0, T=t)\right]=\operatorname{pr}[($ fault causes an error output at time $t+\Delta t) \mid($ fault causes no error output and error state transition at time $t$ )].
$\lambda_{1} \Delta t: \operatorname{pr}[(S=2, T=t+\Delta t) \mid(S=1, T=t)]=\operatorname{pr}[($ fault causes only error state transition at time $t+\Delta t) \mid(f$ fault causes an error output at time $t)]$.
$\lambda_{2} \Delta t: \operatorname{pr}[(S=0, T=t+\Delta t) \mid(S=2, T=t)]=\operatorname{pr}[(f$ fault causes no error output and error state transition at time $t+$ $\Delta t) \mid($ fault causes only error state transition at time $t)]$.


Fig. 1. Continuous parameter Markov model.
$\mu_{0} \Delta t: \operatorname{pr}[(S=0, T=t+\Delta t) \mid(S=1, T=t)]=\operatorname{pr}[($ fault causes no error output and error state transition at time $t+$ $\Delta t) \mid($ fault causes an error output at time $t)]$.
$\mu_{1} \Delta t: \operatorname{pr}[(S=1, T=t+\Delta t) \mid(S=2, T=t)]=\operatorname{pr}[($ fault causes an error output at time $t+\Delta t) \mid(f a u l t$ causes only error state transition at time $t)]$.
$\mu_{2} \Delta t: \operatorname{pr}[(S=2, T=t+\Delta t) \mid(S=0, T=t)]=\operatorname{pr}[(f$ fault causes only error state transition at time $t+\Delta t) \mid($ fault causes no error output and error state transition at time $t$ )].
$1-\lambda_{0} \Delta t-\mu_{2} \Delta t: \quad \operatorname{pr}[(S=0, \quad T=t+\Delta t) \mid(S=0, \quad T=t)]=$ $\operatorname{pr}[($ fault causes no error output and error state transition at time $t+\Delta t) \mid($ fault causes no error output and error state transition at time $t$ )].
$1-\mu_{0} \Delta t-\lambda_{1} \Delta t: \quad \operatorname{pr}[(S=1, \quad T=t+\Delta t) \mid(S=1, \quad T=t)]=$ $\operatorname{pr}[(f a u l t$ causes an error output at time $t+\Delta t) \mid($ fault causes an error output at time $t$ )].
$1-\lambda_{2} \Delta t-\mu_{1} \Delta t: \quad \operatorname{pr}[(S=2, \quad T=t+\Delta t) \mid(S=2, \quad T=t)]=$ $\mathrm{pr}[($ fault causes only error state transition at time $t+$ $\Delta t) \mid($ fault causes only error state transition at time $t)]$.

Obviously, the parameters of the model depend on the circuit, and faults under consideration. Once we have the fault-free state table of the circuit and its error version corresponding to the faults specified, we may proceed to find all the parameters of the model. A rather simple way is to apply a large number of input patterns to the circuit under test with the occurrence of input signal values 0,1 with a constant probability. Under this condition, the behavior of the circuit may be characterized by a Markov process, and the probability of the circuit staying in a specified state assumes a constant value after long input patterns are applied [2], [15]. This property makes our estimation of parameters approach stable values.
In order to simulate the transition behavior of the circuit in respect of the model, we note that we have nine different counts provided to store the information regarding the circuit after a large number of input patterns are applied. Let $C_{a b}=N$ (circuit going from state $a$ to state $b) ; a=0,1,2 ; b=0,1,2$, where $N$ denotes the total occurrence number or count of the event under reference. Specifically, for example, with $a=2, b=1$, we have: $C_{21}=N($ circuit going from state 2 to state 1$)=N($ fault causing only error state transition in input pattern $r$, while causing an error output in input pattern $r+1$ ). All counts are cleared to zero initially. By using a random number generator we can generate an input value on the interval $[0,1]$, and then apply it to the circuit with a certain constant probability. However, instead of physical inputs to the circuit, we may also simulate the stimulation with respect to the fault-free state table of the circuit and its corresponding faulty table. On comparing the status of these two state tables next on each application of a random pattern, we will

(a)

|  | 0 | 1 |
| :---: | :---: | :---: |
| $Q_{1} Q_{2}$ | 0 |  |
| $00=s_{1}$ | $s_{1}, 0$ | $s_{2}, 0$ |
| $01=s_{2}$ | $s_{1}, 0$ | $s_{3}, 0$ |
| $11=s_{3}$ | $s_{1}, 0$ | $s_{4}, 0$ |
| $10=s_{4}$ | $s_{1}, 0$ | $s_{1}, 1$ |

(b)

(c)

Fig. 2. Example of synchronous sequential circuit with corresponding state table and state diagram. (a) Synchronous sequential circuit. (b) State table $M$. (c) State diagram.
have any of the following three different cases in the compared result.

Case 1 Neither output nor state transition is different, and the circuit is in state 0.
Case 2 Output is different, and the circuit is in state 1.
Case 3 Only state transition is different, but output is not different, and the circuit is in state 2.

The circuit is evidently in state 0 initially, since at the beginning of test no differences ever occurred. After the first random pattern is applied, we compare the outcomes with respect to the two different tables, and then decide upon which one of the aforementioned three cases occurs; the state of the circuit in respect of the current input pattern is thus determined. Assume that on application of the first input pattern we have determined the circuit to be in state $i, 0 \leqslant i \leqslant 2$; then $C_{0 i}=C_{0 i}+1$. Next we

|  | 0 | 1 |
| :---: | :---: | :---: |
| $00=S_{1}$ | $S_{4}, 0$ | $S_{3}, 0$ |
| $01=S_{2}$ | $S_{4}, 0$ | $S_{3}, 0$ |
| $11=s_{3}$ | $S_{1}, 0$ | $S_{4}, 0$ |
| $10=S_{4}$ | $S_{1}, 0$ | $S_{1}, 1$ |

Fig. 3. State table $M^{\prime}$ of sequential circuit of Fig. 2 with the fault $11 / 1$.

TABLE I

| $\mathrm{p}(1)$ | $C_{\mathbf{0 0}}$ | $C_{01}$ | $C_{\mathbf{0 2}}$ | $C_{\mathbf{1 0}}$ | $C_{11}$ | $C_{12}$ | $C_{20}$ | $C_{21}$ | $C_{\mathbf{2 2}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0.1 | 1352 | 0 | 1215 | 848 | 1271 | 1552 | 366 | 2401 | 995 |
| 0.2 | 1163 | 0 | 1679 | 848 | 930 | 1315 | 830 | 2163 | 1072 |
| 0.3 | 1087 | 0 | 2132 | 837 | 593 | 1091 | 1294 | 1928 | 1038 |
| 0.4 | 981 | 0 | 2577 | 766 | 364 | 921 | 1811 | 1687 | 893 |
| 0.5 | 833 | 0 | 2910 | 646 | 193 | 899 | 2264 | 1545 | 710 |
| 0.6 | 602 | 0 | 3310 | 489 | 81 | 844 | 2821 | 1333 | 520 |
| 0.7 | 364 | 0 | 3715 | 297 | 27 | 765 | 3418 | 1062 | 352 |
| 0.8 | 176 | 0 | 4116 | 153 | 5 | 632 | 3962 | 785 | 171 |
| 0.9 | 47 | 0 | 4557 | 40 | 0 | 379 | 4517 | 419 | 41 |

apply the second random pattern to the circuit and determine which state it is in. If it is now in state $j, 0 \leqslant j \leqslant 2$, then $C_{i j}=C_{i j}+1$. This process is repeated until a large number of input patterns are applied to the circuit. Suppose a total of $n$ input patterns are applied. Hence we have

$$
n=\sum_{i=0}^{2} \sum_{j=0}^{2} C_{i j}
$$

Let $p_{i j}$ denote the probability that the circuit is transferred from state $i$ to state $j$ after an input pattern is applied. By law of large numbers [31], we have

$$
\operatorname{pr}\left(\left|C_{i j} / n-p_{i j}\right|<\epsilon\right)=1, \text { as } n \rightarrow \infty, \text { for any arbitrary } \epsilon>0
$$

Example: As an illustration, consider the synchronous sequential circuit as shown in Fig. 2, with its corresponding state table $M$ and state diagram [15].

For the circuit of Fig. 2, if we assume a stuck-at-1 fault in line $L 1(L 1 / 1)$, then the state table $M^{\prime}$ of the circuit subject to this fault can be obtained as shown in Fig. 3. We now simulate the fault-free state table $M$ and its faulty version $M^{\prime}$ on a VAX 11/750 system, and apply random patterns generated by a random number generator to these simulated state tables. After 10001 input patterns are applied, we have the results as given in Table I for the different $C_{i j}$ values with different probabilities of a 1 input, $p(1)$. For each value of $p(1)$, we have chosen a different initial value of the random number generator.

From an analysis of the above results, we may observe that the error estimation is less than $1 \%$. However, if we desire to increase the accuracy of estimation further, we just increase the length of the random test-input patterns.

The transition frequency count is a basic element of parameters inference. If we generate 1000 input patterns per ms, we have the rates (parameters) of our model derived as follows (based on the results of Table I).

$$
\begin{array}{lll}
\lambda_{0}=0.0 / \mathrm{ms} ; & \lambda_{1}=0.844 / \mathrm{ms} ; & \lambda_{2}=2.821 / \mathrm{ms} \\
\mu_{0}=0.489 / \mathrm{ms} ; & \mu_{1}=1.333 / \mathrm{ms} ; & \mu_{2}=3.31 / \mathrm{ms}
\end{array}
$$

The relation between these different parameters and each input vector is stochastically independent under the condition of a
large number of random input patterns and stationary input signal probability assignment.

Once the model is established, and all the parameters of the model are calculated by computer simulation, we can write the undernoted set of differential equations involving the state probabilities, on the assumption that at time $T=0$, the fault causes no error output and error state transition in the circuit:

$$
\begin{aligned}
& d p_{0}(t) / d t=p_{1}(t) \mu_{0}+p_{2}(t) \lambda_{2}-p_{0}(t)\left(\lambda_{0}+\mu_{2}\right), \\
& d p_{1}(t) / d t=p_{0}(t) \lambda_{0}+p_{2}(t) \mu_{1}-p_{1}(t)\left(\mu_{0}+\lambda_{1}\right) \\
& d p_{2}(t) / d t=p_{0}(t) \mu_{2}+p_{1}(t) \lambda_{1}-p_{2}(t)\left(\lambda_{2}+\mu_{1}\right)
\end{aligned}
$$

with $p_{0}(0)=1, p_{1}(0)=p_{2}(0)=0$, and $p_{i}(t)$ being the probability at time $t$ for the circuit of staying in state $i, 0 \leqslant i \leqslant 2$.
After solving this linear, homogeneous system of differential equations, we have

$$
\begin{aligned}
p_{0}(t)= & \left(D_{0} / B\right) u(t) \\
& +e^{-(A / 2) t}\left[\left(\left(B-D_{0}\right) / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} t\right. \\
& +\left(\left(2 B C_{0}-A B-A D_{0}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \left.\cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} t\right], \\
p_{1}(t)= & \left(D_{1} / B\right) u(t)+e^{-(A / 2) t}\left[\left(-D_{1} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} t\right. \\
& \left.+\left(\left(2 B C_{1}-A D_{1}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \sin \left(B-A^{2} / 4\right)^{1 / 2} t\right] \\
p_{2}(t)= & \left(D_{2} / B\right) u(t)+e^{-(A / 2) t}\left[\left(-D_{2} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} t\right. \\
& \left.+\left(\left(2 B C_{2}-A D_{2}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \sin \left(B-A^{2} / 4\right)^{1 / 2} t\right],
\end{aligned}
$$

where

$$
\begin{aligned}
& A= \lambda_{0}+\lambda_{1}+\lambda_{2}+\mu_{0}+\mu_{1}+\mu_{2} \\
& B= \lambda_{0} \lambda_{1}+\lambda_{0} \lambda_{2}+\lambda_{1} \lambda_{2}+\mu_{0} \mu_{1}+\mu_{0} \mu_{2} \\
&+\mu_{1} \mu_{2}+\lambda_{0} \mu_{1}+\lambda_{1} \mu_{2}+\lambda_{2} \mu_{0} \\
& C_{0}= \lambda_{1}+\lambda_{2}+\mu_{0}+\mu_{1}, D_{0}=\lambda_{1} \lambda_{2}+\lambda_{2} \mu_{0}+\mu_{0} \mu_{1} \\
& C_{1}= \lambda_{0}, D_{1}=\lambda_{0} \lambda_{2}+\lambda_{0} \mu_{1}+\mu_{1} \mu_{2} \\
& C_{2}= \mu_{2}, D_{2}=\lambda_{0} \lambda_{1}+\lambda_{1} \mu_{2}+\mu_{0} \mu_{2} \\
& \text { and } u(t)=1, \text { for } t \geqslant 0, u(t)=0, \text { for } t<0
\end{aligned}
$$

Obviously,
$\lim _{t \rightarrow \infty} p_{0}(t)+\lim _{t \rightarrow \infty} p_{1}(t)+\lim _{t \rightarrow \infty} p_{2}(t)=\left(D_{0}+D_{1}+D_{2}\right) / B=1$.
With respect to the term $B-A^{2} / 4$ in the above solutions, we may have three different cases.

Case 1: $B-A^{2} / 4=0$.
In this case, the expressions for $p_{0}(t), p_{1}(t)$, and $p_{2}(t)$ are given as

$$
\begin{aligned}
p_{0}(t)= & \left(D_{0} / B\right) u(t)+\left(\left(B-D_{0}\right) / B\right) e^{-(A / 2) t} \\
& +\left(\left(2 B C_{0}-A B-A D_{0}\right) / 2 B\right) t e^{-(A / 2) t} \\
p_{1}(t)= & \left(D_{1} / B\right) u(t)+\left(-D_{1} / B\right) e^{-(A / 2) t} \\
& +\left(\left(2 B C_{1}-A D_{1}\right) / 2 B\right) t e^{-(A / 2) t} \\
p_{2}(t)= & \left(D_{2} / B\right) u(t)+\left(-D_{2} / B\right) e^{-(A / 2) t} \\
& +\left(\left(2 B C_{2}-A D_{2}\right) / 2 B\right) t e^{-(A / 2) t}
\end{aligned}
$$

Thus, for $B-A^{2} / 4=0$, or $A=2 \sqrt{B}$, the probabilities of the three states converge to their stable values in a nonoscillatory manner very quickly, as depicted in Fig. 4.


Fig. 4. Rapid convergence of state probabilities to their stable values in nonoscillatory manner.

Case 2: $B-A^{2} / 4>0$.
In the present case, damping exists, and $p_{0}(t), p_{1}(t)$, and $p_{2}(t)$ decay exponentially in an oscillatory manner, as shown in Fig. 5.

Case 3: $B-A^{2} / 4<0$.
In this case, the expressions for state probabilities can be derived as

$$
\begin{aligned}
& p_{0}(t)=\left(D_{0} / B\right) u(t)+K_{1} e^{-S_{1} t}+K_{2} e^{-S_{2} t} \\
& p_{1}(t)=\left(D_{1} / B\right) u(t)+K_{1}^{\prime} e^{-S_{1} t}+K_{2}^{\prime} e^{-S_{2} t} \\
& p_{2}(t)=\left(D_{2} / B\right) u(t)+K_{1}^{\prime \prime} e^{-S_{1} t}+K_{2}^{\prime \prime} e^{-S_{2} t}
\end{aligned}
$$

where

$$
\begin{aligned}
S_{1} & =A / 2-\left(A^{2} / 4-B\right)^{1 / 2}, \quad S_{2}=A / 2+\left(A^{2} / 4-B\right)^{1 / 2} \\
K_{1} & =\left(C_{0}-S_{1}-D_{0} / S_{1}\right) / 2\left(A^{2} / 4-B\right)^{1 / 2} \\
K_{2} & =\left(C_{0}-S_{2}-D_{0} / S_{2}\right) /-2\left(A^{2} / 4-B\right)^{1 / 2} \\
K_{1}^{\prime} & =\left(C_{1}-D_{1} / S_{1}\right) / 2\left(A^{2} / 4-B\right)^{1 / 2} \\
K_{2}^{\prime} & =\left(C_{1}-D_{1} / S_{2}\right) /-2\left(A^{2} / 4-B\right)^{1 / 2} \\
K_{1}^{\prime \prime} & =\left(C_{2}-D_{2} / S_{1}\right) / 2\left(A^{2} / 4-B\right)^{1 / 2} \\
K_{2}^{\prime \prime} & =\left(C_{2}-D_{2} / S_{2}\right) /-2\left(A^{2} / 4-B\right)^{1 / 2}
\end{aligned}
$$

Here also the probabilities of the three states converge to their stable values in the same nonoscillatory manner as in Case 1, but at a much slower pace.

From the aforementioned analysis we see that in order for a fault in a circuit to be detected quickly with a constant probability, it is necessary that the parameters or rates of the model should satisfy the condition specified by $B-A^{2} / 4 \geqslant 0$. In case this condition is not met, we have simply to modify our input signal probability assignment for the circuit to change the parameters of the model in a way that will increase the convergence


Fig. 5. Convergence of state probabilities in oscillatory manner.
speed of the state probabilities so that the fault may be detected as fast as possible. The easiest way is to start with a reasonably low value for the input signal probability and then to steadily increase its value until the convergence criterion is met. In each stage, depending on the input signal probability, a new set of Markov parameters will have to be generated and checked to see if the model satisfies the condition $B-A^{2} / 4 \geqslant 0$. In the ideal situation we should have $p_{1}(t)$ as large as possible, and $p_{0}(t), p_{2}(t)$ as small as possible; that is, we have to make $\lambda_{1} \lambda_{2}+\lambda_{2} \mu_{0}+\mu_{0} \mu_{1}\left(D_{0}\right)$, and $\lambda_{0} \lambda_{1}+\lambda_{1} \mu_{2}+\mu_{0} \mu_{2}\left(D_{2}\right)$ relatively small compared to $\lambda_{0} \lambda_{2}+\lambda_{0} \mu_{1}+\mu_{1} \mu_{2}\left(D_{1}\right)$.

To further analyze our model, we may develop transition probabilities among the states. Let $p_{i j}(t)$ denote the probability of going from state $i$ at time $t_{0}$ to state $j$ at time $t_{0}+t$. We can hence write the following sets of differential equations in terms of the state transition probabilities:

$$
\begin{aligned}
& d p_{00}(t) / d t=-\left(\lambda_{0}+\mu_{2}\right) p_{00}(t)+\mu_{0} p_{01}(t)+\lambda_{2} p_{02}(t) \\
& d p_{01}(t) / d t=\lambda_{0} p_{00}(t)-\left(\mu_{0}+\lambda_{1}\right) p_{01}(t)+\mu_{1} p_{02}(t) \\
& d p_{02}(t) / d t=\mu_{2} p_{00}(t)+\lambda_{1} p_{01}(t)-\left(\lambda_{2}+\mu_{1}\right) p_{02}(t)
\end{aligned}
$$

with

$$
p_{00}(0)=1, p_{01}(0)=p_{02}(0)=0
$$

and

$$
\begin{gathered}
p_{00}(t)+p_{01}(t)+p_{02}(t)=1 \\
d p_{10}(t) / d t=-\left(\lambda_{0}+\mu_{2}\right) p_{10}(t)+\mu_{0} p_{11}(t)+\lambda_{2} p_{12}(t) \\
d p_{11}(t) / d t=\lambda_{0} p_{10}(t)-\left(\mu_{0}+\lambda_{1}\right) p_{11}(t)+\mu_{1} p_{12}(t) \\
d p_{12}(t) / d t= \\
\mu_{2} p_{10}(t)+\lambda_{1} p_{11}(t)-\left(\lambda_{2}+\mu_{1}\right) p_{12}(t)
\end{gathered}
$$

with

$$
p_{11}(0)=1, p_{10}(0)=p_{12}(0)=0
$$

and

$$
\begin{gathered}
p_{10}(t)+p_{11}(t)+p_{12}(t)=1 \\
d p_{20}(t) / d t=-\left(\lambda_{0}+\mu_{2}\right) p_{20}(t)+\mu_{0} p_{21}(t)+\lambda_{2} p_{22}(t) \\
d p_{21}(t) / d t=\lambda_{0} p_{20}(t)-\left(\mu_{0}+\lambda_{1}\right) p_{21}(t)+\mu_{1} p_{22}(t) \\
d p_{22}(t) / d t=\mu_{2} p_{20}(t)+\lambda_{1} p_{21}(t)-\left(\lambda_{2}+\mu_{1}\right) p_{22}(t)
\end{gathered}
$$

with

$$
p_{22}(0)=1, p_{20}(0)=p_{21}(0)=0
$$

and

$$
p_{20}(t)+p_{21}(t)+p_{22}(t)=1
$$

The previous sets of equations are obviously isomorphic with the set of equations involving $p_{0}(t), p_{1}(t)$, and $p_{2}(t)$ derived previously. These systems of differential equations can be solved as before. The solutions corresponding to the different sets are as given as follows:
$p_{00}(t)=p_{0}(t), \quad p_{01}(t)=p_{1}(t)$, and $p_{02}(t)=p_{2}(t)$, with the parameters being the same as those in $p_{0}(t), p_{1}(t)$, and $p_{2}(t)$.

$$
p_{10}(t)=p_{2}(t)
$$

with $C_{2}^{\prime}=\mu_{0}, D_{2}^{\prime}=\lambda_{1} \lambda_{2}+\lambda_{2} \mu_{0}+\mu_{0} \mu_{1}$,

$$
p_{11}(t)=p_{0}(t)
$$

with $C_{0}^{\prime}=\lambda_{0}+\lambda_{2}+\mu_{1}+\mu_{2}, D_{0}^{\prime}=\lambda_{0} \lambda_{2}+\lambda_{0} \mu_{1}+\mu_{1} \mu_{2}$,

$$
p_{12}(t)=p_{1}(t)
$$

with $C_{1}^{\prime}=\lambda_{1}, D_{1}^{\prime}=\lambda_{0} \lambda_{1}+\lambda_{1} \mu_{2}+\mu_{0} \mu_{2}$,

$$
p_{20}(t)=p_{1}(t)
$$

with $C_{1}^{\prime \prime}=\lambda_{2}, D_{1}^{\prime \prime}=\lambda_{1} \lambda_{2}+\lambda_{2} \mu_{0}+\mu_{0} \mu_{1}$,

$$
p_{21}(t)=p_{2}(t)
$$

with $C_{2}^{\prime \prime}=\mu_{1}, D_{2}^{\prime \prime}=\lambda_{0} \lambda_{2}+\lambda_{0} \mu_{1}+\mu_{1} \mu_{2}$,

$$
p_{22}(t)=p_{0}(t)
$$

with $C_{0}^{\prime \prime}=\lambda_{0}+\lambda_{1}+\mu_{0}+\mu_{2}, D_{0}^{\prime \prime}=\lambda_{0} \lambda_{1}+\lambda_{1} \mu_{2}+\mu_{0} \mu_{2}$.
As in the case of state probabilities, the condition for rapid convergence to stable values for the state transition probabilities as well depends on the value of $B-A^{2} / 4$. If $B-A^{2} / 4 \geqslant 0$, all of the state transition probabilities quickly converge to their stable values. The result about $p_{00}(t)=p_{0}(t), \quad p_{01}(t)=p_{1}(t)$, and $p_{02}(t)=p_{2}(t)$ appears to be reasonable outcome in view of the assumption that $p_{0}(0)=1$.

## III. Fault Testing Strategy

The faults in a digital circuit are detected by applying test patterns to the primary inputs of the circuit, and observing the output response with respect to these input patterns. In the strategy of random testing, a large number of input patterns are generated randomly. However, if a fault is not sensitive to these generated test patterns, a wrong conclusion may be drawn regarding the existence of the fault. One way to minimize the probability of such a wrong conclusion is to apply a large number of test patterns to the circuit until either the fault is detected, or the confidence about the circuit being error free is larger than or equal to some prespecified value. In order to increase our confidence in the testing procedure, we must therefore minimize the probability that a fault exists, but is not detected.

Assume that the test patterns are applied to the circuit under test (CUT) continuously from time $t_{0}$ to time $t_{0}+s$, and the testing is terminated prior to $t_{0}+s$, if the fault is detected. We determine the maximum testing time $s(\max )$ so that the probability of a wrong conclusion is smaller than or equal to some precalculated value $\alpha$, that is,
$\operatorname{pr}$ (fault exists, but is not detected during the interval $\left[t_{0}\right.$, $\left.t_{0}+s\right] \mid$ fault exists $) \leqslant \alpha$. This probability may be decomposed and expressed as [31]:
$\operatorname{pr}\left(\right.$ fault exists, but is not detected during the interval [ $t_{0}$, $\left.t_{0}+s\right] \mid f a u l t$ exists $)=\operatorname{pr}\left(X \cap Y_{1} \cap Z\right)+\operatorname{pr}\left(X \cap Y_{2} \cap Z\right) \leqslant \alpha$,
where $X, Y_{1}, Y_{2}, Z$ are the events, of which $X$ is fault exists in the circuit, $Y_{1}$ is fault causes no error output and error state transition at time $t_{0}, Y_{2}$ is fault causes only error state transition at time $t_{0}$, and $Z$ is fault causes no error output from time $t_{0}$ to time $t_{0}+s$.

We then have

$$
\begin{aligned}
& \operatorname{pr}\left(X \cap Y_{1} \cap Z\right)+\operatorname{pr}\left(X \cap Y_{2} \cap Z\right) \\
&= \operatorname{pr}\left(Z \mid X \cap Y_{1}\right) \cdot \operatorname{pr}\left(Y_{1} \mid X\right) \cdot \operatorname{pr}(X) \\
&+\operatorname{pr}\left(Z \mid X \cap Y_{2}\right) \cdot \operatorname{pr}\left(Y_{2} \mid X\right) \cdot \operatorname{pr}(X)
\end{aligned}
$$

With reference to our model, we can now compute the aforesaid probabilities as

$$
\begin{aligned}
& \operatorname{pr}\left(Z \mid X \cap Y_{1}\right) \\
& =1-p_{01}(s) \\
& =1-\left[\left(D_{1} / B\right) u(s)+e^{-(A / 2) s}\right. \\
& \cdot\left\{-\left(D_{1} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} s\right. \\
& +\left(\left(2 B C_{1}-A D_{1}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \left.\left.\cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} s\right\}\right] \\
& =\left(\left(B-D_{1}\right) / B\right) u(s)-e^{-(A / 2) s} \\
& \cdot\left\{-\left(D_{1} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} s\right. \\
& +\left(\left(2 B C_{1}-A D_{1}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \left.\cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} s\right\} \text {. } \\
& \operatorname{pr}\left(Z \mid X \cap Y_{2}\right)=1-p_{21}(s) \\
& =1-\left[\left(D_{2}^{\prime \prime} / B\right) u(s)+e^{-(A / 2) s}\right. \\
& \left\{-\left(D_{2}^{\prime \prime} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} s\right. \\
& +\left(\left(2 B C_{2}^{\prime \prime}-A D_{2}^{\prime \prime}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \left.\left.\cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} s\right\}\right] \\
& =\left(\left(B-D_{2}^{\prime \prime}\right) / B\right) u(s)-e^{-(A / 2) s} \\
& \cdot\left\{-\left(D_{2}^{\prime \prime} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} s\right. \\
& +\left(\left(2 B C_{2}^{\prime \prime}-A D_{2}^{\prime \prime}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \left.\cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} s\right\} \text {. }
\end{aligned}
$$

To determine $\operatorname{pr}\left(Y_{1} \mid X\right)$ and $\operatorname{pr}\left(Y_{2} \mid X\right)$, assume that the fault existed for a long time prior to $t_{0}$ so that the circuit is in a stable condition, and the steady state probabilities can be used. Hence

$$
\begin{aligned}
& \operatorname{pr}\left(Y_{\mathrm{I}} \mid X\right)=\lim _{t \rightarrow \infty} p_{0}(t)=D_{0} / B \\
& \operatorname{pr}\left(Y_{2} \mid X\right)=\lim _{t \rightarrow \infty} p_{2}(t)=D_{2} / B
\end{aligned}
$$

Finally, let the $a$ priori probability $\operatorname{pr}(X)=\operatorname{pr}($ fault exists $)=p$.

We have
where

$$
\sin \theta=g_{i} /\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}
$$

and

$$
\cos \theta=h_{i} /\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}
$$

Therefore

$$
-\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2} \leqslant g_{i} \cos \beta+h_{i} \sin \beta \leqslant\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}
$$

$$
\text { for } i=1,2 ;
$$

and

$$
\begin{aligned}
\operatorname{pr}( & \left.X \cap Y_{1} \cap Z\right)+\operatorname{pr}\left(X \cap Y_{2} \cap Z\right) \\
\leqslant & p \cdot\left(D_{0} / B\right) \cdot\left[\left(\left(B-D_{1}\right) / B\right)+e^{-(A / 2) s} \Omega_{1}\right] \\
& +p \cdot\left(D_{2} / B\right) \cdot\left[\left(\left(B-D_{2}^{\prime \prime}\right) / B\right)+e^{-(A / 2) s} \Omega_{2}\right] \\
\leqslant & \alpha, \text { where } \Omega_{i}=\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}, i=1,2
\end{aligned}
$$

Hence

$$
\begin{aligned}
(p / B) \cdot e^{-(A / 2) s} \cdot & {\left[D_{0} \Omega_{1}+D_{2} \Omega_{2}\right] } \\
& \leqslant \alpha-\left(p / B^{2}\right) \cdot\left[D_{0}\left(B-D_{1}\right)+D_{2}\left(B-D_{2}^{\prime \prime}\right)\right]
\end{aligned}
$$

Consequently,

$$
\begin{aligned}
e^{(A / 2) s} \geqslant & \left(D_{0} \Omega_{1}+D_{2} \Omega_{2}\right)(p / B) / \\
& {\left[\alpha-\left(p / B^{2}\right) \cdot\left\{D_{0}\left(B-D_{1}\right)+D_{2}\left(B-D_{2}^{\prime \prime}\right)\right\}\right]=W, }
\end{aligned}
$$

and the testing time required is $s=(2 / A) \ln W$.

$$
\begin{aligned}
& \operatorname{pr}\left(X \cap Y_{1} \cap Z\right)+\operatorname{pr}\left(X \cap Y_{2} \cap Z\right) \\
& =p \cdot\left(D_{0} / B\right) \cdot\left[\left(\left(B-D_{1}\right) / B\right) u(s)-e^{-(A / 2) s}\right. \\
& \cdot\left\{-\left(D_{1} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} s\right. \\
& +\left(\left(2 B C_{1}-A D_{1}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \left.\left.\cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} s\right\}\right] \\
& +p \cdot\left(D_{2} / B\right) \cdot\left[\left(\left(B-D_{2}^{\prime \prime}\right) / B\right) u(s)-e^{-(A / 2) s}\right. \\
& \cdot\left\{-\left(D_{2}^{\prime \prime} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} s\right. \\
& +\left(\left(2 B C_{2}^{\prime \prime}-A D_{2}^{\prime \prime}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \left.\left.\cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} s\right\}\right] \leqslant \alpha . \\
& \text { Put }-D_{i}^{-} / B=g_{i},\left(2 B C_{i}^{-}-A D_{i}^{-}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}=h_{i}, \\
& \left(B-A^{2} / 4\right)^{1 / 2} s=\beta \text {, then } \\
& -\left(D_{i}^{-} / B\right) \cos \left(B-A^{2} / 4\right)^{1 / 2} s \\
& +\left(\left(2 B C_{i}^{-}-A D_{i}^{-}\right) / 2 B\left(B-A^{2} / 4\right)^{1 / 2}\right) \\
& \cdot \sin \left(B-A^{2} / 4\right)^{1 / 2} s \\
& =g_{i} \cos \beta+h_{i} \sin \beta \\
& =\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}\left[\left\{g_{i} /\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}\right\} \cos \beta\right. \\
& \left.+\left\{h_{i} /\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}\right\} \sin \beta\right] \\
& =\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2}[\sin \theta \cos \beta+\cos \theta \sin \beta] \\
& =\left(g_{i}^{2}+h_{i}^{2}\right)^{1 / 2} \sin (\theta+\beta) \text {, }
\end{aligned}
$$

This equation gives us an upper bound of testing time after the parameters of the model and $\alpha$ are determined. The necessary condition for this equation to hold is

$$
\alpha>\left(p / B^{2}\right)\left[D_{0}\left(B-D_{1}\right)+D_{2}\left(B-D_{2}^{\prime \prime}\right)\right]
$$

If it is not satisfied, then no test is needed, because the quality of the circuit is good enough to pass the error probability $\alpha$ without any testing.

For a given circuit, with each line $i$ stuck-at- $k, k=0,1$, we may have the corresponding testing time $s(i, k)$ calculated by the above equation. However, in order to test the circuit for an unknown single fault, we must take

$$
s(\max )=\max _{\text {total lines } i} \max _{k=0}^{1} s(i, k)
$$

If we then apply test-input patterns with testing time at least $s$ (max) to the circuit, we will have the confidence degree $1-\alpha$ that no detection error occurs. The procedure can be applied as well to test any combination of $s-a-0$ and $s-a-1$ faults in the circuit.

## IV. Experimentation

A program was written in Fortran language for VAX 11/750 system to simulate sequential circuits and to derive parameters for a continuous parameter Markov model. The parameters for the Markov model were obtained by varying input signal probability values in a manner such that they meet the required convergence criterion, $B-A^{2} / 4 \geqslant 0$, as derived in the previous section. A simple algorithm for calculating the maximum testing time $s$ (max) as used in the simulation is given below.

## Algorithm for Calculating Testing Time

Step 1: Set the error probability ( $\alpha$ ), total input patterns ( $L$ ) per millisecond, total number of simulation run $(R)$, and the probability of stuck faults $(p)$.
Step 2: For the line i under consideration, assign the probability of the line having logic $0\left(P_{i 0}\right)$ to an initial value (possibly 0 ).
Step 3: Simulate the circuit and perform Transition Frequency Count experiment.
Step 4: Generate the set of Markov parameters $\lambda_{i} s$ and $\mu_{j} s$, and calculate $B-A^{2} / 4$.
Step 5: Vary $P_{i 0}$ in appropriate direction (by varying step sizes, if necessary), and repeat Steps 3 and 4 until $B-A^{2} / 4$ approaches 0 .
Step 6: Calculate the testing time ( $s$ ).
We simulated a simple IC (DM74LS164) for our experiment which is an 8-bit serial in/parallel out shift register, as shown in Fig. 6. This 8 -bit shift register has gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the flip-flop to the low level at the next clock pulse, thus providing complete control over the incoming data. To simplify the simulation, the following input conditions were assumed:

1) Clear was connected to high for bit shift operation, and
2) Serial inputs $A$ and $B$ were tied together to simulate single bit input.

Since $R S$ flip-flops constituted the logic diagram, the case with $R=S=1$ was not allowed. Thus faults with $Q_{i}=1$, for $i=$ $A, \cdots, G$, were considered. For each fault category, the rate of generating the input patterns was fixed at 1000 per ms , and a


| Inputs |  |  |  | Outputs |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Clear | Clock | A | B | $a_{A}$ | $\mathrm{O}_{\mathbf{B}}$ | ... | $a_{H}$ |
| L | X | X | x | L | L | ... | L |
| H | L | X | x | $Q_{\text {AO }}$ | $Q_{B 0}$ | ... | $Q_{\text {H0 }}$ |
| H | $\uparrow$ | H | H | H | $Q_{\text {An }}$ | ... | $Q_{\mathrm{Gn}}$ |
| H | $\uparrow$ | L | X | L | $Q_{\text {An }}$ | ... | $Q_{\mathrm{Gn}}$ |
| H | $\uparrow$ | X | L | L | $\mathrm{Q}_{\text {An }}$ | ... | $\mathrm{Q}_{\mathrm{G} n}$ |

(b)
(a)

(c)

Fig. 6. DM54LS164/DM74LS164 $X$-bit serial in/parallel out shift registers. (a) Connection diagram. (b) Function table where $H=$ high level (steady state), $I=$ low level (steady state), $X=$ dont care (any input. including transitions). $\uparrow=$ transition from low to high level. $Q_{A 0} \cdot Q_{B 0} \cdot Q_{H 0}=$ the level of $Q_{A}, Q_{B}$, or $Q_{H}$, respectively. before the indicated steady-state input conditions were established, and $Q_{A n} \cdot Q_{G n}=$ the level of $Q_{A}$ or $Q_{G}$ hefore the most recent $\uparrow$ transition of the clock: indicales a one-bit shift. (c) Logic diagram (courtesy National Semiconductor Corporation).

TABLE II

| Fault Kind | Simulated Markov Parameters ( per ms) | Maximum Testing Time (ms) |
| :---: | :---: | :---: |
| $Q_{A} / 1$ | $\lambda_{0}=0.0: \lambda_{1}=0.023: \lambda_{2}=0.0 ;$ |  |
|  | $\mu_{0}=0.029: \mu_{1}=0.053: \mu_{2}=0.030$ | 47.35 |
| $Q_{B} / 1$ | $\lambda_{0}=0.0: \lambda_{1}=0.029: \lambda_{2}=0.0$ : |  |
|  | $\mu_{0}=0.038: \mu_{1}=0.068: \mu_{2}=0.039$ | 35.61 |
| $Q_{c} / 1$ | $\lambda_{0}=0.0 ; \lambda_{1}=0.129: \lambda_{2}=0.0$ : |  |
|  | $\mu_{0}=0.205 ; \mu_{1}=0.335: \mu_{2}=0.206$ | 6.41 |
| $Q_{D} / 1$ | $\lambda_{0}=0.0 ; \lambda_{1}=0.161: \lambda_{2}=0.0 ;$ |  |
|  | $\mu_{0}=0.202: \mu_{1}=0.335: \mu_{2}=0.203$ | 7.37 |
| $Q_{E} / 1$ | $\lambda_{0}=0.0: \lambda_{1}=0.329: \lambda_{2}=0.0$ : |  |
|  | $\mu_{0}=0.394: \mu_{1}=0.724: \mu_{2}=0.395$ | 4.17 |
| $Q_{F} / 1$ | $\lambda_{0}=0.0 ; \lambda_{1}=0.592: \lambda_{2}=0.0$; |  |
|  | $\mu_{0}=0.751: \mu_{1}=1.344: \mu_{2}=0.752$ | 1.98 |
| $Q_{G} / 1$ | $\lambda_{0}=0.0 ; \lambda_{1}=1.135 ; \lambda_{2}=0.0$ : |  |
|  | $\mu_{0}=1.354 ; \mu_{1}=2.489 ; \mu_{2}=1.355$ | 1.24 |

$95 \%$ confidence interval for detecting the fault was used. The simulation program estimated the testing time for each kind of stuck fault. The results are summarized in Table II.

## V. Conclusion

A continuous parameter Markov model for detecting permanent faults in synchronous sequential circuits by random testing is proposed in this paper. The developed model and the related mathematical analysis provide some useful insights into the nature of faults in relation to random testing in sequential digital circuits and the associated confidence measure. The approach does not require formation of a product state table corresponding to the fault-free and faulty state tables of the circuit; instead, only the state tables of the fault-free circuit and of its faulty version are required to simulate the behavior of the faults.

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## References

[1] A. Gill, Introduction to the Theory of Finite-State Machines. New York. NY: McGraw-Hill, 1962.
[2] T. L. Booth. Sequential Machines and Automata Theory. New York, NY: John Wiley. 1967
[3] S. C. Lee, Digital Circuits and Logic Design. Englewood Cliffs. NJ: Prentice-Hall. 1976
[4] Z. Kohavi, Suitching and Finite Automata Theory. Second ed. New York, NY: McGraw-Hill, 1978.
[5] P. K. Lala. Fautt Tolerant and Fault Testable Hardware Design. London. UK: Prentice-Hall. 1985.
[6] E. J. McCluskey, Logic Design Principles wizh Emphasis on Testable Semicustom Circuits. Englewood Cliffs. NJ: Prentice-Hall, 1986.
[7] S. H. Unger. The Eissence of Logic Circuits. Englewood Cliffs. NJ: Prentice-Hall, 1989.
[8] A. Miczo. Digital Loogic Testing and Simulation. New York, NY: Harper and Row, 1986.
[9] V. D. Agrawal and S. C. Seth, Test Generation for Vl.SI Chips. Washington. DC: IEEE Computer Socicty Press, 1988.
[10] C. L. Sheng and S. R. Das, "On identification of synchronous sequential machines." Automaticu, vol. X. pp. 357-360, May 1972.
[11] M. A. Breuer, "Testing for intermittent faults in digital circuits," IEEE Truns. Comput., vol. C-22. pp. 241-246, Mar. 1973.
[12] S. Kamal and C. V. Page, "Intermittent faults: A model and a detection procedure." HEEE Trans. Comput., vol. C-23. pp. 713-719, July 1974.
[13] J. J. Shedetsky and E. J. McCluskey," The crror latency of a fault in a combinational digital circuit." in Proc. 5th Int. Symp. Fault-Tolerant Computing. pp. 210-214. June 1975.
[14] J. P. Hayes. "Transition count testing of combinational logic circuits." IE:EE Trans. Compur.. vol. C-25. pp. 613-620. Junc 1976.
[15] J. J. Shedletsky and E. J. MeCluskey, "The error latency of a fault in a sequential digital circuit." HEEE Trans. Comput., vol. C-25. pp. 655-654. June 1976.
[16] S. R. Das. P. K. Srimani and C. R. Datta. "On multiple fault analysis in combinational logic circuits by means of Boolean difference." Proc. IEEEE, vol. 64. pp. 1447-1449. Sept. 1976.
[17] J. Savir. "Optimal random testing of single intermittent failures in combinational circuits." in Proc. 7th Int. Symp. Faudt-Tolerant Compuring. pp. 180-185, June 1977.
[18] I. Koren and Z. Kohavi, "Diagnosis of intermittent faults in combinational networks." IEEE: Trans. Comput, vol. C-26, pp. 1154-1158. Nov. 1977.
[19] K. P. Parker and E. J. McCluskey. "Analysis of logic circuits with faults using input signal probabilities," IEEE: Trans. Compur. vol. C-24, pp. 573-578. May 1975.
[20] . "Probabilistic treatment of general combinational networks," JEEE Trans. Comput, vol. C-24, pp. 668-670. June 1975.
[21] S. Y. H. Su. I. Koren, and Y. K. Malaiya, "A continuous-paraneter Markov model and detection procedures for intermittent faults." WEEV: Trans. Comput., vol. C-27, pp. 567-570, June 1978.
[22] S. B. Akers, "Test generation techniques," Computer, vol. 13. pp. 9-15. Mar. 1980.
[23] R. David and P. Thevenod-Fosse, "Minimal detecting transition sequences: Application to random testing." IEEE Trans. Comput., vol. C-29, pp. 514-518, June 1980.
[24] A. R. Virupakshia and V. C. V. P. Reddy, "A simple random test procedure for detection of single intermittent fault in combinational circuits," IEEE Trans. Comput., vol. C-32, pp. 594-597, June 1983.
[25] J. Savir. "A new empirical test for quality of random integer generators." HEEE Trans. Comput., vol. C-32, pp. 960-961, Oct. 1983.
[26] S. K. Jain and V. D. Agrawal. "Statistical fault analysis." HEEE Design and Test of Computers, vol. 2. pp. 38-44. Feb. 1985.
[27] S. C. Seth. L. Pan and V. D. Agrawal, "PREDICT-Probabilistic estimation of digital circuit testability," in Proc. J5th Int. Symp. FauhtTolerant Computing, pp. 220-225, June 1985.
[28] M. Abramovici and P. R. Menon. "A practical approach to fault simulation and test generation for bridging faults." IFEE: Trans. Comput., vol. C-34. pp. 658-663. July 1985.
[29] K. K. Saluja and R. Dandapani, "An alternative to scan design methods for sequential machines," IEEE Trans. Comput., vol. C-35, pp. 384-388. Apr. 1986.
[30] E. Parzen, Stochastic Processes. New York. NY: Holden-Day. 1962.
[31] I. Miller and J. E. Freund. Probability and Sratistics for lingineers. Englewood Cliffs. NJ: Prentice-Hall. 1977.

## System Lifecurves, Acceptability Regions and Reliability

M. NOVÁK


#### Abstract

The investigation of the relations between the lifecurves population and the acceptability regions of technical system can be used as a basis for the system life expectancy analysis and optimization, which is one of the main components of the system reliability optimization.


## I. Introduction

In almost all areas of engineering activity the considerably large and complicated systems are used. With respect to their physical nature, one can distinguish two fundamental types of systems: the natural systems, and the technical systems.

The natural systems exist independently on the human activity and the research interest is concentrated here to the analysis dominantly.

On the contrary, the technical systems are created by man. Therefore, besides the analysis, before all their synthesis and

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design optimization are in the focus of interest. Let us here concentrate to the technical systems only. Nevertheless, the general idea of the presented approach is applicable also on natural systems, of course often with non neglectable complications caused by their much higher complexity.

Suppose that the fundamental synthesis of technical system was already made.

This means, that such a system is known, which satisfies all the requirements given on the system functional properties. The goal of the subsequent optimization procedure is therefore to improve the system properties with respect to certain one or more secondary (i.e., in the primary synthesis procedure not respected) criterion. Between such criteria, the minimization of production costs and/or maximization of production yield and operation reliability is of highest importance.

Let a technical system, determined by its structure and by the value of the vector $X=\left\{x_{i}\right\}_{N}$ of the corresponding $N$ real system parameters be considered. The properties of this system are represented by the set $F=\left\{F_{k}\right\}_{K}$ of the $K$ system functions $F_{k}$.

For the purpose of this paper the following fundamental presumptions are to be made:

1) Suppose, that for some system the realizations between the set $F$ and the vector $X$ are known, i.e., that the tool $F=f(X)$ for the corresponding system analysis is at disposal (in the form of some set of mathematical formulae, or algorithms, graphs, tables, or any computer-realizable procedure). Therefore, one is able to determine for any point in the $N$-dimensional parameter space $\{X\}_{N}$ the corresponding point on the $K$-dimensional system function surface $\{F\}_{K}$. Further on we shall suppose to deal with such systems only.
2) Suppose further, that for practical use, the system can be considered as well operating, if

$$
\begin{equation*}
F-F_{O} \leqslant \Delta F, \tag{1}
\end{equation*}
$$

where $\Delta F$ is the maximal allowed deviation of the real system properties from the ideal design. In (1), the minus sign can be taken in the strict algebraic sense in the case of real $F$ and $K=1$ only. To the ideal designed system the so called nominal set $F_{O}=\left\{F_{k o}\right\}_{K}$ of $K$ nominal systems functions $F_{k O}$ corresponds, which is in the $N$-dimensional parameter space $\{X\}_{N}$ represented by some nominal vector $X_{O}$, so that

$$
\left.f(X)\right|_{X=x_{o}}=F_{o} .
$$

All the points in $\{X\}_{N}$ satisfying (1) are involved in the region of acceptability $R_{A}$, which is a part of the space $\{X\}_{N}$. The analysis of the shapes and sizes of this regions is one of the most important task of the system parameter tolerance theory. The intensive activity of several dozens authors (see [1]-[10] e.g.) in this field in recent years has caused, that now many useful and powerful computer oriented methods for such analysis are at disposal.

## II. The Concept of the System Lifecurves

Suppose further, that for the system under consideration the analysis of the region of acceptability $R_{A}$ was already made and that its boundaries $\hat{R}_{A}$ in the space $\{X\}_{N}$ are known with satisfactory accuracy. If the system is "well designed", for nominal vector $X_{O}$ corresponding to $F_{O}$ the condition $X_{O} \in R_{A}$ holds. Suppose that more realizations (say $M \gg 1$ ) of such system are considered. Because of the manufacturing imperfections, the properties of these systems will coincide with $F_{o}$ only exceptionally and the points $X_{m}(m=1,2, \cdots, M)$, representing these systems in the space $[X]_{N}$ will differ from $X_{O}$. The points $X_{m}$ are distributed in the region of deviations $R_{E}$, surrounding $X_{O}$, according certain statistical distribution, expressed by the set

