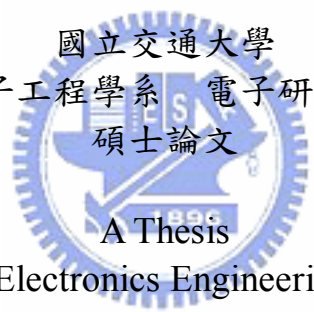
一個可利用在 60GHz 超寬頻系統的全數位式非整數頻率合成器

An All Digital Fractional Frequency Synthesizer for 60GHz UWB System

研 究 生：李彥緯　　Student ： Yen-Wei Lee

指導教授：陳巍仁　　Advisor ： Wei-Zen Chen



國立交通大學

電子工程學系 電子研究所

碩士論文

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics

College of Electrical and Computer Engineering

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

September 2009

Hsin-Chu, Taiwan, Republic of China

中華民國九十八年九月

一個可利用在 60GHz 超寬頻系統之全數位式非整數頻率合成器

研究生: 李彥緯　　指導教授：陳巍仁教授

國立交通大學

電子工程學系電子研究所碩士班

摘要

本論文提出一個可用在 60GHz 超寬頻系統的 40GHz 全數位式非整數頻率合成器。其中，在不使用多模除頻器(Multi-Mode Divider)的狀況下，非整數鎖相功能由一個拉回參考相位積分路徑的回授路徑跟和差調變器(Delta-Sigma Modulator)共同組成，利用此機制可產生涵蓋 37.5 到 45.5GHz 的頻率範圍。且當輸出頻率為 40GHz 時，模擬得到的相位雜訊(Phase Noise)值在頻率偏移為 1MHz 時為-90dBc/Hz。此論文中的晶片是使用 90nm CMOS 技術實現，整體晶片面積為 1.265mm^2，核心電路的部份只佔 0.594mm^2，使用電壓為 1.2V，消耗功率約 52mW。

An All-Digital Fractional Frequency Synthesizer for 60GHz UWB System

Student: Yen-Wei Lee Advisor: Wei-Zen Chen

Department of Electronics Engineering & Institute of Electronics

National Chiao-Tung University

Abstract

A 40 GHz all digital fractional frequency synthesizer for 60GHz UWB system is presented. Without the helping of a multi-mode divider, the fractional phase locking function is achieved by a feedback around the reference integral path and a delta-sigma modulator. In this mechanism, the locking range covers from 37.5 to 45.5GHz. When the output frequency is 40GHz, the simulated phase noise is -90dBc/Hz at 1MHz frequency offset. Implemented in a 90 nm CMOS technology, the core area is only 0.594 mm^2, and the chip size including bonding pad is 1.265mm^2. The ADFPLL core consumes 52mW from a 1.2V supply.

Acknowledgement

終於!!花了兩年的時間，辛苦了無數個白天和夜晚，從一個連什麼是 PLL 都不知道的小毛頭，到現在完成了這部拙作，真是下了不少的功夫。在此，首先要感謝我的指導老師　陳巍仁教授，在這兩年裡面給予我的指導與要求，讓我在這兩年之內成長許多，十分感謝。

這本論文的誕生，說真的，要感謝太多太多的人了。首先要感謝整個研究過程當中給予我最大最大幫助的　楊松諭學長，(簡稱　松諭神，要記得挪抬)，當你還在實驗室時，對於我的諸多問題總是有問必答；即便你已經從實驗室畢業，但當我有任何問題請教你的時候，你還是不厭其煩的寄 e-mail、寫 PDF 檔、甚至是錄下操作影像給予我最完整的幫助。不論是專業還是為人處事上你真的都是我學習的目標，對於你毫不保留的協助我心裡的感謝真的是多到怎麼寫也寫不完，真的是太感謝太感謝你了。接下來則是我們實驗室的第一把交椅-金牌台佑學長，台佑學長不僅教導我很多類比電路的設計概念，還辛苦的陪我 tape out，陪我量測，跟我詳細講解他設計的 DCO 的關鍵部分希望我口試的時候不會被打爆(雖然還是被打爆了 XD)，真的是辛苦你了，心裡的感激也是不知該如何表達。另外，感謝豪哥、巧伶、宗裕、區威、宗恩、國維、塔哥、歐陽、科科以及 527 的各個學長小州哥、老大、宅哥、小凡、邦哥、鴨哥、世範、kila、張錫嘉教授實驗室的玉婷和各位學長、你們在這兩年生活上的陪伴嬉鬧以及在研究裏給予我的幫助，從一開始的設計到晶片的實現、PCB 板的規劃與量測環境的架設，沒有你們的幫助真不知何時還能完成這顆晶片和這篇論文。

接著就是我們廣大的同學群了，現在的室友，想交女友的順天、美食藝術家 kitty，整天嗆我嗆到不行的阿岱爾，跟你們一起住非常的開心，接下來的一年也請多多指教。還有幫愛田由拍照的補刀余祥拳、跟我一起 tape out 到天明的修課達人邱 99、笑聲超機掰的 low low 潮男小云云、好啦下次啦的 rock 阿良、去澎湖後大解放的叔叔阿觀、帥哥肌肉男溫董、每星期準時台中報到的昕爺、常常找不到人的小賴、將為人妻的翁姊、氣

質美女佳琪、台佑閃光筱任謝謝你們這兩年來的陪伴，因為你們讓實驗室裡一成不變的生活變得富饒趣味，你們也是我來實驗室的最大動力，希望大家將來不論研究、工作、生活上都能更進一步。而其他的學弟妹健軒、小毅、書謹、文傑、川毅也希望你們的研究可以順利，找到自己的目標。

另外也要感謝我研究所兩年的室友，曾經的明星外野手金門宅宅宣毅、一起同住六年宿舍然後跟我一樣都是新竹人的完美仁哥、現在住我的宿舍常常靠杯東哥的魔獸宅宅小邱，以及小給外送的老闆（偽）室友什麼都最快的小給、想當韋小寶整天想把正妹的阿扁、來自大甲最近剛交女朋友的家教草莓王大頭、明明是正妹卻交不到男朋友的小路、即將要去德國爽的宜靜還有許許多多族繁不及備載的大學同學群以及球隊的各個學長學弟。這兩年雖然我們不是同班同學了，但我們還是常常一起吃飯聊天打球靠杯，這些生活的點點滴滴為我辛苦的研究生活增加了很多快樂的回憶。在這裡除了恭喜大家順利畢業之外也希望我們依舊能時時連絡，常常出去玩。

此外，要特別感謝陪伴我六年的閃光-于珊，由於你的堅持讓我們實驗室人人都對 open 將的歌朗朗上口，7-11 真該頒個獎給你。也謝謝你這些年來在我不爽的時候聽我鬼叫，謝謝你在我開心的時候跟我分享，謝謝你要常常耐著性子聽我跟你講一堆你聽不懂的鬼東西，因為你的支持讓我更有動力繼續衝下去，謝謝你！還有謝謝在背後默默支持我的家人，老爸老媽你們辛苦了，謝謝你們平時為我和妹妹所做的一切，謝謝你們，你們的支持是我前進的動力。最後，還是不得不說，一份作品的完成真的需要許多人不論實質上或是精神上的幫助，總體說來，得知於人者太多，出之於己者太少，感謝之情，無由表達。要感謝的人真的太多了，所以說，不如謝天吧！

李彥緯 09, Sep, 2009

Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 Motivation

1.1.1 Target Application and its Requirement

Because of the huge progress of the techniques of high definition (HD) image, HD television and HD digital camera become more and more popular; therefore, the technology of HD data transmission turns into the next important competition point and the requirement of it also becomes higher and higher. Fig. 1-1 shows the concept of a digital family.

Digital family is the concept of the connection of all digitalized electronics in the house through internet. In this definition, the main idea of digital family is utilizing the architecture of broadband internet to integrate all 3C termination products in the family. Through this way, all 3C products can share the digitalized

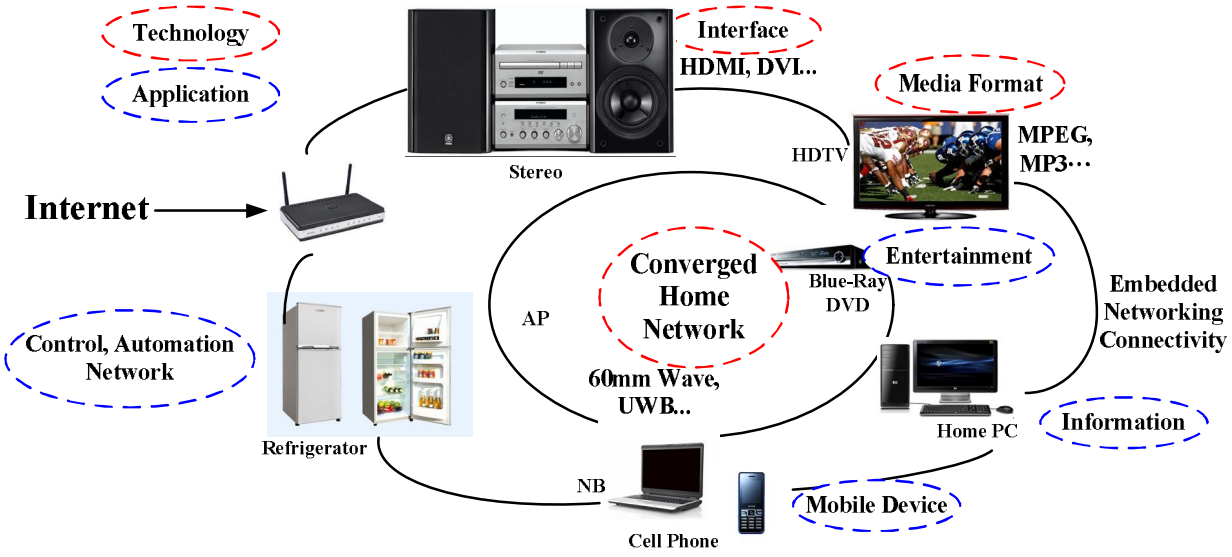


Fig. 1-1 Concept of a digital family

data, so the users can enjoy any content, any time, any where through any device.

Therefore, the dream of digital family can be simply described as the two prime ideas, connecting everything and computing everywhere. In other words, no matter where the users are, they can use monitors, displays, or portable devices to communicate with family central server through the internet to control any digital electronics in the house or download the wanted digitalized content, such as MP3 music, high class MP4 video, or the HD image of ball games which are transmitted from the satellites. However, compare with the wire communication in which most people believe High-Definition Multimedia Interface (HDMI) is the best solution, in order to make "uncompressed" HD signal transmission possible in wireless communication, the researches and progresses of broadband wireless transmission turn into very important.

Because there is no official specification in wireless HDMI, the implementation totally depends on the design houses and research centers. Consider the techniques and the restriction of different countries, 60GHz mm-Wave, MIMO technique in IEEE 802.11n, and ultra-wideband (UWB) are the only three technologies which are possible succeed in this tangled warfare. The maximum data transmission rate of each technology shows in Table 1-1. However, IEEE 802.11n overlaps the 2.4GHz frequency band of Bluetooth and, in this band, there is interference problem between it and microwave ovens. As

Property of 60GHz mm-Wave、802.11n and UWB

Technology	Maximum Data Transmission Rate
60GHz mm wave	2,500Mbit/s
IEEE 802.11n	600Mbit/s
UWB	480Mbit/s

Table 1-1 Maximum data transmission rate of different technologies

802.15.3C Specification			
CHNL_ID	**Center frequency**	**Low frequency**	**High frequency**
1	58.32G	57.24G	59.40G
2	60.48G	59.40G	61.56G
3	62.64G	61.56G	63.72G
4	64.80G	63.72G	65.88G

Table 1-2 Maximum data transmission rate of different technologies

for UWB, there is also interference problem when 5GHz wireless internet and UWB are used at the same time. Contrast with the two technologies, for 60GHz mm-Wave, there are not only no doubt about interference problem but also no license restriction in most countries; therefore, we choose 60GHz mm-Wave as our research direction.

Table 1-2 shows the target specification in 60GHz mm-Wave of IEEE 802.15.3C for personal area network (PAN). In this specification, the frequency band from 57.42 to 65.88GHz is divided into 4 channels, and the central frequency of each channel are 58.32, 60.48, 62.64, and 64.80 GHz. A conventional down conversion receiver is illustrated in Fig. 1-3.

Fig. 1-3 shows the architecture of a conventional down conversion receiver. In the system, the antenna receives the signal and sends the signal into a band-pass filter (BPF) and low-noise amplifier (LNA). After passing through the filter and amplifier, the signal is separated into IQ paths. Meanwhile, a frequency synthesizer generates the required carriers for each channel, and then the mixers in the IQ paths will mix the received signal with a 60GHz carrier and convert the received signal down to the baseband. However, it is hard to implement a suitable frequency synthesizer because the frequency synthesizer must generate the carriers which are centered at 60GHz and covered about 7GHz range. Therefore,

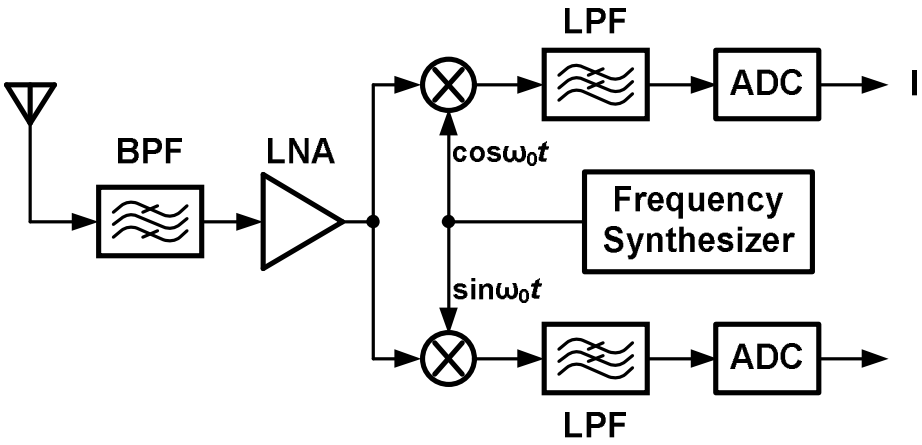


Fig. 1-3 Conventional down conversion receiver

in order to implement a suitable receiver for 60GHz mm-Wave system, a heterodyne receiver is chosen and is illustrated in Fig. 1-2.

In this heterodyne receiver, the antenna also receives the signal and the signal goes through the BPF, the LNA, and three mixers. The first mixer mixes the received signal with a 40GHz carrier, LO1, and then separates the mixed signal into IQ paths. Finally the second and the third mixer in I and Q path, respectively, mix the signal with a 20GHz carrier, LO2, and convert the received signal down to the baseband. In this architecture, the difficulty in the implementation of the frequency synthesizer is highly lowered because the

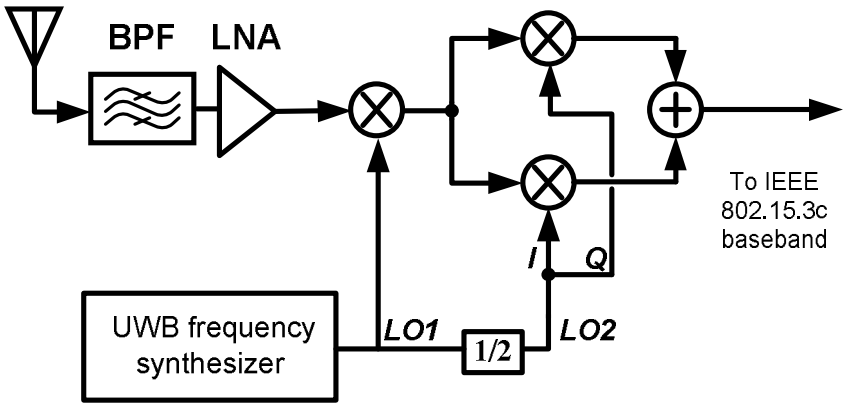


Fig. 1-2 Conventional down conversion receiver

802.15.3c Specification			
CHNL_ID	**Center frequency**	**LO 1**	**LO2**
1	58.32G	38.88G	19.44G
2	60.48G	40.32G	20.16G
3	62.64G	41.76G	20.88G
4	64.80G	43.20G	21.60G

Table 1-3 Central frequencies of LO1 and LO2 in each channel

frequency synthesizer in the heterodyne receiver only has to generate about 40GHz carriers, LO1, and then the receiver will get LO2 by down converting LO1 by 2. Table 1-3 shows the central frequencies of LO1 and LO2, which are 2/3 and 1/3 of the central frequency of each channel, respectively.

1.1.2 Introduction of the Integer-N and Fractional-N Frequency Synthesizers

Frequency synthesizers are the key building blocks for most of the modern electronic and communication systems, including radio receivers, mobile telephones, and satellite receivers. In wireless systems, the fractional-N frequency synthesizer is much more important because it can both generate a high frequency signal with a well-defined frequency and modulate that signal. No matter the integer-N or the fractional-N frequency synthesizer, the basic goal of a frequency synthesizer is to generate a periodic signal with a given frequency and phase relationship with respect to a reference signal. The generated clock signal can be served as clock source for processors, transmit clock in high speed data interfaces, sampling clock for analog to digital converter, and local oscillator signal for wireless transceiver which mixes the signal of interest to a different frequency. Many approaches of frequency synthesizers have been devised over

the years, such as phase-locked loops (PLLs), direct digital synthesis (DDS), and frequency mixing. Among different approaches of frequency synthesizer, most state of the art high-performance frequency synthesizers are based on the phase-locked loops technique.

A phase-locked loop is a frequency control system with negative feedback. By sensing the phase difference between the feedback path of a controlled oscillator and the input reference signal, a PLL generates a signal with the phase that has a fixed relation to the phase of a reference signal. It responds to both the frequency and the phase of the reference signal and automatically raises or lowers the frequency of a controlled oscillator until output signal is matched to the reference in both frequency and phase. A PLL can be used to generate a signal, modulate or demodulate a signal, reconstitute a signal with less noise, or multiply or divide a frequency.

The basic structure of an integer-N phase-locked loop is illustrated in Fig. 1-4 [1], which consists of a controlled oscillator, a phase frequency detector, a loop filter, and a feedback frequency divider. In this architecture a controlled oscillator generates a periodic signal with a frequency f_{OUT} determined by the value of controlled oscillator input. The output clock is divided by a feedback frequency divider having a frequency $f_{FB}=f_{OUT}/N$, where N is the divided ratio of

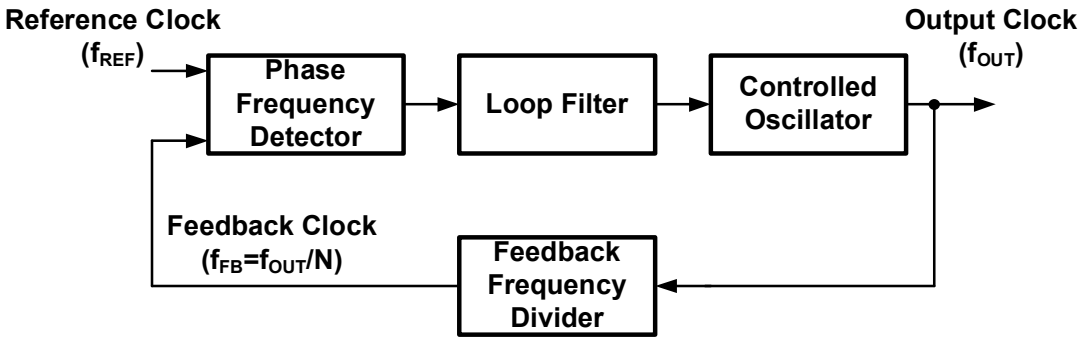


Fig. 1-4 Block diagram of an integer-N phase-locked loop

the frequency divider and it is an integer. A phase frequency detector compares the phase or frequency difference between the feedback clock and a reference clock, having a frequency f_{REF}. The output signal of phase frequency detector which carries the frequency or phase error information is then processed by a loop filter. The abrupt changes in the error information generated by phase frequency detector are then smoothed out by loop filter. Finally, the output of the loop filter feeds to the controlled oscillator and adjusts the frequency f_{OUT} of the output clock. The loop reaches a steady state condition where $f_{OUT}=f_{REF}N$, and the given relationship between the output clock and reference clock is established if the loop is properly designed.

As for the fractional-N phase-locked loop, an introduction to integrate ΣΔ modulator in frequency synthesis can be found in [2], and a basic structure of a conventional fractional-N PLL is shown in Fig. 1-5. This architecture is popular because most of the required signal processing for control can be done in digital domain. Actually, the total operation of a fractional-N frequency synthesizer is similar to that of an inter-N frequency synthesizer, but the divided ratio is no longer an integer-N but a fractional number N.f, which means the output clock is divided by a feedback frequency divider to have a frequency $f_{FB}=f_{OUT}/N.f$.

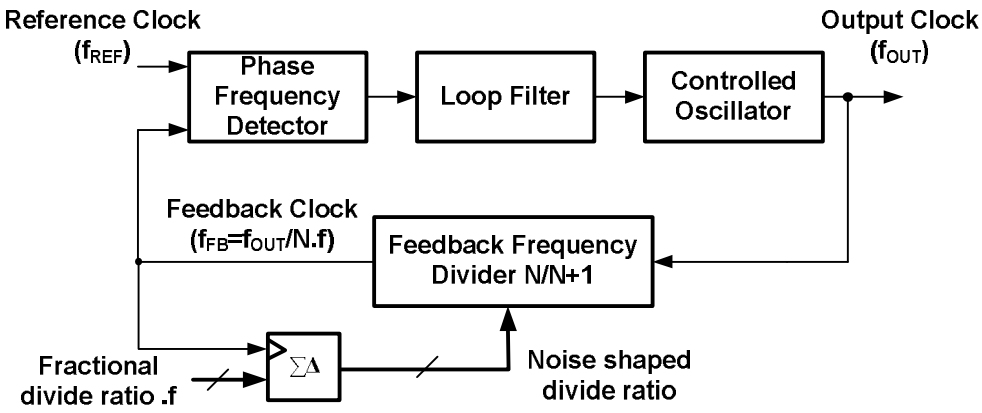


Fig. 1-5 Block diagram of a fractional-N phase-locked loop

Nevertheless, no matter the integer-N or fractional-N PLL, the design of the CMOS integrated PLL based RF synthesizers remains one of the most challenging tasks in communication systems because they must meet the strict requirements of low-cost, low-power, monotonic implementation while also meeting the noise and transient specifications. In general, a frequency synthesizer design can be evaluated by the following considerations: Phase noise or jitter performance, spurious noise performance, frequency hopping speed, tuning bandwidth, rejection of supply or substrate noise, chip area, power consumption and portability for the design to transfer to a different technology node. However, there exist complicated design trade-offs among these criteria mentioned above. Therefore the requirements that a synthesizer must fulfill depend heavily on the specific application.

The conventional PLL based RF synthesizer is usually made as an analog building block. As the feature size of the CMOS technology becomes smaller, the low-voltage deep-submicrometer digital CMOS process allows more and more digital circuits to be integrated in a single ship with higher operation frequency while consuming less power due to smaller parasitic capacitance and lower supply voltage. The analog circuits, however, does not benefit much from the scaling of the CMOS devices. Indeed, the small voltage headroom, high leakage current and the noisy environment on a SOC make the design of high-performance synthesizers more and more difficult. Thus, many research efforts recently focus on the digitally intensive or digitally assisted approach of the RF synthesizer[3]-[5].

However, for integer-N PLL, the smallest frequency space of output clock is the frequency of the reference clock, f_{REF}. In order to exactly control the frequency of output clock, a quite low reference frequency is used. Besides, in

the design of PLL, the bandwidth of the loop filter is usually lower than one tenth of the reference frequency, so a PLL needs to use a low reference frequency and a narrow bandwidth loop filter simultaneously to achieve the high frequency resolution of the output clock and prevent the leakage of the reference signal. Nevertheless, due to the narrow filter bandwidth, the PLL spends a lot of time to lock the target frequency, which means a longer settling time is needed. However, because a fractional-N PLL can use a high frequency signal as the reference clock, it can achieve high frequency resolution of the output clock and meanwhile release the restriction of the filter bandwidth. In addition, another important performance index is the in-band phase noise, and we know the output in-band phase noise in a PLL is the N, the divide ration, times of the phase noise of the reference clock. Therefore, keeping the same output frequency and increasing the reference frequency is an effective way to lower the output in-band phase noise. Theoretically, doubling the reference frequency can lower the output in-band phase 6dB. Furthermore, there is no proper greatest common divisor for the central frequency of each channel in 60GHz mm-Wave system. Therefore, summing up the benefits of digital design and fractional-N PLLs mentioned above, an all-digital fractional-N PLL is chosen to implement a suitable frequency synthesizer for 60GHz mm-Wave system.

1.2 Overview of Thesis

The thesis is organized as follows. In chapter 2, the conventional analog PLL implementations and the state of the art digital frequency synthesizers will be shortly addressed with comments on systems and technology trend. The proposed all-digital phase locked loop (ADPLL) architecture and its operation principle will be presented.

In chapter 3, we make some investigations on the dynamic of the ADPLL. To obtain the noise transfer function of the loop, a linear model for the ADPLL is introduced. The output phase and jitter will be analyzed with the help of the linear model.

Chapter 4 starts with the top level block diagram of the ADPLL. The implementation details of the most important building block, namely the phase detection circuits, the digitally controlled oscillator and the high speed frequency divider, will be described.

In chapter 5, the experiment setup and the photo of the implemented prototype will be presented. Finally, a brief conclusion of this work is given in chapter 6.

Chapter 2 ADPLL Architecture

2.1 Architecture of Fractional BBPLL

2.1.1 Analog Fractional PLL

The structure of the conventional fractional–N PLL (FPLL) is shown in Fig. 2-1. The phase frequency detector (PFD) estimates the phase difference between the reference clock f_{REF} and the divide-by-N.f voltage controlled oscillator (VCO) clock f_{FB} by measuring the time difference between their closest edges and generates either an Up or a Down pulse with width proportional to the measured time difference. The current pulse generated by the charge pump is converted into the control voltage of the VCO at the loop filter. The main task of the loop filter is to suppress the glitches introduced by the charge pump on every phase comparison instance. The ΣΔ modulator is used to control the divider to provide a fractional-N divide ratio for FPLL. The loop automatic adjusts the VCO control

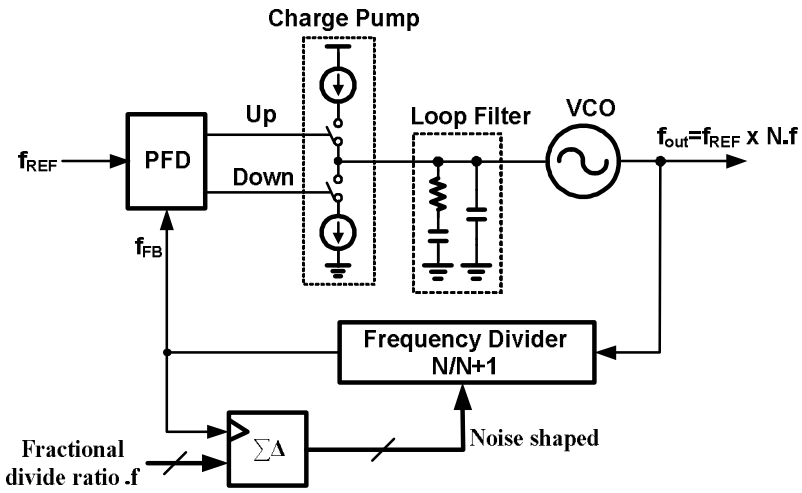


Fig. 2-1 Conventional Fractional-N PLL

voltage by the feedback mechanism, so that under locked conditions, the average output frequency establishes an exact relationship to the reference input frequency.

According to the different goals, by adjusting the loop parameters, the performance of the traditional FPLL can meet the requirements of different applications including high-speed memory interfaces, wireless transceivers, Ethernet receivers, and disk drive read/write channels. Nevertheless, big challenges to implement low-jitter analog synthesizers are coming from future system and technology trends.

The explosive growth of today's telecommunication market has brought an increasing demand for low cost, reduced power consumption and more functionality of the silicon chip. These requirements are driving an unprecedented degree of integration of digital and analog circuitry on the same die forming which is known as System-on-Chip (SoC).

As the technology paradigm shifts into the nano-meter CMOS arena, the advanced process presents the new integration opportunities but complicates the implementation of traditional RF and analog circuits. For example, charge-pump-based PLL implementations in the deep-submicron CMOS may encounter capacitor leakage, current mismatch, and limited dynamic range under low supply voltage, leading to higher noise floor and spurious tone emission. Moreover, the high degree of integration allows more digital switching noise to be coupled into the high-precision analog section through the power supply network and the low-resistance substrate. This degrades the noise signal to noise ratio of the analog circuit and the problem gets worse with the scaling down of the supply voltage.

On the other hand, migrating to the digitally intensive frequency synthesizer can benefit from the advantages of the digital design, including robustness against process-voltage-temperature (PVT) variation and substrate noise, higher flexibility of the loop filter design, fast design turnaround cycles, ease of testability, smaller silicon area and less power dissipation, which can get better with each process node. Consequently, digital intensive or digital assistance approached of the frequency synthesizers have drawn tremendous research efforts recently[3]-[5]. In next section, some of the state of the art all digital synthesizer will be illustrated.

2.1.2 All-Digital PLL

Due to the lack of the low-jitter digitally controlled oscillator (DCO), all digital PLLs just took off in practical high-performance RF applications in the past decade. Recently, a digitally controlled oscillator, which deliberately avoids any analog tuning voltage controls, was first ever presented in[3] for RF wireless

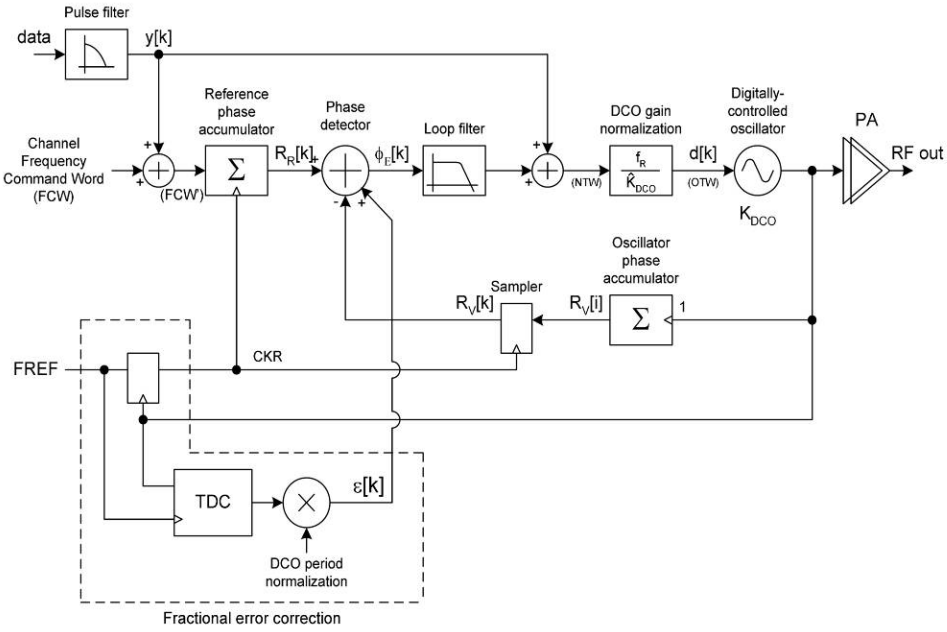


Fig. 2-2 Block diagram of the ADPLL architecture proposed in[4]

applications. The phase domain ADPLL which uses this DCO is also reported in[4]. Its block diagram is shown in Fig. 2-2. Excellent phase noise performance and fine frequency resolution is achieved through the LC-tank based DCO and high-speed ΣΔ dithering. The variable phase $R_V[i]$ is determined by counting the number of rising clock transitions of the DCO oscillator clock, while the reference phase $R_R[k]$ is obtained by accumulating the frequency command word (FCW) with every rising edge of the retimed reference clock CKR. The phase error is resolved by subtracting $R_V[i]$ from $R_R[k]$ and then filtered by a digital loop filter. Finally, the output of the filter is fed to the normalized DCO to adjust the output frequency.

Due to the edge counting nature, the quantization resolution is limited by the DCO clock period. For wireless applications, a finer resolution is required. This is achieved by using the time to digital converter (TDC), which measures the fractional time difference between the reference clock and the next rising edge of the DCO clock. It has a resolution of a single inverter delay, which is better than 40ps in the deep-submicron CMOS process. In order to achieve good phase noise performance, great care must be taken to the TDC layout matching and the accuracy of the DCO period normalization factor for the output of TDC.

In [5] an all digital bang-bang PLL (BBPLL) with spread-spectrum capability is presented for the application of memory controller. The structure of the BBPLL is addressed in Fig. 2-3, where the phase information between the reference clock Fref and the feedback clock Fdiv is estimated by a simple binary phase detector (BPD). Its operation is equivalent to a one bit quantizer for the phase error. Since the BPD is sensitive only to the polarity of the phase information, it may suffer from long locking time with large initial frequency error. According to the phase sensing techniques, the ADPLL can be roughly

classified into two major categories: linear phase detection and binary phase detection. [4] and [5] belong to the former and the latter one, respectively.

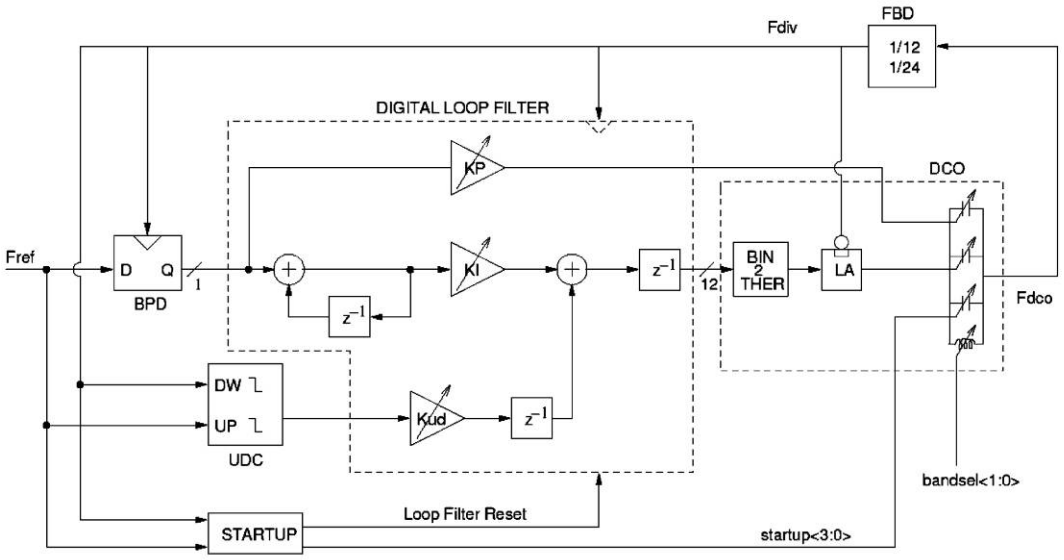


Fig. 2-3 Block diagram of the digital BBPLL architecture proposed in [5].

Compared to using binary phase detector, the ADPLL with linear phase detection may resort to the TDC or more complicated phase detector, which costs great efforts and hard to design. However, though the binary phase detection is much easier to design, it suffers from larger output jitter, higher spur energy and longer settling time, which are all bad characteristics in PLL design.

2.2 Proposed Solution

2.2.1 Proposed Dual Mode Fractional-N ADPLL Architecture

The architecture of the proposed fractional ADPLL is illustrated in Fig. 2-4, which is composed of two phase accumulators PAC1 and PAC2, for reference and feedback path, respectively, a dual-mode phase frequency detector (DPD), an additional negative feedback loop with a programmable gain (Kpd) and a ΣΔ modulator around the PAC1, a digital loop filter with programmable integral (Kip) path, a locking process monitor (LPM), an LC based digital controlled oscillator (DCO) with single variable inductor, and a divide-by 16 prescaler. By setting the required integer (N_i) and fractional frequency multiplication factor (N_f), we get the total frequency multiplication factor (N). When the loop is locked, the output frequency of the ADPLL will be N times of the reference frequency (f_{REF}), which means the relationship between the output and reference frequency is f_{OUT}= f_{REF}*N, where N = N_i +N_f. When the circuit is working, The PAC1 accumulates one sixteenth of the total frequency multiplication factor (N/16), while PAC2 accumulates the prescaler output phase (f_{DIV16}). The phase difference (Φ_E)

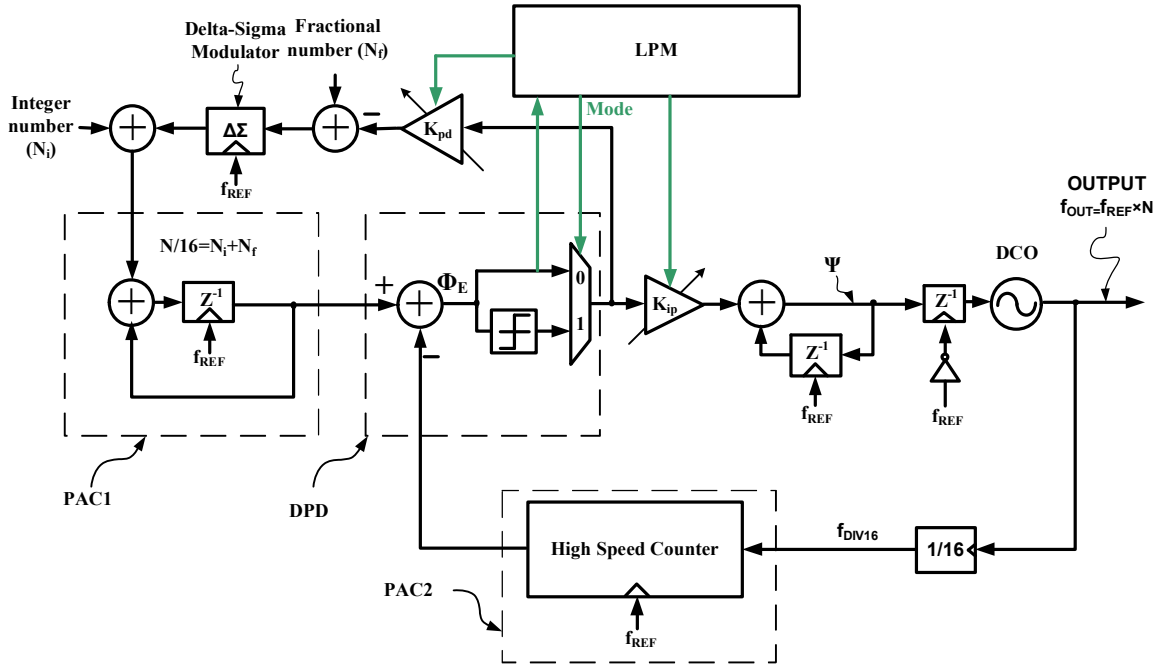


Fig. 2-4 Block diagram of the proposed ADPLL.

between f_{REF} and f_{OUT}/N is then resolved by a subtracter. In the locked state, the difference between the contents in PAC1 and PAC2 is constant. The DPD is operated in the linear mode during frequency acquisition (FA), and turned into binary mode during the phase tracking (PT) process. In order to reduce the power consumption of PAC2, a divide-by 16 prescaler is introduced after the DCO. In the following section, the operation principle of the ADPLL will be discussed in detail.

2.2.2 Overview of the Operation

In the initial phase of the locking process, the loop starts with the FA mode. During this mode, the DPD operates in linear mode (Mode=0) and the accumulator of the integral path in the digital loop filter is disabled, which means the integral path is transformed to a proportional path; meanwhile, the additional negative feedback around the PAC1 is also cut, leading the PLL to become a second order frequency acquisition loop, as shown in Fig. 2-5. To accelerate

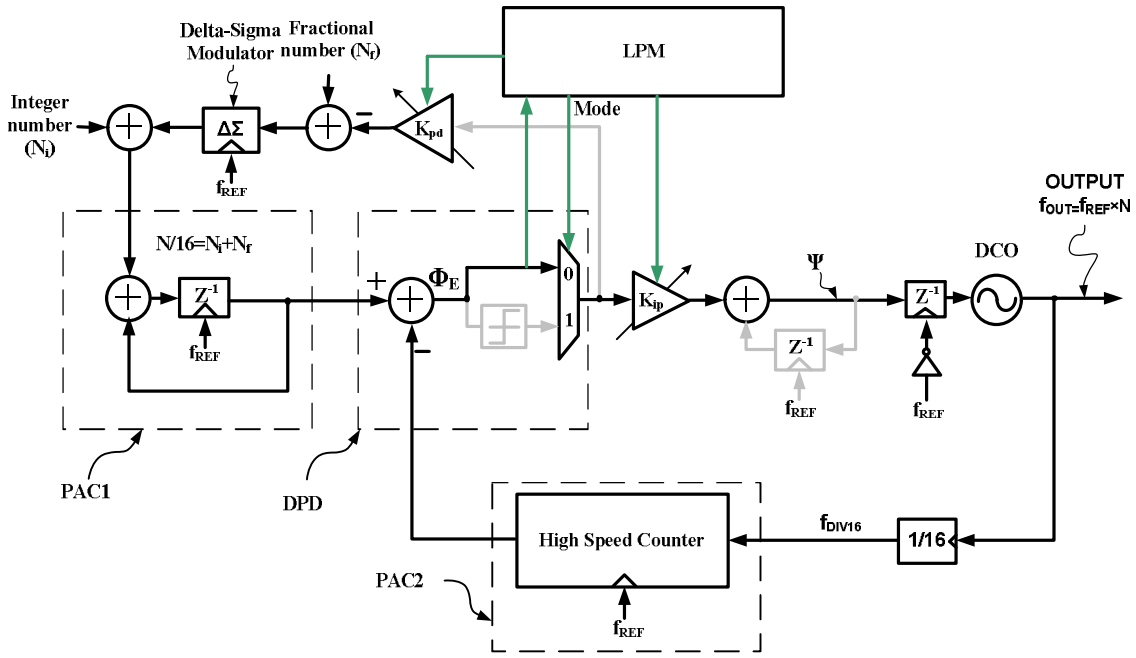


Fig. 2-5 Block diagram of ADPLL in FA mode.

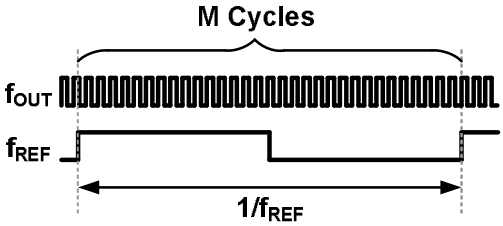


Fig. 2-6 Frequency detection by edge counting.

frequency acquisition, a larger forward path gain $K_{ip,FA1}$ is first applied and then switched to a smaller $K_{ip,FA2}$ after the loop is settled [13].

The principle of the frequency detection can be explained as following. Consider the case shown in Fig. 2-6. If M denotes the number of the rising edge appeared during a reference clock cycle, the relationship between the output frequency f_{OUT} and the reference frequency f_{REF} can be expressed as

$$M = \frac{f_{OUT}}{f_{REF}}. \tag{2-1}$$

The difference between M and the frequency multiplication factor N is

$$M - N = \frac{f_{OUT} - f_{TARGET}}{f_{REF}}, \tag{2-2}$$

where f_{TARGET} is the target output frequency Nf_{REF}. Thus the frequency error can be estimated by (M-N), which can lead to the frequency locked loop as shown in Fig. 2-7. It can be shown that this architecture is equivalent to the structure shown in Fig. 2-5, by moving the accumulator of the loop filter before the subtractor and noting that K_{pd}=0.

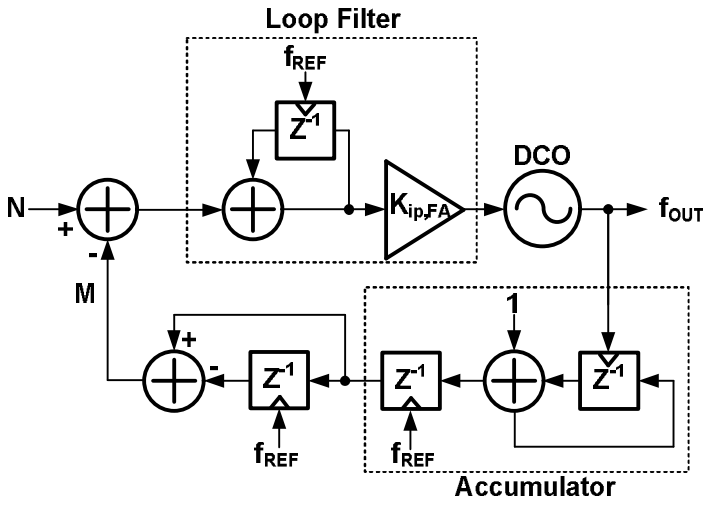


Fig. 2-7 Equivalent frequency locked loop during FA mode.

After Φ_E variation is within 1 LSB, the LPM will launch the PT mode. The accumulator of the integral path in the digital loop filter and the additional negative feedback path around PAC1 are then activated, and the whole system is turned into a 2nd order phase-locked loop, as shown in Fig. 2-8. In the meantime, PAC1 and PAC2 are reset, while the content of the integrator in the loop filter (Ψ) is preset to the current DCO control code. Afterward, the DPD is switched to the

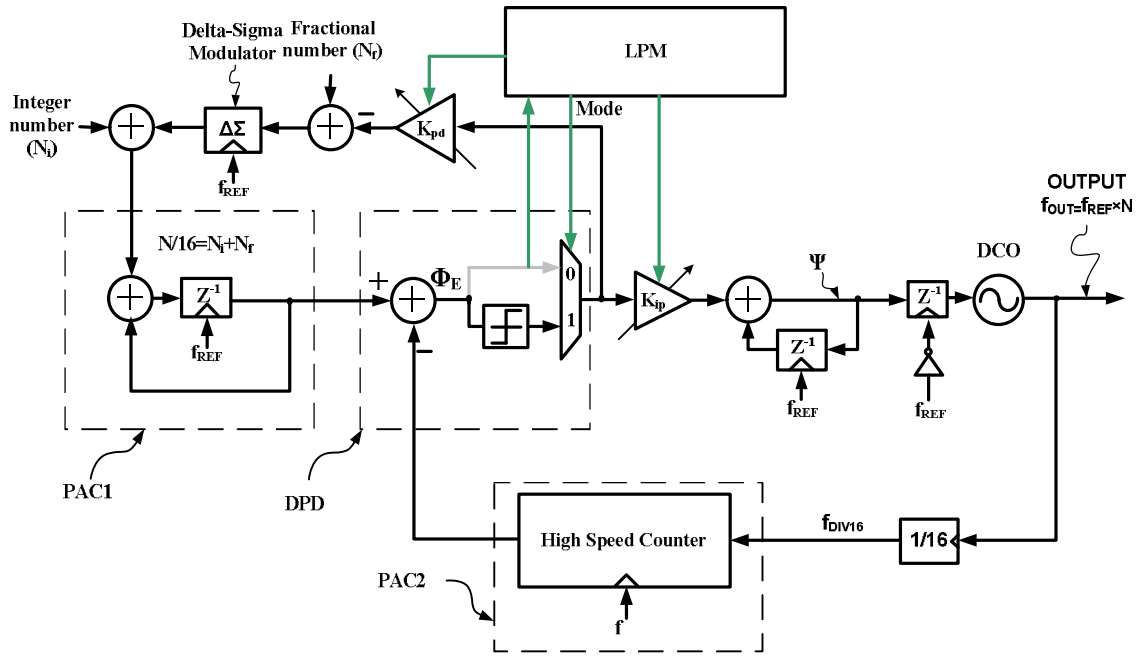


Fig. 2-8 Block diagram of ADPLL in PT mode.

binary phase detection mode by asserting the control signal Mode to 1 without resorting to sophisticated time to digital converter (TDC). In the mode, the DPD senses the phase difference Φ_E on every reference period and generates the output bit stream to the loop filter according to its polarity. For example, if Φ_E is less than zero, DPD outputs -1. If Φ_E is equal or larger than zero, DPD outputs 1. The term BBPLL will be used to represent the ADPLL during PT mode in this thesis.

Chapter 3 Analysis of the ADPLL

3.1 ADPLL in Frequency Acquisition Mode

In order to achieve fast and wide locking process, two different locking modes are used. At the beginning of the locking process, the frequency acquisition mode is first activated and the DCO is locked roughly to the desired frequency. During this mode, the accumulator of the integral path in the digital loop filter is disabled, and the additional negative feedback around PAC1 is cut (K_{pd}=0), therefore, the ΣΔ modulator generates the required fractional number without the additional negative feedback, so the total divide ratio is $N=N_i+N_f$ and the system block diagram can be simplified as shown in Fig. 3-1. The scaling factor $K_{ip,FA}$ introduced in the figure denotes the forward path gain during frequency acquisition mode. In the frequency domain, it controls the gain of the frequency detected in response to the frequency changed at the DCO output. The gain factor $K_{ip,FA}$ also controls several key loop characteristics such as the loop

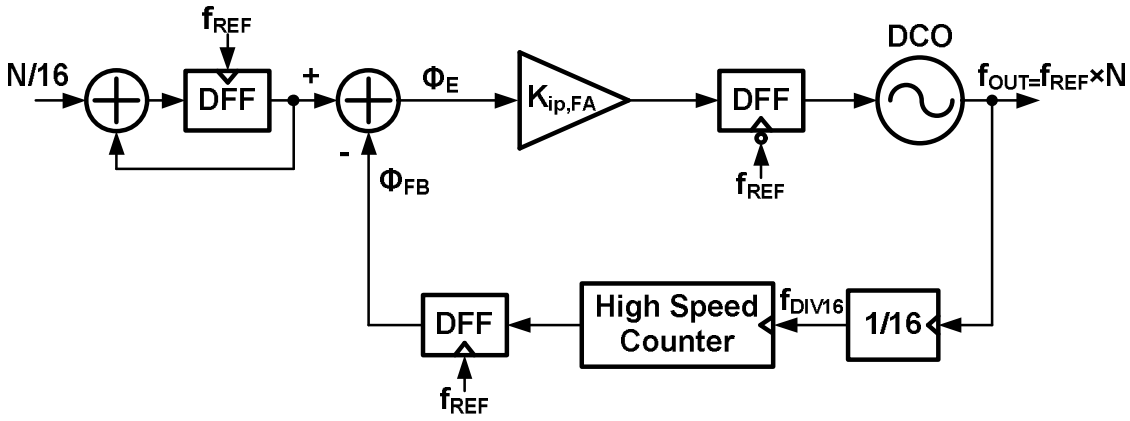


Fig. 3-1 System block diagram during frequency acquisition mode.

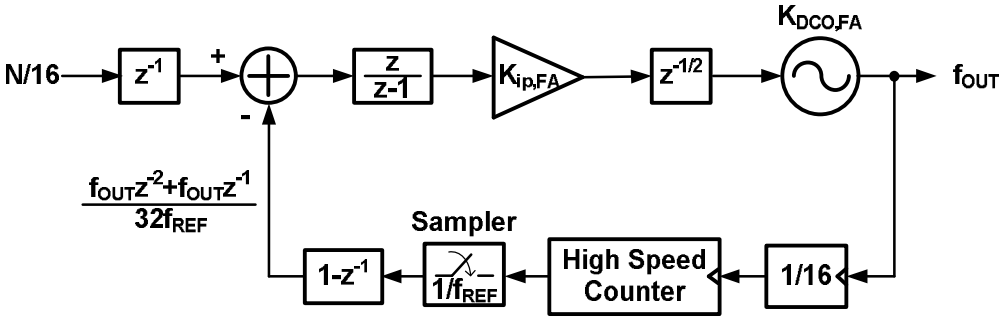


Fig. 3-2 Equivalent system block diagram during frequency acquisition mode.

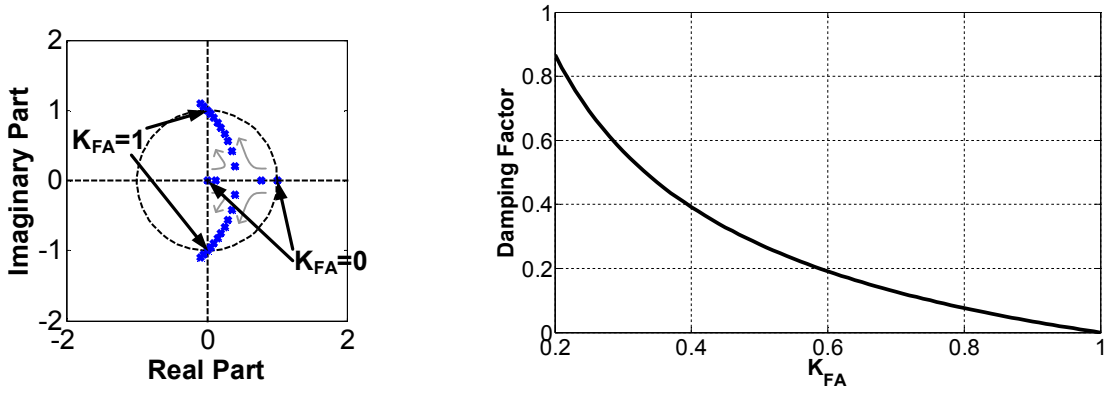
stability, the transient response and the frequency error in the steady state.

In order to investigate into how $K_{ip,FA}$ affects the loop behavior, a discrete time z-domain model is built. As mentioned in chapter 2, the block diagram can be rearranged by moving the accumulating operation after the subtractor, and replaces a differential operator on feedback path as illustrated in Fig. 3-2. Two approximations are used to simplify the model. The first one is to force the uniform sampling or PLL update rate, despite the presence of a small amount of jitter in the reference clock. This approximation is very accurate since the period deviation due to the jitter is several orders of magnitude smaller than the DCO period. The second approximation is the infinite resolution of the phase detection which neglects the fact that the phase information is quantized by the divided DCO clock f_{DIV16}. If the free running frequency of the DCO is ignored and assumed to be 0, the closed loop transfer function can be expressed as

$$H_{FA,C}(z)=\frac{f_{OUT}(z)}{N(z)}=\frac{2f_{REF}K_{FA}z^{-\frac{3}{2}}}{1+(K_{FA}-1)z^{-1}+K_{FA}z^{-2}} \text{ where } K_{FA}=\frac{K_{DCO,C}K_{ip,FA}}{32f_{REF}}, \qquad (3\text{-}1)$$

where $K_{DCO,C}$ denotes the frequency step per control code of the activated varactor bank in the DCO during frequency acquisition mode.

According to the discrete time signal process theorem, the condition for stability of a causal system can be derived by examining the position of its poles.



(a) (b)

Fig. 3-3 (a) Pole-zero plot and (b) the damping factor as a function of K_{FA} of the ADPLL during frequency acquisition mode

For a given system function of a linear and time invariant system, if the outmost pole is included in the unit circle on the pole-zero plot, the system is stable. Considering the transfer function of the ADPLL in frequency acquisition mode, $H_{FA,C}(z)$, the pole-zero plot is illustrated in Fig. 3-3(a) for different K_{FA}. It is clear that the loop stability requires K_{FA} to be less then 1.To gain more clear insight into the time domain behavior, the damping factor which is derived from the equivalent continuous time poles by solving $z=e^{sT}$ is shown in Fig. 3-3(b). The result shows that it's an over damping system when $K_{FA}<0.244$; a critical damping system when $K_{FA}=0.244$; and an under damping system when $K_{FA}>0.244$.

In order to validate the z-domain model of the ADPLL developed here, some simulations are performed by using MATLAB Simulink. Fig. 3-4 shows the simulation results of the time domain response with an initial frequency error of 7GHz. For $K_{FA}=0.6$, it shows a fast response with overshooting while a slow response with longer settling time is obtained for $K_{FA}=0.09$. The result shows a good agreement between simulation and the analytical model.

It should be noted by inspecting the result shown in Fig. 3-4 where some ripples appear on the output frequency in the steady state. This can be explained by taking the quantization effects into consideration. Due to the edge counting nature of the phase detection, the phase error between the reference clock and feedback is quantized with the resolution step determined by DCO clock rate. When the loop is settled, the phase error will be located between two quantization steps, leading to constant output of the phase detection. The phase error will remain unchanged until the accumulated phase error exceeds one quantization step. Then the phase error is corrected by the feedback loop. Thus the ripples are generated on the output of phase detector and the output frequency.

After the loop is settled, due to the limitation of the capture range, the frequency error must be taken into consideration before entering the bang-bang phase tracking mode. As mentioned before, the output of the phase detector iterates between two adjacent values when the loop reaches steady state. In other words, the average of the output frequency in steady state indicates the desired

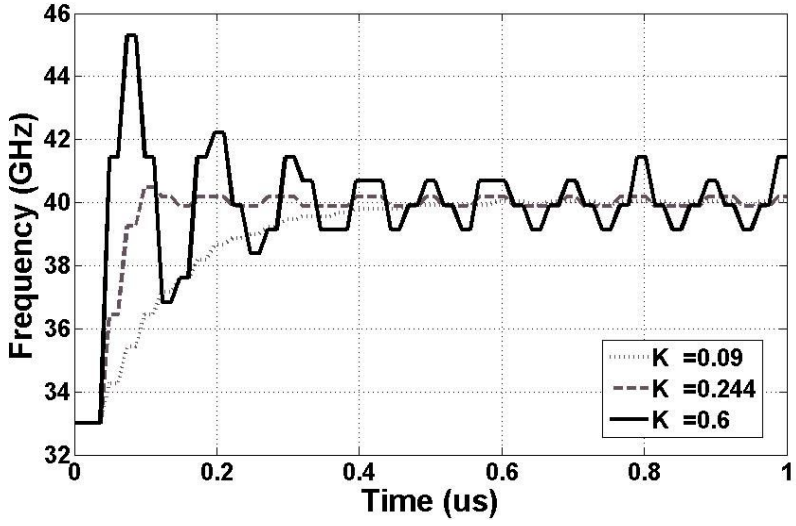


Fig. 3-4 Simulated time domain response of the ADPLL in frequency acquisition mode with 3 different K_{FA} value.

clock rate Nf_{REF}. Therefore, the frequency offset of the loop can be characterized by the frequency step

$$\Delta f_{RES,FA} = K_{ip,FA} K_{DCO,C} \tag{3-2}$$

Equation 3-2 suggests that the forward gain $K_{ip,FA}$ should be kept lower to enhance the frequency resolution. Unfortunately, this suggestion is in conflict with the requirement for shortening the locking time, because when the frequency quantization step is finer, the loop response is slower. Take the critical damping case as an example, substituting K_{FA}=0.244 and f_{REF}=40MHz in equation 3-1, we can obtain $\Delta f_{RES,FA}=K_{ip,FA}K_{DCO,C}$=312.32MHz, which is too large for efficient phase tracking.

Therefore, to speed up the locking process while keeps the frequency resolution high, several different states are used during frequency acquisition mode. At the beginning of the FA mode, $K_{ip,FA}$ is set to 1 and the coarse tuning bank of DCO is first modulated to achieve high loop bandwidth and fast frequency tracking. When the loop is settled first time, the modulated bank is changed to the fine tuning bank of DCO. After the loop is settled again, the first two bits of the ΣΔ tuning bank is chosen and modulated with $K_{ip,FA}$=4 first, and then the smaller $K_{ip,FA}$=1 is applied later to improve frequency resolution and so on. Therefore, the coarse, fine, and the upper bits of ΣΔ tuning bank are activated step by step during this mode, and $K_{DCO,C}$, $K_{DCO,F}$, and $K_{DCO,\Sigma\Delta\_up}$, the frequency variations correspond to one LSB of the coarse, fine, and the upper ΣΔ tuning bank, are about 400MHz/LSB, 150MHz/LSB, and 50MHz/LSB, respectively. Thus from equation 3-1, K_{FA} is 0.312, 0.117, 0.039 and 0.01, respectively. At the end of the frequency acquisition mode, the frequency resolution is 6.25MHz.

3.2 ADPLL in Phase Tracking Mode

3.2.1 Operation Principle of the ADPLL during Phase Tracking Mode

After the initial frequency is locked roughly using the frequency acquisition mode, the finer tuning bank of the DCO and the accumulator of the integral path in the loop filter are activated and the additional negative feedback around PAC1 is linked ($K_{pd} \neq 0$). Then the loop is switched into the bang-bang phase tracking (PT) mode and the system block diagram during this mode is illustrated in Fig. 3-5.

In this design, the PAC1 will ideally accumulate one sixteenth of the total divide ratio (N/16) while the rising edge of the reference clock is coming. The PAC1 adds this divide ratio onto the former result of the accumulator, therefore the output of PAC1 can be viewed as an ideal reference phase value. Meanwhile, the high speed counter in the PAC2, which is connected after the divide-by 16 prescalar, will add 1 onto the former output while the rising edge of the prescalar

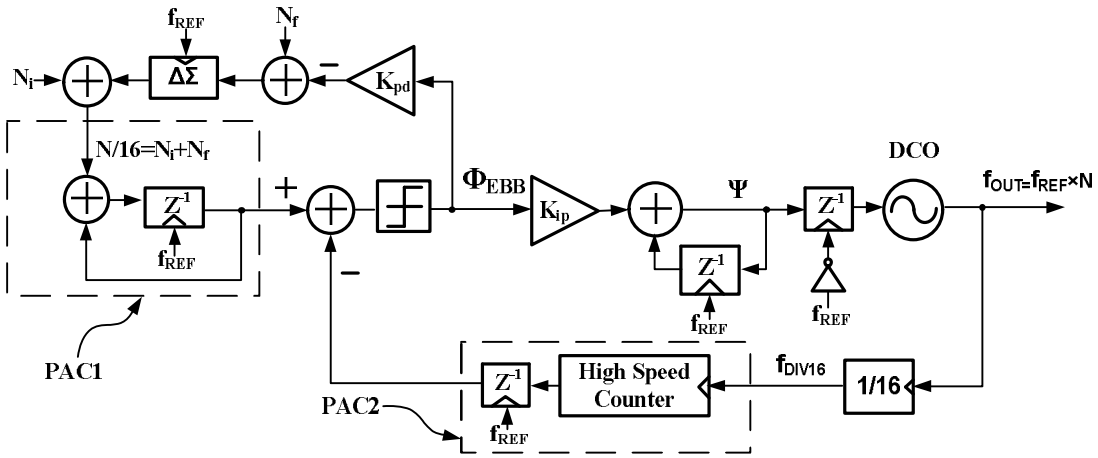


Fig. 3-5 System block diagram during bang-bang phase tracking mode.

is coming, so the output of the PAC2 can be considered as the feedback phase value. Therefore, the BPD subtracts the results of the PAC1 and PAC2 while the rising edge of the reference is coming and sends the quantized result into the next stage.

However, in traditional fractional PLLs concept, because the target relationship between the output frequency of DCO and the reference frequency is not an integer-N, the output phase of the DCO is not an integer-N, neither. In other words, the output of the DCO actually is a fractional-N. Therefore, because the nature of a simple high speed counter can count the integer number only, it can not exactly detect the fractional part of a value while the rising edge of the reference is coming, and an example with divide ratio $N=2_{1/4}$ is shown in Fig. 3-6. On the other hand, the fractional part of the output phase of the DCO will be detected only after it is accumulated for a while to an integer number.

Ideally, PAC1, the reference phase accumulator, will accumulate the fractional divide ratio every reference cycle, but PAC2, the feedback phase accumulator, can not exact detect the fractional part of the feedback phase while the rising edge of the reference is coming. The fractional part of the output phase of the DCO must be accumulated for a while to an integer number then PAC2 can really send the integer phase information. This phase quantization error influences the jitter performance for the fractional-N PLLs very much. In order to solve this problem, PAC1 is connected to an additional negative feedback with a programmable gain (K_{pd}) and a ΣΔ modulator in this design.

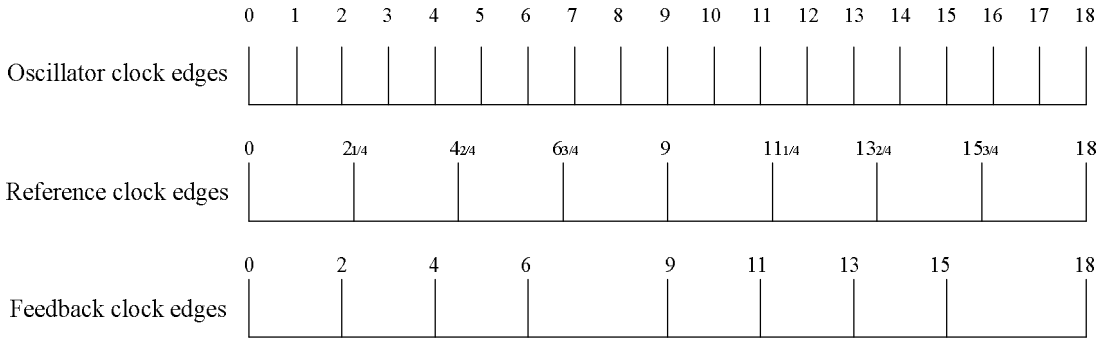


Fig. 3-6 The timing diagram when the total divide ratio is $2_{1/4}$.

The ΣΔ modulator will send different integer output in every reference cycle and accumulate the residue information in its loops. Although the time variant output is a group of integer numbers, the long term average of the ΣΔ modulator output will become a fractional number, the given N_f. In other words, though the divide ratio which is added by PAC1 is integer in every reference cycle, ΣΔ modulator will adjust its output every time to make the long term average of its output converge into the given fractional divide ratio, N_f.

Besides, because the long term detection on the output of the BPD, the additional negative feedback from the output of the BPD will adjust the input of the ΣΔ modulator to align the overflow timing of the output of the ΣΔ modulator with the overflow timing of PAC2. That means if the additional negative feedback loop collects enough information of the overflow timing, the outputs of PAC1 and PAC2 can be synchronized perfectly. Therefore, when the fractional part of the output phase of the DCO is accumulated in the high speed counter and does not overflow, PAC2 can only detect the integer part of the feedback phase. At the same time, the output of the ΣΔ modulator sends 0 into PAC1, so the real divide ratio which is sent into PAC1 is also only the integer part of the total divide ratio. When the fractional feedback phase overflows and PAC2 can detect

it, the output of the ΣΔ modulator sends 1 into PAC1, so the real divide ratio sent into PAC1 is also the overflowed integer part of the total divide ratio. Taking advantage of this mechanism, because the overflows of output of PAC1 and PAC2 can be synchronized, the phase quantization error is reduced; meanwhile, the locking time of the PLLs is shortened because the detection of the phase difference is more accurate. Therefore, this digital fractional PLLs can use only a simple integer accumulator to achieve non-integer divide ratio frequency locking and do not resort to TDC or complicated mathematical algorithm.

3.2.2 Locking Transient of the ADPLL during Phase Tracking Mode

As already mentioned in Chapter 2, the architecture can be further simplified as a digital bang-bang PLL (BBPLL) where a binary phase detector (BPD) and a ΣΔ modulator controlled divide-by-N/N+1 frequency divider are used instead of the binary quantizer, the accumulators and the subtracter as shown in Fig. 3-7. The binary phase detector output Φ_{EBB} is set to -1 when the rising edge of the feedback clock leads the reference clock edge. Otherwise, Φ_{EBB} is set to 1 to indicate that the feedback clock lags the reference clock. The variables D and Ψ introduced in Fig. 3-7 denotes the loop delay time normalized to one reference clock period $1/f_{REF}$ and the integral path output of the loop filter, respectively. In our design, the value of D is 0.5 which is introduced by the re-synchronizing operation before the digital loop filter output feds to the DCO.

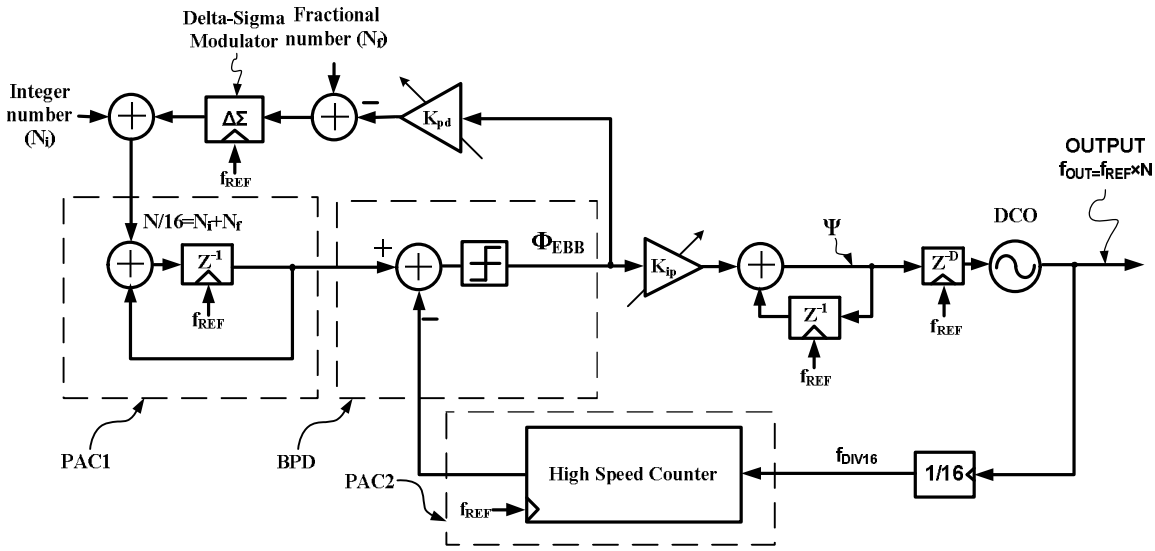
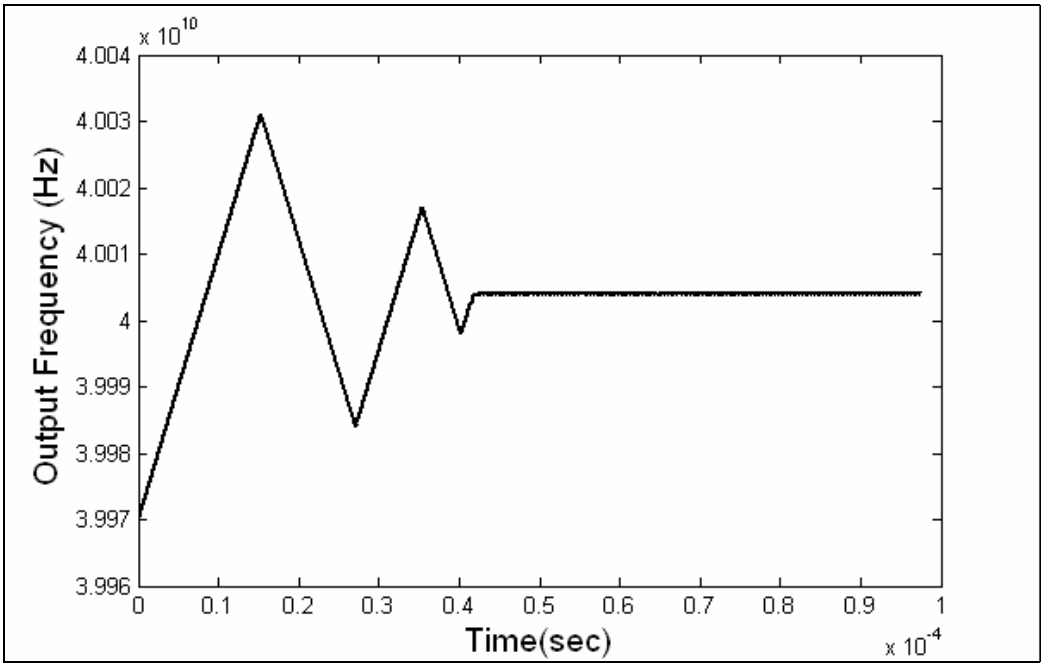


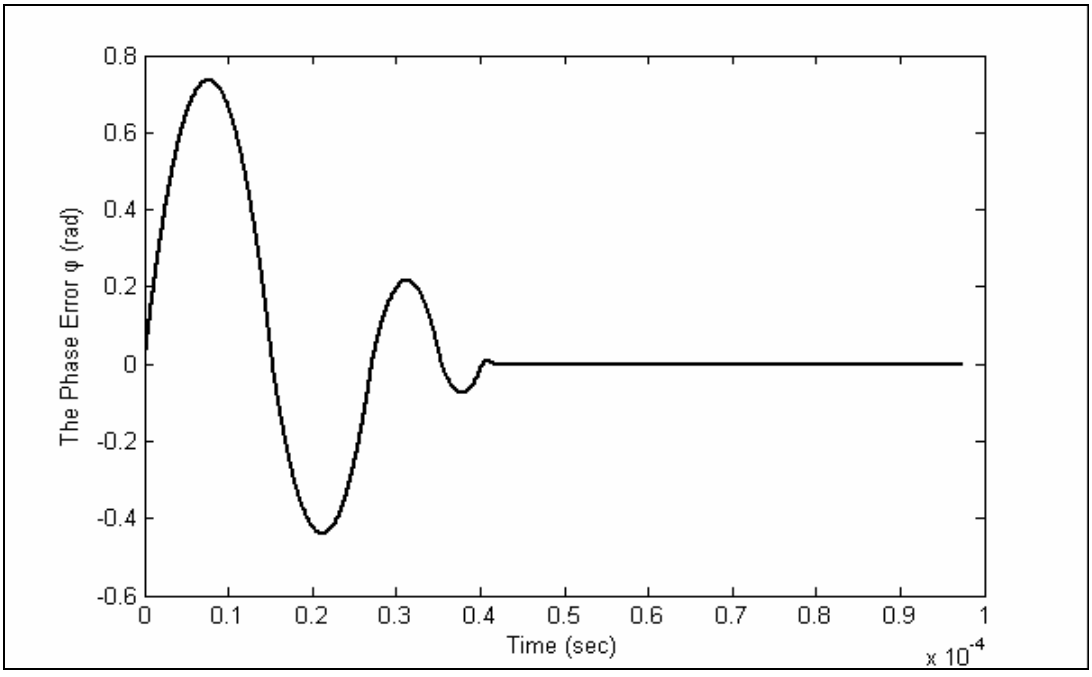
Fig. 3-7 System block diagram during bang-bang phase tracking mode.

The classical frequency analysis of linear PLLs is derived by the Laplace transform or the Z-transform. However, due to the presence of the nonlinear binary phase detector block in the loop, this approach cannot be used for the ADPLL during PT mode. The fundamental aspect of BBPLL is the presence of limit cycles in the loop dynamics. In fact, a BBPLL cannot lock to the reference clock in a traditional sense, where the output of the phase detector and the loop filter voltages settle asymptotically around a fixed value, disturbed only by thermal noise. In order to achieve more insight into the BBPLL characteristics before the analytic equations of the loop property are given, some results of the behavior simulations are shown. Fig. 3-8 shows the simulation results of the locking behavior and the phase plane of a BBPLL with D=0.5, where the phase error φ is the un-quantized phase difference between the reference and feedback loop. It is clear from Fig. 3-8 (a) that the BBPLL output frequency oscillates around a fixed value in locked state. The simulated phase plane is shown in Fig. 3-8(c), where the x-axis is the phase error φ and the y-axis is the integral path output Ψ of the loop filter. Since the integral path output goes into the DCO

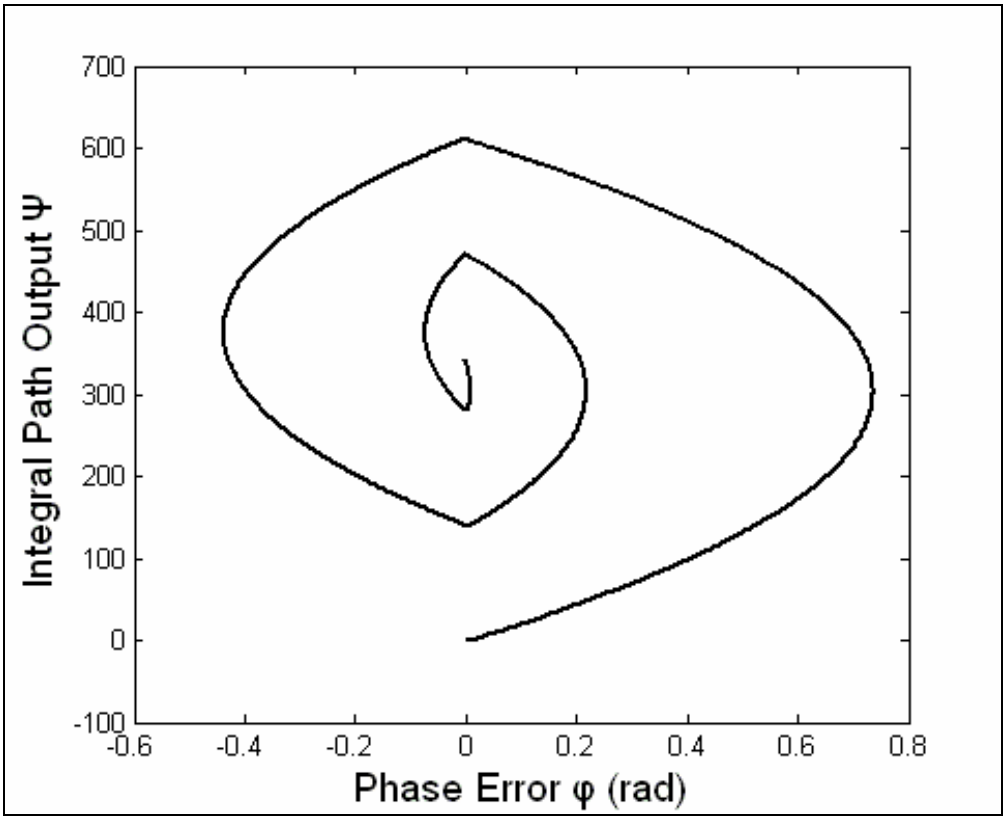
directly, it can be thought as an inner frequency tracking loop. Thus the dynamics of the integral path output Ψ can be treated as the behavior of the tracking frequency. When the stability conditions are met, the trajectory converges toward center and then enters a periodic orbit.



(a)



(b)



(c)

Fig. 3-8(a) Simulated output frequency, (b) phase error versus time and (c) the phase plane of the BBPLL.

3.3 Output Noise Performance of the ADPLL

After the rapid frequency acquisition, the ADPLL will finally reach a steady-state condition in the bang-bang phase tracking mode. The output noise performance in locked state including the spurs, timing jitter and output phase will be investigated. In particular the spur emission will be derived using the nonlinear model, while the output phase noise performance in the present of internal and external noise source will be analyzed with the help of the linear model.

3.3.1 Output Spur

Because of the overflowing in the fractional part divide ratio of the fractional PLLs and the presence of the limit cycles or orbit in the dynamics of the BBPLL, the output clock f_{OUT} is frequency modulated by a periodic control signal in locked state, leading to spurious tone emission.

To gain more insight into the loop dynamics, consider the BBPLL which is free from any internal or external noise source and has the following parameters: f_{REF}=40MHz, K_{ip}=1, K_{pd}=0.04, K_{DCO}=10000, D=0.5 and N=1000.1. Fig. 3-9(a) shows the simulation result of the output frequency versus time in the locked state of the BBPLL with above setting. The result shows that the modulating signal of the carrier is similar to a sampled sine wave with some ripples and the modulating rate is equal to $1/10f_{REF}$ or its harmonic.

Under the assumption of narrow-band frequency modulation, the power level of the spurious tones compared to the carrier can be approximated as [5]:

$$P_{spur} = 20\log(\beta)\ (\text{dBc}),\quad \beta = \frac{\Delta\omega_{pp}}{\omega_m}, \tag{3-3}$$

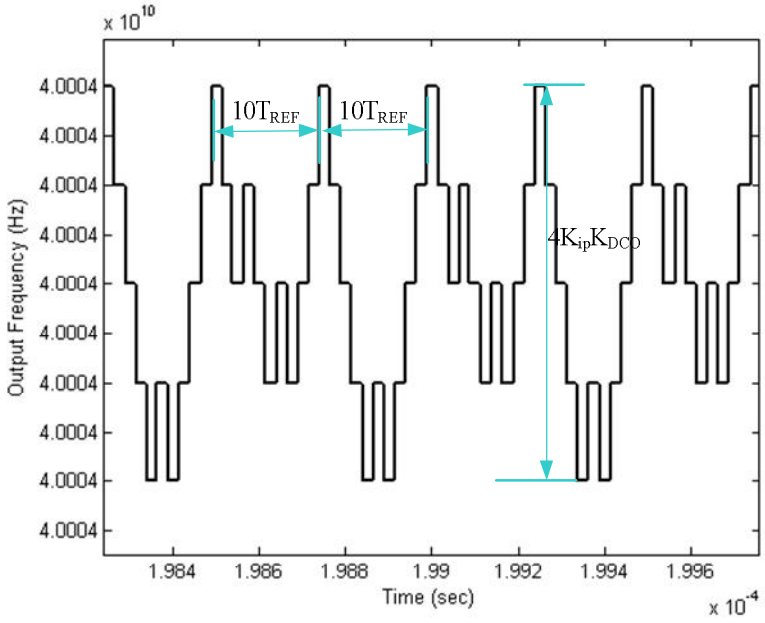
where β is modulation index defined as the ratio of the frequency deviation Δω to the frequency of the modulating wave ω_m in a frequency modulation system when using a sinusoidal modulating wave.

The BBPLL output can be approximated as a frequency modulation signal as the modulating input. By inspection of Fig. 3-9, the peak to peak frequency deviation is given as

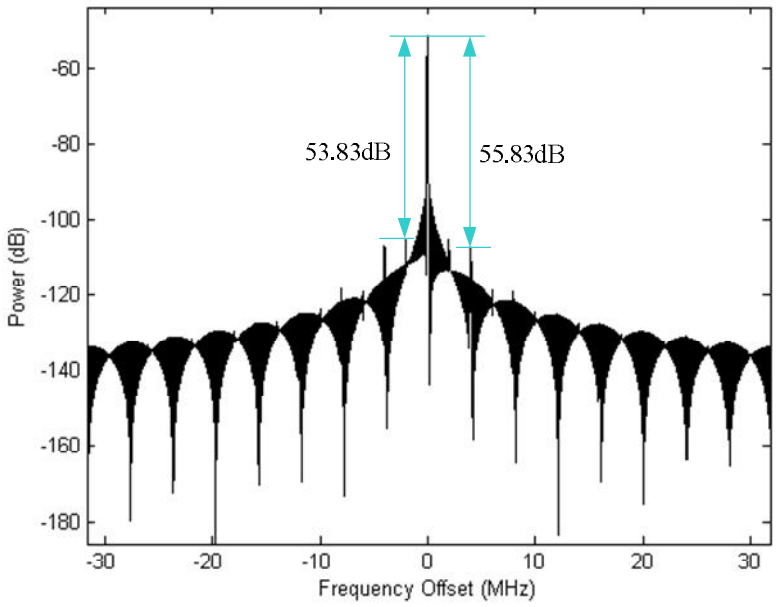
$$\Delta\omega_{pp} = \left(4K_{ip}\right)K_{DCO}. \tag{3-4}$$

From [6], the modulation rate of the BBPLL output is

$$\omega_m = 2\pi\frac{f_{REF}}{10L}, \tag{3-5}$$



(a)



(b)

Fig. 3-9 (a) The simulation results of the output frequency versus time and (b) the output spectrum in locked state of the ADPLL with the following parameters: f_{REF}=40MHz, K_{ip}=1, K_{pd}=0.04, K_{DCO}=10000, D=0.5 and N=1000.1.

where L is the integer value satisfying the following conditions:

$$\frac{D(2+R-RD)}{2+R-2RD} \le L \le \frac{(2-RD)(D+1)}{2-R-2RD}. \qquad (3\text{-}6)$$

An inspection of equation 3-4 and 3-5 reveals that larger $K_{ip}K_{DCO}$ and D will result in larger $\Delta\omega_{pp}$ and smaller ω_m, thus increasing the power level of the spurs.

As the example shown in Fig. 3-9, substituting K_{ip}=1, K_{pd}=0.04, K_{DCO}=10000, and D=0.5 into equation 3-4 and 3-5, we obtain $\Delta\omega_{pp}=4\times10^4$ rad and $\omega_m=2\pi(4\times10^6)$ rad. This gives rise to spurs 4 MHz away on both sides from the oscillating frequency. Their power level is at

$$P_{spur} = 20\log(\beta) = \text{-}55.9 \text{ dB}, \qquad (3\text{-}7)$$

relative to the main carrier tone. In Fig. 3-9(b), the simulated output spectrum is shown and the expression above is confirmed. It should be noted that the analysis is performed under the noise-free assumption. Obviously, this is not a practical case. In fact, the noise will randomize the spurious energy.

3.3.2 The Linear Model of the ADPLL during PT Mode

Although the nonlinear model has been helpful to find the general properties of the trajectories, this approach can not successfully describe the output noise performance under the more realistic assumptions of the presence of internal and external noise sources. A different approach will be demonstrated in the following sections. A continue-time linear model will build for the ADPLL during bang-bang phase tracking mode. Then the system transfer function will be derived to estimate the performance of the loop.

From the system architecture shown in Fig. 3-7, the difficulty to build the linear model for this system is the hard nonlinearity introduce by the binary phase detector. An approach for modeling the binary phase detector is reported in [7] where the phase detector is modeled as a linear block with a gain K_{bpd} as illustrated in Fig. 3-10. The symbol $\Delta t=t_r-t_d$ is the difference between the rising edges instants of the reference (t_r) and feedback clock (t_d). It is clear that in the locked state, the average value of the BPD output $E[\Phi_{EBB}]$ converges to 0. Assume that for some reason the probability distribution of Δt is shifted away from its equilibrium point by a small amount η in the positive direction. In this case the average value of Φ_{EBB} will be slightly positive. Following this circumstances, the phase detector gain can be defined as the rate of change in $E[\Phi_{EBB}]$ due to a small shift η of the probability density function (pdf) around the locked condition:

$$K_{bpd} \equiv \frac{\partial}{\partial \eta}\left(E\left[\Phi_{EBB} \mid shift = \eta\right]\right)\Big|_{\eta \to 0^+} . \tag{3-8}$$

Under this definition, the value of K_{bpd} can be approximated as:

$$K_{bpd} = 2 f_{\Delta t}(0), \tag{3-9}$$

where $f_{\Delta t}$ denotes the pdf of Δt.

When the PLL is locked, the integral path will have centered the dynamics so that we can assume

$$T_{REF} - NT_{DCO,free} - NK_T \Psi[k - D] = 0 . \tag{3-10}$$

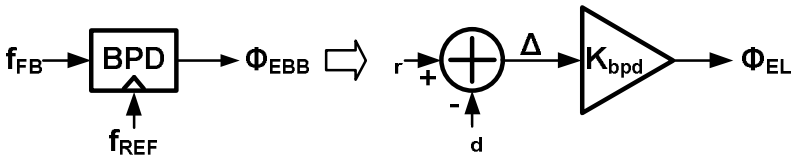


Fig. 3-10 BPD linearized model.

Thus the nonlinear map in the presence of jitter on the reference and DCO clock can be written as:

$$\Delta t[k+1] = \Delta t[k] + t_j - \frac{K_{pd}}{Nf_{REF}} \operatorname{sgn}\left(\Delta t[k]\right), \tag{3-11}$$

where t_j is the timing jitter appeared on reference clock. To emphasize the fact that the loop has a non-integer loop delay of D=0.5, the above expression is rewritten as:

$$\Delta t[k+1] = \Delta t[k] + t_j - \frac{K_{pd}}{Nf_{REF}} \operatorname{sgn}\left(\Delta t[k]\right). \tag{3-12}$$

If it is assumed that $\Delta t[0]=0$ and the values of Δt in the case of unjittered reference and DCO clock is Δt^*, the value of Δt^* can be only on discrete states:

$$\Delta t^* = n\frac{K_{pd}}{Nf_{REF}}, \quad n \in Z \tag{3-13}$$

The probability occupancy of the state n ($\Delta t^* = nN\beta K_T$) is defined as:

$$q_n \equiv P\left[\Delta t^* = n\frac{K_{pd}}{Nf_{REF}}\right], \tag{3-14}$$

then the pdf of Δt, $f_{\Delta t}$, will be given by the superposition of the pdfs of t_j, shifted by an amount equal to each occupied state and weighted by the probability of that in steady-state

$$f_{\Delta t}(a) = \sum_{n=-\infty}^{n=+\infty} q_n f_{t_j}\left(a - n\frac{K_{pd}}{Nf_{REF}}\right). \tag{3-15}$$

In general, the f_{tj} can be modeled as a Gaussian process with variance σ_{tj}^2 where σ_{tj}^2 denotes the jitter variance of reference clock. In formulas

$$f_{t_j}(x) = \frac{1}{\sigma_{t_j}\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{x}{\sigma_{t_j}}\right)^2\right]. \tag{3-16}$$

In order to find $f_{\Delta t}$, a statistical approach is used as following to obtain the value of q_n. From a given state n, Δt^* might go to state n+1or state n-1, and the transition probabilities from state m to state n is defined as

$$P_{m,n} \equiv P\left[\Delta t_{k+1}^{*} \in n \mid \Delta t_{k}^{*} \in m\right]. \tag{3-17}$$

Under the assumption that σ_{tj} is much smaller than loop quantization step $-K_{pd}/Nf_{REF}$, the states n with $|n| \geq 2$ occur with a probability which is negligibly small. Then the state diagram of the system describe in equation 3-12 can be simplified to a three state chain as illustrated in Fig. 3-11.

If $f_{\Delta t}$ is symmetrical around 0 then $q_{-1}=q_1$, and $P_{0,1}=P_{0,-1}=1/2$; therefore, in the case that the loop stays in the same state at the next time index, there exist two possible situations. For example, it might go from state 0 to state 1 at time index k and stay in state 1 at the next time instance k+1 when $\Delta t_{k-1}<0$. Also, it might start from state 1 at the previous time instance k-1 and stay in state 1 at time index k. However, in this case it can never stay in state 1 at next clock cycle. Thus, by inspection of equation 3-12 and noted that $\sigma_{tj} << K_{pd}/Nf_{REF}$

$$P_{1,1} = P_{-1,-1} = \frac{\frac{q_0}{2}}{q_0 + q_1}. \tag{3-18}$$

In the same way, we can find

$$P_{1,0} = \frac{\frac{q_0}{2} + q_1}{q_0 + q_1}. \tag{3-19}$$

To obtain the relationship between the state probability and transition probability, note that q_0 can be expressed as:

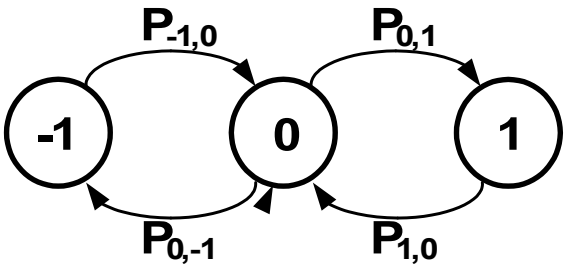


Fig. 3-11 State chain to approximating the BBPLL.

$$q_0 = q_{-1}P_{-1,0} + q_0P_{0,0} + q_1P_{1,0} = 2q_1P_{1,0} + q_0P_{0,0} \tag{3-20}$$

Since the states describe all possible events and they are disjoint, they must satisfy the normalization equation

$$q_{-1} + q_0 + q_1 = 1. \tag{3-21}$$

From equation 3-19, 3-20 and 3-21, we can obtain $q_{-1}=q_0=q_1=1/3$.Substituting these values into equation 3-15 and 3-16 and using the definition of equation 3-9, the equivalence gain of the binary phase detector is

$$K_{bpd} \approx \frac{1}{\sigma_{tj}\sqrt{2\pi}}\left[1+e^{-\frac{1}{2}\left(\frac{K_{pd}}{Nf_{REF}\sigma_{tj}}\right)^2}\right] \tag{3-22}$$

It should be noted that the above gain expression is defined in the unit of (sec)-1. It can be simply converted to the expression in the unit of $(rad)^{-1}$ by applying the relationship

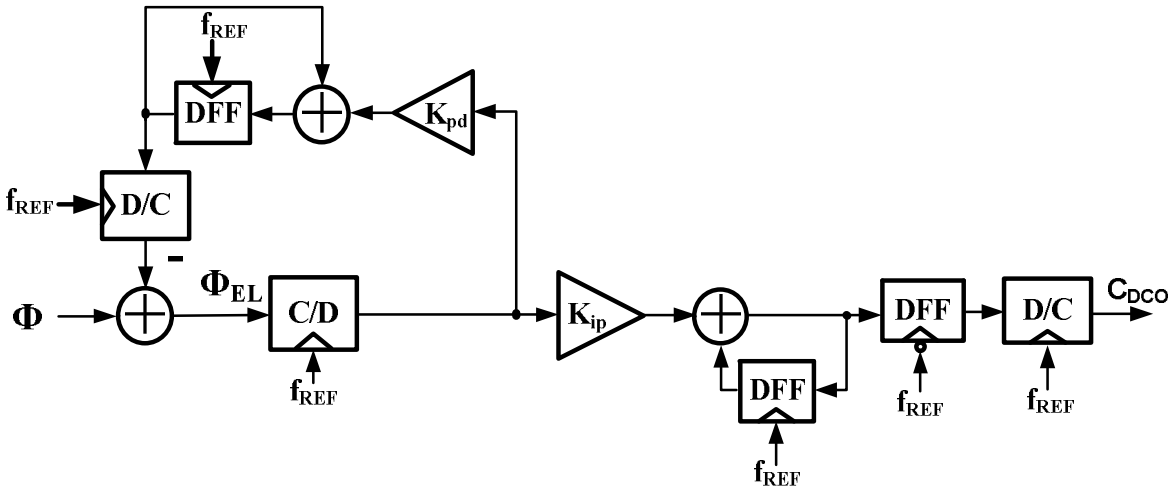
$$K_{bpd,\varphi} = \frac{K_{bpd}}{2\pi f_{REF}}, \tag{3-23}$$

so that

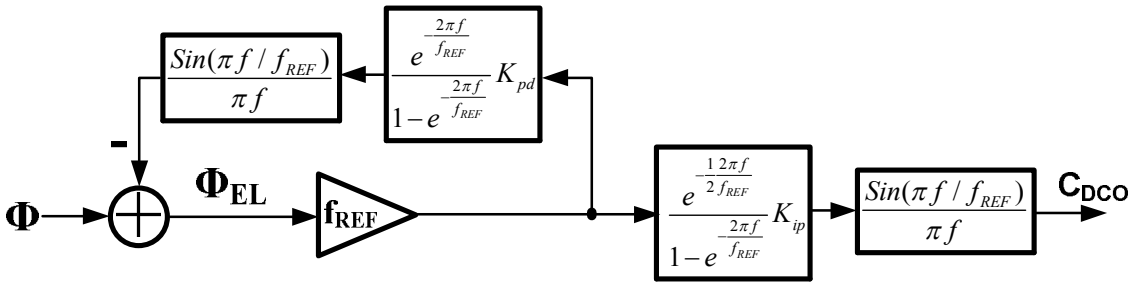
$$K_{BPD,\varphi} \approx \frac{1}{\sigma_{tj}(2\pi)^{\frac{3}{2}} f_{REF}}\left[1+e^{-\frac{1}{2}\left(\frac{K_{pd}}{Nf_{REF}\sigma_{tj}}\right)^2}\right]. \tag{3-24}$$

Fig. 3-12(a) and Fig. 3-12(b) show the discrete time model and the corresponding continuous time approximation of the digital loop filter and the additional negative feedback, respectively. Before the phase error output of the linearized phase detector, Φ_{EL}, is sent to the digital loop filter, the continuous-time signal, Φ_{EL}, is first sampled by the reference clock, which is indicated with the continuous-to-discrete-time (C/D) block. Assume that Φ_{EL} is a band-limited signal and the effect of aliasing is negligible. Then the sampling process can be replaced by a simple gain factor f_{REF}. In the discrete-time IIR filter, the delay in the loop is modeled by the z^{-1} operator defined as $z=\exp(j2\pi f/f_{REF})$.

In Fig. 3-12(a), the signal reconstruction process is represented as a discrete-to-continuous-time(D/C) block. Obviously the DCO holds the frequency constant until the digital loop filter changes its output value. Consequently, the output sequence of the digital filter is reconstructed by the zero-order-hold operation which can be expressed as a sinc function in frequency domain. Finally, the approximated frequency response of the digital loop filter and the additional negative feedback are



(a)



(b)

Fig. 3-12 (a) Discrete time model and (b) continuous time approximation of the digital loop filter.

$$H_{LF}(f)=\frac{K_{ip}e^{-j\frac{1}{2}\frac{2\pi f}{f_{REF}}}}{1\text{-}e^{-j\frac{2\pi f}{f_{REF}}}}\frac{\sin(\pi f/f_{REF})}{\pi f/f_{REF}}$$
$$H_{AF}(f)=\frac{K_{pd}e^{-j\frac{3}{2}\frac{2\pi f}{f_{REF}}}}{1\text{-}e^{-j\frac{2\pi f}{f_{REF}}}}\frac{\sin(\pi f/f_{REF})}{\pi f/f_{REF}} \quad . \qquad (3\text{-}25)$$

Fig. 3-13 shows the complete model of the ADPLL during bang-bang phase tracking mode, in which the DCO is modeled as integration operation with a gain $2\pi K_{DCO}$ and the relationship between the phase of the output signal φ_{OUT} and reference clock φ_{REF} is established by the multiplication ($\times N$) block, where $N=N_i+N_f$. The deviation of the loop transfer functions will be done according to the linear model and the phase noise performance will be analyzed later.

3.3.3 Generated Timing Jitter and Phase Noise

In general, the major noise sources of PLL are the external reference input noise and the internal oscillator natural noise. However, due to the presence of the bang-bang phase detector and the ΣΔ modulator, the noise introduced by the quantization operation must be taken into consideration.

In Fig. 3-14 the linearized model of the ADPLL is illustrated again including the internal and external noise sources. In particular $\varphi_{n,REF}$ is the phase noise on

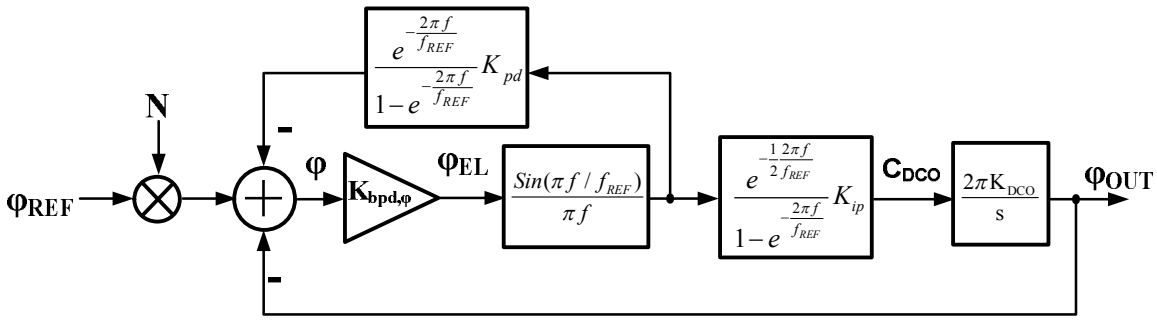


Fig. 3-13 Complete linearized model of the ADPLL during bang-bang phase tracking mode.

the input reference clock, $\varphi_{n,BPD}$ and $\varphi_{n,\Sigma\Delta}$ are the input referred noise due to the quantization of the binary phase detector and the ΣΔ modulator, respectively, and $\varphi_{n,DCO}$ is the phase noise on the DCO output produced by itself. It should be noted that only the deviation to their nominal value are considered for all the quantities in the analysis.

To find the total output noise of the ADPLL, the expression of the power spectral density (PSD) of each noise source is required. Since the signal generator is used for generating the reference clock in the practical implementation of the ADPLL, the phase noise PSD of the reference clock can be estimated as following expression according to the signal generator specifications [8]. The PSD of reference clock is estimate as:

$$S_{\varphi_{n,REF}}(\Delta f) = -132\,(\text{dBc/Hz}). \tag{3-26}$$

In our analysis, the BPD is modeled as a linear block with a gain $K_{bpd,\varphi}$. In order to emulate the quantization effect of the BPD, a input refer jitter is introduced and defined as

$$\varphi_{n,BPD} = \frac{\text{sgn}(\Delta\varphi) - K_{bpd,\varphi}\Delta\varphi}{K_{bpd,\varphi}} = \frac{\text{sgn}(\Delta\varphi)}{K_{bpd,\varphi}} - \Delta\varphi. \tag{3-27}$$

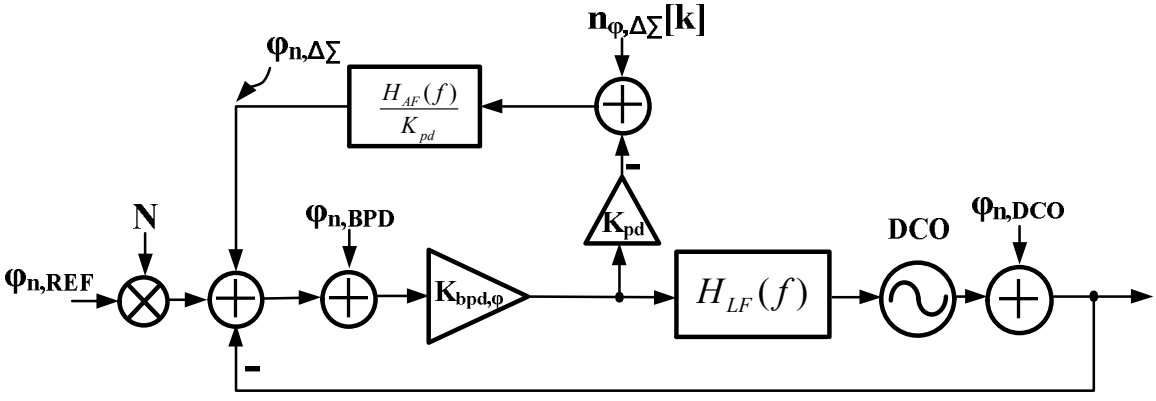


Fig. 3-14 Simplified linearized model of the ADPLL during bang-bang phase tracking mode with internal and external noise sources.

To find the total output phase noise, an approximation of the PSD of $\varphi_{n,BPD}$ is needed. In general, if the jitter of the reference clock is smaller than the BBPLL quantization step K_{pd}/Nf_{REF}, the BBPLL behaves like a first order ΔΣ modulator having a one bit quantizer with step $2K_{pd}/Nf_{REF}$. Thus, $\varphi_{n,BPD}$ can be approximated as a white process with uniform distribution and variance $(2K_{pd}/Nf_{REF})^2/12$. However, if the jitter of the reference clock increases, the ΔΣ loop will be overload and result in slewing [9]. Therefore the variance of $\varphi_{n,BPD}$ will increase. To obtain the expression of its variance for larger input jitter, the approach proposed in [9] is resorted to simulation results. It shows that the jitter introduced by the BPD has a standard deviation which is roughly 3/4 of the standard deviation of the input jitter. From the above discussion, the PSD of the noise produce by the BPD can be defined as [9]

$$S_{\varphi_{n,BPD}}(\Delta f) = \max\left\{\frac{(2\pi)^2 f_{REF}\left(K_{pd}/Nf_{REF}\right)^2}{3}, \left(\frac{3}{4}\right)^2 S_{\varphi_{n,REF}}(\Delta f)\right\} \qquad (3\text{-}28)$$

As for the quantization noise of the ΣΔ modulator, $n_{\varphi,\Delta\Sigma}[k]$ is integrated by $\frac{H_{AF}}{K_{pd}}$ to transfer to phase quantization noise, $\varphi_{n,\Delta\Sigma}$, and the PSD result of $\varphi_{n,\Delta\Sigma}$ can be expressed as[13]:

$$S_{\varphi_n,\Delta\Sigma}(\Delta f) = \frac{1}{12}\times\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \times \frac{1}{f_{REF}} \times \left(2\sin\frac{\pi\Delta f}{f_{REF}}\right)^{2n}, \qquad (3\text{-}29)$$

In equation 3-29, Δf_{res} is the quantization step which indicates the corresponding frequency deviation of one ΣΔ modulator control code, Δf is the offset frequency from the carrier, f_{REF} is the reference frequency, and n is the order of the ΣΔ modulator. Due to the noise shaping capability of the ΣΔ modulator, the quantization noise energy induced by the finite frequency step Δf_{res} is moved toward the high frequency offset at the RF output. With careful

design, the output phase noise contributed from the quantization error of the ΣΔ modulator should decrease while the offset frequency increases, and it must be made below the output phase noise resulted from the reference clock.

Finally, the phase noise of the DCO $\varphi_{n,DCO}$ and its PSD will be derived. Although the profile of the DCO phase noise can be easily obtained from simulation results, the analytic approximation may give more insight about the generation of phase noise in the circuit design phase. Consider the differential LC tank cross-coupled pair oscillator. The generated phase noise can be express as [10]

$$S_{\varphi_{n,DCO}}(\Delta f) = \frac{\overline{i_n^2}/\Delta f}{q_{\max}^2} \frac{\Gamma_{rms}^2}{8\pi^2 \Delta f^2}, \tag{3-30}$$

where $\overline{i_n^2}/\Delta f$ is the PSD of the equivalent parallel current noise, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) associated with that noise source, q_{max} is the maximum signal charge swing which is defined as the product of the tank capacitance and maximum signal swing $C_{tank}V_{swing}$, and Δf is the the offset frequency from the carrier.

In a simplified stationary approach, the total noise power of the tank is mainly due to the cross-coupled transistor pair and the ohmic losses in the tank inductor:

$$\overline{i_n^2}/\Delta f \approx 2kT\gamma\mu_n C_{ox} \frac{W}{L} V_{ov} + \frac{4kT}{R_p}, \tag{3-31}$$

where $R_p \approx 2\pi f_{osc} L_{tank} Q$ is the equivalent parallel resistance at the frequency of oscillation f_{osc}, T is the temperature, k is Boltzmann constant, μ_n is the mobility of the carriers in the channel, C_{ox} is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor, respectively, and V_{ov} is the gate drive of the MOS transistor. γ, however, may be between two and three in the

short-channel devices. For simplicity, the output waveform can be assumed to be a sinusoidal waveform so that $(\Gamma_{rms})^2$ equals to 0.5 [10].

From the model shown in Fig. 3-14, it is straightforward to calculate the total output phase noise by summing the contributions of the different noise sources:

$$S_{\varphi_{n,OUT}}(\Delta f) = \left[S_{\varphi_{n,REF}}(\Delta f) + S_{\varphi_{n,BPD}}(\Delta f)\right] \cdot \left|H_{REF,OUT}(\Delta f)\right|^2 + S_{\varphi_{n,DCO}}(\Delta f) \cdot \left|H_{DCO,OUT}(\Delta f)\right|^2 + S_{n[k],\Sigma\Delta}(\Delta f) \cdot \left|H_{\Sigma\Delta,OUT}(\Delta f)\right|^2 . \quad (3\text{-}32)$$

$H_{REF,OUT}(\Delta f)$, $H_{DCO,OUT}(\Delta f)$, and $H_{\Sigma\Delta,OUT}(\Delta f)$ denote the transfer function from reference signal to PLL output, from DCO output to PLL output and from ΣΔ modulator which can be found by inspecting Fig. 3-14. Thus the transfer functions are

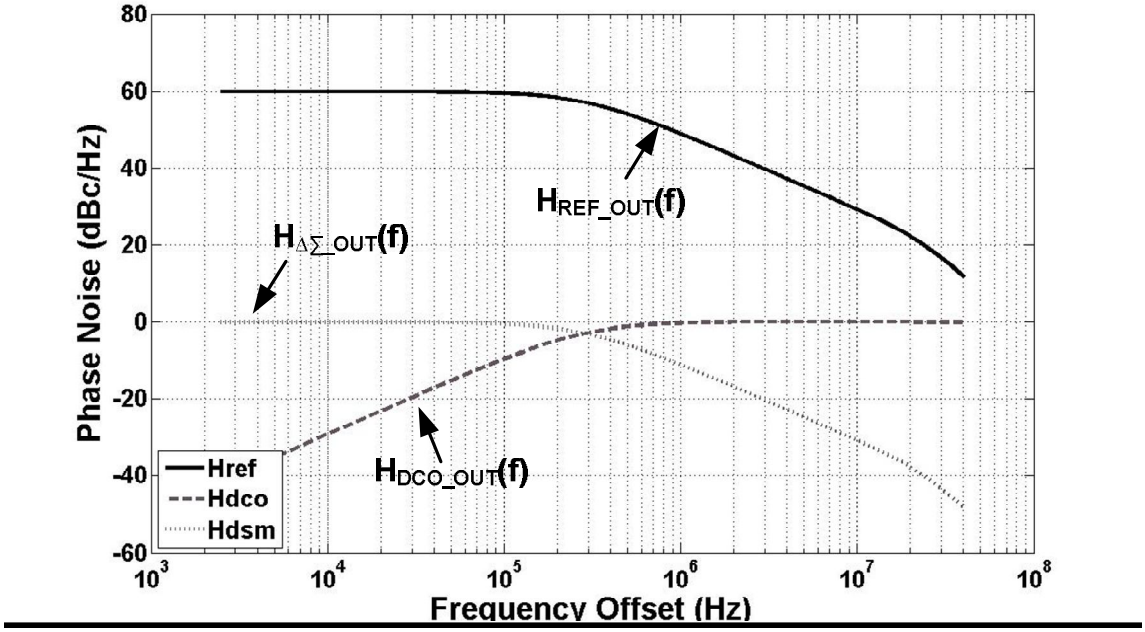
$$H_{REF,OUT}(\Delta f) = N \frac{K_{DCO}K_{BPD,\varphi}H_{LF}}{(1+K_{BPD,\varphi}H_{AF})j\Delta f + K_{DCO}K_{BPD,\varphi}H_{LF}} = H(\Delta f), \quad (3\text{-}33)$$

$$H_{DCO,OUT}(s) = \frac{(1+K_{BPD,\varphi}H_{AF})j\Delta f}{(1+K_{BPD,\varphi}H_{AF})j\Delta f + K_{DCO}K_{BPD,\varphi}H_{LF}} = 1 - \frac{H(\Delta f)}{N}, \quad (3\text{-}34)$$

and

$$H_{\Sigma\Delta}(\Delta f) = \frac{K_{DCO}K_{BPD,\varphi}H_{LF}}{(1+K_{BPD,\varphi}H_{AF})j\Delta f + K_{DCO}K_{BPD,\varphi}H_{LF}} = \frac{H(\Delta f)}{N}. \quad (3\text{-}35)$$

As an example, Fig. 3-15 shows the transfer functions and the output phase noise for the case with following loop parameters: f_{REF}=40MHz, N=1000.1, $K_{DCO}K_{ip}$=7200, K_{pd}=0.004, DCO free running frequency is 40.004 GHz. The result shows the loop bandwidth is about 300kHz. The result also reveals that the output phase noise at lower frequency is dominated by reference noise while it is affected by all DCO phase noise, reference noise, and ΣΔ modulator noise at higher frequency.



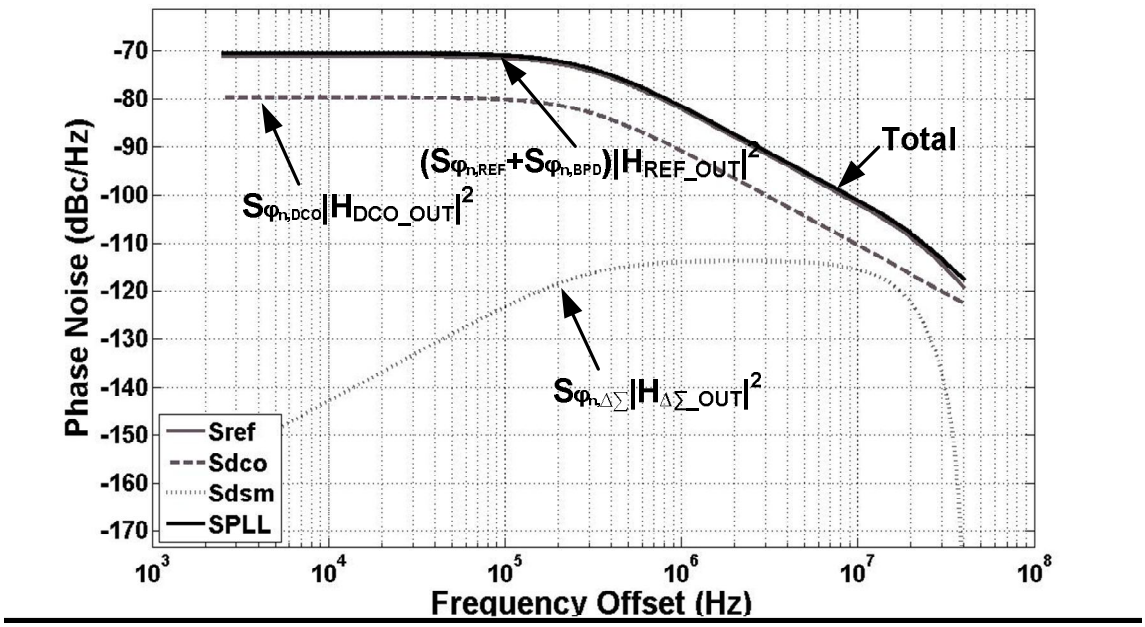


Fig. 3-15 Example computation of ADPLL transfer functions and contribution of each noise source.

Chapter 4 Design and Implementation of the ADPLL

4.1 Block Diagram of the ADPLL

A prototype of the ADPLL has been designed and fully integrated in UMC 90nm CMOS process with 9 metal layers (1P9M). The detailed block diagram of the implemented ADPLL is shown in Fig. 4-1.

The dual mode phase detector (DPD) senses the phase difference between a reference signal (f_{REF}) and feedback signal from digitally controlled oscillator (DCO) by subtracting the output of phase accumulator 2 (PAC2) from that of phase accumulator 1 (PAC1). The phase information of reference signal is estimated by PAC1 which accumulating the total frequency control word N/16, where $N/16= N_i+ N_f$, at every rising edge of the reference signal. At the same time, PAC2 measures the phase information of DCO output signal by counting the number of the rising edge of the divide-by 16 DCO clock f_{DIV16}. The counted value is captured by a register at each reference cycle.

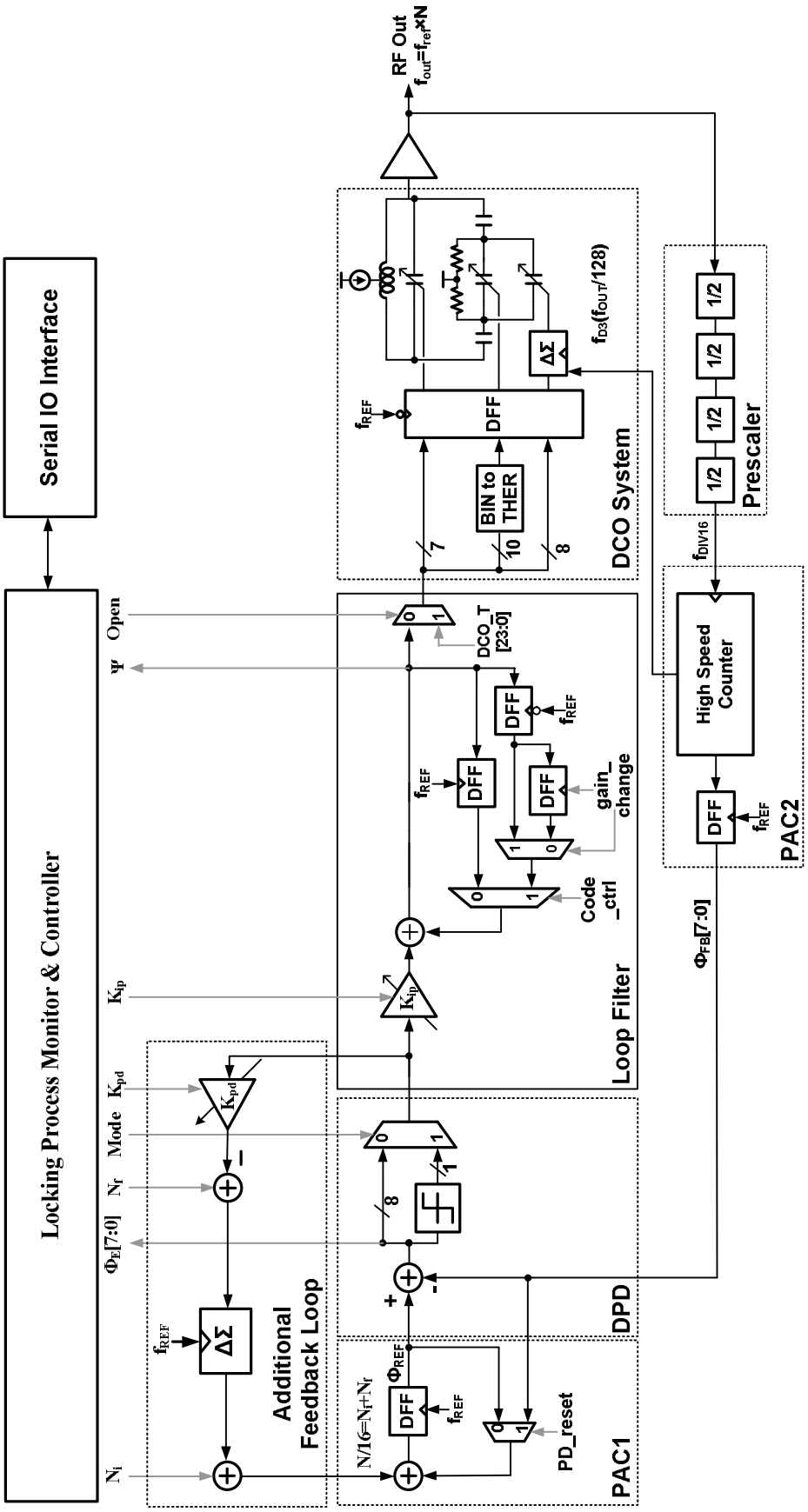


Fig. 4-1 Block diagram of the implemented ADPLL

The DPD sends the phase difference information into the additional feedback loop, which consists of a programmable gain (K_{pd}) and a ΣΔ modulator, and the loop filter, which is a digital integrator with programmable integral gain (K_{ip}). The additional feedback path adds the output of the ΣΔ modulator, which is an integer series but the average of the series is the fractional frequency multiplication factor (N_f), and the integer frequency multiplication factor (N_i), and then sending the result into the PAC1 as the total frequency multiplication factor. As for the loop filter, it processes the phase error information and generates the control code for the DCO. The DCO adjusts the output frequency according to the control code and produces RF signal to output buffer. The frequency of high speed clock signal generated by DCO is then reduced by four stages of divide-by 2 frequency divider and the divided clock signal is fed back to PAC2.

In order to achieve dual mode operation and dynamically loop gain adjusting for fast locking, many multiplexer are inserted into the data paths of the loop. The operation modes and loop gain parameters are controlled by the LPM. In order to test only the isolated DCO performance, a multiplexer has been introduced before the digital input of the DCO. In this way the DCO output frequency can be controlled externally and important properties such as the DCO tuning range and its tuning curves can be easily measured. For measurement considerations, the loop parameters and operation modes can be programmed by the control signals outside of the chip. Loop states and variables can also be read out by the instruments through output ports. In order to reduce the number of pins and occupied chip area, a simple serial-to-parallel interface is used to communicate with external testing instruments.

Owing to most of the building blocks, excluding the DCO, the prescaler and

PAC2, are in digital manner, those circuits can be implemented straightforwardly with the conventional cell-based flow. By introducing the CAD tools in the design flow, design automation techniques including logic synthesis, automatic placement and routing can be utilized to accelerate design cycle of the chip. In the following sections, the most critical building blocks of the ADPLL will be investigated in more detail.

4.2 Phase Detection Circuits

The complete phase detection mechanism includes PAC1, PAC2 and DPD as shown in Fig. 4-2. Although the phase information of DCO output can be estimated by directly counting the number of the arrival rising edge of DCO output, it is difficult to design a counter which can work at such high frequency and the power consumption of the counter may become unacceptable. Thus, a prescaler which divides the DCO output frequency by 16 is inserted between the high speed counter and the DCO output [14].

The high speed counter counts the number of the arrival rising edge of the

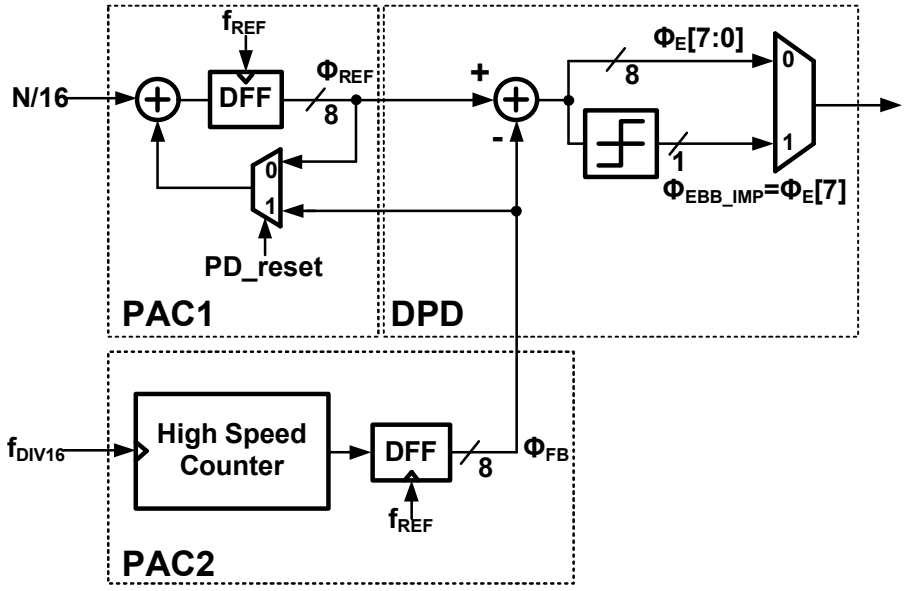


Fig. 4-2 Block diagram of the phase detector

divided signal f_{DIV16} and produces the counter value Φ_{FB} when the rising edge of reference clock f_{REF} arrives. To calculate the phase difference information Φ_E, a subtractor which subtracts the feedback phase information Φ_{FB} from the reference phase information Φ_{REF} is placed after PAC1 and PAC2.

As described in Fig. 4-2, the output of the subtractor is separated into two signal paths. The quantizer connected after the subtractor generates a single bit output Φ_{EBB_IMP} form the phase difference information Φ_E. The binary phase error signal Φ_{EBB_IMP} implemented as the sign bit of the phase difference signal Φ_E and the relation between them can be expressed as following equations:

$$\Phi_{EBB\_IMP} = \begin{cases} 0 \text{ if } \Phi_E \geq 0 \\ 1 \text{ if } \Phi_E < 0 \end{cases}. \quad (4\text{-}1)$$

From this equation, it should be noted that the output of Φ_{EBB_IMP} is 0 or 1 rather then -1 or 1. The reason for it is to simplify the multiplication operations in loop filter and more detail descriptions will be given in section 4.3.

Due to the settling time during PT mode is largely determined by the initial phase error and frequency offset, the starting point of the bang-bang phase locking operation is important and the perturbation caused by the switching between different modes should be minimized. When the loop is in steady-state condition at the end of the fast frequency acquisition process, the DCO control code is stored to a register as the operation mode is changed from the FA mode to the PT mode. This saved DCO control code corresponding to the target oscillation frequency is loaded to the register of integral path in loop filter as the loop entering the PT mode. Simultaneously, the output of phase detector is reset to 0 by equalizing the two input signals of the subtractor. This operation can be achieved by introducing a multiplexer before the register of reference phase accumulator and setting the control signal PD_reset to high.

4.2.1 Modulo arithmetic of the phase detection circuit

Due to the practical limitation of the word length of the arithmetic components, PAC1 and PAC2 are implemented in modulo arithmetic [11]. The reference and feedback phase information, Φ_{REF} and Φ_{FB}, respectively, are linear and grow without bound with the development of time. However, the registers of accumulators can not hold unbound values and the stored values are restricted to the range of 0 to 2^{υ}-1, where υ represents the bit length of the accumulator, and the accumulator will overflow when the accumulated value reaches the upper bound. If the carry-out bits of the accumulator are simply disregarded, the behavior of the accumulator can be modeled as an ideal accumulator followed by a modulo-υ operator as illustrated in Fig. 4-3. After considering the effect of limited bit length of the accumulators, a block diagram representing the simplified phase detector is shown in Fig. 4-4.

In Fig. 4-4, the reference and feedback accumulators are replaced with two ideal accumulators and modulo-2^{υ} arithmetic units. The signals, Φ_{REFO} and Φ_{FBO}, represent the ideal reference and feedback phase information, respectively. To get a clear insight into the characteristics of the architecture, the modulo arithmetic on Φ_{REFO} and Φ_{FBO} could be visualized as two rotating vectors as shown inFig. 4-5. In this figure, Φ_{REF} and Φ_{FB} are positive numbers which have a maximum possible value of (2^{υ}-1) without rollover. If the output of the subtractor is treated as a 2's compliment number, the phase detector output Φ_E has the same range but

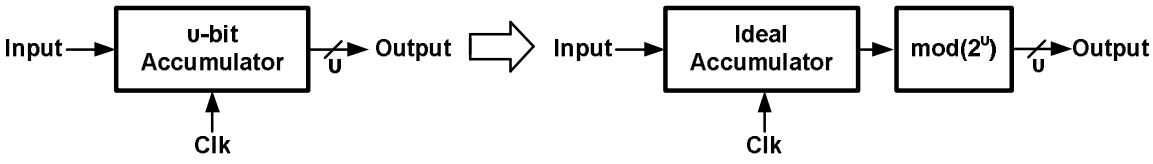


Fig. 4-3 Behavior model of υ-bit accumulator.

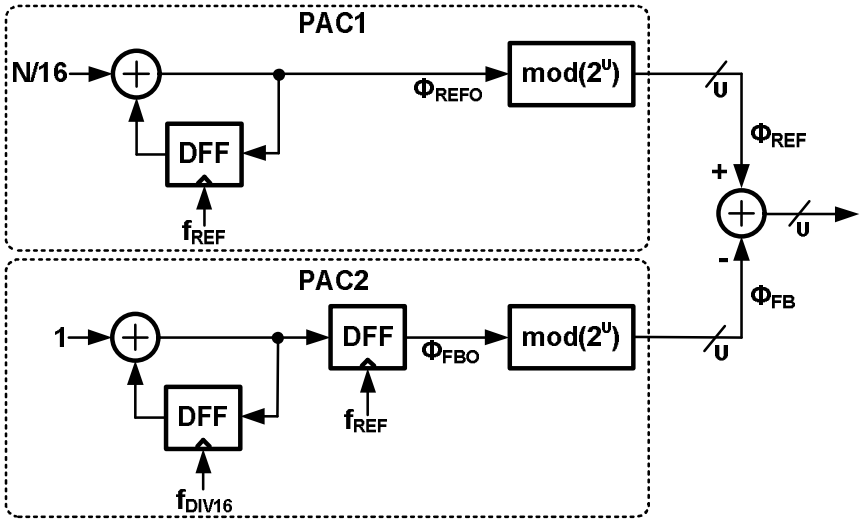


Fig. 4-4 Simplified modulo block diagram of phase detector.

is symmetric around zero. It can be shown that the value of Φ_E lies within $[-2^{(\upsilon-1)}, 2^{(\upsilon-1)}-1]$ and invariably the phase detector output Φ_E indicates the smaller angle between the two vectors.

Due to the modulo arithmetic, the phase detector is not only the arithmetic subtractor of two numbers but also performs a cyclic adjustment as suggested by Fig. 4-5. For the phase detector output to be corresponding to the phase error in perspective, the difference between Φ_{REFO} and Φ_{FBO} should be restricted to the range of $[-2^{(\upsilon-1)}, 2^{(\upsilon-1)}-1]$. Under this limitation, the output of phase detector can be expressed as

$$\Phi_E = \Phi_{REFO} - \Phi_{FBO} \quad when \quad -2^{(\upsilon-1)} \le (\Phi_{REFO} - \Phi_{FBO}) \le 2^{(\upsilon-1)} - 1. \qquad (4\text{-}2)$$

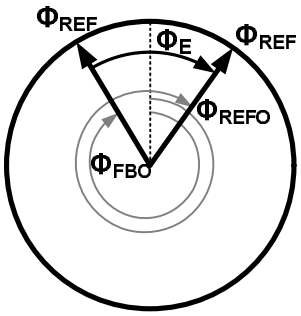


Fig. 4-5 Rotating vector interpretation of the reference and feedback phases.

From equation 4-2 it can be shown that under this condition, the output of phase detector Φ_E is simply an arithmetic subtraction of the two outputs of reference and feedback accumulators. From the design point of view, this condition sets the upper bound of the frequency offset between the target frequency and DCO output frequency ($f_{REF}N$-f_{OUT}). Assuming the initial phase error Φ_E is 0 and the DCO output frequency is f_{OUT}. At the next rising edge of reference clock (f_{REF}), the values of PAC2 and PAC1 increase by N/16 and $f_{OUT}/16f_{REF}$, respectively. To avoid aliasing, the following condition must be met:

$$\begin{aligned} &-2^{(\upsilon-1)} \le \left(\frac{N}{16} - \frac{f_{OUT}}{f_{REF}16} \right) \le 2^{(\upsilon-1)} - 1 \\ &\Rightarrow -f_{REF}\, 2^{(\upsilon+3)} \le \left(f_{TARGET} - f_{OUT} \right) \le f_{REF}\, 2^{(\upsilon+3)} - 1 \end{aligned} \quad , \qquad (4\text{-}3)$$

where $f_{TARGET}=Nf_{REF}$ is the target frequency. It should be noted that during fast frequency acquisition process, the absolute value of the phase error (Φ_{REFO}-Φ_{FBO}) might raise over the upper bound even if the condition mentioned in equation 4-3 is met. Neglecting the overshooting behavior during locking process, the phase detector output should be settled to some value within $[-2^{(\upsilon-1)}, 2^{(\upsilon-1)}-1]$:

$$\begin{aligned} &f_{OUT} = f_{DCO,free} + K_{DCO} K_{ip,FA} \Phi_E \\ &\Rightarrow -2^{(\upsilon-1)} \le \frac{Nf_{REF} - f_{DCO,free}}{K_{ip,FA} K_{DCO}} \le 2^{(\upsilon-1)} - 1 \end{aligned} \qquad (4\text{-}4)$$

In equation 4-4, $K_{ip,FA}$, $K_{DCO,}$ $f_{DCO,free}$ are transferred integral path gain in fast frequency acquisition mode, DCO gain and DCO free running frequency, respectively.

The possibility of aliasing due to the modulo arithmetic during PT process should be also taken into consideration. Assuming the DCO output frequency f_{OUT} equals to the target frequency Nf_{REF}, the range of the phase offset between reference and feedback phase normalized to reference clock period can be

expressed as

$$\frac{-2^{(\upsilon-1)}}{N}\cdot 32\pi \le \varphi \le \frac{2^{(\upsilon-1)}-1}{N}\cdot 32\pi\,, \qquad (4\text{-}5)$$

which has been discussed in chapter 3.

In the implementation of the ADPLL, the bit length of the reference and feedback accumulators must be made sufficiently large to ensure that the conditions list in equations 4-3, 4-4 and 4-5 would be always met. In the design presented in this thesis, two 8-bit accumulators are utilized to construct the PAC1 and PAC2.

4.2.2 PAC2

As shown in Fig. 4-1, the PAC2 is implemented as a high speed counter with the rollover effect as described above. The counter can be implemented quite easily using register-type circuits such as the flip-flops, and a wide variety of design exists. There are two major types of flip-flop based counter according to the clocking mechanism of the registers, namely asynchronous counter and synchronous counter.

The simplest asynchronous counter circuit is a D type flip-flop with input fed from its own inverted output. This counter increase once for every clock cycle and takes two clock cycles to overflow, so every cycle the output of the counter will alternate between 0 and 1. It should be noted that the counter creates an output clock at exactly half the frequency of the input clock and hence it also perform a divide-by 2 operation. The generated signal can clock the next counter stage if more than one stage is connected in series to extend the range of the counter.

An example of a 4-bit asynchronous down counter along with its time diagram is illustrated in Fig. 4-6. This down counter can be easily transformed to an up counter by simply inverting the output of each stage (Q_1~Q_4). Note that it can be shown from Fig. 4-6 that each counter stage working at half of the frequency of previous stage and the rising edge of each output (Q_1~Q_4) does not align to each other. The existence of the unavoidable propagation delay of the flip-flop results in the unstable outputs as the overflows "ripple" from stage to stage. In the case where the instantaneous count is important, the timing skew between stages will cause incorrect counting results. Besides, the increasing of the input frequency and the counter length will worsen the situation. If each stage of the output of an asynchronous counter is sampled by the same clock phase, for an L bits asynchronous counter with the D flip-flop which have a clock to output delay of t_{c-q} and a setup time of t_{setup}, the maximum operating frequency $f_{in,max}$ can be expressed as

$$f_{in,\max} = \left(Lt_{c-q} + t_{setup}\right)^{-1}. \tag{4-6}$$

To solve this issue in the applications where a stable count value is important across several bits, the synchronous counters could be used. Compared with the asynchronous counters in which each flip-flop is triggered by the output

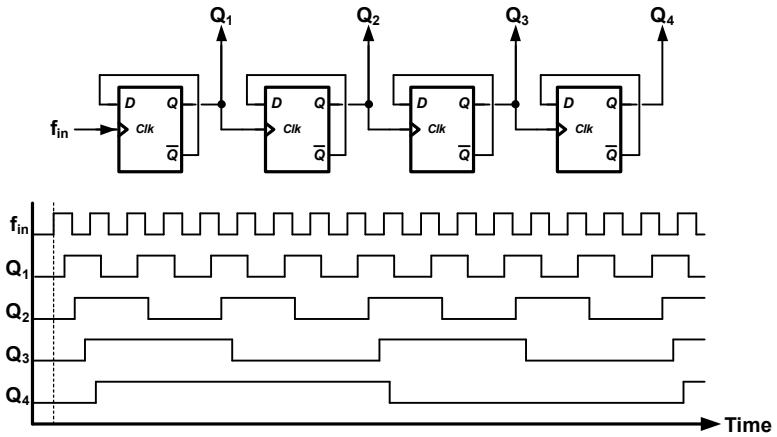


Fig. 4-6 Asynchronous counter.

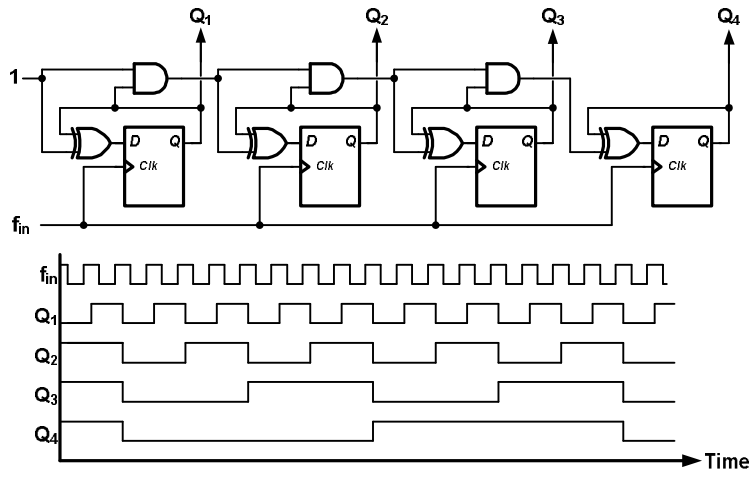


Fig. 4-7 Synchronous counter.

of the preceding stage, the flip-flops of synchronous counters are all triggered by the same clock source. Fig. 4-7 shows a 4-bit synchronous counter composed of logic gates and flip-flops. The time diagram of the counter is also shown in Fig. 4-7 and it can be observed that the signal edge of each stage (Q_1~Q_4) is aligned to the input clock f_{in}. The synchronous output of this counter solves the issue of unsettled output; however, carrier signal propagates in asynchronous counter circuit at the expense of larger power consumption because all the flip-flops in the synchronous counter circuit operate at the frequency which is as high as input clock frequency, so the synchronous counters consume much more dynamic power than asynchronous counters. In addition to the issue of power consumption, the synchronous also suffer the problem of slower operating speed because the maximum operation speed for a L bit synchronous counter can be determined by the time for the carrier signal to propagate from the first stage (LSB) to the last stage (MSB) and could be derived as:

$$f_{in,\max} = \left[t_{c-q} + (L-1)t_{AND} + t_{XOR} + t_{setup}\right]^{-1}, \qquad (4\text{-}7)$$

where $t_{c\text{-}q}$, t_{setup}, t_{AND} and t_{XOR} are the clock to output delay of the flip-flops, the setup time of the flip-flops, the gate delay of the AND gate, and the gate delay of the XOR gate, respectively.

To solve the edge skewing issue and preserve the advantages of high speed operation and low power consumption of the asynchronous counter, a skew-insensitive high speed counter is proposed [14]. The complete block diagram and time diagram of the high speed counter is shown in Fig. 4-8. In this design, the counter consists of a serial of 1-bit counter cells which is composed of a basic 1-bit flip-flop based asynchronous counter, a D type latch to perform sample phase generation and a D type flip-flop to fetch the output from the 1-bit asynchronous counter. Furthermore, it should be noted that the 5 MSBs asynchronous outputs f_{D4}-f_{D8} are sampled by the same signal S_4. From the simulation results, the delay time of the sampling signal S_4 satisfies the time

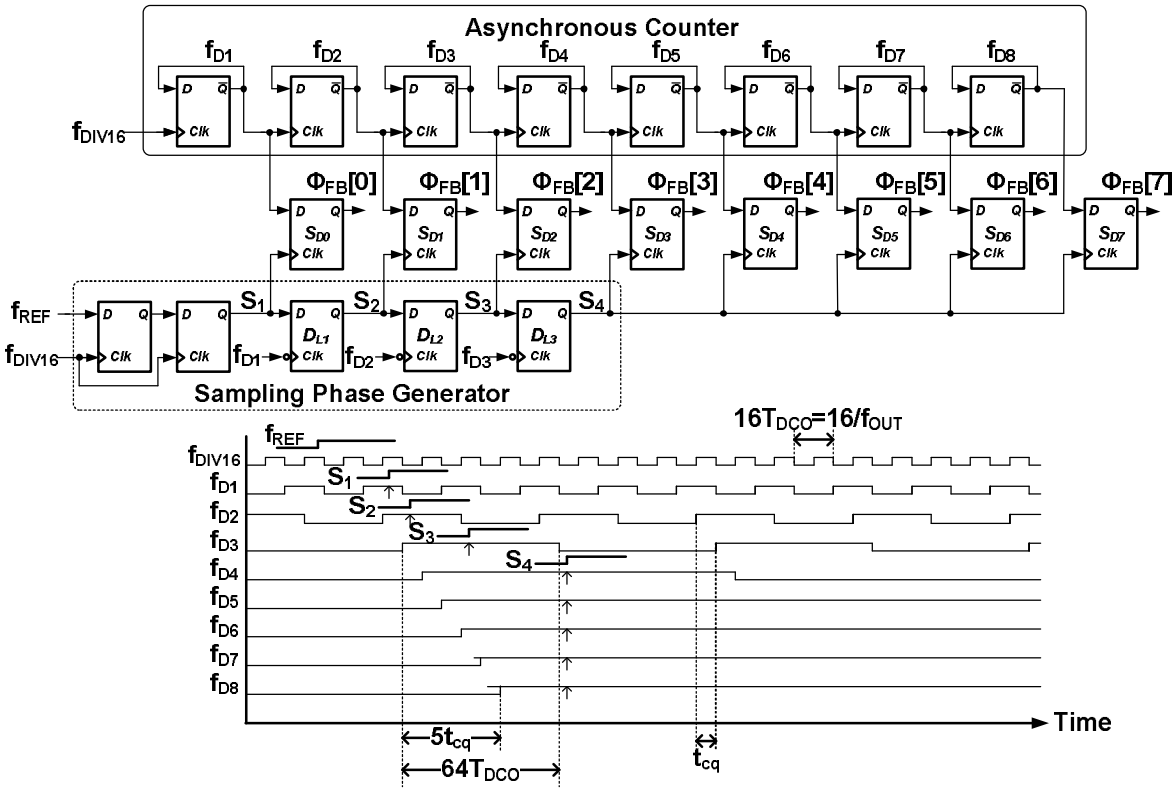


Fig. 4-8 Bock diagram and time diagram of the proposed high speed counter.

requirement for the “carry” signal to propagate from the fourth stage to the last stage of the divider chain, so further generation of the sampling phase is unnecessary.

In addition, due to the non-bound relationship between f_{REF} and f_{DIV16}, it is quite likely that under certain condition, the flip flop may face the metastability problem. During metastability, the output of the flip flop could be undefined at a given clock cycle which is not acceptable for proper system operation. This problem can be solved by passing the lower frequency signal through a series of flip flops which are clocked by the higher frequency clock. The overall probability of metastability condition at output of the system decreases exponentially with the number of the flip flop. Furthermore, the probability of a metastable state of a single flip flop can be reduced by increasing the speed of the flip flop. In order to reduce the probability of a metastable state, the first stage of sampling phase generator in [14] is performed by a pair of sense amplifier based flip flops [12], and Fig. 4-9 shows the schematic of the sense amplifier based flip flop. The advantages of this topology are the fast response time and low power consumption.

When f_{REF} comes into fetch the information of PAC2, the sampling phase S_1 for the 1st stage of the asynchronous counter is generated by resampling f_{REF} through 2 D flip-flops to avoid metastability. S_1 is then postponed by D-latchs D_{L1}-D_{L3}, which are triggered by the falling edge of the 1st – 3rd stage divider outputs f_{D1}-f_{D3}, to generate the sampling phases S_2 – S_4. Thus, a minimum setup time of $4T_{DCO}$-t_{cq} can be guaranteed when retrieving the contents of the ripple counter.

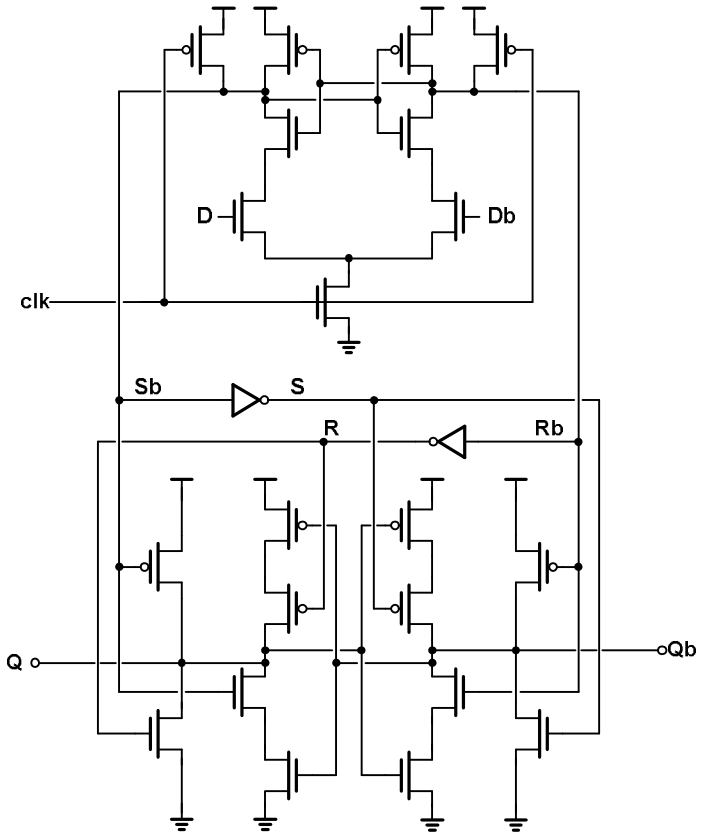


Fig. 4-9 Schematic of the tactical flip flop [12]

4.3 Additional Feedback Loop, Digital Loop Filter and LPM

The additional feedback loop is composed of a programmable gain (K_{pd}) and a ΣΔ modulator as shown in Fig. 4-1. The data path of the ΣΔ modulator is 10 bits wide and represented in two's complement arithmetic, and Fig. 4-10 illustrates the block diagram of the detail implementation of the additional feedback loop. In addition, several multiplexers are used to simplify the operation of PLL. In the beginning of locking, K_{pd}_zero_gain sends 1 when PLL is in frequency acquisition mode and sends 0 later when PLL is in phase tracking mode. It should be noted that the multiplied by K_{pd} and - K_{pd} operation is also replaced by selecting the positive or negative value from multiplexer inputs for easy

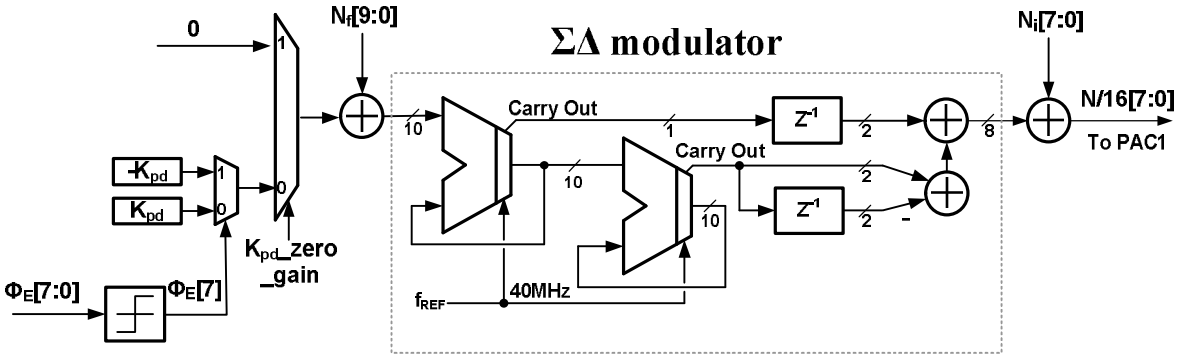


Fig. 4-10 Implementation of the additional feedback loop

implementation. After going through the bang-bang operation, the output of DPD is quantized as the multiplexer input to select K_{pd}. Subtracts the selected K_{pd} value from the fractional frequency multiplication factor (N_f) and sends the result into the ΣΔ modulator. The ΣΔ modulator is implemented as digital second-order MASH-type architecture [13] which can be conveniently realized in digital domain by cell based design flow. Its output is fed to add together with integer frequency multiplication factor (N_i) and then the consequence is sent into the PAC1 as the total frequency multiplication factor (N).

The digital loop filter is an integral path with programmable gain (K_{ip}) as shown in Fig. 4-1, and the data path in the loop filter is 24 bits wide and represented in two's complement arithmetic. Fig. 4-11 illustrates the block diagram of the detail implementation of the digital loop filter. As mentioned before, the multiplied by K_{ip} and - K_{ip} operation is replaced by selecting the positive or negative value from multiplexer inputs. In order to perform the dynamic loop parameters and modes switching, several multiplexers are introduced in the loop filter. The activity of the loop filter incorporated with these multiplexers during the locking process will be described as following.

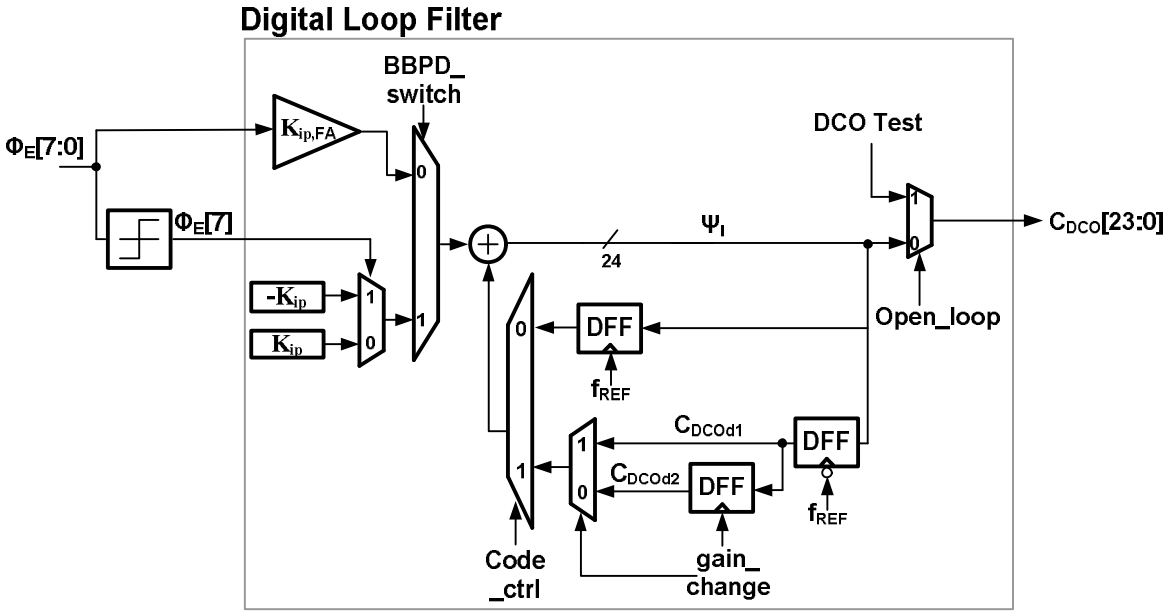


Fig. 4-11 Implementation of the digital loop filter

At the beginning of the locking process, all memory elements are reset synchronous by asserting a control signal. At first, LPM cuts the additional feedback, disables the accumulator in the digital loop filter, and transfers the loop gain to a programmable gain $K_{ip,FA}$ by set K_{pd}_zero_gain to 1, Code_ctrl to 1, and BBPD_switch to 0, respectively. During the FA mode, the output of the phase detector Φ_E is scaled by a value $K_{ip,FA}$ and the output of the digital loop filter first controls the coarse tune bank. After the loop finish the first FA state, the output of the digital loop filter controls the fine tune bank secondly. The scaling operation is implemented in an efficient manner as programmable right-bit-shift operation. To further enhance the locking performance, the FA mode is divided into four stages, one for coarse bank tuning and three for fine tune bank tuning with different gain $K_{ip,FA}$.

At the beginning of this mode, a large gain $K_{ip,FA}$ is used to allow the output frequency to lock quickly and roughly to the target frequency. As mentioned in chapter 2, the time for the control circuit to perform gain scaling is determined by

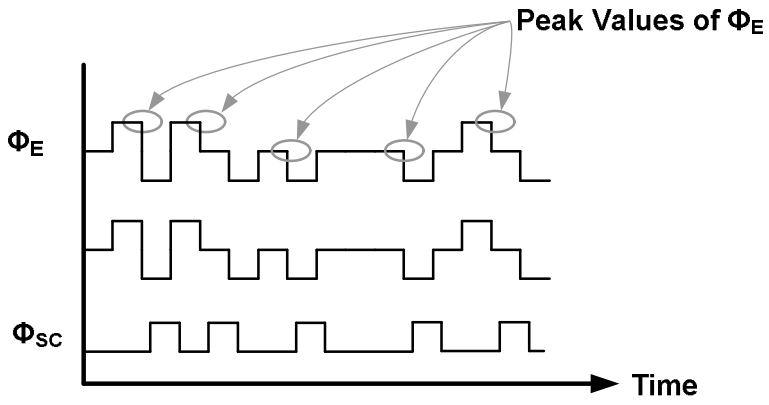
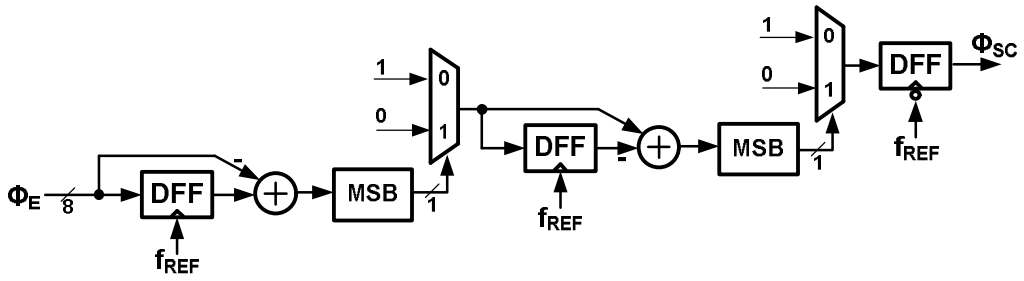


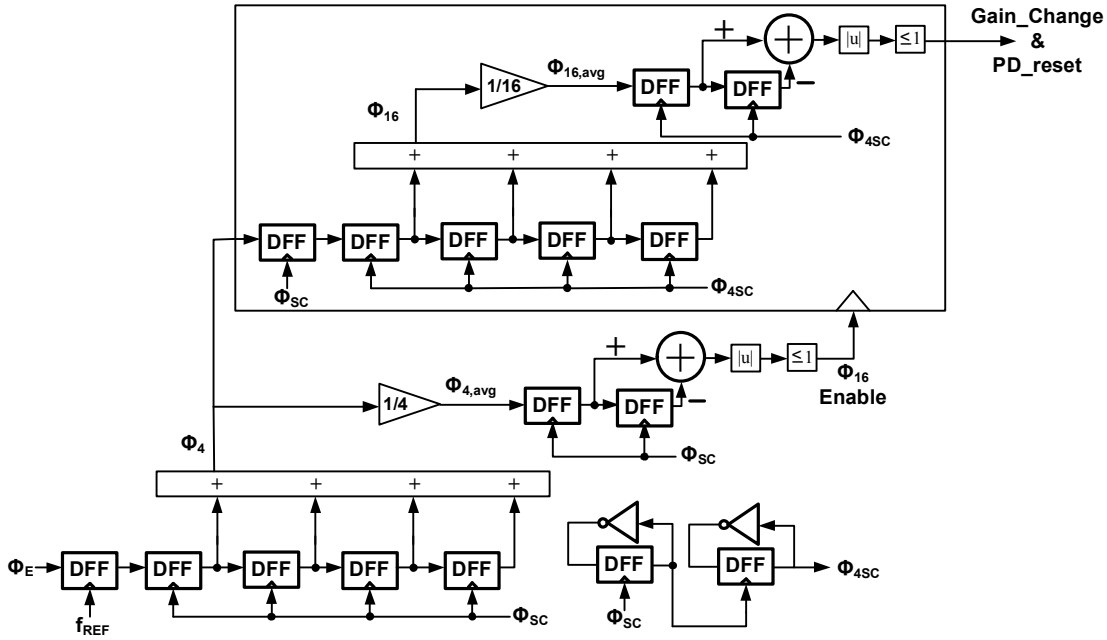
Fig. 4-12 Time diagram of the locking state in PT mode.

the existence of the locking state. The time diagram of Φ_E and Ψ in the locking state can be shown inFig. 4-12. It should be observed that the value of Φ_E is jumping in a small range just like Ψ is when the loop is in a locked state; therefore, this implies that if the loop reaches steady-state condition in FA mode, the behaviors of the peak values of Ψ and Φ_E are exactly the same, and since Φ_E also will stay in a small range, the trigger signal Φ_{SC} only has to sample the peak values of Φ_E, and then the existence of the locking state can be detected.

Fig. 4-13 shows the implementation of the sampling signal Φ_{SC} and the LPM system. The signal Φ_{SC} indicates that there is a top falling transition of the phase detector output Φ_E and also a local maximum value appears on Φ_E. Thus, this operation can be treated as the gradient polarity detector (GPD) of Φ_E. The peak holders store the peak values by using the signal Φ_{SC} to clock a shift register and send the stored value into the first 4-input adder. The result of the adder Φ_4, which is the total value of 4 neighbor peak values of Φ_E, is then averaged by a divide-by 4 operation to generate $\Phi_{4,avg}$, the average of 4 neighbor peak values of Φ_E. After extracting the difference of $\Phi_{4,avg}$ and the absolute value of the difference, if the absolute value is smaller or equals to 1, the 'Φ_{16} Enable' signal is generated to turn on the second locking detector.



(a)



(b)

Fig. 4-13 Implementation of (a) the sampling signal Φ_{SC} and (b)the LPM system.

This second locking detector consists of another set of holders which store the values of Φ_4 by using the signal Φ_{4SC} to clock a shift register, where the holder trigger signal, Φ_{4SC}, is the divide-by 4 sampling signal Φ_{SC}. Thus, the stored values of Φ_4 is sent into the second 4-input adder to form the total value of 4 neighbor values of Φ_4, Φ_{16}, and then the output of the second adder is divided by 16 to generate $\Phi_{16,avg}$, the average of 16 neighbor peak values of Φ_E. Just like

the processes mentioned above, after extracting the difference of $\Phi_{16,avg}$ and the absolute value of the difference, if the absolute value is smaller or equals to 1, the gain_change and PD_reset signal are transferred from 0 to 1, so the new $K_{ip,FA}$ is loaded and PAC1 is reset to PAC2, and then LPM comes into the new observation of FA mode.

When the digital loop goes into the next FA mode, the DCO control code C_{DCO} is stored to the first temporary register as C_{DCOd1} by the falling edge of the reference clock. Furthermore, because C_{DCOd1} is connected to a multiplexer which is controlled by gain_change signal and gain_change is set to 0 to block C_{DCOd1} from the next stage and C_{DCOd2}, the second temporary register controlled by gain_change, still stores the initial value, the output of the multiplexer controlled by Code_ctrl is still C_{DCOd2}. However, when the LPM determines to change the gain, the digital loop filter comes in the transition mode. LPM sets gain_change to high to not only load the value C_{DCOd1} into C_{DCOd2} but also make the output of multiplexer controlled by Code_ctrl equal to C_{DCOd1}; meanwhile, control signal PD_reset shown in Fig. 4-1 is also set to high to reset the phase detector. When the digital loop filter goes into the next stage, the smaller allowed gain for $K_{ip,FA}$ is applied and gain_change signal is set to 0 to load C_{DCOd2} as the initial locking value in this stage. By repeating this process several times, the output frequency will be locked near the target frequency with fast locking time and low frequency error.

After LPM and the digital loop filter repeat the observation and reload operation several times, the output frequency is settled near the target frequency, so, finally, the PT mode is entered. After the last reload in FA mode, at the beginning of PT mode, LPM reconnects the additional feedback and enables the

accumulator in the digital loop filter by set K_{pd}_zero_gain to 0 and Code_ctrl to 0, respectively.

4.4 Digital Controlled Oscillator (DCO)

In this section, the design and implementation of the digitally controlled oscillator (DCO) will be illustrated. The implemented block diagram of the DCO system is shown in Fig. 4-14. The DCO receives a 22-bits wide control word C_{DCO}[22:0] from the loop filter without the sign bit and delivers a differential signal with frequency around 40GHz to the buffers. The structure of the DCO will be introduced below.

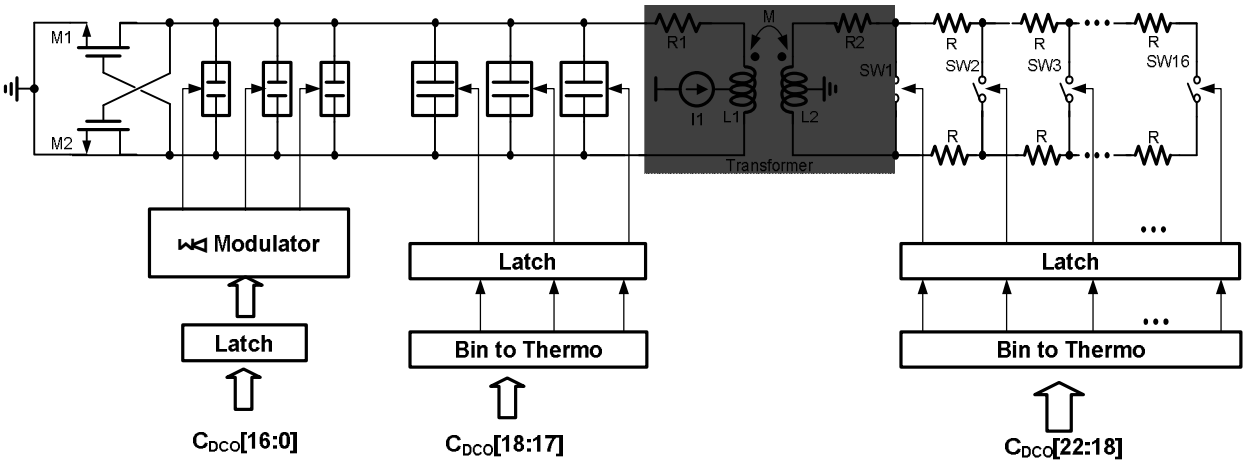


Fig. 4-14 Implemented block diagram of DCO system.

4.4.1 Structure of DCO

Due to its relatively good phase noise, ease of implementation, and better rejection of common-mode additive noise, the cross-coupled inductance capacitance (LC) oscillator is chosen and an equivalent conventional LC oscillator model is shown in Fig. 4-15. However, conventional LC tank VCO in mm-Wave band will suffer from some problems. Compare to the early design of

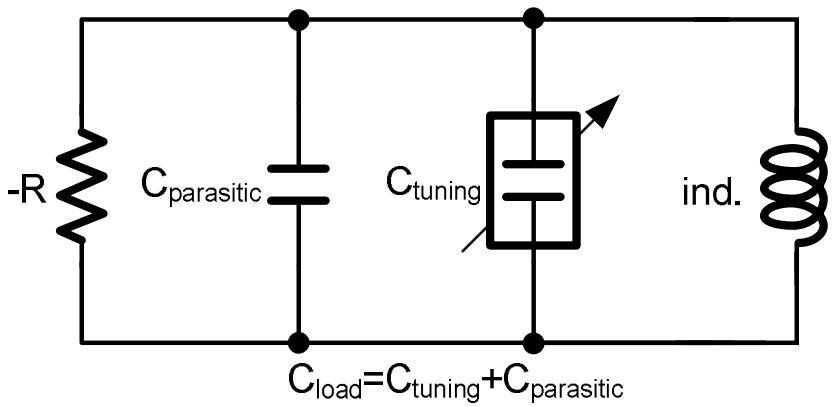


Fig. 4-15 Equivalent conventional LC oscillator model

the DCO, the dominate Q factor is from the inductors (Q_L), but the higher and higher operation frequency lowers the Q factor of varactor (Q_v) and complicates the design. Also, the high frequency tuning range is approximately proportional to reciprocal of the tuning capacitance, $1/C_{tuning}$, and the tuning bank must be divided into several parts to achieve the high tuning resolution. Nevertheless, if the high frequency tuning range and resolution must be met simultaneously, the parasitic capacitance $C_{parasitic}$ also increases and higher the total load capacitance C_{load}; consequently, the overall operation frequency is dropped down. Therefore, there are some compromises among the operation frequency, the tuning range, and the resolution.

In order to break the contradiction, a concept of DCO with single variable inductor is introduced and the equivalent model is illustrated in Fig. 4-16. In this model, through adjusting the inductor, the burden on the capacitor is released; furthermore, the minimum frequency tuning range becomes independent of resonant frequency and C_{load}, and the multi-band operation turns possible.

The equivalent model of the single variable inductor [15], VID, is shown in Fig. 4-17 and the equivalent inductance and resistance is described in equation 4-8 and 4-9, respectively, where R_v is XXX resistance, C_p is the parasitic

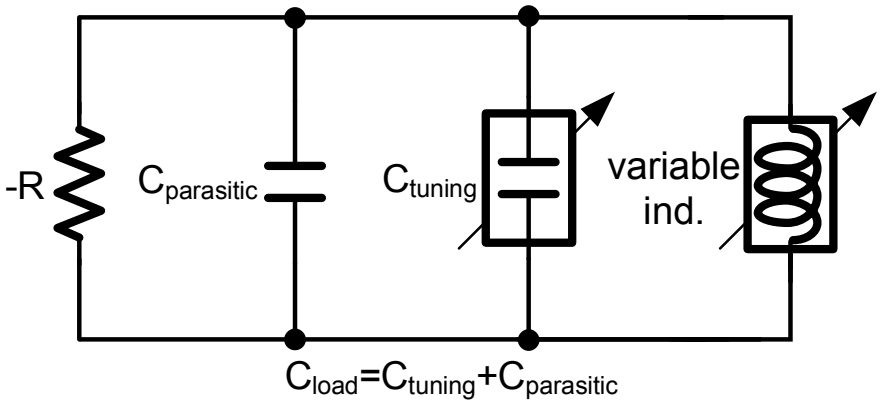


Fig. 4-16 Equivalent model of DCO with single variable inductor

capacitance, k is the coupling factor of the transformer, and L1, L2 are the inductance of primary and secondary coil, respectively.

$$L_{eq}\left(R_v,\omega\right)=\frac{R_v^2L_1\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]^2+\omega^2L_1L_2^2\left(1-k^2\right)^2}{R_v^2\left(1-\omega^2C_vL_2\right)\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]+\omega^2L_2^2\left(1-k^2\right)}. \tag{4-8}$$

$$R_{eq}\left(R_v,\omega\right)=\frac{R_v^2L_1\left[1-\omega^2C_vL_2\left(1-k^2\right)\right]^2+\omega^2L_1L_2^2\left(1-k^2\right)^2}{R_vk^2L_2}. \tag{4-9}$$

By observing these equations, if the self resonance frequency of secondary coil is greater than the operation frequency, i.e. $\omega^2L_2C_v<1$, the minimum and maximum value of the equivalent inductance are derived:

$$L_{\min}=L_{eq}\left(0,\omega\right)=L_1\left(1-k^2\right). \tag{4-10}$$

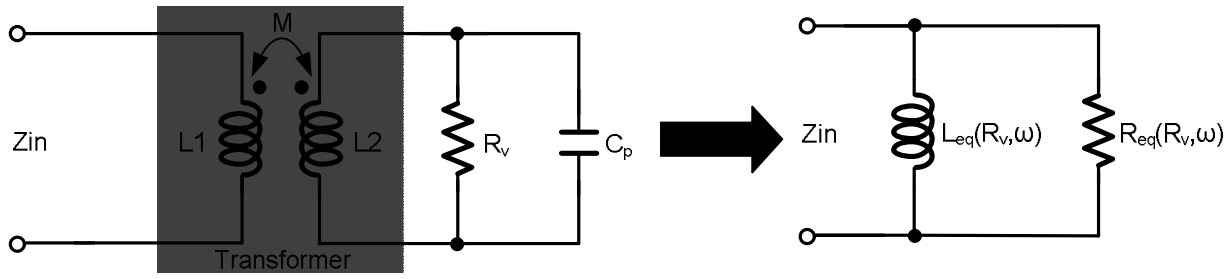


Fig. 4-17 Equivalent model of the single variable inductor [15]

$$L_{\max} = L_{eq}(\infty,\omega) = L_1\left(1+\frac{\omega^2/\omega_2^2}{1-\omega^2/\omega_2^2}k^2\right) > L_1 . \qquad (4\text{-}11)$$

Also, define the tuning percentage of the equivalent inductance, α, and the resonant frequency tuning percentage, β:

$$\alpha = \frac{L_{eq}(\infty,\omega)-L_{eq}(0,\omega)}{L_{eq}(\infty,\omega)} = \frac{k^2}{1-(1-k^2)\omega^2/\omega_2^2} > k^2 . \qquad (4\text{-}12)$$

$$\beta \equiv \frac{2(\omega_{\max}-\omega_{\min})}{\omega_{\max}+\omega_{\min}} > \frac{2\left(1-\sqrt{1-k^2}\right)}{1+\sqrt{1-k^2}} \approx \frac{k^2}{2} . \qquad (4\text{-}133)$$

and these two equations show that α and β are proportional to the coupling factor k only and are independent of resonant frequency and C_{load}.

Fig. 4-18 shows the final DCO architecture in the FPLL. VID in this structure consumes no power due to secondary coil of the transformer connects to ground. M1 and M2 construct the negative impedance just as that in the conventional LC oscillator. The inductor switches 1 to 16, controlled by 4-bit input, forms the coarse tuning bank, and only one switch is opened each time. Different opened switch influences the equivalent value of VID and determines the final operation frequency of DCO. Furthermore, 4-bit varactor bands are introduced in the primary coil of the transformer to provide finer frequency

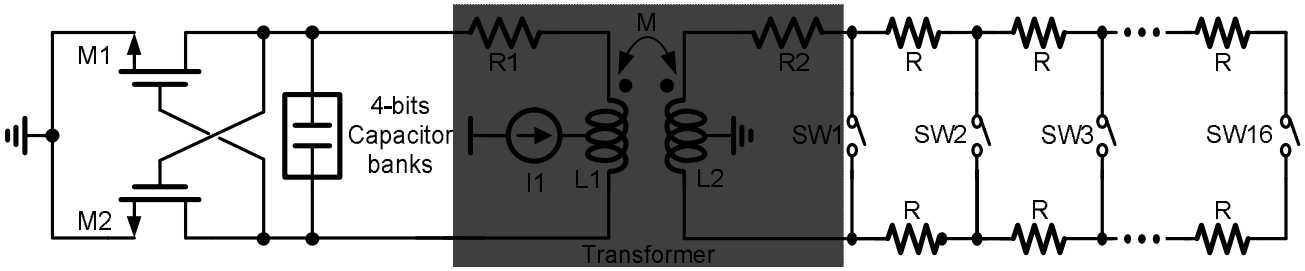


Fig. 4-18 Final DCO architecture

tuning by separating them into 2-bit fine tuning bank and 2-bit ΣΔ bank which are controlled by a 16-bit ΣΔ modulator.

4.4.2 Varactor Banks

Due to the finite DCO frequency resolution, the quantization error will introduce noise to the RF output signal. To gain insight into the quantization effects on the DCO phase noise, consider the quantization noise model, shown in Fig. 4-19 [13]. The quantization process can be modeled as an infinite-precision tuning signal added by an uniformly distributed random variable $\Delta f_{n,0}$ with white noise spectral characteristics. The quantization noise is then converted to phase noise through the $2\pi/s$ integration. The output phase noise due to the finite quantization error can be expressed as [13]:

$$L_{Quantize}(\Delta f) = \frac{1}{12} \times \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 \times \frac{1}{f_{REF}} \times \left(2 sinc \frac{\Delta f}{f_{REF}} \right)^2 \qquad (4\text{-}14)$$

In equation 4-14, Δf_{res} is the DCO quantization step which indicates the corresponding frequency deviation of one DCO control code and Δf means the frequency offset from the carrier. It can be seen that the output phase noise due to quantization process can be reduced by increasing the DCO frequency resolution. With careful design, the phase noise contributed from the quantization should be made below the natural DCO phase noise resulted from the finite quality factor of

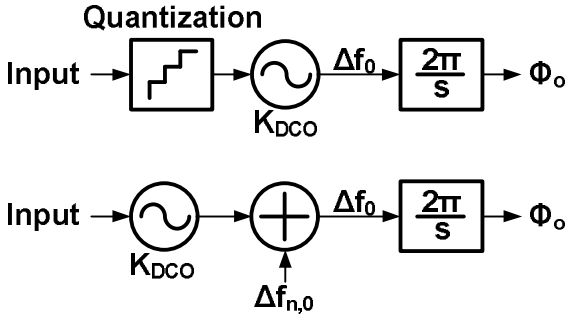


Fig. 4-19 DCO quantization noise model.

the LC tank and noise of active devices. As mentioned before, the phase noise of the LC tank oscillator can be expressed as [10]

$$S_{\varphi_{n,DCO}}(\Delta f) = \frac{\overline{i_n^2}/\Delta f}{q_{\max}^2} \frac{\Gamma_{rms}^2}{8\pi^2 \Delta f^2} \tag{4-15}$$

where $\overline{i_n^2}/\Delta f$ is the PSD of the equivalent parallel current noise, Γ_{rms} is the rms value of the impulse sensitivity function (ISF) associated with that noise source, q_{max} is the maximum signal charge swing which is defined as the product of the tank capacitance and maximum signal swing $C_{tank}V_{swing}$, and Δf is the the offset frequency from the carrier. Consider the DCO with different frequency step Δf_{res} and assume that the quality factor of the inductor is 7 and the phase noise spectrum due to frequency quantization is shown in Fig. 4-20. The spectrum shows that the quantization noise is below the DCO natural noise when Δf_{res} is less than 100kHz. This result suggests that the DCO frequency gain K_{DCO} should be below 100kHz/LSB. However, the finest frequency step achievable by switching a minimum size capacitance is about 50MHz which is much higher

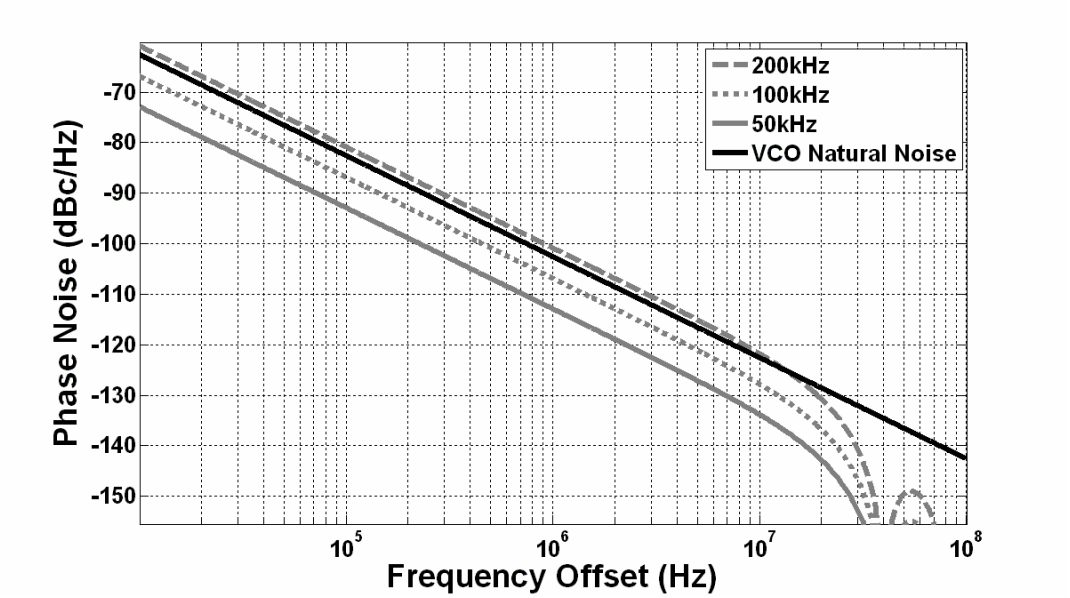


Fig. 4-20 Phase noise due to frequency quantization of different frequency resolution step.

than 100kHz. In order to get finer resolution, a high-speed ΣΔ dithering [13] method is used. Due to the wordlength limitation of the digital dithering circuit, there will still be a phase noise contribution due to the finite resolution per equation 4-14, with $\Delta f_{res}=\Delta f_{res,I}/2^{WF}$. Where $\Delta f_{res,I}$ is the frequency step without utilizing ΣΔ dithering and WF is the wordlength of the dithering circuit.

The structure of the ΣΔ modulator is illustrated in Fig. 4-21. It is implemented as digital second-order MASH-type architecture [13] which can be conveniently realized in digital domain by cell based design flow. Its output is fed to three ΣΔ capacitors. Table 4-1 reports the tuning characteristics of the DCO.

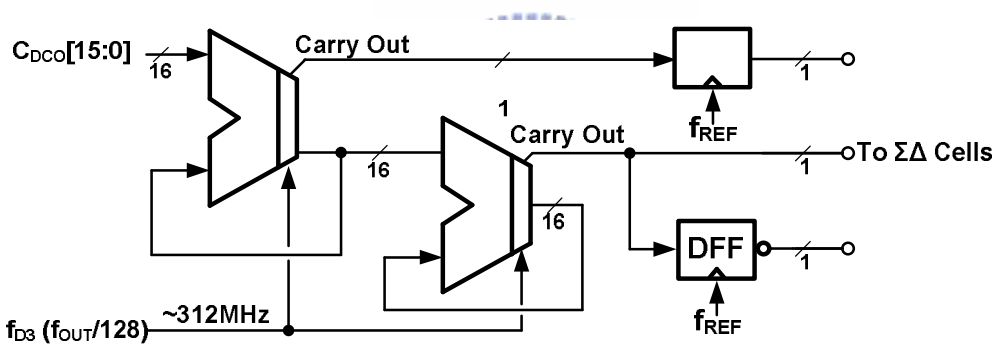


Fig. 4-21 Block diagram of the 2nd MASH-II order ΣΔ modulator.

Table 4-1 Tuning characteristics of the DCO.

Varactor Bank	Weighting	Frequency Step
Coarse Tuning Bank	5-bit Binary	400MHz
Fine Tuning Bank	3-bit Unity	150MHz
ΣΔ Bank	3-bit Unity	50MHz

4.4.3 Simulation results of DCO

The time domain and frequency domain simulations are performed by Hspice and ANSOFT.Fig. 4-22 and Fig. 4-23 shows the frequency tuning range and the phase noise simulation result of the DCO, respectively. The frequency tuning range covers from 37.5 to 45.5GHz and the phase noise reports -110dBc/Hz at 10MHz offset from a 40GHz carrier. The power consumption is about 23mW in TT corner while delivering 700mV$_{pp}$ single-ended output swing.

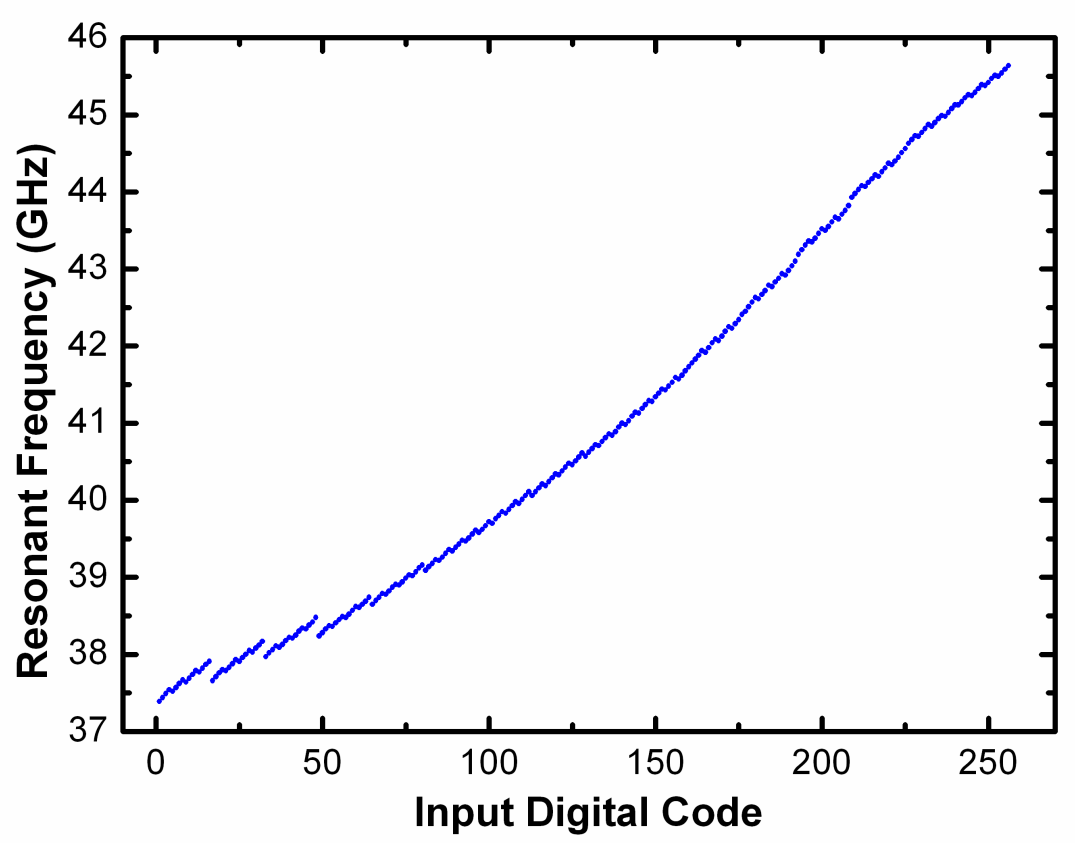


Fig. 4-22 Simulated frequency tuning range of the DCO.

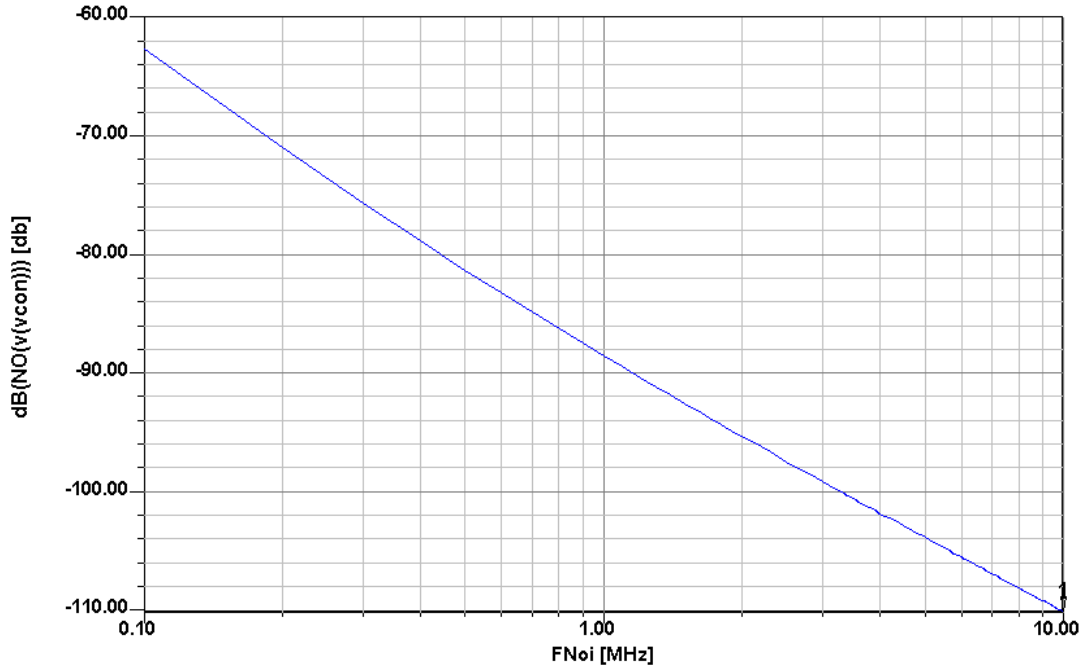


Fig. 4-23 Simulated phase noise performance of the DCO.

4.5 Divide-by-16 Prescaler

Since our goal is focusing on wide-band design, frequency divider with wide locking range is needed. Although conventional injection locked divider could operate at a high speed, it does not provide us with a sufficient locking range, so static current mode divider is necessary. But according to the available information, static frequency divider normally works around a few tens of giga hertz. Even with inductive peaking such as shunt peaking, the operating frequency could hardly exceed 40GHz. Thus a modified version of static frequency divider is readily needed. Fig. 4-25 [16] shows the so-called spilt load frequency divider utilized in this PLL as the first stage of the divider chain. This architecture operates at a higher speed than conventional static frequency divider with inductive peaking since the gate and drain are no longer simultaneously

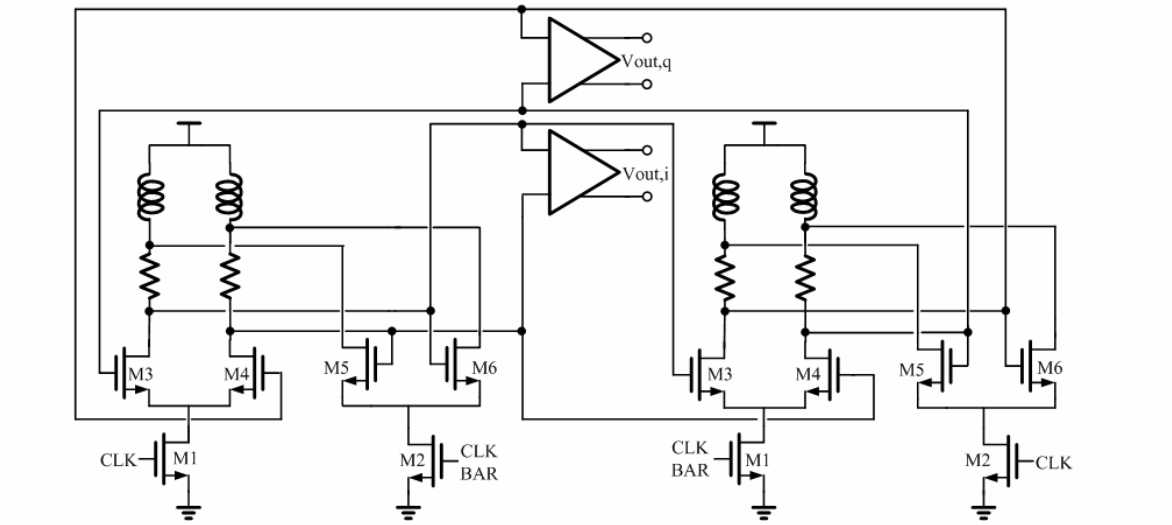


Fig. 4-25 Schematic of the first stage of the divider chain[16]

loading each of the pre-amplifier stage.

For second stage divider, we use conversional static frequency divider as shown in Fig. 4-24 and the following two stages divide-by-4 prescaler is implemented as two cascade divide-by-2 frequency dividers. Each stage employs two D-latches in a master-slave configuration with negative feedback, as shown in Fig. 4-26 [12]. The top PMOS devices act as variable resistance loads,

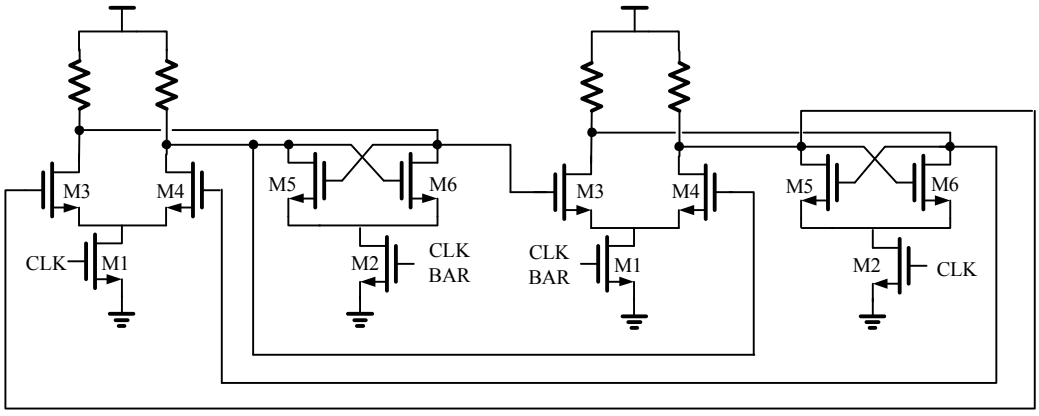


Fig. 4-24 Schematic of the second stage of the divider chain.

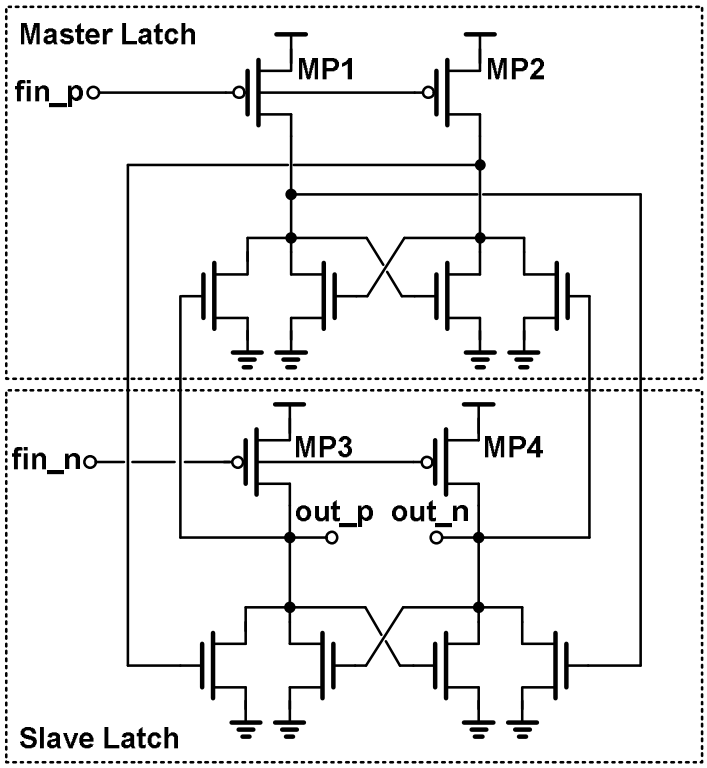


Fig. 4-26 Schematic of the 3rd and 4th divide-by-2 frequency divider. [12].

controlled by fin_p and fin_n. Input and cross-coupled differential pairs are placed in parallel to accomplish sensing and regeneration action. It can be noted that there has no stacked devices and pass gates, which makes it to be suitable in low voltage operation.

The last divider stage is followed by a differential to single ended converter and inverter-based buffers. The simulation results of the divider chain are shown in Fig. 4-27 and the power consumption simulation results are 26.11mW, 27.35mW, and 28.16mW in SS, TT, and FF corner, respectively.

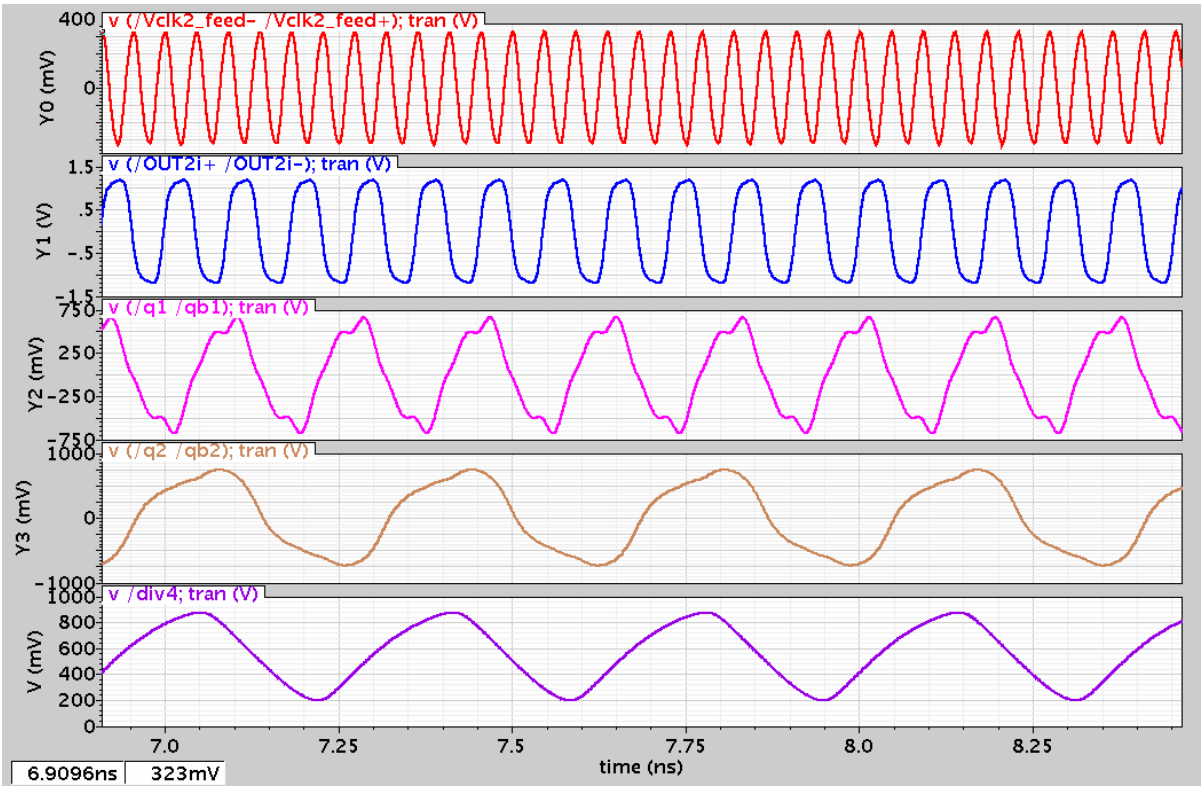


Fig. 4-27 Output simulated wave of each stage divide.

Chapter 5 Experimental Results

5.1 IC Chip

Fig. 5-1 shows the die photograph of the ADPLL. The total silicon dimensions are about 1.265mm^2 (1150μm × 1100μm) including the bonding pads and digital I/O cells. The active area is about 0.594mm^2. Due to the automatic metal filling procedure which is now standard in the advanced CMOS process, there is not much to be seen from the chip photograph. Only some sensitive analog circuits such as inductor coil, MIM capacitors and the varactor bank have been excluded from the filling pattern to diminish the parasitic effects.

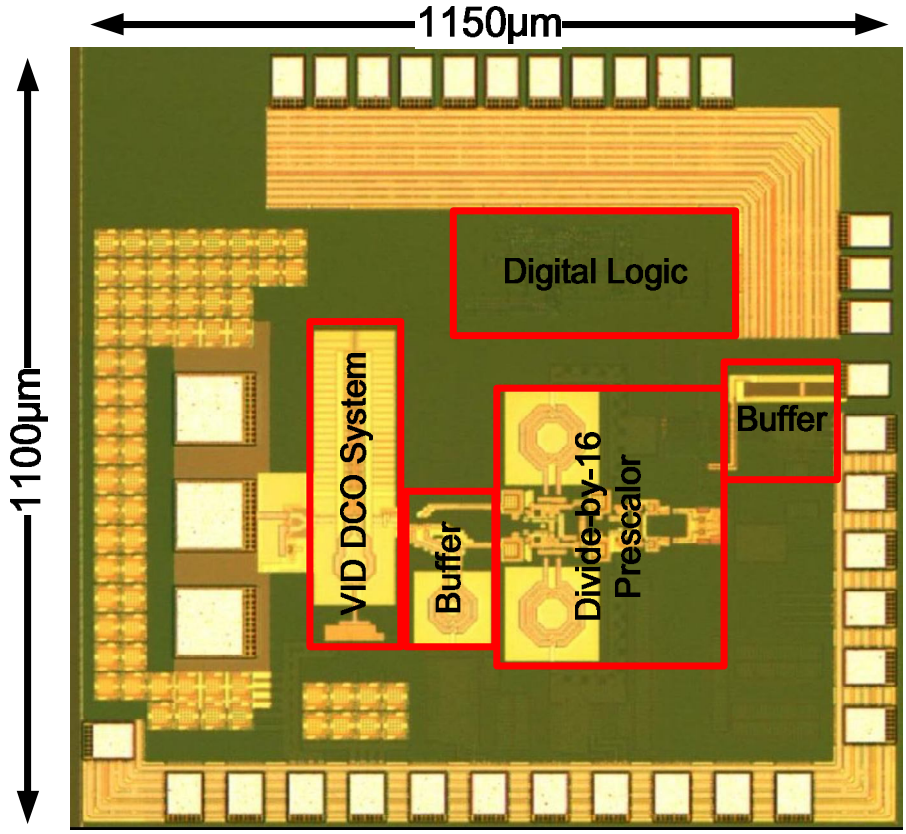
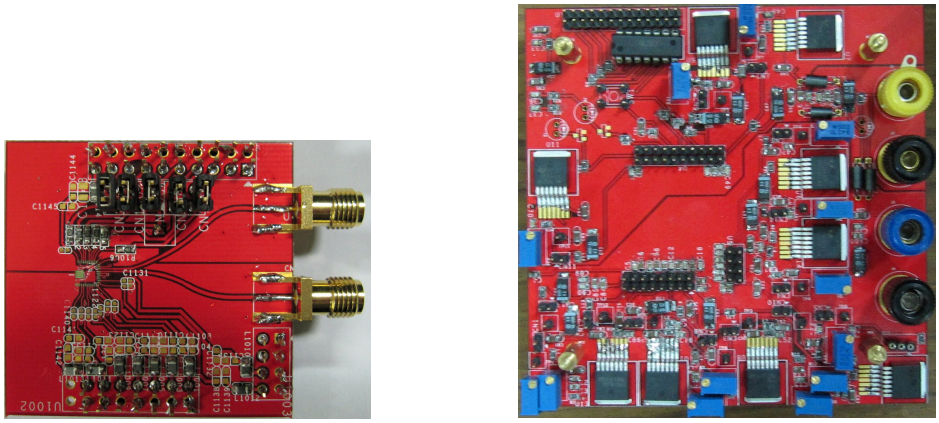


Fig. 5-1 Chip photograph of the implemented FADPLL.

5.2 Evaluation Board

To evaluate the performance of the implemented ADPLL, two printed circuit boards (PCBs) constructed of four layers have been built as shown in Fig. 5-2. Although placing the chip in package enables protection from stress and contamination while eases the connection between chip and printed circuit board (PCB), the package may degrade the chip performance especially in radio frequency applications. Thus, the chip is directly attached to the AC PCB (Fig. 5-2 (a)) and the I/O pads are connected to the signal traces on AC PCB through the bonding wires. The AC PCB is then mounted to the DC PCB (Fig. 5-2 (b)) which provides DC supplies and biases current for the test chip. As the result of the partition, it is facile to replace the test chip by simply substituting the AC PCB without re-soldering the regulator ICs and other passive components.

As shown in Fig. 5-2 (a), the die is located at the center-left of the AC PCB. The 40 GHz RF output is measured on probe, while 40 MHz reference clock and the 1.25 GHz divide-by-32 clock are connected using subminiature version A (SMA) connectors, which provide DC to 18 GHz broadband performance with



(a) (b)

Fig. 5-2 (a)AC PCB and (b)DC PCB for evaluating the chip

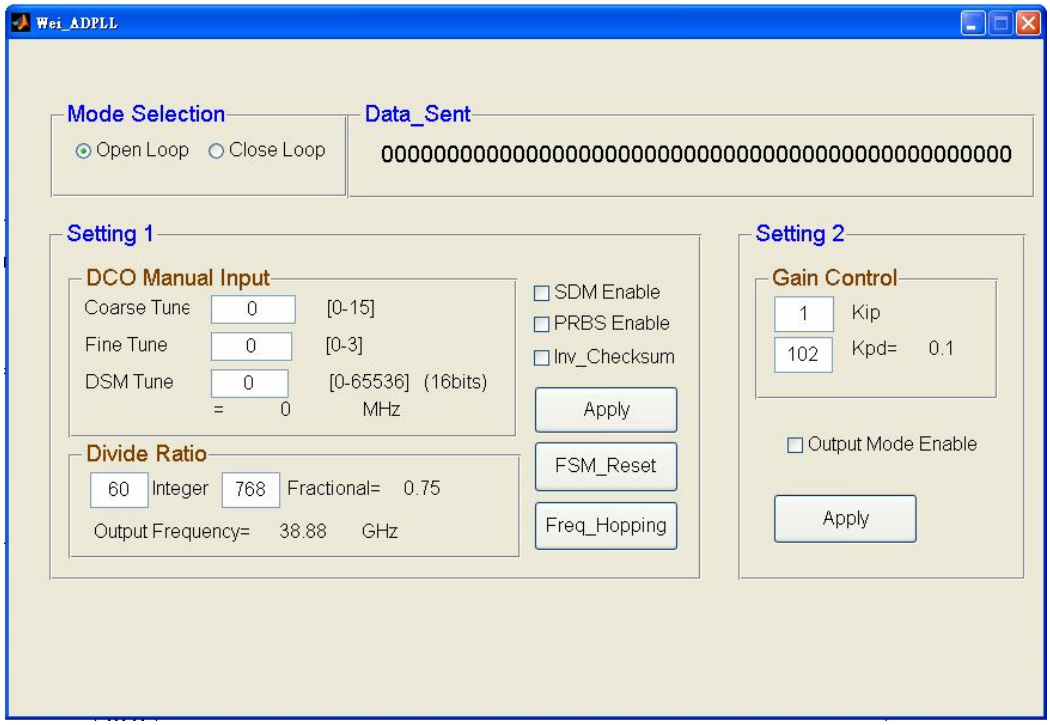


Fig. 5-3 GUI program for controlling the chip

low reflections and constant 50-Ω impedance. The connector on the up side attaches the DC PCB to the computer, whose purpose is to control the chip by reading and writing its registers by means of a graphic user interface (GUI) program (Fig. 5-3) through the parallel port of the PC. The operation mode, the serial output mode, the initial DCO control code and the loop filter parameters of the synthesizer can be remotely controlled by the GUI program.

Three light-emitting diodes (LEDs) are used to indicate the power state, the output pin of the chip serial interface and the result of parity check which provides simple error detection of the input serial data. A push bottom is used as the reset bottom and its output is filtered by a low pass filter to solve key bouncing problem.

5.3 Measurement Setup

Fig. 5-4 shows the measurement environment setup and the equipments. The RF output is measured on probe by the RF1 microwave probing station and then sent to an Agilent E4448A spectrum analyzer, and the reference input clock and the divide-by-32 clock are connected by SMA connectors with 50-Ω characteristic impedance. The 40 MHz reference clock is provided by an Agilent 8257D signal generator which has a phase noise of about -134 dBc/Hz at a 20 KHz offset. The 40 GHz RF output is measured by probing station and then connected to the bias tees to block the DC bias and then fed to the spectrum analyzer or the oscilloscope. The phase noise and spectrum of the closed loop PLL is measured using the Agilent E4448A with the option 226 phase noise measurement utility. The Tektronix DPO71254 real time oscilloscope with 12.5 GHz input bandwidth and up to 50 G sampling rate provides precise timing waveform and jitter measurement.

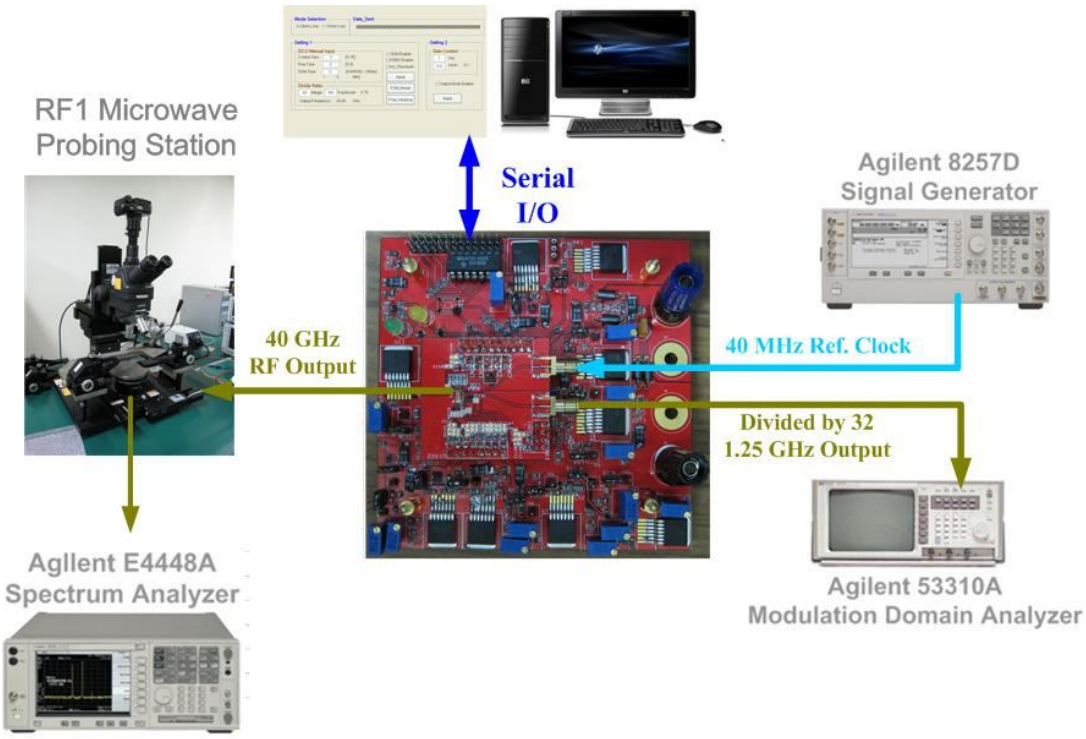


Fig. 5-4 Measurement setup of the test chip.

The frequency hopping time and modulation domain behavior are provided using Agilent 53310A modulation domain analyzer (MDA). Due to the input bandwidth limitation of the MDA, instead of the 40 GHz RF output, the 1.25 GHz divide-by-32 signal is used for measurement. The chip serial interface is connected to the PC parallel port for remote control through an interface on the DC board, which converts TTL signals of the parallel port to open collector signals while provides noise isolation between PC and the test chip.

Chapter 6 Conclusions

This work demonstrates a 40GHz all digital fractional frequency synthesizer for 60 GHz UWB system. Fractional frequency locking ability is achieved by an additional negative feedback with a ΣΔ modulator around the reference phase accumulator while without using multi-mode dividers. With the dual mode phase detector, the loop rapidly locks to the target frequency and then reconstructs to a bang-bang PLL without resorting to the time to digital converter.

A DCO with single variable inductor with varactor bank incorporating 4-bit unity-weighted coarse tuning and 2-bit unity-weighted fine tuning to ensure linearity is presented. The frequency resolution is further enhanced by employing high speed dithering through an 8-bit MASH-11 ΔΣ modulator.

Governed by the programmable gains in the digital loop filter and in the additional negative feedback around the reference phase accumulator, the loop bandwidth is self-adjusted during the frequency acquisition and is fixed in phase tracking process. The simulated phase noise is -90dBc/Hz at 1MHz frequency offset.

Using the UMC 90nm CMOS technology, the implemented prototype occupies only 0.594mm^2 active area and the simulated power consumption is about 52mW.

Finally, because of the digital nature, the ADPLL can be further scaled down for future CMOS process and suitable in SOC designs.

Reference

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Boston, MA: McGraw-Hill, 2001.

[2]I. Galton, "Delta-sigma data conversion in wireless transceivers," *IEEE Trans. Theory Tech.,* vol. 50, no. 1, pp. 302-315, Jan.2002.

[3] R. B. Staszewski, Chih-Ming Hung, D. Leipold and P. T. Balsara, "A first multigigahertz digitally controlled oscillator for wireless applications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 51, pp. 2154-2164, Nov. 2003.

[4] R. B. Staszewski, Chih-Ming Hung, K. Maggio, J. Wallberg, D. Leipold and P. T. Balsara, "All-digital phase-domain TX frequency synthesizer for bluetooth radios in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, vol.1, pp. 272, Feb. 2004.

[5] M. Ferriss and M. P. Flynn, "A 14mW Fractional-N PLL Modulator with a Digital Phase Detector and Frequency Switching Scheme," *IEEE Journal of Solid-State Circuits,* vol. 43, NO. 11, pp. 2464-2471, Nov. 2008.

[6] N. Da Dalt, "A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 52, pp. 21-31, Jan. 2005.

[7] N. D. Dalt, "Markov Chains-Based Derivation of the Phase Detector Gain in Bang-Bang PLLs," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 53, pp. 1195-1199, Nov. 2006.

[8] "Agilent E4448A PSA 系列高性能頻譜分析儀應用手冊," 2008.

[9] N. D. Dalt, "Theory and Implementation of Digital Bang-Bang Frequency Synthesizers for High Speed Serial Data Communications," University of Padova, Ph.D, Feb. 2007.

[10] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid-State Circuits,* vol. 34, pp. 717-724, May. 1999.

[11] R. B. Staszewski and P. T. Balsara, "Phase-Domain All-Digital Phase-Locked Loop," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 52, pp. 159-163, March 2005.

[12] B. Razavi, "A 13.4-GHz CMOS Frequency Divider," *ISSCC*, pp. 176-177, 1994.

[13] R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS,* Wiley-Interscience, 2006.

[14] Song-Yu Yang, Wei-Zen Chen., "A 7.1mW, 10GHz All Digital Frequency Synthesizer with Dynamically Reconfigured Digital Loop Filter in 90nm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 90-91, Feb. 2009.

[15] Chi-Yao Yu, Wei-Zen Chen, Chung-Yu Wu, and Tai-You Lu, "A 60-GHz, 14% Tuning Range, Multi-Band VCO with a Single Variable Inductor," IEEE Asian Solid-State Circuits Conference, Nov. 2008.

[16] Lan-Chou Cho, Chihun Lee, and Shen-Iuan Liu, " A 1.2-V 37–38.5-GHz Eight-Phase Clock Generator in 0.13-_m CMOS Technology," *IEEE Journal of Solid-State Circuits,* vol. 42, NO. 6, pp.1261-1270 Jun. 2007

Vita

基本資料				
中文姓名	李彥緯	英文姓名	Yen-Wei Lee	
聯絡電話	0955734751	電子信箱	leewei.ee96g@nctu.edu.tw	
通訊地址	新竹市柴橋路 59 巷 33 號			
戶籍地址	新竹市柴橋路 59 巷 33 號			
教育背景				
學歷	學校	系所	組別	時間
碩士	國立交通大學	電子所	系統組	96.9~98.9 畢
大學	國立交通大學	電子物理學系		92.9~96.6 畢
高中	新竹市國立新竹高中			89.9~92.6 畢
專長				
修習科目	數位通訊 類比積體電路 計算機結構 半導體物理與元件(一) 鎖相迴路設計與應用 射頻積體電路 積體電路之靜電防護設計特論			
專業能力	類比電路設計 鎖相迴路設計	Full-Custom Design Flow Cell-Based Design Flow		
熟悉軟體	MATLAB/Simulink Virtuoso Calibre Verilog Design Vision	SOC Encounter AnSoft Office: Word, Excel, Power Point		
特殊表現	交通大學赴美國伊利諾大學(UIUC)交換學生一學期 大四書券獎一學期			