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碩 士 論 文

非對稱輕摻雜汲極金屬氧化半導體電晶體應用於2.4GHz之功率放大器

A 2.4GHz CMOS Power Amplifier with Asymmetric-LDD MOS Transistors

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摘 要

本論文展示一種以非對稱輕摻雜汲極金氧半導體電晶體來製作之 2.4GHz 功率放大器，它可以用 TSMC 0.18μm 的 CMOS 一般製程環境來實現。此非對稱輕摻雜汲極金氧半導體電晶體擁有的汲極源極崩潰電壓大約為一般電晶體的 2 倍，所以這個設計約可穩定的操作在 2.5V~3V，而較高的操作電壓使得電路有優越的功率。根據模擬的結果，功率增益可以達到 26.5dB，輸出功率 P1dB 可以達到 24.9dBm，功率增加效率(PAE)在 P1dB 點可以達到 20%，與超過 40dBm 的輸出三階互調截點(OIP3)。

未來的製程不斷縮小，降低工作電壓對於功率放大器是很大的設計瓶頸，此種功率單元的設計方式，將會是製程整合的良好解決方案。

A 2.4GHz CMOS Power Amplifier with Asymmetric-LDD MOS Transistors

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Abstract

This paper presents a 2.4 GHz CMOS power amplifier with asymmetry-LDD transistor and implements in TSMC 0.18 μm CMOS technology. The asymmetry-LDD transistor has about twice drain breakdown voltage to the conventional transistor, hence the voltage source in the design can supply about 2.5V to 3V. And the power amplifier can achieved higher output power. According to simulation result, the power gain is 26.5dB, output P1dB is 24.9dBm, the PAE at P1dB is 20%, and OIP3 is over 40dBm.

In the future, the low voltage is a bottleneck to power amplifier. So this power cell design might be a solution to integrate RFIC power amplifier into system on chip (SOC) with lower cost.

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Chapter 1

Introduction

1.1 RF Transceivers

Over the last few decades, many advances have been made in area of wireless communication technology. Those applications become a part of our live. Such as mobile phone, wireless mouse, keyboard, wireless local area network (W-LAN), notebook, RFID, global positioning system (GPS) etc. In general, communication system can be shown like Fig. 1.1.

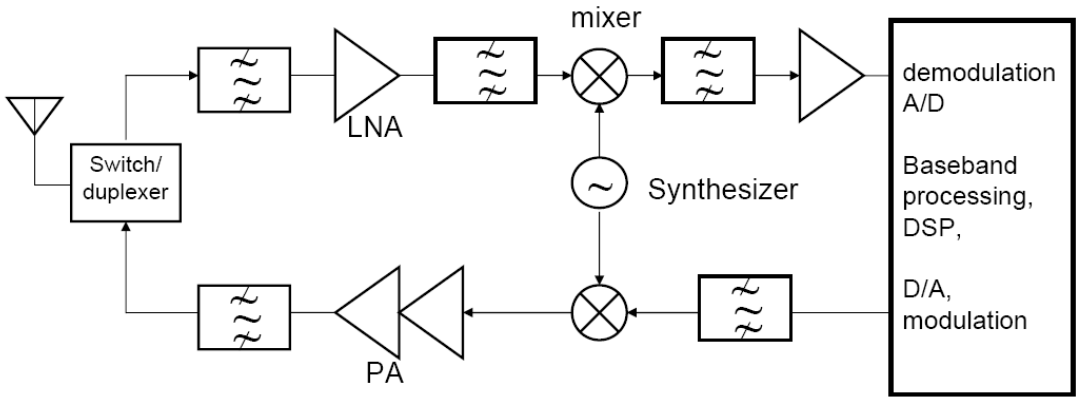


Fig. 1.1 Transceiver block diagram

Fig. 1.1 is a transceiver block diagram, a transceiver means a unit which contains both a receiver and a transmitter. Transmitter transmit the signal after digital signal modulation, receiver receive these signal and demodulate the signal to digital

baseband section. The transceiver is included power amplifier (PA), low noise amplifier (LNA), mixer, voltage controlled oscillator (VCO), phase locked loop (PLL). Power amplifier is the most important device of transmitter, so this research is focus on the design of PA.

PA has to transmit the signal to the air, so it requires large output power with linearity and efficiency. But it is very difficult for it to increase linearly and efficiency at the same time, that is the reason why discrete or hybrid implementations of this circuit are so popular.

Pseudomorphic High Electronic Mobility Transistor (pHEMT) FET, Hetero-junction bipolar transistor (HBT), bipolar junction transistor (BJT), CMOS, Bi CMOS, LDMOS are common implementation of RF integrated circuit.

Each implementation technology has their advantage and drawback, so it is the reason why individual implementation component built systems are favored for so many years. CMOS for base band section, bipolar for IF partition, ceramic for SAW filters, III-V such as GaAs for RF transmitter especially for power amplifier.

1.2 Motivation

In RF circuit design, PA is the most power-required building blocks. Large supply voltage is necessary condition for practical application. CMOS PA design will face the

great impact and hard to survive in advance technology implementation with low supply voltage.

The RF power performance of Si MOSFET has little improvement with down-scaling, which is limited by the inherent low breakdown voltage. This is especially important for RF PA, where the voltage swing is about twice of DC bias voltage. This restriction decreases maximum output power, power density and power-added-efficiency (PAE) to a high degree.

To address this problem, we have previously reported an asymmetric-lightly-doped-drain (LDD) MOS transistor for high frequency RF power application. This new asymmetric-LDD MOS transistor is fully embedded in the conventional foundry logic process with only one additional mask but without extra process step. The source-drain breakdown voltage can be improved as twice as conventional transistor with still high unity current gain cut-off frequency.

In this work we further implemented the asymmetric-LDD MOS transistor for a power amplifier. The output power improves monotonically with increasing operation voltage. This power cell has high breakdown voltage and fully embedded to standard CMOS technology, so I make one step further to realize the power amplifier and prove it works with good performance.

Chapter 2

Concept of Power Amplifier

2.1 Smith Chart

Smith Chart [Fig. 2.1] is a very useful tool for some problems in radio frequency. The Smith Chart can be used to represent some parameters including reflection coefficient, impedance, admittance, S-parameter. It also can plot some circles for constant gain contours or noise figure.

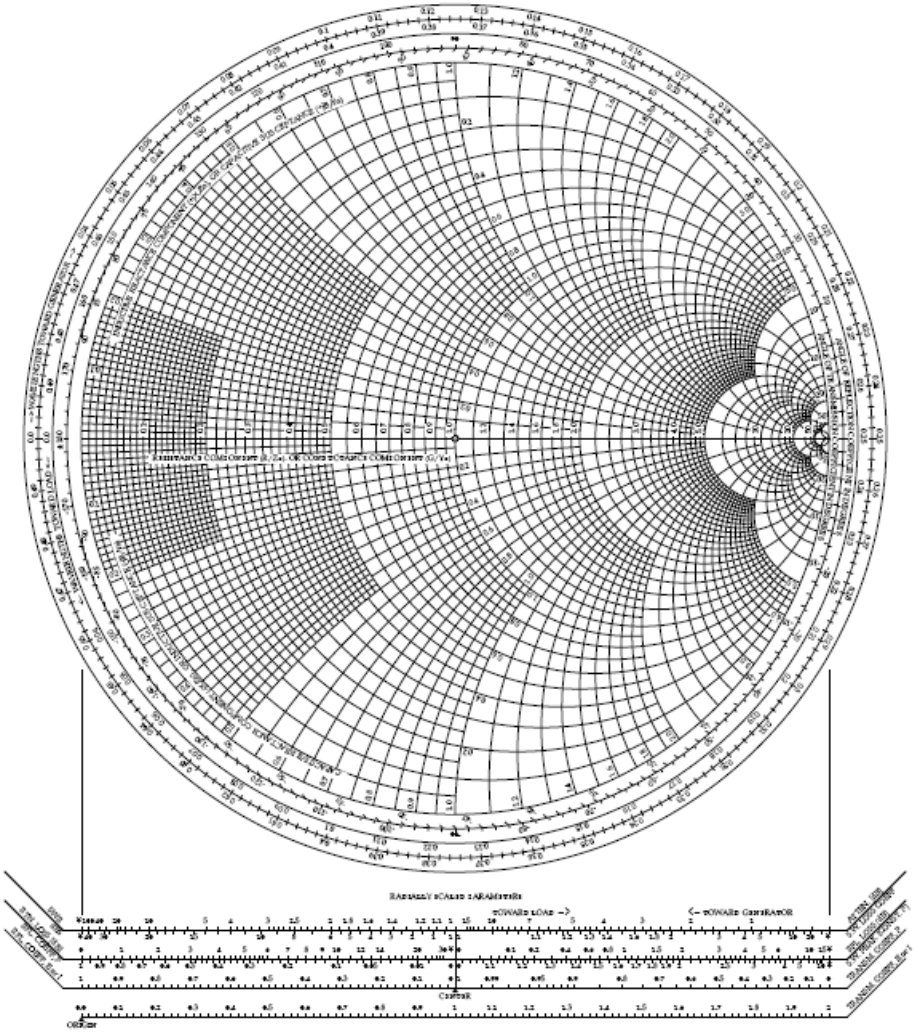


Fig. 2.1 Smith Chart

The Smith Chart is the voltage reflection coefficient in polar form. The reflection coefficient Γ for transmission line can represent as below

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{z_L - 1}{z_L + 1} \tag{2-1}$$

where Z_L is the load, Z_0 is the characteristic impedance, and z_L is the normalized impedance ($z_L = \left(Z_L / Z_0 \right)$). Equation (2-1) also can write as

$$z_L = \frac{1+\Gamma}{1-\Gamma} \tag{2-2}$$

If we decompose equation (2-1) and (2-2) to real part and imaginary part as

$$\Gamma = \Gamma_r + j\Gamma_i \tag{2-3}$$

$$z_L = r_L + jx_L \tag{2-4}$$

and equation (2-2) can rewrite as

$$r_L + jx_L = \frac{(1+\Gamma_r) + j\Gamma_i}{(1-\Gamma_r) - j\Gamma_i} \tag{2-5}$$

Rearrange the above equation, we can obtain

$$\left(\Gamma_r - \frac{r_L}{1+r_L} \right)^2 + \Gamma_i^2 = \left(\frac{1}{1+r_L} \right)^2 \tag{2-6}$$

$$(\Gamma_r - 1)^2 + \left(\Gamma_i - \frac{1}{x_L} \right)^2 = \left(\frac{1}{x_L} \right)^2 \tag{2-7}$$

We use the center of a circle and the radius from equation (2-6). Then we can draw the constant-resistance circles, shown in Fig. 2.2. And we also can draw the constant-reactance circles from equation (2-7), shown in Fig. 2.3.

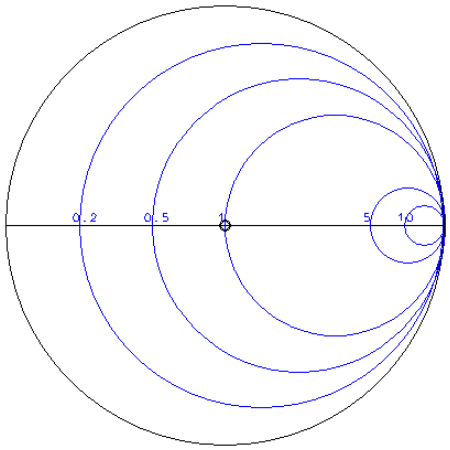


Fig. 2.2 constant-resistance circles

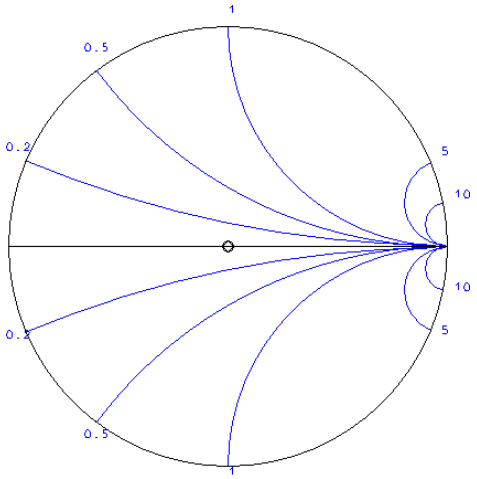


Fig. 2.3 constant-reactance circles

If combine Fig. 2.2 and Fig. 2.3, we can get the Smith Chart.

2.2 Parameter definitions

2.2.1 S-parameter

For low frequency, we can use Z-parameters or Y-parameters to represent circuits. But for high frequency, we require S-parameters due to difficulty of open-circuit and short-circuit conditions in measurement. S-parameters are defined by incident waves and reflected waves. For a two-port network, shown in Fig. 2.4, we define the incident wave and the reflected wave for port 1 are a_1 and b_1. And we define the incident wave and the reflected wave for port 2 are a_2 and b_2.

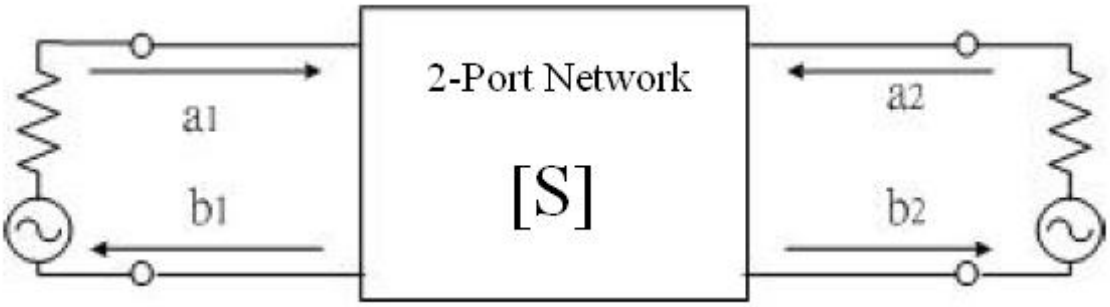


Fig. 2.4 Two-port network

Then we can express the matrix as below.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

The equation can be written as

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2-8}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2-9}$$

From equation (2-8) and (2-9), we obtain

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{2-10}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{2-11}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{2-12}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2-13}$$

The meanings of S-parameters are

S_{11}：The reflection coefficient of port 1, when port 2 is matching.

S_{21}：The transmission coefficient from port 1 to port 2, when port 2 is matching.

S_{12}：The transmission coefficient from port 2 to port 1, when port 1 is matching.

S_{22}：The reflection coefficient of port 2, when port 1 is matching.

2.2.2 Stability

When designing amplifiers, stability is always a concern. Amplifiers can be unstable with certain load and source impedances. We can define some parameters for two-port network [Fig. 2.5].

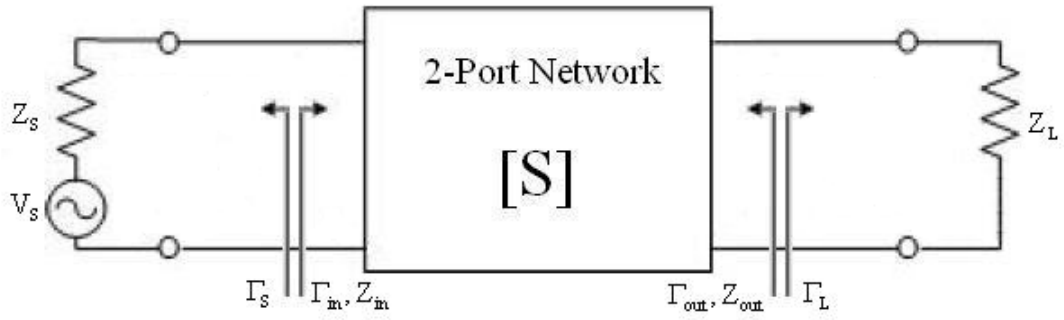


Fig. 2.5 Two-port network stability parameters

For a two-port network, it is potentially unstable when any port has a negative resistance. It represents $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$.

The unconditionally stable is

$$\left|\Gamma_S\right| < 1 \tag{2-14}$$

$$\left|\Gamma_L\right| < 1 \tag{2-15}$$

$$\left|\Gamma_{in}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1 \tag{2-16}$$

$$\left|\Gamma_{out}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\right| < 1 \tag{2-17}$$

From equation (2-14) ~ (2-17), we can get another form

$$K = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|} > 1 \tag{2-18}$$

$$\left|\Delta\right| = \left|S_{11}S_{22} - S_{12}S_{21}\right| < 1 \tag{2-19}$$

where K is stability factor. In general, we use equation (2-18) and (2-19) to determine that the circuit is stable or not.

In addition, we can use stability circle to determine the stable region. The stability circle can draw on Smith Chart directly. The output plane is called Γ_L-plane, and the input plane is called Γ_S-plane. For Γ_L-plane, first, we find the $|\Gamma_{in}|=1$ circle on Smith Chart. Second, note the region for $|\Gamma_{in}|>1$ and $|\Gamma_{in}|<1$. Finally, we can get the stable region ($|\Gamma_{in}|<1$) on Smith Chart, shown in Fig. 2.6.

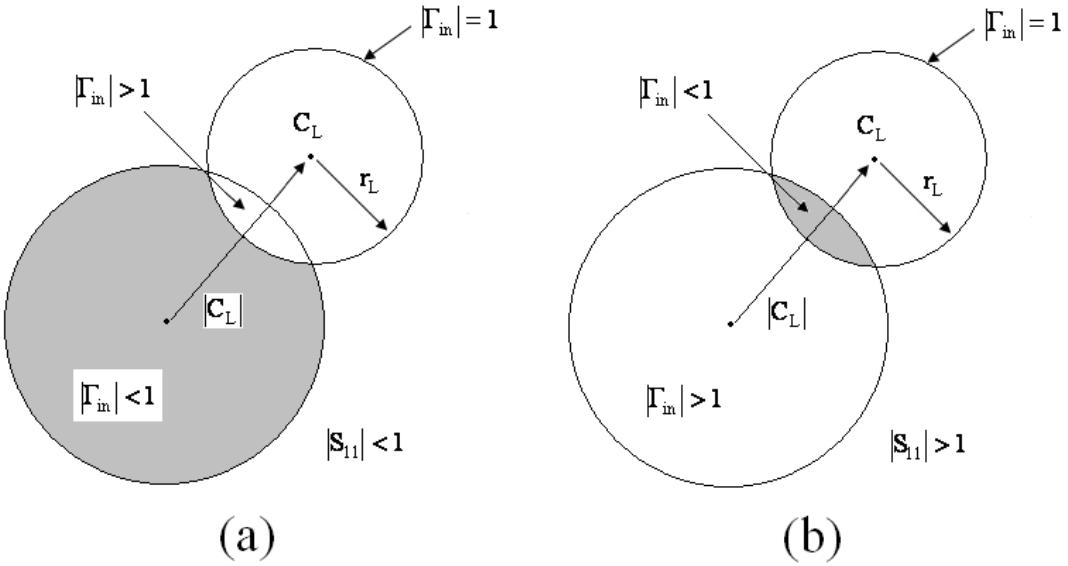


Fig. 2.6 The stable region for Γ_L-plane (a) $|S_{11}|<1$ (b) $|S_{11}|>1$

The Γ_S-plane is the same method for $|\Gamma_{out}|=1$, shown in Fig. 2.7.

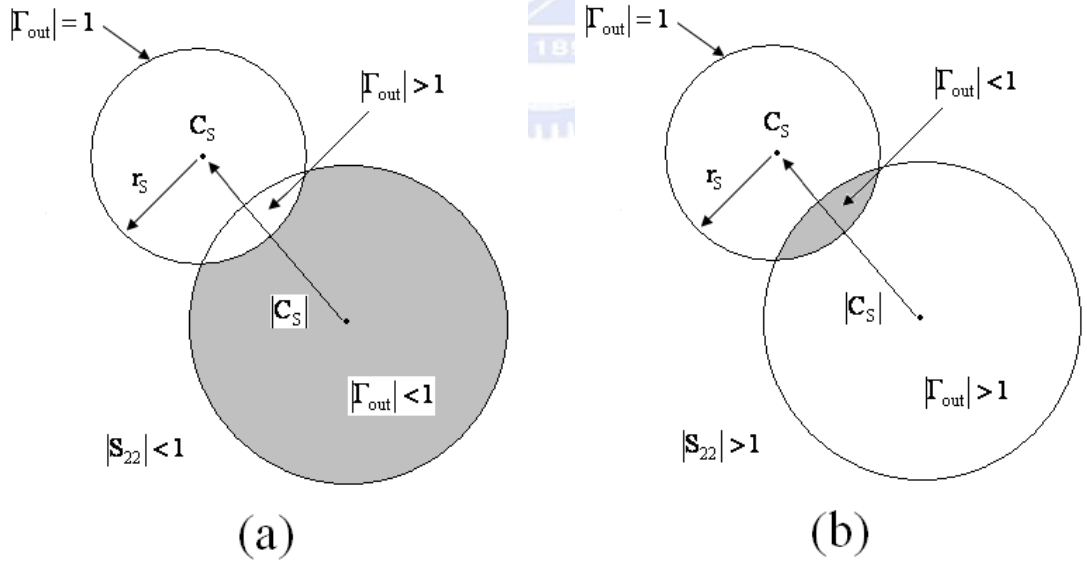


Fig. 2.7 The stable region for Γ_S-plane (a) $|S_{22}|<1$ (b) $|S_{22}|>1$

For output stability circle (Γ_L-plane), the radius and the center of circle is

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{2-20}$$

$$C_L = \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{|S_{22}|^2 - |\Delta|^2} \tag{2-21}$$

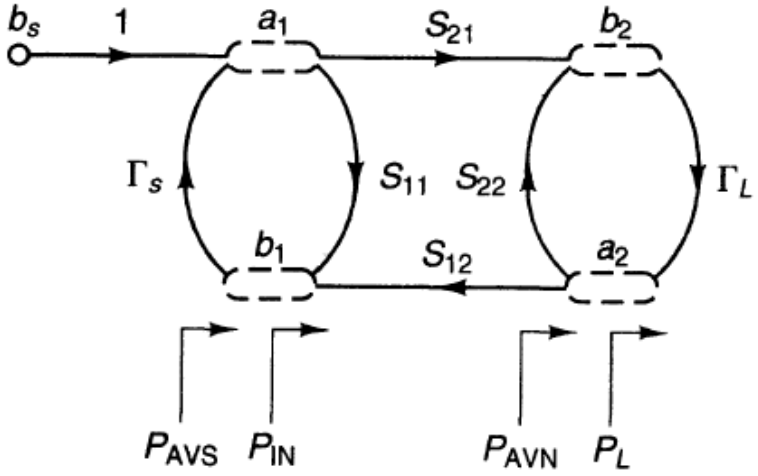
For input stability circle (Γ_S-plane), the radius and the center of circle is

$$r_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{2-22}$$

$$C_S = \frac{\left(S_{11} - \Delta S_{22}^*\right)^*}{|S_{11}|^2 - |\Delta|^2} \tag{2-23}$$

2.2.3 Power gain

Several power gain equations are used in the design of amplifiers. There are signal flow graph and different powers used in gain equations, shown in Fig. 2.8. The transducer power gain G_T, the operating power gain G_P, and the available power gain G_A are defined as follow.



$$P_{IN} = \frac{1}{2}|a_1|^2 - \frac{1}{2}|b_1|^2$$

$$P_L = \frac{1}{2}|b_2|^2 - \frac{1}{2}|a_2|^2$$

$$P_{AVS} = P_{IN}\big|_{\Gamma_{IN}=\Gamma_S^*}$$

$$P_{AVN} = P_L\big|_{\Gamma_L=\Gamma_{OUT}^*}$$

Fig. 2.8 Different power definitions

The definition of transducer power gain G_T is

$$G_T = \frac{P_L}{P_{AVS}} = \frac{\text{power delivered to the load}}{\text{power available from the source}}$$

$$= \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|^2} \qquad (2\text{-}24)$$

The definition of operating power gain G_P is

$$G_P = \frac{P_L}{P_{IN}} = \frac{\text{power delivered to the load}}{\text{power iput to the network}}$$

$$= \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad (2\text{-}25)$$

The definition of available power gain G_A is

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{\text{power available from the network}}{\text{power available from the source}}$$

$$= \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{OUT}|^2} \qquad (2\text{-}26)$$

As stability circle, we can draw the constant gain circle on Smith Chart. The

constant available power gain circle is defined by source reflection coefficient, and the constant operating power gain circle is defined by load reflection coefficient.

There is an example for constant available power gain circles, shown in Fig. 2.9.

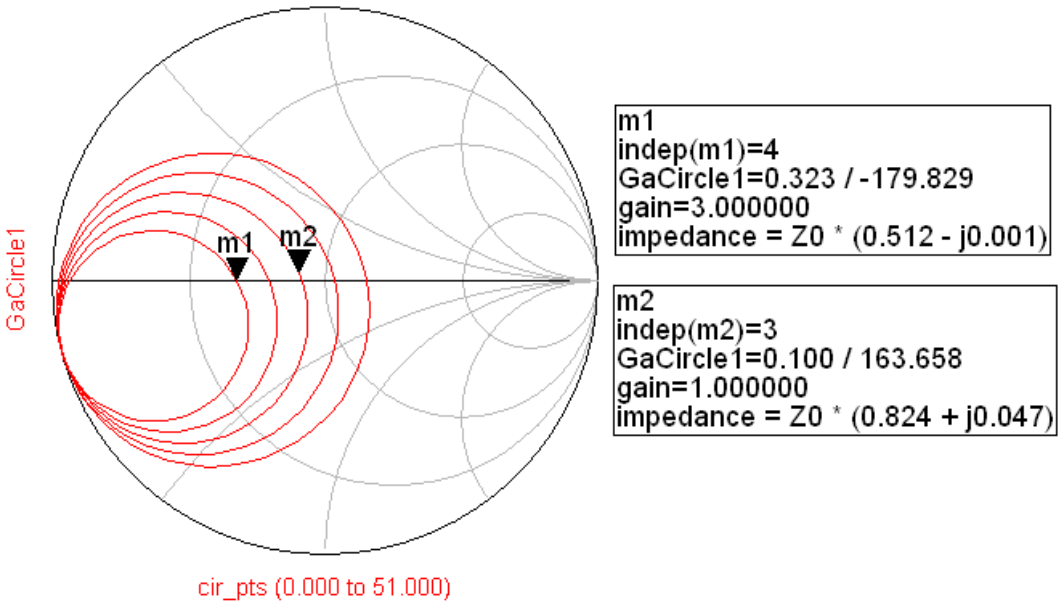


Fig. 2.9 Constant available power gain circles

2.2.4 Output power and P1dB

In general, we use the dBm as the unit for power, and the definition is

$$P_{out}(\text{dBm}) = 10 \cdot \log \frac{P_{out}(\text{mW})}{1(\text{mW})} \tag{2-27}$$

For example, 1W is equal to 30dBm. The equation for output power can be written as

$$P_{out}(\text{dBm}) = P_{in}(\text{dBm}) + \text{Gain}(\text{dB}) \tag{2-28}$$

For ideal case, the gain is the constant, the output power is rising when the input power is rising. But because the non-linear property of active component, the output

power can not increase infinite. With the increase of the power, the gain will reduce gradually. As input power reaches a certain value, the output power can not increase. So we define a point, when the gain is one dB less than the ideal gain, the point is called 1-dB Compression Point. And the output power at this moment is called P1dB. The 1-dB compression point is used to showing the dynamic range of the circuit. The relation between the input power and the output power is shown in Fig. 2.10.

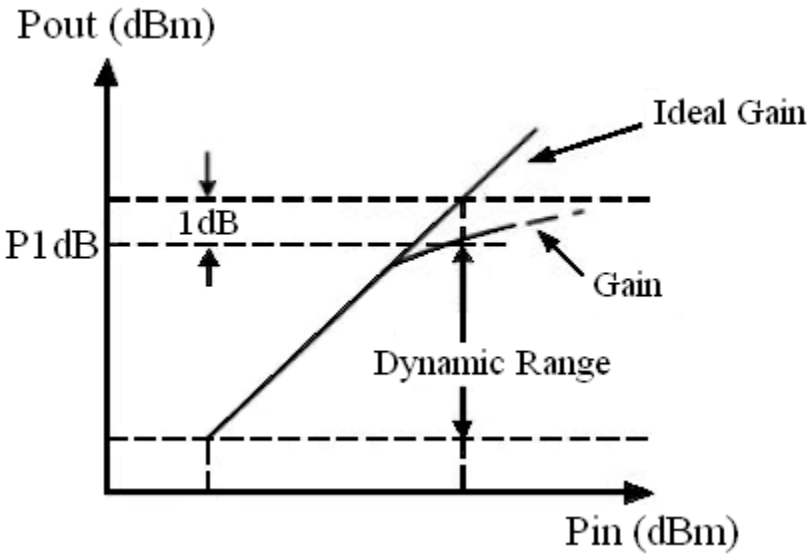


Fig. 2.10 1-dB compression point

2.2.5 Efficiency

For power amplifiers, we can draw a diagram, shown in Fig. 2.11.

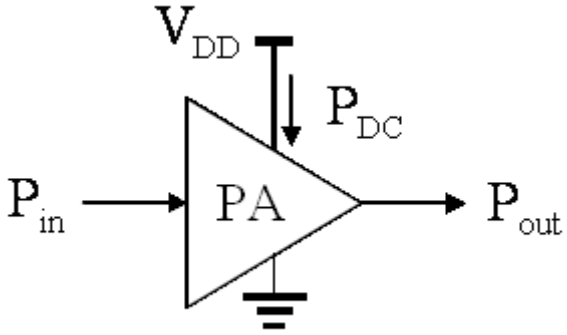


Fig. 2.11 A power amplifier diagram

The efficiency is the conversion ratio from dc power to output power. It plays an important role for power amplifiers. For ideal case, we hope the dc power transform to output power completely. But actuality, it is impossible. There is some power become heat energy. Even if the efficiency is important, we can not increase unrestrictedly. Because it is trade off between the efficiency and the linearity, we must choose the suitable one.

In general, we define three kinds of efficiency for amplifiers.

The first is Drain Efficiency (η_d):

$$\eta_d = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{V_{DC} \cdot I_{DC}} \tag{2-29}$$

The second is Power Added Efficiency (η_{PAE}):

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2-30}$$

Finally is Total Efficiency (η_{total}):

$$\eta_{\text{total}} = \frac{P_{\text{out}}}{P_{DC} + P_{\text{in}}} \tag{2-31}$$

In general cases, $\eta_d > \eta_{PAE} > \eta_{\text{total}}$. But when the power gain is high, we can drive $\eta_d \approx \eta_{PAE} \approx \eta_{\text{total}}$.

2.2.6 Distortion

For active components, they have the effects of nonlinearity. For distortion, we can divide into two kinds, one is harmonic distortion, and another one is Intermodulation Distortion.

For harmonic distortion, it says, when a signal enter a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. If the input is $x(t) = A\cos\omega t$, and the output is

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2-32}$$

then

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \tag{2-33}$$

$$= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \tag{2-34}$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \tag{2-35}$$

In equation (2-34), the term with the input frequency is called the fundamental, and the term with high-order is called the harmonics.

For Intermodulation Distortion, that is, when two signals with different frequency

enter a nonlinear system, the output will produce some components which are not harmonics, they are called intermodulation (IM). It arises from multiplication of the two signals when their sum is raised to a power greater than unity. We assume the input is $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$, and the output is just like equation (2-32). Thus,

$$y(t) = \alpha_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) + \alpha_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 + \alpha_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 \quad (2\text{-}36)$$

Expanding the left side and discarding dc terms and harmonics, we obtain the following intermodulation products:

$$\omega = \omega_1 \pm \omega_2 : \alpha_2 A_1 A_2\cos(\omega_1 + \omega_2)t + \alpha_2 A_1 A_2\cos(\omega_1 - \omega_2)t \quad (2\text{-}37)$$

$$= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 {A_1}^2 A_2}{4}\cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 {A_1}^2 A_2}{4}\cos(2\omega_1 - \omega_2)t \quad (2\text{-}38)$$

$$= 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 {A_2}^2 A_1}{4}\cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 {A_2}^2 A_1}{4}\cos(2\omega_2 - \omega_1)t \quad (2\text{-}39)$$

and these fundamental components

$$\omega = \omega_1, \omega_2 : \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 {A_1}^3 + \frac{3}{2}\alpha_3 A_1 {A_2}^2\right)\cos\omega_1 t + \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 {A_2}^3 + \frac{3}{2}\alpha_3 A_2 {A_1}^2\right)\cos\omega_2 t \quad (2\text{-}40)$$

What we are interested in are the third-order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, because the third-order IM products are of primary interest since they tend to have frequencies that are within the passband, shown in Fig. 2.12.

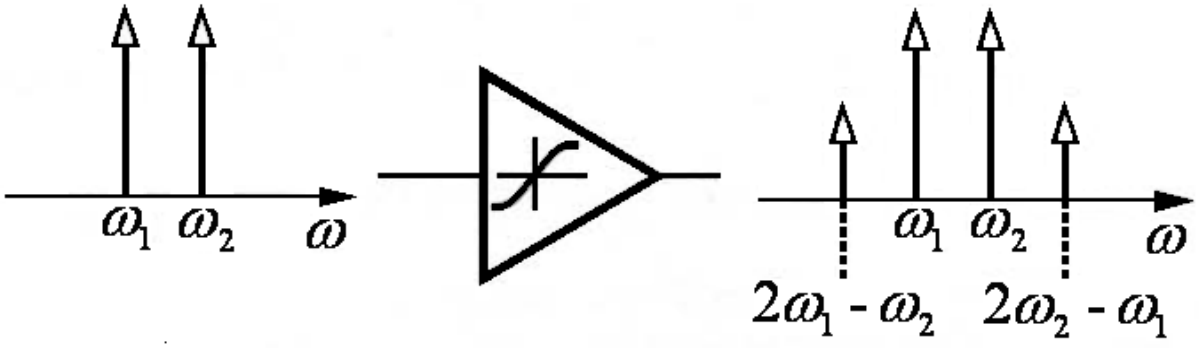


Fig. 2.12 IM in a nonlinear system

The key point here is that if the difference between ω_1 and ω_2 is small, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will be close to ω_1 and ω_2.

IM is a troublesome effect in RF system. If a weak signal accompanied by two strong interferers experiences third-order nonlinearity, then one of the IM products falls in the interest band, corrupting the desired component, showing in Fig. 2.13.

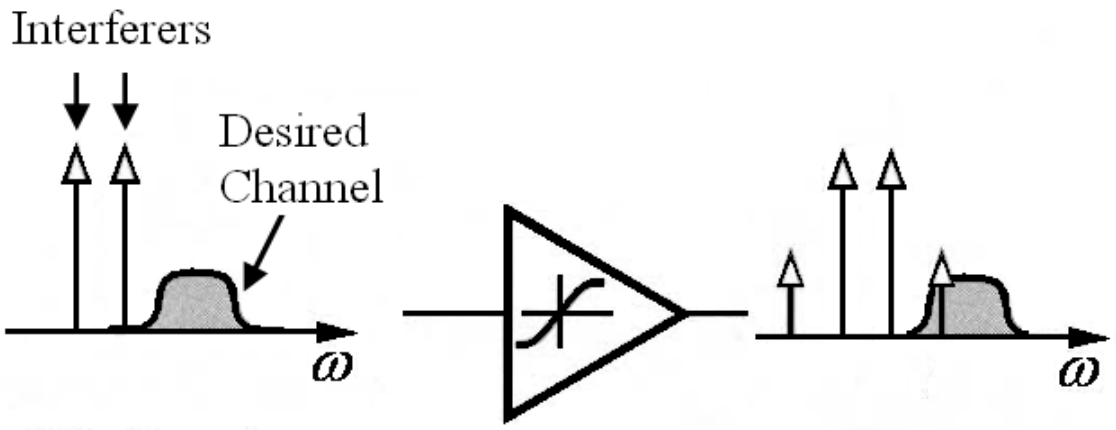


Fig. 2.13 Corruption of a signal due to IM between two interferers

There is a parameter called “third intercept point” (IP3). The parameter is measured

by a two-tone test in which A is chosen to be sufficiently small so that high-order nonlinear terms are negligible and the gain is relatively constant and equal to α_1. The fundamentals increase in proportion to A, and the third-order IM products increase in proportion to A^3, shown in Fig. 2.14(a). If plotted on a logarithmic scale, the magnitude of the IM products grows at three times the rate at which the main components increase. And we define the intersection of the two lines that is the IP3. The horizontal coordinate of the intersection is called the input IP3 (IIP3), and the vertical coordinate is called the output IP3 (OIP3), shown in Fig. 2.14(b).

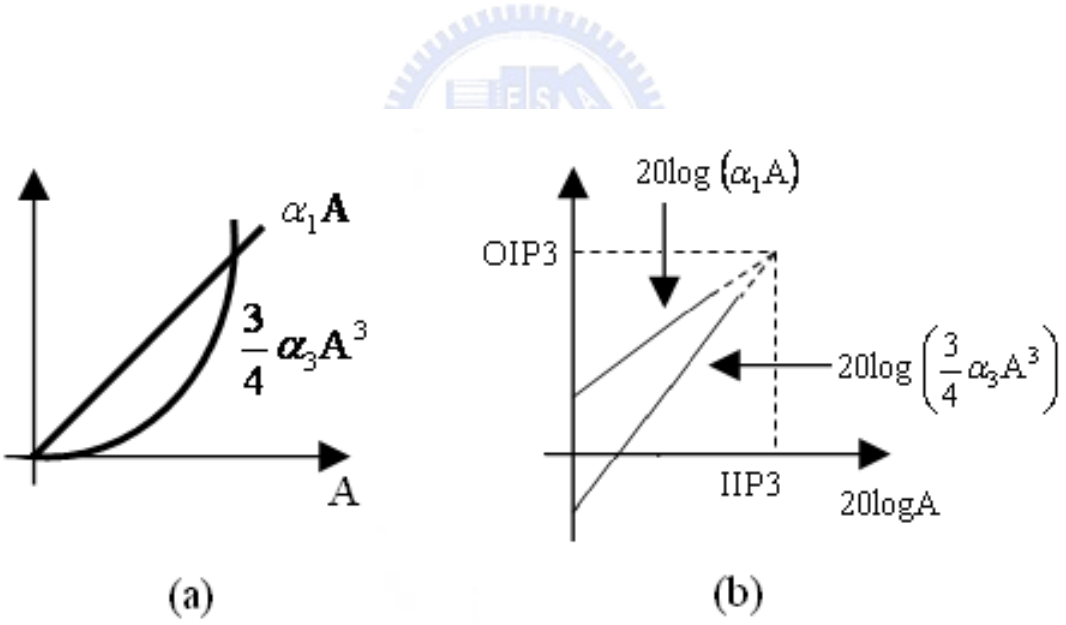


Fig. 2.14 Growth of output components in an IM test

2.2.7 Adjacent channel power ratio (ACPR)

ACPR is a commonly used figure of merit to evaluate the inter-modulation

performance of RF power amplifiers designed for CDMA wireless communication systems, ACPR is a measure of spectral re-growth, appears in the signal sidebands, and is analogous to IM3/IM5 for an analog RF amplifier.

$$\text{ACPR} = \frac{\text{power spectral density in the main channel 1}}{\text{power spectral density in the offset channel 2 or 3}} \tag{2-41}$$

There offset frequencies and measurement bandwidths vary with system application.

2.2.8 Peak-to-Average Ratio (PAR)

All single or multi-carrier (modulated or un-modulated) have a peak-to-average ratio. The ratio between the peak power (Pp) and the average power (Pa) of a signal is called the peak-to-average ratio, i.e.

$$\chi = \frac{P_p}{Pa}, 10\log\frac{Pp}{Pa}(\text{dB}) \tag{2-42}$$

The peak-to-average ratio ΔPs of an input signal consisting of N carriers, each having a average power Pi is defined as

$$\Delta\text{Ps} = \frac{\left(\sum_{i=1}^{n}\sqrt{P_i\chi_i}\right)^2}{\sum_{i=1}^{n}P_i} \tag{2-43}$$

Here χ_i is the peak-to-average ratio of the *i*th carrier. If there are n carriers in a given operating bandwidth, it is easy to see that the theoretical maximum peak-to-average power ratio will be $\sqrt{n}$. Gaussian noise has a peak-to-average ratio of about 9 dB, so very dense multi-carrier systems might require about 6 dB more power

back-off to achieve a similar level of IM distortion compared to a two-carrier signal having the same power.

2.3 Classification of power amplifier

We can determine the class of operation of power amplifiers by the conduction angle, input signal overdrive, and the output load network. The relation between the conduction angle, the input signal over-drive and the power amplifier is shown in Fig. 2.15.

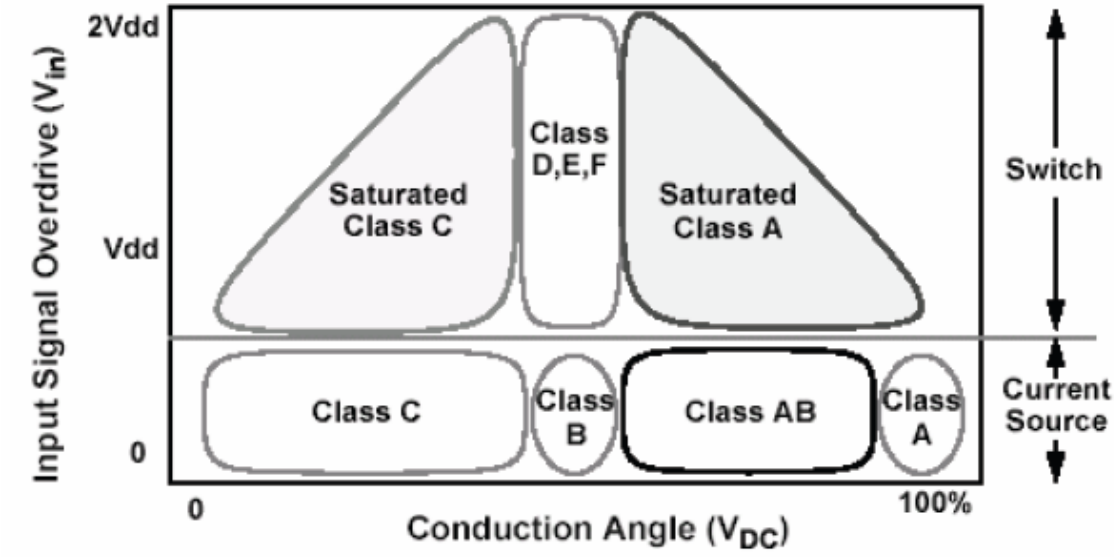


Fig. 2.15 Classification of power amplifier

RF power amplifiers are commonly designated as classes A, B, C, D, E, and F. All

but class A employ various nonlinear, switching, and wave-shaping techniques. Classes of operation differ not in only the method of operation and efficiency, but also in their power output capability. The power output capability or called transistor utilization factor is defined as output power per transistor normalized for peak drain voltage and current of 1 V and 1 A, respectively.

2.3.1 Class A, B, AB, and C

In class A power amplifier, it is biased so that the output current flows at all the time, and the input signal drive level is kept small enough to avoid driving the transistor in cut-off. Or we can say that the conduction angle of the transistor is 360°, meaning that the transistor conducts for the full cycle of the input signal.

When the amplifier in class A, it is inherently linear, hence increasing the quiescent current or decreasing the input signal level monotonically decreases IMD and harmonic levels. Since both positive and negative excursions of the drive affect the drain current, it has the highest gain.

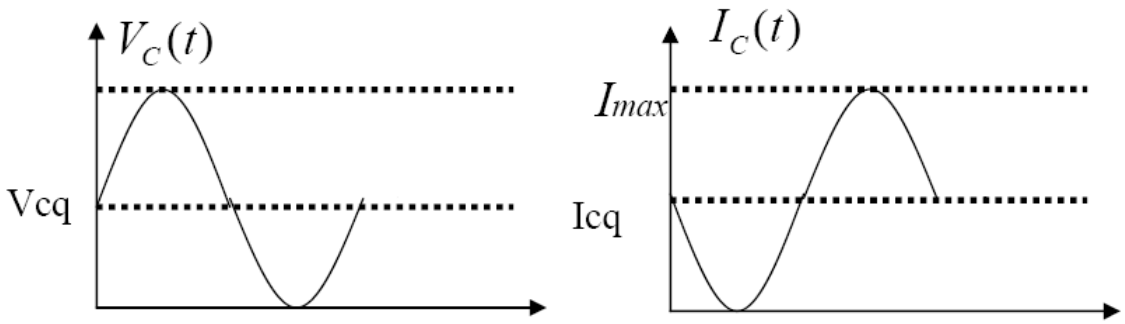


Fig. 2.16 The waveform of voltage and current

The output power is

$$P_{out} = \frac{1}{2}\left(V_{CEQ} - V_{min}\right)\cdot\left(I_{CQ} - I_{min}\right) \tag{2-44}$$

And in ideal case, V_{min} and I_{min} are both equal to zero. So we can get the maximum efficiency is

$$\eta_{c,max} = \frac{P_{out,max}}{P_{DC}} = \frac{\frac{1}{2}V_{CC}I_{CC}}{V_{CC}I_{CC}} = 50\% \tag{2-45}$$

The voltage V_C reaches the maximum value only if the device is off. Typically the efficiency is lower than 40% for linear operation.

The output power capability is

$$P_N = \frac{P_{out}}{V_{max}I_{max}} = \frac{\frac{1}{2}\frac{V_{max}}{2}\frac{I_{max}}{2}}{V_{max}I_{max}} = \frac{1}{8} \tag{2-46}$$

In class B power amplifier, the gate bias is set at the threshold of conduction so that the quiescent drain current is zero. And the conduction angle for the transistor is approximately 180°. Thus the transistor conducts only half of the time, either on positive or negative half cycle of the input signal.

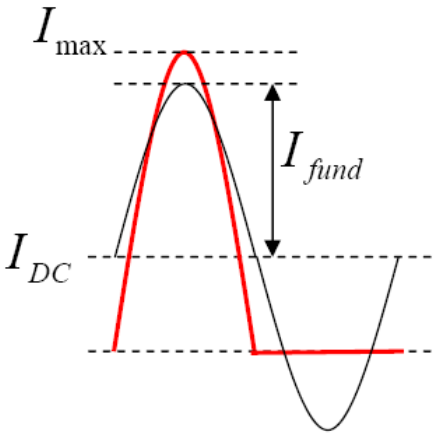


Fig. 2.17 The waveform of current

We can define that

$$I_{fund} = \frac{I_{max}}{2} = I_{CQ} \tag{2-47}$$

$$I_{DC} = \frac{I_{max}}{\pi} \tag{2-48}$$

$$P_{out} = \frac{1}{2}\left(V_{CEQ} - V_{min}\right)\left(I_{fund}\right) \tag{2-49}$$

And in ideal case, V_{min} is zero. So we obtain

$$P_{out,max} = \frac{1}{2} V_{CEQ} I_{fund} \tag{2-50}$$

$$\eta_{c,max} = \frac{P_{out,max}}{P_{DC}} = \frac{\frac{1}{2} V_{CC} \frac{I_{max}}{2}}{V_{CC} \frac{I_{max}}{\pi}} = \frac{\pi}{4} = 78.5\% \tag{2-51}$$

$$P_N = \frac{1}{8} \tag{2-52}$$

Class B amplifiers are more efficient than class A amplifiers.

In class AB power amplifier, it is a compromise between class A and class B in terms of efficiency and linearity. And it is biased typically to a quiescent point, which is in the region between the cutoff point and the class A bias point. In this case, the

transistor will be turn on for more than a half cycle, but less than a full cycle of the input signal. So the conduction angle in class AB is between 180° and 360°, and the efficiency is between 50 % and 78.5 %.

In class C power amplifier, the gate is biased below threshold so that the transistor is on for less than half of a cycle, or the conduction angle is less than 180 degree. The linearity is lost. The efficiency can achieve toward 100 %, but the output drops down to zero. A typical compromise is a conduction angle of 150° and an ideal efficiency of 85 %. It is little used in solid-state PA because it requires low drain resistances, making implementation of parallel-tuned output filters difficult.

The bias condition for various classes of power amplifier on device I-V characteristics is shown in Fig. 2.18.

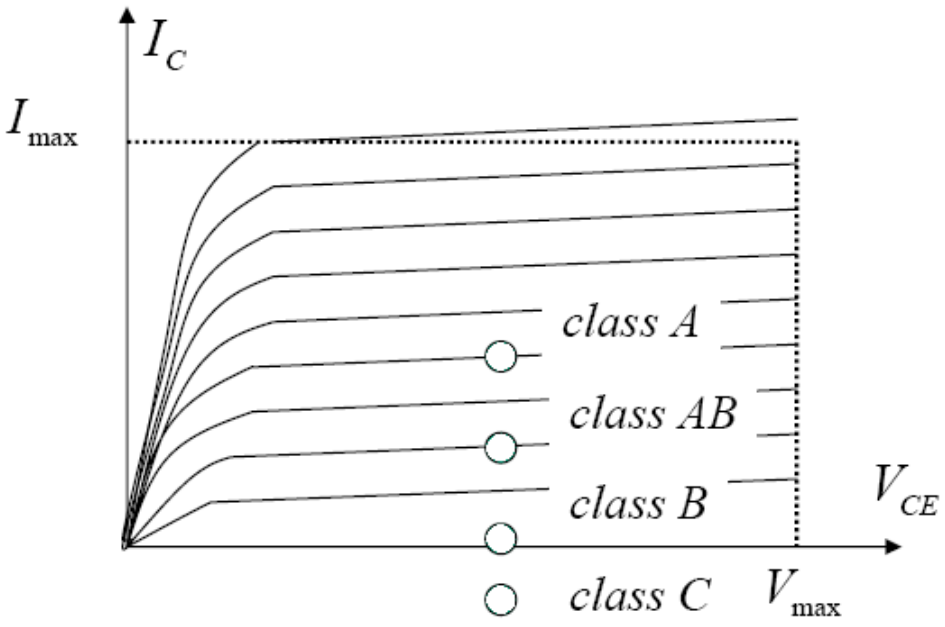


Fig. 2.18 The bias condition for various classes of power amplifier

For these classes, transistor works as a transducer and the RF output power is proportional to the RF input power. And the difference is shown in Table 2.1.

Mode	**Conduction**	**Efficiency**	**Linearity**
Class A	100%	Poor	Excellent
Class AB	50~100%	Between A and B	Between A and B
Class B	50%	Moderate	Moderate
Class C	<50%	Excellent	Poor

Table 2.1 The operation in different mode

The harmonics amplitude is plotted in Fig. 2.19. We can see the odd harmonics be seen to pass through zero at the class B point, but in AB mode, the third harmonic is not negligible.

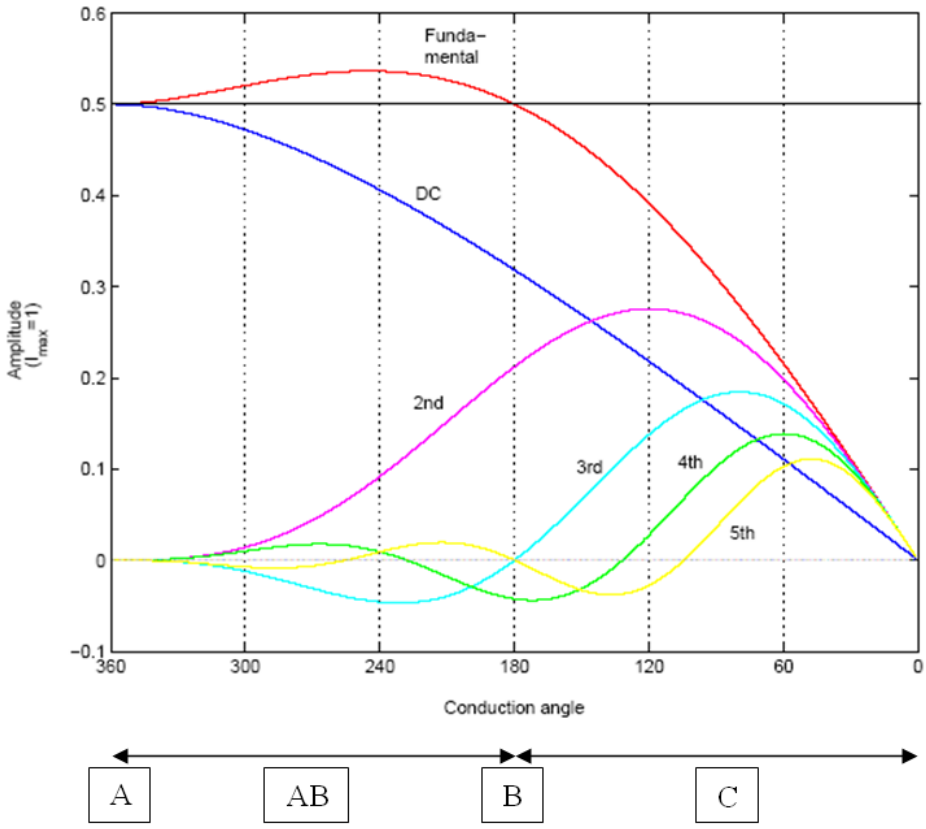


Fig. 2.19 All components in the current waveform

Then we can plot the efficiency and output power on Fig. 2.20. From this figure the main features of class A, AB, B and C can be determined.

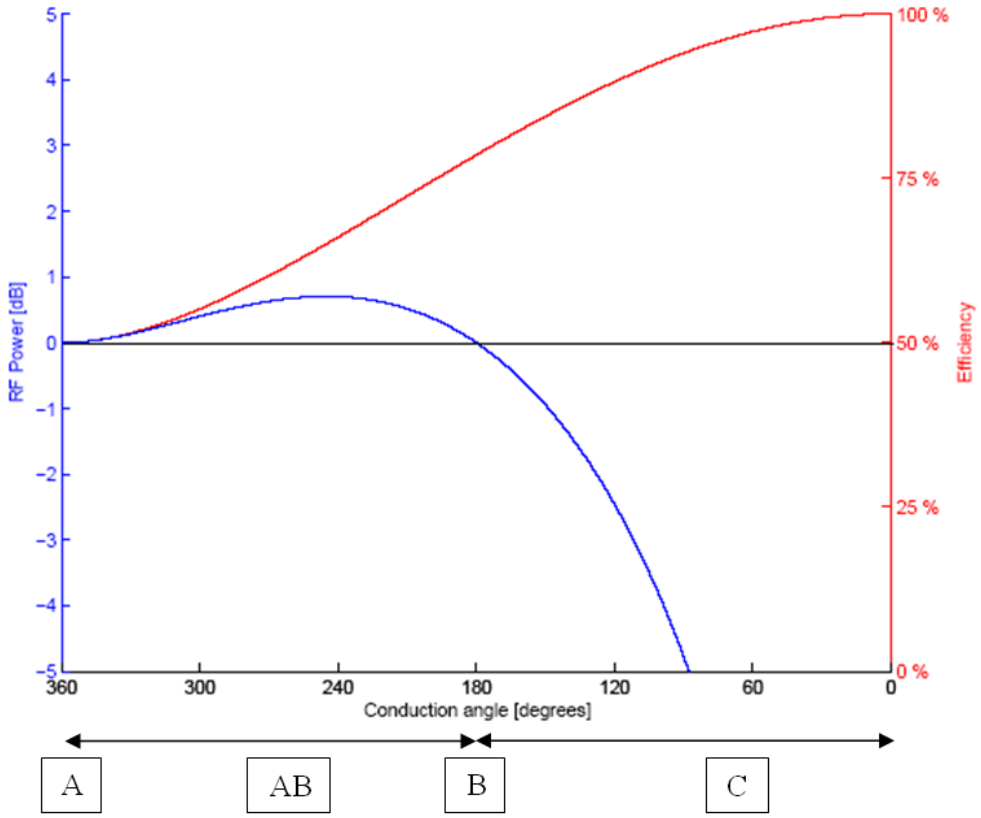


Fig. 2.20 RF power and efficiency with conduction angle

2.3.2 Class D, E, and F

The voltage mode Class D amplifier is defined as a switching circuit that results in the generation of a half-sinusoidal current waveform and a square voltage waveform. The class D power amplifiers use two or more transistors as switches to generate a square drain-voltage waveform. A series-tuned output filter passes only the fundamental frequency component to the load, the class D amplifiers suffer from a number of problems that make them difficult to realize, especially at high frequencies. The output power is

$$P_{out} = \frac{1}{2} I_{out}{}^2 R_L = \frac{1}{2} \left(\frac{\frac{2}{\pi} V_{DD}}{R_L} \right)^2 R_L = \frac{2}{\pi^2} \frac{V_{DD}{}^2}{R_L} \tag{2-53}$$

And

$$P_N = \frac{P_{out}}{V_{DD} \frac{2}{\pi} \frac{V_{DD}}{R_L}} = \frac{1}{\pi} \tag{2-54}$$

Class E employs a single transistor operated as a switch. The drain voltage waveform is the result of the sum of the DC and RF currents charging the drain-shunt capacitance. In optimum class E, the drain voltage drops to zero and has zero slope just as the transistor turns on. The result is an ideal efficiency of 100 %, elimination of the losses associated with charging the drain capacitance in class D, reduction of switching losses, and good tolerance of component variation.

The output power is

$$P_{out} = \frac{2}{1 + \pi^2 / 4} \frac{V_{DD}{}^2}{R_L} \approx 0.577 \frac{V_{DD}{}^2}{R_L} \tag{2-55}$$

And

$$P_N = \frac{P_{out}}{V_{ds,max} I_{ds,max}} = \frac{0.577 \cdot V_{DD}{}^2 / R_L}{3.6 V_{DD} \cdot 1.7 V_{DD} / R_L} \approx 0.098 \tag{2-56}$$

Class F boosts both efficiency and output by using harmonic resonators in the output network to shape the drain waveforms. The voltage waveform includes one or more odd harmonics and approximates a square wave, while the current includes even harmonics and approximates a half sine wave. Alternately (“inverse class F”), the

voltage can approximate a half sine wave and the current a square wave.

The output power is

$$P_{out} = \frac{[(4/\pi)V_{DD}]^2}{2R_L} \approx 0.81\frac{V_{DD}^{\ 2}}{R_L} \tag{2-55}$$

And

$$P_N = \frac{P_{out}}{V_{ds,max}I_{ds,max}} = \frac{P_{out}}{2V_{DD}\cdot\frac{8}{\pi}\frac{V_{DD}}{R_L}} = \frac{1}{2\pi} \approx 0.16 \tag{2-56}$$

For these classes, transistor operates as a switch. And the ideal efficiency is 100 %.

The waveforms of ideal power amplifiers for class A to F are shown in Fig. 2.21.

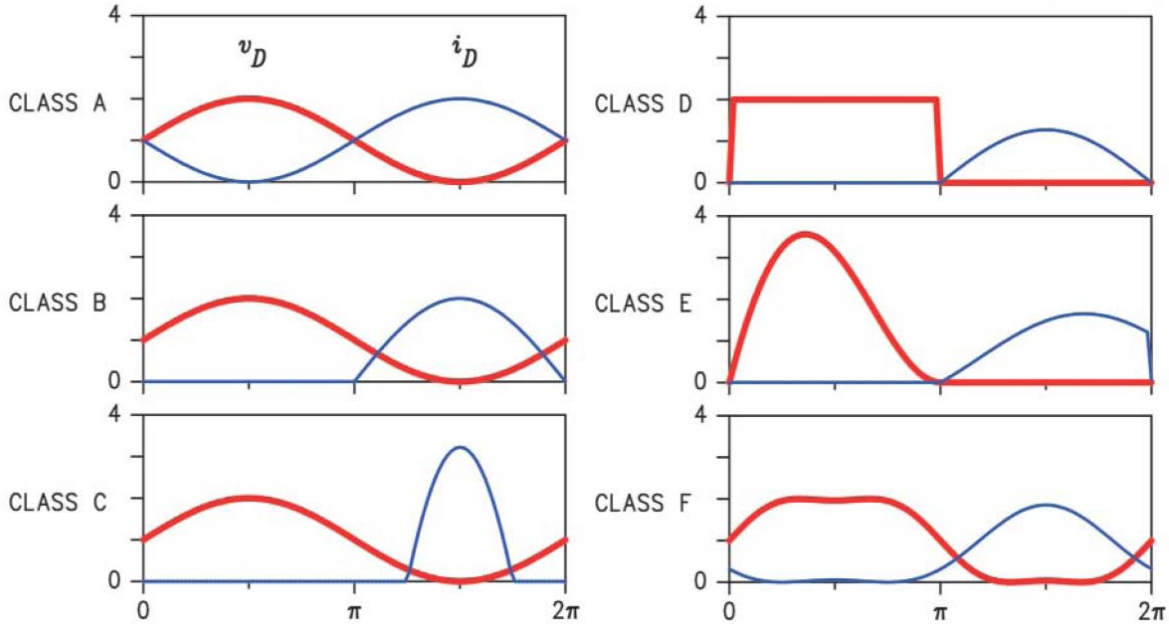


Fig. 2.21 Waveforms of ideal power amplifiers

Chapter 3

Asymmetric LDD MOS Power Cell

3.1 Why asymmetric LDD MOS

In recent research, a new asymmetric-lightly-doped-drain (LDD) MOS transistor that is fully embedded in a CMOS logic without any process modification or extra cost. And it can improve the power performance in radio frequency.

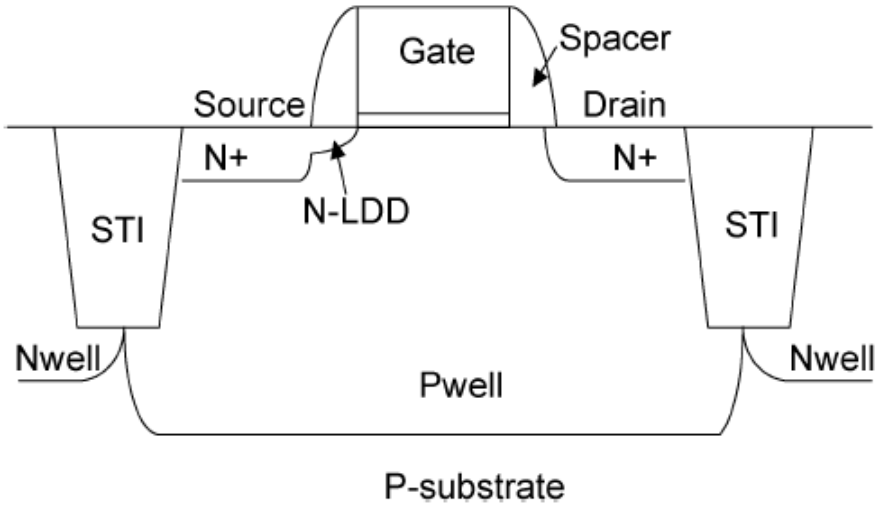


Fig. 3.1 Device structure of asymmetric-LDD MOS

The structure of asymmetric-LDD MOS is shown in Fig. 3.1. The major difference to conventional MOS transistor is no n^+-LDD region at drain side. The formed depletion region under reverse drain bias can sustain large voltage. It can overcome the low breakdown voltage issue for RF power application.

Fig. 3.2 shows the comparison of drain breakdown voltage for conventional and asymmetric-LDD MOS transistors. We can see that the drain breakdown voltage for conventional MOS transistor is about 3.6 V, and the drain breakdown voltage for asymmetric-LDD MOS transistor is about 7.0 V under the same criteria.

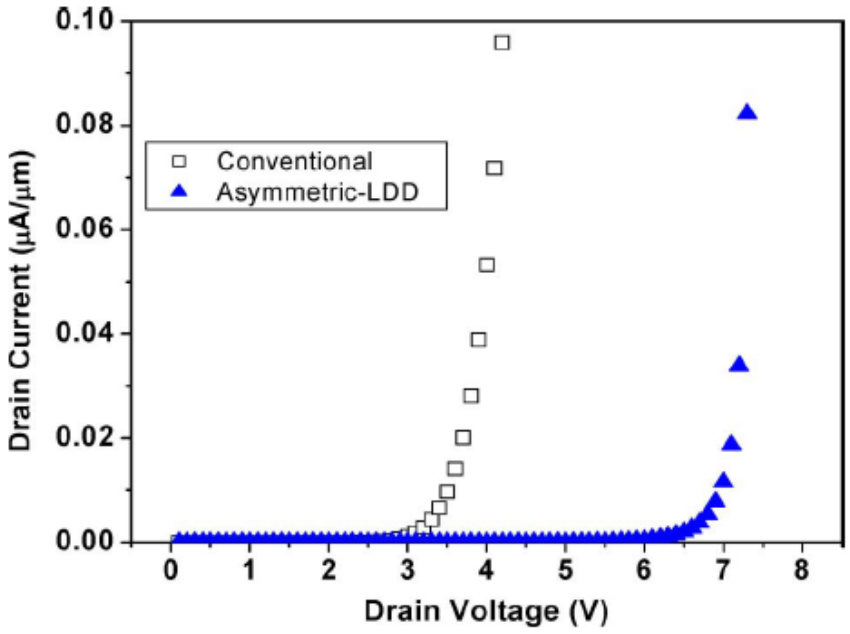


Fig. 3.2 The drain breakdown voltage at V_{gs}=0 V with 0.23 μm gate length

This new structure preserves the high frequency operation of sub- μm MOS transistors with 34 GHz cutoff frequency (f_t), it is close to the 35 GHz of conventional MOS transistor. And the 86 GHz maximum oscillation frequency (f_{max}) higher than the 76 GHz of conventional MOS transistor.

Compare the asymmetric device and the conventional device, we can see that the

asymmetric device has larger output power and higher power-added efficiency. The output power is increased by 38 % from 130 to 180 mW/mm at 2.4 GHz, the PAE can be improved by 16 % to conventional device, shown in Fig. 3.3.

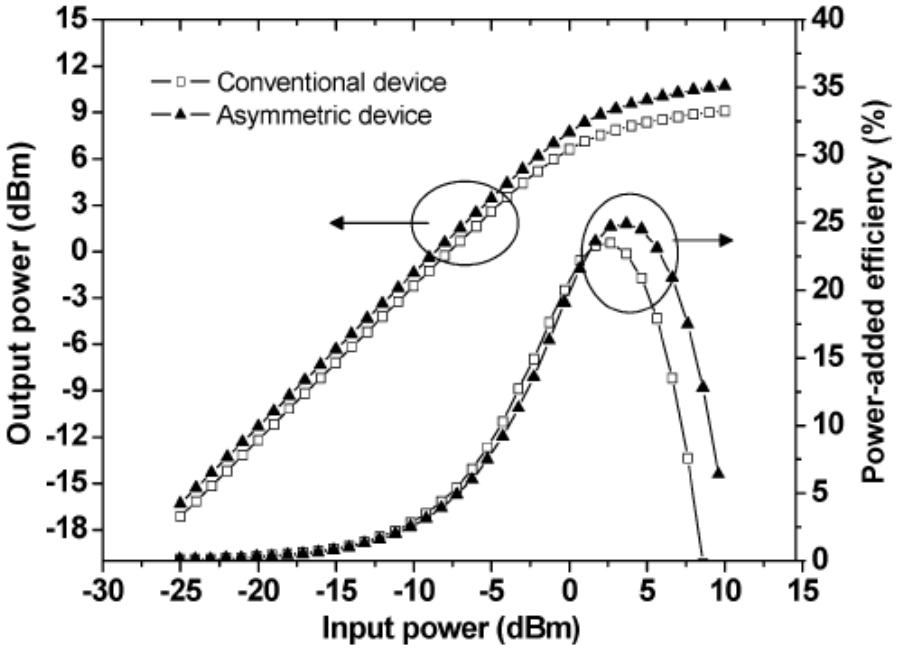


Fig. 3.3 Measured RF output power and PAE versus the input power for conventional and asymmetric-LDD MOS transistors at 2.4 GHz.

3.2 Model building

Without n^+-LDD region at drain side, the decrease with the gate to drain capacitance and the gate to source capacitance. In addition, the depletion layer become longer, the resistance from gate to drain become larger.

The asymmetric LDD NMOS model and the equivalent circuit are shown in

Fig.3.4.

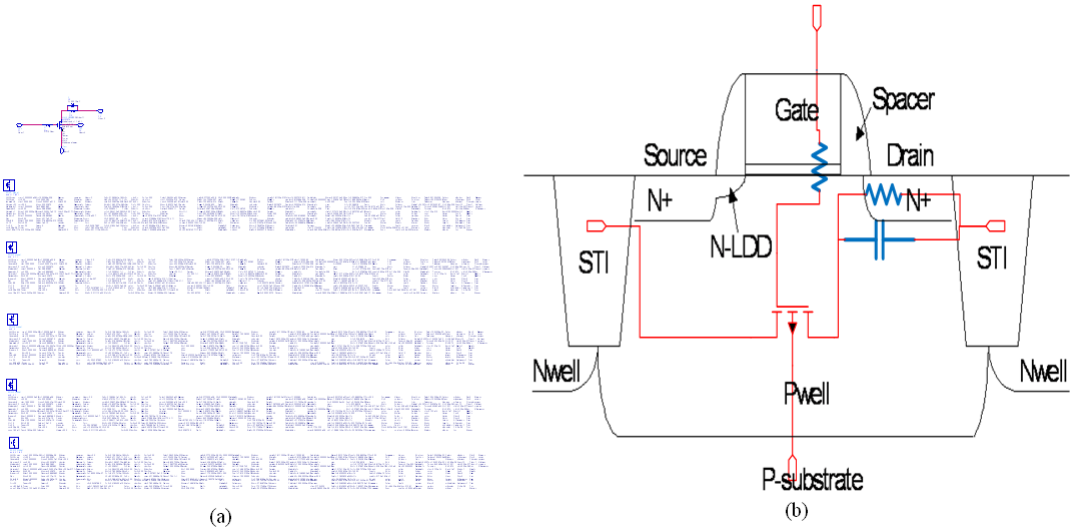


Fig. 3.4 Asymmetric LDD NMOS model (a) The BSIM model of A-LDD NMOS

(b) The equivalent circuit of A-LDD NMOS

Chapter 4

Power Amplifier Design

4.1 Circuit design

In this work, the two-stage circuit has been used to realize a power amplifier. The power amplifier separates into drive stage and power stage. And the drive stage and the power stage operate in class A. The simplified schematic of the circuit is shown in Fig. 4.1.

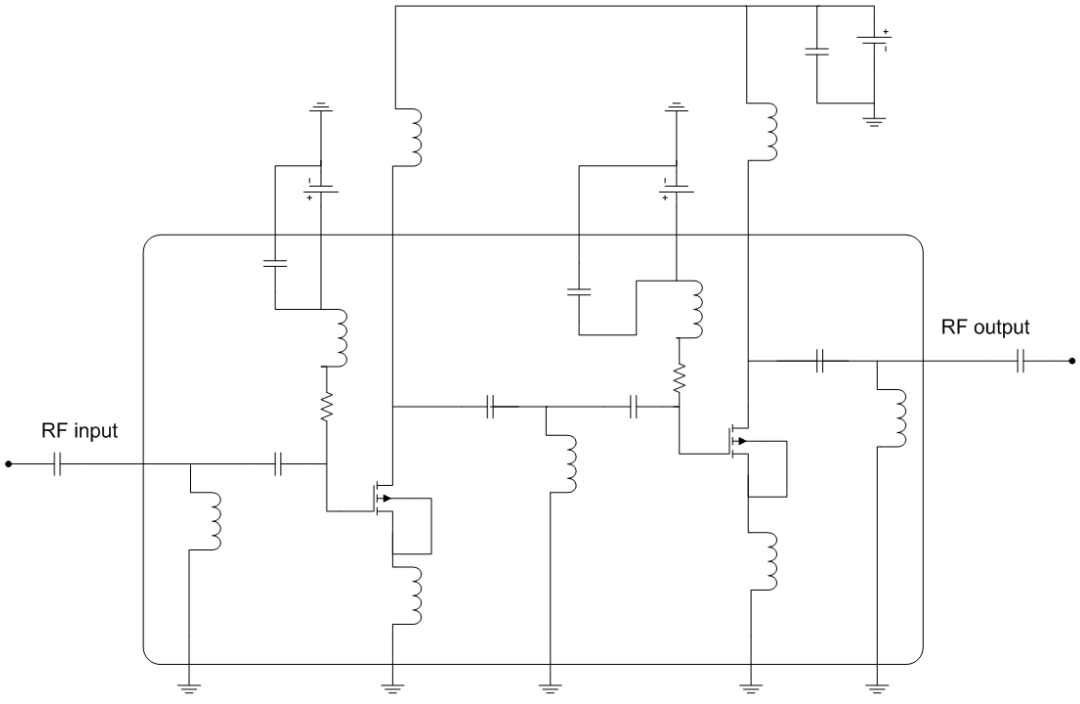


Fig. 4.1 Schematic of the two stage amplifier circuit

For the power efficiency issue, we use the ratio of size for power stage and driver stage is 4:1. In drive stage and power stage, the BSIM3 model of asymmetric-LDD

MOS transistor has been used in PA design. The unit cell of asymmetric-LDD MOS transistor designed in this work has 0.18 μm gate-length, 5 μm width, and 10 gate fingers. And asymmetric-LDD MOS transistors have been implemented by foundry standard 0.18 μm 1P6M process with only one additional mask but without process modification.

4.2 Design flow

For the design of power amplifier, there are some points that must be considered. Such as supply voltage, frequency range, s-parameters, stability, gain, output power, input power levels, linearity and efficiency. So the first step of design, we have to determine the goal. Then use some methods to reach the goal. When the goal is determined, we choose the operating type and the bias point. Then we use the ideal lumped elements to design the input, internal, and the output matching network with some adjustment. After this, we replace the ideal lumped elements with TSMC model. The design procedure of the amplifier has been carried out through the iteration of ADS and EM simulation. The design flow chart is shown in Fig. 4.2.

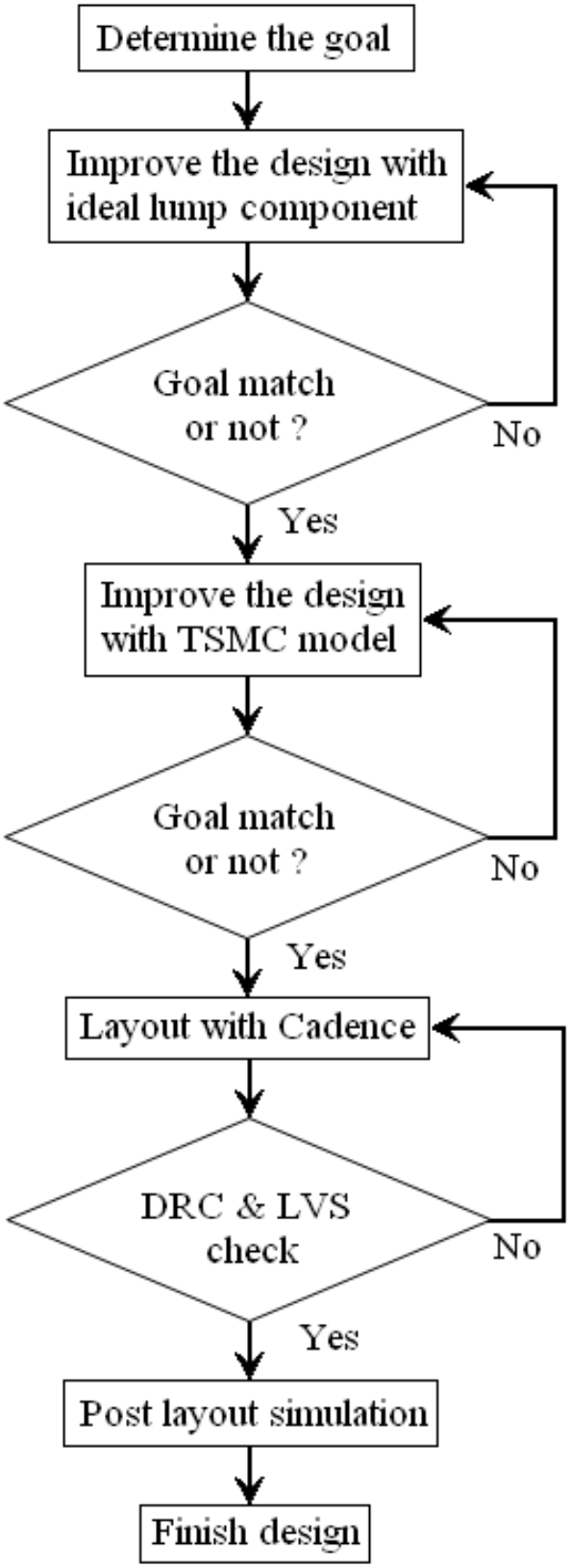


Fig. 4.2 Design flow chart

4.3 Pre-layout simulation

In this work, the goal we want to reach is shown in Table 4.1.

Operating type	Class A
Frequency range	2.4GHz
Supply voltage	3V
S11	<-10dB
Power gain	>20dB
Output P1dB	>24dBm
PAE @ P1dB	>20%
OIP3	>40dBm

Table 4.1 The goal of power amplifier

The architecture we use for the power amplifier is just like Fig. 4.1. The transistors in the power amplifier are asymmetric-LDD MOS transistors that introduce in chapter 3. And all of the transistors have 0.18 μm gate-length, 5 μm width, and 10 gate fingers.

For gate bias, the voltage we use in the drive stage and the power stage are both 1 V. And we add inductor to get the result of RF choke and matching.

For drain bias, we use 3 V. And we add inductor to get the result of RF choke and matching.

For stability, we add resistor at gate and inductor at source to improve it.

So we can draw the schematic like Fig. 4.3.

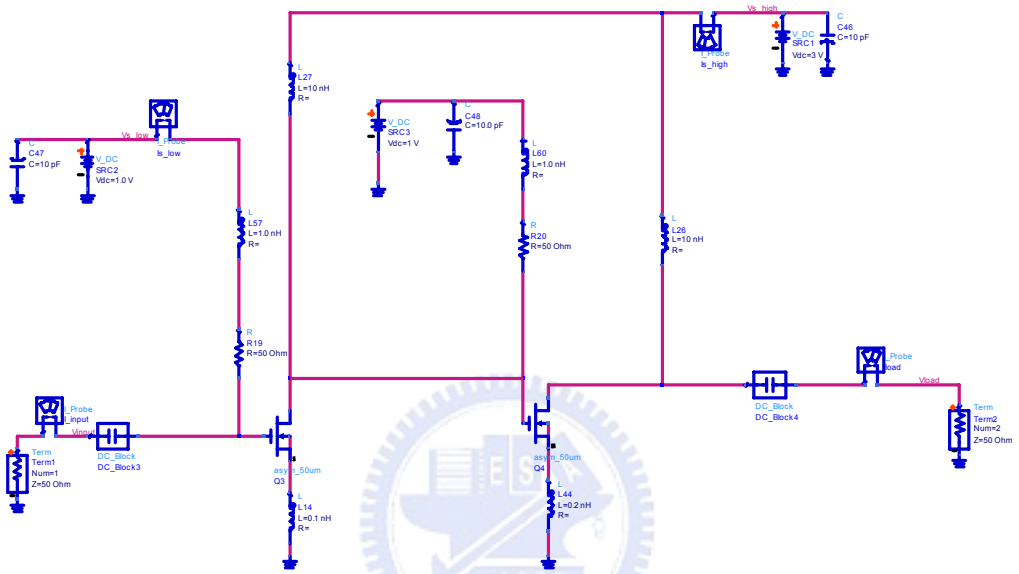


Fig. 4.3 schematic

Then we need to design the matching network. For the input matching network and the inter-stage matching network, we use conjugate matching to get the maximum gain. We use the Smith Chart to design like Fig. 4.4.

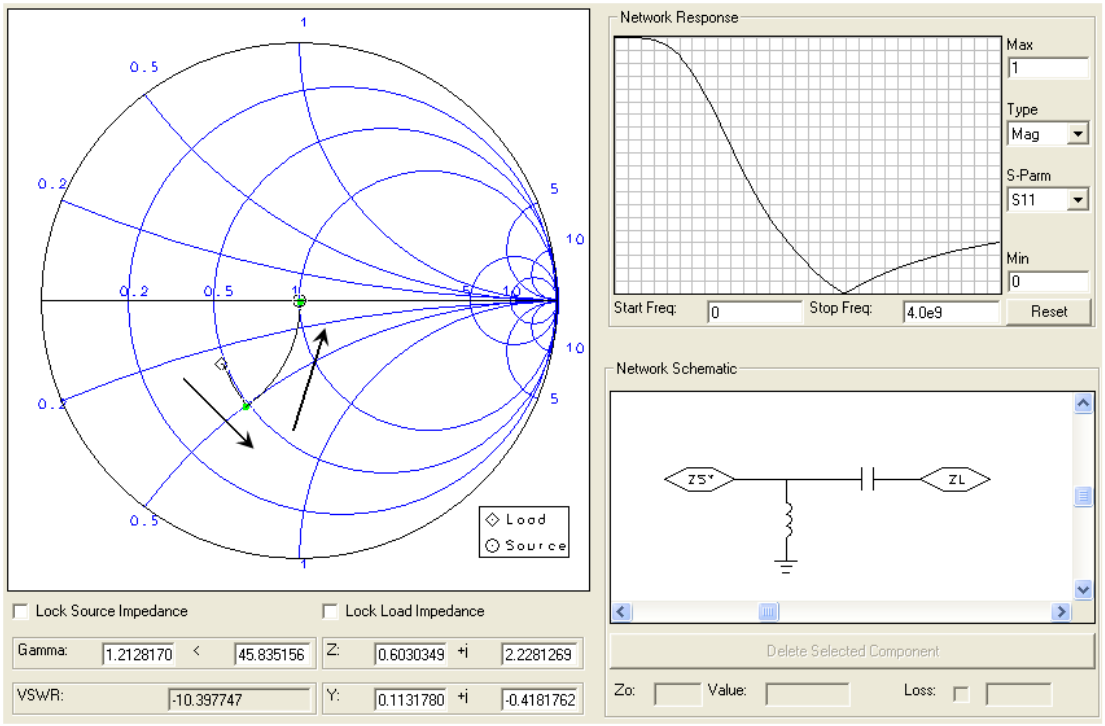


Fig. 4.4 Smith Chart for matching network

After matching, we can get the new schematic like Fig.4.5.

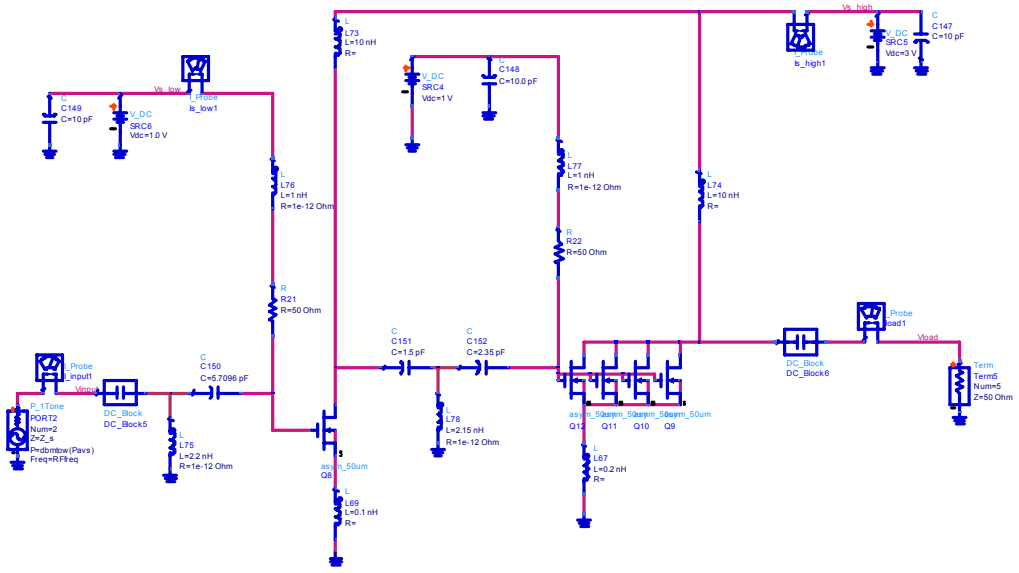


Fig. 4.5 Schematic after input and inter-stage matching

Then we need to design the output matching network. For a power amplifier, the power is very important. So we must design the output matching network to get the maximum power. Here we use the load-pull method in ADS to design. Load-pull is a method that can find out the impedance of the best power and the best efficiency in Smith Chart, shown in Fig. 4.6 and Fig. 4.7.

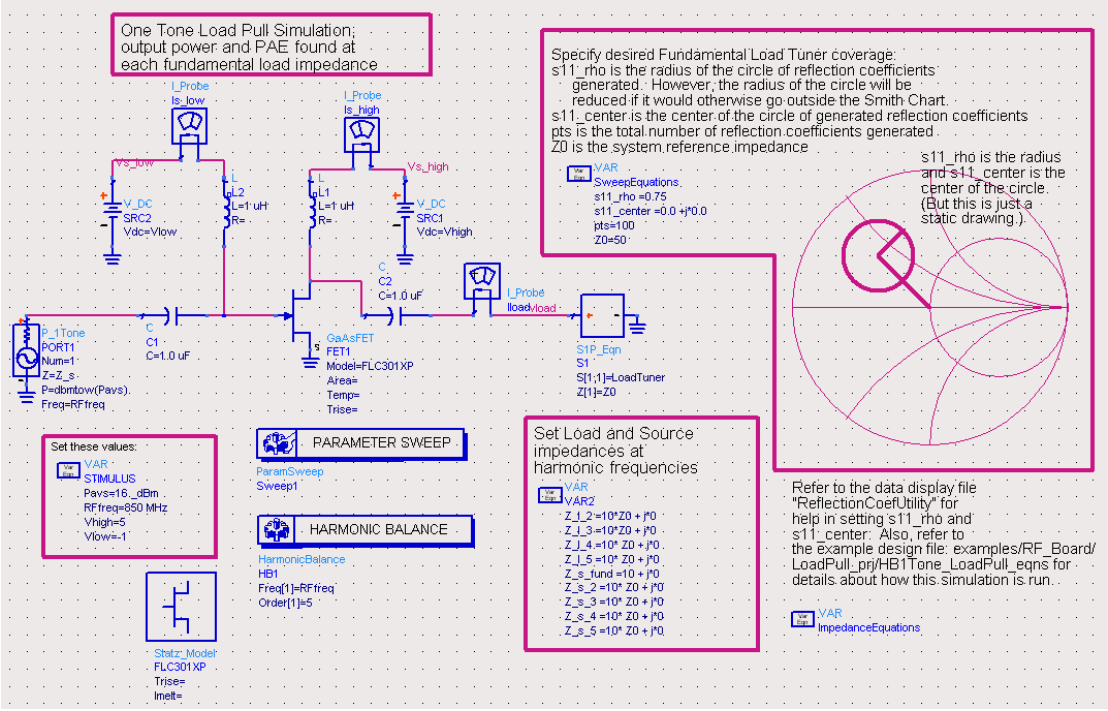


Fig. 4.6 Schematic of load-pull in ADS

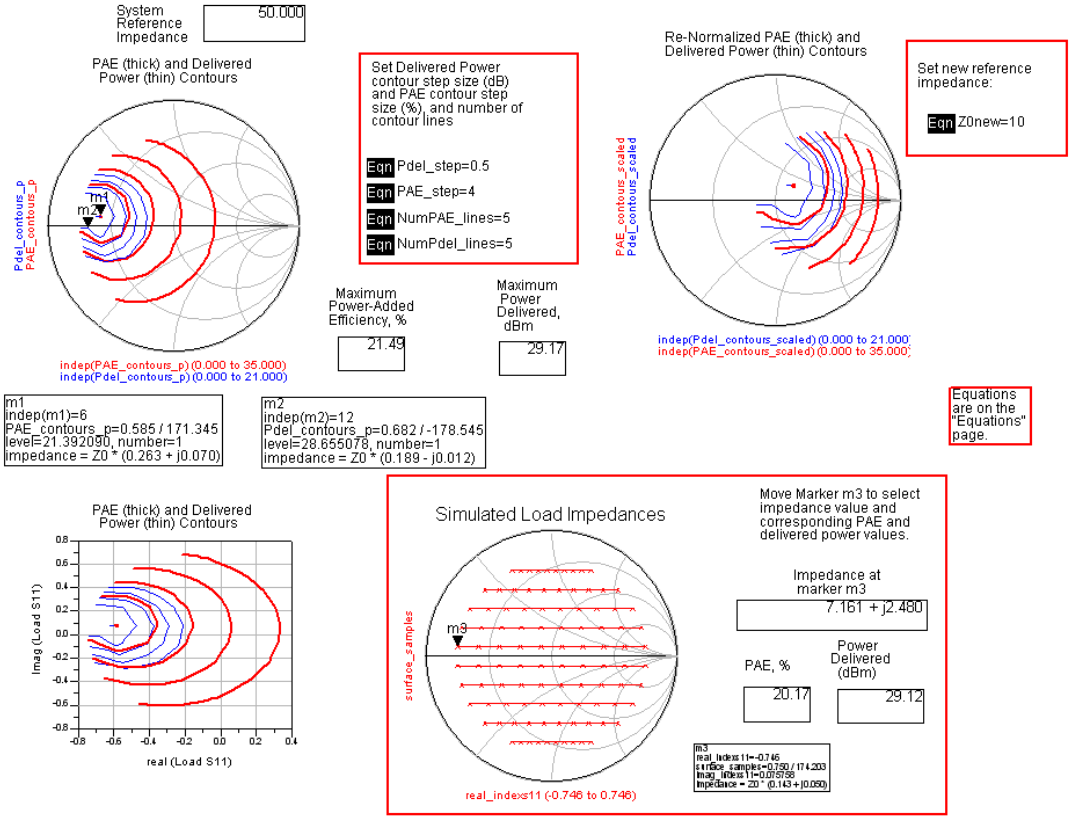


Fig. 4.7 Simulation result of load-pull in ADS

The simulation result of load-pull in this work is shown in Fig. 4.8.

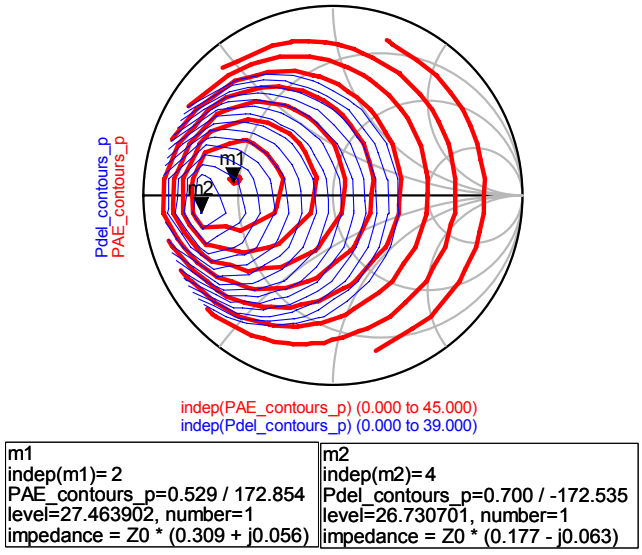


Fig. 4.8 Load-pull for this PA

We can get the impedance for power (blue) and efficiency (red) from Fig. 4.8. We select the point near these two centers of a circle, accord with the goals of power and efficiency at the same time.

After repeated matching, we get the power amplifier with ideal lumped elements. Then we replace the ideal lumped elements with TSMC model. And after tuning, we get the final power amplifier. The schematic is shown as follow.

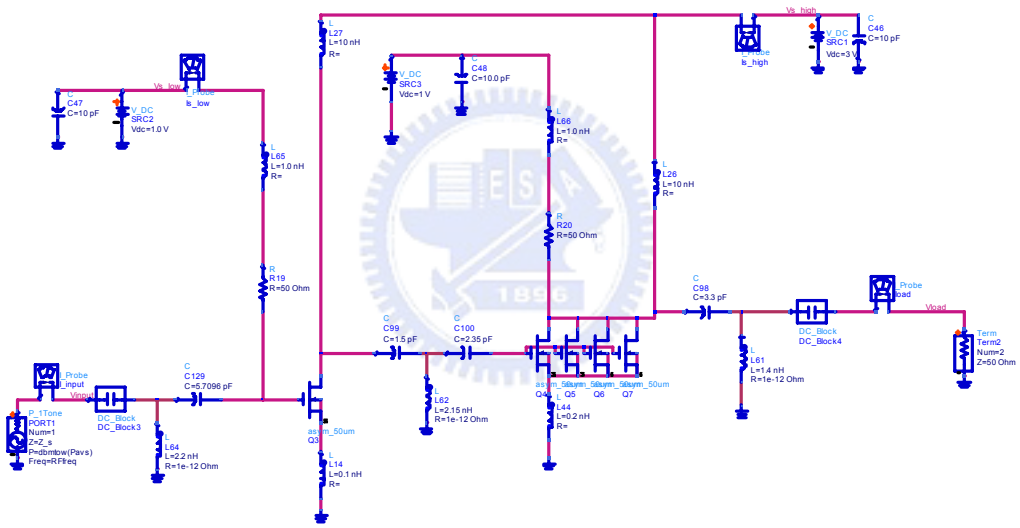


Fig. 4.9 Ideal lump schematic

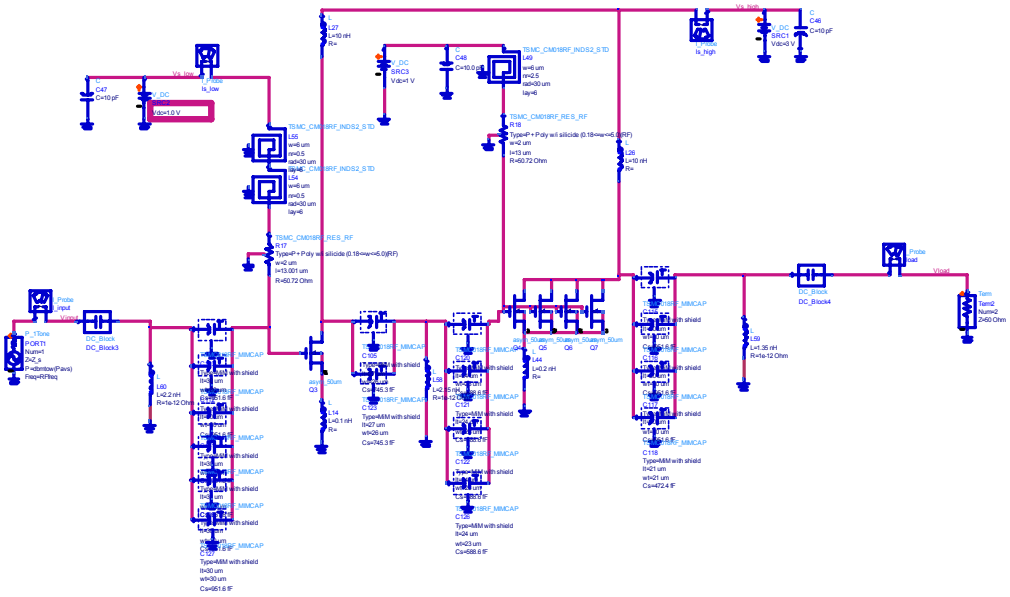


Fig. 4.10 TSMC model schematic

The simulation results are shown as follow.

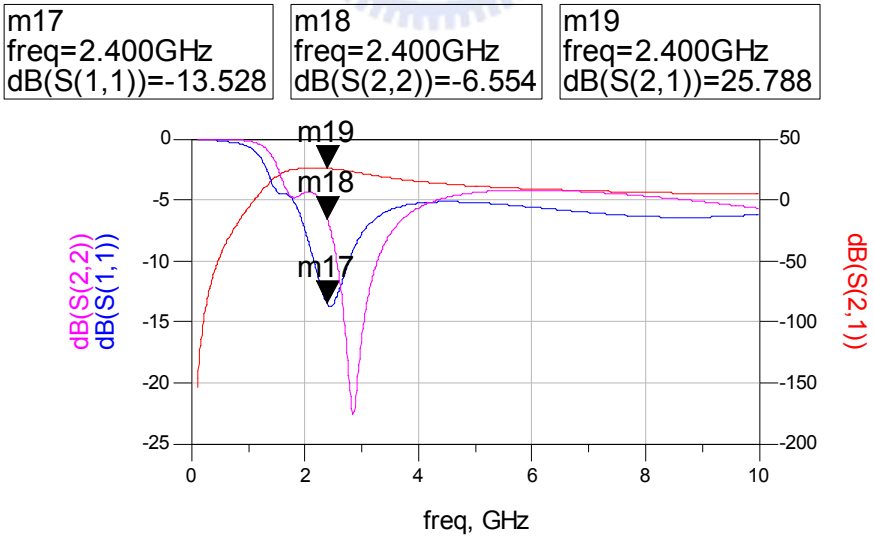


Fig. 4.11 S-parameter of pre-layout simulation

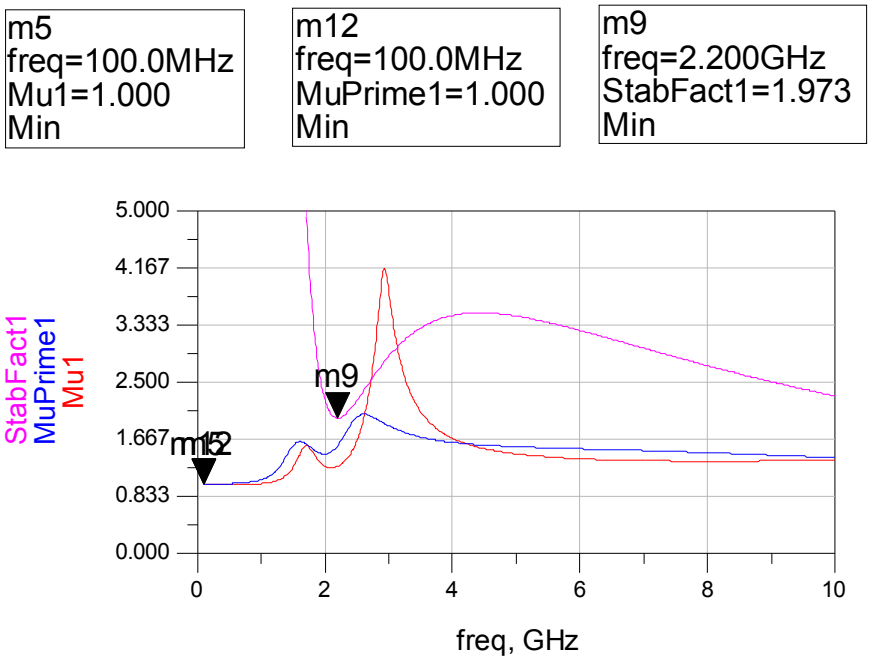


Fig. 4.12 Stability factor of pre-layout simulation

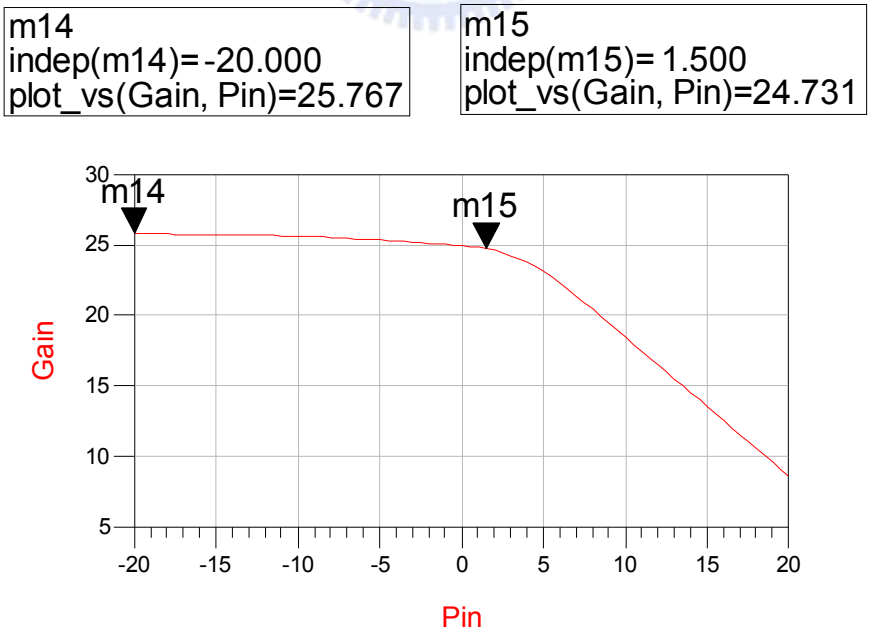


Fig. 4.13 Power gain of pre-layout simulation

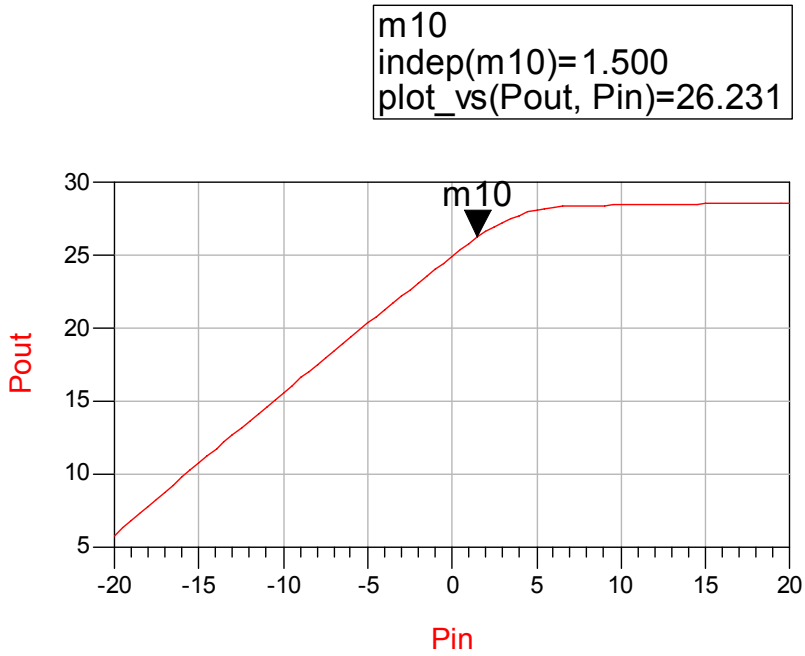


Fig. 4.14 Output power of pre-layout simulation

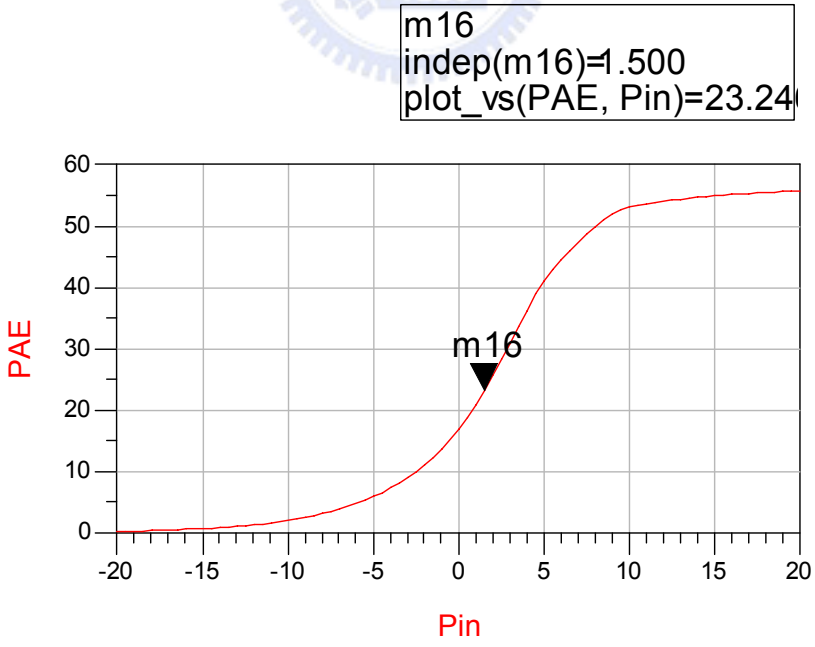


Fig. 4.15 Power Added Efficiency of pre-layout simulation

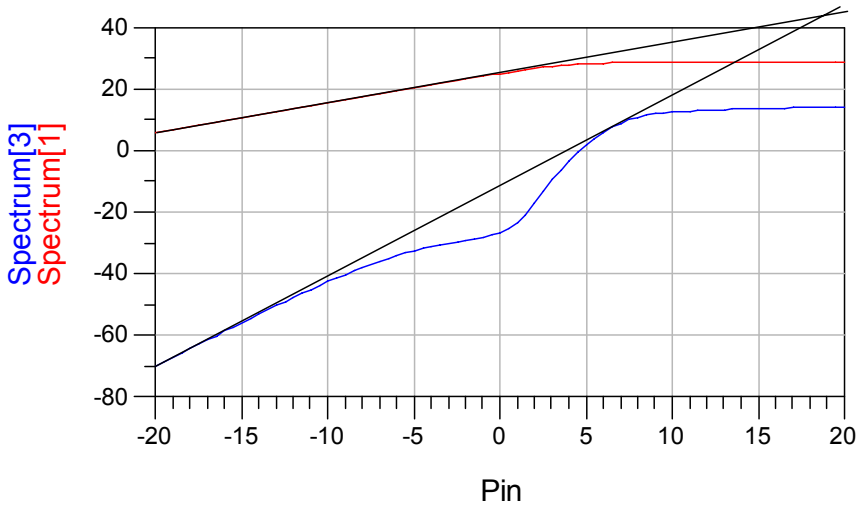


Fig. 4.16 IP3 of pre-layout simulation

The layout has to be modified after post layout simulation.

4.4 Post-layout simulation

The critical DC power line generates parasitic resistance. To prevent loss, the line has to be widened. After modify the layout simulate the circuit again and find the best layout topology.

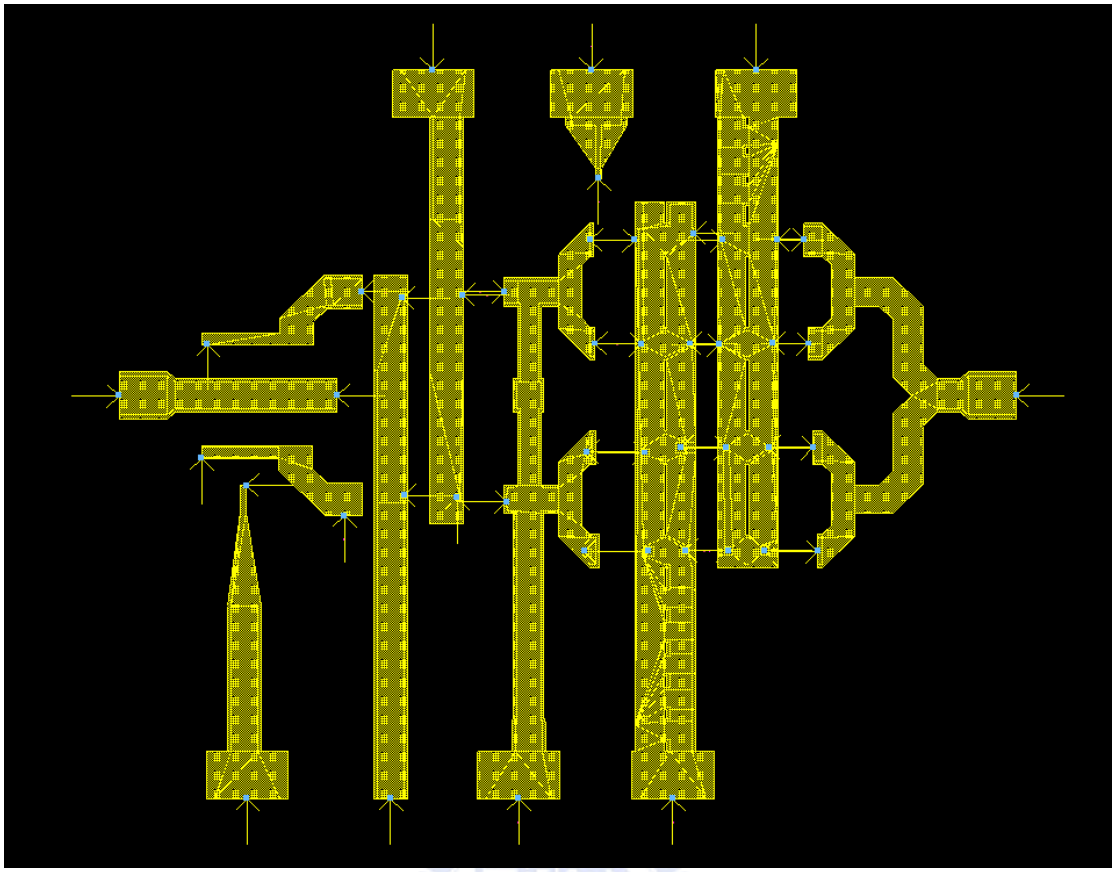


Fig. 4.17 Export the line of layout to momentum ADS system and simulation

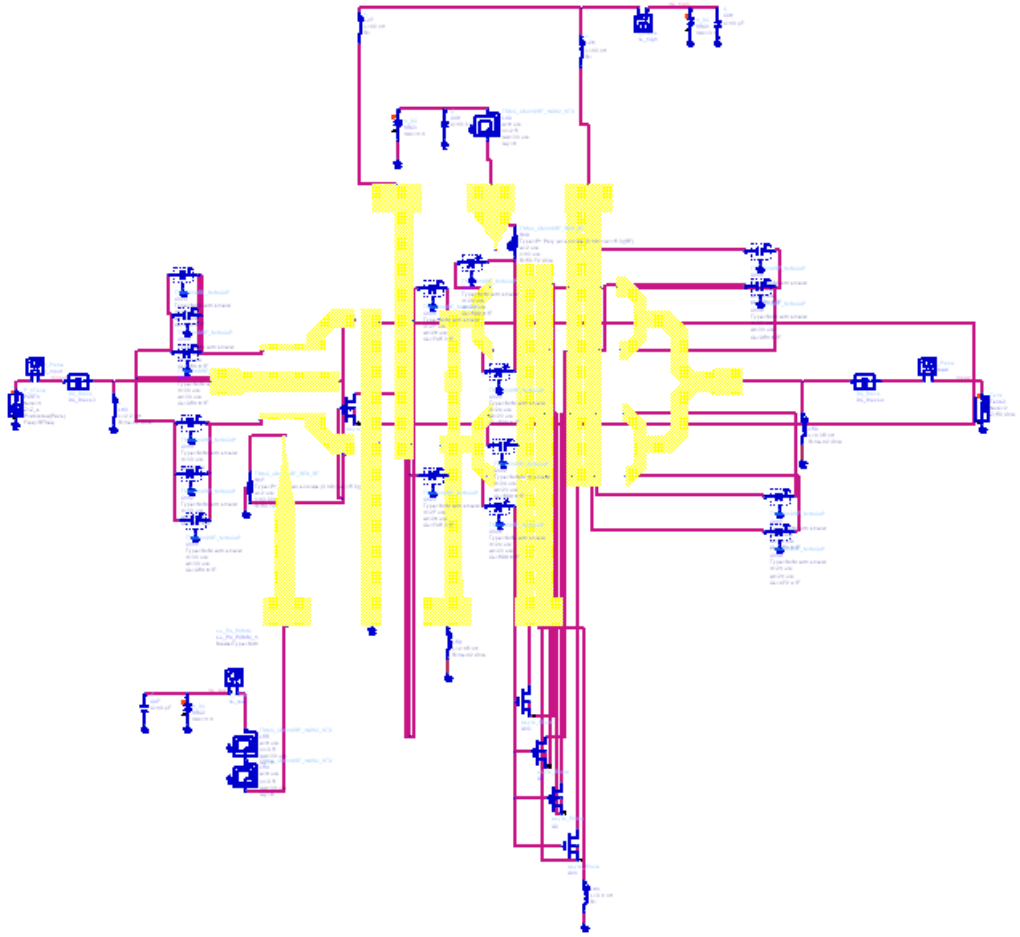


Fig. 4.18 Post-layout simulation with line calculation

Modify the layout with better simulation result. Then determinate the best layout topology and tape out. With the simulation, the final layout is shown in Fig.4.19.

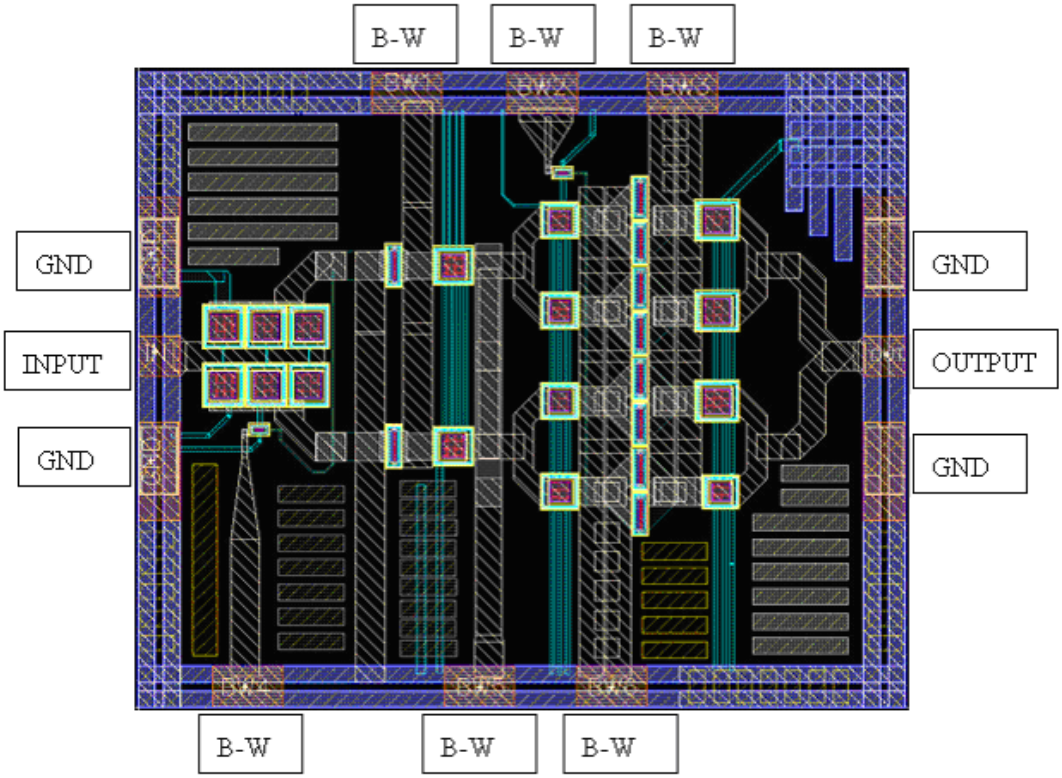


Fig. 4.19 The layout after post-layout simulation

The post-layout simulation results are shown as follow.

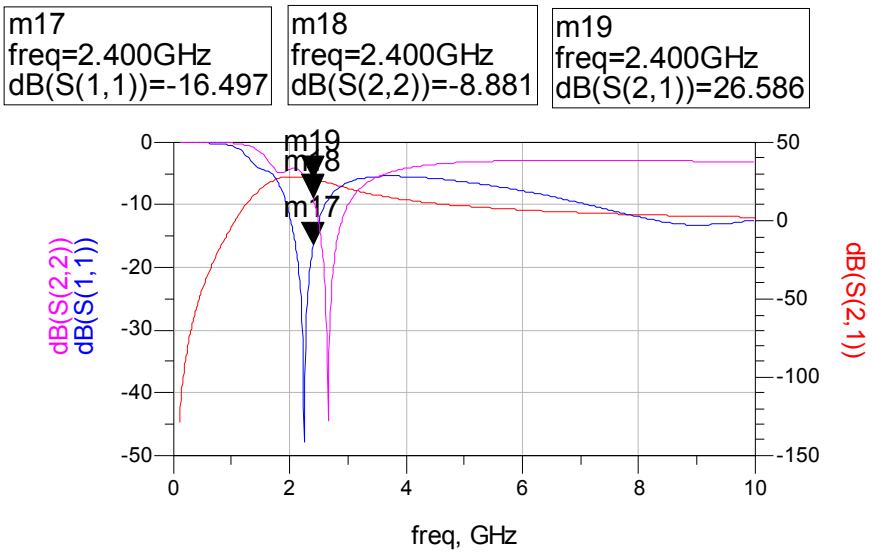


Fig. 4.20 S-parameter of post-layout simulation

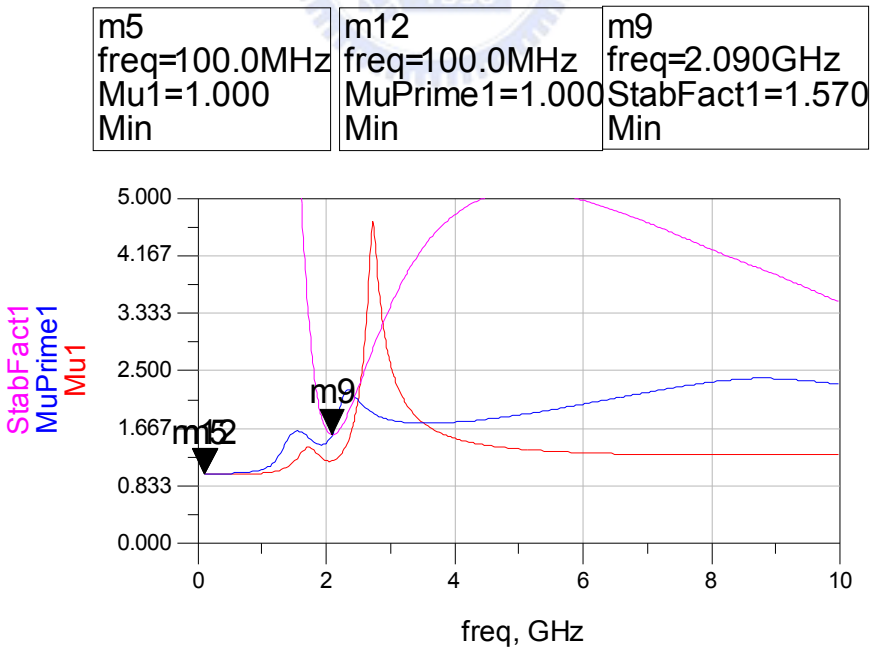


Fig. 4.21 Stability factor of post-layout simulation

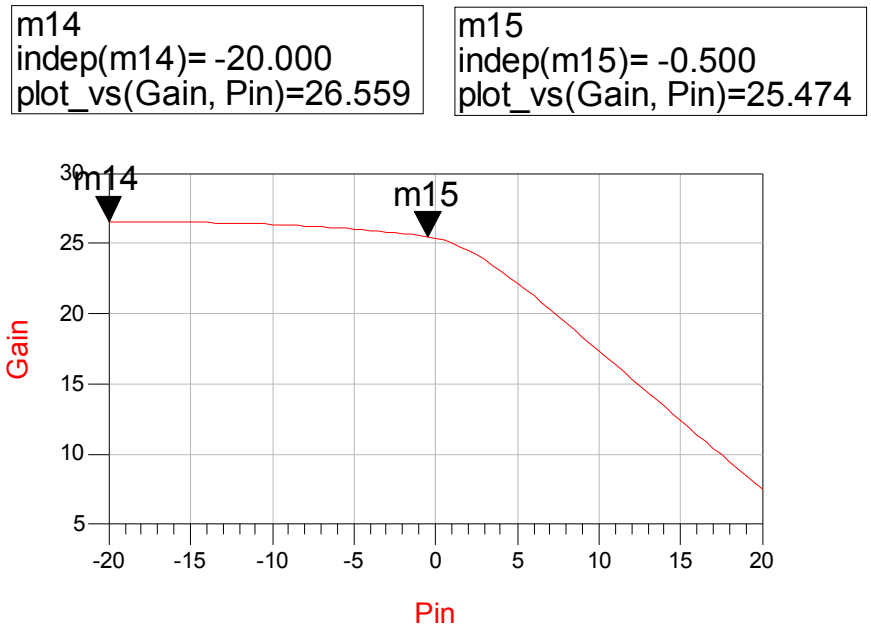


Fig. 4.22 Power gain of post-layout simulation

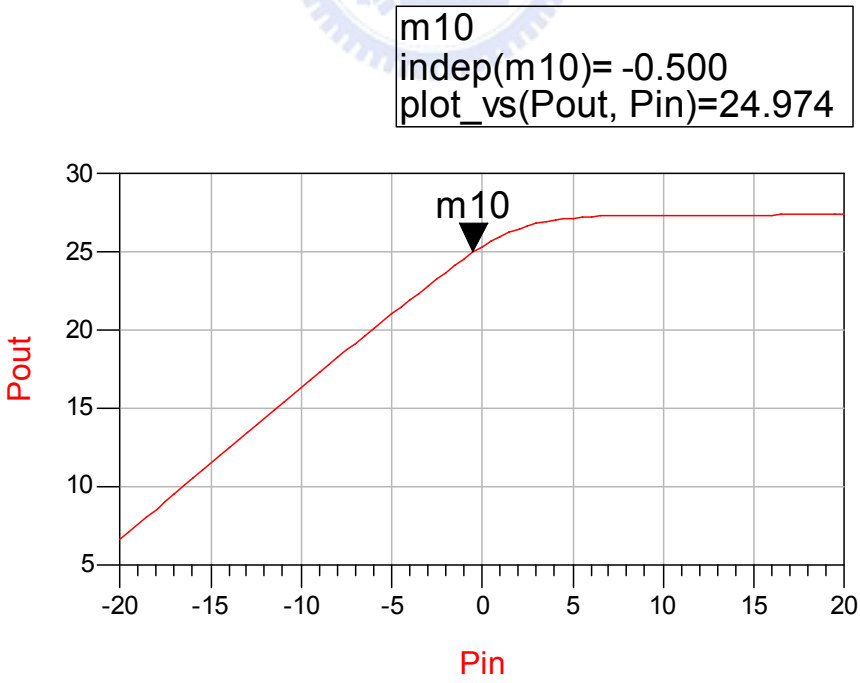


Fig. 4.23 Output power of post-layout simulation

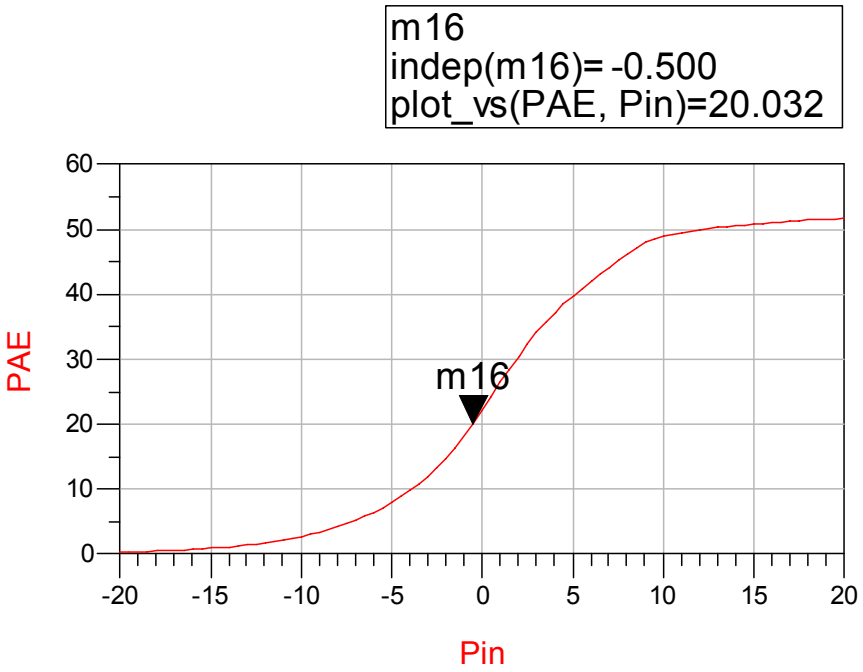


Fig. 4.24 Power Added Efficiency of post-layout simulation

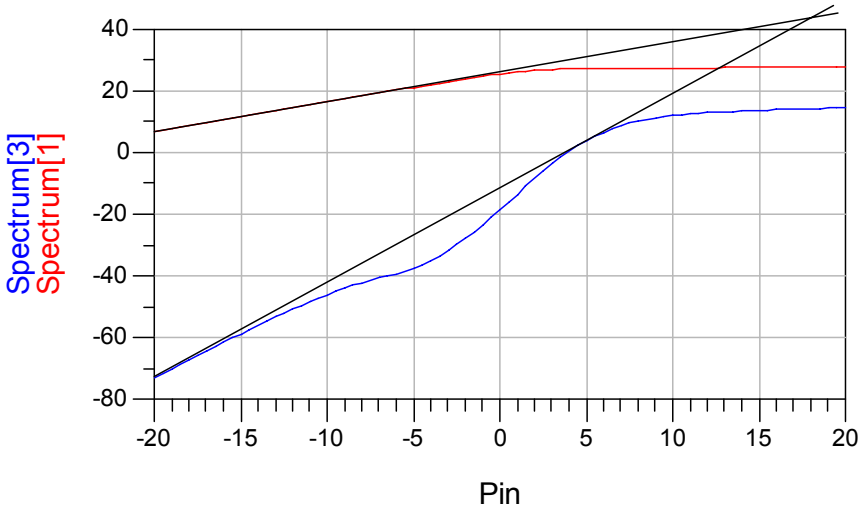


Fig. 4.25 IP3 of post-layout simulation

Summary of post-layout simulation is shown in Table 4.2.

S11	-16.5dB
Power gain	26.5dB
Output P1dB	24.9dBm
PAE @ P1dB	20%
OIP3	>40dBm

Table 4.2 The result of power amplifier

From Table 4.2, we can see the result is up to specification.

4.5 Measurement

For this work, the inductor of matching network is off chip. But there are some mistakes on design, so the chip is not work. The photograph of the chip is shown in Fig. 4.26.

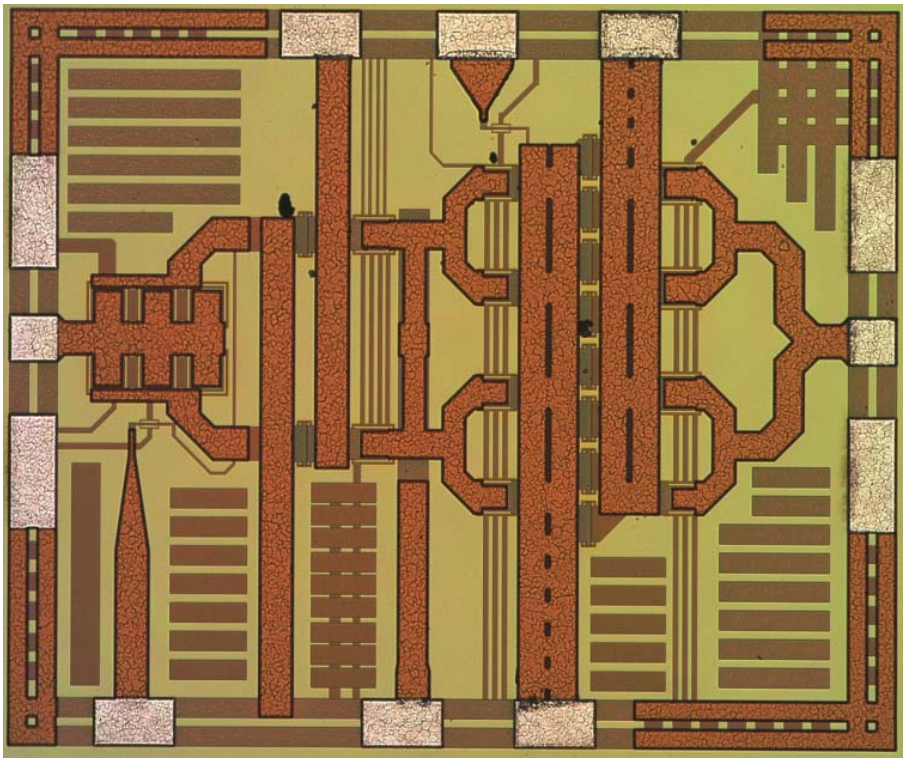


Fig. 4.26 The photograph of the chip

Chapter 5
Conclusion

We have designed an asymmetric-LDD MOS transistor which has twice drain breakdown voltage to the conventional one. Besides, the power amplifier has been designed by single ended and fabricated by TSMC 0.18 μm 1P6M process without any process modification.

According to simulation, this power amplifier can achieve 26.5dB power gain, 24.9dBm output P1dB, and 20% PAE at P1dB.

This research demonstrated that the asymmetric-LDD MOS transistor successfully implemented on a CMOS power amplifier with wonderful performance. This design method has great opportunity to be future trend.

Reference

[1] M.C. King, T. Chang, A. Chin, “RF power performance of asymmetric-LDD MOS transistor for RF-CMOS SOC design”, IEEE Microwave and Wireless Components Letters, vol. 17, no. 6, pp. 445–447, June 2007.

[2] J.F. Chen, J. Tao, P. Fang, C. Hu, “0.35- m asymmetric and symmetric LDD device comparison using a reliability/speed/power methodology”, IEEE Electron Device Letters, vol. 19, no. 7, pp. 216-218, July 1998.

[3] A. Litwin, O. Bengtsson, J. Olsson, “Novel BiCMOS compatible, short channel LDMOS technology for medium voltage RF & power applications”, IEEE Symp, pp. 289-292, 2002.

[4] J.C. Guo, C.H. Huang, K.T. Chan, W.Y. Lien, C.M. Wu, Y.C. Sun, “0.13μm low voltage logic base RF CMOS technology with 115GHz ft and 80GHz fmax”, 33rd European Microwave Conference, pp. 682-686, 2003.

[5] G. Miller Managing, “TSMC announces 0.18-micron mixed signal and RF CMOS processes”, RF Globalnet

[6] K.-E. Ehwald, B. Heinemann, W. Roepke, W. Winkler, H. Rücker, F. Fuernhammer, D. Knoll, R. Barth, B. Hunger, H. E. Wulf, R. Pazirandeh, N. Ilkov, “High performance RF LDMOS transistors with 5nm gate oxide in a 0.25m SiGe:C BiCMOS technology”, IEDM Tech. Dig., pp. 40.4.1-40.4.4, 2001.

[7] C.-C. Yen, H.-R. Chuang, “A 0.25-μm 20-dBm 2.4-GHz CMOS power amplifier with an Integrated diode linearizer”, IEEE Microwave & Wireless Components Letter, vol. 13, no. 2, pp. 45-47, 2003.

[8] V. Knopik, B. Martineau, D. Belot, “20 dBm CMOS class AB power amplifier design for low cost 2GHz-2.45GHz consumer applications in a 0.13μm technology”, Proc. IEEE Int. Symp. Circuits and Systems, Kobe, Japan, vol. 3, pp. 2675-2678, May 2005.

[9] C. Lu, A.-V. H. Pham, M. Shaw, C. Saint, “Linearization of CMOS broadband power amplifiers through combined multi-gated transistors and capacitance compensation”, IEEE Transaction on Microwave Theory and Techniques, pp. 2320-2328, November 2007.

[10] Y. Eo, K. Lee, “A 2.4GHz/5.2GHz CMOS power amplifier for dual-band applications”, IEEE MTT-S Int. Microwave Symp. Dig, Fort Worth, TX, vol. 3, pp. 1539-1542, June 2004.

[11] P. Haldi, D. Chowdhury, G. Liu, A. M. Niknejad , “A 5.8GHz linear power amplifier in a standard 90nm CMOS process using a 1V power supply”, IEEE Radio Frequency Integrated Circuits Symp, pp. 431-434, 2007.

[12] Y. Eo, K. Lee, “High efficiency 5GHz CMOS power amplifier with adaptive bias control circuit”, IEEE RFIC Symp. Dig, Fort Worth, TX, pp. 575-578, June 2004.

[13] E. Chen, D. Heo, M. Hamai, J. Laskar, D. Bien, “0.24-um CMOS technology for bluetooth power applications”, Proc. IEEE Radio and Wireless Conference, pp. 163-166, 2000.

[14] G. Krieger, R. Sikora, P. Cuevas, M. Misheloff, “Moderately doped NMOS (M-LDD)—hot electron and current drive optimization”, IEEE Trans. Electron Devices, vol. 38, pp. 121, January 1991.

[15] T.H. Lee, H. Samawati, H.R. Rategh, “5-GHz CMOS wireless LANs”, IEEE Transaction Microwave Theory and Technique, vol. 50, pp. 268-280, 2002.

[16] T. Sowlati, D. Leenaerts, “A 2.4GHz 0.18um CMOS self-biased cascode power amplifier with 23dBm output power”, ISSCC Advanced RF Techniques, session 17, February 2002.

[17] Thomas H. Lee, The design of CMOS radio-frequency integrated circuit, Cambridge University Press, 2000.

[18] D.M. Pozar, Microwave engineering, Addison-Wesley, 1990.

[19] Behzad Razavi, RF microelectronics, Prentice-Hall, Inc., 1998.

[20] S.C. Cripps, RF power amplifiers for wireless communications, Norwood, MA: Artech House, 1999.