國　立　交　通　大　學

電子工程學系　　電子研究所碩士班

碩 士 論 文

用於植入式癲癇元件之低功率十位元每秒五十萬次取樣逐次漸進式類比數位轉換器

A Low Power 10-Bit 500-KS/s Successive Approximation Analog-to-Digital Converter for Implantable Epilepsy Devices

研 究 生：　陳韋丞

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中華民國九十九年十二月

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摘要

由於先進的積體電路科技，讓醫療器材的微小化得以實現。植入式生醫元件已發展用來治療一些神經疾病。

本論文提出一個用於植入式癲癇元件之低功率十位元每秒五十萬次取樣逐次漸進式類比數位轉換器。用於植入式生醫元件之電路，需考慮到功率消耗的問題。晶片如果產生過多的熱，會導致人體組織溫度上升，並造成危險。因此，低功率為植入式生醫元件的設計重點之一。類比數位轉換器為植入式生醫元件中主要功率消耗的電路之一，如何壓低其功率消耗更為重要。首先，選擇逐次漸進式類比數位轉換器應用於植入式癲癇元件。逐次漸進式類比數位轉換器為最常應用於中等解析度、中等採樣速度之架構。在論文中提出一個有效率的電容陣列可以大幅減少功率消耗。首先，串聯二進位加權式的電容陣列，可以省下百分之五十的切換能量。再來，使用較有效率的切換方法更進一步省下功率消耗。所提出的電容陣列與傳統二進位加權式的電容陣列相比只需要原本功率消耗的百分之四十，並且保持相同的電容誤差表現。

量測結果則為 85 μW 的功率消耗，44.1 dB 的訊號對雜訊諧波比，以及 7.03 的有效位元數。

A Low Power 10-bit 500-KS/s Successive Approximation Analog-to-Digital Converter for Implantable Epilepsy Devices

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Abstract

Because of the advanced IC technology, the microminiaturization of biomedical devices has been achieved. Implantable biomedical devices are used to cure some neural disease.

This paper presents a 1.8V, 10-bit 500-kS/s low power successive approximation (SAR) analog-to-digital converter (ADC) for implantable epilepsy devices in TSMC 0.18μm 1P6M CMOS process. In order to achieve low power design, an efficient capacitor array is proposed to significantly reduce power consumption. First, a binary weighted capacitor array is cascoded to reduce 50% switching energy. Then, part of the junction-splitting switching method is applied to further reduce power dissipation. The proposed capacitor array only consumes 40 % power dissipation of a conventional binary weighted capacitor array, and has the same capacitance mismatch performance.

Measurement results of the proposed SAR ADC show that the total power consumption is 85 μW, the signal-to-noise-distortion ratio (SNDR) of 44.1 dB, and the effective-number-of-bits (ENOB) is 7.03.

誌謝

大學加上研究所，已經在新竹待了七年多。從高中畢業生，到現在即將結束學生生涯，邁入人生的下一個階段，中間接受了許多人的幫助。感謝吳重雨校長多年來的指導與照顧，雖然校務繁忙，但對研究的熱情絲毫不減。感謝研究群的楊文嘉學長、黃祖德學長、蘇烜毅學長、蔡夙勇學長、陳煒明學長、劉麗珍學姊在平時給予的指教，讓我的研究能順利進行。更感謝蔡宗昀、周敬程、周順天、蘇凱悌、陳育祥、賴炯為、許世昕、李彥緯、林彥良、許哲綸、蔡佳琪、溫詠儒、廖勝暉、張家綾的陪伴，他們的活力給了我平時生活很大的調劑。

最後感謝父母的栽培養育，才能有今日的我。

陳韋丞

國立交通大學

中華民國九十九年十二月

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Chapter 1
Introduction

1.1 Background

1.1.1 Implantable biomedical devices

In the past tens of years, the development of the IC industry was marvelous, and now it is still rapid growing. Because of the advanced development of the IC industry, many devices, which were fixed at certain places before, can be easily carried by people now, such as phones, computers, media players, etc. Those influential products enrich modern people's daily life, and it's the time to go deep into people's health care. The mobile applications for business and entertainment are mature now, but there are rare mobile medical devices at the market. After taking care of people's work and happiness, people's health care becomes the latest focus of the IC industry.

Because of better medical care, the longevity of people is extended in developed countries. On the other hand, the expense of bringing up a child in developed countries is more expensive, so the birth rate is gradually declined. Therefore, the health care for elder people will become a major issue in aging societies. A lack of manpower to care elder people is an inevitable problem in the coming future. Fortunately, the advanced IC technology may solve this important problem.

Traditional medical devices equipped in hospitals are cumbersome and fixed at certain places. That makes patients inconvenient to walk around, and people can

only receive treatment in hospital beds. For some patients who need to receive long-time observation, it is inconvenient and unnecessary to go to hospital frequently. Therefore, an implantable medical device for long-time observation is necessary for better health care, and medical staff can be released to serve serious patients. Because of the advanced IC technology, the microminiaturization of some medical devices has been achieved.

An implantable biomedical device is composed of many functional blocks, such as pre-amplifiers, analog-to-digital converters, and digital signal processors. Analog-to-digital converters (ADCs) are ubiquitous blocks that are used in almost all electronic systems to convert physical analog signals to digital data. Often, an ADC is accompanied with a digital signal processor (DSP) to further process and manipulate data in the digital domain. Current trends are to implement as much as the signal processing as possible in the digital domain.

In general, the signal process is preferred to be done with digital approaches than analog ones. Because digital signal processor (DSP) has large noise margin and is insensitive to circuit imperfection. Furthermore, powerful DSP is able to perform complex algorithms or execute programs. The natural signals are continuous-time analog, so an analog-to-digital converter (ADC) is essential. The quality of the digital signals depends on the ADC performance.

1.1.2 ADC Architectures

An advancement of portable biomedical devices has pushed integrated circuits towards very low power consumption in order to extend operation time of battery. To guarantee long-life operation, it is important that the system should have low

power consumption.

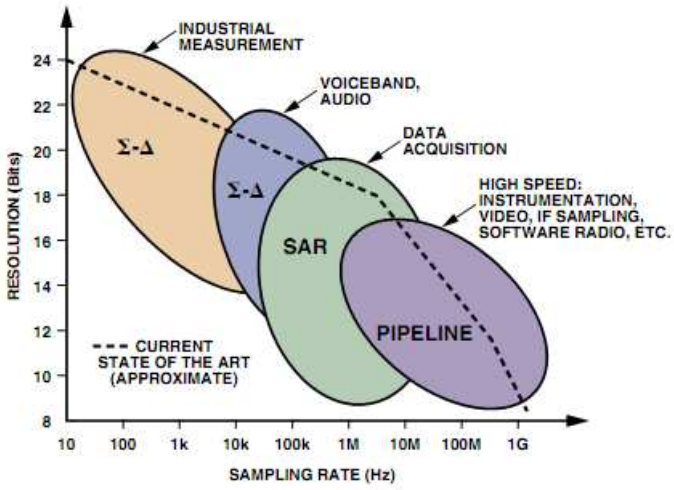


Figure 1 ADC architectures, applications, resolution, and sampling rates.

The classification in Figure 1 [1] shows in a general way how these application segments and the associated typical architectures relate to ADC resolution (vertical axis) and sampling rate (horizontal axis). The dashed lines represent the approximate state of the art in mid-2005. Even though the various architectures have specifications with a good deal of overlap, the applications themselves are key to choosing the specific architecture required.

In the past few years, more and more applications are built with very stringent requirements on power consumption. For electronic systems, such as wireless systems or implantable devices, the power consumption is becoming one of the most critical factors. The stringent requirements on the energy consumption increase the need for the development of low voltage and low power circuit techniques and system building blocks. Analog-to-digital Converters (ADCs) translate the analog quantities into digital language, used in information processing, computing, data transmission and control systems. ADCs are key components for

the design of power limited systems, in order to keep the power consumption as low as possible.

Among the important trade-offs in an ADC, is that of between speed and accuracy. The choice of ADC architectures depends on the application and the requirements of the overall system. In addition, each architecture has its own limitation on different performance criteria, such as speed, power, and area. Nowadays, power consumption is one of the important design specifications in almost all applications. A good understanding of the fundamental limits of ADCs is necessary to achieve an ultra-low-power design. These fundamentals are overviewed in this section.

In order to select the right type of the desired converter, a careful analysis of various classes of converters has been conducted. In practical terms, ADCs can be divided into sigma-delta and Nyquist-rate converters. Among Nyquist-rate converters, flash, pipeline, and SAR architectures are popular.

- **Sigma-Delta ADC**

Figure 2 shows the two major building blocks of a sigma-delta converter are the analog modulator and the digital decimation filter. A sigma-delta ADC contains very simple analog electronics (a comparator, voltage reference, a switch and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. Sigma-delta converters trade speed for resolution. They need to sample many times (at least 16 times and often more) to produce one final sample dictates that the internal analog components in the sigma-delta modulator operate much faster than the final data rate. The digital decimation filter is also a challenge to design and generally consumes a larger silicon area than a simple output decoder. Sigma-delta ADCs are preferred for

the highest levels of bit resolution and demand very fast oversampling clocks making them inherently low-speed converters. The clock generator has a direct influence on the signal-to-noise ratio, but the strict requirement for the clean clock generator makes sigma-delta ADCs not suitable for low-power applications.

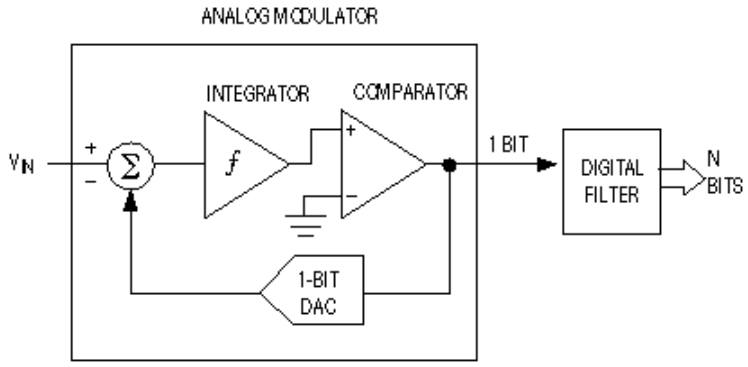


Figure 2 The two major building blocks of a sigma-delta converter are the analog modulator and the digital decimation filter.

- **Flash ADC**

Flash ADC, which is shown in Figure 3, sometimes called parallel ADC, is the fastest type of converter, but has limited resolution, high power dissipation and relatively large chip size. The main reason for the high power consumption is the large number of comparators. For an N-bit converter, we would need (2^N-1) comparators, this means that the number of comparators increases exponentially with the number of bits. The comparator is one of the most power hungry components in ADC. Focusing the attention on limit the power dissipation, different topologies that decrease the number of comparators needed, or avoid that block, should be taken in consideration.

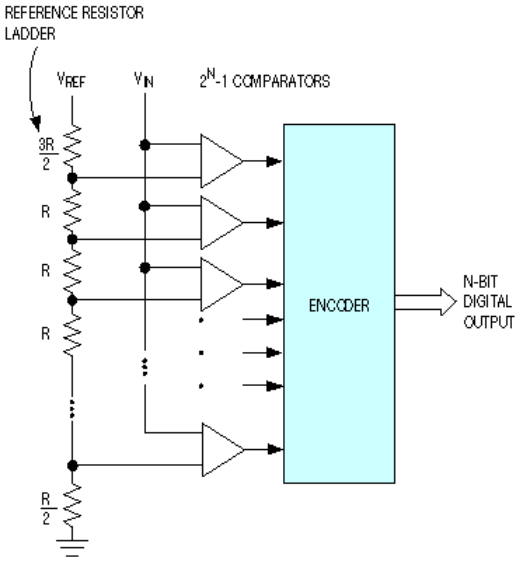


Figure 3 Flash ADCs include 2^{N-1} comparator banks and a reference resistor-divider network

- **Pipeline ADC**

An approach to breaking the exponential dependence of the number of comparators on resolution is the use of a pipeline ADC. Instead of fully parallel comparison, it divides the conversion into several comparison stages. Therefore, the total number of comparators is greatly reduced, only N comparators required for a 1-bit per stage, N-bit pipeline ADC. However, for the pipelined structure inter-stage residue amplification is needed which consumes considerable power and limits high speed operation. While it is possible to make use of open-loop residue amplification, an extra calibration loop is needed, increasing overall complexity and power consumption. Figure 4 shows the pipelined ADC with four 3-bit stages (each stage resolves two bits)

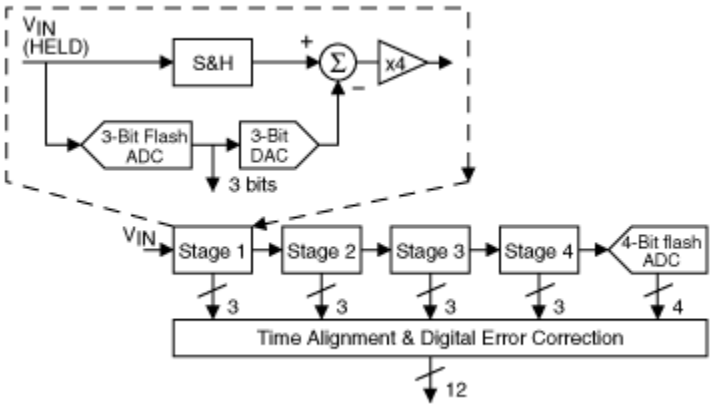


Figure 4 The pipelined ADC with four 3-bit stages (each stage resolves two bits)

- **SAR ADC**

Figure 5 shows typical successive-approximation ADCs consist of a single DAC, a comparator, and a successive-approximation register (SAR), plus a clock and logic control. For low conversion speed, an SAR approach is often used since it also divides a full conversion into several comparison stages in a way similar to the pipeline ADC, except the algorithm is executed sequentially rather than in parallel as in the pipeline case. An N-bit SAR converter utilizes only one comparator with N clock cycles to complete a full conversion. Thus, the total power consumption is normalized to approximately one, while speed is now 1/N. Since the ratio of power and speed represents the energy consumption per conversion sample, SAR converters clearly have a power efficiency advantage over the other approaches. Due to the fact that the power efficiency difference between SAR and flash topologies increases exponentially with the number of bits, N, a SAR converter provides a promising starting point of the successive approximation algorithm has traditionally been a limitation in achieving

high-speed operation.

After careful consideration, SAR ADCs are selected as the preferred converters for biomedical applications because of moderate resolution and moderate speed. Flash converters are simple and used for very high-speed applications. However, the resolution of flash converters is too low to be used in biomedical devices. On the other hand, the higher resolution than flash converters could be achieved by applying the pipeline architecture, but pipeline converters is slower than flash converters. Above two kinds of Nyquist-rate converters are not suitable for the biomedical applications because the operating sampling frequencies are much higher than the medical applications needed. The higher frequency converters are operated at, the more power they consume.

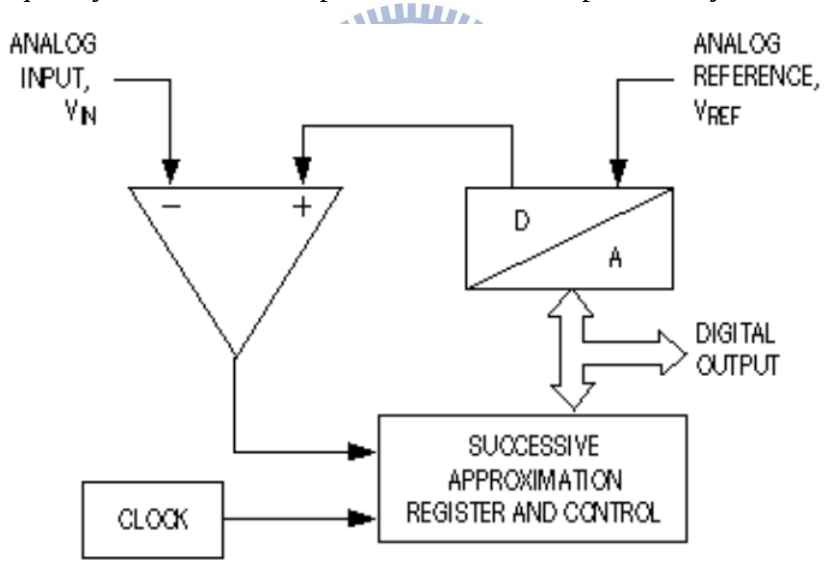


Figure 5 Typical successive-approximation ADCs consist of a single DAC, a comparator, and a successive-approximation register (SAR), plus a clock and logic control.

1.1.3 SAR Architectures

The ADC block is a large part of overall power consumption in the biomedical application, therefore the low power consumption ADC is required. SAR ADCs are the most widely used for low energy application due to its minimum analog blocks.

In SAR analog-to-digital converters, a large amount of power dissipated in switching the capacitor array. For this reason, several DAC topologies have been implemented in order to reduce the switching energy.

- **Binary weighted capacitor array DAC**

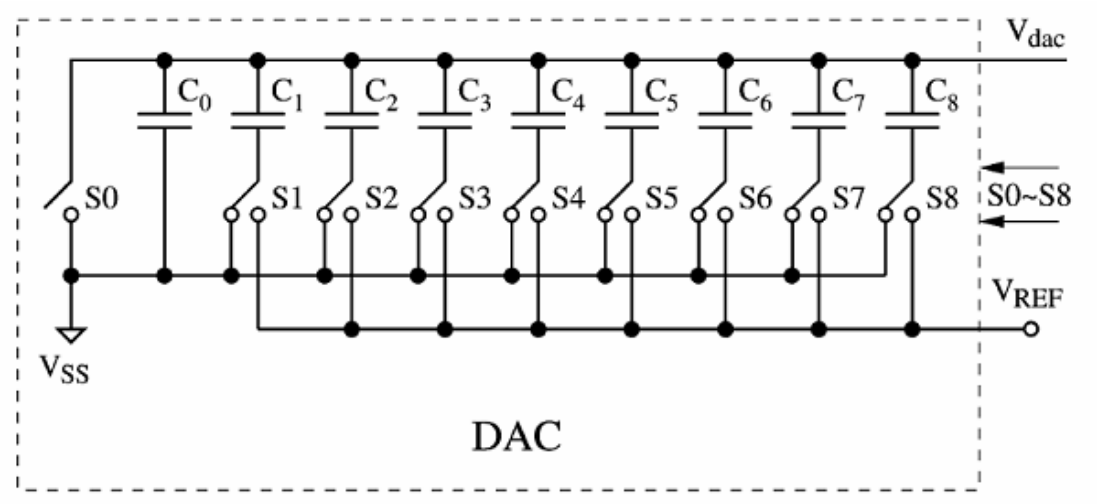


Figure 6 Single ended binary weighted switched capacitor array DAC

This DAC [4][5][6] (Figure 6) is an array of binary weighted capacitors plus one additional capacitor of weight corresponding to the last significant bit (LSB), and switches that connect the capacitor bottom plates to two different voltages: $\mathbf{V}_{REF}$, and ground.

- **Junction-Splitting Capacitor Array**

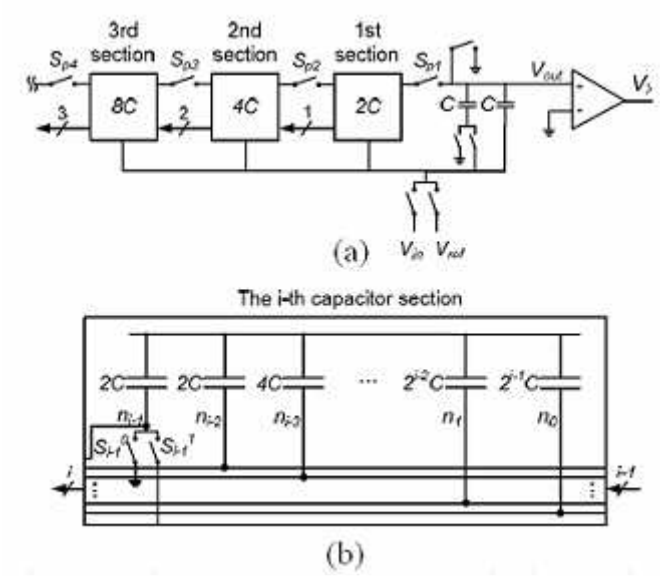


Figure 7 (a) SAR ADC using J-S capacitor array. (b) the ith sub-capacitor section of the J-S capacitor array

The J-S capacitor array [7] (Figure 7) consists of a number of serially connected sections each of which is composed of splitting capacitor. The desired $\mathbf{V}_{OUT}$ is created by appending a sub-capacitor section to the previous capacitor array.

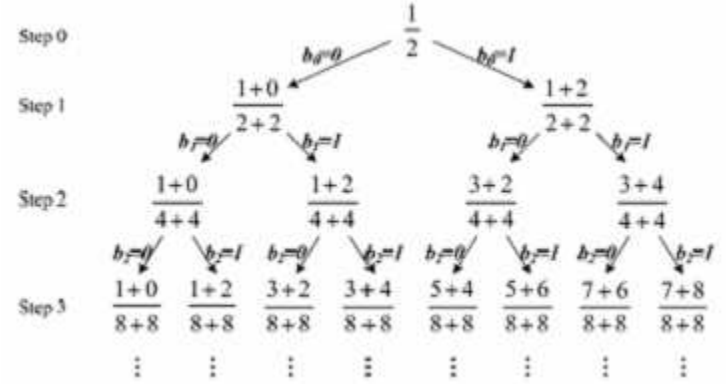


Figure 8 How to make the desired capacitance ratio for the J-S capacitor array

In Figure 8, the denominator and numerator represents $\mathbf{C}_{TOT}$ and $\mathbf{C}_{H}$, respectively, can be seen that $\mathbf{C}_{TOT}$ is not constant, it increases during the

conversion process. First, the MSB, b0, is determined by comparing the input voltage with a half reference voltage. The half reference voltage is achieved by using the two smallest capacitors, one connected to the ground and the other connected to the reference voltage. Then, the next voltage to be compared is made by connecting a sub-capacitor section, one at a time.

- **Energy Efficient Charge-Redistribution DAC**

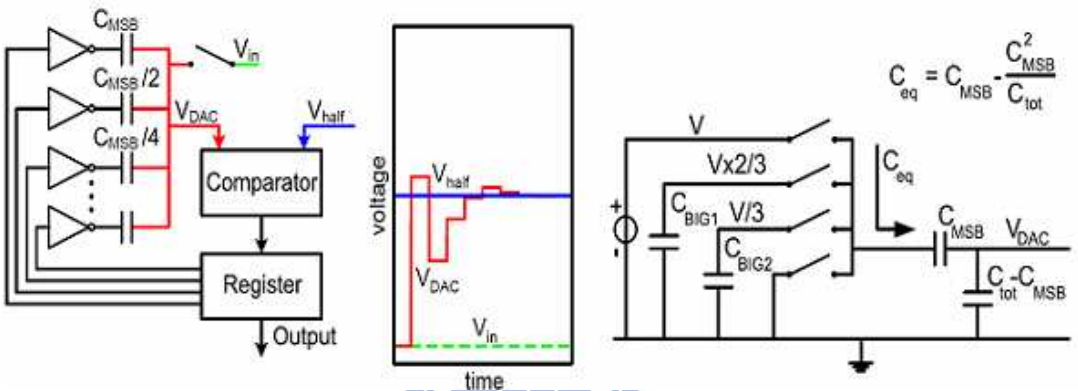


Figure 9 Energy efficient charge redistribution DAC for SAR application.

In energy efficient charge redistribution DAC, [9], first, we reset to a state where the MSB is high and all other bits are low. Next, $\mathbf{V}_{in}$ is sampled onto output $\mathbf{V}_{DAC}$. In a single-ended ADC, VDAC is compared to $\mathbf{V}_{half}$. The comparator decides if the MSB should remain high or set low during the remainder of the conversion. Next, MSB-1 is set to high and the procedure is repeated, until N comparisons have been done for N bits. The difference with respect to the traditional charge redistribution DAC is that the voltage over $\mathbf{C}_{eq}$ is charged from 0 to V in n steps of $\frac{V}{n}$.

1.2 Motivation

As the biomedical technology and IC processing technology grow rapidly, it is

possible to realize a neural recording system on a single chip instead of the conventional one composed of many discrete components, which leads to large power consumption with extra costs. Furthermore, to reduce the patients' discomfort for long-term monitoring, it is encouraged to develop a small-size, light-weight, and implantable system.

Now, we are trying to develop an implantable Epilepsy detection and stimulation system. The system block diagram is shown in Fig 10.

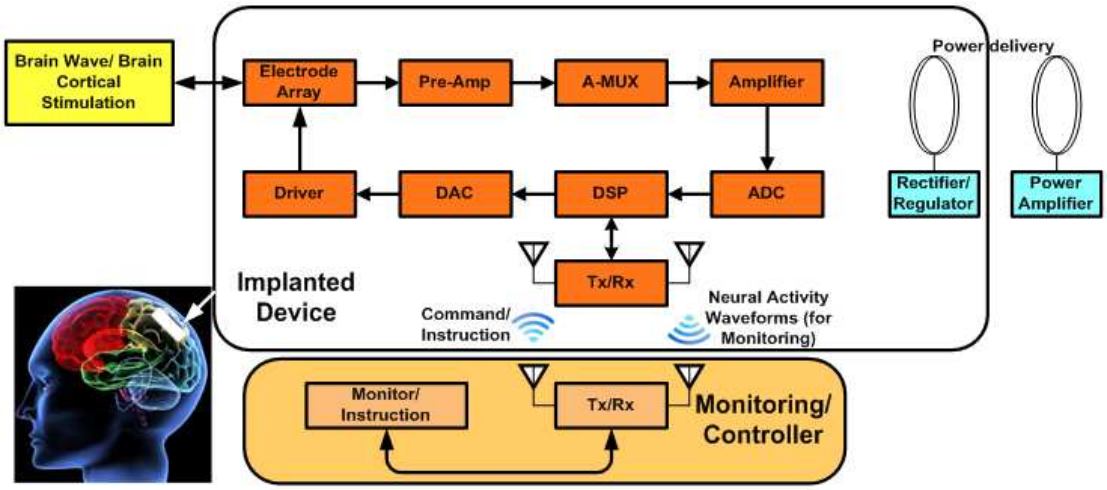


Figure 10 An implantable Epilepsy detection and stimulation system

Target specifications of the ADC block are decided by the bio-signal bandwidth. According to the demand from doctors, they want to observe the bio-signal between 0.1 Hz ~ 7 KHz. Figure 1-8 shows 8 one ADC for 8 preamplifiers under the consideration of area size. Finally, the specification of the ADC is shown in Table 1-1.

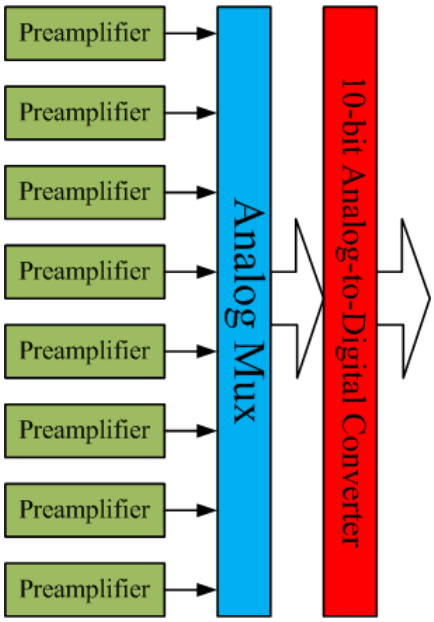


Figure 11 One ADC for 8 preamps

Target Specifications	
Technology	**TSMC 0.18 μm**
Resolution	**10**
Sampling Rate(S/s)	**500 K**
Input Range	**0~1.8 V**
Differential Nonlinearity	**<0.5**
Integral Nonlinearity	**<1**
SNDR@DC	**>55.94**
ENOB@DC	**>9**

Table I Target specifications of the ADC

1.3 Main Results and Thesis Organization

1.3.1 Main Results

A low power 10-bit 500-kS/s SAR ADC for implantable epilepsy devices is designed and measured. In order to achieve low power design, the power consumption of the capacitor array must be first considered. An new capacitor array is proposed to significantly reduce power consumption. First, a binary weighted capacitor array is cascoded to reduce 50% switching energy. A binary weighted capacitor array has good capacitance mismatch performance, but consumes a lot of power dissipation. Two same capacitors are cascoded to reduce total capacitance and power consumption. A cascoded binary weighted capacitor array also has better capacitance mismatch performance when using the same size of the unit capacitance. Then, part of the junction-split switching method is applied to further reduce power dissipation. The junction-split switching method is very efficient, but has problems of floating elements and capacitance mismatch. Part of this switching method is applied to take the benefit and avoid those problems

The proposed SAR ADC is simulated with low power consumption of 80 μW, SNDR of 59.26 dB, ENOB of 9.55. This design is implemented in TSMC 0.18-μm CMOS process.Measurement results of the fabricated SAR ADC perform low power consumption of 85 μW, SNDR of 44.10 dB, and ENOB of 7.03. The chip area is 1 mm^2. Modified simulation results perform low power consumption of 83 μW, SNDR of 57.53 dB, and ENOB of 9.26.

1.3.2 Thesis Organization

This thesis is divided into four chapters. Chapter 1 introduces the background and the motivation of this research. The proposed SAR converter will be presented in Chapter 2. Design consideration of the converter is discussed in Section 2.1. Then the design procedure is presented in Section 2.2. Post-simulation results are shown in Section 2.3. The experimental results will be shown in Chapter 3. Finally, the conclusions and future work will be presented in Chapter 4.

Chapter 2
Circuit Design and Simulation Results

2.1 Design Consideration

The successive approximation (SAR) analog-to-digital converter (ADC) has recently been widely used for moderate-speed moderate-resolution applications where the power consumption is of major concern. The major advantage of SAR ADC is simple and low power because the SAR ADC does not need operational amplifiers.

Two major design issues, which decide the performance of SAR ADCs, should be thought over to achieve a good and robust design. First, a suitable unit capacitance size for the capacitor array is chosen to reduce the thermal noise and capacitance mismatch. The accuracy of SAR ADCs is significantly influenced by these two factors. However, when SAR ADCs are used for high resolution applications, the unit capacitance size is determined by capacitor mismatch. The thermal noise is small enough to neglect.

The other major design issue is the efficiency of switching methods for the capacitor array. For high-resolution applications, the switching energy dominates the total power consumption of the SAR ADC. Many efficient switching methods are developed to reduce the switching energy. The switching energy is significantly decreased by those methods.

2.2 Circuit Design

2.2.1 A Conventional SAR ADC

A conventional binary weighted SAR converter is shown in Fig 12. A SAR converter is basically composed of three main parts. They are a capacitive digital-to-analog converter (DAC), a successive approximation register, and a comparator. A capacitive DAC and a successive approximation register produce an approximation of the input signal. A comparator is composed of preamps and a latch, and determines whether the approximation is too high or too low. The approximation is improved by knowing the result of the last comparison, and the process is repeated until the entire digital word is decoded. The algorithm is described below.

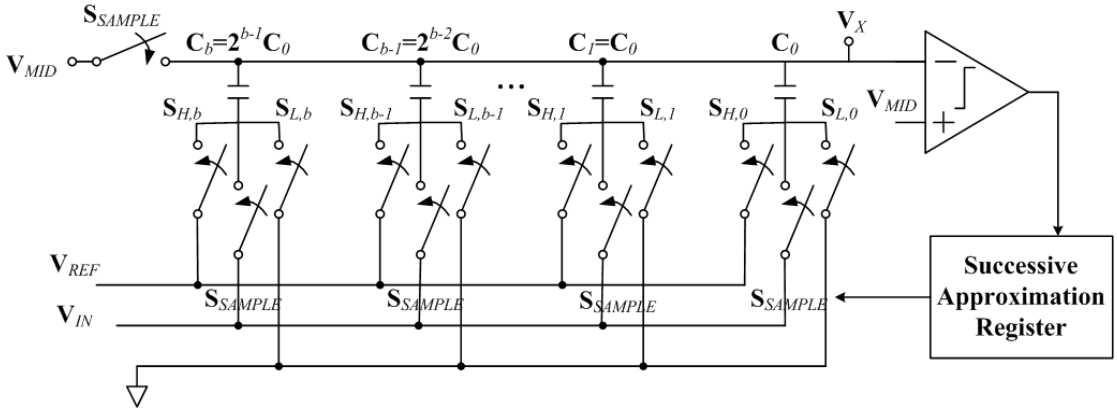


Figure 12 A conventional SAR ADC

In the sampling cycle, $\mathbf{S}_{SAMPLE}$ is high, and the entire capacitor array stores the voltage $\mathbf{V}_{MID}$ - $\mathbf{V}_{IN}$. At the end of sampling cycle, $\mathbf{S}_{SAMPLE}$ is reset to low. Then, the successive conversion cycles are coming. At the beginning of conversion, the MSB cap $\mathbf{C}_b$ is connected to $\mathbf{V}_{REF}$, causing $\mathbf{V}_X$ to settle to

$$\mathbf{V_x = V_{MID} - V_{IN} + \frac{V_{REF}}{2}} \quad \textbf{(1)}$$

And the latch output is

$$\mathbf{D_1} = \begin{cases} 1, & \mathbf{V_{IN}} > \dfrac{\mathbf{V_{REF}}}{2} \\ 0, & \mathbf{V_{IN}} < \dfrac{\mathbf{V_{REF}}}{2} \end{cases} \quad \textbf{(2)}$$

The latch output controls the next switch transition. If $\mathbf{D}_1$ is high, the second largest capacitor is connected to $\mathbf{V}_{REF}$ ($\mathbf{S}_{H,\,b-1}$ =1), raising the voltage at $\mathbf{V}_X$ (this action is called an "up" transition). On the other hand, if $\mathbf{D}_1$ is low, $\mathbf{C}_b$ is returned to ground and $\mathbf{C}_{b-1}$ is connected to $\mathbf{V}_{REF}$ (a "down" transition).

The above process is repeated for successive capacitors in the array. At each stage, the value of $\mathbf{V}_X$ is

$$\mathbf{V_X = V_{MID} - V_{IN} + \frac{C_T}{C_T + C_B} V_{REF}} \quad \textbf{(3)}$$

Where $\mathbf{C}_T$ is the sum of all capacitors connected to the reference voltage ($\mathbf{V}_{REF}$), and $\mathbf{C}_B$ is the sum of all capacitors connected to ground:

$$\mathbf{C_T = \sum_i 2^{i-1} C_0 \text{ for } i \text{ such that } S_{H,i} = 1} \quad \textbf{(4)}$$

$$\mathbf{C_B = \sum_i 2^{i-1} C_0 \text{ for } i \text{ such that } S_{H,i} = 0} \quad \textbf{(5)}$$

2.2.2 The Proposed SAR ADC

Figure 13 shows the architecture of the proposed SAR ADC. A new DAC is proposed to significantly reduce power consumption, and a better switching method [7] is applied to the DAC, too.

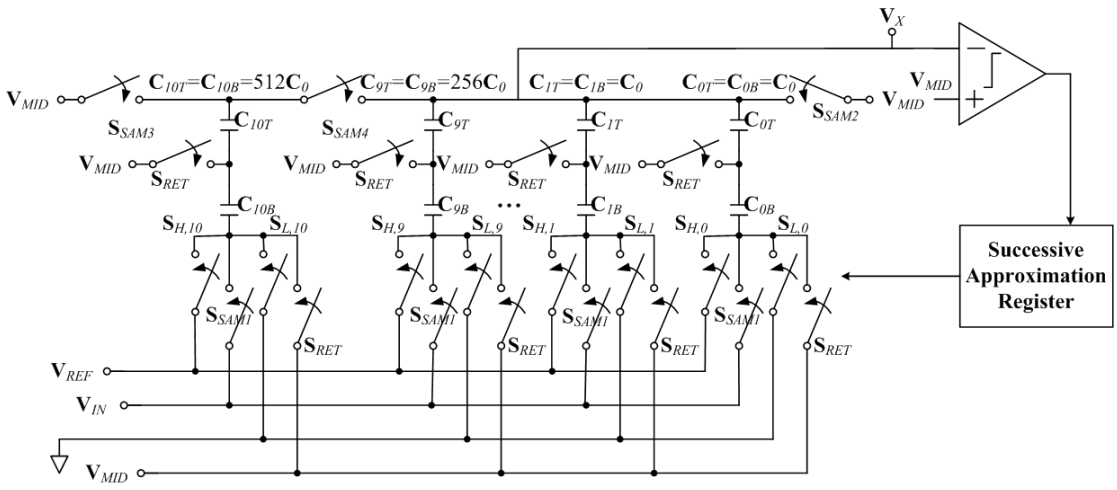


Figure 13 The proposed SAR ADC

The following sections will detailed describe the design of each block, including the DAC, the comparator, and the successive approximation register.

2.2.3 Digital-to-analog converter

The DAC is the most critical component of SAR ADCs, and should be considered carefully. First, the total area is dominated by the DAC composed of many capacitors. Then, although there is no static power consumption from the capacitor array during the operation, the transient power becomes more enormous because of requiring the higher accuracy and speed performance. The DAC consumes a major portion of the total power. Therefore, how to reduce the area and the power consumption of the DAC is the most popular research issue about SAR ADCs in recent years.

The unit capacitance size and the binary weighted capacitor ratio are the reasons that a conventional capacitor array occupies so much area. The thermal noise and the random mismatch between two adjacent capacitors resulting from

different technology decide the unit capacitance size. In most conditions, the effect caused by the thermal noise is too small compared with the last significant bit (LSB) voltage of ADCs so that it could be ignored. Without the effect of the thermal noise, the random mismatch between two adjacent capacitors is the only factor, which decides the unit capacitance size. In a few words, the higher accuracy the ADC requires, the larger size of the unit capacitance is.

A binary weighted capacitor array is the easiest way to implement a DAC, but it requires many different values of capacitors, which demands much area. For an N-bit capacitor array, the largest capacitor is $\mathbf{2}^{N-1}$ times larger than the unit capacitor. Although many non-binary weighted capacitor arrays are developed to reduce area and power consumption, they also make the accuracy performance worse. In short, this is an area / accuracy tradeoff. The most efficient way to reduce area is to implement a DAC by using the most advanced technology. The random mismatch between two adjacent capacitors could be improved by the newest technology.

The other design issue of a DAC is the power consumption. For a binary weighted capacitor array, the power consumption of an N+1 bit resolution capacitor array is 2 times more than an N bit resolution capacitor array. Therefore, for high-resolution applications, the power consumption of a DAC becomes enormous. However, a conventional switching method is very inefficient because many unnecessary switching steps waste considerable power. The operations of the “up” transition and the “down” transition are described in Fig 14. During the operation of the “up” transition, the value of $\mathbf{V}_X$ is lifted from 1/2 $\mathbf{V}_{REF}$ to 3/4 $\mathbf{V}_{REF}$, and no power is wasted. However, during the operation of the “down” transition, the value of $\mathbf{V}_X$ is first down to zero, and then lifted to 1/4 $\mathbf{V}_{REF}$. Obviously, there is much power wasted during the operation of the “down” transition because the

unnecessary charge / discharge actions. How to reuse the charge saved in the capacitor array is an efficient way to improve the switching method.

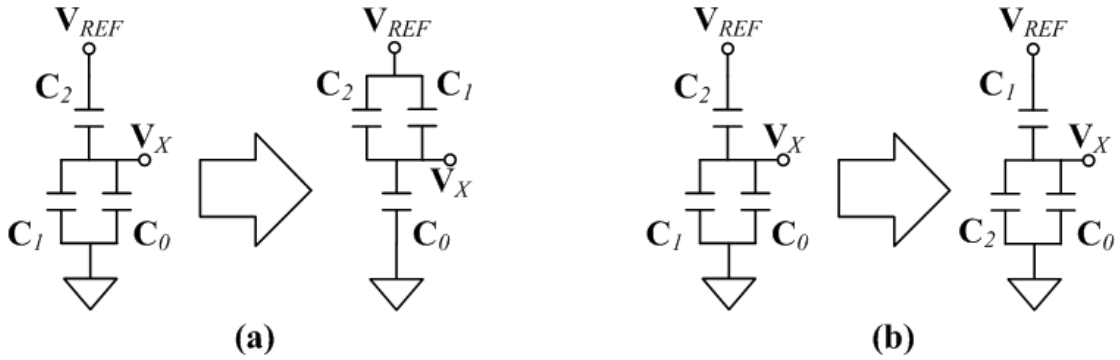


Figure 14 (a) the “up” transition (b) the “down” transition

A. A cascaded capacitor array

A binary-weighted capacitor array is chosen because of the capacitance mismatch performance, which decides the accuracy of the SAR converter. Instead of a conventional binary weighted capacitor array, a cascoded binary weighted capacitor array is used to have the same capacitance mismatch performance and consume less power dissipation. A cascaded capacitor array is shown in Figure 15.

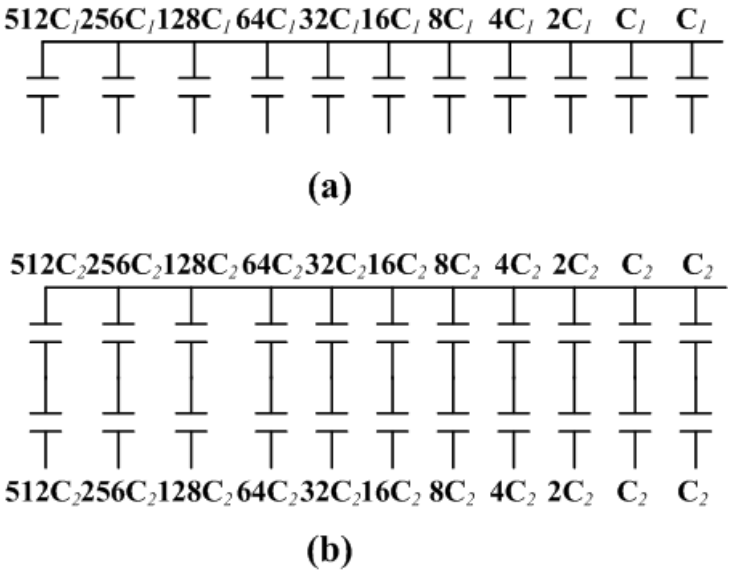


Figure 16 (a) a conventional capacitor array (b) a cascoded capacitor array

When catching sight of this architecture for the first time, the first impression is that a cascoded array occupies more area. However, the unit capacitance size of a cascoded capacitor array is different from a conventional binary weighted capacitor array.

In this design, the total capacitance is large enough to neglect the effect of the thermal noise. Therefore, the unit capacitance size is decided by the random mismatch between the two adjacent capacitors. The mismatch factor is given by the TSMC 0.18μm technology. The detailed Monte-Carlo analysis is performed to determine the value of the unit capacitance. Results of the analysis are shown in Table Ⅱ. From the results of the analysis, a smaller size of the unit capacitance for a cascoded capacitor array is needed to meet the same accuracy requirement. Ideally, the size of the unit capacitance for a cascoded array is half of the value for a conventional array. That is to say, no more area is required to apply this architecture. Because of the limitation of the technology, the size of the unit capacitance is chosen as 20 fF.

C_{unit} (μm×μm)	Mismatch (LSB)	
	Conventional Capacitor Array	Cascoded Capacitor Array
4×4	0.46	0.33
5×5	0.37	0.27
6×6	0.31	0.20
7×7	0.26	0.17
8×8	0.23	0.15
9×9	0.22	0.14
10×10	0.2	0.12

Table II The Monte-Carlo analysis of the random mismatch

A cascoded capacitor array only consumes half power consumption of a conventional capacitor array when using the same size of the unit capacitance.

B. Junction-Split switching method

In addition to applying a cascoded capacitor array, the method of the junction-split capacitor array is applied to the proposed capacitor array in order to further decrease power consumption. The switching transition of the junction-split capacitor array is shown in Figure 17. In case of output code 000, the J-S capacitor array consumes one seventh of the energy required in the conventional capacitor array. The switching energy consumed by a conventional capacitor array at each step is computed as follows, where $\mathbf{E}_0$, $\mathbf{E}_1$ and $\mathbf{E}_2$ represent the energy required to determine $\mathbf{D}_0$,$\mathbf{D}_1$, and $\mathbf{D}_2$.

$$\mathbf{E_0} = -\mathbf{V_{REF}}\mathbf{4C}(-\frac{\mathbf{1}}{\mathbf{2}}\mathbf{V_{REF}} - \mathbf{0}) = \mathbf{2CV_{REF}^2} \quad \textbf{(6)}$$

$$\mathbf{E_1} = -\mathbf{V_{REF}}\mathbf{2C}\left(-\frac{\mathbf{3}}{\mathbf{4}}\mathbf{V_{REF}} - \frac{\mathbf{1}}{\mathbf{2}}\mathbf{V_{REF}}\right) = \frac{\mathbf{5}}{\mathbf{2}}\mathbf{CV_{REF}^2} \quad \mathbf{(7)}$$

$$\mathbf{E_2} = -\mathbf{V_{REF}}\mathbf{C}\left(-\frac{\mathbf{7}}{\mathbf{8}}\mathbf{V_{REF}} - \frac{\mathbf{1}}{\mathbf{4}}\mathbf{V_{REF}}\right) = \frac{\mathbf{9}}{\mathbf{8}}\mathbf{CV_{REF}^2} \quad \mathbf{(8)}$$

On the other hand, the switching energy consumed by the J-S capacitor array at each step is computed as follows:

$$\mathbf{E_0} = -\mathbf{V_{REF}}\mathbf{C}(-\frac{\mathbf{1}}{\mathbf{2}}\mathbf{V_{REF}} - \mathbf{0}) = \frac{\mathbf{1}}{\mathbf{2}}\mathbf{CV_{REF}^2} \quad \mathbf{(9)}$$

$$\mathbf{E_1} = -\mathbf{V_{REF}}\mathbf{C}\left(-\frac{\mathbf{3}}{\mathbf{4}}\mathbf{V_{REF}} + \frac{\mathbf{1}}{\mathbf{2}}\mathbf{V_{REF}}\right) = \frac{\mathbf{1}}{\mathbf{4}}\mathbf{CV_{REF}^2} \quad \mathbf{(10)}$$

$$\mathbf{E_2} = -\mathbf{V_{REF}}\mathbf{C}\left(-\frac{\mathbf{7}}{\mathbf{8}}\mathbf{V_{REF}} + \frac{\mathbf{3}}{\mathbf{4}}\mathbf{V_{REF}}\right) = \frac{\mathbf{1}}{\mathbf{8}}\mathbf{CV_{REF}^2} \quad \mathbf{(11)}$$

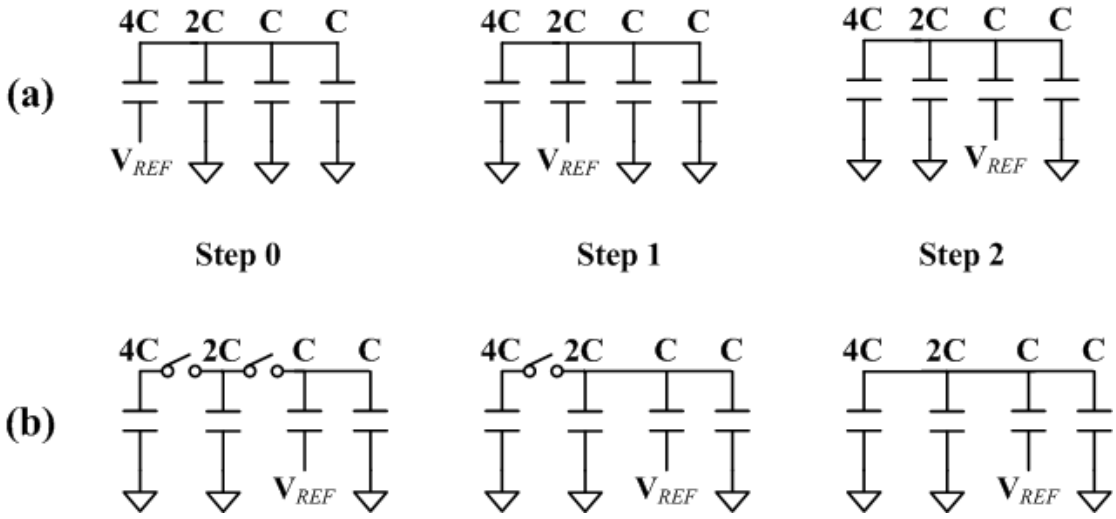


Figure 18 Switch transitions of the 3-bit capacitor array in case of code 000. (a) For the conventional capacitor array. (b) For the J-S capacitor array

The power consumption is remarkably reduced by the J-S capacitor array, but the accuracy performance is also significantly worse by the J-S capacitor array. For the purpose of avoiding the accuracy problem, the switching method is only used to reduce the power consumption of the MSB decision.

C. The proposed capacitor array

The schematic of the proposed DAC capacitor array is shown in Figure 19.

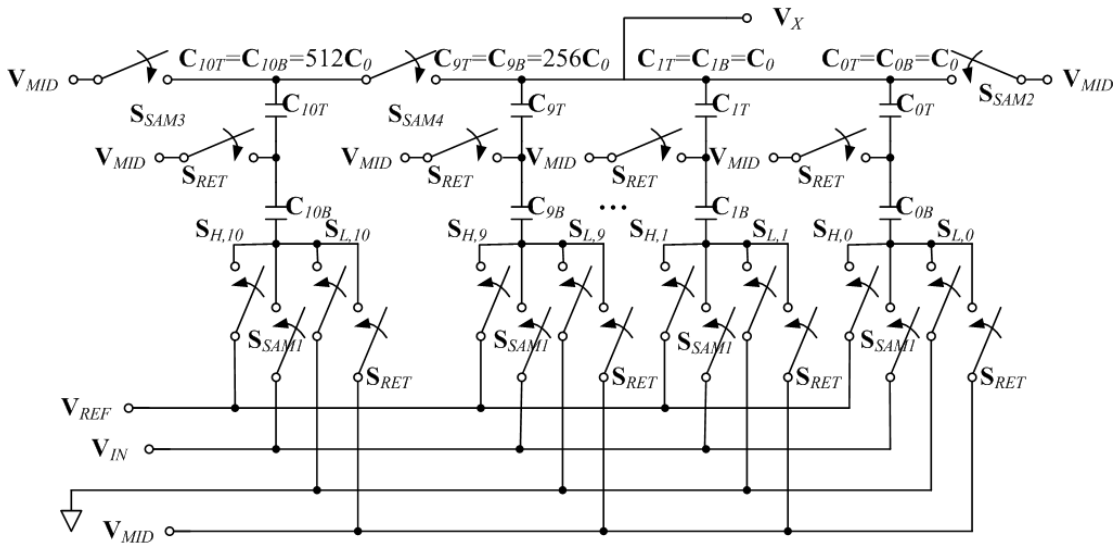


Figure 20 The schematic of the proposed capacitor array

The operations of the proposed capacitor array are as follows. First, for the purpose of avoiding charge accumulation between two series capacitors, the charges on the two capacitors are released by turning on $\mathbf{S}_{RET}$, $\mathbf{S}_{SAM2}$, and $\mathbf{S}_{SAM3}$. Otherwise, $\mathbf{S}_{SAM1}$ and $\mathbf{S}_{SAM4}$ are off. After all charges on the capacitors are released, $\mathbf{S}_{RET}$ is off, but $\mathbf{S}_{SAM2}$ and $\mathbf{S}_{SAM3}$ are still on. At the same time, the operation of sampling is started by turning on $\mathbf{S}_{SAM1}$. At the end of the sampling cycle, $\mathbf{S}_{SAM1}$ is off to end the operation of sampling. Besides, $\mathbf{S}_{SAM2}$ is also off. After the operation of sampling is completed, the conversion is started. The bottom of $\mathbf{C}_{9B}$ is first connected to $\mathbf{V}_{REF}$, and others are connected to the ground excluding the bottom of $\mathbf{C}_{10B}$. The bottom of $\mathbf{C}_{10B}$ remains floating. The value of $\mathbf{V}_X$ is as follow.

$$\mathbf{V_x = V_{MID} - V_{IN} + \frac{1}{2}V_{REF}} \quad \textbf{(12)}$$

If $\mathbf{V}_X$ is higher than $\mathbf{V}_{MID}$, the most significant bit (MSB) $\mathbf{D}_{10}$ is 0; alternatively, $\mathbf{D}_{10}$ is 1. After the first conversion cycle, $\mathbf{S}_{SAM4}$ is on for the operation of the J-S switching method. No matter $\mathbf{D}_{10}$ is 1 or 0, $\mathbf{S}_{H,9}$ keeps on during the second cycle of the conversion. However, if $\mathbf{D}_{10}$ is 0, the bottom of $\mathbf{C}_{10B}$ is connected to the ground. The value of $\mathbf{V}_X$ is as follow.

$$\mathbf{V}_x = \mathbf{V}_{MID} - \mathbf{V}_{IN} + \frac{1}{4}\mathbf{V}_{REF} \quad \textbf{(13)}$$

Alternatively, the bottom of $\mathbf{C}_{10B}$ is connected to $\mathbf{V}_{REF}$. The value of $\mathbf{V}_X$ is as follow.

$$\mathbf{V}_x = \mathbf{V}_{MID} - \mathbf{V}_{IN} + \frac{3}{4}\mathbf{V}_{REF} \quad \textbf{(14)}$$

Again, the value of $\mathbf{V}_X$ is compared with $\mathbf{V}_{MID}$ to decide the second significant bit $\mathbf{D}_9$. According to the value of $\mathbf{D}_9$, the bottom of $\mathbf{C}_{9B}$ is connected to the ground if $\mathbf{D}_9$ is 0; otherwise, the bottom of $\mathbf{C}_{9B}$ is connected to $\mathbf{V}_{REF}$.

The remaining bits are going to be converted as follows. When the conversion cycle for $\mathbf{D}_i$ is coming, the bottom of $\mathbf{C}_{iB}$ is first connected to VREF. Then, the connection of $\mathbf{C}_{iB}$ depends on the result of $\mathbf{D}_i$ as follows.

$$\mathbf{D_i} = \begin{cases} \mathbf{1}, & \textbf{The bottom of } \mathbf{C_{iB}} \textbf{ is connected to} \mathbf{V_{REF}} \\ \mathbf{0}, & \textbf{The bottom of } \mathbf{C_{iB}} \textbf{ is connected to the ground} \end{cases} \quad \textbf{(15)}$$

There are ten conversion cycles needed for 10-bit resolution. When the conversion is completed, 10 bit output codes are transmitted at the same time. All control signal status are listed inTable III. The switching comparison is shown in Figure 21. The proposed capacitor array consumes only 40% power dissipation of a conventional binary weighted capacitor array. Figure 22 shows the timing diagram for the conversion. A complete signal conversion takes twenty clock cycles to finish.

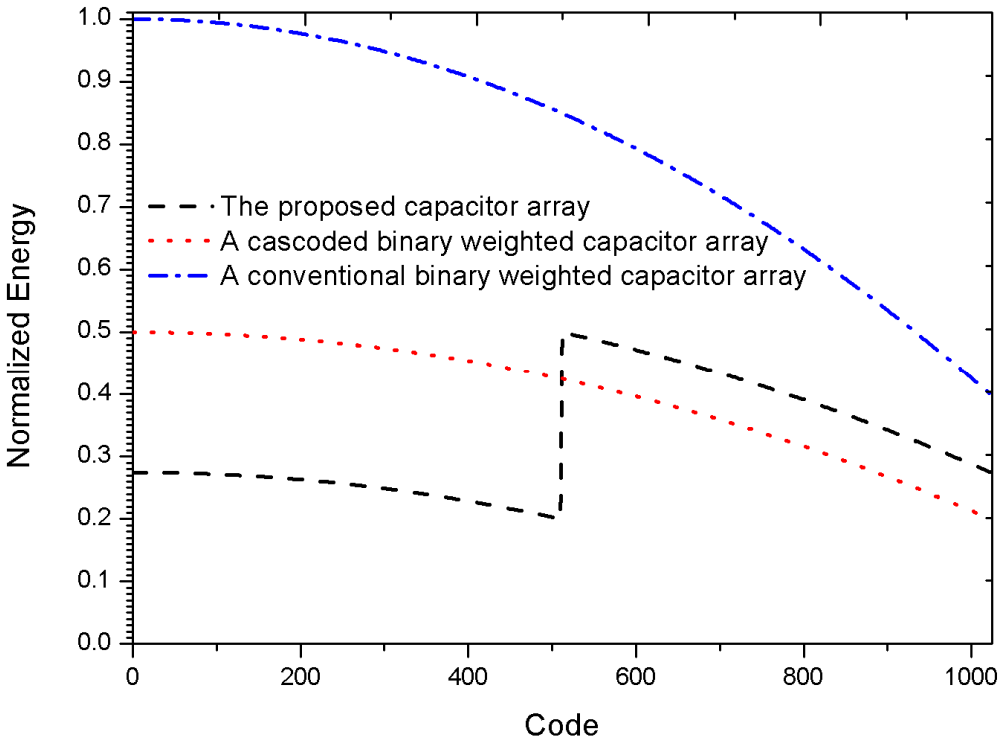


Figure 23 Switching energy comparison

Operation	Switch Status	
	ON	OFF
Reset	$\mathbf{S}_{RET}$, $\mathbf{S}_{SAM2}$, $\mathbf{S}_{SAM3}$	$\mathbf{S}_{SAM1}$, $\mathbf{S}_{SAM4}$
Sampling	$\mathbf{S}_{SAM1}$, $\mathbf{S}_{SAM2}$, $\mathbf{S}_{SAM3}$	$\mathbf{S}_{RET}$, $\mathbf{S}_{SAM4}$
Conversion of $\mathbf{D}_{10}$	$\mathbf{S}_{SAM3}$	$\mathbf{S}_{RET}$, $\mathbf{S}_{SAM1}$, $\mathbf{S}_{SAM2}$, $\mathbf{S}_{SAM4}$
Conversion of $\mathbf{D}_9$~$\mathbf{D}_1$	$\mathbf{S}_{SAM4}$	$\mathbf{S}_{RET}$, $\mathbf{S}_{SAM1}$, $\mathbf{S}_{SAM2}$, $\mathbf{S}_{SAM3}$

Table III Signal Control

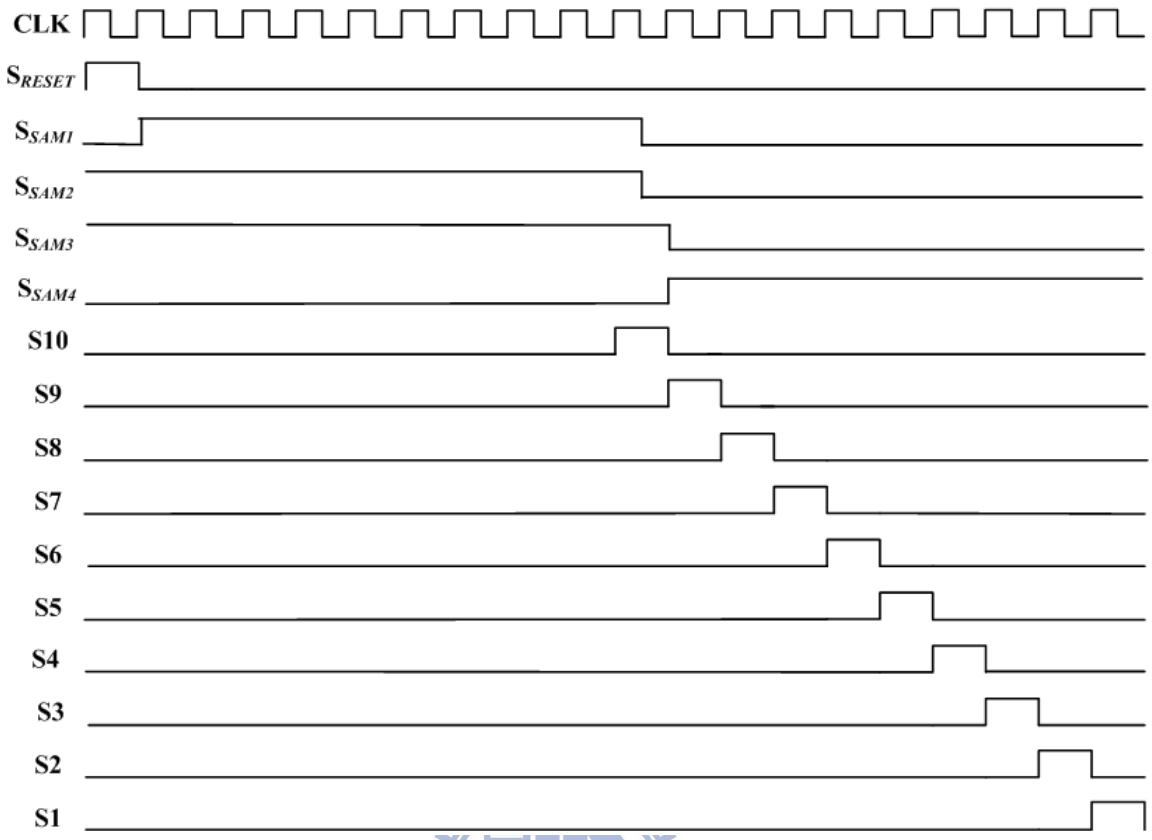


Figure 24 The timing diagram

In order to finish a good design for the proposed capacitor array, the common centroid capacitor array layout is required. Figure 25 shows the detailed floor plan for the proposed capacitor array.

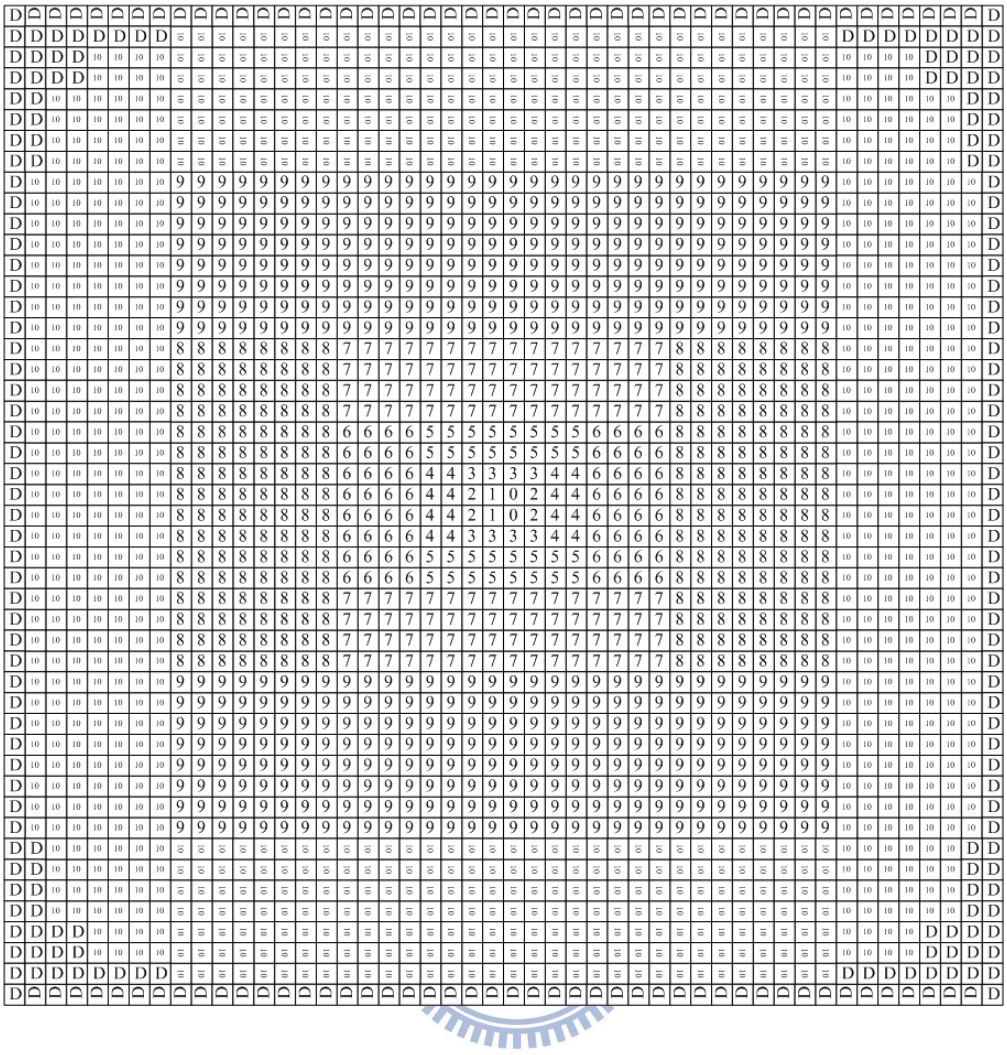


Figure 26 Floor plan of common centroid capacitor array

2.2.4 Comparator

For low-resolution applications, the comparator consumes more power than the DAC. Recently, the SAR architecture is applied to high-resolution applications, and the DAC dominates the power consumption of the ADC. In addition to low-power design of the comparator, the offset voltage of the comparator attracts more attention for high-resolution applications. The block diagram of the comparator is shown in Figure 27. Three stages of preamps are used to significantly reduce the offset voltage. The latch is used to yield the output rapidly. The detailed circuits of

the comparator and the latch are shown in Figure 28. Table IV and Table V shows transistor sizes of the preamp and the latch.

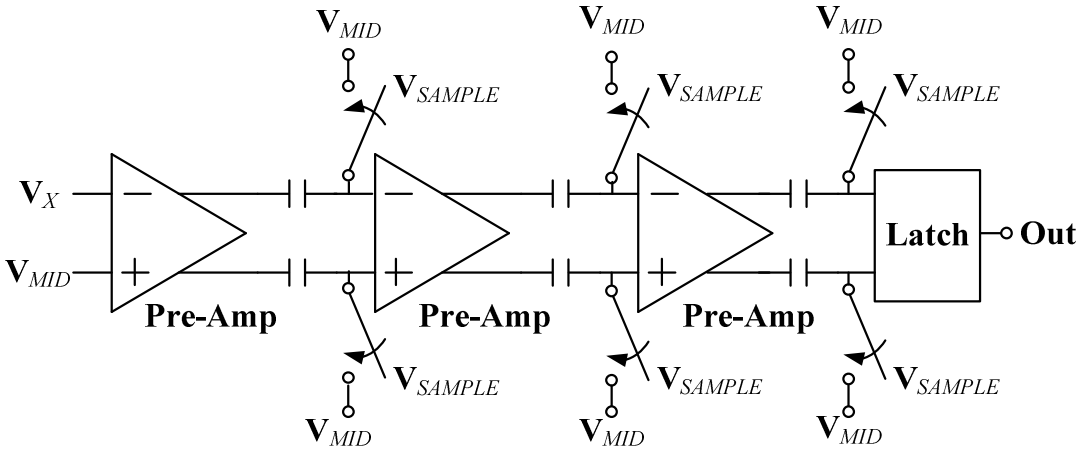


Figure 29 The block diagram of the comparator

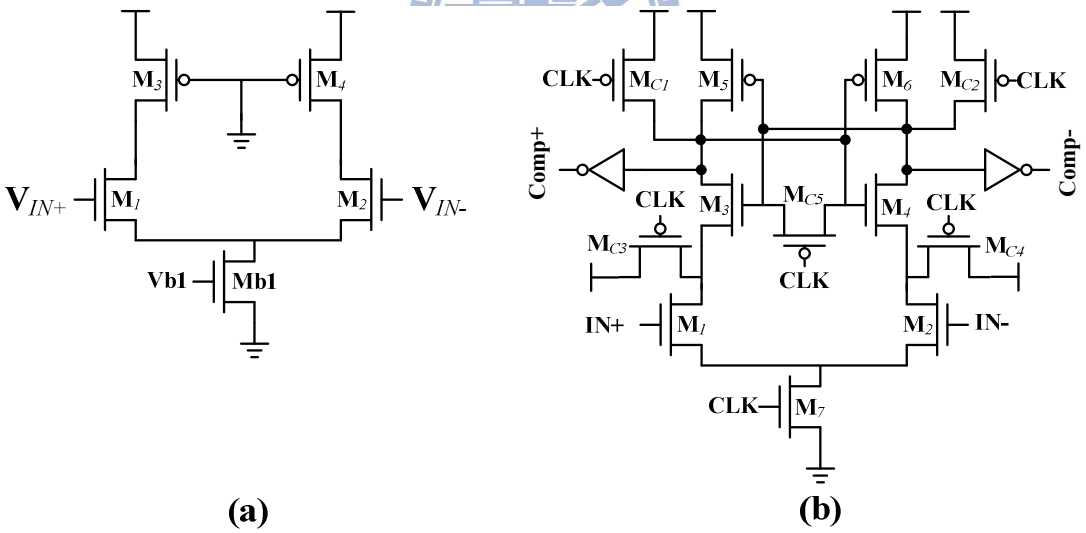


Figure 30 (a) The circuit of the preamp (b) The circuit of the latch

Transistor	W/L (μm)	Multiple
M1, M2	**0.5/0.18**	**4**
M3, M4	**0.25/6**	**1**
Mb1	**20/0.18**	**4**

Table IV Transistor sizes of the preamp

Transistor	W/L (μm)	Multiple
M1, M2	**1/0.18**	**1**
M3, M4	**1/0.18**	**1**
M5, M6	**1/0.18**	**1**
M7	**1/0.18**	**1**
Mc1, Mc2, Mc3, Mc4, Mc5	**0.25/0.18**	**1**

Table V Transistor sizes of the latch

2.2.5 Successive Approximation Register

Digital control circuits include the successive approximation register and control logics. The successive approximation register generates the pulse signal for every bit conversion cycle, and stores the outputs generated by the comparator. The control logics are composed of many simple logic gates, and control the switches to connect to the ground or $\mathbf{V}_{REF}$.

The successive approximation register, which is composed of many D Flip-Flops, is shown in Figure 31. The detailed circuit of a D Flip-Flop is shown in Figure 32.

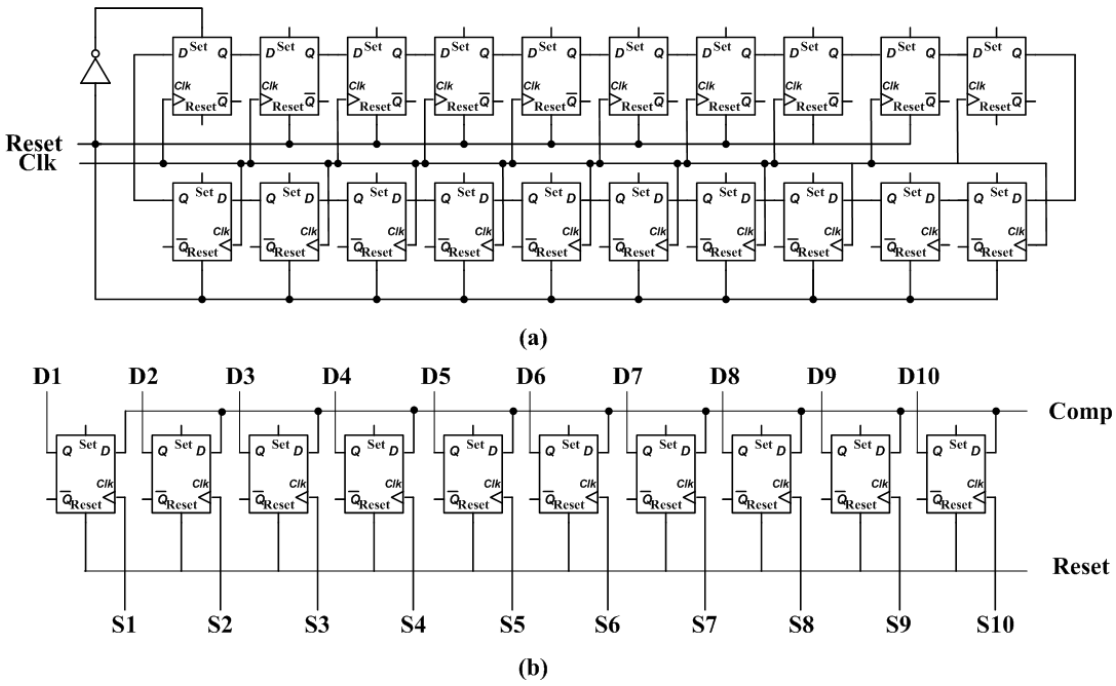


Figure 33 The two main parts of the successive approximation register. (a) The pulse generator generates the pulses needed for every bit-cycle operation. (b) The register stores the output code during the coversion.

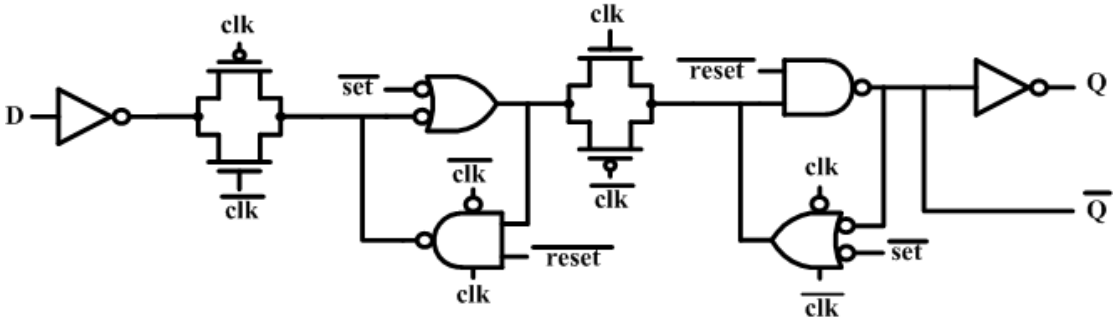


Figure 34 The detailed circuit of a D Flip-Flop.

2.3 Post-Simulation Results

2.3.1 Dynamic Performance

In addition to the DNL and INL, which are usually referred to as static (low frequency) performance measures, another metric to determine the dynamic performance of the ADC is to measure the distortion ratio by applying a sinusoidal input signal and analyze the output codes in terms of frequency content. The frequency power spectrum can later be used to calculate the signal-to-noise and distortion ratio, SNDR, which is the power strength and the effective-number-of-bits, ENOB, which is the actual resolution of the ADC. The ENOB is defined as:

$$\mathbf{ENOB} = \frac{\mathbf{SNDR} - \mathbf{1.76}}{\mathbf{6.02}} \quad \textbf{(16)}$$

where the SNDR is the signal power divided by any distortion and noise in the ADC output with unit in dB.

Figure 35 shows simulation results of 50 kHz 1.8V input sine wave. From the FFT analysis, the signal to noise and distortion ratio (SNDR) is calculated as 59.26 dB, and the effective number of bits (ENOB) is 9.55. In Figure 36, detailed simulation results are performed to compare SNDR at different input frequencies and different corners. Table VI is shown the detailed data number.

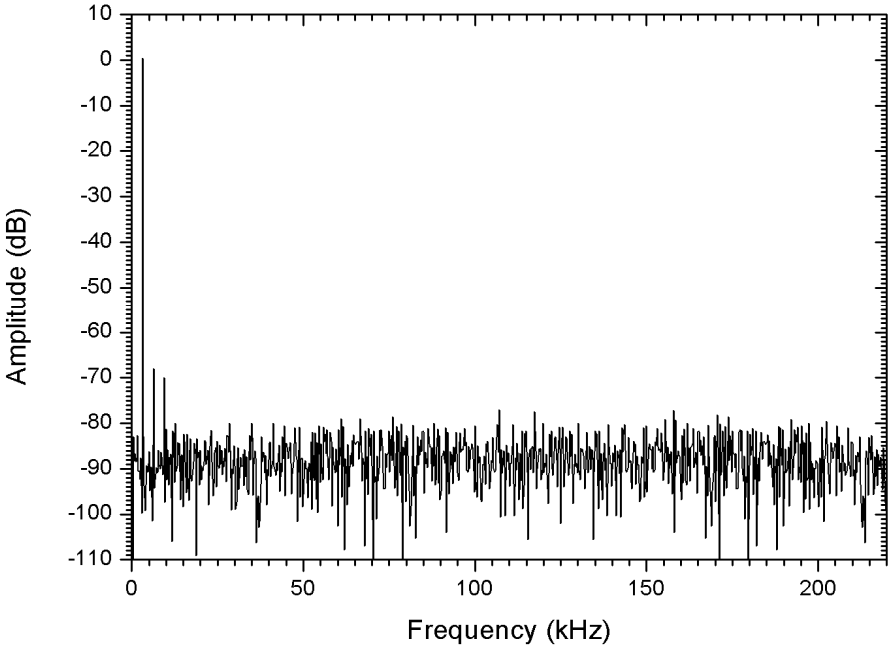


Figure 37 FFT Analysis of TT corner with 1.8V 5.6 kHz input sine wave

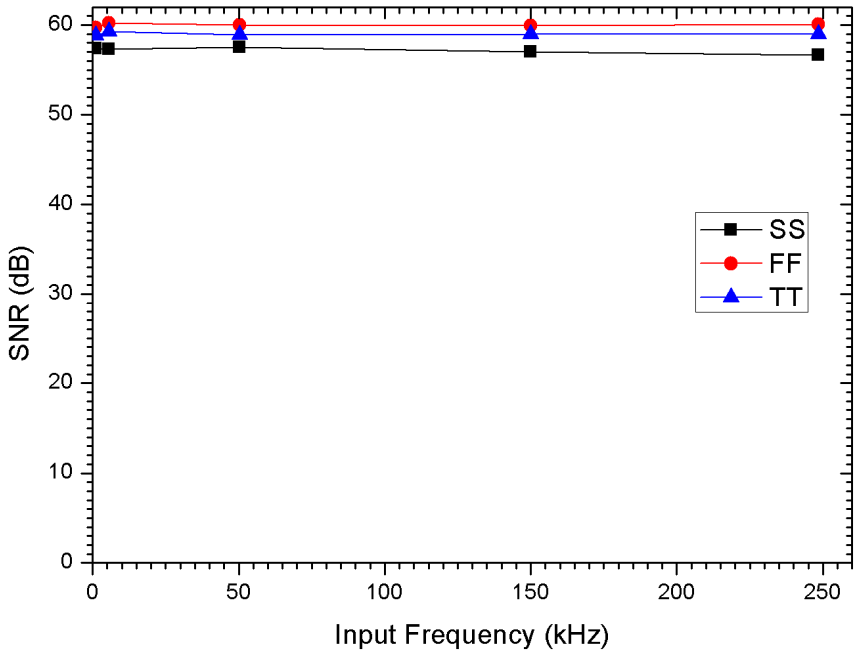


Figure 38 SNDR of different input frequencies and different corners

Corner	Input frequency	SNDR
TT	1 kHz	58.82 dB
	5 kHz	59.26 dB
	50 kHz	58.89 dB
	150 kHz	59.00 dB
	250 kHz	58.98 dB
SS	1 kHz	57.40 dB
	5 kHz	57.30 dB
	50 kHz	57.50 dB
	150 kHz	57.05 dB
	250 kHz	57.67 dB
FF	1 kHz	59.70 dB
	5 kHz	60.02 dB
	50 kHz	60.22 dB
	150 kHz	60.10 dB
	250 kHz	60.01 dB

Table VI SNDR of different input frequencies and different corners

2.3.2 Static Performance

The DNL error defines the difference of the input width of each code with the ideal input width. Although each unique ADC output code corresponds to a certain input signal range, the output code width can be slightly different in reality. When the output code corresponds to a large range of the input signal, it means the code appears too many times comparing with other codes. This results the DNL error to be positive. Consequently, a narrow output code indicates a negative DNL. The DNL equation is defined as:

$$\mathbf{DNL(a)} = \frac{\mathbf{W(a)} - \mathbf{W_{ideal}}}{\mathbf{W_{ideal}}} \quad \mathbf{(17)}$$

The DNL error unit is defined as an ADC LSB. If the DNL error is -1LSB, it means

there is a completely missing output code. As mentioned earlier, the output offset and gain error must be removed before calculating the DNL and INL.

The INL defines the error between the appearance of a certain output code and the actual ideal appearance of the output code. This is also the integral of the DNL errors. INL error is also presented in terms of ADC LSB. Because the INL measures the integral of the output code errors, the magnitude of an INL error can be greater than 1LSB without having any missing output codes. Figure 39 shows the differential nonlinearity (DNL) of the proposed SAR ADC. The simulation result of the DNL is +053/ -0.64 LSB. The integral nonlinearity (INL) is shown in Figure 40, and the value is +0.66/ -0.58 LSB.

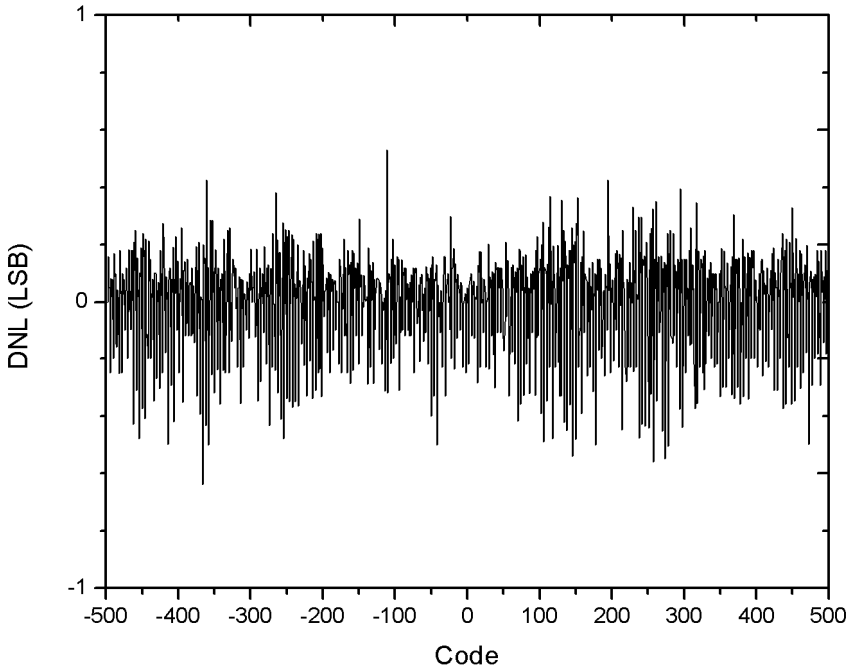


Figure 41 DNL

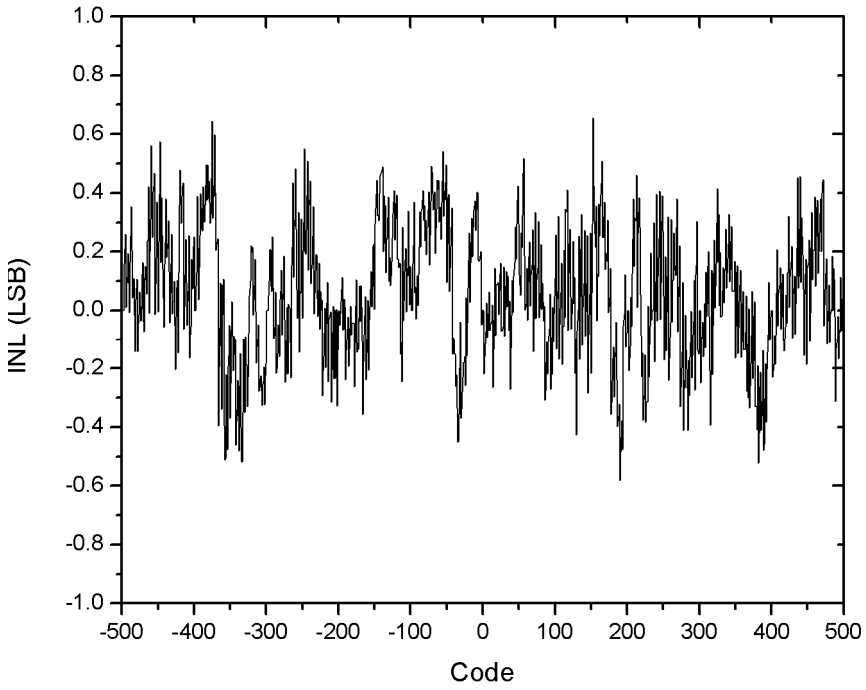


Figure 42 INL

2.3.3 Simulation Results and Comparison

The specification table of the proposed SAR ADC is shown in Table VII. In Table VIII, the comparison table shows the comparison with other references.

	Target Specifications	Post-simulation
Technology	**TSMC 0.18-um CMOS Process**	
Resolution	**10**	
Sampling Rate(S/s)	**500 K**	
Input Range	**0~1.8 V**	
Differential Nonlinearity	**<0.5**	**0.63/-0.54**
Integral Nonlinearity	**<1**	**0.66/-0.58**
SNDR@DC	**>55.94**	**59.26 dB**
ENOB@DC	**>9**	**9.55**
SNDR@Nyquist Rate	**>55.94**	**58.89 dB**
ENOB@Nyquist Rate	**>9**	**9.49**
Power Consumption		**80 µW**
Figure of Merit (fJ/Step)		**222**

Table VII Simulation results

	This Work	[4] JSSC03	[5] ISSCC06	[6] JSSC07	[8] ASSCC09	[9] JSSC10
Technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	65 nm
Resolution	10	8	12	8	10	10
Sampling Rate(S/s)	500 K	100 K	100 K	400 K	500 K	1 M
Input Range (V)	0~1.8	0~1	0~1	0~1	0~1	0~1
Supply Voltage (V)	1.8	1	1	1	1	1
ENOB	9.49	7.9	10.55	7.31	9.4	9
Power Consumption (µW)	80	3.1	25	6.15	42	1.9
FoM (fJ/Step)	222	129	167	97	124	4.4
Normalized FoM (fJ/Step)	68	129	167	97	124	4.4

Table VIII Comparison Table

Chapter 3
Experimental Results

3.1 Layout Descriptions

The die microphotograph is shown in Figure 43. In Figure 44, the location of each individual circuit block is marked on the complete SAR ADC layout. The overall circuit area is 1 mm^2. From this figure, it can be seen that the majority of the ADC area is occupied by the capacitor array. The entire layout was done very conservatively in terms of area, especially the capacitor array. The sensitive comparator circuit is separated from the successive approximation register circuit by large space. In this way, the coupling effect could be suppressed.

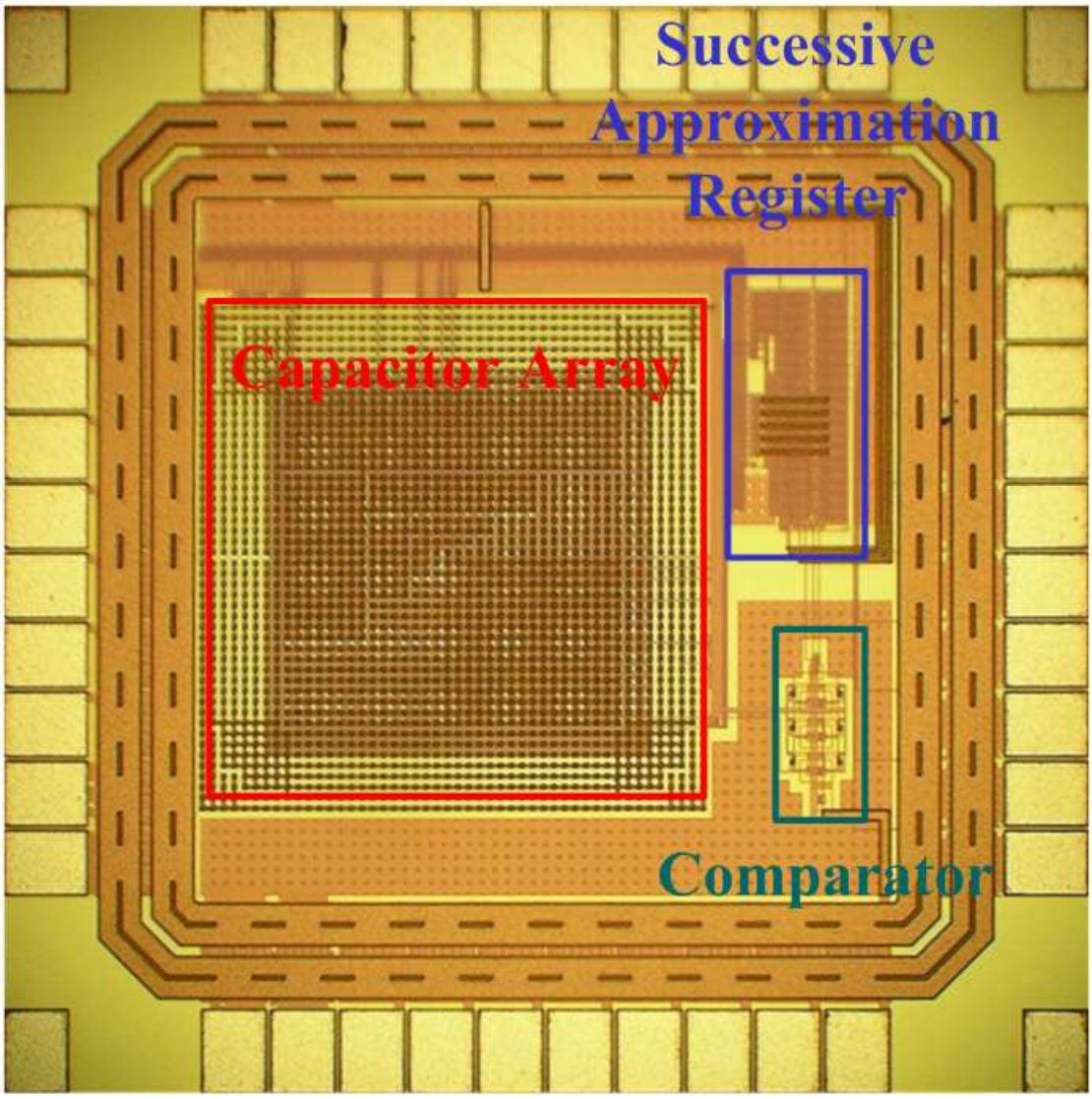


Figure 45 Die microphotograph

3.2 Measurement Setup

The measure environment setup is shown in Figure 46. The signal generator SRS DS360 is used to generate hundreds of kilo hertz sine wave. The supply voltage is from Agilent E3631A , which provides a stable 1.8 V for the proposed ADC. Finally, The logic analyzer Agilent 16822A is used to receive 10-bit output code of the ADC.

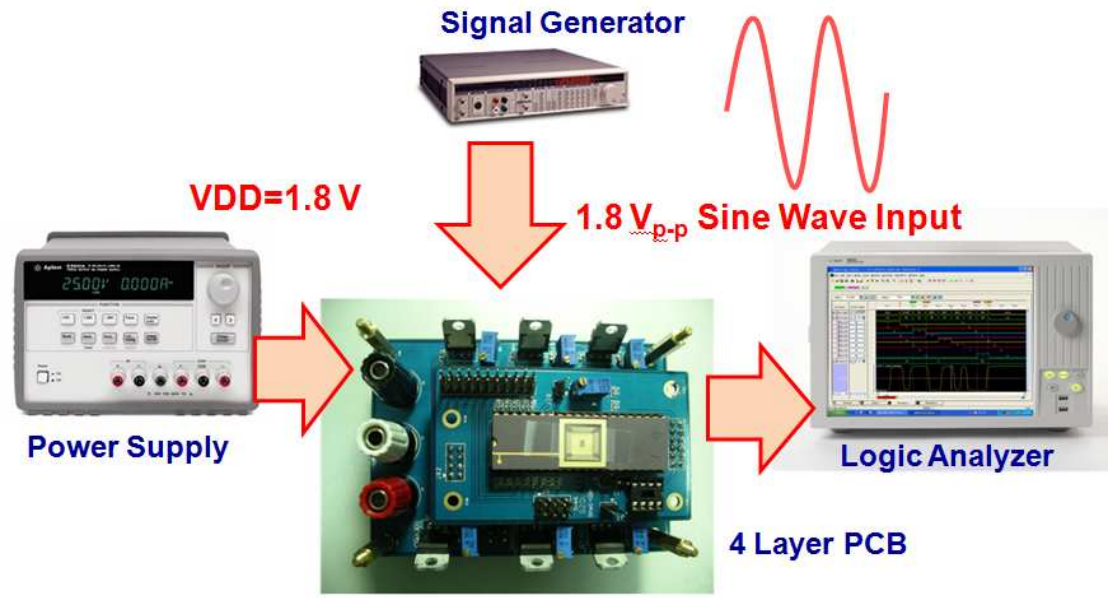


Figure 47 Measurement Setup

3.3 Measurement Results

This section describes the performance of the ADC which is packaged and tested using a custom PCB board.

3.3.1 Dynamic Performance

Figure 48 shows measurement results of 5.6 kHz 1.4V input sine wave. From the FFT analysis, the signal to noise and distortion ratio (SNDR) is calculated as 44.10 dB, and the effective number of bits (ENOB) is 7.03. In Figure 49, measurement results are shown to compare values of SNDR at different input frequencies. Table IX shows different input frequencies and corresponding values of SNDR.

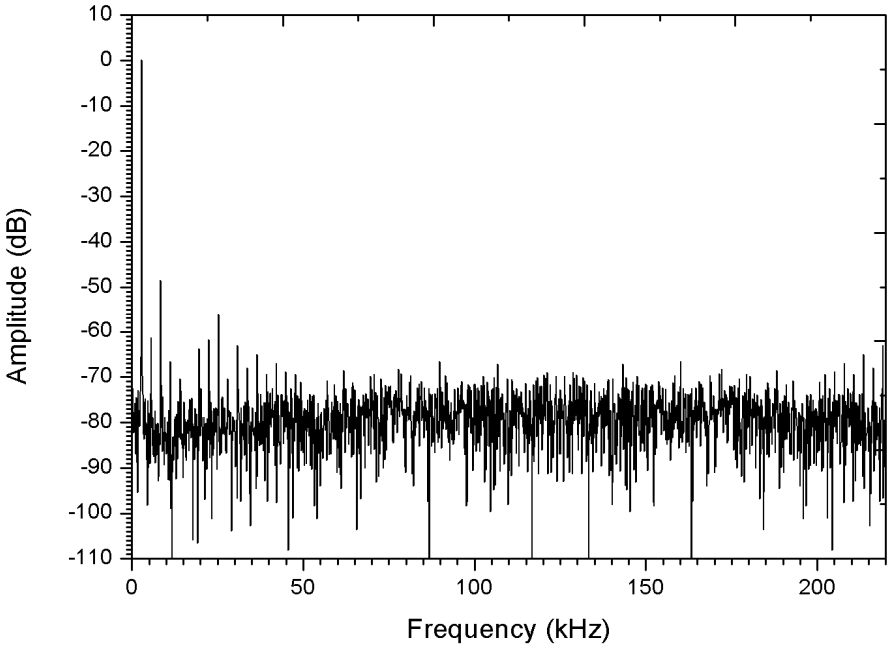


Figure 50 FFT Analysis with 1.4V 5.6 kHz input sine wave

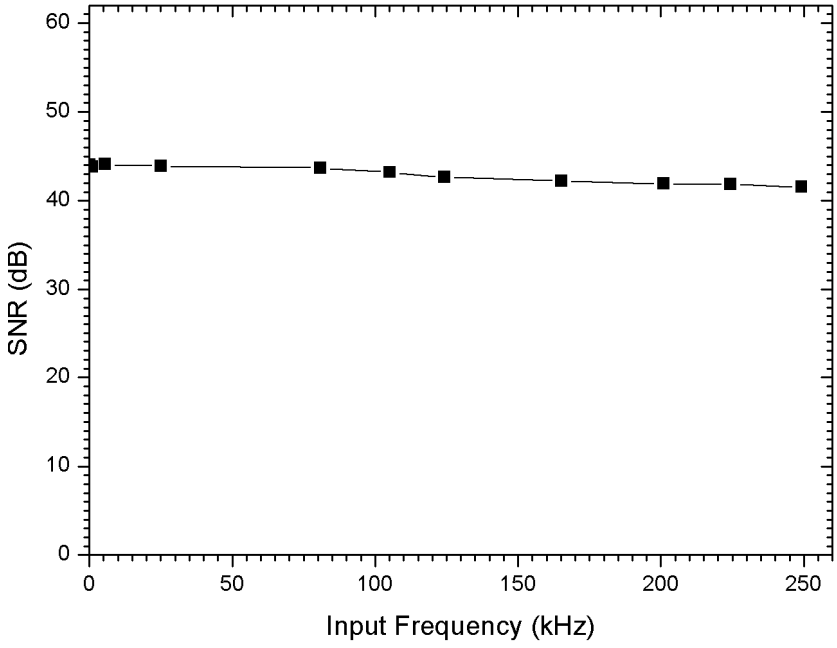


Figure 51 SNDR of different input frequencies

Input Frequency	SNDR
0.1kHz	43.8 dB
1kHz	44 dB
5 kHz	44.1 dB
25 kHz	43.9 dB
80 kHz	43.69 dB
105 kHz	43.2 dB
124 kHz	42.64 dB
165 kHz	42.24 dB
200 kHz	41.91 dB
224 kHz	41.85 dB
249 kHz	41.54 dB

Table IX SNDR of different input frequencies

In Figure 52, measurement results are performed to compare values of SNDR at different sampling rates. Table X shows different sampling rates and corresponding values of SNDR.

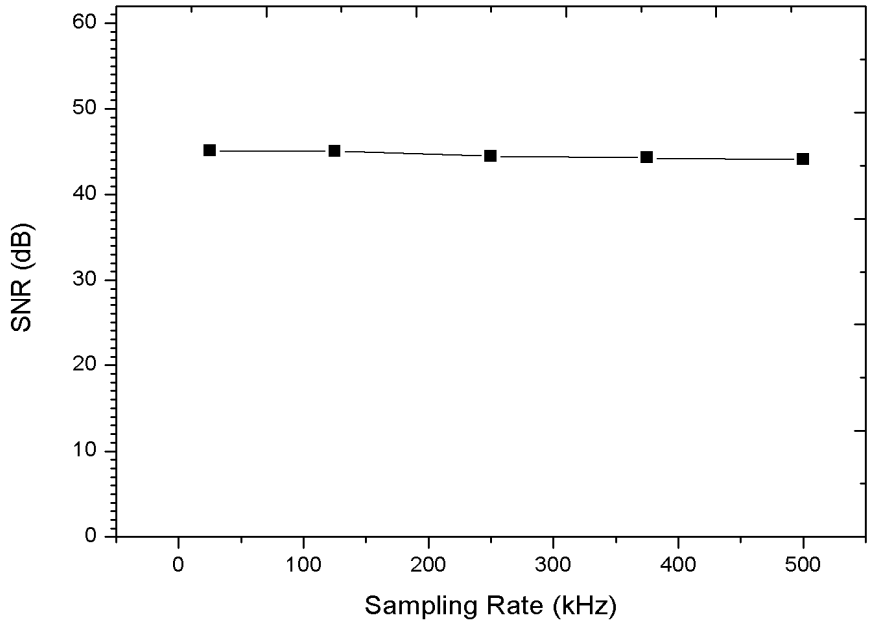


Figure 53 SNDR of Different input frequencies

Sampling Frequency	SNDR
25 kHz	45.15 dB
125 kHz	45.06 dB
250 kHz	44.5 dB
375 kHz	44.3 dB
500 kHz	44.1 dB

Table X SNDR of Different sampling rates

3.3.2 Static Performance

Figure 54 shows the differential nonlinearity (DNL) of the proposed SAR ADC. The measurement result of the DNL is 0.95/-1 LSB. The integral nonlinearity (INL) is shown in Figure 55 and the value is 4.8/-2.7 LSB.

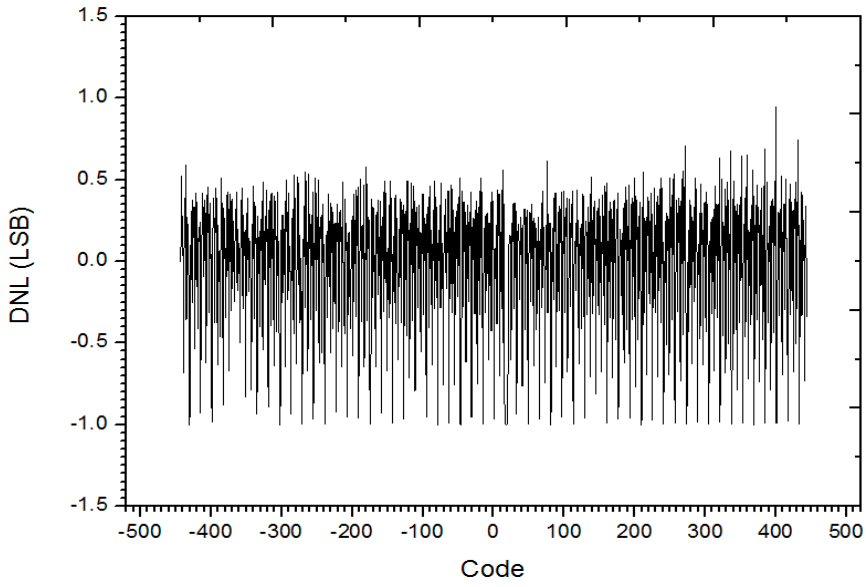


Figure 56 Measurement of DNL

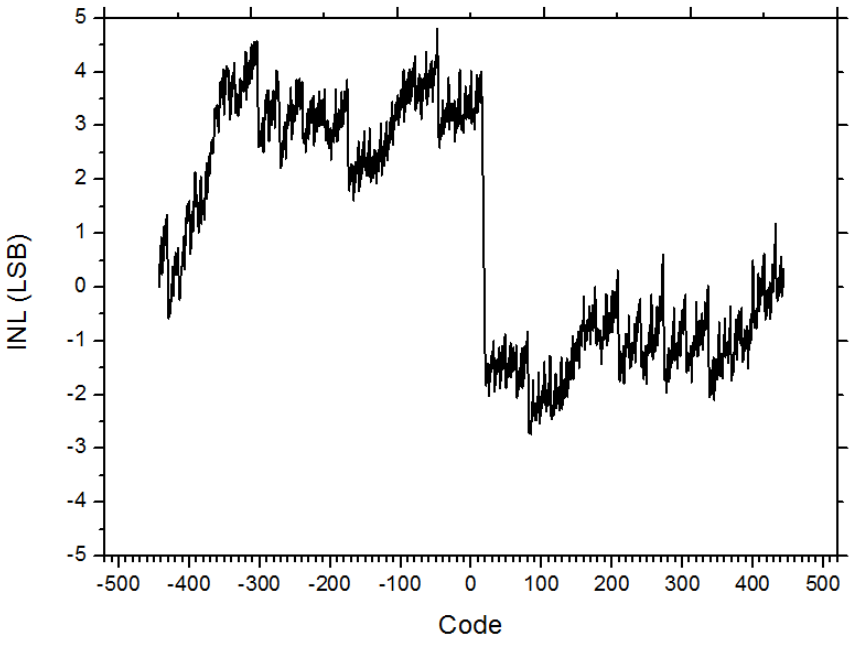


Figure 57 Measurementof INL

3.3.3 Comparison

The comparison between post-simulation results and measurement results are shown in Table XI. Measurement results are obviously worse than post-simulation results. There are some discussions in the next section.

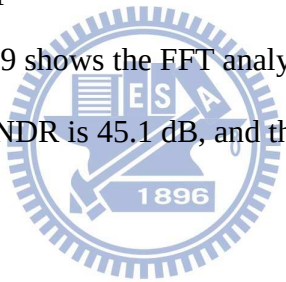
	Target Specifications	Original Post-simulation	Measurement
Technology	**TSMC 0.18 um 1P6M**		
Resolution	**1.8V**		
Sampling Rate(S/s)	**500 K**		
Input Range	**0~1.8V**		
Differential Nonlinearity	**<0.5**	**0.63/-0.54**	**0.95/-1**
Integral Nonlinearity	**<1**	**0.66/-0.58**	**4.8/-2.7**
SNDR@DC	**>55.94**	**59.26 dB**	**44.1 dB**
ENOB@DC	**>9**	**9.55**	**7.03**
SNDR@Nyquist Rate	**>55.94**	**58.89 dB**	**41.54 dB**
ENOB@Nyquist Rate	**>9**	**9.49**	**6.61**
Power Consumption		**80 µW**	**85 µW**

Table XI Comparison between post-simulation results and measurement results

3.4 Discussions

3.4.1 Revised post-simulation

In the original post-simulation, no inductor effects from bonding wires, PCB wires, and conducting wires are included. Therefore, there are no coupling effects on the supply voltage and the ground. This is the reason why original post-simulation results are much better than measurement results. After real conditions are detailed included, revised post-simulation results are performed and show the similar performance like measurement results. Figure 58 shows the difference between the original post-simulation model and the revised post-simulation model. Figure 59 shows the FFT analysis of the revised post-simulation. The value of SNDR is 45.1 dB, and the value of ENOB is 7.2.



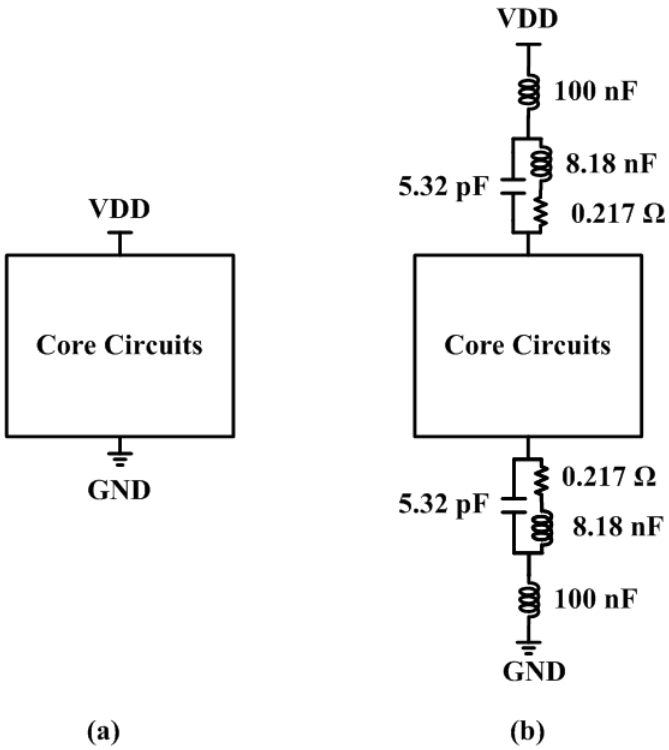


Figure 60 (a) Original post-simulation model (b) Revised post-simulation model

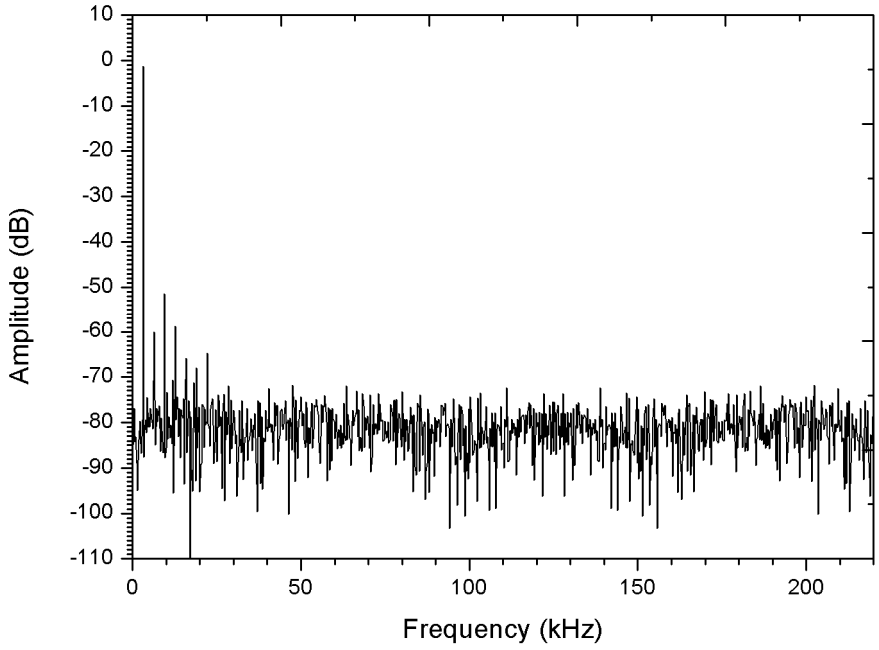


Figure 61 FFT analysis of the revised post-simulation

	Target Specifications	Revised post-simulation	Measurement
Technology	**TSMC 0.18 um 1P6M**		
Resolution	**1.8V**		
Sampling Rate(S/s)	**500 K**		
Input Range	**0~1.8V**		
SNDR@DC	**>55.94**	**45.1 dB**	**44.1 dB**
ENOB@DC	**>9**	**7.2**	**7.03**
SNDR@Nyquist Rate	**>55.94**	**43.2 dB**	**41.54 dB**
ENOB@Nyquist Rate	**>9**	**6.88**	**6.61**
Power Consumption		**81 µW**	**85 µW**
Figure of Merit (fJ/Step)		**1101**	**1310**
Normalized Figure of Merit (fJ/Step)		**340**	**404**

Table XII Comparison between revised post-simulation results and measurement results

3.4.2 Modified post-simulation

Although revised post-simulation result fit measurement results, the layout of the proposed SAR ADC is revolved. Finally, a mistake is found to explain the poor performance of the proposed SAR ADC. The supply voltages of the capacitor array and the successive approximation register are connected together, and the input signal is seriously distorted during sampling. Figure 62 shows how the input signal is distorted by the supply voltage and the ground. In order to solve this problem, the

supply voltage of the capacitor array is separated from the successive approximation register. Figure 63 shows the FFT analysis of the modified post-simulation. The value of SNDR is 57.53 dB, and the value of ENOB is 9.26. From the FFT analysis, the modified post-simulation shows the similar result like the original post-simulation.

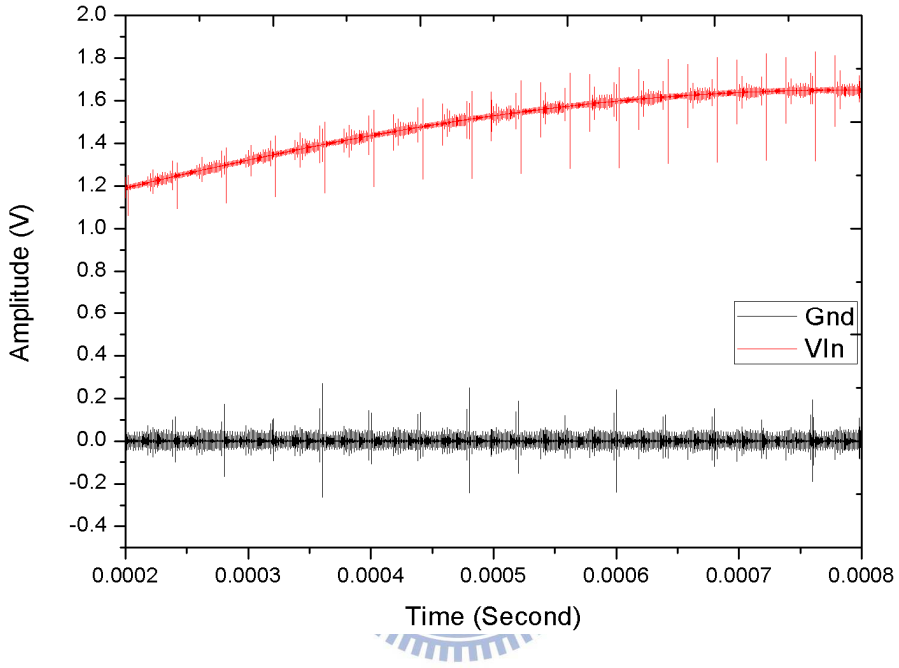


Figure 64 Input signal V_{in} distorted by the supply voltages

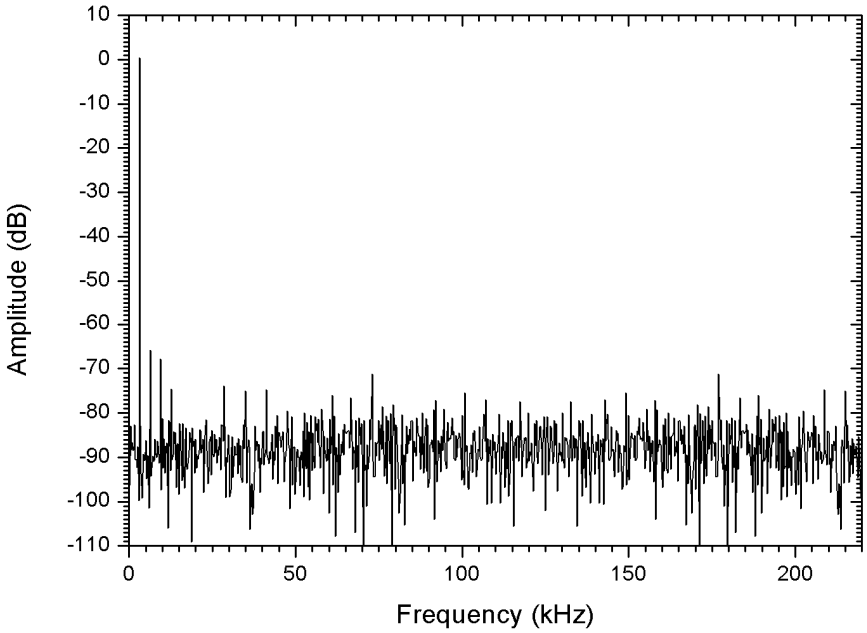


Figure 65 FFT analysis of modified post-simulation

	Target Specifications	Modified post-simulation	Measurement
Technology	**TSMC 0.18 um 1P6M**		
Resolution	**1.8V**		
Sampling Rate(S/s)	**500 K**		
Input Range	**0~1.8V**		
SNDR@DC	**>55.94**	**57.53 dB**	**44.1 dB**
ENOB@DC	**>9**	**9.26**	**7.03**
SNDR@Nyquist Rate	**>55.94**	**56.92 dB**	**41.54 dB**
ENOB@Nyquist Rate	**>9**	**9.16**	**6.61**
Power Consumption		**83 µW**	**85 µW**
Figure of Merit (fJ/Step)		**270**	**1310**
Normalized Figure of Merit (fJ/Step)		**84**	**404**

Table XIII Comparison between modified post-simulation results and measurement results

	This Work	[4] JSSC03	[5] ISSCC06	[6] JSSC07	[8] ASSCC09	[9] JSSC10
Technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	65 nm
Resolution	10	8	12	8	10	10
Sampling Rate(S/s)	500 K	100 K	100 K	400 K	500 K	1 M
Input Range (V)	0~1.8	0~1	0~1	0~1	0~1	0~1
Supply Voltage (V)	1.8	1	1	1	1	1
ENOB	9.26	7.9	10.55	7.31	9.4	9
Power Consumption (µW)	83	3.1	25	6.15	42	1.9
FoM (fJ/Step)	270	129	167	97	124	4.4
Normalized FoM (fJ/Step)	84	129	167	97	124	4.4

Table XIV Comparison Table

Chapter 4
Conclusions and Future Work

4.1 Conclusions

A successive-approximation analog-to-digital converter is presented in this thesis. A 10-bit 500-KS/s SAR ADC, which is designed for implantable epilepsy devices, is proposed in the chapter 2. The proposed binary weighted capacitor array has good capacitance mismatch performance like a conventional binary weighted capacitor array, but only consumes 50% switching energy. Part of the junction-split switching method is also applied to reduce switching energy. The proposed capacitor array only consumes 40% power dissipation of a conventional capacitor array.

Measurement results of the fabricated ADC show low power consumption of 85 μW, SNDR of 44.10 dB, and ENOB of 7.03. The ADC performance is much worse than original post-simulation results because the supply voltage and the ground of the capacitor array and the successive approximation register are connected together. The input signal is seriously distorted.

After the layout is modified, modified simulation results show power consumption of 81 μW, SNDR of 57.53 dB, and ENOB of 9.26, which are similar to the original post-simulation results.

4.2 Future Work

The proposed successive approximation analog-to-digital converter has serious coupling effects because of the connected supply voltage and the ground of the capacitor array and the successive approximation register. The problem could be solved from the layout and then the ADC will have much better performance.

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