國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於太陽能之高效率的電源管理系統

High Efficiency Power Management System For Solar Energy Harvesting Applications

研 究 生：吳俊毅

指導教授：黃 威 教授

中 華 民 國 九 十 八 年 九 月

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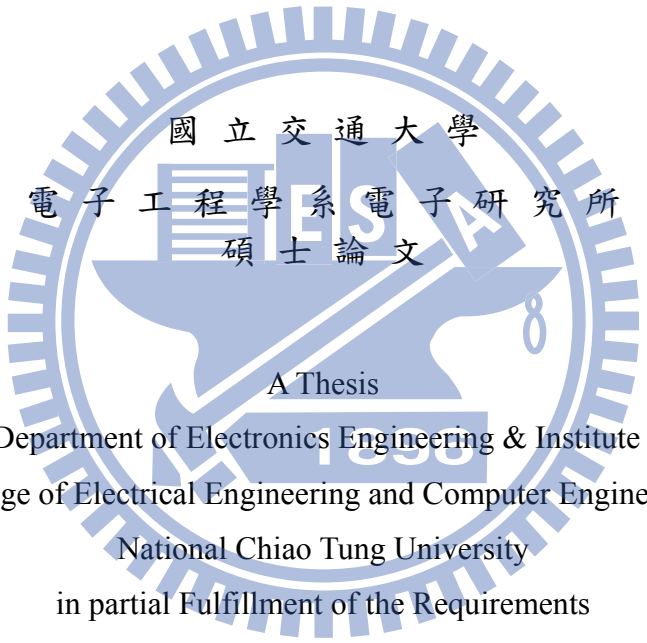

國 立 交 通 大 學

電 子 工 程 學 系 電 子 研 究 所

碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

September 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年九月

應用於太陽能之高效率的電源管理系統

學生：吳俊毅　　指導教授：黃　威　教授

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摘　　要

在本篇論文中，我們將目標放在設計並實現一個應用於太陽能之高效率的電源管理系統。其中包含電壓調節器和交換式電容直流-直流轉換器、高電壓電荷幫浦以及太陽能最大功率追踪控制電路設計。主要的研究成果如下：

1. 在本篇論文中提出了一個可應用於太陽能之高效率的電源管理系統。本系統藉由太陽能採集能量，並且產生不同的電壓位準以應用於 SoC 電壓調節 (例如:1V~0.3V 提供給類比電路和低功率數位電路，-1.2V 提供給記憶體電路，5V 提供給 I/O 元件)。
2. 一個新的連接架構用於改善高電壓電荷幫浦的能量效益和提升負載能力被提出。
3. 提出了一個可應用於太陽能最大功率追踪電路以控制太陽能電池位於最大功率區域並整合至功率管理系統中，使系統可對電池補充能量，並且有效率的利用電池的能量。

High Efficiency Power Management System For Solar Energy Harvesting Applications

Student : Chun-Yi Wu Advisors : Prof. Wei Hwang

Department of Electronics Engineering & Institute of Electronics

National Chiao-Tung University

ABSTRACT

The goal of this research is to design and implement a high efficiency power management system for solar energy harvesting applications. This includes the design of voltage regulator and switched capacitor DC-DC converter, high charge pump and PV cell maximum power tracking control circuit. The major contributions of this thesis are list as follow:

1. A high efficiency power management system for solar energy harvesting applications is proposed. The power management system receives power from photovoltaic (PV) cell and generate different voltage levels which are suitable for SoC integrated regulator applications (such as 1V~0.3V for analog circuitry and low power digital circuitry, -1.2V for memory circuitry, and 5V for I/O components).

2. A novel connect scheme for improving power efficiency and loading capability of charge pump which generates ultra high voltage is proposed.

3. A maximum power tracking circuit for controlling PV cell in maximum power region is proposed and integrated to the power management system for solar energy harvesting applications. The power management system works with a rechargeable battery and uses the energy of battery efficiently.

Acknowledgement

感謝我的指導教授黃威教授，在自由的研究風氣下讓我對自己研究的領域有更加深入的瞭解，並且提供優良的研究環境與充足的研究資源，讓我自由發揮想法和創意來完成這一篇論文。感謝口試委員莊景德教授和周世傑教授在論文上的建議和鼓勵，讓我的論文可以更加完整。

感謝維致學長培養我獨立解決問題的能力，讓我學習遇到任何問題都能靠自己去找到答案。感謝柏蒼學長、明宏學長和浩義學長在研究生活上無私的分享，讓我有了一些不同的體會。感謝同豪學長在研究上的幫忙，讓我可以承接先前的研究成果再加以發揚光大。感謝我的好伙伴益銘、士祺和各方好友的支持與鼓勵，讓苦悶的研究生活不再覺得孤單。

最後我要感謝我的家人對我在生活上的幫助以及精神上的支持，讓我遇到挫折更有勇氣去面對，並且能夠順利的完成碩士的論文研究。

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Chapter 1 Introduction

1.1 Motivation of the Thesis

In the recent years, the market of portable devices likes notebook, cell phone, PDA and smart phone is grow up rapidly and more new portable products will be developed in the near future. In the developing of portable devices, more and more functions are integrated into a product. At the same time, people concern that whether the product can use for a long time without charging the battery in charge socket. And the capacity of batteries improves relatively slowly then the power consumption of the portable devices which is integrated more and more functional blocks. So the environmental power harvesting applications can provide a charge method for overall system and extends the system life.

Due to the green power considerations and eco-awareness, the research of energy harvesting application is getting popular. Previously, the system of tracking maximum output power of photovoltaic cell was implemented in [1]. An ultra-low voltage power management for energy harvesting applications was developed and worked with a FIR filter in [2]. With low output voltage of solar cell, a micro power management system was proposed in [3]. The micro power management system decided the working frequency of charge pump by the room lighting environment and outputted the maximum power to loading circuitry. An energy harvesting application with micro battery was also implemented in [4]. This power management circuit accepted energy from RF power and thermo generator power and outputted the power to micro battery as energy storage. A battery management system for solar energy applications was developed in [5]. The battery management system was used to increase the service life of the battery.

1.2 Research Goals and Major Contributions

The goal of this research is to design and implement a high efficiency power management system for solar energy harvesting applications. This includes the design of voltage regulator and switched capacitor DC-DC converter, high voltage generator and PV cell maximum power tracking control circuit.

The major contributions of this thesis are list as follow:

1. A high efficiency power management system for solar energy harvesting applications is proposed. The power management system receives power from photovoltaic (PV) cell and generate different voltage levels which are suitable for SoC integrated regulator applications (such as 1V~0.3V for analog circuitry and low power digital circuitry, -1.2V for memory circuitry, and 5V for I/O components).
2. A novel connect scheme for improving power efficiency and loading capability of charge pump which generates ultra high voltage is proposed.
3. A maximum power tracking circuit for controlling PV cell in maximum power region is proposed and integrated to the high efficiency power management system for solar energy harvesting applications. The power management system works with a rechargeable battery and efficiently uses the energy of battery.

1.3 Thesis Organization

The rest of the thesis is organized as follows: an overview of solar energy harvesting applications technique is introduced in the Chapter 2. The characteristics of photovoltaic (PV) cell and a maximum peak power tracking technique are introduced. The detail circuit of previous power management system for solar energy harvesting

applications is also introduced.

The techniques of improving the stability and transient response of voltage regulator are introduced in the Chapter 3. The voltage regulator and switched capacitor DC-DC converter for SoC integrated regulator applications are proposed in the Chapter 3. The voltage doubler and Dickson charge pump are introduced in the Chapter 4. The techniques of improving the pumping efficiency of charge pump are also introduced. For improving the power efficiency and loading capability of charge pump which generates ultra high voltage, a novel connect scheme is proposed in the Chapter 4.

An integrated power management system for solar energy harvesting applications is proposed in the Chapter 5. The power management system generates different voltage levels for the SoC integrated regulator applications by voltage regulator, switched capacitor DC-DC converter and charge pump. The power management system contains a maximum power tracking circuitry for controlling PV cell in the maximum power region. By utilizing multi-phase maximum power tracking, we can average the PV cell module output power and provide a constant output power for protecting the rechargeable battery.

Chapter 2 An Overview of Power Management System for Energy Harvesting Applications

This chapter introduces the overview of power management system for energy harvesting applications. The photovoltaic (PV) cell characteristic would be demonstrated in Section 2.1. A maximum peak power tracking system would be introduced in Section 2.2. Section 2.3 and Section 2.4 introduce two different power management systems for solar energy harvesting applications, RF and thermo-generator harvesting applications. Section 2.5 introduces the battery management system for solar energy harvesting applications. Finally, Section 2.6 is the summary.

2.1 Photovoltaic (PV) Cell

The photovoltaic cell converts the light energy into electrical energy. The photovoltaic cell is a nonlinear device which can be represented as a current source model with a PV diode, a shunt resistance (R_{SH}), and a series resistance (R_S), as shown in Fig. 2.1.

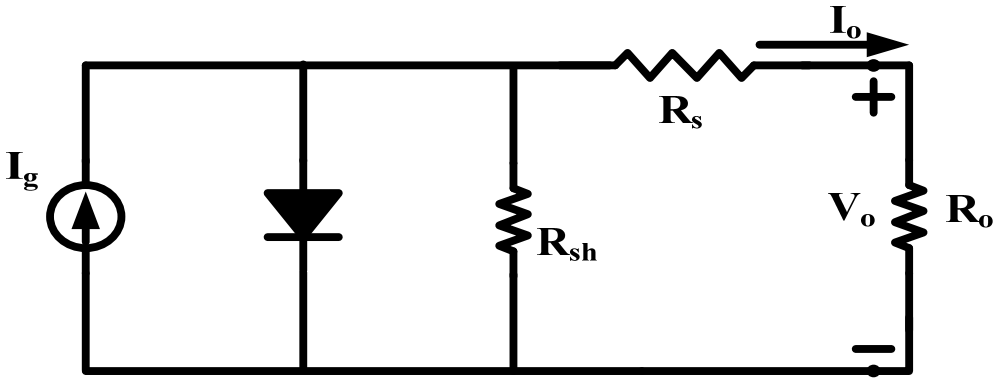


Fig. 2.1 Equivalent circuit of a photovoltaic cell.

The traditional I-V cure characteristic of a photovoltaic cell, while neglecting the internal shunt resistance, is given by the following equation [6]:

$$I_O = I_g - I_{sat}\{\exp[\frac{q}{AKT}(V_O - I_O R_S)] - 1\} \quad (2.1)$$

I_o and V_o describe the output current and the output voltage of the photovoltaic cell respectively. I_g is the generated current for a given solar power, I_{sat} is the reverse saturation current, q is the charge of an electron, A is the ideality factor for a p-n junction, K is the Boltzmann's constant, T is the temperature (K), and R_s is the intrinsic series resistance of the solar array.

According to the following equation (2.2) and (2.3), the saturation current of the photovoltaic cell varies with temperature [6]:

$$I_{sat} = I_{or}\left[\frac{T}{T_r}\right]^3 \exp\left[\frac{qE_{GO}}{KT}\left(\frac{1}{T_r} - \frac{1}{T}\right)\right] \quad (2.2)$$

$$I_g = \left[I_{sc} + K_I\left(T_c - 25\right)\right]\frac{\lambda}{100} \quad (2.3)$$

As shown in (2.2), I_{or} is the saturation current at T_r, T is the temperature of the photovoltaic cell (K), T_r is the reference temperature, E_{GO} is the band-gap energy of the semiconductor used in the solar array. As shown in (2.3), K_I is the short-circuit current temperature coefficient and λ is the solar energy in mW/cm^2. Instead of the I-V characteristic shown in (2.1), the following I-V characteristic equation (2.4) is used to calculate the output voltage of the PV cell:

$$V_o = -I_o R_s + \frac{AKT}{q} \ln\left[\frac{I_q - I_o + I_{sat}}{I_{sat}}\right] \tag{2.4}$$

As shown in (2.4), the electric power generated by a photovoltaic cell varies with the solar radiation value and temperature. Fig. 2.2 shows the I-V and Power-V curve of PV cell under different temperature at I_g=4mA, and Fig. 2.3 shows the Power-V curve of photovoltaic cell under different temperature and current.

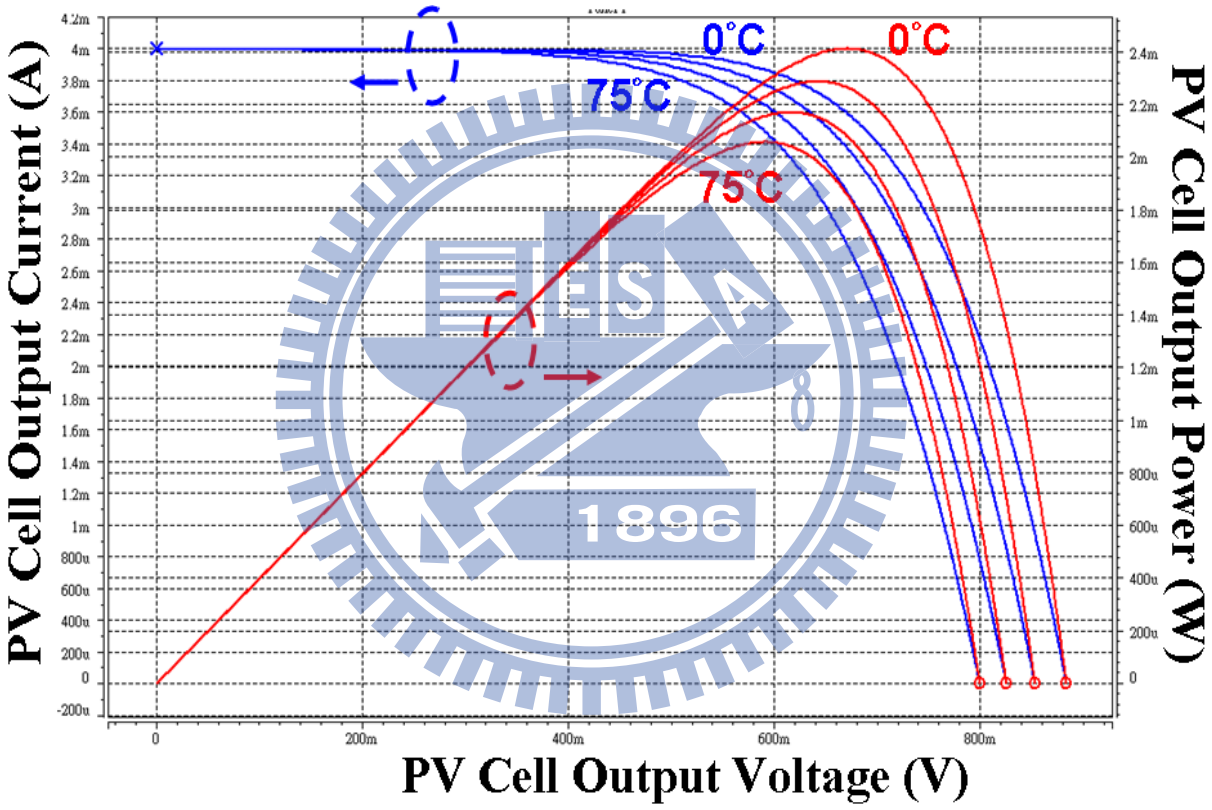


Fig. 2.2 I-V and Power-V curve of PV cell under different temperature at I_g=4mA.

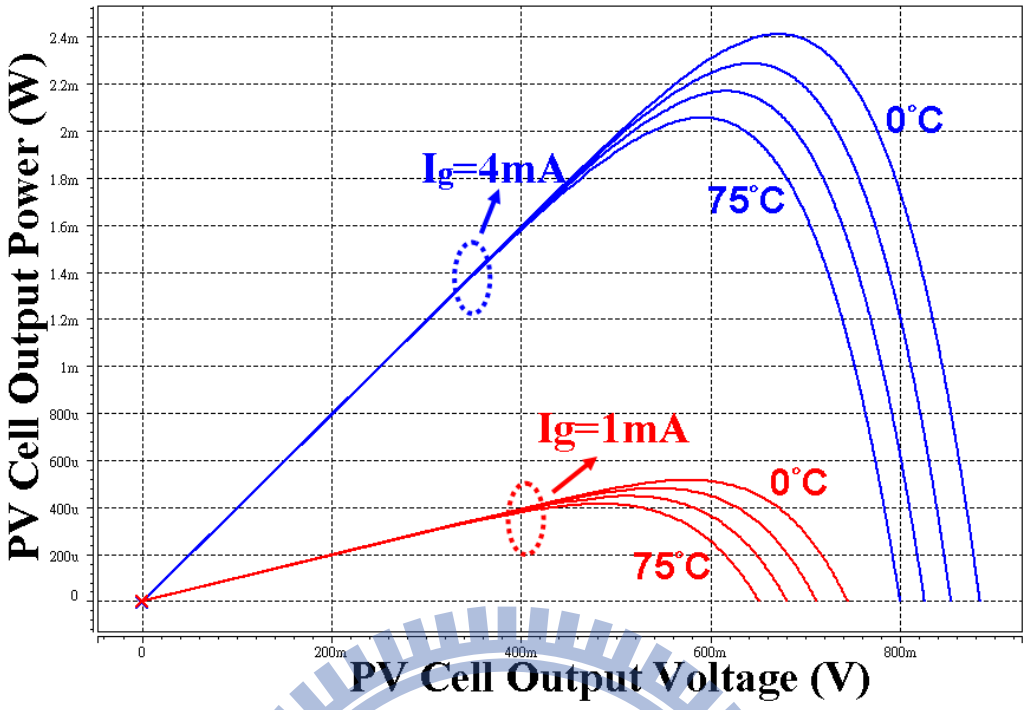


Fig. 2.3 Power-V curve of photovoltaic cell under different temperature and current.

2.2 Maximum Power Tracking and Control Algorithm

2.2.1 Maximum Power Tracking Process

The electrical characteristic of the PV under a given solar energy is described in Fig. 2.4. The PV cell will generate the different output power point either in current source region or in voltage source region which is depended on the different output loadings, where the output current or voltage almost maintains as a constant. The intrinsic impedance of the solar array is low on the right side of the current curve and high on the left side of the current curve. The maximum output power of PV cell occurs at the crossing point of the two regions. The power delivered to the load is the maximum value when the source intrinsic impedance matches the load impedance according to the maximum power transfer theory. So, the impedance shown in the converter side should match the intrinsic impedance of the solar array if the system is controlled to operate close to the maximum power region of the photovoltaic cell.

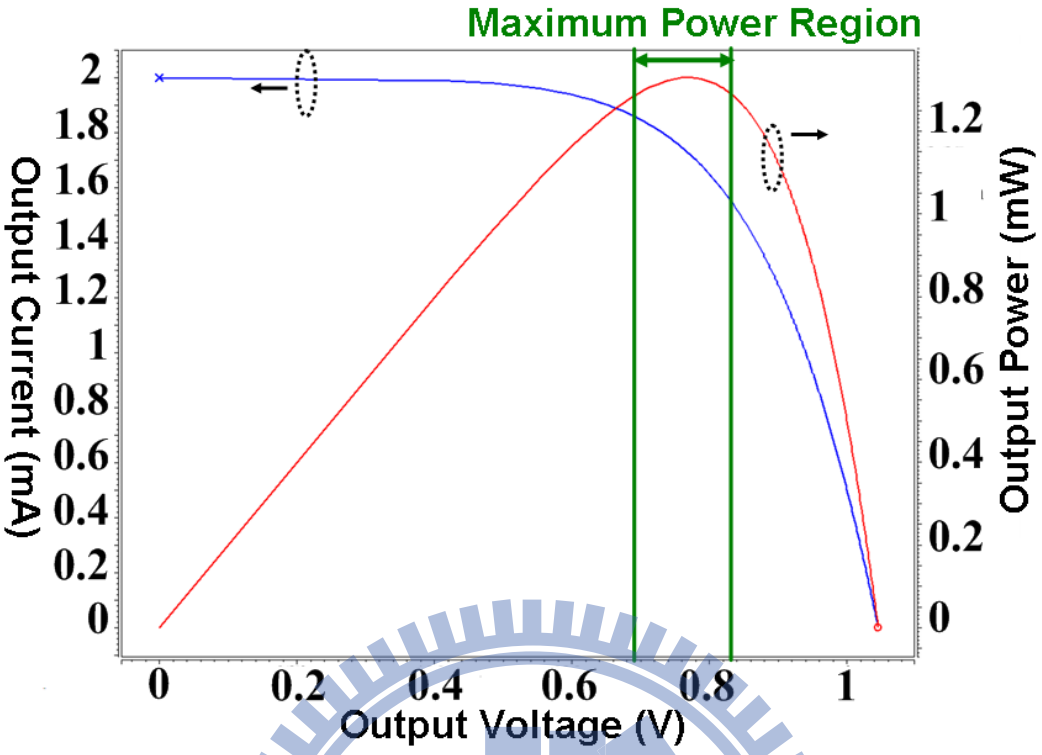


Fig. 2.4 The characteristic curves of PV cell.

In the traditional, most dc/dc converters generate the negative impedance characteristic naturally, through the fact that their current increases when voltage decreases. The behavior is due to the constant input power and the adjustable output voltage of the power supply. If the system generate at the high-impedance (low-voltage) side of the PV cell characteristic curve, the output voltage of PV cell will crash. So, the PV cell is controlled to output at the right side of the curve to perform the tracking process. Otherwise, the converter outputs with the maximum duty cycle, and the output voltage of PV cell is only varied with the given solar energy. Therefore, the system cannot accomplish maximum power tracking and may confuse the present operating point of PV cell for the maximum power point.

Fig.2.5 shows the control flowchart of the maximum power tracking system. When a given perturbation leads to rise in output power of PV cell, the next perturbation is made in the same detection. In this way, the maximum power tracker tracks the maximum power continuously.

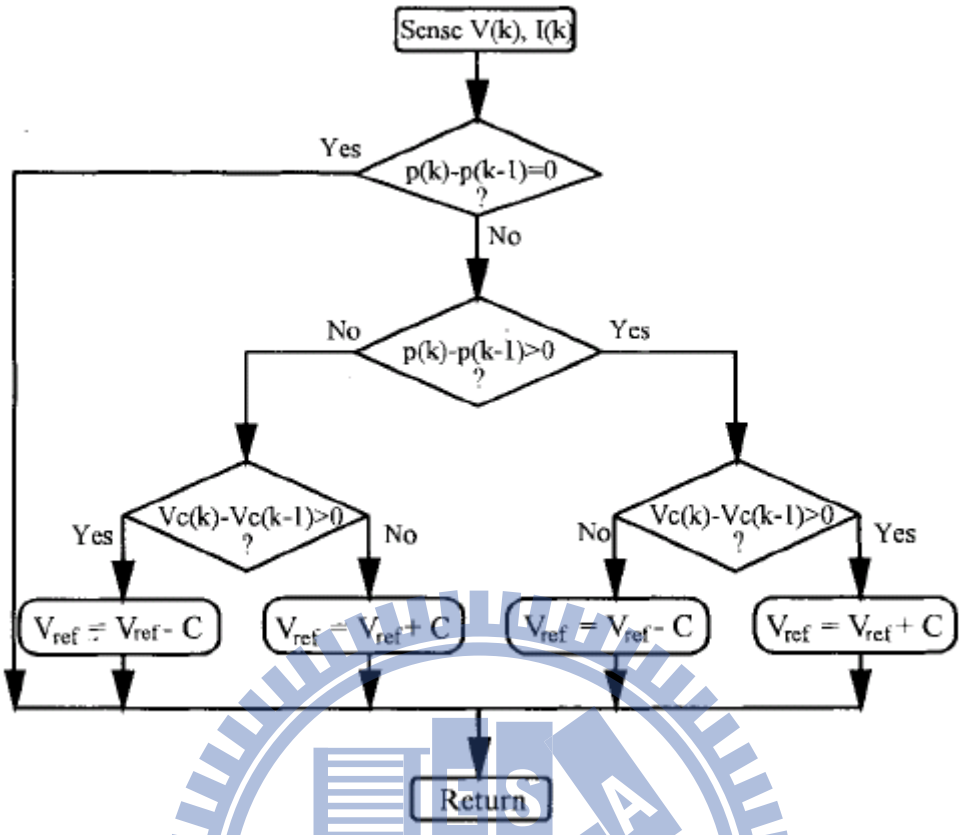


Fig. 2.5 The flowchart of MPT control.

2.2.2 Control Algorithms for Maximum Power Tracking

The perturbation and observation method and the incremental conductance method are control algorithms which are often used to achieve the maximum power tracking. Though the incremental conductance method provides good performance under rapidly changing atmospheric conditions, more sensors are needed to execute the measurements for computations and make decision [7]. While the sensors or the system need more conversion time, the computations will produce the larger amount of power loss. On the contrary, while the sampling and execution speed of the perturbation and observation method is faster, then the power loss of the system will be reduced. Besides, this method only requires two sensors, and reduces of hardware requirement and cost.

Two different control methods are often used to accomplish the maximum power

control [8].

1) Voltage Feedback Control: This method supposes that any fluctuations under the solar energy and temperature of the PV cell are unimportant and that the constant reference voltage is adequate approximation of the true maximum power point. The output voltage of PV cell is used as the control variable for the system. The system maintains the PV cell array operating near its maximum power points by regulating the output voltage of PV cell and matches to a fixed reference value.

The control method is simple, but it has the drawback of neglecting the effect of the solar energy and temperature of the PV cell. This method cannot be widely used to the battery energy storage systems. Hence, the control method is only suitable for using under the constant solar condition, such as a satellite system, because it cannot track the maximum power points of the PV cell when variations in the solar energy and temperature occur.

2) Power Feedback Control: The actual output power of PV cell, for its evaluation from measurements of other quantities, is used as the control variable. Maximum power control can be achieved by forcing the derivative (dP/dV) equal to zero by the power feedback control method. A common approach to the power feedback control is to estimate and maximize the power at the load terminal. However, it maximizes the power to the load, not the power from the PV cell. A converter with MPPT provides high efficiency over a wide range of operating points. The full power may not be supplied to the load completely, due to the power loss for a converter without MPPT. Hence, the design of a high-performance converter with MPPT is a very important issue.

2.3 Ultra Low Voltage Power Management and Computation Methodology for Energy Harvesting Applications

An ultra low voltage power management system for energy harvesting applications is illustrated in Fig. 2.6[2].

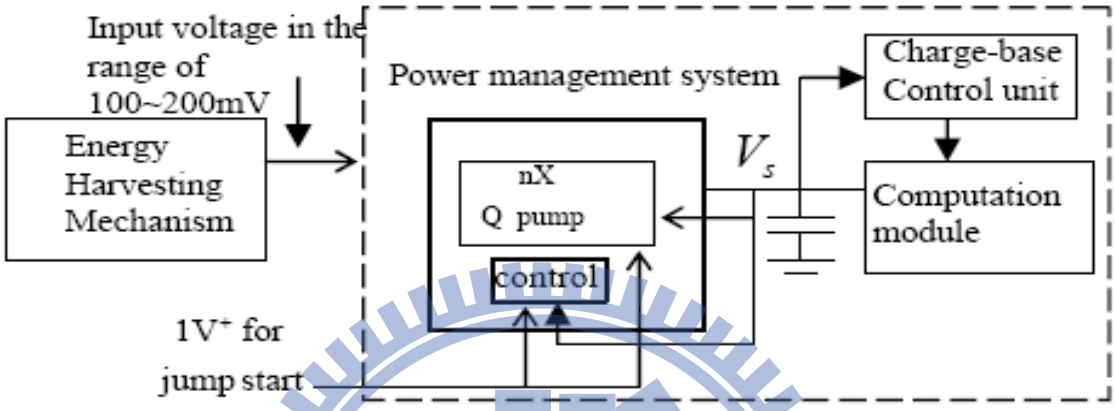


Fig. 2.6 Ultra low voltage power management system for energy harvesting applications.

The ultra low voltage power management system consists of the energy harvesting mechanism, the power management system, the computation module and the charge-based control unit. The environment energy is harvested by the energy harvesting mechanism. The harvested environment energy is transformed into electricity and outputs unregulated voltage.

In this application, the range of output voltage which is harvested from the energy harvesting mechanism is 100mV~200mV. The harvested energy generates unregulated voltage and supply to the source of power management system. There is a charge pump in the power management system. And the charge pump pumps up the voltage to more than 1V for the system. The unregulated voltage (Vs) supplies the controller to let the charge pump is self-powered after it is jump-started. The jump-start circuit is a battery to apply energy during the system is start-up, and be open from the source of the system while the system is self-powered operation. The

unregulated voltage (Vs) supplies the computation unit directly for the cost consideration. Hence the supply voltage fluctuation will impact on the computation unit. The energy is insufficient to maintain continuous computation operation by the impact of the unstable input source energy. The charge-based control unit insures that the energy is sufficient for a step operation of the computation and triggers the calculation operation while enough energy is available.

2.3.1 Power Circuit

The power circuit of this power management system shows in Fig. 2.7[2]. The power circuit has a four stage 16x exponential charge pump circuit, and a clock generator. Because of the voltage source V_{in} is around 80mv~200mv, the circuit needs a start up circuit to trigger the system which is only need to operation at the starting of the circuit operating. When the circuit is triggered, the generated high voltage source V_{out} will supply the harvested power to the clock generator and open the switch between the start-up voltage and the circuit. An energy loop is created to let the circuit is self powered and supplies harvested power to the outside circuit.

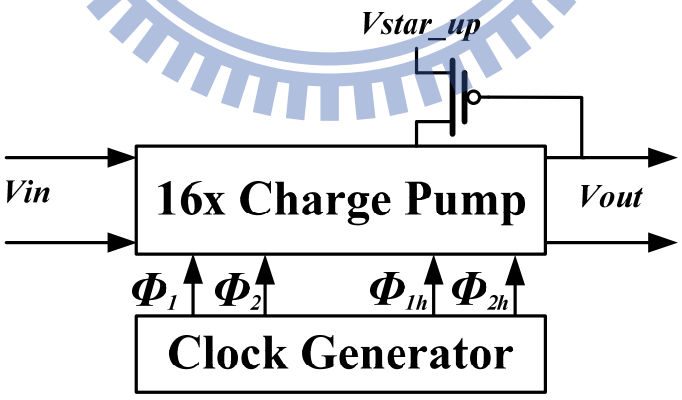


Fig. 2.7 Block diagram of the power circuit.

Two different clock phases are used to drive the charge pump: (φ1, φ2) and (φ1h,φ2h). The signal generator shows in Fig. 2.8[2]. For saving energy, all the inverters in the generator for (φ1, φ2) except for the last one of the buffer stage, has to

be swing between Vdd and Vin. The generator for (φ1h,φ2h), the conventional level shifter is removed and a CMOS inverter create a driving signal swing between 2Vout and 4Vin. By doing so, the clock swing is lower and the energy can back to some nodes in the charge pump circuit which can save more energy.

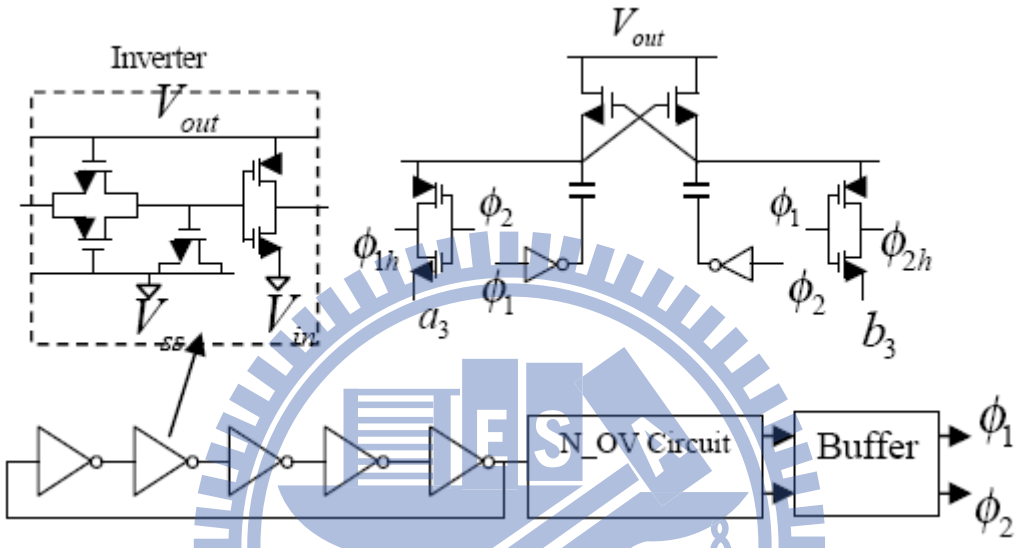


Fig. 2.8 Clock generator.

2.3.2 Computation Module

The unregulated supply voltage impacts the delay of the circuit and will make the timing problem for the operation function. Hence if the computation unit can check the supply voltage variation and adapt the performance of the digital circuit automatically to prevent for the wrong operation will be a good solution. A self-time asynchronous pipeline design [9] is carried out for the computation module. The function of a pipeline stage is only dependent upon the completion of the previous stage, but not reliant the global clock. It is more robust under the voltage variation operation conditions for its previous staged generated timing signals and it is more fitting for the design to track with an unregulated supply voltage. To make easier the

asynchronous hand-shaking protocol and to serve for the static CMOS library, the asynchronous pipeline is implemented by the bundle delay method. The bundle delay is a little bit larger than the computation delay with a safety margin for the voltage variation operation. When the supply voltage is unregulated, the bundle delay will automatically track the change and synchronize the operation in the pipeline. This can tolerant a large variation in the supply voltage.

2.3.3 Charge-Based Control Unit

Because of the variation of the voltage source, sometimes the energy available at a special time interval may be insufficient for a certain operation and if system is running the computation, the computation may be unfinished and the data will be lost when the voltage drops to a lower level. Considering for this situation, a charge-based computation methodology is used. The charge required at different voltage levels for is sure for a certain step operation. The certain step operation refers to a computation which results in data and stores in the memory, or outputs to external device and not to be used again. The certain step operation will only be started when the scavenged power can supply the charge for it with some energy margin. For some ultra low power applications, such as ultra low power wireless sensor device, the computation can operate at a very long clock cycle. The system can make a decision whether an operation could be triggered and executed based on the energy available. Besides, the computation can be prioritized in task level or bit level. Depending on the energy available, different computations will be carried out by depending on the judgment of the charge-based control unit.

2.4 A Micro-Power Management System with Maximum Output Power Control for Solar Energy Harvesting Applications

The micro-power management system with maximum output power control for solar energy harvesting applications shows in Fig. 2.9[3].

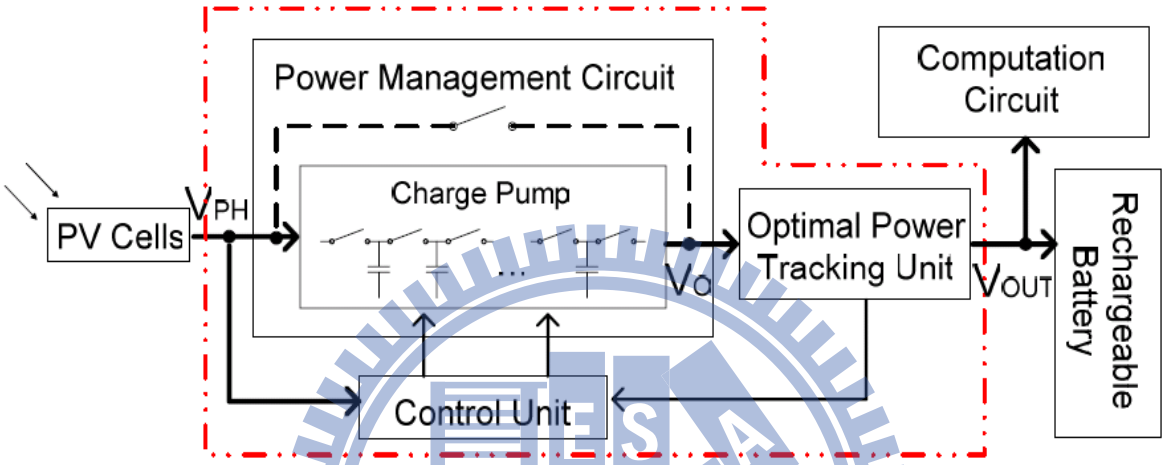


Fig. 2.9 Block diagram of micro-power management system with maximum output power control for solar energy harvesting applications.

By providing energy for different solar energy, the micro-power management system adjusts the voltage of the PV cells and the battery to make the decision whether the charge pump is used or directly bypassed. Under low solar energy, the PV cell output voltage is low and the charge pump pumps up the voltage either for charging the rechargeable battery or providing energy to the computation circuit. At this moment, the optimal power tracking unit checks the charge pump output power and decides the adjustment of the system operating parameter. Depending on the adjustment decision, the control unit adjusts the operating frequency of the charge pump for maximize the power management system output. Rechargeable battery is used to provide the system continuous energy even while the light source is not sufficient.

2.4.1 Optimal Power Tracking Unit

For supplying maximum power to charge the battery or to directly supply the computation circuit, the optimal power tracking unit is applied to monitor the amount of power flowing out of the charge pump. The detail circuit is shown in Fig. 2.10[3].

The optimal power tracking unit monitors the output power of charge pump and generates the adjustment decision for the decision switching frequency of the charge pump so that make the system is operating around the optimal output power point. The optimal power tracking unit contains the current sensing circuit and the decision generation circuit. Since the system output voltage is regulated by the battery and the voltage of the battery which is equivalent a large capacitor changes the voltage very slowly, therefore, maximizing the output power of the system is match to maximizing the system output current. The circuit utilized current sensor to measure the charge pump output current. Depending on the measured current value, the tracking unit decides whether the system is at the optimal point and supplies the corresponding decision signal to adjust the system parameters. The generic hill climbing algorithm is utilized in the circuit for the optimal point tracking. The switching frequency of charge pump adjusts the system output current. Therefore the tracking unit supplies the corresponding voltage value to adjust the switching frequency by the VCO which is in the control unit. A current sensor consists in the tracking unit. By the biasing current sensed through MN_1 and MN_2, the source voltages of MP_3 and MP_4 are clamped at the same voltage condition. While the current sensor power supply V_O is linked to the charge pump output due to the size ratio of MP_1 and MP_2, about 1/N of the total charge pump output current flows to the resistor R_S by the transistor M_S. Therefore the output current level from the charge pump is converted by the voltage drop across R_S (V_S), which is then delivered to the decision generation circuit. The

rest of the charge pump output current would charge the battery or the computation circuit through MP_2 at node V_{OUT}. While the output current from the charge pump is in pulse shape, a smoothing capacitor is connected to the node V_O to obtain a smooth current profile for the accurate measurement of the average value of the output current through the current sensor. The sensed current which is represented by the value of V_S, is delivered to the decision generation circuit to operate the generic hill climbing algorithm. By comparing the current sensed current value with the previous one, the circuit can decide the direction of the change in output current and determine the decision on whether to increase or decrease the charge pump switching frequency. This operation continues and the charge pump output current will oscillate around the maximum current point eventually. In the decision generation circuit, the current detects V_S value and the previous V_S value is stored in the sample capacitors, C_{PP1} and C_{PP2}, alternatively. While C_{PP2} holds the previous value, the transmission gates circuit T_3 and T_4 are off while T_1 and T_2 are on. The current sensed V_S will be stored in C_{PP1}, and V_{check} will output the comparison and detection results from V_{O+} of the comparator. V_{check} is equivalent to logic '1' when the current sample value is larger than the previous sensing value. In the next sample period, T_1 and T_2 will be turned off while T_3 and T_4 are on, and C_{PP1} holds the previous sample while C_{PP2} stores the current V_S value. V_{check} will output the comparison and detection results from V_{O-} for this sample period. This value is XNORed with the previous detection decision which is kept in a D-flipflop and the new adjustment value V_{action} will be reset at the rising edge of the control pulse S_E. The logic control value of the decision signal V_{action} determines whether to increase or decrease the charge pump switching frequency. Relying on the V_{action} logic value, the capacitor C_{VCO} is either charged by the control current i_{b2} through transistor ME_1, or discharged by the current i_{b2} through transistor

ME_4, during the control pulse interval of S_E. In this way, the voltage of V_{VCO} is either increased or decreased and it is then delivered to the control unit to control the charge pump switching frequency through the VCO.

For considering reduce the power overhead, the optimal power tracking unit operation is partition into three different phases during each sample period, which shows in Fig. 2.10. Thus, the sample period demonstrates the time interval between two continuous frequency adjustments. During each period, the transmission gate control signal S_{PP} is either high or low, which decides whether the previous sampled V_S or the current one should be stored in C_{PP1} or C_{PP2}, and whether V_{O+} or V_{O-} of the comparator will output the detection results. Later than each frequency adjustment, the tracking unit is turned off so that all the charge pump output current can flow to V_{OUT}. This describes as the normal working phase. At the end of the normal working phase, sensor control signal S_S will trigger the optimal power tracking unit where the charge pump output current is sensed and the current changing is checked at node V_{check}. This indicates as the sensing phase. After some delay, the tracking unit goes into the evaluation phase in which a pulse S_E is generated. Decision signal is reset in the D-flipflop and the capacitor C_{VCO} is charged or discharged through the S_E pulse interval according to the generated decision. After the operation as described before, the power checking unit is turned off and the operation returns back to normal working phase again.

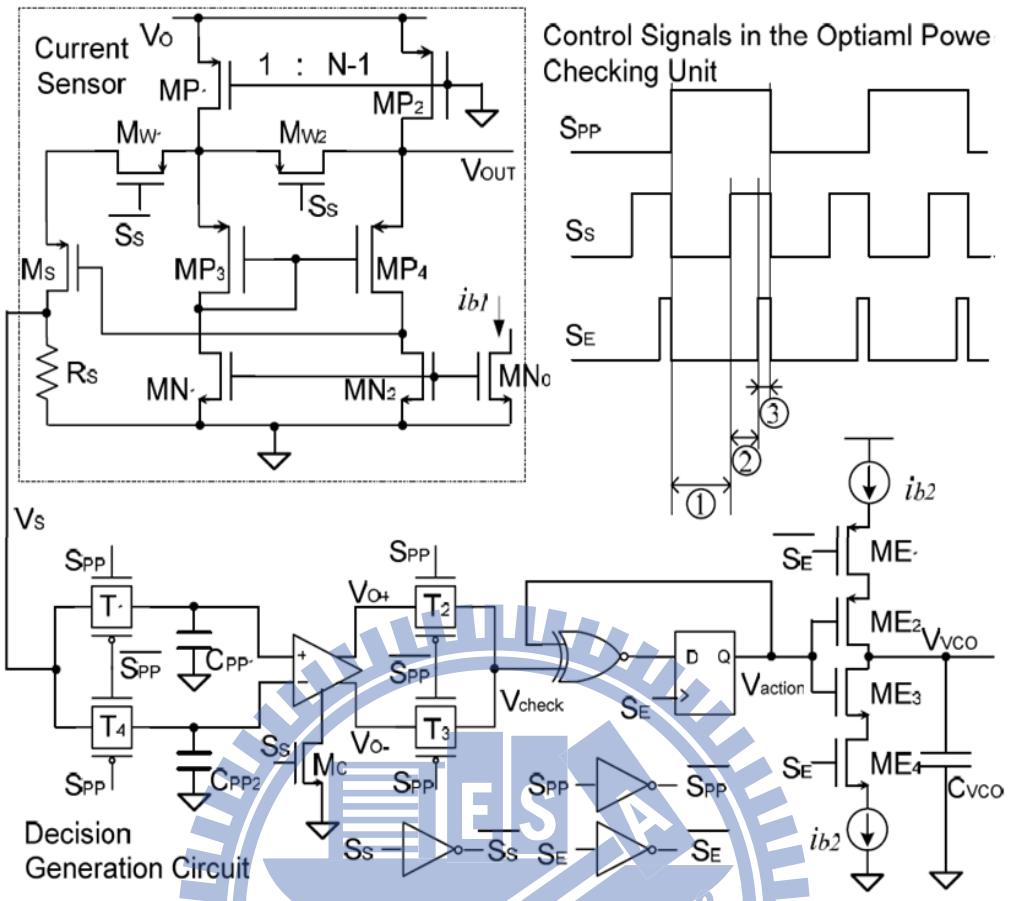


Fig. 2.10 Circuit of the optimal power tracking unit. (①normal working phase, ②sensing phase, ③evaluation phase)

2.4.2 Control Unit

The control unit is utilized to adjust the system operating parameters depend on the determination from the optimal power tracking unit in order to maximize the output power from the charge pump. The charge pump switching frequency has an intense effect on the system output power. A VCO is utilized in the control unit to provide a variable frequency clock. The circuit structure is shown in Fig. 2.11[3]. V_{VCO} is the output detection signal from the optimal power tracking unit which determines the charge pump switching frequency to be outputted through the inverter chain I_1~I_4. A positive edge-triggered D-flipflop resets the clock duty cycle and then delivers the clock signal to the charge pump. For achieving good power transfer efficiency, the

power consumption of the control unit should be minimized. Therefore, the currents of the amplifier branches and the VCO branches should be carefully controlled. Besides, because of V_F varies around the threshold of the inverter I_1, the short circuit current of I_1 is larger than other inverters. For reducing the current loss, the I_1 is carried out in small size. True Single Phase Clocked (TSPC) register is utilized for the D-flipflop in order to reduce the number of transistors and also its power consumption.

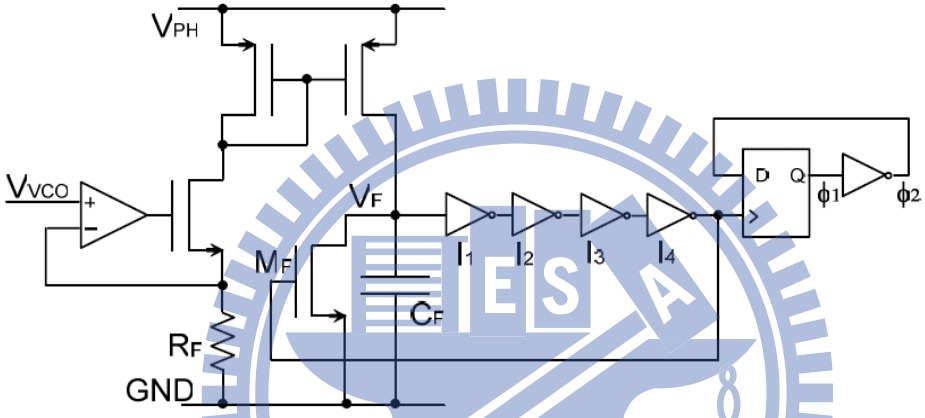


Fig. 2.11 Control unit for the charge pump.

2.5 A Battery Management System for Energy Harvesting Applications

A battery management system for energy harvesting applications is shown in Fig. 2.12[4] which is contained of RF and thermoelectric. A micro-battery utilized as storage unit and power supply manager to convert and control the harvested energy and interface the micro-battery. Both sources are controlled by the ASICs: the micro-battery being charged either using thermal energy scavenged by the thermo-generator associated with the DC/DC converter or using external RF power transferred by the RF converter. The situation of charge of the storage device is monitored periodically.

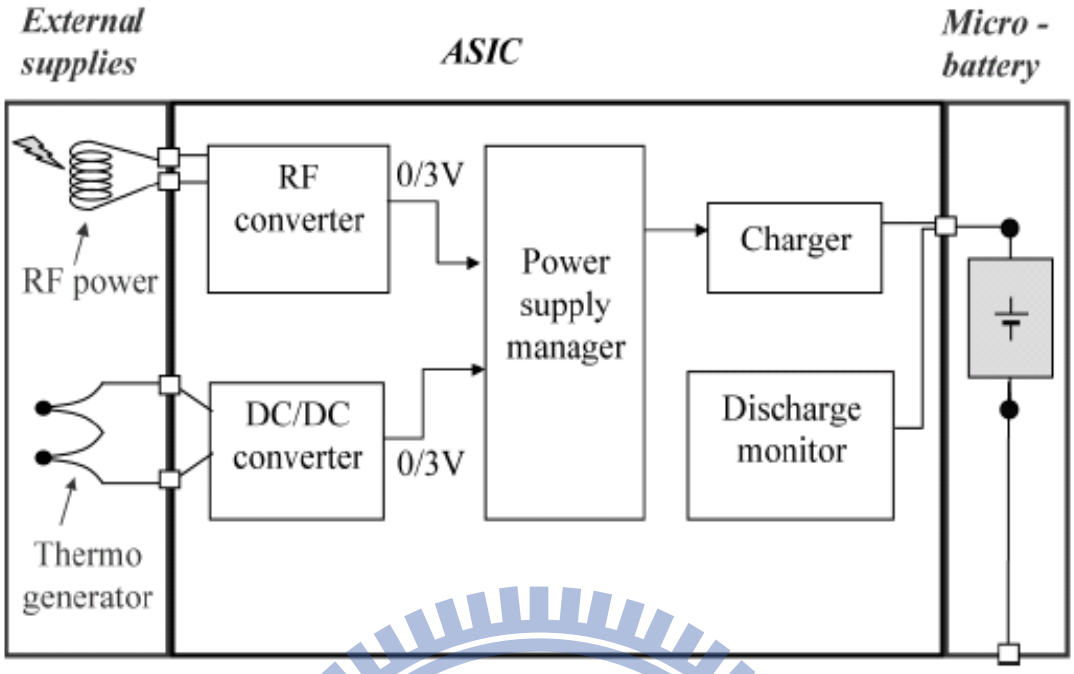
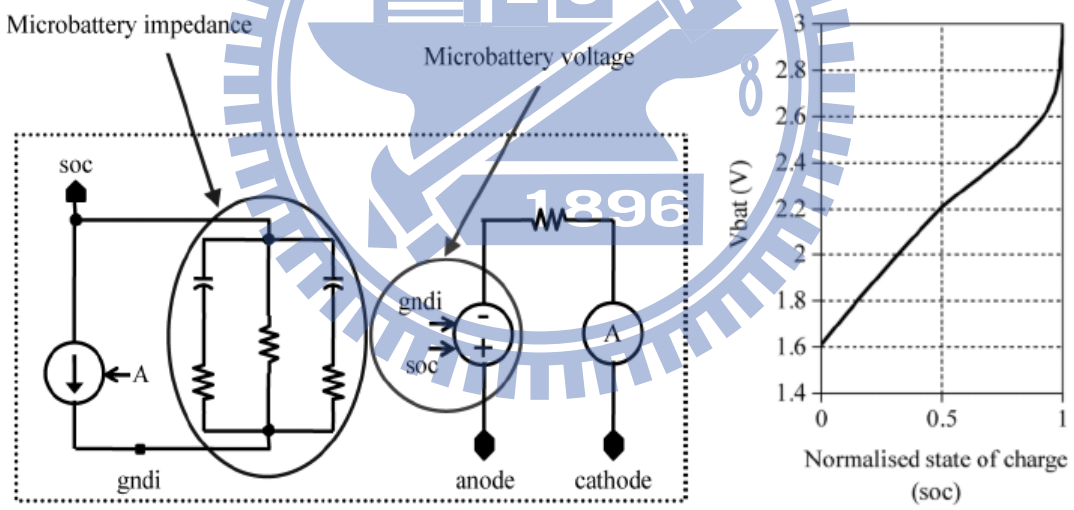


Fig. 2.12 The battery management system for energy harvesting applications.



(a) (b)

Fig. 2.13 (a) Microbattery electrical model. (b) Normalized state of charge.

2.5.1 Thin-Film Solid-State Battery Electrical Model

The circuit model of micro-battery is shown in Fig. 2.13(a) [4]. The voltage-dependent generator generates the micro-battery voltage which is based on a table. The model has two outputs reproducing the battery state of charge and the

voltage across the battery. The normalized state of micro-battery charge voltage is shown in Fig. 2.13(b) [4].

2.5.2 Micro-battery State of Charge Monitor

The micro-battery state-of-charge monitor is provided energy by the micro-battery itself for ensuring permanent monitoring. The state-of-charge monitor should also be resistant to supply voltage fluctuations to be congenial with the micro-battery. The state-of-charge monitor shows in Fig. 2.14[4]. The monitor detects voltage of battery to a reference voltage and sets the digital soc flag signal to “low” level when the micro-battery is discharged.

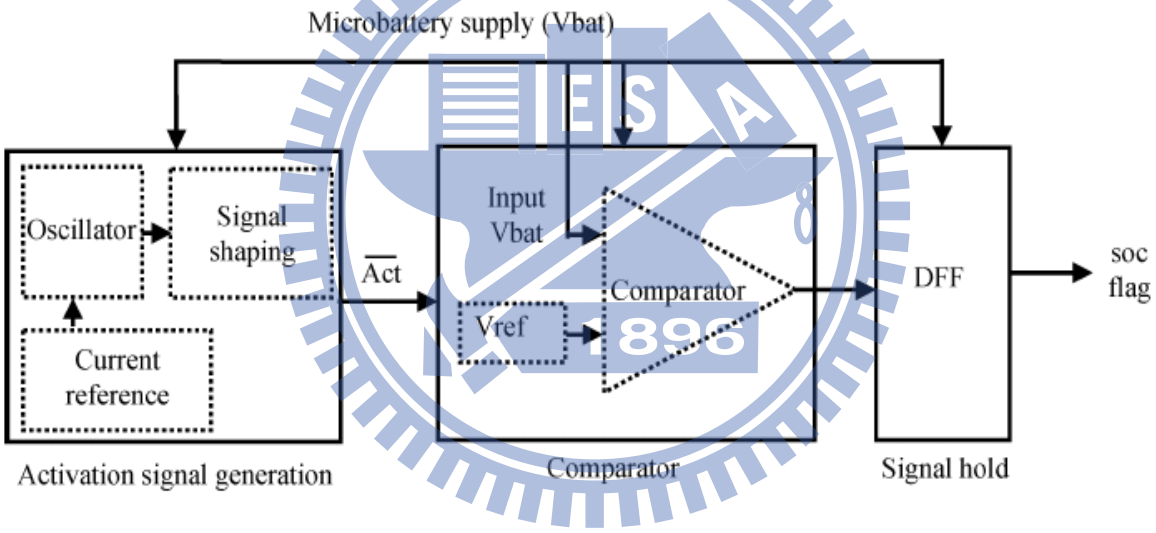


Fig. 2.14 Sate of charge monitor architecture.

For achieving ultra low power consumption, the comparator is periodically triggered, only for one second every hour and a half. This sampling rate is enough because of the micro-battery lasts for about one year for the visualized low duty-cycle applications. The comparator is demonstrated in Fig. 2.14[4], as well as the circuit which sends the comparator control signal, and a last circuit which just keeps the comparator output value when the comparator is turned off.

2.5.3 Power Supply Manager and Battery Charger

The micro-battery could be charged by the thermo-generator's DC/DC output or by the RF converter. Hence, the power supply manager, containing a specific unit along with an asynchronous finite state machine, controls priority between the two sources when they are simultaneously appears and triggers self-powered micro-battery protection avoiding the case of external power source interruption. The micro-battery charge control circuit architecture is demonstrated in Fig. 2.15[4]. The power supply manager provides an internal power supply V_{DD} from the two external sources. This V_{DD} supply is used by the micro-battery charge controller to provide a constant current for the micro-battery charge. The power supply manager also generates an internal power supply Vmax defined instantaneously by the maximum voltage between V_{DD} and V_{bat}. Therefore, this power supply Vmax is steady while using as small power as possible from the battery. It is used to trigger micro-battery protection avoiding inconveniently discharge in case of external power source interruption.

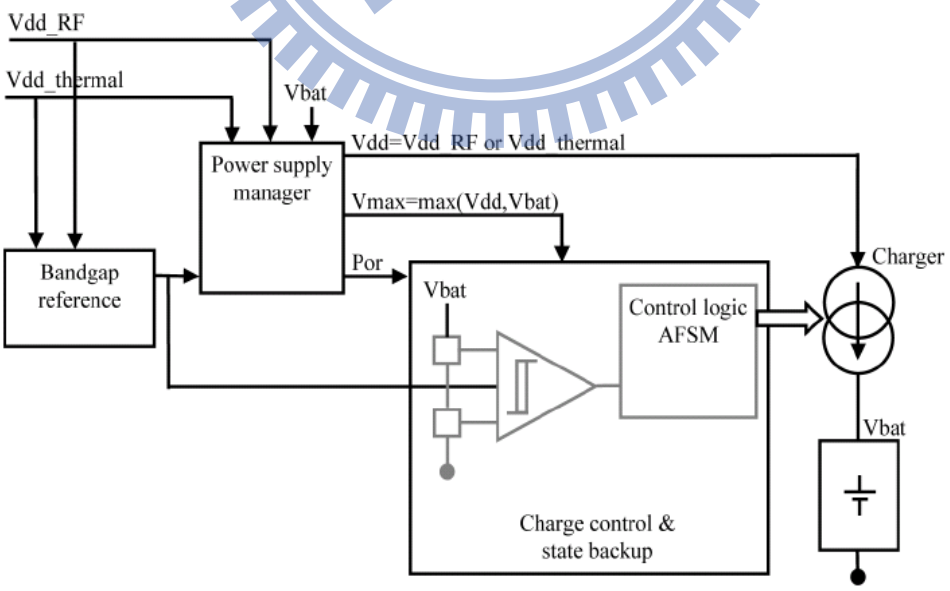


Fig. 2.15 The architecture of micro-battery charge control circuit.

2.5.4 A Battery Management System to Increase the Service Life of Battery

From above section description, there are many power management systems for energy harvesting applications which are combined with a rechargeable battery to maintain the overall source power of the system and make the system can work without the harvesting energy source input. The issue of the harvesting power source is that the power source is unregulated voltage source and can not for charging batteries by a constant voltage. Without the control mechanism, the batteries are usually discharged and it is not possible to assure an optimum charge or discharge cycle. The poor charge or discharge cycle may result in reduction of battery life time. A battery management system is used to avoid the battery from repeatedly overcharged or undercharged. The battery management system is shown in Fig. 2.16[5].

The battery charging method is a very significant factor in extending the life time of the battery in an energy harvesting system. A charge control mechanism is demonstrated in Fig. 2.17[5]. The charge controller has different operation points. The operation points avoid the battery from being overcharged or over-discharged.

1) VR: The voltage regulation operation point limits the maximum voltage that the battery can reach (opens the connection of battery from the array).
2) ARV: The array connects voltage operation point again and gives the voltage at which the battery and array are reconnected.
3) LVD: The low voltage disconnects operation point gives the point at which the battery is disconnected from the load to avoid over-discharged.
4) LRV: The load reconnect voltage operation point gives the voltage at which the load is reconnected to the battery

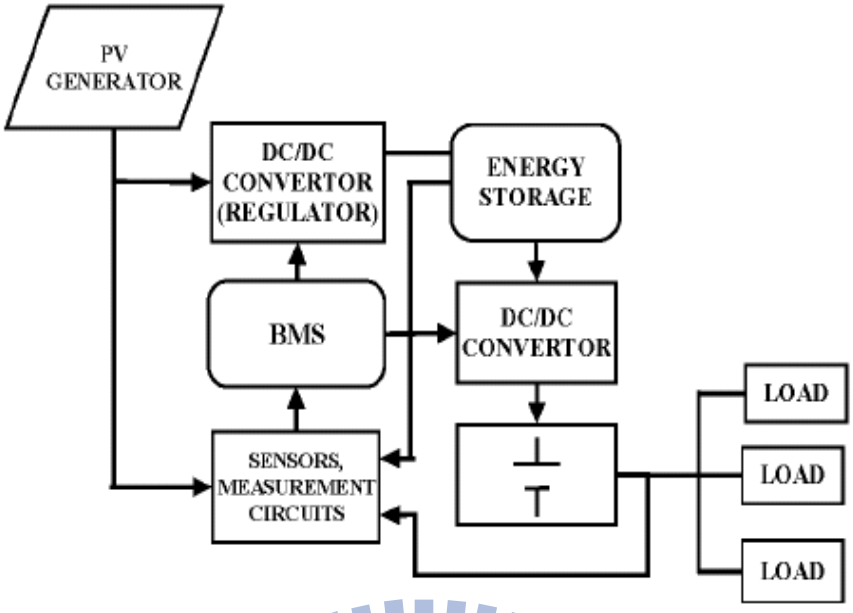


Fig. 2.16 Battery management system with charge controller.

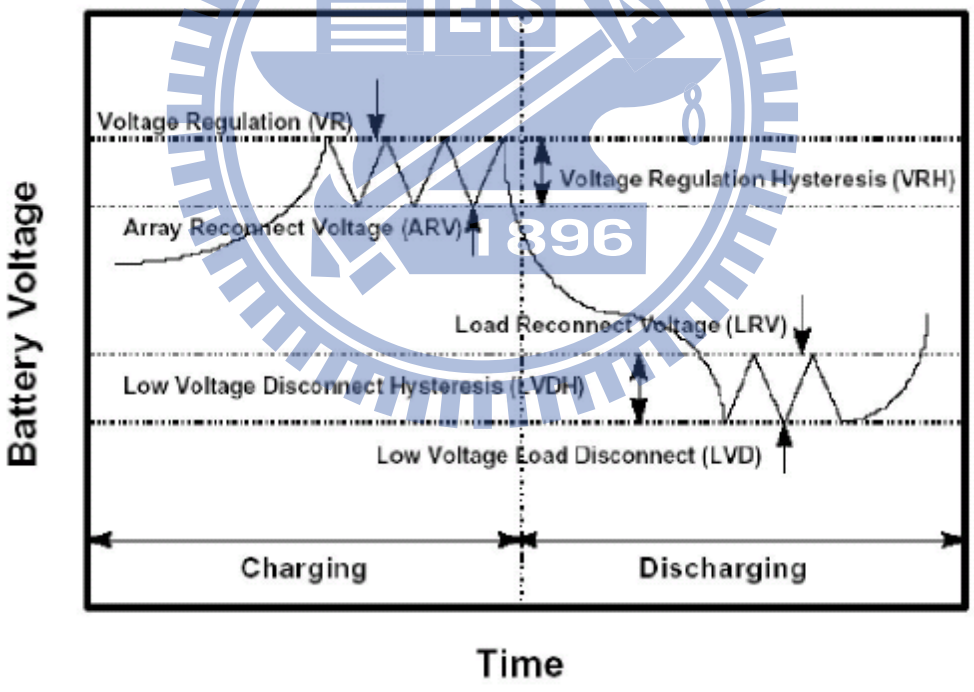


Fig. 2.17 Charge controller set points. [6]

2.6 Summary

In this chapter, the characteristic of PV cell is defined and its circuit model of PV cell is also described. A maximum power tracking technique is used for PV cell. The MPT controller senses the output voltage and current of PV cell and controls the reference voltage of dc/dc converter to keep the PV cell operating in maximum power.

For ultra-low voltage energy scavenging application, a power management system with a small battery for jumping start is described as mention before. The power management system also included a low power clock generator to generate the clock phases for a four stage 16x exponential charge pump circuit. Because of the unpredictable power source and unregulated output voltage, the power management used a charge-base control unit to avoid the computation error.

A charge pump is generally used for solar energy harvesting applications. For efficiency consideration, a micro power management system with maximum output power control is carried out. The system included an optimal power tracking unit to monitor the charge pump output power and made the adjustment decision for the charge pump switching frequency so that the system was working around the optimal output power point.

The battery management system for energy harvesting applications converts the RF power and the thermo-generator power to the micro-battery. The charge monitor is implemented to extend battery operation time and preservation of harvesting energy. The power supply manager detects the usage source is from RF power or from thermo-generator to charge battery. And a battery management system for battery charge method is utilized to avoid overcharged and undercharged for extending the service life time of battery.

Chapter 3 Switched Capacitor DC-DC Converter and Voltage Regulator

The switched capacitor (SC) DC-DC converter and the voltage regulator are composed of a comparator (or an OP amp.), reference voltage generator (or digital to analog converter for dynamic voltage generation) and an output MOSFET. The ideal voltage regulator is low dropout voltage, low quiescent current, good loading capability and small output transient undershoots and overshoots.

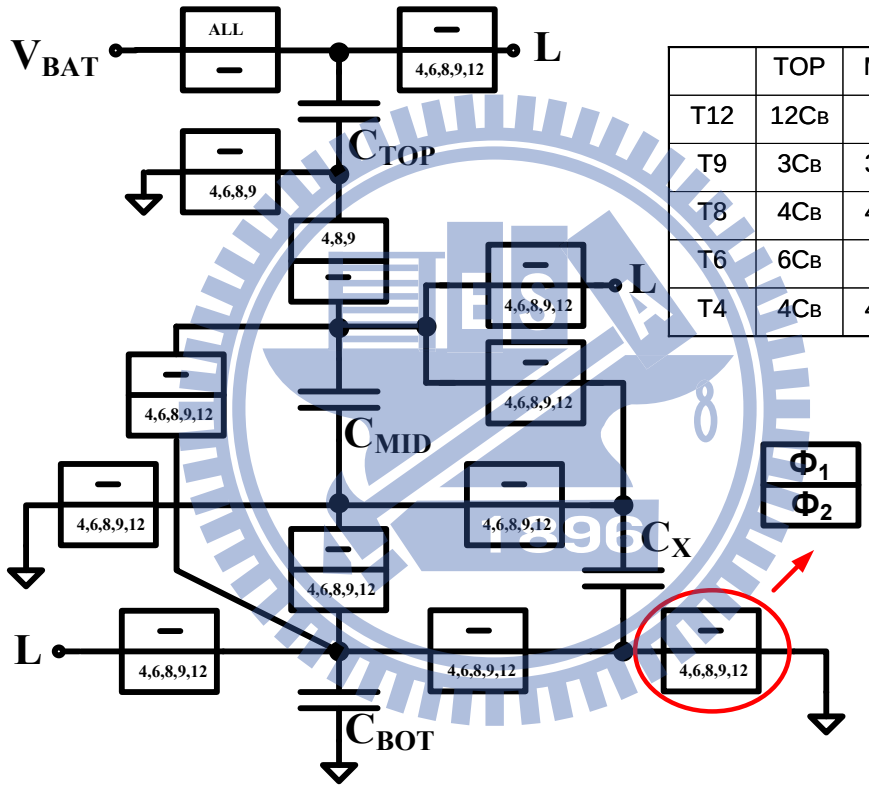
For providing high output current, the transfer MOSFET must be very large. So, the transfer MOSFET will have the large gate capacitor. This will cause stability problem and increase driving power. For archiving high-precision output voltage, a high open loop gain is required. But the phase margin is sacrificed when loop gain is too high and cause regulator unstable. Fast transient response is related to slew rate at the gate drive of the power transistor and the open loop-gain bandwidth. This can be improved by a high slew-rate buffer and advanced frequency compensation technique.

In this Chapter, the techniques of conventional switched capacitor DC-DC converter is explained in Section 3.1, the techniques of improving stability of voltage regulator are illustrated in Section 3.2. A linear regulator using digital buffer is introduced in Section 3.3. The switched capacitor DC-DC converter and voltage regulator is described in Section 3.4. All results are simulated in UMC 90nm CMOS technology model.

3.1 Conventional Switched Capacitor DC-DC Converter

3.1.1 Conventional Structure of Switched Capacitor Matrix

Fig. 3.1 is shown a conventional structure of switched capacitor matrix [42], a multiple-gain DC/DC converter which is used four flying capacitors, C_{TOP}, C_{MID}, C_{BOT} and C_X for delivering charges from the input voltage to convert different output voltages. And the four flying capacitors are large values, and total size is 2.4nF.



	TOP	MID	BOT	X
T12	12C_B	—	—	—
T9	3C_B	3C_B	3C_B	3C_B
T8	4C_B	4C_B	4C_B	—
T6	6C_B	—	6C_B	—
T4	4C_B	4C_B	4C_B	—

Fig. 3.1 Switched capacitor matrix of conventional structure.

The box shown in Fig. 3.1 is representative of a switch which is turned ON depending on the topology in use and the phase of the clock, which are implemented by using N type or P type MOS transistors. The controlling signals of transistor switches are generally using clock signals to control the connections of the flying capacitors by turning on or turning off the transistor switches. When the switch is closed, the resistance of switch is called switch-on resistance. In order to minimize the

energy dissipated in the switch-on resistance, the transistors switches are designed to have a very large ratio of W over L, where W is the gate width and L is the effective gate length. But the very large W makes the dynamic power of control signals increasing and decreases the total conversion efficiency. Therefore, the size of W and the conversion efficiency are trade off.

3.1.2 Conversion Gain Configurations

The operation of switched capacitor matrix is able to provide five different common phases and gain phases, with the gain being the ratio of the output voltage V_{out} to the input voltage V_{in}. The equivalent circuits of these conversion phases are shown in Fig. 3.2 [42].

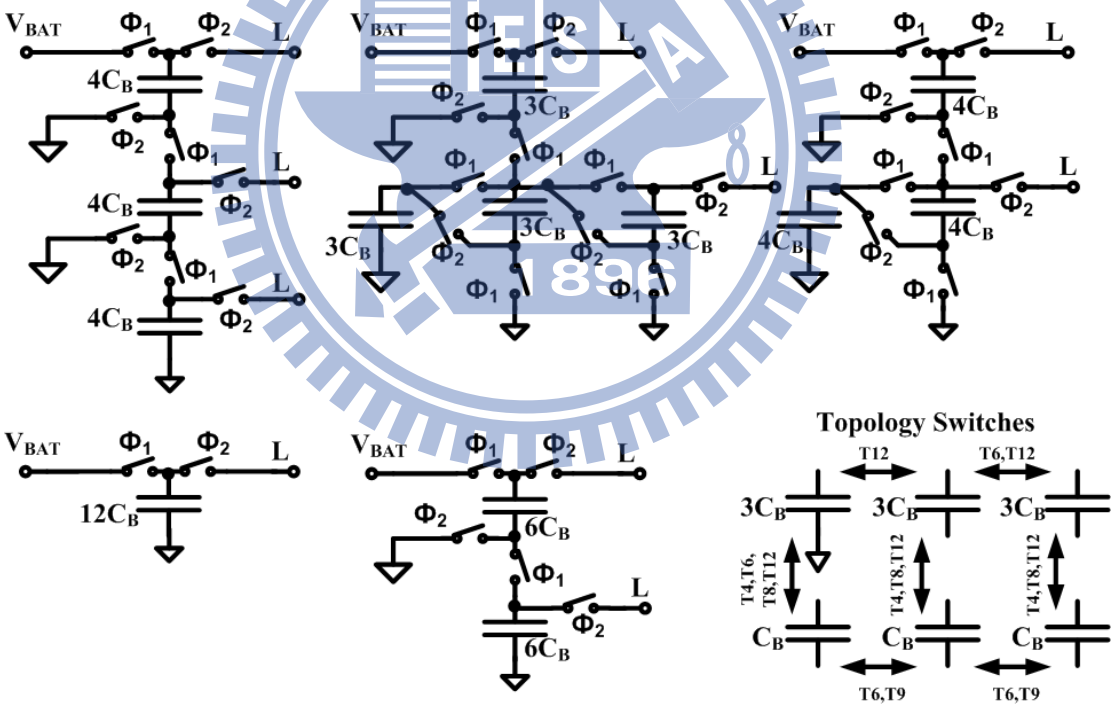


Fig. 3.2 Topologies used to generate a wide range of load voltages from a 1.2V supply.

In these configurations, there are four gain configurations referred as buck stages whose gains are less than 1 and one gain configuration referred as unit gain with gain equal to 1. According to the input and the output, the DC/DC converter is divided to

step-down type or buck type converter ($V_{out}<V_{in}$).

While the converter is clocked and the gain setting is chosen, the switched capacitor matrix is switched between the common phase and the chosen gain phase to transfer charges from the input to the output to keep the chosen output voltage. The gain configuration of 1/2 is used as an example to explain the implementation of gains through the switched capacitor matrix. The equivalent circuit of gain configuration of 1/2 is shown in Fig. 3.3[43] below. The flying capacitor C_f is used to store and transfer energy, and capacitor C_h is the hold capacitor for the output.

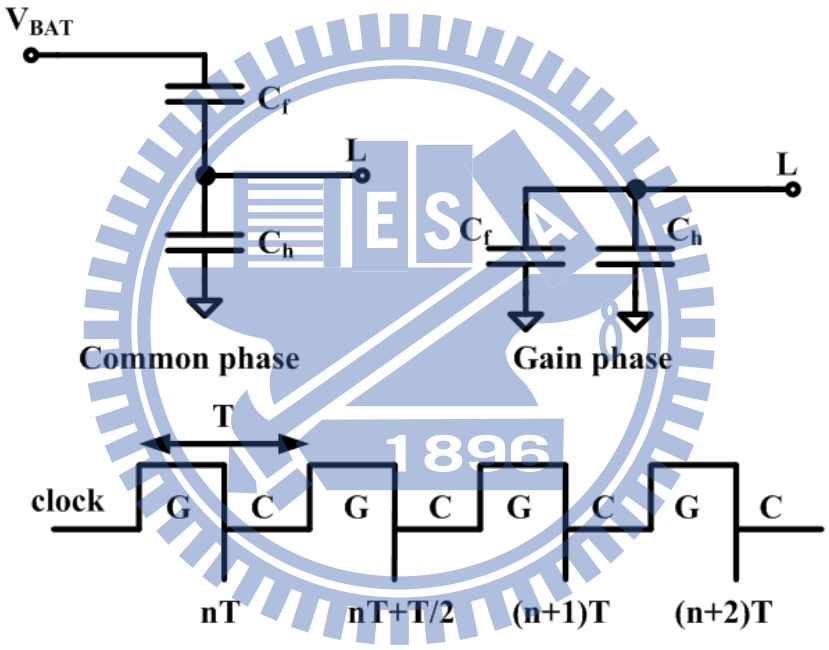


Fig. 3.3 Equivalent circuit of the gain configuration with gain of 1/2.

At time nT, the switched capacitor stays at the end of the gain phase, and the charges in the capacitors C_h and C_f are

$$Q_{ch}(nT) = C_h \bullet V_{out}(nT) \tag{3.1}$$

$$Q_{cf}(nT) = C_f \bullet V_{out}(nT) \tag{3.2}$$

At time nT+T/2, the charge pump stays at the end of the common phase, the

charges in the capacitors Ch and Cf are

$$Q_{ch}(nT+T/2)=C_h \bullet V_{out}(nT+T/2) \tag{3.3}$$

$$Q_{cf}(nT+T/2)=C_f \bullet [V_{in}-V_{out}(nT+T/2)] \tag{3.4}$$

According to the theory of charge conversation, we have

$$Q_{ch}(nT+T/2)-Q_{cf}(nT+T/2)=Q_{ch}(nT)-Q_{cf}(nT) \tag{3.5}$$

Solving Equation (3.1) (3.2) (3.3) (3.4) and (3.5) results in

$$V_{out}(nT+T/2)=\frac{C_f}{C_h+C_f}V_{in}+\frac{C_h-C_f}{C_h+C_f}V_{out}(nT) \tag{3.6}$$

$$Q_{ch}(nT+T/2)=C_h \bullet \frac{C_f}{C_h+C_f}V_{in}+C_h \bullet \frac{(C_h-C_f)}{C_h+C_f}V_{out}(nT) \tag{3.7}$$

$$Q_{cf}(nT+T/2)=C_h \bullet \frac{C_f}{C_h+C_f}V_{in}-C_f \bullet \frac{(C_h-C_f)}{C_h+C_f}V_{out}(nT) \tag{3.8}$$

At time nT+T, the charge pump is switched back to the gain phase. According to the theory of charge conservation, the total charges in the capacitors C_h and C_f are

$$Q_{total}(nT+T)=Q_{ch}(nT+T/2)+Q_{ch}(nT+T/2) \tag{3.9}$$

So the output voltage at time nT+T is

$$V_{out}(n+1)T=\frac{Q_{total}}{C_h+C_f}=aV_{in}+bV_{out}(nT)$$
$$=\frac{2C_hC_f}{(C_h+C_f)^2}V_{in}+\frac{(C_h-C_f)^2}{(C_h+C_f)^2}V_{out}(nT) \tag{3.10}$$

According to Equation (3.11), we can have

$$V_{out}(nT+2T)=aV_{in}+bV_{out}(nT+T)$$
$$=aV_{in}+b[aV_{in}+bV_{out}(nT)]=a(1+b)V_{in}+b^2V_{out}(nT) \tag{3.11}$$

$$V_{out}(nT+3T) = aV_{in} + bV_{out}(nT+2T)$$
$$= aV_{in} + b[a(1+b)V_{in} + b^2V_{out}(nT)] \quad (3.12)$$
$$= a(1+b+b^2)V_{in} + b^3V_{out}(nT)$$

According to Equation (3.12) and (3.13), we can have

$$V_{out}(nT+kT) = a(1+b+b^2+\ldots+b^{k-1})V_{in} + b^kV_{out}(nT)$$
$$= a\frac{1-b^k}{1-b}V_{in} + b^kV_{out}(nT) \quad (3.13)$$

Where k=0,1,2…. ,because of b<1,we can have

$$\lim_{k\to\infty} V_{out}(nT+kT) = \frac{aV_{in}}{1-b}$$
$$= V_{in}\frac{2C_hC_f}{(C_h+C_f)^2}\frac{1}{1-\frac{(C_h-C_f)^2}{(C_h+C_f)^2}} = \frac{V_{in}}{2} \quad (3.14)$$

3.1.3 Pulse Frequency Modulation (PFM)

Pulse frequency modulation (PFM) or pulse skipping is one of typical methods to be used to regulate voltages in DC/DC converters for high efficiency at light loading. The basic idea is demonstrated in Fig. 3.4.

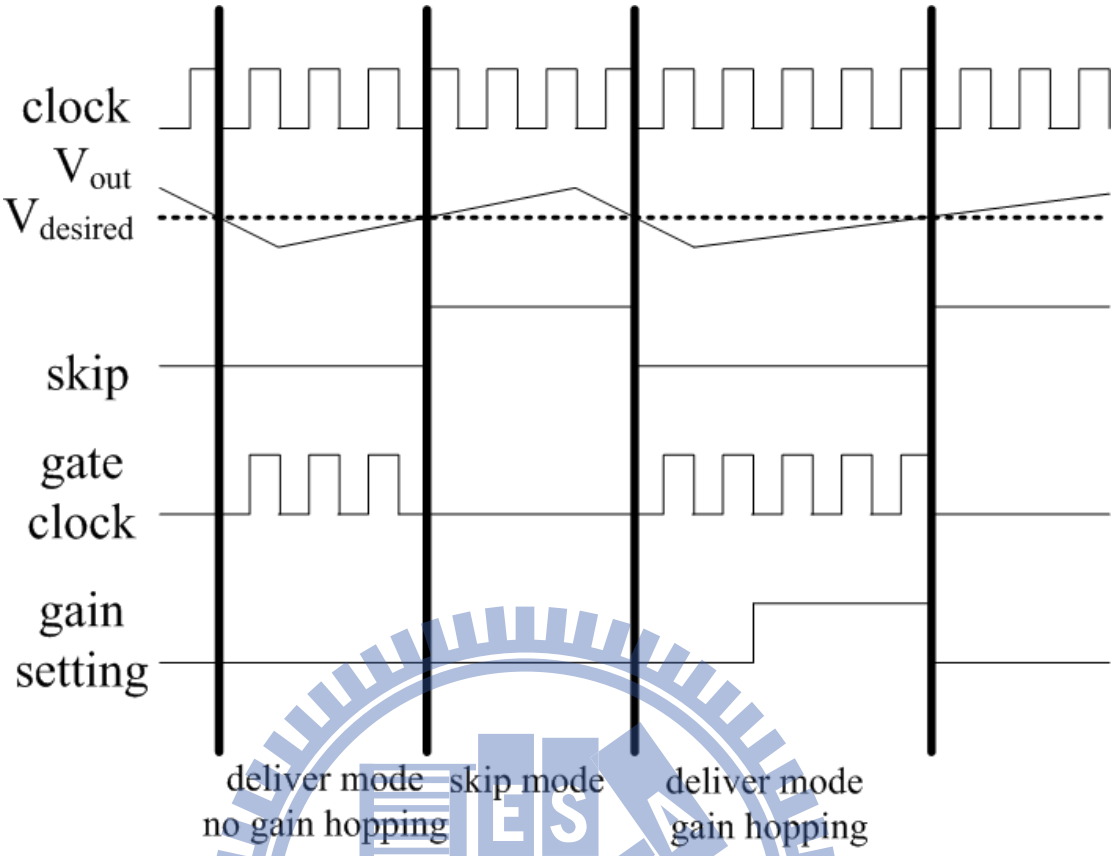


Fig. 3.4 Waveform of PFM and gain hopping.

While the output voltage V_{out} is less than the desired voltage $V_{desired}$, the skip signal is low, and the switched capacitor matrix is clocked to deliver charges constantly to the output. Hence, the output voltage V_{out} is raised. On the other hand, when V_{out} is greater than $V_{desired}$, the skip signal is high, the gate clock of switches is disabled and the charge pump stays in the common phase. Therefore, there are no more charges to be delivered to the output. Then, V_{out} is reduced by the load current. Depending on the switched capacitor matrix's running or stopping, the converter stays in one of two modes: the deliver mode or the skip mode.

3.2 Stability Scheme of Voltage Regulator

3.2.1 The Dynamic-Biased Shunt Feedback Buffer

A typical structure of a low-dropout regulator shows in Fig. 3.5 which consists of an error amplifier comparing the output voltage to the bandgap voltage V_{bg}, a PMOS pass transistor M_p, and the output buffer stage driving M_p. There are three different poles in the voltage regulator structure located at the output node of the error amplifier (N1), the output node of the buffer (N2), and the output node of the voltage regulator (V_{out}). In particular, these poles are given by

$$\begin{aligned} p_1 \mid N_1 &= 1/(r_{o1}C_1) \\ p_2 \mid N_2 &= 1/(r_{ob}C_p) \\ p_o \mid N_{out} &= 1/(R_{oeq}C_L) \end{aligned} \tag{3.15}$$

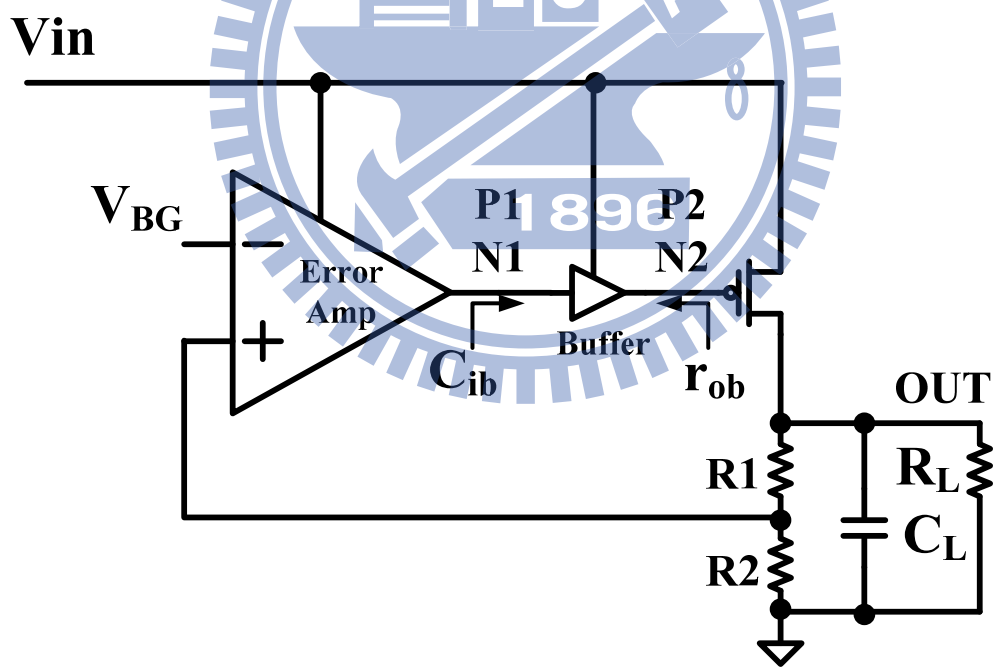


Fig. 3.5 Typical structure of a low-dropout regulator with an intermediate buffer stage.

The r_{o1} is the output resistance of the error amplifier, C_1 is the equivalent capacitance at N_1 which is dominated by the input capacitance of the buffer C_{ib}, r_{ob}, is the output resistance of the buffer, C_p is the input capacitance of M_p, and R_{oeq} is the

equivalent resistance seen at the output of the voltage regulator. Ideally, both C_{ib} and r_{ob} should be very small in order to achieve single-pole loop response by locating both p_1 and p_2 at frequencies much higher than the unity-gain frequency of the regulation loop.

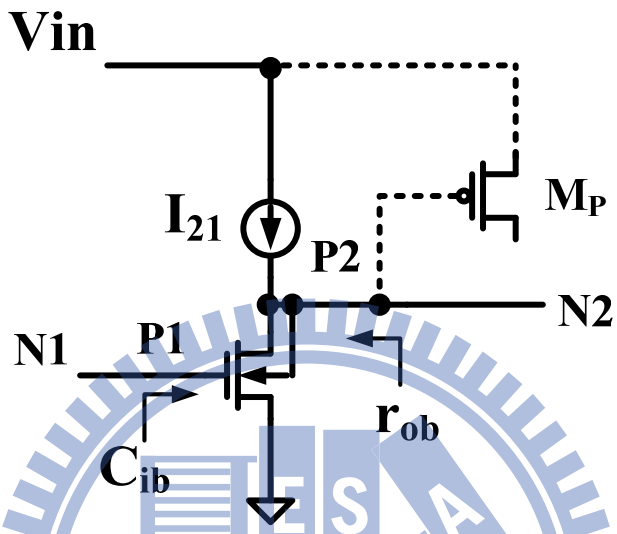


Fig. 3.6 Source-follower implementation of the intermediate buffer stage.

In order to construct the required output buffer stage, a simple PMOS source-follower is first considered for implementing the output buffer and its structure is shown in Fig. 3.6[10]. The PMOS source-follower provides near complete shutdown of the pass device when under the light-load conditions. Because of the output resistance r_{ob} of the source-follower is given by $1/g_{m21}$, it is necessary to increase g_{m21} in order to decrease the value of r_{ob} and allow p_2 to be located at frequencies much higher than the unity-gain frequency of the regulation loop. Transconductance g_{m21} can only be increased either through using a larger W/L ratio of transistor M_{21}, or through increasing the DC biasing current I_{21} through M_{21}, or both. However, increasing I_{21} would increase the total quiescent current of the regulator, and the current efficiency of the voltage regulator is degraded. Using a larger W/L ratio of M_{21} would increase the input capacitance C_{ib} of the buffer, which

is in turn pushes p_1 to a lower frequency and the stability would be poorly affected. A simple PMOS source-follower is, therefore, not a suitable implementation of the output buffer stage in the voltage regulator.

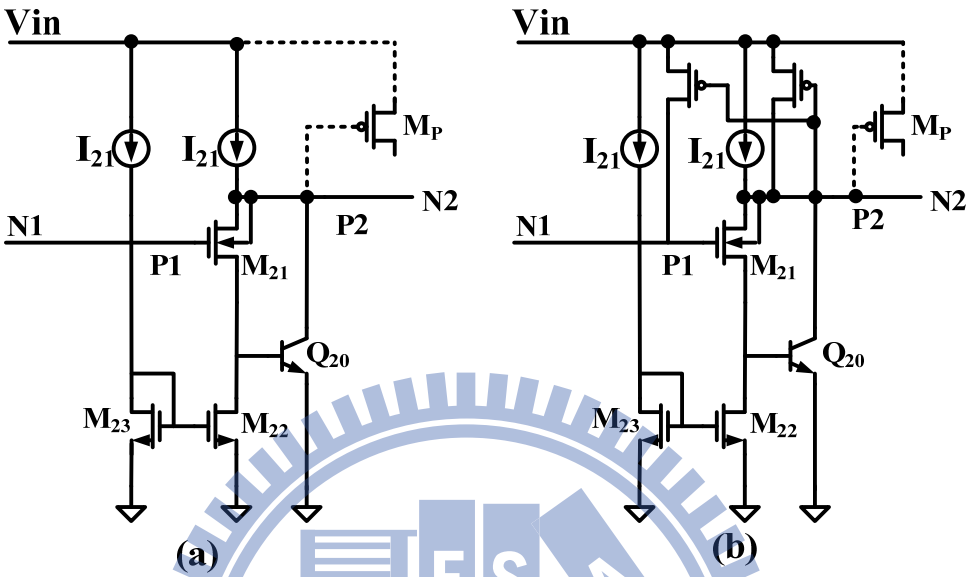


Fig. 3.7 (a) Source-follower with shunt feedback. (b) The buffer with dynamically-biased shunt feedback for output resistance reduction under different load currents.

For minimizing W/L ratio of M_{21} and the quiescent current required to reach a given r_{ob}, the source-follower with negative feedback shown in Fig. 3.7(a)[10] is used. In particular, the npn transistor Q_{20} is the feedback device connected in parallel to the output of the source-follower M_{21} in order to reduce r_{ob} through shunt feedback. When the input voltage at N_1 is constant and the output voltage increases, the magnitude of the drain current of M_{21} also increases, which in turn increases the base current of Q_{20}. As a result, the collector current of Q_{20} increases, reducing the output resistance r_{ob} by increasing the total current that flows into the output node. The output resistance looking into the follower is then given by

$$r_{ob} = \frac{1}{g_{m21}(1+\beta)} \tag{3.16}$$

Equation 3.2 shows that the output resistance of the follower is reduced by the current gain β of the shunt feedback device Q_{20}. For example, when an npn transistor with β more higher then 1 is used, the value of r_{ob} would be decreased and the frequency of p_2 at the gate of the pass device is then pushed to a decade higher. As a result, the quiescent current needed through M_{21} is greatly reduced to realize g_{m21} for a given r_{ob}. Similarly, the required transistor size of source-follower M_{21} is also reduced. The input capacitance of the buffer C_{ib} is then decreased, which allows p_1 given in (3.1) to be located at a higher frequency without dissipating additional quiescent current. It should be noted that the shunt feedback device Q_{20} can also be implemented by a NMOS transistor to achieve a similar reduction in the output resistance.

Because of the unit-gain frequency of the regulation loop increases with the load current, the output resistance of the buffer should decrease when the load current increases in order to maintain p_2 far away the unit-gain frequency under the entire load current range. The buffer with dynamically-biased feedback shows in Fig. 3.7(b)[10]. Two PMOS transistors M_{24} and M_{25} and the npn transistor Q_{20} realize dynamically-biased shunt feedback to decrease r_{ob} under different load current conditions. The output resistance of the buffer is then given by

$$r_{ob} = \frac{1}{g_{m21}(1+\beta)+g_{m24}} \tag{3.17}$$

The g_{m24} is the transconductance of the diode-connected transistor M_{24}. As shown in Fig. 3.7(b), when the load current flowing through the pass device M_p increases, both voltages at N_1 and N_2 decrease. The gate-source voltage of M_{24} is increased and hence more current flows through M_{24}. This current then mirrors through M_{25} such

that the current through the follower device M_{21} dynamically increases with the load current. This boosts the value of g_{m21}, thereby further reducing the output resistance of the buffer according to (3.3). In addition, the increase in g_{m24} with the load current can reduce the value of r_{ob}. This effect is significant under heavy load current conditions. Besides, when the load current increases, part of the dynamically-increased current through M_{21} flows into the base of Q_{20} and increases its collector current. The current gain β of the vertical parasitic npn transistor slightly increases with the collector current, which also helps on reducing the value of r_{ob} when the load current increases.

The dynamically-biased shunt feedback technique reduces both the input and output impedance of the buffer by decreasing the values of C_{ib} and r_{obs}. In particular, the reduction of r_{ob} increases with the change of load current. As a result of p_2 is located at sufficiently high frequencies under different load currents, while the voltage regulator only wastes low quiescent current at no-load condition. The benefit of having a smaller C_1 by using a smaller size of source-follower device in the buffer also improves the stability of the voltage regulator.

3.2.2 Zero-Pole Cancellation

A classical CMOS voltage regulator is shown in Fig. 3.8. This voltage regulator is composed of an error amplifier, a voltage buffer, a power PMOS transistor operating in saturation region, a feedback-resistor network and a voltage reference.

The three poles of this voltage regulator are generated at the output of the voltage regulator, the voltage buffer and the error amplifier, as mentioned in Section 3.2.1. The stability of classical voltage regulator based on dominant-pole compensation with pole-zero cancellation as shown in Fig. 3.9. The second pole p_2 is cancelled by the zero z_1 created by the ESR of the output capacitor. With a large output capacitance,

the voltage regulator stability is achieved by locating p_3 beyond the unity-gain frequency of the loop gain for providing sufficient phase margin. However, when loop gain is too high, p_3 locates before the unity-gain frequency, and an even larger output capacitance is required to retain the voltage regulator stability.

Moreover, the power PMOS transistor in the classical voltage regulator must operate in saturation region for considering the stability problem at different input voltages. The change of the voltage gain due to different drain–source voltage is not substantial when the transistor operates in saturation region [12]–[13]. However, if the transistor operates in linear region at dropout, the transistor will operate in saturation region instead as the input voltage increases. As mentioned before, when the loop gain increases, the classical voltage regulator based on dominant-pole compensation may be unstable. Hence, the power PMOS transistor needs to operate in saturation region throughout the entire range of input voltage, so a large transistor size is required for providing a small saturation voltage at the maximum output current.

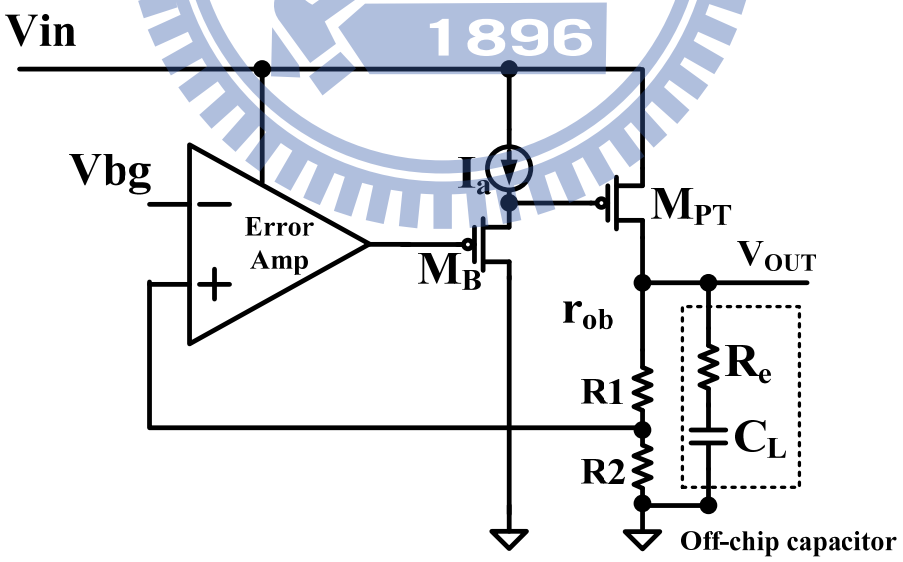


Fig. 3.8 Structure of classical voltage regulator.

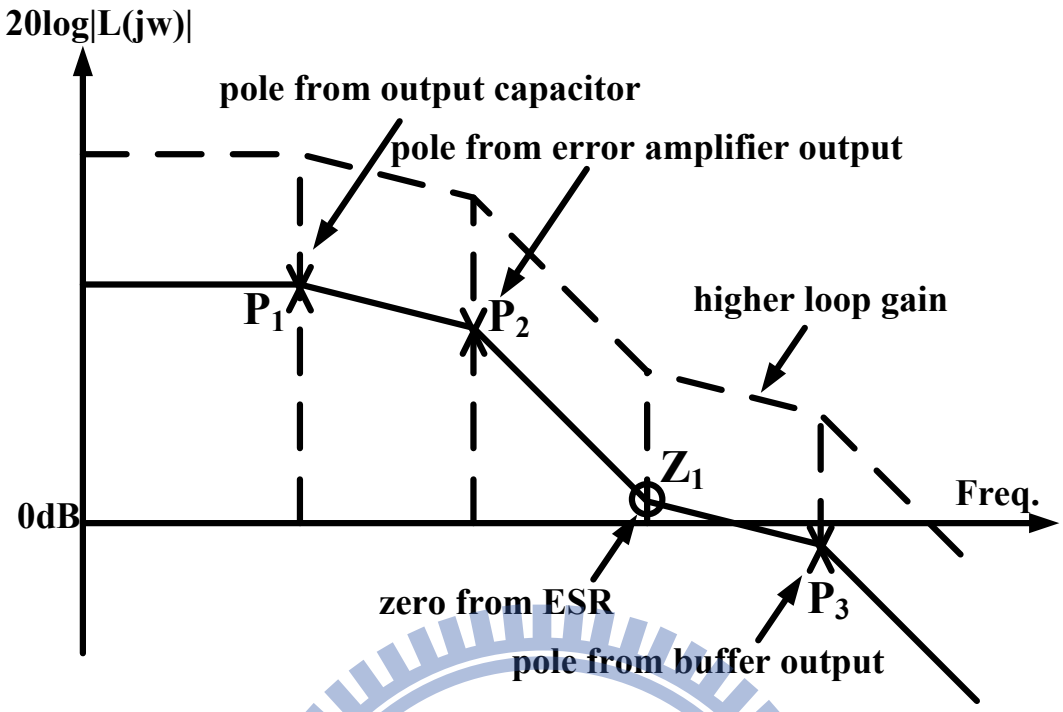


Fig. 3.9 Loop gain of classical voltage regulator.

3.3 Voltage Regulator with Digital Buffer

The conventional linear regulator is shown in Fig. 3.10[16] and has several limitations. First, the same feedback loop is used for feedback the error signal of V_{REF} as well as for responding to varying load demand. This problem can be mitigated by using replica biasing with a fast local feedback loop for load regulation. Second, the transient response time depends on the slew rate of the analog buffer to drive the large output device. The slew rate of a class A buffer is directly proportional to the quiescent current which limited the speed of the fast regulator with single stage load regulation. A class AB buffer is more power-efficient but tends to degrade the phase margin of the feedback loop and leads to more aggressive compensation and lower bandwidth.

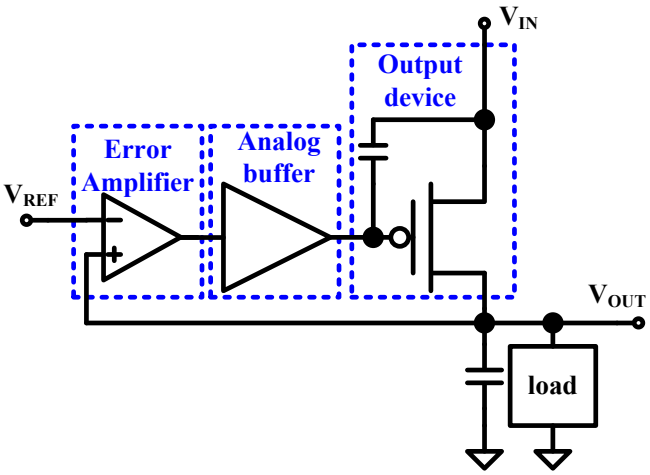


Fig. 3.10 Conventional linear regulator topology.

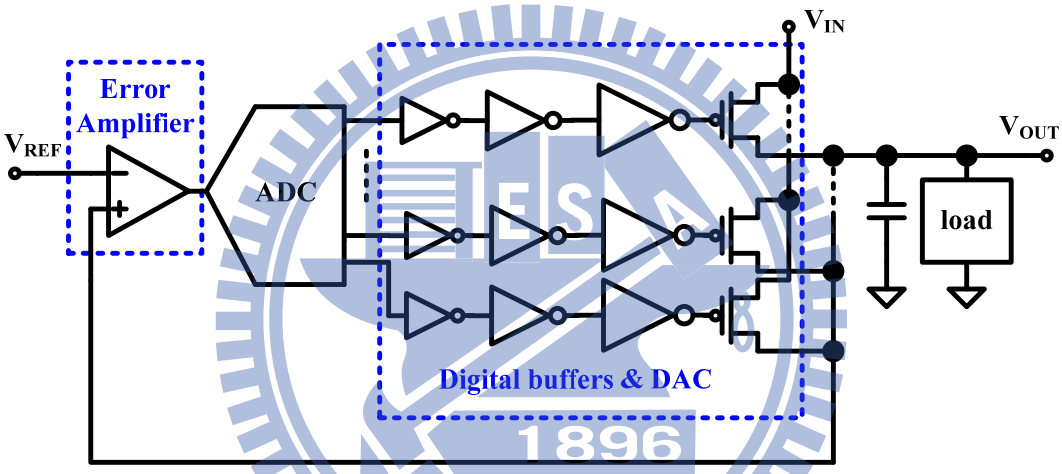


Fig. 3.11 Linear regulator with digital buffer.

The inverters are nearly perfect class AB circuits. They consume little current when idle and provide large output current when switching. As shown in Fig. 3.11[16], the inverters are used as digital buffer. The signal from the error amplifier is first translated by an A/D converter into a thermometer-coded digital output. Digital buffers add drive strength for the A/D converter can quickly turn on and off the parallel legs of the output device. In the steady state, very little current is consumed in driving of the output devices, which eliminates speed-power tradeoff that plagues traditional class A analog buffers. The schematic of regulator is shown in Fig. 3.12[16].

The reference voltage V_{REF} is produced between I_0 and I_5. Circuits in the AMP_1, ADC_1, DAC_1 are supplied between ground and V_{OUT} and circuits in the AMP_2, ADC_2, DAC_2 are supplied between V_{OUT} and V_{IN}. Inverters I_0 – I_2, I_5 – I_7, and the comparators in ADC_1 and ADC_2 are matched to have equal trip point. Inverters I_3 and I_4 have wider NMOS devices to lower the trip point. Inverters I_8 and I_9 have wider PMOS devices to raise the trip point. Skewing of the trip points is indicated by an offset added to the inputs of I_3 and I_8. Gain of AMP_1 and AMP_2 are relative to size of I_1 to I_2, I_3 to I_4, I_6 to I_7 and I_8 to I_9. A feedback signal from V_{OUT} couples to AMP_1 and AMP_2 via the supply rail. The amplifier will create different voltages across the resistive networks of ADC_1 and ADC_2.When V_{OUT}=V_{REF}, the resistors of ADC_1 and ADC_2 are biased below and above the comparator trip points, thereby producing 16-bit thermometer codes of all ones and all zeros, respectively. The NMOS devices of DAC_1 and PMOS devices of DAC_2 are off and the output current is zero.

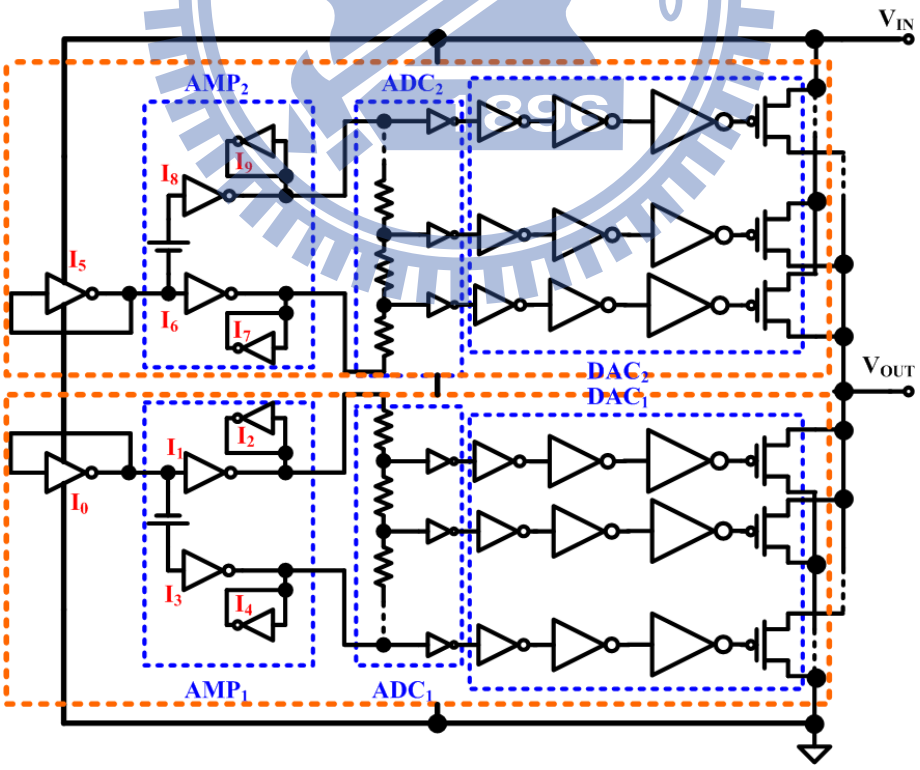


Fig. 3.12 Schematic of linear regulator with digital buffer.

3.4 Switched Capacitor DC-DC Converter & Voltage Regulator

3.4.1 Reference Voltage Circuit

The voltage regulator needs a reference voltage to bias the output voltage. The reference voltage circuit is shown in Fig. 3.13[17]. The reference voltage circuit is composed of a startup circuit and a reference voltage generator. The design concept is shown in Fig. 3.13[17]. The M5 and M8 are operated at saturation region as the current source which is shown in Fig. 3.13. M4, M6 and M7 are operated at linear region as the resistor. In this reference voltage generator, there are two control paths, path1 (P1) and path2 (P2). P1 is a supply-independent skill to reduce the dependency between M2 current and supply voltage. P2 is a negative feedback compensation to increase the V_{ref} stability.

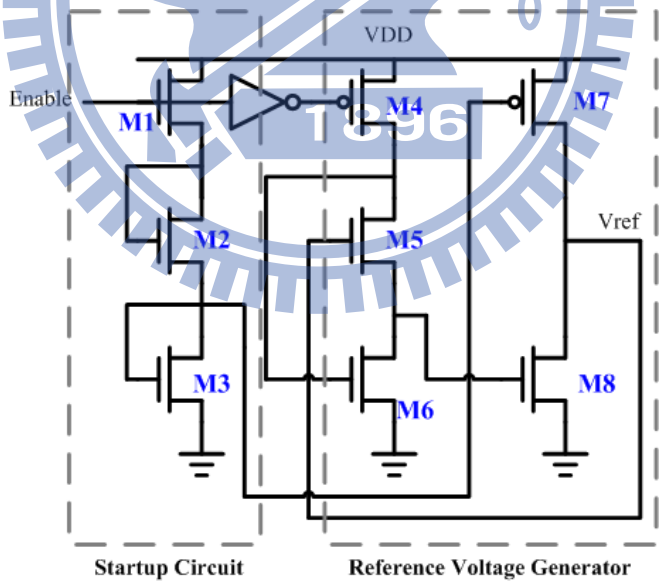


Fig. 3.13 Reference voltage circuit [17].

In order to improve the stability of reference voltage under different temperature, we change the devices of M1 and M7. As shown in Fig. 3.14, M7 is NMOS, and its gate is biased by gate of M2. For biasing M7, the M1 is changed to PMOS.

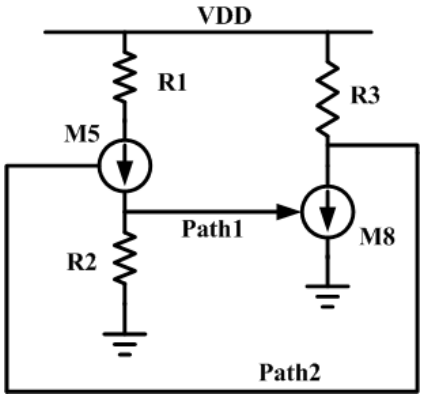


Fig. 3.14 The design of reference voltage circuit [17].

(a)Temperature variation analysis:

The temperature variation affect the threshold voltage of M1~M8 in Fig. 3.13 [17] and Fig. 3.15. In Fig. 3.13, as the temperature going up, the voltage of M3's gate is decreased and M7's threshold voltage is decreased. Thus, the temperature affects the M3 and M7 to increase the current of M7. In Fig. 3.16, as the temperature going up, the voltage of M3's gate is decreased and M7's threshold voltage is decreased. Because the M7 is NMOS, so the temperature affects the M3 to decrease the current of M7. Therefore, the circuit in Fig. 3.15 will more stable in different temperature. The simulation results are shown in Fig. 3.16. The results are simulated in UMC 90nm CMOS technology.

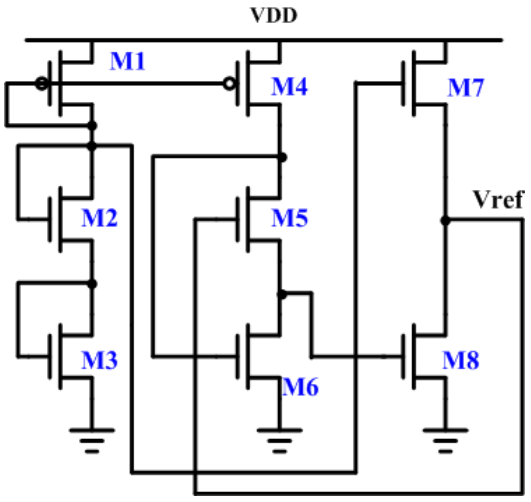
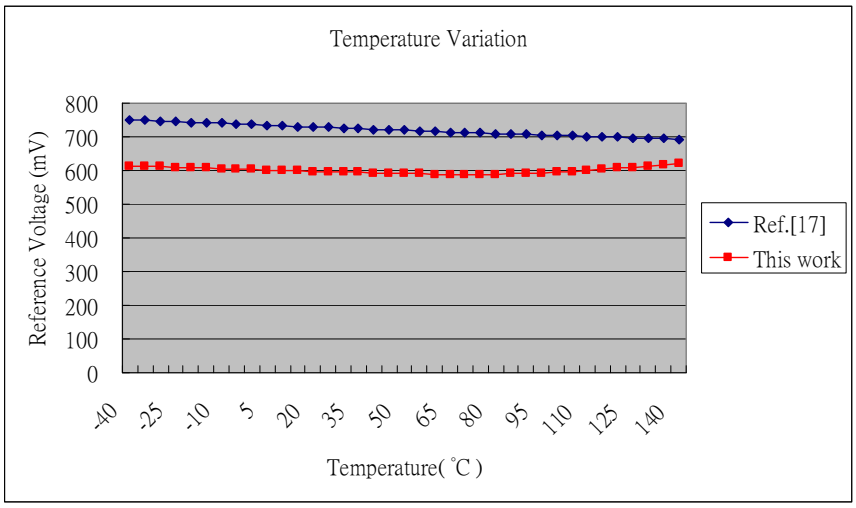
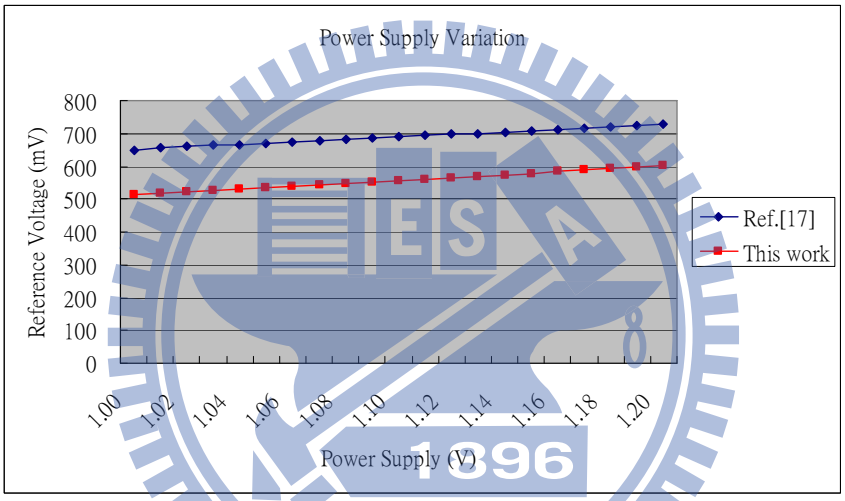


Fig. 3.15 Reference voltage circuit in this work.



(a)



(b)

Fig. 3.16 (a) Temperature variation. (b) Power supply variation.

Table 3.1 Comparison 600mV generator of Ref.[17] and this work.		
	Ref.[17]	**This work**
Technology	**90 nm**	**90 nm**
Supply voltage (Vsupply)	**1.2V**	**1.2V**
Reference voltage (Vref)	**700mV**	**600mV**
Supply variation (1.2V~1V)	**729mV~650mV**	**600mV~513mV**
ΔVref / ΔVsupply (mV/V)	**0.395**	**0.435**
Temperature variation (-40˚C~140˚C)	**752mV~693mV**	**622mV~588mV**
ΔVref / ΔTemperature (mV/˚C)	**0.32**	**0.18**
Power consumption	**74.5uW**	**4.5uW**

(b) Variable voltage reference generation by resistor-string DAC:

The variable voltage reference is generated by resistor-string DAC in Fig. 3.17. The decoder selects the output voltage for variable voltage reference. Fig. 3.18 and Table 3.2 are shown the Variable voltage reference generation with temperature variation.

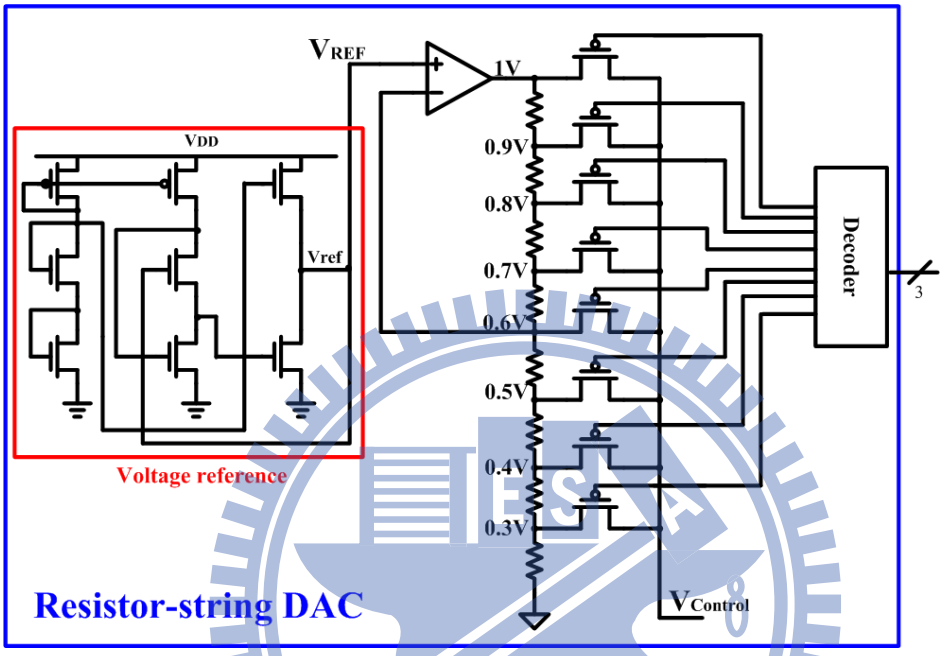


Fig. 3.17 Resistor-string DAC for variable voltage reference generation.

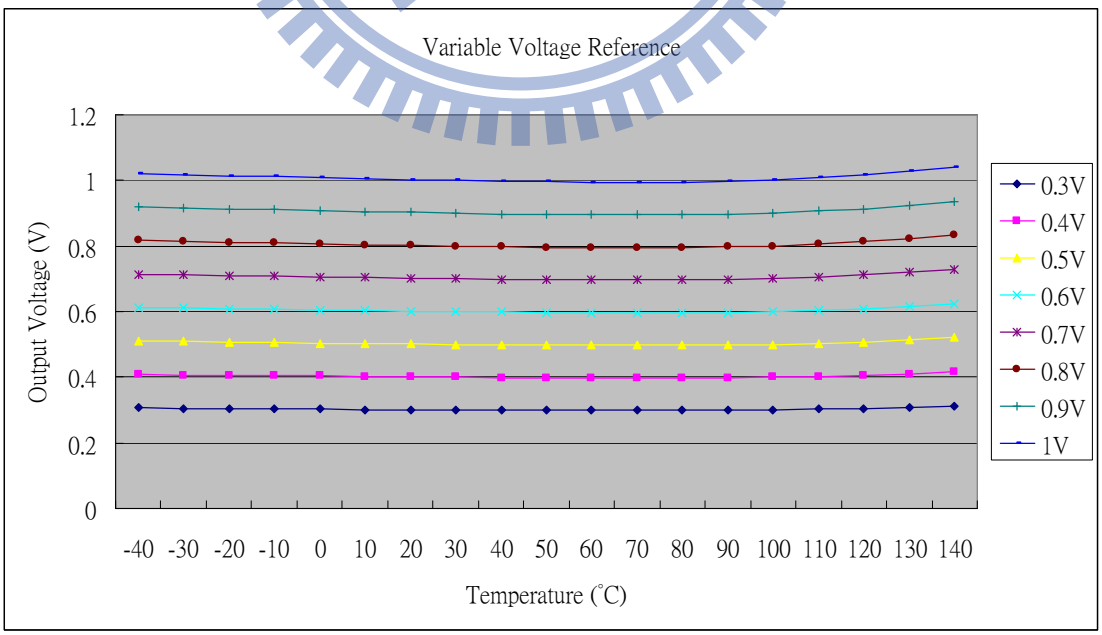


Fig. 3.18 Variable voltage reference generation with temperature variation.

Table 3.2 Temperature variation				
Temperature	**-40˚C**	**30˚C**	**140˚C**	**Variation**
1V	1.02	1.0	1.04	0.04V
0.9V	0.92	0.9	0.94	0.04V
0.8V	0.82	0.8	0.83	0.03V
0.7V	0.71	0.7	0.73	0.03V
0.6V	0.61	0.6	0.62	0.02V
0.5V	0.51	0.5	0.52	0.02V
0.4V	0.41	0.4	0.42	0.02V
0.3V	0.31	0.3	0.31	0.01V

3.4.2 Switched Capacitor DC-DC Converter

The switched capacitor DC-DC converter is composed of a comparator (comp.), a non-overlapping clock generator and a switched capacitor matrix as shown in Fig.3.13. The system sends the voltage control signal to change the topology of switched capacitor matrix and controls the DAC for settling the desire output voltage. The non-overlapping clock generator as shown in Fig.3.19 generates the non-overlapping clock (Φ_1 and Φ_2) to prevent the short circuit current path. And the proposed switched capacitor DC-DC converter can provide voltage form 0.3V~0.6V for low power SoC applications.

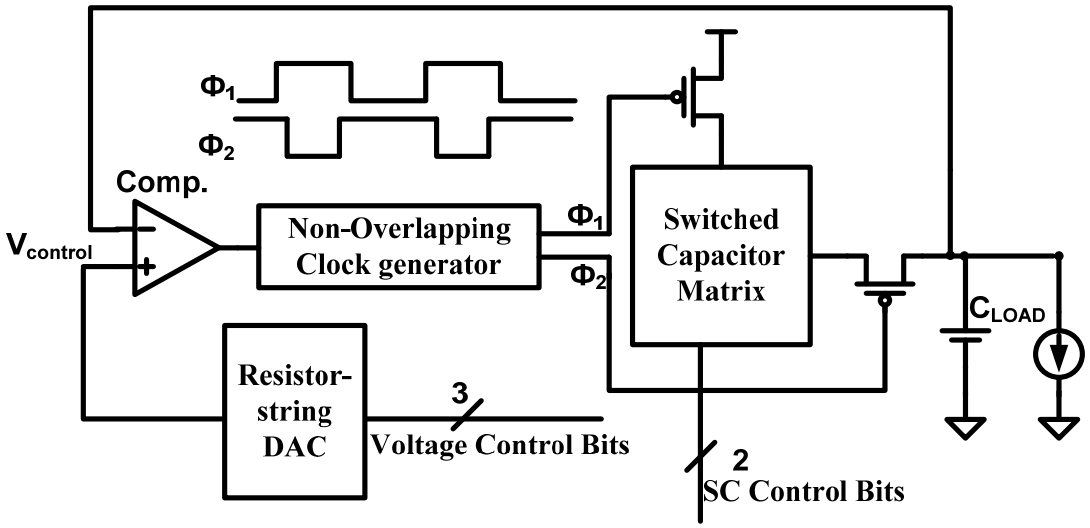


Fig. 3.19 Schematic of switched capacitor DC-DC converter.

Because of the low voltage detection such as 0.3V, the conventional architecture comparator will consume the voltage range $V_{ds}+V_{tn}$. So the input signal should larger then $V_{ds}+V_{tn}$ which is unsuitable for low voltage detection. Therefore, we proposed a new architecture of comparator as shown in Fig.3.20 By replacing the clock controlled current tail NMOS, and using low V_{th} NMOS as differential input, and the clock controlled switches are inserted between differential input and comparator latch. They are same function at small signal operation, but the proposed scheme can sense the voltage signal lager than V_{tn} which is suitable for low voltage sensing. Fig. 3.21 shows the transient response of voltage down conversion which can convert voltage to 0.3V and provide system for dynamic voltage scaling.

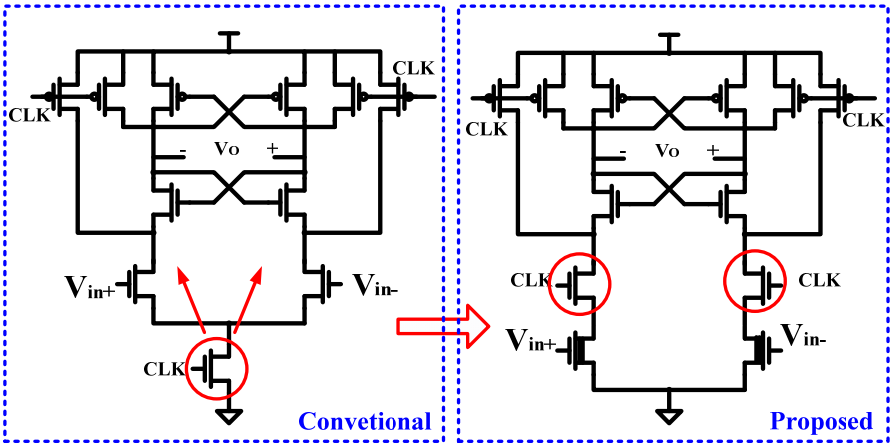


Fig. 3.20 Schematic of switched capacitor DC-DC converter.

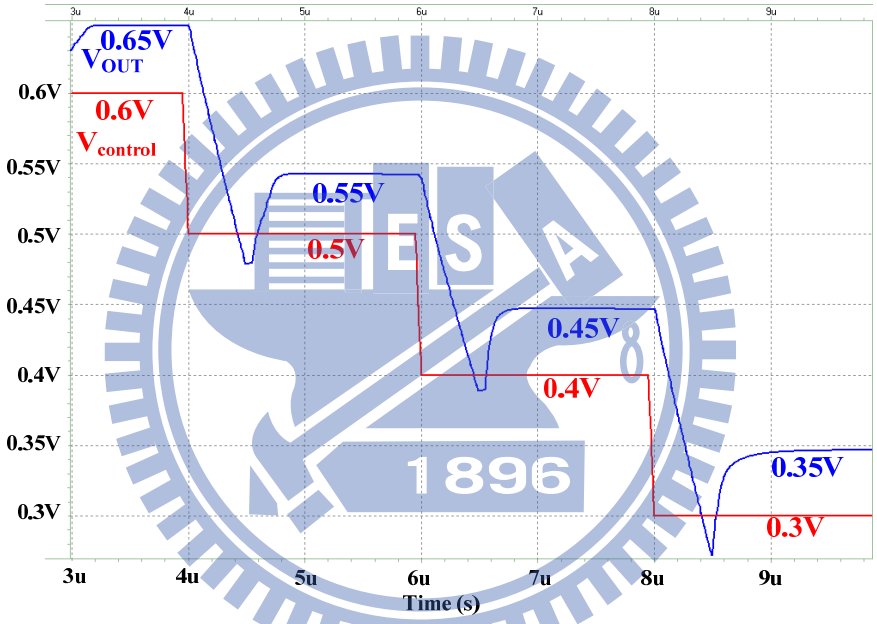


Fig. 3.21 transient response of voltage down conversion.

3.4.3 A Voltage Regulator using Dynamic-Biased OP Amp

In order to decrease the bias current of op amp and stabilize the transient response of regulator simultaneous, we use a dynamic-biased control scheme for biasing op amp. The schematic of proposed voltage regulator is shown in Fig. 3.22.

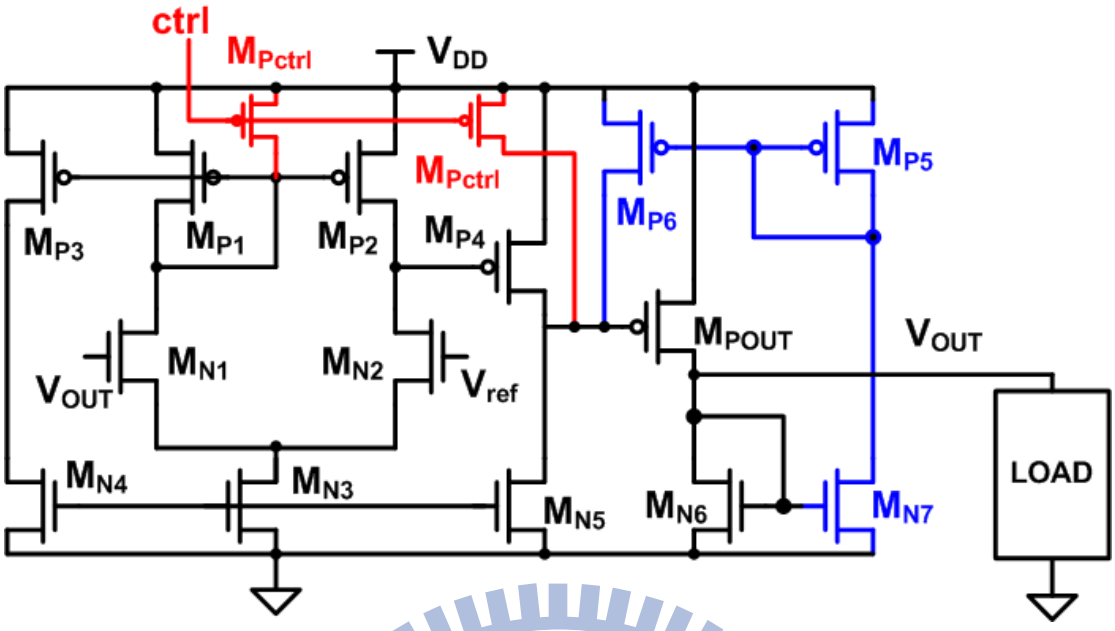


Fig. 3.22 Voltage regulator with dynamic-biased op amp.

The voltage regulator is composed of op amp, a voltage buffer, a POWER PMOS transistor (M_{POUT}) and dynamic-biased circuit. The op amp is composed of M_{P1}, M_{P2}, M_{P3}, M_{N1}, M_{N2}, M_{N3}, and M_{N4}. The voltage buffer is composed of M_{P4} and M_{N5}. The dynamic-biased circuit is M_{P6}. The current of M_{P6} is mirrored by M_{P5}. When there is supplied the surfeit of load current, the current of M_{N7} will mirror the current to M_{P6} and turn off M_{POUT}. As the load current increase suddenly, the current of M_{N6} will decrease. Thus, the M_{P6} will decrease the supply current to help turn on M_{POUT}. With the control of M_{P6}, M_{POUT} can turn on or turn off depend on the loading change.

The simulation results of voltage regulator using dynamic-biased OP amp. are shown in Fig. 3.23. When load current is 20mA, the voltage regulator outputs 1.06V and the quiescent current is 1mA. When load current is 150mA, the output voltage of voltage regulator will drop down and is stable in 963mV. The current efficiency is 99%. The comparison of the dynamic-biased voltage regulator with previous work ([15] and [16]) is shown in Table 3.3 and has better figure of merit.

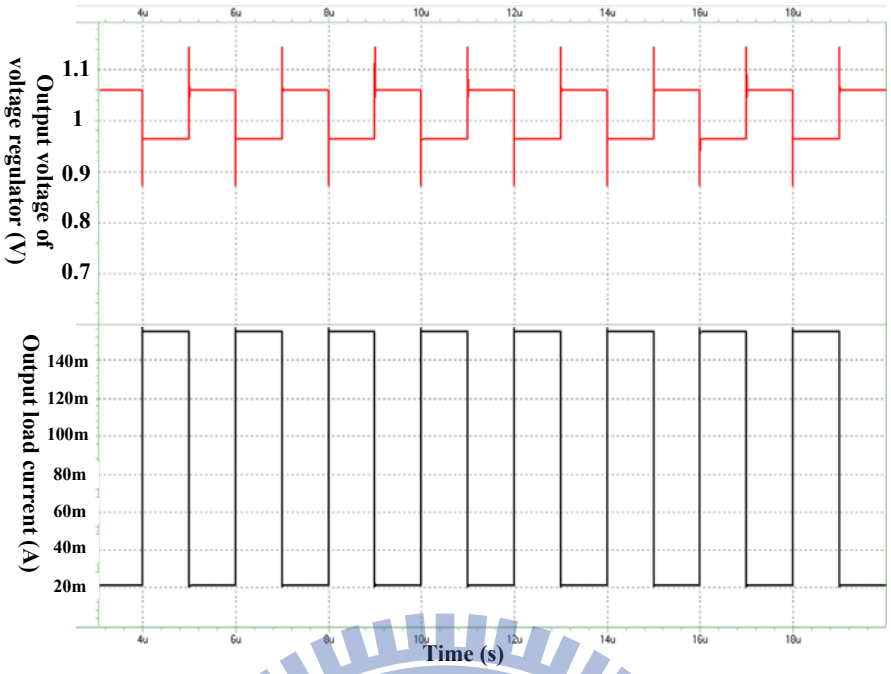


Fig. 3.23 Output voltage of voltage regulator under different Load current.

Table 3.3 Comparison of [15], [16] and proposed voltage regulator.			
	Ref.[15]	Ref.[16]	This work
Technology (nm)	90	90	90
Input Voltage	1.2V	2.4V	1.2V
Output Voltage	0.9V	1.2V	1V
Output droop ΔV_{OUT}	90mV	120mV	96mV
Rise time of Step Load current	100ps	50ps	250ps
MAX Load Current	100mA	1A	150mA
I_Q (quiescent current)	6mA	25.7mA	1mA
Current Efficiency	94.3%	97.5%	99%
Decoupling Cap.	0.6nF	2.4nF	0.4nF
Response time	540ps	288ps	256ps
FOM (figure of merit)	32ps	7.4ps	1.7ps

$$Current\ efficiency = \frac{I_{MAX}}{I_{MAX} + I_Q} \qquad T_R = \frac{C * \Delta V_{OUT}}{I_{MAX}} \qquad FOM = T_R \frac{I_Q}{I_{MAX}} = \frac{C * \Delta V_{OUT}}{I_{MAX}} * \frac{I_Q}{I_{MAX}}$$

C : Decoupling capacitor

ΔV_{OUT} : Output droop

I_{MAX} : Maximum load current

I_Q : Quiescent current

3.4.4 Switched Capacitor DC-DC Converter and Voltage Regulator

Because of the switched capacitor DC-DC converter is easy to convert down voltage for low voltage operation, but it is unable to provide high output current when the system at high voltage operation. Therefore, while the system at high voltage operation we use the voltage regulator to supply high voltage and high output loading current. The schematic of switched capacitor DC-DC converter and voltage regulator is shown in Fig.3.24. The switched capacitor DC-DC converter contains dual switched matrixes which can alternative charge the output voltage. There is a finite state machine (FSM) for controlling the dual switched matrixes and the state diagram is shown in Fig.3.25. When output voltage is lower then control voltage, the comparator sends the control signal (c) to change the dual switched matrixes. And the switched capacitor matrix 1 (SC1) is twice larger than switched capacitor matrix 2 (SC2), because of the SC2 is the auxiliary switched capacitor for supporting output voltage when SC1 is storing energy.

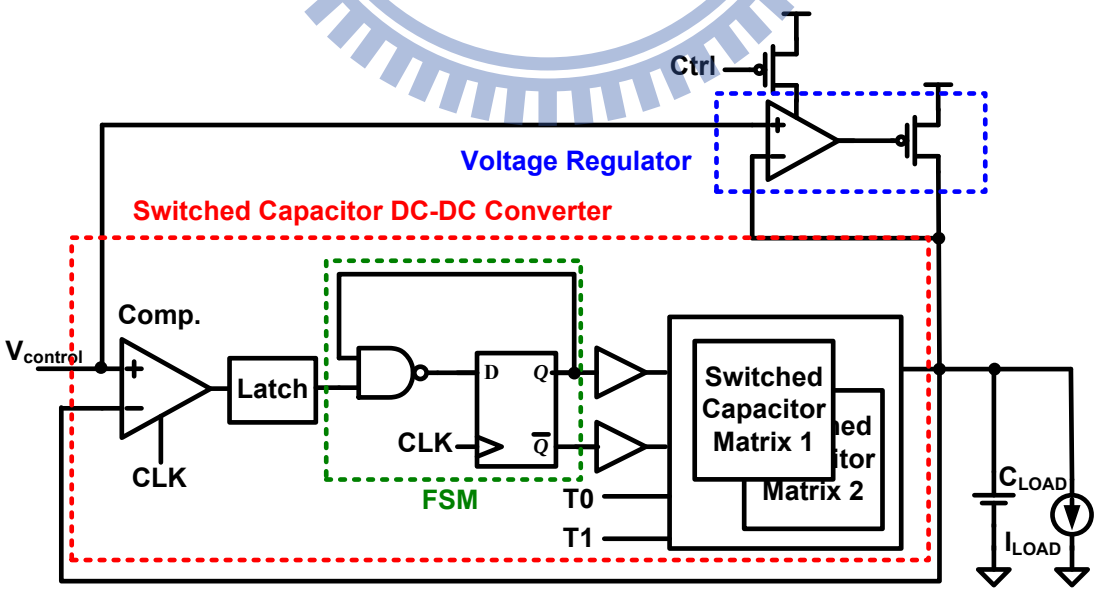


Fig. 3.24 Schematic of switched capacitor DC-DC converter and voltage regulator.

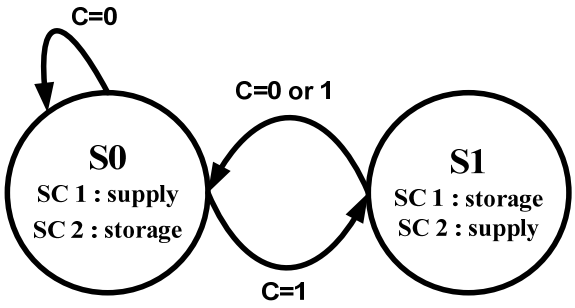


Fig. 3.25 The state diagram of the finite state machine.

The schematic of switched capacitor matrix is shown in Fig.3.26, and the topology of switched capacitor matrix shows in Fig.3.27. T_1 and T_0 are the control signal of switched capacitor topology selection as shown in Fig.3.26. When T_1 T_0 =10, the topology output voltage is 2/3 V_{DD} (V_{DD}=1.2V) and supplies 0.5V and 0.6V output voltage. When T_1 T_0 =11, the topology output voltage is 1/2 V_{DD} and supplies 0.4V and 0.3V output voltage. When T_1 T_0 =01, the topology output voltage is 1/3 V_{DD} and supplies 0.3V output voltage for system standby and data retention. When T_1 T_0 =00, the SC DC-DC converter is disabled.

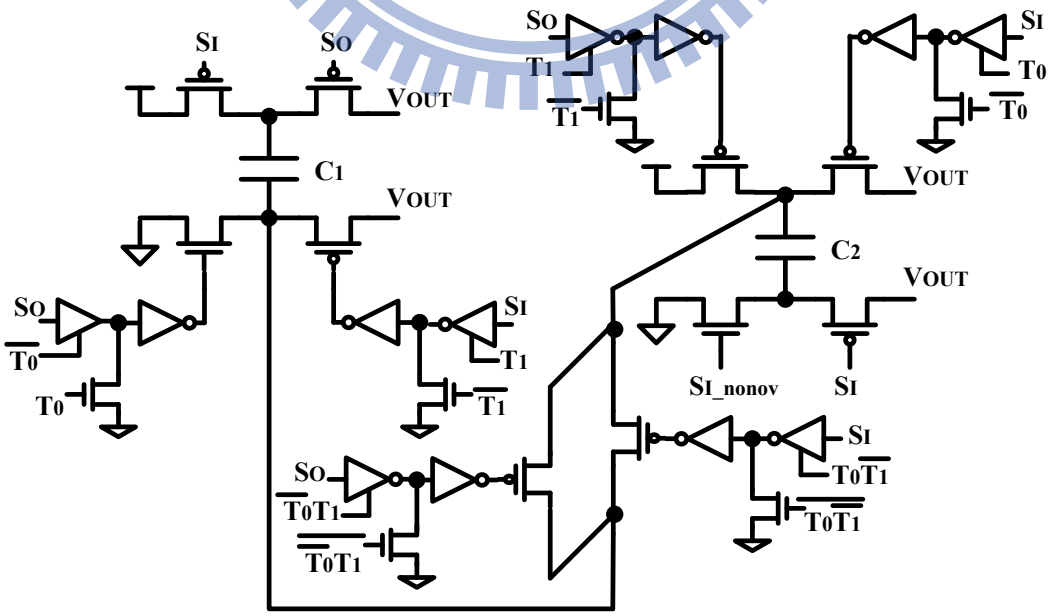
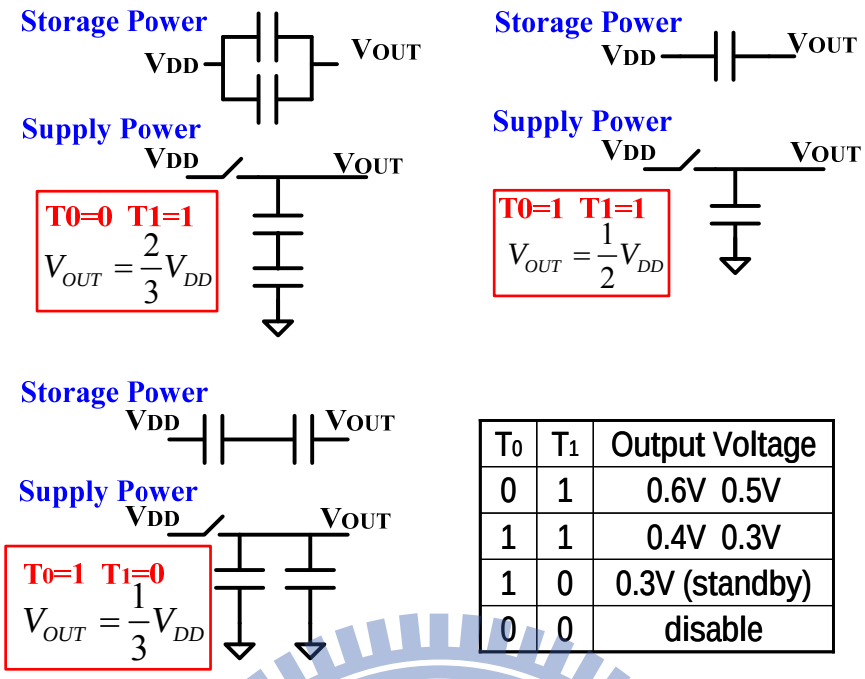


Fig. 3.26 The schematic of switched capacitor matrix.



T_0	T_1	Output Voltage
0	1	0.6V 0.5V
1	1	0.4V 0.3V
1	0	0.3V (standby)
0	0	disable

Fig. 3.27 The topology of switched capacitor matrix.

The efficiency comparison of linear regulator and switched capacitor DC-DC converter is shown in Table 3.4. Because of the power MOS consumes the V_{ds} voltage range, the efficiency of linear regulator is decreased with the low output voltage. Thus, the switched capacitor DC-DC converter is more suitable for supply low output voltage. The transient response of voltage down conversion is shown in Fig.3.28.

Table 3.4 Comparison of linear regulator and SC DC-DC converter.

Technology	UMC 90nm CMOS Technology			
Output Voltage	Output Power	Power Consumption	Efficiency (This work)	Linear regulator Efficiency
0.6 V	216.61 μW	275.72 μW	43.99 %	50%
0.5 V	218.27 μW	189.43 μW	53.56%	41.66%
0.4 V	155.43 μW	81.5μW	65.6 %	33.33%
0.3 V	136.07 μW	144.49μW	48.5%	25%
0.3 V (system standby)	7.088 μW	4.732μW	59.96 %	25%

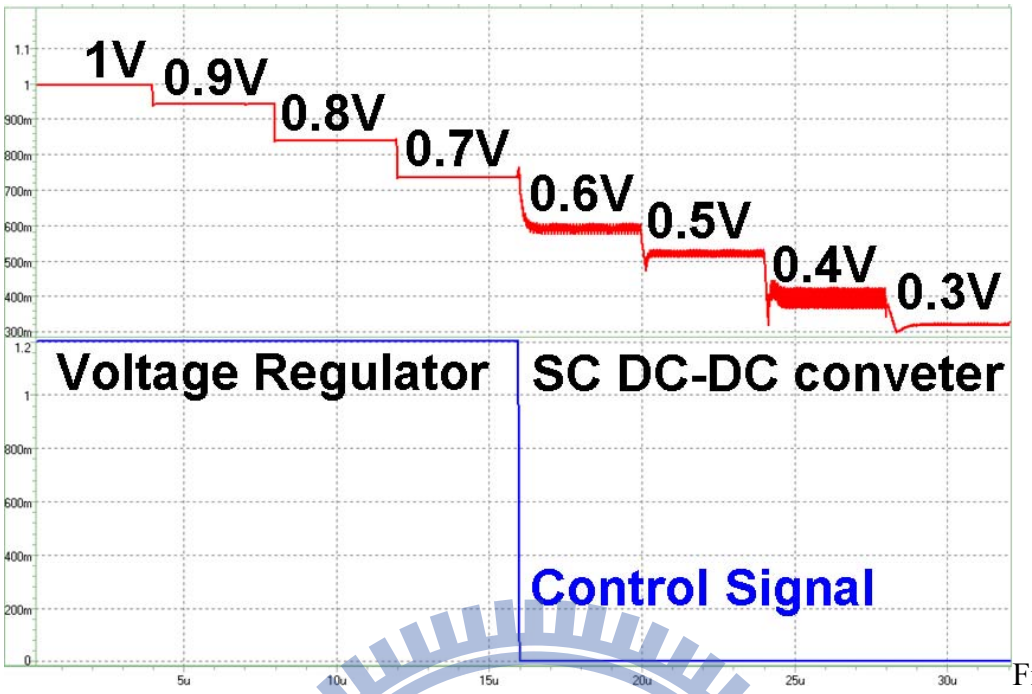


Fig. 3.28 The transient response of voltage down conversion from 1V~0.3V.

3.5 Summary

In this chapter, the operation of switched capacitor type voltage conversion is specified. The ac stability, transient response scheme of voltage regulator is described. The voltage regulator using digital buffer is also introduced. We improve the output loading capability of the switched capacitor by using dual switched capacitor matrixes.

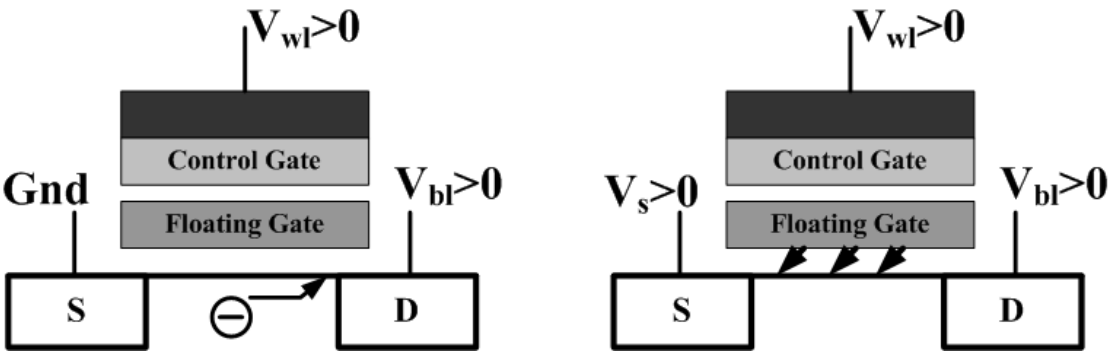
We use the switched capacitor DC-DC converter provide the voltage from 0.6V~0.3V and use the voltage regulator provide the voltage from 1V~0.7V for low power SoC applications. For the low voltage comparison, we propose a low voltage comparator which has the lower input range then the conventional architecture. And a finite state machine is used in switched capacitor DC-DC converter for control the dual switched capacitor matrixes which is utilized to improve the output loading capability. The switched capacitor DC-DC converter and voltage regulator can provide the voltage range from 1V~0.3V and the conversion efficiency of switched capacitor DC-DC converter is better than voltage regulator at low output voltage.

Chapter 4 Charge Pumps

For programming the information of nonvolatile memory such as flash memory, the voltage supplies to the gate must higher than power supply voltage shows in Fig. 4.1(a) [18]. And negative voltage will apply to gate for erasing the information of flash memory which is shown in Fig. 4.1(b). Charge pump is usually used to generating such high voltage and negative voltage.

There are many types of charge pump like voltage doubler, voltage multiplier and Dickson charge pump. The Dickson charge pump is used to generate ultra high voltage such as ten times of power supply voltage. The Dickson charge pump also can generate negative voltage by connecting to ground.

In this Chapter, the voltage doubler is described and analysis in section 4.1. Ultra high voltage can be generated by Dickson charge pump. The techniques of improving the pumping efficiency of Dickson charge pump will be shown in Section 4.2. The negative voltage generator is also demonstrated in Section 4.3. In Section 4.4, we proposed a simple architecture of Dickson charge pump of generating ultra high voltage by reduce body effect. And a new connect scheme of charge pump is proposed for generating ultra high voltage by replace off-chip capacitor with MOS capacitor as pumping capacitor. The simulation results are simulated in UMC 90nm CMOS.



(a) (b)

Fig. 4.1 (a) Programming: channel hot electron injection in the floating gate at the drain side. (b) Erasing: Fowler-Nordheim electron tunneling current through the tunnel oxide from the floating gate to the silicon surface.

4.1 Voltage Doubler

The voltage doubler can double the supply voltage. A voltage doubler is illustrated in Fig. 4.2[22]. During clock phase Φ, switches S_1 and S_3 are short to charge capacitor to V_{DD}. Next switch S_2 is closed and the bottom plate of the capacitor assumes a potential V_{DD}, while the capacitor maintains its charge of $V_{DD}C$ from the previous phase. This means that during $\overline{\Phi}$

$$(V_{out} - V_{DD})C = V_{DD}C \Rightarrow V_{out} = 2V_{DD}$$

Therefore, in the absence of a dc load, an output voltage has been pumped up to twice the supply voltage.

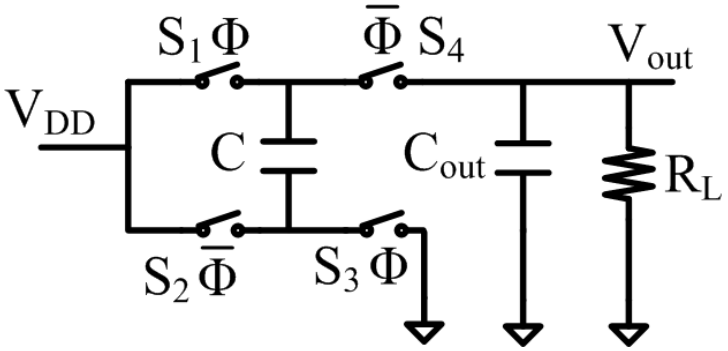


Fig. 4.2 Voltage doubler.

4.1.1 Voltage Multiplier

Voltage multiplication is carried out by cascading more than one capacitor in series. The Cockroft-Walton multiplying circuit shows in Fig. 23. Three capacitors, C_A, C_B and C_C are connected in series and capacitor C_A is connected to the supply voltage V_{DD}. During phase Φ capacitor C_1 is connected to C_A and charge to V_{DD}. When the switches change position during the next cycle, $\overline{\Phi}$, capacitor C_1 will share its charge with capacitor C_B and both will be charged to $V_{DD}/2$ if they have equal capacity. In the next cycle, C_2 and C_B will be connected and share a potential of $V_{DD}/4$ while C_1 is once again charged to V_{DD}. It is thus obvious that if this process continues for a few cycles, charge will be transferred to all the capacitors until a potential of $3V_{DD}$ is pumped up across the output V_{out}.

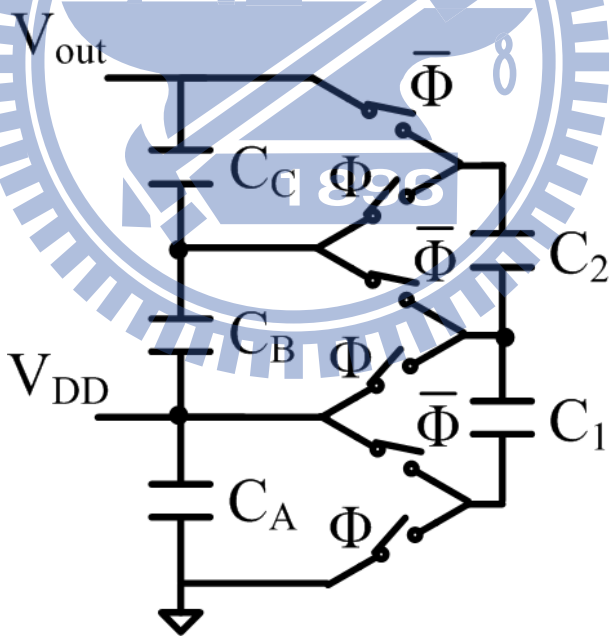


Fig. 4.3 Cockcroft-Walton voltage multiplier

4.1.2 Analysis of Voltage Doubler

A charge pump for flash-EEPROM high-voltage generation shows in Fig. 4.4[23]. It is a boosted up charge pump with a four-phase clocking scheme. This circuit

performs high power efficiency at low loading currents (65% at 40 uA), but the efficiency is poor at high loading current loads (20% at 200 uA). The reason is that in boosted up charge pumps, the transistors should opposed a voltage drop of twice the V_{DD}, and high-voltage transistors are used to prevent breakdown. The main disadvantage is that these transistors have higher voltage threshold and parasitic capacitances with comparison to the standard ones. Thus, their behavior while used as a switch is poor. This makes the efficiency decreased at high current loads and limits the switching frequency around 10–20 MHz. The use of standard transistors is preferable to decrease voltage threshold and parasitic capacitances and to extend current drive capability. Decreased voltage thresholds will make a better behavior of transistor switches, and that will extend efficiency and voltage gain; reduced parasitic capacitances will extend switching frequency, and that will decrease capacitor area.

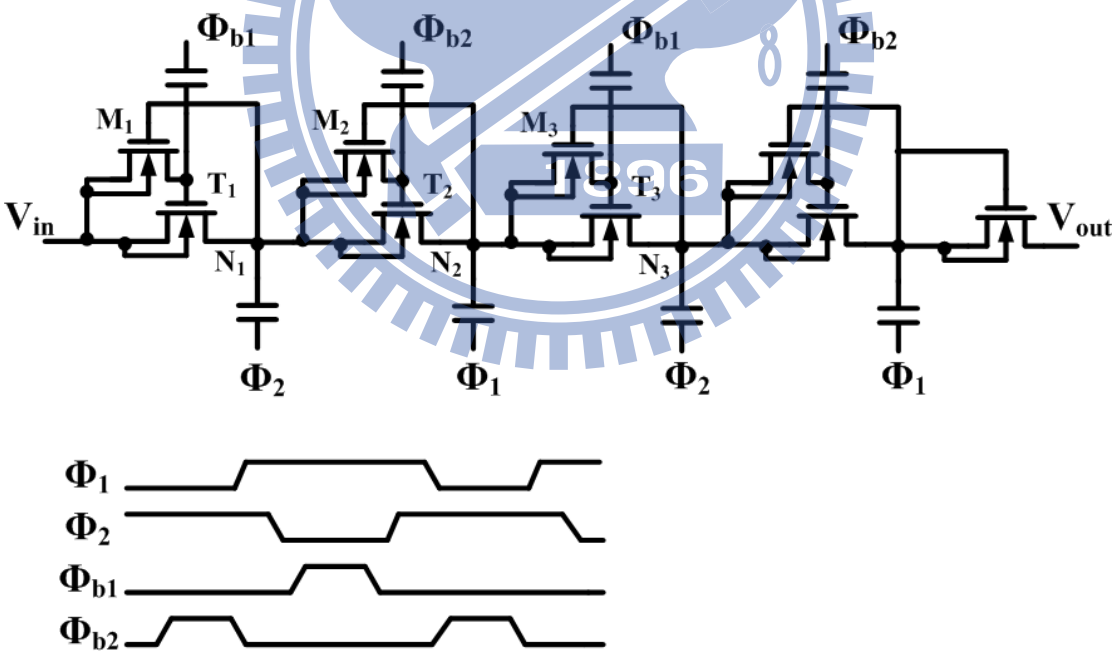


Fig. 4.4 Four stage boosted charge pump for positive high voltage generation with n-MOS transfer gates and conventional four-phase clocking scheme

But, standard transistors cannot apply voltages higher than the supply voltage; this

requires the usage of a different architecture. A simple two-phase voltage doubler shows in Fig. 4.5[24], and reached 70% power efficiency at 2-mA current loading with 100-pF capacitors and 10-MHz switching frequency. But, these voltage doublers cannot be cascaded whereas the breakdown problem in nMOS transistors. This problem could be solved by a triple-well process, which allows changing the nMOS body voltage which is shown in Figs. 4.6(a)[25]. The voltage drop down across each transistor is lower than V_{DD}. Then the charge pump is a cascade of voltage doubler stages with nMOS transistors in triple well; each stage can be conceived with standard transistors and is pumped by a simple two-phase clocking scheme; the final stage is the same as the other stages. This solution has been proposed in [26] for pumping up with no current loading and a low switching frequency at 2-MHz. So, we utilize it also with a current loading and increasing the switching frequency to 100 MHz to reduce the usage of capacitors (2.5 pF).

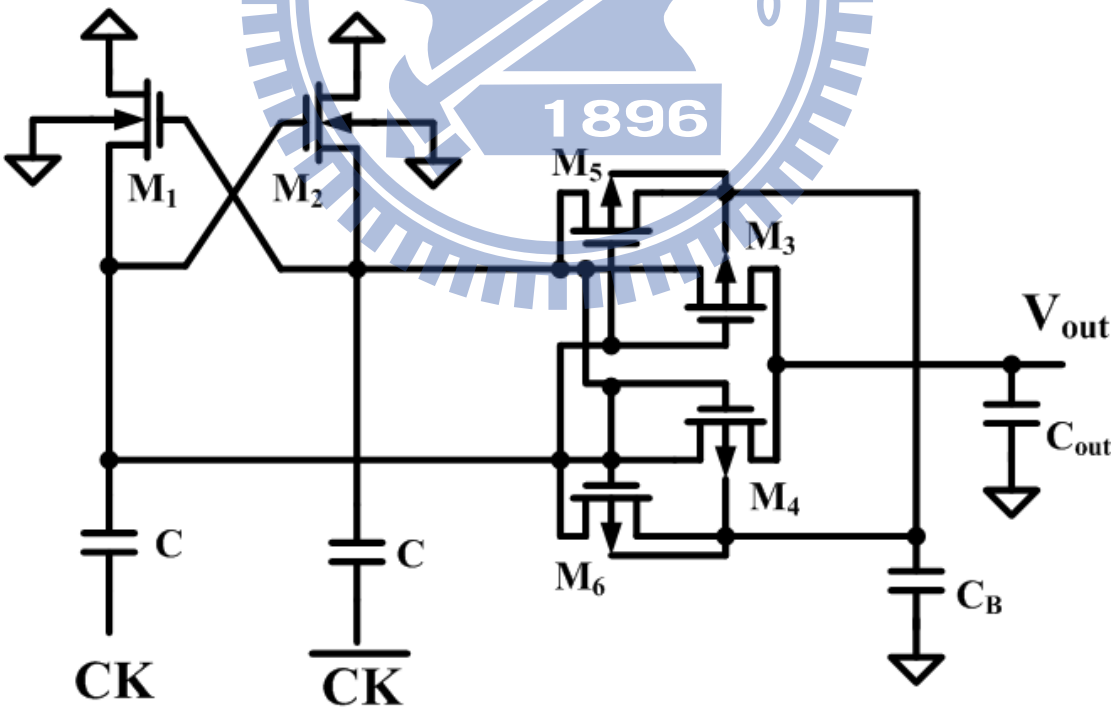


Fig. 4.5 Voltage doubler[24].

As shown in Fig. 4.6(a), assume that I_{out}=0. After the initial situation, a steady situation is reached. During the first half cycle, CK is high, CK_{neg} is low, M_0 and M_3

are on, M_1 and M_2 are off; C_1 is discharged to V_{low} through M_0, while C_0 is charged to V_{high}, which is $V_{low}+V_{DD}$, through M_3. During the second half cycle, CK is low, CK_{neg} is high, M_0 and M_3 are off, M_1 and M_2 are on; C_0 is discharged to V_{low} through M_1, while is C_1 charged to V_{high}, which is $V_{low}+V_{DD}$, through M_2. A voltage gain is pumped up between V_{low} and V_{high}. When $I_{OUT} \neq 0$, the voltage gain is decreased through the stage output resistance and its value can be derived by the following expression:

$$\Delta V = V_{dd} C / (C + C_{par1}) - R_{out} I_{out}$$

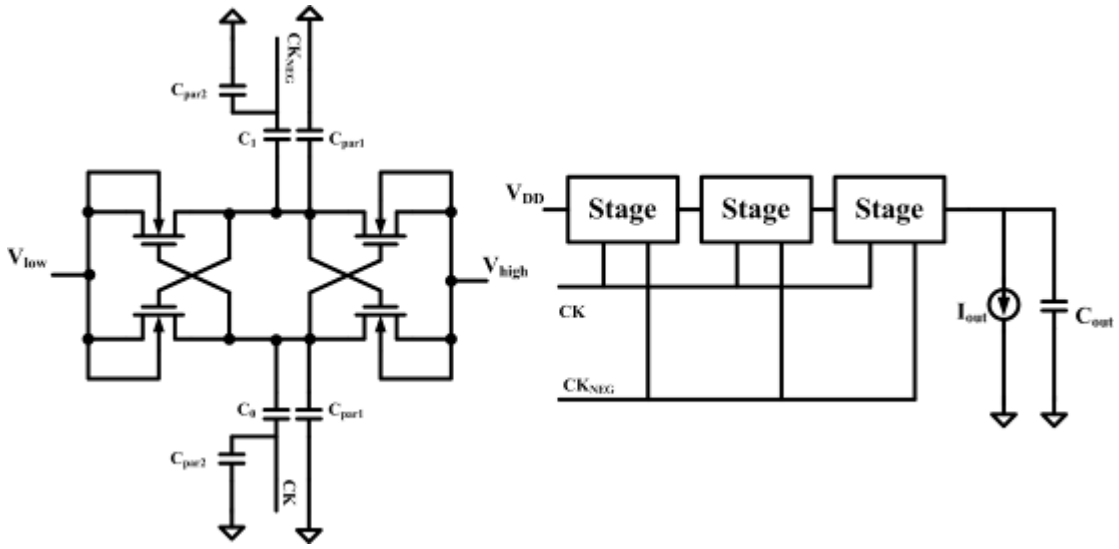
$$R_{out} = f(f_C, R_{switch})$$

$C = C_0 = C_1$, C_{par1} is the parasitic capacitance in the internal nodes of the stage, R_{out} is the stage output resistance and R_{switch} is the on-resistance of the transistor switches. R_{out} has a nonlinear function dependence on f_C and R_{switch}, symbolized by the function *f*. C_{par2} is the bottom plate parasitic capacitance of capacitors C0, C1 shown in Fig. 4.6(a). Cascading *n* stages as shown in Fig. 4.6(b), gives:

$$V_{out} = V_{dd} + n \cdot \Delta V$$

The main current supply to the output loading is given by the stage drivers. Drivers and switches must be well sizing so that for every clock cycle the power transfer is efficient. The proposed values have been chosen for maximum power efficiency at *f* = 100MHz. The following expression is used to evaluate power efficiency, Where $\overline{V_{out}}$ and $\overline{I(V_{dd})}$ are the mean values of V_{out} and $I(V_{dd})$.

$$Eff = 100\% \cdot P_{out} / P_{in} = 100\% \cdot \overline{V_{out}} \cdot I_{out} / V_{dd} \cdot \overline{I(V_{dd})}$$



(a) (b)

Fig. 4.6 (a) Stage schematic of the two-phase charge pump[25]. (b) Complete schematic of the tree-stage two-phase charge pump.

4.2 Dickson Charge Pump

The four-stage diode charge pump circuit using the diodes as the charge transfer devices shows in Fig. 4.7(a) [27]. It is hard to carry out the fully independent diodes in the common silicon substrate. The charge pump circuit with diodes is shown in cannot be integrated into the standard CMOS process. Thus, most charge pump circuits are based on the circuit proposed by Dickson. Fig. 4.7(b) [27] shows the four-stage Dickson charge pump circuit, where the diode-connected MOSFETs are used to converter the charges from the present stage to the next stage. Thus, it can be suitable integrated into standard CMOS processes. Although, the voltage difference between the drain terminal and source terminal of the diode-connected MOSFET is the threshold voltage when the diode-connected MOSFET is turned on. Hence, the output voltage of the four-stage Dickson charge pump circuit has been derived as

$$V_{out} = \sum_{i=1}^{5} (V_{DD} - V_{t(Mi)})$$

$V_{t(Mi)}$ denotes the threshold voltage of the diode-connected MOSFET M*i*. In the traditionally, the body terminals of the diode-connected MOSFETs in the Dickson charge pump circuit are connected to ground. The threshold voltage ($V_{t(Mi)}$) of the diode-connected MOSFET increased due to the body effect. The threshold voltage will enlarge when the source of NMOS is pumped up. Thus, the pumping efficiency will decrease as the pumping stage is increased. For solving this problem, solutions such as CTS, dynamic body bias scheme and four-phase clock scheme are proposed.

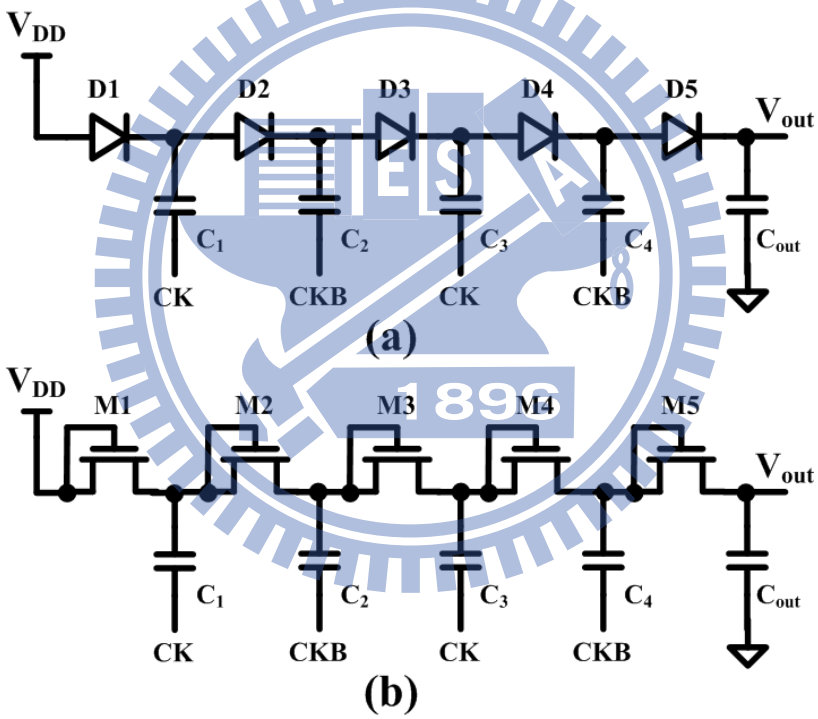


Fig. 4.6 (a) Stage schematic of the two-phase charge pump[25]. (b) Complete schematic of the tree-stage two-phase charge pump.

4.2.1 Charge Transfer Switch

For improving pumping up efficiency, the CTS use NMOS as switch to convert charge. This will ideally increase the pumping up efficiency of every stage by one V_T.

The structure is shown in Fig. 4.8[28].

The Φ_1 and Φ_2 are CLK and CLKB. When voltage is pumped up, the source voltage of next stage will turn on the switch and help previous stage to convert charge directly. But that results the reverse charge sharing problem. For the switches always turn on, the charge of stage will flow back to previous stage when switching. Thus, the dynamic CTS scheme is proposed in Fig. 4.9[28].

When CLK is low, node 1 will be V_{DD} and node 2 will be 3 V_{DD}, then MN1 is turned off and MP1 is turned on. Therefore, the MS1 will turn on to transfer charges from the power supply to node1.When CLK is high, node 1 and node 2 will be 2 V_{DD}, then MN1 is turned on and MP1 is turned off. Thus, the MS1 will turn off to avoid the charges back to the power supply. The problem is that the maximum gate to source voltage will be $3V_{DD}$, this will result the MOS breakdown. Thus, a design for prevention of gate oxide reliability is proposed.

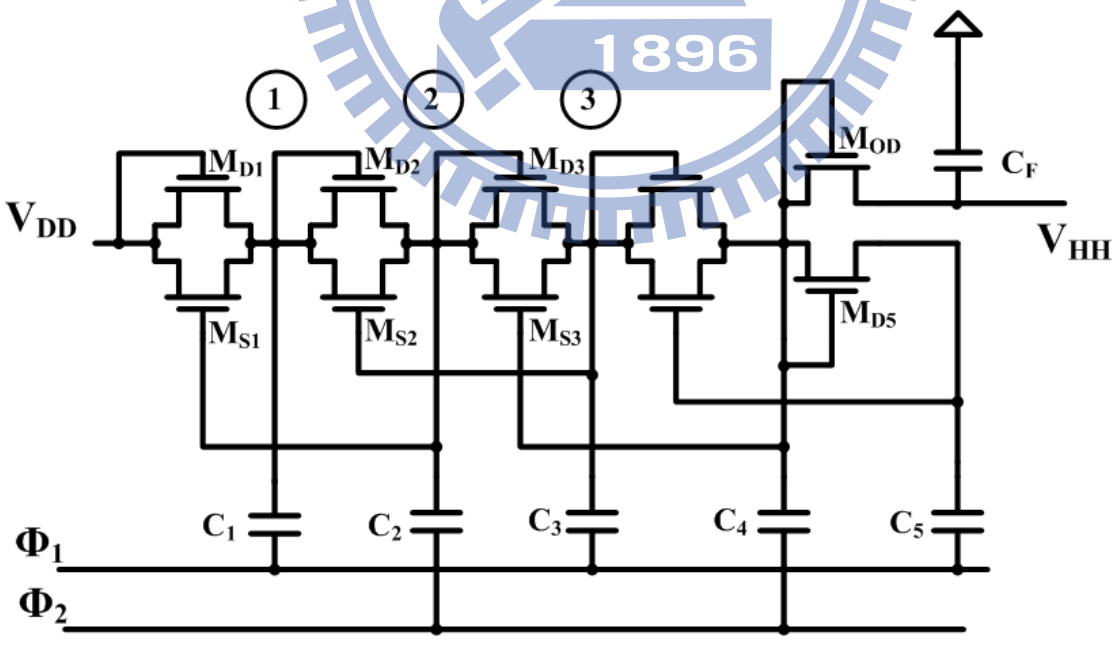


Fig. 4.8 A four-stage charge pump using static CTS's.

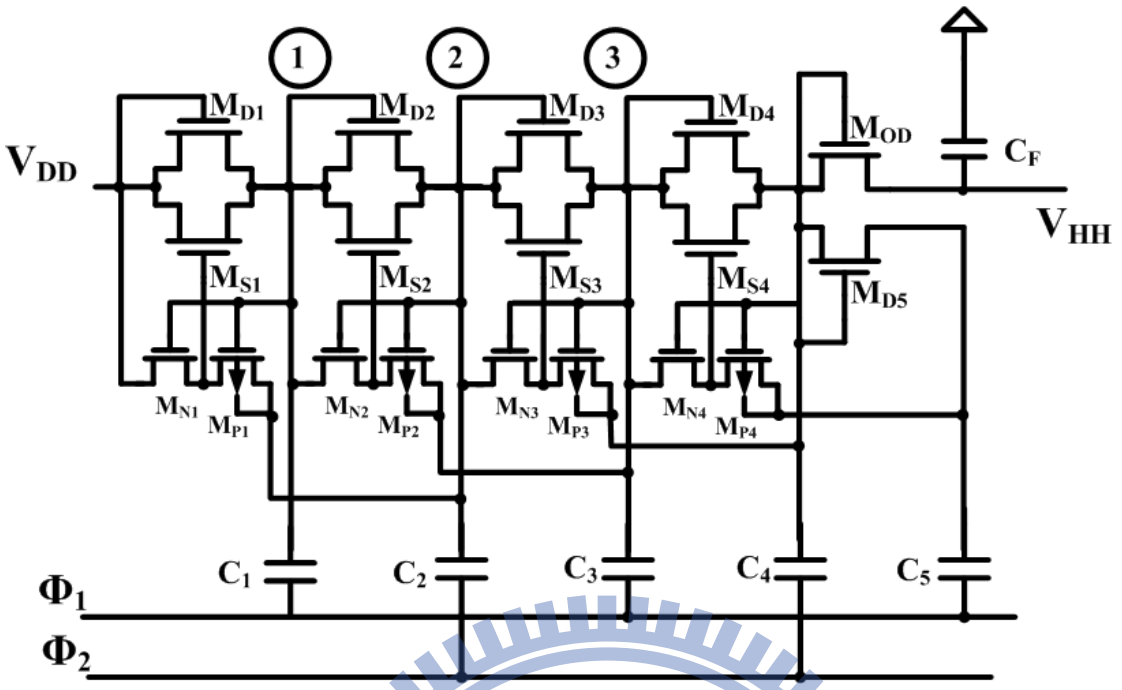


Fig. 4.9 A four-stage charge pump using dynamic CTS's.

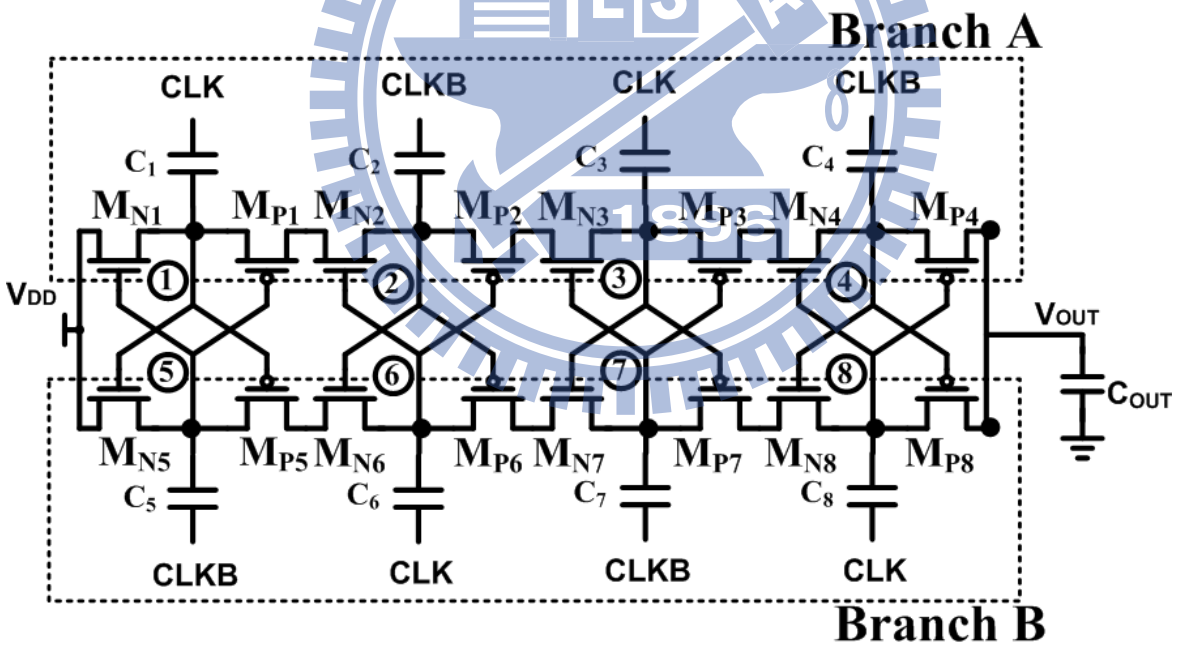


Fig. 4.10 Charge pump circuit with consideration of gate oxide reliability.

4.2.2 Charge Pump With Consideration of Gate Oxide Reliability

For avoiding gate oxide breakdown problem, the charge pump with consideration of gate oxide reliability is shown in Fig. 4.10[27]. For avoiding the body effect, the body of the devices in this charge pump circuit is advocated to be connected to their sources respectively. As shown in Fig. 4.10, there are two charge transfer branches, branch A and branch B. Branch A is composed of transistors MN1, MN2, MN3, MN4, MP1, MP2, MP3, and MP4 with the capacitors C1, C2, C3, and C4. Branch B is composed of transistors MN5, MN6, MN7, MN8, MP5, MP6, MP7, and MP8 with the capacitors C5, C6, C7, and C8. The control signals of branches A and B are entwined. Moreover, clock signals of branches A and B are out-of-phase. When the clock signals of the first and the third pumping stages in the branch A are CLK, those in the branch B are CLKB. Similarly, when the clock signals of the second and the forth pumping stages in the branch A are CLKB, those in the branch B are CLK. Thus, branches A and B can see as two independent charge pump circuits but their output nodes are connected together. Because the clock signals of the branch A and those of the branch B are out-of-phase, the voltage waveforms of nodes 1–4 and those of nodes 5–8 are also out-of-phase. Therefore, branches A and B can pump up the output voltage to high, alternately. The operations of the new proposed charge pump circuit are described as below.

In the first half cycle, the CLK is low, V51 will be V_{DD}, then MN1 will turn on to transfer charges from power supply to node 1, but the MN5 will turned off to cut off the path from node 5 to the power supply. Thus, the node 1 will be charged to V_{DD}-V_{tn}. When CLK is high in first cycle, the node 1 will be $2V_{DD}$-V_{tn} and the node 5 will be charged to V_{DD}. Thus, the V51 will be – (V_{DD}-V_{tn}), then MP1 and MN2 will turn on to transfer charges from node 1 to node 2. In the second half cycle, the node 1 will be

discharged to V_{DD} and node 2 will be $2V_{DD}$. When CLK is high in second cycle, the node 1 will be $2V_{DD}$ and node 2 will be V_{DD}. Thus, the output voltage of this charge pump will be $5V_{DD}$.

4.2.3 Dynamic Bias Scheme

For solving body effect problem, the technique of dynamically biasing body node is carried out. The architecture shows in Fig. 4.11[29]. Its detail operations are described as below.

In first half cycle, the CLK=low and the M1, M2 are turned on, the M3 is turned off. Thus, the body of M1 is connected to terminal V_{DD}. When CLK=high in first cycle, the M1 and M2 are turned off and the M3 is turned on. Thus, the body of M1 is connected to node 1. In the following stage, when the charge-transfer MOSFET is ON, the body of the charge-transfer MOSFET is connected to the source; otherwise, connected to the drain. When the voltage is pumped up, the body will be pumped up too. Thus, the pumping efficiency will not be decreased with increasing pumping stage.

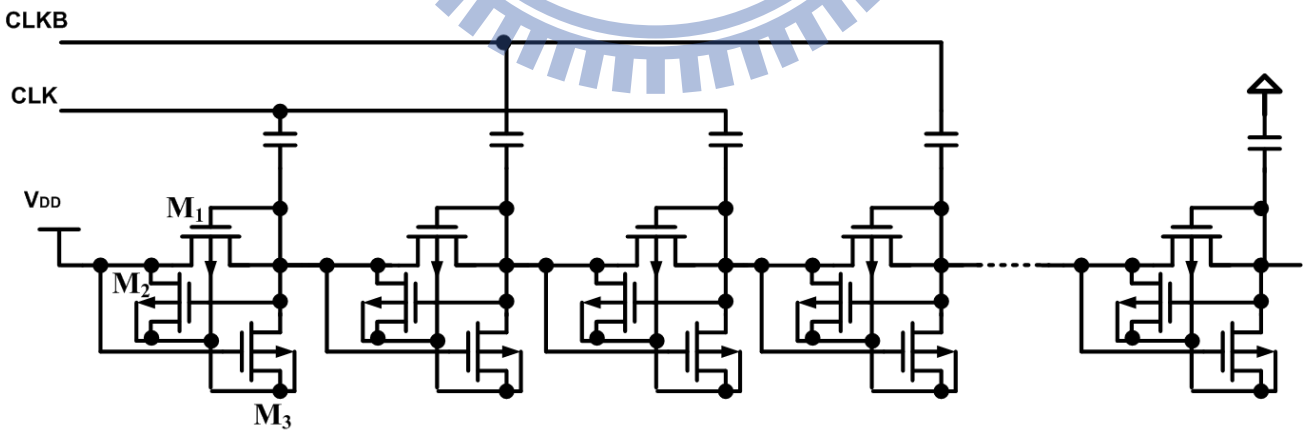


Fig. 4.11 Charge pump circuit with dynamically biasing body node.

4.3 Negative Voltage Generator

The Dickson charge pump also can be used to generate negative voltage as shown in Fig. 4.12. The operation is described below:

In the first half cycle, CLK is high, and the node 1 will be discharged to ground. When CLK is low in first cycle, the node 1 will be $-V_{DD}$ and the M1 is turned off state.

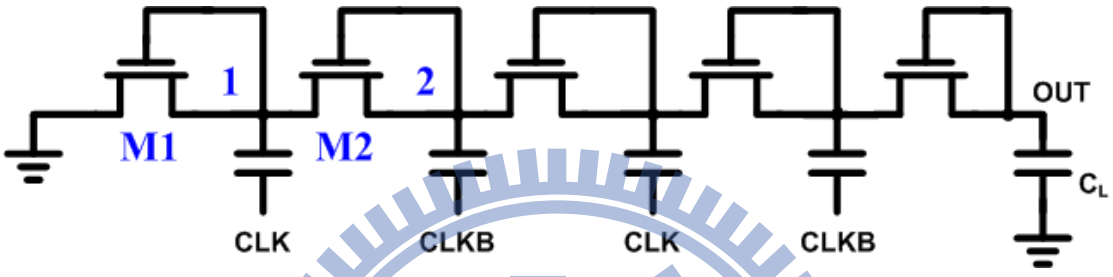


Fig. 4.12 Dickson charge pump generates negative voltage.

In this time, the M2 is turned on and the node 2 will be discharged to ground. When CLK is high in second cycle, the node 2 will be $-V_{DD}$ and node 1 will be 0. When CLK is low in second cycle, the node 2 and node 1 will be $-0.5V_{DD}$. In the end of third cycle, the node 2 will be $-0.75V_{DD}$. In the end of next cycle, the node 2 will be $-0.875V_{DD}$. Thus, the node 2 will generate negative voltage between $-V_{DD}$ and $-2V_{DD}$. Then the OUT will be discharged to $-4V_{DD}$.

4.4 Proposed Charge pump

4.4.1 Dickson Charge Pump for Improving Body Effect

For improving the body effect of Dickson charge pump, the circuit shows in Fig. 4.13. In the first cycle, when CLK is low, the node 1 is charged to $V_{DD}-V_{tn1}(t)$, the $V_{tn1}(t)$ is threshold voltage of MN1:

$$V_{tn1}(t) = V_{t0} + \gamma\left[\sqrt{V_{sb} + 2\phi_f} - \sqrt{2\phi_f}\right]$$
$$= V_{t0} + \gamma\left[\sqrt{(-V_{DD}) + 2\phi_f} - \sqrt{2\phi_f}\right]$$

Therefore, the $V_{tn1}(t)$ is smaller than the threshold voltage of NMOS's body connecting to ground. When CLK is high in first cycle, the node 1 is $2V_{DD}$-$V_{tn1}(t)$. In this time, the threshold voltage of MN1 is $V_{tn1}(t+1)$:

$$V_{tn1}(t+1) = V_{t0} + \gamma\left[\sqrt{V_{sb} + 2\phi_f} - \sqrt{2\phi_f}\right]$$
$$= V_{t0} + \gamma\left[\sqrt{(V_{DD} - V_{tn1}(t)) + 2\phi_f} - \sqrt{2\phi_f}\right]$$

Hence, the leakage flow from node 1 to V_{DD} is reduced. As the voltage pump up in following stages, the threshold voltage of NMOS in every stage is the same as $V_{tn1}(t)$ and improves the body effect.

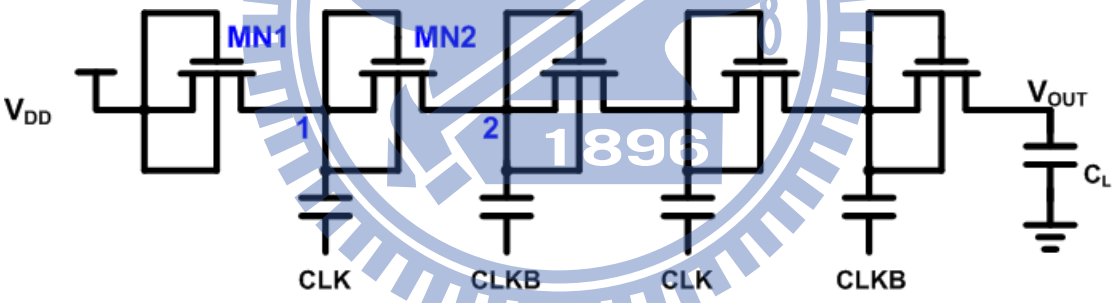


Fig. 4.13 Charge pump for improving body effect.

The comparison of proposed charge pump with previous works is shown in Fig. 4.14 and Fig. 4.15. Charge pumps in this comparison are four stages. The simulation results show that the proposed charge pump has better loading capability and highest power efficiency.

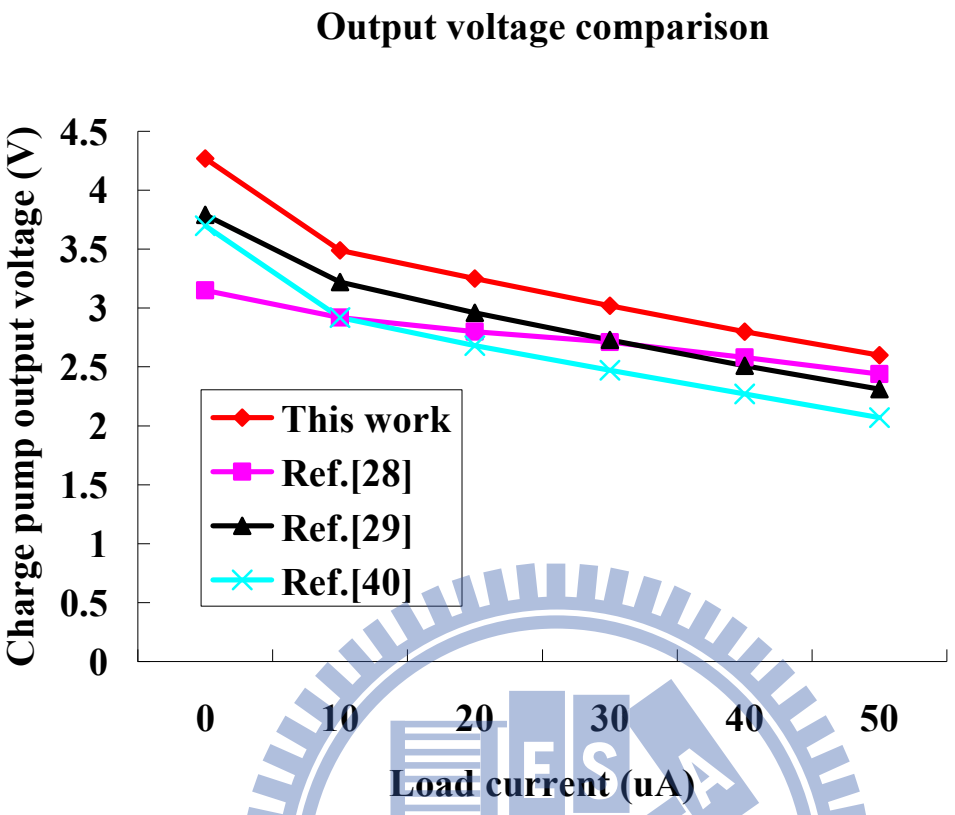


Fig. 4.14 Output voltage of charge pumps in different load current.

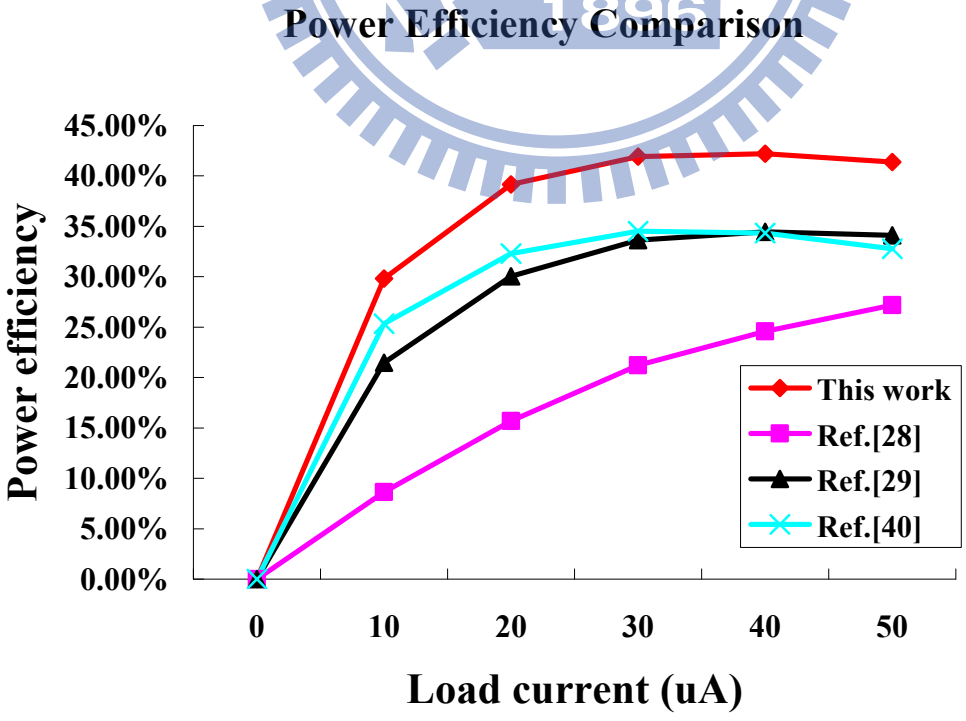


Fig. 4.15 Power efficiency of charge pumps in different load current.

4.4.2 A New Connect Scheme of Charge Pump

For flash memory applications to generate ultra high voltage, the architecture in Fig. 4.10 is implemented. We can cascade more stage to pump up high voltage. Base on this architecture, we carried out a new connect scheme for ultra high voltage generation as shown in Fig.4.16.

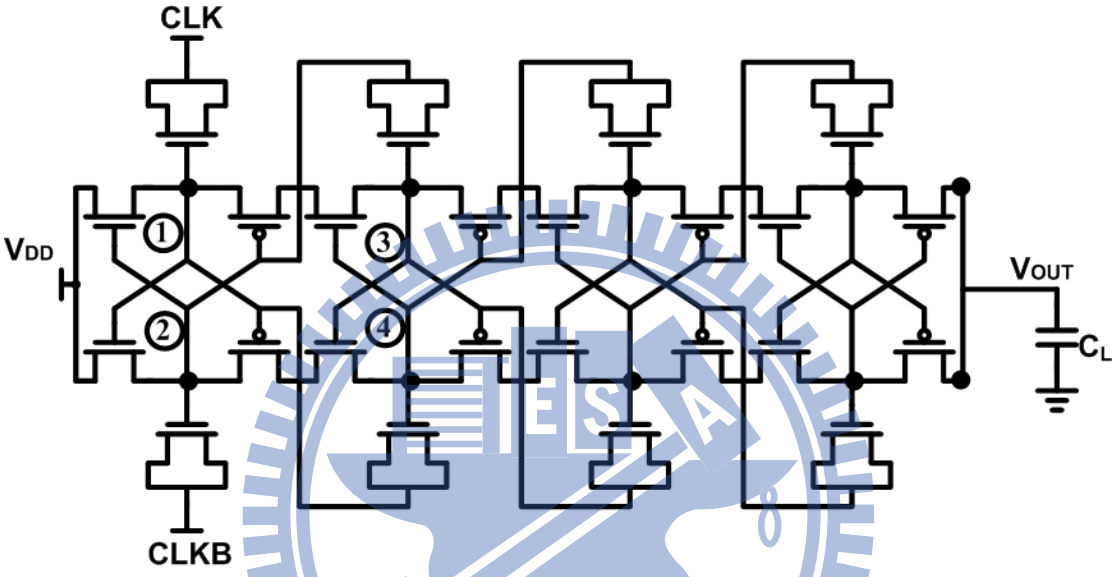


Fig 4.16 the new charge pump connection scheme with MOS capacitor.

In Fig. 4.10, we know that node 1 swings between V_{DD} and $2V_{DD}$. The node 6 will swing between $2V_{DD}$ and $3V_{DD}$ due to the CLK signal swings between 0 and V_{DD}. Base on this concept, we can connect the CLK node of C6 to node 1 due to node 1 swings between V_{DD} and $2V_{DD}$. And we can connect the CLKB node of C2 to node 5 due to node 5 swings between $2V_{DD}$ and V_{DD}. Therefore, the operation of overall architecture is the same as Fig. 4.10. Besides, in this architecture, we can use MOS capacitor to replace off-chip capacitor. In Fig. 4.10, the maximum cross voltage of C2, C3 and C4 are $2V_{DD}$, $3V_{DD}$ and $4V_{DD}$, respectively. And the maximum cross voltage of C6, C7 and C8 are $2V_{DD}$, $3V_{DD}$ and $4V_{DD}$, respectively. If we want to use MOS capacitor to replace the off-chip capacitor in Fig. 4.10, the special mask is needed to prevent the break down of CMOS. In Fig. 4.16, the maximum cross voltage of MC1 ~

MC8 are V_{DD} Thus, the architecture in Fig. 4.16 can be implemented in standard CMOS process without using special mask to avoid the break down of CMOS.

As mention before, the charge pump pumps input current to the output by pumping current to each stage which is controlled by clock. While the charge pump is at the initial condition, the internal nodes of the charge pump are the not pumped up voltage. For fast pumping up the output voltage, we add the diode connected connection as shown in Fig.4.17 to these internal nodes. When each stage is pumped up, then the diode connected connection is open. And at the output stage, there is also the diode connected connection for improving output loading current capability. Fig.4.18 and Fig.4.19 show the circuit operation for current charging and the transient response.

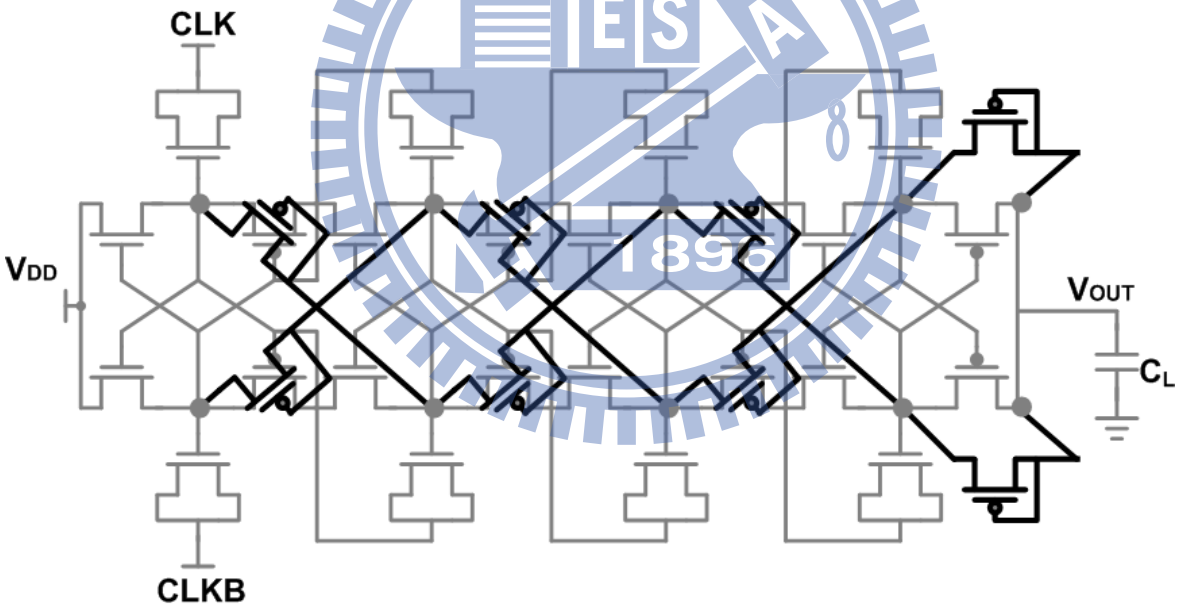


Fig 4.17 the new charge pump connection scheme with diode connected connection.

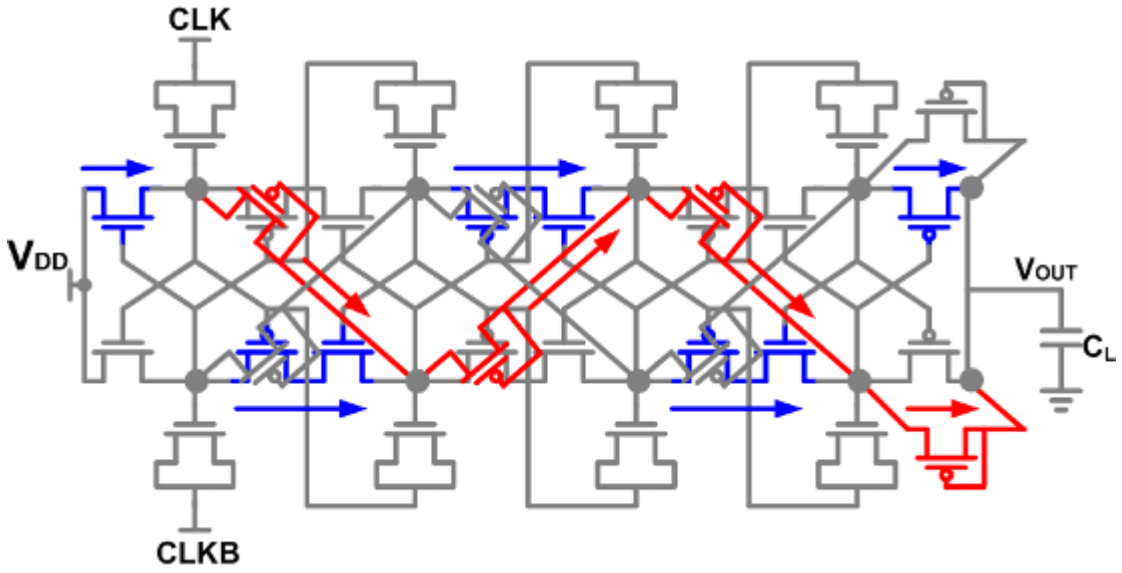


Fig 4.18 The circuit operation for current charging.

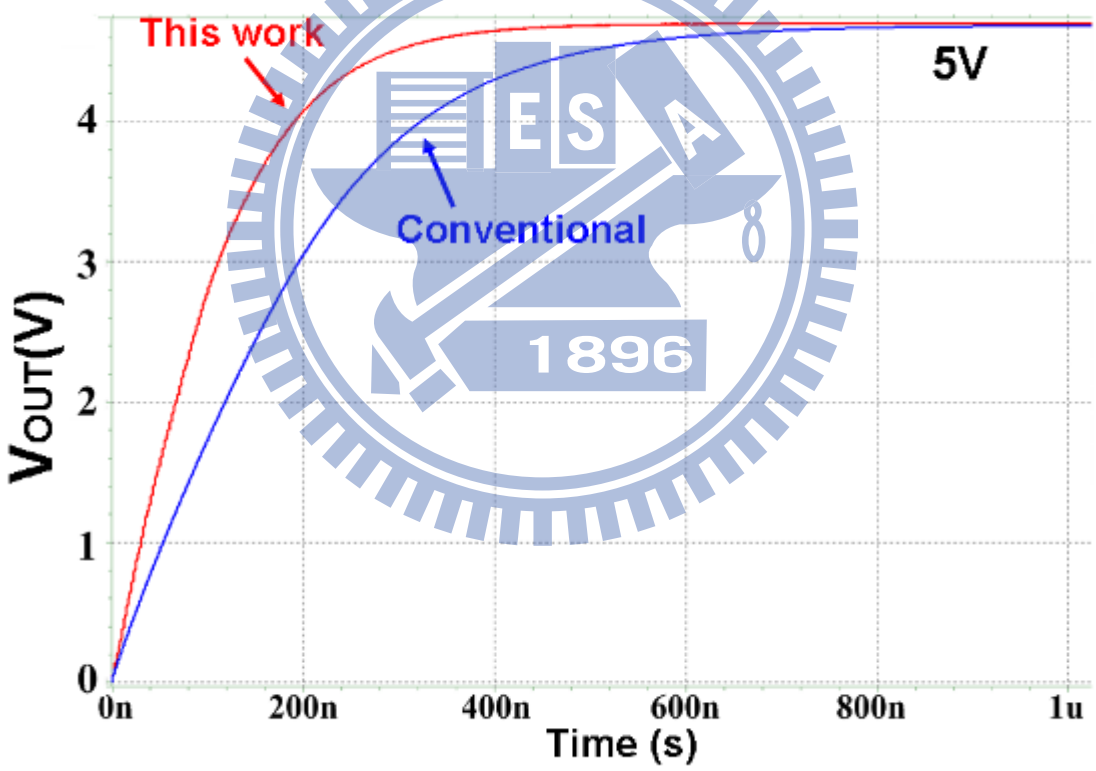


Fig 4.19 The transient response of the new charge pump.

The comparison of [27] and proposed charge pump shows in Fig. 4.20 and Fig. 4.21. The simulation results show that the loading capability and power efficiency of proposed charge pump is nearly the [27] 1.5pF and is better than [27] 1pF.

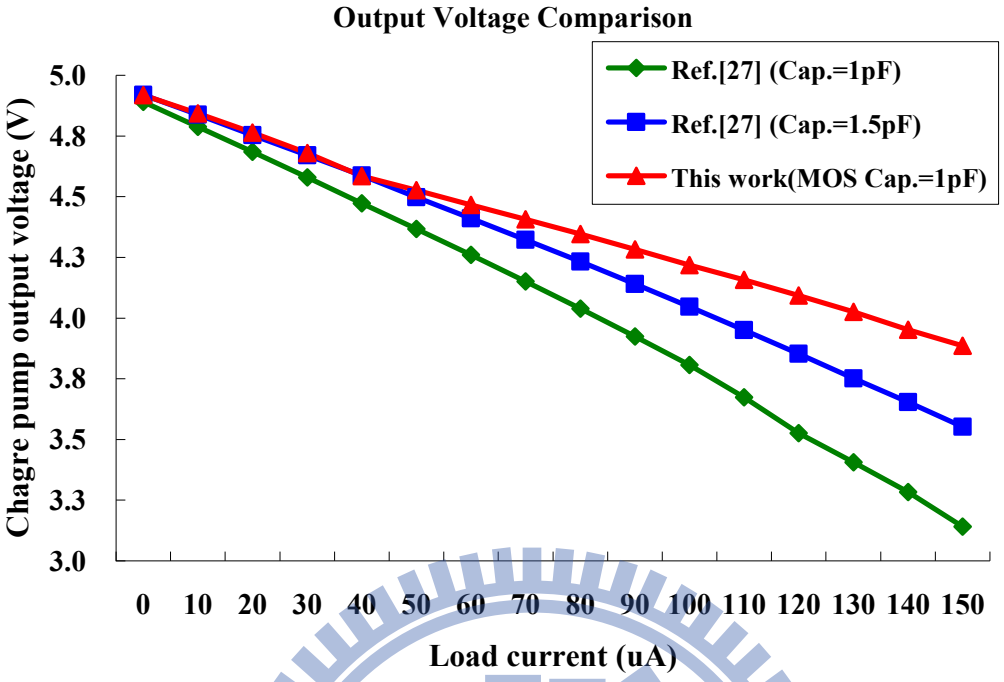


Fig. 4.20 Charge pump output voltage vs. different load current.

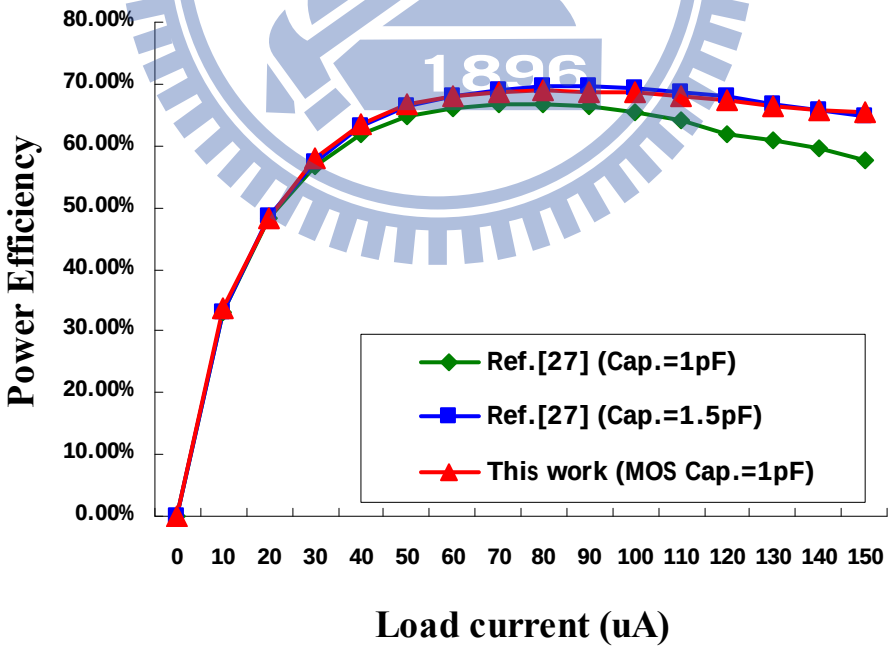


Fig. 4.21 Power efficiency of charge pumps in different load current.

4.5 Summary

In this chapter, the voltage doubler and Dickson charge pump are described. The techniques of improving Dickson charge pump's pumping efficiency are also demonstrated. For flash memory applications, ultra high voltage and negative voltage are utilized for programming and erasing the information in flash memory. To generate ultra high voltage, the gate oxide reliability is considerable. The charge pump designs with gate oxide reliability considering are introduced. The negative voltage generator is also introduced.

Finally, we proposed a new connection scheme for improving pumping efficiency of Dickson charge pump and a new connection scheme for generating ultra high voltage. The proposed solution of Dickson charge pump's body effect problem has the better loading capability and better power efficiency. The proposed new connection scheme improved the loading capability and power efficiency of the charge pump. The charge pump with the new connection scheme can be implemented in standard CMOS process without using special process to prevent the break down of CMOS. And the diode connection scheme can fast pump up output voltage and provide better loading capability.

Chapter 5 High Efficiency Power Management System for Solar Energy Harvesting

An integrated power management system for solar energy harvesting applications is proposed. The power management system receives power from photovoltaic (PV) cell and generate different voltage levels which are suitable for SoC integrated regulator applications (such as 1V~0.3V for analog circuitry and low power digital circuitry, -1.2V for memory circuitry, and 5V for I/O components). The power management system also contains a rechargeable battery which is charged by multi-phase maximum power tracking (MPT) circuitry with the PV cell module. With the MPT circuitry, the power of PV cell can be regulated in the maximum power region. The power efficiency of the MPT circuitry is average about 80%~73%. All results are simulated in UMC 90nm CMOS technology model.

In section 5.1, we will discuss the several kinds of scheme in this system for chosen consideration. The overview of power management system is shown in Section 5.2. The detail circuitry and the characteristic of PV cell are shown in Section 5.3. The results are simulated in UMC 90nm CMOS technology and are shown in Section 5.4. Finally, we will conclude the power management for solar energy harvesting applications in Section 5.5.

5.1 The Scheme of Power Management System for Solar Energy Harvesting Applications

In the application of [41], the system accepts energy from PV cell and provides for the negative voltage generator, the high voltage generator, and the voltage regulator. The system contains rechargeable battery. So, there are a PV cell, a rechargeable battery, a voltage regulator and a charge pump in this system. There are several kinds of scheme in this system for chosen consideration.

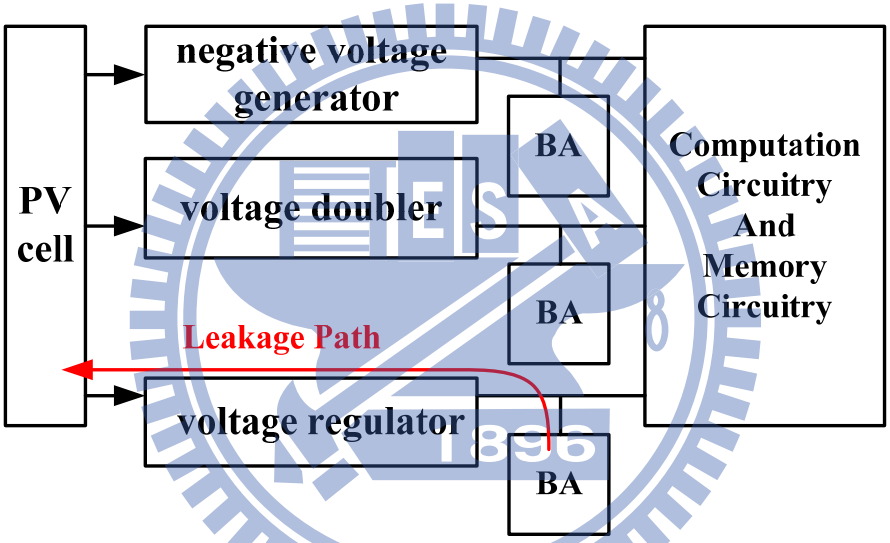


Fig. 5.1 First kind scheme of power management system.

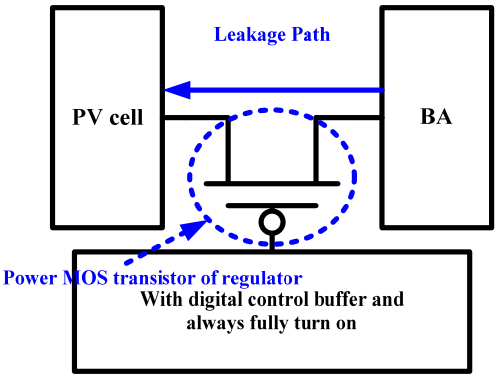


Fig. 5.2 Leakage path of first kind scheme.

1) Case I scheme :

The first kind scheme is shown in Fig. 5.1. The PV cell supplies the negative voltage generator, the high voltage generator and the voltage regulator. The batteries are placed in the output node of every voltage generator.

Drawbacks :

1. This scheme needs tree batteries and need three output pins.
2. The battery in the output of the voltage regulator with digital output buffer has a serious leakage path. When PV cell do not supply energy, there are current flow from battery to PV cell, as shown in Fig. 5.2. As we want the regulator has low drop out, the size POWER MOS must be very large. Thus, the leakage will increase. It is complicated to design a control mechanism for decreasing leakage, because the POWER PMOS must be controlled by the signal from op amp to keep the output voltage of the voltage regulator the same as Vref.
3. The PV cell variation will affect significantly. If the PV cell varies ΔV, the variation will directly affect the output voltage by a multiple of ΔV.

2) Case II scheme :

The second kind scheme is shown in Fig. 5.3. The PV cell supplies the negative voltage generator, the voltage regulator. The high voltage generator is supplied by the voltage regulator. The batteries are placed in the output node of the negative voltage generator and the voltage regulator.

Drawbacks :

1. This scheme needs two batteries and need two output pins.

2. Due to the high voltage generator is charge pump. The size of capacitor in the high voltage generator will be large, because it supplies power to the voltage regulator. If the size of capacitor in the high voltage generator is not large enough, the loading capability of the high voltage generator will be decreased. As the size of capacitor increase, the power consumption of charge pump also increases due to the clock charge and discharge the capacitor at every moment.

3. The PV cell variation will affect significantly. If the PV cell varies ΔV, the variation will directly affect the output voltage by a multiple of ΔV.

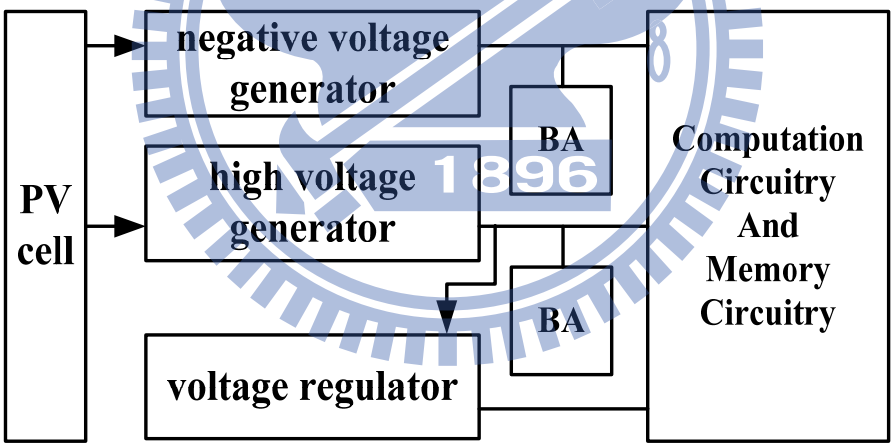


Fig. 5.3 Second kind scheme of power management system.

3) Case III scheme :

The third kind scheme is shown in Fig. 5.4. The PV cell supplies voltage to the voltage regulator. The high voltage generator and negative voltage generator is supplied by the voltage regulator. The batteries are placed in the output node of the

voltage regulator. This scheme needs only one battery and it solve the output variation of high voltage generator and negative voltage generator, because the voltage regulator will regulate the output voltage of PV cell. But it has the same leakage path as shown in Fig. 5.2.

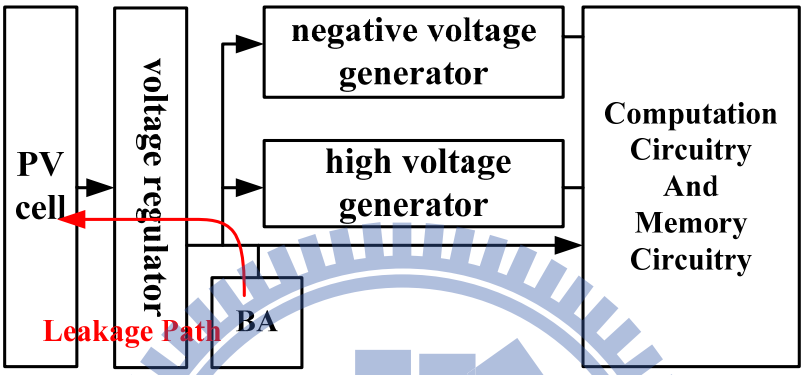


Fig. 5.4 Third kind scheme of power management system.

4) Case IV scheme :

The fourth kind scheme is shown in Fig. 5.5. The battery charger controls the PV cell output voltage and charges the battery. The high voltage generator, the negative voltage generator and the voltage regulator is supplied by the battery. This scheme needs only one battery. The variation problem of is solved by with the battery charger. Although it has a directly leakage path from battery to PV cell, we can add a shutdown mechanism to turn off the battery charger when PV cell is no supply energy.

Base on above discussion, we decide using the fourth kind scheme and add a battery charger to control the PV cell output voltage with the PV cell maximum power control method.

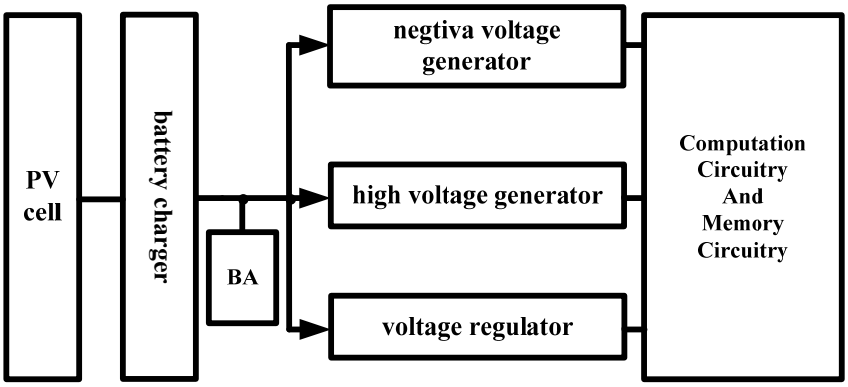
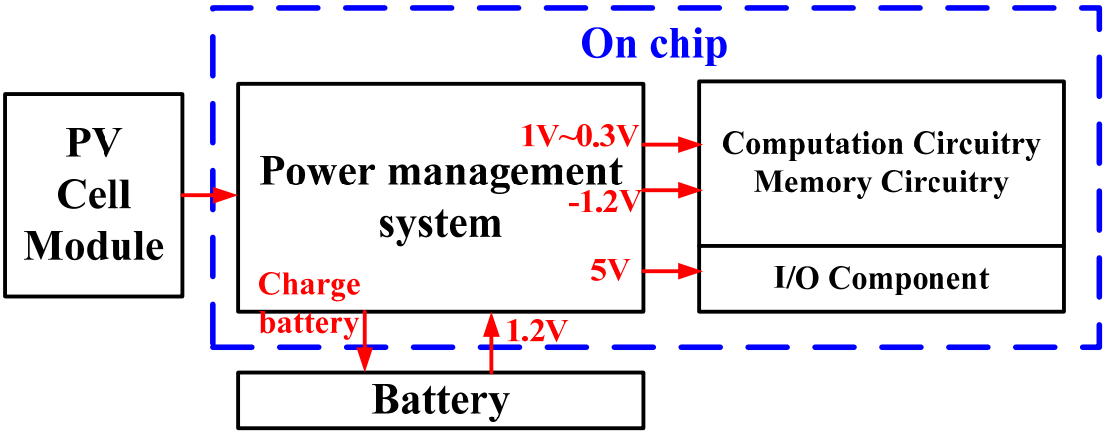


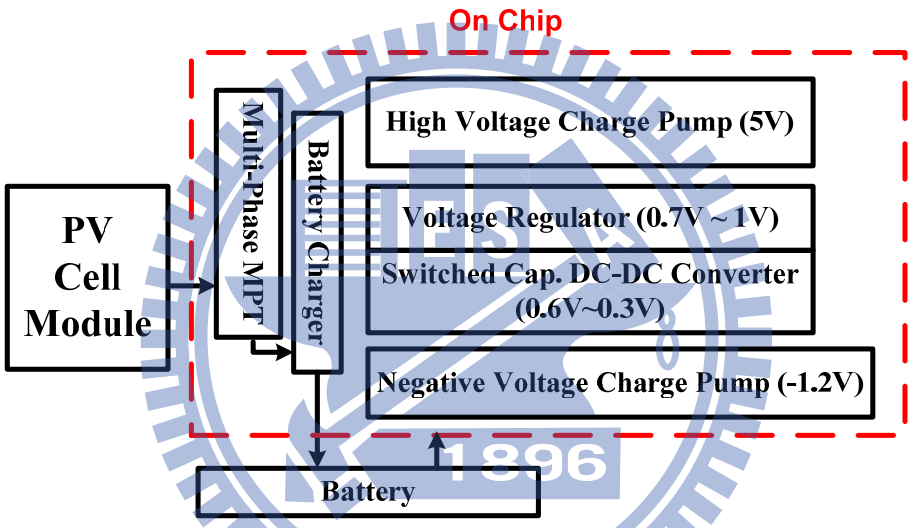
Fig. 5.5 Fourth kind scheme of power management system.

5.2 The Overview of Power Management System for Solar Energy Harvesting Applications

In this work, we develop a high efficiency power management system that is powered by solar energy and outputs different voltage levels for computation circuitry, memory circuitry, and I/O components, as shown in Fig. 5.6(a). The circuit of this system is designed for low power SoC applications. We also propose a multi-phase maximum power tracking circuitry with the PV cell module for regulating the PV cell module in the maximum power region. A switched capacitor (SC) DC-DC converter and a voltage regulator are utilized to supply different voltage levels for dynamic voltage scaling applications. High voltage charge pump and negative voltage charge pump also supply high voltage and negative voltage for overall SoC applications.



(a) Block diagram of the overall system.



(b) Architecture of the power management system.

Fig. 5.6 (a) Block diagram of the overall system. (b) Architecture of the power management system.

The proposed power management system is shown in Fig. 5.6(b). The power management system contains a PV cell module, a multi-phase maximum power tracking circuitry, a voltage regulator, a SC DC-DC converter, a high voltage charge pump, a battery charger and a negative voltage charge pump.

The maximum power tracking circuitry regulates the PV cell I-V characteristic in the maximum power region instead of arbitrary output voltage. The voltage charger

will charge the battery form energy buffer of MPT circuitry. The voltage regulator outputs voltage form 1V~0.7V and the SC DC-DC converter outputs voltage from 0.6V~0.3V which are able to provide the SoC system dynamic voltage. And the high voltage charge pump generates 5V for I/O components by utilizing new connection scheme to replace the off-chip capacitors by NMOS capacitors. The PV cell and battery are also implemented in circuit model and simulated with power management system.

5.3 PV Characteristic and Detail Circuitry

5.3.1 Photovoltaic (PV) Cell

The I-V curve and Power-V curve of PV cell is shown in Fig. 3. The left y-axis is PV cell output current. The right y-axis is PV cell output power. The output voltage of PV cell is between 1V and 0V. The maximum output power of PV cell is 1.32 mW.

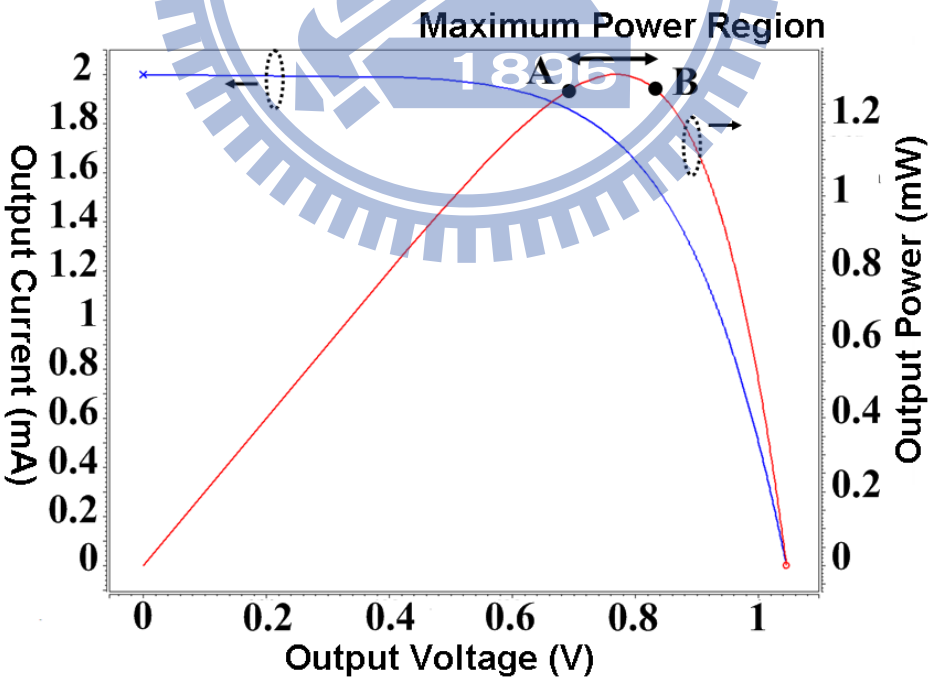


Fig. 5.7 P-V and I-V curve of PV cell. The x-axis is output voltage of PV cell. The left y-axis is load current. The right y-axis is output power.

5.3.2 Maximum Power Tracking (MPT)

The schematic of maximum power tracking circuitry is shown in Fig. 5.8. As shown in Fig. 5.7, the MPT circuitry controls V_{SET} and regulates PV cell output current. The corresponding PV cell output voltage is therefore controlled not to exceed point B. So the output power of PV cell will remain in the maximum power region.

The PV cell output current is sensed by M_S and converts current value to voltage value by R_S. And clock controlled switches sample voltage values to store at S_1 and S_2. When PV cell output voltage passes point A shown in Fig. 5.7, the comparator will detect that S_2 is smaller then S_1 which is over the comparator threshold, and send control signal to reduce V_{SET} for avoiding PV cell output voltage across point B. When the comparator detects that S_2 is larger then S_1, V_{SET} will be increased again and maintain PV cell in maximum power region.

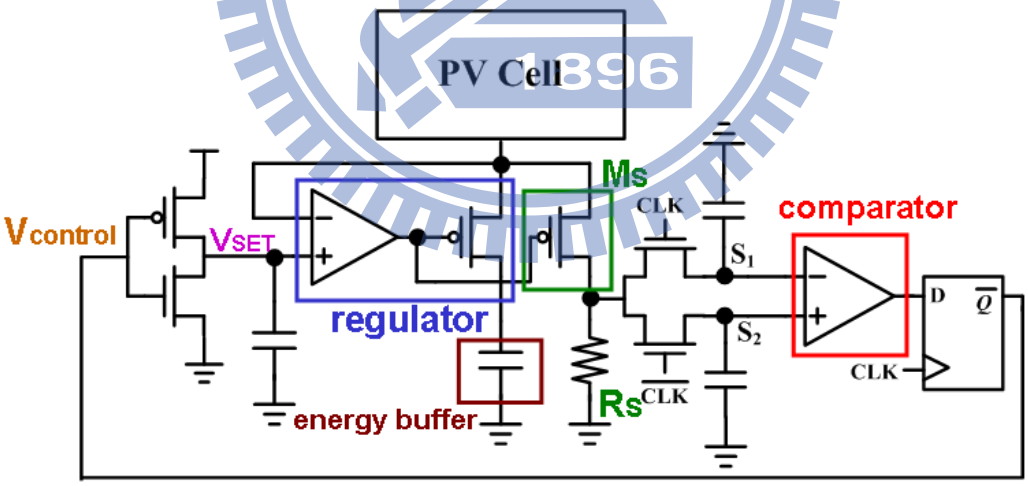


Fig. 5.8 The schematic of maximum power tracking circuitry.

For PV cell module application as shown in Fig.5.9, the multi-phase MPT circuitry will use multi-phase clocking to average total power of each PV cell. So the PV cell module will supply nearly constant average power. The battery charger will charge

the battery by pumping the energy from energy buffer. And the simulation result is shown in Fig. 5.14 and Fig. 5.17.

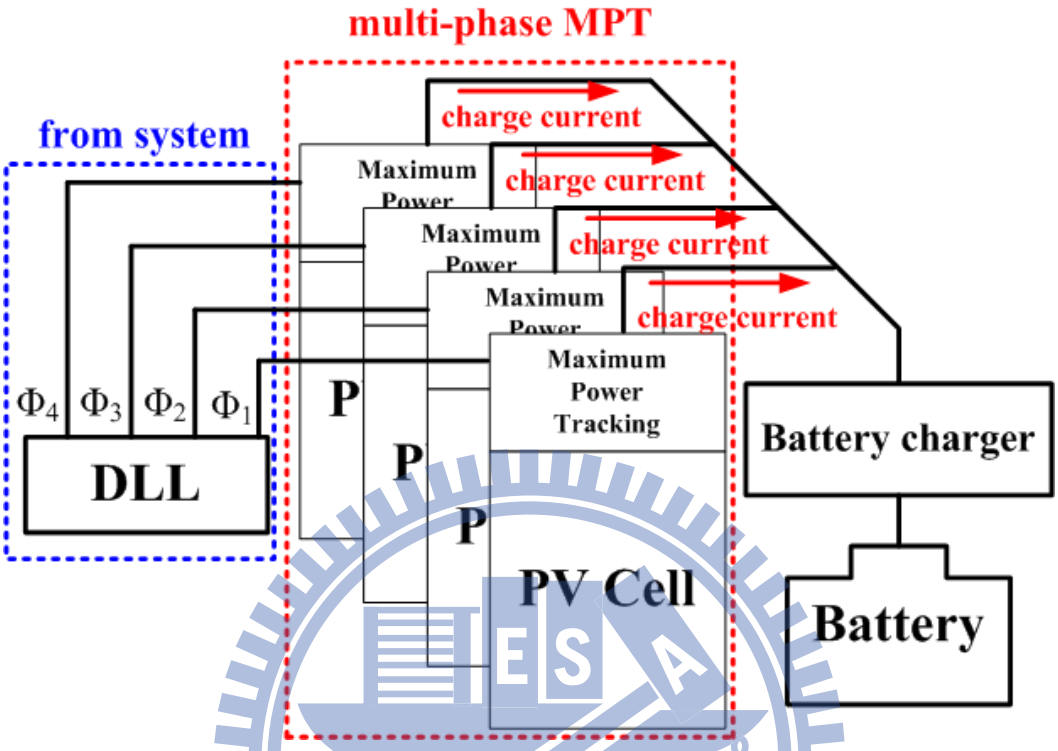


Fig. 5.9 The schematic of multi-phase MPT circuitry.

5.3.3 Voltage Regulator & Switched Capacitor DC-DC Converter

The schematic of voltage regulator and SC DC-DC converter is shown in Fig. 3.18. $V_{control}$ is given by system DAC. When supplying high power operation, the voltage regulator will supply 1V~0.7V. The schematics of the voltage regulator are shown in Fig. 3.16. When ctrl is high the voltage regulator is turned on, and ctrl is low the voltage regulator is turn off. When supplying low power operation, the SC DC-DC converter will supply 0.6V~0.3V. The SC DC-DC converter is shown in Fig. 3.18. T_1 and T_0 are the control signal of switched capacitor topology selection as shown in Fig. 3.21. When T_1 T_0 =10, the topology output voltage is 2/3 V_{DD} (V_{DD}=1.2V) and supplies 0.5V and 0.6V output voltage. When T_1 T_0 =11, the topology output voltage

is 1/2 V_{DD} and supplies 0.4V and 0.3V output voltage. When T_1 T_0 =01, the topology output voltage is 1/3 V_{DD} and supplies 0.3V output voltage for system standby and data retention. When T_1 T_0 =00, the SC DC-DC converter is disabled.

5.3.4 Variable voltage reference generation by DAC

The variable voltage reference is generated by resistor-string DAC in Fig. 5.10. The decoder selects the output voltage for variable voltage reference.

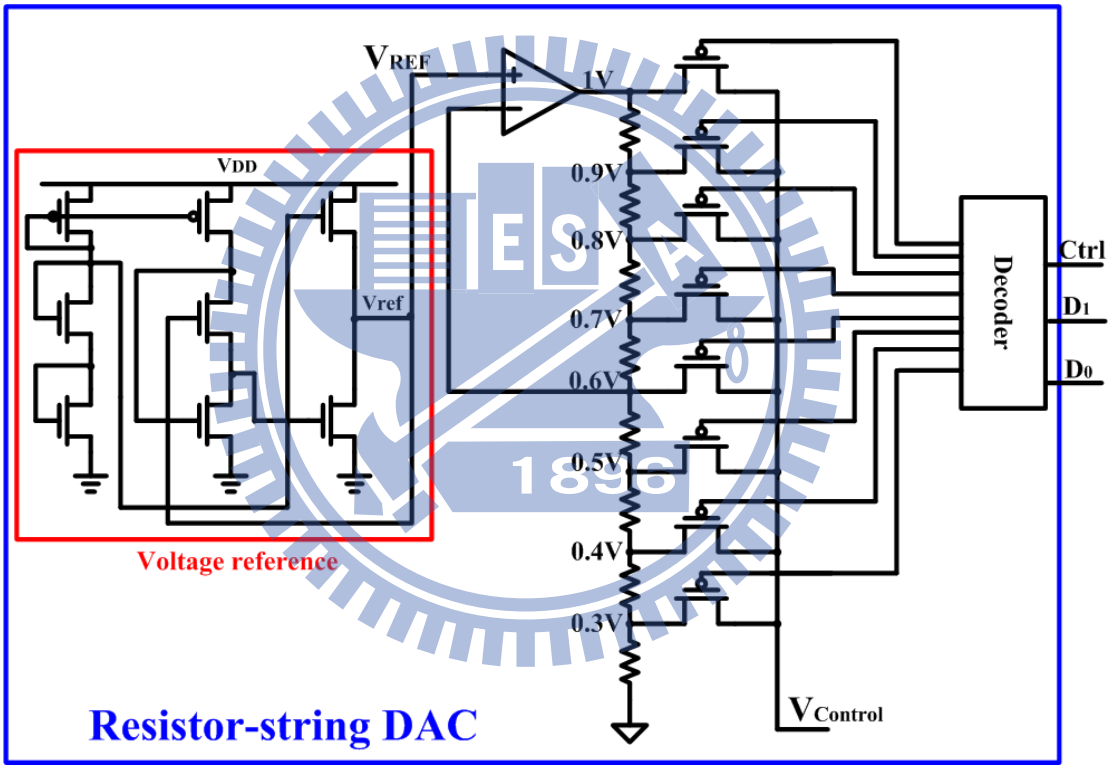


Fig. 5.10 Resistor-string DAC for variable voltage reference generation.

5.3.5 Battery Charger and Negative Voltage Generator

The circuit of battery charger and negative voltage generator is shown in Fig. 5.11. The battery charger is a voltage doubler. It accepts the supply voltage from MPT circuitry energy buffer and charge the battery. The negative voltage generator accepts ground as input voltage. When CLK is high, the voltage of node 2 is 0V and the voltage of node 1 will be “0”. When CLK is low, the voltage of node 1 will be -1.2V

and voltage of node 2 will be discharged to 0V. Then, the output voltage will be -1.2V. When CLK is high, the voltage of node 2 will be -1.2V and node 1 is 0V. Thus, the V_{OUT} node will be -1.2V.

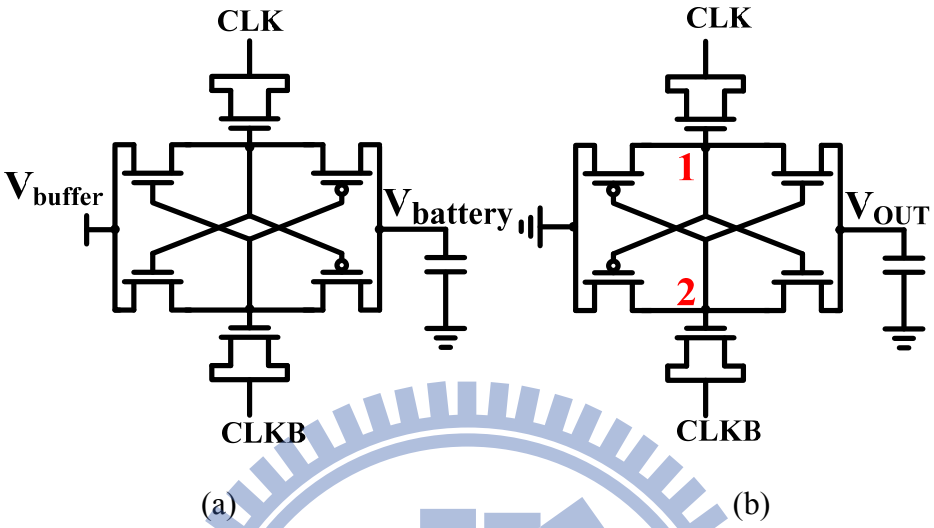


Fig. 5.11 (a) Battery charger. (b) Negative voltage generator.

5.3.6 High voltage Charge Pump

The architecture is based on [27] and replaces the off-chip capacitors by NMOS capacitors. The schematic of high voltage charge pump is shown in Fig. 5.12.

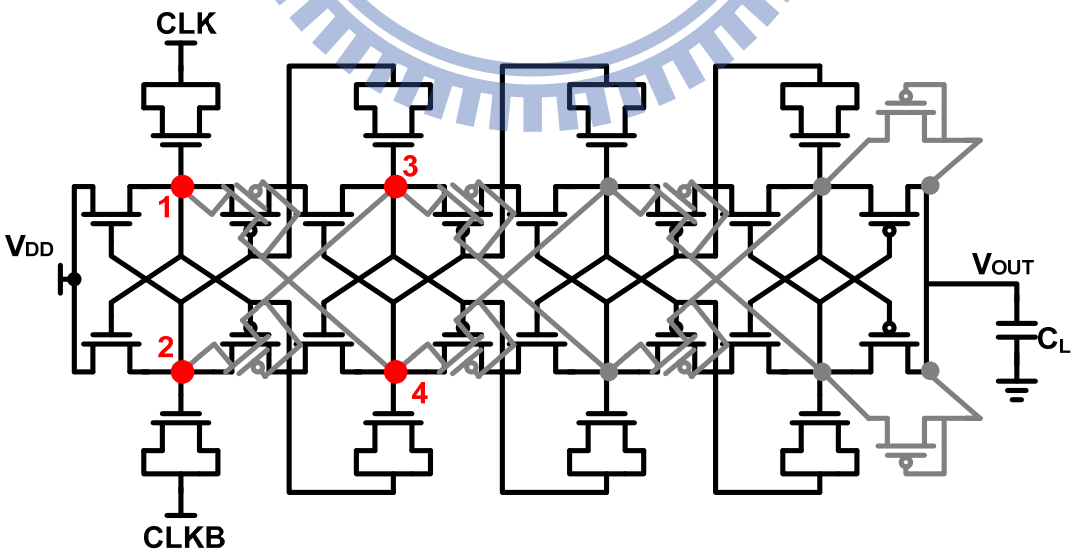


Fig. 5.12 The high voltage charge pump.

In this work, the clock generator is supplied by battery voltage source. The initial

state is that node 1 = 0V and node 2 = 0V. When CLK is high, the node 1 is 1.2V and node 2 is "1.2V-V_{tn}". When CLKB is high, the node 2 is "2.4V- V_{tn}" and the node 1 is 1.2V. As the node CLK is charge to high again, the node 1 is 2.4V. In first stage, the node 1 and node 2 will vibrate between 1.2V and 2.4V. The NMOS capacitors of second stage are connected to node 1 and node 2. Thus the node 3 and node 4 will vibrate between 2.4V and 3.6V. The node V_{OUT} will be 5V.

5.4 Simulation Results

To verify the power management system, the design is implemented in UMC 90nm CMOS technology model. Layout view of the power management system is shown in Fig. 5.13.

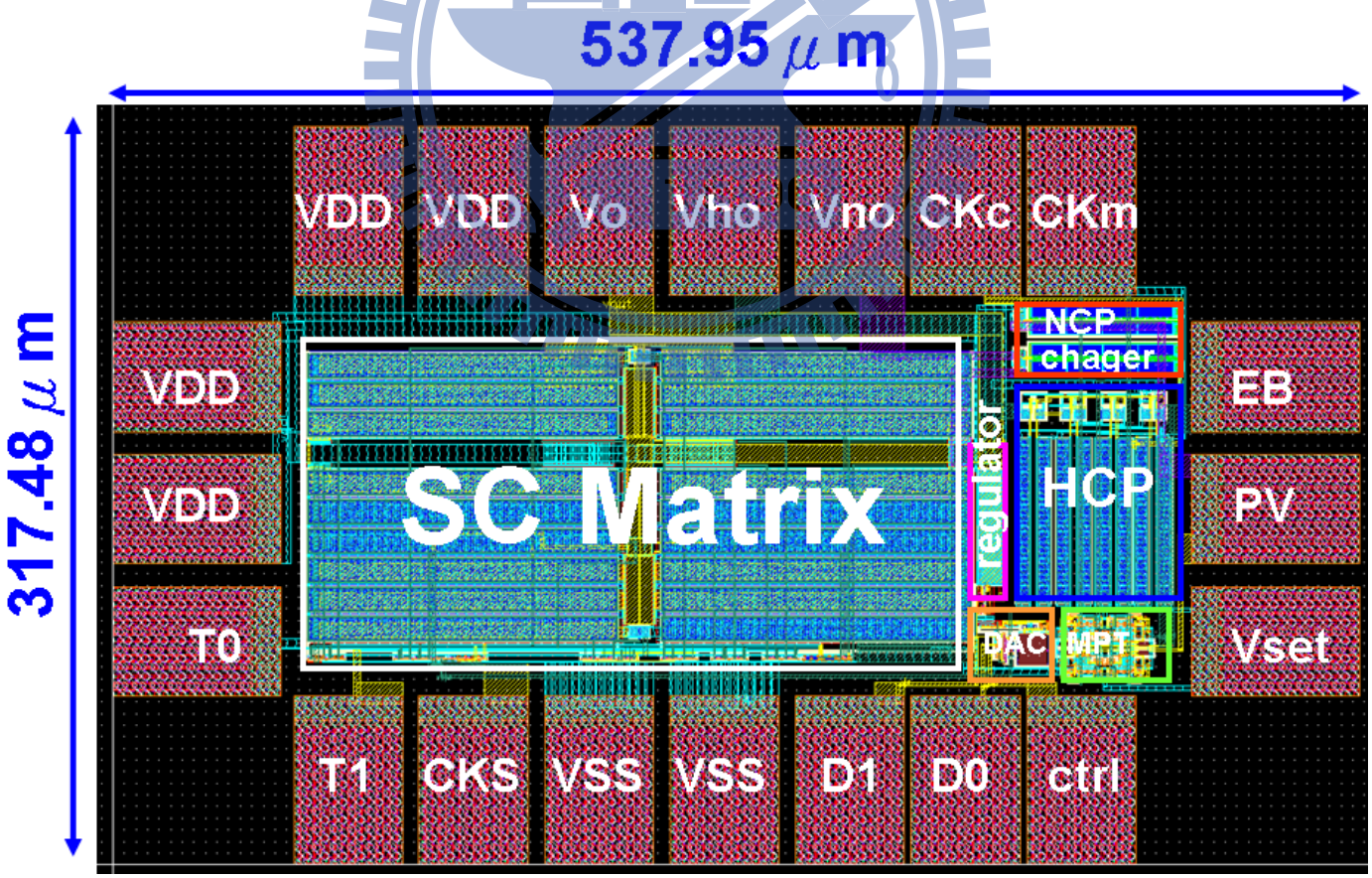


Fig. 5.13 Layout view of the high efficiency power management system for solar

energy harvesting applications.

5.4.1 Maximum Power Tracking

The first simulation is to verify the function of MPT circuitry. In this simulation the supply current of PV cell provide output current from 2mA to 0mA. The MPT of single PV cell is demonstrated in Fig. 5.14. As shown in Fig. 5.14, the PV cell outputs maximum current in the beginning, Vset and Vgate are increased to decrease the output current for searching the maximum power region of PV cell. When the output current of PV cell is decreased, the output voltage of PV cell increases as shown in Fig. 5.7. The output current of PV cell is dynamic controlled to maintain PV cell in maximum power region (1.32mW ~ 1.25mW). Fig. 5.15 shows the different corners transient response. Fig. 5.16 shows the energy charging transient response of energy buffer.

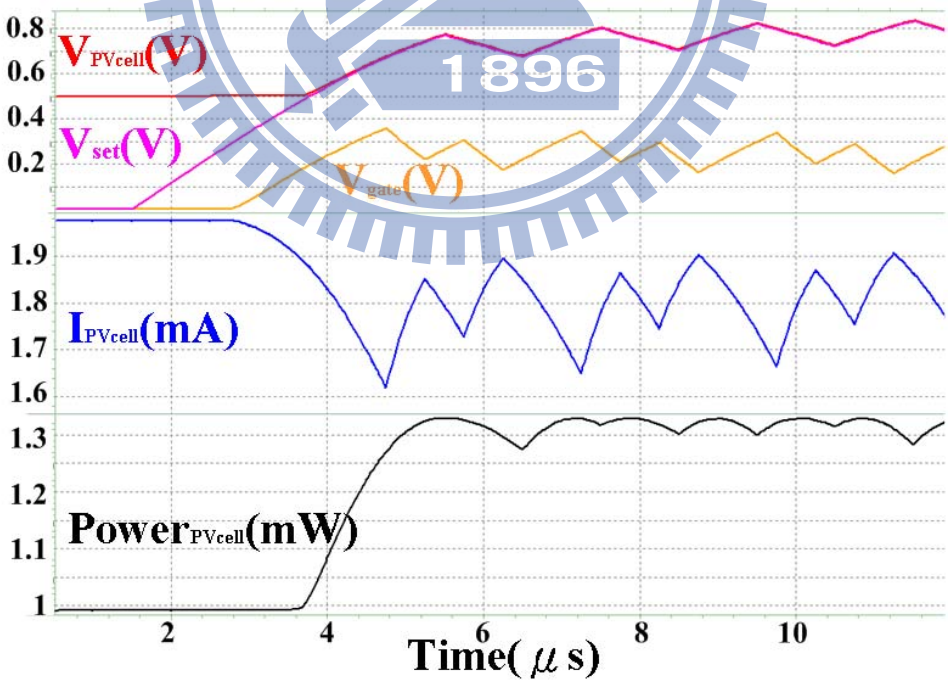


Fig. 5.14 Single PV cell maximum power tracking transient response.

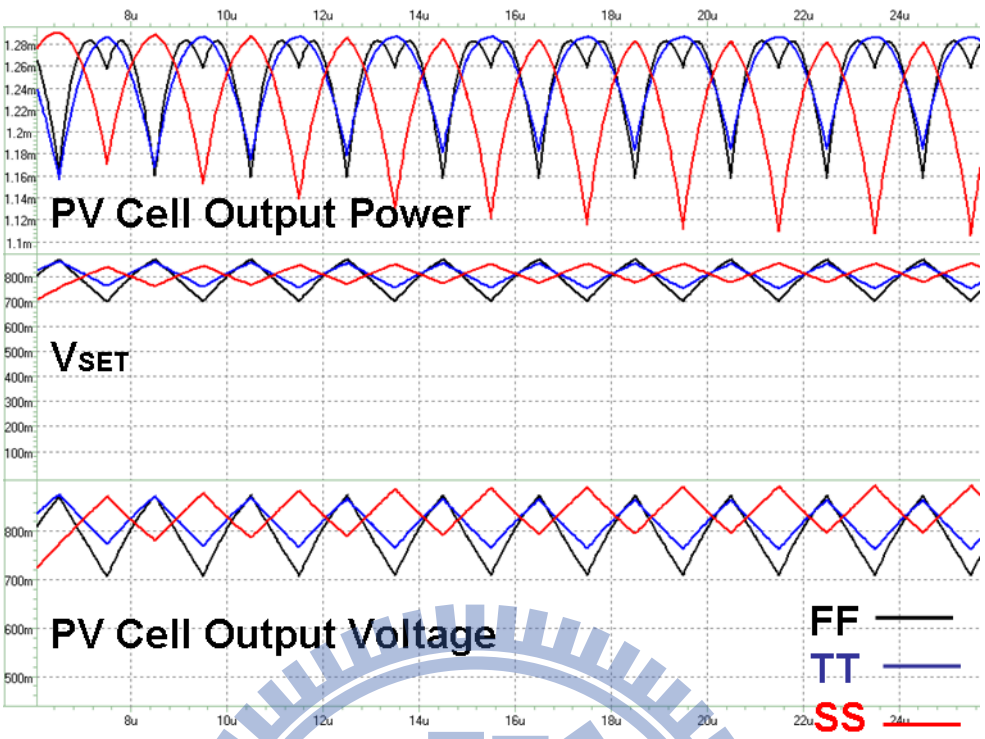


Fig. 5.15 Single PV cell maximum power tracking transient response with different process corner.

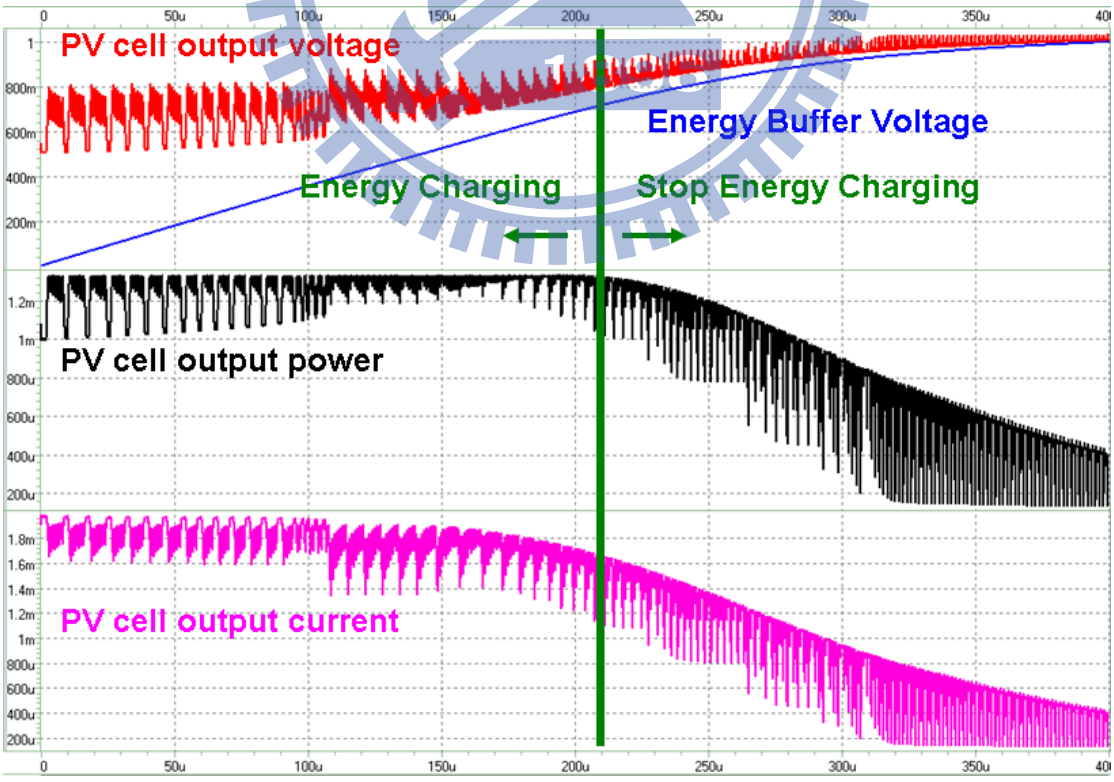


Fig. 5.16 The energy charging transient response of maximum power tracking.

Fig. 5.17 shows the multi-phase MPT with PV cell module. There are four MPT circuitries which are controlled by four different clock phases. The multi-phase control scheme can average the output power ripple. The average output power of PV cell module for each single PV cell is near the maximum power value.

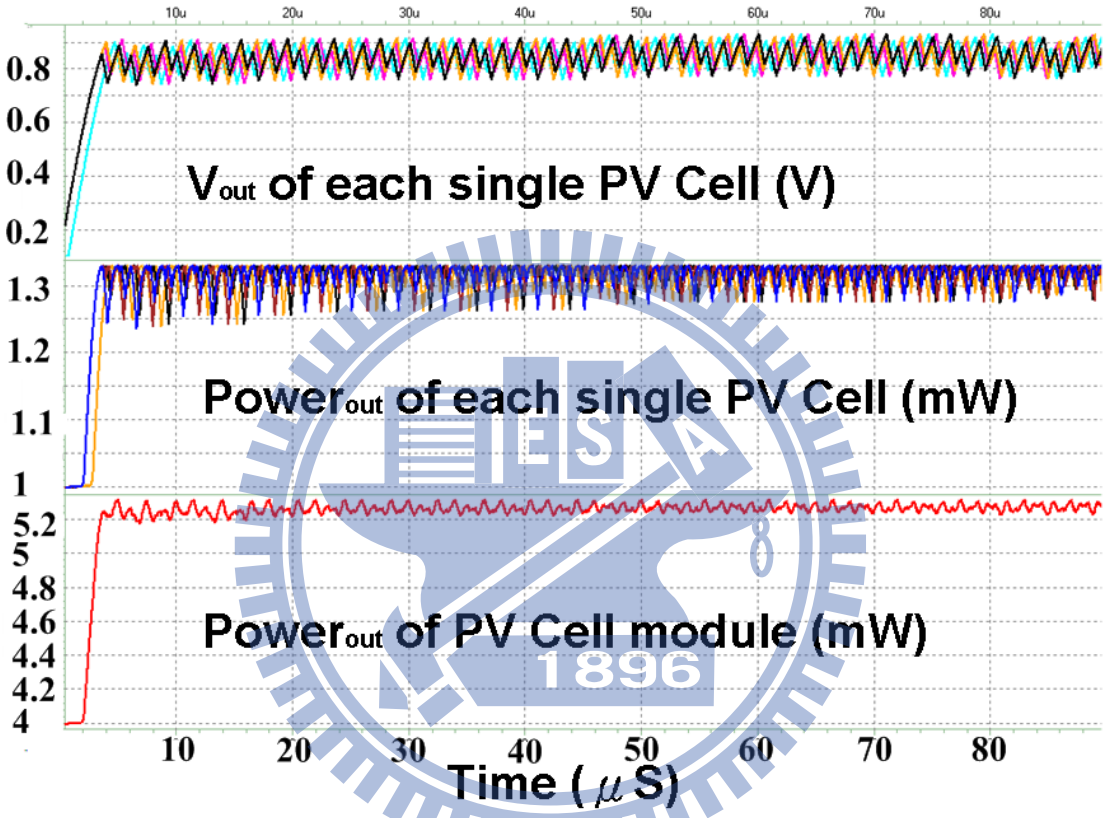


Fig. 5.17 The energy charging transient response of the multi-phase maximum power tracking.

5.4.2 Variable Reference Voltage

The variable voltage reference is generated by resistor-string DAC in Fig. 5.10. The decoder selects the output voltage for variable voltage reference. The simulation result is shown in Fig. 5.18 and Table 5.1.

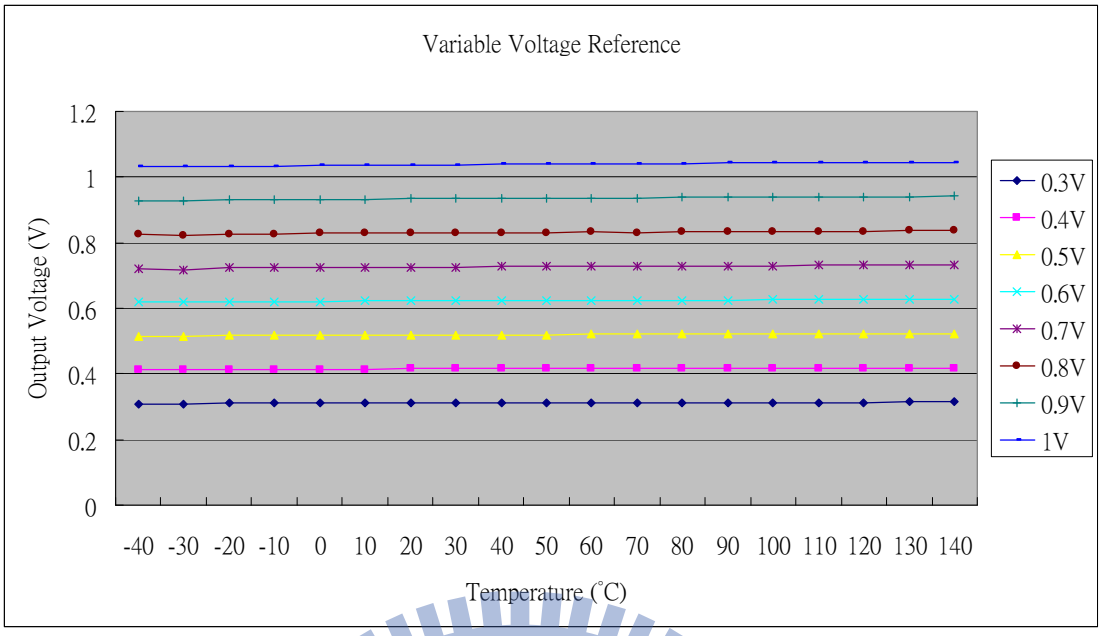


Fig. 5.18 Variable voltage reference generation with temperature variation.

Table 5.1 Temperature variation				
Temperature	**-40˚C**	**30˚C**	**140˚C**	**Variation**
1V	1.03	1.038	1.045	0.015V
0.9V	0.927	0.934	0.941	0.014V
0.8V	0.824	0.828	0.836	0.012V
0.7V	0.718	0.726	0.732	0.014V
0.6V	0.618	0.622	0.627	0.009V
0.5V	0.515	0.519	0.523	0.008V
0.4V	0.412	0.415	0.418	0.006V
0.3V	0.31	0.311	0.314	0.004V

5.4.3 Voltage Generation

The voltage generation of voltage regulator, SC DC-DC converter, negative voltage generator and high voltage charge pump are shown in Fig. 5.18. The voltage regulator

and SC DC-DC converter are able to provide voltage form 1V~0.3V. When Ctrl is low, the voltage regulator supplies 1V~0.7V. When Ctrl is high, the SC DC-DC converter supplies 0.6V~0.3V. The negative voltage generator can generate -1.2V and the high voltage charge pump can supply 5V. The specifications of power management system is summarized in Table 5.2. The system can receive energy from PV cell and generate different voltage for low power SoC applications, and the power efficiency of MPT is about 73%~80%.

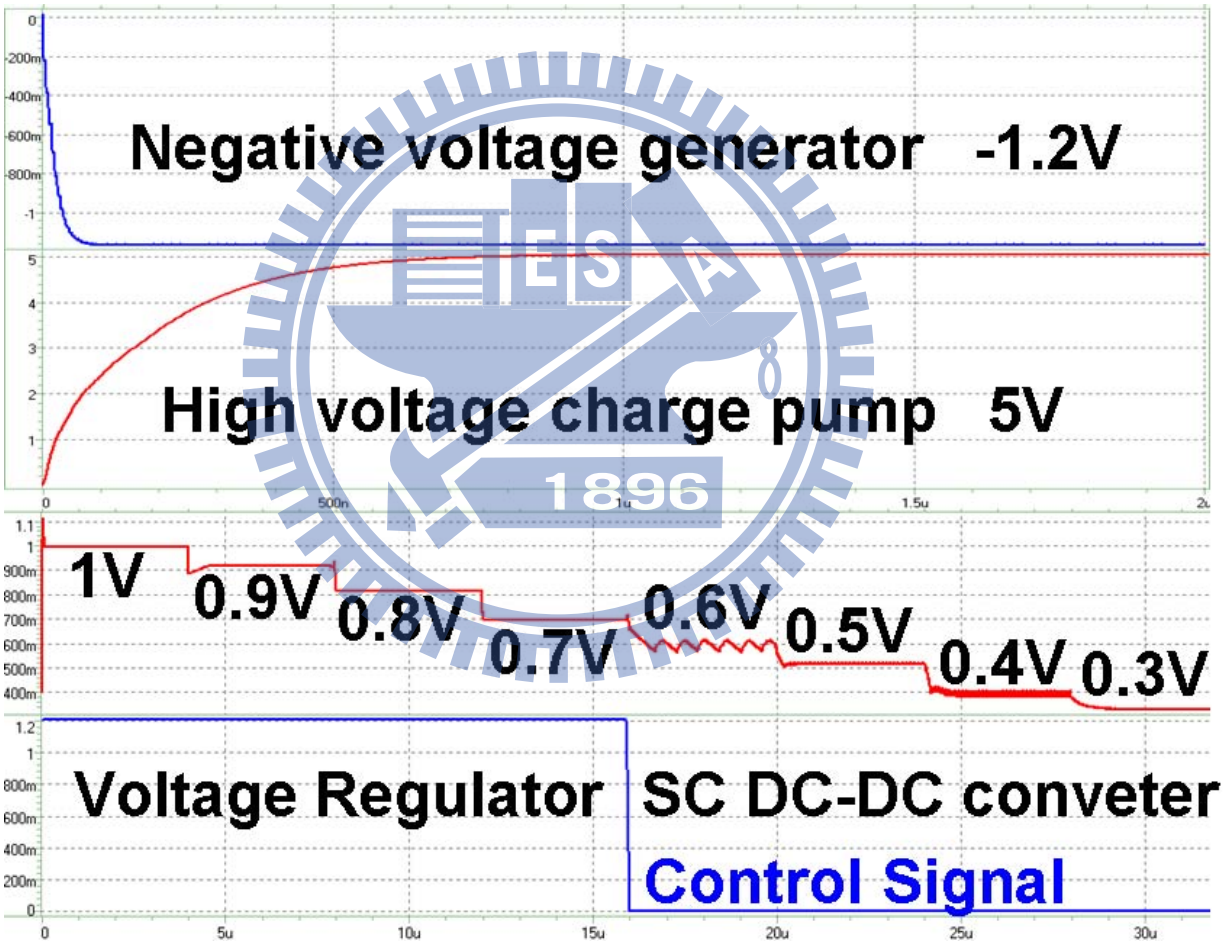


Fig. 5.18 The energy charging transient response of maximum power tracking.

Table 5.2 Power management system for solar energy harvesting.

Technology	Technology UMC 90nm CMOS
Output current of PV cell	2mA~0mA
Output voltage of PV cell	1V~0V
Output power of PV cell	1.32mW~0mW
SC DC-DC converter	0.3V~0.6V
Voltage regulator	1V~0.7V
Negative voltage generator	-1.2V
High voltage charge pump	5V
MPT power efficiency	80%~73%

$$Power\ efficiency = \frac{P_{solar\_in}}{P_{solar\_in} + P_{control\_circuit}}$$

5.5 Summary

An integrated power management system is proposed. The power management system works with PV cell and rechargeable battery. The output current of PV cell varies from 2mA to 0mA and its output voltage varies from 1V~0V.

A high efficiency power management system is proposed in this work. The power management system works with PV cell and rechargeable battery. The power management system receives power form PV cell and generates different voltage levels which are suitable for SoC integrated regulator applications. The power management system outputs 1V~0.3V for analog circuitry and low power digital circuitry, -1.2V for memory circuitry, and 5V for I/O components. The overall system provides a charge method from PV cell and extends the life time of the low power SoC system.

Chapter 6 Conclusion and Future Work

In this thesis, we proposed a switched capacitor DC-DC converter and a voltage regulator for solar cell voltage generation in Chapter 3. A new connect scheme of charge pump for generating ultra high voltage is proposed in Chapter 4. In Chapter 5, we proposed a high efficiency power management for solar energy harvesting applications. The research results of Chapter 3 and Chapter 4 are applied to this power management system. The power management system accepts the power from PV cell and generates different voltage levels which are suitable for SoC integrated regulator applications. The power management system outputs 1V~0.3V for analog circuitry and low power digital circuitry, -1.2V for memory circuitry, and 5V for I/O components. The power management system also contains a rechargeable battery. Therefore, the system can storage energy from PV cell and provides to overall system. We proposed maximum power tracking circuitry for solar cell to control the output power and multi-phase maximum power tracking for averaging the output power of PV cell module.

Base on the energy harvesting concept, there are many available power sources exits in the environment such as RFID power source, thermo-generator, magnetic shaker, piezoelectric element as shown in Fig.6.1. We can integrate more different power sources with various power management control circuits. By depending on the environment conditions for power generation, the power management system can scavenge environment energy for the SoC circuitry. Therefore, the SoC circuitry can be self-powered and extends system life-time without to change battery.

As shown in Fig. 6.2, the inductor-less DC-DC converter can integrate to 3D IC without using inductor components.

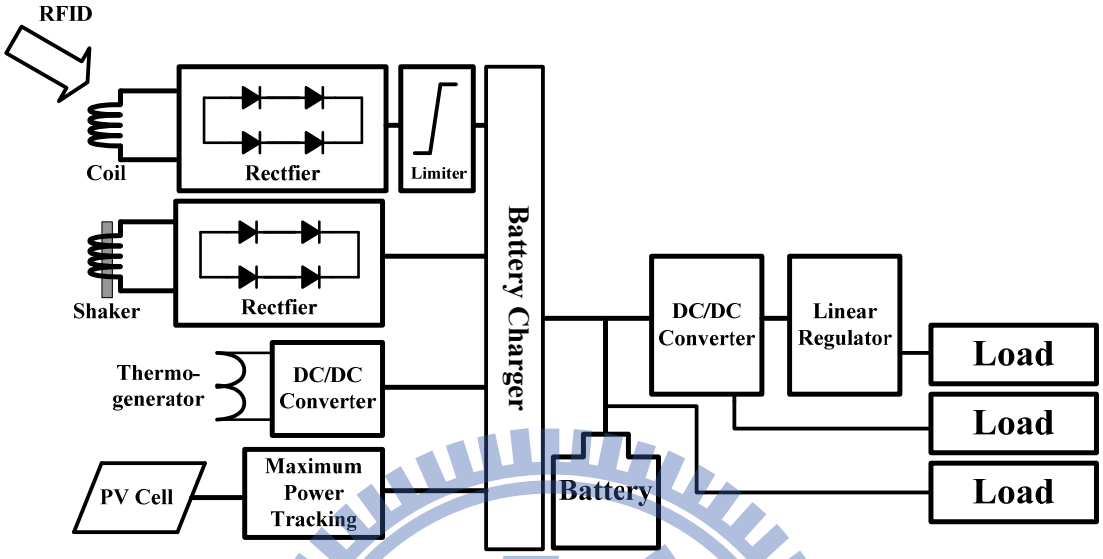


Fig. 6.1 The power management system with different environmental power sources.

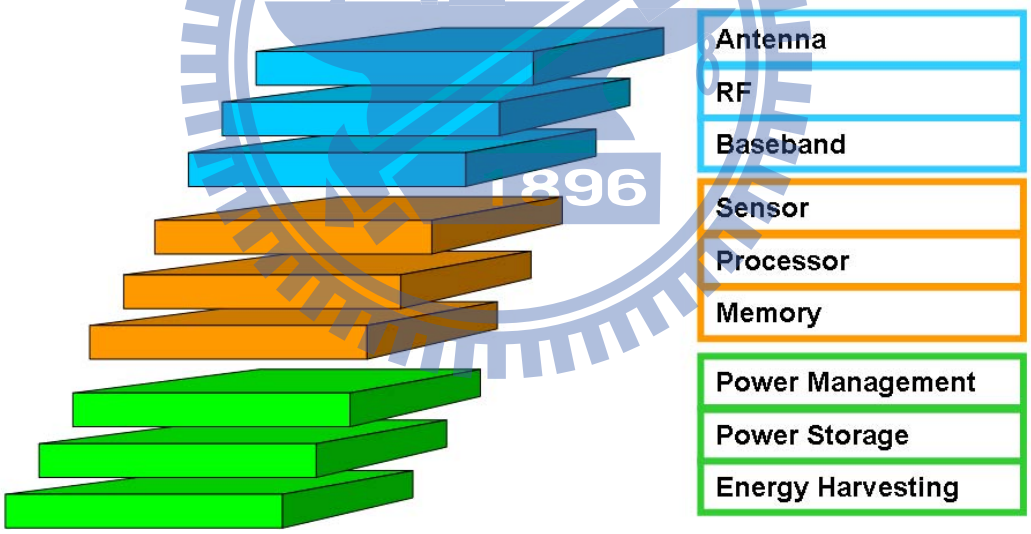


Fig. 6.2 Inductor-less DC-DC converter for 3D IC applications.

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