國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於三維積體電路之
矽穿孔延遲測量器
A TSV Delay Meter for 3D ICs

研 究 生：何承曄

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摘　　要

近年來，隨著半導體製程的不斷進步，電晶體大小已微縮至奈米規模。另一方面，隨著微影製程的困難度愈來愈高，造成新一代製程的製造成本急遽上升。在成本和效能為考量目的之下，工程師們試著將晶片堆疊起來，並建構 SiP 的概念使晶片效能提升、面積縮小。這些堆疊的晶片便是所謂的三維積體電路。其中，負責層與層之間訊號與電源連線的矽穿孔技術扮演著極為重要的角色，利用矽穿孔技術可以大幅縮短線長，提升晶片效能。

受到製程變異影響，訊號通過兩根相同 TSV 時會產生延遲時間差，可能造成同步電路系統準確度受到影響。在此篇論文中，我們設計了一個矽穿孔延遲測量器電路，它可以準確地計算訊號間的延遲時間差，協助後段電路調整此延遲時間差以降低訊號間的延遲誤差。

我們運用台積電 90nm CMOS 製程進行 HSpice 模擬，此電路的最大精確度約 0.74ps，模擬結果顯示延遲誤差小於 0.74ps，證明電路確實能精準算出延遲時間差；此外，此電路的電晶體使用個數約 1200 個，和一個數位電路系統動輒數百萬顆電晶體相比，成本非常小，適合嵌於三維積體電路中作為測試電路。

A TSV Delay Meter for 3D ICs

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Abstract

The manufacturing cost of the advanced process technology rises rapidly; on the other hand, the design complexity of modern designs also increases. To conquer the high cost of a large scale design, the stacked 3D IC is developed. Through-silicon-vias (TSVs) are widely used for vertical interconnection between layers in 3D ICs. Due to process variation, even when a signal passes through two different paths composed of the same series of TSVs, these two paths may incur a delay difference and affect the accuracy of a synchronous system. In this thesis, we present a TSV Delay Meter for calculating delay difference between two paths by HSpice with TSMC 90nm CMOS process. Our results show that the maximum resolution of the meter is about 0.74ps and the simulated delay errors are lower than 0.74ps as well. Hence, the TSV Delay Meter can precisely detect delay difference.

Acknowledgements

I would like to express my gratitude to many people during my Master's career. First, my advisors, Prof. Iris Hui-Ru Jiang and Prof. Chia-Ming Tsai, make me understand the essence of research. Second, I would like to be grateful to the members of my thesis committee, Prof. Kuan-Neng Chen and Prof. Hung-Ming Chen, for their precious suggestions and comments. Third, thanks to the members from IRIS Lab., Lab. 316, and classmates from NCTU and NCHU: Wan-Yu, Huang-Bi, Yen-Ting, Liang-Gi, Cheng-Chi, Yu-Ming, Tsung-Wan, Ya-Chung, Cheng-Han, Hsiang-Yi, Mao-Cheng, Yi-Shing, Jiann-Jiun, Bin-Wei, Zao-An, Yao-Sheng, Chih-Huang, Bao-Yuan, Wen-Peng, Shih-Wen, etc., for their support and encouragement. Fourth, special thanks to Guo-Guang who taught me the insight of business and Chien-Fu who provides me a tutor job. I love business and education so much!

Last but not least, I unfold my honest appreciation to my dear parents, family, and Yi-Ru for their love and support. They are my power of progress!

Cheng-Yeh Ho

National Chiao Tung University

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Chapter 1

Introduction

1.1 Background

In recent years, the process of VLSI is keeping in advance and the transistor size has been scaled down into nanometer technology. Meanwhile, System in Package (SiP) has been applied in the mobile electronic devices to realize small form factor with high performance. On the other hand, power consumption and RC delay induced by long interconnections are great concerns. Moreover, the increasing cost for the newest process also makes industry try to find alternative solutions. Therefore, the engineers start to stack chips vertically in order to shrink the footprint area and boost the performance of a chip. This is the three dimensional integrated circuits (3D IC) that we call.

Compared with the conventional 2D IC, the 3D IC provides a better solution for heterogeneous integration, which enhances performance of the chips. The heterogeneous devices could locate in different substrate materials or different optimized process condition. The characteristics are satisfied with the structure of 3D IC. That is, the 3D IC can stack many layers whose substrate materials or process conditions are different, which enhances the feasibility of heterogeneous integration.

In 3D IC, there are several methods to connect interlayer, which helps signals propagate regularly. In the beginning, a conventional wire-bonding skill is adopted in the interconnection of layers, as shown in Figure 1.1 [1]. However, because of the increase of equivalent series inductance (ESL) and conduction loss, the conventional wire-bonding skill is not good enough at signal integrity and power consumption for

high-speed integrated circuits [2]. Therefore, a through-silicon-via (TSV) technology is developed for the interlayer connection with short length, as shown in Figure 1.2 [3]. Instead of wire-bonding around the stacked chip, the TSV technology constructs vertical paths to connect signals and power supply so the stacked layers have the shortest interconnection, which stands for that the effects of inductance and conduction loss will be eliminated. In addition, the elimination of TSV's diameter is an issue for minimizing the chip area, as shown in Figure 1.3 [4] [5]. Therefore, the TSV technology is the most important interconnection method for high performance in 3D IC.

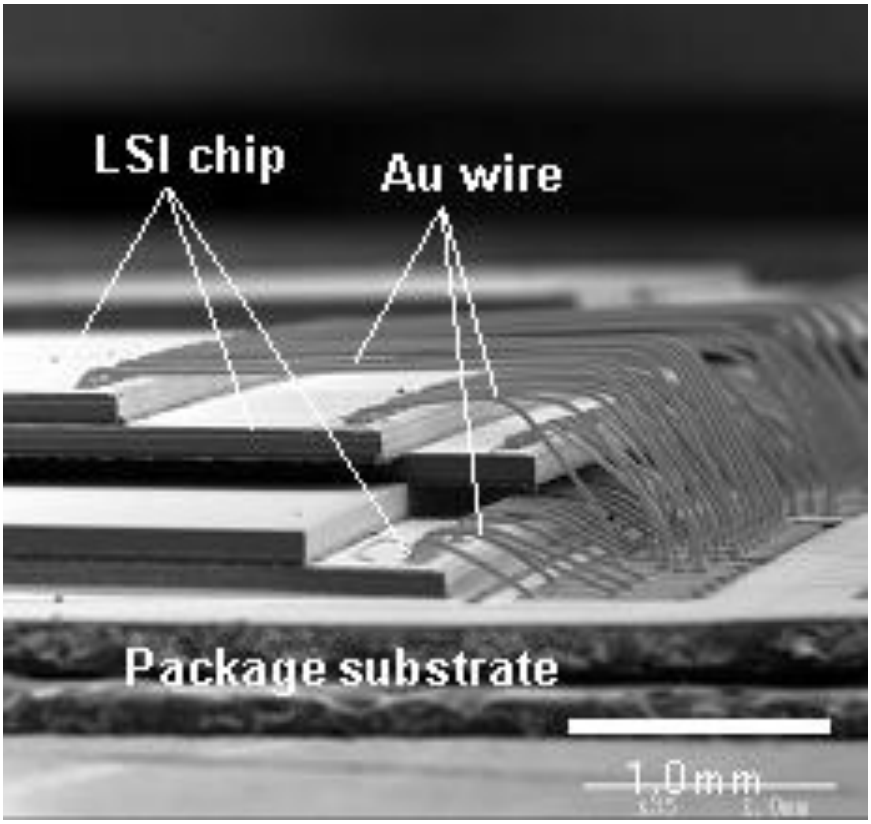


Figure 1.1: A structure of 3D-stacked SiP using wire bonding [1]

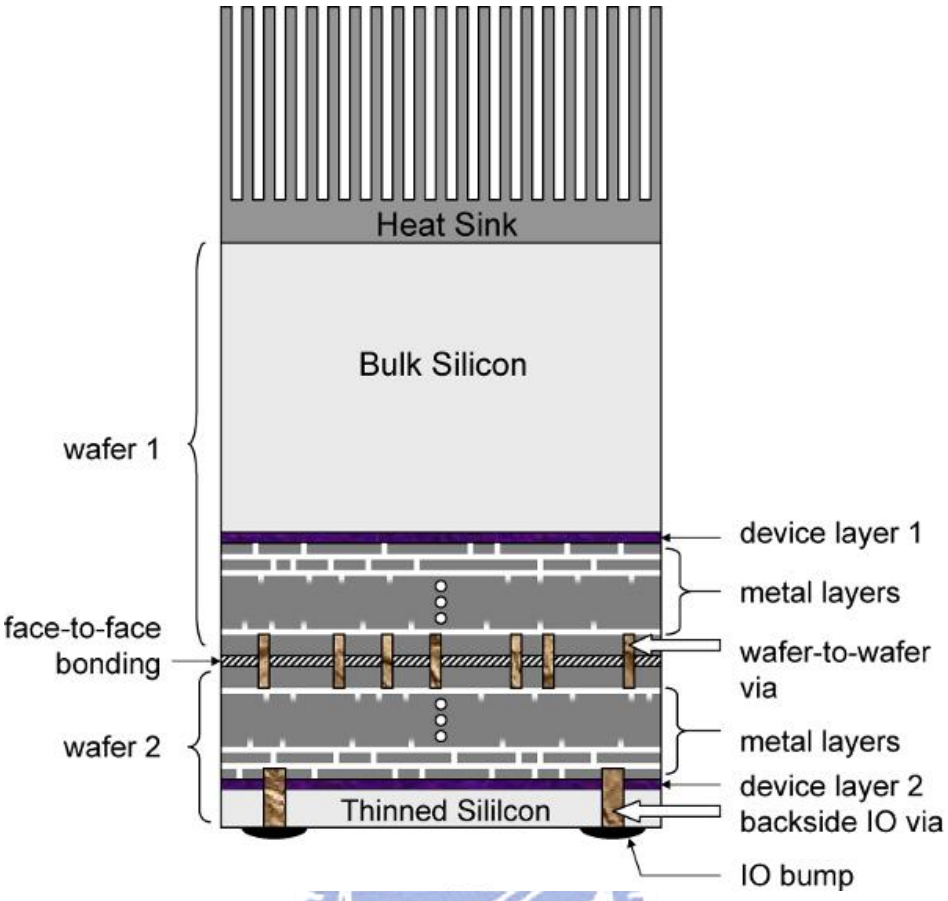


Figure 1.2: A two-layer 3D-IC using TSV interconnection technology [3]

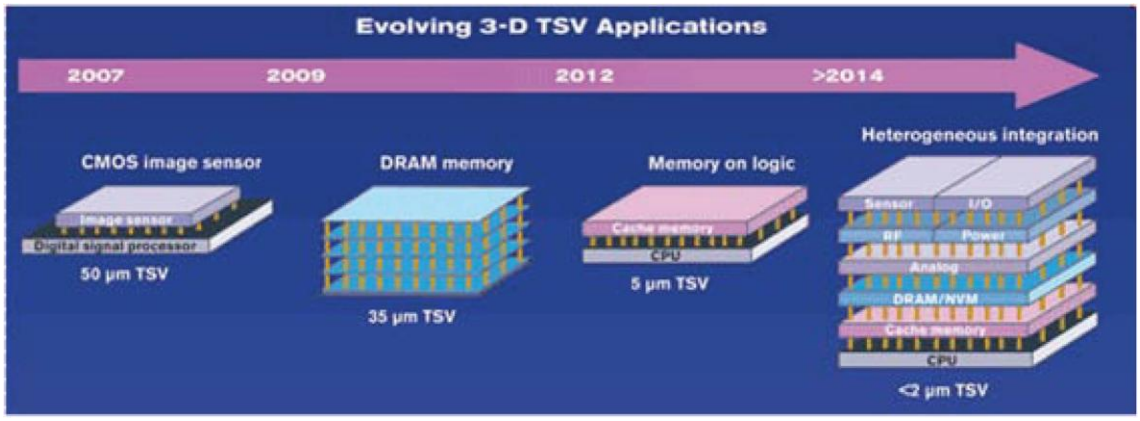
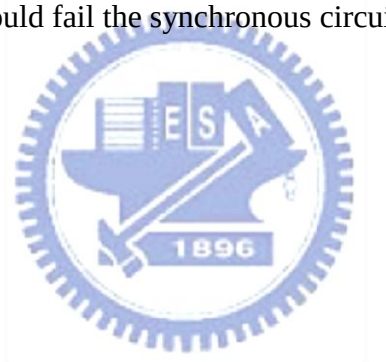


Figure 1.3: Evolving 3D TSV Applications [4] [5]

The three steps of 3D IC manufacturing using TSV are as follows: First, through holes are made by deep Si etching and the holes will be filled with a conductive material like copper, polysilicon, and so on. Second, use grinding skills to perform wafer-thinning. Third, stack the chips by bonding skills. Figure 1.4 shows the flow of TSVs etching [6] and Figure 1.5 presents the wafer level packaging (WLP) process flow of MEMS devices using TSV and Al to Al bonding [7].

Consequently, TSV plays an important role in 3D IC. On the other hand, in a synchronous circuit system, the consistency of the signals is very important. When there are more and more TSVs added in 3D IC, the process variation of the TSVs will affect the consistency of signals seriously, which stands for that the increase in delay difference between signals would fail the synchronous circuit system.



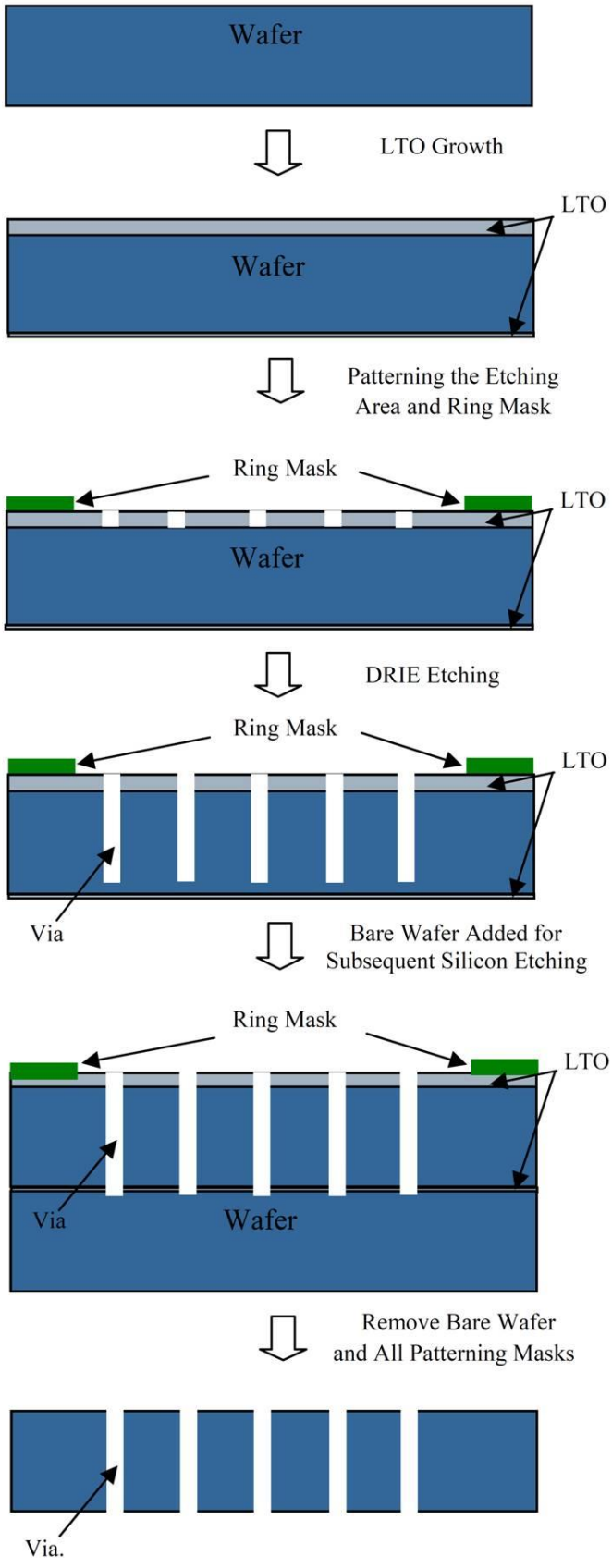


Figure 1.4: TSVs etching by DRIE (wafer level process) [6]

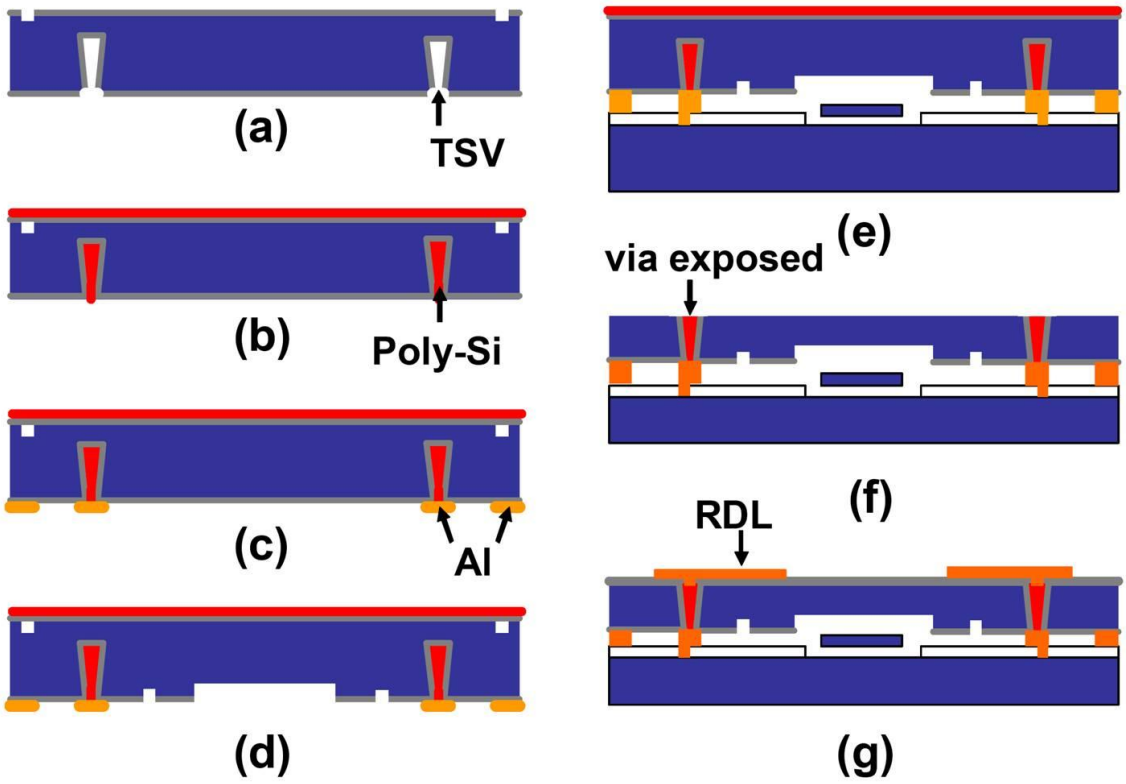


Figure 1.5: Process flow of Wafer level packaging (WLP) (a) TSVs were etched using DRIE (deep reactive ion etched) for 200um deep. (b) Deposit Poly-Si to fill the TSVs for electrical signal path. (c) 0.1um thick TiW and 2um thick Al stacked on the TSVs and the perimeters of an individual die. (d) Etching ~75um deep cavities. (e) Al to Al bonding. (f) Back-grinding and polishing the cap wafer from 380um down to 180um to expose TSVs. (g) RDL (re-distribution layer) metal was patterned to complete the 3D interconnects [7].

1.2 Our Contribution

To ensure that a synchronous circuit implemented by 3D stacking technology could operate correctly, we have to precisely measure the delay difference induced by process variations. Once the delay difference time is acquired, we could apply an extra circuit to adjust signals and compensate the delay error. In this thesis, we develop a TSV Delay Meter to measure the delay difference time resulting from the process variation of the TSVs. The TSV Delay Meter is able to detect time difference between two signal paths by a series of digital codes. The resolution of TSV Delay Meter is $\tau/64$, which is about 0.74ps under TSMC 90nm CMOS technology. The simulation results show that delay error is under $\tau/64$, which implies the TSV Delay Meter works well.

In addition, TSV Delay Meter not only calculates time difference induced by process variation but also detects time difference between two paths composed of different types of TSV for heterogeneous integration. On the other hand, the TSV Delay Meter is able to calculate time difference from one path for evaluating the propagation delay time of a single TSV as well.

1.3 Organization

The remainder of this thesis is as follows: Chapter 2 introduces a TSV model and problem formulation, Chapter 3 presents the circuit structure of TSV Delay Meter, Chapter 4 shows the simulation results, and Chapter 5 makes conclusions for this thesis.

Chapter 2

TSV Model and Problem Formulation

2.1 TSV Technology

A through-silicon-via (TSV), which passes through the substrate of a die, is responsible for interlayer connections of signals and power supply in a stacked 3D IC, as shown in Figure 2.1 [8]. By the manufacturing order before or after devices or back-end-of-line (BEOL), the two primary types of TSV, via-first and via-last, are classified. Figure 2.2 shows the differences between via-first and via-last TSVs [3].

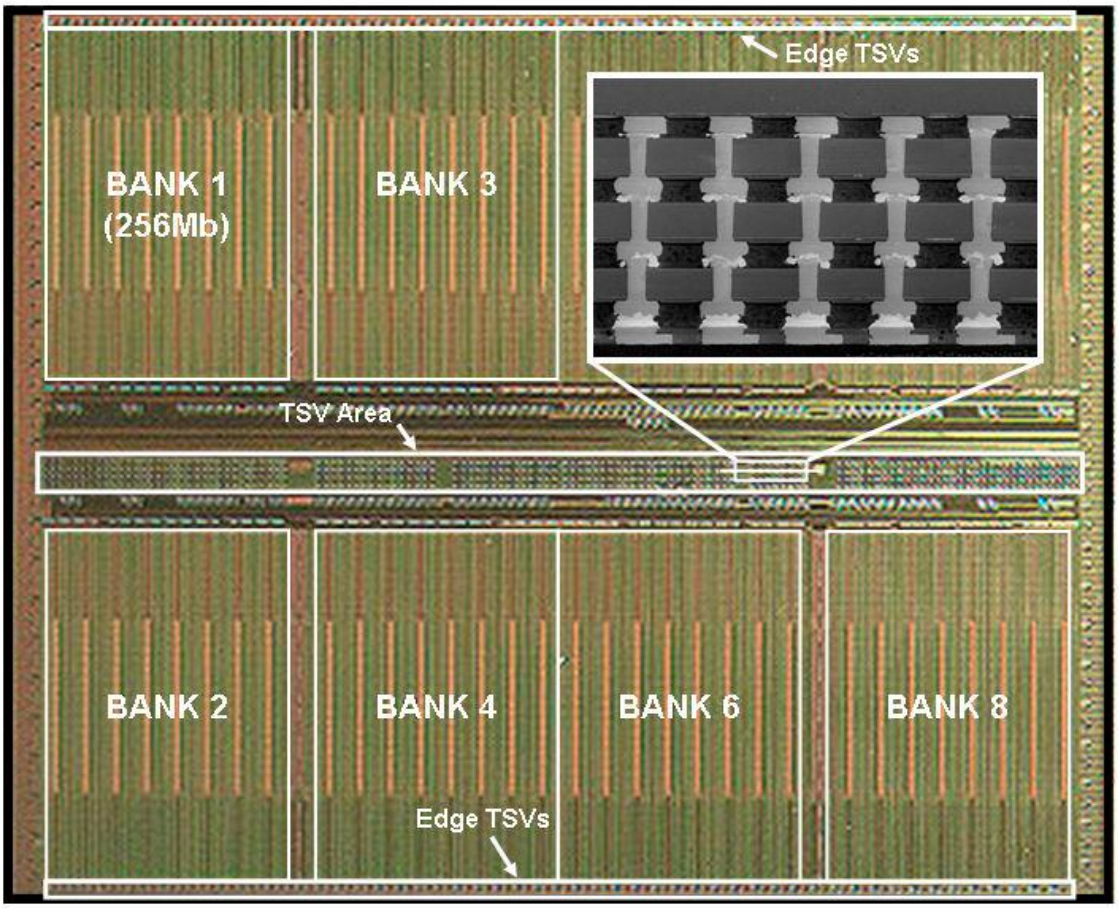


Figure 2.1: A photograph of 3D DDR3 DRAM using TSV technology [8]

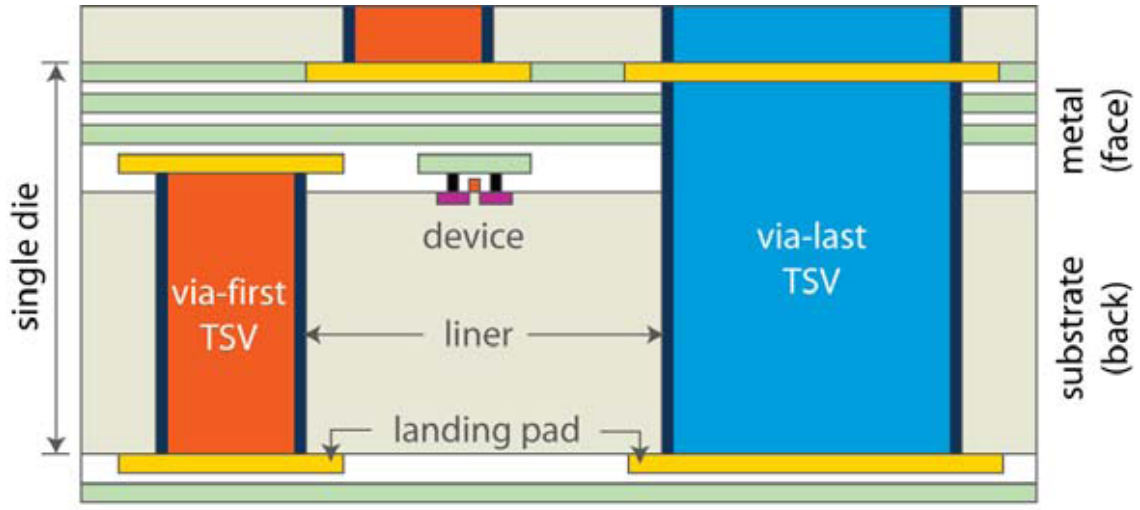


Figure 2.2: Via-first and via-last TSVs [3]

The via-first TSVs are implemented before CMOS and BEOL. To prevent the CMOS process line is affected and contaminated, the filling materials of TSVs should be CMOS compatible. For example, polysilicon, which has electric conductivity, is used for via filling. The implantation of via-first TSVs is at the foundry level so it has better design flexibility than via-last TSVs. In addition, the diameter of via-first TSVs is about 1 to 10um and the aspect ratio (height/diameter) is about 3 to 10 [3].

On the other hand, the via-last TSVs are fabricated after CMOS and BEOL. Hence, metal can be selected as the filling material of TSV such as copper. The copper has great electric and thermal conductivity so the via-last TSVs have no thermal stress issues compared with the via-first TSVs. Moreover, the via-last TSVs are utilized by the package companies which stack the fabricated wafers or dies. During the manufacture of via-last TSVs, the devices could be damaged, which lowers the yield of 3D IC compared with via-first TSVs. Besides, because the procedure of via-last TSVs is behind BEOL, the depth of TSVs is deeper than via-first TSVs, which makes the diameter of via-last TSVs be about 10 to 50um and has the high aspect ratio be about 3 to 15 [3].

2.2 TSV Model

Figure 2.3 shows the characteristics of the TSV, which is composed of lumped devices such as R, L, C, and G [9] [10]. The resistor R and the inductor L are viewed as characteristics of TSV. In addition, for representing lossy and parasitic characteristics induced from an oxide layer and a silicon substrate, the C_{ox}, G_{Si}, and C_{Si} parameters are added into the TSV circuit model where C_{ox} is the parasitic capacitance from an oxide layer, G_{Si} and C_{Si} are from a silicon substrate. The equivalent model of a four-port network using four TSVs also presents that the TSV can be modeled by RLCG devices, as shown in Figure 2.4. Therefore, we regard a TSV model as a combination of lumped devices, as shown in Figure 2.5.

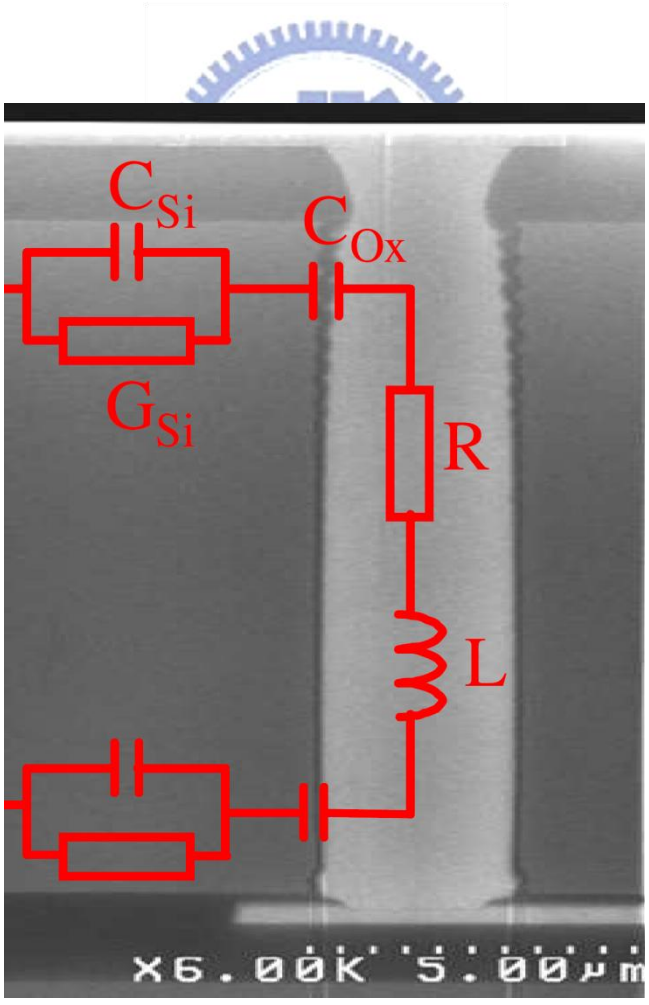
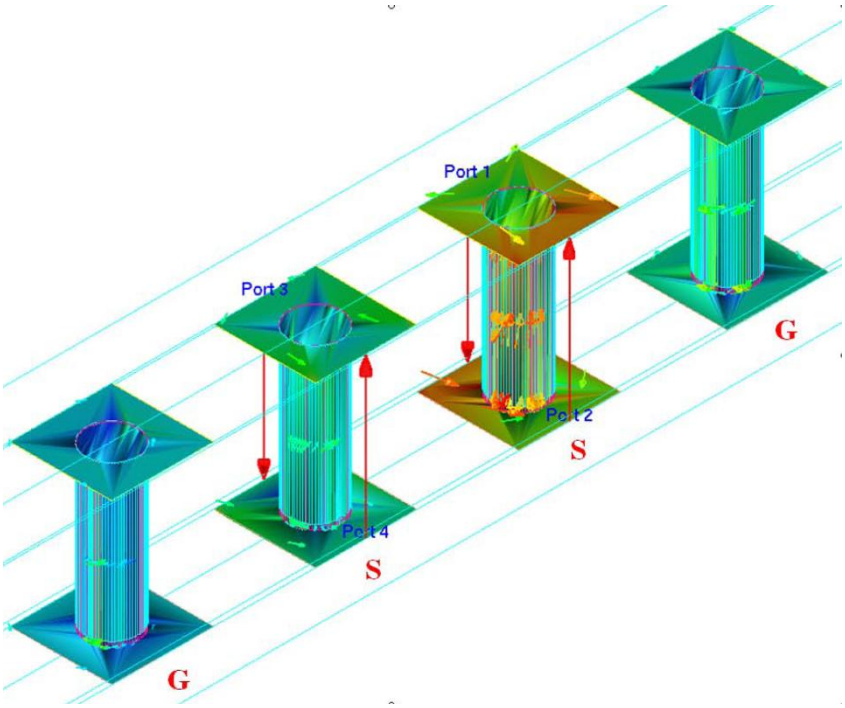
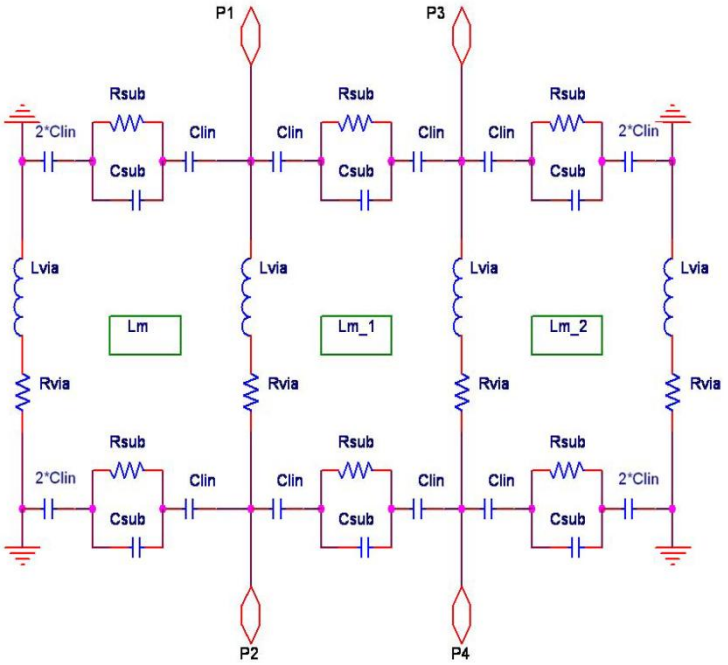


Figure 2.3: Physical equivalent model of TSV [9]



(a)



(b)

Figure 2.4: (a) A 4-port G-S-S-G (G: ground; S: signal) network using 4 TSVs (b) Equivalent model of the network [4]

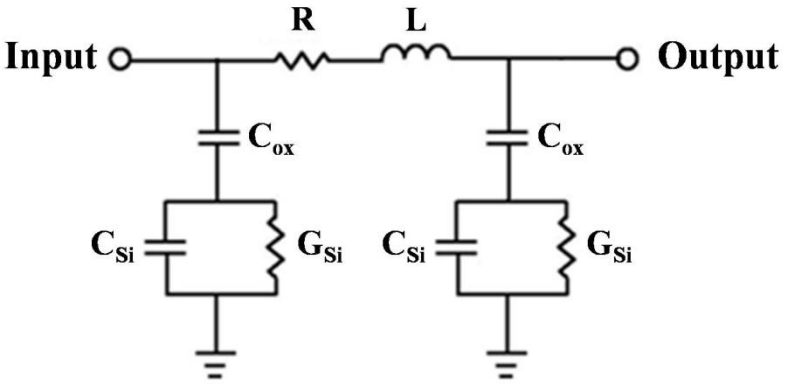


Figure 2.5: A TSV equivalent circuit model

The behavior of TSV is like a transmission line. When a clock signal enters into the TSV equivalent circuit model, compared with the input waveform, the output waveform has overshooting and undershooting effects, as shown in Figure 2.6. The effects induced by the L in RLC circuits could have an uncertainty for a circuit system if the positive or negative undershoot crosses the $V_{dd}/2$. It is an important issue for how to eliminate these effects. On the other hand, the resistors R and the capacitors C affect propagation delay. If the same two signals respectively pass through two different TSV models whose values of RLCG are different, the propagation delay time are totally different. Therefore, the two signal paths will have delay difference.

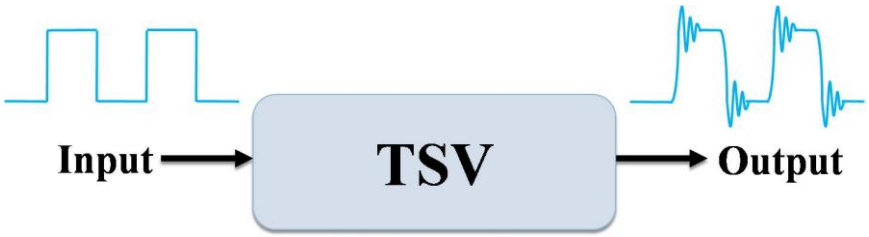


Figure 2.6: A block diagram of a clock signal passes through a TSV

2.3 Problem Formulation

The problem formulation in this thesis is how to precisely find the time of delay difference between the same two signal paths constructed by TSVs. Because of process variation, the propagation delay time of the same two signal paths composed of the identical TSVs will be different. That is, delay difference time between two paths will be induced. This difference could affect a synchronous circuit system to access a wrong data. Therefore, calculating the delay difference time precisely is a subject in this thesis.

Chapter 3

TSV Delay Meter

3.1 Full Structure of TSV Delay Meter

To precisely detect delay difference time between two paths, a TSV Delay Meter is designed. It is composed by the following two blocks: Coarse Delay Detector and Fine Delay Detector, as shown in Figure 3.1. In Figure 3.1, a clock signal passes through two paths and then enters into the meter. Each path has a delay block composed of TSVs, which incurs delay difference between two paths. By the digital codes from the outputs of TSV Delay Meter, we could find the delay difference time exactly. The following sections in this chapter describe the full structure of TSV Delay Meter and its operating theorem.

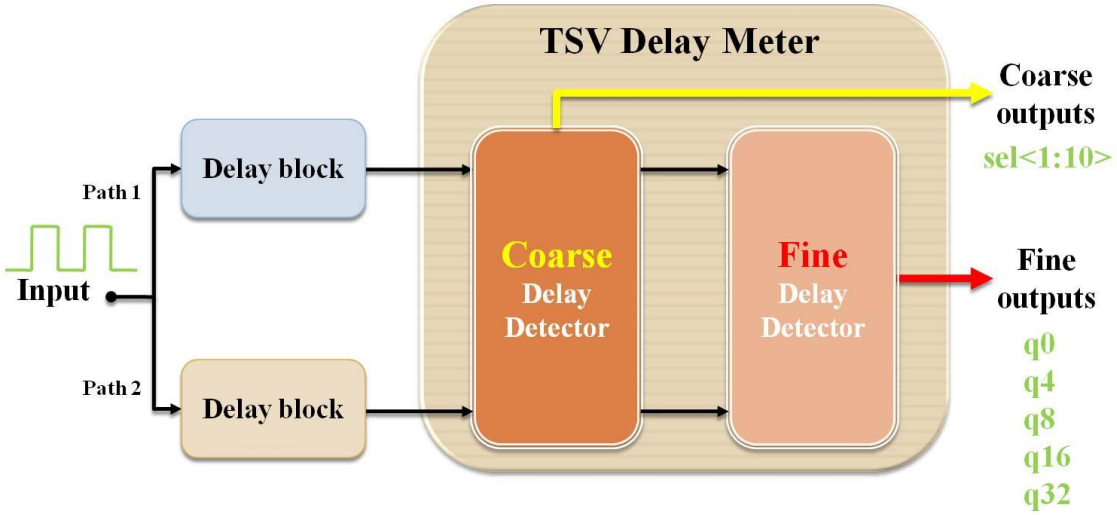


Figure 3.1: Full structure of TSV Delay Meter

3.2 Coarse Delay Detector

Figure 3.2 is a block diagram of the Coarse Delay Detector [11]. It has three parts: a delay line, a digitizer, and a switching detector. The TSV2_clk signal passes through each delay cell (buffer) of the delay line whose propagation delay time is defined as τ and then generates multiphase clocks. The multiphase clocks have two paths: the first path enters the digitizer to compare with the TSV1_clk signal, and the second path, cds<1:10>, is prepared to enter the Fine Delay Detector.

In order to find one of the multiphase clocks synchronized with the TSV1_clk signal, the negative edge-triggered D flip-flops (D-F/F) and the switching detector sense each position of the multiphase clocks. When there is a low-to-high transition from D-F/F output signals, the switching detector activates one of the selection signals (sel<1:10>), i.e., logic 1 is generated. Once the activated selection signal is decided, one of the cds<1:10> signals will be selected and then enter the Fine Delay Detector because this signal is synchronized with TSV1_clk. For example, as shown in Figure 3.3, TSV2_clk produces multiphase clocks like cds<1>, cds<2>, and so on. When TSV1_clk compares with these multiphase clocks, we find that there is a low-to-high transition from cds<2> to cds<3> and then the selection signal sel<2> is activated. Finally, the sel<2> signal selects cds<2> synchronized with TSV1_clk into the Fine Delay Detector. The operating process of this example is presented by Figure 3.4.

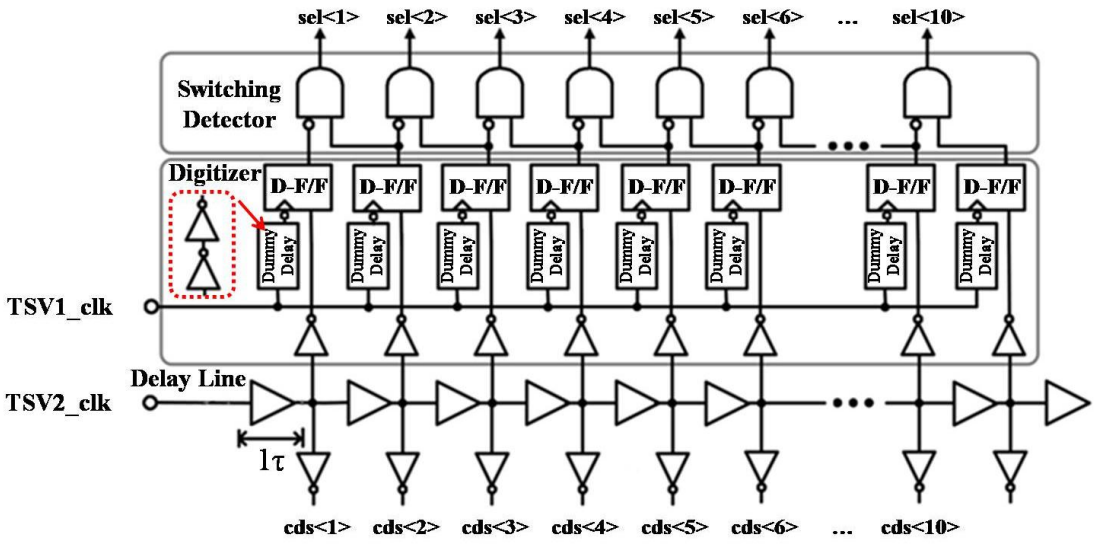


Figure 3.2: A block diagram of Coarse Delay Detector [11]

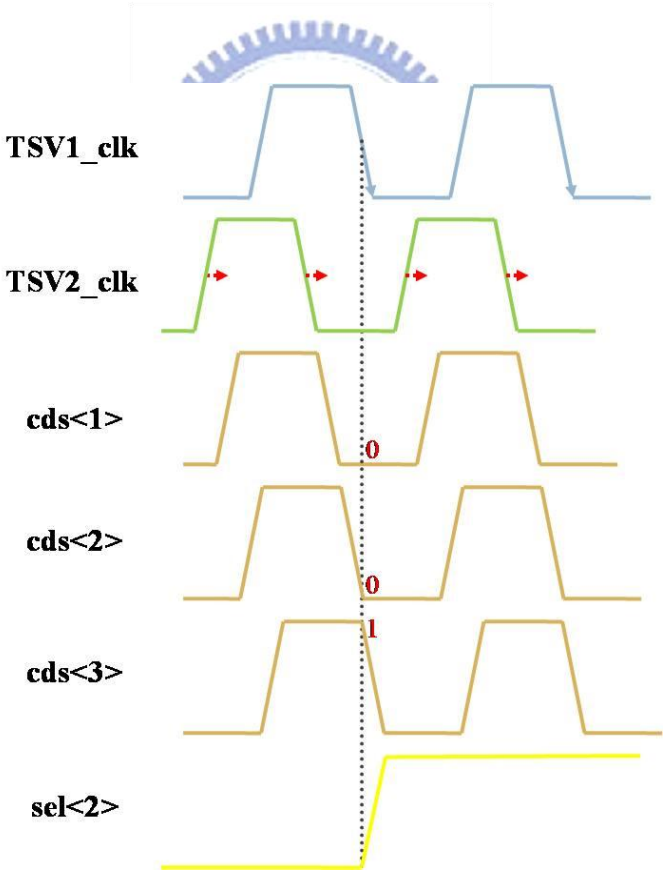


Figure 3.3: An operation of Coarse Delay Detector

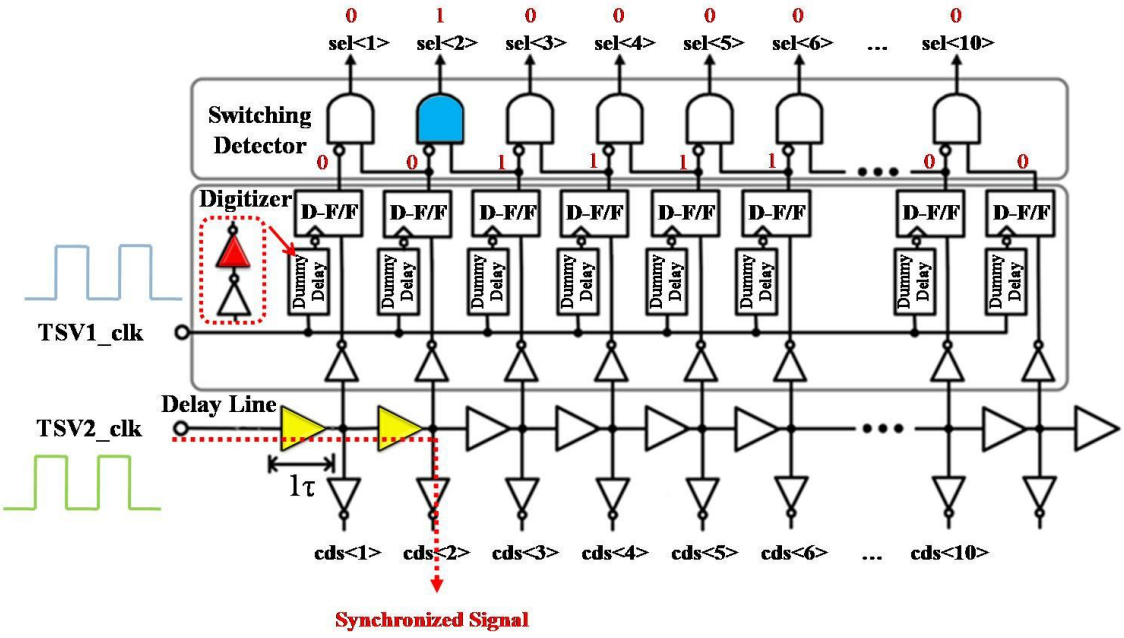


Figure 3.4: An example of the sel<2> signal selects cds<2> synchronized with TSV1_clk into the Fine Delay Detector.

In each path of the multiphase clocks, there is an inverter added between a D-F/F and a delay cell, which ensures the loading capacitance of each delay cell do not vary when each D-F/F switches on and off [12]. This behavior makes each delay cell of the delay line have identical propagation delay time.

There is a dummy delay added in the TSV1_clk signal path. It is composed of two inverters: the first inverter matches the delay time of the inverter from the multiphase clocks and the second inverter makes D-F/F have a setup time of τ/2 for suppressing delay error within τ/2 between the two synchronized signal path, cds<n> and TSV1_clk. Without the second inverter, the delay error is within τ instead of τ/2. For example, the process of delay error elimination is presented as shown in Figure 3.5. Assume that the delay difference of TSV1_clk and TSV2_clk is 2τ and TSV2_clk leads TSV1_clk, TSV2_clk passes through each delay cell whose propagation delay time is τ and the multiphase clocks are produced. In this case, cds<2> exactly synchronized with

TSV1_clk should enter the Fine Delay Detector. At the same time, there should be a low-to-high transition from cds<2> to cds<3> and sel<2> is activated. However, it could be the cds<1> to enter the Fine Delay Detector instead of cds<2>. As shown in Figure 3.5(a), because the cds<2> is synchronized with TSV1_clk exactly, the D-F/F may detect logic 1 or logic 0 uncertainly when cds<2> compares with TSV1_clk. Once logic 1 is detected from cds<2>, it stands for sel<1> is activated and selects cds<1> to enter the Fine Delay Detector with TSV1_clk. Thus, that makes the delay error of τ between two signals entering the Fine Delay Detector. On the other hand, as shown in Figure 3.5(b), with the second inverter, TSV1_clk has an extra propagation delay time of $\tau/2$ that results in the D-F/F detects logic 0 definitely from cds<2>. Finally, sel<2> is activated and selects cds<2> to compare with TSV1_clk correctly. These two signals before entering the Fine Delay Detector have a delay error of $\tau/2$ instead of τ. Therefore, the delay error elimination that makes delay error within $\tau/2$ is achieved by the second inverter of the dummy delay.

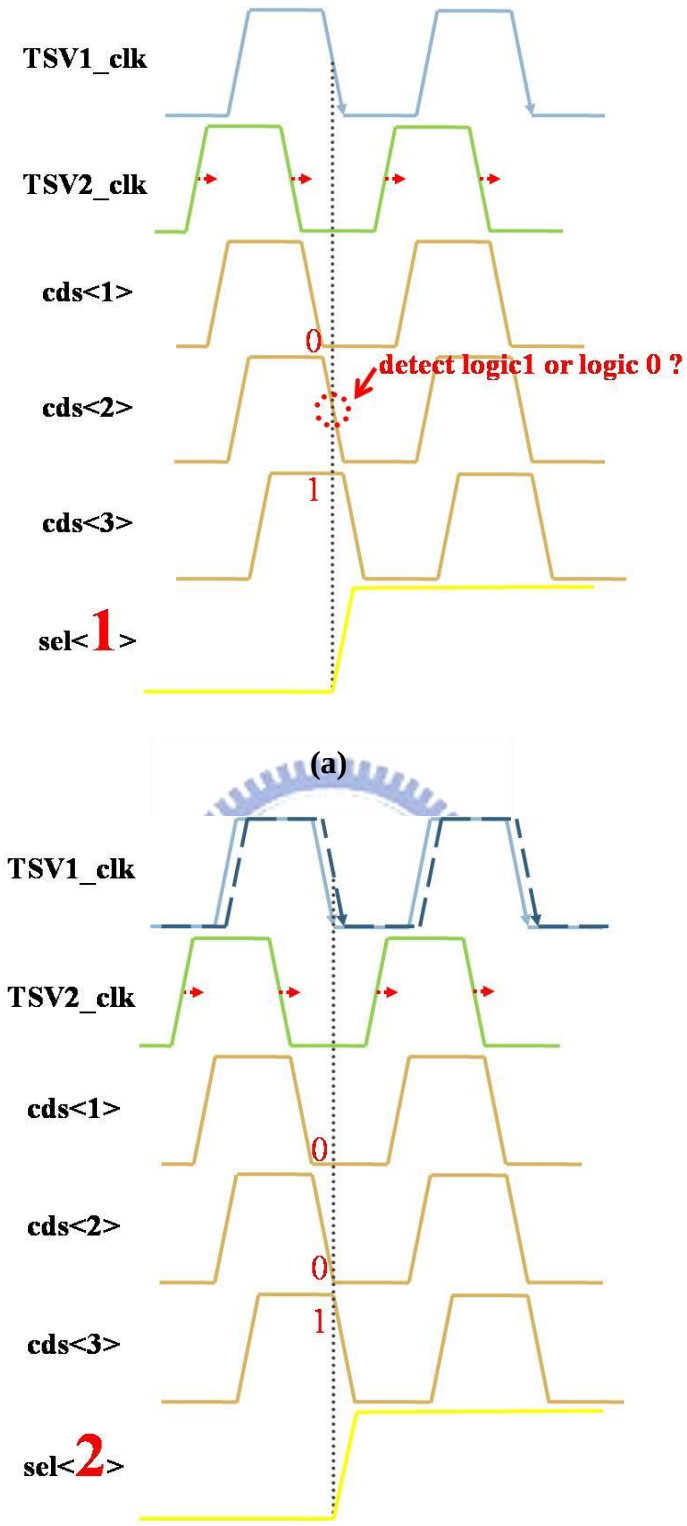


Figure 3.5: Timing diagrams (a) without the second inverter and (b) with the second inverter. Assume the delay difference of TSV1_clk and TSV2_clk is 2τ and TSV2_clk leads TSV1_clk.

3.3 Fine Delay Detector

Figure 3.6 is a block diagram of Fine Delay Detector [11]. The Fine Delay Detector has four stages which is composed of two input buffers, five phase detectors (PD), and four tuned delay lines (TDL). By the five outputs of Fine Delay Detector from the detection of PDs, i.e., q0, q4, q8, q16, and q32, we can know that which input signal is leading or lagging at each stage and then change the propagation delay time of the two signal paths by TDLs in order to match the two signals. In addition, the resolution of Fine Delay Detector attains τ/64, which is better than the τ/2 of the resolution of Coarse Delay Detector.

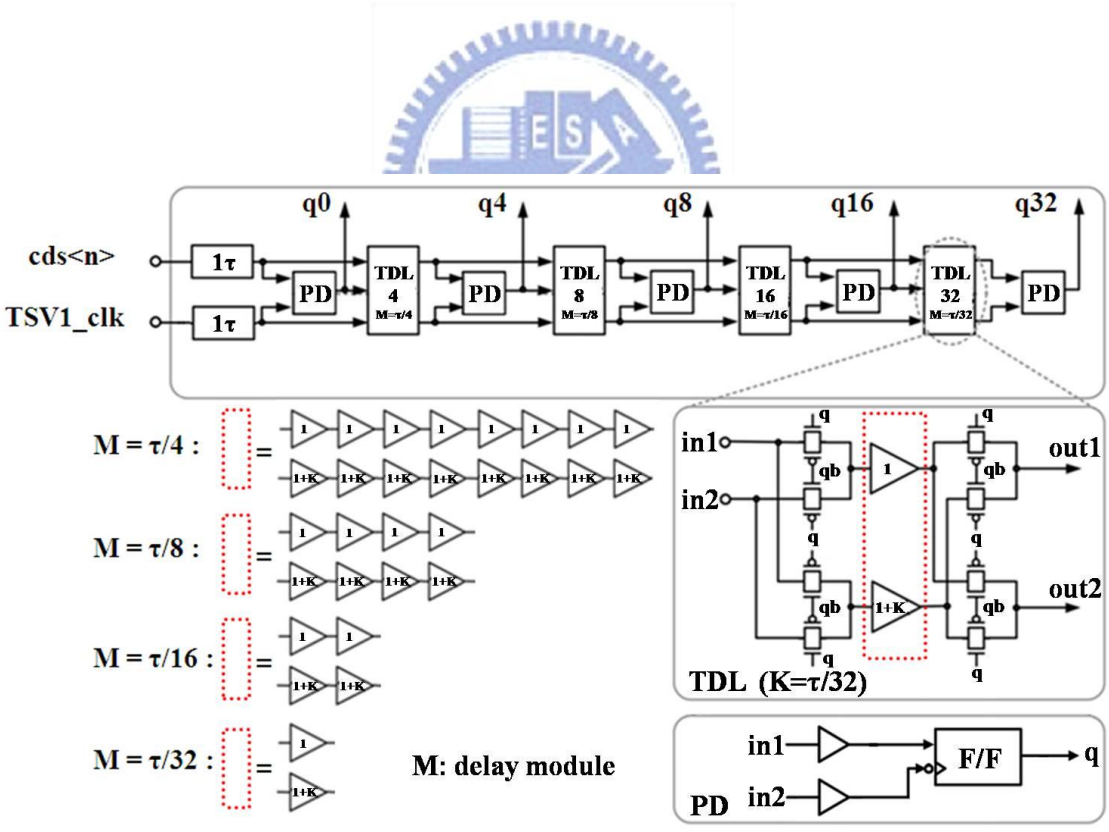


Figure 3.6: A block diagram of Fine Delay Detector [11]

The phase detectors and tuned delay lines play an important role in Fine Delay Detector. The PD uses a negative edge-triggered pass-gate D-F/F in order to enhance the operation of flip-flops and the TDL has one delay module M and eight transmission gates. For enhancing the resolution, each of TDL has different delay module. First, TDL32, its delay module consists of two buffers. The delay difference time of the two buffers is K, where K is $\tau/32$ by tuning the size of transistors. Second, TDL16, its delay module has two series of delay module of TDL32 and makes its delay difference time to be $\tau/16$. By the same method, we know that TDL8 and TDL4 have four series and eight series of delay module of TDL32, respectively.

The reason for adding series of delay module of TDL32 into each TDL is to make consistency. That is, it ensures that the delay difference time of the previous TDL is two times of the next TDL exactly. However, if each delay module of the TDLs only has two buffers and we adjust the size of the transistors respectively to fit every delay difference time K ($K=\tau/4, \tau/8, \tau/16, \tau/32$), the delay difference time of the previous TDL could not be two times of the next TDL exactly because the tuned delay modules do not have a basic unit to make consistency. In other words, the respective tuning method could not guarantee that the delay difference time of each TDL is a multiple of the delay difference time of TDL32 exactly. Therefore, the series structure of the delay module is used in the Fine Delay Detector. By the digital codes from the outputs of Fine Delay Detector, the max resolution of Fine Delay Detector will be $\tau/64$.

Table 3.1 shows the situation of digital output of the PD. When q=0, it stands for that TSV1_clk lags cds<n>. As a result, the cds<n> enters the path of 1+K for more delay time and TSV1_clk enters the path of 1. On the contrary, cds<n> lags TSV1_clk when q=1, so TSV1_clk enters the path of 1+K and cds<n> enters the path of 1.

Table 3.1: The selection of signal paths

	Status	Which signal select the path of 1+K in the TDL?
q = 0	**TSV1_clk lags cds<n>**	**cds<n>**
q = 1	**TSV1_clk leads cds<n>**	**TSV1_clk**

Figure 3.7 shows an example of the operation of the Fine Delay Detector. Suppose that TSV1_clk lags cds<n> 11.37ps, 1τ is equal to 47ps, and the five digital outputs (q0 to q32) of Fine Delay Detector are 01000. First, the signal of q0 which equals 0 means the phase detector detects that TSV1_clk lags cds<n>, so the TSV1_clk enters the normal delay path which has the buffer size of 1 shown in Figure 3.6 and cds<n> enters the long delay path which has the buffer size of 1+K presented in Figure 3.6 with the extra τ/4 delay in TDL4. Second, the signal of q4 which outputs 1 means the phase detector detects that TSV1_clk leads cds<n> after the two signals pass through TDL4, so the TSV1_clk enters the long delay path with the extra τ/8 delay in TDL8 and cds<n> enters the normal delay path at this time. Similarly, the following outputs of q8 and q16 which are equal to 0 make cds<n> enter the long delay path two times from TDL16 to TDL32. The output of q32 is equal to 0, which stands for that we could have an estimation to add the extra τ/64 delay into the cds<n>. Therefore, the total delay difference, D, between TSV1_clk and cds<n> is an equation as follows:

$$\tau/4 + \tau/16 + \tau/32 + \tau/64 = D + \tau/8 + \text{unknown delay error.}$$

Finally, D is equal to 15τ/64, about 11.02ps. Compared with 11.37ps, the value calculated by Fine Delay Detector has a mismatch of 0.35ps, which is lower than τ/64. That is, the mismatch is under the maximum resolution of the Fine Delay Detector.

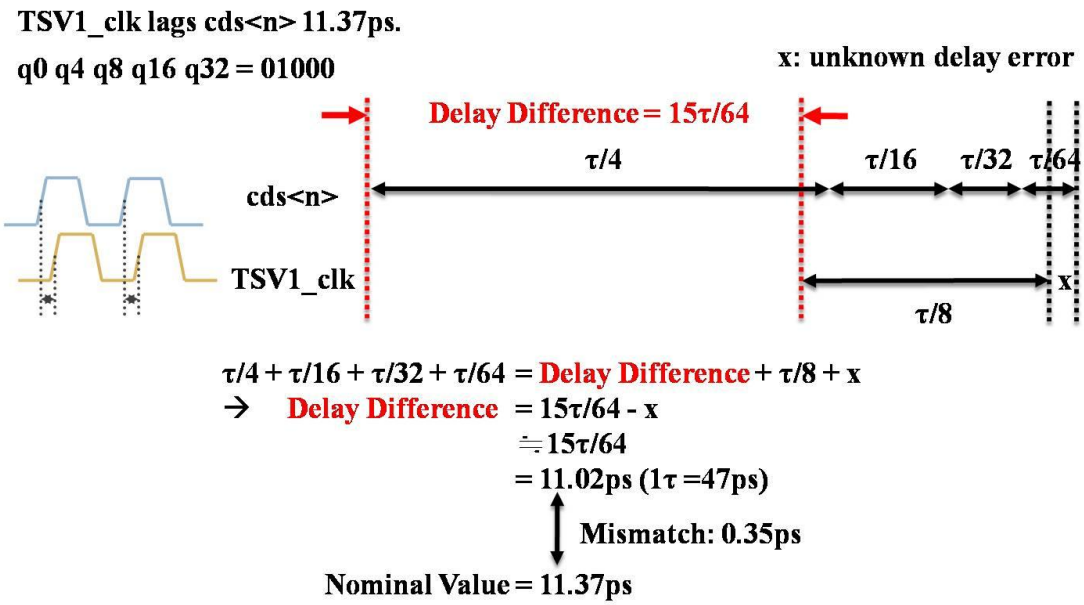


Figure 3.7: An example of TSV1_clk lags cds<n> 11.37ps

3.4 Calculation of Delay Difference Time

After introducing the operation of Coarse Delay Detector and Fine Delay Detector, we present that how the TSV Delay Meter calculates the total delay difference time of TSV1_clk and TSV2_clk in this section. The block diagrams presenting calculation of total delay difference time are shown in Table 3.2. There are two cases: TSV1_clk leads or lags TSV2_clk. If TSV1_clk leads TSV2_clk, the total delay difference time can be expressed as:

$$\tau/2 + (\pi - C - F).$$

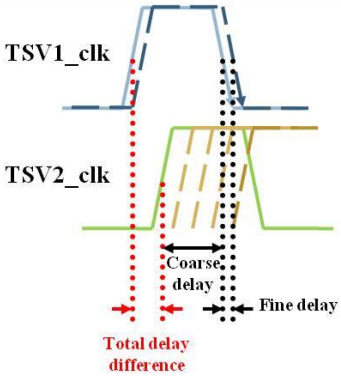
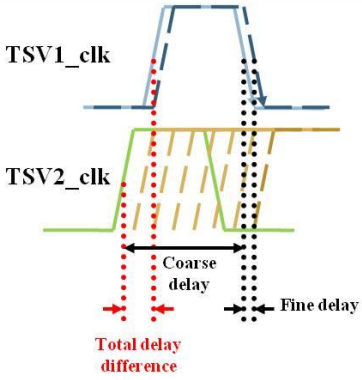
In the foregoing expression, τ/2 stands for the second inverter delay time of the dummy delay cell in Coarse Delay Detector, C is the part of coarse delay time in Coarse Delay Detector, and F is the part of fine delay time in Fine Delay Detector. The part of π－C－F is the answer calculated by TSV Delay Meter. However, τ/2 is also added in this equation. Because the second inverter of dummy delay cell in Coarse Delay Detector is added in the path of TSV1_clk, which decreases the extra delay time of τ/2 when comparing with TSV1_clk and TSV2_clk. Therefore, we need to add τ/2 into the

equation for reflecting the extra delay time and truly expressing the real answer. On the contrary, if TSV1_clk lags TSV2_clk, the total delay difference time is expressed as:

$$(C+F-\pi)-\tau/2.$$

Similarly, the part of $C+F-\pi$ calculated by TSV Delay Meter subtracts $\tau/2$ increasing the extra delay time is the actual answer of delay difference time between TSV1_clk and TSV2_clk.

Table 3.2: Calculation of delay difference time

	TSV1_clk leads TSV2_clk	TSV1_clk lags TSV2_clk
Total delay difference	$\tau/2 + [\pi - C - F]$	$[C + F - \pi] - \tau/2$
Diagrams		

3.5 Simplified Structure of TSV Delay Meter

A simplified structure of TSV Delay Meter is composed of Fine Delay Detector only, as shown in Figure 3.8. When the delay difference time between two paths is lower than τ/2, we do not need to use the Coarse Delay Detector because its resolution of τ exceeds the delay difference time. According to the simulation results, as shown in Chapter 4, every delay difference time between two paths is under τ/2. Thus, we could remove the Coarse Delay Detector and then adopt the simplified structure to be the main structure in this thesis.

However, although the Coarse Delay Detector does not be used in the current 3D IC technology, it still has an opportunity to be applied if a system has more and more transistors and the technology of heterogeneous integration grows rapidly in the future.

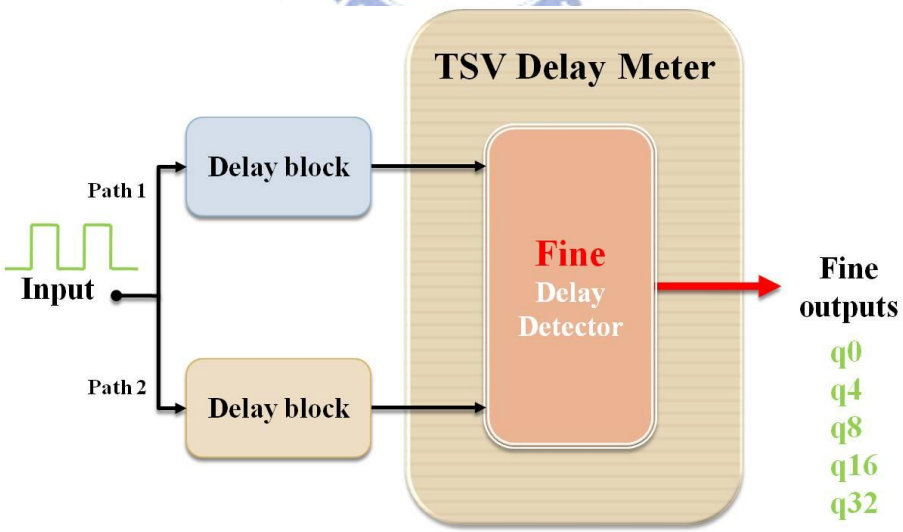


Figure 3.8: Simplified structure of TSV Delay Meter

Chapter 4

Simulation Results

We use TSMC 90nm CMOS process parameters to simulate the performance of TSV Delay Meter by HSpice. The operating voltage is 1.2V, the input clock frequency is 2GHz, and the propagation delay time of a delay cell (a buffer) simulated from the eye diagram is 47ps, i.e., $\tau = 47ps$.

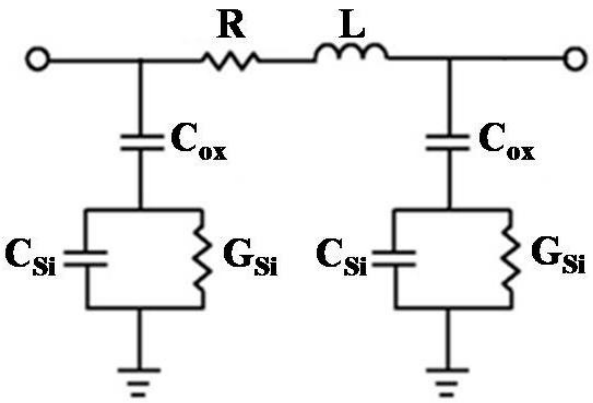
4.1 Resolution Issue

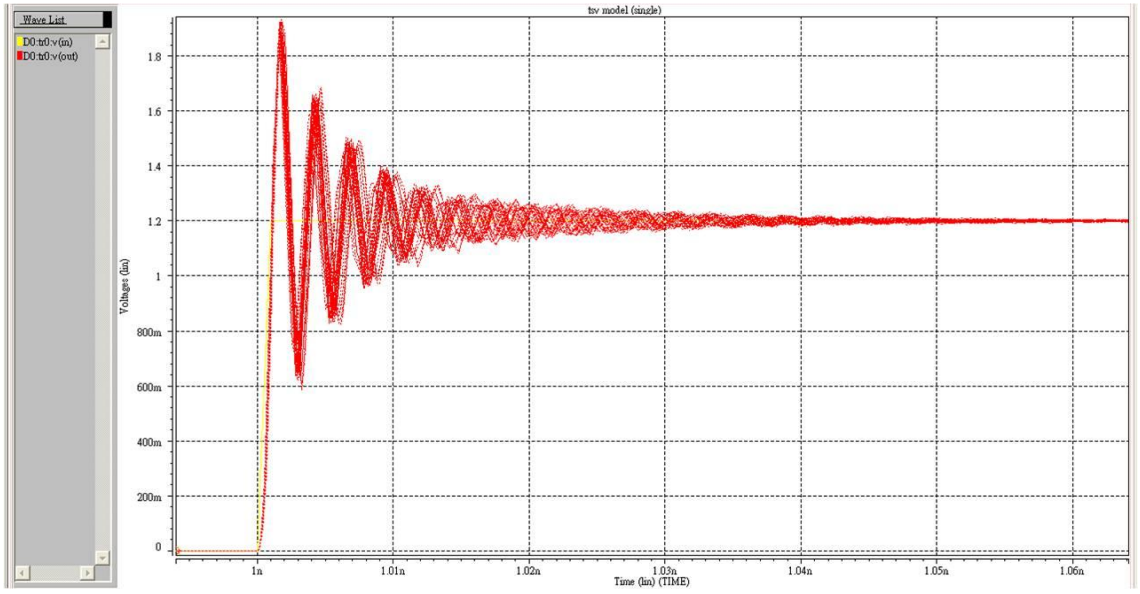
Figure 4.1(a) shows the output waveforms when the input clock enters a TSV equivalent circuit model whose parameter values are listed in Table 4.1. For reflecting the delay difference time induced from process variation, we use the Monte Carlo analysis to adjust the value of each RLCG device. In the Monte Carlo analysis, Gaussian distribution is adopted and the ±30% variation amount of each lumped device is set for presenting large process variation induced from advanced nano CMOS technology. In Figure 4.1(b), we find that the maximum delay difference time is under 0.13ps and it is lower than the resolution of Fine Delay Detector unfortunately. In other words, the TSV delay meter could not find out the delay difference time precisely between two TSVs. A resolution issue is induced.

By Figure 4.1, we observe two things: first, the delay difference time is much lower than the resolution of Coarse Delay Detector. Thus, we adopt a simplified structure of TSV Delay Meter composed of Fine Delay Detector only to be the simulated circuit, as shown in Figure 3.8. Second, the delay difference time is also lower than $\tau/64$, i.e., the maximum resolution of Fine Delay Detector. To overcome the

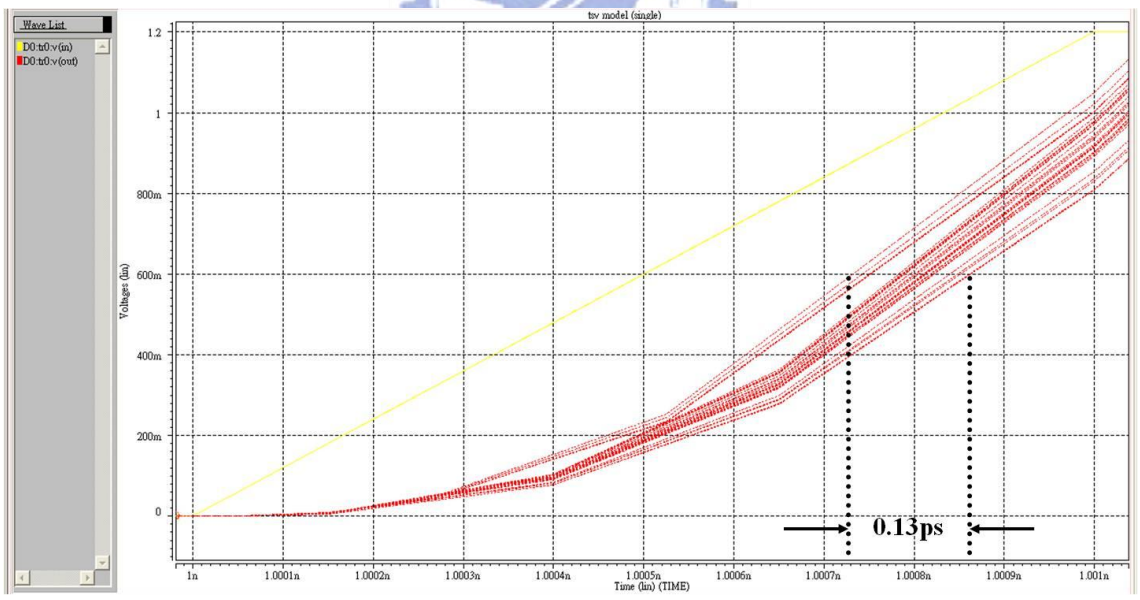
issue, we construct two paths with series TSVs. By series of TSV connected together, TSV Delay Meter is able to accurately detect delay difference time. Because 3D integrated circuit is a structure stacked with many layers, there are a lot of TSVs connected together when the signal propagates from input to output. Therefore, that TSV Delay Meter detects the delay difference time between series TSVs is a reasonable method to solve the resolution issue.

Table 4.1: The parameter values of a single TSV model

	TSV [13]
Diameter	**75 um**
Depth	**90 um**
Material	**Cu**
R	**12 mΩ**
L	**15 pH**
C_{ox}	**800 fF**
C_{Si}	**9 fF**
G_{Si}	**1.92 mS (520 Ω)**
The model of a single TSV	



(a)



(b)

Figure 4.1: (a) Waveforms when a clock signal passes through a TSV (b) An enlarged diagram of (a)

A block diagram of simulated structure is shown in Figure 4.2. The input clock signal has two paths which series the same TSVs with 10 stages to enter the TSV Delay Meter. We suppose that each of the TSVs in path 1 has identical values of the RLCG parameters and each of the TSVs in path 2 has the values of parameters within ±30% process variation compared to path 1. The values of RLCG parameters of the TSVs in path1 and path 2 are shown in Table 4.2.

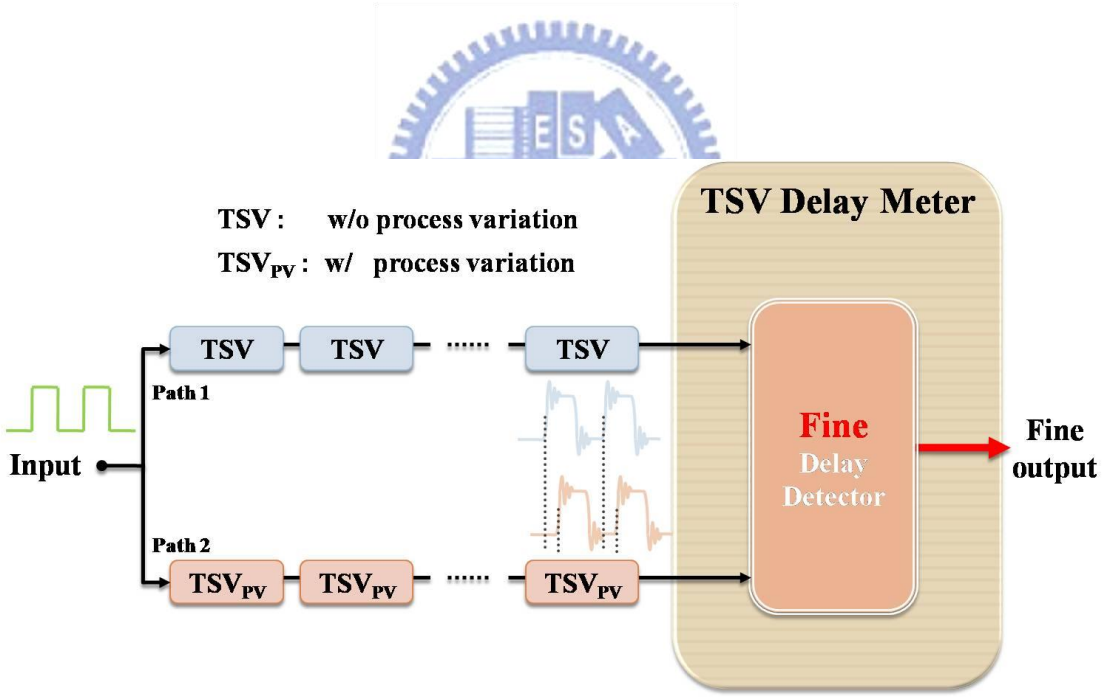
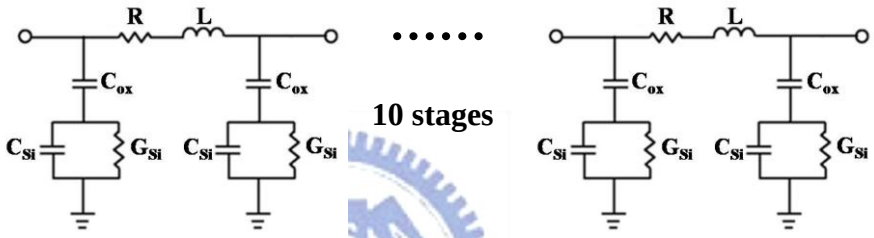


Figure 4.2: A block diagram of detection of process variation

Table 4.2: Parameter values of the model with 10 stages of series TSV

	TSV [13]	TSV_{PV} (TSV±30%)
Diameter	75 um	
Depth	90 um	
Material	Cu	
R	12 mΩ	8.4~15.6 mΩ
L	15 pH	10.5~19.5 pH
C_{ox}	800 fF	560~1040 fF
C_{Si}	9 fF	6.3~11.7 fF
G_{Si}	1.92 mS (520 Ω)	1.344~2.496 mS (400~744 Ω)
The model with 10 stages of series TSV		

After eliminating the range of values of parameters in the path 2, we use the Monte Carlo analysis to simulate 30 output waveforms induced by series TSVs whose values of process variation are given by random, as shown in Figure 4.3 and Figure 4.4. In Figure 4.3 (series 10 stages), we find that the maximum delay difference time between path1 and path2 is 2.146ps, which implies that the delay difference time TSV Delay Meter will find out is either $\tau/64$ or $3\tau/64$. In Figure 4.4 (series 100 stages), the maximum delay difference time is 24.2ps, which implies that the delay difference time TSV Delay Meter will find out is within $31\tau/64$. Therefore, by the method of series TSVs, the TSV Delay Meter will be able to correctly calculate the delay difference time between two paths.

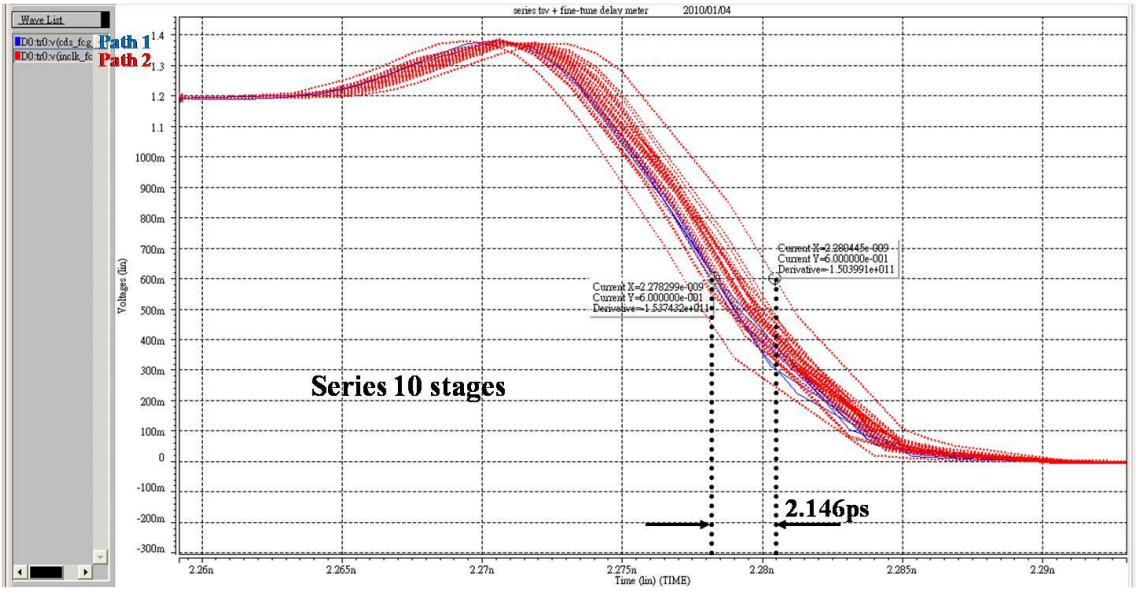


Figure 4.3: Output waveforms of 10 stages of series TSVs

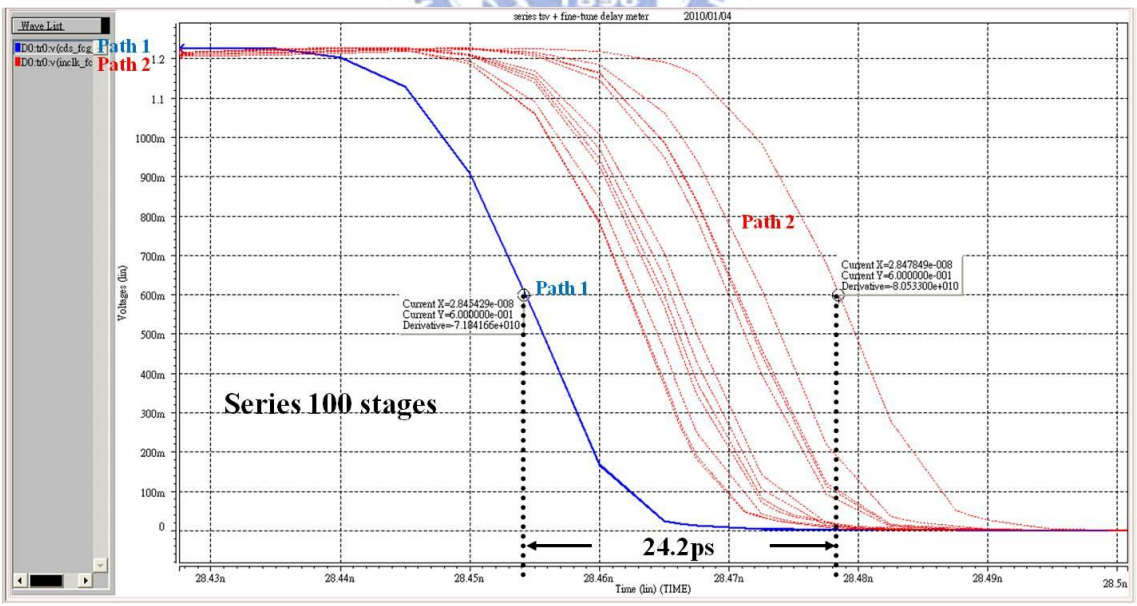


Figure 4.4: Output waveforms of 100 stages of series TSVs

On the other hand, when the percentage of process variation of each TSV in the path 2 is up to 30% exactly, the difference of propagation delay time between path 1 and path 2 is 2.65ps, as shown in Figure 4.5. This time of difference is longer than τ/64, the resolution of Fine Delay Detector, so the TSV Delay Meter operates correctly and then finds out the difference time is 3τ/64 (2.203ps). Compared with the actual difference time, the difference time calculated by TSV Delay Meter has an error with 0.447ps. The error within τ/64 stands for the TSV Delay Meter outputs the digital codes accurately.

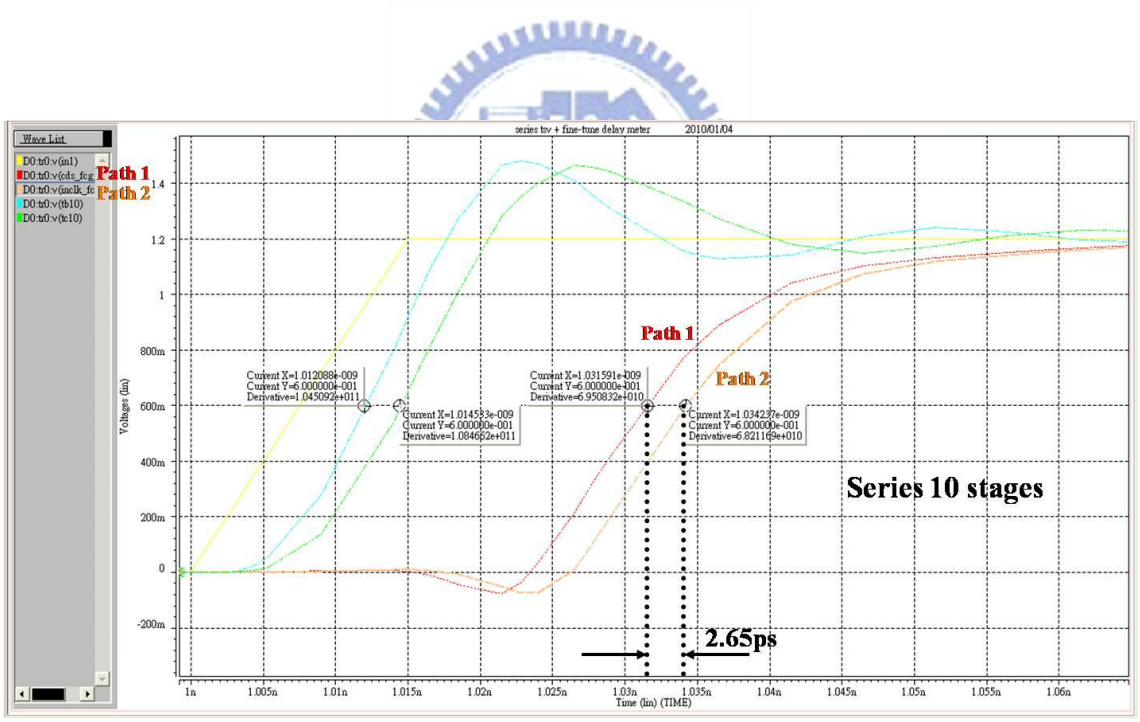


Figure 4.5: Output waveforms of series TSVs with +30% process variation

4.2 Application for Heterogeneous Integration

In addition to measuring the delay difference time induced by process variation, TSV Delay Meter is used to calculate the delay difference time between different types of TSV as well. Because of the development in 3D IC, we could apply heterogeneous integration to enhance performance of the chip. Thus, a signal could be propagated through many paths composed of different types of TSV.

In this application, we choose three types of TSV as the simulation objects. By the two paths composed of series TSVs, the TSV Delay Meter detects the delay difference time between two paths. Table 4.3 shows the characteristics in each type of the TSVs.

Table 4.3: Characteristics of the three types of TSVs

	TSV_1 [10]	TSV_2 [13]	TSV_3 [14]
Diameter	**3um**	**75um**	**55um**
Depth	**15um**	**90um**	**125um**
Material	**Cu**	**Cu**	**Cu**
R	**170mΩ**	**12mΩ**	**50mΩ**
L	**10pH**	**15pH**	**40pH**
C_{ox}	**30fF**	**800fF**	**910fF**
C_{Si}	**6fF**	**9fF**	**9fF**
G_{Si}	**0.5mS**	**1.92mS**	**1.69mS**

Moreover, there are three structures to be constructed and to be detected by the TSV Delay Meter. First, the structure A, whose waveforms entering the TSV Delay Meter are pulled out from different number of series TSVs, is shown in Figure 4.6. Second, the structure B, whose waveforms entering the TSV Delay Meter are pulled out from the same number of series TSVs, is shown in Figure 4.7. Third, the structure C, whose waveforms entering the TSV Delay Meter are pulled out from different number of series TSVs but in the same path, is shown in Figure 4.8.

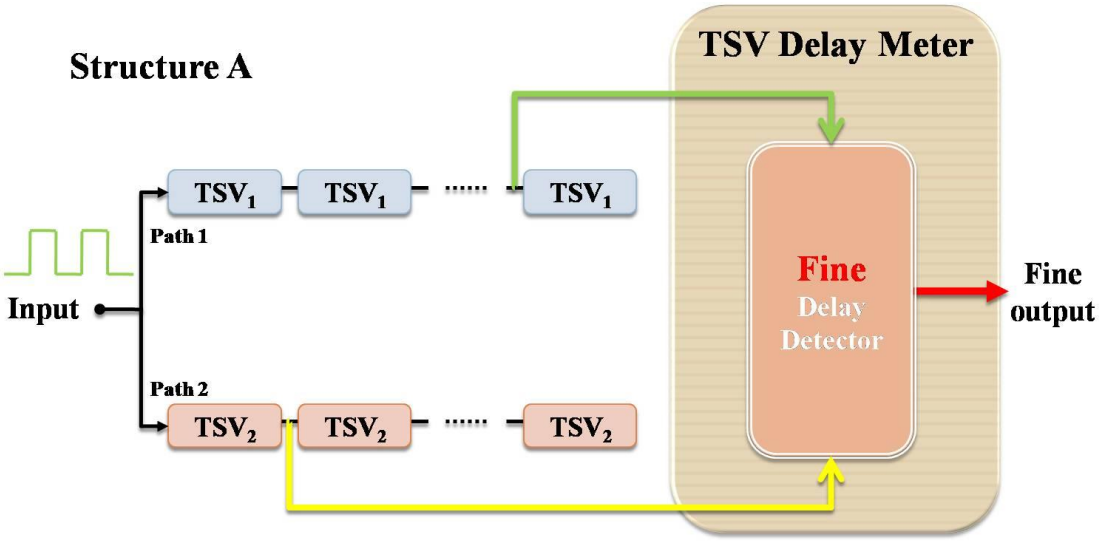


Figure 4.6: Structure A

(Waveforms pulled out from different number of series TSVs.)

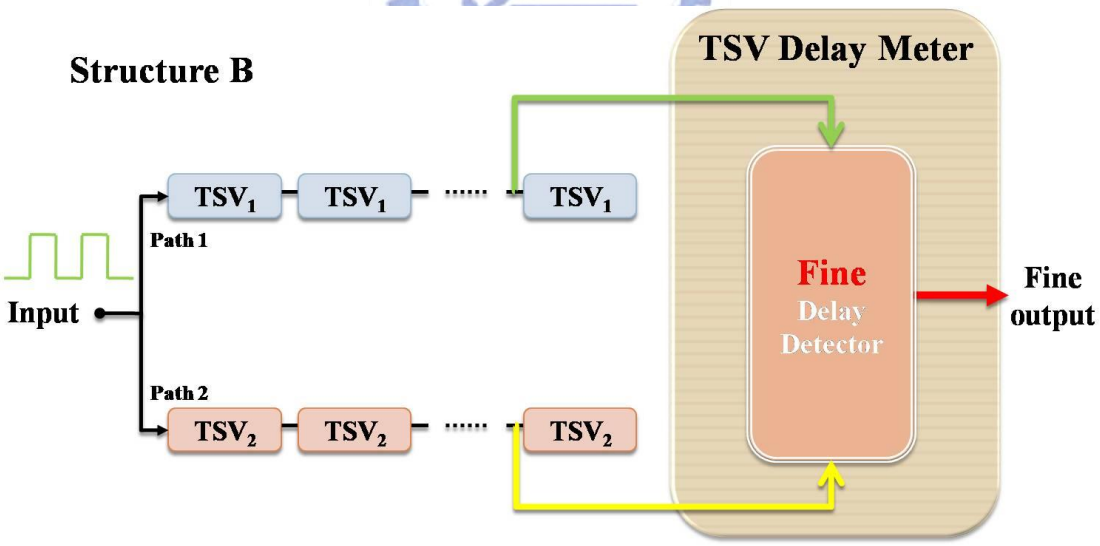


Figure 4.7: Structure B

(Waveforms pulled out from the same number of series TSVs.)

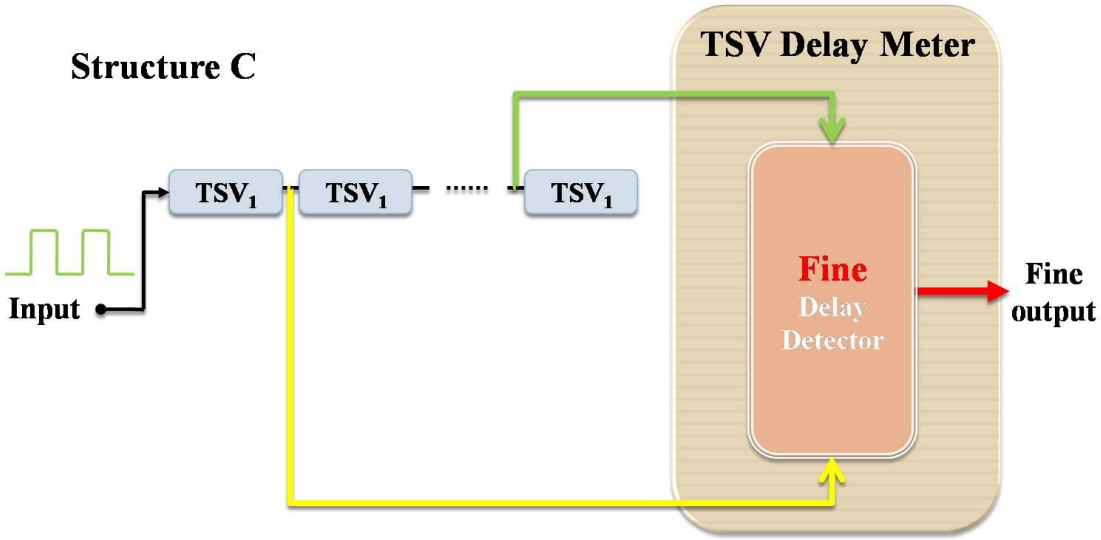


Figure 4.8: Structure C

(Waveforms pulled out from different number of series TSVs in the same path.)

Table 4.4 shows the simulation results of the three structures. In this table, the delay error is defined as the time of a simulation result minus the difference time of two waveforms in front of the Fine Delay Detector and the error rate is defined as the value of the delay error divided by the difference time in front of the Fine Delay Detector. We find that all of the delay error in the simulation results is under $\tau/64$, which stands for that TSV Delay Meter is able to accurately calculate the delay difference time between different types of TSV. Therefore, the TSV Delay Meter not only detects time difference from process variation, but also calculates time difference between various types of TSV in the heterogeneous integration.

Table 4.4: The simulation results of structure A, structure B, and structure C

Type	Cases	Initiative Delay Difference	Delay Difference Before FDD	Simulation Results	Delay Error	Error Rate
Structure A	TSV_1 (5 stages) TSV_2 (1 stage)	1.290ps	1.370ps	2.203ps (3τ/64) Code:01110	0.833ps	60.80%
	TSV_3 (5 stages) TSV_2 (1 stage)	6.730ps	8.540ps	8.078ps (11τ/64) Code:01010	0.462ps	5.41%
Structure B	TSV_1 (5 stages) TSV_2 (5 stages)	2.783ps	3.604ps	3.672ps (5τ/64) Code:01101	0.068ps	1.89%
	TSV_2 (5 stages) TSV_3 (5 stages)	2.646ps	3.884ps	3.672ps (5τ/64) Code:01101	0.212ps	5.46%
	TSV_1 (5 stages) TSV_3 (5 stages)	5.459ps	7.110ps	6.609ps (9τ/64) Code:01011	0.501ps	7.05%
Structure C	TSV_1 (1 stage) TSV_1 (5 stages)	1.750ps	2.020ps	2.203ps (3τ/64) Code:10001	0.183ps	9.06%
	TSV_2 (1 stage) TSV_2 (5 stages)	3.986ps	4.843ps	5.141ps (7τ/64) Code:10011	0.298ps	6.15%
	TSV_3 (1 stage) TSV_3 (5 stages)	6.217ps	7.691ps	8.078ps (11τ/64) Code:10101	0.387ps	5.03%

4.3 Discussions

To evaluate the area that TSV Delay Meter occupies, we calculate the number of transistor of Coarse Delay Detector and Fine Delay Detector as shown in Table 4.5. There are 656 and 496 transistors in Coarse Delay Detector and Fine Delay Detector, respectively. In other words, the total number of transistor that the TSV Delay Meter consumes is about 1200. Compared with the number of transistor in a system, which usually has millions of transistors or more, the number of transistor in the TSV Delay Meter is so minor that the cost of area in a chip will not increase substantially while adding a TSV Delay Meter into the system. As a result, the TSV Delay Meter is a reasonable method to solve the detection of time difference in 3D IC.

Table 4.5: (a) Number of transistor of Coarse Delay Detector and Fine Delay Detector (b) Characteristics of Coarse Delay Detector and Fine Delay Detector

(a)

Coarse Delay Detector			Fine Delay Detector	
Total number of transistor	656		Total number of transistor	496
Component	No.		Component	No.
Inverter	22		Buffer	2
Buffer	12		Phase detector	5
Dummy delay	11		Tuned Delay Line 4	1
D Flip-Flop	11		Tuned Delay Line 8	1
Switching detector	10		Tuned Delay Line 16	1
			Tuned Delay Line 32	1

(b)

Coarse Delay Detector			Fine Delay Detector		
Name	**Description**	**# of MOS**	**Name**	**Description**	**# of MOS**
Transmission gate	PMOS*1 NMOS*1	2	Transmission gate	PMOS*1 NMOS*1	2
Inverter	PMOS*1 NMOS*1	2	Inverter	PMOS*1 NMOS*1	2
Buffer	Inverter*2	4	Buffer	Inverter*2	4
Dummy delay	Inverter*2	4	Tuned buffer	Inverter*2	4
D Flip-Flop	Inverter*8 Buffer*4 Transmission gate*4	40	D Flip-Flop	Inverter*8 Buffer*4 Transmission gate*4	40
Switching detector	NAND gate*1 Inverter*2	8	Phase detector	Buffer*2 D Flip-Flop*1	48
			Tuned delay line 4 (TDL4)	Buffer*12 Tuned buffer*8 Transmission gate*8	96
			Tuned delay line 8 (TDL8)	Buffer*8 Tuned buffer*4 Transmission gate*8	64
			Tuned delay line 16 (TDL16)	Buffer*6 Tuned buffer*2 Transmission gate*8	48
			Tuned delay line 32 (TDL32)	Buffer*5 Tuned buffer*1 Transmission gate*8	40

Chapter 5

Conclusions

5.1 Conclusions

In this thesis, we introduce the development and the characteristics of 3D IC. 3D IC has an advantage of heterogeneous integration, which enhances performance of the chip. In 3D IC, the Through-Silicon-Via (TSV) technology plays an important role for the interlayer connection. The processes of TSV technology are classified as two types: via-first and via-last. The via-first process fabricates TSV before CMOS and BEOL, and the via-last process finishes TSV after CMOS and BEOL.

The TSV equivalent circuit model is composed of RLCG lumped devices. Because of process variation, the delay difference time will be induced when a signal passes through two paths composed of the same series TSVs. Thus, the TSV Delay Meter is designed for precisely calculating the time difference in this thesis. Using the Monte Carlo analysis to simulate the performance of TSV Delay Meter by TSMC 90nm CMOS process, we could know the resolution of the meter is $\tau/64$, about 0.74ps. The simulation results show that delay error is lower than $\tau/64$, which stands for that TSV Delay Meter operates accurately. In addition, the cost of TSV Delay Meter using about 1200 transistors is much lower than the cost of a system.

Consequently, TSV Delay Meter is feasible to find time difference accurately, which helps a system to adjust delay error and enhance performance in 3D IC.

5.2 Future Work

Not only TSVs but also transistors incur process variability. Although the internal circuit of this meter may induce errors on the measured time differences, in this thesis, we consider only one TSV Delay Meter is burried into a chip. Since this meter is the consistent reference to all measured results, the relative (instead of exact) values should be concerned. Thus, we do not need to consider process variation of transistors when a single TSV Delay Meter is burried into a chip.

However, if a chip is burried with more than one meter, each meter may be biased with different amount of process variation. Thus, the future work should consider the impact of process variation on transistors.

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