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橫向擴散的射頻金氧半場效電晶體之特性分析與模型建立

Characterization and Modeling of RF LDMOS

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中華民國 九十八 年 七 月

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中文摘要

近年來，射頻橫向擴散金氧半場效電晶體（RF LDMOS）在手機基地台中，作為功率放大氣得重要元件。為了能符合新一代通訊標準的需求，必須不斷地改善 LDMOS 的特性。在本論文中，我們將探討四種結構：fishbone、square、octagon 和 circle 的直流、高頻和射頻功率特性。為了得到較低的汲極電阻，我們採用了不同於傳統結構的三種「環狀」結構。除此之外，為了抑制 square 結構所附帶角落的影響，我們將四方形的環修正為八角形和圓形的環。另外，還針對 square 結構，去探討不同通道寬度的影響，得知通道較小的元件具有較佳的直流表現，但是，在高頻部分則呈現較差的結果。為了進一步地了解元件參數對高頻特性的影響，我們建立了小訊號等校電路，將其參數萃取出並分析比較。實驗結果顯示，我們所設計的環狀結構，透過汲

極面積的增加，能夠有效地降低汲極端的寄生電阻，因而改善元件的截止頻率（f_T）和最大震盪頻率（f_{max}）。此外輸出功率、功率增益以及附加功率效率均有較佳的表現，而線性度和崩潰電壓則和 fishbone 結構不相上下。使用 circle 結構可以得到較大的電流和轉導，因為能更有效地減少汲極端寄生電阻。由於 circle 結構只更動光罩之設計，至程流程並無改變，因此實為一大優點。

另一方面，我們也完整的分析元件的電容特性。由於 LDMOS 的通道為非均勻摻雜且具有漂移區，因此電容會有峰值產生。我們發現 square 結構會出現第二個峰值，而 circle 結構則和 fishbone 結構一樣只有單一峰值。這是因為 square 結構再轉角處的電流密度較小，使得電子速度需要較大的閘極偏壓才能進入類飽和狀態。

我們使用修改過的 MM20 模型去建立 fishbone 和 circle 結構的元件模型，藉由使用 T-CAD 模擬軟體，得到橫向電場和空乏區的分佈。另外得知具有 field plate 結構的元件操作在發生 quasi-saturation 下，在漂移區中，其電場較為均勻並能使電阻降低。利用模擬的結果去修改 MM20 模型成為一個簡單且沒有太多複雜運算的模型，能容易地去描繪出元件的電性。利用修改過的模型去萃取出 fishbone 和 circle 結構的元件參數並比較分析，結果顯示，這些參數所表達的訊息與第二章小訊號參數的結果相輔相成，具有相似的趨勢。因此，使用這模

型模擬不同步局設計的 RF LDMOS，所得到的 I-V 和 C-V 曲線也與量測的電性曲線相符，確實得到精確的一致性。

Characterization and Modeling of RF LDMOS

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Abstract

RF LDMOS nowadays plays an important role in the RF power amplifier applications in base stations for personal communication systems. In order to meet the demands imposed by new communication standards, the performance of LDMOS is subject to continuous improvements. In this thesis, four types of layout structures, fishbone, square, octagon and circle were studied for DC, high-frequency, and RF power characteristics. To achieve lower drain resistance, we adopted "ring" structures in the layout design. In addition, to reduce corner effect, we modified the square ring structures to octagon and circle rings. For square structures, variation of channel widths was investigated. The device with smaller W_{ch} shows better DC performance but shows worse RF performance. In order to determine the effect of device parameters on high-frequency characteristics more clearly, small-signal equivalent circuit was built to be analyzed. From the simulation results, the smaller drain parasitic resistance in the ring structures could be the key factor for improving f_T and f_{max} contrasting to fishbone structure. As for microwave power characteristics, output power, power gain and power added efficiency (PAE) were improved with a similar linearity with the same breakdown voltage. The extra areas in the drift region would

have lowered the drain parasitic resistance and improve the on-resistance. By using the circle structure, higher drain current and transconductance were shown by the reason of larger equivalent W/L and lower drain parasitic resistance comparing to square. Its reveals that the circle structure had a better performance, without altering the process flow.

In another part of this thesis, we discussed and analyzed the capacitance characteristics completely. For having a non-uniform doping channel and the existence of the drift region, C_{GS}+ C_{GB} and C_{GD} exhibit a peak in LDMOS. In the square structure, the second peaks in a capacitance-voltage curve have been observed at high drain voltages for the first time. Besides, the circle structure has the same capacitance characteristics as the fishbone structure that indicates only one peak in the capacitance curve. While the corner region of the drift in the square shows lower current density than the edge region, it needs higher gate voltage to enter quasi-saturation. By increasing the gate voltage, the current in the corner region is high enough to make the velocity of electrons in the drift saturated.

The device models have been built for fishbone and circle structures by using the modified MM20. We obtain the lateral electric field distribution and the depletion distribution by using T-CAD simulated software. The device with field plate has uniform electric field and lower resistance in the drift region as device enters quasi-saturation. From the result of simulation, we modify the MM20 to a simple model. It is easier to describe the electrical characteristics of device. The extracted model parameters were also investigated for fishbone and circle structures. These parameters present the similar information as chapter 2. Therefore, this model shows an accurate description on I-V and C-V curves, and provides a good agreement between simulated and measured data for the RF LDMOS with different layout designs.

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Contents

Chinese Abstract i

English Abstract iv

Acknowledgement vi

Contents vii

Table Captions xi

Figure Captions xii

Chapter 1 Introduction

1.1 Introduction to RF LDMOS 1

1.2 Advantages Compared to the Bipolar Technology 2

1.3 Advantages Compared to Other Materials 2

1.4 Motivation 3

1.5 Thesis Organization 4

Chapter 2 Characterization of RF LDMOS with Different Layout Designs

2.1 Introduction 5

2.2 Device Structures 5

2.2.1 DC Characteristics 6

2.2.2 High-frequency Characteristics 7

2.2.3 RF Power and Linearity 10

2.3 Summary 12

Chapter 3 Characterization of RF LDMOS with Different Channel Widths

3.1 Introduction 27

3.2 RF LDMOS with Square Structure 27

3.2.1 DC Characteristics 27

3.2.2 High-frequency Characteristics 28

3.2.3 RF Power and Linearity 30

3.3 Summary 31

Chapter 4 Capacitance Characteristics of RF LDMOS with Different Layout Design

4.1 Introduction 41

4.2 Capacitances versus V_{GS} for Fishbone LDMOS 41

4.3 Capacitances versus V_{GS} for Different Layout Structures 43

4.4 Summary 43

Chapter 5 Modified MOS Model 20 (MM20) for LDMOS

5.1 Introduction 48

5.2 T-CAD Simulation 48

5.3 Modeling Strategy 49

5.4 Results and Discussion 52

5.5 Summary 53

Chapter 6 Conclusions and Suggestion

6.1 Conclusion 60

Reference 62

Table Captions

Chapter 2

Table 2-1 Extracted R_{on} and V_{BD} for four different layout structures. 13

Table 2-2 Extracted g_m, R_d C_{gd} and C_{gs} to see their effects on f_T for different layout structures. 13

Table 2-3 Individual effects of the model parameters on f_T. The square device is as a reference. 14

Table 2-4 Extracted R_g, R_d, C_{gd}, C_{gs}, C_{ds} and C_{jdb} to see their effects on f_{max} for different layout structures. 14

Table 2-5 Individual effects of the model parameters on f_{max}. The square device is as a reference. 15

Table 2-6 C_{jdb} and DNW area for four different layout structures. 15

Table 2-7 IIP3 and OIP3 for four different layout structures. 16

Chapter 3

Table 3-1 Extracted R_{on} and V_{BD} for the square device with different channel widths. 32

Table 3-2 Extracted g_m, R_d C_{gd} and C_{gs} to see their effects on f_T for square device with different channel widths. 32

Table 3-3 Individual effects of the model parameters on f_T. The square_10x40 is as a reference. 33

Table 3-4 Extracted R_g, R_d, C_{gd}, C_{gs}, C_{ds} and C_{jdb} to see their effects on f_{max} for square device with different channel widths. 33

Table 3-5 Individual effects of the model parameters on f_{max}. The square_10x40 is as a reference. 34

Table 3-6 IIP3 and OIP3 for square device with different channel widths. 34

Chapter 5

Table 5-1 Extracted V_{FB}, μ_{ch}, μ_{dr}, θ_{3dr}, R_{dr} and L_D from modified MM20 for different layout structures. 54

Figure Captions

Chapter 2

Fig. 2-1 LDMOS layout structures: (a) fishbone, (b) square and (c) circle. 17

Fig. 2-2 Schematic cross section of an LDMOS transistor. 17

Fig. 2-3 (a) Subthreshold and (b) output characteristics of LDMOS transistors with different layout designs. 18

Fig. 2-4 R_{TH} of LDMOS transistors with different layout design. 19

Fig. 2-5 Dependence of (a) |h21| and (b) MSG/MAG on frequency obtained from S-parameter measurements. 20

Fig. 2-6 (a) f_T and (b) f_{max} versus gate voltage with different layout design. 21

Fig. 2-7 A simple equivalent circuit model of the LDMOS. 22

Fig. 2-8 Effects of small-signal model parameters on (a) f_T and (b) f_{max}. 23

Fig. 2-9 The drain to body junction capacitance 24

Fig. 2-10 Output power, power gain and PAE versus input power with different layout designs. 25

Fig. 2-11 Drain current versus gate voltage with different layout designs. The input signal was biased at V_{GS}=2.5V and the negative duty cycle of output signal was clipped by the cutoff region. 25

Fig. 2-12 Average drain current as a function of the input power with different layout designs. 26

Fig. 2-13 Output power and third-order intermodulation power versus input power with different layout designs. 26

Chapter 3

Fig. 3-1 (a) Subthreshold and (b) output characteristics of LDMOS transistors with different channel widths. 35

Fig. 3-2 R_{TH} of LDMOS transistors for square structure with different channel widths. 36

Fig. 3-3 (a) f_T and (b) f_{max} versus gate voltage for square structure with different channel widths. 37

Fig. 3-4 Effects of small-signal model parameters on (a) f_T and (b) f_{max}. 38

Fig. 3-5 Output power, power gain and PAE versus input power with different channel widths. 39

Fig. 3.6 Drain current versus gate voltage with different channel widths. The input

signal was biased at V_{GS}=2.5V and the negative duty cycle of output signal was clipped by the cutoff region. 39
Fig. 3-7 Average drain current as a function of the input power with different channel widths. 40
Fig. 3-8 Output power and third-order intermodulation power versus input power with different channel widths. 40

Chapter 4

Fig. 4-1 Extracted C_{GS}+C_{GB}, C_{GD} and the drain current versus gate voltage at different drain biases for the fishbone structure. 45
Fig. 4-2 Extracted C_{GS}+C_{GB} and C_{GD} versus gate voltage at different drain biases for the (a) square and (b) circle structure. 46
Fig. 4-3 Extracted C_{DG} versus gate voltage at different drain biases for the fishbone, square and circle structure. 47
Fig. 4-4 Schematic view of layout structure and current distribution: (a) fishbone structure, (b) square structure and (c) circle structure. 47

Chapter 5

Fig. 5-1 The right figure shows the space charge distribution of LDMOS at V_g= 2.5V and V_d= 10V and the left figure shows the electric field along the channel region to drift region. 55
Fig. 5-2 The right figure shows the space charge distribution of LDMOS at V_g= 10V and V_d= 10V and the left figure shows the electric field along the channel region to drift region. 55
Fig. 5-3 The right figure shows the space charge distribution of LDMOS at V_g= 2.5V and V_d= 10V and the left figure shows the electric field along the channel region to drift region. 56
Fig. 5-4 The right figure shows the space charge distribution of LDMOS at V_g= 10V and V_d= 10V and the left figure shows the electric field along the channel region to drift region. 56
Fig. 5-5 Measured (mark) and simulated (line) drain current (I_{DS}) versus gate voltage at different drain biases for the (a) fishbone and (b) circle structures. 57
Fig. 5-6 Measured (mark) and simulated (line) drain current (I_{DS}) versus drain voltage at different gate biases for the (a) fishbone and (b) circle structures.. 58
Fig. 5-7 Measured (mark) and simulated (line) C_{GS}+C_{GB} and C_{GD} versus gate

voltage at different drain biases for the (a) fishbone and (b) circle structures. 59

Chapter 1

Introduction

1.1 Introduction to RF LDMOS

In our life, the power device is used in many electronic products. The Lateral-Diffused MOS (LDMOS) transistor is one of the power devices. The LDMOS has been used in switching applications for many years. In the early 70's, the first publication of LDMOS was demonstrated in microwave operation, and with technology development the LDMOS operating frequency entered into the GHz range gradually, which covered the frequency range of many of today's popular wireless products, like: Wireless infrastructure (GSM, EDGE, WCDMA, and WiMAX); Broadcast; pulsed radar; industrial, scientific and material (ISM) applications; avionics and military applications [1]. Up to 2005, Si LDMOS covered about 90 percent of the high power RF amplification applications in the 2GHz and higher frequency range, according to market analyst company Yole Développement. For more convenient life, the wireless infrastructure requiring RF power amplification is gradually built in the modern city, and the power amplifiers have to be low cost, high efficiency, and good linearity [2]. LDMOS technology plays an important role in the RF power amplifier applications in base stations for personal communication systems for frequencies up to 2.14 GHz. However it is possible, and demonstrated, to use LDMOS for frequencies up to 3.8 GHz with the latest LDMOS technology development [3]. Moreover, LDMOS transistors for amplifier applications has gone through a great development with improvements in available output power, power gain, power added efficiency and linearity together with improvements in hot carrier reliability and thermal resistance in last five years [4]. And the LDMOS technology can be incorporated in CMOS process, it is very important for power integrated circuits.

1.2 Advantages Compared to the Bipolar Technology

The advantages of using LDMOS for high power high frequency applications are on the following points:

High linearity: the process controlled short channel length makes the device works in velocity saturation. The linear relation of drain current and gate voltage leads to a constant transconductance and improves the linearity.

Higher gain: the power gain can be improved by the lower source inductance and lower feedback capacitance. The former can be done by tying the source and P-body together to the RF ground. In bipolar, the backside collector requires insulating from the ground and the top side emitter needs bond wire to connect to the ground. The additional bond wire introduces high inductance and limits the power gain. Also, the LDMOS is a lateral structure device which has lower feedback capacitance compared with a bipolar transistor. In addition, the LDMOS has negative temperature coefficient and does not need ballast resistor which used in bipolar and degrade the bipolar's power gain. Therefore, the LDMOS provides higher gain than bipolar for the same output power level. This means that less amplifier stages are needed, and thus gives higher reliability and lower cost.

Thermal stability: LDMOS has no thermal runaway problem due to its negative temperature coefficient. The higher drain current leads to higher temperature which lowers the channel mobility and resulting in a drop in drain current. On the other hand, the temperature coefficient in bipolar is positive and more prone to thermal runaway

High ruggedness: LMODS has positive temperature coefficient of channel resistance and high drain-source breakdown voltage. Consequently, LDMOS has excellent ruggedness into an output mismatch VSWR typically 10:1 whereas the bipolar can only accept 3:1 [5-6].

1.3 Advantages Compared to Other Materials

The other possible materials which can be used for base station applications include

GaAs and wide bandgap materials: SiC and GaN. GaAs based power devices can achieve higher drain efficiency and linearity due to a higher electron mobility and higher saturation velocity then silicon. However, the fact is that the saturation velocity for GaAs decreases and can be comparable to the saturation velocity for silicon at high electric field. And the lower thermal conductivity (~ 0.46 W/cm K) of GaAs is disadvantage to the high power final stage amplifiers which is needed in base station transmitters. The wide bandgap materials: SiC and GaN, which have good material properties and obtain high electric breakdown voltage and high saturation velocity. The problem for SiC is the possibility to manufacture defect free substrates. However with device continuous scaling down, silicon technology can keep playing an important role in RF systems due to reduced cost compared to other compound materials under equivalent performance. In order to compete with silicon and GaAs, the GaN and SiC have to get right way to overcome high cost. After all a superior technology must be cost competitive [7]. For silicon LDMOS, high thermal conductivity (~ 1.5 W/cm K) and quite high operation voltage make this technology suitable for base station power amplifier.

1.4 Motivation

With process technology development, the device is going to small size by reducing gate length. And power device also scales down the gate length and the drift length to improve on-resistance and transconductance. However, there is a limit of scaling down due to high-voltage on working. The choice of on-resistance and breakdown voltage is a trade-off in the conventional LDMOS. Several researchers have proposed solutions to these trade-offs such as using a double-doped offset [8], or a stacked or step drift region [9], or even the strain structure [10], or changing the process flow. There is also other solution to solve the trade-off between the on-resistance and breakdown voltage by optimizing the layout design. In this thesis, four types of layout structures (fishbone, square, octagon and circle) were studied for DC, high-frequency, and RF power characteristics. According to its structure, the parasitic

drain resistance of the LDMOS becomes more important than that of the conventional MOSFET for the present drift region. In order to effectively use layout area and reduce the parasitic effect from metal connected line or device to enhance the performance of device, we have to know which parts of the device have a great influence. In addition, the device capacitances influence the input, output and feedback capacitances, which are important in the dynamic operation, and have large impact on device high-frequency performance. The capacitance characterization and modeling of LDMOS transistors have been studied widely [11-13]. Finally, an accuracy model that describes the electric characteristics of RF LDMOS is needed for circuit design. In this thesis, an LDMOS modeling technique was also investigated.

1.5 Thesis Organization

The content in this thesis includes the following parts.

Chapter 1 introduces the LDMOS for RF applications and the motivation of this thesis.

Chapter 2 presents the DC, high-frequency and RF power performances of LDMOS with different layout structures. In addition, the small-signal model parameters were extracted to investigate their effects on f_T and f_{max}.

In chapter 3, the DC, high-frequency and RF power performances of square LDMOS with various channel widths were analyzed. Also, the small-signal model parameters were extracted to investigate their effects on f_T and f_{max}.

Chapter 4 presents the unusual capacitance behavior of RF LDMOS with fishbone, square and circle structures. Capacitance versus gate voltages with different drain voltage was investigated.

Chapter 5 presents the modified MM20 modeling for RF LDMOS.

Finally, the conclusions of this thesis are summarized in Chapter 6.

Chapter 2

Characterization of RF LDMOS with Different Layout Designs

2.1 Introduction

In high-power applications, the RF transistors are usually implemented in a "fishbone" structure, as shown in Fig. 2.1(a). All the gate fingers are divided into several subcells, in each of which, 2-10 gate fingers are grouped together. For RF performance concern, multi-finger layouts are used to design wide MOSFETs for reducing the gate resistance and source/drain junction capacitance. Since the gate resistance would limit the power gain attainable at a certain frequency and thus f_{max} [14-18]. The drain resistance which includes accumulation layer resistance and JFET resistance are the main component in LDMOS to have influence on the on-resistance. Here, in order to achieve lower on-resistance, we adopted a "square" structure which is different from the "fishbone" in the LDMOS layout design (see Fig. 2.1(b)). However, in our previous study, we found that the square structure has higher gate capacitances compared to that of fishbone structure, owing to the corner effect [19]. In order to reduce the corner effect, we modified the square ring structures to octagon and circle rings (see Fig. 2.1(c)) in this work. Then we investigated the DC, high-frequency, and RF power characteristics of the devices with different layout structures.

2.2 Device Structures

RF LDMOS transistors were fabricated using a 0.5 μm LDMOS process. The schematic cross section of the device is shown in Fig. 2.2. The drain region was extended under the gate oxide and consisted of a lightly doped N-well drift region and an N^- region with higher doses for on-resistance control. The source region and the p-body were tied together to eliminate extra surface bond wires to reduce the source inductance and improve the RF performance in a power amplifier configuration [20]. The gate oxide thickness was 135 Å and the mask

channel length (L_{CH}) was 0.5 μm. The drift length ($L_{Drift}=L_{OV}+L_{FOX}$) was 2.4 μm. The fishbone structure used in this study had 10 cells which each cell had 4 fingers with finger width L_F=10 μm. For the other structures, the width of each gate ring was 40 μm and each cell was arranged as a 5x2 array in one device. The source region was surrounded by the drain region, while the gate was located between the source and the drain (see Fig. 2.1). To compare the performance of all structures fairly, the total channel width is the same (W= 400 μm).

2.2.1 DC Characteristics

The *I–V* characteristics of the LDMOS with different layout structures are shown in Fig. 2.3. For ring structures, the circle device shows the highest drain current and transconductance than others, and the square device shows the worst performance. Because the square structure has additional four corners, where the drain current density is lower than that in edges, the effective drain resistance would be higher than that in octagon and circle structures. It results a lower drain current compared to that in other structures. The dc characteristics of fishbone device are also shown in Fig. 2.3. The drain current and transconductance are not lower than the ring structures in low- and medium-bias regions, but in high-bias region the drain current would be suppressed more due to the quasi-saturation effect. Because the fishbone structure has higher resistance in the drift region, a larger voltage drop in drift region will exist than that of ring structures. As a result, the carriers in the drift region of the fishbone device will enter the velocity saturation earlier than ring structures. When the velocity saturation in the drift region occurs, the device will operate in "quasi-saturation", where the intrinsic MOS is still in linear operation. This effect is generally observed at high gate voltages. As the device enter the quasi-saturation, the gate control ability decreases which limits the drain current level and delays the transition between linear and saturation regime. So when the device operates at high power condition, the ring structure has a better performance due to reduced quasi-saturation effect.

From the output *I–V* characteristics of the fishbone structure, we observe a negative output resistance in the high-current region. With high current density in the transistor, the rise in device temperature resulted from the dissipated power becomes significant. The increased device temperature reduces the carrier mobility and saturation velocity [21]. Fig. 2.4 shows the thermal resistance (R_{th}) of three different layout structures. The fishbone device has higher thermal resistance compared to ring devices. Due to compact layout area, the self-heating effect in the fishbone structure is significant. The device self-heating can be improved by increasing the distance between each cell of fishbone.

The drain-source on-resistance is an important parameter for describing the performance of LDMOS transistors. The on-resistance (R_{on}) is extracted from the linear forward I–V characteristics at gate voltage V_{GS} = 2.5 V, since it is predominated by the drift region under such a condition (see Table 2-1). R_{on} is related to the drain current and is dependent on the drain resistance. Among the ring structures, the R_{on} is lowest in the circle device, and it is interpreted as being due to a lowest drain resistance, In Table 2-1, we also observe that the R_{on} in fishbone device is lower than that in ring devices due to lower channel resistance. This result is limited by standard processing. In addition, another important parameter is breakdown voltage for LDMOS. We obtain that the four devices have the similar breakdown voltage ($V_{BD}\cong$ 41-43V).

2.2.2 High-frequency Characteristics

To characterize the high-frequency performance, the S-parameters were measured on-wafer from 0.1 to 30 GHz using an HP8510 network analyzer and then de-embedded by subtracting the OPEN dummy. Fig. 2.5 shows the high-frequency characteristics of circle structure. The maximum stable gain/maximum available gain (MSG/MAG) and short-circuit current gain (h_{21}) were calculated from S parameters. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were determined as the frequency where the current gain was 0 dB

and the frequency where MAG was 0 dB, respectively. The transistors were measured at drain voltage V_{DS}=20 V with different gate voltages. From Fig. 2.6, f_T had maximum values at V_{GS}=2.5 V, where the transconductance showed a peak. With increasing the gate voltage, both f_T and f_{max} decreased owing to the mobility degradation and quasi-saturation effects.

The cutoff frequency and maximum oscillation frequency for the LDMOS with different layout structures are compared in Fig. 2.6. The transistors were biased at V_{GS}=2.5 V and V_{DS}=20 V to obtain the maximum value of f_T. It is observed that the values of f_T in these layout structures are circle > octagon > square > fishbone and the values of f_{max} are square > circle > octagon > fishbone.

By analyzing a MOSFET small-signal equivalent circuit, we can determine the effect of device parameters on high-frequency characteristics more clearly. We adopted a simple model (shown in Fig. 2.7) and extracted the equivalent circuit parameters of the LDMOS by the method described in ref. 22. After de-embedding the extrinsic parasitic resistances and the substrate-related parameters, the intrinsic components could be directly extracted from intrinsic Y-parameters (Y_i) by the following equations [23]:

$$C_{gd} = -\frac{1}{\omega}\mathrm{Im}(Y_{i,12})$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{i,11}) - \omega C_{gd}}{\omega} \cdot \left(1 + \frac{(\mathrm{Re}(Y_{i,11}))^2}{(\mathrm{Im}(Y_{i,11}) - \omega C_{gd})^2}\right)$$

$$C_{ds} = \frac{1}{\omega}\mathrm{Im}(Y_{i,22} + Y_{i,12})$$

$$R_i = \frac{\mathrm{Re}(Y_{i,11})}{(\mathrm{Im}(Y_{i,11}) - \omega C_{gd})^2 + (\mathrm{Re}(Y_{i,11}))^2}$$

$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{i,22})}$$

$$g_{m0} = \sqrt{((\mathrm{Re}(Y_{i,21}))^2 + (\mathrm{Im}(Y_{i,21}) + \omega C_{gd})^2) \cdot (1 + \omega^2 C_{gs}^2 R_i^2)}$$

$$\tau = \frac{1}{\omega} arc\sin\left(\frac{-\omega C_{gd} - \mathrm{Im}(Y_{i,21}) - \omega C_{gs} R_i \mathrm{Re}(Y_{i,21})}{g_m}\right)$$

Using extracted parameters from the existing device and altering one parameter at the time, the effect of model parameters on the cutoff frequency and maximum oscillation frequency can be visualized. The influences of model parameters on f_T and f_{max} are shown in Fig. 2.8. The x-axis showed the parameter value departure from the initial value in percent. The y-axis showed the change in frequency in percent. Parameters not shown in the figure had approximately the same value for the ring and fishbone structures or had a minor influence on f_T and f_{max}. As shown in Fig. 2.8(a), the intrinsic transconductance (g_m), gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) have large effect on f_T. The cutoff frequency can be expressed in a simple way of $f_T = g_m/ 2\pi (C_{gs}+ C_{gd})$ which is related to the g_m and input intrinsic capacitances ($C_{in}= C_{gs}+ C_{gd}$). The extracted model parameters that affect the f_T more significantly are listed in Table 2-2. For ring structures, we find that the slight increase of f_T in circle device is mainly due to the slight increase of g_m. When g_m increases from 34.58 mA/V to 35.92 mA/V and 36.7 mA/V for octagon and circle respectively contrasting with square structure, f_T is improved by about 3.7% and 5.9% (see Table 2-3). The gate capacitances are nearly unchanged. For fishbone device, however, the drain resistance (R_d) is large and its effect on f_T cannot be ignored. R_d represents the drain contact resistance and part of the drift region. As compared to square device, R_d has been increased from 2.6 Ω to 9.05 Ω for fishbone device, and thus f_T becomes worse about -3.9%. In addition, the lower C_{gd} and higher C_{gs} in the fishbone structure cause about 3.7% and -7.2% changes in f_T due to different layout design. Otherwise the intrinsic g_m of fishbone is the biggest among four structures and makes f_T increase about 6.5%. As illustrated in Fig. 2.8(b), in addition to the intrinsic parameters, the R_d, gate resistance (R_g), drain-source capacitance (C_{ds}) and drain-substrate junction capacitance (C_{jdb}) have apparent effects on f_{max} [24]. The extracted model parameters that affect f_{max} more significantly are listed in Table 2-4. The square structure has the highest f_{max} due to lower parasitic drain junction capacitance (C_{jdb}) and gate to source capacitance (C_{gs}). The C_{jdb} can be separated into two parts; one is between P-body

and DNW, another is between DNW and substrate (see Fig. 2.9), and then the C_{jdb} is relative to area of DNW. Because the square structure has small area, the DNW area and thus the C_{jdb} are small (see Table 2-6). Contrary to square, the fishbone structure has the lowest f_{max} due to higher R_d and C_{gs} in addition to lower f_T. Comparing to the square structure, the octagon and circle structures have lower f_{max} due to larger C_{jdb} and drain to source capacitance (C_{ds}). A part element of C_{ds} represents the overlap of metal conducting wires. Although f_{max} should be improved with the g_m increasing, the other parameters will also affect the f_{max}. For ring structures, the C_{ds} increases from 97.62 fF to 119.9 fF and 119.8 fF for octagon and circle respectively contrasting with square structure, both f_{max} become worse about -2.9% (see Table 2-5). In addition, the C_{jdb} increase from 52.13 fF to 129.9 fF and 132.3 fF, the f_{max} also become worse about -7.6% and -7.8%. For fishbone structure, we are easy to find the R_d has a great impact on f_{max} and becomes important. As compared to square device, R_d has been increased from 2.6 Ω to 9.05 Ω for fishbone device, and thus f_{max} becomes worse about -23.8%. In addition, the lower C_{gd} and higher C_{gs} in the fishbone structure cause about 8.6% and -6.9% changes in f_{max} due to different layout design. Otherwise the extrinsic parameters (R_g and C_{ds}) also make f_{max} increase about 5.7% and 6.8% respectively. Consequently, the f_{max} for circle structure is lower than the one for square structure by about -3.5% (f_{max} was 14.74 GHz for the square structure and 14.22 GHz for the circle structure). The f_{max} for octagon structure is lower than the one for square structure by about -10.7% (f_{max} was 14.74 GHz for the square structure and 13.16 GHz for the circle structure). The f_{max} for fishbone structure is lower than the one for square structure by about -11.2% (f_{max} was 14.74 GHz for the square structure and 13.09 GHz for the fishbone structure).

2.2.3 RF Power and Linearity

As well as the high-frequency characteristics, the microwave power characteristics are also investigated using the load-pull measurement. In our study, the source and load

impedances were tuned for maximum power gain and maximum output power, respectively. The power tune is setup at 2 dBm before the power gain starts to degrade. For having the value of f_{max} in the range from 13 GHz to 15 GHz, the devices were measured at 1.8 GHz with gate bias V_{GS}=2.5 V and drain bias V_{DS}=20 V. Figure 2.10 shows the output power, power gain and power added efficiency (PAE) with different layout designs. There are only three layout structures of LDMOS: fishbone, square and circle, because the octagon structure is similar to circle structure.

The power gain is related to f_{max}. The square device has largest power gain and the fishbone device has smallest power gain (see Fig. 2.10). We find that the power gain of square structure degrades earlier than others when input power goes beyond 1-dB compression point (P_{1dB}). The main reason for gain compression is attributed to the clipping effect. The border of output I-V curve will cause output waveform to be clipped for MESFET, PHEMT and HBT [25-27]. The clipping effect can also been found in LDMOS. Figure 2.11 shows the drain current versus gate voltage with input and output waveform for different layout designs. Part of the AC-signals on the drain current would be cut off as the input power becomes larger enough. At this condition, the average drain current increased with the increasing input power (see Fig. 2.12) and the power gain has been compressed. This is because the dynamic load line exceeds the border of DC I-V. For the square structure, the drain current makes the negative duty cycle of output waveform enter the cutoff region earlier. This indicates that the average drain current started to increase earlier (see Fig. 2.12) and the gain compression occurs prior. And another two structures have the similar characteristics that the gain compression occurs lately. Generally the device operating range is before P_{1dB} point, so the circle has wider operating range than square. Consequently, although the square structure shows higher value of output power, power gain and PAE, the operating range is narrower slightly. Since the DC behaviors were changed, the linearity would also be affected with different layout designs. The input and output third-order intercept points (IIP3 and OIP3) for

three structures are listed in Table 2-7. As measuring IM3, the output impedance is tuned at maximum gain. The IIP3 and OIP3 are different in three structures due to different load impedance (as shown in Fig. 2.13).

2.3 Summary

LDMOS with different structures for RF applications are investigated. The ring structure has a better performance than the fishbone structure, without altering the process flow. The quasi-saturation effect is suppressed in the LDMOS with the ring structure due to lower drain parasitic resistance. In addition, the f_T and f_{max} are also enhanced for the ring structure due to the lower drain parasitic resistance. The distance of each cell for ring structure can be reduced to improve RF performance because the self-heating effect for ring device is smaller than one for fishbone device. The circle device can improve the disadvantage of square device on DC performance due to uniform current density that reduces the drain resistance. Although the square structure shows higher value of output power, power gain and PAE, the operating range and linearity are worse than circle. Our results suggested that, using a circle structure, both better DC and RF characteristics can be achieved.

Table 2-1 Extracted R_{on} and V_{BD} for four different layout structures.

	R_{on} (Ω-㎜)	V_{BD} (V)
Fishbone	22.95	41
Square	24.59	42
Octagon	23.57	43
Circle	23.05	41

Table 2-2 Extracted g_m, R_d C_{gd} and C_{gs} to see their effects on f_T for different layout structures.

	g_m (mA/V)	R_d (Ω)	C_{gd} (fF)	C_{gs} (fF)	f_T (GHz)
Fishbone	36.9	9.05	147.2	1080	4.67
Square	34.58	2.6	185.4	986	4.71
Octagon	35.92	2.48	193.4	998.2	4.81
Circle	36.7	2.2	194.6	1013	4.87

Table 2-3 Individual effects of the model parameters on f_T. The square device is as a reference.

		g_m	R_d	C_{gd}	C_{gs}
Fishbone	f_T Difference (%)	6.5	-3.9	3.7	-7.2
Octagon		3.7	0.1	-0.7	-1.1
Circle		5.9	0.2	-0.9	-2.2

Table 2-4 Extracted R_g, R_d, C_{gd}, C_{gs}, C_{ds} and C_{jdb} to see their effects on f_{max} for different layout structures.

	R_g (Ω)	R_d (Ω)	C_{gd} (fF)	C_{gs} (fF)	C_{ds} (fF)	C_{jdb} (fF)	f_{max} (GHz)
Fishbone	1.91	9.05	147.2	1080	53.97	39.87	13.09
Square	2.43	2.6	185.4	986	97.62	52.13	14.74
Octagon	2.48	2.48	193.4	998.2	119.9	129.9	13.16
Circle	2.71	2.2	194.6	1013	119.8	132.3	14.22

Table 2-5 Individual effects of the model parameters on f_{max}. The square device is as a reference.

		g_m	R_g	R_d	C_{gd}	C_{gs}	C_{ds}	C_{jdb}
Fishbone	f_{max} Difference (%)	5.9	5.7	-23.8	8.6	-6.9	6.8	2.5
Octagon		3.4	-0.7	0.8	-1.8	-1	-2.9	-7.6
Circle		5.4	-2.9	3	-2	-2.1	-2.9	-7.8

Table 2-6 C_{jdb} and DNW area for four different layout structures.

	C_{jdb} (fF)	DNW area (um^2)
Fishbone	39.87	8617.1
Square	52.13	8867.4
Octagon	129.9	10145.4
Circle	132.3	10570.3

Table 2-7 IIP3 and OIP3 for four different layout structures.

	IIP3 (dBm)	OIP3 (dBm)
Fishbone	15.04	31.03
Square	12.92	30.58
Circle	15.52	32.38

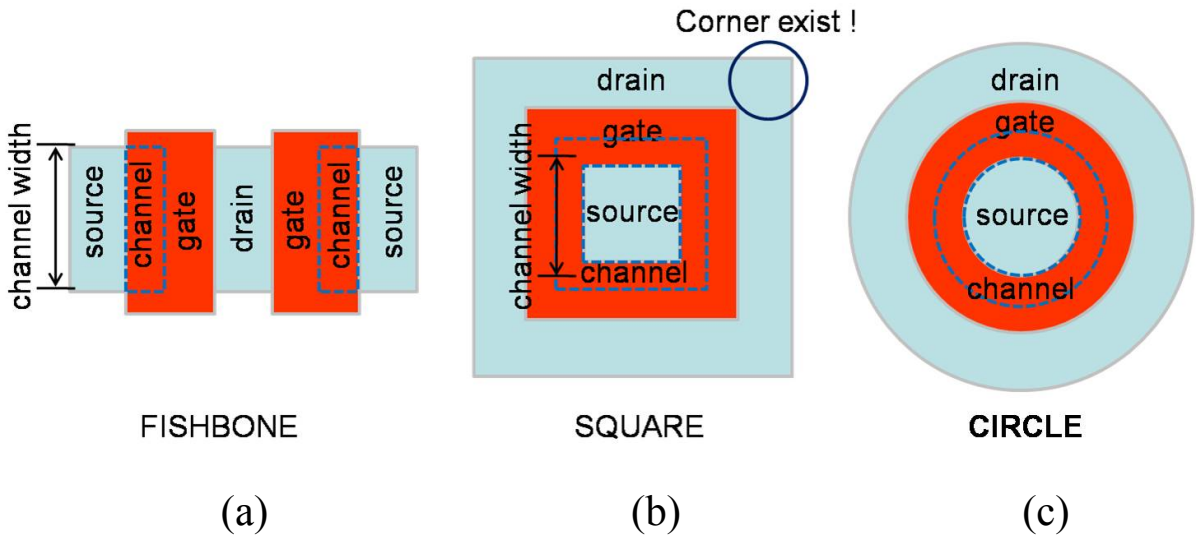


Fig. 2.1 LDMOS layout structures: (a) fishbone, (b) square and (c) circle.

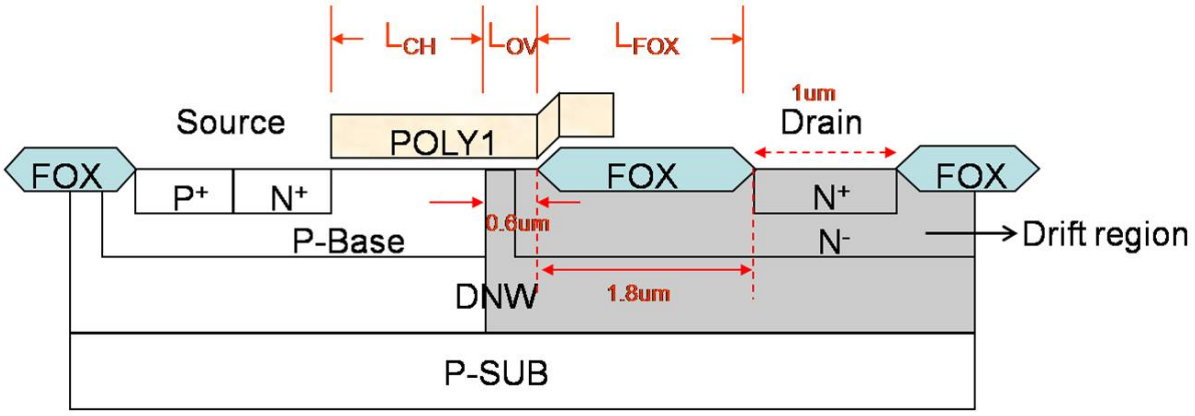
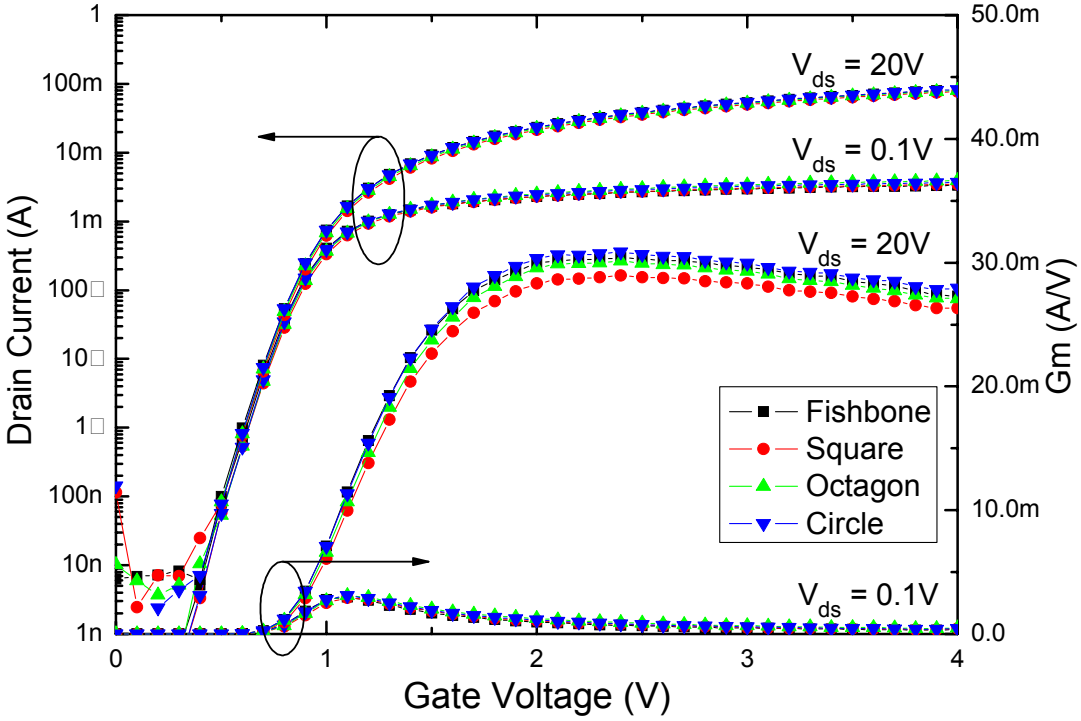
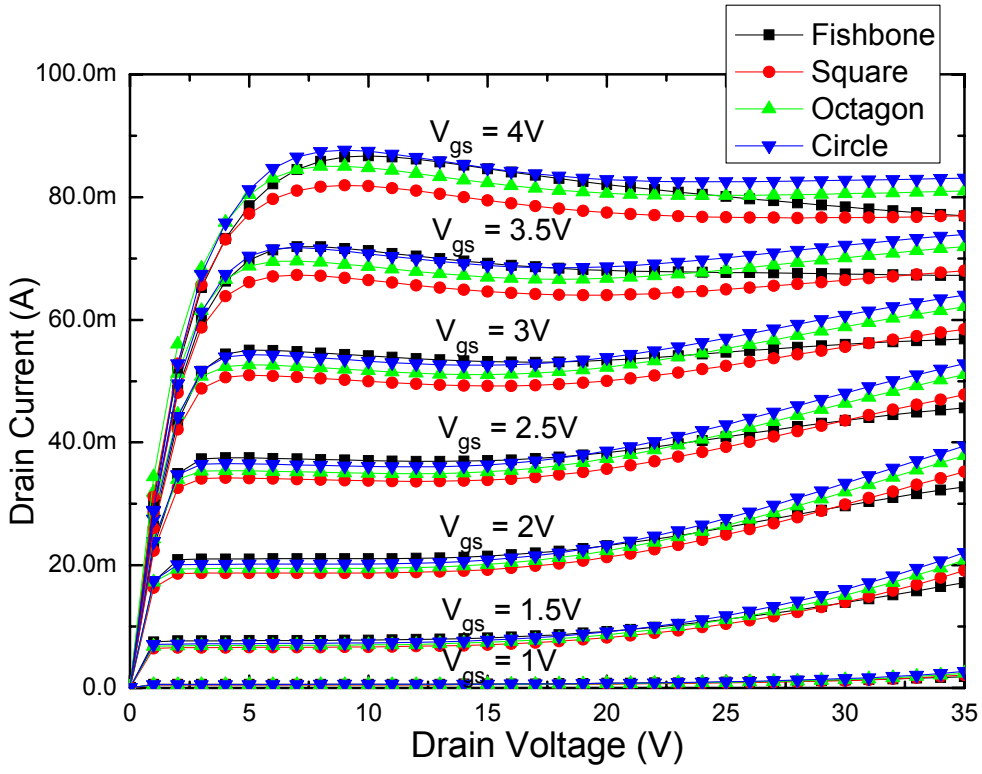


Fig. 2.2 Schematic cross section of an LDMOS transistor.



(a)



(b)

Fig. 2.3 (a) Subthreshold and (b) output characteristics of LDMOS transistors with different layout designs.

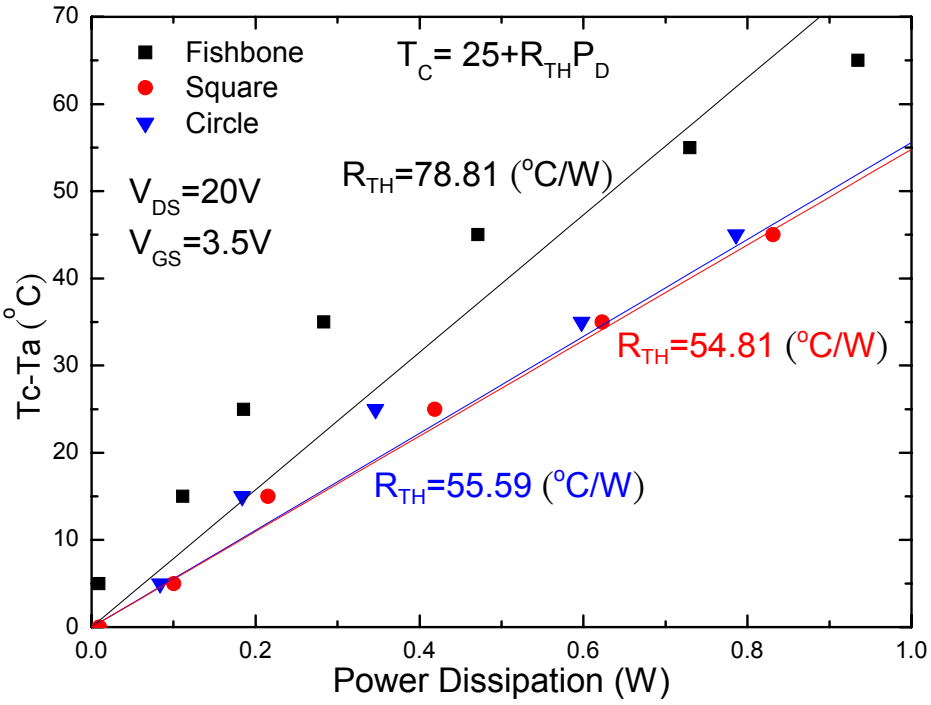
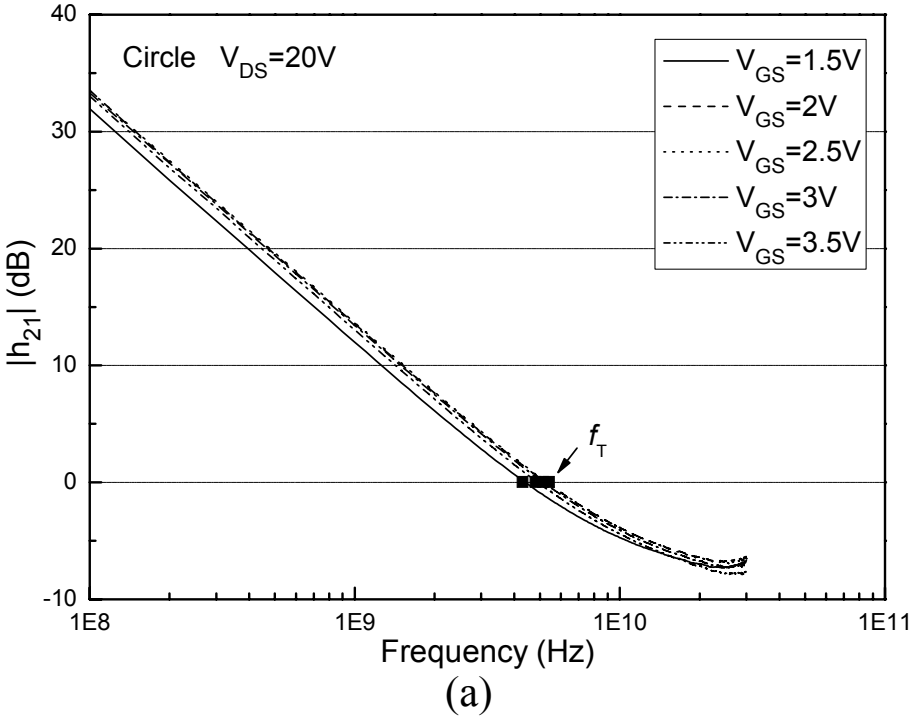
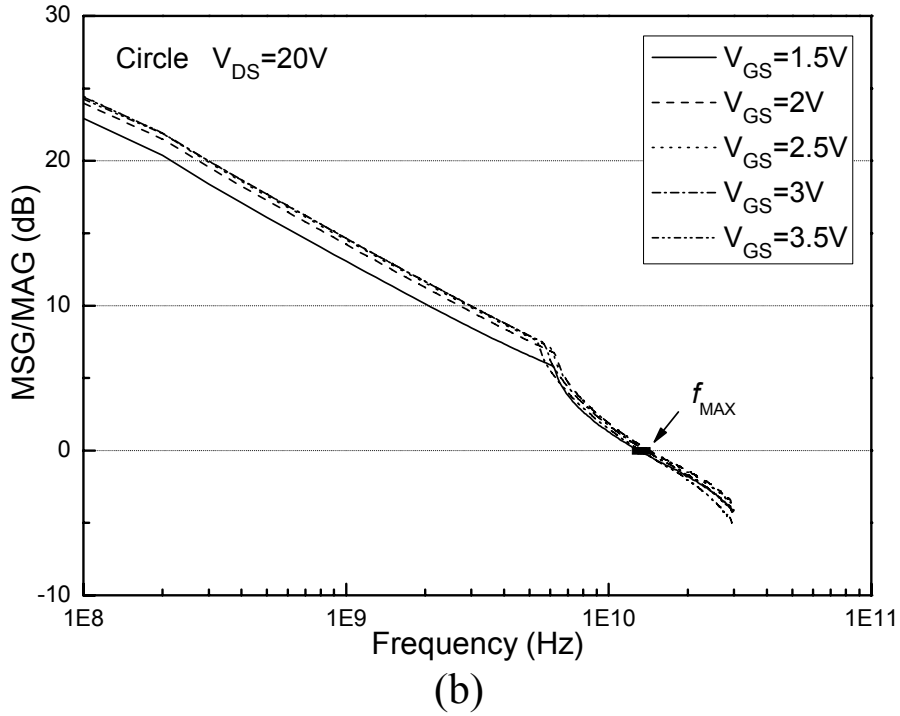


Fig. 2.4 R_{TH} of LDMOS transistors with different layout design.

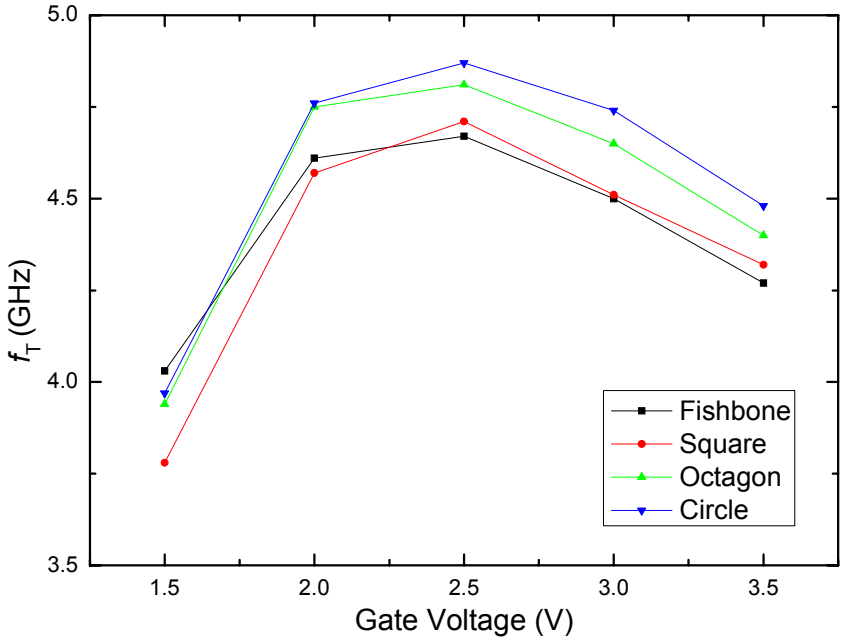


(a)

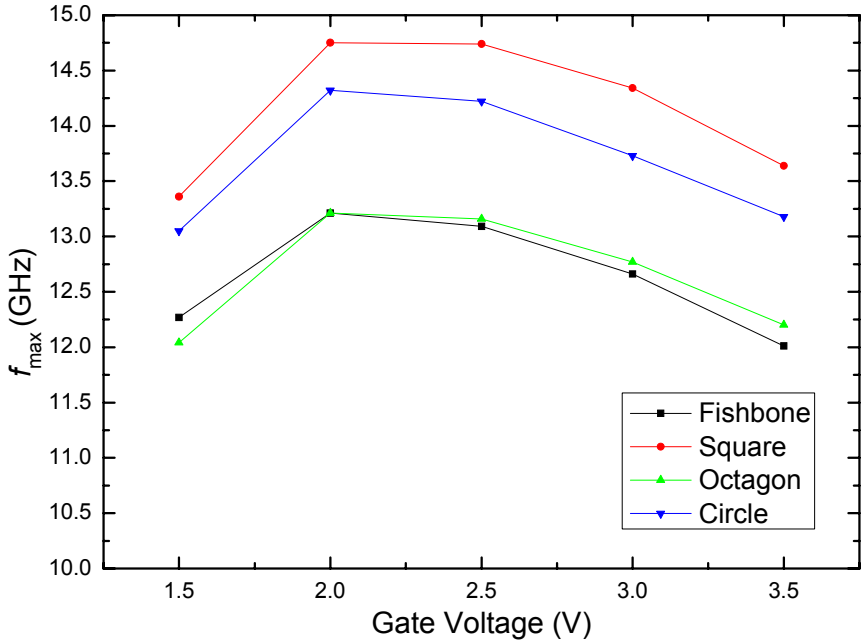


(b)

Fig. 2.5 Dependence of (a) |h21| and (b) MSG/MAG on frequency obtained from S-parameter measurements.



(a)



(b)

Fig. 2.6 (a) f_T and (b) f_{max} versus gate voltage with different layout design.

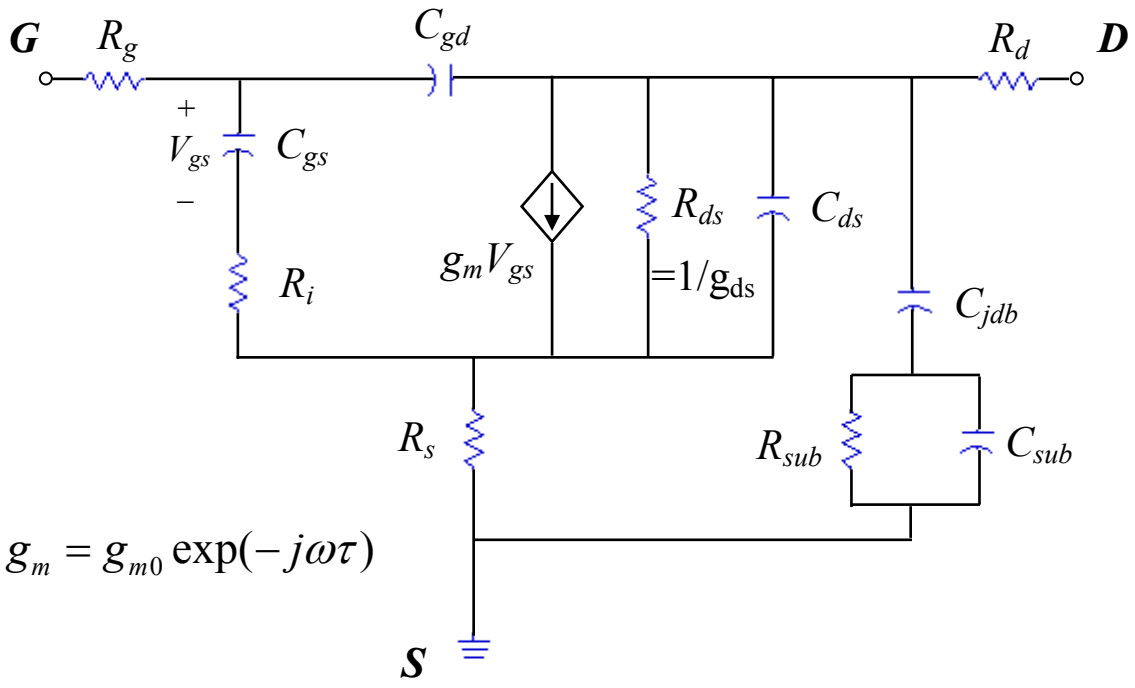
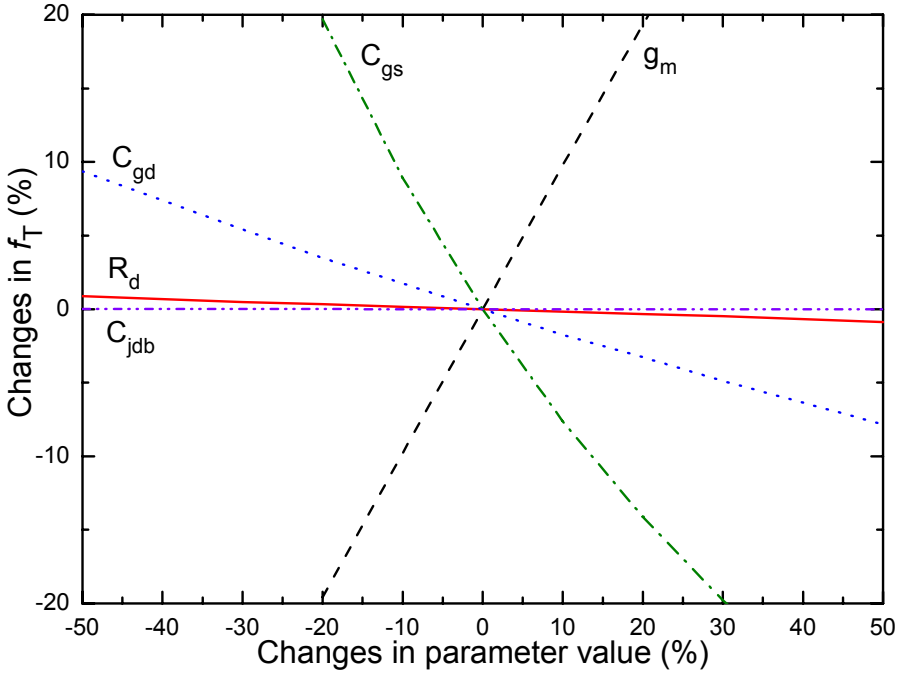
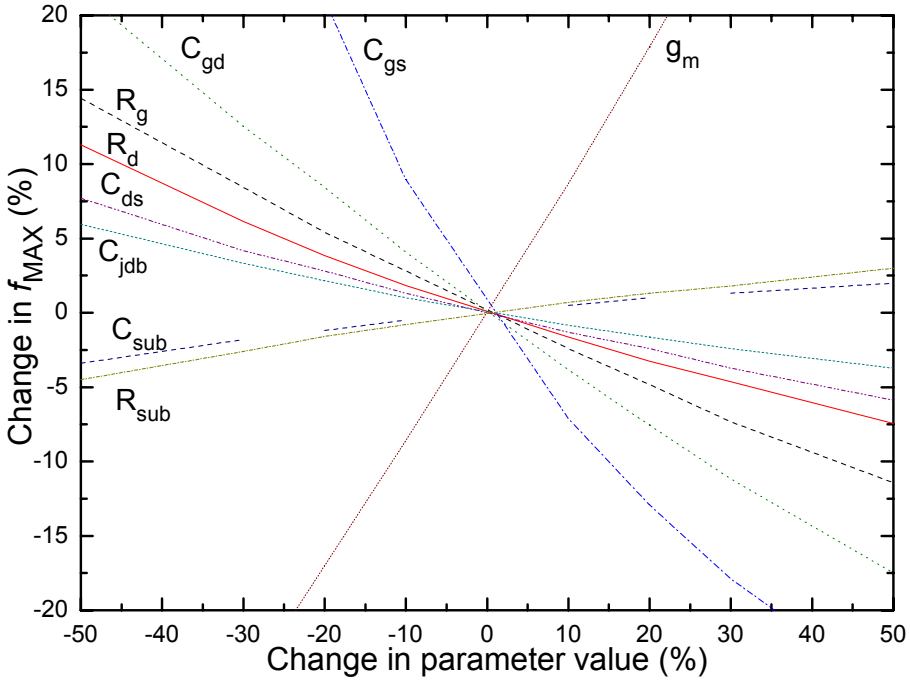


Fig. 2.7 A simple equivalent circuit model of the LDMOS.



(a)



(b)

Fig. 2.8 Effects of small-signal model parameters on (a) f_T and (b) f_{max}.

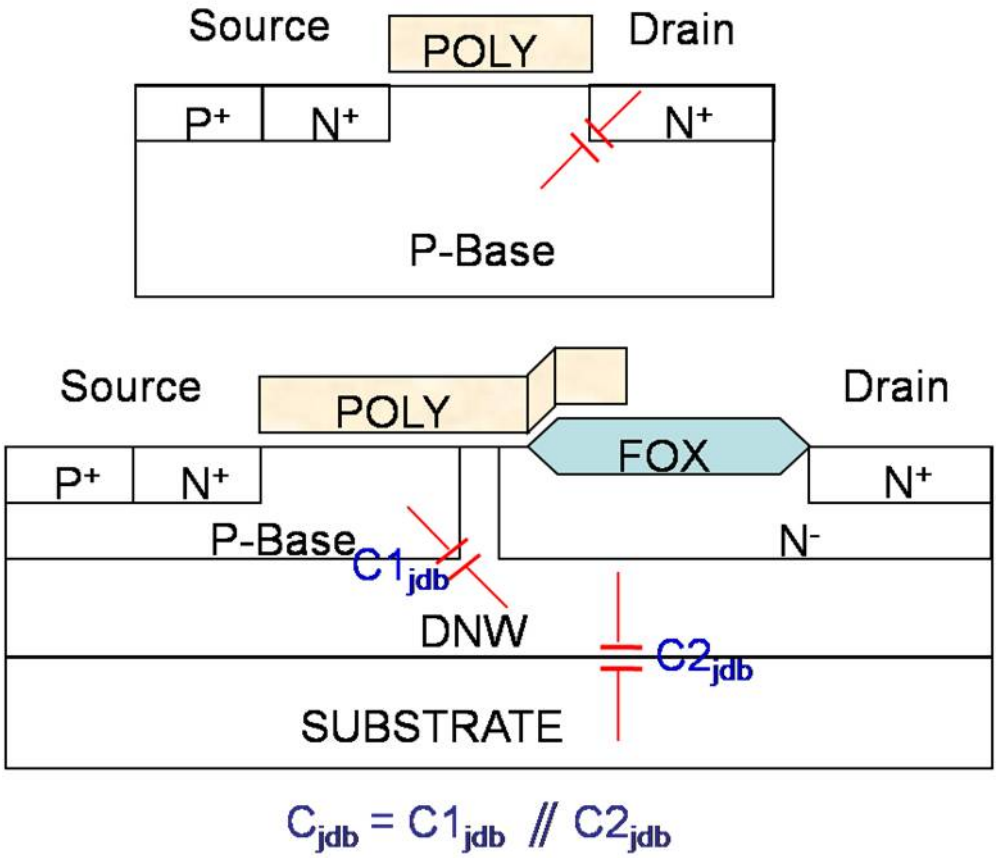


Fig. 2.9 The drain to body junction capacitance

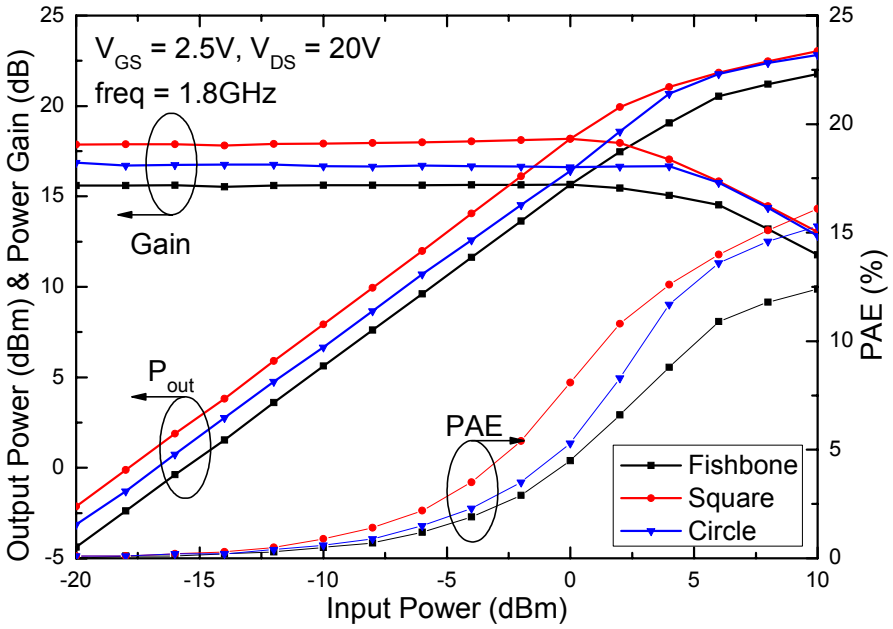


Fig. 2.10 Output power, power gain and PAE versus input power with different layout designs.

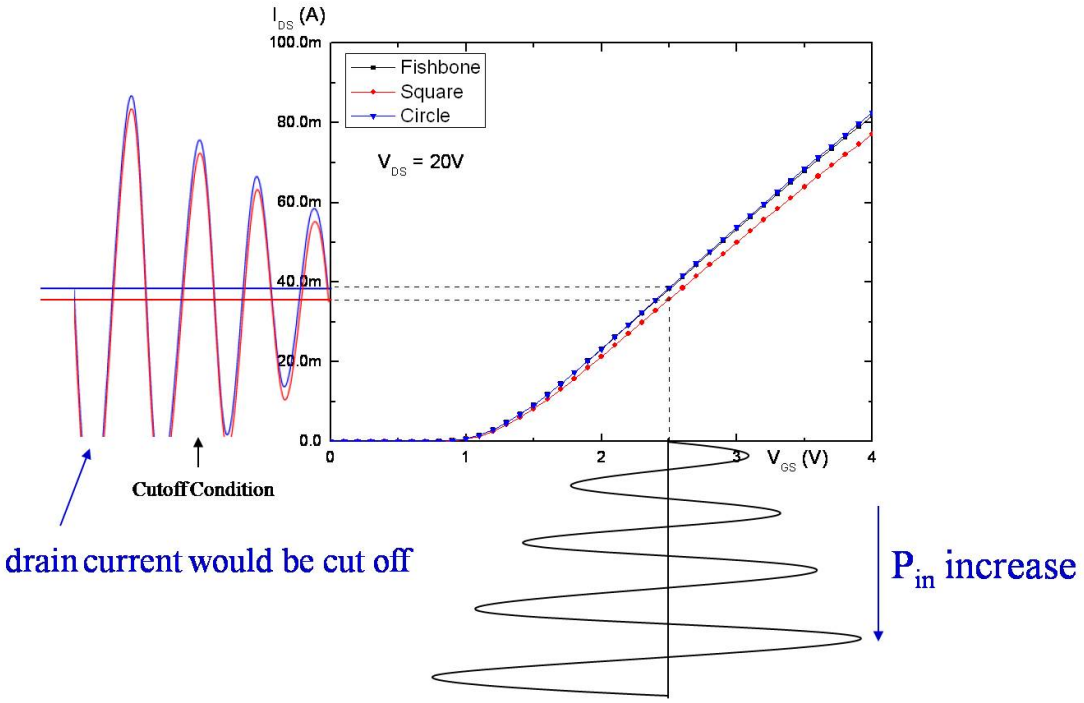


Fig. 2.11 Drain current versus gate voltage with different layout designs. The input signal was biased at V_{GS}=2.5V and the negative duty cycle of output signal was clipped by the cutoff region.

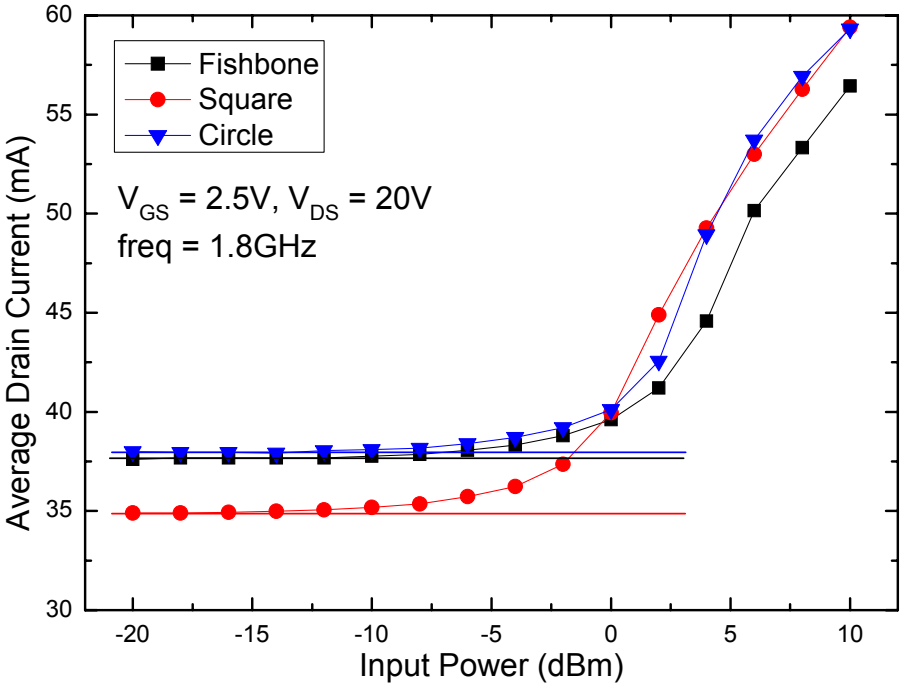


Fig. 2.12 Average drain current as a function of the input power with different layout designs.

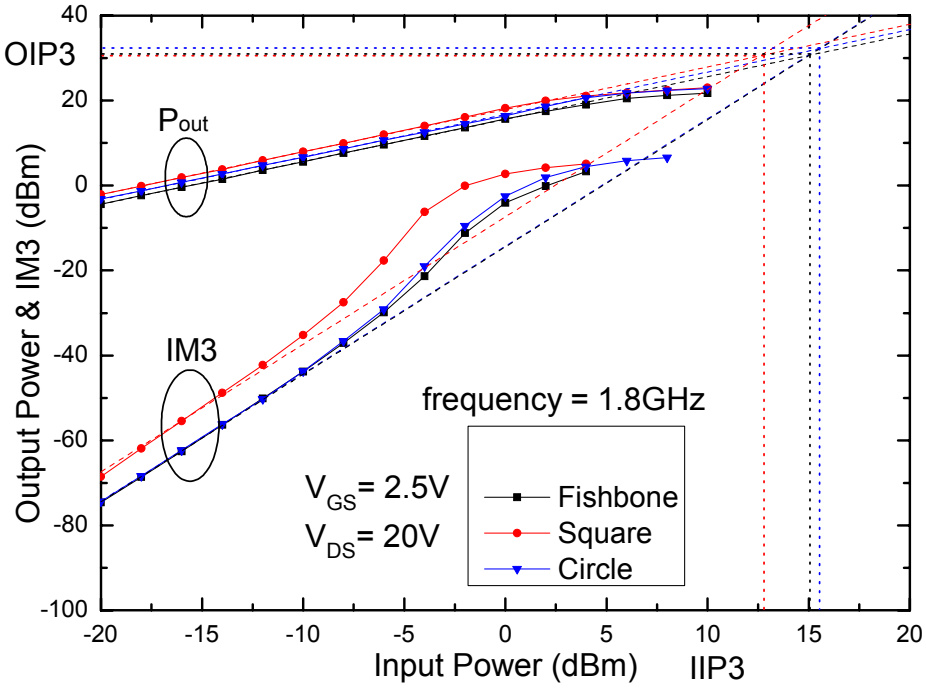


Fig. 2.13 Output power and third-order intermodulation power versus input power with different layout designs.

Chapter 3

Characterization of RF LDMOS with Different Channel Widths

3.1 Introduction

The corner effect of square structure is described in chapter 2. Under fixing the drift length, we studied the corner effect by changing the channel width of a cell. Different ratios of corner areas to edge area would result in different drain parasitic resistances and capacitances [19]. Square structures with different channel widths for DC, high-frequency, and RF power characteristics are investigated.

3.2 RF LDMOS with Square Structure

The square device used in this study had different channel widths per a cell (W_{ch}=20 μm, 40 μm and 100 μm). For making a fair comparison, these devices had the same total channel width (W=400 μm). Therefore, the cells in the these devices were arranged as 10x2, 5x2 and 2x2 arrays, respectively. These devices are named as "square_20x20", "square_10x40" and "square_4x100", respectively.

3.2.1 DC Characteristics

Fig. 3.1 shows the *I–V* characteristics of the LDMOS with different channel widths. The device with larger W_{ch} shows a lower drain current and transconductance. Also with a larger W_{ch}, the higher resistance in the drift region leads to the quasi-saturation effect occurs earlier. The extracted on-resistance and breakdown voltage with various channel widths per a cell are shown in Table 3-1. The R_{on} is extracted from the linear forward *I-V* characteristics at gate voltage V_{GS}=2.5 V and normalized to the total width. As indicated in Table 3-1, the devices with different channel widths have similar breakdown voltage. In addition, we find that, as the

channel width increases, the R_{on} increases due to the increase of drain series resistance. By fixing the drift length, the ratio of corner area to side area will be reduced with increasing W_{ch}. Therefore, the device with large W_{ch} has smaller equivalent drift width compared to the device with small W_{ch}, leading to higher drain resistance.

From the output *I–V* characteristics, we observe a negative output resistance in the high-current region. With high current density in the transistor, the rise in device temperature resulted from the dissipated power becomes significant. Fig. 3.2 shows the thermal resistance (R_{th}) with different channel width per a cell. The device with large W_{ch} has higher thermal resistance than that with small W_{ch} due to compact layout area and has significant self-heating effect. The device self-heating can be improved by increasing the distance between each cell.

3.2.2 High-frequency Characteristics

The dependences of the cutoff frequency and maximum oscillation frequency on the channel width for the LDMOS are compared in Fig. 3.3. The transistors are biased at V_{GS}=2.5 V and V_{DS}=20 V to obtain the maximum value of f_T. It is obvious that f_T and f_{max} both decrease with decreasing W_{ch} due to lower parasitic capacitance. On the other word, the both values of f_T and f_{max} in these layout devices are square_4x100 > square_10x40 > square_20x20.

By analyzing a MOSFET small-signal equivalent circuit, we can determine the effect of device parameters on high-frequency characteristics more clearly. Using extracted parameters from the existing device and altering one parameter at the time, the effect of model parameters on the cutoff frequency and maximum oscillation frequency can be visualized. The influences of model parameters on f_T and f_{max} are shown in Fig. 3.4. The x-axis showed the parameter value departure from the initial value in percent. The y-axis showed the change in frequency in percent. Parameters not shown in the figure had approximately the same value for the square structures or had a minor influence on f_T and f_{max}. As shown in Fig. 3.4(a), the

intrinsic transconductance (g_m), gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) have large effect on f_T. The cutoff frequency can be expressed in a simple way of $f_T = g_m/ 2\pi (C_{gs}+ C_{gd})$ which is related to the g_m and input intrinsic capacitances ($C_{in}= C_{gs}+ C_{gd}$). The extracted model parameters that affect the f_T more significantly are listed in Table 3-2. According to above equation, we know that the f_T is proportional to g_m, but the measured data we obtained is reverse proportional to g_m. So we confirm that the f_T is relative to C_{in} and C_{in} increases with increasing the extra area of drift region. In addition, the f_{max} has the similar appearance. Comparing to square_10x40, as C_{gd} is changed from 185.4 fF to 275.7fF and 130.4 fF for square_20x20 and square_4x100, f_T vary about -7.6% and 5.4% respectively (see Table 3-3). Similarly, C_{gs} is also changed from 986 fF to 971 fF and 994 fF for square_20x20 and square_4x100 and makes f_T about 1.3% and -0.7% changes respectively. Therefore, it is obvious that the C_{gd} has a great effect on f_T for these devices. The increasing area of drift region led to C_{gd} rise, and decreasing area of source led to C_{gs} reduce for square device. As illustrated in Fig. 3.4(b), in addition to the intrinsic parameters, the R_d, gate resistance (R_g), drain-source capacitance (C_{ds}) and drain-substrate junction capacitance (C_{jdb}) have apparent effects on f_{max}. The extracted model parameters that affect f_{max} more significantly are listed in Table 3-4. The transistor has larger value of f_{max} with increasing channel width due to smaller C_{ds} and C_{gd}. The former is relative to the overlapped area of metal conducting wires and the later is relative to the drift region area. In addition, one reason results the lowest f_{max} for square_20x20 is larger C_{jdb}. The value of C_{jdb} is relative to the DNW area and device area. Comparing to square_10x40, C_{gd} varies from 185.4 fF to 275.7 fF and 130.4 fF for the square_20x20 and square_4x100, and make f_{max} about -17.1% and 12.4% changes respectively (see Table 3-5). Another parameter affects f_{max} more is C_{ds}. As C_{ds} is changed from 97.62 fF to 149.9 fF and 58.32 fF for the square_20x20 and square_4x100, the f_{max} vary about -6.3% and 6.1% respectively. In addition, the square_20x20 and square_4x100 both have smaller R_g and cause f_{max} about 8.4% and 7% changes due to different cell arrangement.

The R_d also has a little effect and makes f_{max} about 4.7% and -5.9% changes for the square_20x20 and square_4x100. Otherwise, the larger C_{jdb} just in square_20x20 decreases f_{max} about -8.6% contrasting with square_10x40. Consequently, Comparing to square_10x40, using the square_20x20, we estimate that f_{max} become worse by about -16.1% (f_{max} was 12.37 GHz for the square_20x20 and 14.74 GHz for the square_10x40) and using the square_4x100, we estimated that f_{max} become better by about 6.4% (f_{max} was 15.68 GHz for the square_4x100 and 14.74 GHz for the square_10x40). Therefore, C_{gd} is the key factor for improving f_T and f_{max} by using the square structure.

3.2.3 RF Power and Linearity

The load-pull measurement uses the same setup as chapter 2. Figure 3.5 shows the output power, power gain and power added efficiency (PAE) for square device with different channel widths. The power gain characteristic is related to f_{max}. The transistor with llarge W_{ch} has larger power gain and out power but they degrade earlier when input power was larger than 1-dB compression point (P_{1db}) (see Fig. 3.5). The main reason for gain compression is attributed to the clipping effect that is explained in chapter 2. As the channel width increase, the lower drain current makes the negative duty cycle of output waveform enter the cutoff region earlier (see Fig. 3.6). This indicates that the average drain current started to increase earlier (see Fig. 3.7) and the gain compression occurs prior. The transistor with large channel width has wider operating range that is before P_{1dB} point. Consequently, although the square device with large channel width shows higher value of output power, power gain and PAE, the operating range is narrow slightly. Since the DC behaviors were changed, the linearity would also be affected with various channel widths. The input and output third-order intercept points (IIP3 and OIP3) for three channel widths are listed in Table 3-6. The IIP3 and OIP3 are similar for different channel widths (as shown in Fig. 3.8).

3.3 Summary

The square devices with various channel widths for RF applications are investigated. The transistor with large W_{ch} has better f_T, f_{max}, and RF power due to lower drain parasitic capacitance, but it also has larger on-resistance and narrower operating range due to larger drain parasitic resistance. It shows a trade-off between the DC performance and the RF performance. In addition, the area of square device with large W_{ch} is smaller than one with small W_{ch}, leading to more serious self-heating effect. It also shows a trade-off between the area of device and the self-heating effect.

Table 3-1 Extracted R_{on} and V_{BD} for square device with different channel widths.

	R_{on} (Ω-㎜)	V_{BD} (V)
Square_20x20	23.75	41
Square_10x40	24.59	42
Square_4x100	25.14	42

Table 3-2 Extracted g_m, R_d C_{gd} and C_{gs} to see their effects on f_T for square device with different channel widths.

	g_m (mA/V)	R_d (Ω)	C_{gd} (fF)	C_{gs} (fF)	f_T (GHz)
Square_20x20	34.97	1.97	275.7	971	4.47
Square_10x40	34.58	2.6	185.4	986	4.71
Square_4x100	34.1	3.58	130.4	994	4.86

Table 3-3 Individual effects of the model parameters on f_T. The square_10x40 is as a reference.

		g_m	R_d	C_{gd}	C_{gs}
Square_20x20	f_T Difference (%)	1.1	0.4	-7.6	1.3
Square_4x100		-1.3	-0.7	5.4	-0.7

Table 3-4 Extracted R_g, R_d, C_{gd}, C_{gs}, C_{ds} and C_{jdb} to see their effects on f_{max} for square device with different channel widths.

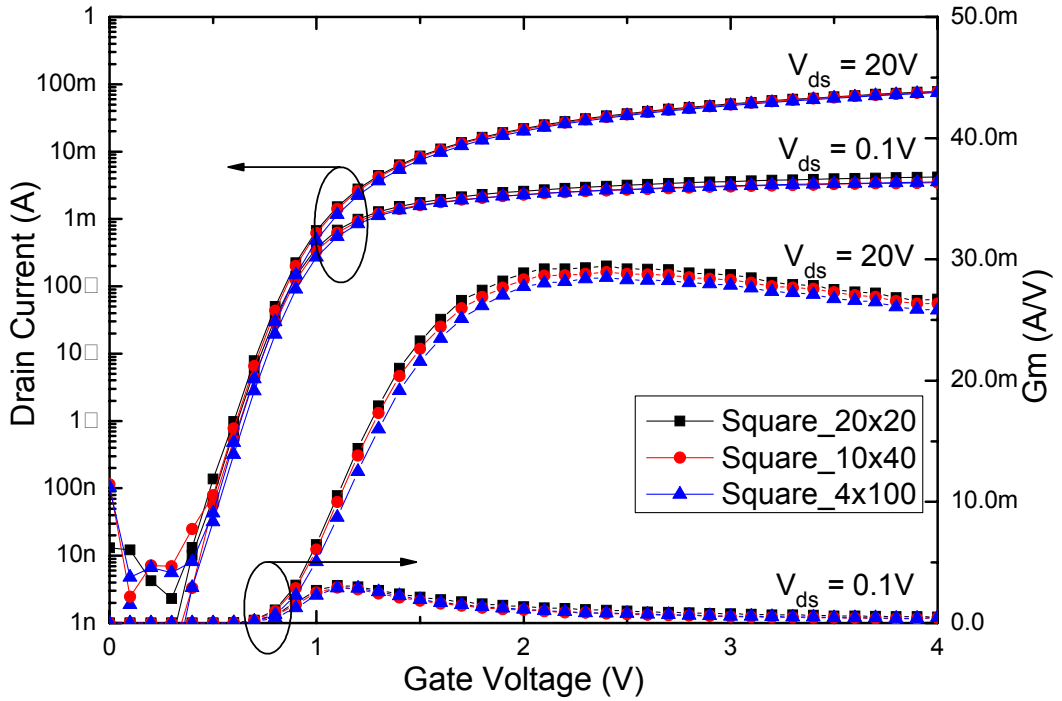
	R_g (Ω)	R_d (Ω)	C_{gd} (fF)	C_{gs} (fF)	C_{ds} (fF)	C_{jdb} (fF)	f_{max} (GHz)
Square_20x20	1.69	1.97	275.7	971	149.9	149.3	12.37
Square_10x40	2.43	2.6	185.4	986	97.62	52.13	14.74
Square_4x100	1.8	3.58	130.4	994	58.32	42.86	15.68

Table 3-5 Individual effects of the model parameters on f_{max}. The square_10x40 is as a reference.

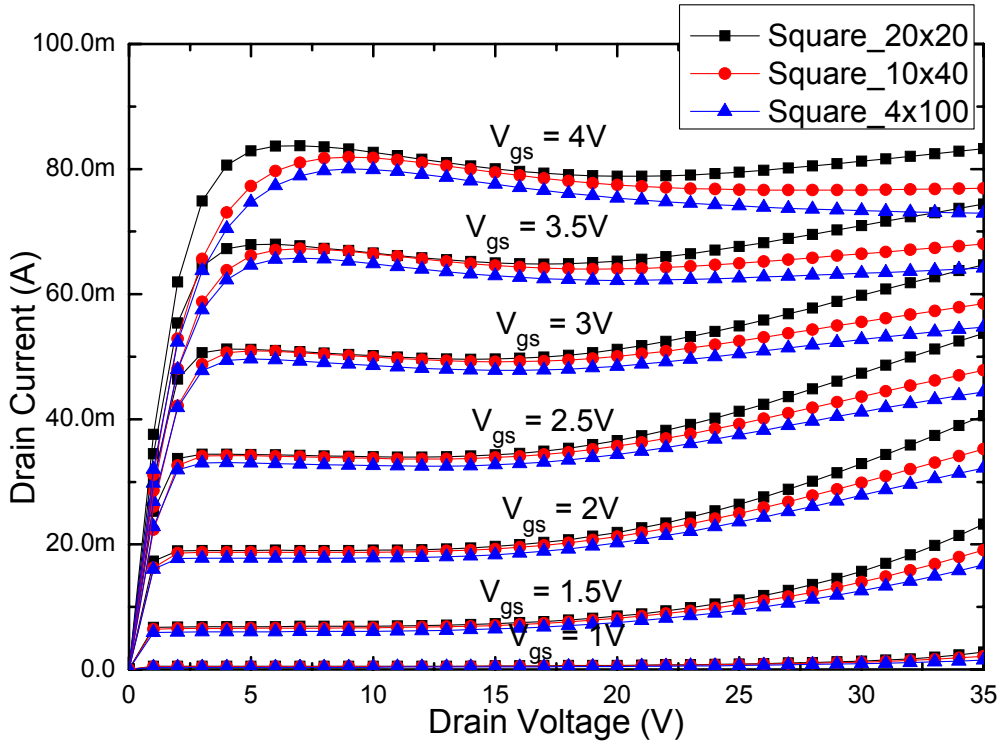
		g_m	R_g	R_d	C_{gd}	C_{gs}	C_{ds}	C_{jdb}
Square_20x20	f_{max} Difference (%)	0.9	8.4	4.7	-17.1	1.2	-6.3	-8.6
Square_4x100		-1.2	7	-5.9	12.4	-0.7	6.1	1.8

Table 3-6 IIP3 and OIP3 for square device with different channel widths.

	IIP3 (dBm)	OIP3 (dBm)
Square_10x40	15.78	30.24
Square_20x20	16.43	33.14
Square_4x100	24.18	41.35



(a)



(b)

Fig. 3.1 (a) Subthreshold and (b) output characteristics of LDMOS transistors with different channel widths.

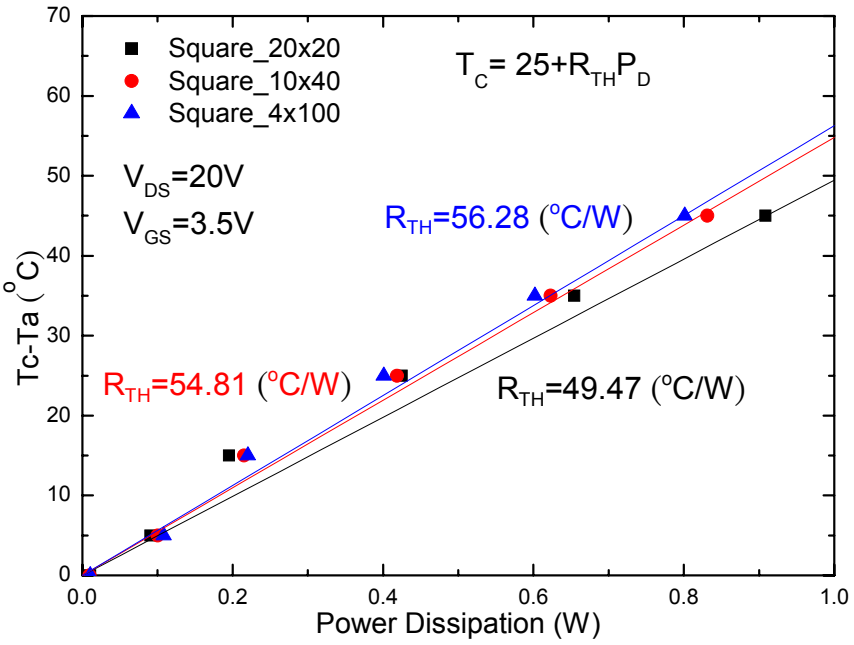
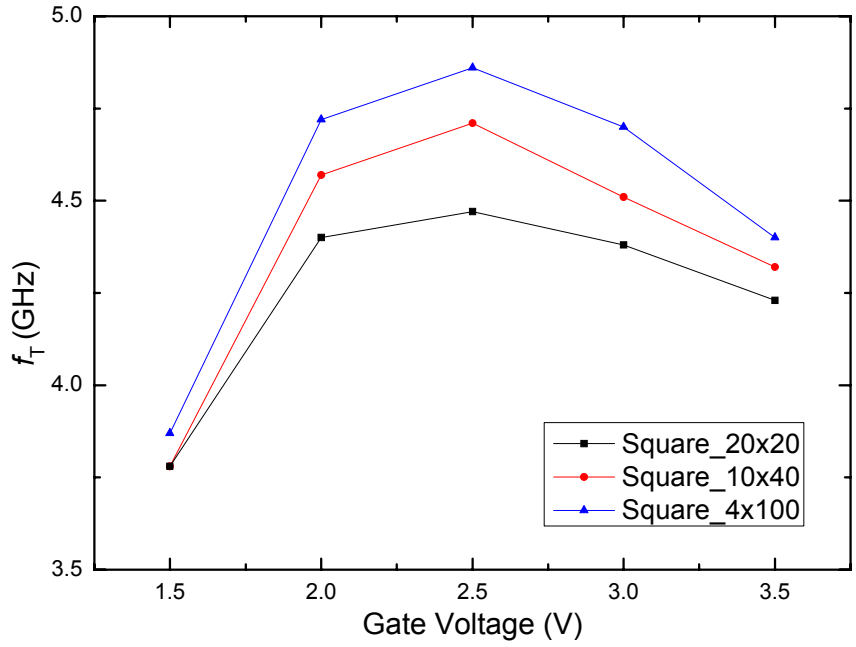
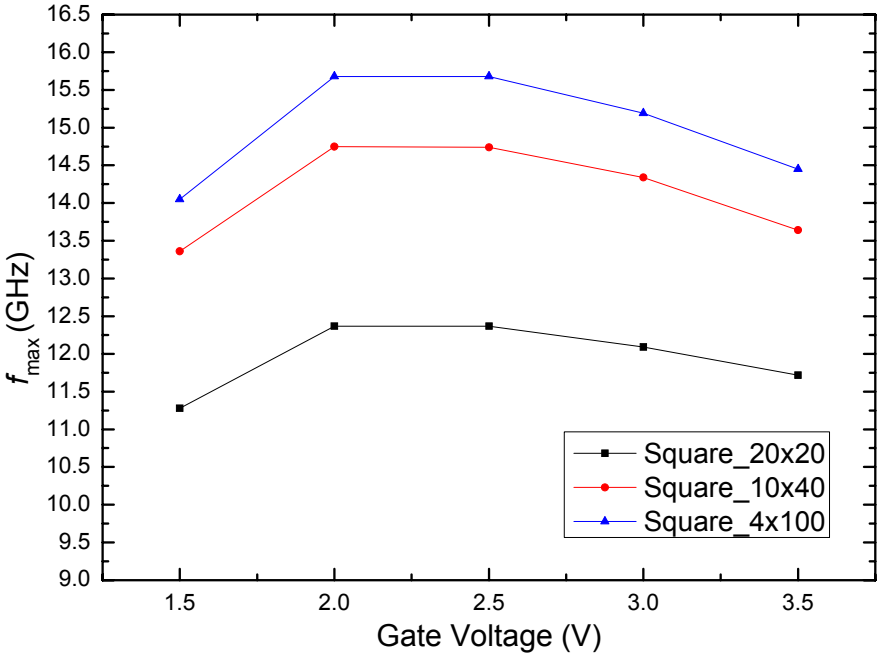


Fig. 3.2 R_{TH} of LDMOS transistors for square structure with different channel widths.

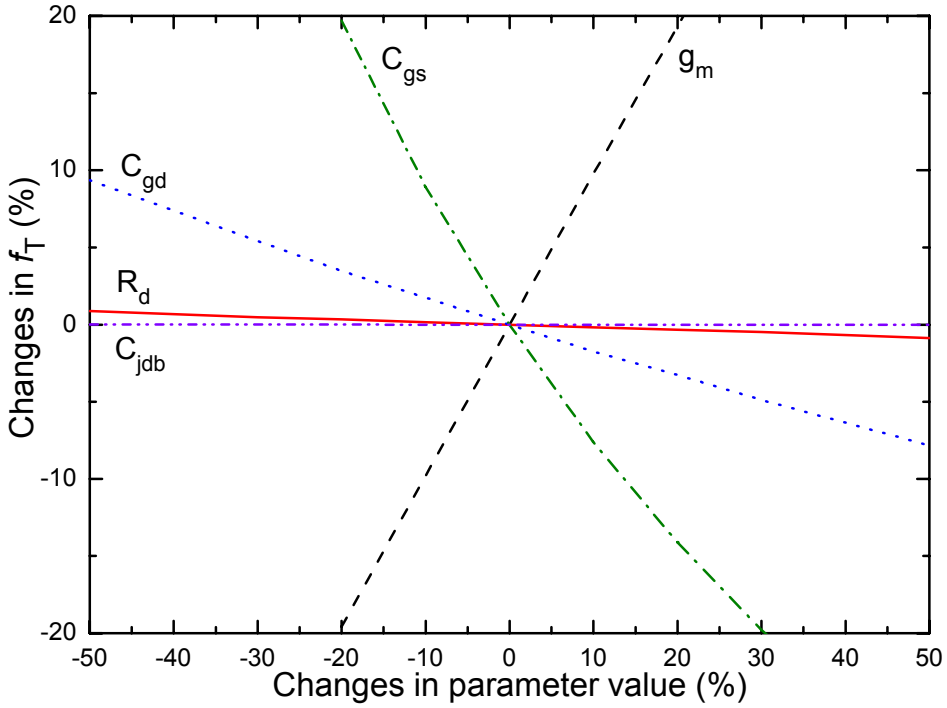


(a)

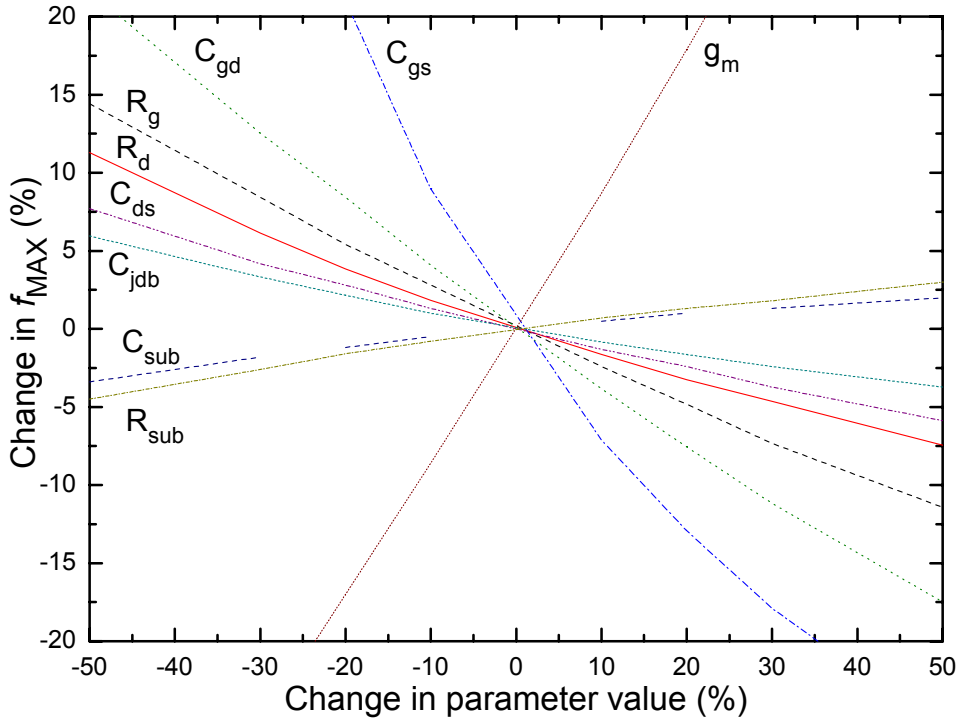


(b)

Fig. 3.3 (a) f_T and (b) f_{max} versus gate voltage for square structure with different channel widths.



(a)



(b)

Fig. 3.4 Effects of small-signal model parameters on (a) f_T and (b) f_{max}.

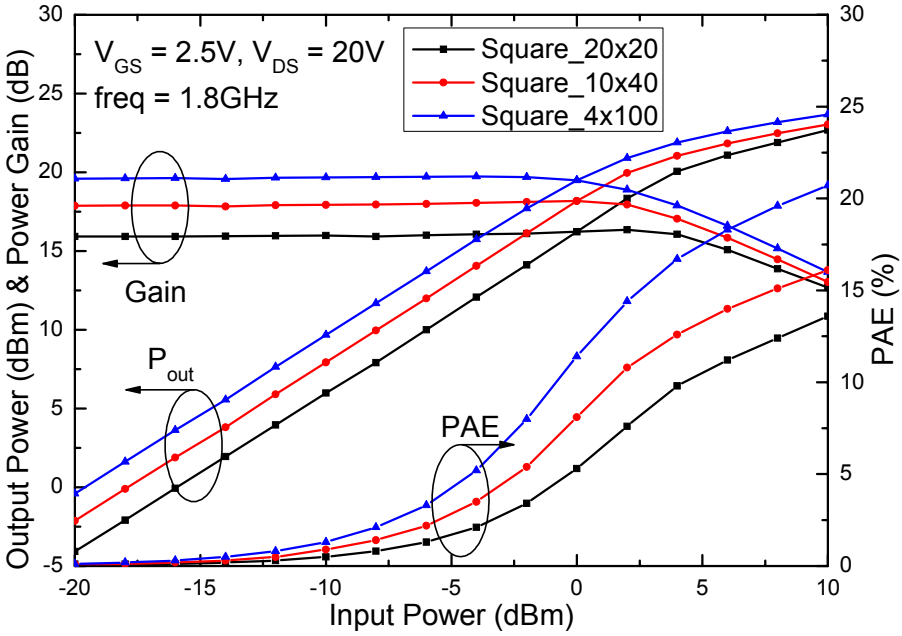


Fig. 3.5 Output power, power gain and PAE versus input power with different channel widths.

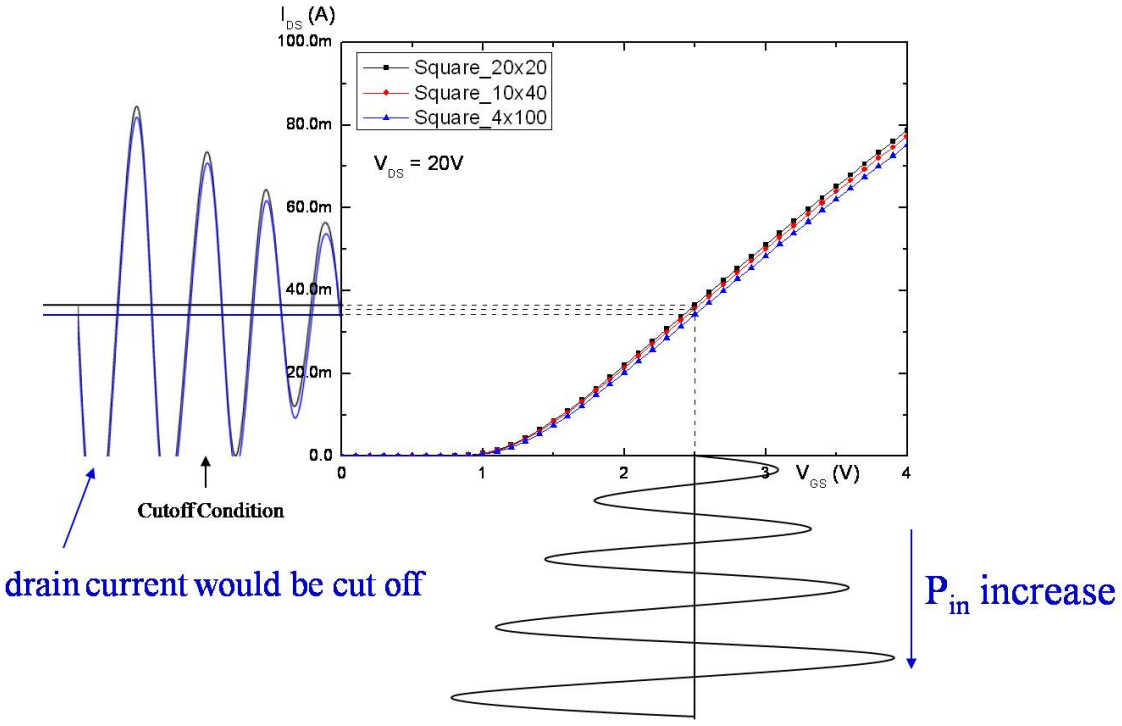


Fig. 3.6 Drain current versus gate voltage with different channel widths. The input signal was biased at V_{GS}=2.5V and the negative duty cycle of output signal was clipped by the cutoff region.

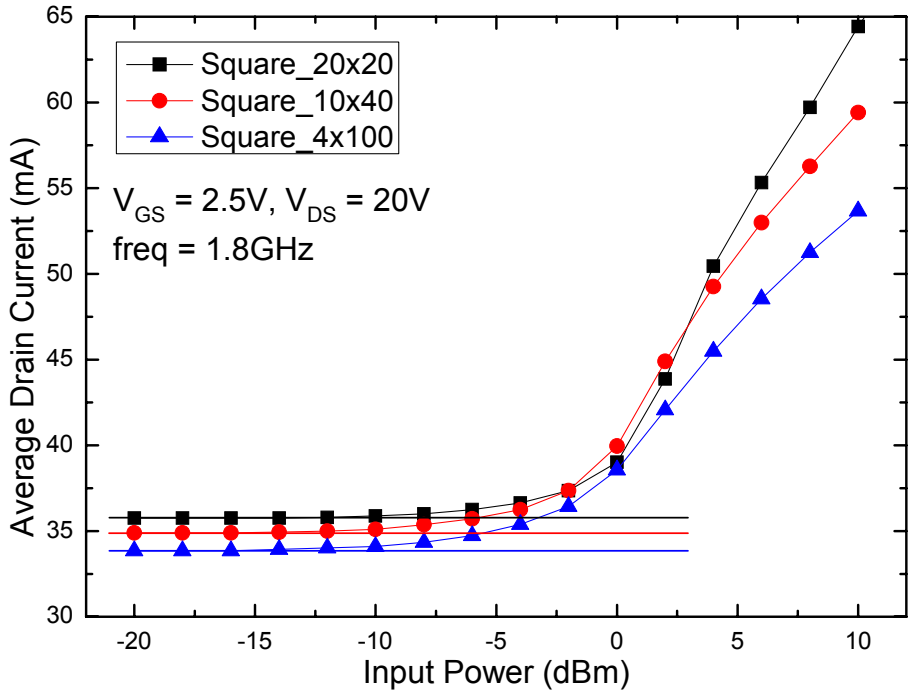


Fig. 3.7 Average drain current as a function of the input power with different channel widths.

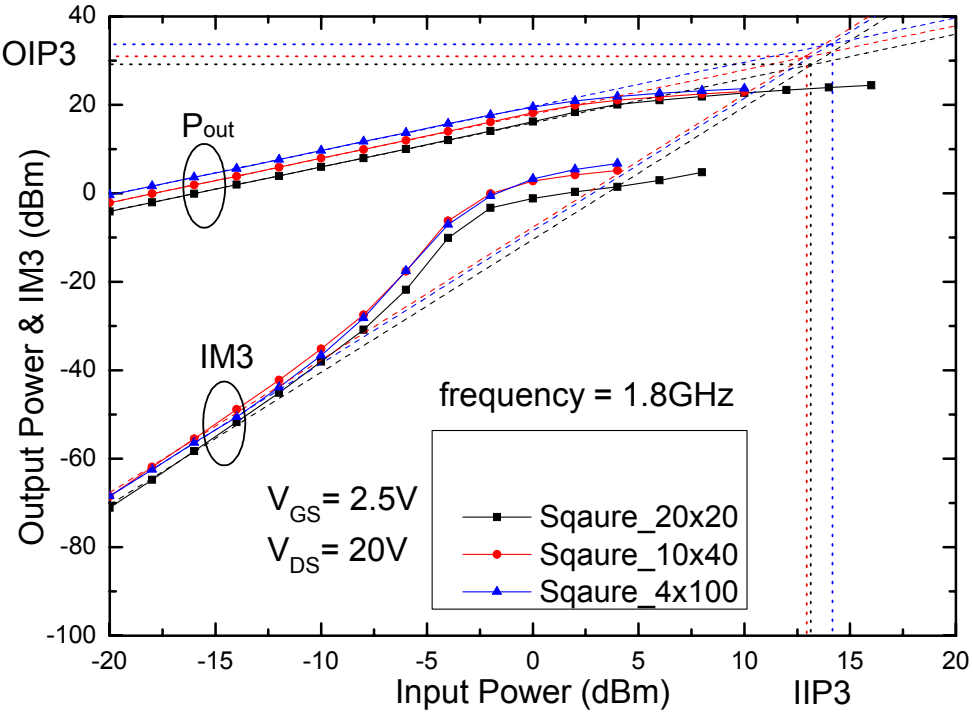


Fig. 3.8 Output power and third-order intermodulation power versus input power with different channel widths.

Chapter 4

Capacitance Characteristics of RF LDMOS with Different Layout Designs

4.1 Introduction

Because the device capacitances influence the input, output and feedback capacitances, which are important in the dynamic operation, and have large impact on device high-frequency performance, the capacitance characterization and modeling of LDMOS transistors have been studied widely [28]-[31]. As compared to the conventional MOSFET, a non-uniform doping channel and a drift region in LDMOS result in the unusual behavior in capacitances [32]-[33]. And the characteristics of ring structure are different from traditional RF LDMOS (fishbone). Therefore we are interested to know the effect of layout design on the capacitance characteristics of LDMOS transistors.

4.2 Capacitances versus V_{GS} for Fishbone LDMOS

The capacitances we analyzed in this chapter were extracted form the S-parameters. Using an HP8510 network analyzer, S-parameters were measured on-wafer from 0.1 to 5GHz for different temperatures and then de-embedded by subtracting the OPEN dummy. Different control biases were applied from an HP4142B source measure unit to sweep from accumulation to strong inversion. The gate-to-source/body capacitance (C_{GS}+ C_{GB}) and gate-to-drain capacitance (C_{GD}) and drain-to- gate capacitance (C_{DG}) has been extracted from the de-embedded S-parameters at low frequency range by the formula described in chapter 2. In order to improve the RF performance, the source and P-body have been tied together to the RF ground. Therefore, the extracted gate-to-source capacitance (C_{GS}) and gate-to-body

capacitance (C_{GB}) cannot be separated.

For fishbone structure, the extracted C_{GS}+ C_{GB} and C_{GD} as functions of gate voltage (V_{GS}) for drain voltage V_{DS}=0.1, 1, 5, 10 and 20V at room temperature are shown in Fig. 4.1. At low drain bias (V_{DS}=0.1 V), the C_{GS}+ C_{GB} presents a similar behavior to the conventional MOSFET. For the lateral non-uniformly doped channel in LDMOS, the doping concentration was lower at the drain side than the source side. Hence, the drain end will be inverted prior to the source end, resulting in a peak in C_{GD} [31]. As the drain end was inverted, the accumulation electron charge sheet in N-type drift region will cause C_{GD} to increase as gate voltage (V_{GS}) increases. Once the V_{GS} exceeds the threshold voltage (i.e. source end was inverted), the C_{GD} starts to fall as the electron charge sheet is no longer connected only to the drain.

By increasing the drain voltage (V_{DS}>1 V), both C_{GS}+C_{GB} and C_{GD} present peaks. Because the inversion charges may be injected from the intrinsic MOSFET to the depleted area of the drift, the C_{GD} and C_{GS}+C_{GB} increase with increasing gate voltages and the C_{GS}+C_{GB} even rises over the limit of inversion [29]. In LDMOS, existed drift region resulting in the effect of quasi-saturation. Before the device entered the quasi-saturation regime, the drain side channel voltage (V_{ch}) increased as the V_{GS} increased just like in the conventional MOSFET. Then, V_{ch} decreased as the V_{GS} increased after the device enters the quasi-saturation regime [34]. Therefore, the C_{GS}+C_{GB} could exceed the value of total gate oxide capacitance due to change in surface potential in the drift goes negative where the change in gate voltage was still positive [35]. In the quasi-saturation regime, the surface potential variation becomes small gradually leads to the fall of the C_{GS}+C_{GB} and C_{GD}. Accordingly, the C_{GS}+C_{GB} and C_{GD} reach maximum at the onset of quasi-saturation. In Fig. 4.1, the corresponding drain currents at drain voltages V_{DS}=1, 10 and 20 V were also presented. Because the higher drain voltage leads to a higher gate voltage at the onset of quasi-saturation, the peaks shift to higher gate voltages. In addition, the peak value increases

in C_{GS}+C_{GB} and decreases in C_{GD} as the V_{DS} increases as shown in Fig. 4.1. It attributed to the charge partitioning under the gate when varying the drain voltage.

4.3 Capacitances versus V_{GS} for Different Layout Structures

For the square structure, however, second peak in C_{GS}+C_{GB} and C_{GD} are observed when biasing at high drain voltage (V_{DS}=10 and 20 V) (see Fig. 4.2). But there are no additional peaks in C_{GS}+C_{GB} and C_{GD} for circle structure that has ring shape like square structure. The same phenomenon is shown in Fig. 4.3, the C_{DG} falls slowly at high drain voltages for square structure as gate voltage increases. From Fig. 4.3, the C_{DG} almost equals to each other for three structures before the device entered the quasi-saturation regime. When gate voltage exceeds threshold voltage, the C_{DG} starts to increase quickly due to the channel region is inverted to attract charges. As shown in Fig. 4.4, the currents flow from drain to source with uniform distribution in the full region of the fishbone and circle structures. However, in the square structure, the corner region of the drift shows lower current density than the edge region [36], [37], and thus it is needed higher gate voltage to enter quasi-saturation. At the first peak, although the edge of the square ring is operated in quasi-saturation region, the corner is still in pre-quasi-saturation. By keeping increasing the gate voltage, the current in the corner region is high enough to make the velocity of electrons in the drift saturated. Therefore, the corner region operates in quasi-saturation and second peaks are generated in the C_{GS}+C_{GB} and C_{GD}.

4.4 Summary

In this chapter, the capacitance characteristics of RF LDMOS transistors with different layout structures are studied. Since LDMOS transistor has a lateral non-uniform doping channel and a drift region, peaks in C_{GS}+C_{GB} and C_{GD} have been observed. For the ring

structure, two peaks in a capacitance-voltage curve have been observed at high drain voltages due to the additional corner effect. Besides, the circle structure has the same capacitance characteristics as the fishbone structure that indicates only one peak in the capacitance curve. We have to consider these parameters like the threshold voltage, quasi-saturation current and drift depletion capacitance that affect the capacitance in the LDMOS capacitance model.

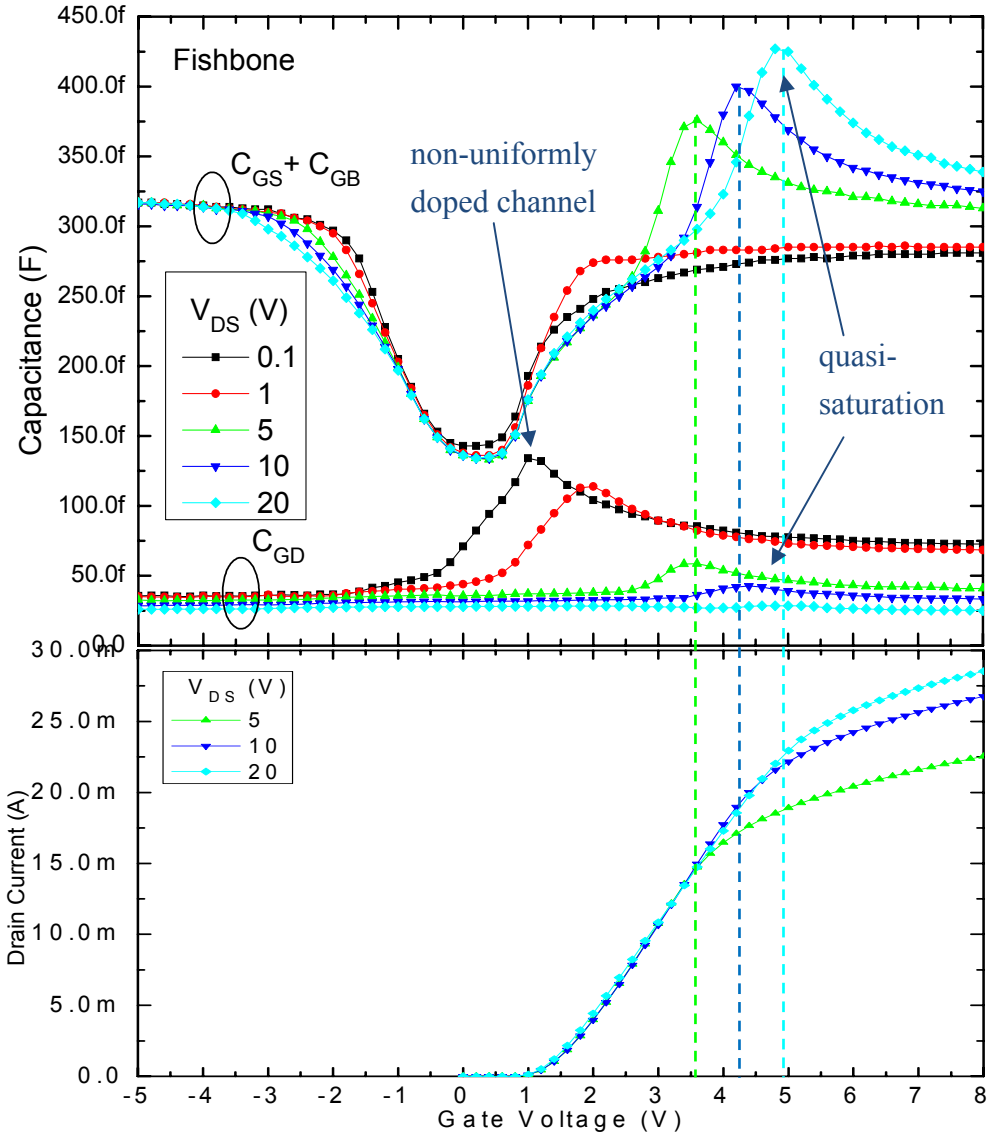
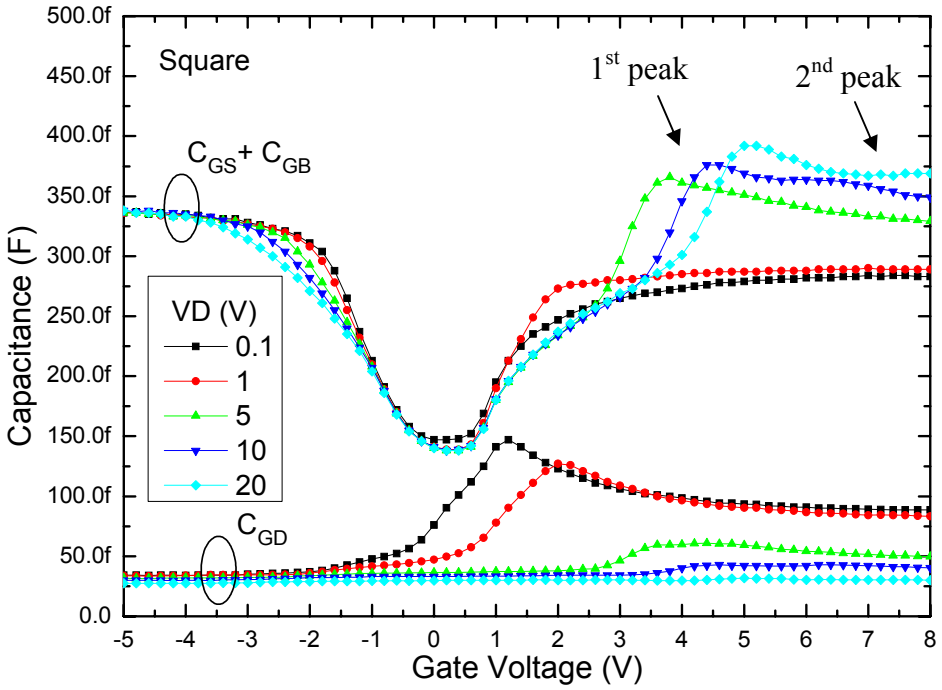
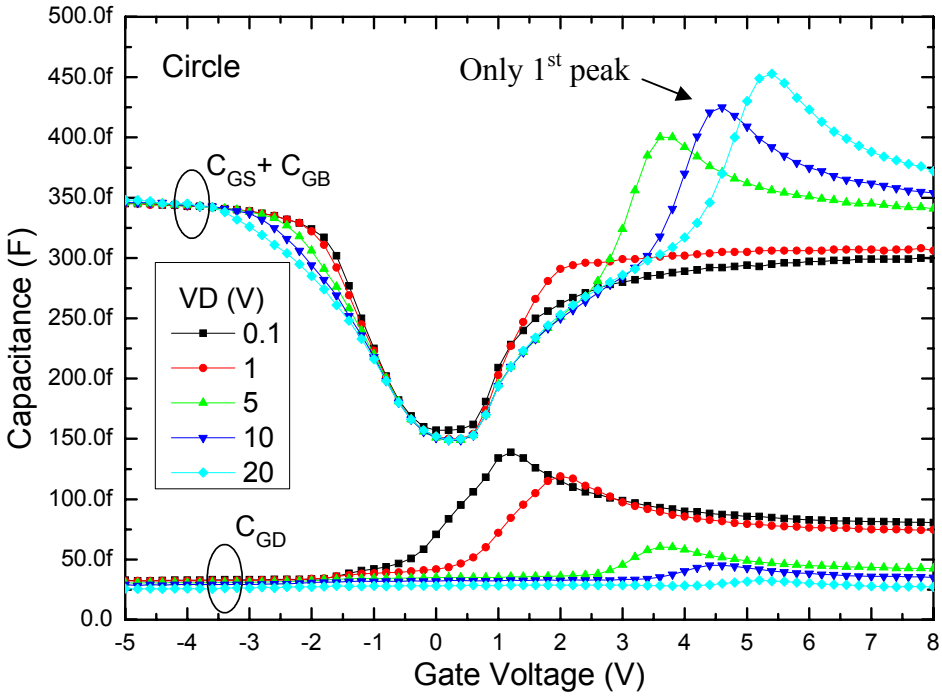


Fig. 4.1 Extracted C_{GS}+C_{GB}, C_{GD} and the drain current versus gate voltage at different drain biases for the fishbone structure.



(a)



(b)

Fig. 4.2 Extracted C_{GS}+C_{GB} and C_{GD} versus gate voltage at different drain biases for the (a) square and (b) circle structure.

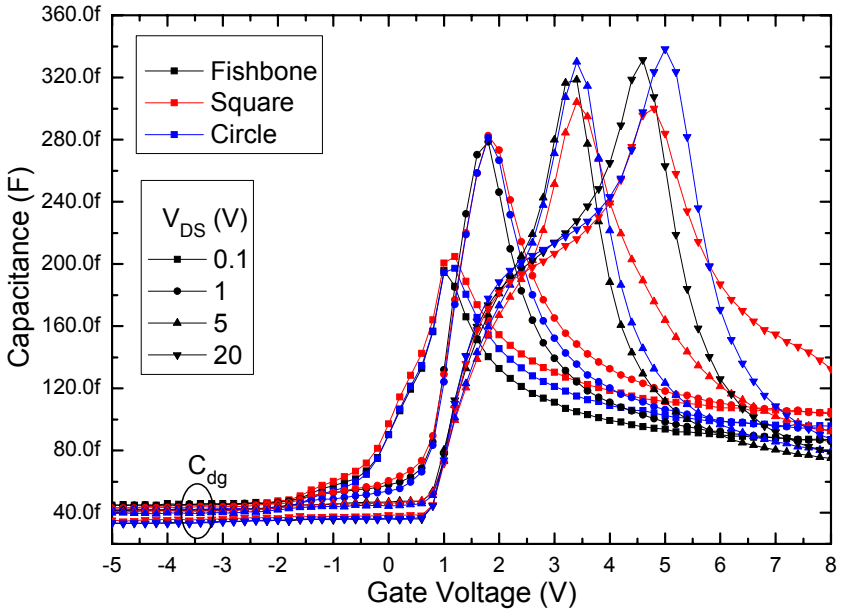
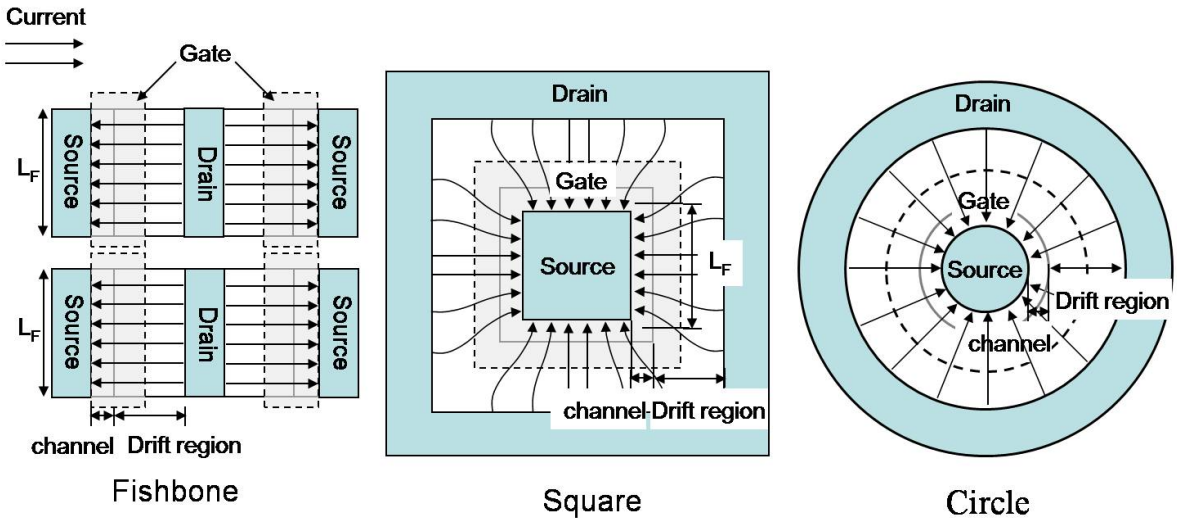


Fig. 4.3 Extracted C_{DG} versus gate voltage at different drain biases for the fishbone, square and circle structure.



(a) (b) (c)

Fig. 4.4 Schematic view of layout structure and current distribution: (a) fishbone structure, (b) square structure and (c) circle structure.

Chapter 5

Modified MOS Model 20 (MM20) for LDMOS

5.1 Introduction

The MOS Model 20 (MM20) is a compact MOSFET model focusing on DC characteristics. It has been developed to describe the electrical behavior of the region under the thin gate oxide of a high-voltage MOS device, like an LDMOS device. MM20 combines MOS Model 9 (MM9) for the channel region and MOS Model 31 (MM31) for the drift region under the thin gate oxide. This model calculates the equations that are describing transistor electrical characteristics in surface-potential formulations. In order to improve the convergence behavior during circuit simulation, it uses an internal voltage at the transition (node Di) from the channel region to the drift region to calculate the surface potentials [38]. The surface potential as a function of the terminal voltages is obtained by the explicit expression as derived in ref. 39. Using these equations can describe the all operation regimes (accumulation, depletion, and inversion in both the channel region and the drift region). In addition, the MM20 also include several important physical effects like mobility reduction, velocity saturation, drain-induced barrier lowering, static feedback, channel length modulation, and weak avalanche (or impact ionization). If transistors have an additional thick field oxide, this model can be used in series with a separate model for the drift region under the thick field oxide. Consequently, the MM20 provides an accurate description in all operating regimes, ranging from subthreshold to superthreshold, in both the linear and saturation regime [40].

5.2 T-CAD Simulation

We simulate the quasi-saturation effect in the LDMOS by using the T-CAD simulation

software. The structure is built on measured device in 2D dimension, and we do our best to make the simulation factor as the same as real phenomenon. Fig. 5.1 shows the simulated structures showing lateral electric field and the depletion region at V_g = 2.5 V and V_d = 10 V. The maximum lateral electric field occurs at the pinch-off region near the gate edge and the drift region under the FOX is inversion. At this condition, the device does not yet enter quasi-saturation and channel current still increases with increasing gate voltage. Under V_g = 10 V and V_d = 10 V, the space-charge distribution changes, and the maximum lateral electric field shifts toward the drain and occurs in the drift region (see Fig. 5.2). Additionally, the lateral electric field decreases near the gate edge and the drift region under the FOX becomes accumulation. At this condition, the drain current is dominated by drift region and the device enters quasi-saturation [41]. Above described device have the poly gate covering on FOX and this poly gate is called field plate. Next, we discuss the device only have poly gate on the channel region. Fig. 5.3 shows the device does not enter quasi-saturation and is biased at V_g = 2.5 V and V_d = 10 V. It is the same as Fig. 5.1 that the maximum lateral electric field occurs at the pinch-off region near the gate edge and the drift region under the FOX is inversion. As device is bias at V_g = 10 V and V_d = 10 V, the maximum lateral electric field still occurs in the channel region (see Fig. 5.4). In addition, the space-charge distribution does not change much and the most drift region under the FOX is still inversion. Therefore, the device with field plate can make the drift region transfer its type from inversion to accumulation and make the lateral electric field distribute uniformly. So, it would increase the device breakdown voltage.

5.3 Modeling Strategy

For simplicity, some physical effects like self-heating and weak avalanche are not concluded in the modified model. Besides, based on the T-CAD simulation results, we have modified the drift region current for better fitting our measured I-V and C-V curves.

The device DC model would be developed with analysis of carrier transport in the channel and drift regions. The drain current is separated from two elements, one is through the intrinsic MOS channel (I_{ch}) and the other is through the drift region (I_{drift}), and the two currents are formulated respectively in terms of the external bias V_G, V_D, V_S, V_B and the unknown voltage V_{Di}. Then, V_{Di} is solved automatically by equating I_{ch} to I_{drift}. Therefore, the drain current is expressed explicitly by the external terminal voltage. The channel current is expressed as follow:

$$I_{ch} = \frac{W \times \mu_{eff}^{ch} \times C_{ox}}{L_{ch}} \times \frac{\left(V_{inv0} - \frac{1}{2} \xi V_{DiS} \right) \times V_{DiS}}{1 + \theta_3 \times V_{DiS}}$$

Here, μ_{eff}^{ch} is the effective electron mobility in the channel region, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the thin-gate-oxide capacitance per unit area, V_{inv0} represents the inversion charge Q_{inv} per unit area at the source side, and $\theta_3 = \mu_{ch} / (L_{ch} v_{sat})$ represents velocity saturation in the channel region, with μ_{ch} the zero-field electron mobility in the channel region and v_{sat} the saturated drift velocity of electrons. The factor $\xi = (\partial Q_{inv}/ \partial \psi_s)/ C_{ox}$ reflects the variation of inversion charge with surface potential, and is taken as $\xi = [1+ (1/ 2 \cdot \gamma_0)] /\sqrt{(V_1 + \psi_{s0})}$, where γ_0 is the body factor at the source, V_1 = 1 V, and ψ_{s0} is the surface potential at the source. From Fig. 5.2 & Fig. 5.4, as the device enter quasi-saturation, the voltage drop in the drift region increases led to the maximum electric felid occurs in the drift region and drain current is dominated by drift region. The effective electron mobility (μ_{eff}^{dr}) is used to describes this effect. As electric felid increase in the drift region, the carrier velocity will enter saturation regime and θ_{3dr} ($= \mu_{eff}^{dr} / (L_{dr} v_{sat})$) can describes this effect. When device without field plate is biased gate voltage from 2.5 V to 10 V, the current have to pass through a depletion region under Fox. Therefore, the high resistance (R_{dr}) limits the current in the drift region when device enter quasi-saturation. In addition, the device with field plate has different

performance. As V_G= 2.5V, the drift region under Fox is depletion region and like general performance (see Fig. 5.3 & 5.4). As V_G= 10V, the drift region under Fox becomes electrons accumulated layer and the drain resistance is lower to enhance current (see Fig. 5.1& 5.2). The parameter R_{dr} is concluded in V_{qDi} and ξ_{dr} which simple equation is $V_{qDi}= L_{dr}f_{lin}/(W\mu_{dr}C_{ox}R_{dr})$, where f_{lin} is a function about the depletion thickness. The drift region current can be represented by combining above descriptions and be expressed as follow:

$$I_{dr} = \frac{W \times \mu_{eff}^{dr} \times C_{ox}}{L_{dr}} \times \frac{\left(V_{qDi} - \frac{1}{2} \times \xi^{dr} \times V_{DDieff}\right) \times V_{DDieff}}{1 + \theta_3^{dr} \times V_{DDieff}}$$

Where μ_{eff}^{dr} is the effective electron mobility in the drift region, θ_{3dr} represents the occurrence of velocity saturation in the drift region, and $V_{qDi} = -Q_{dr} / C_{ox,}$ where Q_{dr} is the charge density per unit area underneath the thin-gate oxide including accumulation and depletion in the drift region, for simplicity, ξ_{dr} represents the variation of accumulation charge with voltage.

In order to calculate the capacitance, we present nodal charges in the channel and drift region as follow:

$$Q_G^{ch} = W \times L \times C_{ox} \times \left(V_{oxm} + \left(\frac{F_j}{12X_i}\right) \times dV_{inv}\right)$$

$$Q_D^{ch} = -\frac{W \times L \times C_{ox}}{2} \times \left(V_{invm} - \frac{dV_{inv}}{6}\right) \times \left(1 - \frac{F_j}{2} - \frac{F_j^2}{20}\right)$$

$$Q_S^{ch} = -\frac{W \times L \times C_{ox}}{2} \times \left(V_{invm} + \frac{dV_{inv}}{6}\right) \times \left(1 + \frac{F_j}{2} - \frac{F_j^2}{20}\right)$$

$$Q_B^{ch} = -\left(Q_G^{ch} + Q_D^{ch} + Q_S^{ch}\right)$$

$$Q_G^{dr} = -\left(Q_G^{dr} + Q_D^{dr} + Q_S^{dr}\right)$$

$$Q_D^{dr} = -\frac{W \times L_D \times C_{ox}}{2} \times \left(V_{qDm} - \frac{dV_{qD}}{6} \right) \times \left(1 - \frac{F_{jdr}}{2} - \frac{F_{jdr}^2}{20} \right)$$

$$Q_S^{dr} = -\frac{W \times L_D \times C_{ox}}{2} \times \left(V_{qDm} + \frac{dV_{qD}}{6} \right) \times \left(1 + \frac{F_{jdr}}{2} - \frac{F_{jdr}^2}{20} \right)$$

$$Q_B^{dr} = -\frac{W \times L_D \times C_{ox}}{2} \times \left(V_{invDi} + V_{invDx} \right)$$

Where V_{oxm} represents the average voltage drop across the oxide, and $F_j = dV_{inv} / (V_{invm} + \xi\Phi_T)$, and $V_{invm} = 0.5(V_{inv0} + V_{invL})$, and $dV_{inv} = (V_{inv0} - V_{invL})$. Beside, $F_{jdr} = (dV_{qD}/V_{qDm})$, $V_{qDm} = 0.5 (V_{qDi} + V_{qDx})$, and $dV_{qD} = (V_{qDi} - V_{qDx})$, where V_{qDi} and V_{qDx} are drift region charge at D_i and D_x, respectively.

5.4 Results and Discussion

The model parameters of fishbone and circle devices were extracted from their I-V and C-V curves. The measured and simulated I-V curves are shown in Figs. 5.5 and 5.6. The simulated results show excellent consistency with the measured data for two structures except at high drain voltages. At high drain voltages, the drain current is influenced by self-heating and weak avalanche effects, which have been ignored in our model. Fig. 5.7 shows the simulated and measured $C_{gs} + C_{gb}$ and C_{gd} versus gate voltage with different drain voltages. The simulated capacitance characteristics also show consistency with the measured data for two structures. Some extracted model parameters are listed in Table 5-1. For circle structure, the electron mobility in the drain region (μ_{dr}) is larger than fishbone structure due to lower drain parasitic resistance. The parameter R_{dr} in the circle structure is lower and enhances the drift region current. In the chapter 2, we also know the fishbone structure having high R_D which is extracted from small signal circuit model causes to the device enter the quasi-saturation earlier. In addition, the θ_{3dr} is similar because effective drift length (L_{dr}) is longer for circle structure. From the C-V curves, we find that the flat band voltage occurs at

V_G= -1.7~-2V and is smaller for circle structure. This is similar as the extracted model parameter V_{FB}. Mover, the electron mobility in the channel region (μ_{ch}) is lager for fishbone structure due to lower channel resistance. So, the fishbone device has larger transconductor and these performances are agreement with chapter 2.

5.5 Summary

The device models have been obtained for fishbone and circle structures by using the modified MM20. The quasi-saturation effect dominated in the drift region is also considered. From I-V and capacitance characteristics, this model shows an accurate description in all operating regimes, and provides a good agreement between simulated and measured data. In addition, we confirm the device enters the quasi-saturation earlier due to higher drain parasitic resistance and the drain parasitic resistance is lower for circle structure. Consequently, the extracted model parameters have been analyzed and present the similar information as chapter 2.

Table 5-1 Extracted V_{FB}, μ_{ch}, μ_{dr}, θ_{3dr}, R_{dr} and L_D from modified MM20 for different layout structures.

	V_{FB}	μ_{ch}	μ_{dr}	θ_{3dr}	R_{dr}	L_D
Fishbone	-1.832	194.6m	694.2u	330m	86.54	270n
Circle	-1.85	181.5m	782.7u	332.6m	76.31	280n

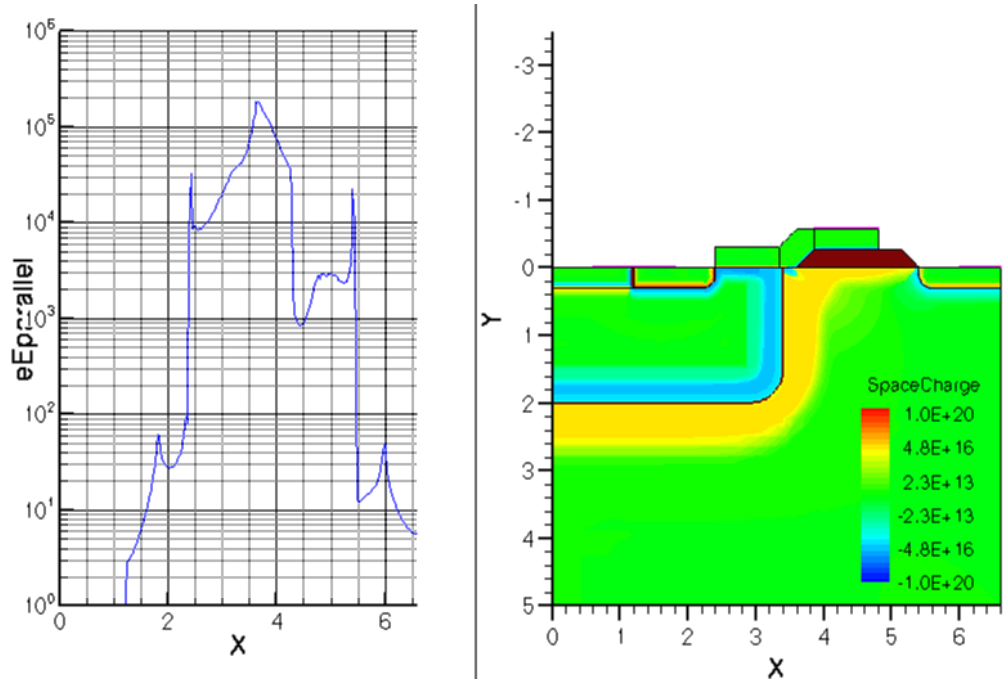


Fig. 5.1 The right figure shows the space charge distribution of LDMOS at V_g= 2.5V and V_d= 10V and the left figure shows the electric field along the channel region to drift region.

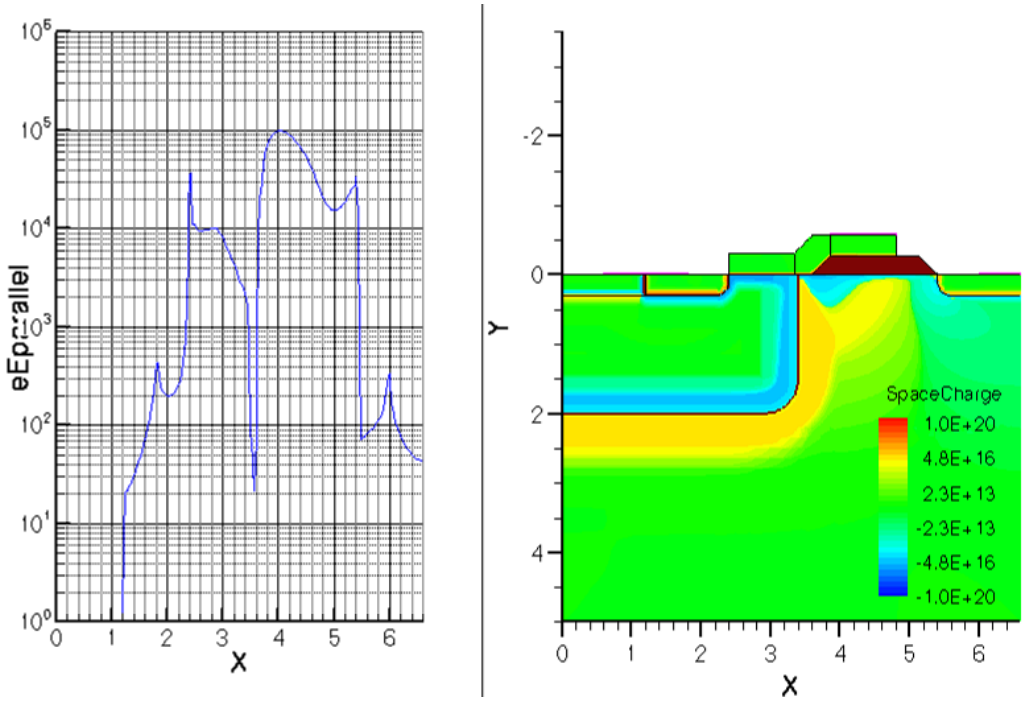


Fig. 5.2 The right figure shows the space charge distribution of LDMOS at V_g= 10V and V_d= 10V and the left figure shows the electric field along the channel region to drift region.

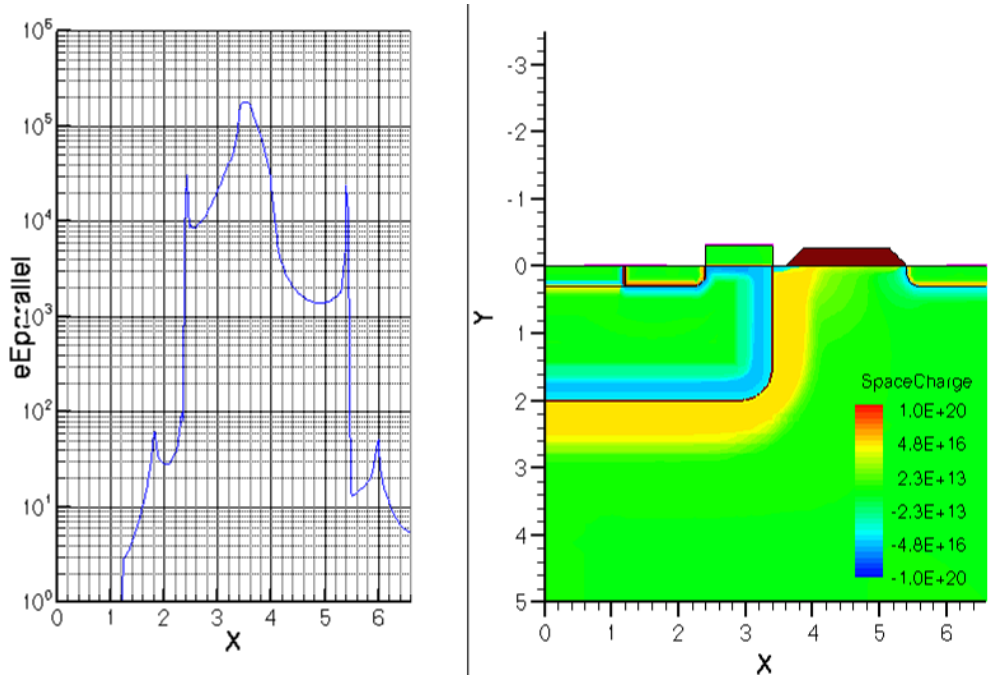


Fig. 5.3 The right figure shows the space charge distribution of LDMOS at V_g= 2.5V and V_d= 10V and the left figure shows the electric field along the channel region to drift region.

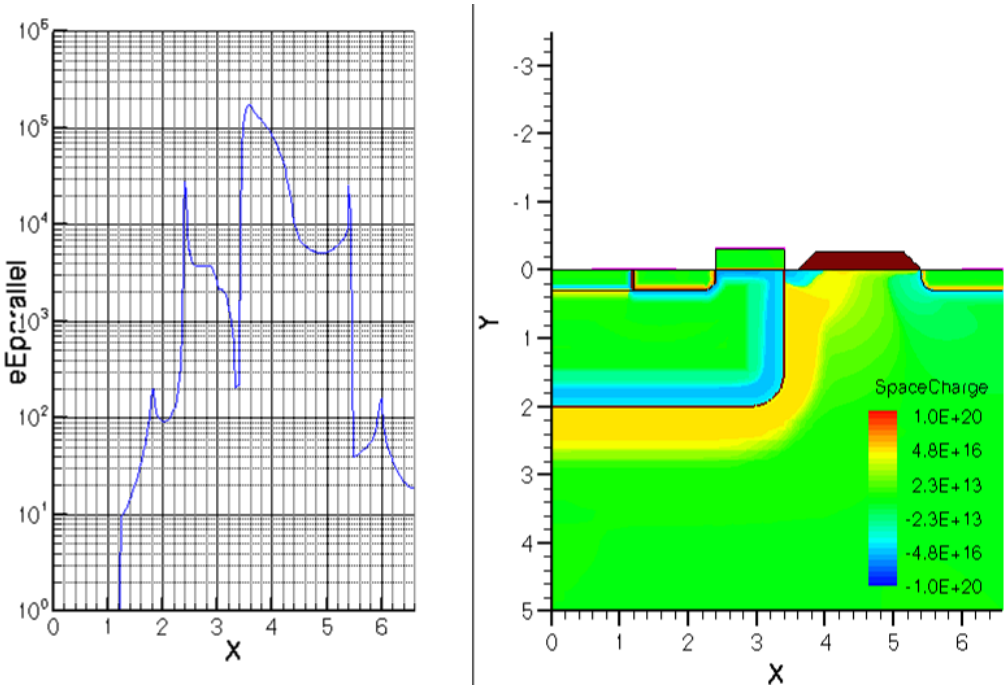
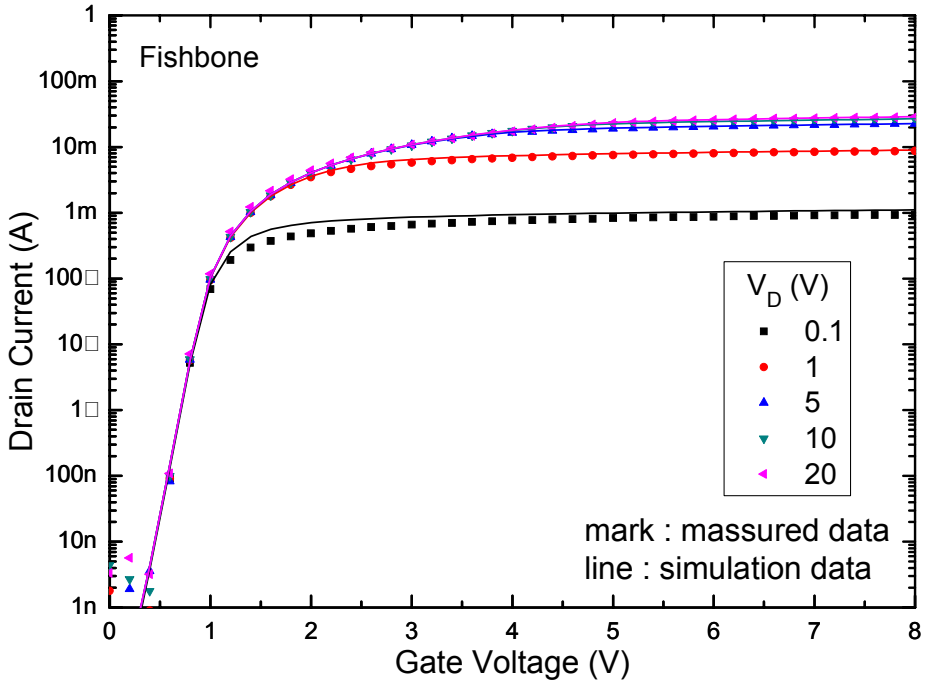
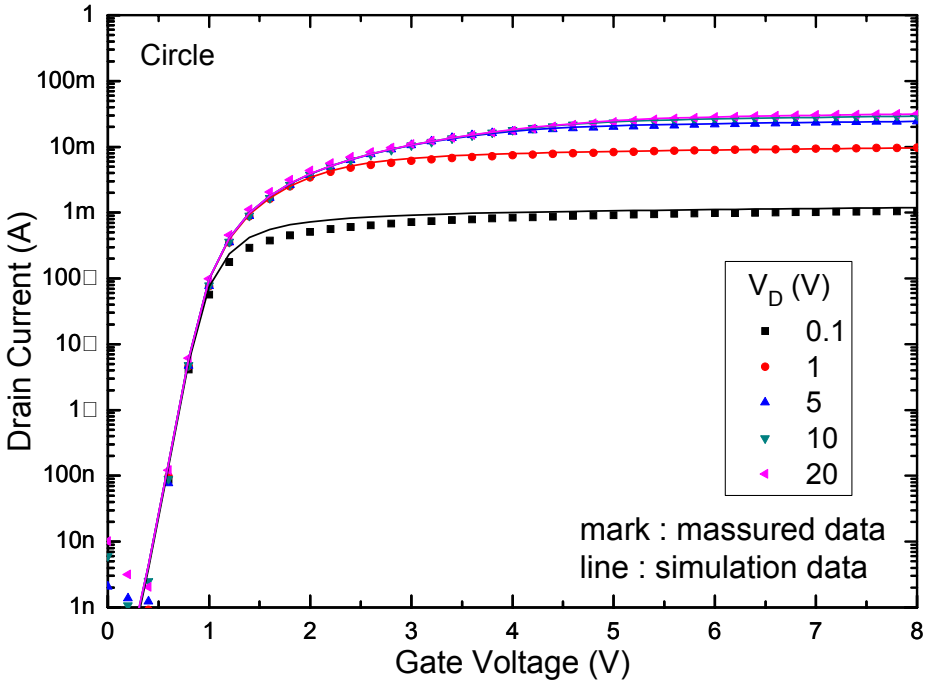


Fig. 5.4 The right figure shows the space charge distribution of LDMOS at V_g= 10V and V_d= 10V and the left figure shows the electric field along the channel region to drift region.

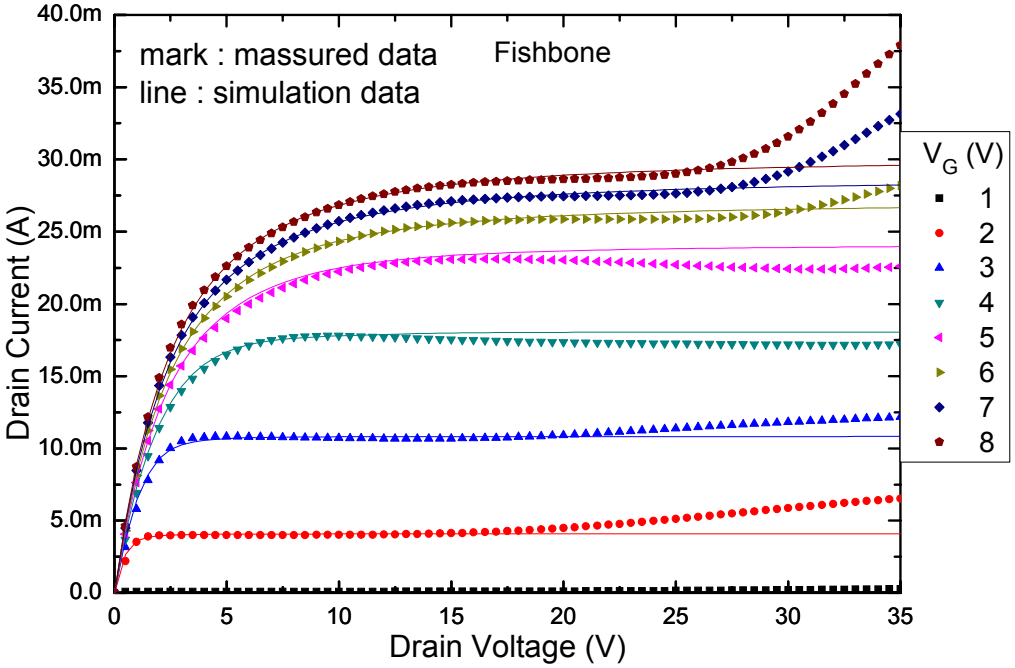


(a)

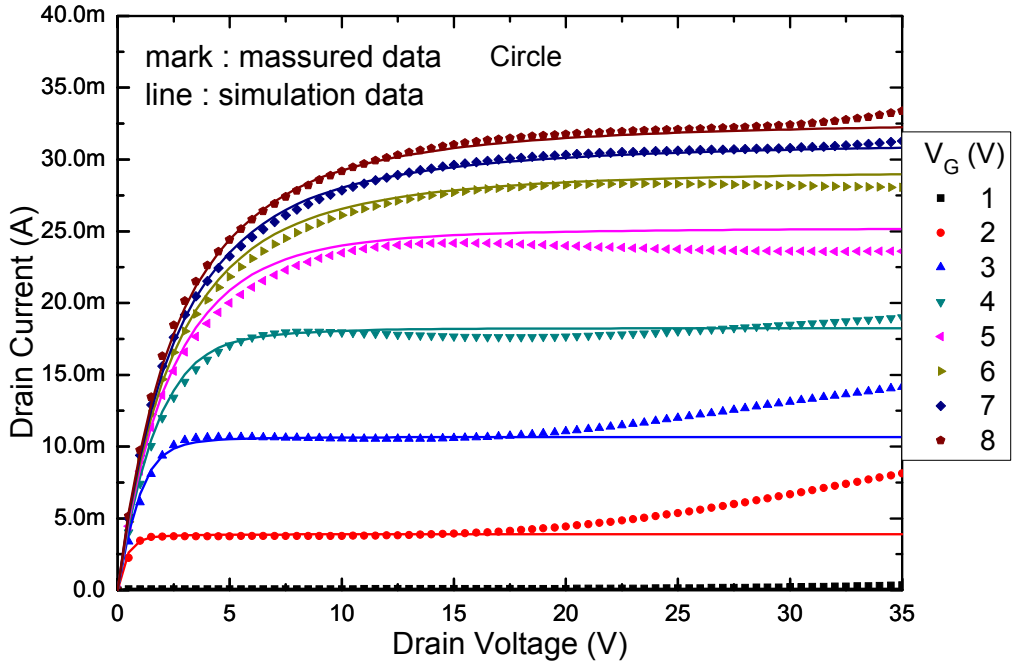


(b)

Fig. 5.5 Measured (mark) and simulated (line) drain current I_{DS} versus gate voltage at different drain biases for the (a) fishbone and (b) circle structures.

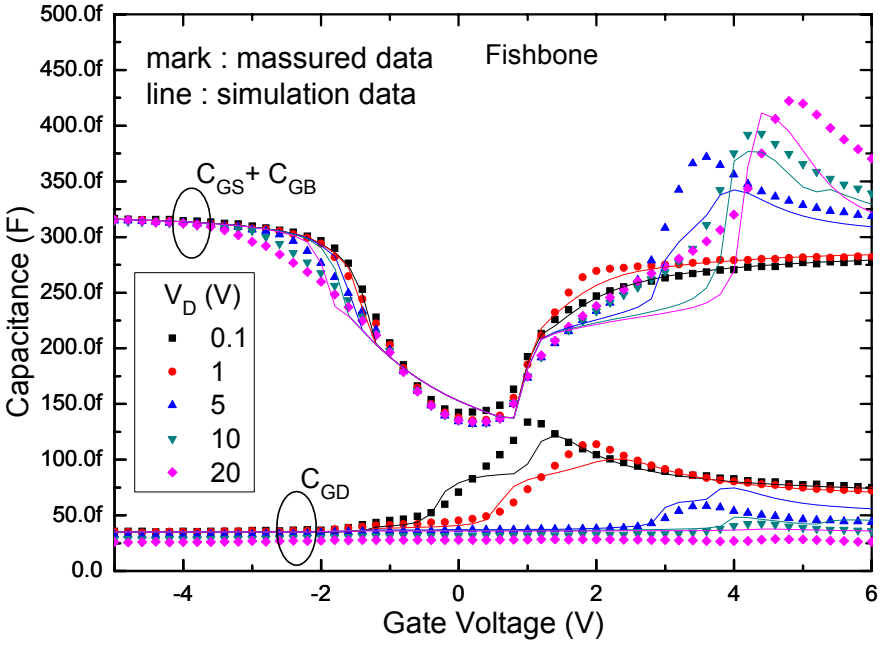


(a)

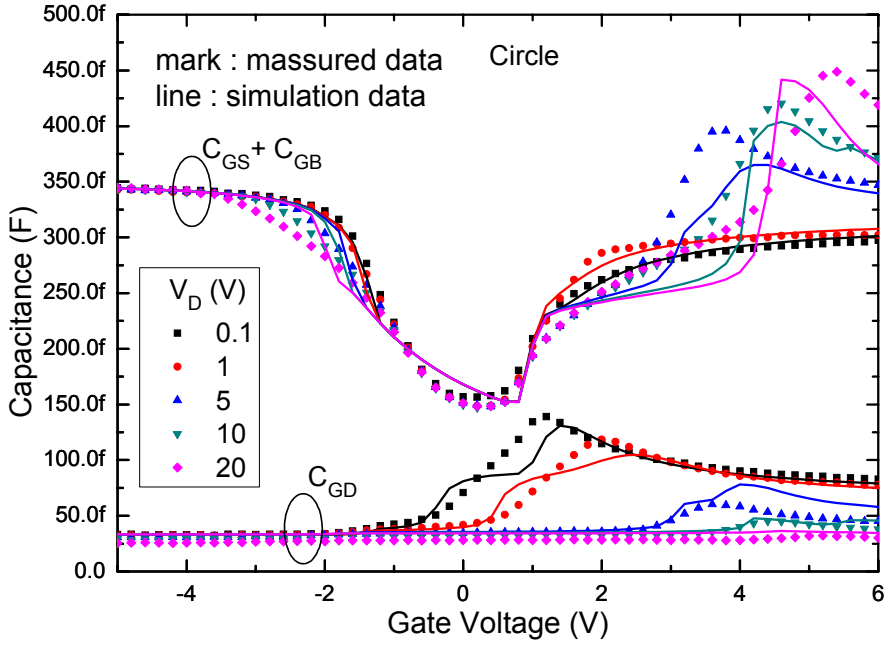


(b)

Fig. 5.6 Measured (mark) and simulated (line) drain current I_{DS} versus drain voltage at different gate biases for the (a) fishbone and (b) circle structures.



(a)



(b)

Fig. 5.7 Measured (mark) and simulated (line) C_{GS}+C_{GB} and C_{GD} versus gate voltage at different drain biases for the (a) fishbone and (b) circle structures.

Chapter 6

Conclusions and Suggestion

6.1 Conclusion

We have investigated the DC, AC, high-frequency, RF power characteristics and DC model of LDMOS transistors with different layout designs. Based on the same distance of each cell, we find that the cutoff frequency, maximum oscillation frequency and power performance were improved using the ring structures. In the traditional design, the ring (also called enclosed, edgeless, or donut in other literatures) structures were used to lower the parasitic capacitances for more linear and faster devices [43-44]. For MOSFET, the conventional parasitic drain capacitance refers to the n+ drain to p-substrate junction capacitance. Hence, the drain was always surrounded by the transistor channel and source to reduce the area. In LDMOS, however, the parasitic drain capacitance refers to the deep n-well (DNW) to p-substrate junction capacitance. Therefore, drain outside or inside for ring structure has no impact on drain capacitance. Since larger area for output terminal could reduce the parasitic drain resistance, ring structures with drain outside layout would be the better choice for the LDMOS. This layout design can improve the performance without altering the process flow. In addition, we also find that the transconductance, on-resistance, cutoff frequency and linearity were improved except maximum oscillation frequency and power performance by using the circle structure. It is obvious that the circle structure success to compress the corner effect in the square structure and improve the DC performance. Finally, the modified MM20 shows an accurate description on DC and capacitance characteristics. And the results are agreement with above descriptions.

In chapter 2 fishbone, square, octagon and circle structure were investigated. Fishbone and ring structures were compared. The fishbone structure has better on-resistance and

linearity due to lower channel resistance but it has larger R_{TH}. The RF performance like f_T, f_{max} and power were improved for the ring structures due to the lower drain parasitic resistance. If reducing the distance of each cell in the ring structure, the RF performance will be enhanced much due to decrease the parasitic capacitance and maintain the same DC performance as fishbone. In addition, square and circle structures were also compared. The DC performance like drain current and transconductance were enhanced for the circle structure due to lower drain parasitic resistance and uniform drain current density contributed by canceling the corner of drift region.

In chapter 3 square devices with various channel width were investigated. The device with larger W_{ch} has better f_T, f_{max}, RF power and linearity due to lower drain parasitic capacitance, but it also has larger on-resistance due to larger drain parasitic resistance. It shows a trade-off between the DC performance and the RF performance.

Capacitance characteristics were analyzed completely in chapter 4. For having a non-uniform doping channel, C_{GD} exhibits a peak at the threshold voltage. For existence of the drift region, C_{GS}+ C_{GB} and C_{GD} show a peak at the onset of quasi-saturation. In the square structure, the second peaks in a capacitance-voltage curve have been observed at high drain voltages due to the additional corner effect. Moreover, the circle structure only has the first peaks in a capacitance-voltage curve just like as fishbone.

In chapter 5 the modified MM20 is used to simulate the LDMOS with different layout design. This model provides an accurate description in all operating regimes, ranging from subthreshold to superthreshold, in both the linear and saturation regime and includes physical effects like mobility reduction, velocity saturation, drain-induced barrier lowering, static feedback and channel length modulation. A comparison with DC and capacitance measurements on LDMOS device shows a very good agreement. In addition, the extracted model parameters have been analyzed and show an agreement with chapter 2.

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