國立交通大學

電子工程學系 電子研究所

博 士 論 文

高壓製程積體電路之

靜電放電防護設計與應用

Design and Applications of ESD Protection

in High-Voltage Integrated Circuits

研 究 生：陳穩義

指導教授：柯明道 教授

中 華 民 國 一 百 年 十 二 月


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研 究 生：陳穩義　　Student：Wen-Yi Chen

指導教授：柯明道　　Advisor：Ming-Dou Ker

國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

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摘要

高壓製程積體電路在車用電子，消費性電子產品，以及驅動電路等方面，近年來均獲得極大的重視與廣泛應用。在電子系統中，靜電放電防護能力為產品可靠度的重要指標之一。在高壓製程中，由於複雜的元件結構，其靜電放電防護設計，具有相當之困難度及挑戰。

N 型橫向雙擴散金氧半電晶體 (n-channel lateral DMOS)普遍具有不佳之靜電放電防護能力；為了提升該元件之靜電放電防護能力，一具格子形狀 (waffle)之特殊佈局方式於章節二中提出。該佈局方式可使元件保存其電流驅動能力，並於對角線上得到額外之觸發點；透過該額外觸發點，N 型橫向雙擴散金氧半電晶體得以透過基極觸發之技巧，來促進靜電放電發生時，元件之均勻導通程度，以提升其靜電放電防護能力。該佈局成效已於一 0.5 微米及一 0.35 微米高壓製程中獲得實際驗證。

使用矽控整流器為在高壓製程中提升靜電放電防護能力的解決方案之一。然而，矽控整流器在實際應用中，會造成其他可靠度疑慮，例如元件之安全操作區間(Safe Operating Area)受到壓縮。在章節三中，首先針對安全操作區間及目前習知的改進技術，做一詳細的介紹。於章節四中，則特別提出一多晶矽閘極彎曲之特殊元件佈局方式，以改善因使用矽控整流器在 N 型橫向雙擴散金氧半電晶體中，對安全操作區間所造成的負面影響。

除兩種元件等級的新型佈局方式外，由於積體電路產品需要達到靜電放電防護能力的規格要求，本論文分別於章節五及章節六，提出兩個已成功

應用於商用積體電路產品的創新靜電放電防護設計。此兩個靜電放電防護設計，皆應用於全金屬矽化物製程(fully-silicided)之積體電路產品。使用全金屬矽化物製程可提升積體電路產品的電路性能，但卻會造成靜電放電防護能力的下降。特殊的靜電放電防護設計，為全金屬矽化物製程中的必要設計。章節五中，透過兩種鎮流電阻(ballast resistance)設計方式，順利將一款微控制積體電路晶片之人體靜電放電模式靜電放電防護能力，由 1.5 千伏特提升至超過 6 千伏特。

章節六的全金屬矽化物製程靜電放電防護設計，為專為電壓程式腳位應用所做出的創新設計。在記憶體寫入時，該電壓程式腳位將升壓至一大於正常工作電壓之電位。因此，該腳位之靜電放電防護設計，需符合開汲極與故障保險(open drain / fail safe)的設計需求：自電壓程式腳位至電源線間，不能有順偏二極體的存在，以避免漏電流的產生。此外，該靜電放電防護設計，在電壓程式訊號具備極快速的電壓上升時間(數十奈秒等級)下，仍可避免誤觸發的問題，不影響記憶體寫入的操作。此一特性，使得具備該靜電放電防護設計的微控制器，可通用市面上多種記憶體寫入器。本靜電放電防護設計，已於一矽晶片上實際驗證，可提供五千伏特之人體靜電放電防護耐受度。

在廣泛的可靠度議題中，除靜電放電防護設計外，閂鎖效應為另一個重要的設計考量。在考量閂鎖效應時，元件之維持電壓(holding voltage)為一重要的參考指標。章節七則探討 N 型橫向雙擴散金氧半電晶體，其維持電壓對時間的關聯性。透過長脈寬傳輸線觸波產生系統的量測，發現 N 型橫向雙擴散金氧半電晶體的維持電壓，會隨著時間的經過而下降。該現象將造成未來高壓製程中閂鎖效應的測試方式與佈局準則訂定的不同考量。

簡而言之，本論文提出創新的學術研究貢獻，更針對實際積體電路產品之靜電放電防護，做出切題且創新的實用設計。本論文促進了解高壓製程中元件於靜電放電時的反應與現象，並提供數種於高壓積體電路製程中可實用的靜電放電防護解決方案。

DESIGN AND APPLICATIONS OF ESD PROTECTION IN HIGH-VOLTAGE INTEGRATED CIRCUITS

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Abstract

High-voltage (HV) technologies are booming in recent years due to the increasing demand on automotive electronics, consumer integrated circuits (ICs), driver circuits for display panels and so forth. To have a rigorous end product or electronic system, electrostatic discharge (ESD) is one of the most important factors affecting IC reliabilities; IC industries are struggling for good ESD protection designs due to the structural complexity of transistors and application varieties in HV technologies.

The n-channel lateral DMOS (nLDMOS) devices in HV technologies are known to have poor ESD robustness. To improve the ESD robustness of nLDMOS, a co-design method combining a new waffle layout structure and a trigger circuit is proposed in chapter 2 to fulfill the body current injection technique. The proposed layout and circuit co-design method on high-voltage nLDMOS has been successfully verified in a 0.5-μm 16-V BCD process and a 0.35-μm 24-V BCD process without using additional process modification. Experimental results have shown significantly improved turn-on uniformity and ESD robustness of nLDMOS.

Silicon controlled rectifier (SCR) in HV technologies is usually embedded in output arrays to provide a robust and self-protected ESD capability. Though the embedded SCR has

been proven as an excellent approach to increasing ESD robustness, mis-triggering of the embedded SCR during normal circuit operating conditions can bring other application reliability concerns. The safe operating area (SOA) of output arrays due to SCR insertion has seldom been evaluated. In chapter 3, SOA is first reviewed and in chapter 4, the impact of embedding SCR to the electrical SOA (eSOA) of an nLDMOS array is investigated. Experimental results showed the nLDMOS array suffers substantial degradation on eSOA due to the embedded SCR. Design approaches, including a new proposed poly bending layout, is proposed in chapter 4. With the poly bending layout method, both high ESD robustness and a wide SOA can be achieved at the same time on an nLDMOS output array.

In addition to the two layout designs in Chapter 2 and 4, another two practical fully-silicided designs have been applied to IC products and have passed product-level ESD verifications. Silicidation is a common process step which can improve the circuit operating speed but has been reported to substantially decrease ESD robustness of MOSFETs. Silicide blocking is a useful method to alleviate this ESD degradation from silicidation, but it requires additional mask and process steps and the fabrication cost is increased. For cost reduction, two new ballasting layout schemes are included in chapter 5 to effectively improve ESD robustness of fully-silicided push-pull I/O buffers without using the silicide blocking. Results from real IC products have confirmed that the new ballasting layout schemes can successfully increase human-body model (HBM) ESD robustness of fully-silicided I/O buffers from 1.5 to over 6 kV.

The other fully-silicided ESD protection design in chapter 6 is for ICs with a voltage programming (V_{PP}) pin. When programming read only memories (ROM), a voltage higher than the normal power supply voltage (V_{DD}) is applied to the V_{PP} pin. A fail-safe structure that does not have a diode current path to V_{DD} power supply line is necessary for a V_{PP} pin. A new V_{PP} pin ESD protection design is necessary for the fully-silicided and the fail-safe requirements. The design proposed in chapter 6 not only meets the two requirements but also

features high resistivity to mis-triggering when the V_{PP} programming voltage has a fast rise time. This special design consideration makes ICs with the ESD protection design be compatible to ROM programmers that can have fast voltage slew rate on V_{PP} pins when programming. This new V_{PP} pin ESD protection design has been successfully verified on a commercial IC product and equipped the IC with an HBM ESD protection level of 5 kV.

Besides the requirement of high ESD robustness, latchup is another important reliability consideration for silicon ICs, especially in HV technologies. Holding voltage is one of the critical design considerations when developing elements with high latchup immunity. Because a HV device is easily damaged by the huge power generated from direct current (DC) curve tracer, the device holding voltage with respect to latchup immunity is often referred to the holding voltage measured by TLP systems with a 100-ns pulse width. To evaluate the validity of this practice, a long-pulse TLP system were used to investigate characteristics of an nLDMOS's holding voltage in time domain. Measurement results in chapter 7 revealed that the self-heating effect results in overestimation of the holding voltage acquired from a 100-ns TLP system. A gradually decreasing holding voltage of the nLDMOS in time domain is observed, which leads to new concerns when engineering holding voltage of transistors in HV technologies. With these novel results in HV technologies, this dissertation provides both advanced academia research achievements and practical ESD design solutions to IC industries.

Acknowledgment

在報考博士班前，曾經有前輩在鼓勵之餘也告訴我，博士班是一條漫長而孤獨的道路。從打開這扇門起跑開始，到撰寫這篇致謝準備朝向接下來的目標前進；回首這段時間的歷程，不自覺令人想起這句感觸良多的話語。在這條路上，我想我是幸運的；因為不論在學業或精神上，我都得到許多來自師長、同儕或家人的支持，讓我得以順利完成博士學業。

來自家人的陪伴與支持，一直是我在感到無助和徬徨時最大的精神支柱。我要向我的父親陳世霖先生，以及母親林清珠女士，獻上最崇高的感謝與敬意。由於有您們對我從小無怨的付出，以及一路給我的關心和栽培，才讓我的人生得以有諸多的選擇，並完成我的博士學業。希望在不久的將來，我能開始回報您們的恩情。我也要感謝我的太太陳瑩柳女士；由於妳的存在與陪伴，增添了這條孤獨道路上的溫暖。同時，也感謝我的哥哥陳瑞宗先生、嫂嫂林易汶女士，您們所帶給我屬於家人的親情，是一種無可取代的聯繫與鼓勵。

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陳 穩 義
謹誌於臺灣‧新竹
中華民國 100 年 12 月

William Wen-Yi Chen
in Hsinchu, Taiwan
December, 2011

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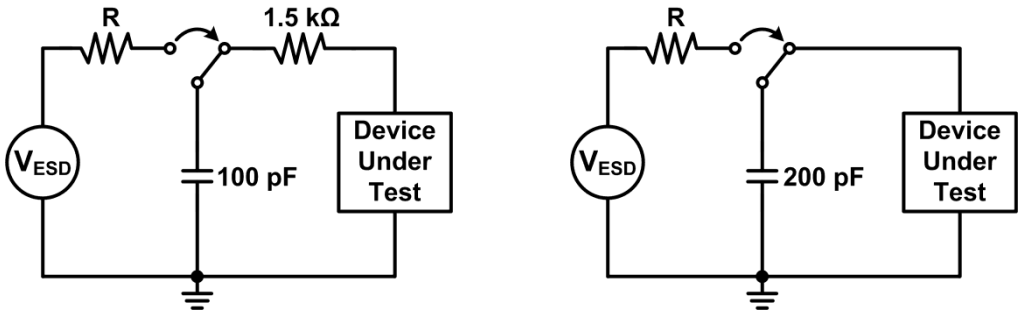
Chapter 1

Introduction

In this chapter, the role and applications of high-voltage (HV) technologies in integrated circuits (ICs) are introduced. Test methods and standards of electrostatic discharge (ESD) related to this dissertation are reviewed as well. Followed by the dissertation organization, this chapter provides motivation and staring materials to the research results of this dissertation.

1.1. High-Voltage Technologies in Integrated Circuits

With the thriving applications in consumer electronics, automotive electronics, display driver and power management ICs…etc., HV technologies are booming in recent years. Due to different application-oriented considerations, HV technologies have a wide spectrum of power levels and can mainly be classified in three categories [1]. The first category has a wide operating voltage (from several tens of volts up to 300 V) but low operating current. Examples for this category include plasma display panel (PDP), light-emitting diode (LED), and liquid crystal display (LCD) driver ICs. A cost-effective solution is usually the development target of this category. The second category has a relatively low (< 100 V) operating voltage. Examples for this category include automotive electronics and power management ICs for computers. Low turn-on resistance, fast switching speed and robust operating characteristics are requirements for this category. The third category has a relatively high blocking voltage (> 200 V). Motors, electric vehicle drivers, or lamp ballasts are examples for this category. Usually special power transistors like insulated gate bipolar transistors (IGBTs) are used in this category because the on-resistances of conventional silicon power MOSFETs are too large to accept.



(a) (b)

Fig. 1.1. Equivalent circuits of (a) HBM and (b) MM ESD tests.

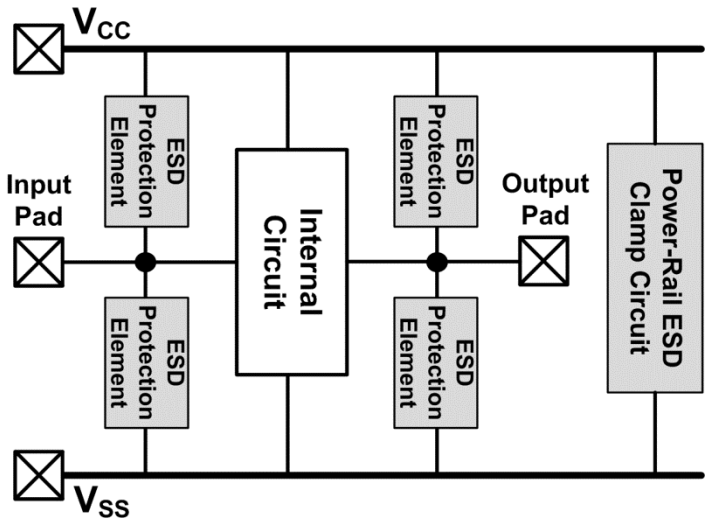


Fig. 1.2. A complete ESD protection network for general CMOS ICs.

1.2. ESD and Its Design Challenges in High-Voltage Technologies

ESD is one of the most important reliability concerns for IC products. To protect ICs from being damaged by ESD, on-chip ESD protection design is necessary [2]. Due to different charging and discharging mechanisms, there are three component-level models used to simulate the ESD events and to test the robustness of IC products: human-body model (HBM), machine model (MM), and charged-device model (CDM) [3]–[5]. HBM or MM mimics ESD events when an IC is discharged to ground through a human body or a machine,

respectively. Equivalent circuits of HBM and MM ESD tests are shown in Fig. 1.1(a) and (b). Since either input/output (I/O) pins or power pins can be grounded in ESD events, on-chip ESD protection designs are not only necessary to I/Os but also to V_{DD} and V_{SS} power pins. A complete ESD protection network to general CMOS ICs is shown in Fig. 1.2. Both I/O ESD protection elements and power-rail ESD protection circuits are required for a whole-chip ESD protection design [6].

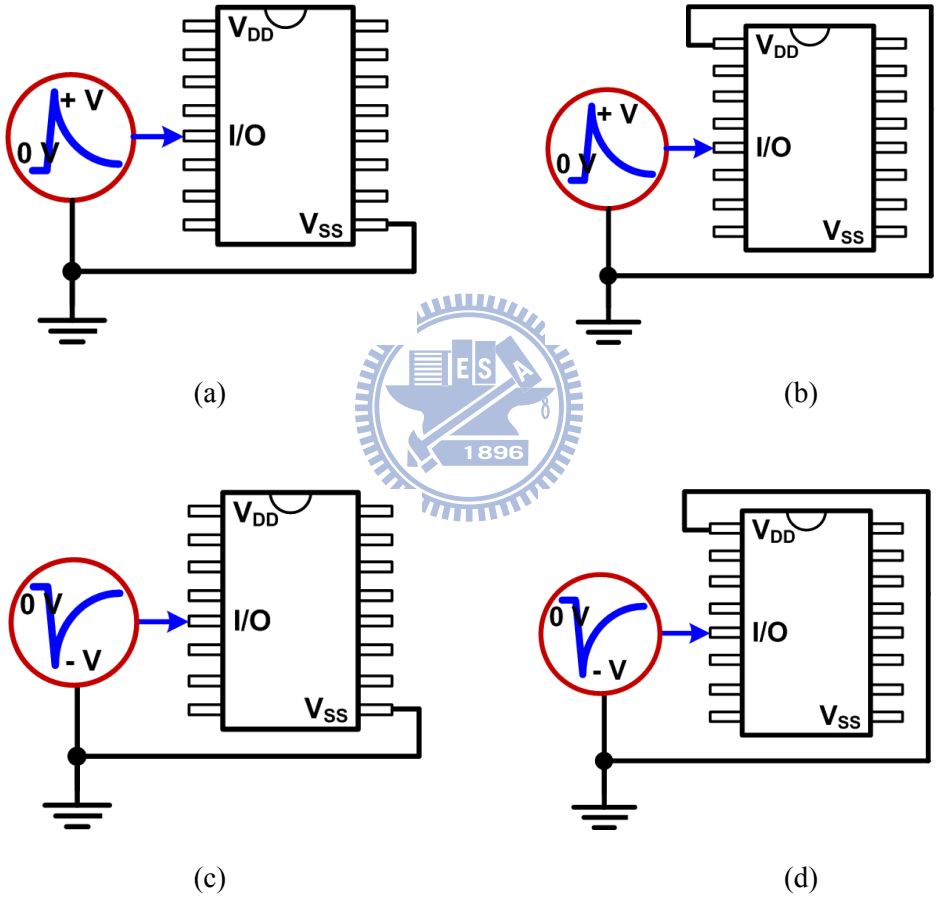
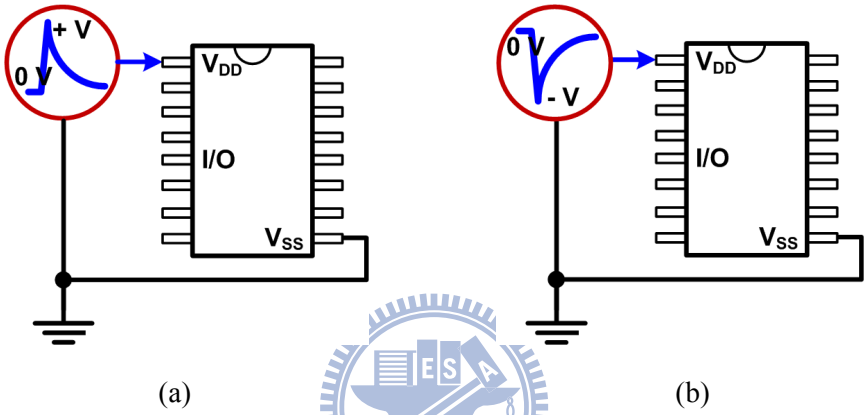


Fig. 1.3. Packaged IC tests at I/O pins with (a) positive-to-V_{SS} (PS-), (b) positive-to-V_{DD} (PD-), (c) negative-to-V_{SS} (NS-), and (d) negative-to-V_{DD} (ND-), mode ESD stresses.

For packaged ICs that have multiple pins, the ESD tests have to compromise with the testing time and the pin combinations. Electrostatic charges can be either positive or negative, and the grounded pin for an I/O ESD test can be either V_{DD} or V_{SS}. Accordingly, there are

four ESD test combinations at an I/O pin: positive-to-V_{SS} (PS-mode), positive-to-V_{DD} (PD-mode), negative-to-V_{SS} (NS-mode), and negative-to-V_{DD} (ND-mode) ESD stresses (see Fig. 1.3). ESD stresses between power pins (V_{DD} to V_{SS}) are also specified in the standards to verify the whole-chip ESD protection capability, as the test diagram shown in Fig. 1.4. Typically, the basic ESD specification for commercial IC products is to pass 2-kV HBM ESD stresses.



(a) (b)

Fig. 1.4. Packaged IC tests with (a) positive and (b) negative ESD stresses between power pins.

Though HV transistors are designed to sustain voltages ranging from several tens up to more than thousands of volts, their ESD protection levels do not scale with rated blocking voltages. On the contrary, due to their complicated device structures, ESD protection levels are usually poor and hard to engineer. In [7], a strong non-uniform turn-on effect in a HV ESD protection NMOS was observed, *i.e.* the ESD protection level does not linearly scale with the device dimension. Accordingly, even a large ESD protection device is utilized as the on-chip ESD protection element, a poor ESD protection level can still result. Fig. 1.5 shows the measured MM ESD protection levels of gate-grounded n-channel lateral DMOS (gg-nLDMOS) with different effective channel widths. Strong non-uniform turn-on effect is confirmed comparing the ideal and measured MM ESD robustness.

In HV applications, often the open drain structure is necessary especially when driving

external inductive loads. Traditionally, the power-rail ESD clamp circuit in Fig. 1.2 is able to help discharge ESD current and is critical to high ESD protection levels. In an open drain or a fail-safe structure, there is no (parasitic) forward diode from input/output (I/O) pad to the V_{CC} HV power supply line. The power-rail ESD clamp circuit hence does not help discharge ESD current, PS-mode ESD stresses for example (see Fig. 1.6); the ESD protection design at an I/O pad has to take all the ESD current. The open drain structure puts a big challenge to ESD design engineers, and ESD design solutions to the open drain structure are hence valuable to IC industries.

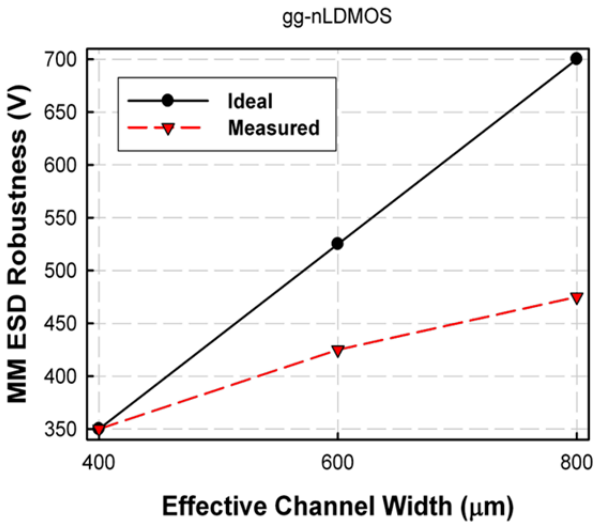


Fig. 1.5. Measured MM ESD protection levels of nLDMOS with different effective channel widths.

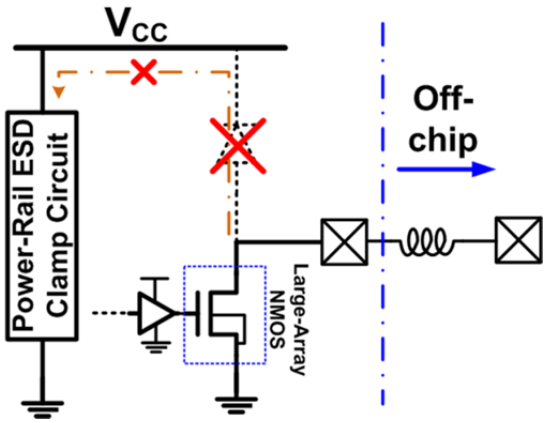


Fig. 1.6. ESD current discharging path in an open drain structure. Without a forward diode from the pad to the HV V_{CC} power supply line, power-rail ESD clamp circuit does not help discharge ESD current.

Besides the general expectation of a robust electronic system (superior IC reliability), cost is another practical consideration for IC design companies. Cost reduction without downgrading the reliability specification is common to IC industries. Since silicide blocking is dedicated for the purpose of ESD protection, fully-silicided design is straightforward to the cost reduction of silicon chips. To have a fully-silicided design with high ESD robustness, novel design techniques have been being requested by the IC industries and the design challenge is stringent.

1.3. Dissertation Organization

With the above-mentioned ESD design challenges, IC industries are eager to have robust ESD protection solutions so as to enhance product yields and stability. This dissertation accordingly focuses on the improvement techniques to HV MOSFETs' ESD protection levels. Several new design concepts and practical ESD design solutions that have been realized in commercial IC products are proposed in this dissertation. This dissertation consists of 8 chapters. With the HV N-Well that encloses the nLDMOS, the substrate-triggered technique which is well-known in low-voltage logic technologies is not applicable in the traditional layout method of HV transistors. To alleviate the non-uniform triggering among nLDMOS, a new waffle layout method enabling the body current injection is proposed in chapter 2.

In chapter 3, the safe operating area (SOA) which defines the I-V switching boundaries of a HV transistor is reviewed. SOA characterization methods and improvement methods are discussed in this chapter. The SOA discussion is related to the electrical SOA improvement method in chapter 4 that solves the degraded SOA of an nLDMOS when a silicon controlled rectifier (SCR) is integrated for ESD purposes.

In chapters 5 and 6, there are two fully-silicided ESD solutions that have been implemented on commercial IC products. Designs in chapter 5 enhance ESD protection level

through layout method and are universal to IC products with push-pull output drivers. In chapter 6, the design is specially devised for voltage programming pins that have the fail-safe requirement so as to prevent leakage current when programming internal memories. The ESD design also prevents the latchup-like problem when the programming signal has a fast voltage rise time.

A study to the holding voltage of nLDMOS is included in chapter 7. Holding voltage is a key design consideration for developing high latchup-resistant ESD protection elements. A gradually decreased transistor holding voltage is observed and analyzed by using long-pulse transmission line pulsing (TLP) system [2]. This phenomenon has a negative impact to IC latchup and hence leads to new latchup design considerations.

Chapter 8 summarizes the results of this dissertation and its contribution to future reliability researches. To sum up, this dissertation includes not only new and useful academia ESD research results, but also practical ESD design solutions to the IC industries.

Chapter 2

Waffle Layout Structure With Body-Injected Technology in BCD High-Voltage Processes

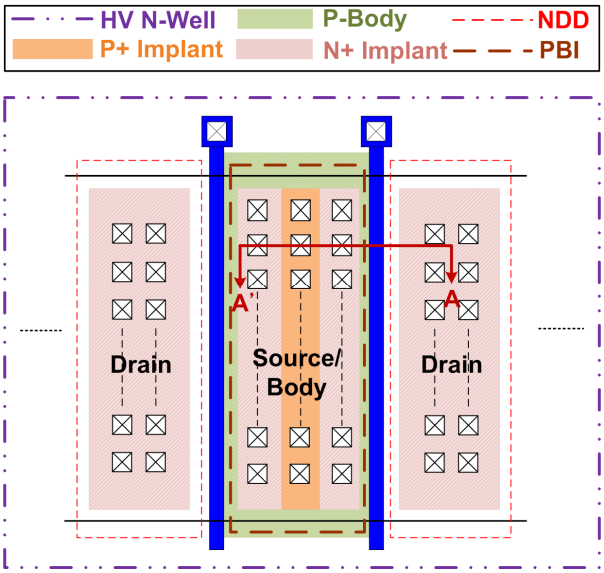
2.1. Background

With the thriving applications in silicon ICs, the demands of HV ICs are increasing rapidly [8]. In HV ICs, the power supply voltage (V_{CC}) is often over ten volts or even higher. To fabricate devices to sustain such a high operating voltage, not only the process complexity is increased but also the difficulty to guarantee the reliability of HV devices. ESD is an important and inevitable event ICs during fabrication, packaging, and assembling processes [9]–[12]. ESD protection in HV technology is challenging and has received a lot of attention recently [13]–[16].

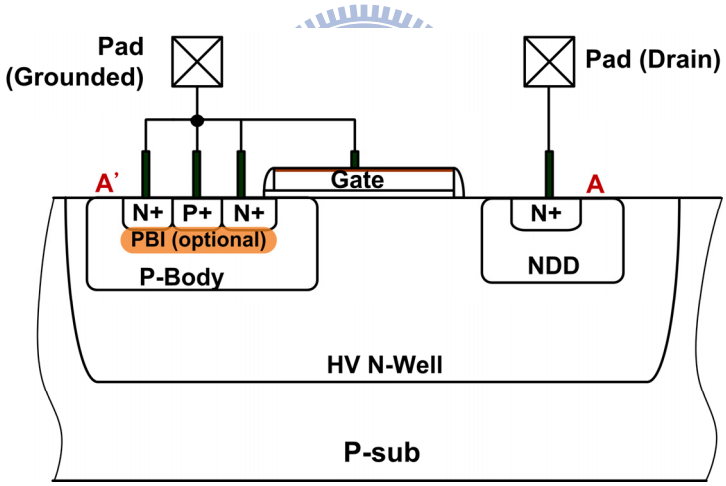
To improve the ESD robustness of HV NMOS, several techniques related to process modifications have been reported [16]–[20]. The method of inserting N+ buried layer (NBL) has been used to enhance the ESD robustness of nLDMOS [16]. However, additional process steps and mask layers are needed. Besides, a heavily doped P-type body implantation has been used to avoid the non-uniform triggering of parasitic NPN bipolar junction transistors (BJTs) when a HV NMOS is drawn with large array, *i.e.* large device dimensions (W/L) [20].

In this chapter, the influence of highly doped P-type boron implantation (PBI) layer to the ESD robustness of nLDMOS is first investigated. The nLDMOS was designed to discharge ESD current through the parasitic BJT inherent in the nLDMOS. A circuit and layout co-design method is then proposed to improve ESD robustness of the nLDMOS [21], [22]. The proposed method exploits the body current injection to improve turn-on uniformity of nLDMOS devices during ESD stresses. Therefore, it does not require process modifications or additional mask layers. The proposed method was verified in a 0.5-μm 16-V and a

0.35-μm 24-V bipolar CMOS DMOS (BCD) process.



(a)



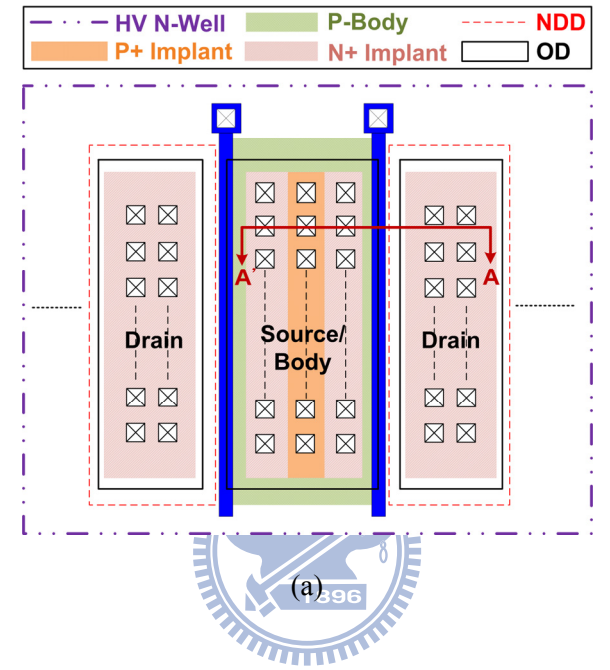
(b)

Fig. 2.1. (a) Layout diagram and the (b) device cross-sectional view along A-A' line of an nLDMOS in a 0.5-μm 16-V BCD process with the optional PBI layer.

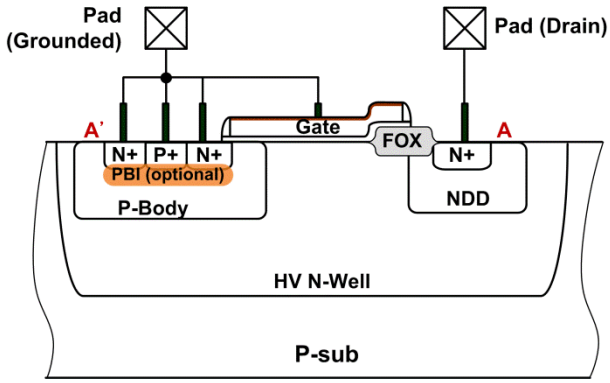
2.2. Effect of P-type Boron Implantation on ESD Performance of High-Voltage nLDMOS

Fig. 2.1(a) shows the traditional (stripe) layout diagram of an nLDMOS in the 0.5-μm 16-V BCD process. The nLDMOS in the 0.5-μm 16-V BCD process is defined within one

single OD region, so that the gap between N+ drain and the poly gate is the active area. Device cross-sectional view of the 16-V nLDMOS along A-A' line in Fig. 2.1(a) is shown in Fig. 2.1(b). A PBI layer is optionally implanted underneath the source N+ and P+ regions in the 16-V nLDMOS to investigate its effectiveness on ESD robustness.



(a)



(b)

Fig. 2.2. (a) Layout diagram and the (b) device cross-sectional view along A-A' line of the nLDMOS in a 0.35-μm 24-V BCD process.

For nLDMOS in the 0.35-μm 24-V BCD process, drain and source/body regions are defined in different active areas, as shown in Fig. 2.2(a). The gap between N+ drain and poly gate of the nLDMOS device is a field oxide (FOX) region. Device cross-sectional view along

A-A' line of the 24-V nLDMOS in Fig. 2.2(a) is shown in Fig. 2.2(b). The FOX gap of the 24-V nLDMOS can avoid the field crowding near the drain of nLDMOS, which, in turn, helps the nLDMOS to sustain the high operating voltage of 24 V. In both 16 and 24 V technologies, the nLDMOS devices are surrounded by HV N-Well [23]; P-Body regions in an nLDMOS are fully separated from the common p-type substrate (P-sub). P+ body pick up at every source region is required to bias the P-Body. Channel lengths are defined by the overlapped region of P-Body and the poly gate.

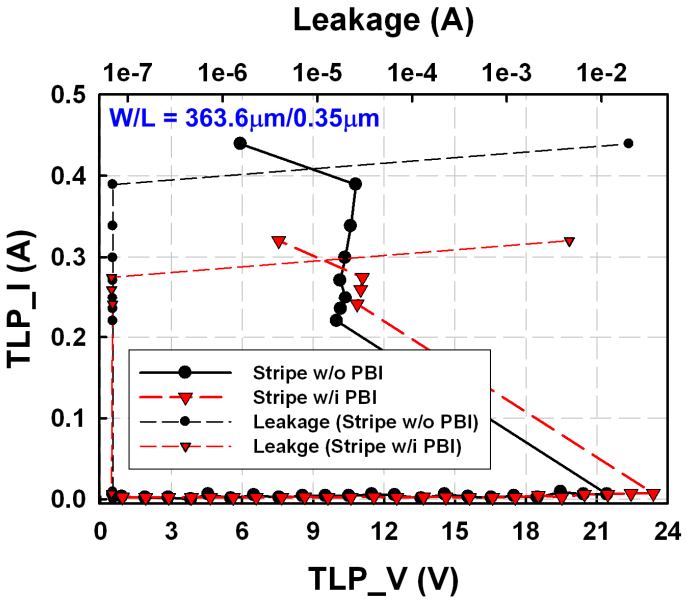


Fig. 2.3. TLP-measured I-V characteristics of gate-grounded 16-V nLDMOS devices with or without the PBI layer.

To analyze characteristics of devices under HBM ESD stresses, TLP system with 100-ns pulse width has been commonly adopted [24], and Fig. 2.3 shows the TLP-measured I-V characteristics of the 16-V nLDMOS with traditional (stripe) layout style. Both 16-V nLDMOS with and without PBI layer in Fig. 2.3 have the same device dimension (W/L) of 363.6 μm/0.35 μm with each finger width of 45.45 μm. From the TLP measurement results, the bipolar trigger voltage (V_{t1}) of the gate-grounded 16-V nLDMOS without PBI

implantation is 21.4 V. With the heavily doped PBI to reduce the parasitic P-Body resistance, V_{t1} of the gate-grounded 16-V nLDMOS is increased to 23.4 V. Because the bipolar beta gain in the nLDMOS is also suppressed by the PBI layer, holding voltage of the first snapback is slightly increased from 10 to 10.86 V. However, the secondary breakdown current (I_{t2}) of the 16-V nLDMOS was found to be degraded from 0.39 to 0.28 A due to the PBI layer.

To explain the degradation on ESD robustness of nLDMOS with PBI, the typical I-V characteristic of a gate-grounded NMOS (ggNMOS) during ESD stresses is depicted in Fig. 2.4. When the voltage across the ggNMOS is higher than the reverse drain/body junction breakdown voltage, drain current of the ggNMOS starts to increase due to the avalanche generation. The junction breakdown (V_{AV}) is typically defined as the voltage corresponding to a 1-μA current level of the ggNMOS. Before the avalanche generation current is large enough to forward bias the parasitic body/source junction diode, the ggNMOS acts as a reverse-biased PN junction (HV N-Well/P-Body in Fig. 2.2(b)). Therefore, the voltage keeps increasing without snapback. When the avalanche-generated holes forward bias the body/source junction diode, NPN BJT is turned on to initiate snapback. Due to the turn-on operation of BJT inherent in the ggNMOS, the voltage across the ggNMOS is clamped down to the holding region. The maximum reverse diode current before the snapback of ggNMOS is defined as I_{t1}. For devices with large-array design, the effective device width (W) is usually higher than several thousands of micrometers in order to have high driving capability or low turn-on resistance in specified applications. With a large effective device width, considerable I_{t1} can flow through large-array devices before the BJT triggers. Due to the area consideration, large array devices are not drawn with ESD design rules and non-uniform triggering among BJT inherent in the large-array device is serious. Consequently, triggering of BJT often induces devastating results to large-array devices [20]. Triggering of BJT has also been reported as the cause of ESD failures in HV power-rail ESD clamp circuits that utilize big field-effect transistors (BigFETs) [25].

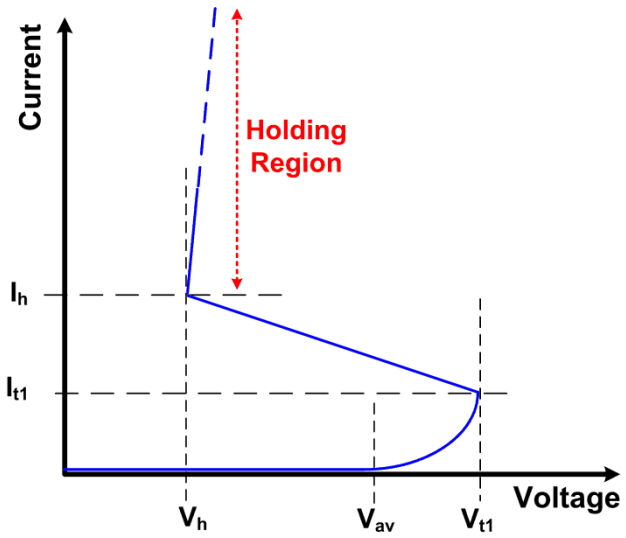


Fig. 2.4. The typical I-V characteristic of a gate-grounded NMOS under ESD stresses.

For the 16-V nLDMOS, the heavily doped PBI reduces the effective resistance of P-Body (R_{body}); I_{t1} of nLDMOS is increased because turn on of BJT requires ($I_{t1} \times R_{body}$) ≥ V_{tdiode}, where V_{tdiode} is the voltage to forward bias the P-Body/N+ junction diode. Due to the fact that considerable I_{t1} can flow through large-array nLDMOS where BJT triggering is devastating, the additional P-type body implantation is beneficial to the ESD robustness of stand-alone large-array nLDMOS. ESD energy is mainly discharged through the reverse diode current (I_{t1}) of the large-array nLDMOS. However, without snapback to clamp down the voltage, large-array nLDMOS is not suitable to protect internal circuits.

For ESD protection nLDMOS devices that are not large-array devices, they usually rely on the turn-on operation of BJT to clamp down ESD voltages to their holding regions and to protect the gate oxide of internal circuits. They are therefore drawn with ESD design rules and the overall effective gate widths are much smaller compared to those of large-array nLDMOS devices. These devices exhibit low I_{t1} because the high current density (I_{t1}/W) makes the P-Body/N+ diode easily forward biased under ESD stresses. As a result, the effect of PBI on increasing I_{t1} is negligible. As shown in Fig. 2.3, both 16-V nLDMOS with and

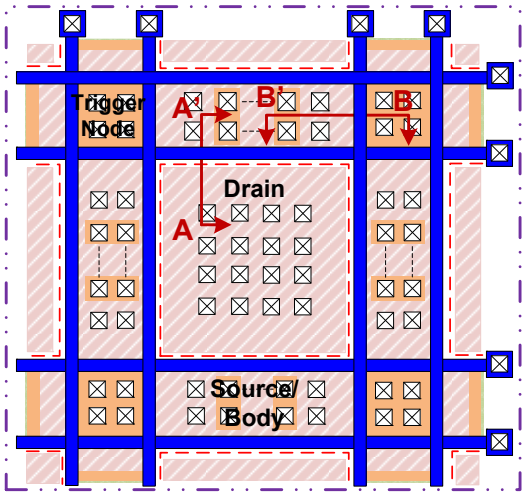
without PBI implantation exhibit low I_{t1} current. Furthermore, the magnitude of I_{t1} is not critical for a non-large-array ESD protection nLDMOS. With the bipolar beta gain being suppressed, the measured I_{t2} of nLDMOS was found to be degraded by PBI.

2.3. New Waffle Layout Structure for ESD Improvement

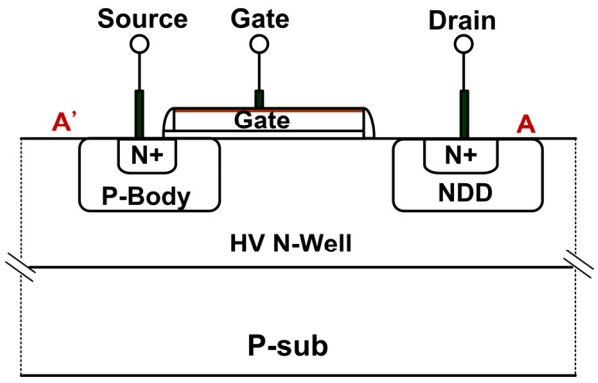
From the measurement results in Fig. 2.3, it is known that the PBI layer degrades ESD robustness of nLDMOS when the nLDMOS device relies on the parasitic BJT to discharge ESD energies. Because the available process modification from foundry is not effective in improving ESD robustness of snapback-based nLDMOS, a layout technique without additional mask or process step is proposed.

In low-voltage (LV) CMOS technologies, one of the most effective methods to increase ESD robustness is the substrate-triggered / substrate-pump technique [26]-[31]. To inject the substrate-triggered current into the base of the parasitic NPN BJT inherent in a LV NMOS, a P+ trigger node was placed at drain and connected to the trigger circuit [27]. However, in HV nLDMOS, the base of its parasitic NPN BJT is surrounded by the HV N-Well. The traditional layout method to inject the substrate-triggered current in LV technologies hence cannot be implemented in HV BCD processes.

To effectively inject the trigger current into the P-Body (the base of NPN BJT), nLDMOS realized in waffle layout style is proposed. Fig. 2.5(a) shows the layout diagram of nLDMOS with the waffle layout style (waffle nLDMOS). In the waffle nLDMOS, the drain of nLDMOS is drawn in a square. Source and body of the waffle nLDMOS are laid out at four sides of the drain square. Such a waffle layout style leads to four squares (Trigger Nodes) at the diagonal corner of a drain square. Both the P-Body regions in the two studied BCD processes are implanted before the formation of gate oxide; therefore the four squares at the diagonal corner of drain are shorted to the body pick up at source/body region. Device cross-sectional views along A-A' and B-B' lines of Fig. 2.5(a) are shown in Fig. 2.5(b) and



(a)



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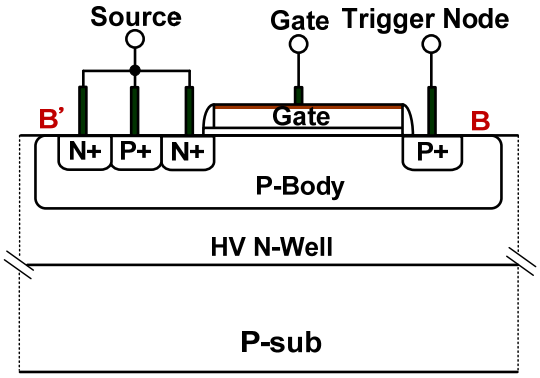


(c)

Fig. 2.5. (a) Layout top view, (b) device cross-sectional view along A-A', and (c) device cross-sectional view along B-B', of an nLDMOS with the proposed waffle layout style in the 0.5-μm 16-V BCD process.

2.5(c), respectively. By using the waffle layout, the body current can be injected from trigger nodes and be collected by the grounded P+ pick up at the source/body. The injected body current acts as the base current to turn on the parasitic NPN BJT. The P+ contacts at source/body in the waffle layout can ensure the grounded body potential during normal circuit operation. Trigger nodes of the waffle nLDMOS are dynamically biased through the circuit co-design method. A trigger circuit is designed to distinguish normal circuit operating and ESD stress conditions [6]. During normal circuit operating conditions, the trigger circuit biases the trigger nodes of the waffle nLDMOS at ground. During ESD stress conditions, the trigger circuit provides the required body injection current to enhance the turn-on uniformity of the waffle nLDMOS.

2.3.1. In the 0.5-μm 16-V BCD Process

To verify the ability to turn on the parasitic NPN BJT, a stand-alone waffle nLDMOS with its trigger nodes connected to a bonding pad was injected with different levels of DC body current (I_B) through its trigger nodes. Measurement setup is shown in the inset of Fig. 2.6, where the R_{Body} denotes the equivalent resistance of P-Body from the trigger nodes to the P+ body pick-ups. With the larger injected I_B current, the nLDMOS exhibited the higher collector current I_C. This result shows the parasitic NPN BJT can be successfully triggered on through the body current injection.

To provide the body current during ESD stresses, a trigger circuit composed of a RC distinguisher and a HV inverter was fabricated on-chip. Because the ESD voltage transition has a rise time in the order of nanoseconds but normal circuit power-on transition is in the order of milliseconds, they can be distinguished through a proper design of the RC distinguisher. Corresponding measurement setup to verify the stand-alone trigger circuit is shown in the inset of Fig. 2.7. During the verification measurement, output of the stand-alone trigger circuit was externally short to the trigger nodes of a stand-alone 16-V waffle

nLDMOS. Fig. 2.7 shows that the trigger circuit can provide a peak trigger current ($I_{Trigger}$) of 25 mA to the trigger nodes of the stand-alone waffle nLDMOS when a 20-V voltage pulse with 10-ns rise time (t_r) and 1-μs pulse width (t_{pw}) was applied. After 200 ns, $I_{Trigger}$ fades to 0 mA because of the RC distinguisher.

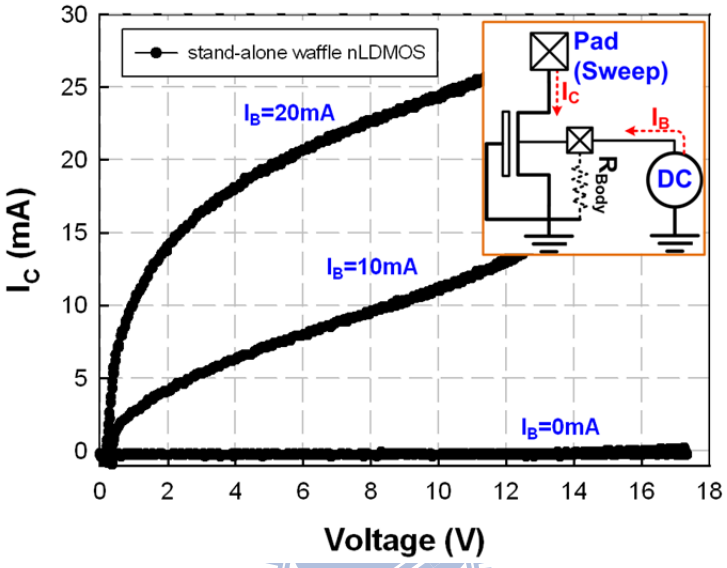


Fig. 2.6. Turn-on verification of the stand-alone 16-V nLDMOS drawn in waffle style with DC body current (I_B) injected from the trigger nodes.

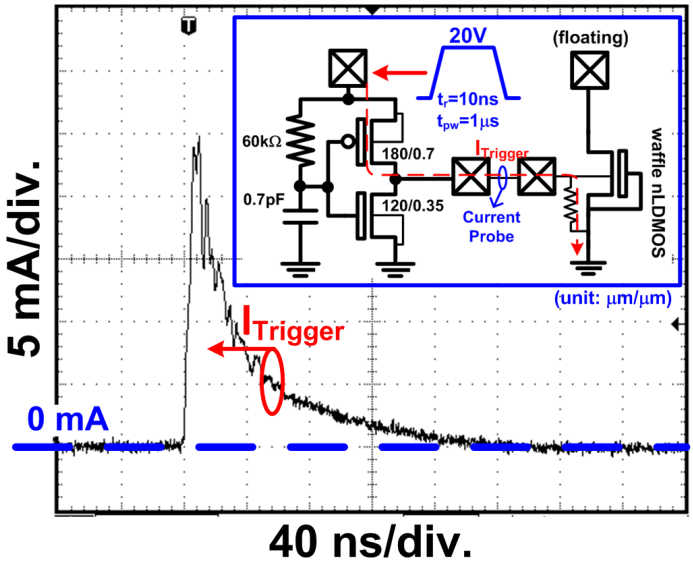


Fig. 2.7. Turn-on verification of the stand-alone trigger circuit in the 0.5-μm 16-V BCD process. The measurement setup is shown in the inset of this figure.

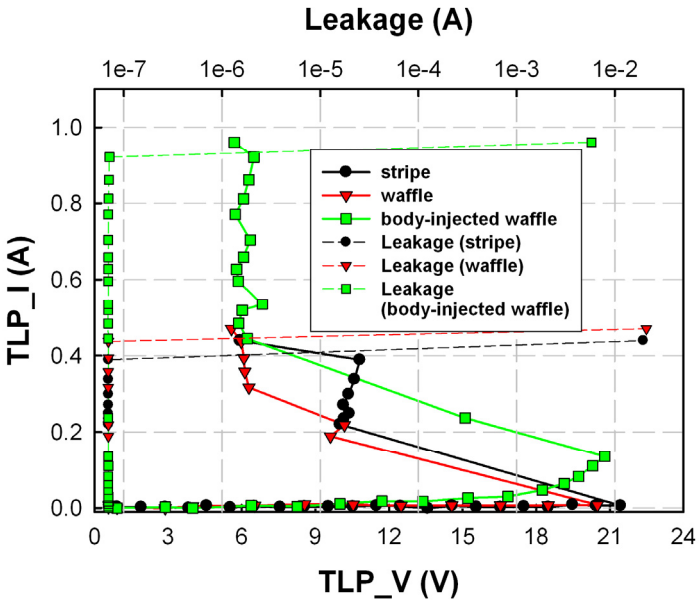


Fig. 2.8. The 100-ns TLP-measured I-V curves of 16-V nLDMOS with stripe, waffle, and body-injected waffle layout style.

The 100-ns TLP-measured I-V curves among the stand-alone stripe, stand-alone waffle, and body-injected waffle nLDMOS devices are shown in Fig. 2.8. The stripe nLDMOS in Fig. 2.8 has the layout style of Fig. 2.1(a). The waffle nLDMOS in Fig. 2.8 has the layout style of Fig. 2.5(a), and the trigger nodes of the waffle nLDMOS are short to source internally. The body-injected waffle nLDMOS in Fig. 2.8 has the layout style as that shown in Fig. 2.5(a), and the trigger nodes in the body-injected waffle nLDMOS were connected internally to the trigger circuit through metal interconnection. The trigger circuit has the same design parameters to the one verified in Fig. 2.7. These three nLDMOS have the same device dimension of 363.6 μm/0.35 μm in layout. Failure criterion is the same to all devices, 1-μA leakage current under 16-V drain bias voltage. Measured results show that the stripe and the waffle nLDMOS have roughly the same secondary breakdown current (I_{t2}) of 0.39 and 0.41 A, respectively, if the body current injection was not applied. By applying the body current injection, I_{t2} of the waffle nLDMOS can be significantly increased from 0.41 to 0.95 A. From

the 100-ns TLP measurement, a more than 2X increase on I_{t2} has been achieved through the waffle layout style and the body current injection. Measured HBM ESD robustness for stand-alone stripe, stand-alone waffle, and body-injected waffle nLDMOS devices are 0.75, 0.75, and 1.25 kV, respectively.

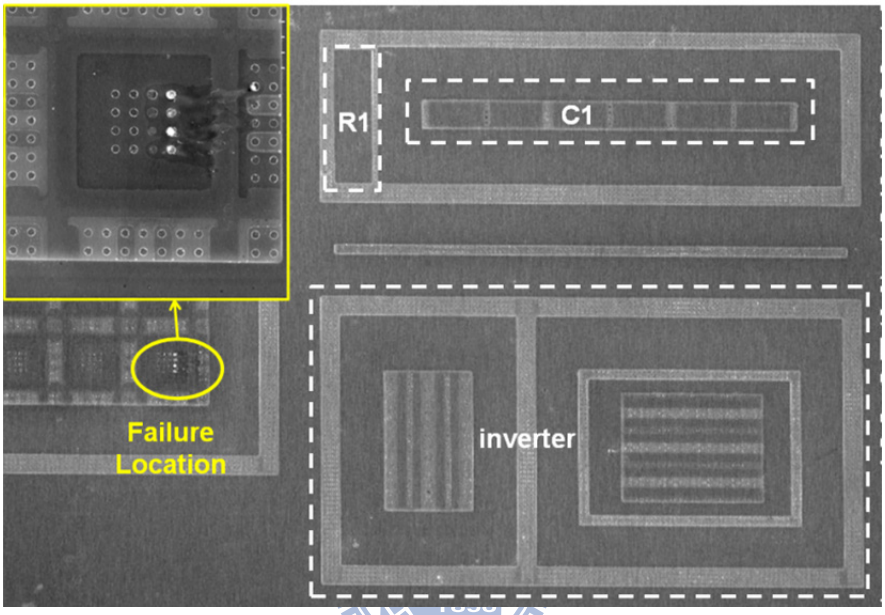


Fig. 2.9. Scanning electron microscope (SEM) image of the body-injected waffle nLDMOS after 100-ns TLP measurement.

Scanning electron microscope (SEM) image of the body-injected waffle nLDMOS after 100-ns TLP measurement is shown in Fig. 2.9. The failure location of the body-injected waffle nLDMOS was found on the drain of nLDMOS. This result shows that the ESD current is mainly discharged by the nLDMOS instead of the trigger circuit, and confirms the improvement on ESD robustness from the waffle layout and the body current injection.

2.3.2. In the 0.35-μm 24-V BCD Process

In the 0.5-μm 16-V BCD process, substantial improvement on the ESD robustness of nLDMOS has been achieved by using the waffle layout style along with the trigger circuit to provide body current injection. To study the width scaling to the ESD protection level of

nLDMOS, the circuit and layout co-design technique was fulfilled in a 0.35-μm 24-V BCD process.

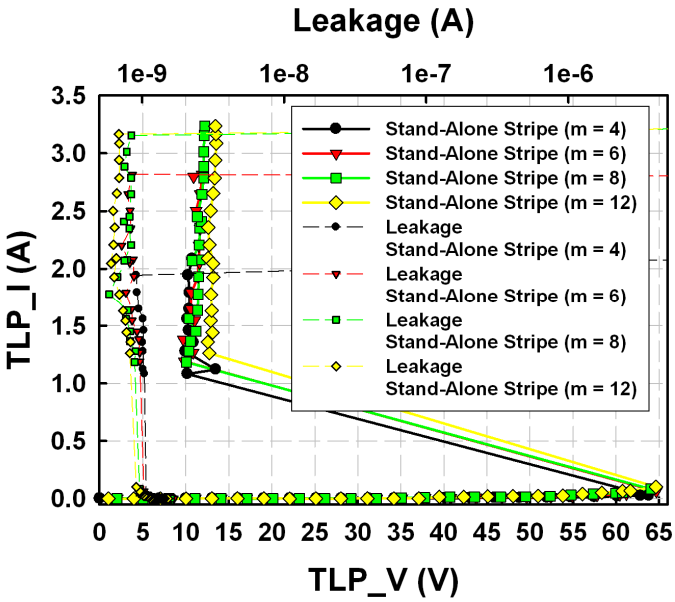


Fig. 2.10. TLP-measured I-V characteristics of stand-alone 24-V nLDMOS in stripe layout style. Dimension for each finger of the stripe nLDMOS is 73.2 μm/0.75 μm.

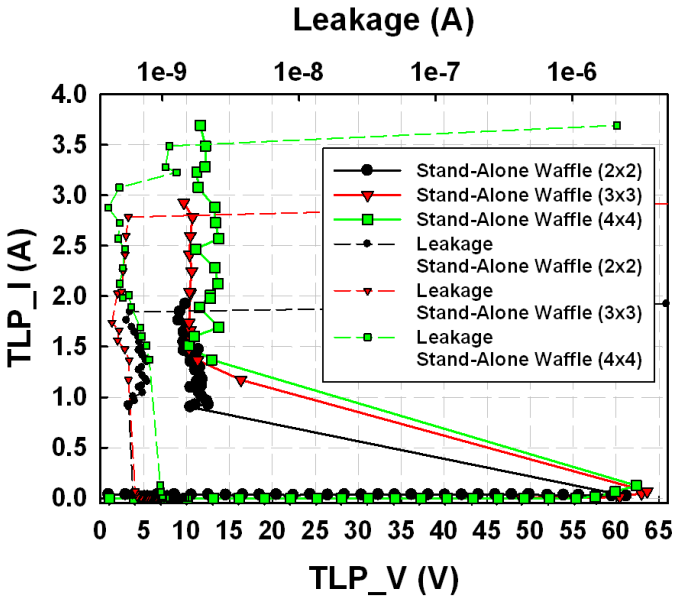
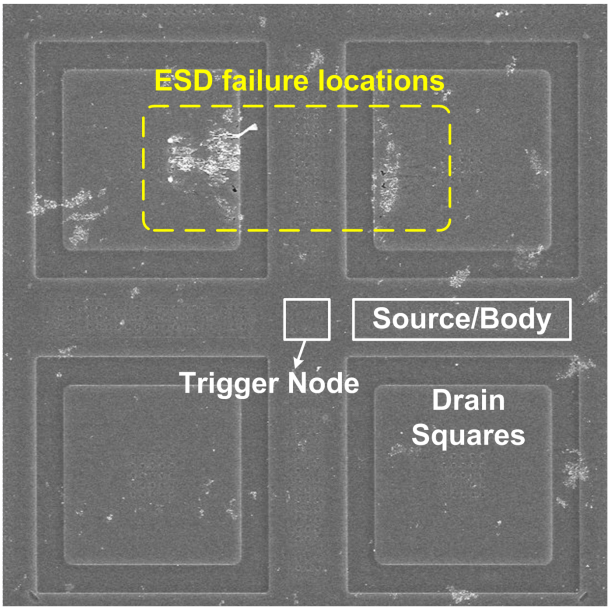
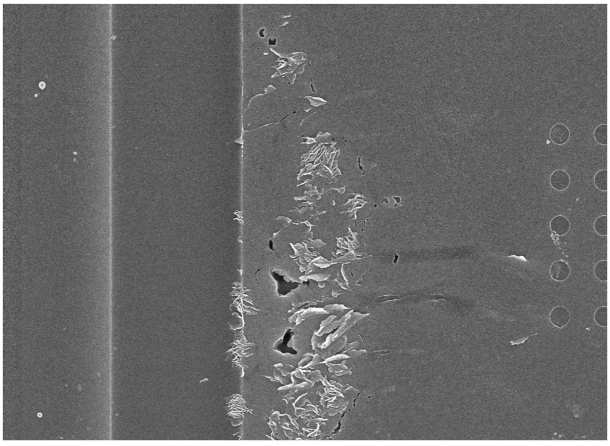


Fig. 2.11. TLP-measured I-V characteristics of stand-alone 24-V nLDMOS in waffle layout style. Dimension for each drain square of the waffle nLDMOS is 73.2 μm/0.75 μm.



(a)



(b)

Fig. 2.12. (a) SEM image of the stand-alone 24-V waffle nLDMOS with 2×2 drain squares after 100-ns TLP measurement and (b) the enlarged image of ESD the failure locations.

TLP-measured I-V characteristics of stand-alone stripe nLDMOS and stand-alone waffle nLDMOS in the 0.35-μm 24-V BCD process are shown in Fig. 2.10 and 2.11, respectively. The measured I_{t2} for stand-alone stripe nLDMOS with 4, 6, 8, and 12 fingers are 1.94, 2.81, 3.15, and 3.16 A, respectively. Each finger of the 24-V stripe nLDMOS is 73.2 μm/0.75 μm. For stand-alone waffle nLDMOS with 2×2, 3×3, and 4×4 drain squares, the measured I_{t2} are 1.8, 2.78, and 3.49 A, respectively. Each drain square of the 24-V waffle nLDMOS is also

73.2 μm/0.75 μm. From the TLP measurement results, non-linear scaling of ESD robustness to the device width was observed on both stand-alone waffle and stand-alone stripe nLDMOS. SEM image of the stand-alone 2×2 waffle nLDMOS after TLP measurement is shown in Fig. 2.12(a). ESD failures were found only on two drain squares of the 2×2 stand-alone waffle nLDMOS. Furthermore, the enlarged image of the ESD failure locations in Fig. 2.12(a) is shown in Fig. 2.12(b). Surface current filamentation are observed in Fig. 2.12(b), which implies a superficial current discharging of the stand-alone nLDMOS devices during ESD stresses.

In the 0.35-μm 24-V BCD process, ESD detection circuit was also composed of a RC distinguisher and a HV inverter. A stand-alone trigger circuit was fabricated on-chip to verify the driving capability of the trigger circuit, as shown in Fig. 2.13. Corresponding measurement setup and device dimensions of the HV inverter are shown in the inset of Fig. 2.13. Output of the stand-alone trigger circuit was externally short to trigger nodes of a stand-alone waffle nLDMOS. A voltage pulse with 10-ns t_r and 1-μs t_{pw} was given into the stand-alone trigger circuit. Measurement result showed a peak $I_{Trigger}$ of 50 mA into the trigger nodes of the waffle nLDMOS.

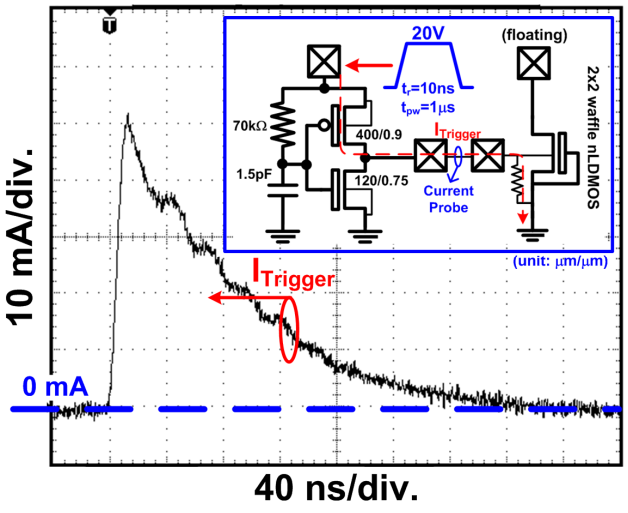


Fig. 2.13. Turn-on verification of the stand-alone trigger circuit in the 0.35-μm 24-V BCD process. The measurement setup is shown in the inset of this figure.

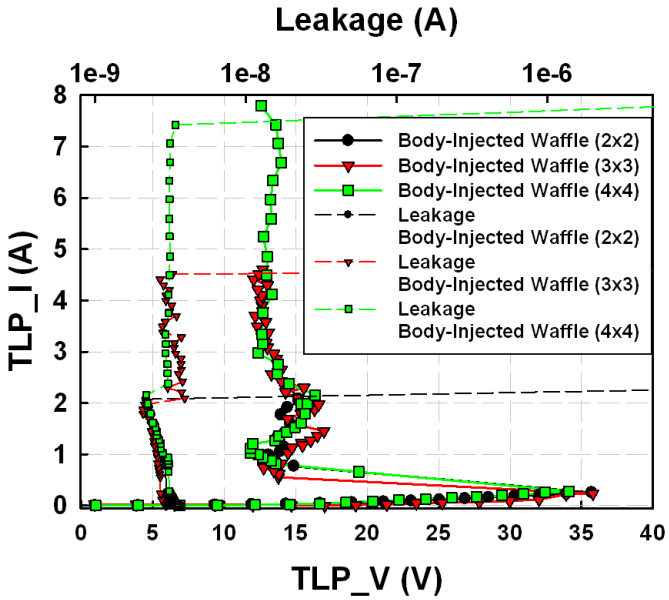


Fig. 2.14. TLP-measured I-V characteristics of body-injected 24-V nLDMOS with waffle layout style.

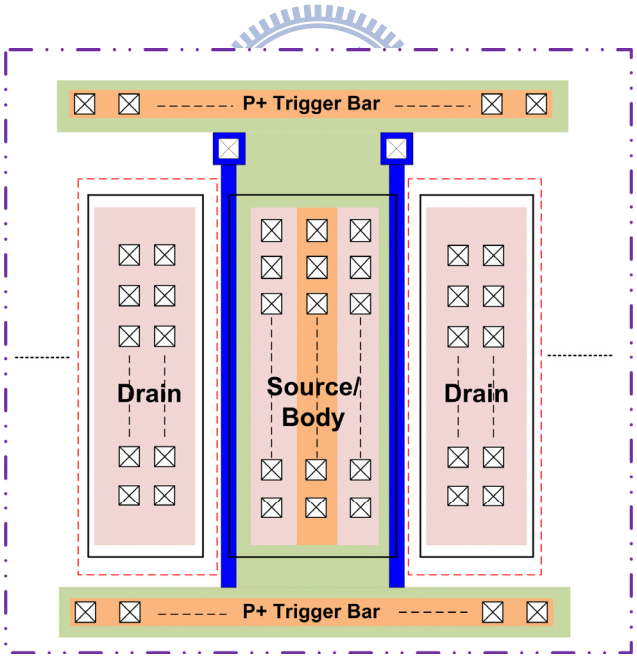


Fig. 2.15. Layout diagram of the 24-V stripe nLDMOS with additional P+ trigger bars at upper and bottom of the device for body current injection.

With the body current injection, TLP-measured I-V characteristics for body-injected waffle nLDMOS are shown in Fig. 2.14. TLP-measured I_{t2} for body-injected waffle nLDMOS with 2×2, 3×3, and 4×4 drain squares are 2.07, 4.41, and 7.42 A, respectively. Besides the

body-injected waffle nLDMOS, the body current injection method was managed to be implemented on the nLDMOS with stripe layout style. As the layout diagram shown in Fig. 2.15, two P+ trigger bars were drawn at two sides of the 24-V nLDMOS with the stripe layout style. Output of trigger circuit was connected internally to these two P+ trigger bars, and these two P+ trigger bars were electrically short to ground through P+ source and the P-Body.

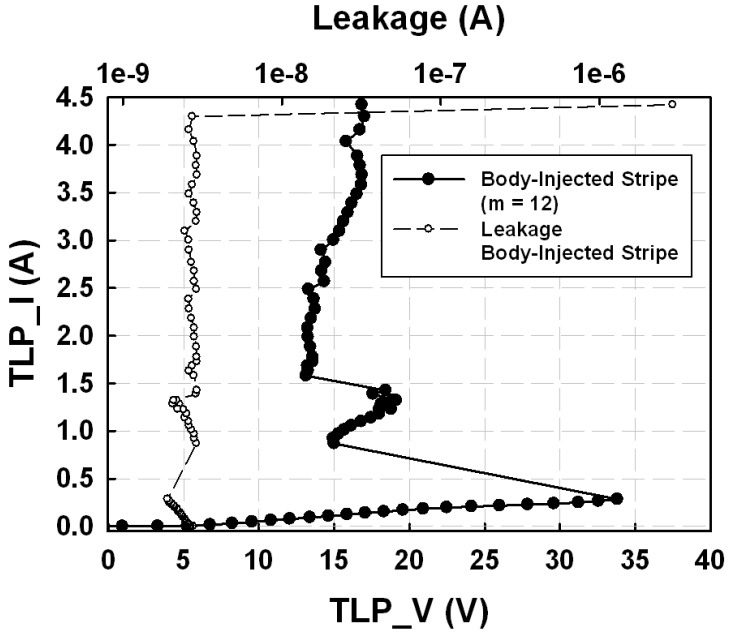


Fig. 2.16. TLP-measured I-V characteristics of body-injected 24-V nLDMOS in stripe layout style.

For body-injected stripe nLDMOS, the studied device has 12 fingers with each finger width of 73.2 μm/0.75 μm. TLP-measured I-V characteristic for the body-injected stripe nLDMOS is shown in Fig. 2.16. Compare to the stand-alone stripe nLDMOS with 12 fingers, the measured I_{t2} is increased from 3.16 to 4.2 A by using the body current injection.

To compare the ESD performances between different types of nLDMOS, TLP-measured I_{t2} values are normalized to corresponding effective device widths (W) as shown in Fig. 2.17. For stand-alone nLDMOS devices, a slightly higher normalized I_{t2} is found on the stripe nLDMOS when the number of finger is 4. With the increasing number of fingers, normalized

I_{t2} for stand-alone stripe nLDMOS is found to degrade more rapidly than that for stand-alone waffle nLDMOS. For stripe nLDMOS devices, fingers were drawn in parallel. For waffle nLDMOS devices, drain squares were expanded both horizontally and vertically. As a result, horizontal layout width of stripe nLDMOS is larger than that of waffle nLDMOS. For example, the layout width for the stripe nLDMOS with 12 fingers is 180.2 μm; the layout width for the waffle nLDMOS with 4x4 drain squares is 136.5 μm. Because bonding pads were in the middle of the DUTs, stripe nLDMOS has a higher mismatch of parasitic metal resistance from the bonding pad to each finger of the nLDMOS. Accordingly, the stand-alone stripe structure shown in Fig. 2.17 shows a severer degradation rate on the normalized I_{t2} values as compared to the stand-alone waffle structure [20].

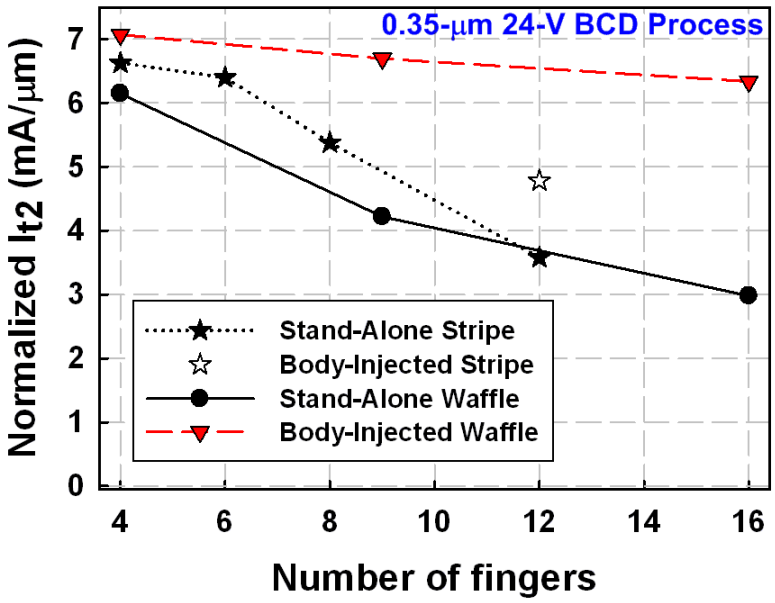


Fig. 2.17. Normalized I_{t2} current among different types and fingers of 24-V nLDMOS.

With the body current injection, stripe nLDMOS with P+ trigger bars was found to have normalized I_{t2} lie in between stand-alone nLDMOS devices and body-injected waffle nLDMOS. SEM image of the body-injected stripe nLDMOS with P+ trigger bars after TLP measurement is shown in Fig. 2.18. From the SEM image, contact spiking was observed in

every finger of the body-injected stripe nLDMOS. However, contact spiking was found only on drain regions near the two P+ trigger bars. No ESD failure was observed in the center portion of the stripe nLDMOS with body current injection. Because the body current was injected from the two P+ trigger bars which was grounded by the P+ body contacts at source side, parasitic BJTs closer to the P+ trigger bars have smaller parasitic P-Body resistance from the P+ trigger bars to the grounded P+ body contacts. As a result, parasitic BJTs closer to the P+ trigger bars receive higher body injection current during ESD stresses. This inhomogeneous body current distribution leads to the result that ESD failures were found to localize on the drain contacts close to the two P+ trigger bars. For nLDMOS devices in waffle layout style, because the side width of each drain square is 18.3 μm (much shorter than the 73.2-μm finger width of the body-injected stripe nLDMOS), they were less impacted by the inhomogeneous body current distribution. Body-injected waffle nLDMOS thereby performed higher normalized I_{t2} than that of body-injected stripe nLDMOS.

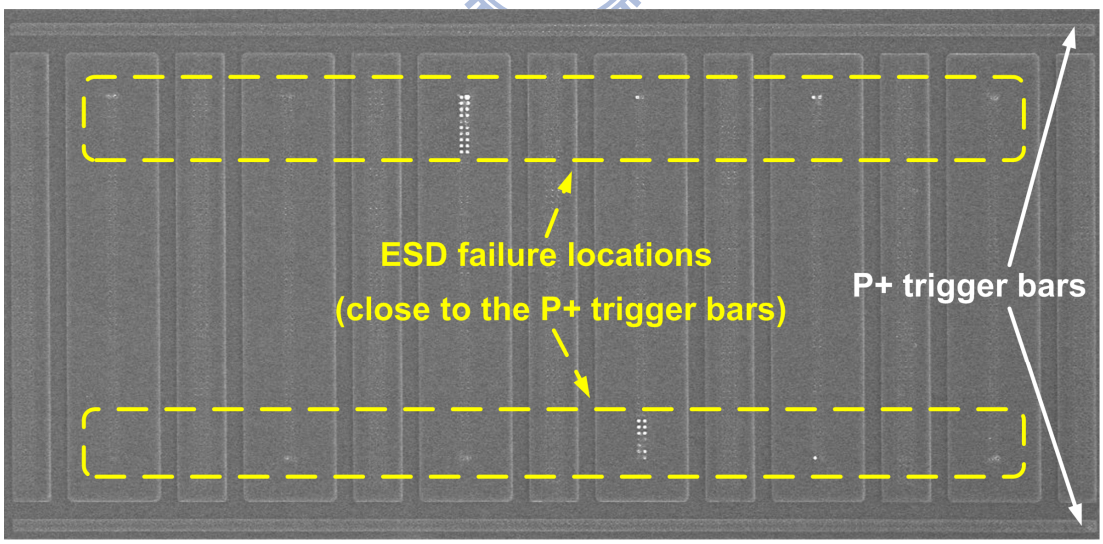


Fig. 2.18. SEM image of the body-injected 24-V nLDMOS with stripe layout style after 100-ns TLP measurement.

From the normalized I_{t2} among different types of nLDMOS devices shown in Fig. 2.17, non-uniform triggering was found to be substantially alleviated by using the waffle layout

style and the body current injection. Body-injected waffle nLDMOS therefore exhibits the highest normalized I_{t2} among different types of nLDMOS shown in Fig. 2.17. Optical beam induced resistance change (OBIRCH) and SEM images of the body-injected waffle nLDMOS with 4×4 drain squares after TLP measurement are shown in Fig. 2.19. OBIRCH analysis shows uniform ESD failure locations on the waffle nLDMOS instead of the trigger circuit, which implies that ESD current is properly discharged through the ESD protection nLDMOS. With ESD failures spreading on every drain square of the 4×4 waffle nLDMOS, SEM image further confirms that uniform triggering of nLDMOS is successfully achieved by using the body current injection. From the TLP measurement results and failure analyses, the effectiveness of body current injection on improving ESD robustness of HV nLDMOS has been verified. ESD robustness of nLDMOS devices studied in this chapter is summarized in Table 2.1.

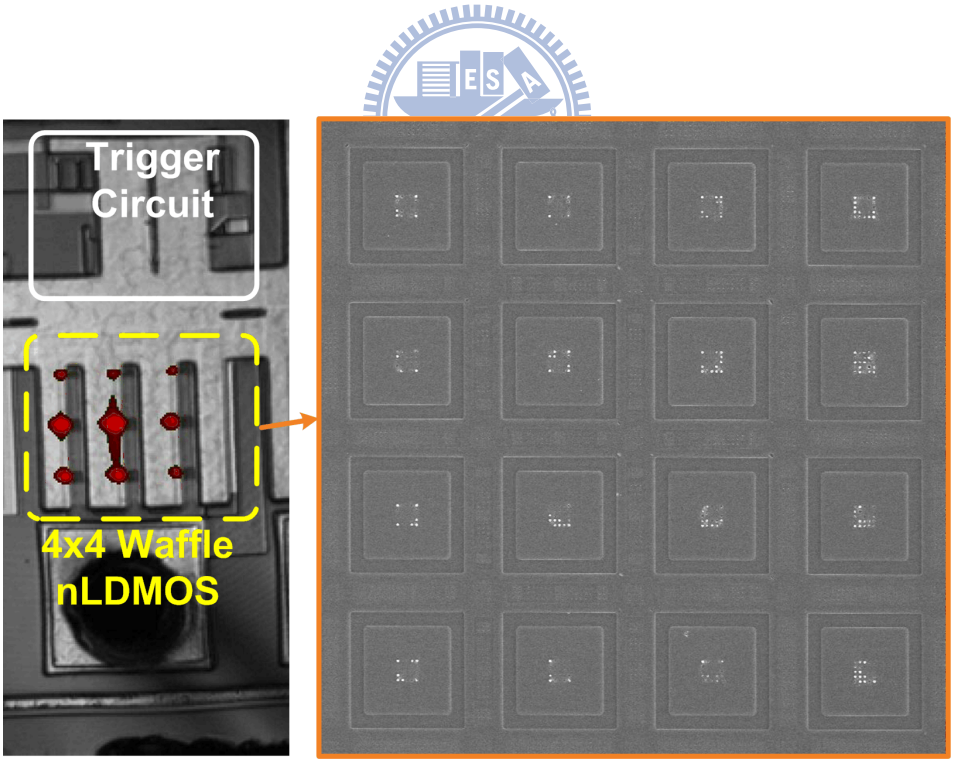


Fig. 2.19. OBIRCH and SEM images of the body-injected 24-V nLDMOS with waffle layout style after 100-ns TLP measurement.

TABLE 2.1

ESD ROBUSTNESS OF NLDMOS DEVICES

		W/L (μm/μm)	I_{t2} (A)	HBM (kV)
16-V nLDMOS	Stand-Alone Stripe	(45.45/0.35) x 8	0.39	0.75
	Stand-Alone Waffle	(40.4/0.35) x 9	0.41	0.75
	Body-Injected Waffle		0.95	1.25
24-V nLDMOS	Stand-Alone Stripe	(73.2/0.75) x 4	1.94	3.5
		(73.2/0.75) x 6	2.81	4
		(73.2/0.75) x 8	3.15	5
		(73.2/0.75) x 12	3.16	5.5
	Body-Injected Stripe	(73.2/0.75) x 12	4.2	7
	Stand-Alone Waffle	(73.2/0.75) x 4	1.8	3
		(73.2/0.75) x 9	2.78	4.5
		(73.2/0.75) x 16	3.49	6.5
	Body-Injected Waffle	(73.2/0.75) x 4	2.07	4
		(73.2/0.75) x 9	4.41	7
		(73.2/0.75) x 16	7.42	>8

2.4. Summary

nLDMOS transistors in HV technologies are known to have poor ESD robustness. Additional P-type boron implantation was found to degrade ESD robustness of snapback-based nLDMOS. Through the collaboration of the proposed waffle layout style and the ESD trigger circuit, the body-injected technique was fulfilled in a 0.5-μm 16-V and a 0.35-μm 24-V BCD process. The 100-ns TLP measurement results showed substantially improved I_{t2} on waffle nLDMOS. Failure analyses further revealed improvement on the turn-on uniformity of nLDMOS by the body current injection. From these experimental results, the body-injected technique is effective in increasing the ESD robustness of nLDMOS.

Chapter 3

Overview to The SOA Characterization and Improvement Techniques in Power MOSFETs

3.1. Background

High voltage and high current operations are common environments for power semiconductor devices. To sustain the high V_{CC} operating voltage, sufficient breakdown voltage (BV_{DSS}) is a must for power semiconductors. To minimize the power consumption over a switching transistor, device turn-on resistance per unit area, *i.e.* the specific on-resistance R_{SP}, is another important factor for the development of power devices. Safe operating area (SOA), as the third factor to meet the HV and high current requirements, defines the voltage-current boundary in which a power transistor can safely switch. The three factors, BV_{DSS}, R_{SP}, and SOA, are therefore known as the design triangle of power semiconductor devices as shown in Fig. 3.1 [32].

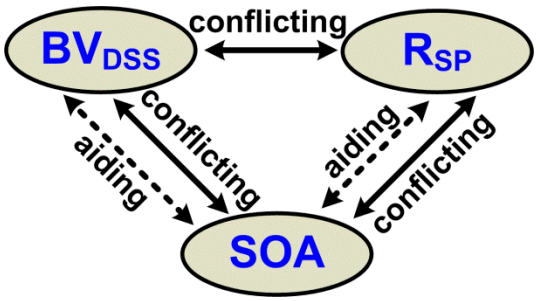


Fig. 3.1. The design triangle of power semiconductor devices (redrawn after [32]).

3.2. Physical Limitation of SOA

The physical limitation of SOA in a power MOSFET lies in the triggering of intrinsic BJTs [33]. The equivalent circuit model of a HV NMOS is shown in Fig. 3.2. R_D, R_S, and R_B are respectively (parasitic) drain, source, and body resistors of the HV NMOS; I_h is the hole

current that can forward bias the bipolar base-emitter junction through R_B and trigger on the intrinsic NPN BJT. Major sources of the current I_h include avalanche-generated holes (I_{AV}) and thermal generation (I_{TG}) due to device self-heating, which can be expressed as

$$I_h = I_{AV} + I_{TG} \quad . \tag{3.1}$$

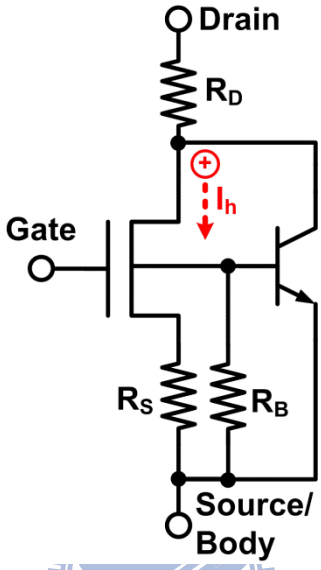


Fig. 3.2. The equivalent circuit model of a HV NMOS. Parasitic BJT and resistors are included.

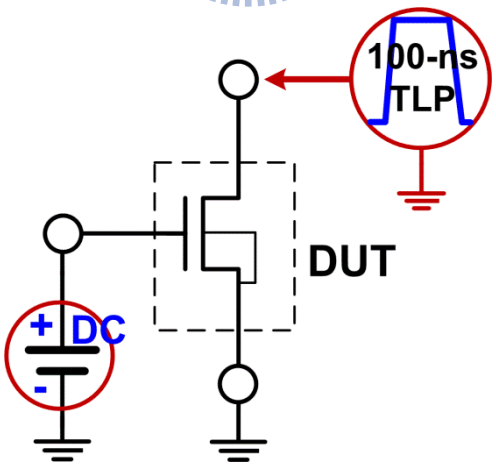


Fig. 3.3. The test setup of eSOA measurement with 100-ns TLP.

From equation (3.1), I_{AV} is a result of impact ionization, so that it is a function of both the drain-source current I_{DS} and avalanche multiplication factor M [33]. To minimize the effect of device self-heating and to estimate the impact to SOA that comes from I_{AV}, DUTs are usually

stressed by pulses with a short pulse width. Such an electrical SOA (eSOA) boundary is important when thermal effect is not strongly involved during operation; small devices that benefit from good lateral thermal spreading, for example [32]. A 50-Ω TLP system that delivers square pulses with an 100-ns pulse width is usually adopted for the measurement of eSOA [24], [32]. The setup of eSOA measurement is shown in Fig. 3.3, and measured eSOA boundaries of two 24-V nLDMOS are shown in Fig. 3.4. Because snapback (triggering of the intrinsic BJT) usually causes irreversible damage to a power MOSFET or induces circuit malfunctions, the eSOA boundary is defined by sweeping different gate biases and connecting the I-V points right before the device snapback. A higher gate bias causes a reduction in V_{DS} rating because a higher I_{DS} accelerates the number of electron-hole pairs generated from impact ionization (higher I_{AV}).

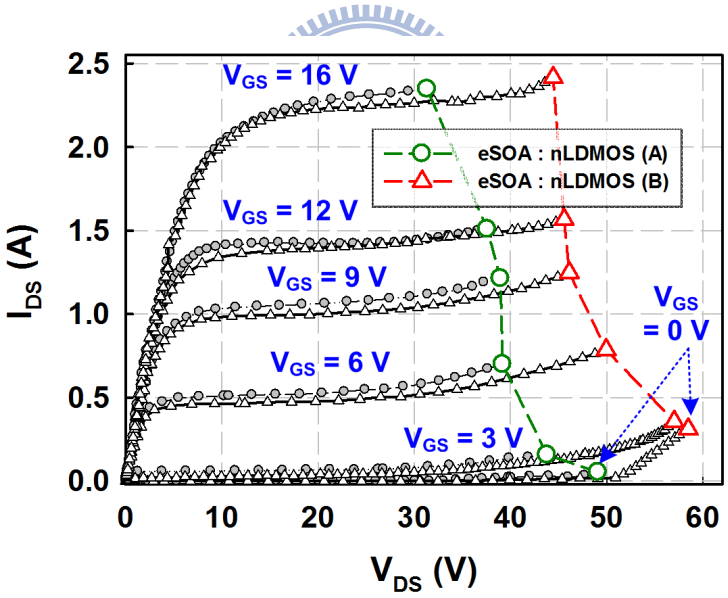


Fig. 3.4. Measured eSOA boundaries of two nLDMOS transistors.

When a power MOSFET operates with strong device self-heating, I_{TG} in equation (3.1) can become the dominating factor to cause device failure. The intrinsic doping concentration (n_i) in a semiconductor device is a strong function of temperature [34]

$$n_i = \sqrt{N_c N_V} e^{-E_G/2KT} \quad , \tag{3.2}$$

where K is the Boltzmann constant, T is the temperature, E_G is the energy bandgap, and N_C and N_V are the effective electron and hole density of states, respectively. From equation (3.2), extrinsic doping concentration is overwhelmed by n_i under high temperatures and the device become intrinsic semiconductor. Thermal SOA (tSOA) defines the boundary of device failure initiated by thermal instability [32], [35]. Tendencies of eSOA and tSOA boundaries with respect to temperature and pulse widths are depicted in Fig. 3.5 [32], [36]. When temperature increases, usually the eSOA shifts downward. A longer pulse width induces a stronger device self-heating, and the tSOA shifts inward. At a certain pulse width the tSOA boundary becomes enclosed within the eSOA. The tSOA is accordingly important for a large-area power MOSFET that has severe thermal accumulation, or when a power MOSFET is operated with a long (~ms) pulse time, solenoid drivers for example.

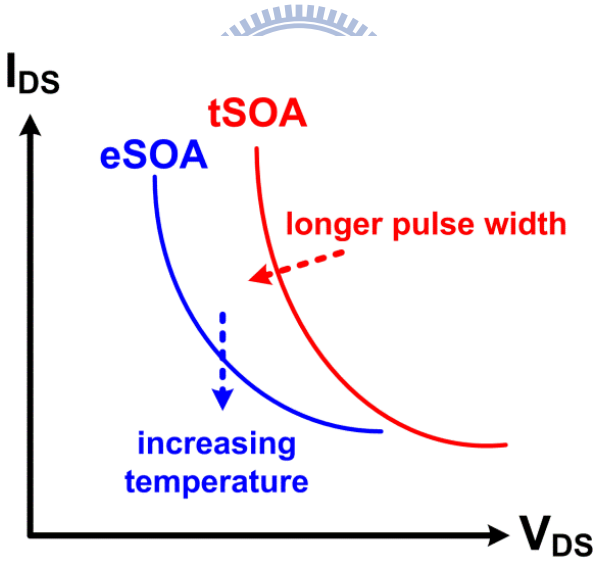


Fig. 3.5. A diagram showing tendencies of eSOA and tSOA with respect to temperature and pulse widths.

Though eSOA and tSOA define boundaries from different mechanisms, the two effects are usually coupled in nature as an electrothermal effect [36], [37]. R_D, R_S, and R_B resistors in the equivalent circuit model have positive temperature coefficients. The increases in R_D and R_S resistances under high temperature can suppress I_{AV} due to a reduced I_{DS}. The increases in R_B

resistance, on the contrary, help forward bias the base emitter junction and make the parasitic BJT easier to be triggered on. Avalanche multiplication factor M and the built-in potential of a bipolar base-emitter junction are also functions of temperature [32]. Techniques to decouple the electrical and thermal effects through deactivating the parasitic BJT showed an appreciable electrothermal coupling to determine the SOA of power MOSFETs [38], [39]. It is therefore hard to acquire pure electrical or thermal SOA under different gate biases, and the SOA chart of a power MOSFET usually has boundaries under different pulse widths. Fig. 3.6 is an example showing different regions of SOA for a power MSOFET. There are four regions in Fig. 3.6; region (A) is limited by the turn on resistance $R_{DS,ON}$ of the power MOSFET. Region (B) is limited by the current carrying capability either from the power MOSFET or the package. Region (C) is determined by the operating current and voltage across the power MOSFET (power limited). When pulse width increases, region (C) moves downward due to the increasing device self-heating and the electrothermal coupling. Region (D) is defined by the maximum drain to source voltage rating, the BV_{DSS}. In Fig. 3.6, because boundaries are defined when turning the power transistor into on-state, it is referred to as the forward-biased SOA (FB-SOA).

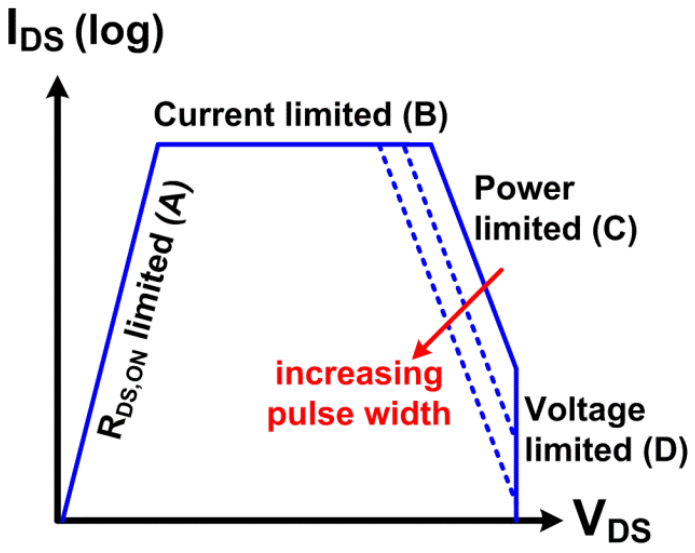


Fig. 3.6. A Diagram showing FB-SOA of a power MOSFET.

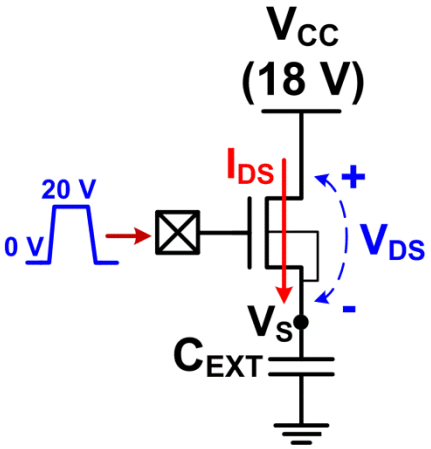


Fig. 3.7. Test circuit of an nLDMOS switching an external capacitor. C_{EXT} with different capacitances were used in this test.

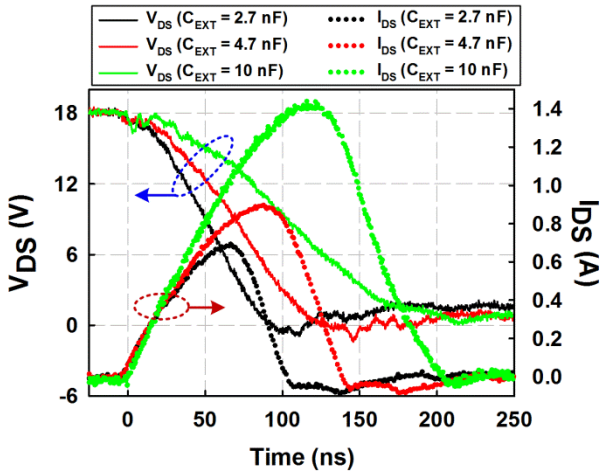
3.3. Switching Reactive Loads

Power transistors are used to drive various loads in industrial and automotive applications. A switching trajectory within the SOA boundary ensures safe operation of a power transistor. A wide SOA boundary is therefore preferred so as to enhance device reliability under various operating conditions. It is equally important to understand the I-V loci when switching different loads.

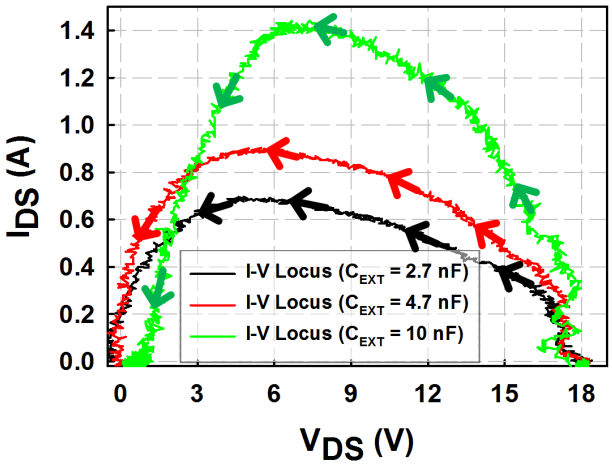
3.3.1. Capacitive Load

For a resistive load, the switching loci are relatively simple and follow the Ohm's law. However, when switching a reactive load, the switching loci become complicated. Voltage and current can have phase differences, resulting in high voltage and high current to occur at the same time. Test circuit of an nLDMOS to drive a large external discrete capacitor, output of a gate driver IC for example, is shown in Fig. 3.7. Capacitances used in the test circuits were 2.7, 4.7, and 10 nF. When the nLDMOS is switched on, C_{EXT} is charged up through the I_{DS} current of the nLDMOS. However, due to the RC time delay from the resistances of nLDMOS and metal wiring, and the capacitance of $C_{EXT,}$ source voltage (V_S) of the

nLDMOS is not pulled high immediately. Measured I-V waveforms in Fig. 3.8(a) clearly show the high V_{DS} and high I_{DS} to happen at the same time. The I_{DS} current in Fig. 3.8 is acquired from a current probe; the V_{DS} voltage is calculated from ($V_{CC} - V_S$); V_S is measured by using a voltage probe. When C_{EXT} is increased, a larger RC time delay causes a larger and a longer I_{DS}-V_{DS} stress across the nLDMOS. The I-V switching trajectories in Fig. 3.8(a) are redrawn in Fig. 3.8(b). Waveforms in Fig. 3.8(a) also suggest that when switching a capacitive load, eSOA is important due to the relatively short I-V stress time across the switching transistor [32].



(a)



(b)

Fig. 3.8. Measured (a) turn-on waveforms and (b) I-V trajectories of an nLDMOS switching capacitors with different capacitance values.

3.3.2. Inductive Load (Unclamped Inductive Switching)

Another typical example is the switching trajectory for inductive turn-off. Application example includes the solenoid driver or the relay actuator. The test circuit and some parameters used are shown in Fig. 3.9. Without additional clamping element in parallel to the inductor, this test is usually referred to as the unclamped inductive switching (UIS) and is important for stringent operating environments such as automotive electronics [40]–[42]. When the nLDMOS is turned on, the current increasing rate follows the relationship

$$\frac{di}{dt} \approx \frac{V_{CC}}{L_{EXT}} \quad , \tag{3.3}$$

where the total series resistance along the circuit is assumed to be small. As the measured I-V waveforms shown in Fig. 3.10(a), within the turn-on period T_{PW} (pulse width of the gate signal V_{GS}) the measured I_S current linearly increases with time and the V_{DS} has a voltage level close to the ground. During the turn-on stage, the total energy stored in the inductor is given by

$$E = \frac{1}{2} L_{EXT} I_{AS}^2 \quad . \tag{3.4}$$

I_{AS} is the load current right before switching off the nLDMOS; I_{AS} in Fig. 3.10(a) is ~110mA for example.

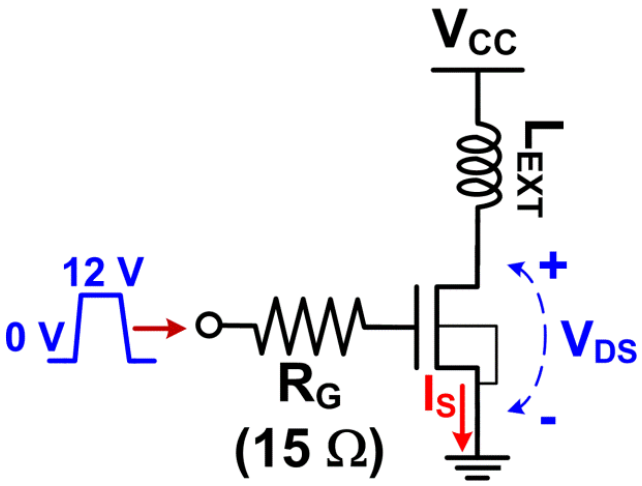


Fig. 3.9. Test circuit for unclamped inductive switching of an nLDMOS.

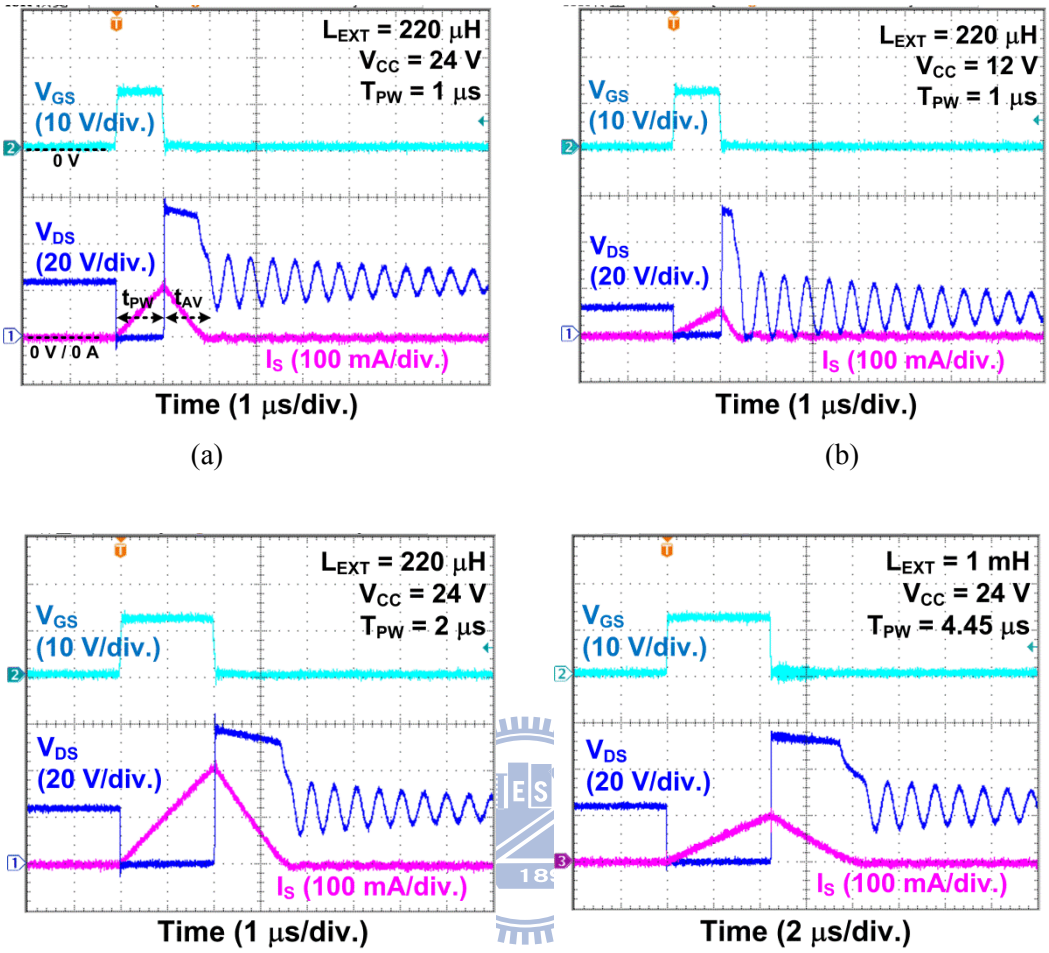


Fig. 3.10. Measured UIS waveforms with different L_{EXT}, V_{CC}, or T_{PW} parameters. (a) L_{EXT} = 220 µH, V_{CC} = 24 V, T_{PW} = 1 µs, (b) L_{EXT} = 220 µH, V_{CC} = 12 V, T_{PW} = 1 µs, (c) L_{EXT} = 220 µH, V_{CC} = 24 V, T_{PW} = 2 µs, and (d) L_{EXT} = 1 mH, V_{CC} = 24 V, T_{PW} = 4.45 µs.

When the nLDMOS is switched off, the current flowing through the inductor cannot immediately drop to zero. The energy stored in the inductor drives up the V_{DS} voltage of the nLDMOS and forces the nLDMOS to discharge the load energy through avalanche breakdown [43]–[45]. The peak current I_{AS} corresponds to the avalanche current, and the energy EAS to be dissipated during inductive turn-off is

$$E_{AS} = \frac{1}{2} L_{EXT} I_{AS}^2 \frac{BV}{BV - V_{CC}} \quad . \tag{3.5}$$

As the measured waveforms shown in Fig. 3.10(a), when the V_{GS} is turned off, the V_{DS}

voltage shoots up to the breakdown voltage (BV) of the nLDMOS (~58 V); current begins to decrease linearly and the V_{DS} voltage is kept high until I_S drops to zero. The current decreasing rate during inductive turn-off follows

$$\frac{di}{dt} = \frac{BV - V_{CC}}{L_{EXT}} \quad . \tag{3.6}$$

Since the switching transistor is operated under avalanche breakdown, the time to discharge the energy stored in the inductor is usually referred to as t_{AV}. From equation (3.6), t_{AV} can be derived as [45]

$$t_{AV} = \frac{L_{EXT} \times I_{AS}}{BV - V_{CC}} \quad . \tag{3.7}$$

With the above equations, several parameters affecting the UIS waveforms can be observed from Fig. 3.10. When V_{CC} voltage is reduced from 24 to 12 V, equations (3.3) and (3.7) suggest that I_{AV} should be reduced to a half and t_{AV} is shortened as well (Fig. 3.10(a) and 3.10(b)). The voltage oscillation after t_{AV} is due to the LC oscillation of the L_{EXT} and the parasitic capacitance of the voltage probe. Increasing the T_{PW} width from 1 to 2 μs doubles I_{AV}; t_{AV} increases as well (Fig. 3.10(a) and 3.10(c)). When the inductance is increased from 220 μH to 1mH, T_{PW} is increased from 1 to 4.45 μs to reach the same I_{AV} current (Fig. 3.10(a) and 3.10(d)). From equations (3.5) and (3.7), at the same I_{AV} the larger inductance results in a longer t_{AV} and a larger energy to be dissipated, i.e. the transistor is stressed more severely.

From Fig. 3.10(a) and 3.10(c), dependence between the peak V_{DS} voltage and the I_{AV} magnitude during inductive turn-off, though weak, is also observed. For a gate-grounded nLDMOS entering avalanche breakdown, the I-V characteristic is illustrated as Fig. 3.11. When the V_{DS} voltage across an nLDMOS is higher than its BV_{DSS}, avalanche current I_{AV} starts to flow; snapback does not happen immediately until the current magnitude reaches I_{t1}, at which the BJT base-emitter junction is forward biased through R_B (Fig. 3.2). The I_{AS} current level during UIS test cannot exceed I_{t1}, otherwise the nLDMOS snaps back and a latchup-like electrical overstress (EOS) will permanently damage the nLDMOS. For an UIS

test with a peak inductor current I_{AS1}, the energy stored in the inductor will correspondingly charge up the drain voltage to V_{DS1} during inductive turn-off so as to keep the current continuity. From Fig. 3.11, it is known that a higher peak inductor current I_{AV2} causes a higher voltage V_{DS2} during inductive turn-off. Note that I_{TG} in equation (3.1) can contribute greatly to the device snapback in UIS because of the high power during avalanche breakdown and the long t_{AV} during inductive turn-off (from several μs up to several tens of ms) [46].

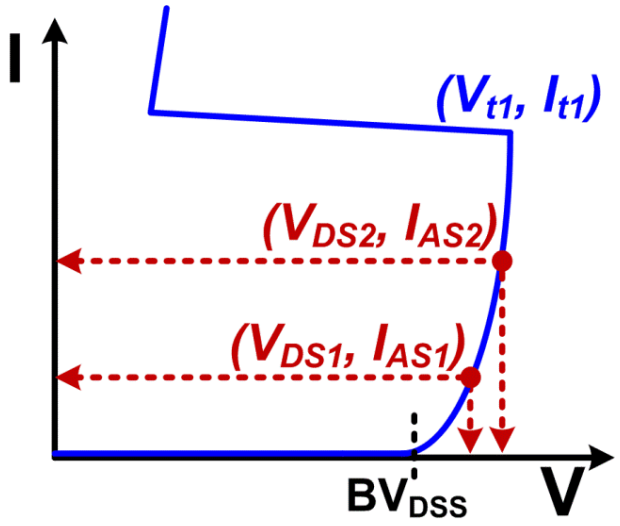


Fig. 3.11. A diagram depicting the I-V characteristic of a gate-grounded nLDMOS.

Because the stress across the transistor in an UIS test happens during transistor turnoff, it is classified as the reverse-biased SOA (RB-SOA) and usually has different rating methods than the FB-SOA. The term RB-SOA is often reserved for BJTs switching unclamped inductive load, and for MOSFETs UIS is used more often. To evaluate the transistor ruggedness against UIS, two parameters are usually adopted as the benchmark. The first parameter is the maximum allowable switching current ($I_{AS,Max}$) without inducing transistor failure [40], [47]. The other rating method uses the maximum energy $E_{AS,Max}$ dissipated in the switching transistor without inducing failure as the benchmark. The second method is usually referred to as the energy capability of a power MOSFET [41].

3.3.3. Inductive Load (Clamped Inductive Switching)

Due to the high junction temperature over a MOSFET during avalanche breakdown, UIS is a harsh test for power MOSFETs. In practical designs, the clamped inductive switching (CIS) is usually used to bypass the energy during inductive turn-off without avalanching the switching transistor.

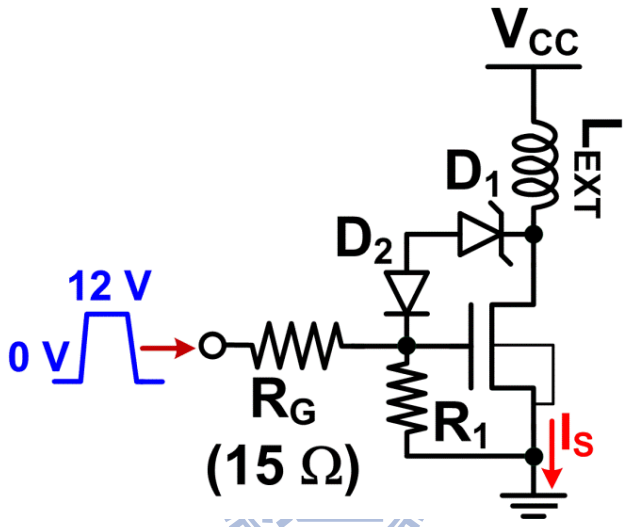


Fig. 3.12. A CIS test circuit using a zener diode to clamp the nLDMOS drain voltage during inductive turnoff.

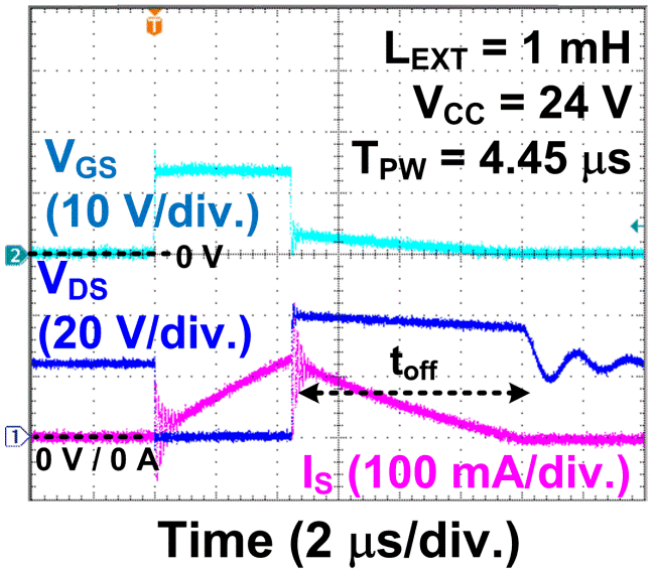


Fig. 3.13. Measured I-V waveforms of the CIS test circuit. The breakdown voltage of the zener diode is 37 V.

An example of the CIS circuit is shown in Fig. 3.12 [38], [48]. When switching off the inductive load, the zener diode D_1 breaks down and a current I_Z pulls high the gate potential of the nLDMOS through the diode D_2 and the R_1 resistor. The D_1 diode is chosen to have a breakdown voltage BV_Z smaller than the BV_{DSS} of the nLDMOS so as to prevent nLDMOS from avalanche breakdown. The drain voltage of the nLDMOS during inductive turn-off is therefore limited at $V_{clamp} = BV_z + V_{diode} + (R_1 \times I_Z)$. With the gate potential pulled high, the energy stored in the inductor is mainly discharged through the channel current of the nLDMOS. Measured I-V waveforms of the zener-clamped CIS circuit are shown in Fig. 3.13; BV_Z of the D_1 in Fig. 3.13 is 37 V, and the nLDMOS is the same transistor used to measure Fig. 3.10. When switching off the inductor, the measured V_{DS} voltage is clearly limited at a lower voltage level around 40 V. Note that in CIS, FB-SOA of the switching transistor is important as well because the transistor has to sustain V_{clamp} and the inductive turn-off current at the same time.

In the zener-clamped CIS circuit, because the drain voltage of the nLDMOS is limited at V_{clamp}, the time t_{off} to dissipate the energy stored in the inductor becomes

$$t_{off} = \frac{L_{EXT} \times I_{MAX}}{V_{clamp} - V_{CC}} \quad , \tag{3.8}$$

where I_{MAX} is the current right before switching off the nLDMOS. Comparing equations (3.7) and (3.8), with the V_{clamp} smaller than the breakdown voltage of nLDMOS, the zener-clamped CIS results in a longer inductive turn-off time as shown in Fig. 3.13. The energy dissipated in the nLDMOS during the turn-off period becomes

$$E_{AS} = \frac{1}{2} L_{EXT}\, I_{MAX}^2 \frac{V_{clamp}}{V_{clamp} - V_{CC}} \quad . \tag{3.9}$$

When measuring energy capabilities, equations (3.5) and (3.9) show that different inductances, current magnitudes, zener diodes…etc have to be changed during tests to figure out the $E_{AS,MAX}$ of a DUT. It is, however, inconvenient and difficult to control. To facilitate the measurement, alternative rectangular power pulsing (RPP) test methods which use

rectangular voltage or current pulses with different pulse widths have been proposed [48]. Voltage and current RPP testing circuits are shown in Fig. 3.14(a) and 3.14(b), respectively. The RPP tests save the usage of external inductors. Energy capabilities of DUTs can be easily figured out simply by varying the pulse width or the magnitude of delivered voltage / current pulses. Though in a real inductive switching condition the current waveform is in a triangular shape, RPP tests have been verified to deliver reasonably accurate results [48].

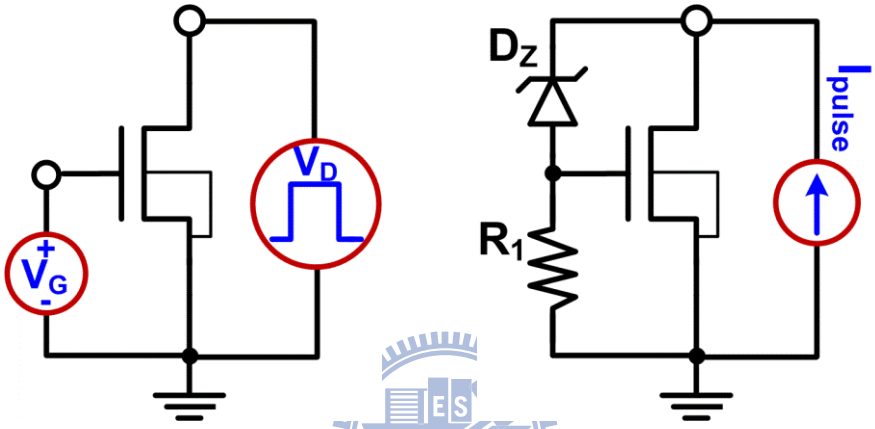


Fig. 3.14. Measurement setups for (a) voltage and (b) current rectangular power pulsing test circuits (redrawn after [48]).

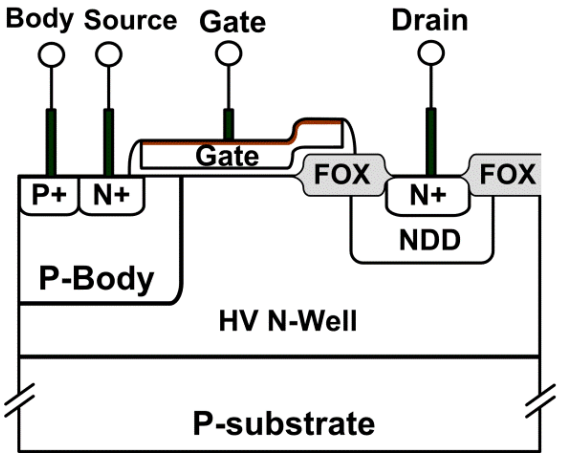
3.4. Techniques to SOA Improvement

Aside from the CIS method to assist transistors, techniques to improve the intrinsic SOA of power MOSFETs are always preferred. This section introduces the SOA improvement techniques that have been reported.

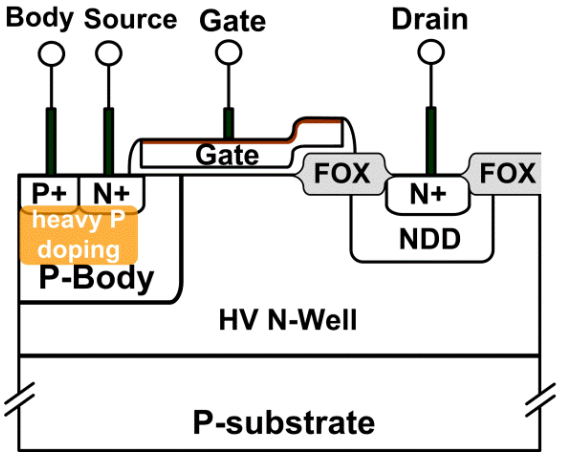
3.4.1. Additional Body Implantation

Since the criterion for a BJT to be triggered on is the forward conduction of its base-emitter junction, reducing the parasitic R_B resistor in Fig. 3.2 is effective in widening the MOSFET SOA [49]–[51]. The process integration method in reducing the R_B resistor is illustrated in Fig. 3.15. Comparing to the regular nLDMOS structure shown in Fig. 3.15(a),

an additional P-type body implantation is added to elevate the doping concentration of P-body (see Fig. 3.15(b)). Measured eSOA of the regular nLDMOS is the boundary (A) in Fig. 3.4; nLDMOS with the additional P-type implantation at body has the eSOA boundary (B) in Fig. 3.4. Both devices have the same effective width of 4800 μm. It is clear from Fig. 3.4 that the additional P-type body implantation substantial improves the FB-SOA of power MOSFETs. With the reduced R_B, $I_{AS,MAX}$ in an UIS test for the 4800-μm nLDMOS improves from 100 to 350 mA as well, a result consistent to previous publications [49], [50].

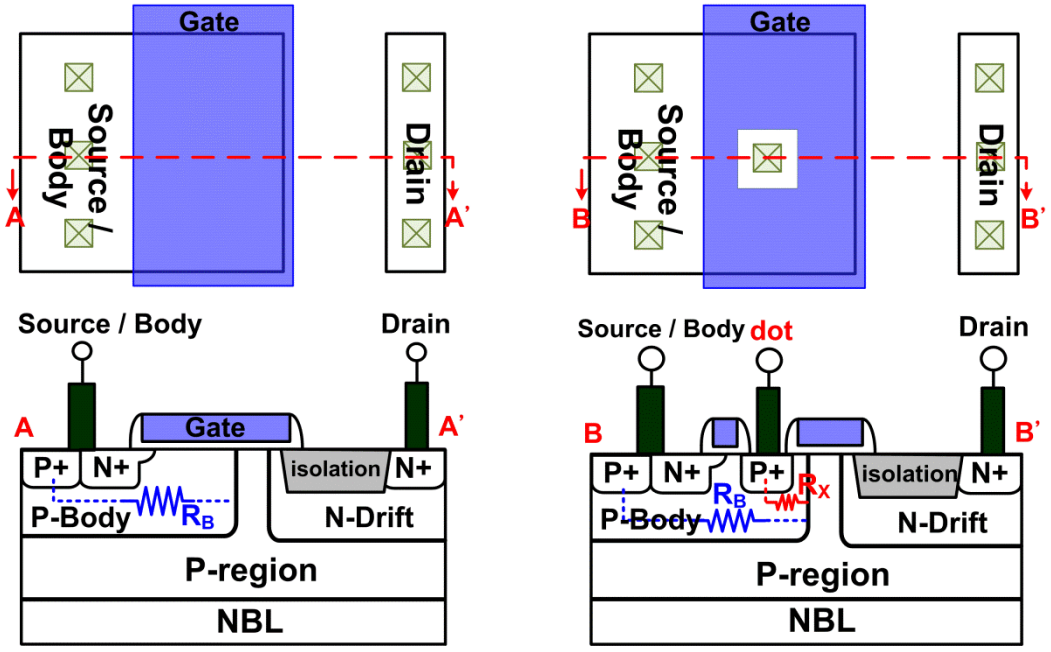


(a)



(b)

Fig. 3.15. Device cross-sections of (a) a regular nLDMOS and (b) an nLDMOS with additional P-type implantation at body to improve SOA.



(a) (b)

Fig. 3.16. Layout and device cross-sectional views of (a) a regular LDMOS and (b) a dotted-channel LDMOS for SOA improvement (redrawn after [52]).

3.4.2. Dotted Channel LDMOS

An approach to reducing the R_B resistance and suppressing the BJT action through process integration is useful, but often inaccessible to fabless IC design companies. A layout technique for the SOA improvement without modifying process steps or mask layers is reported in [52]. As illustrated in Fig. 3.16, poly gate in a dotted-channel LDMOS is intentionally drawn with open squares in layout to insert P+ diffusion regions and metal contacts (dots). When these dots are grounded through metallurgical connection, an additional parasitic resistor R_X is formed (see Fig. 3.16(b)); R_X is in parallel with the body resistor R_B of a regular LDMOS and hence, the effective body resistance R_B' in a dotted-channel LDMOS becomes (R_B // R_X) to suppress the parasitic BJT.

In the dotted-channel layout, in order to open dots in transistor poly gate the gate length may need to be extended, depending on the technology node being used. Moreover, to prevent transistor breakdown voltage from being affected by the dots, the distance between

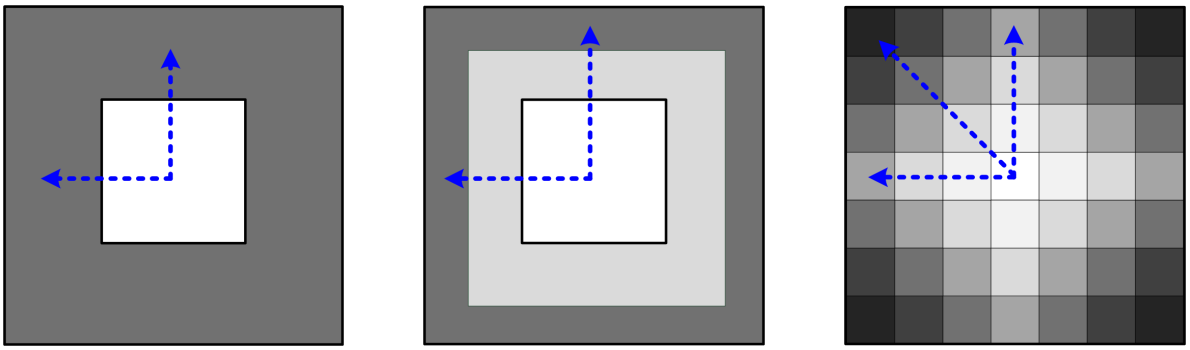
the dotted contact and the drift region has to be larger than the minimum allowable channel length [52]. These restrictions result in a negative impact to transistor R_{SP}, and the quantity of impact is highly process-dependent. Another poly-bending layout technique that bends the poly gate in 45 degree can incorporate grounded dots as well and minimize the impact of gate lengthening to R_{SP} [53]. In addition to the SOA improvement, both layout techniques exhibited remarkably increased secondary breakdown current to electrostatic discharges (ESD) [3].

3.4.3. Drift Configurations

It is well known that for a power MOSFET under high current conduction, the kirk effect shifts the high electric field region toward the transistor drain contacts [54]. Since the avalanche current that induces both the triggering of parasitic BJTs and the electrothermal coupling is a result of the high electric field, engineering the drift region of a power MOSFET is another approach to the SOA adjustment. A higher doping concentration in the drift region of an nLDMOS can compensate the negative electron charges during transistor on-state and hence push the onset of kirk effect to a higher current level [55]. However, increasing the doping concentration in the drift region degrades the device BV_{DSS} as well [56]. Lengthening the drift region is another way to widen the device SOA because the higher series resistance from the drift region limits the transistor saturation current. This, however, results in a higher transistor R_{SP}. An adaptive method that has an additional n-type adaptive region at drain was accordingly proposed to counteract the drawbacks and to improve the transistor SOA [56]–[58]. Besides the benefit on the SOA, the drain profile has also been reported as a key device parameter for implementing a power MOSFET with high ESD protection level [59], [60].

3.4.4. Thick Copper Metallization

For a power transistor that operates with a long on-state period or has a large device area (~mm^2), thermal effect is prominent and the transistor junction temperature can become high enough to initiate thermal runaway [61], [62]. The removal of the temperature rise within the active transistor in response to the dissipated energy accordingly helps improve the device stability. In power technologies, this can be accomplished by using a heat sink over the power transistor. Due to the good thermal properties and mature process integration techniques to handle with, copper is chosen over other metal materials to serve as a waver-level heat sink [62]–[64]. This on-chip technique is equally important for sub-millisecond operations where the time is not enough for the IC packaging to give an effect to the device temperature [65], [66]. The copper metallization has been demonstrated to substantially improve the transistor energy capability, and a thicker copper metallization further enhances the improvement [62]–[66]. Moreover, it is also used as a surface layer of metal wiring to solve the voltage de-biasing effect [67] in large power MOSFETs and to save power consumption through the reduced overall R_{ON} [62], [68].



(a) (b) (c)

Fig. 3.17. Illustration of power MOSFET arrays with (a) single step, (b) dual step, and (c) checkerboard, layout design for improving the uniformity of power distribution (redrawn after [69]).

3.4.5. Power Distribution

With the strong device self-heating involved in switching a large power MOSFET, the temperature spread across the transistor array is found to be inhomogeneous. Device edges benefit from a better thermal removal through surrounding silicon and the weak spot (highest temperature) hence locates at the center of the array [62], [69]. A uniform temperature distribution across the power transistor array that eliminates the weak spot hence improves the transistor energy capability.

From the 1-dimentional heat flow theory, a simple relationship between power dissipation, temperature increase and time is

$$\Delta T = \frac{2P}{\sqrt{\pi k \rho c_p} A_E} \sqrt{t} \quad , \tag{3.10}$$

where k is thermal conductivity, ρ is density, c_p is specific heat capacity, and A_E is active area. From equation (3.10), the temperature increase is proportional to the power dissipation and the square root of time. Having different operation time among an array is less practical; uniform power distribution across a power MOSFET array is more feasible. With the MOSFET saturation current being

$$I_{D,sat} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \quad , \tag{3.11}$$

a multi-step layout design utilizing different current carrying capabilities is proposed to engineer the power distribution (Fig. 3.17) [69]. Power MOSFET arrays are divided into regions of different channel lengths (L) or oxide thickness. Arrows in Fig. 3.17 indicate the direction of increasing current carrying capability (shorter channel length for example). Experimental results in [69] showed a more than 20% improvement on the energy capability and less than 10% increase on transistor turn-on resistance. Moreover, the simple single-step design was able to optimize the power distribution to its fullest already [69].

3.5. Summary

A wide SOA is required to sustain the high voltage and high current that happens across a power MOSFET at the same time, switching reactive loads for example. Through the circuit design technique, clamped inductive switching can help improve SOA when switching an inductive load. Process integration approaches such as a thick top metal layer, a heavily doped body region, or the adaptive drift implantation improve intrinsic SOA of power MOSFETs. Besides the circuit and the process integration methods, layout modifications can also enhance SOA of power MOSFETs. In summary, safe operating area is one of the most important indicators for the reliability of power MOSFETs. Research and improvement techniques on the SOA will keep continuing as an essential and critical factor in the development of power MOSFETs.

Chapter 4

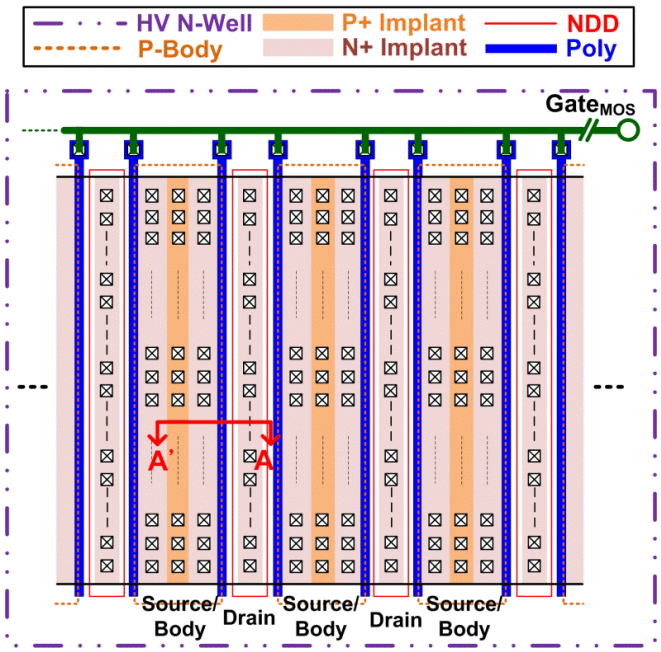
High-Voltage Output Arrays and The Poly-Bending Layout for the eSOA improvement of SCR-nLDMOS

4.1. Background

For output drivers that are designed to drive considerable amount of current (output arrays), ESD design rules are usually not applied to such output arrays to minimize their layout area in silicon chips [70]. These output arrays therefore are incapable of being self-protected against ESD stresses, and some additional ESD design techniques are needed to provide adequate capabilities to survive the general ESD specification of 2-kV HBM ESD test for commercial products [3]. Additional ESD protection circuit in parallel to the output array is one of the possible design solutions, but trigger competition between the ESD protection circuit and the output array can usually lead to an upset result on ESD protection level [71]. As a result, self-protected output arrays are preferable to HV technologies. The silicon-controlled rectifier (SCR) inserting into HV output arrays has been reported as an area-efficient method to equip HV output arrays with superior ESD robustness [72]–[75].

Though embedding SCR in HV output arrays is very effective in improving ESD robustness, mis-triggering of the embedded SCR imposes new reliability concerns during normal circuit operating conditions, especially in some applications that require both high current and high drain-to-source voltages (V_{DS}) at the same time. In [74] and [75], inserting SCR to a HV output array has been reported to diminish the SOA boundary of the output array. It is therefore important to have a more deep investigation on the impact of embedded SCR structure to the SOA of HV output arrays. In this chapter, different layout parameters and device configurations have been studied for the optimization of SOA and ESD robustness

of nLDMOS arrays in a 24-V BCD process.



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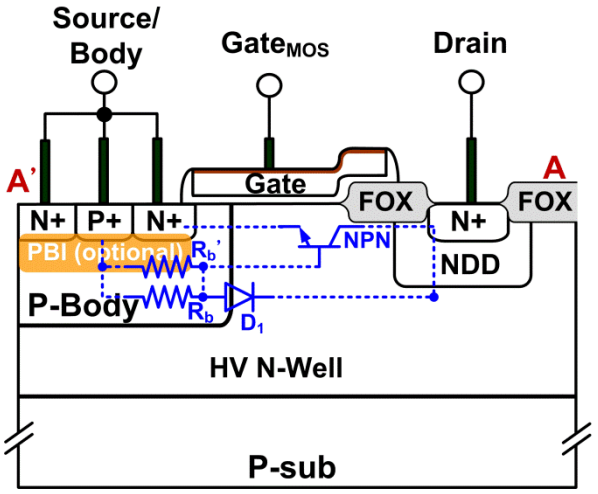


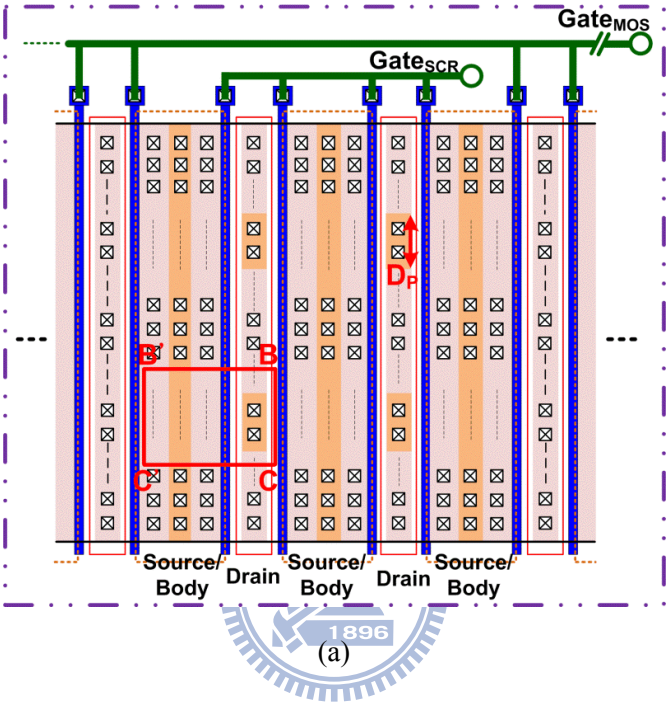
(b)

Fig. 4.1. (a) Layout top view and (b) device cross-sectional view along A-A' line of an nLDMOS without embedded SCR.

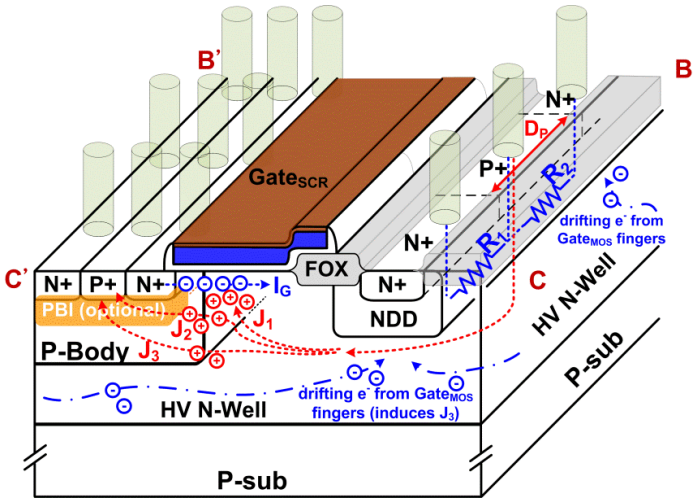
4.2. Test Structures of HV nLDMOS

Layout top view and device cross-sectional view of an nLDMOS in the 24-V process are shown in Fig. 4.1(a) and 4.1(b), respectively. The PBI layer in Fig. 4.1(b) is the optional

P-type body implantation layer. To emulate the high-current driving requirement of output arrays in practical IC products, devices were drawn in large arrays with total effective width (W) of 4800 μm. Width and channel length of a single finger are kept the same in layout for all studied devices, 100 and 0.35 μm, respectively.



(a)



(b)

Fig. 4.2. (a) Layout top view and (b) device cross-sectional view along B-B'-C-C' region of an nLDMOS with embedded SCR.

To study the impact on eSOA due to embedded SCR structure, layout top view of an nLDMOS array with embedded SCR (SCR-nLDMOS) is shown in Fig. 4.2(a). Embedded SCR was centralized within the central four fingers of nLDMOS arrays by replacing part of drain implantation from N+ to P+. The four fingers that contain the embedded SCR is referred to as $Gate_{SCR}$ fingers, and the rest 44 fingers that do not have SCR structure are referred to as $Gate_{MOS}$ fingers. Total effective widths of SCR-nLDMOS arrays were kept the same to that of nLDMOS arrays, 4800 μm. Device cross-sectional view along B-B'-C-C' square in Fig. 4.2(a) is shown in Fig. 4.2(b). P+ implantation at drain regions is the anode of the SCR, and the SCR current path is P+ – (NDD / HV N-Well) – P-body – N+ source. Gate connection for $Gate_{SCR}$ fingers was intentionally separated from $Gate_{MOS}$ fingers and was either internally short circuited to $Gate_{MOS}$ fingers or internally short circuited to source/body (grounded) for further investigation. Width of a drain P+ implantation is defined as D_P width. All studied SCR-nLDMOS arrays have the same total effective SCR anode width of 200 μm in the 4 $Gate_{SCR}$ fingers. As a result, a SCR-nLDMOS with D_P of 10 μm means that there are 5 P+ segments in each finger, and each P+ segment is 10-μm wide. The 5 P+ segments are evenly spread along the 100-μm finger width. Three different D_P widths of 50, 10, and 5 μm, were studied in the test vehicle.

4.3. Electrical SOA of nLDMOS and SCR-nLDMOS Arrays

To analyze the impact of embedded SCR to device ruggedness under normal circuit operating conditions, eSOA with 100-ns TLP and DC gate bias was used throughout the study in this chapter. All measurements were conducted under the room temperature of 300 k.

4.3.1. PBI Layer to eSOA of nLDMOS

In an nLDMOS, the parasitic NPN BJT as indicated in Fig. 4.1(b) consists of (N+/NDD/HV N-Well) – P-body – N+ source. R_b in Fig. 1(b) denotes the parasitic resistor

from P-body without the optional PBI layer, whereas R_b' denotes the parasitic resistor from the PBI layer. When the gate voltage is biased above 0 V, channel electrons entering a high electric field region due to a high V_{DS} voltage can undergo the carrier multiplication process, which accelerates the electron-hole pair generation and usually leads to a reduced bipolar trigger voltage.

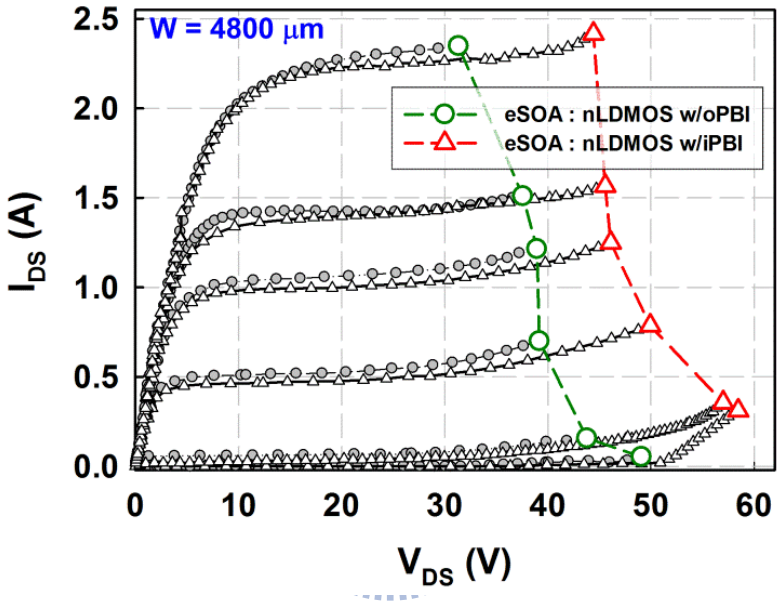


Fig. 4.3. Measured eSOA of nLDMOS with and without PBI layer. DUTs with I_{DS} from low to high were measured under gate biases of 0, 3, 6, 9, 12, and 16V.

TLP-measured I-V characteristics under different gate biases and the eSOA of nLDMOS arrays with and without PBI are shown in Fig. 4.3. Because PBI layer introduces a R_b' resistor in parallel with the P-body resistor R_b as shown in Fig. 4.1(b), base-emitter junction of the parasitic NPN BJT becomes harder to be forward biased. nLDMOS with PBI layer therefore shows a wider eSOA in Fig. 4.3 than that of nLDMOS without PBI layer [51]. Under the gate bias of 0 V (gate-grounded), measured leakage current of both nLDMOS in Fig. 4.3 immediately increased from pico-amp range to over 1 μA after snapback. Measured bipolar trigger currents (I_{t1}) in Fig. 4.3 are 311 and 53 mA for gate-grounded nLDMOS with

and without PBI, respectively. Because both nLDMOS arrays failed immediately after snapback, the measured I_{t1} values are equal to their secondary breakdown currents (I_{t2}). Both nLDMOS arrays (with and without PBI) possess a virtual zero HBM ESD protection level, therefore the embedded SCR structure becomes a necessity to provide self-protected ESD protection capability to these two nLDMOS arrays.

4.3.2. SCR-nLDMOS and D_P width to eSOA ($Gate_{SCR}$ internally short circuited to $Gate_{MOS}$)

With the SCR embedded in an nLDMOS array (SCR-nLDMOS), parasitic devices become more complicated than that of nLDMOS without embedded SCR. Equivalent circuit of the embedded SCR is shown in Fig. 4.4. The equivalent circuit in Fig. 4.4 resembles an insulated gate bipolar transistor (IGBT) [76], except for the R_N connecting emitter and base of PNP BJT. The R_N resistor comes from the N+ regions next to D_P, *i.e.* R_1 and R_2 in parallel as shown in Fig. 4.2(b). Therefore, SCR-nLDMOS with a smaller D_P width has a smaller equivalent R_N.

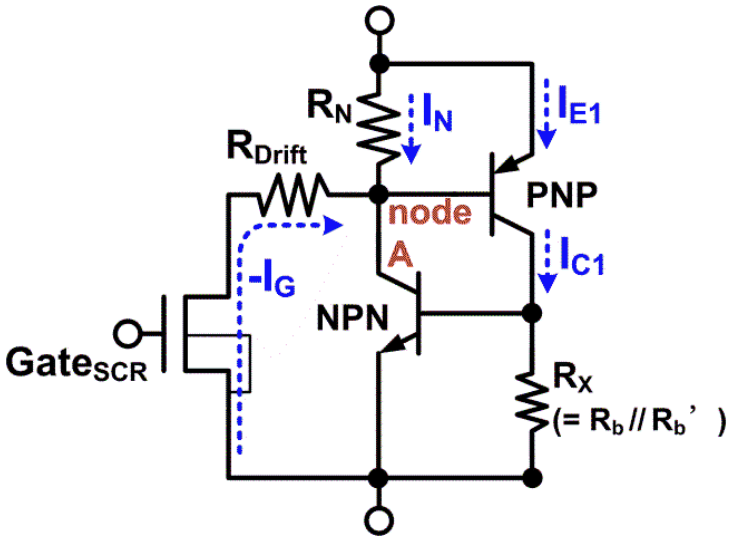
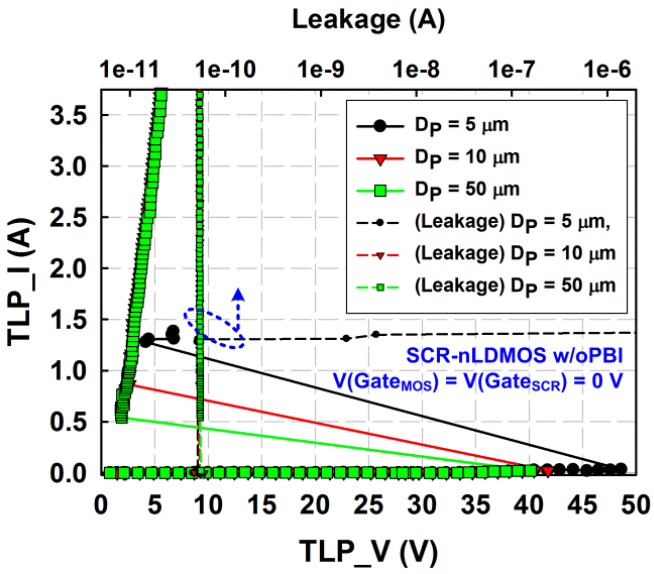


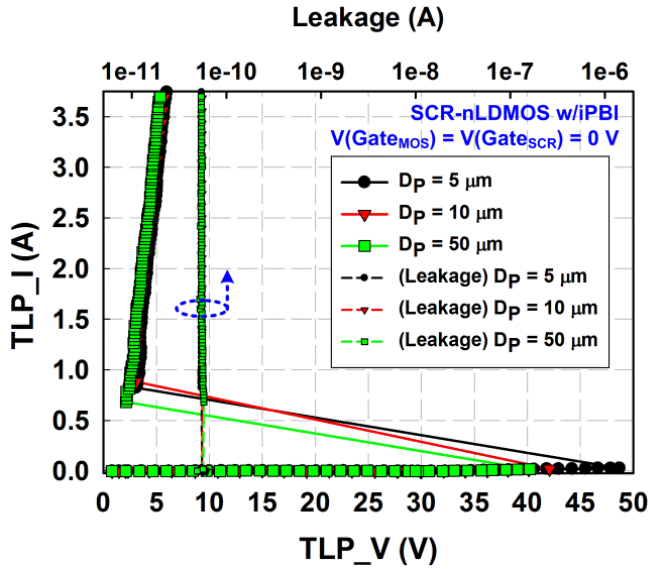
Fig. 4.4. The equivalent circuit of the embedded SCR in the nLDMOS arrays.

It should be noted that in a high voltage technology where IGBT is a dedicated power device, the regenerative feedback of parasitic SCR in the IGBT is suppressed carefully to avoid latch up under normal circuit operating conditions [77]–[79]. However, for HV technologies with relatively low voltage ratings (typically < 200 V processes, so that the studied process is included, too), IGBT usually is not a dedicated device and SCR is used for ESD protection purposes. SCR structures in these technologies are made up of parasitic BJTs without being specially suppressed during process development. As a result, the sum of open-base current gains of parasitic PNP (α_{PNP}) and NPN (α_{NPN}) BJTs in these technologies can be higher than 1 to initiate regenerative feedback even under normal circuit operating conditions [80].

Measured TLP I-V curves of SCR-nLDMOS without and with PBI layer are shown in Fig. 4.5(a) and 4.5(b), respectively. Gate bias for DUTs in Fig. 4.5 was 0 V, and leakage currents were measured under the drain bias of 24 V. In Fig. 4.5(a), both SCR-nLDMOS with D_P of 10 and 50 μm can sustain 100-ns TLP stresses higher than the limitation of the TLP system used, 3.75A. For SCR-nLDMOS with D_P of 5 μm, because a smaller D_P width results in a smaller R_N resistor, emitter-base junction of PNP BJT becomes harder to be forward biased. As a result, D_P of 5 μm in Fig. 4.5(a) exhibits the highest measured trigger voltage (V_{t1}) of 48.62 V. Measured V_{t1} for nLDMOS without PBI in Fig. 4.3 is 49.04 V. These two measured V_{t1} values of 48.62 and 49.04 V show that when D_P is as small as 5 μm, trigger competition can easily happen between the 4 fingers with embedded SCR ($Gate_{SCR}$ fingers) and the other 44 fingers without embedded SCR ($Gate_{MOS}$ fingers). As a result, instead of showing a high TLP-measured I_{t2}, SCR-nLDMOS with D_P of 5 μm failed (leakage current increased over 10X) at 1.31 A in Fig. 4.5(a). Because the failure arises from trigger competition between $Gate_{SCR}$ and $Gate_{MOS}$ fingers, a virtual zero ESD protection level on SCR-nLDMOS without PBI under D_P of 5 μm is possible.



(a)



(b)

Fig. 4.5. Measured TLP I-V characteristics of SCR-nLDMOS (a) without PBI and (b) with PBI. Gate bias for all DUTs was 0 V and leakage currents were measured under 24-V drain bias.

For SCR-nLDMOS with PBI, because the measured V_{t1} for gate-grounded nLDMOS with PBI in Fig. 4.3 is increased to 58.47 V, trigger competition between $Gate_{SCR}$ and $Gate_{MOS}$ fingers is averted. All DUTs in Fig. 4.5(b) therefore have I_{t2} higher than the equipment limitation of 3.75 A. Effectiveness on embedded SCR to improve ESD robustness therefore has been verified through measurement results in Fig. 4.5.

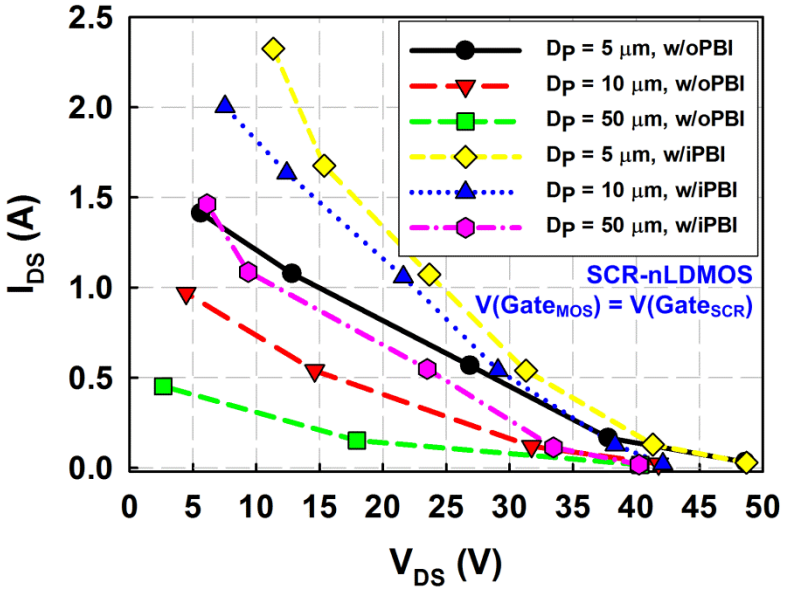


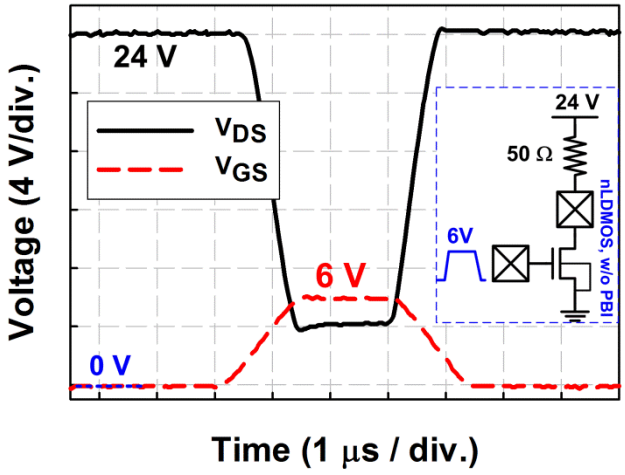
Fig. 4.6. Measured eSOA of SCR-nLDMOS with $Gate_{SCR}$ short circuited to $Gate_{MOS}$. The corresponding gate biases for the I_{DS} from low to high were 0, 3, 6, 9, 12, and 16 V, respectively. Some measured DUTs have less than 6 data points because these DUTs under high gate biases were driven directly into SCR operation without manifesting distinct snapback to determine their eSOA boundaries.

When the potential of $Gate_{SCR}$ is pulled high to induce channel current, electrons are provided from the N+ source (I_G) and holes emitting from P+ anode of SCR can be recombined with these electrons. This is shown as J_1 current flow in Fig. 4.2(b). However, instead of being recombined with electrons, part of the emitting holes from P+ anode is drawn to the vicinity of channel due to the negative charge of electrons and then be swept to the grounded P+ body contacts through the P-body/PBI (J_2 current flow in Fig. 4.2(b)). These holes traveling through P-body/PBI develop a voltage drop across the base-emitter junction of NPN BJT, which will eventually trigger on NPN BJT and lead to positive regenerative feedback of SCR during normal circuit operating conditions. This can also be understood from the equivalent circuit shown in Fig. 4.4 where the I_G current serves as the base current of PNP BJT and further induces the I_{C1} collector current [81]. Once the base-emitter junction

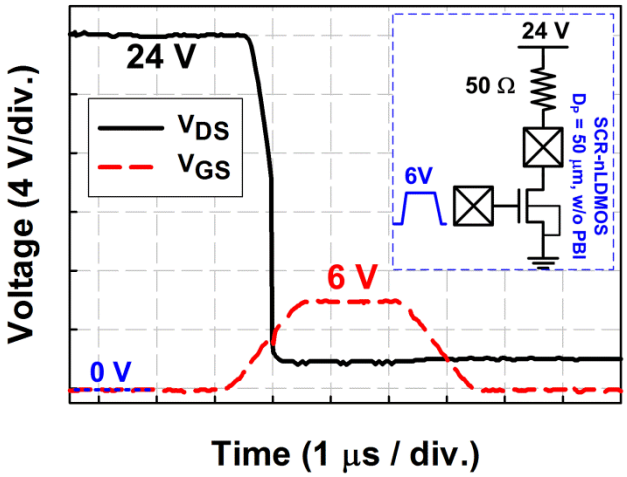
of NPN BJT in Fig. 4.4 is forward biased, SCR is triggered on and latchup happens.

Measured eSOA for SCR-nLDMOS without and with PBI layer are shown in Fig. 4.6. DUTs in Fig. 4.6 have $Gate_{SCR}$ internally connected to $Gate_{MOS}$, so that when a positive gate bias is applied to DUTs in Fig. 4.6, $Gate_{SCR}$ potential is pulled high along with $Gate_{MOS}$ potential. Comparing eSOA shown in Fig. 4.3 and 4.6, a substantially narrowed eSOA due to embedded SCR is observed. This means by inserting SCR into nLDMOS arrays for ESD protection, the SOA boundary is changed from the triggering of NPN BJT to the triggering of SCR due to the strong positive regenerative feedback of the P-N-P-N structure.

Comparing measurement results in Fig. 4.6 with the same D_P width, SCR-nLDMOS with PBI layer constantly shows a better eSOA performance than that of SCR-nLDMOS without PBI layer. This is due to the fact that PBI layer not only suppresses bipolar beta gain of NPN BJT (β_{NPN}), but also makes base-emitter junction of NPN BJT harder to be forward biased. Measurement results in Fig. 4.6 also reveal a strong dependency of eSOA to D_P width. Under the same gate and anode voltages, a smaller R_N (shorter D_P) helps keep the node A voltage in Fig. 4.4 at a relatively higher potential. This diminishes the emitting holes from P+ SCR anode by reducing the voltage difference across the emitter-base junction of PNP BJT. With the number of holes emitting from P+ anode being suppressed, J_2 current in Fig. 4.2(b) to forward bias the base-emitter junction of NPN BJT is reduced as well. Accordingly, SCR-nLDMOS with a shorter D_P width showed a better eSOA performance in Fig. 4.6. However, combining the information from Fig. 4.5(a) and 4.6, though reducing D_P width when embedding SCR to nLDMOS array is beneficial to eSOA, there is a limitation on the smallest applicable D_P width which comes from the condition of trigger competition between $Gate_{SCR}$ and $Gate_{MOS}$ fingers.



(a)



(b)

Fig. 4.7. Measured voltage waveforms when switching a 50-Ω resistive load under 24-V power supply voltage and a 0-to-6 V voltage pulse on gate. DUTs are (a) nLDMOS without embedded SCR and (b) SCR-nLDMOS with D_P of 50 μm. Both measured DUTs do not have the PBI layer. $Gate_{SCR}$ in the measured SCR-nLDMOS is short circuited to $Gate_{MOS}$.

Importance of the substantially narrowed SOA to the device reliability for circuit operation is shown in Fig. 4.7(a) and 4.7(b). In Fig. 4.7(a), an nLDMOS (without PBI) was used to drive a 50-Ω resistive load, which is common in analog circuit applications. As the measurement setup shown in the inset of Fig. 4.7(a), the 50-Ω resistor was biased at 24 V, and a 0-to-6 V V_{GS} pulse was applied to turn on and turn off the DUT. Measured V_{DS} and V_{GS}

waveforms in Fig. 4.7(a) show that the nLDMOS without PBI can safely drive the 50–Ω resistive load. However, when doing the same 50-Ω resistive load test on SCR-nLDMOS with D_P of 50 μm (without PBI), DUT was burned out after the measurement. As the measurement results shown in Fig. 4.7(b), measured V_{DS} drops to the holding voltage of the embedded SCR (~2 V) when the DUT starts to conducting current. SCR is triggered on during the circuit switching, so that the latchup-like failure happens, and the DUT can no longer be controlled by the gate bias. Accordingly, though inserting SCR to nLDMOS has been proven to substantially increase ESD robustness, the degraded SOA should be carefully examined to avoid device failure under normal circuit operating conditions.

4.3.3. $Gate_{SCR}$ bias to eSOA of SCR-nLDMOS (ggSCR-nLDMOS)

Because the channel current I_G which induces J_1 and J_2 currents in Fig. 4.2(b) has been identified as one of the major sources to trigger SCR, metal connection of $Gate_{SCR}$ was changed from being internally short circuited to $Gate_{MOS}$ to the source/body (ggSCR-nLDMOS). This keeps I_G equal to zero during normal circuit operating conditions and thus eliminates J_1 and J_2 in Fig. 4.2(b). Disadvantage of this ggSCR-nLDMOS configuration is obviously the reduced current driving capability, but since embedded SCR was centralized within only 4 out of 48 fingers, the reduced current driving capability can be easily compensated by increasing the total number of fingers in the output array. As the measurement results shown in Fig. 4.8, substantial improvement on eSOA was achieved simply by changing the $Gate_{SCR}$ connection. When $Gate_{SCR}$ was connected to $Gate_{MOS}$ (Fig. 4.6), the measured maximum V_{DS} ratings under 12-V gate bias for SCR-nLDMOS with PBI and D_P of 5, 10, and 50 μm are 15.37, 12.41, and 6.11 V, respectively. By changing the $Gate_{SCR}$ connection to the source/body, the measured maximum V_{DS} ratings under 12-V gate bias for D_P of 5, 10, and 50 μm in Fig. 4.8 are substantially increased to 37.42, 31.4, and 27.05 V, respectively.

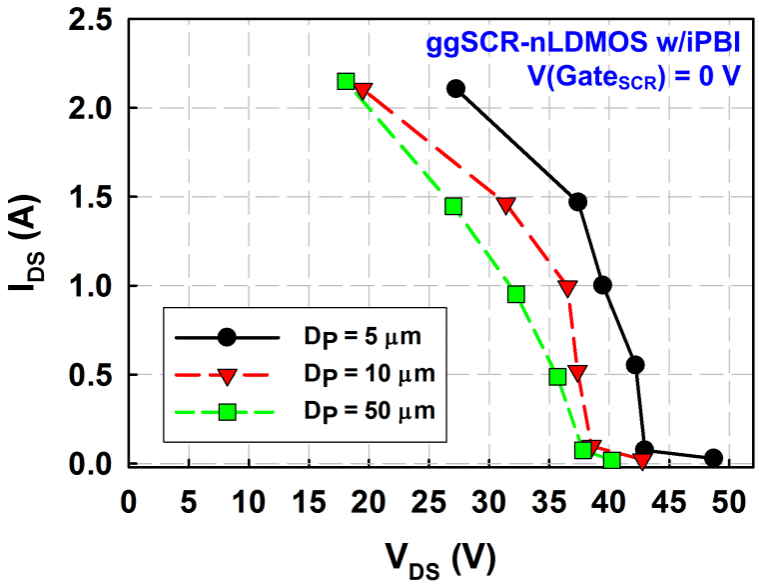


Fig. 4.8. Measured eSOA of ggSCR-nLDMOS ($Gate_{SCR}$ internally short to source/body). The corresponding gate biases for the I_{DS} from low to high were 0, 3, 6, 9, 12, and 16 V, respectively.

Despite that $Gate_{SCR}$ has been grounded to eliminate J_1 and J_2 currents, the measured eSOA boundaries in Fig. 4.8 still show a strong dependency to the gate biases. Moreover, a faster roll off on the measured V_{DS} ratings is observed under high gate biases. For example, the measured V_{DS} ratings in Fig. 4.8 for D_P of 10 μm decrease only from 38.53 to 36.53 V, when the gate bias was increased from of 3 and 9 V. However, the V_{DS} ratings suffer a much severer degradation from 31.4 to 19.47 V, when the gate bias was increased from 12 to 16 V. This suggests the existence of another factor affecting the triggering of embedded SCR, and this factor manifests stronger under high gate biases. In fact, because all fingers of an output array were drawn in a same HV N-Well, part of avalanche-generated electrons from $Gate_{MOS}$ fingers can drift through the shared HV N-Well. Since the N+ drain regions in $Gate_{SCR}$ fingers possess the same potential to drain of $Gate_{MOS}$ fingers, these drifting electrons can be collected by the N+ drain in $Gate_{SCR}$ fingers. These drifting electrons collected by N+ drain in $Gate_{SCR}$ fingers, as labeled in Fig. 4.2(b), therefore induce a voltage drop underneath the P+ anode of embedded SCR, allowing holes to emit from P+ anode. These emitting holes are

illustrated as J_3 current flow in Fig. 4.2(b). J_3 can be easily swept to grounded P+ body contacts to build up a voltage across base-emitter junction of the parasitic NPN BJT because of a wide depletion region in HV N-Well under high V_{DS} voltages. For example, ggSCR-nLDMOS with D_P of 50 μm in Fig. 4.8 has the measured V_{DS} rating of 18.08 V under 16-V gate bias, which is high enough to create a wide depletion region in HV N-Well in the studied 24-V process and help sweep the J_3 current toward grounded P+ body contacts.

For HV nLDMOS, it has been reported that effectiveness of channel current to accelerate the carrier multiplication process under high V_{DS} voltages can be relatively weak when gate biases are low. This comes from the mismatch on locations of the maximum current density and the maximum electric field under low gate biases. When the gate bias is high enough to induce channels underneath FOX, coincide of the channel current and the strong electric field start to accelerate the electron-hole pair generation. Therefore, it was observed that V_{t1} of HV NMOS only starts to roll off significantly under high gate biases. Accordingly, effect of this J_3 current due to drifting electrons becomes weak under low gate biases. Triggering of embedded SCR under low gate biases mainly comes from avalanche-generated electron-hole pairs in $Gate_{SCR}$ fingers themselves. Device breakdown voltage (I_{DS} at 1 μA when V_{GS} is 0 V) measured by 4155 parameter analyzer is ~35 V, and such measurement results show that this device breakdown voltage is irrelevant to D_P width. Under high gate biases, effect of J_3 becomes stronger because of a higher number of drifting electrons from $Gate_{MOS}$ fingers, and the measured V_{DS} ratings start to roll off below 35 V with a faster speed, as shown in Fig. 4.8.

4.4. Poly Bending Structure to SCR-nLDMOS

Despite a remarkably wider eSOA has been achieved by eliminating J_1 and J_2 currents through connecting $Gate_{SCR}$ to ground, the J_3 current still cause some degradation on eSOA performance especially under high gate biases. To further improve the eSOA and alleviate the degradation due to J_3, a new poly bending (PB) layout structure for SCR-nLDMOS arrays

(PB-SCR-nLDMOS) has been proposed. For all studied PB-SCR-nLDMOS, D_P width was kept at 50 μm and devices were drawn with PBI layer.

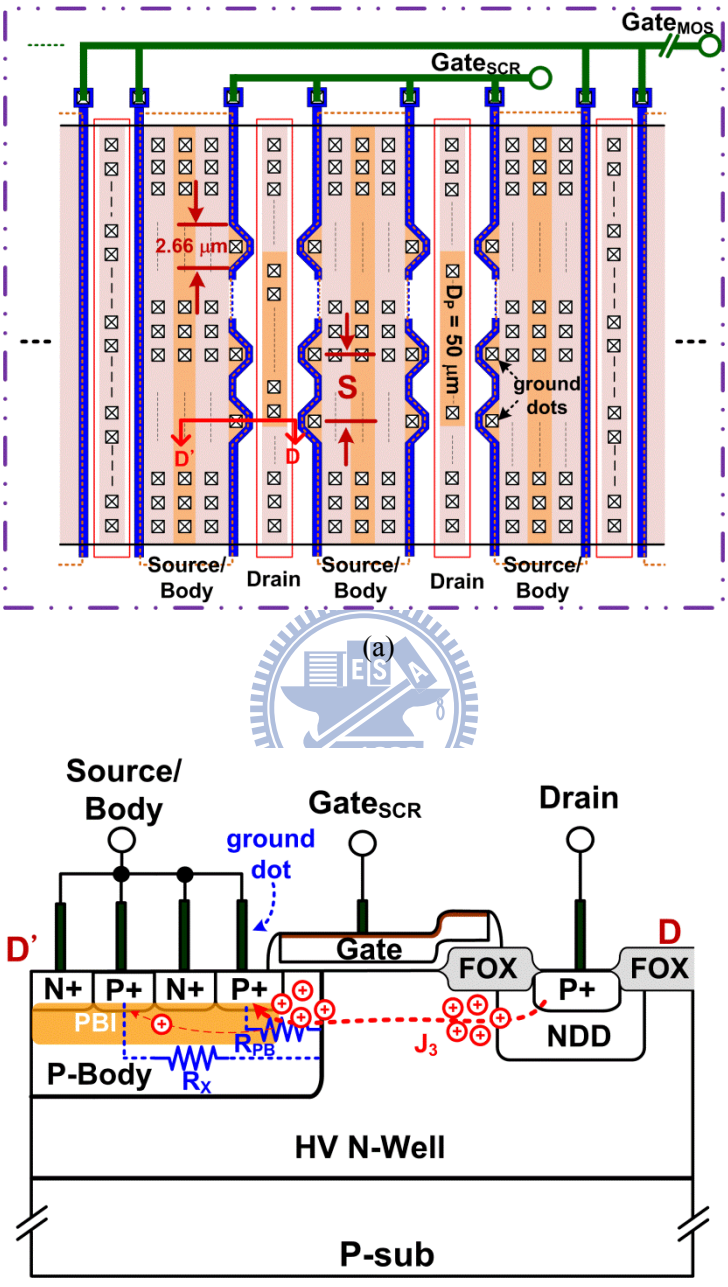


Fig. 4.9. (a) Layout top view and (b) cross-sectional view along D-D' line of SCR-nLDMOS with the proposed poly bending structure. Widths and spacings in figures are not drawn to scale.

In the poly bending layout, $Gate_{SCR}$ has been modified from a straight poly line from top to bottom of drain regions to part of a straight poly line in parallel with N+ drain but several

trapezoids in parallel with P+ drain, as the layout top view of a PB-SCR-nLDMOS shown in Fig. 4.9(a). By bending the poly gate in layout, additional P+ diffusion regions filling trapezoids can be inserted at source side. Each trapezoid region was drawn with one contact (ground dot) connecting to source/body. The bottom length of every trapezoids is 2.66 μm (top edge of P+ to bottom edge of P+), and the pitch between two adjacent ground dots is defined as S in the layout of Fig. 4.9(a).

Device cross-sectional view along D-D' line in Fig. 4.9(a) is shown in Fig. 4.9(b). When the emitting holes from P+ anode are swept toward the ground potential (the J_3 current flow), most of the emitting holes are collected by the ground dot because its parasitic resistance R_{PB} is smaller than the parasitic resistance R_X from P-body/PBI to the P+ body contact, as shown in Fig. 4.9(b). Moreover, holes collected by the ground dots do not build up the voltage underneath N+ source, *i.e.* do not help forward bias the base-emitter junction of NPN BJT. Accordingly, only a small part of J_3 that is not collected by the ground dot can help trigger embedded SCR, which, in turn, substantially alleviates the degradation on eSOA due to the J_3 current flow.

Measured eSOA for PB-SCR-nLDMOS arrays are shown in Fig. 4.10. For comparison, the measured eSOA of ggSCR-nLDMOS with D_P of 50 μm in Fig. 4.8 is also included in Fig. 4.10 and labeled as ggSCR-nLDMOS. In Fig. 4.10, PB structures that have $Gate_{SCR}$ connected to $Gate_{MOS}$ show narrower eSOA boundaries compared to that of ggSCR-nLDMOS when S are 10 and 15 μm. When S is reduced to 5 μm, PB structure (with $Gate_{SCR}$ connected to $Gate_{MOS}$) shows a better eSOA performance than that of ggSCR-nLDMOS in Fig. 4.10. In the studied PB structures, because the bottom length of a trapezoid is 2.66 μm, S of 15 μm indicates that there is a 12.34-μm long straight poly line between two ground dots to induce J_1 and J_2 currents and to further trigger on the embedded SCR when $Gate_{SCR}$ is connected to $Gate_{MOS}$. When S is larger than 5 μm, J_1 and J_2 currents dominate the triggering mechanism of embedded SCR, so that measurement results for PB

with S of 10 and 15 μm are inferior to ggSCR-nLDMOS in Fig. 4.10. However, by comparing the eSOA of SCR-nLDMOS with 50-μm D_P and PBI in Fig. 4.6, and the eSOA of PB-SCR-nLDMOS with S of 10 and 15 μm in Fig. 4.10, improvement on eSOA by using the poly bending layout structure is still noticeable. This result comes from the fact that the ground dots introduce another parasitic resistor R_{PB} in parallel with the R_X resistor in Fig. 4.4, which widens the eSOA boundary by making base-emitter junction of parasitic NPN BJT harder to be forward biased. When S is reduced to 5 μm, the straight poly line between two adjacent ground dots which can induce J_1 and J_2 currents is greatly reduced to 2.34 μm. Note that there is no channel current flowing widthwise along the trapezoidal regions because of the P+ region in ground dots to cut off electron current flow (Fig. 4.9(b)). A better eSOA performance is therefore observed when S is reduced to 5 μm.

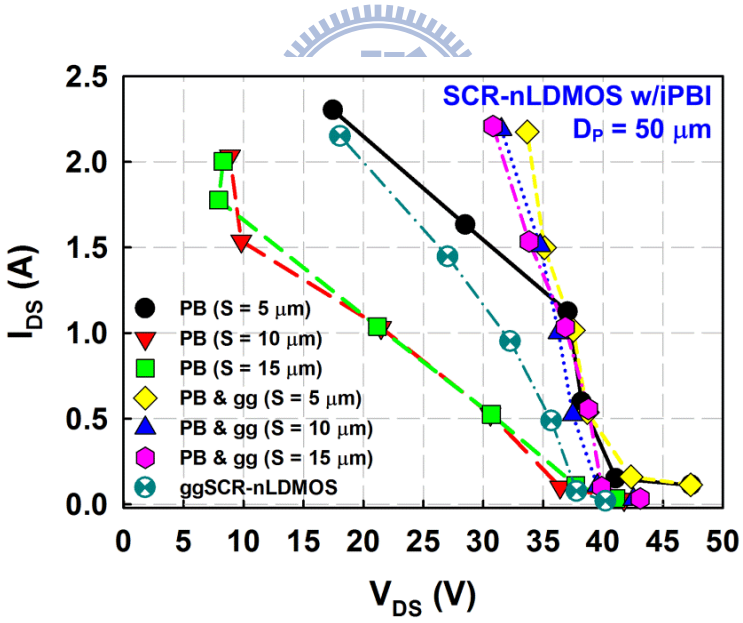


Fig. 4.10. Performance of poly bending structure on eSOA of SCR-nLDMOS. The "PB" devices have poly bending structure with $Gate_{SCR}$ internally connected to $Gate_{MOS}$. The "PB & gg" devices have poly bending structure with $Gate_{SCR}$ internally connected to source/body. The corresponding gate biases for the I_{DS} from low to high were 0, 3, 6, 9, 12, and 16 V, respectively.

When $Gate_{SCR}$ is connected to source/body to rule out the effects from J_1 and J_2, effectiveness of the poly bending structure on suppressing J_3 starts to manifest clearly.

Substantially widened eSOA boundaries, especially under high gate biases, have been observed from the measurement results in Fig. 4.10 (PB & gg devices). Measured V_{DS} ratings for PB & gg devices in Fig. 4.10 under 16-V gate bias are 30.81, 31.52, and 33.67 V for S of 15, 10, and 5 μm, respectively. In summary, grounding $Gate_{SCR}$ fingers not only blocks J_1 and J_2 currents, but also benefits from the reduced surface field (RESURF) effect of poly field plate in $Gate_{SCR}$ fingers. The additional P+ ground dots in poly bending structure further reduce the bipolar beta gain and lower the base resistance of parasitic NPN BJTs. With above reasons, the eSOA of SCR-nLDMOS can be greatly improved by using the poly bending layout structure with grounded $Gate_{SCR}$ fingers.

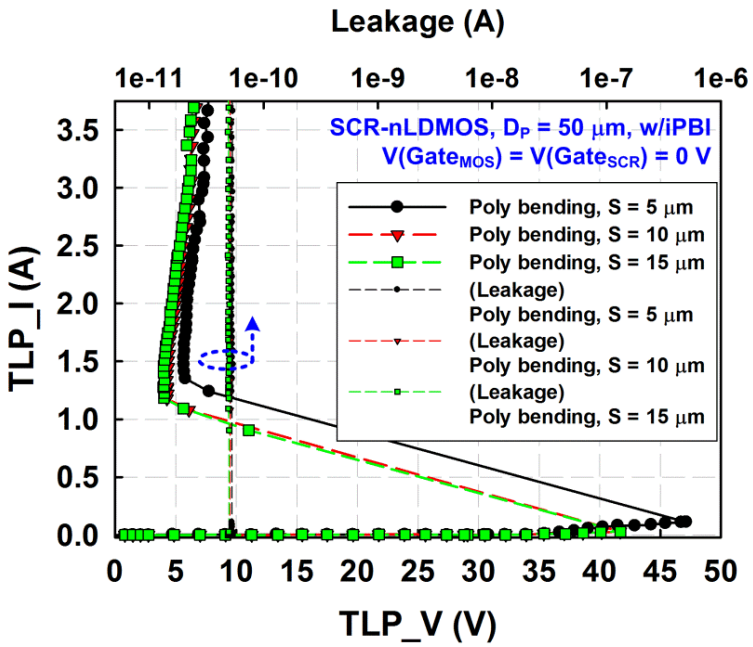


Fig. 4.11. Measured TLP I-V characteristics of poly bending SCR-nLDMOS with different S spacings. Gate bias for all DUTs was 0 V and the leakage currents were monitored under 24-V drain bias.

TLP-measured I-V characteristics for PB-SCR-nLDMOS with D_P of 50 μm are shown in Fig. 4.11. All measured devices in Fig. 4.11 have I_{t2} higher than the equipment limitation of 3.75 A. Measured holding voltages (V_h) for PB-SCR-nLDMOS with S of 15, 10, and 5 μm in

Fig. 4.11 are 3.99, 4.26, and 5.67 V, respectively. Measured V_h for SCR-nLDMOS with D_P of 50 μm in Fig. 4.5(b) is 2.14 V. Accordingly, from the viewpoint of power dissipation during ESD stresses, poly bending structure is expected to have some negative impact on the ESD robustness. However, because the measured HBM ESD robustness for all DUTs in Fig. 4.11 is higher than 8 kV, the PB-SCR-nLDMOS arrays are still extremely robust against ESD stresses.

4.5. Summary

In HV technologies, output arrays with embedded SCR are usually adopted for on-chip ESD protection. However, a substantially narrowed eSOA has been found due to the insertion of SCR into HV nLDMOS. Embedding SCR therefore may jeopardize the reliability of output arrays during normal circuit operating conditions, even though it provides a superior ESD robustness to protect output array. Experimental results showed that SCR insertion with small but multiple P+ segments can help alleviate the degradation on eSOA. By grounding the gates of fingers in the embedded SCR, eSOA can be substantially widened. But, drifting electrons due to carrier multiplication process from adjacent conducting fingers can still result in a roll off on the maximum V_{DS} rating, especially under high gate bias conditions. Through the proposed poly bending structure, impact from these drifting electrons can be mitigated and a further widened eSOA has been achieved. With the high ESD robustness and greatly widened eSOA boundaries shown in this chapter, the poly bending layout structure with a proper gate connection has been verified as a promising design technique to enhance reliability of high voltage output arrays with embedded SCR.

Chapter 5

New Ballasting Layout Schemes to Improve ESD Robustness of I/O Buffers in Fully-Silicided CMOS Processes

5.1. Background

To increase the driving capability and the maximum operating frequencies of MOSFETs, silicidation has been widely adopted in chip fabrications since deep-submicron CMOS era. In the fully-silicided CMOS technologies, the silicidation is typically carried out through metallurgical reaction between silicon and the pre-deposited silicide metal (Titanium, Cobalt, or Nickel) [82]–[85]. With proper annealing steps, refractory metal silicides are formed to provide a low resistivity for the diffusions and poly silicon gates of MOSFETs.

Although the low resistivity from silicides is advantageous to the driving capability and operating frequencies of MOSFETs, it has been reported that silicidation induces electrostatic discharge (ESD) degradation due to the current crowding within a shallow surface [86]. Moreover, the bend-down of silicidation located near the shallow trench isolation (STI) corner leads to deterioration of ESD robustness of fully-silicided devices [87]. Owing to these effects during ESD stresses, silicidation has been confirmed to result in precipitous degradation on ESD protection levels of CMOS ICs in advanced CMOS technologies.

To recover the silicidation-induced degradation on ESD robustness, CMOS processes with additional silicide blocking (SB) has been proposed [88]–[94]. Because the temperature for silicon dioxide (SiO_2) to form metallurgical silicides is higher than that for silicon, SB can be achieved by depositing sacrificial oxide on the selected regions before the deposition of silicide metal. The sacrificial oxide therefore separates the contact between silicon and the silicide metal, preventing these selected regions from silicidation during the subsequent

annealing processes. By using the SB on ESD protection devices, ESD robustness of CMOS ICs can be restored without affecting the operating speed of internal circuits. However, to deposit the sacrificial oxide and to define the selected regions for silicide blocking, additional mask and process steps are required. As a result, introducing SB into the CMOS manufacturing processes will increase the fabrication cost. To compromise with the fabrication cost, or owing to the inaccessibility of SB in some given process technologies, some cost-effective ballasting techniques have been proposed to improve ESD robustness of fully-silicided MOSFETs [95]–[108].

The mechanism and previous works of ballasting techniques on fully-silicided MOSFETs are briefly reviewed in this chapter. Two new ballasting layout schemes are proposed to effectively improve ESD robustness of I/O buffers with fully-silicided NMOS and PMOS transistors. Experimental results from real IC products fabricated in a 0.35-μm fully-silicided CMOS process have confirmed that the new ballasting layout schemes can successfully increase HBM ESD robustness of fully-silicided I/O buffers from the original 1.5 to over 6 kV without using the additional silicide-blocking mask. Moreover, by using the new proposed ballasting layout schemes, no additional layout area of I/O buffers is required, compared to that drawn with the traditional silicide-blocking technique [97].

5.2. Review on Ballasting Techniques for Fully-Silicided I/O Buffers

Due to the huge discharging current in ESD events, current crowding has been known to cause serious impact on ESD protection devices. By increasing the ballast resistance in the ESD protection MOSFETs, ESD current path can be spread deeper into the substrate of large volume, which in turn improves ESD robustness [86]. Moreover, sufficient ballast resistance can improve the turn-on uniformity of ESD protection NMOS with multi-fingers in layout.

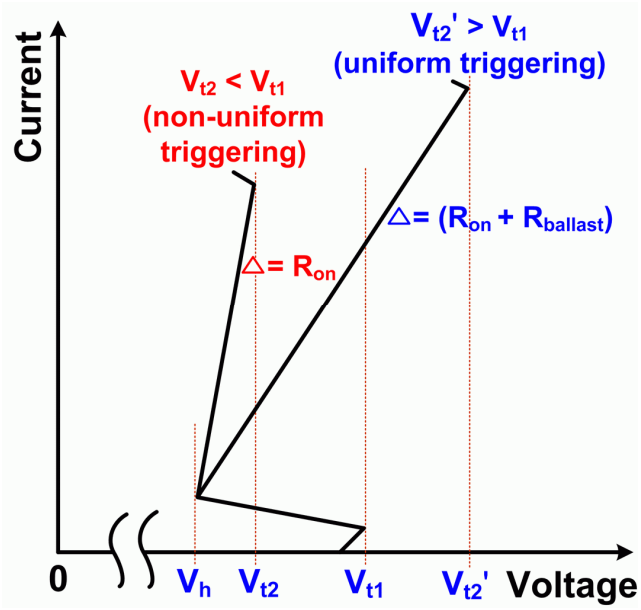


Fig. 5.1. Current-voltage (I-V) characteristics of gate-grounded NMOS for ESD protection, indicating the relation between V_{t2} and V_{t1} values to the uniform or non-uniform triggering.

In a multi-finger NMOS, different distances from the drain region of each finger to the grounded guard ring result in asymmetry of substrate resistance, which causes the central fingers of NMOS to be more easily triggered on under ESD stresses [26]. After the triggering of the multi-finger NMOS under ESD stresses, the ESD overstress voltage is clamped to its holding voltage (V_h) plus the product of ESD current (I_{ESD}) and the turn-on resistance (R_{on}). The typical I-V curve of gate-grounded NMOS under ESD stress is illustrated in Fig. 5.1. Without sufficient ballast resistance, ($I_{ESD} \times R_{on}$) is not large enough to make the secondary breakdown voltage (V_{t2}) higher than the trigger voltage (V_{t1}). As a result, ESD current is concentrated in some earlier turned-on area to cause local damages but the rest area cannot be triggered on in time to discharge ESD current. Such non-uniform turn-on behavior among the multiple fingers of NMOS limits its ESD robustness, even if the NMOS was drawn with a large device dimension. By introducing the ballast resistance $R_{ballast}$, turn-on resistance of the multi-finger NMOS can be increased from R_{on} to (R_{on} + $R_{ballast}$). As long as the V_{t2}' can be increased greater than V_{t1}, the multi-finger NMOS can be uniformly triggered on during ESD

stresses [109]. As a result, sufficient ballast resistance can force ESD current being conducted into the deeper substrate, and also increase the ESD robustness due to the improvement of turn-on uniformity among the multiple fingers of gate-grounded NMOS.

To realize the ballast resistance in fully-silicided NMOS, one of the layout methods is to use the high sheet resistance from N-Well. Fig. 5.2 shows the device cross-sectional view of an NMOS with the N-Well ballasting technique. The ballast N-Well electrically shorts the separated diffusions and contributes the desired $R_{ballast}$ to the overall turn-on resistance of NMOS [95]–[97]. The holding voltage and the trigger voltage of NMOS may be also increased due to the insertion of ballast N-Well. For the facility of description, the separated diffusion that connects to the input/output (I/O) pad is labeled as the island diffusion in this chapter. The other separated diffusion, which is closer to the gate of MOSFET, is labeled as the drain diffusion. Isolation in figures of this chapter represents either field oxide (FOX) or STI.

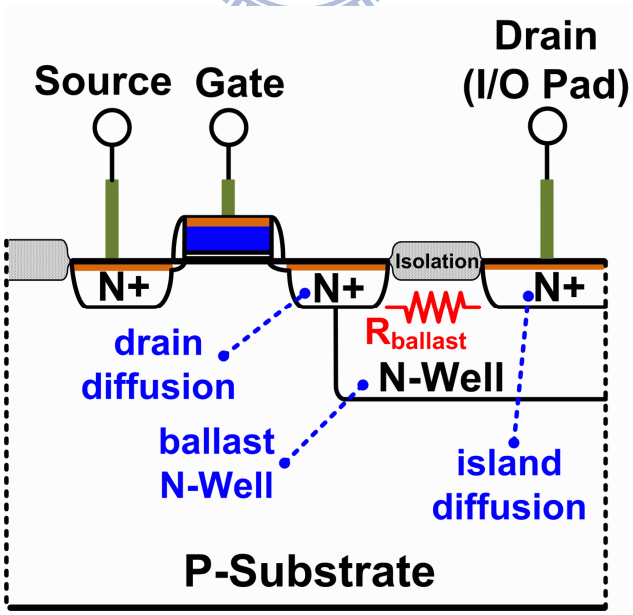
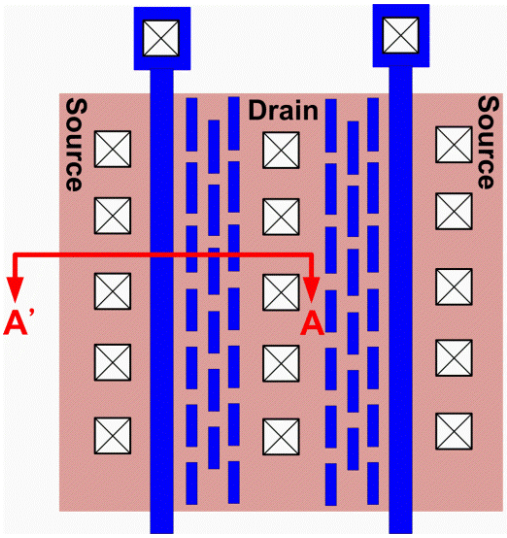


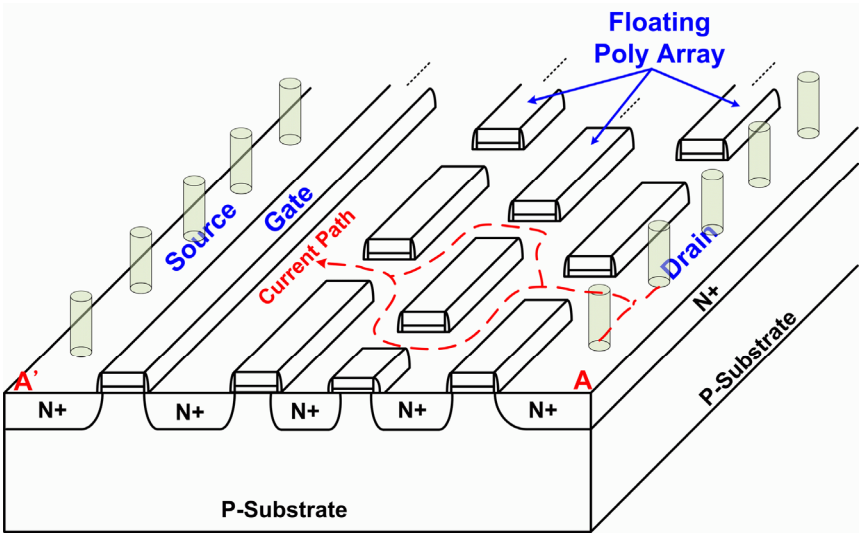
Fig. 5.2. Ballast N-Well to increase the ballast resistance of NMOS. The separated diffusion region that connects to I/O Pad is labeled as island diffusion, and the diffusion region that closer to the gate is labeled as drain diffusion.

Although the ballast N-Well is useful to increase ESD robustness of fully-silicided NMOS, it makes layout area to expand due to the process ability of defining the minimum spacing between two adjacent diffusion regions. Generally, technology nodes with isolation of local oxidation of silicon (LOCOS) ask for larger spacing for two adjacent diffusion regions than those with STI isolation because of the bird's beak encroachment during wet oxidation [110]. With the finest process controllability over the gate length in CMOS technologies, replacing the separation between island and drain diffusions from FOX (or STI) to dummy poly gate minimizes the spacing between two adjacent diffusion regions [98], [99]. Although the N-Well ballasting technique is useful and easy to be utilized on fully-silicided NMOS, it cannot be applied to fully-silicided PMOS which is implemented in the N-Well.

In CMOS technologies, the resistance from a single contact, via, or interconnects keeps increasing due to the constant shrinkage on either horizontal or vertical dimensions [111]. As a result, some ballasting techniques with back-end elements were used to build up the ballast resistance without increasing the process complexity [100]–[104]. By stacking as many metal layers as possible to construct a vertically meandering ESD current path, the back-end-ballast (BEB) technique is simple to increase the ballast resistance in the ESD protection MOSFETs. Poly BEB and contact ballasting (CTB) techniques further segment the current conduction path into several parallel branches, and insert polysilicon or diffusion resistors in series with every back-end segmentation to facilitate the ballast of BEB technique [100]–[103]. When a local segment starts to suffer current crowding, the poly or diffusion resistor on the segment induces current defocus feedback, which forces ESD current to redistribute and hence improves the turn-on uniformity during ESD stresses [100], [104].



(a)



(b)

Fig. 5.3. The (a) layout top view and (b) device cross-sectional view along A-A' line of the fully-silicided NMOS with floating poly array (FPA) technique [107].

To further shrink the layout area of the fully-silicided MOSFETs due to the additional polysilicon resistor in the poly BEB technique, the active-area-segmentation (AAS) technique has been proposed [104]. In the AAS technique, source or drain regions are segmented to diffusion stripes to ballasts the MOSFET for ESD protection with current defocus feedback. Moreover, the AAS technique holds the potential of featuring extremely compact layout area.

The bulk coupling effect therefore alleviates the non-uniform triggering and increases the ESD robustness of MOSFETs [112]. Effectiveness of the bulk coupling effect has been confirmed by floating the body of NMOS under ESD stresses [113].

Besides, some ballasting methods manage to increase the ballast resistance by creating a horizontally meandering current path on diffusion regions, such as the staggered diffusion technique [106] and the floating poly array (FPA) technique [107]. As the layout top view of FPA technique shown in Fig. 5.3(a), the interlaced floating poly array intervenes in the straightforward current path along A-A'. The current flow path is therefore forced to wind within the FPA as indicated in Fig. 5.3(b), which increases the equivalent ballast resistance to improve ESD robustness.

From the previous works, sufficient ballast resistance drives ESD current deeper into substrate to gain better heat dissipation. The ballast resistance contributes to the overall turn-on resistance, which fulfills the ($V_{t2} > V_{t1}$) condition to enhance the turn-on uniformity of NMOS under ESD stresses. Even in the condition of ($V_{t2} < V_{t1}$), current defocus feedback and bulk coupling effect can still prevent MOSFETs from being easily filamented during ESD events.

5.3. Fully-Silicided I/O Buffers under ESD Stresses

Because there are four ESD test modes at an I/O pad, both the NMOS and the PMOS in an I/O buffer are susceptible to ESD failure. For example, the PS-mode ESD tests can lead to breakdown of the driver NMOS whereas the ND-mode ESD tests can lead to breakdown of the driver PMOS. Though the whole-chip ESD protection scheme equipped with power rail ESD clamp circuit is effective to discharge ESD energy by avoiding junction breakdown of I/O buffers [6], the overshooting or undershooting voltage are still harmful to the I/O buffer, especially under the conditions with high ESD stress voltage.

In this section, effectiveness of the N-Well ballasting technique to whole-chip ESD

robustness of fully-silicided I/O buffers is investigated. Chips are fabricated in a 0.35-μm 5-V fully-silicided CMOS process with LOCOS isolation. Silicide blocking is not available in this process due to the consideration of cost reduction. Because the N-Well ballasting technique cannot be applied to PMOS, the driver PMOS in the I/O buffer discussed in this section was left un-ballasted. All I/O buffers are self-protected, which have no additional ESD protection device connected to the I/O pad. The whole-chip ESD protection scheme with the corresponding device dimensions are illustrated in Fig. 5.4. Operating frequency specification of the I/O buffers is 20 MHz. The main ESD protection NMOS (M_{N2}) in the active power-rail ESD clamp circuit has a total device dimension (W/L) of 1680 μm/1.25 μm. For fully-silicided I/O buffers without ballasting, no ballasting technique was applied to M_{N2} of the power-rail ESD clamp circuit. With the proposed layout schemes, the N-Well ballasting technique was also applied to M_{N2} of the power-rail ESD clamp circuit when the N-Well ballasting technique was applied in the I/O buffers.

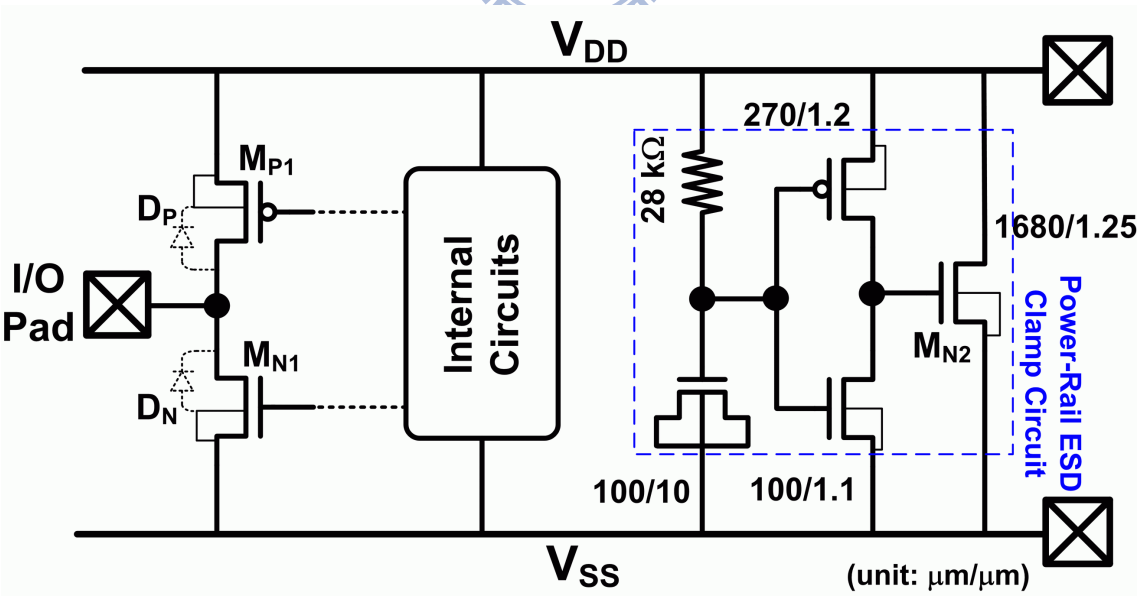


Fig. 5.4. Whole-chip ESD protection scheme and the corresponding device dimensions of the power-rail ESD clamp circuit.

Target for ESD robustness of those IC products requested by customers is to pass 6-kV HBM ESD test. To verify ESD robustness, the starting voltage of HBM ESD test is 0.5 kV, and the step voltage during ESD tests is 0.5 kV. Each pin is stressed three times with the specified HBM ESD level and the failure criterion is an over 20% I-V shift compared to the original I-V curve before ESD stress. The test will stop when ESD failure happens on one or more I/O (including power) pin(s).

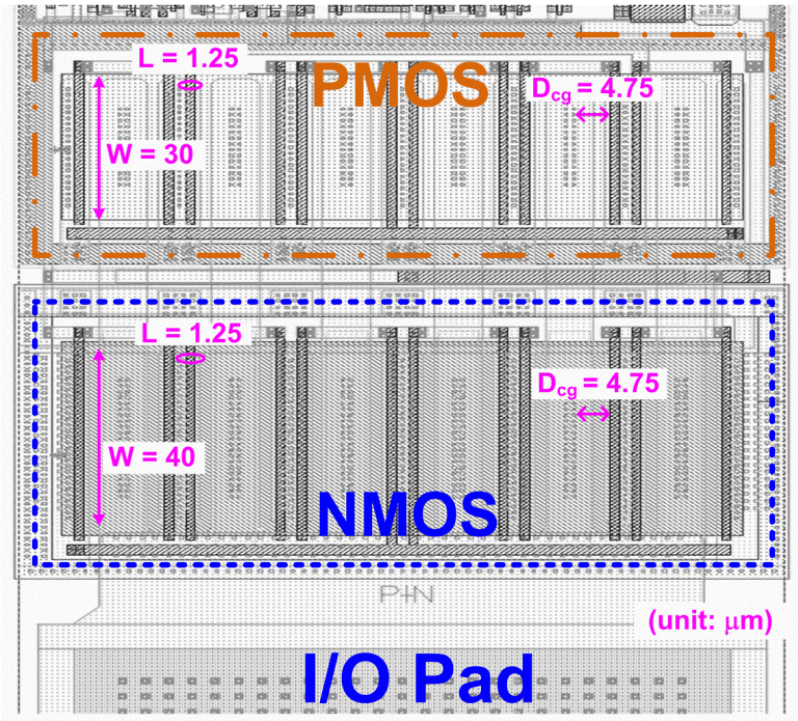


Fig. 5.5. Layout top view of the self-protected fully-silicided I/O buffer in a CMOS IC product.

5.3.1. Fully-Silicided I/O Buffer Without Ballasting

In nowadays CMOS ICs, to minimize the required layout area for I/O buffers, self-protected I/O design (I/O buffer without additional ESD protection devices) is usually adopted. Layout of the self-protected I/O buffers in a CMOS IC product is shown in Fig. 5.5. Gate length in the I/O buffer is increased to avoid the reverse channel length dependency [114]. Device dimension of the driver NMOS (M_{N1}) is 480 μm / 1.25 μm with each finger width of 40 μm, and device dimension of the driver PMOS (M_{P1}) is 360 μm / 1.25 μm with each finger width of 30 μm. Both NMOS and PMOS have drain contact to poly gate edge

(D_{cg}) of 4.75 μm, which is originally drawn for silicide-blocking rules. However, to reduce the fabrication cost, no silicide-blocking is adopted in the given CMOS process for IC production. The main ESD protection NMOS in the active power-rail ESD clamp circuit has the same layout style as that of the driver NMOS in I/O buffer.

TABLE 5.1
ESD ROBUSTNESS AMONG THE I/O BUFFERS

	HBM ESD Robustness (unit: kV)				
	PS-mode	PD-mode	NS-mode	ND-mode	V_{DD}-to-V_{SS}
Fully-Silicided I/O Buffer without Ballasting	1.5	2.5	> 8	4.5	> 8
I/O Buffer with N-Well Ballasting Technique on NMOS	7	> 8	> 8	4	> 8
I/O Buffer with the New Proposed Type-A Layout Scheme	6	6	> 8	> 8	> 8
I/O Buffer with the New Proposed Type-B Layout Scheme	7	> 8	> 8	> 8	> 8

ESD test results in Table 5.1 show that the fully-silicided I/O buffers without ballasting failed to pass the essential ESD specification of 2-kV HBM ESD stresses. Among the ESD measurements of the un-ballasted I/O buffers, PS-mode ESD test has the lowest ESD protection level. Under the PS-mode ESD stresses, the ESD current is first discharged to V_{DD} through the forward diode D_P inherent in M_{P1}, and to the grounded V_{SS} through the power-rail ESD clamp circuit. In spite of the gate driven technique to enhance turn-on speed of the power-rail ESD clamp circuit during ESD stresses [115], [116], the overshooting voltage on the I/O pad cannot be completely suppressed due to the inevitable turn-on resistance of devices and interconnects. Consequently, for lack of proper ballasting design, when the overshooting voltage on the I/O pad induces breakdown on the fully-silicided driver NMOS, it is easily filamented due to severe current crowding and non-uniform triggering.

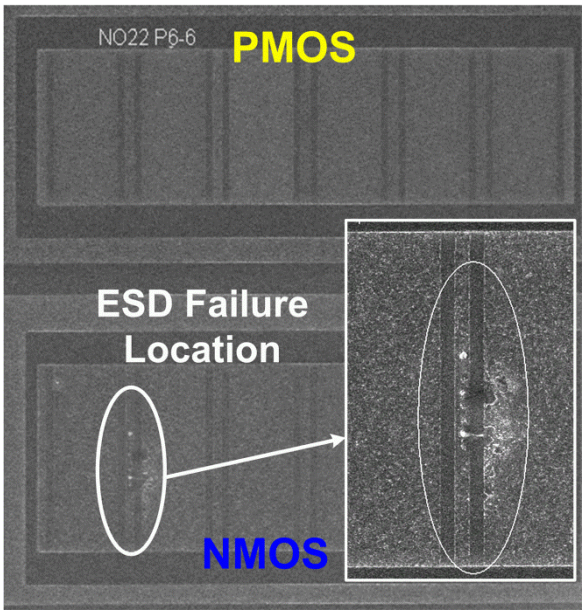


Fig. 5.6. SEM image of the fully-silicided I/O buffer without ballasting after 2-kV PS-mode ESD stress. ESD failure is found on only one finger of the driver NMOS. Current filamentation is also observed on the surface of the driver NMOS without ballasting.

SEM image of the un-ballasted I/O buffer after 2-kV PS-mode ESD stress is shown in Fig. 5.6, where the trace of current filamentation is found on the driver NMOS. The failure analysis (FA) result has verified that the driver NMOS is driven into breakdown during the 2-kV PS-mode ESD test. Non-uniform triggering among the multiple fingers of the un-ballasted driver NMOS can also be clearly observed in Fig. 5.6, since ESD failure only locates on one of the fingers. The surface burned-out trace from drain to the grounded source further indicates insufficient ballast resistance to make ESD current crowding within limited shallow depths. Accordingly, the D_{cg} spacing of 4.75 μm in a fully-silicided NMOS is insufficient to provide adequate ballast resistance due to the small sheet resistance from silicides.

5.3.2. I/O Buffer with N-Well Ballasting Technique on Driver NMOS

To enhance the PS-mode ESD robustness, the N-Well ballasting technique was applied to the driver NMOS of I/O buffer [95]. The main ESD protection NMOS (M_{N2}) in the active

power-rail ESD clamp circuit was also implemented with N-Well ballasting. The driver PMOS was still left un-ballasted in this test. Fig. 5.7 shows the diagram of the I/O buffer with a sketch of its metal connection to the I/O pad. To keep the same cell width of I/O buffers in IC chips, both Dcg spacing and gate length are kept the same as those in the I/O buffers without ballasting. Spacing for island diffusion and drain diffusion is 1.75 μm in layout. In the I/O buffers with N-Well ballasting, each finger width of driver NMOS is 30 μm, and each finger width of driver PMOS is 25 μm. The total device dimension (W/L) of NMOS (PMOS) in I/O buffer is 360 μm / 1.25 μm (300 μm / 1.25 μm). Driver NMOS with ballast N-Well in this test was laid out with truncation to the island diffusions to prevent ESD damage from the tips of N+ island diffusions to the P+ guard ring. With the foundry-provided N-Well sheet resistance of 800Ω/□, the overall resistance imposed on NMOS (with 12 fingers in parallel) due to the ballast N-Well is 800 Ω × (1.75 μm/30 μm) ÷ 12 = 3.88 Ω. With the operating frequency specification of 20 MHz, the driving capability can be effectively compensated by transistor sizing to meet the desired specification of I/O applications. For example, the output resistance of a driver NMOS with 12-mA driving specification is 0.4 V ÷ 12 mA = 33.33 Ω, which is much higher than the 3.88-Ω parasitic resistance from ballast N-Well.

Moreover, the parasitic junction capacitance (C_j) and sidewall capacitance (C_{jsw}) of N-Well/P-Substrate junction are 1.08×10^{-4} and 7.32×10^{-4} pF/μm, respectively. C_j and C_{jsw} of N+/P-Substrate junction are 6.19×10^{-4} and 2.58×10^{-4} pF / μm, respectively. Although the C_{jsw} value for N-Well is higher than the C_{jsw} value for N+ diffusion, the C_j value for N-Well is much lower than the C_j value for N+ diffusion due to the larger depletion width of N-Well/P-Substrate junction. For self-protected driver NMOS, due to the large device width and the increased drain contact to poly gate spacing, the C_j value will take a major portion in the overall junction capacitance. As a result, the added capacitance due to ballast N-Well can be small and does not affect the I/O operating frequency specification of 20 MHz.

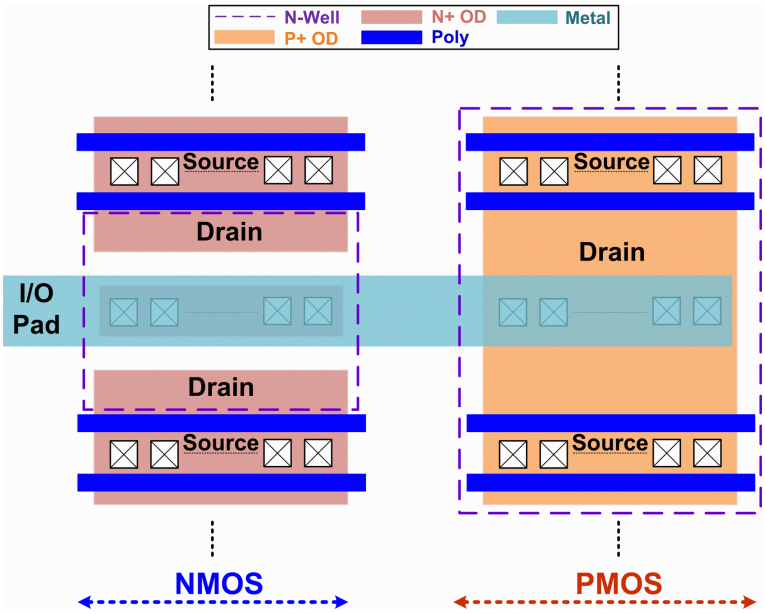


Fig. 5.7. Diagram to show the metal connection to the I/O pad for the driver NMOS with ballast N-Well but the driver PMOS without ballasting.

ESD measurement results for the I/O buffers with N-Well ballasting technique are shown in Table 5.1. Although N-Well ballasting technique substantially increases PS-mode ESD robustness to 7 kV, the 4-kV ND-mode ESD test result has become the bottleneck for the I/O buffers to achieve the performance target of 6-kV HBM ESD robustness.

During the ND-mode ESD tests, ESD current is discharged through the power-rail ESD clamp circuit and the forward diode D_N inherent in the driver NMOS. As a result, the voltage across the V_{DD} and I/O pad is

$$\Delta V_{ND} = [I_{ESD} \times (R_{on,\ Power\text{-}Rail} + R_{VSS} + R_{on,\ DN}) + V_{t,\ DN}] \quad , \qquad (5.1)$$

where the $R_{on,\ Power\text{-}Rail}$ and $R_{on,\ DN}$ denote the turn-on resistance of power-rail ESD clamp circuit and the diode D_N during ESD stresses; R_{VSS} denotes the effective resistance of the V_{SS} interconnection, and $V_{t,\ DN}$ is the cut-in voltage of the diode D_N. At high I_{ESD} level, *i.e.* high ESD stress voltage, the ΔV_{ND} can exceed V_{t1} of the driver PMOS and induce triggering of the parasitic PNP BJT in the PMOS. As a result, part of the ESD current is discharged through the driver PMOS under high ESD current conditions. For lack of proper ballasting, ESD

current discharged through the driver PMOS is crowded within the shallow surface, which further deteriorates the ESD robustness of driver PMOS. For I/O buffers with N-Well ballasting technique on driver NMOS, the PMOS has smaller device width than that in the fully-silicided I/O buffers. Accordingly, though driver PMOS in the two structures are both fully-silicided without ballasting, I/O buffer with N-Well ballasting technique on driver NMOS has lower ND-mode ESD robustness (4 kV) compared to ND-mode ESD robustness of fully-silicided I/O buffer without ballasting (4.5 kV).

SEM image of the I/O buffer after 4.5-kV ND-mode ESD stress is shown in Fig. 5.8. Current traces from source of the driver PMOS toward its drain regions are observed, which confirms that breakdown of the un-ballasted driver PMOS is the limitation to ESD robustness of I/O buffer with N-Well ballasting technique. Failure spots are found within more than one of the PMOS fingers because PMOS devices barely exhibit snapback phenomenon in deep-submicron CMOS technologies [86].

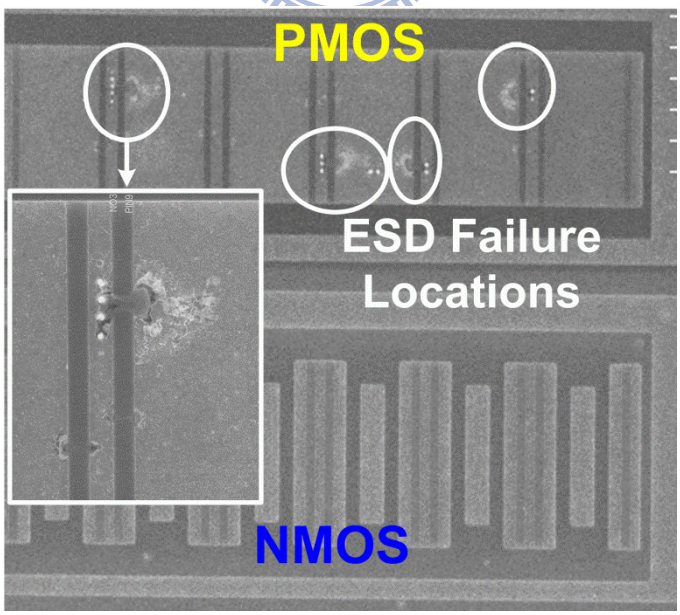


Fig. 5.8. SEM image of the fully-silicided I/O buffer with N-Well ballasting technique on the driver NMOS after 4.5-kV ND-mode ESD stress. Failure locations are found on the driver PMOS due to the triggering of parasitic BJT in PMOS.

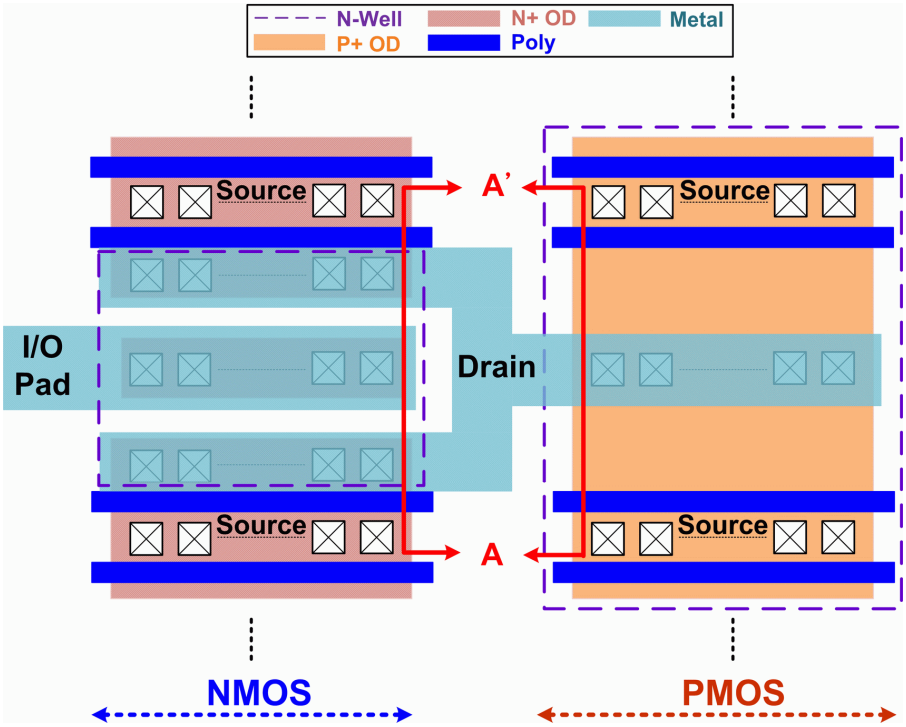


Fig. 5.9. Diagram to show the metal connection to the I/O pad for the driver NMOS realized with type-A layout scheme.

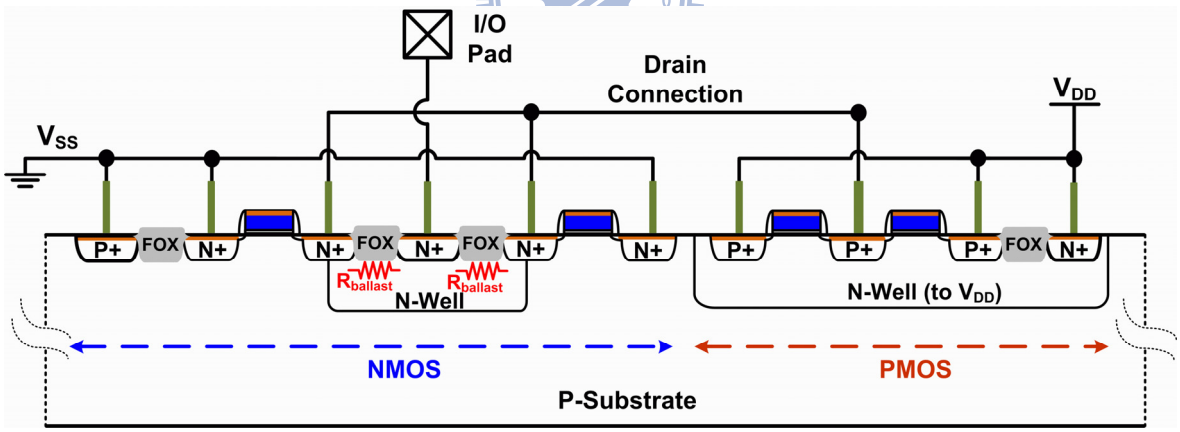


Fig. 5.10. Cross-sectional view along A-A' line of the fully-silicided I/O buffer realized with the type-A layout scheme.

5.4. New Layout Schemes for Fully-Silicided I/O Buffers

Though the N-Well ballasting technique prevents PS-mode ESD failure on the driver NMOS and increases the whole-chip ESD protection level from 1.5 to 4 kV, it still fails to meet the adequate performance target of 6-kV HBM ESD robustness. From the ESD

measurement and FA results, ballasting technique on the driver PMOS is vital to the improvement of ESD robustness on fully-silicided I/O buffers. As a result, two new layout schemes are proposed to ballast both NMOS and PMOS devices in the I/O buffer. The new proposed designs have been verified in some IC products fabricated in the same 0.35-μm 5-V fully-silicided CMOS process, and have been confirmed with substantial improvement on the whole-chip ESD protection level.

5.4.1. I/O Buffer with The New Proposed Layout Scheme (Type A)

To provide efficient ballast on the driver PMOS, Fig. 5.9 shows the diagram of type-A layout scheme. The driver NMOS in the type-A layout scheme is drawn with N-Well ballasting. However, the drain of the driver PMOS is not connected directly to the I/O pad. Instead, drain of the PMOS is connected to the drain diffusion of the driver NMOS, which is electrically connected to the I/O pad by means of the ballast N-Well. The driver NMOS and PMOS in the type-A layout scheme have the same device dimensions as those in the I/O buffers with N-Well ballasting technique on driver NMOS. The main ESD protection NMOS (M_{N2}) of the power-rail ESD clamp circuit in this scheme is N-Well ballasted. Device cross-sectional view along A-A' in Fig. 5.9 is shown in Fig. 5.10. It can be understood from Fig. 5.10 that only the island diffusion of the driver NMOS is directly connected to the I/O pad. Through such a layout arrangement, PMOS current is forced to flow through the N-Well ballast resistor in the driver NMOS, enforcing the N-Well to ballast both driver NMOS and PMOS during ESD stresses.

In the type-A layout scheme, the ESD current under PS-mode ESD tests first flows to the floating V_{DD} through the N-Well ballast resistor and the D_P diode. Then, the ESD current is discharged to the grounded V_{SS} through the power-rail ESD clamp circuit. Under the PD-mode ESD tests, the ESD current is first discharged to the grounded V_{DD} through the N-Well ballast resistor and the D_P diode. Therefore, voltages across the stressed I/O pad and

ground under the PS- and PD- mode ESD tests are

$$\Delta V_{PS} = [I_{ESD} \times (R_{ballast} + R_{on,\,DP} + R_{VDD} + R_{on,\,Power\text{-}Rail}) + V_{t,\,DP}] \quad (5.2)$$

and

$$\Delta V_{PD} = [I_{ESD} \times (R_{ballast} + R_{on,\,DP} + R_{VDD}) + V_{t,\,DP}] \quad . \quad (5.3)$$

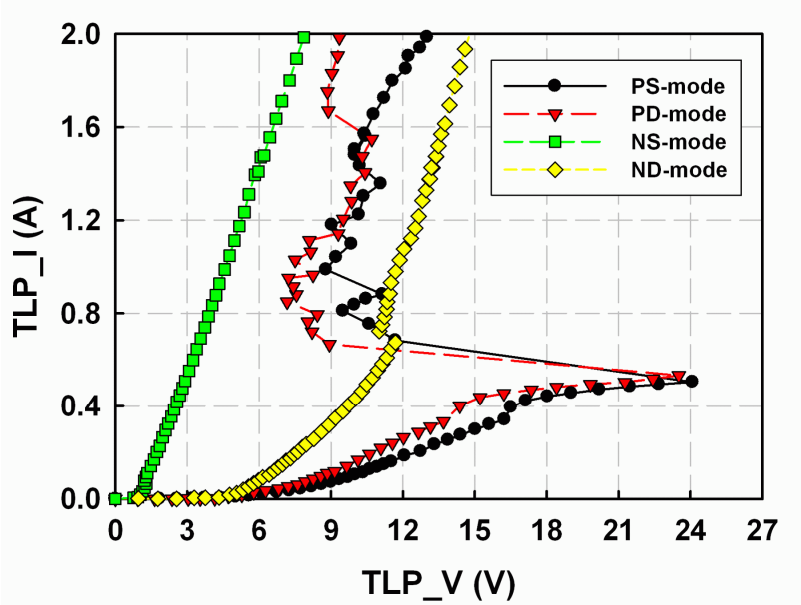


Fig. 5.11. TLP-measured I-V curves for the I/O buffer with the type-A layout scheme. The tests were manually stopped at 2 A without causing failure to the I/O buffer.

With the ESD current being forced to flow through the N-Well under PS- and PD- mode conditions, it has been reported that the N-Well resistor under high current level exhibits high resistance characteristic due to drift velocity saturation [97]. As the TLP measurement results shown in Fig. 5.11, under PS-mode (positive TLP stress on I/O pad with V_{SS} relatively grounded) and PD-mode (positive TLP stress on I/O pad with VDD relatively grounded) TLP measurements, the drift velocity saturation results in the 24-V voltage at I_{ESD} of 0.5 A. The applied voltage is mainly dropped within the N-Well region. At the same time, electron-hole pairs are generated to support the increased current, and electric field is built up toward the N+ island diffusion/N-Well junction. The electric field build-up eventually results in

avalanche breakdown to happen at the N+/N-Well junction, which results in the snapback as observed in Fig. 5.11. With the avalanche breakdown at N+/N-Well junction, the hole concentration can exceed the background doping of N-Well, and results in conductivity modulation to lower the turn-on resistance of N-Well [116], [117]. For NS-mode (positive TLP stress on V_{SS} pin with I/O pin relatively grounded) and ND-mode (positive TLP stress on V_{DD} pin with I/O pin relatively grounded) TLP measurements, ESD currents are discharged through the D_N diode and the power-rail ESD clamp circuit (in ND-mode test) without flowing through the ballast N-Well. Therefore, the high resistance characteristic from N-Well is not observed in the ND- and NS- mode TLP I-V curves in Fig. 5.11.

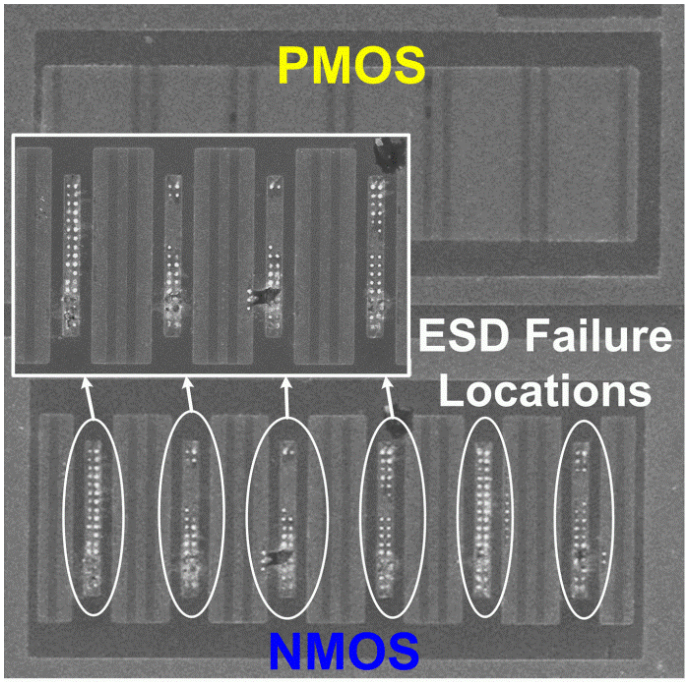


Fig. 5.12. SEM image of the fully-silicided I/O buffer realized with the type-A layout scheme after 6.5-kV PS-mode ESD stress. Uniformly distributed N+-to-N-Well ESD damages are found on the driver NMOS.

HBM ESD measurement results in Table 5.1 show that the fully-silicided I/O buffers with the type-A layout scheme have the PS- and PD-mode ESD protection levels as high as 6 kV. Under the ND-mode ESD tests, though the ΔV_{ND} can exceed V_{t1} of the driver PMOS under

high ESD stress voltage, the N-Well ballast resistor suppresses the ESD current discharged through the PMOS. Accordingly, fully-silicided I/O buffers with type-A layout scheme have ND-mode HBM ESD robustness over 8 kV. By using the type-A layout scheme, ND-mode ESD failure on the driver PMOS has been successfully overcome and the 6-kV performance target has been achieved.

Among the four ESD test modes on I/O buffers, ESD current under PS- and PD-mode ESD tests has to flow through the ballast N-Well. The N+/N-Well junction breakdown is expected to result in large power dissipation over the ballast N-Well, which results contact spiking on island diffusions of the driver NMOS. With the ESD current flowing from island diffusion through the ballast N-Well to the drain diffusion of driver NMOS, melted metal contacts can result in a short from island diffusion to the drain diffusion of driver NMOS, which results in substantial shift of I-V curve compared to the original I-V curve before ESD stress. The I/O buffer is then judged as a failure because short of island and drain diffusions results in I-V shift over 20% compared to the original I-V curve before ESD stress. The melted metal contacts may also result in a short from island diffusion to the P-Substrate, which can also cause sharp I-V shift after ESD stress. Consequently, the N+-to-N-Well ESD failure has become the limitation to the type-A layout scheme. As the SEM image shown in Fig. 5.12, the I/O buffer after 6.5-kV PS-mode ESD stress shows N+-to-N-Well failure on the driver NMOS. From the uniformly distributed ESD failure locations in Fig. 5.12, the effectiveness of the type-A layout scheme to ballast the I/O buffer for ESD protection has been verified.

5.4.2. I/O Buffer with The New Proposed Layout Scheme (Type B)

In the type-A layout scheme, though the ballast N-Well leads to significant improvement on ESD robustness, it also introduces the ($I_{ESD} \times R_{ballast}$) voltage drop to ΔV_{PS} and ΔV_{PD}. The $R_{ballast}$ of N-Well resistor becomes large under high current conditions. The increased ($I_{ESD} \times R_{ballast}$) voltage drop pinches the ESD protection window and makes internal circuits more

susceptible to ESD failure. Even though the internal ESD failure was not observed, eliminating the $R_{ballast}$ term in ΔV_{PS} and ΔV_{PD} is also beneficial to the PS- and PD- mode ESD tests. Since the main ESD protection device in a power-rail ESD clamp circuit generally has been drawn with large device dimension, it usually stands much higher ESD stress levels than the NMOS or PMOS in I/O buffers. Furthermore, averting the PS- and PD-mode ESD current from being discharged through the $R_{ballast}$ can further avoid the N+-to-N-Well ESD failure.

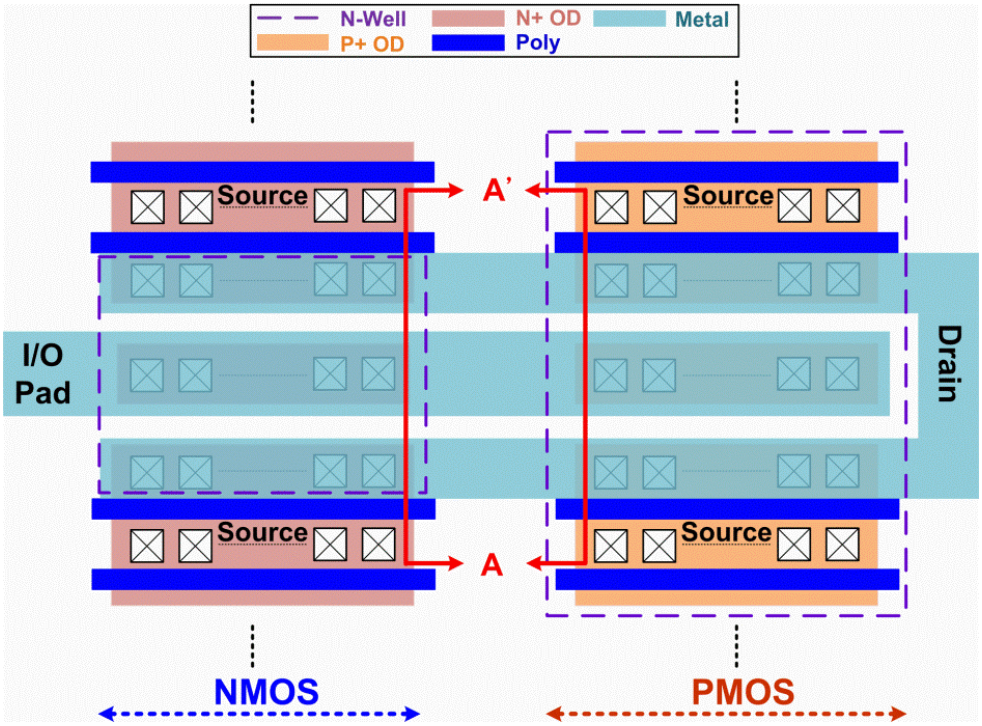


Fig. 5.13. Diagram to show the metal connection to the I/O pad for driver NMOS and PMOS in the type-B layout scheme.

To modify the type-A layout scheme and to eliminate the $R_{ballast}$ term under PS- and PD-mode ESD tests, type-B layout scheme is proposed. A diagram is shown in Fig. 5.13 to illustrate the type-B layout scheme, where the N-Well ballast resistor is applied to both driver NMOS and PMOS. Drain of the driver PMOS is separated into drain diffusion and island diffusion by FOX, as shown in Fig. 5.13. Drain diffusions of driver PMOS and NMOS are connected to each other, and island diffusions of both driver PMOS and NMOS are directly

connected to the I/O pad. With such a distinct metal routing in the type-B layout scheme, the P+ island diffusion provides an efficient discharging path for PS- and PD-mode ESD tests, where ESD current can be discharged directly through the D_P diode without flowing through the ballast N-Well in NMOS. The cross-sectional view along A-A' line in Fig. 5.13 is shown in Fig. 5.14. Under the normal circuit operating conditions, with the shorted drain diffusions of driver NMOS and PMOS, PMOS can pull high the I/O pad through the ballast N-Well in the driver NMOS. Device dimensions for driver NMOS and PMOS in type-B layout scheme are the same to those in type-A layout scheme, and I/O buffers with either type-A or type-B layout scheme can meet the operating frequency specification of 20 MHz.

By avoiding ESD current to flow through the ballast N-Well under PS- and PD- mode ESD stresses, the ESD currents are mainly discharged through the diode D_{P1} and the power-rail ESD clamp circuit (in PS-mode). As the PS- and PD- mode TLP-measured I-V curves shown in Fig. 5.15, high resistance characteristic from the ballast N-Well in type-A layout scheme is avoided in the type-B layout scheme. Therefore, ΔV_{PS} and ΔV_{PD} in the type-B layout scheme are much smaller compared to those in the type-A layout scheme. Under ND-mode and NS-mode conditions, the D_N diode and the power-rail ESD clamp circuit are effective in discharging ESD currents, as shown in Fig. 5.15.

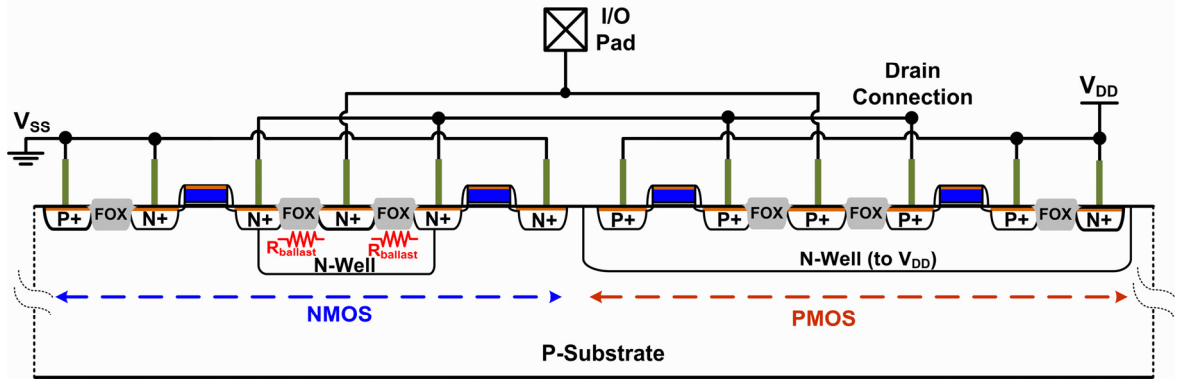


Fig. 5.14. Cross-sectional view along A-A' line of the fully-silicided I/O buffer realized with the type-B layout scheme.

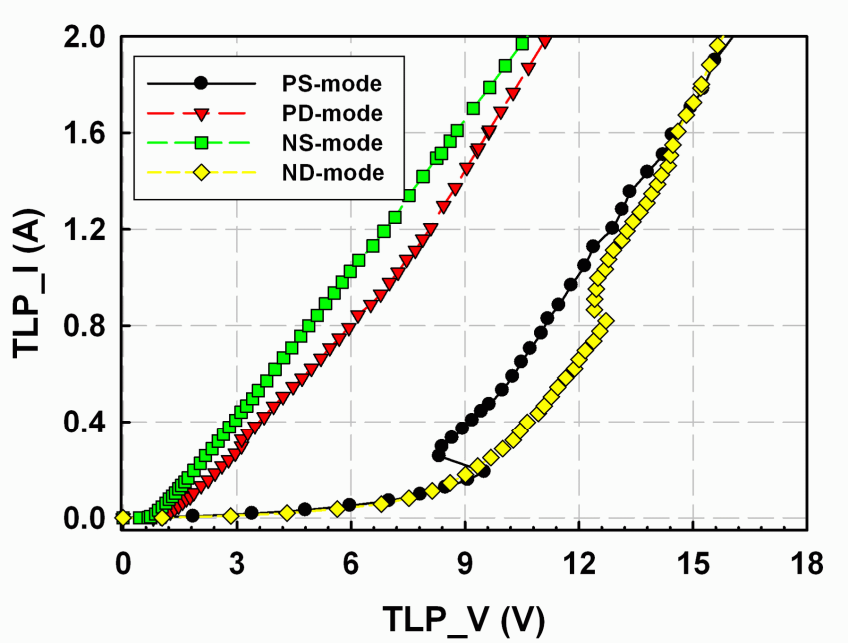
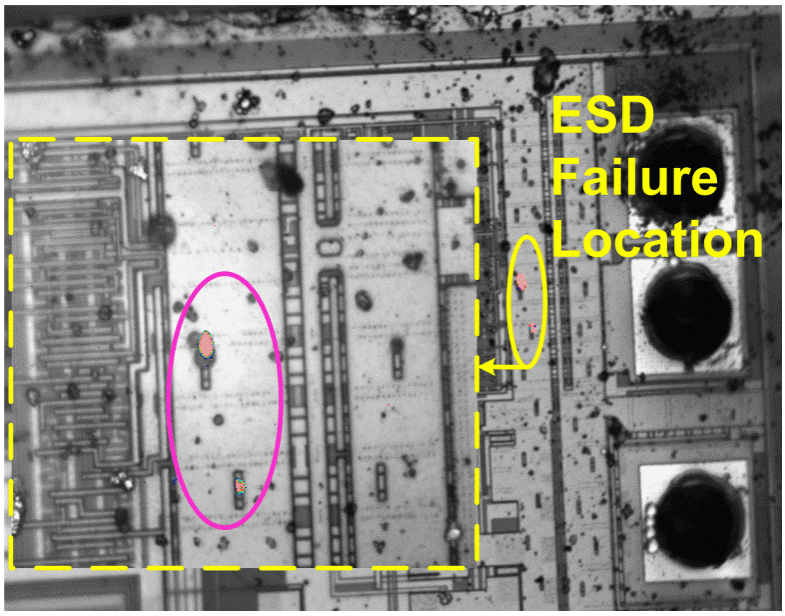
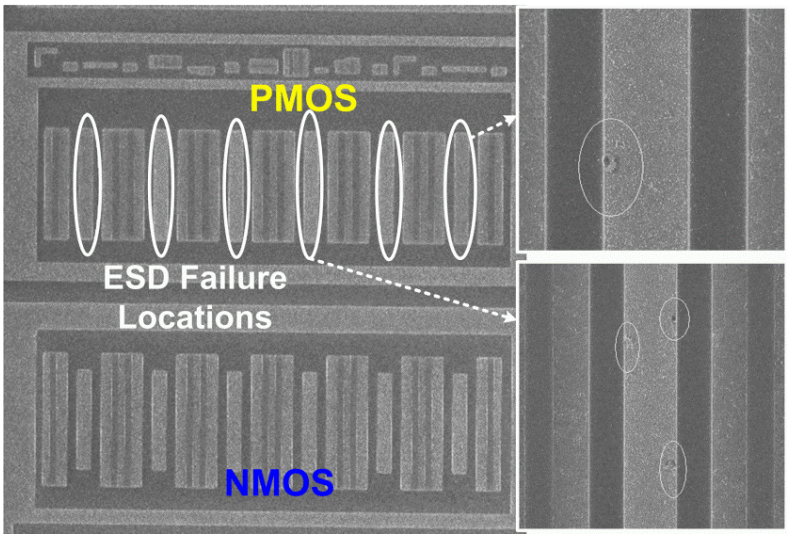


Fig. 5.15. TLP-measured I-V curves for the I/O buffer with the type-B layout scheme. The tests were manually stopped at 2 A without causing failure to the I/O buffer.

Because the ESD current can be discharged without flowing through the ballast N-Well in the driver NMOS, the N+-to-N-Well ESD failure on driver NMOS is avoided in the type-B layout scheme. Moreover, the N-Well can ballast the driver NMOS when ΔV_{PS} or ΔV_{PS} is higher than $V_{t1,MN1}$. PS-mode HBM ESD robustness of the I/O buffer has therefore been increased to 7 kV, and the PD-mode HBM ESD robustness has been increased to over 8 kV, as shown in Table I. Emission microscope (EMMI) analysis in Fig. 5.16(a) shows that failure of the I/O buffer with the type-B layout scheme after 7.5-kV PS-mode ESD stress locates on the driver PMOS. The corresponding SEM image of the failure on the driver PMOS in Fig. 5.16(a) is shown in Fig. 5.16(b). Without the ESD damage on source but silicides meltdown on island diffusions, SEM image reveals the PS-mode ESD failure on the P+/N-Well diode (D_P) of driver PMOS, which has further confirmed that the type-B layout scheme has taken advantage of the highest whole-chip ESD protection capability from the I/O buffers.



(a)



(b)

Fig. 5.16. (a) EMMI and (b) SEM images of the fully-silicided I/O buffer realized with the type-B layout scheme after 7.5-kV PS-mode ESD stress.

5.5. Summary

Silicidation used in CMOS processes has been reported to cause substantial degradation on ESD robustness of CMOS devices. To mitigate the negative impact on ESD robustness from silicidation, two new ballasting layout schemes for fully-silicided I/O buffers are proposed.

The new proposed ballasting layout schemes have been verified on a real IC product fabricated in a 0.35-μm 5-V fully-silicided CMOS process. Without adequate ballasting technique in the original layout, the fully-silicided I/O buffer has a very poor ESD level of 1.5 kV in HBM ESD tests. Ballast N-Well on the driver NMOS is useful to avoid PS-mode ESD failure on NMOS, but the ND-mode ESD failure over the un-ballasted driver PMOS limits the ESD robustness to only 4 kV. With the proposed type-A layout scheme, the whole-chip ESD protection level has been improved to the performance target of 6-kV HBM ESD robustness. The proposed type-B layout scheme further increases the whole-chip ESD robustness up to 7 kV. No additional mask or process step are required to fulfill either one of the new proposed layout schemes. The new proposed ballasting layout schemes are process-portable to different CMOS technologies. Moreover, the type-B layout scheme ballasts I/O buffers without imposing the ballast resistance on the ESD protection window. With the new proposed ballasting layout schemes, the additional mask and process steps for silicide blocking can be omitted to reduce the fabrication cost without sacrificing the ESD robustness of IC products.

Chapter 6

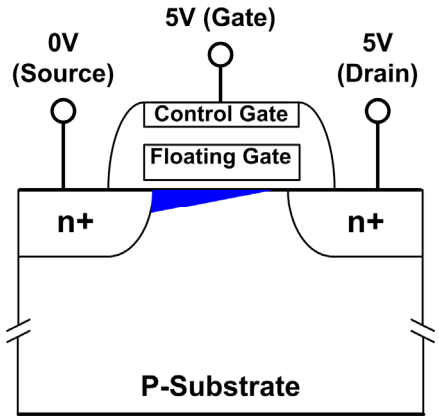
Fully-Silicided ESD Protection Design on The Voltage Programming Pins of ICs with One-Time Programming Memories

6.1. Background

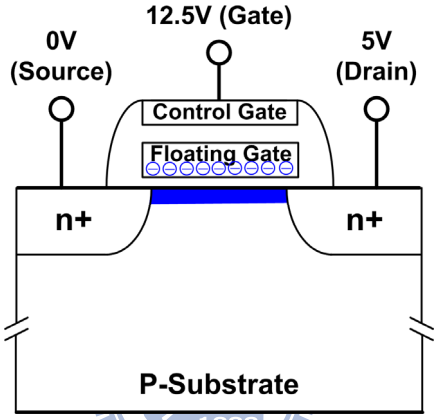
One-time programming (OTP) read only memory (ROM) has been widely implemented in micro-controllers (MCUs) [118]. To successfully program the memory cells, a HV on the voltage programming (V_{PP}) pin is necessary to induce channel hot electrons or to burn out the fuse [119], [120]. Because the programming voltage (V_{PP} voltage) is higher than the V_{DD} normal operating voltage of internal circuits, current paths from the V_{PP} pin to the V_{DD} power supply line is unallowable. With the forbidden current path from V_{PP} pin to the V_{DD} power supply line, such a V_{PP} pin suffers a stringent challenge on ESD protection design.

With silicide blocking (SB) being omitted in the studied process of this chapter, novel fully-silicided design for the V_{PP} pin ESD protection is necessary. The open-drain structure further increases the ESD design challenge. An efficient ESD protection design for fully-silicided ICs with voltage programming pin is therefore a highly challenging reliability issue to IC designers [121]–[124]. Moreover, to make the MCUs universally compatible to different ROM programmers, V_{PP}-pin ESD protection designs are often required to have high immunity against fast voltage transition during memory programming.

In this chapter, a new ESD protection design for fully-silicided V_{PP} pin is proposed, including a circuit design to avoid the mis-triggering of ESD protection device during the programming conditions when V_{PP} voltage has a fast rise time. The proposed ESD protection design has been successfully verified on a commercial IC product with OTP memory cells in a 0.35-μm fully-silicided CMOS process.



(a)



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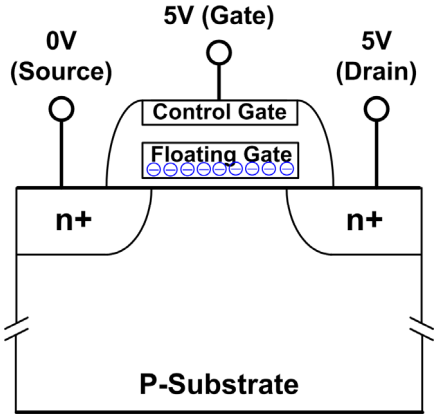


(c)

Fig. 6.1. (a) Normal operating condition of the memory unit before programmed. Channel can be induced under V_{GS} of 5 V and V_{DS} of 5 V. (b) Bias conditions of the memory unit during programming. A high control gate bias of 12.5 V is used to draw channel hot electrons into the floating gate. (c) Normal operating condition of the memory unit after programmed. Channel cannot be induced under V_{GS} of 5 V and V_{DS} of 5 V due to the trapped electrons in the floating gate.

6.2. Design Considerations of Voltage Programming Pins

6.2.1. OTP Memory Cells

To electrically program the OTP memory cells, Fig. 6.1 depicts the required bias conditions on the memory unit (NMOS cell) which has a control gate and a floating gate. Before programming, there is no or only a few charges in the floating gate. Original threshold voltage of a non-programmed NMOS cell is defined as V_{t0}. V_{t0} is smaller than 5 V so that the NMOS cell can be turned on (channel can be induced) when the control gate is biased at 5 V (Fig. 6.1(a)). To program the NMOS cell, a high gate bias of 12.5 V (V_{PP} voltage) is applied on the control gate and the drain of NMOS cell is biased at V_{DD} of 5 V. With the high gate bias of 12.5 V on the control gate, electrons permitted from the source can pass through the insulating layer beneath the floating gate to be accumulated in the floating gate (Fig. 6.1(b)). After a span of field programming time, the 12.5 V V_{PP} voltage is removed and the electrons that accumulated in the floating gate are trapped in the floating gate. The trapped electrons in the floating gate can substantially increase the threshold voltage of the NMOS cell from V_{t0} to V_t'. As long as the number of electrons trapped in the floating gate is large enough (the programming time is long enough), V_t' can be higher than 5 V. Consequently, the channel of NMOS cell can no longer be induced by the 5 V gate bias, and the NMOS cell becomes an open circuit after programming, as shown in Fig. 6.1(c). By exploiting this principle, on-chip memory arrays can be programmed to represent different digital codes to calibrate IC products or to predefine different IC functions to broaden their application scopes [125].

6.2.2. V_{PP} Programming Waveforms

To design an ESD protection circuit for voltage programming pins, it is essential to understand the V_{DD} and V_{PP} programming waveforms. The typical measured V_{DD} and V_{PP} programming waveforms are shown in Fig. 6.2. Under the V_{PP} programming condition, V_{DD}

voltage is charged up from 0 to 5 V before the set in of V_{PP} voltage ramping, so that internal circuits such as control logic or address decoder can function properly. After the V_{DD} voltage has been charged to 5 V, the programmer pulls high the V_{PP} voltage from 0 to 12.5 V, as shown in Fig. 6.2.

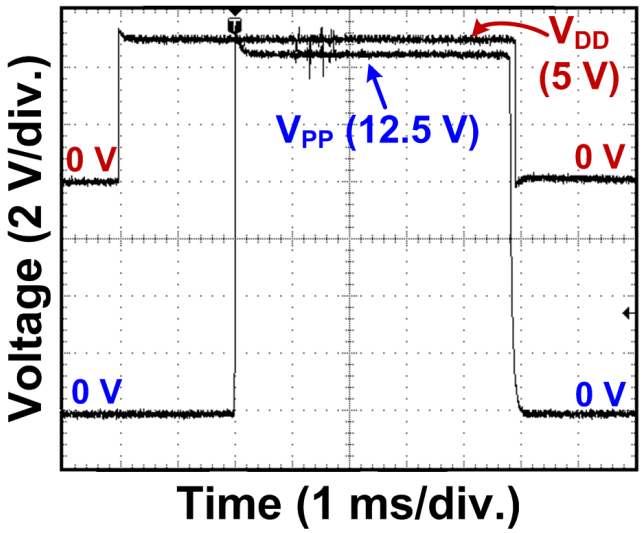


Fig. 6.2. Measured voltage waveforms on V_{DD} and V_{PP} pins during programming.

To comprehensively protect I/O pins against ESD stresses, a typical rail-based ESD protection scheme is shown in Fig. 6.3, where two diodes D_U and D_N are used to divert ESD stress energy at the I/O pad to the V_{DD} or the GND power supply lines. Because the power-rail ESD clamp circuit is especially designed with a large ESD protection device (M_{N4}), it is effective in discharging ESD energy between power supply lines. Through the D_U and D_N diodes in cooperation with the power-rail ESD clamp circuit, the rail-based ESD protection scheme has been reported as an effective method to significantly improve ESD robustness of the I/O pin. However, since the 12.5 V V_{PP} voltage is higher than the 5 V V_{DD} voltage during programming, the diode D_U that diverts the high V_{PP} voltage to the V_{DD} power supply line is prohibited. Otherwise, the memory cells cannot be successfully programmed due to insufficient voltage on the V_{PP} pin. Without the diode D_U, power-rail ESD clamp

circuit cannot help discharge ESD energy at the I/O pad under PS- and PD-mode ESD tests. Accordingly, I/O pins without a forward diode from the I/O pad to the V_{DD} power supply line usually have a low ESD protection level, especially under PS- and PD-mode ESD tests. Mixed-voltage I/O buffers where I/O voltages would be higher than their V_{DD} voltages suffered the same limitation, too[126].

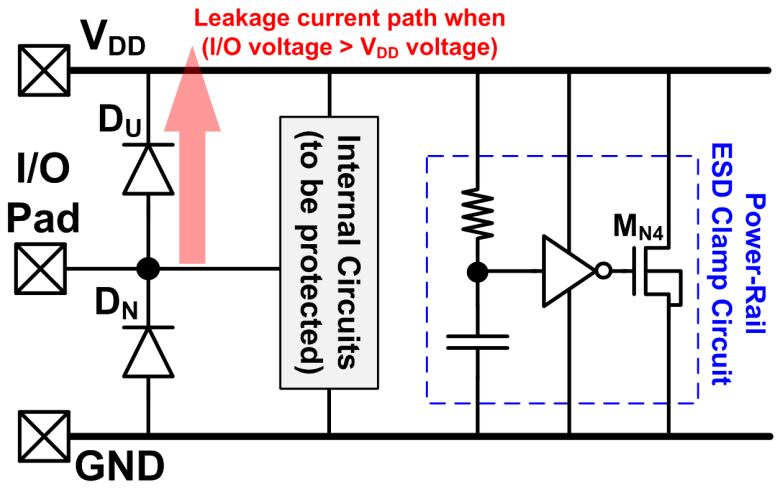


Fig. 6.3. Traditional whole-chip ESD protection scheme with the power-rail ESD clamp circuit. The diode D_U results in an unwanted leakage current path when I/O voltage is higher than the V_{DD} voltage during some special circuit operating conditions.

Besides the inability of employing power-rail ESD clamp circuit under PS- and PD-mode ESD tests, the rise time of programming voltage on V_{PP} pin ($T_{R,VPP}$) is another design issue that strongly affects the ESD protection design to V_{PP} pin. Since the V_{PP} programming voltage is externally supplied from a programmer, different programmers may have different driving capabilities to result in huge differences between slew rates of programming voltages on V_{PP} pin. The rise time of V_{PP} programming voltage may be as slow as several microseconds [127], or as fast as several tens of nanoseconds in different programming environments [127], [128]. Because the rise time of ESD voltage has the same timescale to that of fast V_{PP} programming voltage (several tens of nanoseconds), some of traditional ESD

protection designs could be mis-triggered by their ESD trigger circuits. A primary ESD protection PMOS with a RC timer to control its gate voltage was reported to protect the programming pin by Im et al [129]. The RC timer should have a time delay over several hundreds of nanoseconds, so that the gate of ESD protection PMOS can be kept low to turn on PMOS during the ESD transition. However, when the rise time of the V_{PP} programming voltage was also in the same scale as that of ESD transient voltage, the simple RC timer directly connected to the programming pin cannot distinguish between the normal programming event and ESD transition event. The ESD protection PMOS in [129] would be turned on both during V_{PP} programming and ESD transition. The turned-on PMOS during programming event will pull down the V_{PP} voltage to cause a false programming result. Additional modification should be added into the design of [129] to avoid the false programming issue when the programmer provides the V_{PP} programming voltage pulse with a fast rise time. To avoid the mis-triggering issue and make ICs comprehensively compatible to programmers from different manufacturers, a wide range of acceptable V_{PP} voltage rise time during programming is requested by customers.

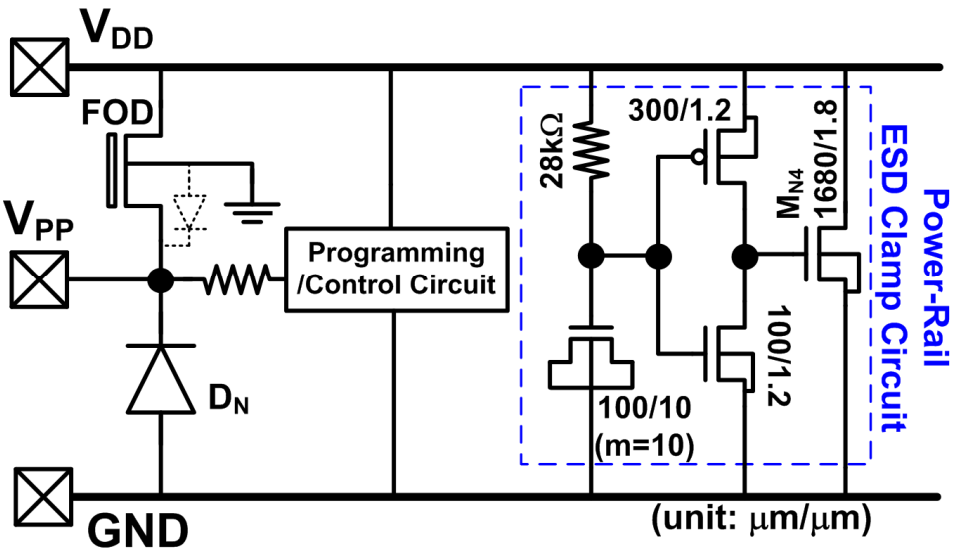


Fig. 6.4. Previous ESD protection design for V_{PP} pin. It can be safely programmed with fast V_{PP} voltage rise time but has a lower ESD protection level of only 2 kV in HBM.

6.2.3. Previous ESD Protection Designs for V_{PP} Pins

A previous ESD protection design for V_{PP} pin used in some IC product is shown in Fig. 6.4. Without any ESD trigger circuit in this ESD protection design, both the ESD protection devices, FOD (field oxide device) and the diode D_N, are insensitive to the rise time of V_{PP} programming voltage. Under ND- and NS-mode ESD tests, the power-rail ESD clamp circuit and the diode D_N provide effective ESD discharging paths. Under PS-mode ESD test, ESD voltage induces breakdown of the diode D_N to conduct ESD current through the reverse-biased junction of D_N. A FOD device is placed between the V_{PP} pin and the V_{DD} line, so that PD-mode ESD energy can be directly discharged to the grounded V_{DD} line through the n-p-n bipolar junction transistor (BJT) inherent in the FOD [130]. Because the diode inherent in the FOD device has a breakdown voltage higher than 12.5 V, the FOD device does not result in current path from the V_{PP} pin to the V_{DD} line during programming. Under PS-mode ESD test, FOD can help divert some ESD energy to the V_{DD} line, and it can be further discharged to the grounded GND through the power-rail ESD clamp circuit. By using this previous ESD protection design, the measured HBM ESD protection level on V_{PP} pin is only 2 kV verified in an IC product.

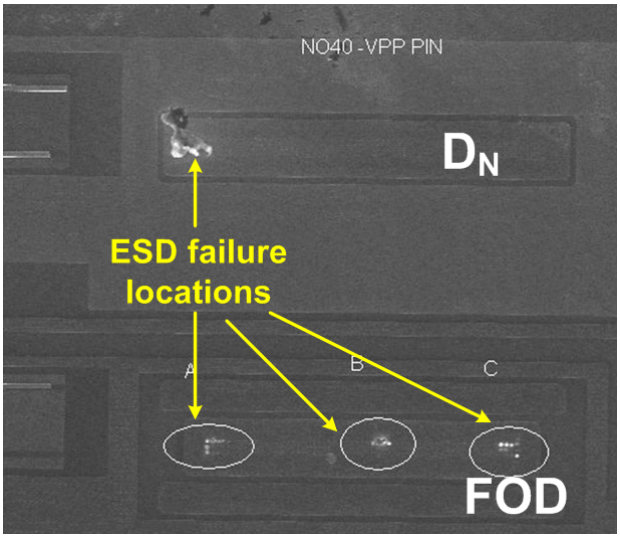


Fig. 6.5. SEM image of the previous ESD protection design after 2.5-kV PS-mode ESD test. ESD failure locations were found on both the FOD device and the diode D_N.

SEM image of the previous ESD protection design after 2.5-kV PS-mode ESD test is shown in Fig. 6.5. ESD failure locations were found on both the FOD device and the diode D_N. The failure analysis verified that the FOD device can help discharge ESD energy under PS-mode ESD test. The previous ESD protection design can provide the typical HBM ESD protection level of 2 kV to the IC product, but the specified HBM ESD protection level has recently been increased from 2 to 4 kV by customers with high reliability requirement. For lack of ESD trigger circuit in the previous ESD protection design, further enlarging the device width of FOD did not improve HBM ESD protection level due to the well-known non-uniform triggering phenomenon [26]. Moreover, for cost reduction, silicide blocking (SB) was not used in such IC products. Without silicide blocking, severe current crowding phenomenon and current filamentation further deteriorate the linearity of ESD robustness to the device dimension of an ESD protection device. ESD trigger techniques have been reported to effectively relieve the negative impact on ESD robustness due to silicidation. Accordingly, with the inability to meet the new requirement of 4-kV HBM ESD protection level by the previous ESD protection design, a new ESD protection design is therefore requested and proposed. The new proposed ESD protection design can not only exploit the ESD trigger technique to achieve high ESD robustness, but also avoid the mis-triggering of ESD protection device under V_{PP} programming voltage with a fast rise time.

6.3. New Proposed V_{PP} ESD Protection Design

The new proposed ESD protection design on V_{PP} pin is composed of a snapback ESD protection device (M_{N2}), an ESD trigger circuit (R_1, M_{C1}, M_{P1}, and M_{N1}), an ESD bus, two diodes (D_1 and D_2), and a fail-safe NMOS M_{N3}, as shown in Fig. 6.6. The ESD trigger circuit in the proposed design is connected to the V_{PP} pin through the ESD bus and the diode D_2. The output of the ESD trigger circuit is connected to the substrate of M_{N2} to fulfill the substrate-triggered technique [26]. Floor plan of the proposed ESD protection design in an IC

product realized in a 0.35-μm fully-silicided CMOS process is shown in Fig. 6.7. Device dimensions of the proposed ESD protection design and the power-rail ESD clamp circuit used in the IC product are listed in Table 6.1. In the proposed ESD protection design, M_{N1}, M_{N2}, M_{C1}, and M_{P1} are HV symmetry devices that have thick gate oxide and lightly-doped n-drift (for HV NMOS) or p-drift (for HV PMOS) regions at source/drain to sustain the high programming voltage [131], [132].

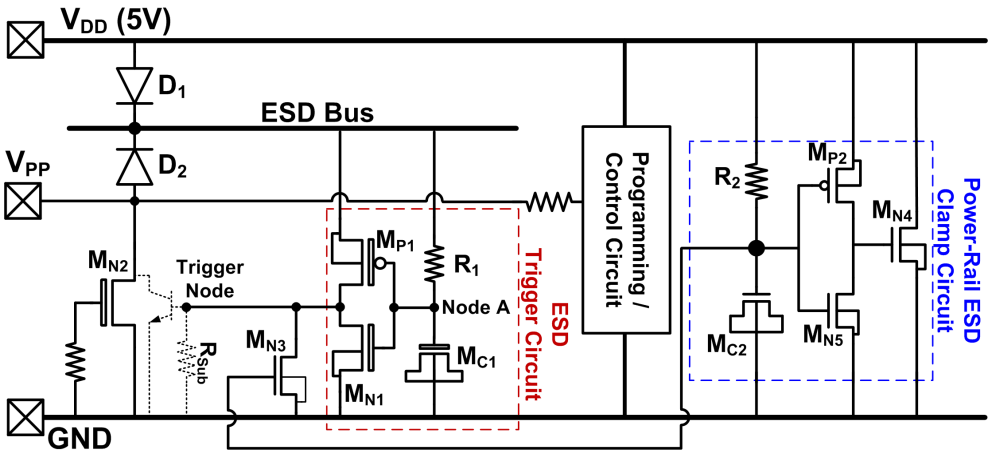


Fig. 6.6. The proposed ESD protection design for V_{PP} programming pin.

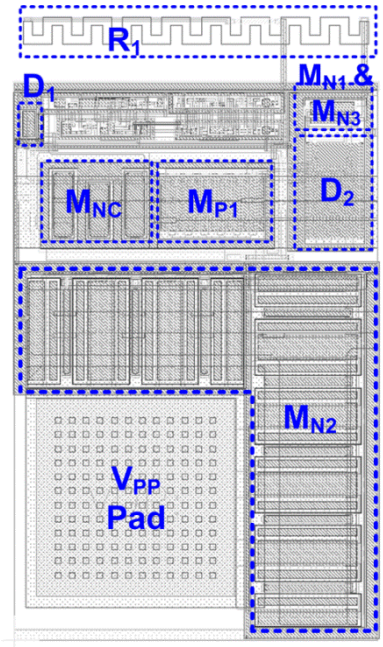


Fig. 6.7. Layout top view of the proposed ESD protection design for V_{PP} pin, which was realized in a 0.35-μm fully-silicided CMOS process.

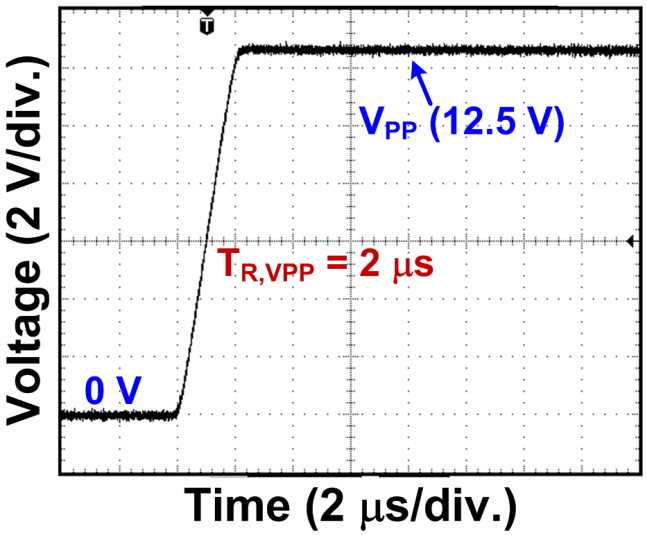
TABLE 6.1
DEVICE DIMENSIONS OF THE ESD PROTECTION DESIGN

	Device Dimension	
R_1	28.3 kΩ	–
R_2	28 kΩ	–
M_{C1}	43.5 μm/ 23 μm	HV Device
M_{C2}	100 μm/ 10 μm	LV Device
M_{P1}	300 μm/ 1.2 μm	HV Device
M_{P2}	300 μm/ 1.2 μm	LV Device
M_{N1}	20 μm/ 1.2 μm	HV Device
M_{N2}	720 μm/ 1.2 μm	HV Device
M_{N3}	40 μm/ 0.35 μm	LV Device
M_{N4}	1680 μm/ 1.8 μm	LV Device
M_{N5}	100 μm/ 1.2 μm	LV Device

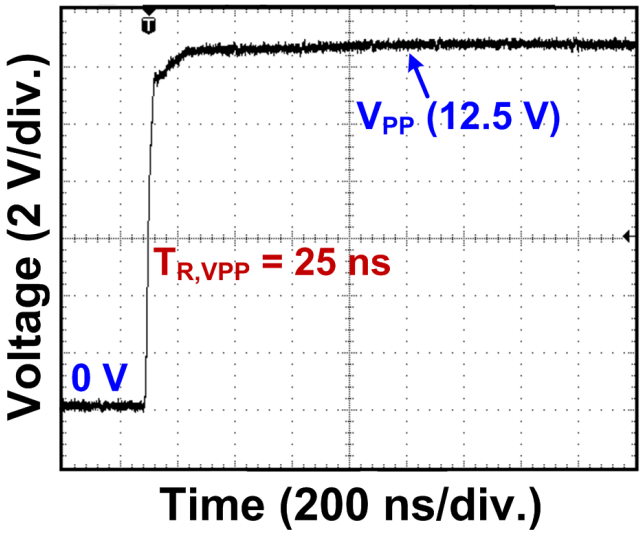
During normal circuit operating conditions, V_{DD} pin is biased at 5 V and V_{PP} pin is either 0 or 5 V. Through the D_1 diode, the ESD bus is charged up to a voltage level close to V_{DD} of 5 V. The resistor R_1 passes the voltage on ESD bus to the node A (V_A) during normal circuit operating condition. With the same source voltage and gate voltage on M_{P1}, M_{P1} is kept off and the output current from the ESD trigger circuit to the trigger node is 0 A. With the gate of M_{N2} being grounded, M_{N2} is safely kept off during normal circuit operating condition without interfering I/O signals at V_{PP} pin.

Under V_{PP} programming where the V_{PP} voltage has a slow voltage rise time ($T_{R,VPP}$ in the order of microseconds), voltage on the node A (V_A) can follow up the V_{PP} voltage transition because the time delay from R_1 and M_{C1} in Fig. 6.6 is smaller than the V_{PP} voltage rise time. Consequently, M_{P1} is safely kept off when $T_{R,VPP}$ is slow, and M_{N2} is off as well. The proposed ESD protection design therefore does not interfere with V_{PP} programming when $T_{R,VPP}$ is slow. However, when the V_{PP} programming voltage has a rise time as fast as several tens of nanoseconds, V_A can no longer follow up the voltage transition on V_{PP} pin. Because the ESD protection NMOS (M_{N2}) in the proposed design is with substrate-triggered design, the amount of substrate-triggered current that flows into the trigger node could turn on

parasitic BJT inherent in M_{N2}. Accordingly, to suppress the current that may falsely flow into the substrate of M_{N2} during fast V_{PP} voltage rising, a fail-safe NMOS (M_{N3}) was added at the output of ESD trigger circuit. Gate of M_{N3} is connected to V_{DD} through the resistor R_2 so that M_{N3} is kept on during V_{PP} programming to provide a low-impedance current path to shunt



(a)



(b)

Fig. 6.8. Measured voltage waveforms on V_{PP} pin during programming with (a) slow $T_{R,VPP}$ of 2 μs and (b) fast $T_{R,VPP}$ of 25 ns. V_{DD} was biased at 5 V during the tests.

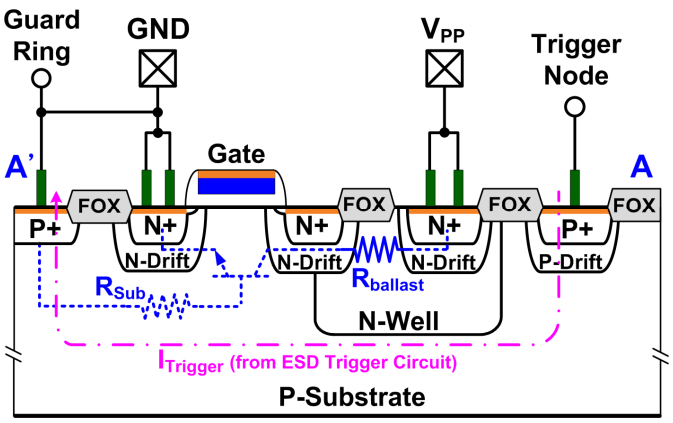
any M_{P1} output current to ground. M_{N3} can thus stabilize ground potential of the trigger node to prevent M_{N2} from being mis-triggered during V_{PP} programming. Because drain of M_{N3} is connected to the trigger node, parasitic R_{Sub} and body diode of M_{N2} keeps drain of M_{N3} at a low voltage level. Without a high voltage across M_{N3}, it was realized with a low-voltage device to maximize its capability of stabilizing the trigger node during V_{PP} programming with a fast rise time. Moreover, the initial voltage at node A is biased at V_{DD} through the diode D_1 and the ESD bus, which reduces the M_{P1} overdrive voltage to suppress the amount of mis-triggering current that may falsely flow into the trigger node due to fast V_{PP} programming voltage.

To verify the ability of the proposed design against mis-triggering during V_{PP} programming, 0-to-12.5 V voltage pulses with different pulse rise time ($T_{R,VPP}$) were applied to V_{PP} pin of the IC product realized in the 0.35-μm CMOS process. V_{DD} was biased at 5 V during the tests. Figs. 6.8(a) and 6.8(b) show the measured voltage waveforms on V_{PP} pin with slow (2 μs) and fast (25 ns) input voltage rise time, respectively. Both measured voltages on V_{PP} pin were successfully ramped up to 12.5 V, which has verified that the mis-triggering issue of M_{N2} was successfully prevented in the new proposed ESD protection design.

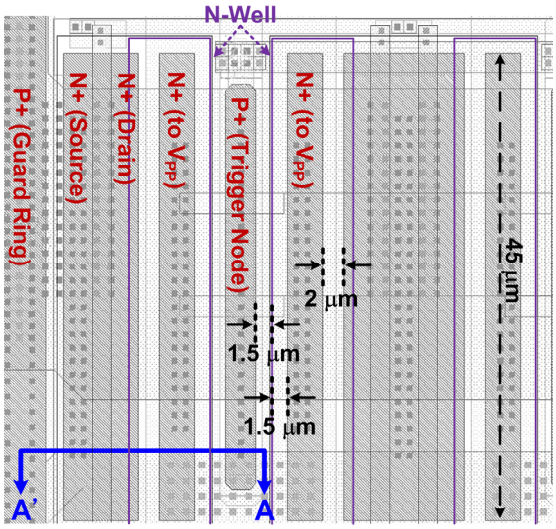
6.4. Implementation and ESD Testing Results

6.4.1. Ballast Layout to Fully-Silicided High-Voltage NMOS

In a multi-finger NMOS, different distances from the drain region of each finger to the grounded guard ring result in asymmetry of substrate resistance (R_{Sub}), which causes the central fingers of NMOS to be more easily triggered on under ESD stresses. After triggering of the central fingers under ESD stresses, the ESD overstress voltage is clamped down by these earlier turned-on fingers. Without sufficient ballast resistance, it is highly possible that the central fingers are burned out before the clamped voltage is large enough to trigger



(a)



(b)

Fig. 6.9. (a) Device cross-sectional view and (b) layout top view of the high-voltage ESD protection NMOS (M_{N2}) with P+ trigger node and the N-Well ballast layout realized in a fully-silicided CMOS process.

the rest fingers of the NMOS. As a result, ESD current is concentrated in some earlier turned-on area and the rest area cannot be triggered on in time to discharge ESD current. Such non-uniform turn-on behavior among the multiple fingers of NMOS limits its ESD robustness, even if the NMOS was drawn with a large device dimension. By introducing the ballast resistance $R_{ballast}$ to balance the turn-on resistance of the multi-finger NMOS, turn-on uniformity of the multi-finger NMOS during ESD stresses can be improved. Moreover, it has

been reported that by increasing the ballast resistance, ESD current path can be spread deeper into the substrate of large volume, which in turn improves ESD robustness as well. As the discussion in Chapter 5, sufficient ballast resistance can force ESD current deeper into the substrate to have a better heat dissipation, and also increase the ESD robustness due to the improvement of turn-on uniformity among the multiple fingers of NMOS.

The N-Well ballast layout was applied to adequately increase ballast resistance to M_{N2} without using the SB [122]. Device cross-sectional view of the fully-silicided high-voltage ESD protection NMOS (M_{N2}) with the N-Well ballast layout is shown in Fig. 6.9(a). Drain of M_{N2} is electrically short to the V_{PP} pad through the N-Well. With the high sheet resistance of N-Well due to its relatively low doping concentration, the N-Well can provide the $R_{ballast}$ to improve ESD robustness of the fully-silicided M_{N2}. Moreover, the P+ trigger nodes inserted in the device were short to the output of ESD trigger circuit (Trigger Node in Fig. 6.6), so the M_{N2} is implemented with substrate-triggered design to further improve its ESD protection level. Layout top view of M_{N2} is shown in Fig. 6.9(b). No additional mask layers or process steps are required to implement this ESD device in a fully-silicided CMOS process.

6.4.2. ESD Discharging Paths

To protect the V_{PP} pin against the four I/O ESD test modes, current discharging paths of the proposed ESD protection design are illustrated in Figs. 6.10(a) to 6.10(d). Under NS-mode ESD test, the ESD current is discharged through the P-Substrate/N+ diode D_{MN2} inherent in M_{N2} (Fig. 6.10(a)). Under ND-mode ESD test, the ESD current is discharged through the power-rail ESD clamp circuit, the GND line, and the D_{MN2} (Fig. 6.10(b)). Because the D_{MN2} is efficient in discharging ESD energy under forward conduction condition and the gate-driven M_{N4} in the power-rail ESD clamp circuit has a large device dimension of 1680 μm/1.8 μm, V_{PP} pin can have high ESD robustness under the NS- and ND-mode ESD tests.

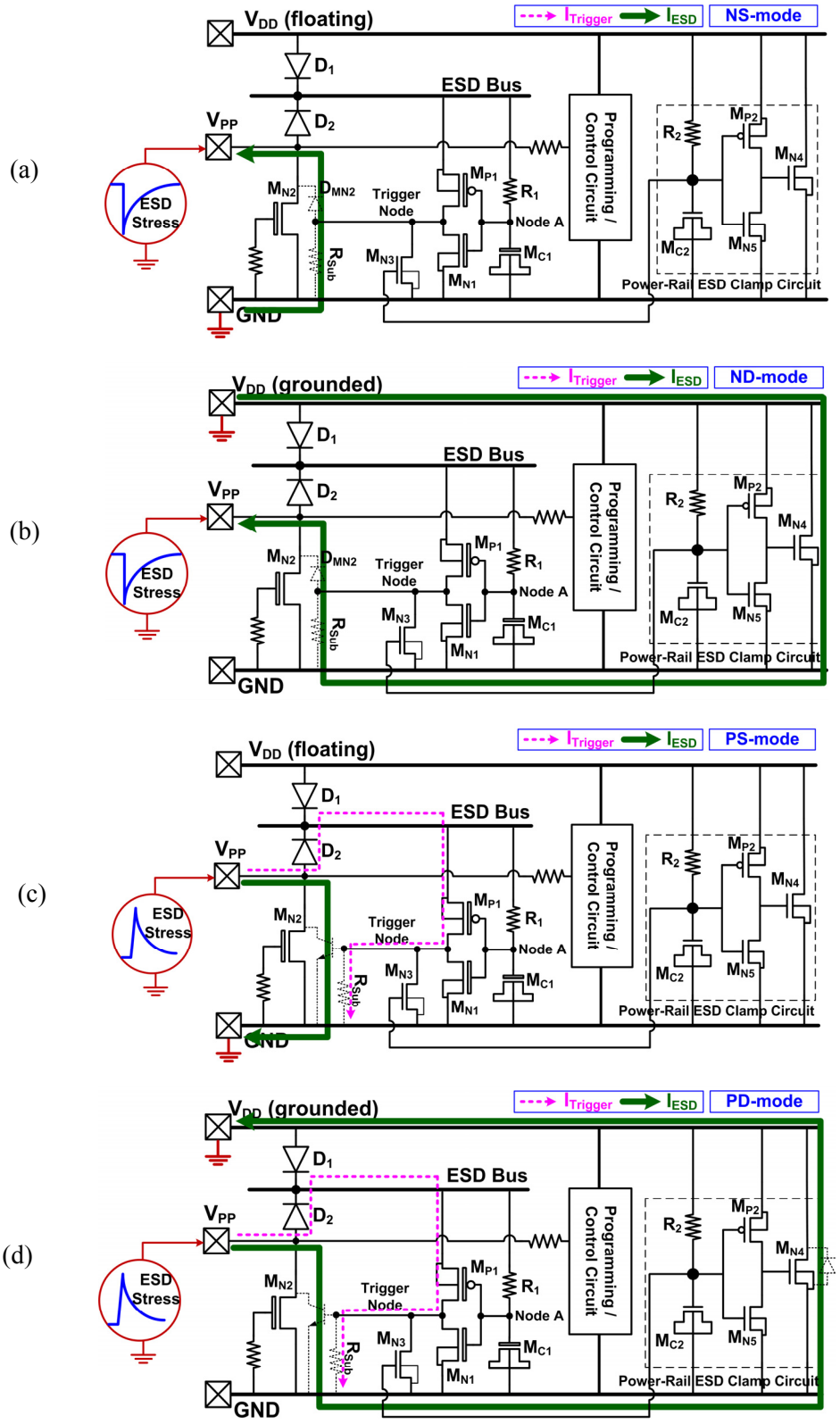


Fig. 6.10. ESD current discharging paths under (a) NS-, (b) ND-, (c) PS-, and (d) PD- mode, ESD tests. The dashed lines denote the substrate-triggered current to trigger on the ESD protection device M_{N2} and the solid lines show the primary ESD current flow.

Under PS-mode ESD test, initial ESD energy is diverted to the ESD bus through the diode D_2 to elevate the voltage level on ESD bus. The time delay from R_1 and M_{C1} keeps the node A at a low voltage level relative to that of ESD bus. Consequently, M_{P1} is turned on to provide substrate-triggered current into P+ trigger nodes of M_{N2}, as the dashed line ($I_{Trigger}$) shown in Fig. 6.10(c). The substrate-triggered current can efficiently trigger on the parasitic n-p-n BJT inherent in M_{N2}, and the PS-mode ESD current (I_{ESD}) is primarily discharged to the grounded GND line through the parasitic BJT. Under PD-mode ESD test, the ESD trigger circuit can provide substrate-triggered current $I_{Trigger}$ to turn on M_{N2} as well. The PD-mode ESD current I_{ESD} is therefore discharged to the grounded V_{DD} line through the substrate-triggered M_{N2}, the floating GND line, and the parasitic diode inherent in M_{N4} (Fig. 6.10(d)).

6.4.3. ESD Measurement Results

Among the ESD current discharging paths, it is known that PS- and PD-mode ESD tests are critical to V_{PP}-pin ESD protection because the ESD current is primarily discharged through the parasitic BJT inherent in the fully-silicided M_{N2}. The proposed ESD protection design under PS-mode ESD stresses was evaluated by using 100-ns TLP system. Failure criterion during TLP test was defined with 1 μA leakage current under 5 V bias on V_{PP} pin. With the substrate-triggered technique, the parasitic BJT inherent in M_{N2} was triggered on at ~10 V, and the measured secondary breakdown current was 3.8 A, as shown in Fig. 6.11. Measured HBM ESD protection levels of the IC product equipped with previous ESD protection design (Fig. 6.4) or the new proposed ESD protection design (Fig. 6.6) at V_{PP} pin are summarized in Table 6.2. In the HBM ESD tests, the starting test voltage was 0.5 kV, and the step voltage was 0.5 kV. V_{PP} pin was stressed three times at each HBM ESD level. Shift of I-V curve is the typical failure criterion used in the HBM ESD tests. Before ESD stress, a ±25V voltage sweep with limited current supply was applied on V_{PP} pin to acquire a fresh I-V

curve as the reference. Another post-stress I-V curve was measured and compared to this fresh I-V curve after the V_{PP} pin had been stressed three times at each selected ESD test level. It was judged as a failure when the post-stress I-V curve deviates more than 20% from its fresh I-V curve.

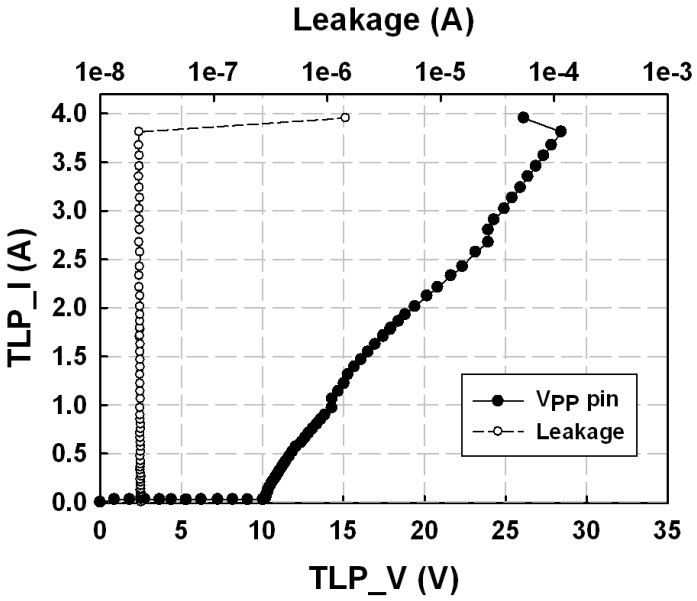


Fig. 6.11. TLP-measured *I-V* characteristics of the proposed ESD protection design under PS-mode ESD stress.

TABLE 6.2
MEASURED HBM ESD ROBUSTNESS OF THE IC PRODUCT
WITH PREVIOUS ESD PROTECTION DESIGN OR THE PROPOSED ESD PROTECTION DESIGN AT V_{PP} PIN.

	PS-mode	PD-mode	NS-mode	ND-mode
Original Design (Fig. 6.4)	2 kV	3.5 kV	4.5 kV	4.5 kV
Proposed Structure (Fig. 6.6)	5 kV	5 kV	> 8 kV	> 8 kV

With the PS- and PD-mode test results on V_{PP} pin listed in Table 6.2, the substrate-triggered technique in collaboration with the N-Well ballast layout can successfully enhance the turn-on speed and turn-on uniformity of M_{N2}. Therefore, HBM ESD protection

levels can be significantly increased up to 5 kV. For NS- and ND-mode ESD tests, because device dimension of the parasitic diode D_{MN2} is larger than that of the diode D_N in the previous ESD protection design, the proposed ESD protection design showed a higher HBM ESD protection level of over 8 kV. From the measurement results shown in Table 6.2, the custom-specified 4-kV HBM ESD protection level has been successfully achieved by the proposed ESD protection design. Die photograph of the IC with the proposed ESD protection design is shown in Fig. 6.12, which has a die size of 3.72 mm^2. The layout area of the proposed ESD protection circuit for V_{PP} pin is 24186 μm^2, where M_{N2} occupies a silicon area of 15900 μm^2.

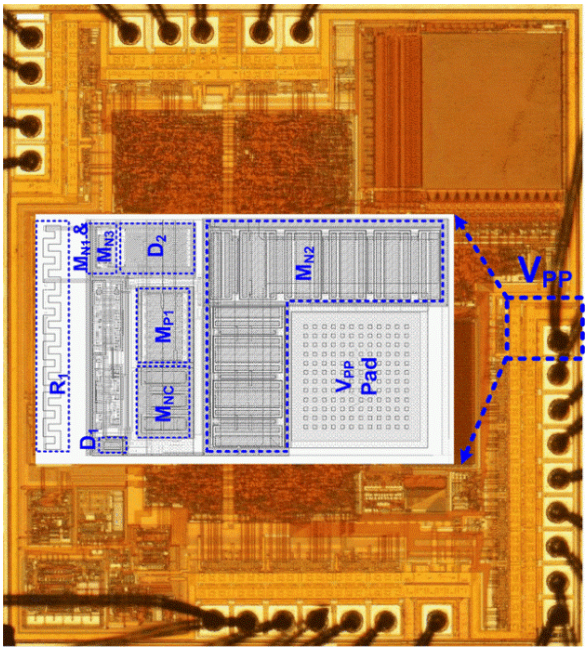


Fig. 6.12. Die photograph of the IC with proposed ESD protection design at V_{PP} pin. Technology node used in this work is a 0.35-μm fully-silicided CMOS process with OTP memory cells.

V_{PP} pin with the proposed ESD protection design after 5.5-kV PD-mode HBM ESD test was analyzed by OBIRCH SEM, as shown in Fig. 6.13(a) and 6.13(b), respectively. OBIRCH analysis revealed the location of ESD damage on the ESD protection NMOS M_{N2}. No light spots (no ESD damages) were found on internal circuits or the ESD trigger circuit. SEM

analysis further confirmed that ESD failure spots were located on M_{N2}. These failure analyses have verified that the proposed ESD protection design at V_{PP} pin is effective to protect internal circuits from being damaged by ESD stresses.

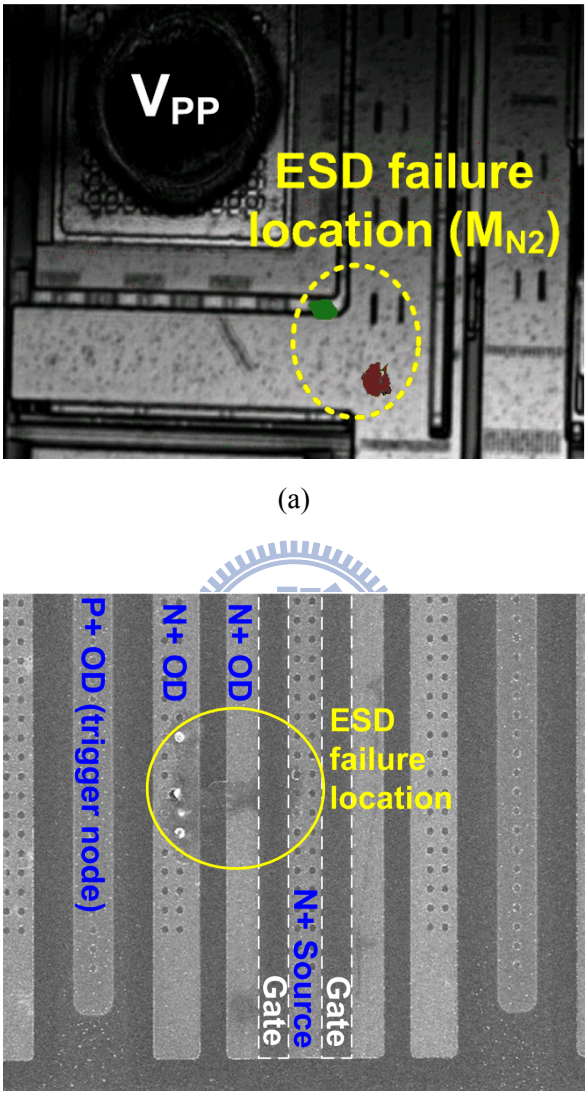


Fig. 6.13. (a) OBIRCH and (b) SEM images of the V_{PP} pin with the proposed ESD protection design after 5.5-kV PD-mode HBM ESD stress.

6.5. Summary

Due to the high programming voltage on V_{PP} pin, the ESD diode placed from I/O pad to V_{DD} is prohibited, which results in a stringent ESD design challenge for V_{PP} pin. Moreover,

the rise time of V_{PP} programming voltage could be as fast as several tens of nanoseconds to cause mis-triggering issue in some traditional ESD protection designs. A new ESD protection design has been proposed to overcome the mis-triggering issue due to fast V_{PP} programming voltage. A low-voltage NMOS was added at the output of ESD trigger circuit to overcome the mis-triggering issue on the ESD protection device during V_{PP} programming. Moreover, ESD bus in the proposed design can help prevent the mis-triggering issue as well by reducing the overdrive current from ESD trigger circuit. The proposed ESD protection design has been successfully implemented on a commercial IC product fabricated in a 0.35-μm fully-silicided CMOS process with OTP memory cells. Experimental results showed that the new design can successfully avoid the mis-triggering issue on ESD protection device when V_{PP} voltage had a rise time as fast as 25 ns. Under ESD stress conditions, ESD protection device can be efficiently triggered on by substrate-triggered current to achieve a high HBM ESD protection level of 5 kV. Accordingly, with a high immunity against mis-triggering and a good ESD robustness, the new proposed design is a competent ESD protection solution to the CMOS IC products with high-voltage programming pin.

Chapter 7

Investigation on The Transistor Holding Voltage Acquired from TLP in a High-Voltage Technology

7.1. Background

Due to the high power supply voltage of HV ICs, latchup issue has become one of the most serious problems in HV applications, especially on the power-rail ESD protection devices [133]. Furthermore, HV ICs usually have high junction breakdown voltage and high gate oxide breakdown voltage, therefore the ESD design effort is focused on increasing the holding voltage (V_h) and minimizing the latchup sensitivity.

To analyze the device characteristics under ESD stresses, 100-ns TLP system has been widely adopted. TLP is a system which pre-charges the transmission line (T-line) through a high-voltage power supply and then discharges the pre-charged energy into the device under test (DUT). A TLP system generates a square wave to stress the DUT, and with gradually increased pre-charged voltages on T-line, a TLP system is capable of measuring the snapback I-V characteristics of devices. For example, the device trigger voltage (V_{t1}), holding voltage (V_h), secondary breakdown current (I_{t2})…and so forth. Different from the 100-ns TLP system, a traditional curve tracer which sweeps a low-frequency voltage sine wave over the DUT can measure the snapback I-V characteristics, too. The frequency of the sine wave is low enough, so that the curve tracer measurement is considered as a DC measurement. Due to the long measurement duration, a curve tracer may damage the DUT especially under the snapback I-V measurement. Therefore, the holding voltages measured from the 100-ns TLP are sometimes regarded as reference data to latchup sensitivity in IC industry.

In this chapter, the holding voltages of an nLDMOS have been investigated by TLP systems with different pulse widths and the curve tracer. Transient latchup (TLU) test was

exploited to validate the measurement results.

7.2. Device Structure

The device cross-sectional view of an nLDMOS in a 0.25-μm 18 V BCD process is shown in Fig. 7.1. The clearance from drain contact to poly gate edge, N+ extension from the drain contact, and the gate length L_{ch} (poly gate overlap P-Drift) of the nLDMOS are optimized for ESD robustness. Gate and source electrodes of the nLDMOS are shorted together through internal metal wiring. The nLDMOS is laid out in finger type with each finger width of 50 μm, and the total device width is 400 μm.

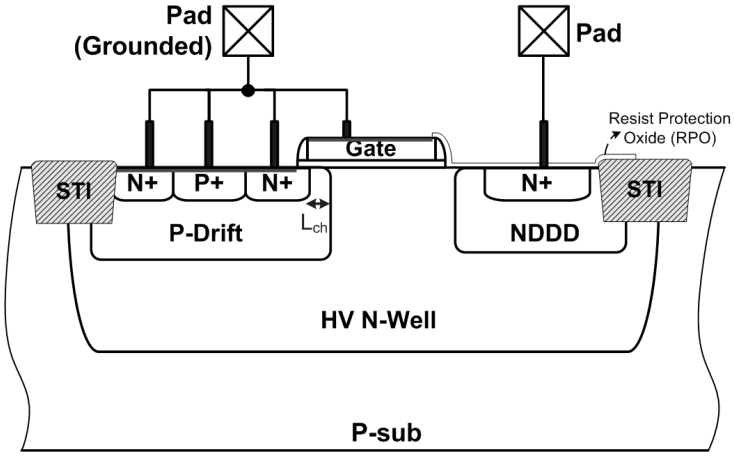
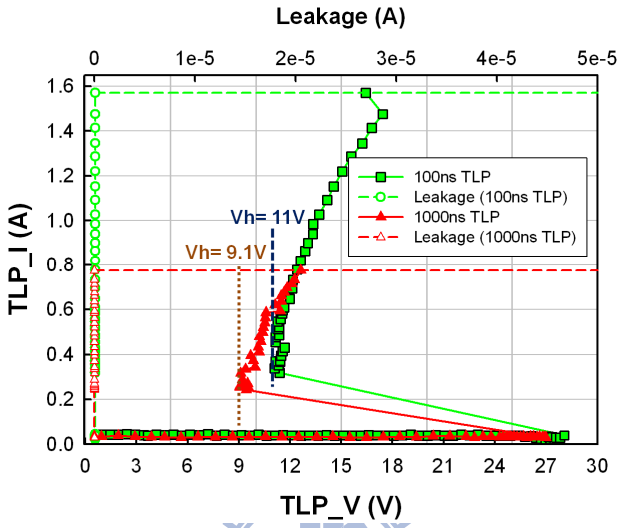


Fig. 7.1. Device cross-sectional view of the nLDMOS in an 18 V BCD process.

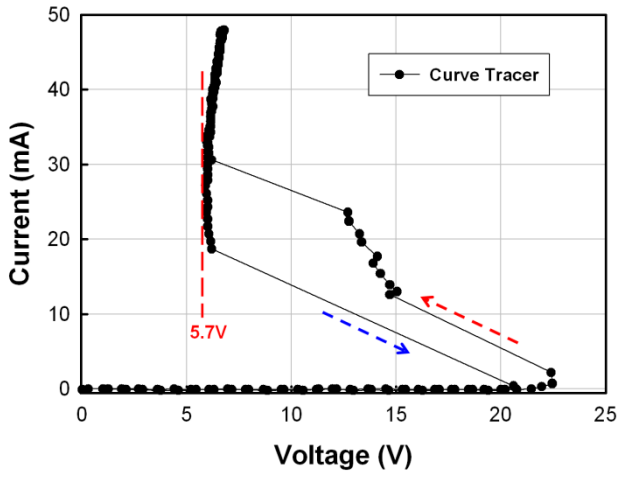
7.3. Experimental Results and Discussion

The I-V characteristic of the nLDMOS under 100-ns TLP measurement is shown in Fig. 7.2(a) (squares). Steps of the T-line pre-charge voltage are 0.5 V, and I-V points are the averaged data from 50% to 90% of the pulse period. I_{t2} of the nLDMOS is 1.5 A, and the corresponding HBM ESD robustness is higher than the general requirement of 2 kV. From the 100-ns TLP measurement, the nLDMOS shows a holding voltage of 11 V. However,

distinct from the results of low voltage devices, the holding voltage of nLDMOS under curve tracer measurement shows a substantial inconsistency to that measured by 100-ns TLP. As shown in Fig. 7.2(b), the holding voltage of nLDMOS under curve tracer measurement is 5.7 V only.



(a)



(b)

Fig. 7.2. I-V characteristics of the nLDMOS measured by (a) 100-ns and 1000-ns TLP, and (b) a DC curve tracer.

To investigate the huge V_h roll off from 100-ns TLP (11 V) to curve tracer (5.7 V), long-pulse TLP system with 1000-ns pulse width [134] was exploited. The long-pulse TLP

system is capable of providing pulse widths longer than100ns, so that the time-domain device behavior of HV devices after 100ns can be further observed. As the measured result shown in Fig. 7.2(a) (solid triangles), nLDMOS under 1000-ns TLP has V_h of 9.1 V, which is lower than the V_h under 100-ns TLP measurement but higher than the V_h under curve tracer measurement. The corresponding time-domain current and voltage waveforms of 1000-ns TLP measurement are shown in Fig. 7.3, where perceptible degradation over time is observed.

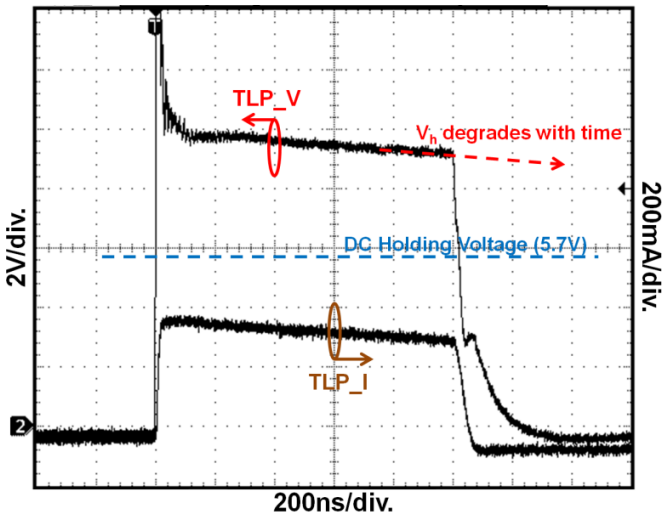


Fig. 7.3. Time-domain waveforms of the nLDMOS under 1000-ns long-pulse TLP measurement.

From the Wunsch-Bell model, the simplified temperature model $T(0,\tau)$ under the power source of a rectangular pulse with duration τ is $T(0,\tau)=\frac{q_0}{\sqrt{\pi D}}\sqrt{t}$ $(t<\tau)$ [135]. As a result, device temperature increases with time (t) during the duration of TLP pulses (τ). In HV devices, the high device holding voltages can further accelerate the self-heating effect. With the increasing device temperature over time, β-gain of the parasitic bipolar inherent in nLDMOS also increases. The holding voltage of nLDMOS therefore degrades while the time increases, as the waveform shown in Fig. 7.3. Extrapolating the measured voltage waveform in Fig. 7.3, time for the nLDMOS to reach V_h of 5.7 V is estimated as 3.2 μs.

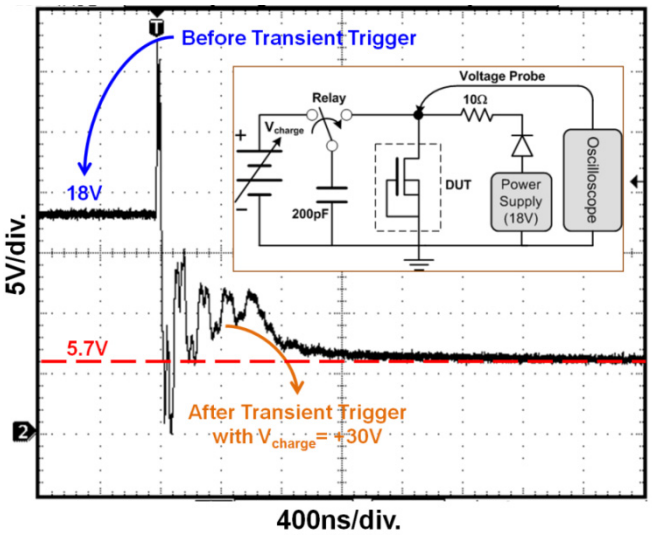


Fig. 7.4. Time-domain voltage waveform of the nLDMOS under transient latchup measurement with initial positive V_{charge} of +30V.

Transient latchup test has been verified as an effective test method to evaluate the susceptibility of CMOS ICs to the latchup induced by transient noises in field applications [136]–[138]. The test setup for TLU is shown in the inset of Fig. 7.4. In the TLU test, the nLDMOS was initially biased at normal circuit operating voltage of 18 V. A transient noise is injected into nLDMOS from the transient trigger source with pre-charged voltage V_{charge} of +30 V. After the transient triggering, the nLDMOS was driven into latchup state and clamped down the supply voltage. From the measured voltage waveform of TLU test in Fig. 7.4, the nLDMOS clamped the supply voltage to ~5.7 V, which is the same value of V_h under curve-tracer measurement. Moreover, time for nLDMOS to clamp the supply voltage into a steady state is roughly around 1000 ns, whereas the voltage at 1000 ns under 1000-ns TLP measurement in Fig. 7.3 is ~9 V. In consequence, the TLU test has verified that the TLP system overestimates the holding voltage of a HV device, which, in turn, could underestimate its susceptibility to latchup.

7.4. Summary

The holding voltage of an nLDMOS in a HV BCD process has been investigated by TLP measurements with different pulse widths and DC curve tracer. It is found that the holding voltages of an 18-V nLDMOS measured by 100-ns TLP system and curve tracer are substantially different, 11 and 5.7 V , respectively. The self-heating effect which degrades the holding voltage of nLDMOS over time has been observed. By using the long-pulse TLP, the self-heating speed of the HV transistors can be quantitatively estimated. TLU test further verifies that TLP systems overestimate the holding voltage of nLDMOS and underestimate its susceptibility to latchup. As a result, TLP measurement is not suitable for investigating the holding voltage of HV devices, especially for the latchup development because latchup events have the time duration longer than a millisecond.

Chapter 8

Conclusions and Future Works

This chapter summarizes main results of this dissertation and from the research results some suggestions and future works are proposed.

8.1. Main Results of This Dissertation

After a brief ESD introduction in Chapter 1, a waffle layout method that utilizes the body-current injection on the nLDMOS is proposed in Chapter 2. Through TLP and ESD measurements and failure analyzes, experimental results show that this proposed method is able to substantially improve turn-on uniformity of nLDMOS transistors in a 0.5-μm 16-V and a 0.35-μm 24-V BCD process. This waffle layout structure is suitable for I/O or power-rail ESD clamp circuit.

For open-drain structures, integrating SCR into output nLDMOS is a common ESD solution. However, the safe operating area, as one of the important reliability indicators of output arrays, is degraded due to the embedded SCR. In Chapter 3, SOA is reviewed along with some up-to-date technologies on improving SOA of HV transistors. Following the SOA review in Chapter 3, a poly bending method that alleviates the degradation on SOA performance but keeps the high ESD robustness from SCR is proposed in Chapter 4. With the poly bending layout method, a HV output array that has both high ESD robustness and wide SOA is available for HV ICs. Combining the results in Chapter 2 and 4, the two methods can provide excellent ESD robustness to HV ICs with either traditional or open-drain structures.

With ESD being a practical reliability requirement of ICs, two ESD designs for fully-silicided technologies are included in Chapter 5 and Chapter 6. In Chapter 5, two novel ballasting techniques are proposed. The proposed methods ballast not only the output NMOS,

but also the output PMOS transistor to maximize the ESD robustness. From measurement results on a real IC product, the two ballasting method effectively equipped the IC with at least 6 kV HBM ESD robustness.

In chapter 6, a fully-silicided ESD protection design for voltage programming pins is proposed. The proposed design features both high ESD protection level and high immunity against mis-triggering when the input voltage has a rise time similar to ESD events, tens of nanoseconds. A commercial IC equipped with this ESD protection circuit passed 5-kV HBM ESD robustness. Finally, in Chapter 7, a new phenomenon of HV transistors' holding voltage in response to stress time is investigated by using TLP systems with different pulse widths. Results in Chapter 7 are useful for the future development of high-latchup-immunity transistors or ICs in HV technologies.

8.2. Future works

For the operation of power MOSFETs, it is very often that the transistors' drain or ground potentials be perturbed greatly, especially when switching with a large current. Noise immunity of the nLDMOS transistors and the impact that comes from the SCR insertion is an important future work thereof. A challenge to this study would be the fact that noises from different systems or applications are case-sensitive, and presently there is no unified standard or platform suitable for device-level measurements. Testing ICs on their system boards is necessary for this noise study on power MOSFETs.

The V_{PP} pin ESD protection design in Chapter 6 has the lowest potential of 0 V because of its application specifications. For ICs with their lowest voltage potentials below 0 V, e.g. NAND memories, the ESD protection design along with its trigger circuit should be modified and it would be both interesting and useful to implement such an application-oriented ESD protection design.

With the high power supply voltages in HV applications, latchup is an extremely challenging reliability topic. Designing a structure with high latchup immunity has been an important development target in HV ICs for decades. From the research results in Chapter 7, the challenge becomes more stringent and correct measurement techniques to evaluate the latchup immunity of HV transistors are equally important. With the new observed phenomenon, latchup in HV ICs will face new challenges; new physical mechanisms to be discovered as well. Accordingly, latchup is a topic not only intriguing but also valuable to the IC industries, and worthy to put further efforts for future works and developments.

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Design and Applications of ESD Protection in High-Voltage Integrated Circuits

Publication List

(A). International Journal Papers:

[1] **Wen-Yi Chen**, E. Rosenbaum, and M.-D. Ker, "Diode-triggered silicon-controlled rectifier with reduced voltage overshoot for CDM ESD protection," *IEEE Trans. Device and Mater. Reliab.*, in press, 2012.

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(B). International Conference Papers:

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(C). US Patents:

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