

國立交通大學

電子工程學系電子研究所

博士論文

先進互補式金氧半電晶體及快閃式記憶元件中單
一電荷效應之統計性研究

Statistical Study of Single Charge Phenomena in
Advanced CMOS and Flash Memory

研究生：邱榮標

指導教授：汪大暉 教授

中華民國一〇二年二月

先進互補式金氧半電晶體及快閃式記憶元件中單一電荷效
應之統計性研究

Statistical Study of Single Charge Phenomena in Advanced
CMOS and Flash Memory

研究生：邱榮標

Student : Jung-Piao Chiu

指導教授：汪大暉

Advisor : Tahui Wang

國立交通大學

電子工程學系 電子研究所



A Dissertation

Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

February 2013

Hsinchu, Taiwan, Republic of China

中華民國一〇二年 二月

先進互補式金氧半電晶體及快閃式記憶元件中單一電荷效應之統計性研究

學生：邱榮標

指導教授：汪大暉博士

國立交通大學 電子工程學系 電子研究所

摘 要

本篇論文主要著重在單電子效應於先進互補式金氧半電晶體(advanced CMOS)及快閃式記憶元件(flash memory)之應用。高介電閘極氧化層(high- k)之可靠性議題，如電壓溫度引致不穩定(BTI)、隨機電報雜訊(RTN)之研究，亦有所探討。更利用蒙地卡羅模擬進一步驗證理論及實驗。

第一章首先描述本論文中單電子效應之應用研究成果。首先探討高介電閘極材料(high- k)金氧半電晶體元件中，藉由量測 NBTI 加速測試中，單一電荷捕捉及釋放所造成的臨界電壓及特徵時間變化，進一步探討在奈米級元件的可靠性議題。接下來吾人討論於 pMOSFET 中，同為單電子效應之 RTN 及 NBTI 的異同，並利用 reaction-diffusion(RD)模型及蒙地卡羅方法模擬 NBTI 缺陷之產生。此外，吾人於此篇論文最後，討論於快閃式記憶元件中寫入載子對於 RTN 之影響，主要探討浮動閘極(floating gate)、平面(planar)及鰭狀(FinFET)氮化矽(SONOS)快閃式記憶元件中，載子寫入前後 RTN 之變化。

在第二章中，吾人探討了在小面積 high- k 元件中，NBTI 造成之總臨界電壓變化(ΔV_t)分佈及其形成原因。吾人量測大量小面積元件之單電荷產生特徵時間及其造成之臨界電壓變化。吾人發現單電荷產生之特徵時間有數 decade 之廣，並

提出用 reaction-diffusion(RD)模型中之反應活化能角度詮釋此一現象，更進一步由特徵時間分佈萃取出反應活化能分佈。最後吾人提出一統計模型，此模型基於 RD 模型之基礎加入反應活化能分佈及單電荷造成之臨界電壓變化分佈。最後以蒙地卡羅模擬重現實驗 ΔV_t 分佈及其和 NBTI 操作時間的關係。

第三章延續第二章之主題，探討小面積 high-k 元件中，NBTI 造成之總臨界電壓變化(ΔV_t)分佈及其形成原因。不同於其他可靠度議題，NBTI 在操作電壓移除後有一特殊之回復現象。利用類似前一章的方法，吾人量測大量小面積元件之單電荷逸散特徵時間及其造成之臨界電壓變化。吾人以「熱助穿隧」模型解釋，並由缺陷能量分佈、空間分佈及反應活化能分佈進一步探討並萃取出反應活化能分佈。最後提出一統計模型，以熱助穿隧模型為基礎加上反應活化能分佈，完整解釋並預測回復現象造成之 ΔV_t 分佈及其和回復時間之關係。

單電子效應的應用除了 NBTI 之外，另一個重要的可靠度議題就是 RTN。這兩種現象之機制確有相似之處，近年來甚至有人認為 NBTI 是 RTN 在特殊偏壓條件下的產物。在第四章，吾人量測並比較製程產生之 RTN 缺陷(fresh RTN)、NBTI 操作產生之 RTN 缺陷(post-NBTI stress RTN)、NBT 測試過程中之單電荷引致臨界電壓變化，結果發現 NBTI 測試過程中之平均單電荷引致臨界電壓變化量大於製程產生之缺陷。為此吾人用 RD 模型進行 3D 模擬，結果顯示因為 NBTI 測試產生之缺陷位置較容易出現在主要電流滲透路徑，進而產生較大之單電荷引致臨界電壓變化。也間接證明 NBTI 之缺陷為新產生之缺陷，和製程產生之 RTN 缺陷不同。

在第五章中，吾人探討 SONOS 元件的寫入電荷對於 RTN 引致臨界電壓變化量的影響。吾人量測並模擬 RTN 在浮動式閘極(floating gate)、平面式 SONOS、鰭式 SONOS 之振幅大小，並記錄其在寫入/抹除前後的變化。研究發現 RTN 在

平面式 SONOS 寫入/抹除前後有大量的變化，而浮動式閘極幾乎在寫入/抹除前後擁有同樣大小之 RTN。主要是因為 SONOS 中氮化矽層儲存之電荷為一離散的狀態，使寫入/抹除前後之電流滲透路徑改變，而浮動式閘極因為電荷儲存層為導體，故 RTN 之大小不會因為寫入/抹除動作而有變化。最後吾人發現當 SONOS 由平面式結構進入鰭式結構，RTN 在寫入/抹除前後之變化量會被大幅度的壓抑，主要是因為電流導通路徑的限縮，及高度之對稱性使得寫入電荷對於電流導通路徑擁有等量的影響。

在第六章中，吾人研究了 nanowire-like 結構中的 RTN 振幅。在較寬的通道寬度元件中，電流導通路徑主要由隨機參雜決定，RTN 振幅也由缺陷位置和電流滲透路徑決定。但在 nanowire-like 結構，電流路徑被侷限於一個一維的通道，一個參雜僅能改變區域導通瓶頸(導電率)，而無法改變導通路徑。在本章中，吾人嘗試提出一個模型來描述 nanowire-like 結構的 RTN 振幅分佈。模型顯示 RTN 振幅的機率分佈遵守 Poisson 分佈，吾人亦利用蒙地卡羅模擬來證實理論。此外，如上一章提到的，由於在 SONOS 元件中寫入載子和通道參雜對於電流滲透路徑有一些類似的特性，此一理論亦可延伸並用於未來 nanowire-like 結構的 SONOS 快閃式記憶元件。

最後於第七章，吾人將對本論文做個總結。

關鍵字：蒙地卡羅模擬，先進互補式金氧半電晶體，氮化矽快閃式記憶元件，浮動式閘極快閃式記憶元件，高介電閘極氧化層，負電壓溫度引致不穩定，隨機電報雜訊，反應-擴散模型，熱助穿隧模型，單電荷產生，單電荷散逸，反應活化能萃取，缺陷位置萃取，電流通道滲透效應，布瓦松分佈

Statistical Study of Single Charge Phenomena in Advanced CMOS and Flash Memory

Student : Jung-Piao Chiu

Advisor : Dr. Tahui Wang

Department of Electronics Engineering & Institute of Electronics
National Chiao Tung University

ABSTRACT

This thesis will focus on single charge phenomena characterization and its applications to advanced CMOS and non-volatile flash memory. The reliability issues, such as negative bias temperature instability (NBTI) and random telegraph noise (RTN) in advanced gate dielectric (high- k), are studied statistically. Monte Carlo simulations are also performed to corroborate our model and experiment data.

In Chapter 1, applications of single charge phenomena statistics are firstly addressed. The second and the third chapters are the investigations of threshold voltage shifts arise from NBTI stress and post-NBTI recovery, respectively. And the fourth chapter is the study of NBTI and RTN amplitude distributions in high- k gate dielectric pMOSFETs. The program charge effect on RTN amplitude and its device structural dependence in SONOS flash memory is investigated in Chapter 5. Finally, an RTN amplitude distribution model is proposed in Chapter 6.

In Chapter 2, origins of a NBTI induced ΔV_t distribution in small-area HfSiON gate dielectric pMOSFETs are explored and characterized. We measure individual

trapped hole creation times and corresponding threshold voltage shifts during NBTI stress in a large number of devices. Wide dispersion of trap creation characteristic times in several decades is observed, which we attribute to an activation energy distribution in the reaction-diffusion (RD) model. We extract an activation energy distribution including a local electric field effect from measured characteristic times. A statistical model for an NBTI ΔV_t distribution by employing the RD model and convolving extracted activation energy and a single trapped hole induced V_t shift is developed. Our model reproduces measurement results of an overall NBTI induced ΔV_t distribution and its stress time evolutions well.

In Chapter 3, NBTI trapped charge characteristics and recovery mechanisms are examined by a statistical study of individual trapped charge emissions in small-area HfSiON/metal gate pMOSFETs. We measure trapped charge emission times in NBTI recovery in a large number of devices. The characteristic time distributions of the first three emitted holes are obtained. The distributions can be well modeled by using a thermally-assisted tunnel (ThAT) detrapping model. NBTI trapped charge energy and spatial distributions and its activation energy distribution in the ThAT model are discussed and extracted. We develop a statistical NBTI recovery ΔV_t model based on the ThAT and an extracted activation energy distribution. Our model can reproduce a recovery ΔV_t distribution and its temporal evolutions in small-area devices very well.

RTN and NBTI stress induced threshold voltage (V_t) fluctuations in high-k gate dielectric and metal-gate pMOSFETs are investigated in Chapter 4. We measured RTN amplitude distributions before and after NBTI stress. RTN in post-stressed devices exhibits a broader amplitude distribution than the pre-stress one. In addition, we trace a single trapped charge induced ΔV_t in NBTI stress and find that the average ΔV_t is significantly larger than a ΔV_t caused by RTN. A 3D atomistic simulation is performed to compare a single-charge induced ΔV_t by RTN and NBTI. In our simulation, the probability distribution of a NBTI trapped charge in the channel is

calculated from the reaction-diffusion model. Our simulation confirms that the NBTI induced ΔV_t indeed has a larger distribution tail than RTN due to a current-path percolation effect.

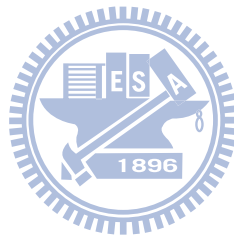
Nitride program charge effect on the amplitude of RTN in SONOS flash cells is investigated in Chapter 5. We measure and simulate RTN amplitudes in floating gate flash, planar SONOS, and FinFET SONOS cells. We find that a planar SONOS has a wide spread in RTN amplitudes after programming while a floating gate flash cell has identical RTN amplitudes in erase and program states. The spread of program-state RTN in a planar SONOS is attributed to a current-path percolation effect caused by random discrete nitride charges. The RTN amplitude spread can be significantly reduced in a surrounding gate structure, such as FinFET SONOS, due to a higher degree of symmetry in a program charge distribution.

In Chapter 6, amplitudes of RTN in MOSFETs possessing a nanowire-like channel are explored and modeled analytically. In large gate width MOSFETs, conducting current paths are modulated by random substrate dopants and large-amplitude RTN is attributed to a current path percolation effect. In ultra-thin body and narrow gate width MOSFETs, a current flow is physically confined to a one-dimension-like channel. A dopant charge does not alter a current path, but only modulates a local channel conductivity near the dopant. In this work, we attempt to derive an analytical RTN model for circuit simulation based on random dopant induced local conductivity modulation in a one-dimensional channel. We make an assumption that RTN amplitudes are linearly dependent on the number of dopants in the vicinity of an RTN trap. An influence range of a dopant charge is evaluated approximately from the Thomas-Fermi screening theory. The validity of this assumption is examined by numerical device simulation or experiment. Our model shows that RTN induced threshold voltage shifts exhibit a Poisson distribution. A Monte Carlo analysis of RTN induced ΔV_t by using a 3D device simulator is

performed to compare with our model. Reasonably good agreement between our model and the Monte Carlo RTN simulation is obtained for various doping concentrations and channel lengths.

Conclusions are finally made in Chapter 7.

Keyword: Monte Carlo simulation, advanced CMOS, SONOS, floating-gate flash, high- k , NBTI, RTN, reaction diffusion (RD) model, thermally-assisted-tunneling (ThAT) model, single charge creation, single charge emission, activation energy extraction, percolation effect, trap position extraction, Poisson distribution



ACKNOWLEDGEMENT

I would first like to express my deep gratitude to my advisor, Prof. Tahui Wang. His insightful guidance and encouragement are indispensable to the accomplishment of this dissertation.

I also show my appreciation to all of the committee members for their invaluable comments and suggestions. Moreover, I would like to acknowledge Dr. Chih-Sheng Chang and all the members in ATRD for their kindly support during my part-time job at TSMC.

During my study, many important people have influenced me. I would like to thank Dr. C. J. Tang, Dr. H. C. Ma, and Dr. C. C. Cheng for their guidance during my initial stage of Ph.D. study. In particular, the assistance in executing routine measurements and simulations from Mr. T. Y. Lin, Mr. C. Y. Wang, Mr. S. S. Liang, Mr. M. W. Wang, Mr. H. D. Hsieh and Mr. C. W. Li is also greatly appreciated. I am also indebted to the Wang and Chung group members of Emerging Device and Technology Lab, who had made life fun. Thanks to all who accompany me, their encouragement made me become more aggressive.

Scholarship from the department of electronics engineering at NCTU and from ZyXEL is deeply acknowledged for easing my financial pressure. I would also appreciate the National Science Council for providing me the travel grants to present papers in international conferences.

Finally, I would present my deepest love to my parents. Their love is the most important power supporting me. This dissertation is dedicated to them.

謝誌

首先，感謝指導教授汪大暉博士。沒有汪教授的教誨與鼓勵，這本論文將無法完成。

特別感謝論文口試委員在百忙之中給予寶貴的建議與指教。另外，在台灣積體電路製造公司工讀期間，前瞻技術研發部經理張智勝博士及所有全體同仁在研究與工作上的大力協助，在此由衷感謝。

在求學過程中，感謝學長唐俊榮博士、馬煥淇博士以及鄭志昌博士不吝分享所學，讓我快速進入狀況。此外，感謝學弟東陽、志宇、書祥、明瑋、泓達以及啟偉分擔實驗及模擬的工作。因為有你們的協助，使得這本論文更加充實。同時也感謝前瞻元件與技術實驗室所有成員，他們為我的博士班生涯增色許多。感謝所有陪伴過我的人，你們的支持鼓勵是我前進的動力。

感謝國立交通大學電子研究所及朱順一合勤科技提供獎學金，減輕我的經濟壓力。在此向國科會(National Science Council) 致上誠摯的謝意，提供經費補助，讓我前往國際會議發表論文。

最後，我要感謝長久以來支持我的家人，他們的愛是我的重要支柱。這本論文，獻給他們。

CONTENTS

Chinese Abstract		i
English Abstract		iv
Acknowledgement		viii
Contents		x
Table Captions		xiii
Figure Captions		xiv
List of Symbols		xxi
Chapter 1	Introduction	1
1.1	Backgrounds	1
1.2	Description of the Problem	3
1.3	Organization of this Dissertation	4
Chapter 2	Statistical Characterization of Individual Charge Trapping Times and Modeling of ΔV_t Distribution by NBTI Stress	10
2.1	Preface	10
2.2	Characterization of Individual NBTI Trapped Charge Creation	12
2.2.1	Devices and Measurement Setup	12
2.2.2	Single Charge Creation Induced Δv_t Distribution	13
2.2.3	Characteristic Times for Trapped Charge Creation	13
2.2.4	Activation Energy Distribution	15
2.3	Modeling of an NBTI Induced ΔV_t Distribution	16
2.3.1	Measured NBTI Induced ΔV_t Distribution	16
2.3.2	Monte Carlo Simulation Flow	17
2.3.3	Monte Carlo Simulation Results and Discussion	18
2.4	Summary	19
Chapter 3	Statistical Characterization and Modeling of a ΔV_t Distribution and Its Temporal Evolutions in NBTI Recovery	34
3.1	Preface	34
3.2	Statistical Characterization of NBTI Recovery	35
3.2.1	Single Charge Emission Induced Δv_t Distribution	35
3.2.2	Trapped Charge Emission Times	36
3.2.3	Trapped Charge Spatial and Energy Distributions	37
3.2.4	Activation Energy Distribution	39
3.2.5	Reproducible Feature of NBTI Recovery	41
3.2.6	Comparison with Charge Trapping/De-trapping Model	41
3.3	Modeling of a Recovery ΔV_t Distribution	43
3.3.1	Measured NBTI Induced ΔV_t Distribution	43
3.3.2	Monte Carlo Simulation Flow	43
3.3.3	Monte Carlo Simulation Results and Discussion	44

3.4	Summary	44
Chapter 4	A Comparative Study of NBTI and RTN Amplitude Distributions in High-k Gate Dielectric pMOSFETs	61
4.1	Preface	61
4.2	Measurement Results and Discussion	62
	4.2.1 Devices and Measurement Setup	62
	4.2.2 Distribution of Single Charge Induced v_t shifts	62
	4.2.3 Trap Position Extraction	63
4.3	Simulation of a NBTI Stress Induced Δv_t	63
	4.3.1 3D atomistic Monte Carlo Simulation Method	63
	4.3.2 Results and Discussion	64
4.4	Summary	66
Chapter 5	Program Charge Effect on Random Telegraph Noise Amplitude and Its Device Structural Dependence in SONOS Flash Memory	76
5.1	Preface	76
5.2	Program Charge Effect on RTN Amplitude in Floating Gate and SONOS Flash Memory	77
	5.2.1 Measurement of RTN Amplitude in MLC Flash	77
	5.2.2 Statistics Result of Program-state and Erase-state RTN	78
	5.2.3 Correlation Factor for Program-state and Erase-state RTN	78
	5.2.4 P/E Cycle Dependence of RTN	79
	5.2.5 3D Atomistic Simulation of RTN	79
5.3	Device Structural Dependence on RTN in SONOS Flash Memory	80
	5.3.1 Program Charge Effect on RTN in FinFET SONOS	80
	5.3.2 Degree of Inversion in FinFET SONOS	81
	5.3.3 Channel Width Effect on Program Charge Induced Percolation Effect	81
5.4	Summary	82
Chapter 6	Physical Origin and Analytical Modeling of RTN Amplitude Distribution in MOSFETs with a Nanowire Like Channel	103
6.1	Preface	103
6.2	One-Dimensional Channel RTN Simulation	105
6.3	Analytical RTN Amplitude Distribution Model	108
6.4	Results and Discussion	109
6.5	Summary	110
Chapter 7	Conclusions	121
References		124

Vita
Publication List

139
140

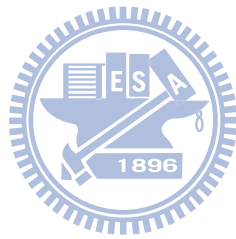


TABLE CAPTIONS

Chapter 2

Table 2.1 Comparison of trapped charge creation and emission characteristics in NBTI stress and NBTI recovery. i is a sequence number in trapped charge creation in NBTI stress or trapped charge emission in NBTI recovery. 24

Chapter 5

Table 5.1 Measured RTN correlation factors in FG flash, planar SONOS and FinFET SONOS cells. 89

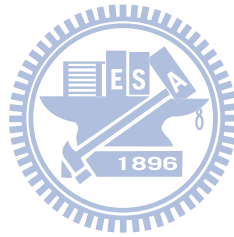


FIGURE CAPTIONS

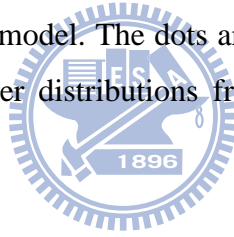
Chapter 1

- Fig. 1.1 Projections of gate leakage current and equivalent oxide thickness (EOT) from ITRS roadmap for low-standby-power applications. 6
- Fig. 1.2 A typical two-level RTN waveform resulting from electron capture/emission at an oxide trap. τ_c and τ_e are electron capture and emission times, respectively. ΔI_d is RTN amplitude. 7
- Fig. 1.3 Typical V_t traces during NBTI stress (a) and recovery (b). Each step-like “quantum jump” represents a single charge capture/emission. 8
- Fig. 1.4 (a) Estimation of threshold voltage shift as a function of process node [1.39] (b) measured V_t distribution of a 4-level MLC with level enlarged [1.39] and (c) noise distributions of 90nm, 70nm, and 50nm flash memory technologies [1.40]. 9

Chapter 2

- Fig. 2.1 Comparison between I_d degradation traces in (a) nowadays (b) previous devices. 20
- Fig. 2.2 Example V_t trace in NBTI stress in a high-k gate dielectric pMOSFET. τ_1 , τ_2 and τ_3 are the 1st, the 2nd and the 3rd trapped hole creation times. $\Delta v_{t,1}$, $\Delta v_{t,2}$ and $\Delta v_{t,3}$ are the 1st, the 2nd and the 3rd trapped hole induced threshold voltage shifts. The inset shows subthreshold I_d - V_g before and after NBTI stress. 21
- Fig. 2.3 The probability density function of a single trapped charge (hole) induced threshold voltage shift. The solid line represents an exponential fit. 22
- Fig. 2.4 The probability distribution of a trapped hole creation time in NBTI stress collected from about 130 devices. τ_1 , τ_2 and τ_3 are the 1st, the 2nd and the 3rd trapped hole creation times, respectively. The solid line represents a Gaussian fit. 23
- Fig. 2.5 Effective activation energy distributions extracted from measured trap creation times, τ_1 , τ_2 and τ_3 . The solid line represents a Gaussian-distribution fit to the E_{eff} translated from τ_1 . 25
- Fig. 2.6 NBTI induced ΔV_t versus number of trapped holes in a device at a stress time of 0.5sec (a) and 5sec (b). Each data point represents a device. The slope of a straight line represents an average Δv_t caused by a single trapped hole. 26

Fig. 2.7	The mean of the ΔV_t distribution versus NBTI stress time from measurement and from our model.	27
Fig. 2.8	The variance of the ΔV_t distribution versus NBTI stress time from measurement and from our model.	28
Fig. 2.9	A Monte Carlo simulation flowchart. M is the number of precursors in a device. A precursor density of $1 \times 10^{12} \text{ cm}^{-2}$ is assumed.	29
Fig. 2.10	Monte Carlo generated τ_i distributions. Only $i=1$ to 4 are shown in the figure.	30
Fig. 2.11	Trapped charge creation time distributions from measurement (symbols) and from Monte Carlo simulation (lines) after the re-ordering. The Monte Carlo simulated $\langle \log(\tau_2) \rangle - \langle \log(\tau_1) \rangle$ is 1.68 and $\langle \log(\tau_3) \rangle - \langle \log(\tau_1) \rangle$ is 2.67.	31
Fig. 2.12	Complementary cumulative distribution functions (1-CDF) of NBTI induced ΔV_t from measurement and from our model. The stress time is 0.01sec, 1sec and 100sec, respectively. The inset shows the probability distributions of ΔV_t from measurement and this model.	32
Fig. 2.13	Comparison of NBTI induced ΔV_t distributions (1-CDF) calculated from this model and from the Poisson model. The dots are measurement result. The inset shows trapped charge number distributions from the two models. The stress time is 100 sec.	33



Chapter 3

Fig. 3.1	Example ΔI_d and V_t traces in NBTI relaxation. τ_1 , τ_2 and τ_3 are the 1 st , the 2 nd and the 3 rd trapped hole emission times, respectively. $\Delta v_{t,i}$ ($i=1,2,3$) represents a single emitted charge induced threshold voltage shift.	46
Fig. 3.2	The magnitude distributions of $\Delta v_{t,1}$, $\Delta v_{t,2}$ and all collected $\Delta v_{t,i}$ from NBTI recovery traces in 170 high-k/metal gate pMOSFETs. The solid line represents an exponential fit.	47
Fig. 3.3	The probability density distributions of a trapped charge (hole) emission time in a $\log(\tau)$ scale. τ_1 , τ_2 and τ_3 are the 1 st , the 2 nd and the 3 rd trapped hole emission times, respectively. The mean ($\langle \log(\tau_i) \rangle$) and the standard deviation (σ_i) of the distributions are indicated in the figure. The symbols are measurement result and the solid lines are from Monte Carlo simulation. A Monte Carlo simulation procedure is given in Fig. 3.10.	48

Fig. 3.4	Histogram of all trapped charge emission times in a $\log(\tau)$ scale collected from 170 devices. The occurrence number distribution is rather uniform in a period from 10^{-2} s to 10^3 s.	49
Fig. 3.5	Schematic representation of a band diagram of a high-k/metal gate pMOSFET in relaxation. x_i and E_t represent a trapped charge position and energy.	50
Fig. 3.6	Activation energy (E_a) distributions extracted from the τ_1 , τ_2 and τ_3 , respectively. τ_0 in Eq. (4) is chosen such that the mean of the E_a is about 0.5eV. The solid line is a Gaussian-distribution fit.	51
Fig. 3.7	The dependence of $\langle\tau_1\rangle$ on recovery temperature. The extracted activation energy is about 0.5eV. Each data point is an average of ten readings.	52
Fig. 3.8	Dependence of trapped electron emission times on recovery gate voltage. 15 measurements are made for each recovery V_g to take average.	53
Fig. 3.9	A PDF plot of an emission time measured from an individual trap.	54
Fig. 3.10	An illustration of difference of trap energy between NBTI and RTN defects.	55
Fig. 3.11	A total V_t shift (ΔV_t) versus number of emitted trapped holes in a device at a recovery time of 0.1s, 10s and 1000s. Each data point represents a device. The slope of a straight line represents an average Δv_t caused by a single trapped hole emission.	56
Fig. 3.12	The evolution of ΔV_t with a recovery time. The solid line represents an average of measured ΔV_t traces in 170 devices. The symbols are the mean of Monte Carlo simulated ΔV_t distributions. A logarithmic time dependence of ΔV_t is obtained.	57
Fig. 3.13	Simulation flowchart of a Monte Carlo based ΔV_t distribution model for NBTI recovery in small area devices.	58
Fig. 3.14	The probability density distributions of NBTI recovery ΔV_t in 80nmx30nm pMOSFETs from measurement and from a Monte Carlo simulation. The recovery time is 0.1s, 10s, and 1000s.	59
Fig. 3.15	The variance of a recovery ΔV_t distribution versus a recovery time in 80nmx30nm pMOSFETs from measurement and from a Monte Carlo simulation.	60

Chapter 4

Fig. 4.1	(a) RTN measured at $V_D = -0.05V$ and a target I_D of $-500nA$. The V_t waveform is obtained from the measured drain current divided by a transconductance. (b) Threshold voltage trace in NBTI stress. The stress condition is $ V_g - V_t = 1.5V$ and the measurement condition is the same as RTN measurement.	68
Fig. 4.2	(a) Cumulative probability distribution of a single trapped charge induced Δv_t in RTN vs. NBTI. RTN is measured in fresh devices. (b) Cumulative probability distributions of a single-charge induced Δv_t for RTN in fresh devices and in post-NBTI stress devices. The minimum detectable Δv_t is about $1mV$.	69
Fig. 4.3	(a) RTN trap position distribution along the channel extracted from 124 devices. L_{trap} is the distance of a trap from the source and L_{DS} denotes a channel length. (b) RTN trap position distribution along the channel extracted from 124 devices. x_t is the distance of a trap from the channel.	70
Fig. 4.4	RTN amplitude distributions versus trap vertical (a) and lateral (b) positions.	71
Fig. 4.5	Relative NBTI trap creation probability versus a local surface hole concentration. A local hole concentration and a surface electric field are calculated from a 3D device simulation with random and discrete substrate dopants. In the calculation, E_0 in Eq. (2) is $1.1MV/cm$.	72
Fig. 4.6	Complementary cumulative probability distributions of RTN and NBTI amplitudes from 3D atomistic simulation. The simulated devices have a gate length of $30nm$ and a gate width of $30nm$. The NBTI trapped charge position in the simulation is selected according to its creation probability calculated from Eq. (4.2).	73
Fig. 4.7	Cumulative probability density distributions of RTN induced Δv_t amplitude in devices with $W/L = 30nm/30nm$ w/ and w/o random doping and $W/L = 40nm/40nm$.	74
Fig. 4.8	Single charge induced Δv_t distributions in different device sizes [4.2].	75
 Chapter 5		
Fig. 5.1	An illustration of two different program charge storage characteristic resulting distinct outcome of percolation path. Continuous distribution in FG flash and random discrete distribution in SONOS flash.	84
Fig. 5.2	RTN amplitude versus drain current in a FG flash cell at two program window : $1V, 2V$. The drain voltage in measurement is $0.7V$ and the gate voltage is	85

varied.

- Fig. 5.3 RTN amplitude versus drain current in a SONOS flash cell at two program window : 0.8V, 1.5V. The drain voltage in measurement is 0.7V and the gate voltage is varied. 86
- Fig. 5.4 Measured program-state RTN amplitude versus erase-state RTN amplitude in 40 FG flash cells. The RTN amplitude is measured at $I_d=500\text{nA}$ @ $V_d=0.7\text{V}$. The device dimension is $W/L=0.11\mu\text{m}/0.09\mu\text{m}$. The program window is 1V or 2V. 87
- Fig. 5.5 Measured program-state RTN amplitude versus erase-state RTN amplitude in 60 planar SONOS cells. The RTN amplitude is measured at $I_d=500\text{nA}$ @ $V_d=0.7\text{V}$. The SONOS cells have $W/L=0.09\mu\text{m}/0.08\mu\text{m}$, a 2.8nm tunnel oxide, a 6nm Si_3N_4 and a 6nm top oxide. 88
- Fig. 5.6 RTN amplitude versus drain current in a FG flash cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied. 90
- Fig. 5.7 RTN amplitude versus drain current in a SONOS cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied. 91
- Fig. 5.8 Measured RTN waveform and I_d versus V_g plot (a) in erase-state and (b) in program-state of a SONOS cell. Electron trapping at an interface trap is manifested by a current discontinuity in the I_d - V_g plot. 92
- Fig. 5.9 The waveform of two-level RTN current switching is observed in erase-state and 1st and 2nd program-state. 93
- Fig. 5.10 Simulation flow chart of our 3D atomistic simulation for RTN amplitude at program state and erase state for both FG flash and planar SONOS flash. 94
- Fig. 5.11 Simulated RTN amplitude versus drain current in a FG flash cell. Program-state and erase-state have the same placement of substrate random dopants. The RTN trap is placed in the middle of the device. 95
- Fig. 5.12 Simulated RTN amplitude versus drain current in a planar SONOS cell. Program-state and erase-state have a fixed placement of substrate dopants. Ten different sets of random program charges are simulated. An RTN amplitude due to number fluctuation is calculated with continuous substrate doping and program charges. 96
- Fig. 5.13 Cross-section of a FinFET SONOS and the electron concentration contour in the 97

FinFET SONOS obtained from a 2D simulation.

- Fig. 5.14 RTN amplitude versus drain current in a FinFET SONOS cell for two P/E cycles. 98
- Fig. 5.15 Program-state RTN amplitude versus erase-state RTN amplitude in FinFET SONOS cells. The fin width is 10nm. (a) RTN is measured at $I_d=500\text{nA}$ and (b) RTN is measured at $I_d=200\text{nA}$. 99
- Fig. 5.16 In a planar SONOS, percolation paths are widely distributed in the gate width direction. In a FinFET SONOS, conducting paths are confined to a small region in the corner of the Si fin. 100
- Fig. 5.17 Measurement of the correlation factor in FinFET SONOS with two different fin width, 10 nanometer and 25 nanometer. The correlation factor increases from 0.82 to 0.94 as the fin width reduces from 25 nanometer to 10 nanometer. 101
- Fig. 5.18 A 3D RTN simulation in planar SONOS with different channel width. The correlation factor is calculated based on a sample size of 40 devices. 102

Chapter 6

- Fig. 6.1 3D atomistic simulation of an electron concentration distribution in a cylindrical channel MOSFET. The diameter of the channel is 6nm. (a) Electron concentration distributions in two cross-sections, A and B. B has a dopant charge at the center and A does not have a dopant charge. (b) An electron density distribution along the channel. The Thomas-Fermi screening length ($[kT/4\pi n_c e^2]^{1/2}$) is shown in the figure. 112
- Fig. 6.2 Illustration of a one-dimensional channel RTN simulation scheme. The simulated MOSFET has a double gate structure. The channel is divided into many 1nm slices. In simulation, a dopant charge is placed uniformly in a slice and an RTN charge is placed in a 1nm bar on top of the channel. 113
- Fig. 6.3 Complementary cumulative distribution function (1-CDF) of RTN induced ΔV_t from a 3D atomistic simulation and from the 1D channel RTN simulation. The devices have a doping concentration of $1 \times 10^{19}/\text{cm}^3$ and a channel length of 40nm. The gate width is 20nm in (a) and 7nm in (b). 114
- Fig. 6.4 1D channel Monte Carlo simulation of RTN induced ΔV_t . The channel length is 40nm and each device has 14 dopants. A dopant number in the RTN trap section (n) is equal to 0, 1, 2 and 3, respectively. For each n , we simulate 100 devices. 115

(a) RTN induced V_t shifts in totally 400 devices. (b) The distribution of RTN induced ΔV_t for each n .

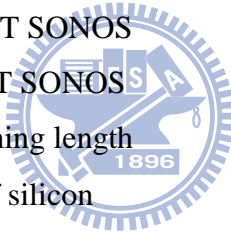
- Fig. 6.5 Average RTN amplitude and a standard deviation versus a dopant number in an RTN trap section (n). 116
- Fig. 6.6 Measured average RTN induced ΔV_t versus a CHE program window in 45 SONOS cells. A linear relationship between the ΔV_t and a program V_t window is obtained. 117
- Fig. 6.7 Complementary cumulative distribution function of RTN induced ΔV_t from 1D channel Monte Carlo RTN simulation and from this analytical model. The doping concentration is $1 \times 10^{19}/\text{cm}^3$, $7 \times 10^{18}/\text{cm}^3$ and $5 \times 10^{18}/\text{cm}^3$ respectively. The gate length is 40nm. 118
- Fig. 6.8 Complementary cumulative distribution function of RTN induced ΔV_t from 1D channel Monte Carlo RTN simulation and from this analytical model for two different gate lengths, $L_c=30\text{nm}$ and 40nm . The doping concentration is $1 \times 10^{19}/\text{cm}^3$. 119
- Fig. 6.9 Complementary cumulative distribution function of RTN amplitude distribution in FinFET SONOS cells with a fin width=10nm. A Poisson-like shape is obtained. 120



LIST OF SYMBOLS

ΔV_t	Threshold voltage shift in total during stress/recovery
Δv_t	Single charge induced threshold voltage shift during stress/recovery
σ_s	Standard deviation of NBTI stress induced Δv_t
t	Time
n	Power factor in RD model
N	Total number of stress created traps
ΔI_d	Drain current shift in total during stress/recovery
g_m	Transconductance
SS	Subthreshold swing
i	Trap creation/emission sequence number
τ_i	Characteristic time of i -th charge creation/emission
$\langle \rangle$	Mean value
σ_i	Standard deviation of τ_i
N_t	Bulk trap number
γ	Electric field acceleration parameter [1.28]
F	Electric field
E_D	Activation energy combined for D_{H2} , k_H , and k_{H2} [1.28]
W	Device channel width
L	Device channel length
D_0	Pre-factor of Arrhenius diffusivity in RD model
K_{F0}	Pre-factor of Arrhenius generation rate in RD model
K_{R0}	Pre-factor of Arrhenius recombination rate in RD model
k_B	Boltzmann constant
T	Temperature
E_{eff}	Effective activation energy including a local electric field effect in stress
M	Precursor number
σ_r	Standard deviation of NBTI recovery induced Δv_t
E_a	Effective activation energy of trap emission in NBTI recovery
T_{IL}	Interfacial later thickness

x_i	Distance of the i -th trapped charge from HK/IL interface
E_t	Trap energy
Φ_B	HK/IL conduction band offset
m_{IL}^*	Effective mass of hole in IL
m_{HK}^*	Effective mass of hole in HK
m_0	Free electron mass
q	Electronic charge
\hbar	Reduced Planck constant
d	HK thickness
Δx	Distance between adjacent trapped charges
τ_c	RTN capture time
τ_e	RTN emission time
σ_0	Trap cross section
v_{th}	Thermal velocity
f	Correlation factor
H_{fin}	Fin height of a FinFET SONOS
W_{fin}	Fin width of a FinFET SONOS
l	Thomas-Fermi screening length
ϵ_{Si}	Dielectric constant of silicon
$C(N,n)$	Binomial coefficient
λ	Mean value in a Poisson distribution



Chapter 1

Introduction

1.1 Backgrounds

The dimensions of the smallest demonstrated prototypes of silicon based CMOS devices [1.1][1.2] have been rapidly approaching the physical limit. Continual downscaling boosts device performance to meet the Moore's Law at the expense of growing leakage problems. The gate leakage currents [1.3] and the channel leakage currents [1.4] increase rapidly with decreasing gate dielectric thickness and with shorter channel length respectively. The resultant intolerable standby power consumption has made further scaling impractical. To resolve this issue, introduction of high permittivity (high-k) materials as the gate dielectrics [1.5][1.6] have been proposed to suppress gate leakage current due to physical thickness and keep the equivalent-oxide-thickness (EOT) reasonably small at the same time to maintain the high performance, as shown in Fig. 1.1. Part of this work thus concentrates on the high-k dielectric reliability.

In nowadays high-k technology, Hf-based materials are most promising and their film chemistry [1.7][1.8], process optimization [1.9][1.10], as well as reliability assessment and analysis [1.11]-[1.13] are being extensively studied. Recently, HfSiON has been successfully integrated into CMOS devices as gate dielectric for low power applications with good reliability, comparable mobility (as SiO₂), and greatly reduced gate leakage [1.9][1.11].

As one of the most important degradation modes in CMOS technologies, the negative bias temperature instability (NBTI) has been known since the 1970s [1.14].

The reaction-diffusion (RD) model [1.14]-[1.17] and a charge trapping model [1.18]-[1.23] are commonly adopted for NBTI degradation. The RD model can well describe the mean of an NBTI induced ΔV_t distribution, or a ΔV_t in a large area device. However, hydrogen back-diffusion [1.17] in the framework of the RD model was not able to explain a NBTI recovery phenomenon which shows a $\log(t)$ dependence of ΔV_t on relaxation time [1.24][1.25]. Since it was suggested that RD model cannot explain NBTI recovery transient and the shape of AC duty cycle dependence [1.21]. This apparent failure of RD framework has inspired a reintroduction of “well-based” charge trapping model [1.21]-[1.23][1.26]. However, the charge trapping model fails to explain the power-law dependence of ΔV_t evolution on stress time.

Aforementioned, unlike most reliability effects, NBTI V_t degradation recovers partly after the removal of stress [1.27]. Wang et al used a fast transient technique to characterize NBTI recovery and found a $\log(t)$ dependence of ΔV_t on relaxation time [1.24]. A $\log(t)$ dependence was also reported in [1.25] where the authors proposed a dispersive transport model within the RD framework to overcome the apparent deficiency of the RD model in relaxation time dependence. Alam et al ascribed a $\log(t)$ recovery transient to a fast charge detrapping process on top of slower N_{it} re-passivation as encapsulated by the RD model [1.28][1.29]. More recently, Grasser et al used a time dependent defect spectroscopy method to investigate NBTI recovery and concluded that NBTI recovery is due to thermally-assisted discharging of traps and no diffusion process is involved [1.23].

In addition to NBTI, random telegraph noise (RTN) phenomenon arising from charge emission and capture at an interface trap site [1.30]-[1.33] has been recognized as a new scaling concern in both advanced CMOS [1.34]-[1.36] and flash memory

[1.37]-[1.42]. Typical two-level RTN pattern is shown in Fig. 1.2.

With respect to flash memory devices, they play an important role in VLSI industry with their wide applications. NOR-type flash memory is suitable for code storage applications, such as mobile phones and handheld devices. On the other hand, NAND-type flash memory is suitable for data storage applications, such as USB and solid-state-disk (SSD). Part of this work thus concentrates on the RTN effect on flash memory cells.

1.2 Description of the Problem

As device dimensions reduce to a nanometer scale, the number of traps generated by NBTI stress varies significantly from a device to a device due to stochastic process of trap generation and dispersion of activation energy in the RD model. In these nanoscale transistors, NBTI induced ΔV_t scatters widely and it is no longer sufficient to consider just the mean value of ΔV_t in circuit simulation. An accurate model of an entire ΔV_t distribution and its stress time evolution is needed in a worst-case circuit simulation to ensure that the tail of ΔV_t distribution does not cross the reliability criteria during the specified lifetime of an integrated circuit [1.43]-[1.45]. While the mean of an NBTI ΔV_t distribution, or a ΔV_t in a large area device, can be well described by the RD model [1.14][1.16][1.17][1.28], the RD model alone is insufficient to predict an entire ΔV_t distribution in small area devices with stress time. On the other hand, the post-NBT recovery has the same issue that ThAT model alone is insufficient to predict an entire ΔV_t distribution in small area devices with recovery time. As a result, we develop statistical models for both NBTI stress and recovery by characterization of single charge creation/emission (Fig. 1.3) using fast transient measurement technique.

Furthermore, as the technology node is scaled down, RTN also becomes a more and more important reliability issue in both CMOS and flash memory technologies. A single charge trapping/detrapping will induce a large fluctuation in read current and thus a read failure. As a result, the RTN amplitude and its trap positions are also studied in this dissertation.

In terms of charge storage devices, two state-of-the-art structures attract great attention. One is floating gate (FG) flash and the other is charge trapping (CT) flash. Recently, 3D structures have been proposed for flash memory arrays. V_t fluctuations originated from a large-amplitude RTN tail will cause a read error and become a prominent issue in designing a multilevel-cell (MLC) flash memory in 45nm technology node and beyond, as shown in Fig. 1.4. We will thus focus on the RTN amplitude distributions and its dependence on program window in FG, planar SONOS and FinFET SONOS flash memory cells.

At present, RTN amplitude model is an empirical formula. However, the underlying RTN physical mechanism must be understood in order to make meaningful projection of device/circuit lifetime. Since it's hard to derive a 3D RTN amplitude model directly, we start from 1D device structures which are also promising candidates in future VLSI technology. We use a 3D Monte Carlo simulation to verify our model.

1.3 Organization of this dissertation

This dissertation consists of seven chapters. The scope of the dissertation mainly focuses on the applications of single charge phenomena in advanced CMOS and SONOS flash memory. Following the introduction, the characterization and physical mechanisms of the NBTI degradation in a small-area high-k/metal-gate pMOSFET

are described in Chapter 2. A statistical model for an NBTI induced ΔV_t distribution by employing the RD model and convolving extracted activation energy including a local electric field effect and a single trapped hole induced V_t shift is developed. NBTI trapped charge characteristics and recovery mechanisms are proposed in Chapter 3 by a statistical study of individual trapped charge emissions in small-area HfSiON/metal-gate pMOSFETs. We develop a statistical NBTI recovery ΔV_t model based on the ThAT and an extracted activation energy distribution. In Chapter 4, we compare the RTN and NBT-stress induced ΔV_t amplitude distributions. A 3D atomistic simulation is performed to compare a single-charge induced ΔV_t by RTN and NBTI. In Chapter 5, nitride program charge effect on the amplitude of RTN in flash cells is investigated. We measure and simulate RTN amplitudes in floating gate flash, planar SONOS, and FinFET SONOS cells. In Chapter 6, an RTN amplitude distribution model in nanowire-like structures is developed. A Poisson distribution is proposed and partly verified using measurement in SONOS flash memory cells. Finally, conclusions are drawn in Chapter 7.

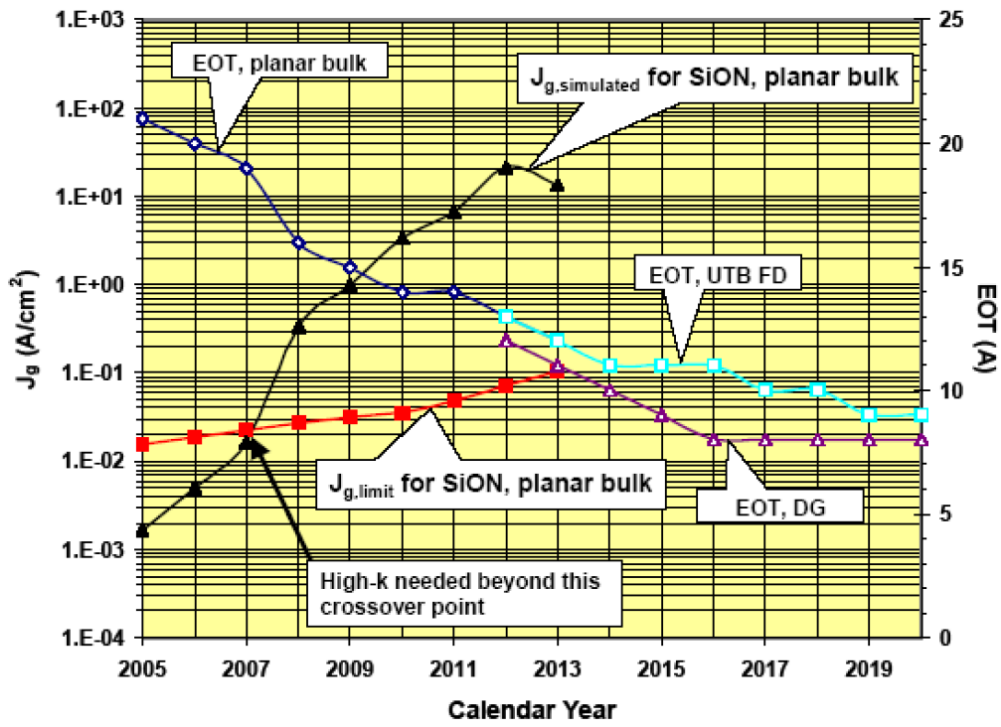
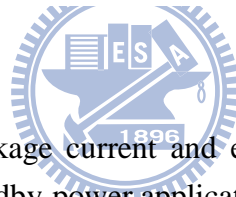
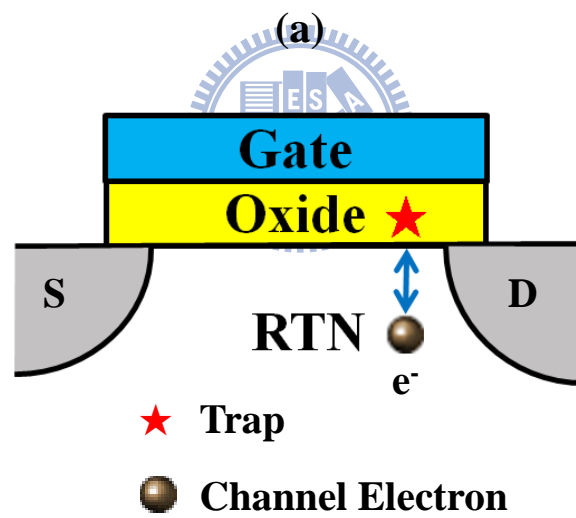
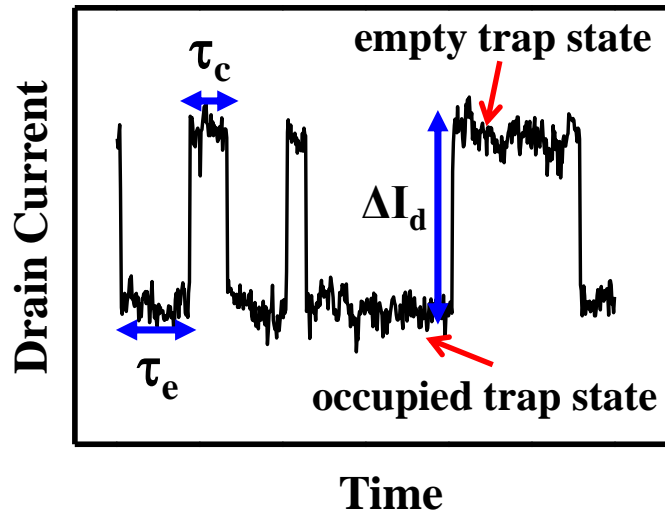


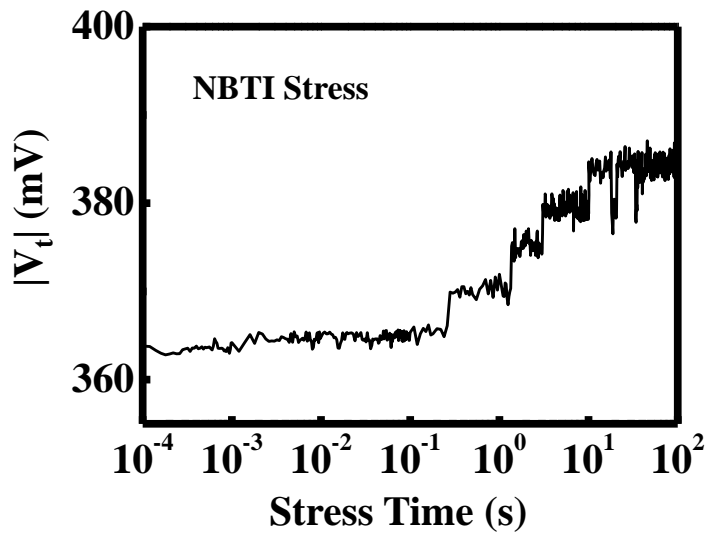
Fig. 1.1 Projections of gate leakage current and equivalent oxide thickness (EOT) from ITRS roadmap for low-standby-power applications.



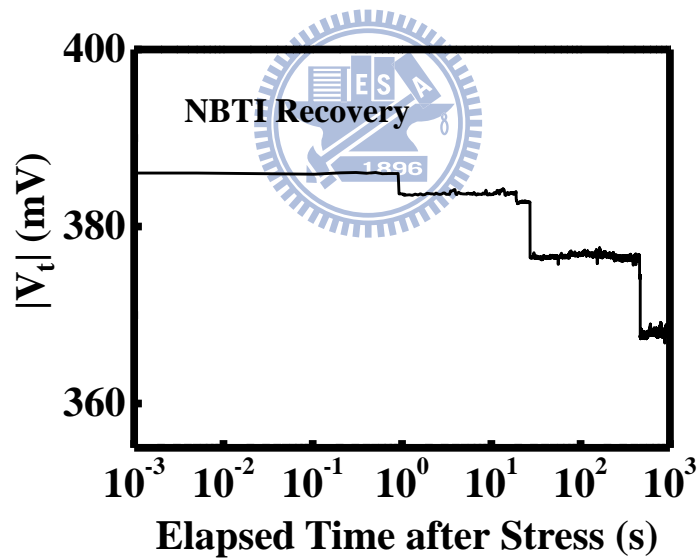


(b)

Fig. 1.2 A typical two-level RTN waveform resulting from electron capture/emission at an oxide trap. τ_c and τ_e are electron capture and emission times, respectively. ΔI_d is RTN amplitude.

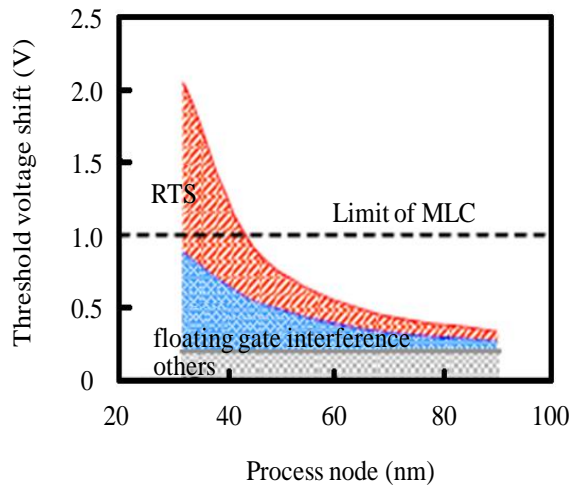


(a)

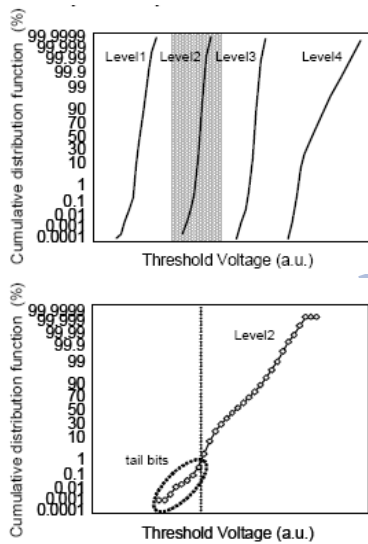


(b)

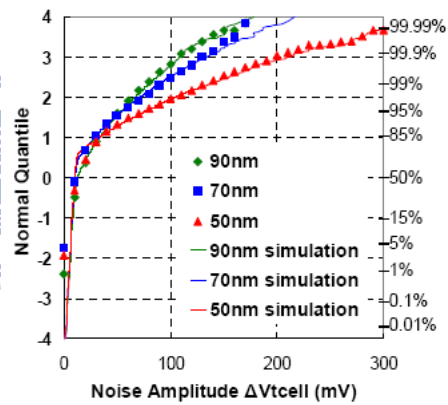
Fig. 1.3 Typical V_t traces during NBTI stress (a) and recovery (b). Each step-like “quantum jump” represents a single charge creation/emission.



(a)



(b)



(c)

Fig. 1.4 (a) Estimation of threshold voltage shift as a function of process node [1.39] (b) measured V_t distribution of a 4-level MLC with level enlarged [1.39] and (c) noise distributions of 90nm, 70nm, and 50nm flash memory technologies [1.40].

Chapter 2

Statistical Characterization of Individual Charge Trapping Times and Modeling of ΔV_t Distribution by NBTI Stress

2.1 Preface

Negative bias temperature instability has been recognized as a major concern in scaled high-permittivity (high-k) gate dielectric pMOSFETs because of its significant impact on performance and reliability in digital and analog circuits [1.43][2.1]-[2.6]. NBTI caused noise margin degradation in a SRAM cell and frequency degradation in a ring oscillator have been reported [2.1]. NBTI severity aggravates as supply voltage reduces in device scaling. In addition to digital circuits, NBTI is of particular importance for analog applications where the ability to match device characteristics to a high precision is critical [2.3]. For instance, in digital-to-analog converters, NBTI can pose a serious reliability issue as a small V_t shift in bias current source can cause large gain errors [2.4].

As device dimensions reduce to a nanometer scale, the number of traps generated by NBTI stress varies significantly from a device to a device due to stochastic process of trap generation and dispersion of activation energy in the RD model. In these nanoscale transistors, NBTI induced ΔV_t scatters widely and it is no longer sufficient to consider just the mean value of ΔV_t in circuit simulation. An accurate model of an entire ΔV_t distribution and its stress time evolution is needed in a worst-case circuit simulation to ensure that the tail of ΔV_t distribution does not cross the reliability criteria during the specified lifetime of an integrated circuit [1.43]-[1.45]. While the mean of an NBTI ΔV_t distribution, or a ΔV_t in a large area device, can be well

described by the RD model [1.14][1.16][1.17][1.28], the RD model alone is insufficient to predict an entire ΔV_t distribution in small area devices.

We first measured an I_d degradation in a large-area device (Fig. 2.1(a)). As compared with our earlier works [1.18], initial trap density is suppressed (from 50% to 20%) due to the improvement of device fabrication technique. Consequently, a RD model rather than a charge trapping model is more adaptable to our present measurement results.

A V_t shift in an NBTI stressed device can be expressed as the sum of each individual trapped charge induced Δv_t , i.e., $\Delta V_t = \sum_{i=1}^N \Delta v_{t,i}$, where N is a total number of stress created traps in a device and Δv_t denotes a single trapped charge caused V_t shift. Two factors affect a ΔV_t distribution. One is the dispersion of Δv_t and the other is fluctuations in number of traps N in stressed devices. The origin and the magnitude distribution of Δv_t have been investigated thoroughly [2.7][2.8]. Previous characterization and 3D atomistic simulation show that a Δv_t exhibits an exponential distribution approximately, i.e., $f(|\Delta v_t|) = \exp(-|\Delta v_t|/\sigma_s)/\sigma_s$, due to a random substrate dopant induced current-path percolation effect [2.7][2.9]. To derive a ΔV_t distribution, we still need a distribution model for a trap number N . In literature, a Poisson distributed N was usually assumed [2.7][2.8][2.10]. The Poisson model is, however, based on a notion that individual trapped charge creations during NBTI stress are independent. In other words, each new trap creation in a device has the same probability regardless of how many traps have been created. Nevertheless, the RD model and measurement result show that NBTI degradation obeys a power-law dependence on stress time, i.e., $t^{1/n}$ with $n \sim 6$ [1.28][2.11], implying that a new trap creation rate decreases with an increasing trapped charge number. Therefore, the use of a Poisson model is contradictory to the RD model and measurement result and may

exaggerate N and a ΔV_t distribution tail significantly. To resolve this discrepancy, Alam et al simulated a trap number distribution by using a Markov Chain Monte Carlo method [2.12] to consider stochastic process of trap generation within a RD framework. However, they did not consider the dispersion of activation energy in the RD model. As a result, their simulated trap characteristic time distribution is much narrower than measurement result in [2.13].

In this work, we characterize NBTI trap creation and V_t shifts in small area devices. Unlike a large-area device, NBTI induced V_t degradation proceeds in discrete steps in small area devices [2.9][2.13]. Due to the discrete nature of a V_t evolution, we are able to measure individual trapped charge creation times and each trapped charge induced V_t shift. An effective activation energy distribution including a local electric field in the RD model will be extracted from measured trapped charge creation times. A Monte Carlo model employing the RD model and an extracted activation energy distribution will be developed to simulate an NBTI ΔV_t distribution and its stress time evolutions.

2.2 Characterization of Individual NBTI Trapped Charge Creation

2.2.1 Devices and Measurement Setup

The devices have a drawn gate length of 30nm, a gate width of 80nm and a high-k (HfSiON) gate dielectric with an equivalent oxide thickness of ~1nm. Similarly to [1.19], the characterization is performed in a stress-measurement-stress (SMS) sequence. In NBTI stress phase, $V_{gs}=-1.8V$ and $V_d=0V$ at room temperature. In measurement phase, the drain voltage is $-0.05V$ and the gate voltage is adjusted to have a drain current of about 500nA in a fresh device. Drain current variations are traced with a switch delay time less than $1\mu s$ using Agilent B1500.

2.2.2 Single Charge Creation Induced ΔV_t Distribution

A corresponding ΔV_t trace is obtained from a measured ΔI_d divided by a transconductance. An example V_t trace is shown in Fig. 2.2. To check on interface trap creation, we monitor transconductance (g_m) and subthreshold swing (SS) degradations during the stress. The subthreshold I_d - V_g characteristics before and after an NBTI stress are shown in the inset of Fig. 2.2. An almost parallel shift after stress is observed, thus indicating that V_t degradation is mainly caused by fixed trapped charge creation rather than interface trap creation. Both SS and g_m degradations are less than 5% in the stress period. For simplicity, a constant transconductance is used when converting ΔI_d into a V_t trace in Fig. 2.2. Each abrupt V_t change ($\Delta V_{t,i}$) in Fig. 2.2 is due to a single trapped hole creation, where i denotes a trapped charge creation sequence number.

We collect all $\Delta V_{t,i}$ in about 130 devices. The magnitude distribution of ΔV_t is plotted in Fig. 2.3. The solid line in Fig. 2.3 represents an exponential fit with a slope (σ_s) of 3.3mV.

2.2.3 Characteristic Times for Trapped Charge Creation

In addition to ΔV_t , individual trapped charge creation times are clearly defined in Fig. 2.2. We collect the first three trapped hole creation times, i.e., τ_i , $i=1,2,3$, in about 130 devices. The probability density functions (PDFs) of $\log(\tau_i)$ are shown in Fig. 2.4. It should be remarked that about 3% devices have less than 3 traps created in a stress period of 100sec. Table 2.1 shows the mean ($\langle \log(\tau_i) \rangle$) and the standard deviation (σ_i) of the three $\log(\tau_i)$ distributions. For comparison, the $\langle \log(\tau_i) \rangle$ and σ_i in NBTI recovery from [2.14] are also shown in the Table 2.1. Distinctly different features

between stress mode and recovery mode are noticed. We find that $\langle \log(\tau_i) \rangle \sim \langle \log(\tau_1) \rangle \sim n \log(i)$ and the standard deviations $\sigma_1 > \sigma_2 > \sigma_3$ in NBTI stress while $\langle \log(\tau_{i+1}) \rangle \sim \langle \log(\tau_i) \rangle \sim \text{constant}$ and the standard deviations $\sigma_1 < \sigma_2 < \sigma_3$ in NBTI recovery. The detail explanations for the features in NBTI recovery has been given in Chapter 3. In this Chapter, we are focused on the characteristics of stress.

The measured τ_i spreads over several decades of time. There are two possible reasons for the wide spread. One is the stochastic process of trap generation in the RD model and the other is the dispersion of activation energy including a local electric field effect (effective activation energy (E_{eff}) hereafter). Other parameters in the RD model or other processes are unlikely to cause such wide spread. The stochastic process of trap generation has been investigated in [2.12] by using a Markov chain Monte Carlo method. Their simulated trap creation time distribution is much tighter than our measured result. Consequently, we attribute the wide spread of trap characteristic times mainly to the dispersion of activation energy arising from different local chemistry in the RD model. Furthermore, the fitting parameters vary a lot from Alam's own publications. In other words, the stochastic process is negligible, as compared to the dispersion of activation energy. As a result, in the following, a statistical τ_i distribution model considering only an activation energy distribution will be developed.

According to the RD model, the stress time dependence of the number of NBTI generated traps in a device is shown below [1.28],

$$N_t = A \exp\left(\frac{2\gamma F}{3}\right) \exp\left[\frac{-E_D}{k_B T}\right] t^n, \quad n \sim 6, \quad (2.1)$$

and

$$A \equiv WLD_0^{1/6} \left[\frac{K_{F0}[SiH][h^+]}{pK_{R0}} \right]^{2/3}, \quad (2.2)$$

where W is a gate width, L is a gate length, K_{F0} , K_{R0} and D_0 are the pre-factors of forward and reverse reaction rate constants and diffusivity in a Arrhenius activation energy, respectively [2.11], and p is the local channel hole concentration. The effective activation energy (E_{eff}) in Eq. (2.1) is defined as

$$E_{eff} = E_D - \frac{2}{3} \gamma F k_B T. \quad (2.3)$$

By re-arranging the terms in Eq. (2.1), the relationship between the i -th trapped charge creation time (τ_i) and effective activation energy is shown below

$$\log(\tau_i) = \frac{nE_{eff}}{2.3k_B T} + n \log(i) - n \log(A). \quad (2.4)$$

From the above equation, the relationship of the mean of the $\log(\tau_i)$ is obtained,

$$\langle \log(\tau_i) \rangle - \langle \log(\tau_1) \rangle = n \log(i), \quad (2.5)$$

n is about 5.6 in our measurement in an initial stress stage. Thus, we can therefore obtain $\langle \log(\tau_2) \rangle - \langle \log(\tau_1) \rangle = 5.6 \log(2) = 1.69$ and $\langle \log(\tau_3) \rangle - \langle \log(\tau_1) \rangle = 5.6 \log(3) = 2.67$ without regard to activation energy. The calculated result from Eq. (2.5) is in reasonable agreement with the measurement result in Table 2.1.

2.2.4 Activation Energy Distribution

In the following, we will extract an activation energy distribution from measured trap characteristic times. By re-arranging the terms in Eq. (2.4), effective activation energy can be readily obtained as follows,

$$E_{eff} = \frac{2.3k_B T}{n} [\log(\tau_i) - n \log(i) + n \log(A)]. \quad (2.6)$$

We can translate the measured $\log(\tau_i)$ distribution into a relative activation energy distribution by subtracting a term $n \log(i)$ from it. Extracted E_{eff} distributions from τ_1 , τ_2 and τ_3 , respectively, are shown in Fig. 2.5. Generally, the E_{eff} distributions from the τ_1 , τ_2 and τ_3 have a reasonable match. Note that the E_{eff} from the τ_1 is slightly broader than the other two distributions, as pointed out in Table I. The pre-factor A in Eq. (2.6) is chosen such that an average value of E_{eff} is about 0.12eV [2.15]. The solid line in Fig. 2.5 represents a Gaussian distribution fit to the E_{eff} of τ_1 with a mean of 0.12eV and a standard deviation of 0.015eV.

2.3 Modeling of an NBTI Induced ΔV_t Distribution

2.3.1 Measured NBTI Induced ΔV_t Distribution

We measure NBTI induced ΔV_t distributions at different stress times. We record the number of generated traps and a total V_t shift in each device. Fig. 2.6 shows the measurement result at a stress time of 0.5sec and 5sec. The y-axis is ΔV_t and the x-axis is the number of trapped holes. Each data point represents a device. The measurement data points scatter along a straight line, as shown in Fig. 2.6. The slope of the line is about 3.3mV, i.e., an average single-charge induced V_t shift. A straight line with a slope of 3.3mV is drawn as a reference rather than a real average value. ΔV_t and NBTI trap number distributions spread as stress time increases. We extract

the mean and the variance of the ΔV_t distributions. An average of ΔV_t in 130 devices is plotted in Fig. 2.7. The mean follows a power law dependence on stress time ($t^{1/n}$) in five decades of time with n about 6. The variance of the ΔV_t distribution also increases with stress time, as shown in Fig. 2.8. In our earlier work, we reported a two-stage V_t degradation by BTI stress [1.18]. The first stage is ascribed to the charging of pre-existing high-k dielectric traps and exhibits a $\log(t)$ dependence. The second stage degradation is caused by high-k dielectric trap creation and follows a power law dependence on stress time. In this work, we do not observe the stage of $\log(t)$ degradation in our stress period possibly because of fewer pre-existing traps in the current samples.

2.3.2 Monte Carlo Simulation Flow

A statistical model based on a Monte Carlo (MC) approach is developed to calculate the number of traps (N) and entire ΔV_t distributions. A Monte Carlo flowchart is shown in Fig. 2.9. In our MC simulation, a Poisson-distributed precursor number (M) in each device is assumed with a mean value of 24 in an 80nmx30nm device, which corresponds to a precursor density of 10^{12} cm^{-2} [2.16]. A sequence number (i) is assigned to each precursor in a device. The activation energy of each precursor is chosen according to the measured E_{eff} distribution in Fig. 2.5. A trapped charge creation time is then computed from Eq. (2.4). The simulated $\log(\tau_i)$ distributions are shown in Fig. 2.10. Each distribution has the same shape as the activation energy. Due to a significant overlap of the distributions, some precursors with a larger sequence number are converted to a trapped charge earlier than the ones with a smaller i . Thus, we re-order trapped charge creation sequence number in each device. The τ_i distributions after the re-ordering are shown in Fig. 2.11. The measured

result is also shown in the figure for comparison. Two points should be noted. First, after the re-ordering, the standard deviation of $\log(\tau_i)$ decreases with an increasing i . This feature is consistent with the measurement result in Table 2.1. Second, The shape of the $\log(\tau_i)$ distribution with $i=1$ is least affected by the re-ordering. Consequently, we used the measured result of τ_1 to extract an E_{eff} distribution in Fig. 2.5.

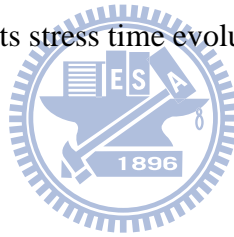
2.3.3 Monte Carlo Simulation Results and Discussion

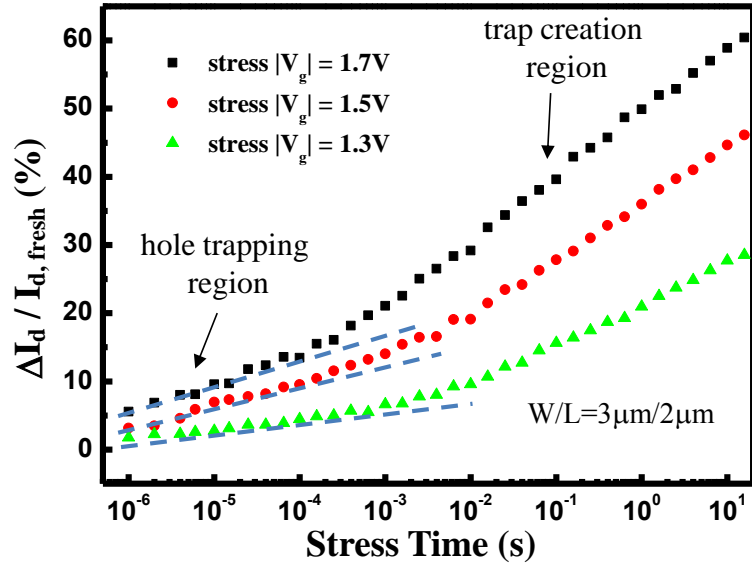
For a stress time t_s , the number of trapped charges N is computed by counting all the precursors with τ_i ($i=1,2,\dots,M$) less than t_s . For each counted trapped charge, a Δv_t is selected based on an exponential distribution, $f(|\Delta v_t|)=\exp(-|\Delta v_t|/\sigma_s/\sigma_s)$, with $\sigma_s=3.3\text{mV}$. A ΔV_t at a stress time t_s can be computed by summing up all the Δv_t , i.e., $\Delta V_t = \sum_{i=1}^N \Delta v_{t,i}$. In total, 5×10^5 devices are simulated. The mean and the variance of the simulated ΔV_t distributions versus stress time are shown in Fig. 2.7 and Fig. 2.8, respectively. Our simulation is in good agreement with measurement results. In addition, we compare measured and simulated ΔV_t distributions at different stress times. Complementary cumulative distribution functions (1-CDF) of NBTI induced ΔV_t at a stress time of $t_s=0.01\text{sec}$, 1sec and 100sec are plotted in Fig. 2.12. The inset of the figure is the probability density function of ΔV_t . Good agreement between our model and measurement is obtained. We also compare our model with the Poisson distributed trap number model [2.7]. To examine the difference in a ΔV_t distribution tail, complementary cumulative distribution functions (1-CDF) of the two models at a stress time of 100sec are plotted in Fig. 2.13 with a logarithmic scale in y-axis. The probability distributions of a trapped charge number from the two models are plotted in the inset. The Poisson model apparently yields a broader distribution in trapped charge number (N) and thus a larger ΔV_t tail. The difference between the two models

increases with stress time as more trapped charges are created.

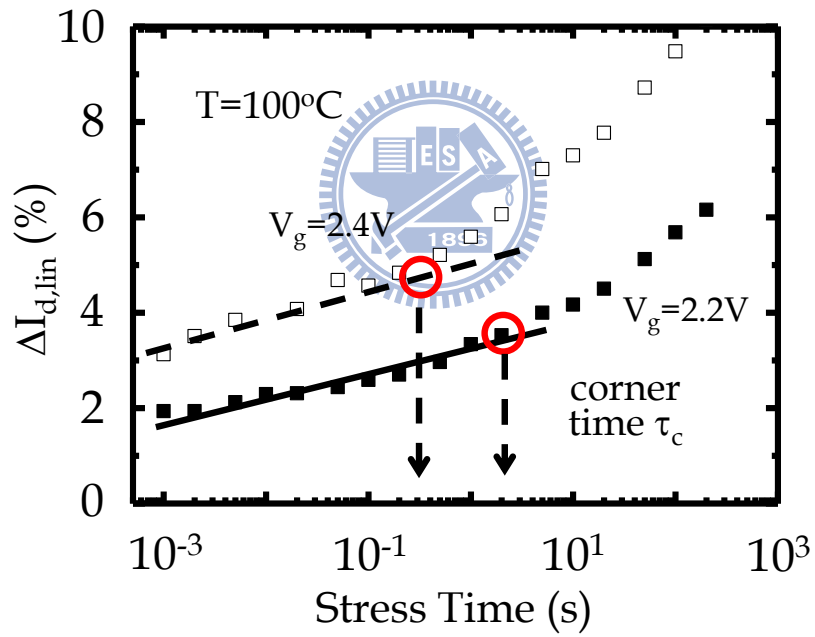
2.4 Summary

We characterize NBTI trap creation in a large number of high-k dielectric pMOSFETs. Origins of an NBTI induced ΔV_t distribution have been identified. The broad distribution of trap creation times is attributed to an activation energy distribution in the RD model. An activation energy distribution including a local electric field effect has been extracted from measured trap characteristic times. We develop a statistical model to simulate an NBTI induced ΔV_t distribution in small area devices. The correlation between an activation energy distribution and an NBTI ΔV_t distribution has been established. Our model can reproduce the measurement results of an NBTI ΔV_t distribution and its stress time evolutions well.





(a)



(b)

Fig. 2.1 Comparison between I_d degradation traces in (a) nowadays (b) previous devices.

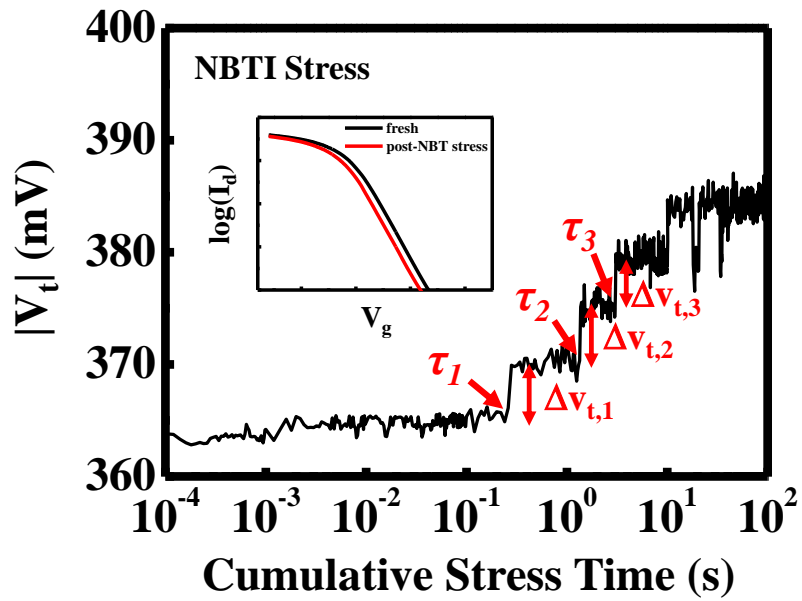


Fig. 2.2 Example V_t trace in NBTI stress in a high-k gate dielectric pMOSFET. τ_1 , τ_2 and τ_3 are the 1st, the 2nd and the 3rd trapped hole creation times. $\Delta V_{t,1}$, $\Delta V_{t,2}$ and $\Delta V_{t,3}$ are the 1st, the 2nd and the 3rd trapped hole induced threshold voltage shifts. The inset shows subthreshold I_d - V_g before and after NBTI stress.

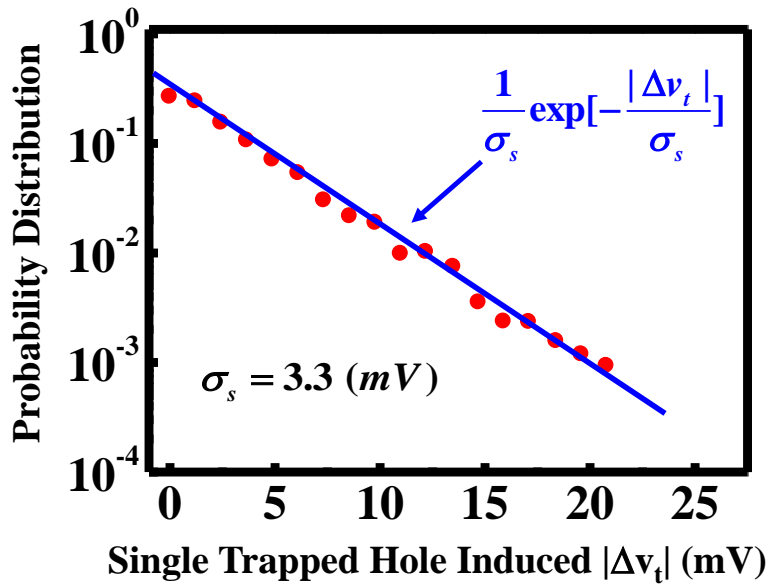


Fig. 2.3 The probability density function of a single trapped charge (hole) induced threshold voltage shift. The solid line represents an exponential fit.

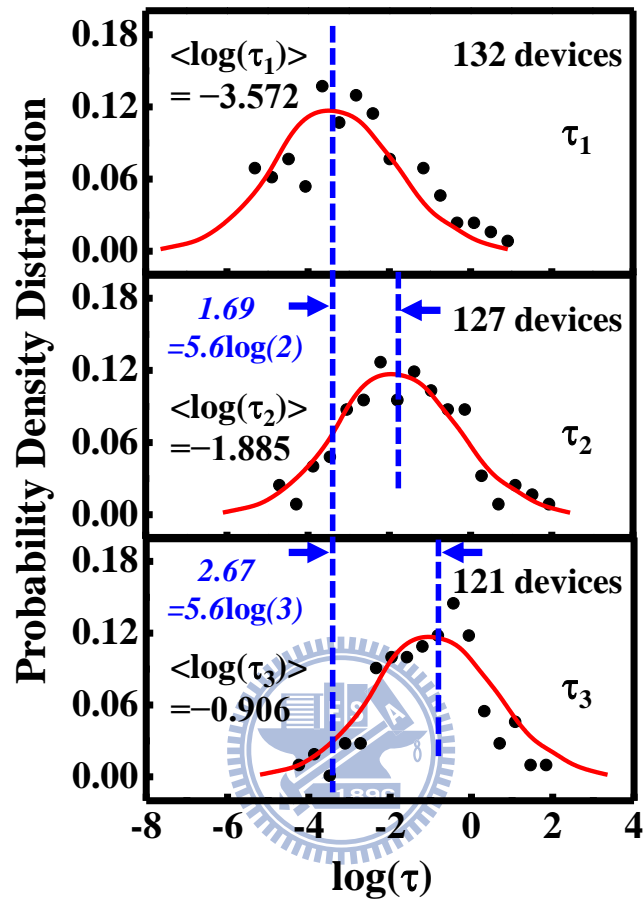


Fig. 2.4 The probability distribution of a trapped hole creation time in NBTI stress collected from about 130 devices. τ_1 , τ_2 and τ_3 are the 1st, the 2nd and the 3rd trapped hole creation times, respectively. The solid line represents a Gaussian fit.

Table 2.1 Comparison of trapped charge creation and emission characteristics in NBTI stress and NBTI recovery. i is a sequence number in trapped charge creation in NBTI stress or trapped charge emission in NBTI recovery.

	NBTI Stress	NBTI Recovery
τ_i	<i>i-th</i> trapped hole creation time	<i>i-th</i> trapped hole emission time
mean of $\log(\tau)$ ($\langle \log(\tau) \rangle$)	$\langle \log(\tau_1) \rangle = -3.572$ $\langle \log(\tau_2) \rangle = -1.885$ $\langle \log(\tau_3) \rangle = -0.906$	$\langle \log(\tau_1) \rangle = -1.009$ $\langle \log(\tau_2) \rangle = 0.036$ $\langle \log(\tau_3) \rangle = 1.074$
standard deviation of $\log(\tau)$ (σ)	$\sigma_1 = 1.436$ $\sigma_2 = 1.379$ $\sigma_3 = 1.282$	$\sigma_1 = 1.070$ $\sigma_2 = 1.181$ $\sigma_3 = 1.285$
distinctive features	$\langle \log(\tau_i) \rangle - \langle \log(\tau_1) \rangle = n \log(i)$ $\sigma_1 > \sigma_2 > \sigma_3$	$\langle \log(\tau_{i+1}) \rangle - \langle \log(\tau_i) \rangle = \text{constant}$ $\sigma_3 > \sigma_2 > \sigma_1$

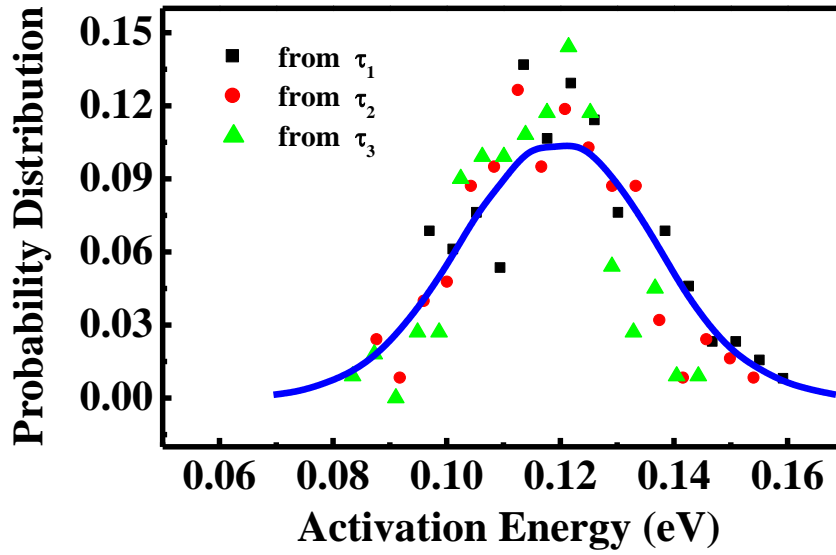


Fig. 2.5 Effective activation energy distributions extracted from measured trap creation times, τ_1 , τ_2 and τ_3 . The solid line represents a Gaussian-distribution fit to the E_{eff} translated from τ_1 .

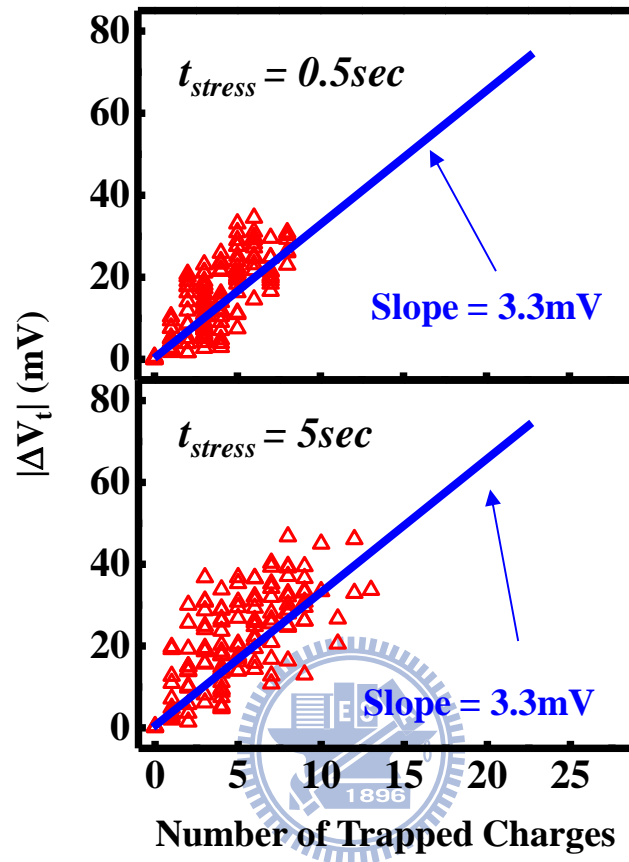


Fig. 2.6 NBTI induced ΔV_t versus number of trapped holes in a device at a stress time of 0.5sec (a) and 5sec (b). Each data point represents a device. The slope of a straight line represents an average Δv_t caused by a single trapped hole.

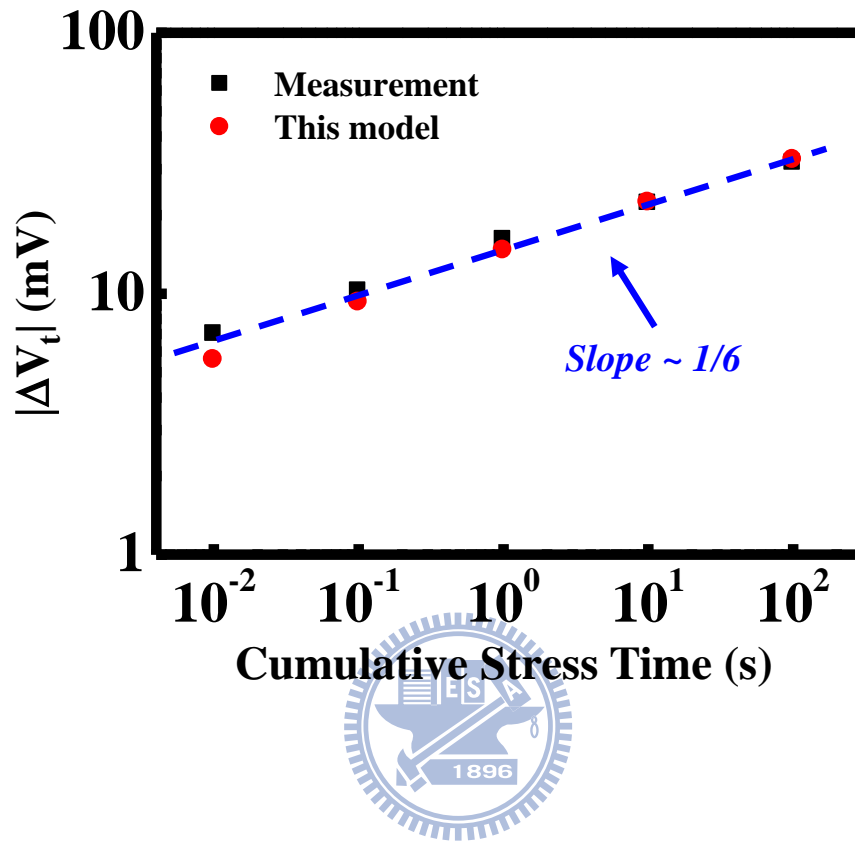


Fig. 2.7 The mean of the ΔV_t distribution versus NBTI stress time from measurement and from our model.

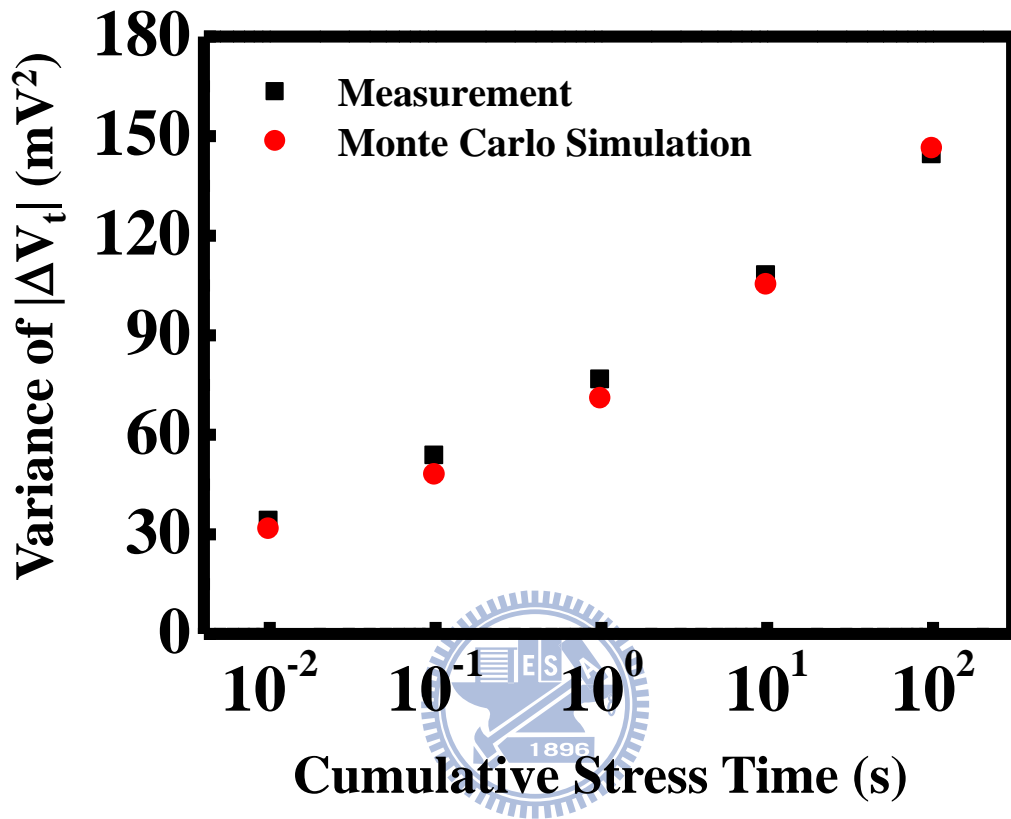


Fig. 2.8 The variance of the ΔV_t distribution versus NBTI stress time from measurement and from our model.

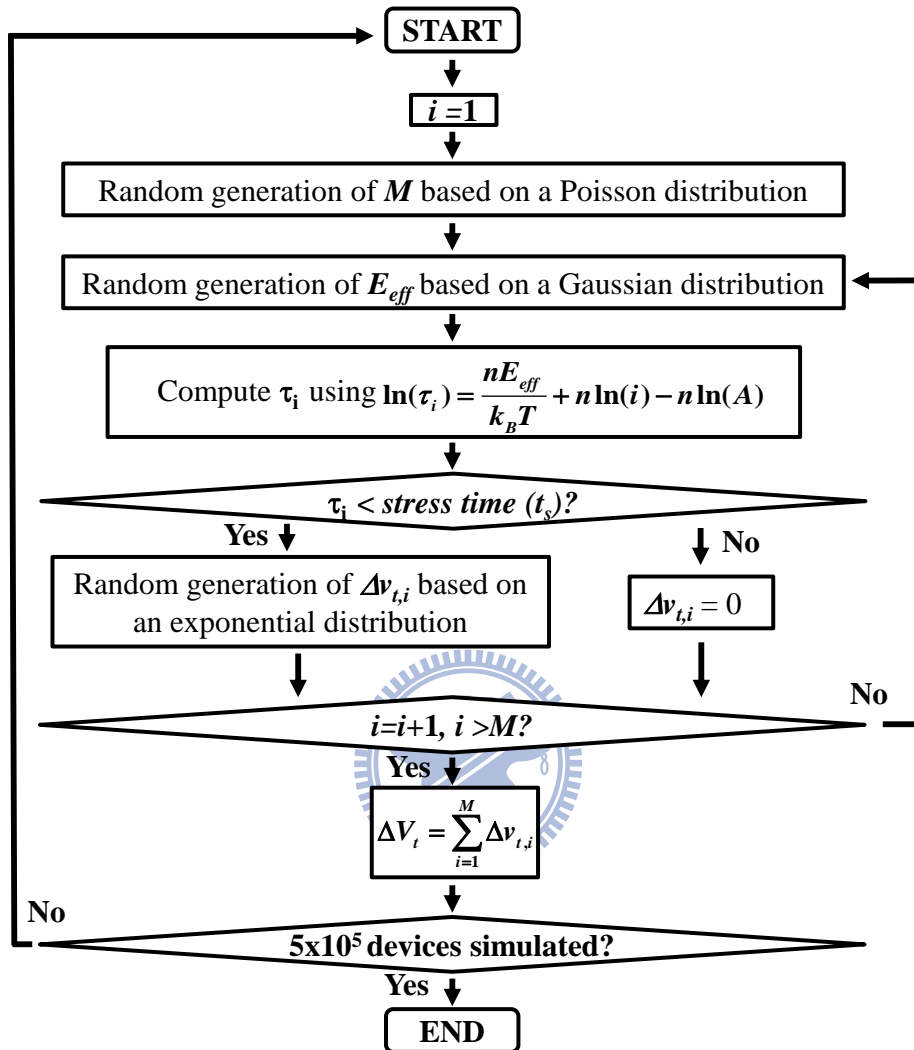


Fig. 2.9 A Monte Carlo simulation flowchart. M is the number of precursors in a device. A precursor density of $1 \times 10^{12} \text{ cm}^{-2}$ is assumed.

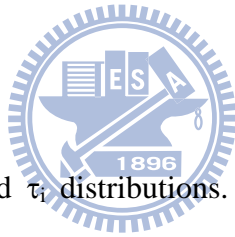
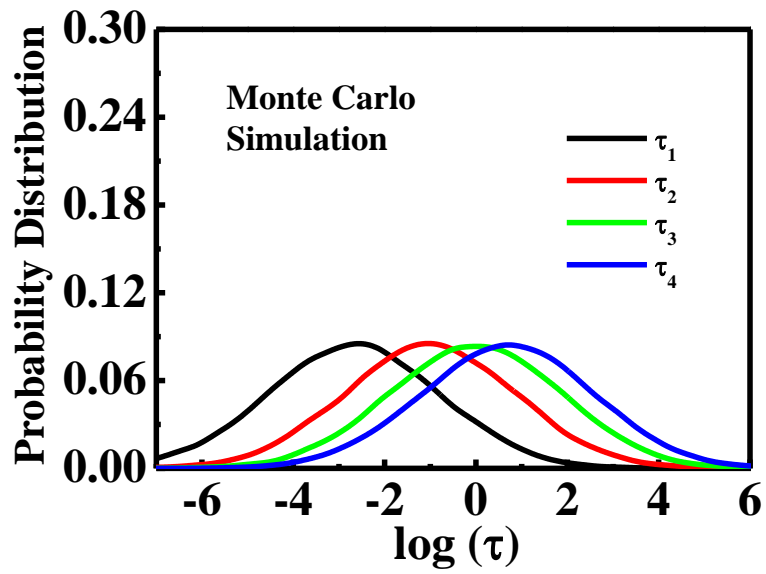


Fig. 2.10 Monte Carlo generated τ_i distributions. Only $i=1$ to 4 are shown in the figure.

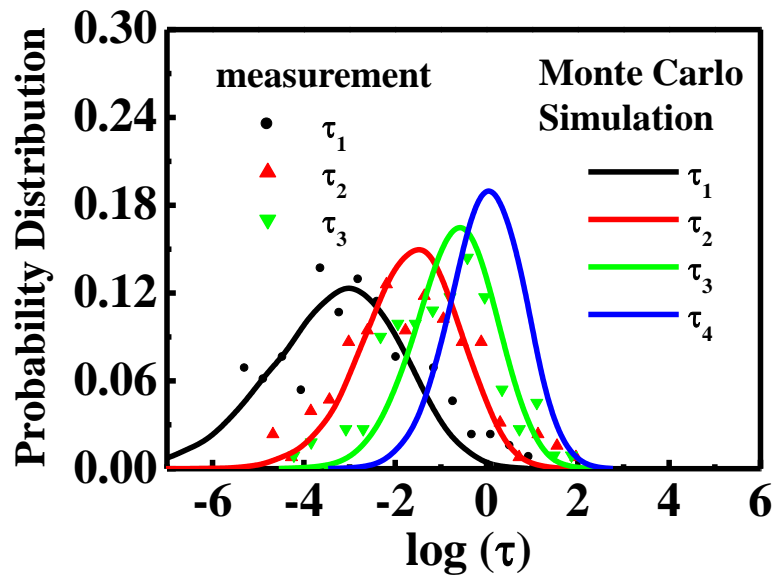


Fig. 2.11 Trapped charge creation time distributions from measurement (symbols) and from Monte Carlo simulation (lines) after the re-ordering. The Monte Carlo simulated $\langle \log(\tau_2) \rangle - \langle \log(\tau_1) \rangle$ is 1.68 and $\langle \log(\tau_3) \rangle - \langle \log(\tau_1) \rangle$ is 2.67.

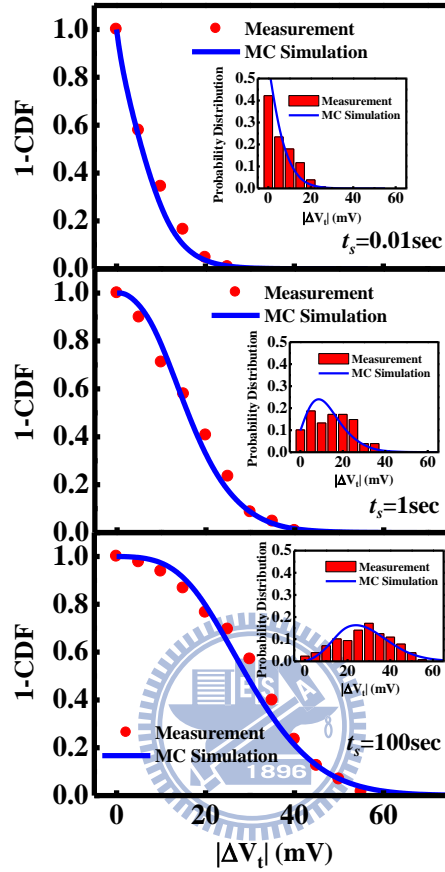


Fig. 2.12 Complementary cumulative distribution functions (1-CDF) of NBTI induced ΔV_t from measurement and from our model. The stress time is 0.01sec, 1sec and 100sec, respectively. The inset shows the probability distributions of ΔV_t from measurement and this model.

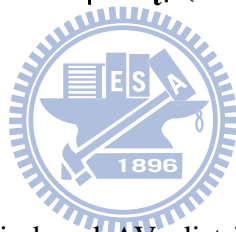
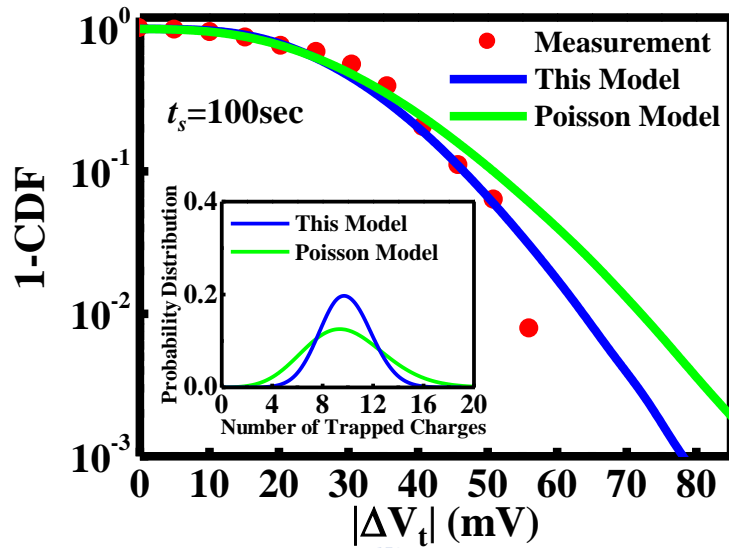


Fig. 2.13 Comparison of NBTI induced ΔV_t distributions (1-CDF) calculated from this model and from the Poisson model. The dots are measurement result. The inset shows trapped charge number distributions from the two models. The stress time is 100 sec.

Chapter 3

Statistical Characterization and Modeling of a ΔV_t

Distribution and Its Temporal Evolutions in NBTI Recovery

3.1 Preface

Unlike most reliability issues, NBTI V_t degradation recovers partly after the removal of stress [1.27]. Several circuit techniques exploiting NBTI recovery have been proposed to alleviate NBTI severity in memory and logic circuits [3.1][3.2]. To improve a design window that is tightened by several variability sources, the integration of NBTI degradation and recovery characteristics into a circuit simulation is called for in modern CMOS technology [3.3]. Hence, underlying degradation and recovery mechanisms of NBTI must be understood in order to make a meaningful projection of a device/circuit lifetime.

While the reaction-diffusion (RD) model [1.14]-[1.17] are commonly adopted for NBTI degradation, no consensus regarding NBTI recovery mechanisms has been reached. Hydrogen back-diffusion in the framework of the RD model was first proposed to explain a NBTI recovery phenomenon [1.17]. A threshold voltage shift relaxation of the form of $\Delta V_t(t) = V_t(0)(1 - \sqrt{t/2t_0} / \sqrt{1+t/t_0})$ is anticipated from the back diffusion theory. Wang et al used a fast transient technique to characterize NBTI recovery and found a $\log(t)$ dependence of ΔV_t on relaxation time in a time span from 10^{-3} s to 10^2 s [1.24]. Moreover, they characterized individual trapped hole emissions in small-area devices and proposed a thermally assisted charge tunnel detrapping (ThAT) model for a recoverable component in relaxation [1.24][3.4]. A $\log(t)$ dependence was

also reported in [1.25] where the authors proposed a dispersive transport model within the RD framework to overcome the apparent deficiency of the RD model in relaxation time dependence. Alam et al ascribed a $\log(t)$ recovery transient to a fast charge detrapping process on top of slower N_{it} re-passivation as encapsulated by the RD model [1.28][1.29]. More recently, Grasser et al used a time dependent defect spectroscopy method to investigate NBTI recovery and concluded that NBTI recovery is due to thermally-assisted discharging of traps and no diffusion process is involved [1.23]. Their conclusions are consistent with [1.24].

In most of earlier works, NBTI behavior was characterized in large-area devices [1.25][3.5] and studies were based on an average and continuous V_t evolution [1.25][1.28][1.29][3.5]. In contrast, NBTI degradation/recovery proceeds in discrete steps in small area devices [1.24][2.7]. Due to the discrete nature of a V_t evolution, we are able to measure individual trapped charge emission times and each single trapped charge induced V_t shift. Statistical characterization of NBTI degradation/recovery in small area devices therefore provides important information to help understand a responsible mechanism as well as trapped charge behaviors such as trapped charge energy and spatial distributions and its activation energy distribution. Moreover, a NBTI model accounting for an entire ΔV_t distribution is required in a worst-case circuit simulation.

In this work, a statistical model based on a ThAT model and an extracted activation energy distribution will be developed for a NBTI recovery ΔV_t distribution and its temporal evolutions.

3.2 Statistical Characterization of NBTI Recovery

3.2.1 Single Charge Emission Induced ΔV_t Distribution

The DUTs are the same as the devices described in Chapter 2. The devices are first stressed at $V_g = -1.8V$ for 100sec at room temperature. The recovery characterization scheme is similar to our previous work [1.19], i.e., in a relaxation-measurement-relaxation sequence. Both NBT stress and post-NBT recovery characterizations are performed at room temperature. In measurement phase, the drain voltage is $-0.05V$ and the gate voltage is chosen such that the pre-stress drain current is about 500nA. Drain current variations are recorded using Agilent B1500. A corresponding ΔV_t trace is obtained from a measured ΔI_d divided by a transconductance [3.6]. Fig. 3.1 shows example ΔI_d and V_t traces in NBTI relaxation. Each abrupt V_t change ($\Delta v_{t,i}$) in the trace is due to a single trapped hole emission, where i denotes a charge detrapping sequence number. We collect all $\Delta v_{t,i}$ in about 170 devices. The magnitude distributions of $\Delta v_{t,1}$, $\Delta v_{t,2}$ and all collected Δv_t are plotted in Fig. 3.2. Emitted trapped charges have almost the same Δv_t distribution regardless of a sequence number, or in other words, emitted charges are independent with respect to Δv_t . The solid line in Fig. 3.2 represents an exponential distribution fit, $f(|\Delta v_t|) = \exp(-|\Delta v_t|/\sigma_r)/\sigma_r$ with a σ_r of 3.3mV. The origins and the distribution of the Δv_t have been studied thoroughly and the exponential distribution is realized due to a random substrate dopant induced current path percolation effect [2.7][2.9].

3.2.2 Trapped Charge Emission Times

Individual trapped charge emission times, for example, τ_1 , τ_2 and τ_3 in Fig. 3.1, are clearly defined. We measure the first three emitted charge characteristic times (τ_i , $i=1,2,3$). The emission characteristic times scatter over several decades of time. The probability density functions (PDFs) of the $\log(\tau_i)$, $i=1,2,3$, are shown in Fig. 3.3. The mean ($\langle \log(\tau_i) \rangle$) and the standard deviation (σ_i) of the distributions are indicated in

the figure. The relationship between the $\langle \log(\tau_i) \rangle$ ($i=1,2,3$) is easily identified. The mean increases by the same amount with a sequence number, i.e., $\langle \log(\tau_{i+1}) \rangle - \langle \log(\tau_i) \rangle \approx 1.04$. On the other side, the standard deviation σ_i increases with i from $\sigma_1=1.070$ to $\sigma_3=1.285$, but its dependence on a sequence number i is more subtle and requires consideration of trapped charge spatial and energetic distributions and its activation energy. We collect all the charge emission times in about 170 devices and plot their occurrence number distribution in a $\log(\tau)$ scale in Fig. 3.4. A rather uniform distribution from 10^{-2} s to 10^3 s in Fig. 3.4 is obtained, thus implying a $\log(t)$ dependence of a recovery ΔV_t in a large area device.

3.2.3 Trapped Charge Spatial and Energy Distributions

According to the ThAT model [3.4], a trapped charge tunnel emission time in a high-k MOSFET can be expressed as

$$\tau_i = \tau_0 \exp\left(\frac{E_a}{kT}\right) \exp(\alpha_{IL} T_{IL}) \exp(\alpha_k x_i) \quad (3.1)$$

and

$$\alpha_{IL} = \frac{2\sqrt{2m_{IL}^* q(E_t + \phi_B)}}{\hbar} \quad (3.1a)$$

$$\alpha_k = \frac{2\sqrt{2m_{HK}^* qE_t}}{\hbar} \quad (3.1b)$$

where the pre-factor τ_0 is a lumped parameter, E_a is activation energy, T_{IL} is an interfacial layer thickness, x_i denotes a trapped charge distance to the HK/IL interface

and E_t is a trapped charge energy. Other variables have their usual definitions in [3.4]. The hole tunneling mass used in this work is $m_{IL}^*=0.41m_0$ [3.7] and $m_{HK}^*=0.18m_0$ [3.8]. According to Eq. (3.1), a tunneling front moves in a speed of $d=2.3/\alpha_k$ per decade of time. A removable trapped charge density (N_t) in relaxation therefore can be extracted from the emission occurrence number versus $\log(\tau)$ in Fig. 3.4 as follows,

$$N_t = \frac{\text{no. of emitted charges/device/decade}}{W \times L \times d} = \frac{\alpha_k \times (\text{no. of emitted charges/device/decade})}{2.3 \times W \times L} \quad (3.2)$$

Since the number of emitted charges exhibits a uniform distribution approximately in each decade of time in Fig. 3.4, we obtain a constant removable trapped charge density N_t in space. With respect to a trapped charge energy distribution, we calculated a voltage drop across an interfacial oxide in NBTI stress by a numerical device simulation [3.9]. The voltage drop is about 0.8V at a stress V_g of $-1.8V$. We therefore assume that removable trapped holes are uniformly distributed in an energy range of 0 to 0.8eV above the Si valence band-edge, corresponding to an E_t value of 2.7eV to 3.5eV with respect to the valence band-edge of the HfSiON. This assumption is also adopted in [3.10] and is supported partly by a charge pumping measurement result [3.11].

Fig. 3.5 illustrates a removable trapped charge distribution and a band diagram in recovery. The calculated value of α_k is from 7.2 to 8.1nm⁻¹. For simplicity, we used an average $\overline{\alpha_k}$ (=7.65nm⁻¹) in Eq. (3.2) and obtain a N_t of 1.3x10¹⁸cm⁻³. An average distance (Δx) between two adjacent trapped charges in the gate-to-substrate direction is about $\Delta x=1/WLN_t \sim 0.32$ nm.

In addition, the ratio of the emission times of two consecutive emitted trapped

charges is

$$\begin{aligned} \langle \log(\tau_{i+1}) \rangle - \langle \log(\tau_i) \rangle &= \frac{1}{2.3} \times [\overline{\alpha}_k \cdot (\langle x_{i+1} \rangle - \langle x_i \rangle)] \\ &\equiv \frac{1}{2.3} \times (\overline{\alpha}_k \cdot \Delta x) \end{aligned} \quad (3.3)$$

Eq. (3.3) shows that the mean of the $\log(\tau_i)$ increases with i by the same amount, i.e., $\alpha_k \Delta x / 2.3 = 1.06$, without regard to activation energy. Eq. (3.3) is consistent with the measurement result in Fig. 3.

3.2.4 Activation Energy Distribution

The wide spread of the trapped charge emission times in NBTI recovery is attributed to an activation energy distribution in the ThAT model due to local chemistry because other variables in the model are unlikely to cause such wide spread. From Eq. (3.1), E_a can be expressed as

$$E_a = kT[2.3 \log(\tau_i) - 2.3 \log(\tau_0) - \alpha_{IL} T_{IL} - \alpha_k x_i] \quad (3.4)$$

Based on a uniform distribution of x_i and E_t and a measured τ_i distribution, we can extract a relative E_a distribution according to Eq. (3.4). A Monte Carlo procedure is employed to extract an E_a distribution. In the Monte Carlo procedure, a removable trapped charge number in each device is selected according to a Poisson distribution [2.7] with an average number of $N_t W L T_{HK}$, where T_{HK} is the thickness of a high-k dielectric. The use of a Poisson distribution here is an approximation and its validity has been discussed in [2.13]. Then, removable trapped charges are randomly placed in the HK layer. A sequence number is assigned to each trapped charge according to its

distance to the HK/IL interface. The nearest trapped charge has a sequence number $i=1$, and the second nearest one has $i=2$ and so on. The E_t of a trapped charge is randomly selected in a range from 2.7eV to 3.5eV, as explained above. The extracted E_a distributions from τ_1 , τ_2 , and τ_3 , respectively, are shown in Fig. 3.6. An excellent match between the two E_a distributions of $i=2$ and $i=3$ is obtained. This excellent match ascertains Eq. (3.4) and the ThAT model. It should be remarked that the distortion of the E_a distribution of $i=1$ is understood because our recovery measurement starts with a time delay of 5ms. Thus, some emitted charges with very short τ (< 5 ms) are not counted. In Fig. 3.6, an appropriate τ_0 is chosen such that the mean of an E_a distribution (~ 0.5 eV) is consistent with published results in literature [2.10]. The solid line in Fig. 3.6 represents a Gaussian distribution fit with a mean of 0.5eV and a standard deviation of 0.08eV. To explain the broadening of the $\log(\tau_i)$ with a sequence number i in Fig. 3.3, we re-arrange the terms in Eq. (3.4) and obtain the following equation:

$$\log(\tau_i) = \frac{1}{2.3} \left[\frac{E_a}{kT} + 2.3 \log(\tau_0) + \alpha_{IL} T_{IL} + \alpha_k x_i \right] \quad (3.5)$$

As i increases, the tunneling distance x_i is larger and the variance of the term $(\alpha_k x_i)$ in the right hand side increases and so does the variance of $\log(\tau_i)$. The broadening of the $\log(\tau_i)$ distribution with a sequence number i in recovery is a salient feature of the ThAT model with the spread of trapped charge energy. This feature is predicted from Eq. (3.5) and verified by the measurement result in Fig. 3.3.

The dependence of a hole emission time on recovery temperature is characterized. The temperature study is somewhat difficult because some of NBTI traps might be annealed at high temperatures. For this reason, we chose a single-NBTI trap device.

We take an average of τ_1 from ten measurements on the same device by repeatedly re-filling a NBTI trap, i.e., a refilling-recovery-refilling sequence. The result in Fig. 3.7 shows a linear relationship between a hole emission time $\langle \log(\tau) \rangle$ and $1/kT$, suggesting a thermally-assisted process and Arrhenius activation energy.

3.2.5 Reproducible Feature of NBTI Recovery

Besides activation energy extraction (temperature dependence), the reproducible feature of NBTI emission allows us to characterize electric field dependence of individual NBTI traps. Fig. 3.8 shows that a longer trap emission time as recovery V_g increases implies a trapped charge emit to channel rather than gate. This V_g -dependent emission feature also ruled out a back-diffusion process due to neutral H species diffusion. Furthermore, we recorded the emission time distribution of an individual NBTI trap. The emission time follows an exponential distribution, as shown in Fig. 3.9.



3.2.6 Comparison with Charge Trapping/De-trapping Model

Aforementioned in preface, a “well-based” charge trapping/de-trapping model proposed by IMEC is also widely accepted as a NBTI recovery model [1.23]. IMEC’s model is derived from standard RTN equations and our model is derived from a standard direct tunneling formula. At the first sight, both approaches look reasonable. But the two models have distinctly different field dependence. IMEC’s model shows very strong oxide field dependence (exponential dependence) and our (ThAT) model does not.

In our opinions, their model equation is only good for RTN or NBTI stress, but not for NBTI recovery for the following reasons.

In IMEC derivation [1.23],

$$\tau_c / \tau_e = \exp((E_F - E_T) / kT) \propto \exp(xF / V_T), \quad (3.6)$$

$$\tau_c = \frac{1}{pv_{th}\sigma_0} \exp\left(\frac{x}{x_0}\right) \exp\left(\frac{\Delta E_B}{kT}\right), \quad (3.7)$$

The Eq. (3.7) is independent of an electric field (F).

Combining Eq. (3.6) and Eq. (3.7), they obtained an exponential dependence of τ_e on an electric field. However, we cannot agree on their Eq. (3.7) in the case of NBTI recovery. A capture time τ_c is originally expressed as $\tau_c = 1/pv_{th}\sigma$ for a trap at Si/SiO₂ interface (activation energy is included in σ). To account for a trap depth x inside an oxide, a tunneling term $\exp(x/x_0)$ is included in the τ_c . (Note that IMEC use the same direct tunneling equation as our model, i.e., no electric field dependence). The modified equation of τ_c is valid for a trap with energy within the Si band-gap (e.g., an RTN trap).

In NBTI recovery, a hole trap with energy above the silicon valence band-edge might have been filled because of a large stress V_g applied before recovery. In our manuscript, we point out that NBTI trapped holes have energy in a range of 0~0.8eV above the Si valence band edge. To deal with those traps in NBTI recovery, the capture time $\tau_c = 1/pv_{th}\sigma \exp(x/x_0)$ is not right because not all of the channel holes have sufficient energy to enter those traps. Therefore, a Boltzmann factor should be included in the τ_c , i.e., $\tau_c = 1/pv_{th}\sigma \exp(x/x_0) \exp(\Delta E/kT)$, where ΔE is an energy difference between a trap level and the valence band-edge, as illustrated in Fig. 3.10. Since ΔE has the same field dependence as Eq. (3.6), it cancels out the term

$\exp(xF/V_T)$ in Eq. (3.6) and leaves τ_e independent of an electric field. The outcome is the same as our model based on direct tunneling. The measurement result (Fig. 6 in our paper [3.4], and Fig. 7 in IMEC's paper [1.23]) also does not support exponential field dependence in NBTI recovery. Moreover, electric field is a secondary effect in our model.

3.3 Modeling of a Recovery ΔV_t Distribution

3.3.1 Measured NBTI Induced ΔV_T Distribution

We measure threshold voltage shifts in a large number of devices at different recovery times. The number of emitted holes and a total threshold voltage shift (ΔV_t) in each device are recorded. Fig. 3.11 shows the measurement results at a recovery time of 0.1sec, 10sec and 1000sec. The y-axis is a total ΔV_t and the x-axis is the number of emitted holes. Each data point represents a device. The measurement results scatter along a straight line. The slope of the line is about 3.3mV, i.e., an average single-charge induced V_t shift. The ΔV_t and the emitted charge number distributions broaden with recovery time in the measurement period. An average of recovery V_t traces in 170 devices is plotted in Fig. 3.12, which reflects an observed recovery characteristic in a large-area device.

3.3.2 Monte Carlo Simulation Flow

A Monte Carlo ΔV_t distribution model based on the ThAT and the extracted trapped charge spatial, energetic and activation energy distributions is developed. The simulation flowchart is shown in Fig. 3.13. The Monte Carlo simulation can reproduce the τ_1 , τ_2 , and τ_3 distributions well, as shown by the solid lines in Fig. 3.3. The broadening of the $\log(\tau_i)$ with i can be well described by our MC simulation.

Moreover, we can use the procedure to generate τ_i distributions for $i > 3$. For a recovery time t_r , the number of emitted charges (N) is computed by counting all the charges with τ_i less than t_r . For each emitted charge, a Δv_t is randomly selected based on the distribution $f(|\Delta v_t|) = \exp(-|\Delta v_t|/\sigma_r)/\sigma_r$ with $\sigma_r = 3.3\text{mV}$. A total ΔV_t is then calculated as $\Delta V_t = \sum_{i=1}^M \Delta v_{t,i}$. In total, 5×10^5 devices are simulated in the MC simulation.

3.3.3 Monte Carlo Simulation Results and Discussion

The simulated and measured ΔV_t distributions are shown in Fig. 3.14 at a recovery time of $t_r = 0.1\text{s}$, 10s and 1000s . Our model is in good agreement with measurement. The mean and the variance of the ΔV_t distributions versus recovery time are shown in Fig. 3.12 and Fig. 3.15 for comparison. Our model can reproduce the $\log(t)$ dependence in a large-area device as well as an overall ΔV_t distribution and its temporal evolution in small-area devices. In short, the $\log(t)$ behavior is a result of a uniform spatial distribution of trapped charges while the E_a and E_t distributions affect a ΔV_t distribution and its temporal evolution in small-area devices.

3.4 Summary

We use a statistical approach to exploring NBTI recovery mechanisms and trapped charge characteristics. Thermally-assisted trapped charge tunnel emission has been confirmed to be a major mechanism in NBTI recovery. We extract a trapped charge activation energy distribution in the ThAT model for the first time. We find that the emission time distribution of trapped charges broadens as a sequence number increases. This feature is successfully explained by the ThAT model and verified by measurement. A Monte Carlo based statistical model for a post-NBTI ΔV_t distribution

is developed for small area devices. Our model can predict a ΔV_t distribution and its temporal evolution in relaxation very well.



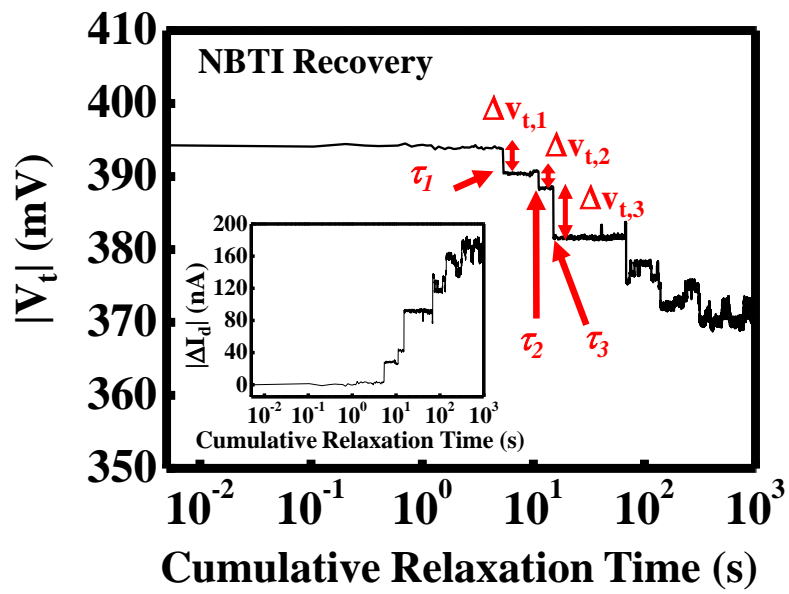


Fig. 3.1 Example ΔI_d and V_t traces in NBTI relaxation. τ_1 , τ_2 and τ_3 are the 1st, the 2nd and the 3rd trapped hole emission times, respectively. $\Delta v_{t,i}$ ($i=1,2,3$) represents a single emitted charge induced threshold voltage shift.

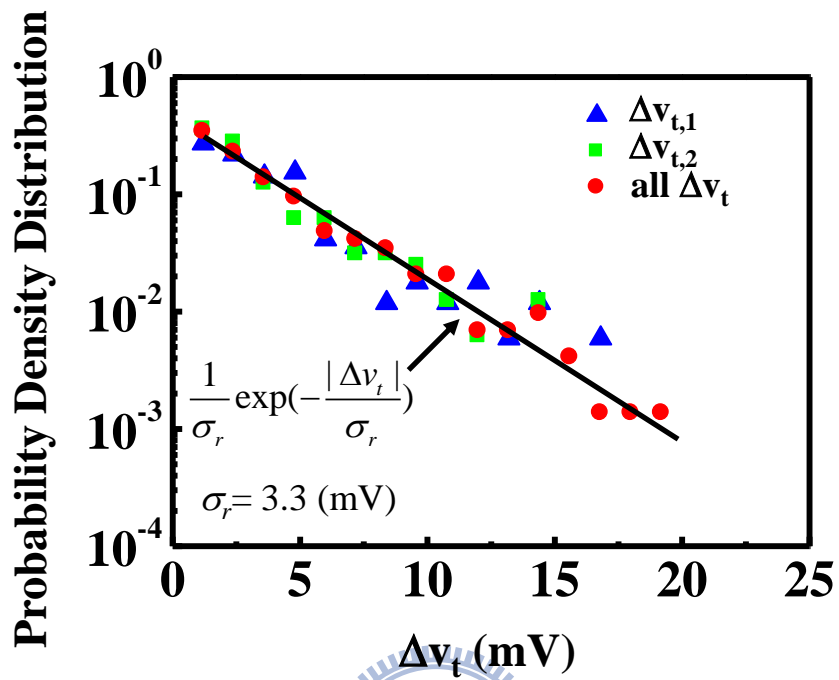


Fig. 3.2 The magnitude distributions of $\Delta v_{t,1}$, $\Delta v_{t,2}$ and all collected $\Delta v_{t,i}$ from NBTI recovery traces in 170 high-k/metal gate pMOSFETs. The solid line represents an exponential fit.

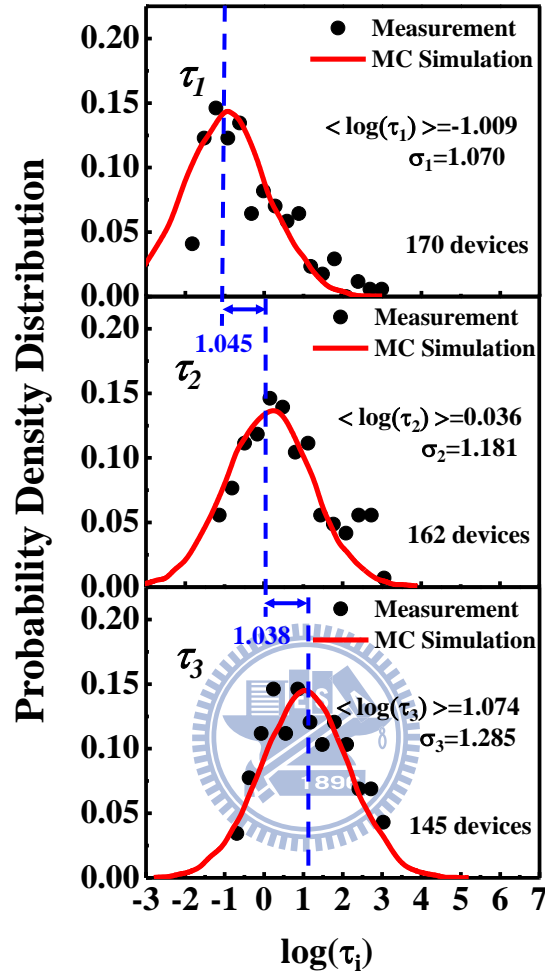


Fig. 3.3 The probability density distributions of a trapped charge (hole) emission time in a $\log(\tau)$ scale. τ_1 , τ_2 and τ_3 are the 1st, the 2nd and the 3rd trapped hole emission times, respectively. The mean ($\langle \log(\tau_i) \rangle$) and the standard deviation (σ_i) of the distributions are indicated in the figure. The symbols are measurement result and the solid lines are from Monte Carlo simulation. A Monte Carlo simulation procedure is given in Fig. 3.10.

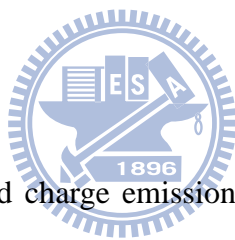
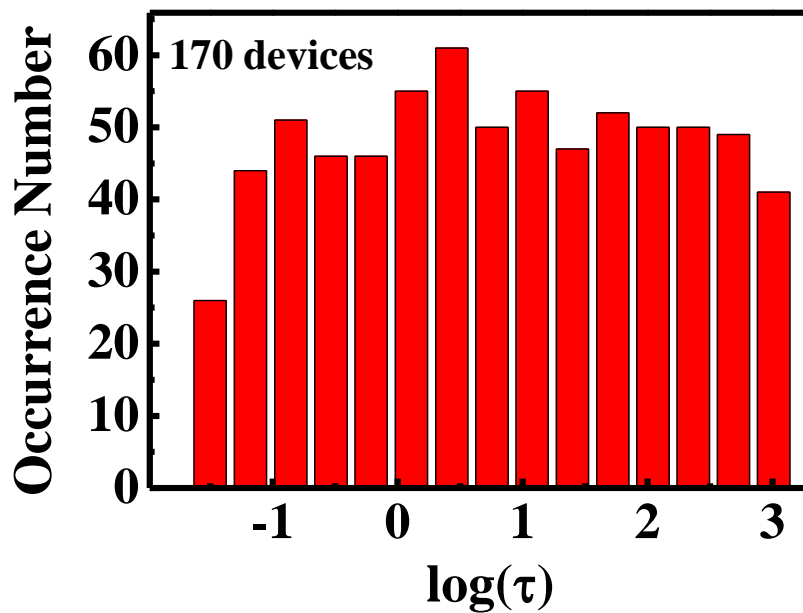


Fig. 3.4 Histogram of all trapped charge emission times in a $\log(\tau)$ scale collected from 170 devices. The occurrence number distribution is rather uniform in a period from 10^{-2} s to 10^3 s.

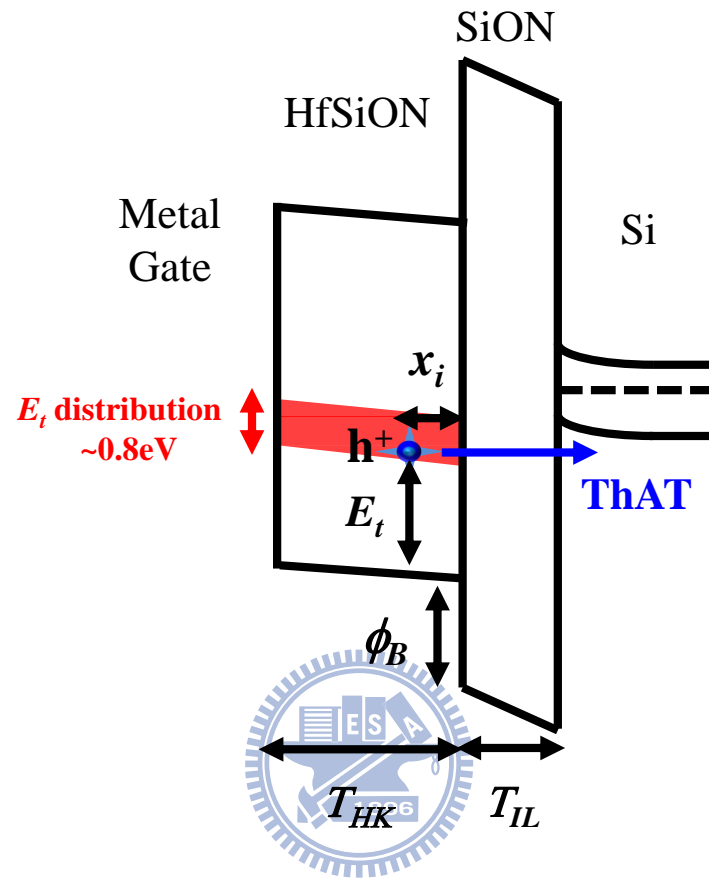


Fig. 3.5 Schematic representation of a band diagram of a high-k/metal gate pMOSFET in relaxation. x_i and E_t represent a trapped charge position and energy.

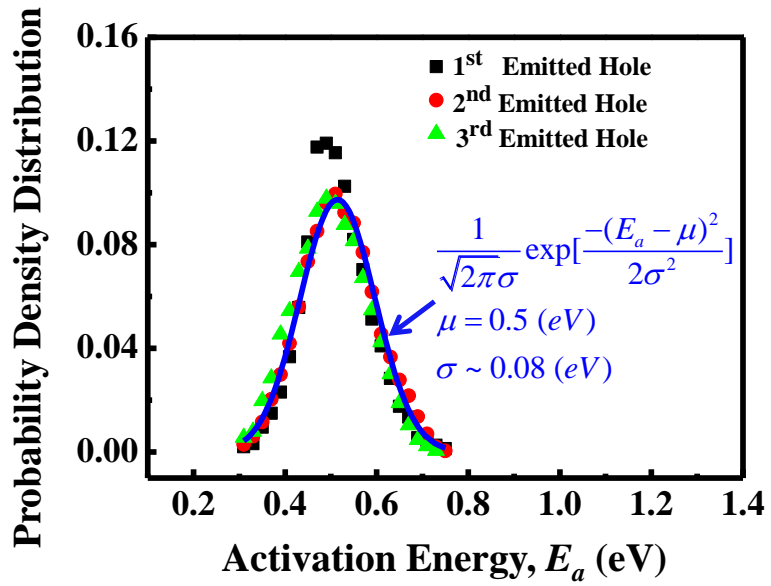


Fig. 3.6 Activation energy (E_a) distributions extracted from the τ_1 , τ_2 and τ_3 , respectively. τ_0 in Eq. (3.4) is chosen such that the mean of the E_a is about 0.5eV. The solid line is a Gaussian-distribution fit.

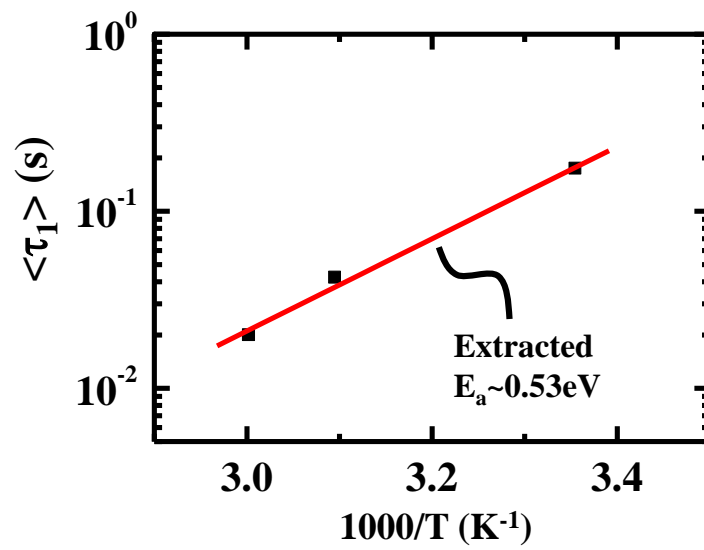


Fig. 3.7 The dependence of $\langle \tau_1 \rangle$ on recovery temperature. The extracted activation energy is about 0.5eV. Each data point is an average of ten readings.

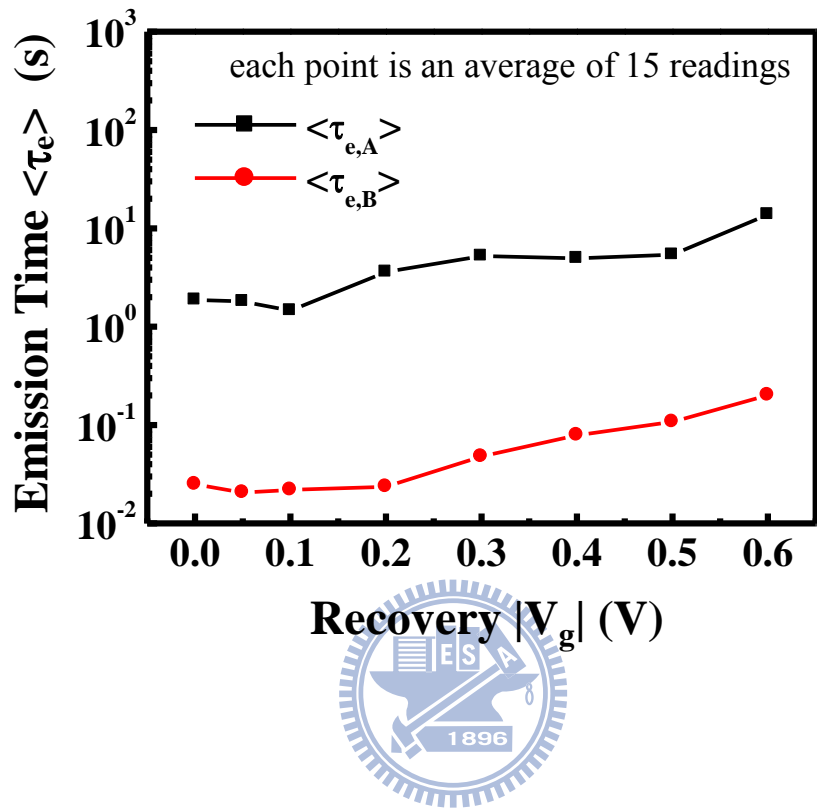


Fig. 3.8 Dependence of trapped electron emission times on recovery gate voltage. 15 measurements are made for each recovery V_g to take average.

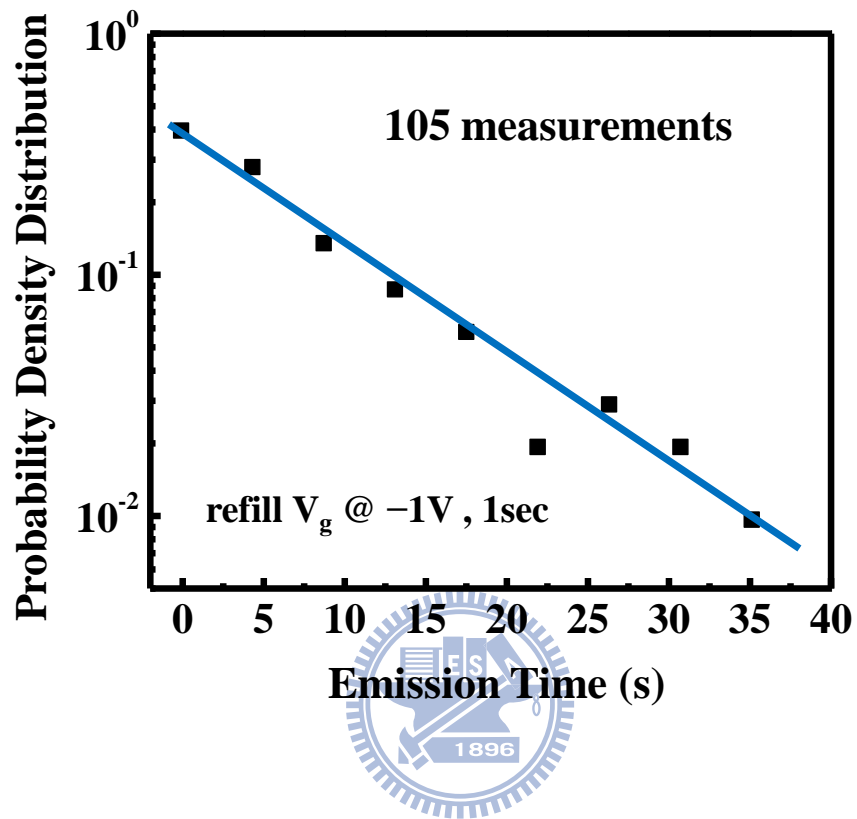


Fig. 3.9 A PDF plot of an emission time measured from an individual trap.

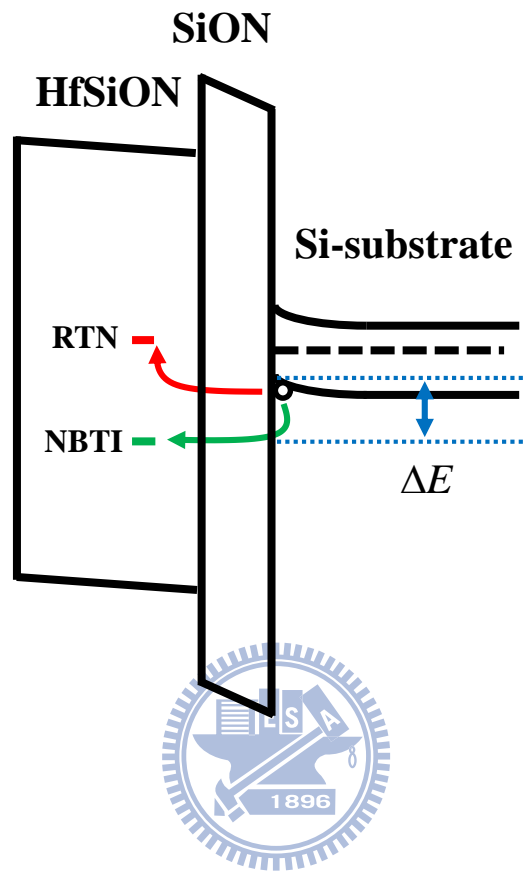


Fig. 3.10 An illustration of difference of trap energy between NBTI and RTN defects.

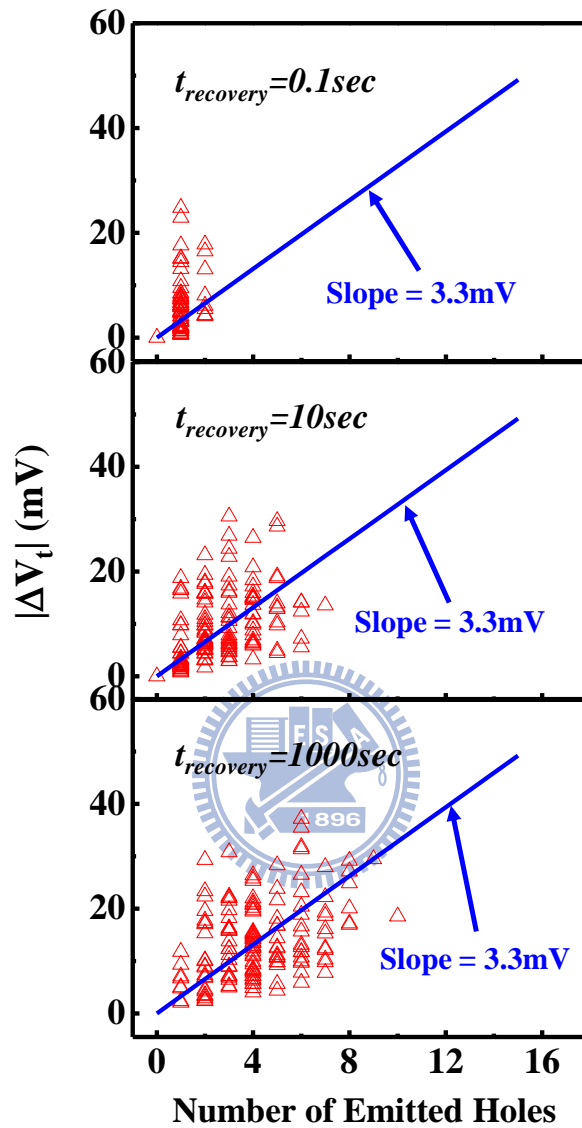


Fig. 3.11 A total V_t shift (ΔV_t) versus number of emitted trapped holes in a device at a recovery time of 0.1s, 10s and 1000s. Each data point represents a device. The slope of a straight line represents an average Δv_t caused by a single trapped hole emission.

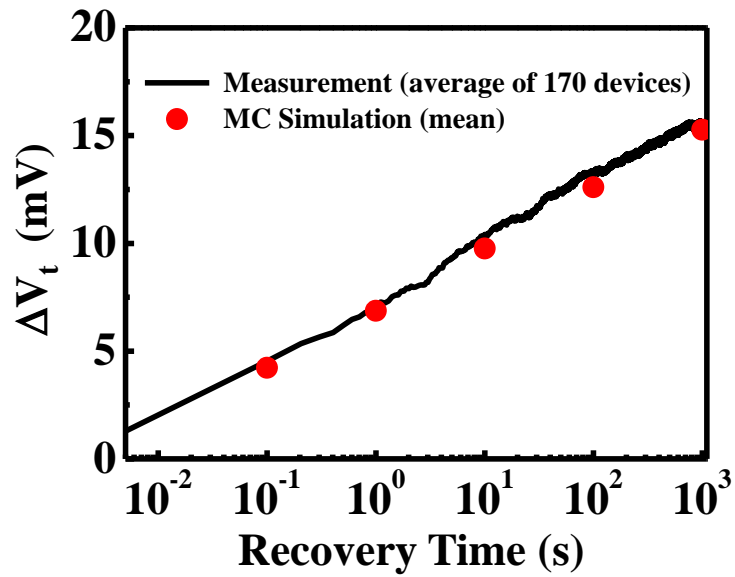


Fig. 3.12 The evolution of ΔV_t with a recovery time. The solid line represents an average of measured ΔV_t traces in 170 devices. The symbols are the mean of Monte Carlo simulated ΔV_t distributions. A logarithmic time dependence of ΔV_t is obtained.

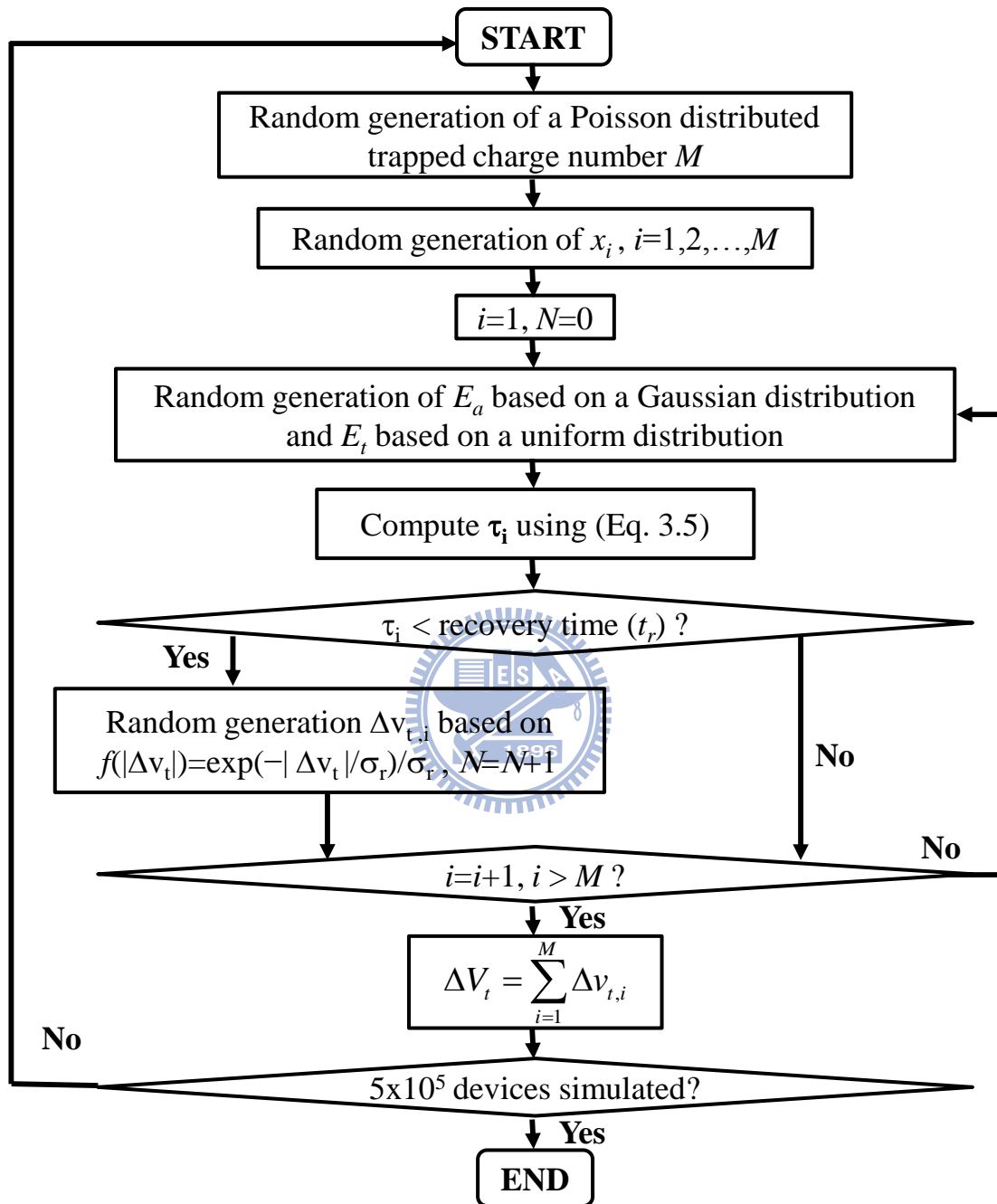


Fig. 3.13 Simulation flowchart of a Monte Carlo based ΔV_t distribution model for NBTI recovery in small area devices.

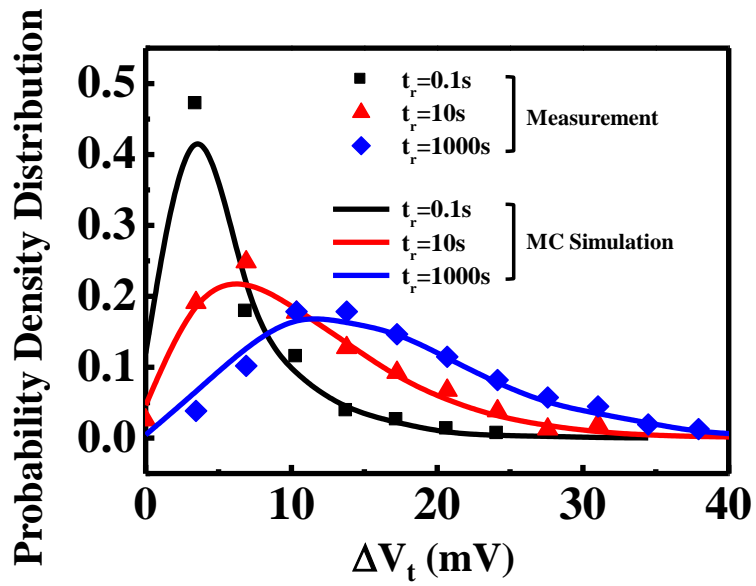


Fig. 3.14 The probability density distributions of NBTI recovery ΔV_t in 80nm x 30nm pMOSFETs from measurement and from a Monte Carlo simulation. The recovery time is 0.1s, 10s, and 1000s.

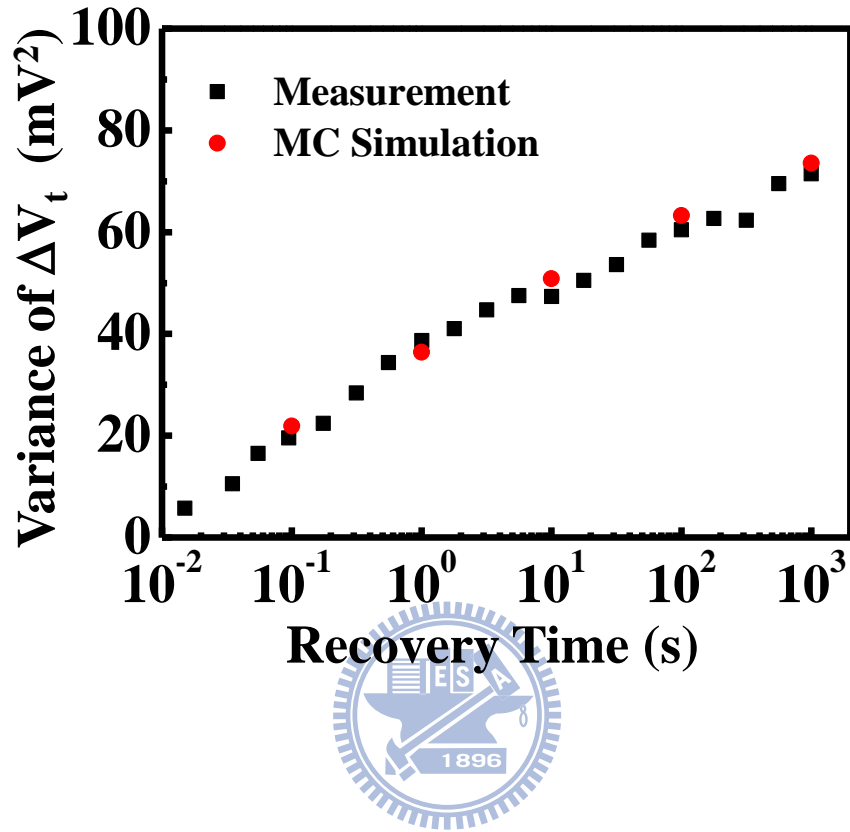


Fig. 3.15 The variance of a recovery ΔV_t distribution versus a recovery time in 80nmx30nm pMOSFETs from measurement and from a Monte Carlo simulation.

Chapter 4

A Comparative Study of NBTI and RTN Amplitude Distributions in High-k Gate Dielectric pMOSFETs

4.1 Preface

In addition to NBTI, RTN is also recognized as a major reliability issue in CMOS scaling [1.36][1.38][1.39]. Single charge trapping/detrapping induced threshold voltage fluctuations in RTN and NBTI have been widely explored [1.19][2.7]. Similar phenomenology has been found in both of them. For example, discrete charge trapping/detrapping is observed in RTN and NBTI traces, as illustrated in Fig. 4.1. The abrupt changes of a threshold voltage (Δv_t) in Fig. 4.1 are realized due to a single charge trapping/detrapping in a gate dielectric. Previous studies have shown that the magnitude of the Δv_t varies from a device to a device in RTN measurement and from a trapped charge to a trapped charge during NBTI stress [2.7]. The Δv_t magnitude distribution can be approximated by an exponential function, i.e., $f(|\Delta v_t|) = \exp(-|\Delta v_t|/\sigma)/\sigma$, either for RTN [1.40] or for NBTI [2.7]. A 3D atomistic Monte Carlo simulation [4.1][4.2] has shown that the Δv_t distribution tail is attributed to a current-path percolation effect arising from random dopants in substrate. Since RTN traps in un-stressed devices and NBTI stress created charges may have a different spatial distribution in the channel, their current-path percolation effects and thus the Δv_t distribution may be different and require a further study.

In this work, we characterize RTN and NBTI in high-k gate dielectric and metal gate pMOSFETs. The devices have a drawn gate length of 30nm and a gate width of 80nm. A 3D Monte Carlo simulation is performed to calculate RTN and NBTI caused

Δv_t distributions due to a percolation effect. In NBTI simulation, the RD model [4.3] is employed to calculate a trap creation probability distribution in the channel.

4.2 Measurement Results and Discussion

4.2.1 Devices and Measurement Setup

In RTN measurement, the drain voltage is -0.05V and the gate voltage is adjusted to have a target drain current of -500nA . A typical RTN waveform is shown in Fig. 4.1(a). The threshold voltage fluctuations are obtained from a measured drain current divided by a transconductance. Two-level switching due to a single charge trapping/detrapping is observed. In NBTI characterization, the stress condition is $|V_g - V_t| = 1.5\text{V}$ and $V_d = 0\text{V}$ at room temperature. Threshold voltage variations with stress time are also traced in the same condition as RTN measurement with a switch delay time less than $1\mu\text{s}$ using Agilent B1500. A representative NBTI trace is shown in Fig. 4.1(b). Each sudden v_t jump is due to creation of a single trapped charge.

4.2.2 Distribution of Single Charge Induced v_t shifts

We collect all the single charge induced Δv_t in about 300 samples. The cumulative probability distribution of Δv_t amplitude is shown in Fig. 4.2. In Fig. 4.2(a), we compare RTN and NBTI amplitude distributions. The RTN distribution is measured in fresh devices. The NBTI has a considerably broader amplitude distribution ($\sigma = 3.34\text{mV}$) than RTN ($\sigma = 1.12\text{mV}$), suggesting that NBTI has a larger impact on CMOS reliability than RTN due to a larger Δv_t tail. Moreover, we compare RTN amplitude distributions in pre-NBTI stress devices and in post-NBTI stress devices in Fig. 4.2(b). The post-stress one apparently has a larger Δv_t tail. As a result, we conclude that NBTI stress created traps have a larger single-charge induced Δv_t

distribution tail. The RTN amplitude distribution arises from NBT-stress is indeed larger than fresh RTN amplitude distribution, which ascertains a new trap creation during NBTI.

4.2.3 Trap Position Extraction

To explore the physics that a NBTI stress created charge has a larger Δv_t distribution tail, we performed a 3D atomistic Monte Carlo simulation for both RTN and NBTI. In RTN amplitude simulation, substrate dopants are randomly and discretely placed in a simulated device and an RTN trap is randomly selected in the channel. The random placement of an RTN trap is based on an assumption that RTN traps in fresh devices (for example, process induced traps) have a uniform distribution in the channel. This assumption is actually verified by measurement. In Fig. 4.3(a), we extract an RTN trap lateral position in 124 devices by using a method similar to [4.4][4.5] and the trap position distribution is rather uniform along the channel. In addition, the vertical positions of initial traps are also profiled, as shown in Fig. 4.3(b), which indicates that process-induced traps are mostly located in HK/IL interface and HK bulk dielectric rather than in IL. Furthermore, we intend to correlate RTN amplitudes with their trap positions. However, no specific correlations are found between RTN amplitudes and the trap positions which manifests that current path percolation effect plays a more important role than trap position, as shown in Fig. 4.4.

4.3 Simulation of a NBTI Stress Induced Δv_t

4.3.1 3D atomistic Monte Carlo Simulation Method

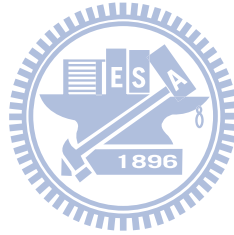
To explore RTN and NBTI induced Δv_t amplitude fluctuations, a Monte Carlo simulation by using ISE TCAD [3.9] is proposed [4.1]. In RTN simulation, trap

positions are randomly and uniformly chosen on the channel surface. In NBTI simulation, to select a trapped charge position, we first calculate a trap creation probability at each grid point in the surface of the channel. According to the RD model and assuming that the reaction phase dominates the process, the NBTI trap generation rate, in the initial stage of stress (i.e., the trap density N_t is small), can be expressed by

$$\frac{dN_t}{dt} = k_F N_0 \quad (4.1)$$

where N_0 is the total number of Si-H bonds. k_F is the Si-H dissociation rate constant, which is formulated as [1.15]

$$k_F \propto p \cdot \exp\left(\frac{F}{E_0}\right) \quad (4.2)$$



where p is a channel surface hole concentration and F is a local electric field. The local hole concentration p and the electric field F are obtained from a 3D device simulation with random substrate dopants. Thus, the relative trap creation probability at each point of the channel can be calculated from the product of p and $\exp(F/E_0)$.

4.3.2 Results and Discussion

Fig. 4.5 shows the calculated trap creation probability versus a local surface hole concentration in NBTI stress. The result shows that the trap creation probability increases with a hole concentration. In other words, a trap tends to be created in a high hole density region (i.e., a critical current path) in NBTI stress. In our NBTI amplitude simulation, we select a trapped hole position according to the calculated

probability distribution rather than a uniform probability distribution for RTN. 200 simulations are performed for each distribution curve in Fig. 4.6. It should be mentioned that the simulated device size is $W/L=30\text{nm}/30\text{nm}$ rather than a measured device size of $W/L=80\text{nm}/30\text{nm}$. The reason is that the simulation time is about 2hrs for a $W/L=30\text{nm}/30\text{nm}$ device, but is about 3 days for a $W/L=80\text{nm}/30\text{nm}$ device. The entire probability distribution consists of more than 200 devices. Thus, the total simulation time becomes prohibitive for a real device size. In addition, it is not our intention to directly fit the simulation to the measurement result because we do not know an exact doping profile in measured devices. Instead, our purpose is to show, by simulation, that the Δv_t distributions from traps created according to the RD model and from traps induced by process, which are believed to have a random distribution in the channel, have different amplitudes and standard deviation. This result is expected to be the same regardless of a device size.

To explain the difference in the shape of the Δv_t distribution in larger devices and in smaller devices (exponential distribution-like versus normal distribution-like), first, we need to know the magnitude of a single charge induced Δv_t is affected by three factors, percolation effect, number fluctuation and mobility fluctuation. Mobility fluctuation is unimportant while the rest of two can be taken into account appropriately in a 3D simulation. We perform device simulations for a uniform and continuous doping profile (w/o percolation) and for a random and discrete doping distribution (w/ percolation) in two different device sizes, $W/L=30\text{nm}/30\text{nm}$ and $W/L=40\text{nm}/40\text{nm}$. The simulation result is shown in the Fig. 4.7. For a $30\text{nm}/30\text{nm}$ device, the flatter part of the distribution is recognized due to number fluctuation from the comparison of the simulation results w/ and w/o a percolation effect. The tail part of the distribution apparently arises from a percolation effect since the uniform doping

does not have such a tail. As device size increases, the flatter part becomes narrower due to a smaller number fluctuation effect and thus the distribution is more like an exponential distribution. A similar trend is also found in Fig. 1 of a paper by Christian Monzio Compagnoni et al. [4.2], as shown in Fig. 4.8. Likewise, their distribution is more like a Poisson distribution in smaller devices and is like an exponential function in larger devices. This Poisson-like RTN amplitude distribution in a small-area device will be discussed in Chapter 6.

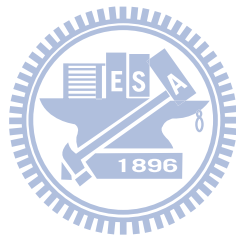
The simulated RTN and NBTI amplitude distributions are compared in Fig. 4.6. Our simulation confirms that the NBTI has a larger Δv_t tail. The reason is that a NBTI charge tends to be created in a critical path and a trapped charge in a critical current path has a larger influence on a channel current, thus resulting in a larger Δv_t due to a percolation effect. The difference in the shape of the distribution in measurement (Fig. 4.2) and in simulation (Fig. 4.6) is believed due to a different device size. A device size effect on the shape of the distribution can be found in [4.2]. Another possible reason is that our doping profile is fixed. An exponential ΔV_t distribution can be observed from a various random dopant distribution. [4.6]

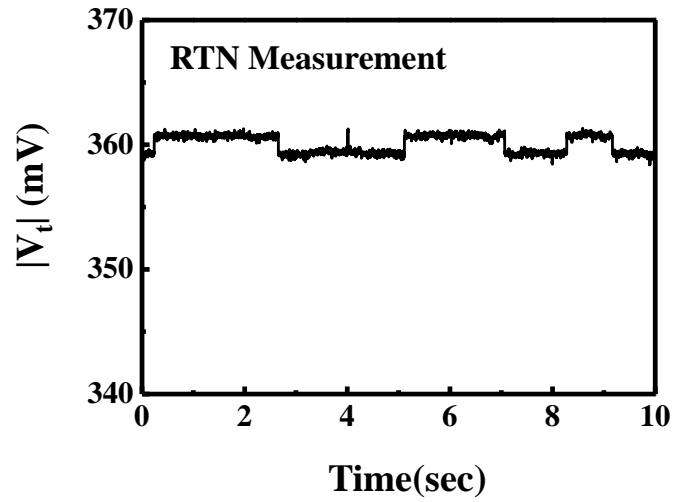
A similar argument can be applied to post-stress RTN in Fig. 4.2(b). In post-stressed devices, there exist two kinds of RTN traps, process induced traps (initial traps) and stress created traps. The initial traps have a tight Δv_t distribution while the stress created traps have a broader one. The overall distribution in post-stress devices therefore has a larger distribution tail.

4.4 Summary

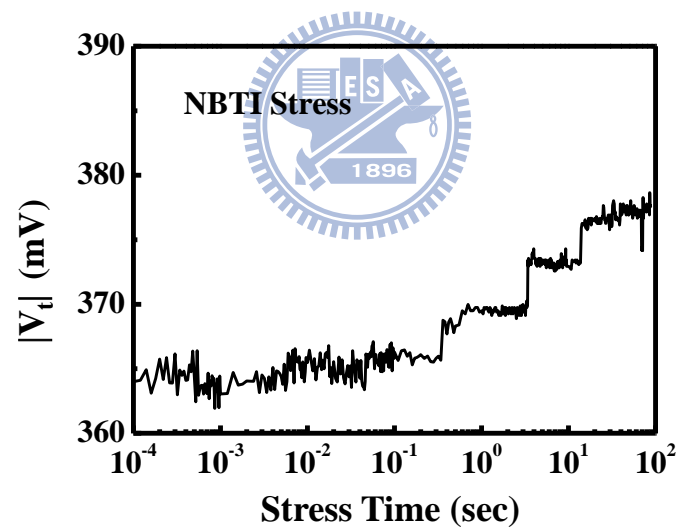
Single trapped charge induced Δv_t distributions in RTN and NBTI are characterized and simulated in pMOSFETs. Our simulation method takes into account

a trap creation probability in NBTI stress. Our study shows that a NBTI stress created charge has a larger Δv_t distribution tail than RTN due to current path percolation effect. This large NBTI induced distribution tail poses to be a serious CMOS reliability concern and should be carefully considered in a precise NBTI lifetime model.



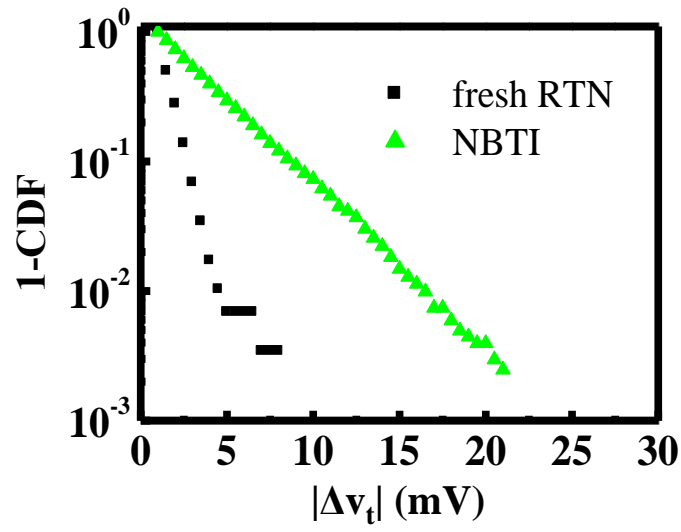


(a)

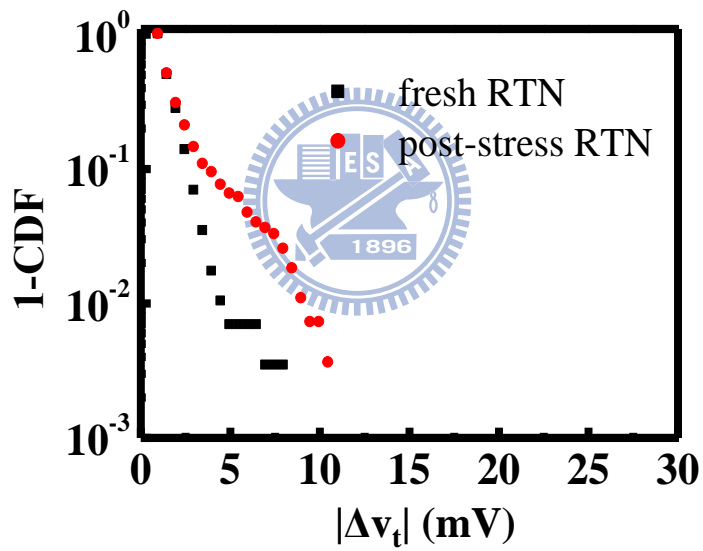


(b)

Fig. 4.1 (a) RTN measured at $V_d = -0.05V$ and a target I_d of $-500nA$. The V_t waveform is obtained from the measured drain current divided by a transconductance. (b) Threshold voltage trace in NBTI stress. The stress condition is $|V_g - V_t| = 1.5V$ and the measurement condition is the same as RTN measurement.

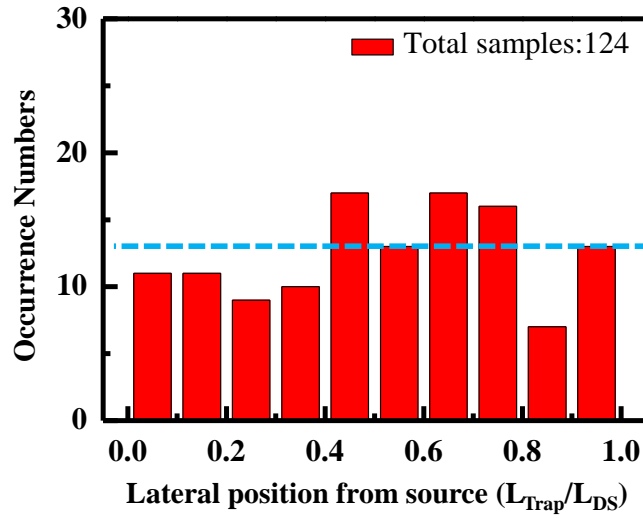


(a)

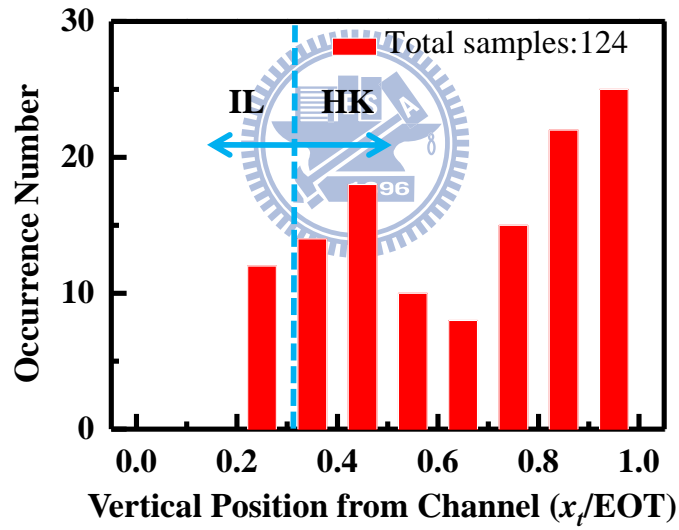


(b)

Fig. 4.2 (a) Complementary cumulative probability distribution (1-CDF) of a single trapped charge induced Δv_t in RTN vs. NBTI. RTN is measured in fresh devices. (b) 1-CDF of a single-charge induced Δv_t for RTN in fresh devices and in post-NBTI stress devices. The minimum detectable Δv_t is about 1mV.

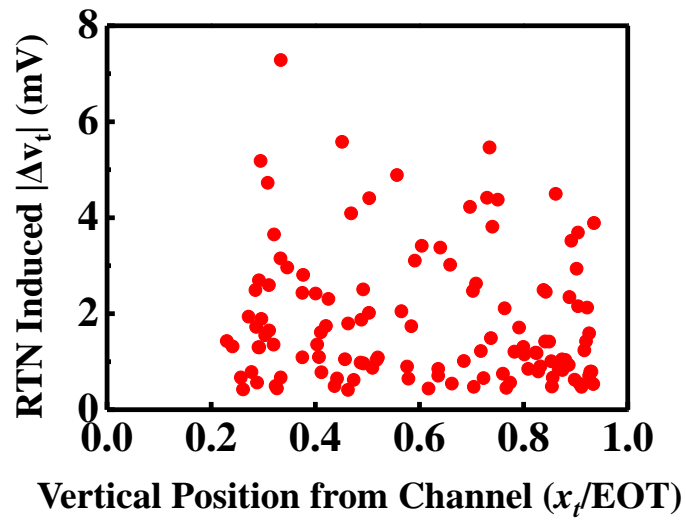


(a)

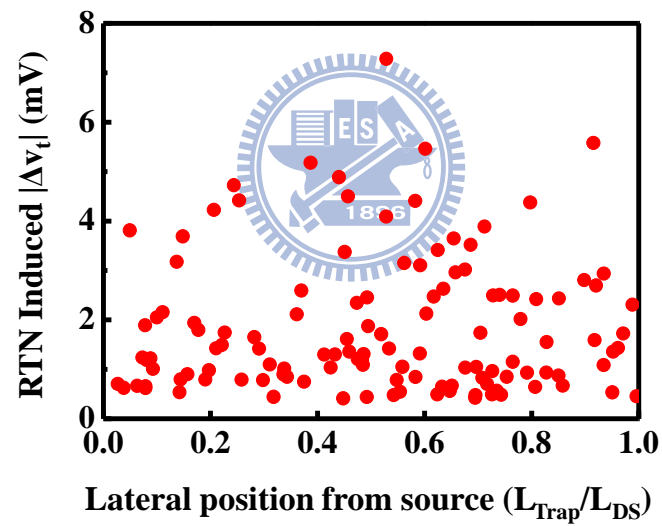


(b)

Fig. 4.3 (a) RTN trap position distribution along the channel extracted from 124 devices. L_{trap} is the distance of a trap from the source and L_{DS} denotes a channel length. (b) RTN trap position distribution along gate-to-bulk direction extracted from 124 devices. x_t is the distance of a trap from the channel surface.



(a)



(b)

Fig. 4.4 RTN amplitude distributions versus trap vertical (a) and lateral (b) positions.

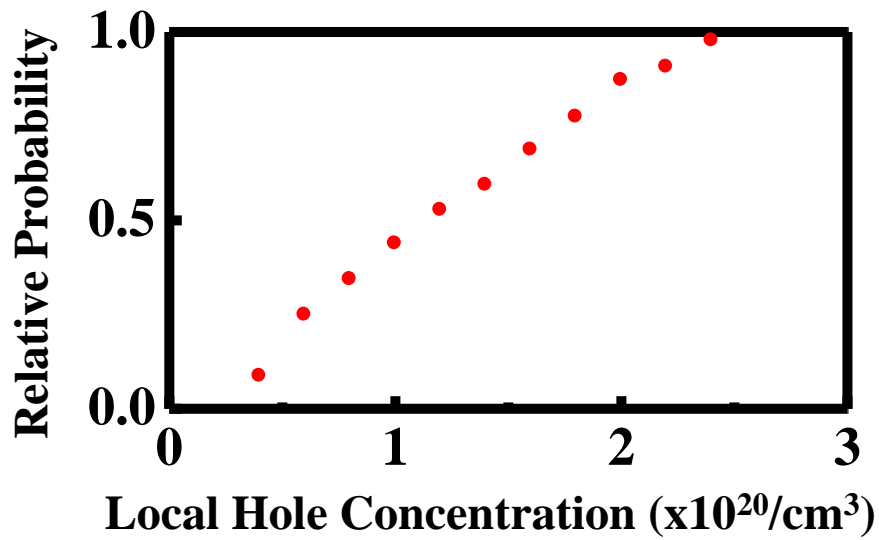


Fig. 4.5 Relative NBTI trap creation probability versus a local surface hole concentration. A local hole concentration and a surface electric field are calculated from a 3D device simulation with random and discrete substrate dopants. In the calculation, E_0 in Eq. (4.2) is 1.1MV/cm.

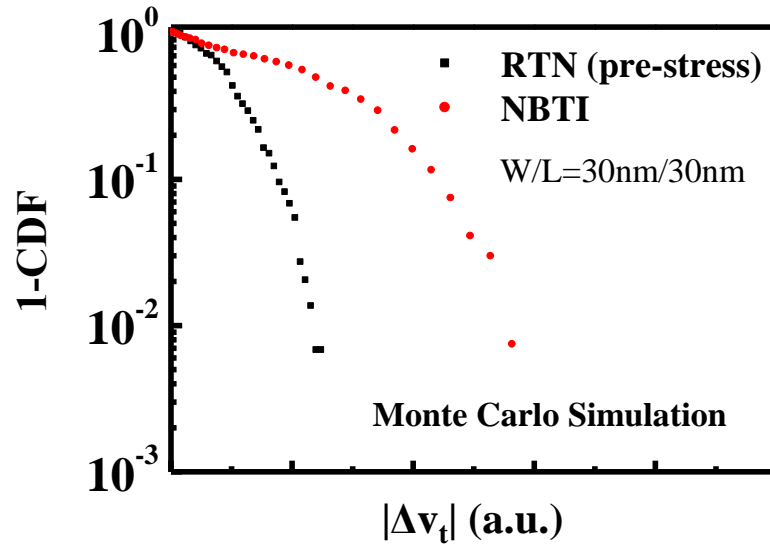


Fig. 4.6 Complementary cumulative probability distributions of RTN and NBTI amplitudes from 3D atomistic simulation. The simulated devices have a gate length of 30 nm and a gate width of 30nm. The NBTI trapped charge position in the simulation is selected according to its creation probability calculated from Eq. (4.2).

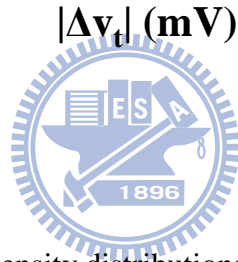
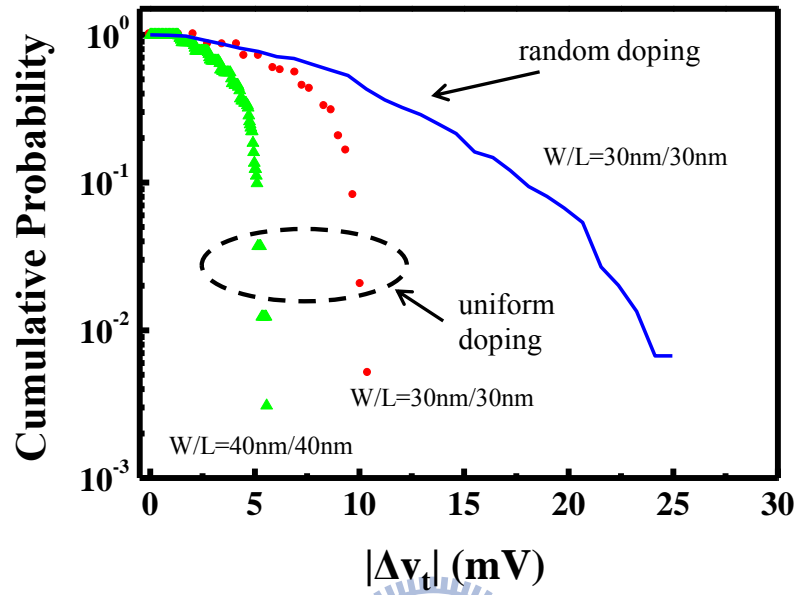


Fig. 4.7 Cumulative probability density distributions of RTN induced Δv_t amplitude in devices with $W/L=30\text{nm}/30\text{nm}$ w/ and w/o random doping and $W/L=40\text{nm}/40\text{nm}$.

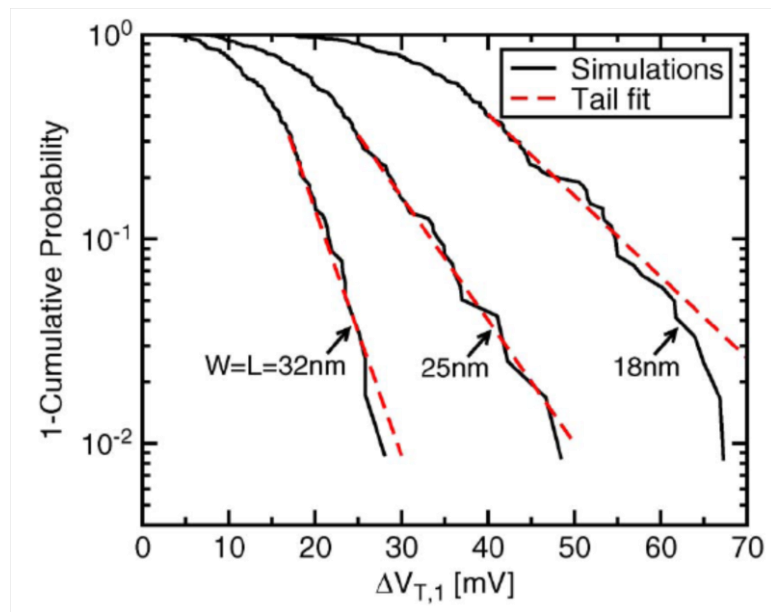


Fig. 4.8 Single charge induced Δv_t distributions in different device sizes [4.2].



Chapter 5

Program Charge Effect on Random Telegraph Noise

Amplitude and Its Device Structural Dependence in SONOS

Flash Memory

5.1 Preface

Random telegraph noise arising from electron emission and capture at an interface trap site has been recognized as a new scaling concern in flash memories [1.37]-[1.40]. V_t fluctuations originated from a large-amplitude RTN tail will cause a read error and become a prominent issue in designing a multilevel-cell (MLC) flash memory in 45nm technology node and beyond [1.39]. A statistical model based on a three-dimensional Monte Carlo simulation has shown that single-trap RTN amplitudes and thus V_t fluctuations exhibit an exponential distribution, i.e., $f(\Delta v_t) = \exp(-\Delta v_t/\sigma)/\sigma$ [4.7][5.1]. In a FG flash memory, the RTN tail is attributed to random dopant induced current-path percolation effects and σ is dependent on a substrate doping concentration. Unlike a FG flash, where program charges are stored in a conducting poly-silicon FG, program charges in a SONOS cell are stored randomly and discretely in a silicon nitride layer. (Fig. 5.1) Current percolation paths in a program-state of a MLC SONOS are determined by the placement of both substrate dopants and nitride trapped charges.

In this work, we characterized RTN in erase and program states in FG flash, planar SONOS and FinFET SONOS cells. $+V_g/-V_g$ FN injection is employed for program and erase. The program V_t window is chosen to be 1V for MLC application.

5.2 Program Charge Effect on RTN Amplitude in Floating Gate and SONOS Flash Memory

5.2.1 Measurement of RTN Amplitude in MLC Flash

In order to identify the concept of program charge induced percolation effect, first of all we measured single-trap RTN relative amplitudes ($\Delta I_d/I_d$) versus drain current in both FG flash cell (Fig. 5.2) and SONOS flash cell (Fig. 5.3) with different program window for MLC application. The FG flash cell dimension is $W/L=0.11\mu\text{m}/0.09\mu\text{m}$. RTN amplitudes in erase-state and in two different program-state are set at the same read current level of 500nA, drain voltage at 0.7V.

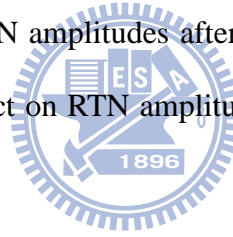
We find that program-state and erase-state RTN amplitude are identical, no matter program ΔV_t is 1V or 2V. However, as we measured single-trap RTN relative amplitudes versus drain current in a SONOS flash cell (cell dimension: $W/L=0.09\mu\text{m}/0.08\mu\text{m}$, a 2.8 nanometer tunnel oxide, a 6 nanometer silicon nitride and a 6 nanometer top oxide) with program window 0.8V and 1.5V, the curve of erase-state and program-state misalign.

The result can be explained by the idea we mentioned earlier in preface: (i) The program charges in the FG flash is continuous distribution and does not affect the percolation paths caused by substrate dopants due to a conducting charge storage layer (poly-Si). (ii) The current percolation paths are affected by the placement of both substrate dopants and random program charges in SONOS flash due to discrete charge storage. Furthermore, we can get that RTN amplitude decreases as drain current increases indicating that number fluctuation dominates at high current level and percolation effect plays a more important role at low current level.

5.2.2 Statistics Result of Program-state and Erase-state RTN

We also measured single-trap RTN relative amplitudes ($\Delta I_d/I_d$) in 40 FG flash cells and 60 SONOS flash cells, then we perform a bit-by-bit tracking plot of program-state RTN amplitude versus erase-state RTN amplitude. Devices with RTN amplitudes less than 3% are excluded to avoid possible measurement errors. In the case of FG flash, we find that almost all the dots lay on the straight line with slope=1, which indicates program-state and erase-state RTN have identical amplitudes in each FG cell (Fig. 5.4).

As a contrast, a distinctly different feature is obtained in planar SONOS cells. The RTN amplitudes spread in a wide range after programming and are almost independent of erase-state RTN (Fig. 5.5). One erase-state RTN amplitude might have many possible program-state RTN amplitudes after programming. Therefore, we can deduce that program charge effect on RTN amplitude is insignificant in FG flash but severe in SONOS flash.



5.2.3 Correlation Factor for Program-state and Erase-state RTN

To quantify program charge effect on RTN amplitude, a correlation factor, f , for program-state and erase-state RTN is defined as [5.2]

$$f = \frac{\sum (x - \bar{x})(y - \bar{y})}{\sqrt{\sum (x - \bar{x})^2 \sum (y - \bar{y})^2}} \quad (5.1)$$

where x and y denote RTN amplitudes in erase-state and in program-state, respectively, and \bar{x} and \bar{y} are average values.

A larger correlation factor suggests a smaller program charge induced percolation effect. Table 5.1 shows the measured correlation factor is 0.998 in FG flash,

suggesting no program charge effect on RTN while the correlation factor reduces to 0.286 in planar SONOS flash.

5.2.4 P/E Cycle Dependence of RTN

The RTN amplitude versus the drain current in the first three P/E cycles in FG flash is shown in Fig. 5.6. The result shows program-state and erase-state have the same RTN characteristics and implies that program charges in a FG do not alter current percolation paths caused by substrate dopants and no P/E cycle dependence. The first three P/E cycles in SONOS flash is shown in Fig. 5.7. The program-state RTN amplitude varies from cycle to cycle, suggesting that random program charges play an important role in current percolation paths. The measured RTN waveforms and the $I_d - V_g$ for SONOS flash are shown in Fig. 5.8 and the waveforms of the first two program-states are shown in Fig. 5.9. Two-level current switching is observed in both erase and program-states, showing that RTN arises from a single interface trap and no additional traps are created during P/E cycles. As a result, we affirm that the variation of RTN amplitude from cycle to cycle is attributed to different program charge percolation paths, not additional trap creation.

5.2.5 3D Atomistic Simulation of RTN

To evaluate percolation effect on RTN, we performed a 3D atomistic simulation [4.7] for FG and SONOS cells. The first step is establishing a flash cell for both FG and planar SONOS and then placing random discrete dopants in substrate and defining a site of an interface trap inside bottom oxide layer.

We need to consider two individual states: trapping and detrapping when simulating RTN amplitude. The first one with nothing is placed at the interface trap

standing for emission trap state in RTN phenomenon lets us extract an I-V curve, and the second one with an electron charge is put in the interface trap symbolizing occupation trap state lets us extract another I-V curve. Once we get the two I-V curve, we can calculate the relative RTN amplitude by calculating $\Delta I_d/I_d$. So, the simulation of erase state RTN amplitude can be achieved by following the procedure above.

When simulating program state RTN amplitude, two different program charge storage characteristics in FG and SONOS flash have to be taken into account respectively. In FG cell simulation, program charges have a continuous distribution and an equi-potential condition in a FG is obtained in the simulation. Besides, in a SONOS cell, nitride program charges are randomly placed. So again, the simulation of program state RTN amplitude can also be accomplished by the same method. Fig. 5.10 is our simulation flow chart for reference.

Fig. 5.11 shows our simulated RTN amplitude versus the drain current in a FG cell. The program and erase-state RTN are measured in three P/E cycles. The RTN amplitudes are all the same in three P/E cycles, in agreement with our measured result. Fig. 5.12 shows the simulation result in a planar SONOS cell. Ten different sets of random program charges with a similar program-state V_t are simulated. In all simulations no matter it is program-state or erase-state, a fixed placement of random substrate dopants and interface trap is used. The simulation shows that program-state RTN has a wide spread in amplitudes since each set of program charges results in a different current percolation path, the large variation of program-state RTN amplitude can be realized.

5.3 Device Structural Dependence on RTN in SONOS Flash Memory

5.3.1 Program Charge Effect on RTN in FinFET SONOS

Now, we are going to discuss a device structure effect on RTN in SONOS flash. In a FinFET structure which conducting current is confined to the corners of a silicon fin in weak inversion condition (Fig. 5.13). The percolation effect can be quite different from a planar SONOS.

Fig. 5.14 shows our measured program and erase-state RTN in FinFET SONOS for two P/E cycles. The fin height (H_{fin}) is 40nm and the fin width (W_{fin}) is 25 nm. Unlike a planar SONOS (Fig. 5.5), program-state and erase-state RTN are almost the same in a FinFET SONOS. It is apparent that the program-state RTN amplitude spread is significantly reduced in the FinFET SONOS (correlation factor $f=0.941$) as compared to the planar SONOS ($f=0.286$) which means that FinFET structure can substantially reduce program charge induced percolation effect. The correlation factors can be found in Table 5.1.



5.3.2 Degree of Inversion in FinFET SONOS

Degree of inversion may be one of the reasons that cause the reduction of percolation effect in FinFET SONOS. As we mentioned earlier, in a condition of stronger inversion, number fluctuation replaces percolation effect to become the decisive factor in RTN amplitude. To clarify this point, we measured RTN at a smaller drain current reduced from 500nA to 200nA. The RTN amplitude increases as drain current level decreases. However, we still find a good correlation between erase-state and program-state (Fig. 5.15). Stronger inversion does not seem to be the cause of the high correlation factor in FinFET SONOS.

5.3.3 Channel Width Effect on Program Charge Induced Percolation Effect

The second possible reason for the large correlation factor in FinFET SONOS is

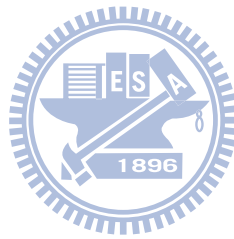
the confinement of channel current. In a large-width planar SONOS, percolation paths are widely distributed in the width direction. Program-state and erase-state may have different percolation paths, as illustrated in Fig. 5.16. In a FinFET SONOS, however, the channel current is confined in the small region in Silicon fin. There are seldom choices for current percolation, so the program-state and erase-state have the same conducting path. Thus, program charge effect on RTN is smaller.

Fig. 5.17 shows that the program-state RTN spread can be further reduced as a fin width reduces from 25nm to 10nm. The measured correlation factor increases from $f=0.817$ in $W_{fin}=25\text{nm}$ and $f=0.941$ in $W_{fin}=10\text{nm}$ (Table 5.1). We also perform a 3D RTN simulation in planar SONOS with different channel width, as shown in Fig. 5.18. Our simulation indeed shows that the correlation factor increases with a decreasing gate width. The measurement and simulation reveal the same trend that smaller channel width lead to smaller program charge induced percolation effect on RTN amplitude due to confinement of channel percolation. This current path confinement effect will be discussed in the following Chapter.

5.4 Summary

Read failure due to a RTN induced v_t tail is an important issue in flash memory scaling. In a FG flash, RTN amplitudes are mainly determined by random dopant induced percolation effect and identical in erase and program states. However, in a planar MLC SONOS, we find that RTN amplitudes have a wide spread after program. The program-state RTN distribution is affected by both random program charges and substrate dopants. In addition, the RTN amplitude varies from P/E cycle to P/E cycle due to program induced percolation effect. Therefore the program charge effect has to be considered in RTN modeling in MLC SONOS.

According to our experiments and simulations, the program charge induced percolation effect can be significantly reduced in a surrounding gate structure, such as a FinFET SONOS.



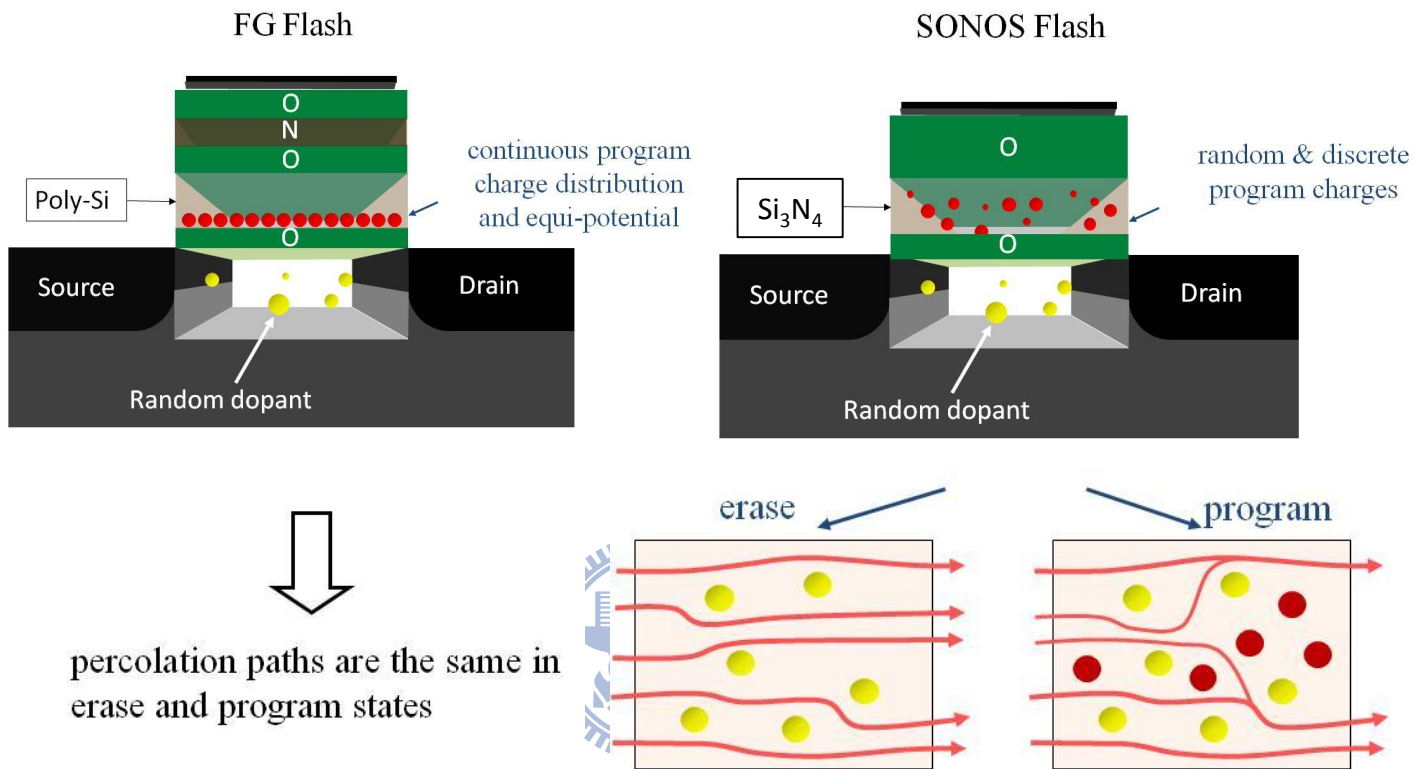


Fig. 5.1 An illustration of two different program charge storage characteristic resulting distinct outcome of percolation path. Continuous distribution in FG flash and random discrete distribution in SONOS flash.

Floating Gate cell

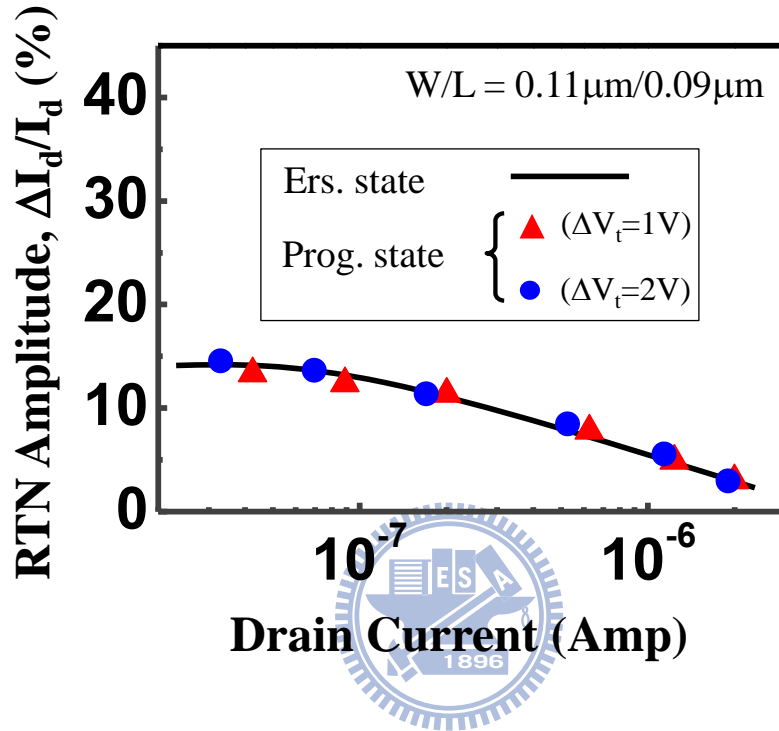


Fig. 5.2 RTN amplitude versus drain current in a FG flash cell at two program windows : 1V, 2V. The drain voltage in measurement is 0.7V and the gate voltage is varied.

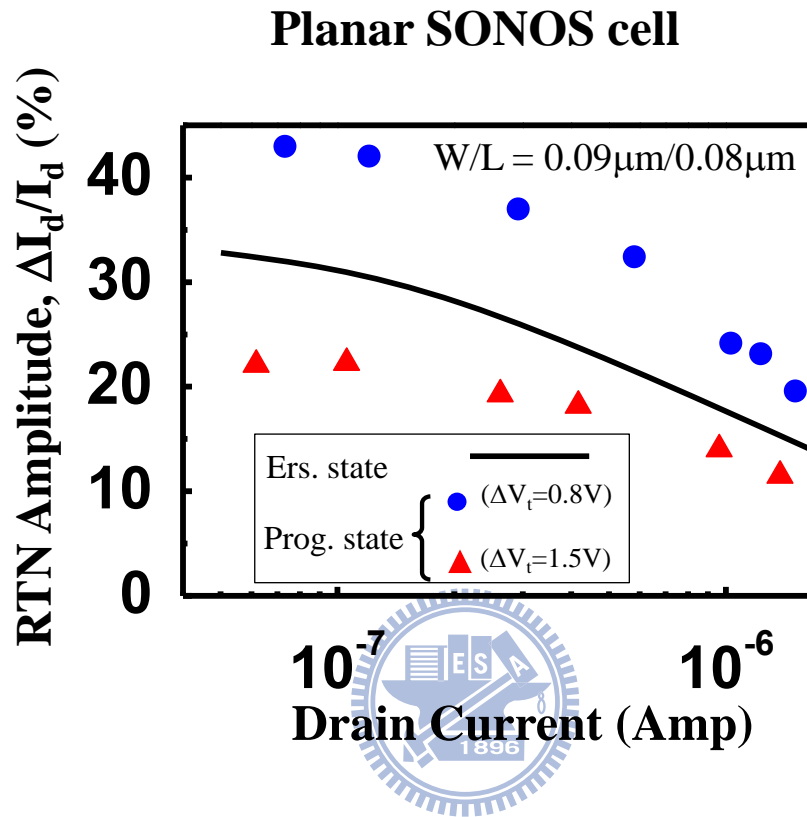


Fig. 5.3 RTN amplitude versus drain current in a SONOS flash cell at two program windows : 0.8V, 1.5V. The drain voltage in measurement is 0.7V and the gate voltage is varied.

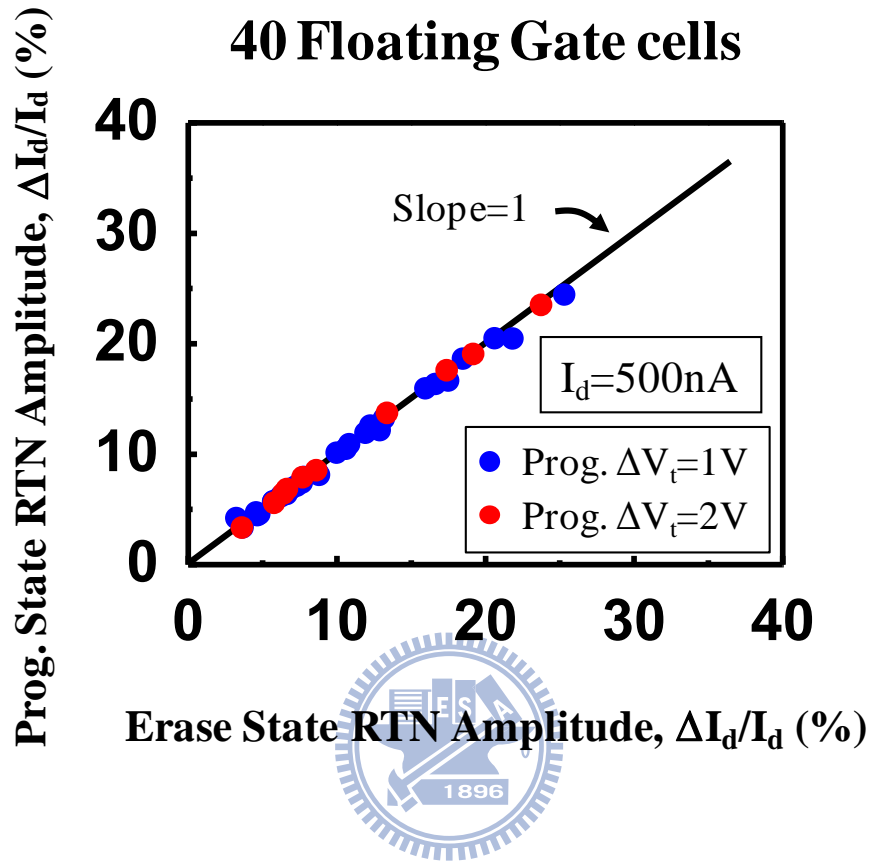


Fig. 5.4 Measured program-state RTN amplitude versus erase-state RTN amplitude in 40 FG flash cells. The RTN amplitude is measured at $I_d=500nA$ @ $V_d=0.7V$. The device dimension is $W/L=0.11\mu m/0.09\mu m$. The program window is 1V or 2V.

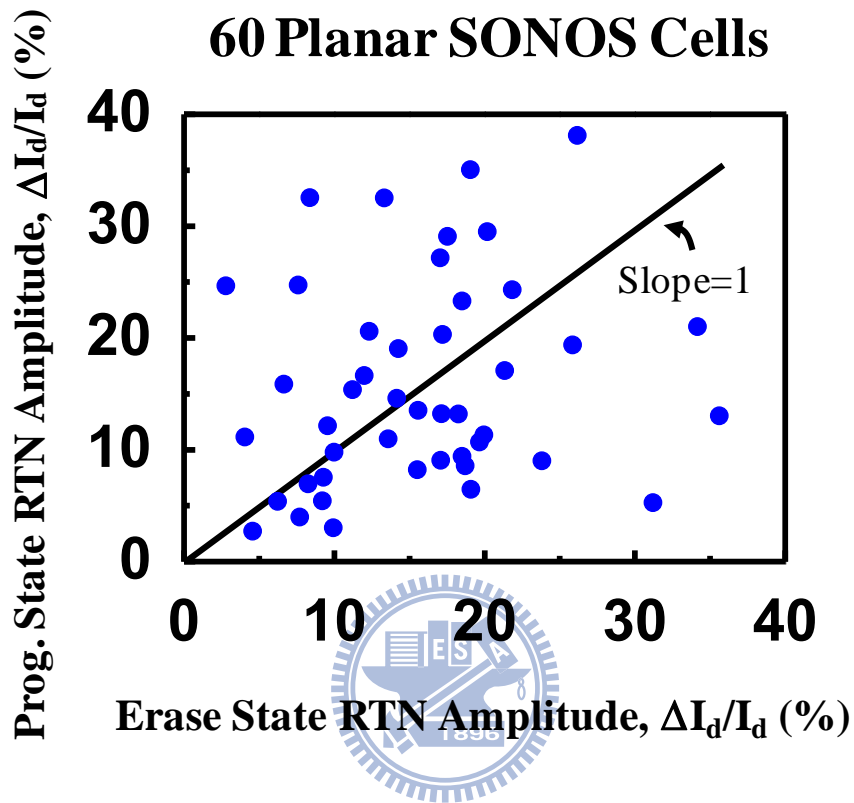
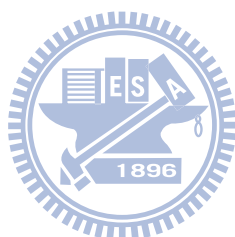


Fig. 5.5 Measured program-state RTN amplitude versus erase-state RTN amplitude in 60 planar SONOS cells. The RTN amplitude is measured at $I_d=500\text{nA}$ @ $V_d=0.7\text{V}$. The SONOS cells have $W/L=0.09\mu\text{m}/0.08\mu\text{m}$, a 2.8nm tunnel oxide, a 6nm Si_3N_4 and a 6nm top oxide.

Table 5.1 Measured RTN correlation factors in FG flash, planar SONOS and FinFET

SONOS cells.

Correlation Factor			
Floating Gate	Planar SONOS	FinFET SONOS	
0.998	0.286	$W_{FIN}=25$	$W_{FIN}=10$
		0.817	0.941



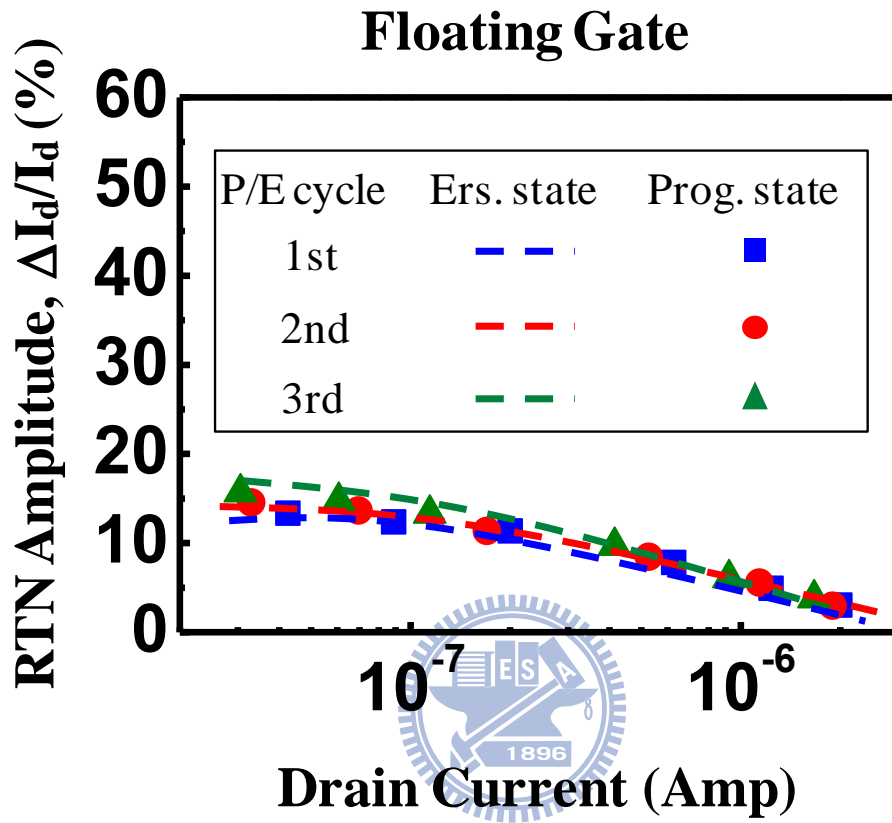


Fig. 5.6 RTN amplitude versus drain current in a FG flash cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied.

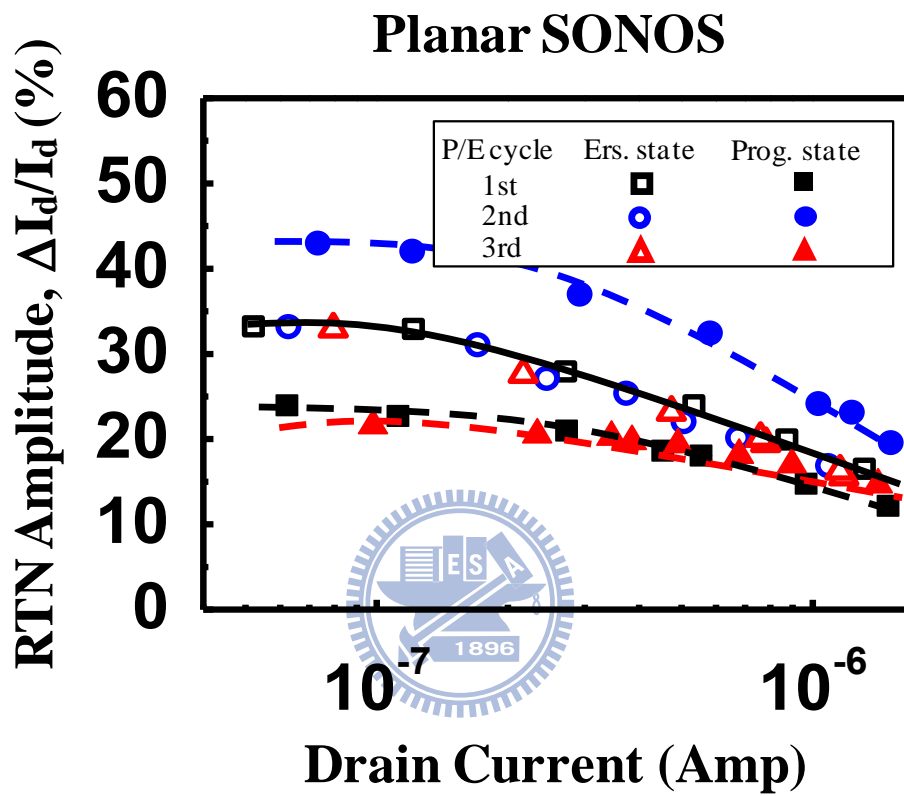


Fig. 5.7 RTN amplitude versus drain current in a SONOS cell in three P/E cycles. The V_t window is 1V. The drain voltage in measurement is 0.7V and the gate voltage is varied.

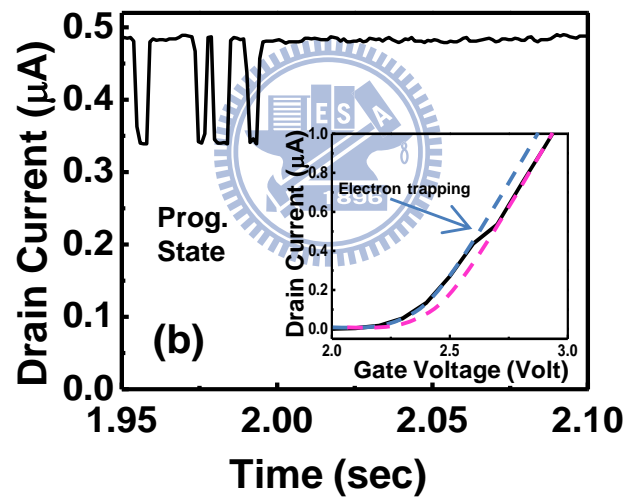
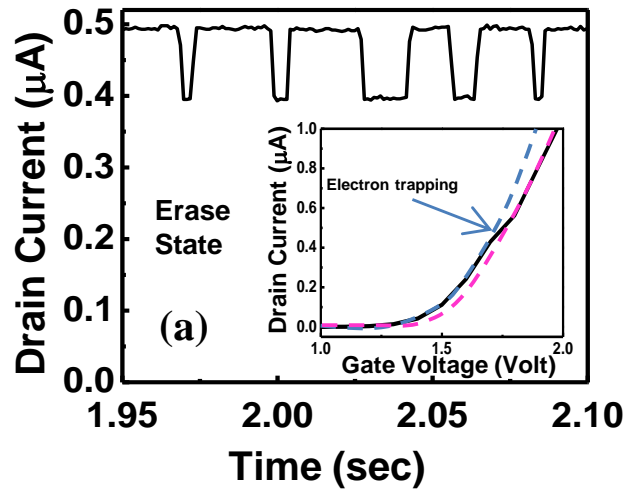


Fig. 5.8 Measured RTN waveform and I_d versus V_g plot (a) in erase-state and (b) in program-state of a SONOS cell. Electron trapping at an interface trap is manifested by a current discontinuity in the I_d - V_g plot.

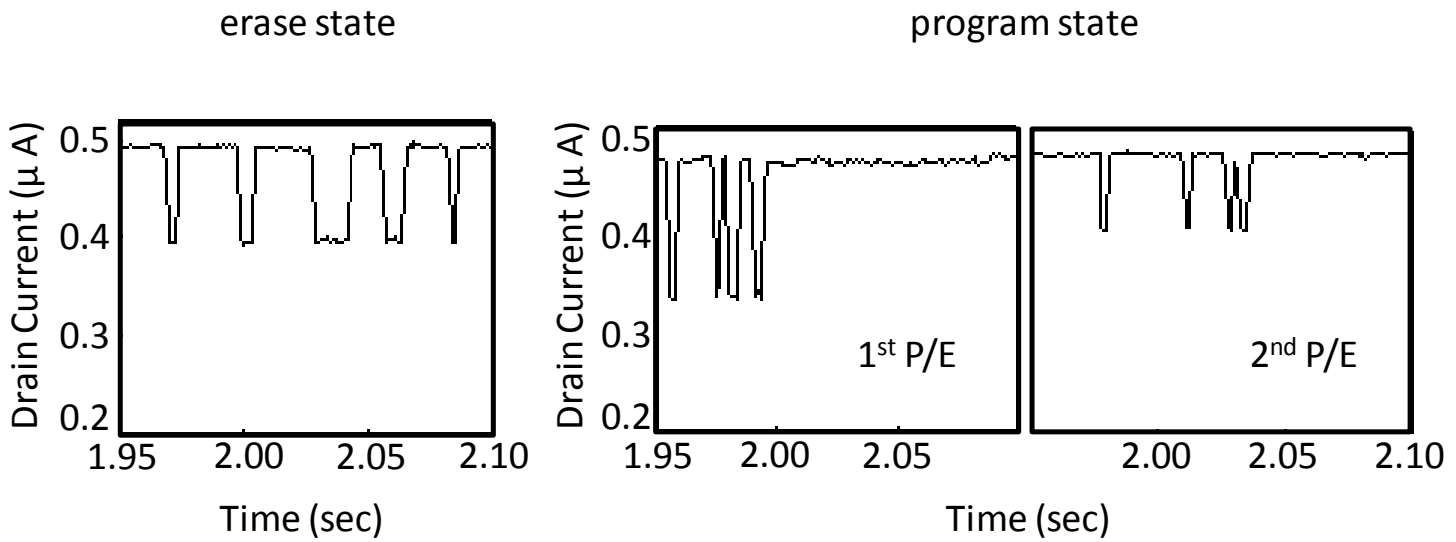


Fig. 5.9 The waveform of two-level RTN current switching is observed in erase-state and 1st and 2nd program-state.

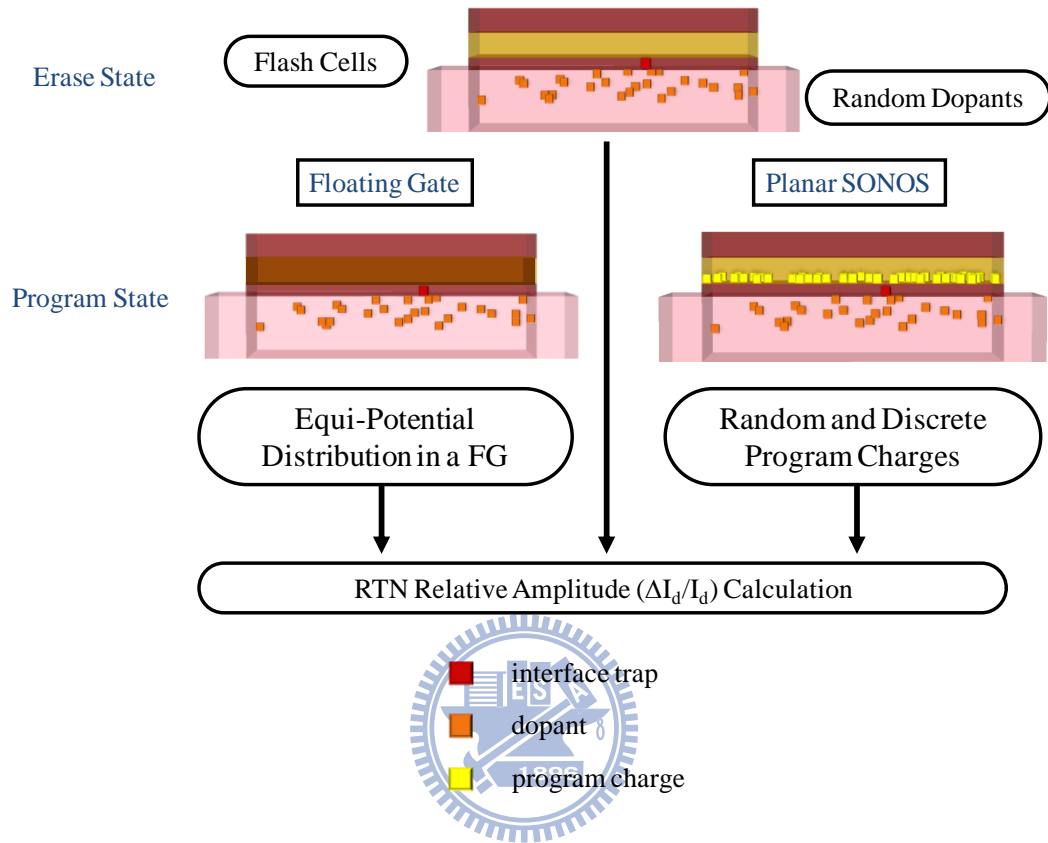


Fig. 5.10 Simulation flow chart of our 3D atomistic simulation for RTN amplitude at program state and erase state for both FG flash and planar SONOS flash.

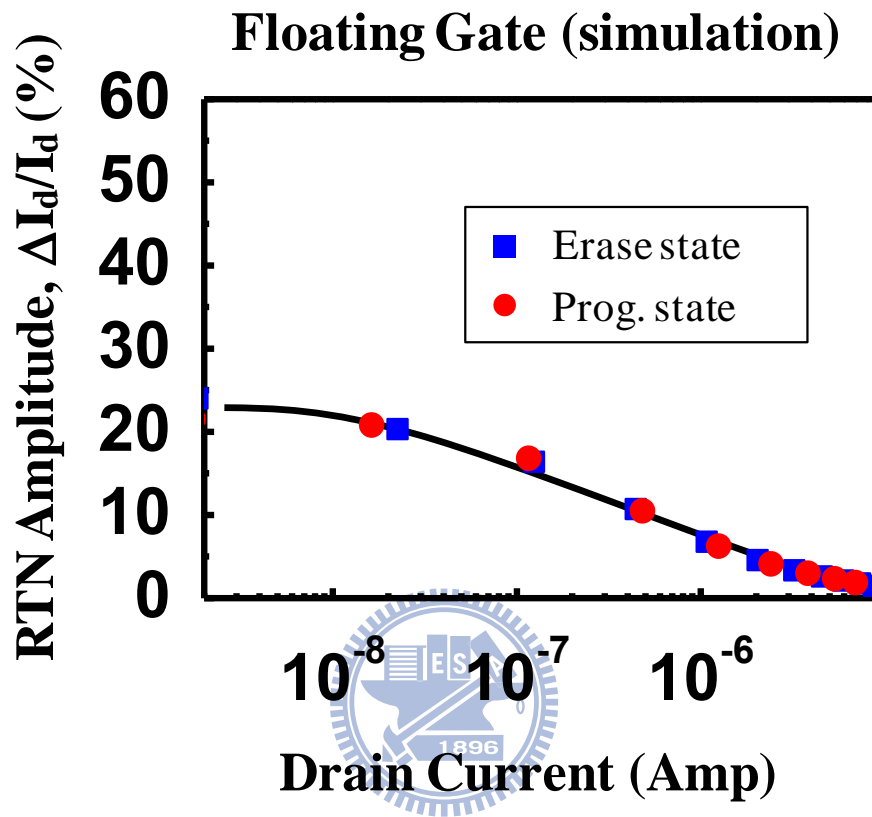


Fig. 5.11 Simulated RTN amplitude versus drain current in a FG flash cell. Program-state and erase-state have the same placement of substrate random dopants. The RTN trap is placed in the middle of the device.

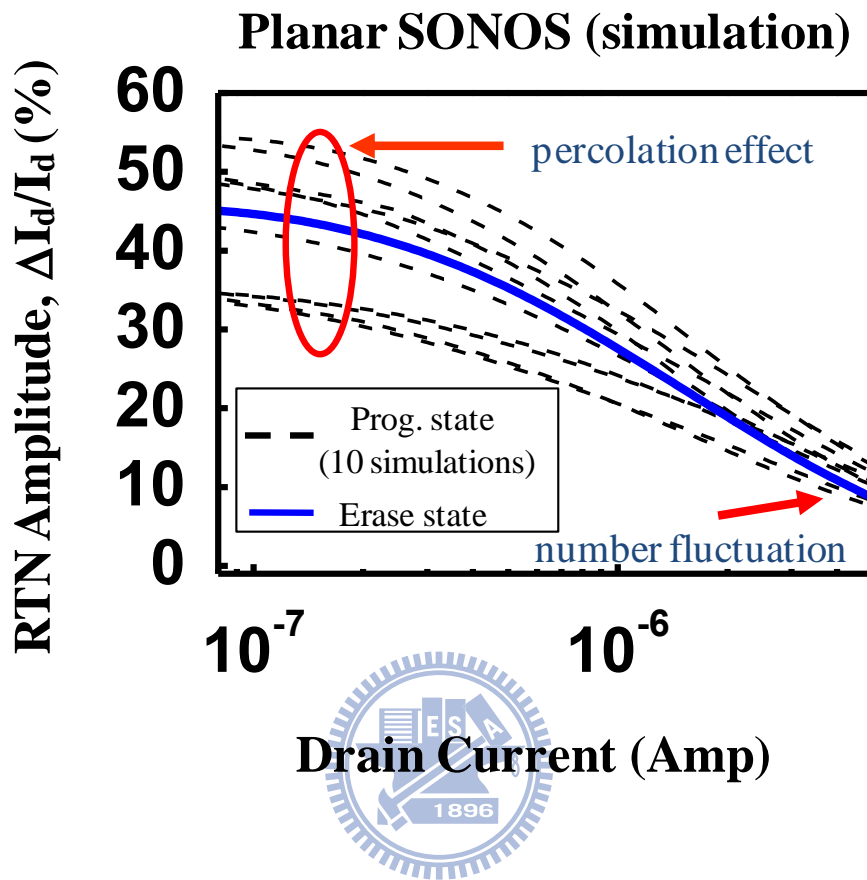


Fig. 5.12 Simulated RTN amplitude versus drain current in a planar SONOS cell. Program-state and erase-state have a fixed placement of substrate dopants. Ten different sets of random program charges are simulated. An RTN amplitude due to number fluctuation is calculated with continuous substrate doping and program charges.

FinFET SONOS Gate

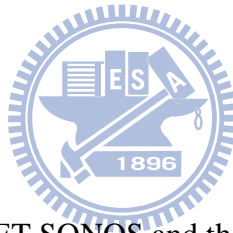
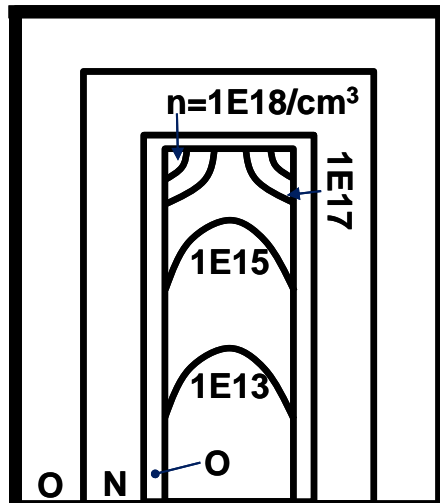


Fig. 5.13 Cross-section of a FinFET SONOS and the electron concentration contour in the FinFET SONOS obtained from a 2D simulation.

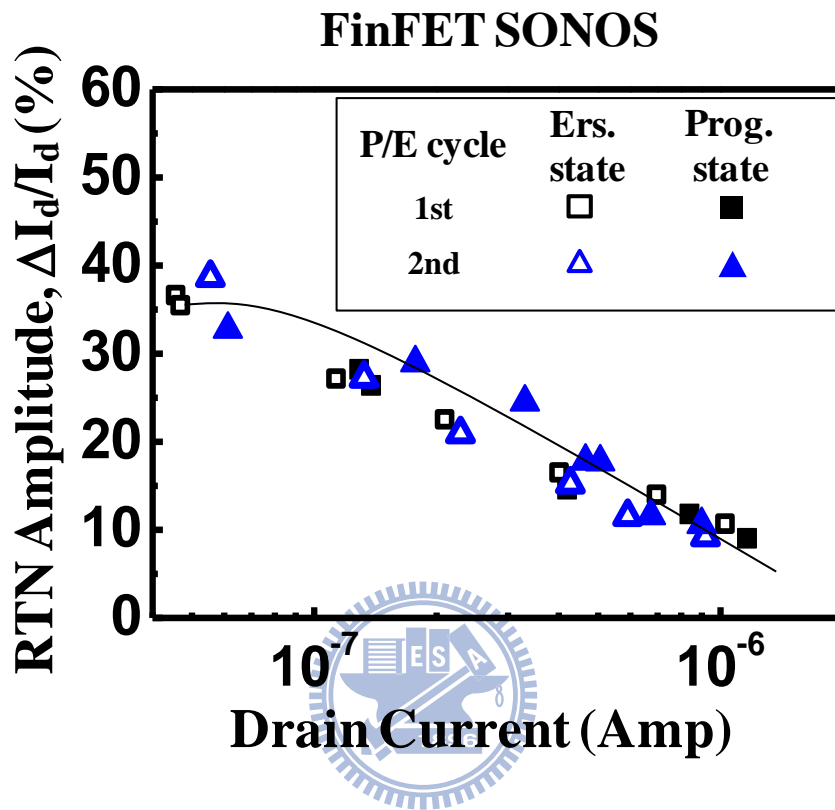
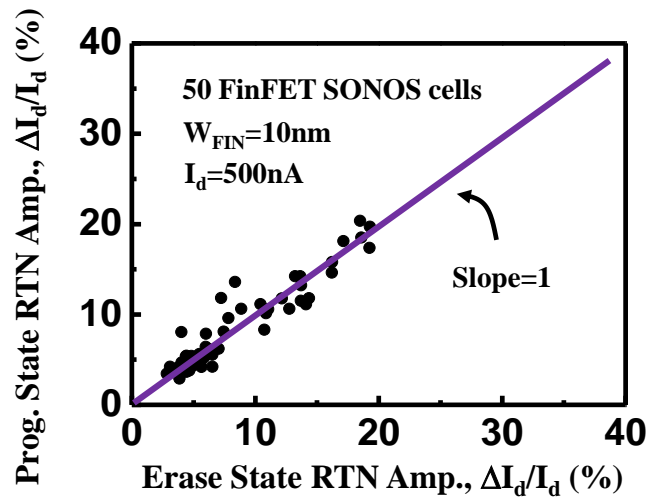
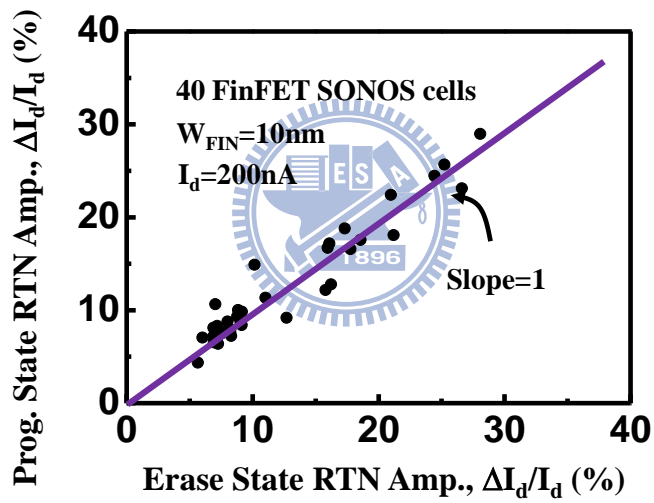


Fig. 5.14 RTN amplitude versus drain current in a FinFET SONOS cell for two P/E cycles.



(a)



(b)

Fig. 5.15 Program-state RTN amplitude versus erase-state RTN amplitude in FinFET SONOS cells. The fin width is 10nm. (a) RTN is measured at $I_d=500\text{nA}$ and (b) RTN is measured at $I_d=200\text{nA}$.

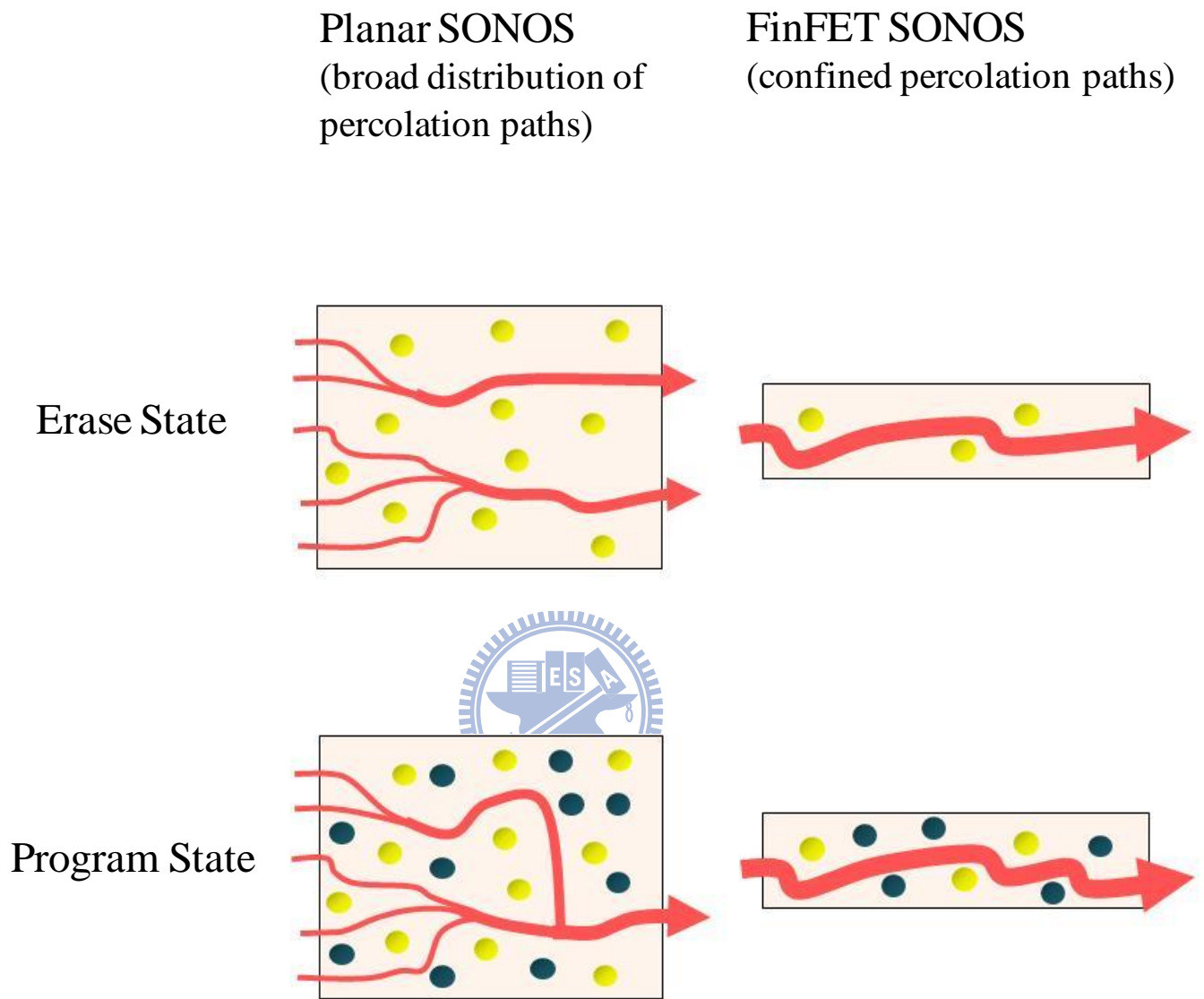
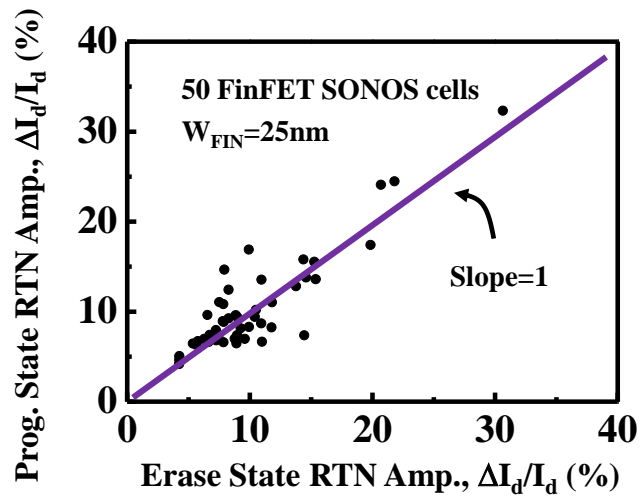
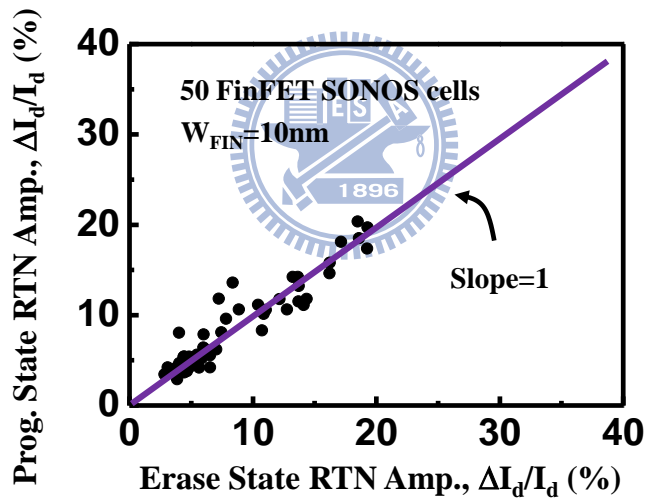


Fig. 5.16 In a planar SONOS, percolation paths are widely distributed in the gate width direction. In a FinFET SONOS, conducting paths are confined to a small region in the corner of the Si fin.



(a)



(b)

Fig. 5.17 Measurement of the correlation factor in FinFET SONOS with two different fin widths, 10 nanometer and 25 nanometer. The correlation factor increases from 0.82 to 0.94 as the fin width reduces from 25 nanometer to 10 nanometer.

Simulation (Planar SONOS)

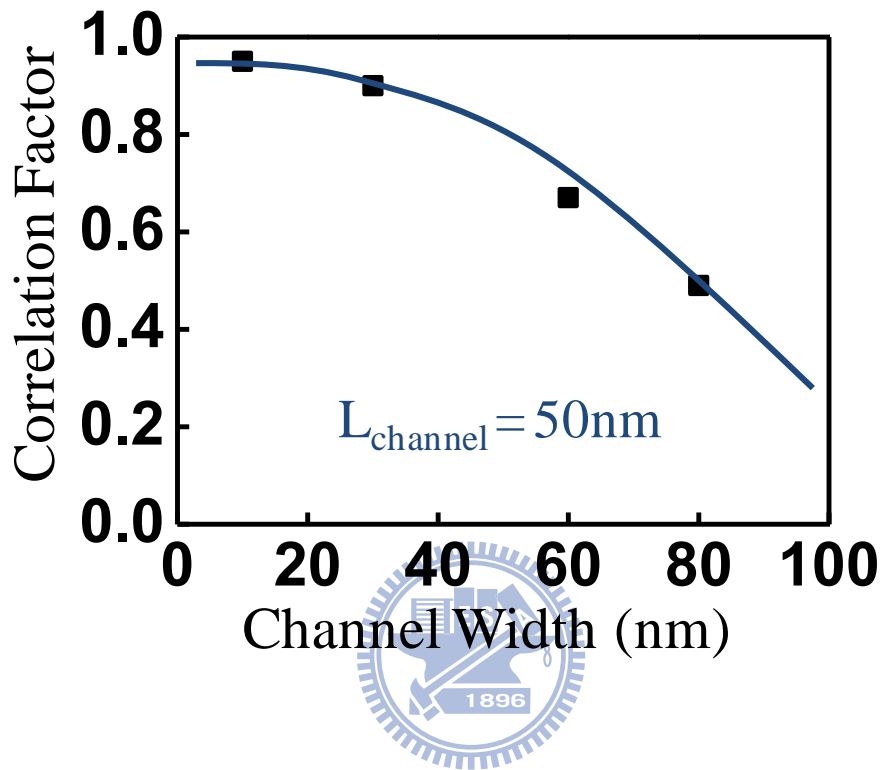


Fig. 5.18 A 3D RTN simulation in planar SONOS with different channel width. The correlation factor is calculated based on a sample size of 40 devices.

Chapter 6

Physical Origin and Analytical Modeling of RTN Amplitude Distribution in MOSFETs with a Nanowire-Like Channel

6.1 Preface

Random telegraph noise (RTN) has been recognized as a major reliability concern in CMOS and flash memory devices. Extensive characterization, modeling and numerical simulation of a single charge trapping and detrapping induced threshold voltage fluctuations in RTN have been performed [1.34][4.1][5.1][6.1]-[6.3]. Studies have shown that RTN amplitudes scatter over a wide range as device dimensions reduce. Several factors affecting RTN amplitudes have been discussed [1.40][6.1]-[6.3][5.1]. According to McWhorter's and Hooge's works [6.4][6.5] and later a unified noise model proposed by Hu [6.6], trapping/detrapping of a single carrier charge near the Si/SiO₂ interface would modulate a channel carrier density and mobility. RTN amplitudes can be modeled by the fluctuations of a carrier number and mobility. The position of an RTN trap in a channel also affects RTN amplitudes because of a different electrostatic effect on channel conduction. For example, an RTN trap in the center of the channel has larger electrostatic control and thus larger RTN amplitudes [5.1][6.7]. Aside from the main part of an RTN amplitude distribution, recent studies show that RTN exhibits a large distribution tail in scaled CMOS and flash memory devices. An empirical formula $f(|\Delta V_t|) = \exp(-|\Delta V_t|/\sigma)/\sigma$ was adopted to approximate an RTN tail, where σ is a function of a substrate doping concentration and device dimensions [1.40][5.1]. A 3D atomistic Monte Carlo

simulation by Asenov [4.1] shows that the spread of RTN amplitudes is attributed to a current path percolation effect arising from random substrate dopants. A similar ΔV_t distribution tail was also observed in BTI induced V_t shifts in MOSFETs [2.7] and in a single program charge loss induced V_t retention loss in SONOS flash cells [6.8] for the same origin. Although various theoretical models have been proposed to calculate random dopant induced fluctuations of device characteristics such as the variance of threshold voltage [6.9]-[6.14], rare efforts have been made in the past to explain a random dopant induced RTN amplitude distribution by an analytical approach. Furthermore, to improve a design window that is tightened by several variability sources in modern CMOS technology, the integration of RTN characteristics into a circuit simulation is called for in advanced CMOS circuit design. An analytical RTN model accounting for an entire amplitude distribution is therefore required in a worst-case circuit simulation.

As the scaling of CMOS technology advances, a gate width and a body thickness of a MOSFET are reduced. To further improve device reliability and performance, novel MOSFET structures such as FinFET and nanowire MOSFETs have been proposed [6.15]-[6.17]. In these devices, a channel cross-section in the current flow direction is very small. The influence range of a dopant charge would cover an entire cross-section, thus making a channel one-dimension-like. In such one-dimensional channel MOSFETs, a dopant charge or an RTN trapped charge does not alter a current path, but only modulates a local conductivity in the channel. Fig. 6.1 illustrates a conduction electron density distribution in a 40nm-long cylindrical channel nMOSFET from a 3D device simulation. The channel has a diameter of 6nm. A dopant charge is placed at a distance of $x=30\text{nm}$ from the source. The influence of the dopant charge extends to a whole cross-section, as shown in Fig. 6.1(a). An electron

density along the channel is plotted in Fig. 6.1(b). A screening length calculated from the Thomas-Fermi theory [6.18] is also drawn in the figure, which will be discussed later. As shown in Fig. 6.1(b), a dopant charge interaction range can be roughly estimated on the order of the screening length. In this work, we derive an analytical RTN distribution model based on random dopant induced conductivity modulation in a channel. Our model will be verified by a numerical device simulation.

6.2 One-Dimensional Channel RTN Simulation

To explore RTN amplitude fluctuations in a nanowire channel MOSFET, a 1D channel Monte Carlo RTN simulation by using ISE TCAD [3.9] is developed. In an ideal 1D channel device, current path modulation does not exist. To remove a percolation effect in simulation, we place a dopant charge uniformly in a 1nm slice in a channel and an RTN charge in a 1nm bar on the top of a channel, as illustrated in Fig. 6.2. This simulation approach is reasonable when the size of a channel cross-section is comparable to a Thomas-Fermi screening length. The minimum grid size in simulation is 0.2nm. Our simulation does not take into account a local modulation in a mobility associated with a trapped charge. Size quantization effects are not included, either. We choose a double-gate MOSFET structure as an example for the purpose of better numerical simulation convergence. The devices have a gate width of 7nm, a silicon film thickness of 5nm and a channel length of 40nm and 30nm, respectively. The gate dielectric has an equivalent oxide thickness of about 0.9nm. To verify the accuracy of the 1D simulation scheme, we perform a conventional 3D atomistic RTN simulation for comparison. In 3D atomistic simulations, a dopant charge is placed in a 2nm cube. Fig. 6.3 shows complementary cumulative distribution functions (1-CDF) of RTN induced ΔV_t from the 1D channel and 3D atomistic simulations. At a large

gate width, for example, $W=20\text{nm}$ in Fig. 6.3(a), we find a large difference in the distribution tails from the 3D and 1D simulations. The 3D simulation has a larger ΔV_t tail due to a current-path percolation effect in the channel width direction. However, as a gate width reduces to 7nm (Fig. 6.3(b)), the 1D channel simulation result converges to the 3D atomistic simulation quite well. It should be mentioned that RTN amplitude depends on a measurement current level. In a nanowire channel MOSFET, a conventional V_t definition, i.e., $I_D=1\mu\text{A}/\mu\text{m}$, is no longer appropriate because of volume inversion. Here, we define a V_t as a gate voltage when I_D is 200 nA at a V_{ds} of 0.02 V . Our simulated RTN amplitude (ΔV_t) is relatively small compared to published result [6.8] because the V_t is defined at a higher current level.

To gain insight into RTN characteristics in 1D channel MOSFETs, we perform a 1D channel Monte Carlo RTN simulation in a large number of devices. The simulated devices have a channel length (L_c) of 40nm and a doping concentration of $1 \times 10^{19}/\text{cm}^3$. At such doping level, each device has 14 dopants on an average. Channel dopants are randomly placed in a channel, and so is an RTN trap. In addition, we divide the channel into a number of sections with an RTN trap at the center of a section. The width of each section (l) is chosen to be two times the Thomas-Fermi screening length, i.e.,

$$l = 2 \cdot \left[\frac{\epsilon_{si} kT}{n_c e^2} \right]^{1/2} \quad (6.1)$$

where n_c is a channel electron concentration, k is the Boltzmann constant and other variables have their usual definition. Thus, only dopants in the same section as an RTN trap would affect a local conductivity at the trap site. The number of dopants in an RTN trap section is denoted by n .

Simulated RTN amplitudes with $n=0, 1, 2, 3$ are shown in Fig. 6.4 (a). For each n , we simulate 100 devices. The distribution function of RTN induced ΔV_t for each n is plotted in Fig. 6.4(b). Standard deviation and average RTN amplitude versus a dopant number n in an RTN trap section is shown in Fig. 6.5. We observe two salient features about the RTN distributions. First, we find that the RTN distributions in Fig. 6.4(b) are relatively tight in sense that their standard deviation is small, as compared to an incremental change of average RTN amplitude with n , thus implying that RTN amplitudes are mostly affected by local dopants. For simplification, we use a δ -function to approximate an RTN amplitude distribution for each n in our model development.

We would like to remark that a calculated Thomas-Fermi screening length is much smaller than the width of an electron depletion region caused by a dopant charge, as shown in Fig. 6.1. The assumption of a section size (l) equal to two times the screening length is actually an approximation. The standard deviation in Fig. 6.5, or the locality of RTN amplitudes, can be further improved by adjusting a section size. For RTN circuit simulation, l can be treated as a fitting parameter for the best fit to measurement. Second, we find that an average RTN induced ΔV_t increases almost linearly with a dopant number n in the range of interest. Based on the approximations of the δ -function distribution and the linear dependence, we therefore can write down an expression for an RTN induced ΔV_t as follows.

$$\Delta V_t(n) = \Delta V_0 + \alpha \cdot n \quad (6.2)$$

where α is a slope in Fig. 6.5.

Furthermore, we verify the linear relationship between average RTN amplitude

and a number of local charges by measuring RTN in channel hot electron programmed SONOS cells. Aforementioned in Chapter 5, program charges in SONOS play a similar role as channel dopant. The reason to use SONOS cells is that we can adjust the number of injected local trapped charges by CHE program and measure corresponding RTN amplitudes [4.5]. Fig. 6.6 shows an average RTN induced ΔV_t from an ensemble of 45 devices versus a program V_t window. Note that the latter is proportional to a number of program trapped charges. In the measurement range, a linear relationship is a good approximation.

6.3 Analytical RTN Amplitude Distribution Model

In our model, the channel is divided into a number of sections. The width of sections is l and the total number of sections in a device is $p(=L_c/l)$. Since dopants are randomly placed in a channel, the probability density function (f) of the number of dopants (n) in a certain section, where an RTN trap is located, can be expressed by a Binomial distribution, i.e.,

$$f(n; N, p) = C_n^N \cdot \left(\frac{1}{p}\right)^n \cdot \left(1 - \left(\frac{1}{p}\right)\right)^{N-n} \quad (6.3)$$

where $C(N, n)$ is a binomial coefficient and N denotes the total number of dopants in a device. As N and p are sufficiently large, Eq. (6.3) can be approximately by a Poisson distribution

$$f(n; \lambda) = e^{-\lambda} \cdot \frac{\lambda^n}{n!} \quad (6.4)$$

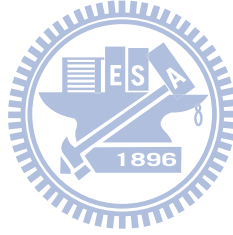
where

$$\lambda = N \cdot \frac{1}{P} \quad (6.5)$$

Substituting Eq. (6.2) into Eq. (6.4), we obtain a probability distribution function of RTN induced ΔV_t as

$$f(\Delta V_t) = e^{-\lambda} \cdot \frac{\lambda^{\frac{\Delta V_t - \Delta V_0}{\alpha}}}{\left(\frac{\Delta V_t - \Delta V_0}{\alpha}\right)!} \quad (6.6)$$

As pointed out, an RTN trap at a different channel position exerts different electrostatic influence on channel conduction. Rigorously speaking, α and ΔV_0 should be a function of an RTN trap section index. For simplicity, we neglect such trap position dependence here.



6.4 Results and Discussion

We compare our analytical model with 1D channel Monte Carlo simulation results for different doping concentrations and gate lengths. Fig. 6.7 shows calculated complementary cumulative distribution function (1-CDF) of RTN induced ΔV_t for a doping concentration of $5 \times 10^{18}/\text{cm}^3$, $7 \times 10^{18}/\text{cm}^3$, and $1 \times 10^{19}/\text{cm}^3$, respectively. The gate length is 40nm. The symbols represent our model result and the solid lines are obtained from 1D channel Monte Carlo simulation. All three distributions with different amount of channel dopants have the same l ($=3.4\text{nm}$), α ($=3.2\text{mV}$) and ΔV_0 ($=2.9\text{mV}$). About 500 devices are simulated for each doping concentration. In general, our analytical model agrees with the simulation result quite well. The flatter part of the complementary cumulative distribution plots is recognized due to ΔV_0 , which reflects simply a carrier number fluctuation. On the other side, the RTN distribution

tail is caused by the aggregation of dopants near an RTN trap. The RTN tail is more pronounced at a larger doping concentration.

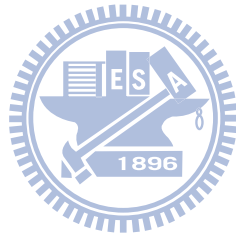
Fig. 6.8 shows the complementary cumulative distribution functions of RTN induced ΔV_t at two channel lengths, 40nm and 30nm. Since a carrier number fluctuation is more significant as device size reduces, ΔV_0 and α are larger in a shorter device. Here, α is 3.7mV and ΔV_0 is 3.8mV for a channel length of 30nm. Note that the calculated distribution function at a larger gate length looks more like an exponential distribution because the flatter part (ΔV_0) is narrower. Our model result is in good agreement with the simulation at these two lengths. In short, we have developed an analytical model for RTN amplitude distribution in a nanowire-like channel MOSFETs.

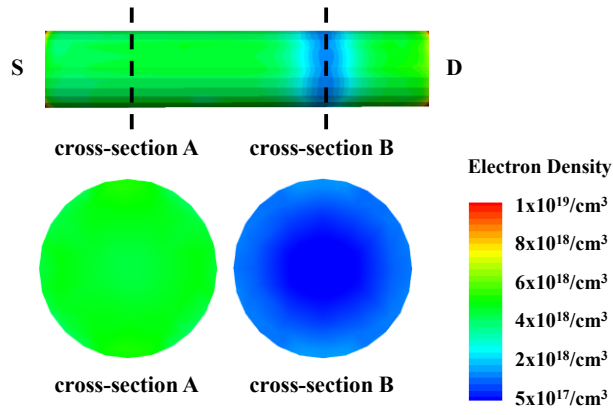
The model has only a few parameters, which can be extracted from a Monte Carlo simulation. For circuit simulation, these parameters can be treated as fitting parameters to match measurement results. Finally, we extracted RTN amplitude distributions from FinFET SONOS cells used in Chapter 5 (Fig. 5.15(a)). A Poisson-like shape is observed, as shown in Fig. 6.9.

6.5 Summary

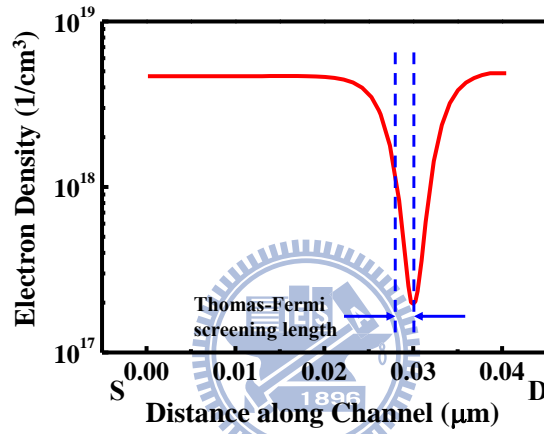
In a MOSFET with a nanowire-like channel, RTN amplitude fluctuations can no longer be explained by a current-path modulation effect. We perform a 1D channel Monte Carlo RTN simulation to investigate RTN behavior without the presence of such current-path modulation. Based on the simulation results in a large number of devices, we conclude that RTN amplitudes in a 1D channel device are dependent on the number of dopants nearby an RTN trap. According to the findings, we develop an analytical RTN amplitude distribution model for MOSFETs having a

one-dimension-like channel. Our model can fit the Monte Carlo RTN simulation results quite well for different doping concentrations and gate lengths.





(a)



(b)

Fig. 6.1 3D atomistic simulation of an electron concentration distribution in a cylindrical channel MOSFET. The diameter of the channel is 6nm. (a) Electron concentration distributions in two cross-sections, A and B. B has a dopant charge at the center and A does not have a dopant charge. (b) An electron density distribution along the channel. The Thomas-Fermi screening length ($[kT/4\pi n_e e^2]^{1/2}$) is shown in the figure.

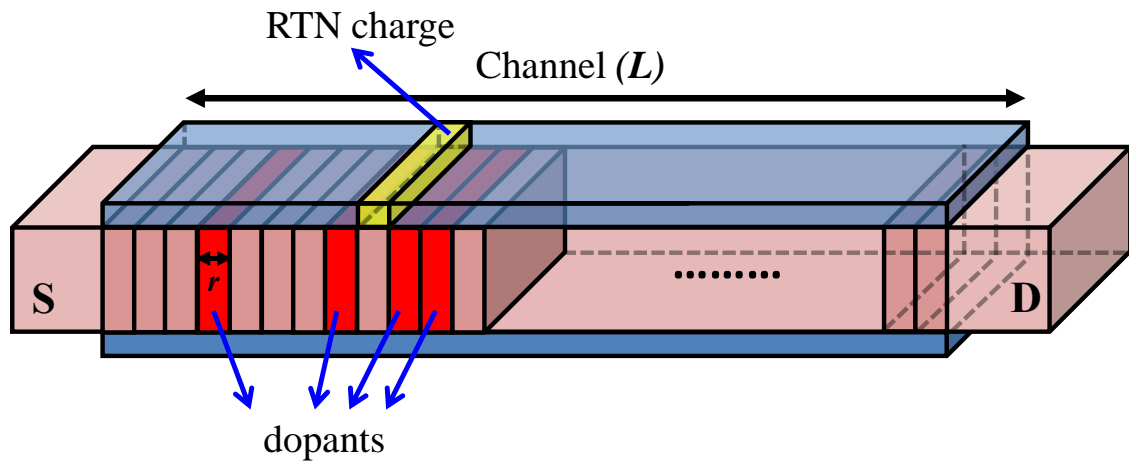
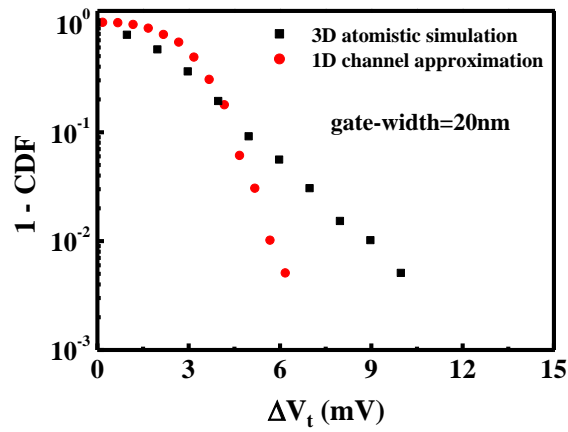
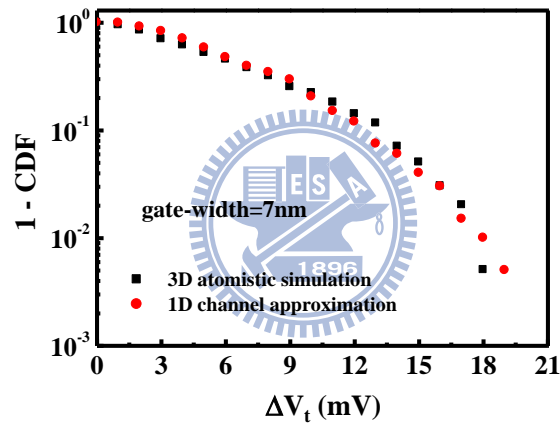


Fig. 6.2 Illustration of a one-dimensional channel RTN simulation scheme. The simulated MOSFET has a double gate structure. The channel is divided into many 1nm slices. In simulation, a dopant charge is placed uniformly in a slice and an RTN charge is placed in a 1nm bar on top of the channel.

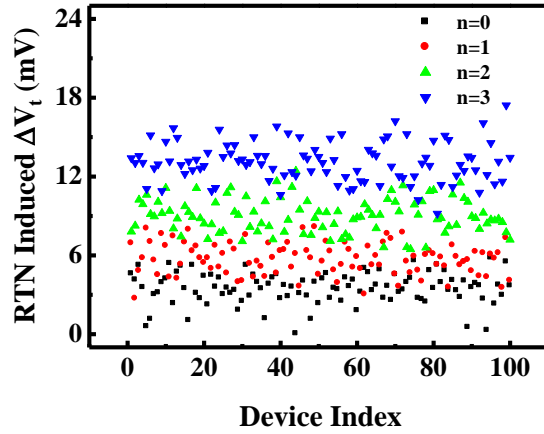


(a)

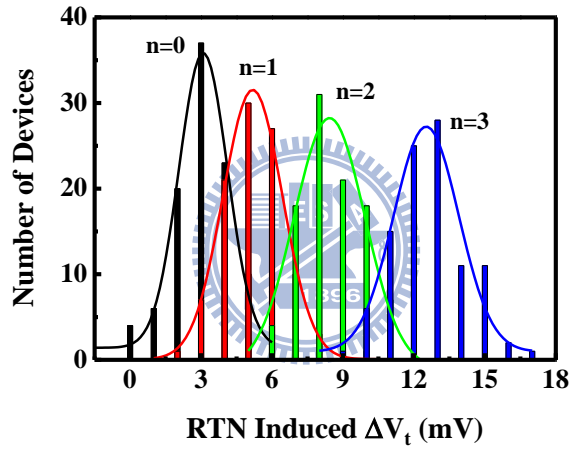


(b)

Fig. 6.3 Complementary cumulative distribution function (1-CDF) of RTN induced ΔV_t from a 3D atomistic simulation and from the 1D channel RTN simulation. The devices have a doping concentration of $1 \times 10^{19}/\text{cm}^3$ and a channel length of 40nm. The gate width is 20nm in (a) and 7nm in (b).



(a)



(b)

Fig. 6.4 1D channel Monte Carlo simulation of RTN induced ΔV_t . The channel length is 40nm and each device has 14 dopants. A dopant number in the RTN trap section (n) is equal to 0, 1, 2 and 3, respectively. For each n , we simulate 100 devices. (a) RTN induced V_t shifts in totally 400 devices. (b) The distribution of RTN induced ΔV_t for each n .

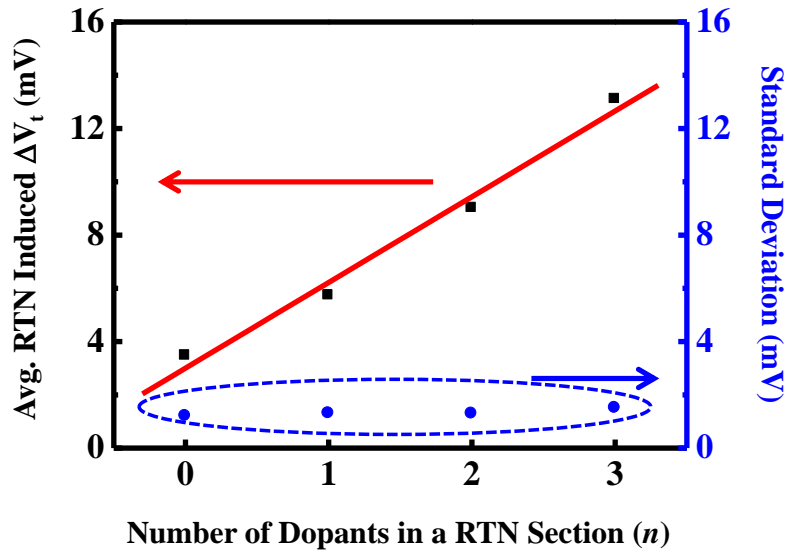


Fig. 6.5 Average RTN amplitude and a standard deviation versus a dopant number in an RTN trap section (n).



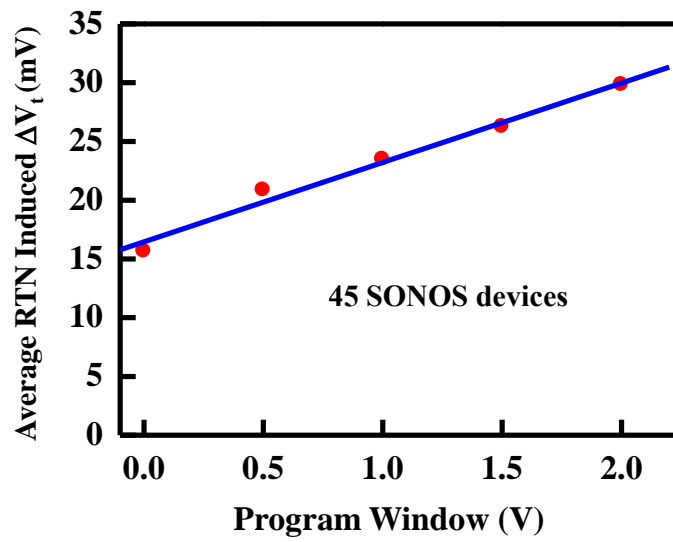


Fig. 6.6 Measured average RTN induced ΔV_t versus a CHE program window in 45 SONOS cells. A linear relationship between the ΔV_t and a program V_t window is obtained.

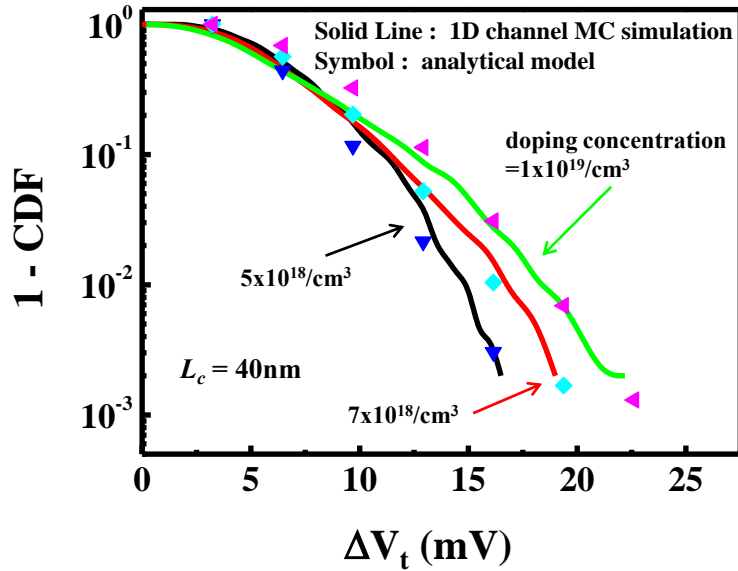


Fig. 6.7 Complementary cumulative distribution function of RTN induced ΔV_t from 1D channel Monte Carlo RTN simulation and from this analytical model. The doping concentration is $1 \times 10^{19}/\text{cm}^3$, $7 \times 10^{18}/\text{cm}^3$ and $5 \times 10^{18}/\text{cm}^3$ respectively. The gate length is 40nm.

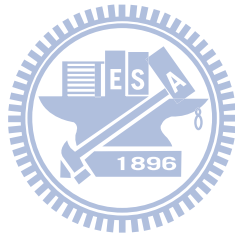
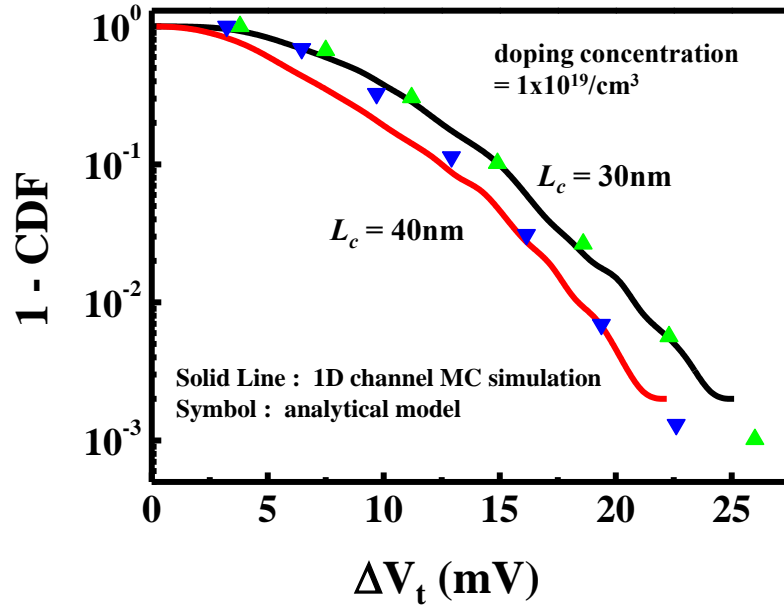


Fig. 6.8 Complementary cumulative distribution function of RTN induced ΔV_t from 1D channel Monte Carlo RTN simulation and from this analytical model for two different gate lengths, $L_c=30\text{nm}$ and 40nm . The doping concentration is $1 \times 10^{19} / \text{cm}^3$.

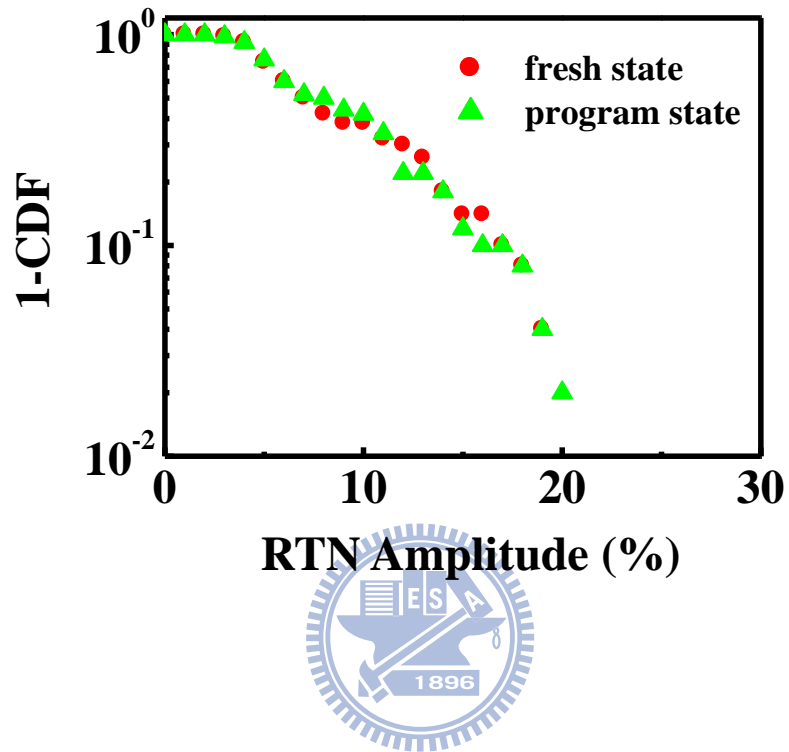


Fig. 6.9 Complementary cumulative distribution function of RTN amplitude distribution in FinFET SONOS cells with a fin width=10nm. A Poisson-like shape is obtained.

Chapter 7

Conclusions

In short, this dissertation has involved major reliability issues in high-k (HfSiON)/metal gate(TiN) pMOSFET, among them, NBTI and RTN are studied. Single charge phenomena are characterized statistically to get insight of threshold voltage shift distributions in small-area devices. The RTN in non-volatile flash memory cells and its structural dependence are also studied. Contributions of each subject in this work are summarized as follows.

First, we characterize NBTI trap creation in a large number of high-k dielectric pMOSFETs. The broad distribution of trap creation times is attributed to an activation energy distribution in the RD model. An activation energy distribution including a local electric field effect has been extracted from measured trap characteristic times. We develop a statistical model to simulate an NBTI induced ΔV_t distribution in small-area devices. Our model can reproduce the measurement results of an NBTI ΔV_t distribution and its stress time evolutions well.

Next, continued from the preceding paragraph, since ΔV_t recovers partly after a NBTI stress, we use a similar statistical approach as in Chapter 2 to exploring NBTI recovery mechanisms and trapped charge characteristics. Thermally-assisted trapped charge tunnel emission has been confirmed to be a major mechanism in NBTI recovery, which is proposed in our earlier papers [3.4]. We extract a trapped charge activation energy distribution in the ThAT model for the first time. We find that the emission time distribution of trapped charges broadens as a sequence number increases. This feature is successfully explained by the ThAT model and verified by

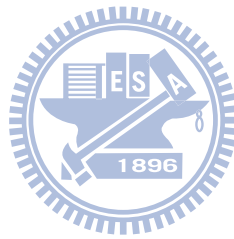
measurement. A Monte Carlo based statistical model for a post-NBTI ΔV_t distribution is developed for small area devices. Our model can predict a ΔV_t distribution and its temporal evolution in relaxation very well. In chapter 2 and 3, NBTI induced ΔV_t distributions are successfully characterized and predicted.

Then, single trapped charge induced Δv_t distributions in RTN and NBTI are characterized and simulated in pMOSFETs. Our simulation method takes into account a trap creation probability in NBTI stress. Our study shows that a NBTI stress created charge has a larger Δv_t distribution tail than RTN due to current path percolation effect. This large NBTI induced distribution tail poses to be a serious CMOS reliability concern and should be carefully considered in a precise NBTI lifetime model.

Furthermore, with respect to non-volatile flash memories, RTN induced Δv_t in FG and SONOS cells and its structural dependence are investigated. In a FG flash, RTN amplitudes are mainly determined by random dopant induced percolation effect and identical in erase and program states. However, in a planar MLC SONOS, we find that RTN amplitudes have a wide spread after program. The program-state RTN distribution is affected by both random program charges and substrate dopants. In addition, the RTN amplitude varies from P/E cycle to P/E cycle due to program induced percolation effect. Therefore the program charge effect has to be considered in RTN modeling in MLC SONOS. According to our experiments and simulations, the program charge induced percolation effect can be significantly reduced in a surrounding gate structure, such as a FinFET SONOS.

Finally, we discussed that RTN amplitude fluctuations in a MOSFET with a nanowire-like channel can no longer be explained by a current-path modulation effect. We perform a 1D channel Monte Carlo RTN simulation to investigate RTN behavior without the presence of such current-path modulation. Based on the simulation results

in a large number of devices, we conclude that RTN amplitudes in a 1D channel device are dependent on the number of dopants nearby an RTN trap. According to the findings, we develop an analytical RTN amplitude distribution model for MOSFETs having a one-dimension-like channel. Our model can fit the Monte Carlo RTN simulation results quite well for different doping concentrations and gate lengths. This model can also apply to SONOS flash memory cells since nitride program charges and substrate dopants have some similar features about channel current path percolation effect, as investigated in Chapter 5.



References

Chapter 1

- [1.1] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chuang, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5nm-gate nanowire FinFET," *Symp. on VLSI Tech.*, pp. 196-197, 2004.
- [1.2] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "FinFET scaling to 10nm gate length," *IEDM Tech. Dig.*, pp. 251-254, 2002.
- [1.3] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Elec. Dev. Lett.*, vol. 18, pp. 209-211, 1997.
- [1.4] J. Wang, and M. Lundstrom, "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?," *IEDM Tech. Dig.*, pp. 707-710, 2002.
- [1.5] H. Iwai, S. Ohmi, S. Akama, C. Ohshima, A. Kikuchi, I. Kashiwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama, and Y. Yoshihara, "Advanced gate dielectric materials for sub-100 nm CMOS," *IEDM Tech. Dig.*, pp. 625-628, 2002.
- [1.6] T. P. Ma, "Making silicon nitride film a viable gate dielectric," *IEEE Trans. on Elec. Dev.*, vol. 45, pp. 680-690, 1998.
- [1.7] T. Watanabe, M. Takayanagi, K. Kojima, K. Sekine, H. Yamasaki, K. Eguchi, K. Ishimaru, and H. Ishiuchi, "Impact of Hf concentration on performance

- and reliability for HfSiON-CMOSFET,” *IEDM Tech. Dig.*, pp. 507-510, 2004.
- [1.8] C. Choi, C. S. Kang, C. Y. Kang, R. Choi, H. J. Cho, Y. H. Kim, S. J. Rhee, M. Akbar, and J. C. Lee, “The effects on nitrogen and silicon profile on high-k MOSFET performance and bias temperature instability,” *Symp. on VLSI Tech.*, pp. 214-215, 2004.
- [1.9] H.C.-H. Wang, S.-J. Chen, M.-F. Wang, P.-Y. Tsai, C.-W. Tsai, T.-W. Wang, S.M. Ting, T.-H. Hou, P.-S. Lim, H.-J. Lin, Y. Jin, H.-J. Tao, S.-C. Chen, C.H. Diaz, M.-S. Liang, and C. Hu, “Low power device technology with SiGe channel, HfSiON, and poly-Si gate,” *IEDM Tech. Dig.*, pp. 161-164, 2004.
- [1.10] J. C. Lee, H. J. Cho, C. S. Kang, S. Rhee, Y. H. Kim, R. Choi, C. Y. Kang, C. Choi, and M. Abkar, “High-k dielectrics and MOSFET characteristics,” *IEDM Tech. Dig.*, pp. 95-98, 2003.
- [1.11] H.C.-H. Wang, C. W. Tsai, S. J. Chen, C. T. Chan, H. J. Lin, Y. Jin, H. J. Tao, S. C. Chen, C. H. Diaz, T. Ong, A. S. Oates, M. S. Liang, and M. H. Chi, “Reliability of HfSiON as gate dielectric for advanced CMOS technology,” *Symp. on VLSI Tech.*, pp.170-171, 2005.
- [1.12] T. Kauerauf, R. Degraeve, F. Crupi, B. Kaczer, G. Groeseneken, and H. Maes, “Trap generation and progressive wearout in thin HfSiON,” *Proc. Int. Reliab. Phys. Symp.*, pp. 45-49, 2005.
- [1.13] A. Shanware, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, H. Bu, M. J. Bevan, R. Khamankar, S. Aur, P. E. Nicollian, J. McPherson, and L. Colombo, “Evaluation of the positive bias temperature stress stability in HfSiON gate dielectrics,” *Proc. Int. Reliab. Phys. Symp.*, pp. 208-213, 2003.
- [1.14] K. O. Jeppson, and C. M. Svensson, “Negative Bias Stress of MOS Devices

- at High Electric Fields and Degradation of MNOS Devices,” *J. Appl. Phys.*, vol. 48, pp. 2004-2014, 1977.
- [1.15] M. A. Alam, and S. Mahapatra, “A Comprehensive Model of PMOS NBTI Degradation,” in *Microelectron. Reliab.*, vol. 45, pp. 71-81, 2005.
- [1.16] S. Ogawa, and N. Shiono, “Generalized Diffusion-Reaction Model for the Low-Field Charge Build up Instability at the Si-SiO₂ Interface,” *Phys. Rev. B*, vol. 51, pp. 4218-4230, 1995.
- [1.17] M. A. Alam, “A Critical Examination of the Mechanics of Dynamic NBTI for PMOSFETs,” in *IEDM Tech. Dig.*, pp. 345-348, 2003.
- [1.18] C. T. Chan, C. J. Tang, Tahui Wang, H. C.-H. Wang, and D. D. Tang, “Positive Bias and Temperature Stress Induced Two-Stage Drain Current Degradation in HfSiON nMOSFETs,” in *IEDM Tech. Dig.*, pp.571-574, 2005.
- [1.19] C. T. Chan, C. J. Tang, T. Wang, H. C. -H. Wang, and D. D. Tang, “Characteristics and Physical Mechanisms of Positive Bias and Temperature Stress-Induced Drain Current Degradation in HfSiON nMOSFETs,” *IEEE Trans. on Elec. Dev.*, vol. 53, pp. 1340-1346, 2006.
- [1.20] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichiger, P. Hehenberger, P.-J. Wagner, F. Schanovsky, J. Franco, M. T. Luque, and M. Nelhiebel, “The Paradigm Shift in Understanding the Bias Temperature Instability : From Reaction-Diffusion to Switching Oxide Traps,” *IEEE Trans. on Elec. Dev.*, vol. 58, pp. 3652-3665, 2011.
- [1.21] T. Grasser, B. Kaczer, and W. Goes, “An Energy Level Perspective of Bias Temperature Instability,” in *Proc. Int. Reliab. Phys. Symp.*, pp. 28-38, 2008.
- [1.22] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M.

- Nelhiebel, "A Two-stage Model for Negative Bias Temperature Instability," in *Proc. Int. Reliab. Phys. Symp.*, pp. 33-44, 2009.
- [1.23] T. Grasser, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, and B. Kaczer, "The Time Dependent Defect Spectroscopy (TDDS) Technique for the Bias Temperature Instability," in *Proc. Int. Reliab. Phys. Symp.*, pp. 16-25, 2010.
- [1.24] C. T. Chan, H. C. Ma, C. J. Tang, and T. Wang, "Investigation of Post-NBTI Stress Recovery in pMOSFETs by Direct Measurement of Single Oxide Charge De-Trapping," *Symp. on VLSI Tech.*, pp. 90-91, 2005.
- [1.25] B. Kaczer, V. Arkhipov, R. Degraeve, N. Collaert, G. Groeseneken, and M. Goodwin, "Disorder-Controlled-Kinetics Model for Negative Bias Temperature Instability and its Experimental Verification," in *Proc. Int. Reliab. Phys. Symp.*, pp. 381-387, 2005.
- [1.26] V. Huard, "Two independent components modeling for Negative Bias Temperature Instability," in *Proc. Int. Rel. Phys. Symp.*, pp.33-42, 2010.
- [1.27] S. Mahapatra, K. Ahmed, D. Varghese, A. E. Islam, G. Gupta, L. Madhav, D. Saha, and M.A. Alam, "On the Physical Mechanism of NBTI in Silicon Oxynitride p-MOSFETs: Can Difference in Insulator Processing Conditions Resolve the Interface Trap Generation versus Hole Trapping Controversy?," in *Proc. Int. Reliab. Phys. Symp.*, pp. 1-9, 2007.
- [1.28] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A. Alam, "Recent Issues in Negative Bias Temperature Instability: Initial Degradation, Field Dependence of Interface Trap Generation, Hole Trapping Effects and Relaxation," *IEEE Trans. on Elec. Dev.*, vol. 54, pp. 2143-2154, 2007.
- [1.29] S. Mahapatra, A. E. Islam, S. Deora, V. D. Maheta, K. Joshi, and M. A. Alam,

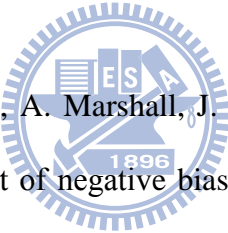
- “A Critical Re-evaluation of the Usefulness of R-D Framework in Predicting NBTI Stress and Recovery,” in *Proc. Int. Reliab. Phys. Symp.*, pp. 614-623, 2011.
- [1.30] M. H. Tsai, H. Muto, and T. P. Ma, “Random telegraph signals arising from fast interface states in metal-SiO₂-Si transistors,” *Appl. Phys. Lett.*, vol. 61, pp. 1691, Oct. 1992.
- [1.31] K. Kandiah, M. O. Deighton, and F. B. Whiting, “A physical model for random telegraph signal currents in semiconductor devices”, *J. Appl. Phys.*, vol.66, pp. 937, July 1989.
- [1.32] M. J. Kirton, and M. J. Uren, “Noise in solid state microstructure: A new perspective on individual defects, interface states, and low frequency noise,” *Adv. in Phys.*, vol. 38, pp. 367-468, 1989.
- [1.33] H. Muller, and M. Schulz, “Conductance modulation of submicrometer metal-oxide-semiconductor field-effect transistors by single electron trapping,” *J. Appl. Phys.*, vol. 79, no. 8, pp. 4178-4186, Apr. 1996.
- [1.34] N. Tega, H. Miki, Z. Ren, C. P. D’Emic, Y. Zhu, D. J. Frank, J. Cai, M. A. Guillorn, D.-G. Park, W. Haensch, and K. Torii, “Reduction of Random Telegraph Noise in High-k/ Metal-Gate Stacks for 22 nm Generation FETs,” in *IEDM Tech. Dig.*, pp. 771-774, 2009.
- [1.35] M. Tanizawa, S. Ohbayashi, T. Okagaki, K. Sonoda, E. Eikyu, Y. Hirano, K. Ishikawa, O. Tsuchiya, and Y. Inoue, “Application of a Statistical Compact Model for Random Telegraph Noise to Scaled-SRAM V_{min} Analysis,” *Symp. on VLSI Tech.*, pp. 95-96, 2010.
- [1.36] T. Grasser, H. Reisinger, W. Goes, Th. Aichinger, Ph. Hehenberger, P.-J. Wagner, M. Nelhiebel, J. Franco, and B. Kaczer, “Switching Oxide Traps as

- the Missing Link Between Negative Bias Temperature Instability and Random Telegraph Noise,” in *IEDM Tech. Dig.*, pp. 1-4, 2009.
- [1.37] N. Tega, H. Miki, T. Osabe, A. Kotabe, K. Otsuga, H. Kurata, S. Kamohara, K. Tokami, Y. Ikeda, and R. Yamada, “Anomalous Large Threshold Voltage Fluctuation by Complex Random Telegraph Signal in Floating Gate Flash Memory,” in *IEDM Tech. Dig.*, pp. 491-494, 2006.
- [1.38] P. Fantini, A. Ghetti, A. Marinoni, G. Ghidini, A. Visconti, and A. Marmiroli, “Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices,” *IEEE Electron Device Lett.*, Vol.28, pp. 1114-1116, 2007.
- [1.39] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya, “The Impact of Random Telegraph Signals on the Scaling of Multilevel Flash Memories,” in *VLSI Circuit Symp.*, pp. 112-113, 2006.
- [1.40] K. Fukuda, Y. Shimizu, K. Amemiya, M. Kamoshida, and C. Hu, “Random Telegraph Noise in Flash Memories-Model and Technology Scaling,” in *IEDM Tech. Dig.*, pp. 169-172, 2007.
- [1.41] A. S. Spinelli, C. M. Compagnoni, R. Gusmeroli, M. Ghidotti, and A. Visconti, “Investigation of the Random Telegraph Noise Instability in Scaled Flash Memory Arrays,” *Jpn. J. Appl. Phys.*, vol. 47, no. 4, pp. 2598-2601, 2008.
- [1.42] S. H. Gu, C. W. Li, Tahui Wang, W. P. Lu, K. C. Chen, Joseph Ku, and Chih-Yuan Lu, “Read Current Instability Arising from Random Telegraph Noise in Localized Storage, Multi-Level SONOS Flash Memory,” *IEDM Tech. Dig.*, pp. 487-490, 2006.
- [1.43] S. E. Rauch, “Review and Reexamination of Reliability Effects Related to

NBTI-Induced Statistical Variations,” *IEEE Trans. on Dev. Mater. Rel.*, vol. 7, no. 4, pp. 524-530, 2007.

- [1.44] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, “Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology,” *IEEE Trans. on Dev. Mater. Rel.*, vol. 7, no. 4, pp. 509-517, 2007.
- [1.45] R. Vattikonda, W. Wang, and Y. Cao, “Modeling and minimization of PMOS NBTI effect for robust nanometer design,” in *Proc. ACM/IEEE Des. Autom. Conf.*, pp. 1047-1052, 2006.

Chapter 2

- 
- [2.1] V. Reddy, A.T. Krishnan, A. Marshall, J. Rodriguez, S. Natarajan, T. Rost, and S. Krishnan, “Impact of negative bias temperature instability on digital circuit reliability,” in *Microelectron. Reliab.*, vol. 45, pp. 31-38, 2005.
- [2.2] W. Wang, S. Yang, S. Bhardwaj, R. Vattikonda, S. Vrudhula, F. Liu, and Y. Cao, “The impact of NBTI on the performance of combinational and sequential circuits,” in *Proc. DAC*, pp. 364-369, 2007.
- [2.3] M. Agostinelli, S. Lau, S. Pae, P. Marzolf, H. Muthali, and S. Jacobs, “PMOS NBTI-induced circuit mismatch in advanced technologies,” in *Microelectron. Reliab.*, vol. 46, pp. 63-68, 2006.
- [2.4] N. K. Jha, P. S. Reddy, D. K. Sharma, and V. R. Rao, “NBTI Degradation and Its Impact for Analog Circuit Reliability,” *IEEE Trans. on Elec. Dev.*, vol. 52, no. 12, pp. 2609-2615, 2005.
- [2.5] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, “Impact of NBTI on SRAM

- read stability and design for reliability,” in *Proc. Int. Symp. on Quality Elec. Design*, pp. 213-218, 2006.
- [2.6] G. La Rosa, W. L. Ng, S. Rauch, R. Wong, and J. Sudijono, “Impact of NBTI induced statistical variation to SRAM cell stability,” in *Proc. Int. Reliab. Phys. Symp.*, pp. 274-282, 2006.
- [2.7] B. Kaczer, T. Grasser, Ph. J. Roussel, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, “Origin of NBTI Variability in Deeply Scaled pFRTs,” in *Proc. Int. Reliab. Phys. Symp.*, pp. 26-32, 2010.
- [2.8] B. Kaczer, Ph. J. Roussel, and T. Grasser, “Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices — Application to NBTI,” *IEEE Elec. Dev. Lett.*, vol. 31, no. 5, pp. 411-413, 2010.
- [2.9] J. P. Chiu, Y. T. Chung, Tahui Wang, Min-Cheng Chen, C. Y. Lu, and K. F. Yu, “A Comparative Study of NBTI and RTN Amplitude Distributions in High-k Gate Dielectric pMOSFETs,” *IEEE Elec. Dev. Lett.*, vol. 33, no. 2, pp. 176-178, 2012.
- [2.10] M. Toledano-Luque, B. Kaczer, J. Franco, P. J. Roussel, T. Grasser, T. Y. Hoffmann, and G. Groeseneken, “From mean values to distributions of BTI lifetime of deeply scaled FETs through atomistic understanding of the degradation,” in *Symp. on VLSI Tech.*, pp. 152-153, 2011.
- [2.11] A. T. Krishnan, S. Chakravarthi, P. Nicollian, V. Reddy, and S. Krishnan, “Negative bias temperature instability mechanism: The role of molecular hydrogen,” *Appl. Phys. Lett.*, vol. 88, no. 15, p. 153518, 2006.
- [2.12] A. E. Islam and M. A. Alam, “Analyzing the distribution of threshold voltage

- degradation in nanoscale transistors by using reaction-diffusion and percolation theory”, *J. Comput. Electron*, vol. 10, no. 4, pp. 341-351, 2011.
- [2.13] Jung-Piao Chiu, Chi-Wei Li, and Tahui Wang, “Characterization and modeling of trap number and creation time distributions under negative-bias-temperature stress,” *Appl. Phys. Lett.*, vol. 101, no. 8, p. 082906, 2012.
- [2.14] J. P. Chiu, H. D. Hsieh, and Tahui Wang, “Statistical Characterization and Modeling of a ΔV_t Distribution and Its Temporal Evolutions in NBTI Recovery”, submitted to *IEEE Trans. Electron Devices*
- [2.15] S. Rangan, N. Mielke, and E. C. C. Yeh, “Universal Recovery Behavior of Negative Bias Temperature Instability,” in *IEDM Tech. Dig.*, pp.341-344, 2003.
- [2.16] A. Stesmans, “Dissociation kinetics of hydrogen-passivated Pb defects at the (111) Si/SiO₂ interface,” *Phys. Rev. B*, vol. 61, no. 12, pp. 8393-8403, 2000.

Chapter 3

- [3.1] T. Siddiqua and S. Gurumurthi, “Enhancing NBTI Recovery in SRAM Arrays through Recovery Boosting,” *IEEE Trans. on VLSI Systems*, pp. 616-629, 2012.
- [3.2] J. Shin, V. Zyuban, P. Bose and T. M. Pinkston, “A Proactive Wear-out Recovery Approach for Exploiting Micro-architectural Redundancy to Extend Cache SRAM Lifetime,” in *Proc. Int. Symp. Comput. Architecture*, pp. 353-362, 2008.
- [3.3] H. Kufluoglu, V. Reddy, A. Marshall, J. Krick, T. Ragheb, C. Cirba, A.

- Krishnan and C. Chancellor, "An Extensive and Improved Circuit Simulation Methodology for NBTI Recovery," in *Proc. Int. Reliab. Phys. Symp.*, pp. 670-675, 2010.
- [3.4] T. Wang, C. T. Chan, C. J. Tang, C. W. Tsai, H. C. -H. Wang, M. H. Chi and D. D. Tang, "A Novel Transient Characterization Technique to Investigate Trap Properties in HfSiON Gate Dielectric MOSFETs — From Single Electron Emission to PBTI Recovery Transient," *IEEE Trans. Electron Devices*, vol. 53, pp. 1073-1079, 2006.
- [3.5] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin and C. Schlunder, "Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultra-Fast Vt-Measurements", in *Proc. Int. Reliab. Phys. Symp.*, pp. 448-453, 2006.
- [3.6] M. Denais, A. Bravaix, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, Y. Rey-Tauriac, and N. Revil, "On-the-fly Characterization of NBTI in Ultra-thin Gate Oxide PMOSFETs" in *IEDM Tech. Dig.*, pp.109-112, 2004.
- [3.7] H. Y. Yu, Y. T. Hou, M. F. Li and D. -L. Kwong, "Hole Tunneling Current Through Oxynitride/Oxide Stack and the Stack Optimization for p-MOSFETs," *IEEE Electron Device Lett.*, vol. 23, pp. 285-287, 2002.
- [3.8] Y. T. Hou, M. F. Li, H. Y. Yu, Y. Jin and D. -L. Kwong, "Quantum Tunneling and Scalability of HfO₂ and HfAlO Gate Stacks," in *IEDM Tech. Dig.*, pp. 731-734, 2002.
- [3.9] ISE TCAD Manual Release 10.0, Integr. Syst. Eng., Zurich, Switzerland, 2004.
- [3.10] Z. Q. TEO, D. S. ANG and G. A. Du, "Observation of Two Gate Stress Voltage Dependence of NBTI Induced Threshold Voltage Shift of Ultra-thin

Oxynitride Gate P-MOSFET,” in Proc. Int. Reliab. Phys. Symp., pp. 1002-1004, 2009.

- [3.11] Y. Y. Liao, S. F. Horng, Y. W. Chang, T. C. Lu, K. C. Chen, T. Wang and C. Y. Lu, “Profiling of Nitride-Trap-Energy Distribution in SONOS Flash Memory by Using a Variable-Amplitude Low-Frequency Charge-Pumping Technique,” *IEEE Electron Device Lett.*, vol. 28, pp. 828-830, 2007.

Chapter 4

- [4.1] A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, “RTS Amplitudes in Decananometer MOSFETs: 3-D Simulation Study,” *IEEE Trans. Electron Devices*, vol. 50, no.3, pp. 839-845, Mar. 2003.
- [4.2] Monzio Compagnoni, Aurelio Mauri, Salvatore Maria Amoroso, Alessandro Maconi, Eugenio Greco, Alessandro S. Spinelli, and Andrea L. Lacaita, “Comprehensive Investigation of Statistical Effects in Nitride Memories—Part II: Scaling Analysis and Impact on Device Performance,” *IEEE Trans. Electron Devices*, pp. 2124-2131, 2010.
- [4.3] M. A. Alam, A. Krishnan, “NBTI: Process, Device and Circuit”, *Int. Reliability Phys. Symp. (IRPS)*, p.212, 2005 Tutorial.
- [4.4] Sanghoon Lee, Heung-Jae Cho, Younghwan Son, Dong Seup Lee, and Hyungcheol Shin, “Characterization of Oxide Traps Leading to RTN in High-k and Metal Gate MOSFETs,” in *IEDM Tech. Dig.*, pp. 1-4, 2009.
- [4.5] Huan-Chi Ma, You-Liang Chou, Jung-Piao Chiu, Yueh-Ting Chung, Tung-Yang Lin, Tahui Wang, Yuan-Peng Chao, Kuang-Chao Chen, Chih-Yuan Lu, “A Novel Random Telegraph Signal Method to Study

Program/Erase Charge Lateral Spread and Retention Loss in a SONOS Flash Memory,” *IEEE Trans. Electron Devices*, vol. 58, pp. 623-630, 2011.

- [4.6] S. M. Amoroso, L. Gerre, S. Markov, F. Adamu-Lema and A. Asenov, “Comprehensive statistical comparison of RTN and BTI in deeply scaled MOSFETs by means of 3D ‘atomistic’ simulation,” *European Solid State Device Res. Conf. (ESSDERC)*, pp. 109-112, 2012

Chapter 5

- [5.1] A. Ghetti, C. Monzio Compagnoni, F. Biancardi, A. L. Lacaita, S. Beltrami, L. Chiavarone, A.S. Spinelli, and A. Visconti, “Scaling trends for random telegraph noise in deca-nanometer Flash memories,” *IEDM Tech. Dig.*, pp. 835 - 838, 2008.
- [5.2] P. Hoel, S. Port and C. Stone Introduction to Probability Theory, Houghton Mifflin Co., 1977.

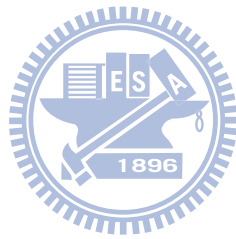
Chapter 6

- [6.1] C. Surya and T. Y. Hsiang, “Surface mobility fluctuations in metal-oxide-semiconductor field-effect transistors,” *Phys. Rev. B.*, vol. 35, pp. 6343-6347, 1987.
- [6.2] K. K. Hung, P. K. Ko, Chenming Hu and Yiu Chung Cheng, “Random Telegraph Noise of Deep-Submicrometer MOSFET’s,” *IEEE Elect. Dev. Lett.*, vol. 11, pp. 90-92, 1990.
- [6.3] Ming-Horn Tsai, T. P. Ma and Terence B. Hook, “Channel Length

- Dependence of Random Telegraph Signal in Sub-Micron MOSFET's," *IEEE Elect. Dev. Lett.*, vol. 15, pp. 504-506, 1994.
- [6.4] A. L. McWhorter, "1/f noise and germanium surface properties," in *Semiconductor Surface Physics*. Philadelphia, PA: Univ. Pennsylvania Press, pp. 207–228, 1957.
- [6.5] F. N. Hooge, "1/f noise," *Physica*, vol. 83B, pp. 14-23, 1976.
- [6.6] K. K. Hung, P. K. Ko, Chenming Hu and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol.37, no.3, pp. 654-665, 1990.
- [6.7] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs," *IEEE Trans. Electron Devices*, vol.50, no.9, pp. 1837-1852, 2003.
- [6.8] Yueh-Ting Chung, Tzu-I Huang, Chi-Wei Li, You-Liang Chou, Jung-Piao Chiu, Tahui Wang, M. Y. Lee, Kuang-Chao Chen and Chih-Yuan Lu, " V_t Retention Distribution Tail in a Multi-time Program MLC SONOS Memory Due to a Random Program Charge Induced Current Path Percolation Effect," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1371-1376, 2012.
- [6.9] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulation study," *IEEE Trans. Electron Devices*, vol.45, no.12, pp.2505-2513, 1998.
- [6.10] K. R. Lakshmikumar, R. A. Hadaway and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analogue design," *IEEE J. Solid State Circuits*, vol. SC-21, pp. 1057–1066, 1986.
- [6.11] K. Takeuchi, T. Tatsumi and A. Furukawa, "Channel engineering for the

- reduction of random-dopant-placement-induced threshold voltage fluctuations,” in *IEDM Tech. Dig.*, pp. 841-844, 1997.
- [6.12] Peter A. Stolk, Frans P. Widdershoven and D. B. M. Klaassen, “Modeling Statistical Dopant Fluctuations in MOS Transistors,” *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1960-1971, 1998.
- [6.13] K. Sonoda, K. Ishikawa, T. Eimori and O. Tsuchiya, “Discrete Dopant Effects on Statistical Variation of Random Telegraph Signal Magnitude,” *IEEE Trans. Electron Devices*, vol.54, no.8, pp.1918-1925, 2007.
- [6.14] Yiming Li, Shao-Ming Yu, Jiunn-Ren Hwang and Fu-Liang Yang, “Discrete Dopant Fluctuations in 20-nm/15-nm-Gate Planar CMOS,” *IEEE Trans. Electron Devices*, vol.55, no.6, pp. 1449-1455, 2008.
- [6.15] Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chenming Hu, “Sub 50-nm FinFET: PMOS,” in *IEDM Tech. Dig.*, pp. 67-70, 1999.
- [6.16] Ming Li, Kyoung Hwan Yeo, Sung Dae Suk, Yun Young Yeoh, Dong-Won Kim, Tae Young Chung, Kyung Seok Oh and Won-Seong Lee, “Sub-10 nm Gate-All-Around CMOS Nanowire Transistors on Bulk Si Substrate,” *Int. Symp. on VLSI Tech. (VLSI)*, pp. 94-95, 2009.
- [6.17] Kyoung Hwan Yeo, Sung Dae Suk, Ming Li, Yun-young Yeoh, Keun Hwi Cho, Ki-Ha Hong, SeongKyu Yun, Mong Sup Lee, Nammyun Cho, Kwanheum Lee, Duhyun Hwang, Bokkyoung Park, Dong-Won Kim, Donggun Park and Byung-Il Ryu, “Gate-All-Around (GAA) Twin Silicon Nanowire MOSFET (TSNWFET) with 15 nm Length Gate and 4 nm Radius Nanowires,” in *IEDM Tech. Dig.*, pp. 539-542, 2006.

- [6.18] J.-N. Chazalviel, “Coulomb Screening by Mobile Charges: Applications to Material Science, Chemistry and Biology,” pp. 15-19, 1999.



學經歷表 Vita

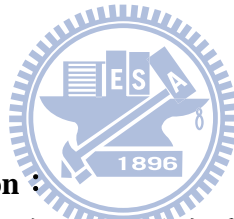
姓名/Name : 邱榮標 Jung-Piao Chiu 性別/Sex : 男 Male
生日/DOB : 1985/10/13 籍貫 : 高雄市

學歷/Education :

市立高雄高級中學	2000.09-2003.06
National Tainan First Senior High School	
國立交通大學電子工程學系	2003.09-2007.06
Department of Electronics Engineering, NCTU	
國立交通大學電子工程研究所博士班	2007.09-2013.02
Ph.D. Program, Department of Electronics Engineering, NCTU	

經歷/Experience :

半導體元件物理助教、固態物理助教
TA of Semiconductor Physics and Devices and TA of Solid-State Physics
台積電兼任工程師
Part-time engineer in TSMC



博士論文題目/Ph.D. Dissertation :

先進互補式金氧半電晶體及快閃式記憶元件中單一電荷效應之統計性研究
Statistical Study of Single Charge Phenomena in Advanced CMOS and Flash Memory

Publication List

(a) Journal Papers

- (1) **Jung-Piao Chiu**, Yu-Heng Liu, Hung-Da Hsieh, Chi-Wei Li, Min-Cheng Chen and Tahui Wang, "Statistical Characterization and Modeling of the Temporal Evolutions of ΔV_t Distribution in NBTI Recovery in Nanometer MOSFETs," to be published in *IEEE Trans. on Elect. Dev.*, 2013.
- (2) **J.P. Chiu**, C.W. Li and Tahui Wang, "Characterization and modeling of trap number and creation time distributions under negative-bias-temperature stress," *Applied Phys. Lett.*, Vol.101, 082906, 2012.
- (3) Y.T. Chung, T.I. Huang, C.W. Li, Y.L. Chou, **J.P. Chiu**, Tahui Wang, M.Y. Lee, K.C. Chen, C.Y. Lu, " V_t Retention Distribution Tail in a Multi-Time-Program MLC SONOS Memory due to a Random Program Charge Induced Current-Path Percolation Effect," *IEEE Trans. on Elect. Dev.*, Vol. 59, pp. 1371-1376, 2012.
- (4) **J.P. Chiu**, Y.T. Chung, Tahui Wang, M.C. Chen, C.Y. Lu, and K.F. Yu, "A Comparative Study of NBTI and RTN Amplitude Distributions in Hgh-k Gate Dielectric pMOSFETs", *IEEE Elect. Dev. Lett.*, Vol. 33, pp.176-178, 2012.
- (5) H.C. Ma, Y.L. Chou, **J.P. Chiu**, Y. T. Chung, T. Y. Lin, Tahui Wang, Y.P. Chao, K.C. Chen, and Chih-Yuan Lu, "A Novel Random Telegraph Signal Method to Study Program/Erase Charge Lateral Spread and Retention Loss in a SONOS Flash Memory", *IEEE Trans. on Elect. Dev.*, Vol. 58, pp. 623-630, 2011.
- (6) H.C. Ma, Y.L. Chou, **J.P. Chiu**, Tahui Wang, S.H. Ku, N.K. Zou, Vincent Chen, W.P. Lu, K.C. Chen, and Chih-Yuan Lu, "Program Trapped Charge Effect on Random Telegraph Noise Amplitude in a Planar SONOS Flash Memory Cell," *IEEE Elect. Dev. Lett.*, vol. 30, pp.1188-1190, 2009.

(b) Conference Papers

- (7) Y.L. Chou, **J.P. Chiu**, H.C. Ma, Tahui Wang, Y.P. Chao, K.C. Chen, and Chih-Yuan Lu "Use of Random Telegraph Signal as Internal Probe to Study Program/Erase Charge Lateral Spread in a SONOS

- Flash Memory” *Int. Reliability Phys. Symp. (IRPS)*, pp.960-963, 2010.
- (8) **J.P. Chiu**, Y.L. Chou, H.C. Ma, Tahui Wang, S.H. Ku, N.K. Zou, Vincent Chen, W.P. Lu, K.C. Chen, and Chih-Yuan Lu, “Program Charge Effect on Random Telegraph Noise Amplitude and Its Device Structural Dependence in SONOS Flash Memory,” *IEEE International Electron Device Meeting (IEDM)*, pp.843-846, 2009.
- (9) H.C. Ma, **J.P. Chiu**, C.J. Tang and Tahui Wang, “Investigation of Post-NBT Stress Current Instability Modes in HfSiON Gate Dielectric pMOSFETs by Measurement of Individual Trapped Charge Emissions,” *Int. Reliability Phys. Symp. (IRPS)*, Montreal, Canada, pp.51-54, 2009.

著作總點數： 11 (依新法記點)

