國立交通大學

電控工程研究所

碩　士　論　文

具負載適應增益調適混合信號控制之邊界模式功率因數修正交-直流轉換器

Design of a Load Adaptive Gain Adjustment Mixed-Signal Critical Mode PFC AC-DC Converter

研 究 生：詹茗皓

指導教授：鄒應嶼 博士

中華民國　九十八　年　十　月

具負載適應增益調適混合信號控制之邊界模式功率因數修正交-直流轉換器

Design of a Load Adaptive Gain Adjustment Mixed-Signal Critical Mode PFC AC-DC Converter

研 究 生：詹茗皓　　Student: Ming-Hao Chan

指導教授：鄒應嶼 博士　Advisor: Dr. Ying-Yu Tzou

國立交通大學

電控工程研究所

碩士論文

A Thesis

Submitted to Institute of Electrical and Control Engineering

College of Electrical Engineering

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master

in

Electrical Engineering

October 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年十月

具負載適應增益調適混合信號控制之邊界模式功率因數修正交-直流轉換器

研究生：詹茗皓　　指導教授：鄒應嶼 博士

國立交通大學電控工程研究所

中文摘要

本論文研製具負載適應增益調適混合信號控制之邊界模式功率因數修正(critical-mode power-factor-correction, CRM PFC)交-直流轉換器，可應用於中低功率電子設備如:可攜式電子產品或照明設備。本文所研製的混合信號控制其中電流迴路使用類比方式實現，電壓迴路則以數位方式實現。本文並提出負載適應增益調適(load adaptive gain adjustment)以及帶拒濾波器(notch filter)於數位電壓迴路，使系統輸出電壓可達到最佳動態特性且仍可使輸入電流具備低總諧波失真(total-harmonic-distortion, THD)以及高功率因數(power-factor, PF)。在類比電流迴路中，類比電流比較器為抑制雜訊的影響會加入磁滯比較區間 (hysteresis band)，但是磁滯比較區間過大會導致系統輸入線電流失真；另外，由於交-直流轉換器中開關以及二極體的寄生效應使得在切換過程會產生高頻振盪，因此零電流偵測比較器的參考電壓大小會影響開關導通時刻，進而影響輸入電流的諧波失真，因此本論文針對磁滯比較區間以及參考電壓大小對於輸入電流諧波失真的影響進行分析，並選取適當的磁滯比較區間及參考電壓值以符合輸入電流規範。在數位電壓迴路中，類比數位轉換器(analog-to-digital converter, ADC)以及數位類比轉換器(digital-to-analog converter, DAC)量化效應會使電流命令波形失真，而進一步使輸入電流波形失真，因此本論文分析如何選取適當的取樣率(sampling rate)以及位元長度(bit length)。交-直流轉換器為了使輸入線電流不受市電兩倍頻漣波的影響，因而限制輸出電壓暫態響應速度，本論文加入帶拒濾波器於電壓迴路，濾除兩倍線頻，以提升系統的動態響應並且使線電流不受輸出電壓漣波的影響。由於在不同負載情況下，系統的動態特性也隨之變動，本論文提出負載適應增益調適機制，根據不同負載狀況，適時修正電壓控制器參數，使系統輸出動態響應於不同負載狀況

下皆能維持穩定且快速的動態響應。本論文使用電路模擬軟體 PSIM 驗證所提出控制架構，在實驗驗證方面使用德州儀器 (Texas Instrument, TI)推出之數位信號處理器 DSP(TMS320LF2407)實現數位電壓迴路，而類比電流迴路則以意法半導體(STMicroelectronis)推出的 CRM PFC IC L6561 實現。由模擬及實驗結果相互驗證本論文所提之控制架構；加入帶拒濾波器，當頻寬提昇至 30 Hz 時，輸入線電流的總諧波失真在滿載狀況下仍可維持在 6 %；而負載適應增益調適機制，使得在輕載或重載情況下，進行相同負載變化量的切載測試，其動態響應速度以及穩定度皆相同，因此可顯示此控制架構的可行性及有效性。

Design of a Load Adaptive Gain Adjustment Mixed-Signal Critical Mode PFC AC-DC Converter

Student: Ming-Hao Chan Advisor: Dr. Ying-Yu Tzou

Institute of Electrical and Control Engineering
National Chiao Tung University

Abstract

This thesis develops a mixed-signal critical mode power-factor-correction (PFC) AC-DC converter with load adaptive gain scheduling. The peak current mode control is applied and analyzed by using the analog circuit. The voltage control loop is implemented in digital approach by using a digital notch filter and load adaptive gain adjustment to optimize the dynamic responses and maintain high power-factor (PF) with low total-harmonic-distortion (THD) in line current.

This thesis analyzes the effect of the hysteresis band effect of the analog current comparator and the effect of the reference voltage in zero current detecting comparator on current command. In digital voltage loop, the proper quantization resolutions of both analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are analyzed and determined. The digital voltage controller uses a digital notch filter to achieve fast dynamic response and still maintain low THD with high PF. An adaptive gain sheduling is applied for achieving the optimal dynamic response of the output voltage at different load variation conditions. The proposed mixed-signal PFC AC-DC converter with load adaptive gain scheduling has been verified by using computer simulation software (PSIM). This thesis uses the DSP EVM board TMS320LF2407 from Texas Instrument and the CRM PFC IC L6561 from STMicroelectronics to implement the experimental verification. The simulation and experimental results can verify the viability and effectiveness of the proposed control architecture.

誌　謝

首先我要特別感謝我的老師鄒應嶼教授這兩年來的悉心指導，除了提供一個完善的研究環境外，也讓我參與許多重要的研究計畫，也因此我才能夠在研究過程中學習到許多正確的做事觀念與方法；而在每一次的研究討論中，總是能夠仔細地分析問題，提出一些新穎的想法；在老師耐心的教導與鼓勵下，本論文才能如此順利地完成。感謝諸位口試委員：李迪章教授與蔡明發助理教授在口試時所給予的寶貴建議。

感謝育宗學長不吝傳授知識與經驗，讓我獲益良多。感謝昔日的同窗夥伴袈瀚、超哥、宗翰、哲瑋與家豪相互扶持與鼓勵。感謝學弟王仔、康康、甫尊、小江、智偉與小賴，因為你們的加入，讓實驗室充滿了朝氣與歡笑，豐富了我的研究生活；也希望將來大家在社會上都能夠很有成就，同時不要忘記我們永遠都是實驗室的夥伴。感謝月貴與思穎，在一些瑣碎的行政事務上的協助。

特別感謝家人能夠體諒我忙碌的研究生活，一路陪伴在我左右；在我遇到挫折或失意時能夠給予我最真誠的關懷與鼓舞，讓我能夠堅持我的理想；同時在我快樂時，也能夠與我一同分享成功時的喜悅。

僅以此論文獻給所有關心我的長輩、親戚與朋友…

詹茗皓

2009秋天 於新竹交大

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction

1.1 Research Background and Recent Development

Power supplies for the portable and lighting equipments have become more and more important in daily life. It is well known that power supplies connected to AC line introduced harmonic components to the input line current. The harmonic components cause several problems such as heating, voltage distortion, radiated and conducted noises which will reduce the capability of the mains. And so on, high quality electricity is required and hence the power factor (PF) of electrical application has to be improved. The solutions are referred to power-factor-correction (PFC) techniques which are applied for the front-end of the electric equipments.

The main purposes for the PFC AC-DC converter enforced the input line current to be sinusoidal and in phase with the input line voltage. According to different control topologies, the general approaches, which implement PFC controllers, can be classified into two methods: one is passive approach and the other one is active approach. Traditionally, a full bridge rectifier with passive components is used as AC-DC converter, but the nonlinear line current characteristic will produce significantly harmonic distortions to induce the lower PF. The higher peak value of line current will introduce larger power losses either. In active PFC approaches, PWM converter is employed to overcome the drawback of lower PF in the passive method. The active PFC topologies are composed by energy storage devices, power switch, and the feedback control loop circuit, which enhances the current command changing to follow the variation of output voltage and inductor current.

Recently, active PFC approaches are used in many kinds of fields. According to different operating modes of inductor current, there are continuous-conduction-mode (CCM) PFC and discontinuous-conduction-mode (DCM) PFC. In CCM PFC, the inductor current ripple is usually small enough, so that the line current total-harmonic-distortion (THD) can be reduced as small as possible. In generally, the CCM PFC techniques are widely applied for the applications above 250 W to 10 kW. When the power level is under 250 W, the DCM PFC techniques are widely applied for decreasing the inductor size. Moreover, the control architecture of DCM PFC can be simplified because of the ability of self current following. Among the techniques of DCM PFC, the critical-conduction-mode (CRM) PFC is the most popular solution for low power applications due to the current ripple is only twice of the average current to reduce the cost of the devices in power stages [1]-[4].

There are mainly two traditional approaches, which can be classified by control architectures: the multiplier approach and the voltage-follower approach. The multiplier approach uses a multiplier to generate the shape of the current command. The current operating mode is usually in CCM or in CRM. Although the multiplier has good performance, the control loop is more complicated for design as well. The multiplier accuracy and input range will significantly influence the system performance. There are mainly three current control methods, which are using the multiplier approach: average current control, peak current control, and hysteresis current control [5], [6].

The voltage-follower scheme is simpler than multiplier scheme. Because the current operating mode of voltage-follower method is in DCM or CRM conditions, the components in the power stage have to suffer large variations of voltage and current.

Whatever the multiplier approach or the voltage-follower approach has their own advantages in different applications. Table 1.1 shows the commercial PFC ICs which are generally used.

TABLE 1.1
GENERALLY USED COMMERCIAL PFC ICS IN INDUSTRY

Manufacturer	CRM PFC	CCM PFC
Infineon	TDA4862, TDA4863	ICE1PCS01
ST Microelectronics	L6561, L6562	L4981
Fairchild	FAN7527	FAN4800
Texas Instruments	MC33262, MC34262	UC3854, UCC3817
International Rectifier		IR1150S

Although the product life span of telecom equipment will evolve within 18 to 24 months [21], the power supply technology is not developing so quickly. Reusing the previous design could be cost more efficiency. Therefore, developing the products by reusing the power supply product should make flexibility a must. Up until the last couple of years, digital controller has gradually become important for PFC controller due to the communication ability, flexibility, and capability in implementation of nonlinear control. With the advances of the IC industry, it is possible to select a capable and cost effective digital signal processor (DSP). The selection of the DSP may depend more on availability of special on-chip hardware features such as analog-to-digital converters (ADC) and digital-to-analog converters (DAC). The trade-off of PFC controller exists between cost and system performance. Consequently, the issue of cost effectiveness is always the goal of academic research and companies.

1.2 RESEARCH MOTIVATION AND PURPOSE

In recent years, the requirements of power supplies grow up quickly. Hence the quality of the power electronic equipments is concerned. Worse power quality will bring many problems such as large harmonics of line current, power pollution, and low efficiency in power transmission. And so on, a large amount of countries have developed relevant laws and regulations for electrical and electric equipment such as EN61000-3-2. These standards can force the equipment products to meet the regulations. Therefore, there are some orientations

to improve the electronic power quality and efficiency.

With the fast evolution of portable commercial electronic equipments, the further requirements of PFC controllers in power system must be more intelligent to adopt the wide range of applications. Therefore, the flexibility of digital controller is noticed.

The analog approach has some deficiencies when compared to the digital control solution: Need to be tuned to each power level. It can not be programmable and hence certainly can not be altered in different applications. Require a relatively large number of extra components (resistors, capacitors etc.). Due to the influence of the thermal effect on power system reduces the life time of analog approach. Analog circuits suffer the disturbance of noise. Therefore, the digital approach is applied for overcoming those drawbacks of analog solutions. The digital approach suffers from the sampling rate and quantization error. The analog approach is more accurate due to avoid the effects of sampling errors, bit resolutions, and computation delays. And so on, combining merits of both analog approach and digital solution is an optimal solution of PFC controllers for electrical techniques [8]-[11].

1.3 THE RESEARCH METHODS AND SYSTEM OVERVIEW

The thesis focuses on the low power consumptive applications, such as portable tools and lighting equipments. The critical conduction mode which is at the boundary of CCM and DCM is more appropriate than DCM PFC in these applications. DCM has higher peak inductor current comparing to CRM in the same average line current. Hence, CRM is generally preferred in low power applications due to the lower maximum current stress in power components, zero-current turn-on, and smaller storage component for example inductance.

The CRM PFC is a variable switching frequency system and its' maximum value is occurs at the zero crossing of rectified line voltage. If the digital controller is applied for the

current control loop of CRM PFC, it needs extremely large sampling rate to detect the correct peak position of inductor current and then comparing with the current command. The large sampling rate not only introduces significantly power losses but also increases the cost. It stands to reason that the thesis applies analog approach for the current control loop of CRM PFC.

On the other hand, the bandwidth of the voltage control loop has to be low enough to reduce the effect of output voltage ripple. Since the analog approach applies for the inner current loop, the digital solution takes care of the outer voltage loop, which does not require fast clock to implement. The load adaptive gain scheduling can be simply developed by the digital method either. Therefore, the proposed control architecture can be implemented simply and inexpensively. Fig. 1.1 shows the block diagram of the proposed mixed-signal CRM PFC AC-DC converter.

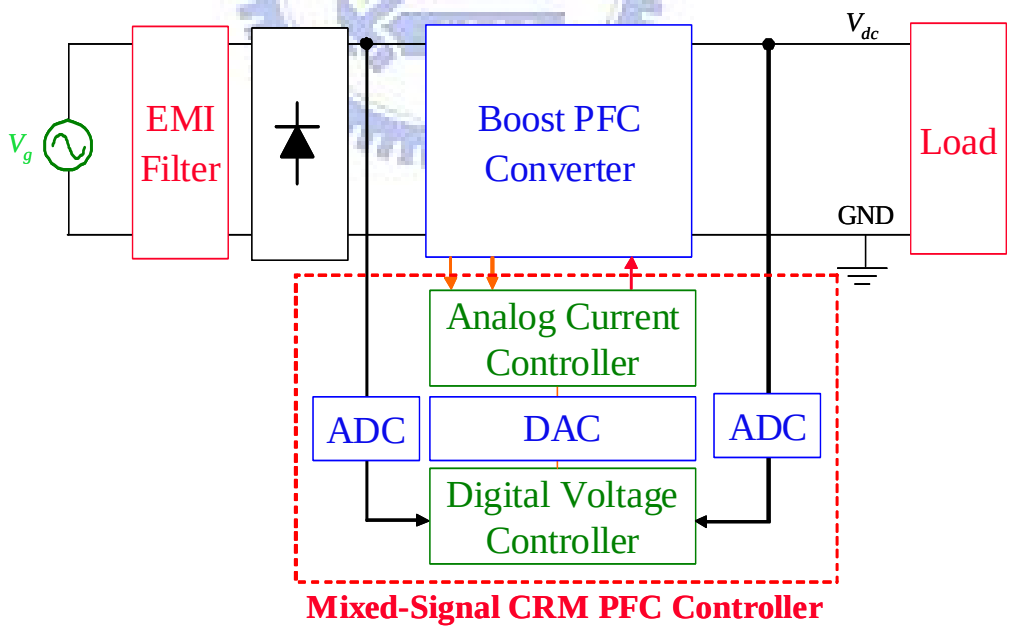


Fig. 1.1. The block diagram of purposed mixed-signal CRM PFC AC-DC converter.

1.4 THESIS ORGANIZATION

The thesis is organized as follows:

Chapter 1 introduces the research background, overview the different PFC control topologies, and the motivation of this thesis. The advantages of mixed-signal CRM PFC controller are described.

Chapter 2 gives the different structure and the steady state analysis of the CRM PFC boost converter. The ways to select the storage components and the power consumptions on each component are given.

Chapter 3 focuses on the analysis and design of the sub-circuits, such as current comparator, bit resolutions and sampling rates of ADC, and bit resolutions of DAC, of mixed-signal CRM PFC controller. And so on, the specifications of this mixed-signal CRM PFC controller can be decided.

Chapter 4 models the control-to-output circuit of mixed-signal CRM PFC by average method. Then the dynamic response is analyzed and the digital voltage controller can be designed by the average small signal model.

Chapter 5 is implemented the mixed-signal CRM PFC by DSP EVM board, TMS320LF2407A, from Texas Instrument (TI) and the analog CRM control IC, L6561, from STMicroelectronics. The experimental results can be shown and analyzed by circuit simulation software (PSIM).

In chapter 6, some concluding is summarized.

Chapter 2

Analysis of CRM PFC AC-DC Converter

2.1 Fundamental Principles of PF

Improving PF has a lot of advantages such as increasing power usage efficiency, reducing power line capacity, dropping peak line current, and decreasing the power line pollution [7]. Therefore, many nations have formulated some standards for electrical and electronic equipment. In AC network, the power factor (PF) is defined as the ratio of real power to apparent power which can be written as

$$PF = \frac{\text{Real Power}}{\text{Apparent Power}} = \frac{P}{S}. \tag{2-1}$$

Let $v_{in}(t)$ is sinusoidal line voltage and $i_g(t)$ is sinusoidal line current with the line period T_{line}, the root-mean-square (RMS) values of $v_g(t)$ and $i_g(t)$ can be defined as follow

$$V_{g,rms} = \sqrt{\frac{1}{T_s} \cdot \int_0^{T_s} v_g{}^2(t)dt}, \tag{2-2}$$

$$I_{g,rms} = \sqrt{\frac{1}{T_s} \cdot \int_0^{T_s} i_g{}^2(t)dt}. \tag{2-3}$$

(2-1) can be rewritten as

$$PF = \frac{\frac{1}{T_s} \cdot \int_0^{T_s} v_g(t) \cdot i_g(t)dt}{V_{g,rms} \cdot I_{g,rms}}. \tag{2-4}$$

Lower power factor means the power plants have to supply more and more energy to

maintain the same electronic equipment operating. The Fourier series of sinusoidal line current with high order harmonic distortions ($i_g(t)$) can be expressed as

$$i_g(t) = \sqrt{2} \cdot I_{g1} \cdot \sin(\omega_1 t - \theta_1) + \sum_{k=2}^{\infty} \sqrt{2} \cdot I_{gk} \cdot \sin(\omega_k t - \theta_k) \tag{2-5}$$

where I_{g1} is the line current fundamental component, I_{gk} means the k^{th} order component of line current, ω_1 is the fundamental frequency, θ_1 is the phase angle between line voltage and line current fundamental component, and ω_k is the k^{th} order frequency. Because the real power is only concerned with the fundamental harmonic part of line current, as shown in Fig. 2.1, the real power can be presented as

$$P = V_{g,rms} \cdot I_{g1} \cdot \cos\theta_1 \tag{2-6}$$

where $\cos\theta_1$ is displacement power factor (DPF). According to (2-4), the PF can be revised as

$$PF = \frac{I_{g1}}{I_{g,rms}} \cdot \cos\theta_1 \tag{2-7}$$

where I_{g1} quoition $I_{g,rms}$ is the ditortion factor (DF). To concern the influence of high order harmonic of line current, we define the total harmonic distortion (THD) as

$$THD = \frac{\sqrt{I_{g,rms}^{\ 2} - I_{g1}^{\ 2}}}{I_{g1}} = \frac{\sqrt{\sum_{k=2}^{\infty} I_{gk}^{\ 2}}}{I_{g1}} \tag{2-8}$$

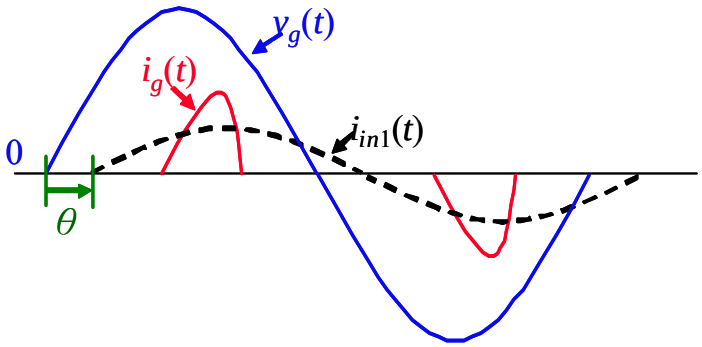


Fig. 2.1. Relationships between line voltage, line current and its fundamental harmonic.

Then the relationship between THD and DF can be given as

$$\mathrm{DF} = \frac{1}{\sqrt{1+(THD)^2}} \tag{2-9}$$

and the relationship between PF and THD is

$$PF = \frac{1}{\sqrt{1+(THD)^2}} \cdot DPF \tag{2-10}$$

Consequently, PF can be improved by controlling the line current to shape to line voltage and hence the high order harmonics of line current can be reduced. Therefore, low THD and high PF are achieved.

2.2 Introduction of CRM PFC Control Architecture

CRM PFC AC-DC converter has the features of zero current turn on and smaller components size, the inductor current peak is the double of line current peak. Therefore CRM PFC is popular for low power applications which are usually under 250 W. Advantages and disadvantages of CRM PFC method are shown in Table 2.1.

CRM PFC AC-DC converter schemes have two main architectures. One uses a multiplier for generating a current command which is proportional to the rectified line voltage, as shown in Fig. 2.2. The operating principle is shown in Fig 2.3. The switch, Q, is turned off when the sensed switching current achieves the current command, $V_{multout}$, and turned on when the inductor current reaches zero. Due to the control method, the on-time of switch will be a constant value. Then, the line current will trace to the line voltage as shown in (2-11). Therefore, higher power factor and lower harmonic distortion will be ensured. Some commercial CRM control ICs are such as L6561 from STMicroelectronics, TDA4863 from Infineon, MC33262 from ON Semiconductor, UCC28050 from Texas Instruments etc [32].

$$t_{on} = L \cdot \frac{I_{L,pk}(t)}{V_{in}(t)} \tag{2-11}$$

TABLE 2.1

ADVANTAGE AND DISADVANTAGES OF THE CRITICAL MODE PFC

Advantage	Disadvantage
- *Simple Control Scheme:* No need current controller, few external components - *Ease of Stabilization:* No need compensation ramp - *Zero Current Turn On:* Reduce the switching loss - *Current Protection:* Current sensing limits the maximum current	- *Variable Switching Frequency:* Grave EMI disturbance - *High Components Tolerance:* The larger current peak value induces more expensive components. - *Zero-Crossing Distortion:* Largest switching frequency and duty

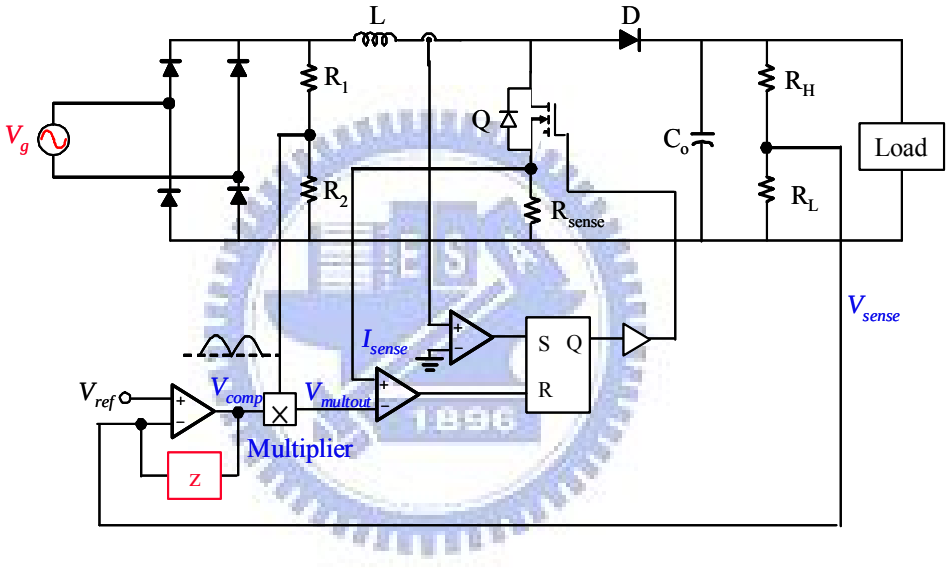


Fig. 2.2. The circuit architecture of the CRM PFC with multiplier.

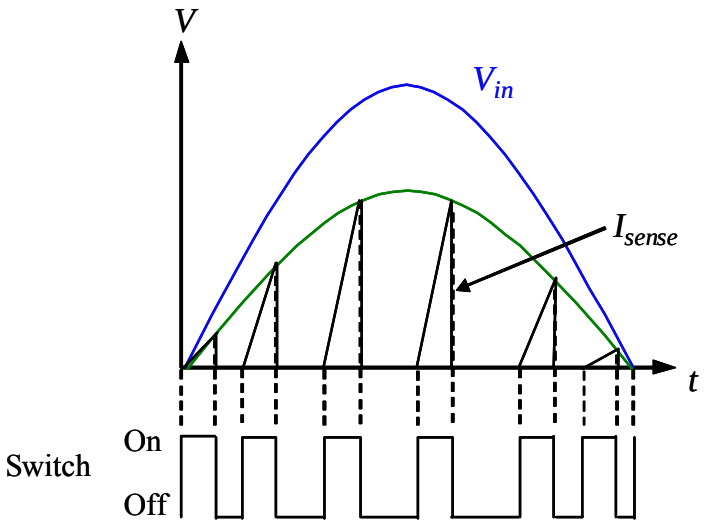


Fig. 2.3. Main waveforms of the CRM PFC with multiplier.

The other control strategy has the same purpose to maintain the on-time of switch as a constant value. This architecture is no need of a multiplier but uses the comparing result between the constant ramp, V_{ramp}, which is produced from a saw tooth generator and the output signal of the voltage error amplifier, V_{comp}. In this method, rectified line voltage sensing can be eliminated as shown in Fig. 2.4. And the operating principle is shown in Fig. 2.5. These topologies of CRM PFC AC-DC converters are fewer than the topologies with multiplier such as FAN7529 from Fairchild and SG6961 from System General [33].

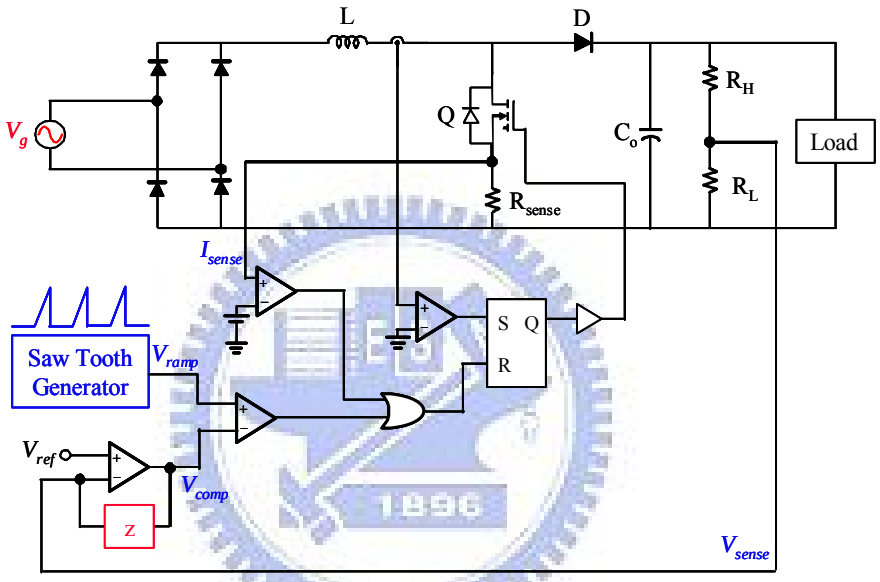


Fig. 2.4. The circuit architecture of the CRM PFC without multiplier.

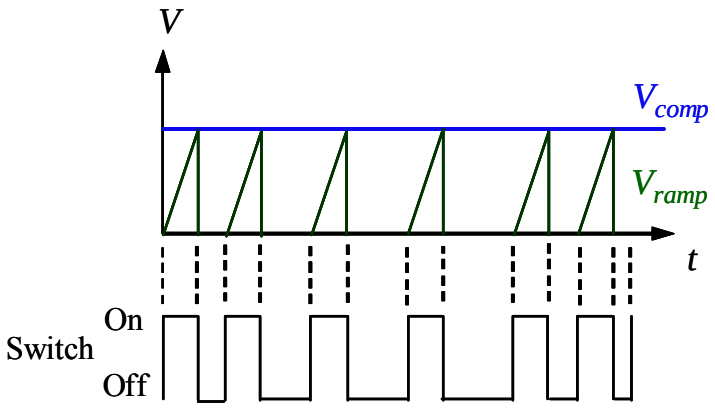


Fig. 2.5. Main waveforms of the CRM PFC without multiplier.

This thesis aimed at the CRM PFC AC-DC converter with a multiplier. The analysis and design flow of the control architecture will be given.

2.3 ARCHITECTURE OF MIXED-SIGNAL CRM PFC AC-DC CONVERTER

This section presents a mixed-signal CRM PFC AC-DC converter and the overall system block diagram of the mixed-signal control for the CRM PFC AC-DC converter is as shown in Fig. 2.6. This control architecture includes the inner analog current control loop with the outer digital voltage control loop. The current loop adopts peak current mode control to make inductor current can fast track with command. The voltage loop uses controller to regulate output voltage at setting level and adds the notch filter to eliminate double line frequency, achieve a fast dynamic response, keep the line current with low THD distortion, and maintain high PF. This thesis presents a mixed-signal CRM PFC AC-DC converter which combines the benefits of analog circuit and digital circuit implementation techniques to achieve good dynamic response for output voltage and the low THD with high power factor (PF) for input line current.

Analog PFC control techniques can provide current regulation with low total-harmonic-distortion (THD) on input line current under large input line voltage range which is dominantly adopted for practical implementation. In practice, the feasible control schemes are realized with commercial PFC ICs to meet the requirements both on performance and cost. With the increasingly stringent requirements both on applications and cost issues, digital PFC control techniques are merging to simplify the external control circuits and ease to implement complex control algorithm though circuit design for various applications. However, a pure digital realization of the PFC control scheme requires the realization of accurate and synchronous high frequency signals between the PWM control and feedback sampling. In contrast, mixed-signal realization of the PFC control scheme can combine advantages of fast response analog circuit for current loop control and flexible digital circuit realization for voltage loop control.

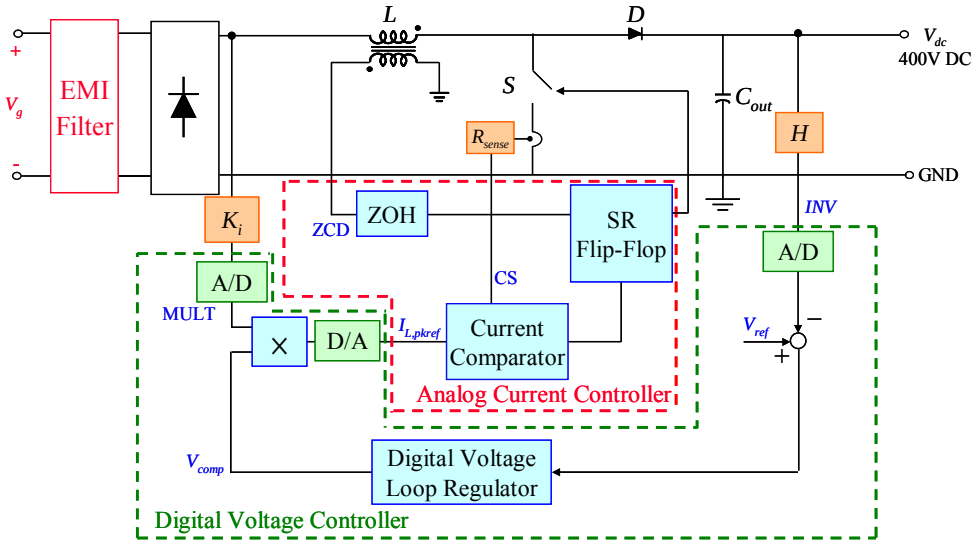


Fig. 2.6. Overall system block diagram of mixed-signal CRM PFC AC-DC converter.

Current Loop Comparator

The current loop comparator compares the sensing voltage across the current sensing resistor below the MOSFET with the inductor current command signal delivered by the multiplier. Then, the current loop comparator can exactly determine the time when the external MOSFET has to be turned off.

The current loop comparator has a hysteresis band to eliminate the noise disturbance from the practical circuits. But this hysteresis band also induces harmonic distortion in the line current. The appropriate value of hysteresis band in the current comparator is an important issue in the design procedure.

Zero Current Detector

The zero current detector (ZCD) function places an important role in CRM PFC AC-DC converter. The comparator of ZCD compares the voltage crossing on the secondary side of the transformer (V_{ZCD}) with the zero current detecting reference voltage ($V_{ref,d}$). When the inductor current is down to zero, the switch will turn on.

Because of the parasitic capacitors of the MOSFET C_{oss} and the boost diode C_D,

resonating with the inductor, an additional delay time (T_d) is induced to the inductor current at zero crossing. This delay time will cause the line current harmonic distortion. The zero current detecting reference voltage influences the delay time. Therefore, the proper reference voltage should be determined.

Analog to Digital Converter

Analog-to-digital converter (ADC) is a converter to convert analog signal into digital signal for digital control. The ADC is used at the output voltage feedback sensing and the rectified line voltage sensing.

The signal calculated in digital control system is realized by binary form. The resolution of ADC induces quantization error into the signal. Because the feedback of rectified line voltage determines the shape of inductor current command, the effect of ADC resolution on rectified line voltage is the most significant problem which is induced the harmonic distortion in line current. Moreover, lower sampling rate may introduce aliasing effect. The aliasing effect will also cause the line current high order terms. Therefore, the proper ADC resolution and sampling rate are important.

Digital to Analog Converter

Digital-to-analog converter (DAC) converts the digital current command back to analog signal. The quantization effect will directly influence the shape of inductor current command to induce the high order distortions. Therefore, the DAC resolution should high enough to enforce the line current THD to meet the regulations.

Digital Voltage Control Loop

The voltage compensator eliminates the error part between the feedback output voltage and the reference voltage (V_{ref}). For reducing the effect of output voltage ripple on output of

voltage compensator (V_{comp}) the bandwidth of the voltage loop will be set at much lower than the frequency of output voltage ripple.

The analog multiplier has the nonlinear problem and has to implement with complicated circuit. Therefore, the multiplier is implemented in digital approach which only has to concern the quantization effect on digital calculation. The multiplier has two inputs: the first one takes a partition of the instantaneous rectified line voltage and the second one is the output of the voltage compensator. The output of the multiplier ($V_{multout}$) is the inductor current command. Then, this current command will send into the current loop comparator to make the line voltage and line current in phase.

2.4 Analysis of CRM PFC Power Stage

The main attributes of the components of CRM PFC AC-DC converter, such as output capacitor and inductor value, need to be governed. Then, the power losses on each component should be estimated to calculate the efficiency of the CRM PFC circuit.

2.4.1 Analysis and Design of CRM PFC Power Stage

The design basic specifications are shown in Table 2.2. Then, the main elements of the CRM PFC power stage can be determined.

Table 2.2
Specifications of the CRM PFC AC-DC conveter

Parameter	Specification
Rated Output Power (P_{out})	100 W
Input Voltage ($V_{g,rms}$)	110 Vac
Line Frequency (f_{line})	60 Hz
Minimum Switching Frequency (f_{sw})	40 kHz
Output Voltage (V_{out})	400 Vdc
Output Voltage Ripple (ΔV_{out})	< 1 %
System Efficiency (η)	90%
Hold-Up Time (t_{holdup})	20 ms

The design flows for the main components are as shown in below. There are many factors involved in the design process. However, the equations below are intended to provide a framework for the design.

Determination of Output Capacitor

There are two methods to decide the output capacitor value. One way focuses on the ripple of the output voltage. There are two factors induce the output voltage ripple. One is introduced by the MOSFET switching frequency and the other one is caused by the rectified line voltage which has 120 Hz ripple. The output voltage ripple generated by the MOSFET switching frequency is much smaller than the ripple generated by the rectified line voltage. Assuming the line current is pure sinusoidal. The relationship between average inductor current during a switching period ($i_L(t)$) and input power (P_{in}) is represented as

$$i_L(t) = \frac{\sqrt{2} \cdot P_{in}}{V_{g,rms}} \cdot \sin(\omega t) \tag{2-12}$$

the input instantaneous power is

$$P_{in}(t) = 2 \cdot P_{in} \cdot \sin^2(\omega t). \tag{2-13}$$

Therefore, the current flowing through the output capacitor ($i_c(t)$) is

$$i_c(t) = \eta \cdot \frac{P_{in}(t)}{V_{out}} - \eta \cdot \frac{P_{in}}{V_{out}} = C \cdot \frac{dV_{out}}{dt}. \tag{2-14}$$

Substituting (2-13) into (2-14)

$$V_{out} \cdot \frac{dV_{out}}{dt} = \frac{\eta \cdot P_{in}}{C} \cdot \left[2 \cdot \sin^2(\omega t) - 1\right] \tag{2-15}$$

Integrated both sides of (2-15) can be given as

$$V_{out} \cdot \left[V_{out}(t) - V_{out}\right] = 0.5 \cdot \left(-\eta \cdot \frac{P_{in}}{C \cdot \omega}\right) \cdot \sin(2\omega t) \tag{2-16}$$

where $V_{out}(t)$ is equal to $[V_{out} + \Delta v_{out,ripple}(t)]$, the combination of output voltage DC term and AC term. The ripple of output voltage is

$$\Delta v_{out,ripple}(t) = -\frac{\eta \cdot P_{in} \cdot \sin(2\omega t)}{2 \cdot C \cdot \omega \cdot V_{out}} \tag{2-17}$$

the peak-to-peak value of output voltage ripple ($\Delta V_{out,ripple}$) can be got

$$\Delta v_{out,ripple} = \frac{\eta \cdot P_{in}}{C \cdot \omega \cdot V_{out}}. \tag{2-18}$$

According to the output voltage ripple specification from Table 2.2, the output capacitance can be given as below

$$\begin{aligned} C &= \frac{\eta \cdot Pin}{\Delta v_{out,ripple} \cdot \omega \cdot V_{out}} \\ &= \frac{100}{400 \cdot 1\% \cdot 2\pi \cdot 60 \cdot 400} = 166\,\mu\text{F}. \end{aligned} \tag{2-19}$$

Another considers the effect of hold-up time. Hold-up time is an important factor related to the amount of energy that the output capacitor needs to store. Generally, hold-up time range from 16 to 50 ms. A great majority of the industry requirement is 20 ms. This takes into consideration the minimum voltage the PFC pre-regulator will allow the output voltage to drop to while sustaining the output load (Usually is down to 95 % of output voltage). The energy storing in output capacitor can be expressed by below energy equation

$$\frac{1}{2} \cdot C \cdot \left({V_{out}}^2 - {V_{out,\min}}^2 \right) = P_{out} \cdot t_{holdup}. \tag{2-20}$$

According to the specification of hold-up time, the output capacitor can be decided as

$$\begin{aligned} C &= \frac{2 \cdot P_{out} \cdot t_{holdup}}{{V_{out}}^2 - {V_{out,\min}}^2} \\ &= \frac{2 \cdot 100 \cdot 20m}{400^2 - 380^2} = 256\,\mu\text{F}. \end{aligned} \tag{2-21}$$

Comparing above results of two methods, the output capacitor can be determined by larger one which is 300 μF as shown in Fig. 2.7. The output ripple can be

recalculated

$$\Delta v_{out,ripple} = \frac{100}{300\mu \cdot 2\pi \cdot 60 \cdot 400} = 2.2\ \text{V}. \tag{2-22}$$

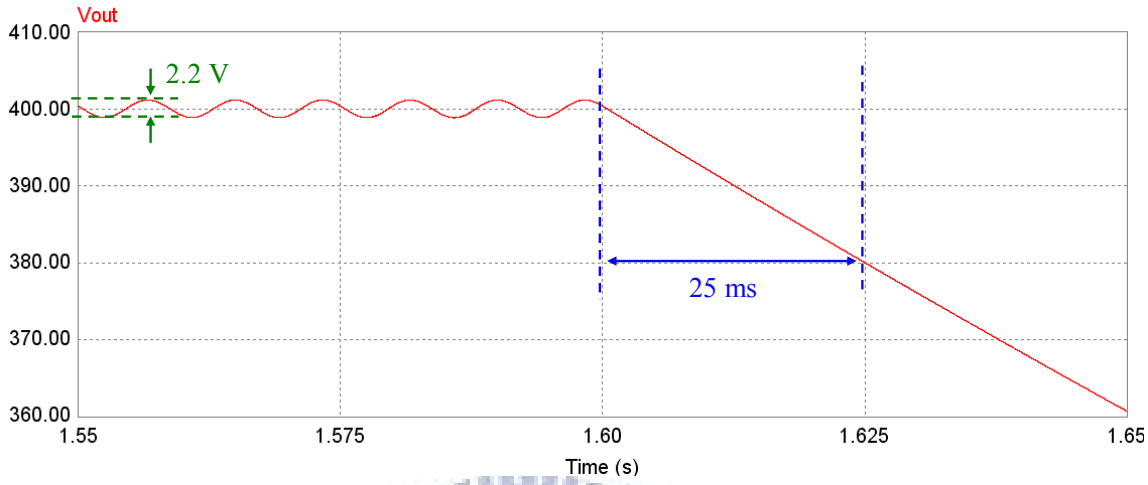


Fig. 2.7. The simulation of the hold-up time and output voltage ripple.

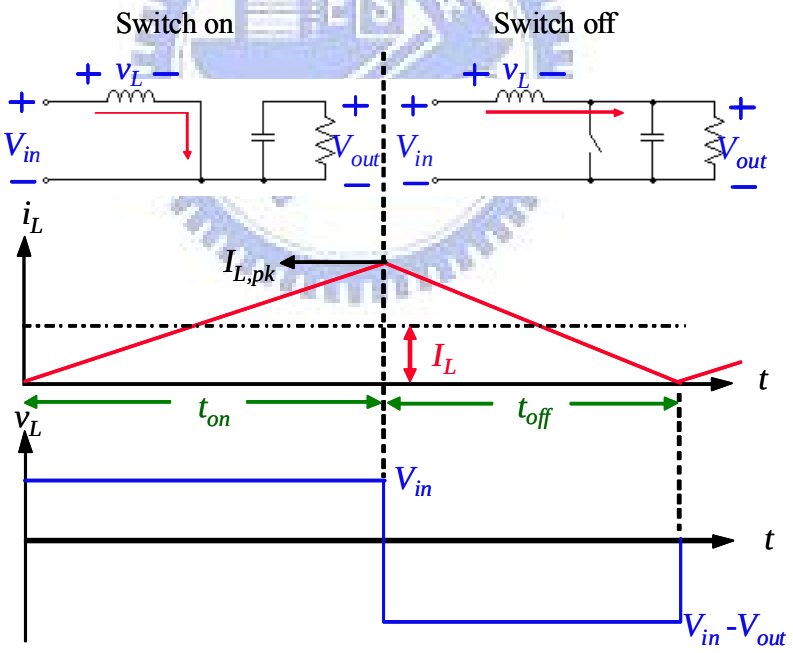


Fig. 2.8. Switching Sequences of the CRM PFC power stage.

Determination of Inductor

The off-time of the MOSFET is based on the input line voltage and the inductance, which also dictates the operating frequency range. The design of the inductor is based on the

switching frequency. As shown in Fig. 2.8, the off-time of the MOSFET is

$$t_{off} = L \cdot \frac{I_{L,pk}(t)}{V_{out} - V_{in}(t)}. \tag{2-23}$$

Combining (2-11) and (2-23), the switching frequency (f_{sw}) is

$$f_{sw} = \frac{1}{t_{on} + t_{off}} = \frac{V_{in}(t) \cdot [V_{out} - V_{in}(t)]}{L \cdot V_{out} \cdot I_{L,pk}(t)}. \tag{2-24}$$

The CRM PFC AC-DC converter has variable switching frequency from (2-24). Therefore, the minimum switching frequency will occur at the peak of line voltage.

$$f_{sw} \geq \frac{V_{in,pk} \cdot (V_{out} - V_{in,pk})}{L \cdot V_{out} \cdot I_{L,pk}} \tag{2-25}$$

where $V_{in,pk}$ is the input peak voltage and $I_{L,pk}$ is the peak inductor current. And the average inductor current during a switching period can be represented as

$$I_{g,pk} = \frac{1}{2} \cdot I_{L,pk\max} = \sqrt{2} \cdot \frac{P_{out}}{\eta \cdot V_{g,rms}}. \tag{2-26}$$

According to Table 2.2, the specification of the lowest switching frequency is 40 kHz. Substituting (2-26) into (2-25), the relationship between inductance and the lowest switching frequency is as follow

$$L \leq \frac{V_{in,pk}{}^2 \cdot (V_{out} - V_{in,pk}) \cdot \eta}{V_{out} \cdot f_{sw,\min} \cdot 2 \cdot 2P_{out}}. \tag{2-27}$$

From (2-27), the inductance should be lower than 835 μF. In this thesis, the inductance is decided as 800 μF. Because that the boost converter operates in the CRM, the relationship between the rectified line voltage and output voltage is

$$V_{out} = \frac{1}{1 - D} \cdot V_{in}(t) \tag{2-28}$$

where D is the duty cycle of the switch. The minimum duty cycle which occurs at the peak of line voltage can be calculated by (2-28).

$$D_{\min} = 1 - \frac{V_{in,pk}}{V_{out}} = 1 - \frac{156}{400} = 61\% \tag{2-29}$$

The peak of inductor current ($I_{L,pk}$) can be expressed as

$$I_{L,pk} = 2 \cdot \sqrt{2} \cdot I_{g,rms} = 2 \cdot \sqrt{2} \cdot \frac{P_{out}}{V_{g,rms}} \tag{2-30}$$

When the line voltage is 110 Vrms, the inductor current peak is 2.57 A. The typical waveforms of the CRM PFC AC-DC converter are shown in Fig. 2.9. At the zero-crossing of line voltage, the energy stored in the inductor is not enough to drive the resonant capacitor to the output voltage. At this critical input line voltage level, the line current distortion will occur.

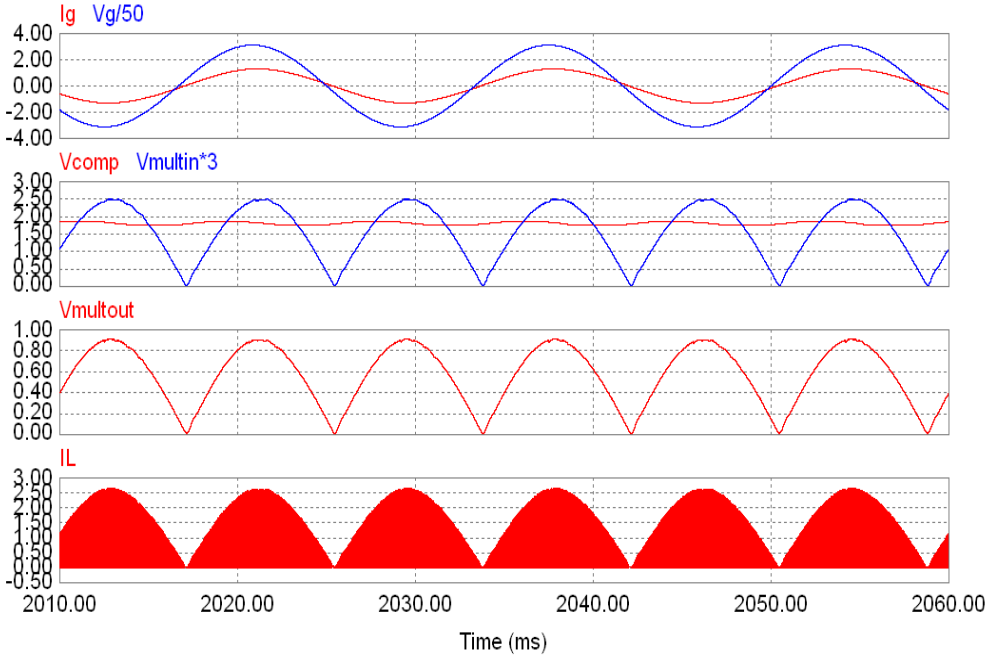


Fig. 2.9. Typical waveforms of CRM PFC AC-DC converter.

2.4.2 Calculation of Current RMS Values for Power Components

The efficiency of the CRM PFC power stage is an important issue. Therefore, the RMS current on each component are significant for design procedure [12]-[14].

Rectifier Bridge

The diode of rectified bridge can be approximated by the serial connection of a forward voltage (V_F) and a resistance (R_F). The current flowing through the rectifier bridge (I_{in}) is equal to the inductor current (I_L). The inductor current waveform is shown in Fig. 2.10. Assuming the switching frequency is much higher than the line frequency. Then, the instantaneous peak value of inductor current is

$$i_{L,pk}(\theta) = 2 \cdot \sqrt{2} \cdot \frac{P_{in}}{V_{g,rms}} \cdot \sin\theta. \tag{2-31}$$

The RMS value of the inductor current triangle over the corresponding switching period T_s ($i_{L,rms}(\theta)$) is represented by

$$\begin{aligned} i_{L,rms}(\theta) &= \sqrt{\frac{1}{T_s} \cdot \left[\int_0^{t_{on}} \left(\frac{I_{L,pk} \cdot \sin\theta}{t_{on}} \cdot t \right)^2 dt + \int_{t_{on}}^{T_s} \left[\frac{I_{L,pk} \cdot \sin\theta}{t_{off}} \cdot (Ts - t) \right]^2 dt \right]} \\ &= \sqrt{\frac{1}{3} \cdot (I_{L,pk} \sin\theta)^2}. \end{aligned} \tag{2-32}$$

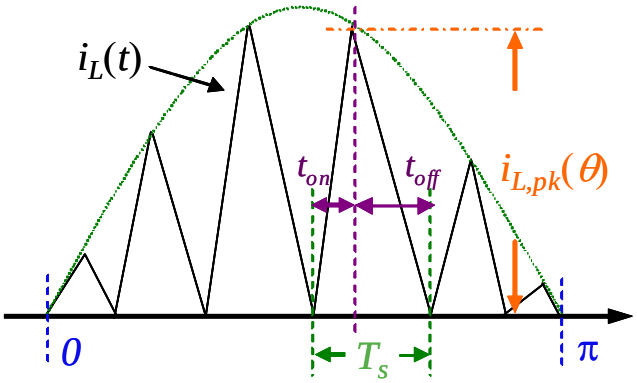


Fig. 2.10. The waveform of inductor current.

As the consequence, the RMS value of the inductor current is

$$I_{L,rms} = \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi}\left[i_{L,rms}(\theta)\right]^2 d\theta} = \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi}\left[\frac{1}{3}\cdot(I_{L,pk}\cdot\sin\theta)^2\right]} = \frac{1}{\sqrt{6}}\cdot I_{L,pk} = I_{in,rms}. \tag{2-33}$$

Then, the power consumption of the four diodes of the rectifier bridge, $P_{loss,br}$, can be estimated as follow

$$P_{loss,br} = 4\cdot\left[V_F\cdot I_{in,rms}\cdot\frac{\sqrt{2}}{\pi}\right] + 4\cdot\left[\frac{I_{in,rms}}{\sqrt{2}}\right]^2\cdot R_F. \tag{2-34}$$

MOSFET and Current Sensing Resistance

CRM PFC AC-DC converter presents a challenge because of the high peak currents which will introduce higher switching conduction losses. The power consumption on the switching current sensing resistance should be concerned either. The waveform of switching current is shown in Fig 2.11. The RMS value of the switching current triangle over the corresponding switching period T_s ($i_{Q,rms}(\theta)$) can be as

$$i_{Q,rms}(\theta) = \sqrt{\frac{1}{T_s}\cdot\int_0^{t_{on}}\left[\frac{I_{L,pk}\cdot\sin\theta}{t_{on}}\cdot t\right]^2 dt} = \frac{I_{L,pk}\cdot\sin\theta}{\sqrt{3}}\cdot\sqrt{\frac{t_{on}}{T_s}}. \tag{2-35}$$

The CRM PFC operates at the border of the CCM and DCM, then the expression gives the duty cycle in a CRM AC-DC converter applications.

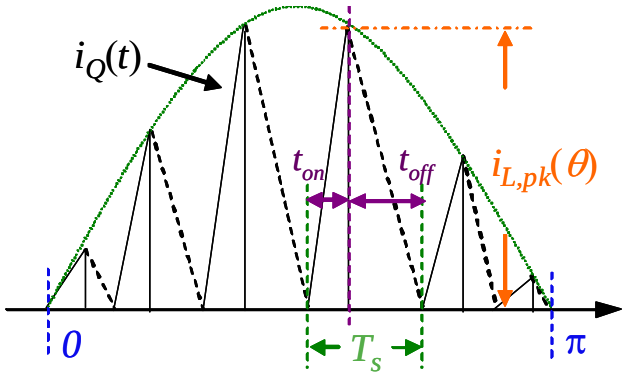


Fig. 2.11. The current waveform of MOSFET.

$$\frac{t_{on}}{T_s} = 1 - \frac{V_{in}(\theta)}{V_{out}} = 1 - \frac{\left|\sqrt{2} \cdot V_{g,rms} \cdot \sin\theta\right|}{V_{out}}. \tag{2-36}$$

As the consequence, the RMS value of the MOSFET current is

$$\begin{aligned} I_{Q,rms} &= \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} \left[i_{Q,rms}(\theta)\right]^2 d\theta} \\ &= \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} \left[\frac{(I_{L,pk} \cdot \sin\theta)^2}{3} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{g,rms} \cdot \sin\theta}{V_{out}}\right)\right] d\theta} \\ &= \frac{2}{\sqrt{3}} \cdot \frac{P_{out}}{V_{g,rms}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{g,rms}}{3\pi \cdot V_{out}}}. \end{aligned} \tag{2-37}$$

The conducting switch can be equivalent to a resistance, $R_{ds,on}$. The power loss on both switch and current sensing resistance, R_{sense}, is as follow

$$P_{loss,on} = \left[R_{ds,on} + R_{sense}\right] \cdot {I_{Q,rms}}^2. \tag{2-38}$$

Diode RMS Current

The freewheeling diode of CRM PFC AC-DC converter will be a fast recovery one. The diode current waveform is shown in Fig. 2.12. The RMS value of the diode current over the corresponding switching period T_s, is given by

$$\begin{aligned} i_{D,rms}(\theta) &= \sqrt{\frac{1}{T_s} \cdot \int_{t_{on}}^{T_s} \left[\frac{I_{L,pk} \cdot \sin\theta}{t_{off}} \cdot (T_s - t)\right] 2dt} \\ &= \frac{I_{L,pk} \cdot \sin\theta}{\sqrt{3}} \cdot \sqrt{\frac{t_{off}}{T_s}}. \end{aligned} \tag{2-39}$$

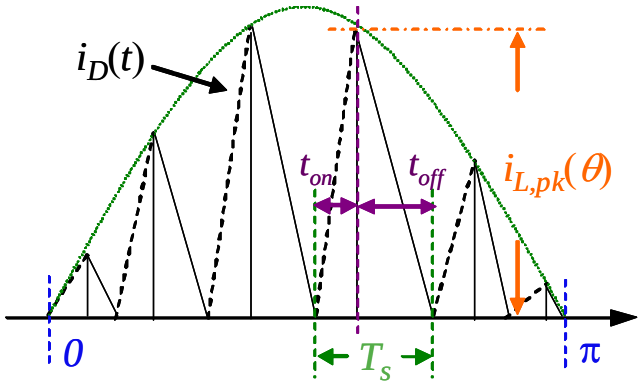


Fig. 2.12. The diode current waveform.

where the ratio of switching off-time over one switching cycle is

$$\frac{t_{off}}{T_s} = \frac{V_{in}(t)}{V_{out}} = \frac{\left|\sqrt{2}\cdot V_{g,rms}\cdot \sin\theta\right|}{V_{out}}. \tag{2-40}$$

As the consequence, the RMS value of the diode current is

$$\begin{aligned} I_{D,rms} &= \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi}\left[i_{D,rms}(\theta)\right]^2 d\theta} = \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi}\left[\frac{\sqrt{2}}{3}\cdot\frac{V_{g,rms}}{V_{out}}\cdot {I_{L,pk}}^2\cdot\sin^3\theta\right]d\theta} \\ &= \frac{2}{3}\cdot I_{L,pk}\cdot\sqrt{\frac{\sqrt{2}\cdot V_{g,rms}}{\pi\cdot V_{out}}} \end{aligned} \tag{2-41}$$

and the average current flowing through the diode is equal to the output average current.

$$I_{D,avg} = \frac{P_{out}}{V_{out}}. \tag{2-42}$$

The diode can be also approximated to a serial connection of a forward voltage, V_{FD}, and a resistance, R_{FD}. Therefore, the power consumption can be estimated as

$$P_{loss,diode} = V_{FD}\cdot I_{D,avg} + R_{FD}\cdot {I_{D,rms}}^2. \tag{2-42}$$

Output Capacitor

The capacitor current is the difference between the diode current and the current absorbed by the load as shown in Fig. 2.13.

$$i_C(t) = i_D(t) - i_{out}(t) \tag{2-43}$$

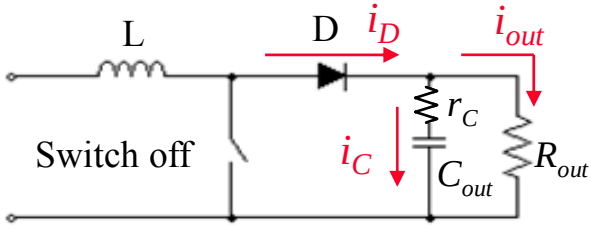


Fig. 2.13. The output capacitor current waveform.

Assuming the output voltage and the output current, i_{out}, will be constant value.

$$i_{out}(t) = I_{out} = \frac{P_{out}}{V_{out}} \tag{2-44}$$

The RMS value of the capacitor current is

$$\begin{aligned} I_{C,rms} &= \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} [i_D(\theta) - i_{out}(\theta)]^2 d\theta} \\ &= \sqrt{{I_{out}}^2 + {I_{D,rms}}^2 - \frac{2}{\pi} \cdot \int_0^{\pi} [i_D(\theta) \cdot I_{out}] d\theta} \\ &= \sqrt{{I_{D,rms}}^2 - {I_{out}}^2}. \end{aligned} \tag{2-45}$$

The practical capacitor has a serial resistance, r_C, which induces power loss on the output capacitor.

$$P_{loss,ESR} = {I_{C,rms}}^2 \cdot r_C \tag{2-46}$$

So that, the total power loss and efficiency of the power stage can be calculated. Power losses on each component are shown in Fig. 2.14.

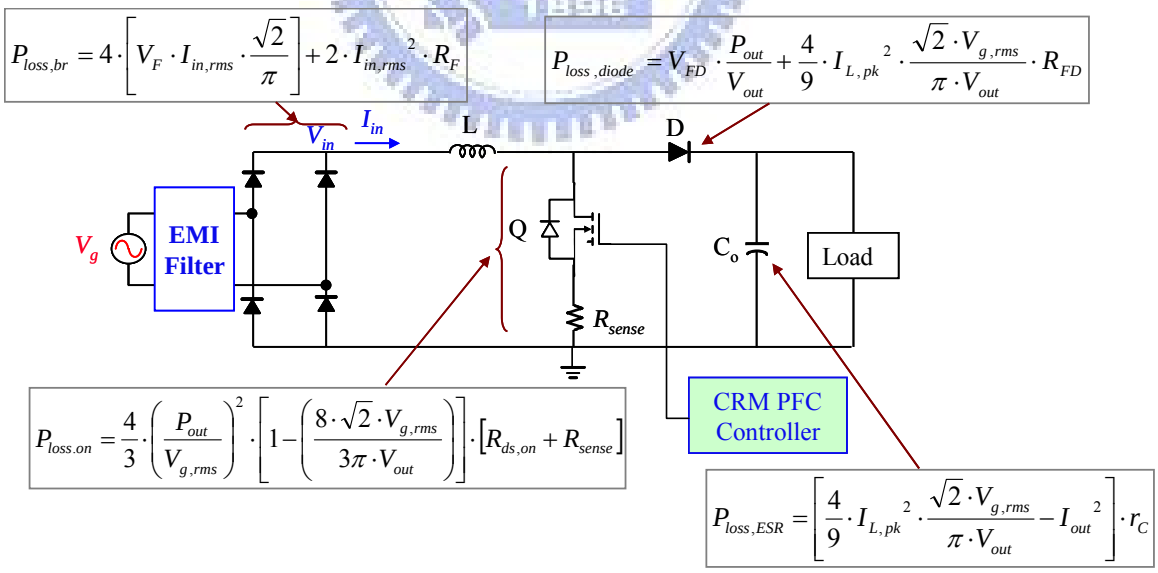


Fig. 2.14. The power losses on the power components.

Chapter 3

Analysis and Design of Mixed-Signal CRM PFC AC-DC Converter

3.1 Analysis and Design of Analog Current Control Loop

3.1.1 Design of the Current Loop Comparator

Switching current is detected by the sensing resistor under the MOSFET, and the sensed voltage compares with the inductor current command from the multiplier output. When the sensed voltage is over the current command, the output of the current comparator will be high. The current comparator output connects to the reset pin of RS flip-flop, causing the MOSFET turned off. The circuits near by the current loop comparator are shown in Fig. 3.1 [15], [16].

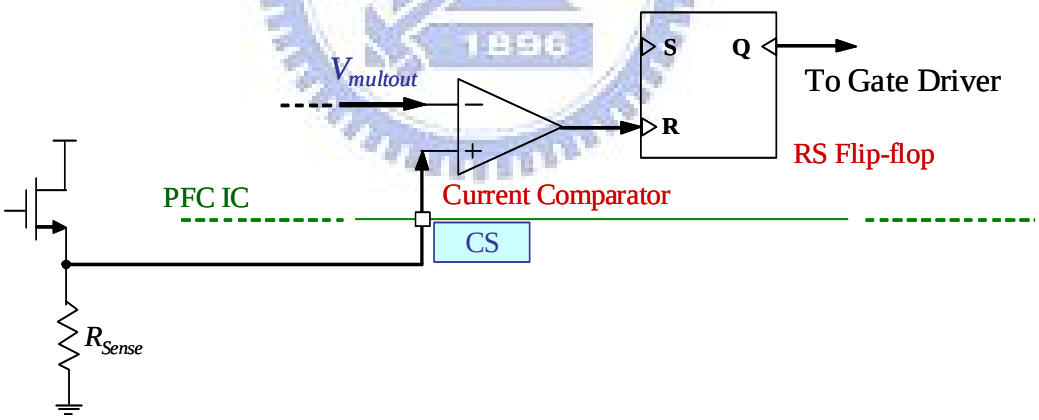


Fig. 3.1. Circuit nears by the current loop comparator.

For the current loop comparator of peak current mode control loop, hysteresis band is necessary to eliminate the disturbance of noise to obtain a correct switching signal. Fig. 3.2 shows the reference waveform of inductor current with hysteresis band. However, as mentioned in the previous analysis, over-wide hysteresis band can also induce input current harmonic distortion.

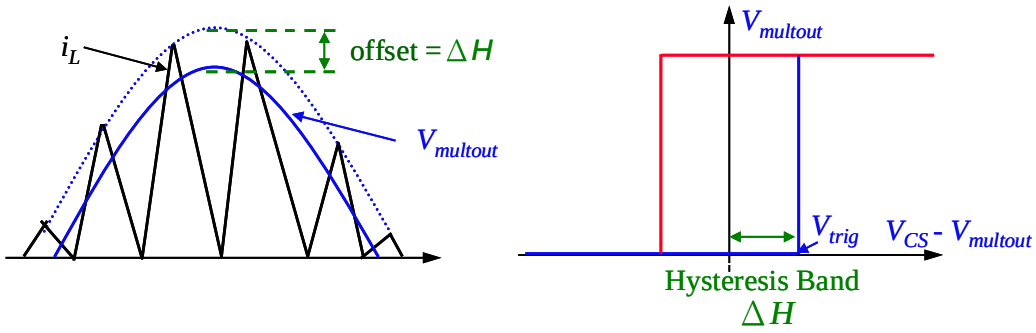


Fig. 3.2. The reference waveform of inductor current with hysteresis band.

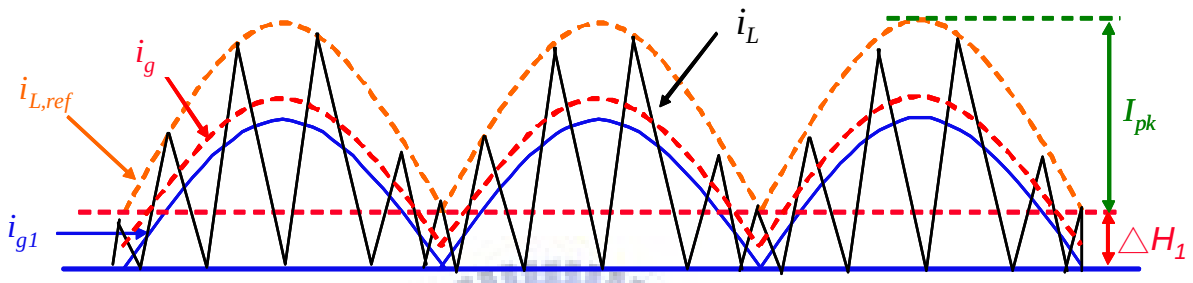


Fig. 3.3. The relationship between hysteresis band and fundamental waveform of line current.

For analyzing the effect of the hysteresis band on line current, the fundamental component of the line current with hysteresis band is an important issue. Fig. 3.3 shows the relationship between hysteresis band and fundamental waveform of line current. The hysteresis band is resulting a dc component (ΔH_1) in the reference signal of inductor current, $i_{L,\mathrm{ref}}$, i_{g1} is the input line current fundamental component, and i_g is the line current waveform.

In Fig. 3.3, assuming that the switching frequency is much higher than the line frequency, the relationship between the fundamental component of line current and the hysteresis band is as follow

$$\begin{aligned} I_{g1,rms} &= \frac{1}{2}\cdot\frac{1}{\sqrt{2}}\cdot\frac{2}{\pi}\cdot\int_0^{\pi} i_{L,ref}\cdot\sin\theta d\theta \\ &= \frac{1}{2}\cdot\frac{1}{\sqrt{2}}\cdot\frac{2}{\pi}\cdot\int_0^{\pi}(\Delta H_1 + I_{pk}\cdot\sin\theta)\cdot\sin\theta d\theta \\ &= \frac{1}{2}\cdot\frac{1}{\sqrt{2}}\cdot\left(\frac{4\cdot\Delta H_1}{\pi}+I_{pk}\right)=\frac{P_{out}}{\eta\cdot V_{g,rms}} \end{aligned} \tag{3-1}$$

and the dc component, ΔH_1, can be rewritten as

$$\Delta H_1 = \Delta H \cdot \frac{1}{R_{sense}}. \tag{3-2}$$

If the value of I_{pk} is given, the line current RMS value can be calculated as

$$\begin{aligned} I_{g,rms} &= \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} \left(\frac{1}{2} \cdot I_{pk} \cdot \sin\theta + \frac{1}{2} \cdot \Delta H_1 \right) d\theta} \\ &= \frac{1}{2} \cdot \sqrt{\left(\frac{1}{2} \cdot {I_{pk}}^2 + \frac{4}{\pi} \cdot I_{pk} \cdot \Delta H_1 + {\Delta H_1}^2 \right)}. \end{aligned} \tag{3-3}$$

According to (3-3), the THD and PF can be expressed as follow

$$THD = \frac{I_{gdis,rms}}{I_{g1,rms}} = \frac{\sqrt{{I_{g,rms}}^2 - {I_{g1,rms}}^2}}{I_{g1,rms}} \tag{3-4}$$

$$PF = \frac{I_{g1,rms}}{I_{g,rms}} = \frac{1}{\sqrt{1+THD^2}}. \tag{3-5}$$

The simulation waveforms of line current with different hysteresis bands are shown in Fig. 3.4. When hysteresis band is 200 mV, the line current will distort at zero crossing. According to (3-1), (3-3), and (3-4), the relationship between hysteresis band influence and THD can be retrieved at the conditions of rated power and 110 Vrms line voltage as shown in Fig. 3.5. Fig. 3.6 shows these relationships with different line voltages. The THD of line current can be determined by harmonic regulation. Therefore, the proper hysteresis band can be selected. In this thesis, the hysteresis band is selected at least under 50 mV to make THD lower than 5 % at rated power.

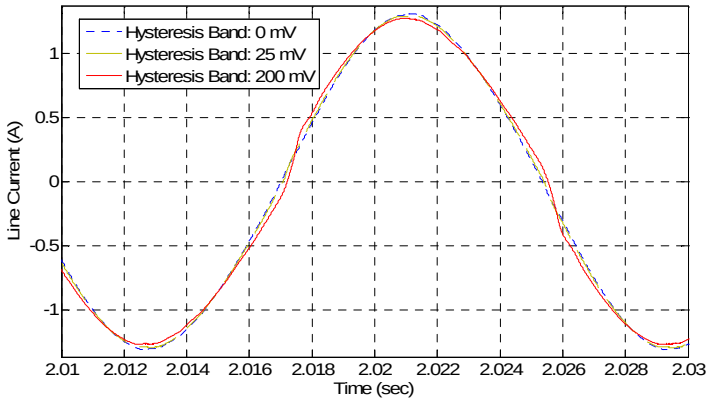


Fig. 3.4. Line current waveforms with different hysteresis bands.

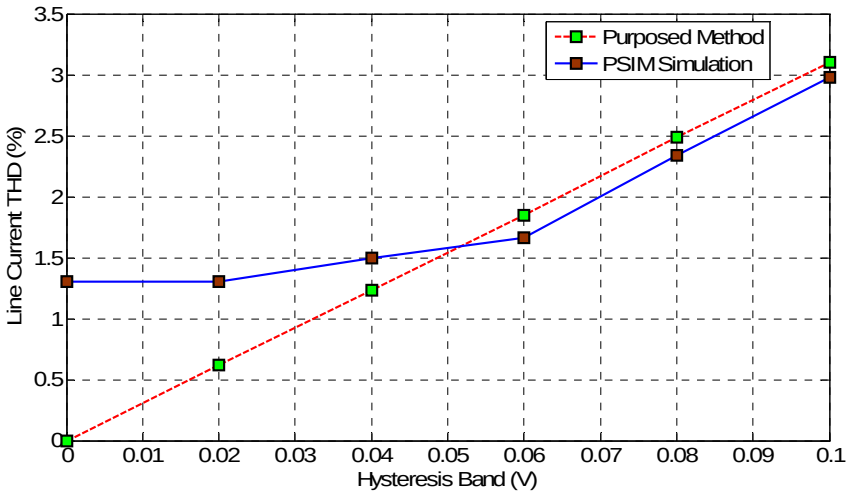


Fig. 3.5. The relationship between hysteresis band and line current THD.

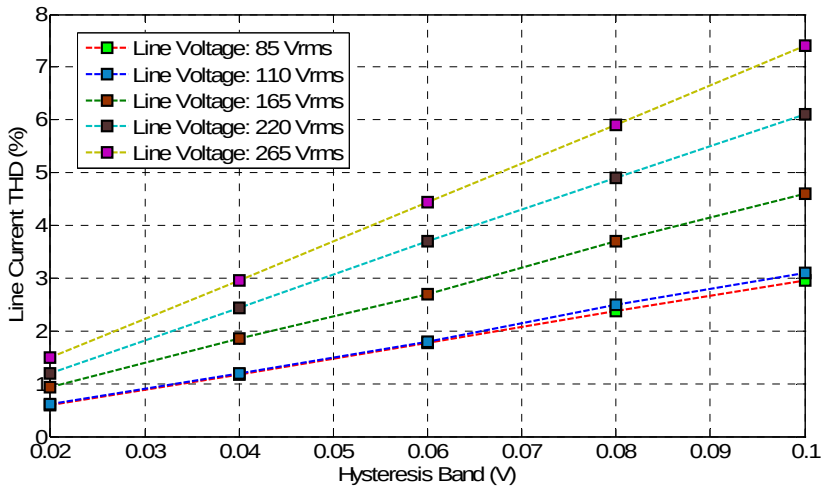


Fig. 3.6. The relationship between hysteresis band and line current THD with different line voltages.

3.1.2 Design of ZCD Comparator

Zero-current-detector (ZCD) technique is an important part to maintain that the inductor current operates in the critical mode. It is sensing the voltage of the nodes between the inductor and the power switch, V_{ZCD}. When the switch turns on, V_{ZCD} is reducing to zero because that the conduction resistor is small and the inductor current linearly increases. When the switch is turns off, V_{ZCD} is pulled high to be clamped by the zener diode and the inductor current decays to zero. V_{ZCD} compares with a reference voltage, $V_{ZCD,ref}$, and then the ZCD comparator output connects to the S pin of the RS flip-flop, as shown in Fig. 3.7 [17], [18].

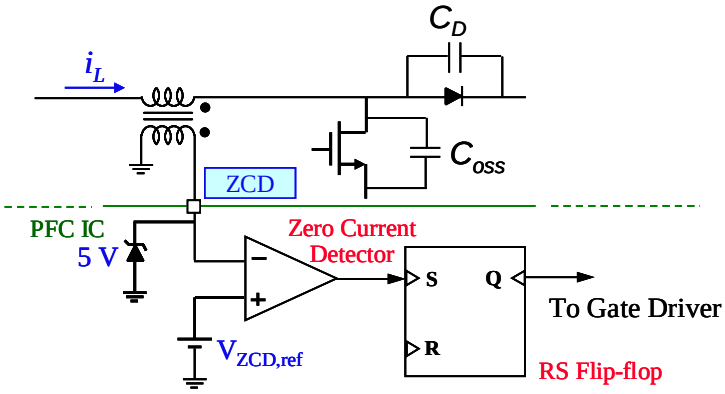
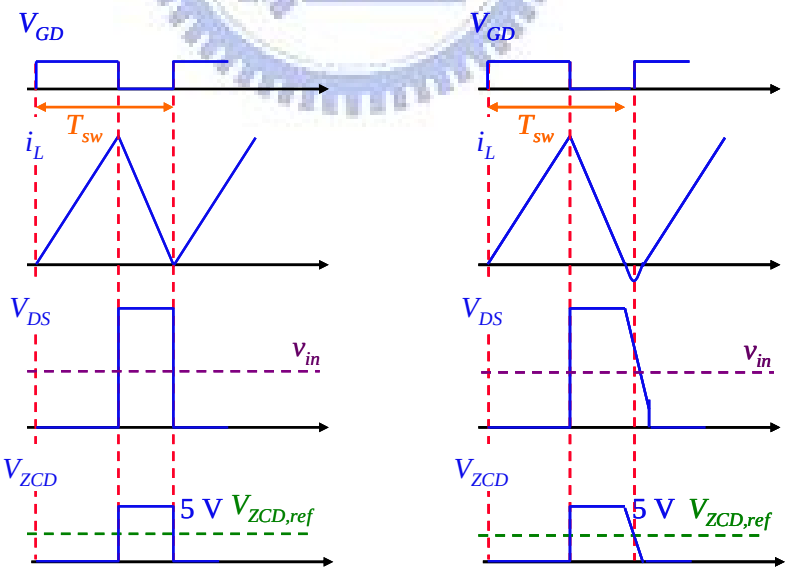


Fig. 3.7. Circuits near by the ZCD comparator.

The MOSFET turns on with hard switching causing the additional delay, T_d, when the circuit operates at CRM. Under this delay region, the voltage of V_{ZCD} will not drop to zero straightly as shown in Fig. 3.8 (a) but decade on a constant rate as shown in Fig 3.8 (b). Therefore, the different values of reference voltage, $V_{ZCD,ref}$, which compares with V_{ZCD}, cause the different turn-on times and induce line current distortion. The relationship between reference voltage, $V_{ZCD,ref}$, and line current THD is shown in Fig. 3.9 at rated power and the summation of C_{oss} and C_D is 0.2 nF. Then, the properly value of $V_{ZCD,ref}$ is 1.5 V.



(a) (b)

Fig. 3.8. Key switching waveforms of critical mode operation (a) without delay (b) with delay, T_d.

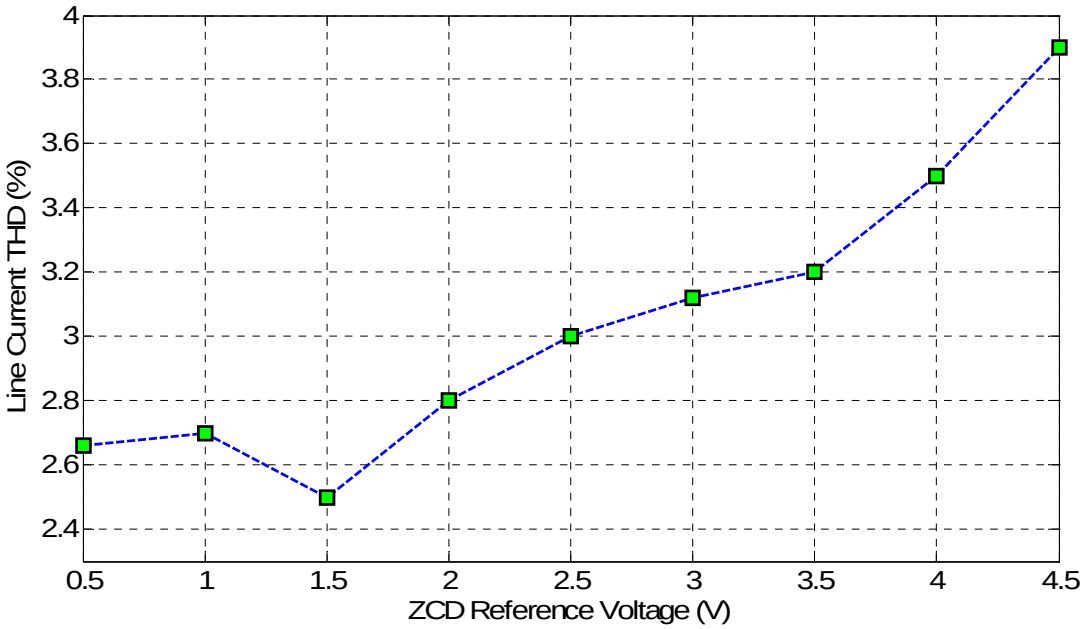


Fig. 3.9. The relationship between $V_{ZCD,ref}$ and line current THD.

3.2 Analysis and Design of Digital Voltage Control Loop

3.2.1 Issues of Quantization Effect on Digital Control

Implementing digital control on a continuous time system needs an ADC and a DAC for digital and analog signal interface. The striking difference between "analog" and "digital" control is the quality and the amount of information available for the controller to make decisions regarding the operation of the power stage. The control algorithm in digital control system is realized by binary calculation. The presence of a signal of frequency higher than half of the sampling frequency can affect the controller by the aliasing effect [19]-[21].

3.2.2 Sampling Frequency

To find a properly sampling rate, the aliasing effect should be concerned. Aliasing is a phenomenon associated with any device or process where the data are divided into individual samples. Any frequency above half of the sampling frequency will cause aliasing effect. Fig. 3.10 shows the aliasing effect by sampling a 120 Hz sinusoidal wave with 150 Hz sampling frequency.

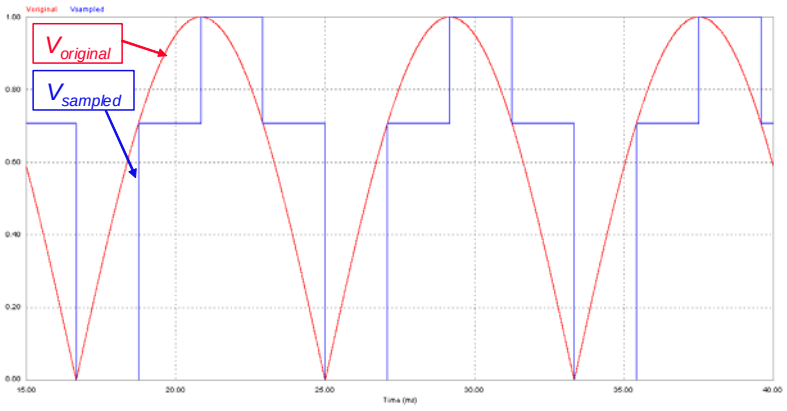


Fig. 3.10. Sampling a 120 Hz rectified sinusoidal wave at 480 Hz sampling frequency.

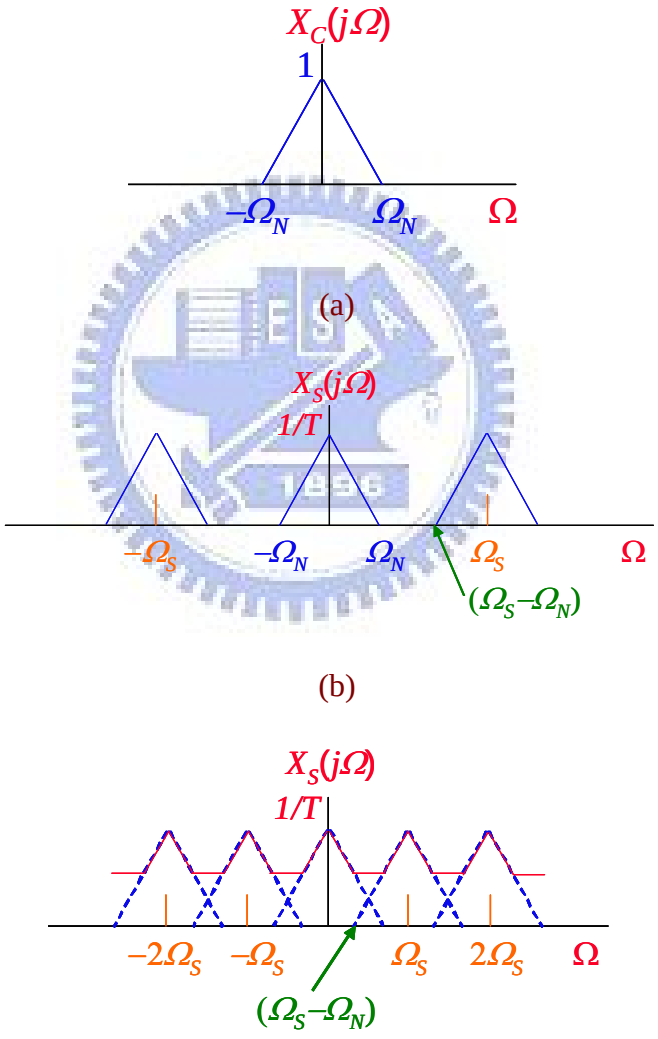


Fig. 3.11. Illustration of the aliasing effect in frequency domain (a) Spectrum of original signal, (b) Spectrum of the sampled signal with $\Omega_S > 2\Omega_N$, and (c) Spectrum of the sampled signal with $\Omega_S < 2\Omega_N$..

From a frequency domain standpoint, frequency component of the sampled signal above half of sampling frequency, f_{sample}, is wrapped around appearing as a lower frequency component. Fig. 3.11 shows the aliasing effect in frequency domain.

The aliasing effect can induce confusion and serious error in digital control. If the sampled signal processed has a wide bandwidth, the sampling rate should be high enough to reduce the aliasing effect. Although higher sampling frequency can reduce distortion, but it will be more expensive and larger power consumption. The lowest sampling frequency which the CRM PFC AC-DC converter needed without aliasing error is an important comment in this thesis.

In the comment, the CRM PFC AC-DC converter needs two ADCs. One samples the rectified sinusoidal wave of rectified line voltage. The other one samples the dc value of feedback output voltage. The lowest sampling frequency will be limited by the rectified sinusoidal wave. Thus Fig. 3.12 shows the normalized harmonic ratios for 120 Hz rectified sinusoidal wave. From Fig. 3.12, the harmonic component of 120 Hz rectified sinusoidal wave will decay to 1 % at 960 Hz. For keeping these harmonics within half of the sampling frequency, the sampling rate of rectified line voltage should be larger than 2 kHz. A 5 kHz sampling frequency is selected.

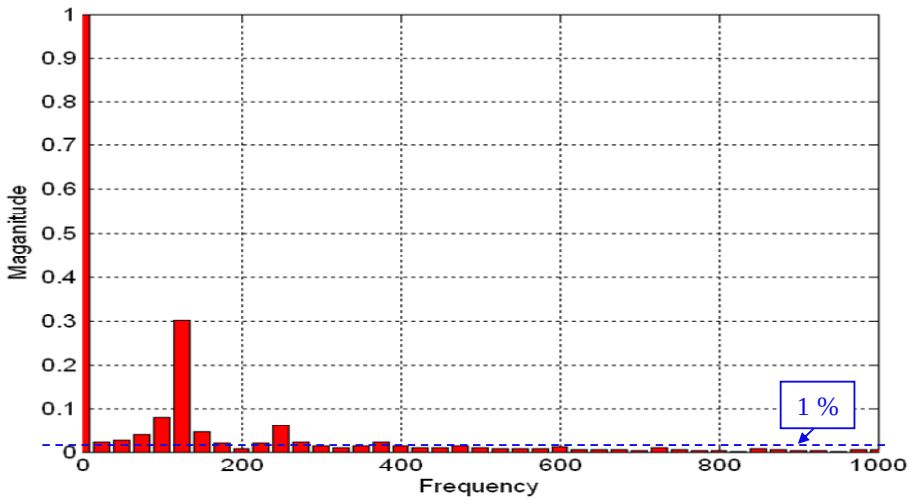


Fig. 3.12. Normalized harmonic ratios for rectified sinusoidal wave.

3.2.3 Determination of Bit Resolution

In digital control implementation, the continuous signals are converted into discrete signals at the input of the voltage controller and the output of the voltage controller is converted the discrete signal back into a continuous one by a DAC. And so on, ADC truncates input signal and DAC truncates the output signal to their least-significant-bit (LSB). The procedure can be modeled as a quantizer that introduces disturbance and noise into the control system inducing undesired harmonic distortion at the output of voltage controller. The input and output of a quantizer are shown in Fig. 3.13.

The equivalent of the quantizer is shown in Fig. 3.14. The difference between the original signal and quantized signal can be modeled by an error component introduced into the system. Although it is difficult to predict the frequency and shape of the error signal, the maximum amplitude can be limited between the ranges of $\Delta/2$ to $-\Delta/2$, where Δ equals one quantization step.

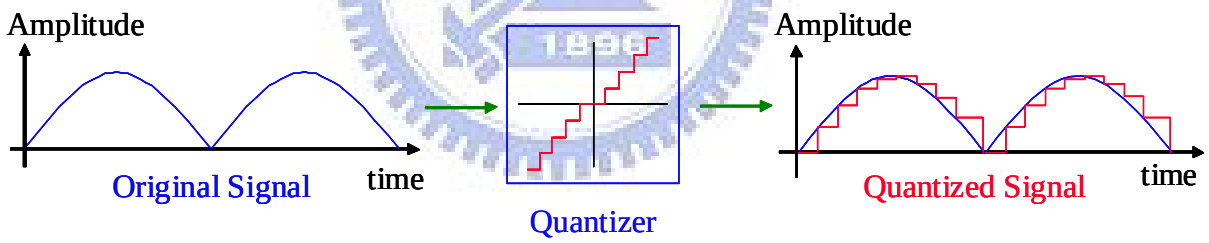


Fig. 3.13. Quantization effect on rectified input line voltage feedback.

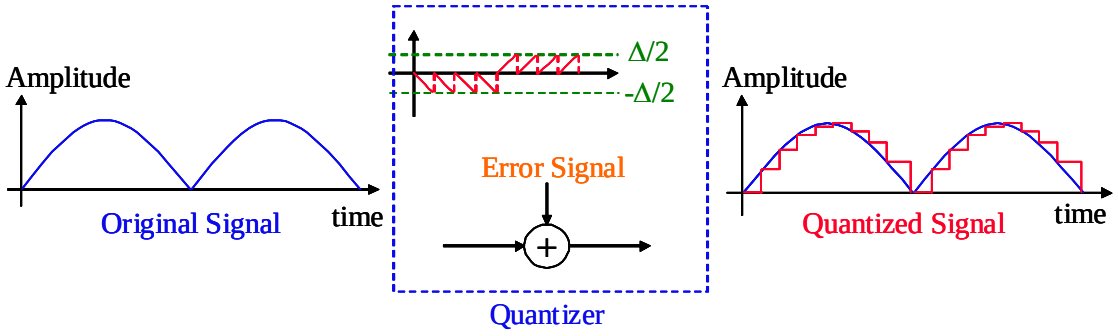


Fig. 3.14. The model of quantization effect.

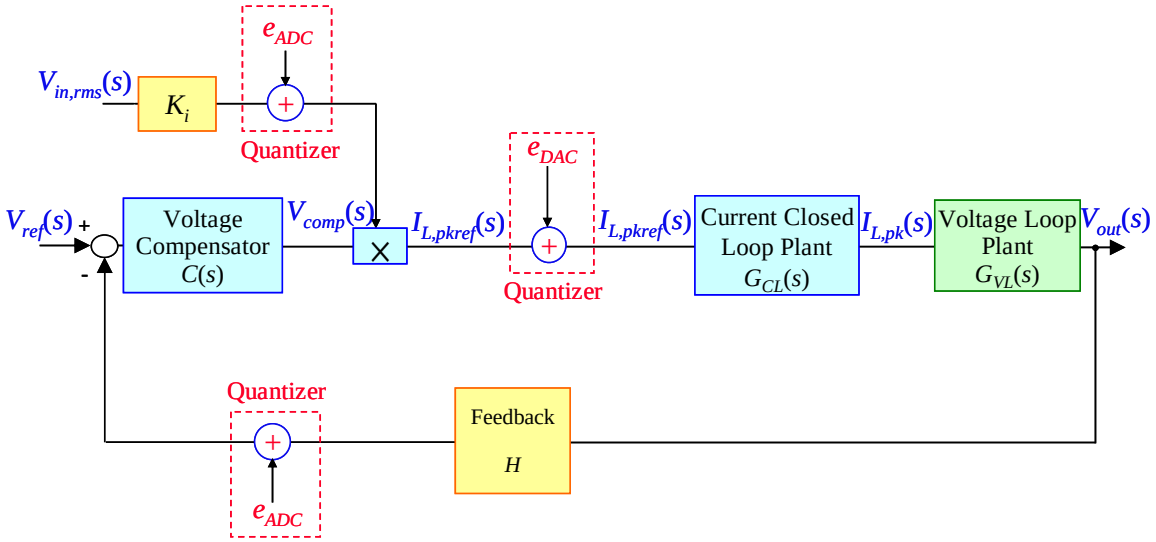


Fig. 3.15. The mixed-signal control system block diagram includes quantization noises.

In this thesis, the purposed mixed-signal control system can be represented as Fig. 3.15 by substituting the quantizer with the error model. Because the both ADC and DAC quantization errors induce the harmonic distortion into the line current, the proper resolutions for ADC and DAC are important issues. The main objective of this section is to quantify these ADC and DAC resolutions, as required to meet the harmonic regulation.

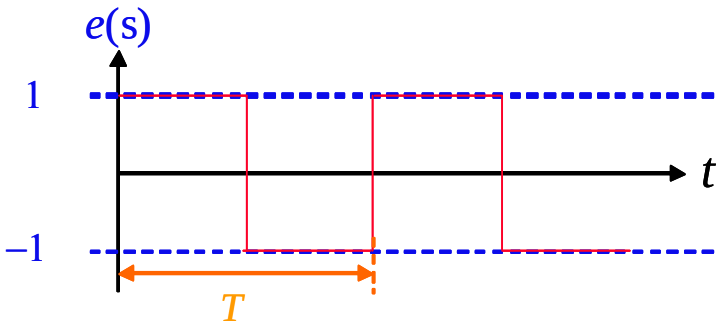
In order to determine the level of introduced harmonic components, two kinds of regular shape waveforms are used to represent the error signal. And the resolution can be found out by calculating the fundamental part of this regular shape waveform. Two regular shapes are discussed.

Square waveform

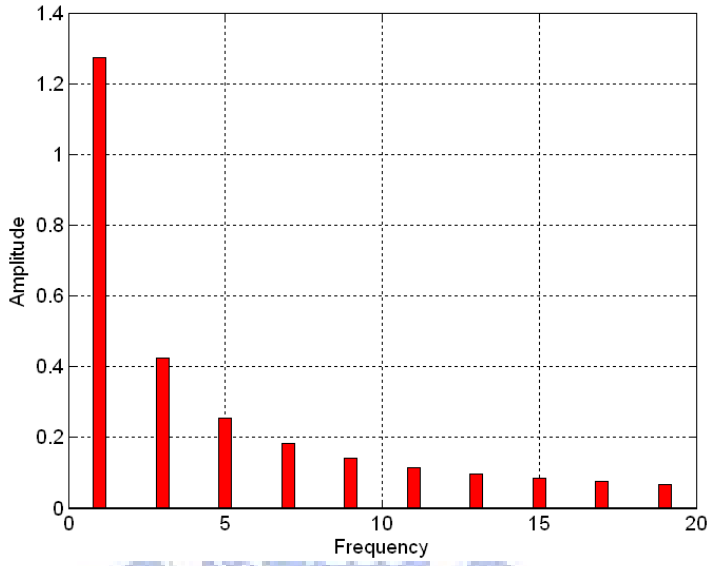
For a square waveform of frequency *f*, the harmonic components are found by Fourier series as follows

$$a_n = \begin{cases} \dfrac{4}{n \cdot \pi} & , n = odd \\ 0 & , n = even \end{cases} \tag{3-6}$$

where a_n is the amplitude of harmonic components and n is the harmonic order. The square error waveform and harmonic ratio are shown in Fig. 3.16.



(a)



(b)

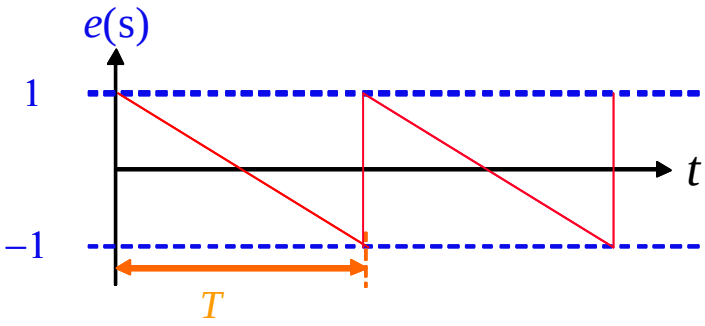
Fig. 3.16. (a) Square error waveform and (b) harmonic ratio.

Saw tooth waveform

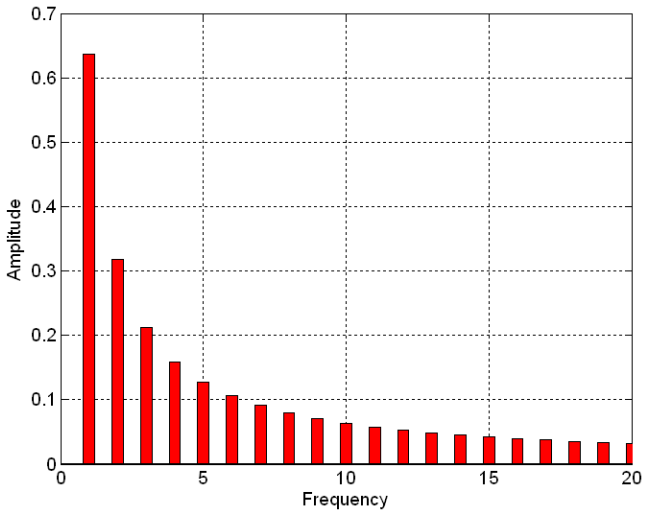
For a saw tooth waveform of frequency *f*, the harmonic components are as follows by Fourier series

$$a_n = \frac{2}{n \cdot \pi} \quad , n = 1,2,3\cdots \tag{3-7}$$

where a_n is the amplitude of each harmonic components and n is the harmonic order. The saw tooth error waveform and the harmonic ratio are show in Fig. 3.17.



(a)



(b)

Fig. 3.17. (a) Saw tooth error waveform and (b) harmonic components.

And the square error waveform will introduce the maximum harmonic distortion with the worst harmonic amplitude of the error signal.

$$\left|e_{ADC}(j\omega)\right|_{\max} = \frac{4}{\pi}\cdot\frac{\Delta}{2} \tag{3-8}$$

$$\left|e_{DAC}(j\omega)\right|_{\max} = \frac{4}{\pi}\cdot\frac{\Delta}{2} \tag{3-9}$$

From above error estimation equations, the adequate resolution for this mixed-signal CRM PFC AC-DC converter can be calculated.

3.2.3.1 Rectified Line Voltage ADC Resolution

The main purpose in PFC converter is forced the line current tracking the line voltage, a rectified sinusoidal waveform. The rectified line voltage is sampled for giving the shape of the current reference. For reducing the harmonic distortions in line current, the ADC resolution of the rectified line voltage feedback should be high enough to eliminate the noise from quantization error as shown in Fig. 3.18.

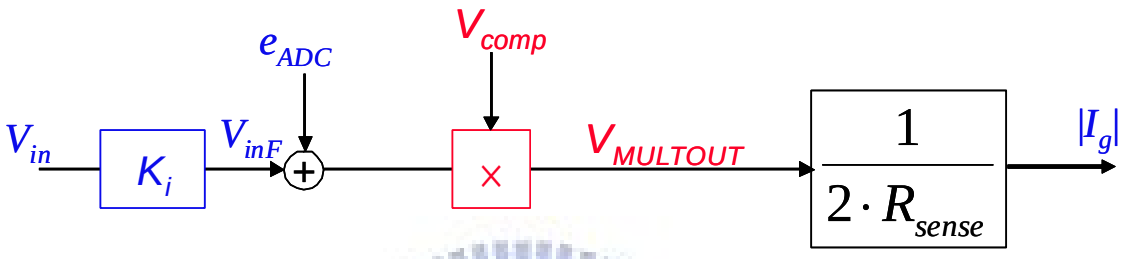


Fig. 3.18. Quantization noise from ADC resolution of rectified line voltage feedback.

Assuming the current loop bandwidth is much higher than line frequency, the inductor current will track the current command, $V_{multout}$, immediately. Then the relationship between quantization noise of rectified line voltage feedback and line current waveform can be derived as follows

$$\left|\tilde{i}_g\right| = \left|e_{ADC}(j\omega)\right|_{\max} \cdot V_{comp} \cdot \frac{1}{2 \cdot R_{sense}}. \tag{3-10}$$

Though the amplitude and frequency of the quantization noise introduced by ADC of the rectified line voltage feedback varies under different conditions, $|e_{ADC}(j\omega)|$ has a maximum amplitude as (3-8). At low frequency condition, the above equation can be arranged as

$$\left|\tilde{i}_g\right| = \frac{4}{\pi} \cdot \frac{\Delta}{2} \cdot V_{comp} \cdot \frac{1}{2 \cdot R_{sense}} \tag{3-11}$$

TABLE 3.1
LIMITS FOR CLASS C EQUIPMENT IN EN 61000-3-2

Harmonic order n	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency %
2	2
3	30×λ*
5	10
7	7
9	5
11 ≦ n ≦ 39	3
(Odd harmonics only)	
* λ is the circuit power factor	

Table 3.1 shows the EN 6100-3-2 Class C requirement. The lowest limit of line current harmonic RMS value varies by different line current RMS value and the minimum value is 3 % of line current RMS value.

$$\frac{4}{\pi}\cdot\frac{\Delta}{2}\cdot V_{comp}\cdot\frac{1}{2\cdot R_{sense}}\le\frac{P_{out}}{\eta\cdot V_{in,rms}}\cdot\frac{3}{100}\cdot\sqrt{2} \tag{3-12}$$

Recombining the (3-12), the relationship between resolution and ratio of rectified line voltage feedback can be found out.

$$\Delta\le\frac{\pi}{2}\cdot K_i\cdot V_{in,pk}\cdot\frac{3}{100} \tag{3-13}$$

The worst case occurs at minimum RMS value of line voltage. If K_i is 0.0052, the minimum resolution should be lower than 0.025. This is equivalent to 8-bit resolution. From Fig. 3.19, the required ADC resolution can be also revealed that the required resolution is 8-bit.

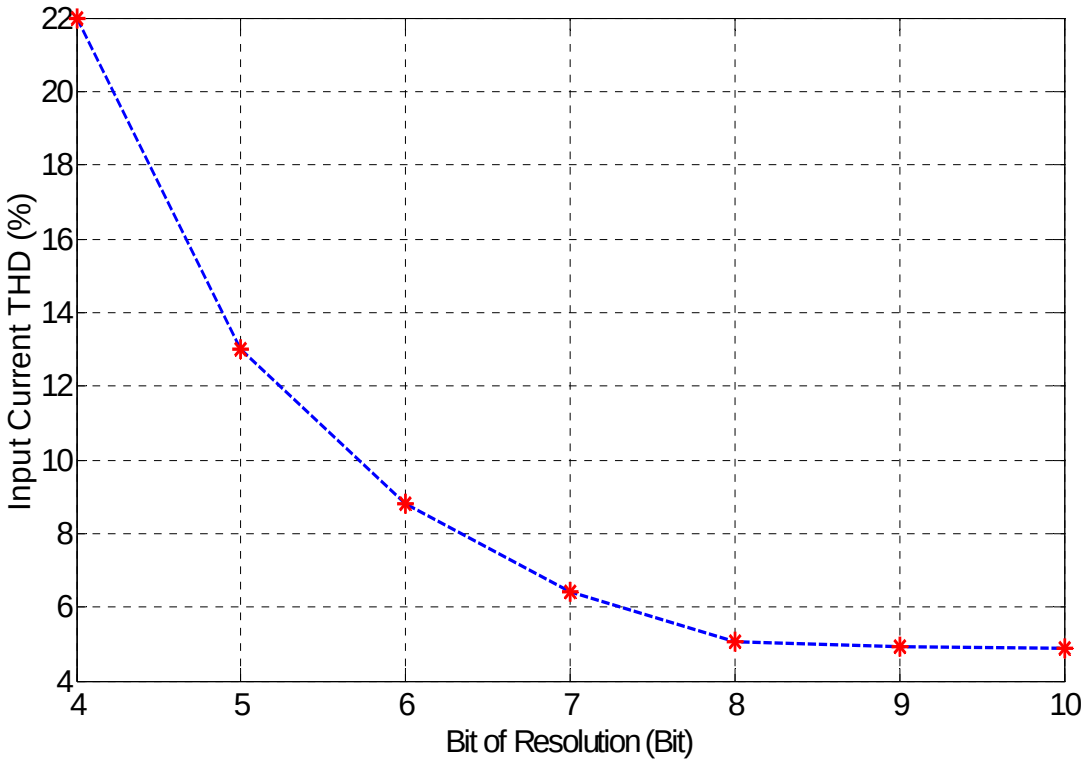


Fig. 3.19. The relationship between ADC resolutions and line current THD.

3.2.3.2 Output Voltage ADC Resolution

The purpose of negative feedback of the output voltage is forcing the output voltage to track the voltage reference. The ADC resolution induces error component into the output voltage. The quantization noise introduces to voltage controller is shown in Fig. 3.20.

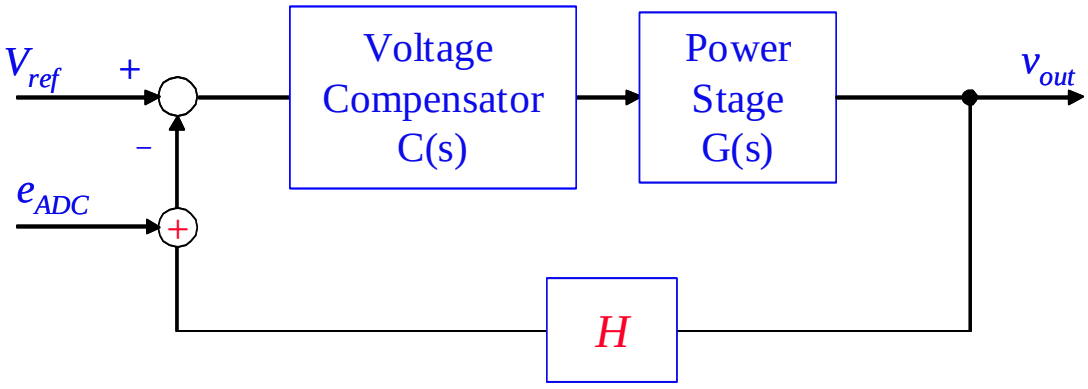


Fig. 3.20. Noise introduced by ADC of output voltage feedback.

From Fig. 3.20, the relationship between quantization noise and output voltage is derived as below

$$\tilde{v}_{out} = e_{ADC} \cdot \frac{C \cdot G}{1 + C \cdot G \cdot H}\bigg|_{V_{ref}=0} \tag{3-14}$$

At low frequency range $f << f_s$, (3-14) can rewrite as

$$\left|\tilde{v}_{out}\right|_{\max} \approx \frac{4}{\pi} \cdot \frac{\Delta}{2} \cdot \frac{1}{H} \tag{3-15}$$

Assuming the variation of output voltage should be limited below the ratio of the output voltage ripple to output voltage dc value, 0.4 %.

$$\frac{4}{\pi} \cdot \frac{\Delta}{2} \cdot \frac{1}{H} \le \frac{0.4}{100} \cdot 400 \tag{3-16}$$

When H = 0.00625, the minimum ratio of output voltage error to output voltage dc value is 1.57 %. This is equivalent to 8-bit resolution.

3.2.3.3 DAC Resolution of Current Command

The DAC truncates the digital current command back into analog. Fig. 3.21 shows the noise introduced by DAC. Assuming the current loop bandwidth is much higher than line frequency, the inductor current will track the current command, $V_{multout}$, immediately. Then the relationship between quantization noise of rectified line voltage feedback and line current waveform can be derived as follows

$$\left|\tilde{i}_g\right| = \left|e_{\mathrm{DAC}}(j\omega)\right|_{\max} \cdot \frac{1}{2 \cdot R_{sense}} \tag{3-17}$$

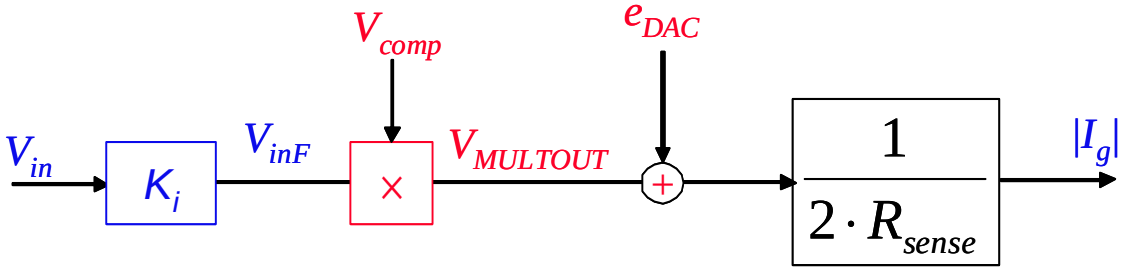


Fig. 3.21. Noise introduced by DAC.

From Fig. 3.21 and Table 3.1, the lowest limit of line current harmonic RMS value varies by different line current RMS value and the minimum value is 3 % of line current RMS value.

$$\Delta \le \pi \cdot R_{sense} \cdot \frac{P_{out}}{\eta \cdot V_{in,rms}} \cdot \frac{3}{100} \cdot \sqrt{2} \tag{3-18}$$

The worst case occurs at minimum operating power and maximum line voltage. Then the minimum resolution should be lower than 0.4 %. This is equivalent to 10-bit resolution.

Chapter 4

Discrete Small-Signal Analysis and Controller Design of Digital Voltage Loop

This chapter discusses an average small-signal model of CRM PFC AC-DC converter. The design flow of this digital voltage controller will be given to adapt widely load variations. The control architecture purposes to achieve adequately phase margin and improve dynamic responses. For ensuring a stable and fast dynamic responses over a widely load variations of steady-state conditions, the digital notch filter and load adaptive gain scheduling are applied for CRM PFC AC-DC converter in this thesis.

4.1 Discrete Time Small-Signal Model of Voltage Loop

To the aim of finding a digital voltage controller able to achieve high power factor and low harmonic distortion, it is necessary to get an insight into the mixed-signal CRM PFC AC-DC converter. Fig. 4.1 shows the mixed-signal control architecture of boost CRM PFC. The voltage controller gives the current command. Then, current control loop forced the inductor current to track the current command. The power stage converts the output current to output voltage. The overall block diagram of the mixed-signal CRM PFC AC-DC converter is shown in Fig. 4.2 [22]-[24].

The average small-signal method is used to model the CRM PFC AC-DC converter. In this thesis, the line current is assumed to track the line voltage correctly, and the circuit is analyzed on an average basis over a line period. This analysis is essential for the proper design of the feedback circuit, which regulates the output voltage of the power factor circuit.

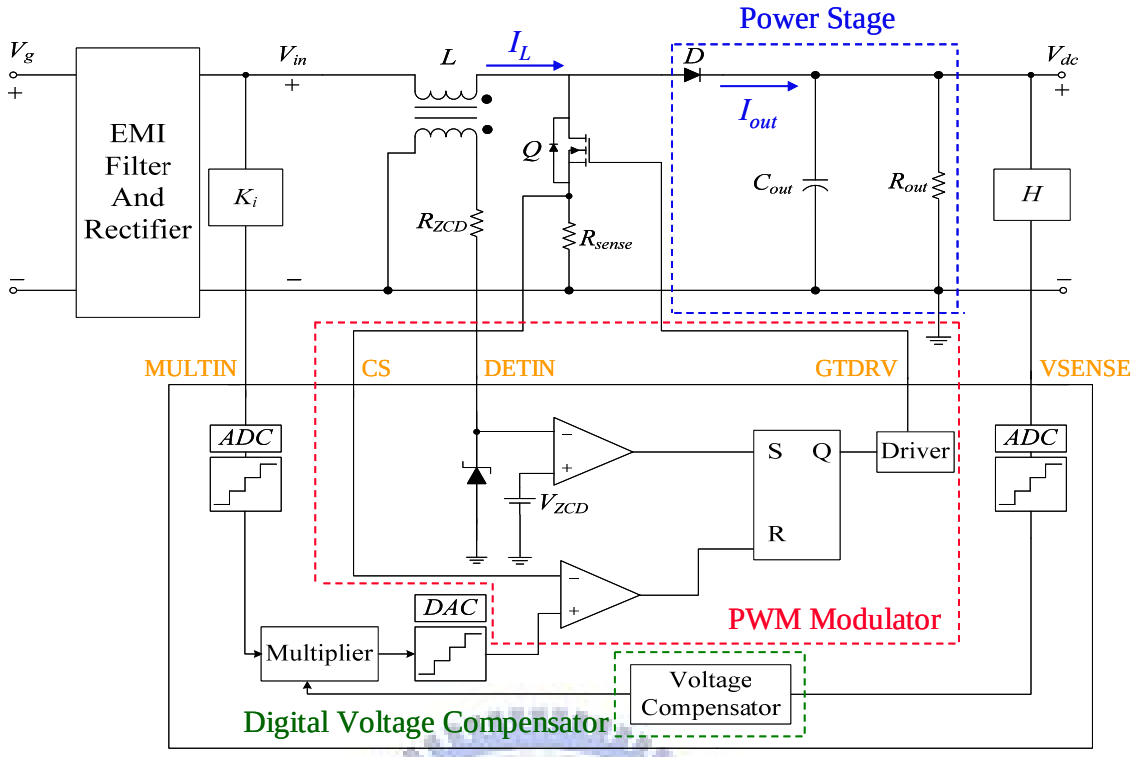


Fig. 4.1. Mixed-signal control structure of the mixed-signal CRM PFC AC-DC converter.

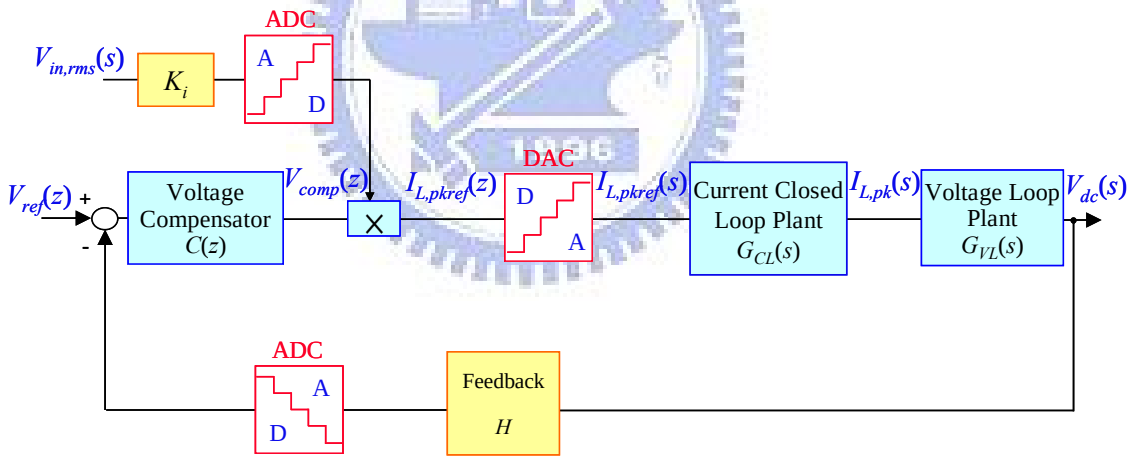


Fig. 4.2. The overall block diagram of the mixed-signal CRM PFC AC-DC converter.

The voltage control loop is to eliminate the output voltage steady-state error. For designing the voltage control loop, the transfer function from the output of voltage compensator to the output voltage is a significant issue. The control loop of CRM PFC AC-DC converter concerns from the output of voltage compensator to the output voltage at first.

The output voltage is assumed to be constant over a switching period, and the output

current is chopped at high frequency with a sinusoidal envelope equal to that of the line current. The input power is fully transferring to output power. And so on, the power balance equation for a line period is

$$v_{g,rms} \cdot i_{g,rms} = v_{out} \cdot i_{out} \tag{4-1}$$

where v_{out} is the dc output voltage and i_{out} is the average current over a line period. For the current control loop, line-reference control, the controller governing the line current is

$$i_{g,rms} = \frac{v_{g,rms} \cdot K_i}{2 \cdot R_{sense}} \cdot V_{comp} \tag{4-2}$$

substituting the (4-2) into (4-1) gives

$$\left(\frac{v_{out}}{v_{g,rms}} \right)^2 = \frac{v_{out}}{i_{out}} \cdot \frac{K_i \cdot V_{comp}}{2 \cdot R_{sense}}. \tag{4-3}$$

Then, this thesis defines the steady-state conversion ratio (M) of the CRM system.

$$M = \frac{V_{out}}{V_{g,rms}} = \sqrt{\frac{V_{out}}{I_{out}} \cdot \frac{K_i \cdot V_{comp}}{2 \cdot R_{sense}}} \tag{4-4}$$

The ratio of V_{out} to I_{out} can be defined as

$$r_{out} = \frac{V_{out}}{I_{out}}. \tag{4-5}$$

The small-signal disturbances can be added into each factor such as line voltage, line current, output voltage, output current, and output of voltage compensator. Each element can be expressed as the combination of a dc component and an ac part.

$$\begin{cases} v_{g,rms} = V_{g,rms} + \hat{v}_{g,rms} \\ i_{g,rms} = I_{g,rms} + \hat{i}_{g,rms} \\ v_{out} = V_{out} + \hat{v}_{out} \\ i_{out} = I_{out} + \hat{i}_{out} \\ v_{comp} = V_{comp} + \hat{v}_{comp} \end{cases} \tag{4-6}$$

Substituting the above equations into (4-1) gives

$$\frac{\left(V_{g,rms}+\hat{v}_{g,rms}\right)^2}{2\cdot R_{sense}}\cdot K_i\cdot\left(V_{comp}+\hat{v}_{comp}\right)=\left(V_{out}+\hat{v}_{out}\right)\cdot\left(I_{out}+\hat{i}_{out}\right). \tag{4-7}$$

Eliminating small-signal high order terms and dc components yields the above equation as

$$\hat{i}_{out}=\frac{2\cdot M}{r_{out}}\cdot\hat{v}_{g,rms}+\frac{V_{g,rms}\cdot K_i}{2\cdot M\cdot R_{sense}}\cdot\hat{v}_{comp}-\frac{1}{r_{out}}\cdot\hat{v}_{out}. \tag{4-8}$$

The (4-2) can be similarly perturbed to give

$$I_{g,rms}+\hat{i}_{g,rms}=\frac{\left(V_{g,rms}+\hat{v}_{g,rms}\right)}{2\cdot R_{sense}}\cdot K_i\cdot\left(V_{comp}+\hat{v}_{comp}\right). \tag{4-9}$$

Then, eliminating small-signal cross-products and dc components simplifies (4-9) as

$$\hat{i}_{g,rms}=\frac{V_{g,rms}}{2\cdot R_{sense}}\cdot K_i\cdot\hat{v}_{comp}+\frac{M^2}{r_{out}}\cdot\hat{v}_{g,rms}. \tag{4-10}$$

According to (4-8) and (4-10), the small-signal circuit model can be shown in Fig.4.3.

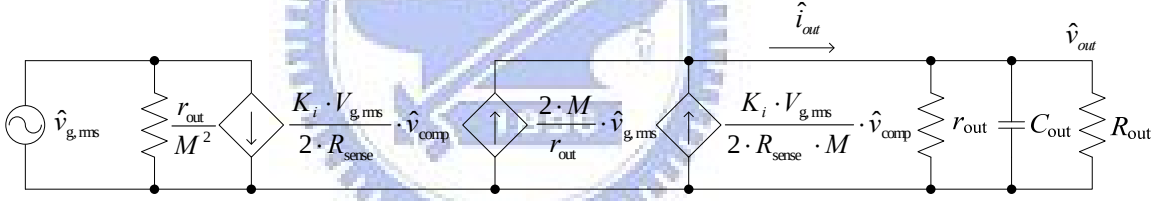


Fig. 4.3. Average small-signal circuit model of CRM PFC AC-DC converter.

Notice that this circuit is not a simple controlled current source feeding the output load, due to the presence of the equivalent resistor (r_{out}). The transfer function of the current closed loop plant can be found out

$$G_{CCL}(s)=\frac{\hat{i}_{out}}{\hat{v}_{comp}}=\frac{K_i\cdot V_{g,rms}}{2\cdot R_{sense}}\cdot\frac{1}{\sqrt{\frac{K_i}{2\cdot R_{sense}}\cdot V_{comp}\cdot r_{out}}}. \tag{4-11}$$

The transfer function of the voltage loop plant is also given

$$G_{PS}(s)=\frac{\hat{v}_{out}}{\hat{i}_{out}}=\frac{\left(r_{out}\,//\,R_{out}\right)}{1+s\cdot C_{out}\cdot\left(r_{out}\,//\,R_{out}\right)}. \tag{4-12}$$

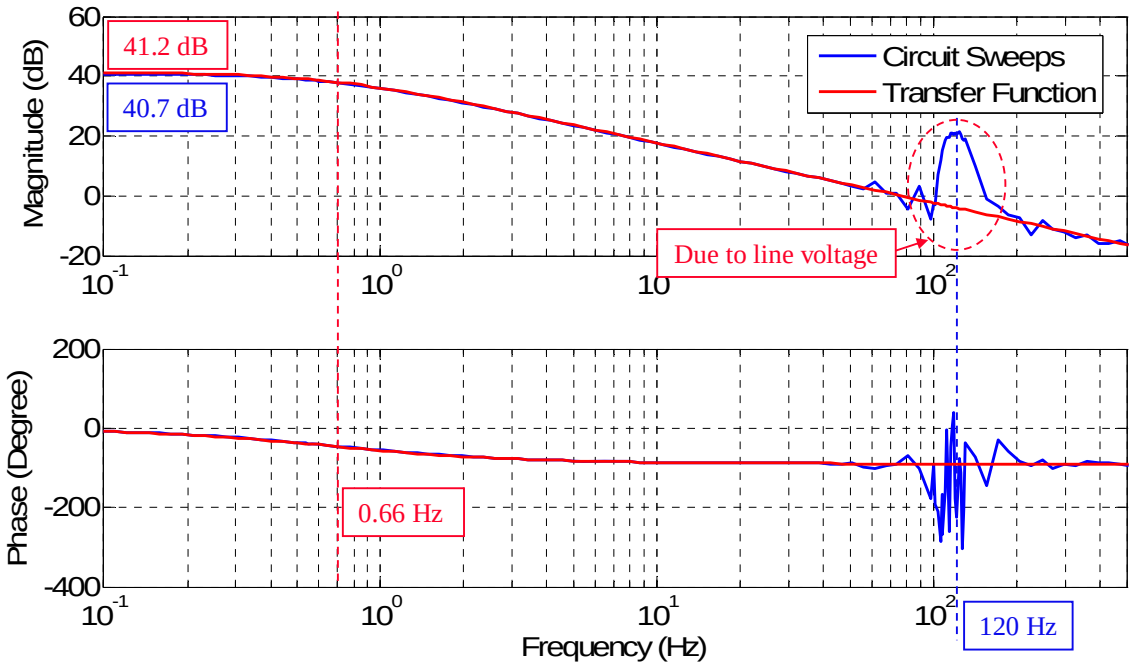


Fig. 4.4. Frequency response of transfer function compares with circuit sweeps.

For a resistive load, the equivalent resistance (r_o) is equal to the load resistance (R_{out}). The total transfer function of the current closed loop and the voltage loop plant can be represented as

$$G_{CO}(s) = \frac{\hat{v}_{out}}{\hat{v}_{comp}} = \frac{K_i \cdot V_{g,rms}^{\ 2}}{2 \cdot V_{out} \cdot R_{sense}} \cdot \frac{R_{out}}{2 + s \cdot R_{out} \cdot C_{out}}. \quad (4\text{-}13)$$

From (4-13), it is apparent that the gain of the control-to-output function is strongly dependent on the line voltage RMS value. To achieve the design purpose, $G_{CO}(s)$ will be considered in the maximum line voltage condition, where the loop gain and the loop bandwidth are both maximum values. The frequency response of the control-to-output transfer function, $G_{CO}(s)$, compares with the frequency response of the circuit sweep as shown in Fig. 4.4.

The application of any kind of discretization method always implies a loss of performance with respect to a purely analog control implementation. There are many methods of conversion methods which are distinguished by different integral methods, such as

"forward Euler integration," "backward Euler integration," and "trapezoidal integration." In *s*-domain, it is difficult to model the sample and hold function of ADC and the computation delay. So designing an analog compensator may not be a good idea. Although the analog voltage controller is accurate, converting it into discrete plant may compromise its performance. And so on, this thesis designs the voltage controller directly in the *z*-domain.

For modeling the sample-and-hold delay function, the relationship between input signal, $s(t)$, and output signal, $s_o(t)$, of the sample-and-hold block is given

$$\begin{aligned} s_o(t) = {} & s(0)\cdot[u(t)-u(t-T_{sample})]+s(T_{sample})\cdot[u(t-T_{sample})-u(t-2\cdot T_{sample})] \\ & +s(2\cdot T_{sample})\cdot[u(t-2\cdot T_{sample})-u(t-3\cdot T_{sample})]+\cdots \end{aligned} \tag{4-14}$$

where $u(t)$ is the unit step function. The Laplace transform of above equation is as follow

$$S_o(s) = \left[\sum_{n=0}^{\infty} s(n\cdot T_{sample})\cdot e^{-n\cdot T_{sample}}\right]\cdot\frac{1-e^{-T_{sample}\cdot s}}{s} \tag{4-15}$$

The forward part of (4-15) is a function of the input signal and the sampling period. And the backward factor is independent of the input signal. Then the effect of the sample-and-hold function, $G_{SH}(s)$, can be determined as

$$G_{SH}(s) = \frac{1-e^{-T_{sample}\cdot s}}{s} \tag{4-16}$$

For discretizing the transfer function of the control-to-output transfer function with sample-and-hold function, Fig. 4.5 shows the procedure. The first step is combining $G_{CO}(s)$ and $G_{SH}(s)$.

$$G_{CO}(s)\cdot G_{SH}(s) = \frac{K_i\cdot {V_{g,rms}}^2}{2\cdot V_{dc}\cdot R_{sense}}\cdot\frac{R_{out}}{2+s\cdot R_{out}\cdot C_{out}}\cdot\frac{1-e^{-T_{sample}\cdot s}}{s} \tag{4-17}$$

The function , $(1-e^{-T_{sample}\cdot s})$, can be directly transfering into z-domain as $(1-z^{-1})$. Therefore, the above equation can be separated into two parts.

$$G_{SHD}(s) = 1-e^{-T_{sample}\cdot s} \tag{4-18}$$

and

$$G_{COS}(s) = \frac{K_i \cdot {V_{g,rms}}^2}{2 \cdot V_{dc} \cdot R_{sense}} \cdot \frac{R_{out}}{2 + s \cdot R_{out} \cdot C_{out}} \cdot \frac{1}{s}. \tag{4-19}$$

Then, $G_{COS}(s)$ is converted back to continuous time domain by inverse Laplace transform.

$$G_{COS}(t) = \frac{K_i \cdot {V_{g,rms}}^2 \cdot R_{out}}{4 \cdot V_{dc} \cdot R_{sense}} \cdot \left[1 - e^{-\frac{2}{R_{out} \cdot C_{out}} \cdot t}\right] \tag{4-20}$$

The continuous time domain can be convertered to discrete time domain.

$$G_{COS}(n \cdot T_{sample}) = \sum_{n=0}^{\infty} \frac{K_i \cdot {V_{g,rms}}^2 \cdot R_{out}}{4 \cdot V_{dc} \cdot R_{sense}} \cdot \left[1 - e^{-\frac{2}{R_{out} \cdot C_{out}} \cdot n \cdot T_{sample}}\right] \tag{4-21}$$

Transferring the above function from discrete time domain to z-domain

$$\begin{aligned} G_{COS}(z) &= \sum_{k=0}^{\infty} G_{COS}(k \cdot T_{sample}) \cdot z^{-k} \\ &= \frac{K_i \cdot {V_{g,rms}}^2 \cdot R_{out}}{4 \cdot V_{dc} \cdot R_{sense}} \cdot \frac{z^{-1} \cdot \left(1 - e^{-\frac{2}{R_{out} \cdot C_{out}} \cdot T_{sample}}\right)}{\left(1 - z^{-1}\right) \cdot \left(1 - e^{-\frac{2}{R_{out} \cdot C_{out}} \cdot T_{sample}} \cdot z^{-1}\right)} \end{aligned} \tag{4-22}$$

Finally, the discrete time model of the control-to-output will be given

$$\begin{aligned} G_{COD}(z) &= G_{COS}(z) \cdot G_{SHD}(z) \\ &= \frac{K_i \cdot {V_{g,rms}}^2 \cdot R_{out}}{4 \cdot V_{dc} \cdot R_{sense}} \cdot \frac{z^{-1} \cdot \left(1 - e^{-\frac{2}{R_{out} \cdot C_{out}} \cdot T_{sample}}\right)}{1 - e^{-\frac{2}{R_{out} \cdot C_{out}} \cdot T_{sample}} \cdot z^{-1}}. \end{aligned} \tag{4-23}$$

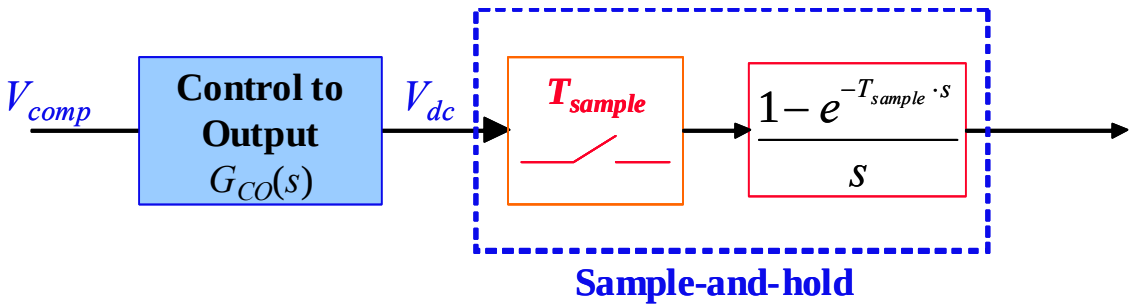


Fig. 4.5. The control-to-output transfer function with sample-and-hold.

The discrete model gives nearly the same frequency response with the continuous model with sample and hold when the frequency of sampled signal is below half of the sampling frequency. Fig. 4.6 shows the comparison of the discrete model with different integral ways and the continuous model.

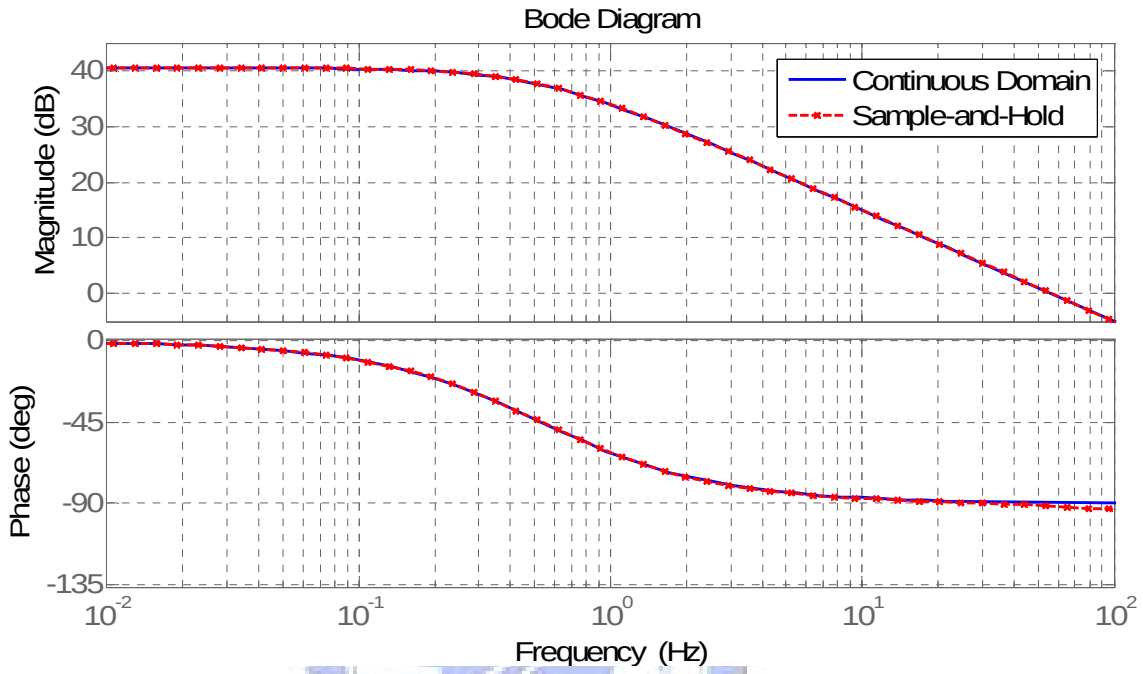


Fig. 4.6. Comparison of the discrete model and continuous model.

4.2 DESIGN OF DIGITAL VOLTAGE CONTROLLER

4.2.1 Design of Voltage Compensator

For designing the digital control compensator, the effect of the output voltage ripple on inductor current command should be concerned at first. Fig. 4.7 shows that the output voltage ripple will be introduced into the output of voltage compensator (V_{comp}). This ripple induced harmonic components in the inductor current command ($V_{multout}$) [21].

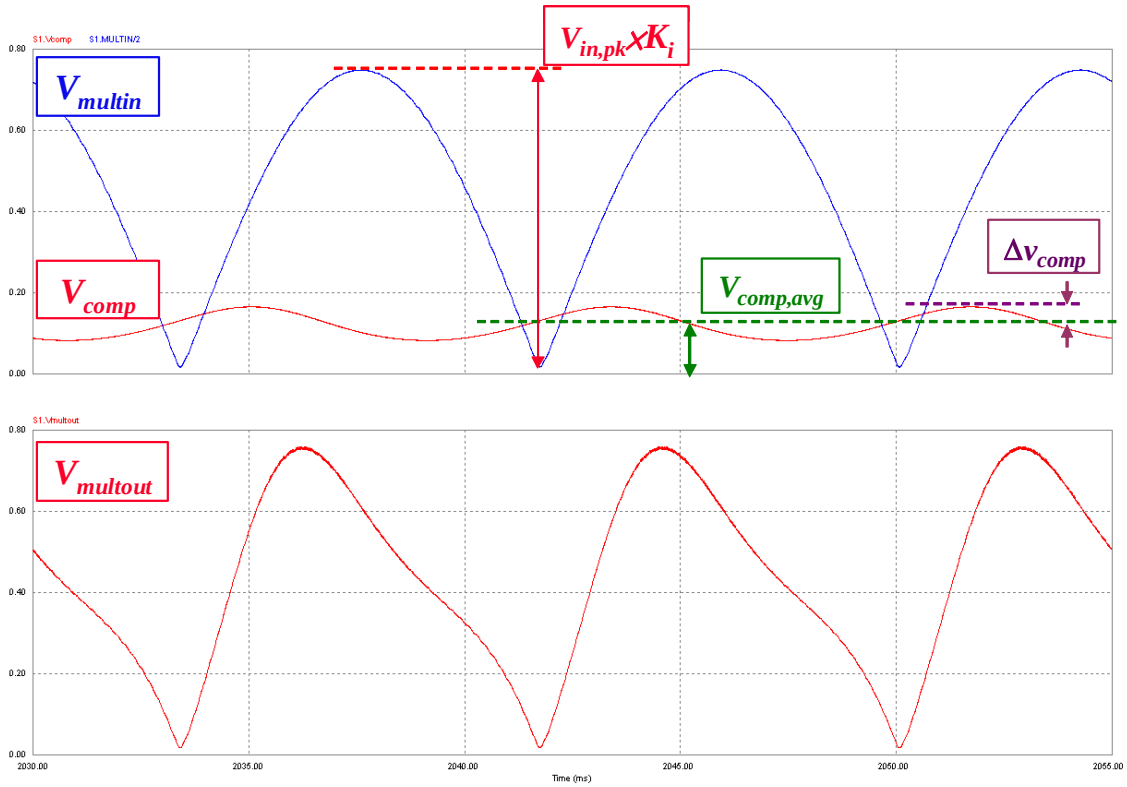


Fig. 4.7. The effect of output voltage ripple on inductor current command.

The feedback of rectified line voltage and the output of the voltage compensator can be represented as follows

$$\begin{cases} V_{multin}(\theta) = K_i \cdot V_{in,pk} \cdot \sin\theta \\ V_{comp}(\theta) = V_{comp,avg} + \Delta v_{comp} \cdot \sin(2\theta) \end{cases} \tag{4-25}$$

The output of multiplier ($V_{multout}$) will equal to the product of V_{multin} and V_{comp} can be given

$$\begin{aligned} V_{multout}(\theta) &= V_{comp,avg} \cdot K_i \cdot V_{in,pk} \cdot \sin\theta + 2 \cdot \Delta v_{comp} \cdot K_i \cdot V_{in,pk} \cdot \cos\theta \cdot \sin^2\theta \\ &= V_{comp,avg} \cdot K_i \cdot V_{in,pk} \cdot \sin\theta \cdot \left[1 + 2 \cdot \frac{\Delta v_{comp}}{V_{comp,avg}} \cdot \cos\theta \cdot \sin\theta \right]. \end{aligned} \tag{4-26}$$

The relationship between the normalized output voltage ripple of voltage compensator and the THD of the inductor current command is an important issue.

$$
\begin{aligned}
V_{multout,rms} &= \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi} V_{multout}{}^2(\theta)d\theta} \\
&= V_{comp,avg}\cdot K_i \cdot V_{in,pk}\cdot\sqrt{\frac{1}{\pi}\cdot\int_0^{\pi}\sin^2\theta\cdot\left[1+2\cdot\frac{\Delta v_{comp}}{V_{comp,avg}}\cdot\cos\theta\cdot\sin\theta\right]^2 d\theta} \\
&= V_{comp,avg}\cdot K_i \cdot V_{in,pk}\cdot\sqrt{\frac{1}{2}+\frac{1}{2}\cdot\left(\frac{\Delta v_{comp}}{V_{comp,avg}}\right)^2}
\end{aligned}
\tag{4-27}
$$

The fundamental component of the inductor current command can be noticed by Fourier series.

$$
\begin{aligned}
V_{multout1,rms} &= \frac{1}{\sqrt{2}}\cdot\frac{2}{\pi}\cdot\int_0^{\pi}\left[V_{multout}(\theta)\cdot\sin\theta\right]d\theta \\
&= \frac{1}{\sqrt{2}}\cdot V_{comp,avg}\cdot K_i\cdot V_{in,pk}\cdot\frac{2}{\pi}\cdot\int_0^{\pi}\sin^2\theta\cdot\left[1+2\cdot\frac{\Delta v_{comp}}{V_{comp,avg}}\cdot\cos\theta\cdot\sin\theta\right]d\theta \\
&= \frac{1}{\sqrt{2}}\cdot V_{comp,avg}\cdot K_i\cdot V_{in,pk}
\end{aligned}
\tag{4-28}
$$

And so on, the THD of the inductor current command can be got.

$$
\begin{aligned}
THD &= \frac{\sqrt{V_{multout,rms}{}^2 - V_{multout1,rms}{}^2}}{V_{multout1,rms}} \\
&= \frac{\Delta v_{comp}}{V_{comp,avg}}
\end{aligned}
\tag{4-29}
$$

If given a maximum acceptable THD of 10 % at the rated output power, (4-27) means that the normalized inductor current command ripple should be smaller than 10 %. Selecting the voltage compensator gain at 120 Hz should be based on this criterion. The design of the digital voltage compensator of CRM PFC controller significantly influences the performance of the circuit in terms of the THD of the line current. Although lower bandwidth can effectively eliminate the influence of output voltage ripple on current command, it will also reduce the dynamic response. The proper bandwidth is concerned. For eliminating the steady-state error and regulating bandwidth, the proportional-integral (PI) controller is selected in this thesis. The voltage loop with digital voltage compensator is shown in Fig. 4.8.

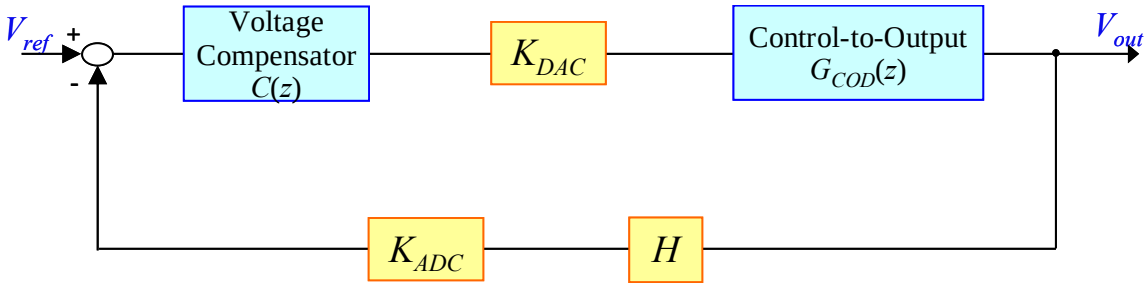


Fig. 4.8. The block diagram of digital voltage control loop.

The following equations are derived in Fig. 4.8.

$$C(z) = K_P \cdot \frac{z + A_v}{z - 1} \tag{4-30}$$

$$K_{ADC} = \frac{2^{B_{ADC}} - 1}{V_{ref,ADC}} \tag{4-31}$$

$$K_{DAC} = \frac{V_{ref,DAC}}{2^{B_{DAC}} - 1} \tag{4-32}$$

where B_{ADC} = 8 for bit resolution of ADC of output voltage feedback, $V_{ref,ADC}$ = 3.3 V for reference voltage of ADC of output voltage feedback, B_{DAC} = 10 for bit resolution of DAC, $V_{ref,DAC}$ = 3.3 V for reference voltage of DAC, and H = 0.00625 for feedback gain of output voltage.

For the requirement given in section 4.2.3.1, the distortion requirement of current command is obtained

$$\Delta v_{comp} \le 10\% \cdot V_{comp.avg} = 10\% \cdot \frac{2 \cdot P_{out} \cdot R_{sense} \cdot K_{ADC} \cdot K_{DAC}}{\eta \cdot V_{g,rms}^{\ 2} \cdot K_i}. \tag{4-33}$$

Furthermore, the ripple of voltage compensator output can be represented as

$$\Delta v_{comp} = \Delta V_{dc,ripple} \cdot H \cdot K_{ADC} \cdot K_{DAC} \cdot \left| C(e^{j2\omega_{line} T_{sample}}) \right|. \tag{4-34}$$

From chapter 2, the output voltage ripple can be known.

$$\Delta V_{dc,ripple} = \frac{P_{out}}{C_{out} \cdot \omega_{line} \cdot V_{dc}}. \tag{4-35}$$

Following (4-33), the gain of the digital voltage compensator at $2\omega_{line}$ should satisfy

$$\left|C(e^{j2\omega_{line}T_{sample}})\right| \cong K_P \le 10\% \cdot \frac{2 \cdot P_{out} \cdot R_{sense}}{\Delta V_{dc,ripple} \cdot H \cdot \eta \cdot {V_{g,rms}}^2 \cdot K_i} \tag{4-36}$$
$$= 6.$$

The voltage open loop transfer function is

$$\begin{aligned} T_{vz}(z) &= C(z) \cdot K_{DAC} \cdot G_{COD}(z) \cdot H \cdot K_{ADC} \\ &= K_P \cdot \frac{z + A_v}{z - 1} \cdot z^{-1} \cdot 0.000024 \cdot {V_{g,rms}}^2 \cdot \frac{0.0007}{z - 0.9993}. \end{aligned} \tag{4-37}$$

There are two variables: the zero of voltage compensator A_v and the crossover frequency of voltage loop f_c. Assume the phase margin of voltage loop is 80 degrees.

$$\begin{cases} K_P = 6 \\ \angle T_{vz}(e^{j\omega_c T_{sample}}) = -180° + 80° \\ \left|T_{vz}(e^{j\omega_c T_{sample}})\right| = 1 \end{cases} \tag{4-38}$$

From (4-38), we have derived:

$$\begin{cases} K_P = 6 \\ \angle(e^{j\omega_c T_{sample}} - A_v) - \angle(e^{j\omega_c T_{sample}} - 1) - \angle(e^{j\omega_c T_{sample}} - 0.9993) = -100° \\ 0.0018 \cdot \dfrac{K_P \cdot \left|e^{j\omega_c T_{sample}} - A_v\right|}{\left|e^{j\omega_c T_{sample}} - 1\right| \cdot \left|e^{j\omega_c T_{sample}} - 0.9993\right|} = 1 \end{cases} \tag{4-39}$$

And so on, the parameters of the digital voltage compensator can be found by MATLAB.

$$\begin{cases} \omega_c = 56 rad/\sec \\ K_P = 6 \\ A_v = 0.996 \end{cases} \tag{4-40}$$

The bandwidth of this control system will be about 9 Hz. Therefore, the digital voltage compensator transfer function is

$$C(z) = 6 \cdot \frac{z - 0.996}{z - 1}. \tag{4-41}$$

Fig. 4.9 compares the frequency responses of voltage loop gain between circuit sweep and the transfer function calculating.

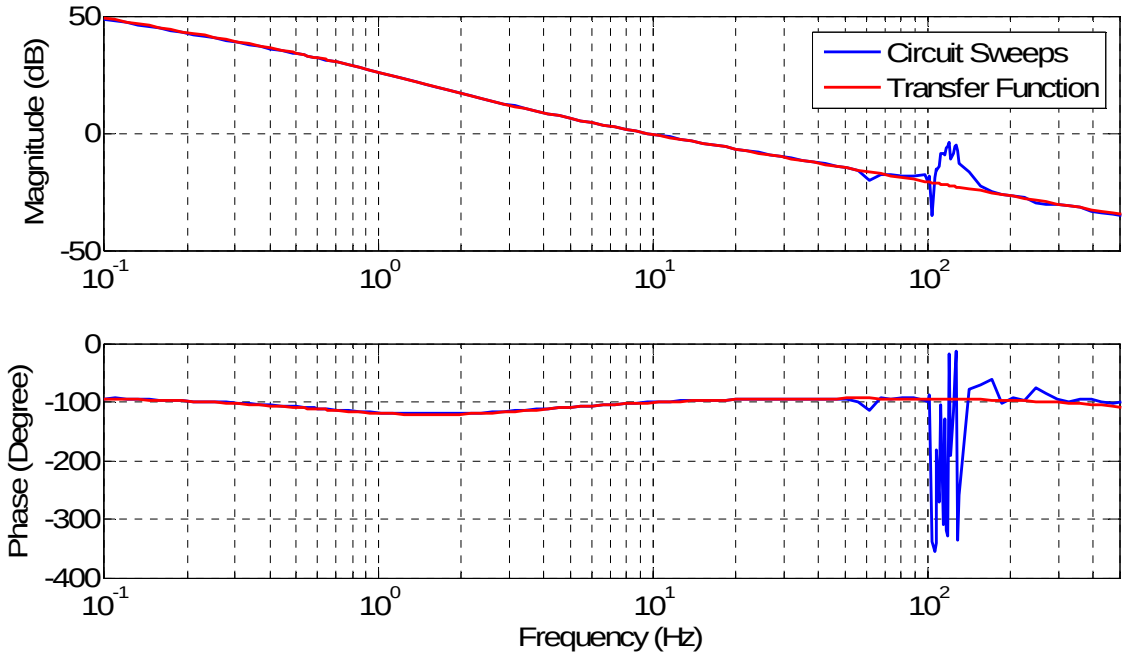


Fig. 4.9. Comparing frequency responses of loop gain between circuit sweeps and transfer function.

4.2.2 Design of Digital Notch Filter

From the result of previous section, the effect of the output voltage ripple induces lower voltage loop bandwidth. This paper adds a digital notch filter to eliminate the ripple effect on the input line current THD as shown in Fig. 4.10 [25]-[28]. The transfer function of a second-order notch filter in *s*-domain can be expressed as

$$N(s) = K_n \cdot \frac{s^2 + \lambda^2}{s^2 + bs + \lambda^2}. \tag{4-43}$$

When the notch filter center frequency $\omega_o = \lambda$, there is no signal transmission through the filter. And b is the 3 dB rejection bandwidth. Using the bilinear transformation to transfer $N(s)$ to z-domain as follow

$$N(z) = K_n \cdot \frac{(1+\lambda^2) - 2(1-\lambda^2)z^{-1} + (1+\lambda^2)z^{-2}}{(1+\lambda^2+b) - 2(1-\lambda^2)z^{-1} + (1+\lambda^2-b)z^{-2}} \tag{4-44}$$

The center frequency of the notch filter in z-domain can be obtained by setting the value of magnitude for zero, which yields the magnitude of the notch filter is dropped to 3 dB from the dc value of the notch filter in z-domain are found as follow

$$\cos(\omega_o T_{\text{sample}}) = \frac{1-\lambda^2}{1+\lambda^2} \tag{4-45}$$

Note that the frequencies ω_1 and ω_2 where the magnitude is determined by

$$\begin{aligned}\cos(\Omega T_{\text{sample}}) &= \cos[(\omega_2 - \omega_1)T_{\text{sample}}] \\ &= \frac{(1+\lambda^2)^2 - b^2}{(1+\lambda^2)^2 + b^2}\end{aligned} \tag{4-46}$$

where Ω is the 3 dB bandwidth of the notch filter. From (4-45) and (4-46), the λ and b can be determined as

$$\lambda = \sqrt{\tan^2(\frac{\omega_o T_{\text{sample}}}{2})} \tag{4-47}$$

$$b = (1+\lambda^2)\cdot\tan(\frac{\Omega T_{\text{sample}}}{2}) \tag{4-48}$$

The center frequency of notch filter is placed at the double line frequency, which is 120 Hz ($2\omega_{\text{line}} = \omega_o$), and the 3 dB bandwidth of the notch filter sets at 50 Hz. This thesis sets the parameters of the notch filter, which are λ = 0.038 and b = 0.159, to satisfy the requirement. Fig. 4.11 and Fig. 4.12 show the input line current without and with notch filter, the load variation sets a step current load, which changes from 50 % to 100 %. In Fig. 4.11, the output voltage transient time is 40 ms and the input line current THD is 20 %. When the notch filter is applied in the voltage loop, the transient time still maintains at 40 ms but the input line current THD can be improved down to 6 % as shown in Fig. 4.12.

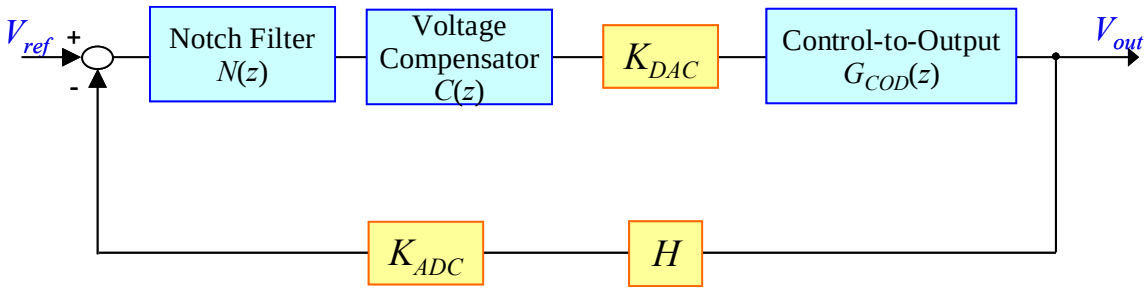


Fig. 4.10. Block diagram of the digital voltage control loop with notch filter.

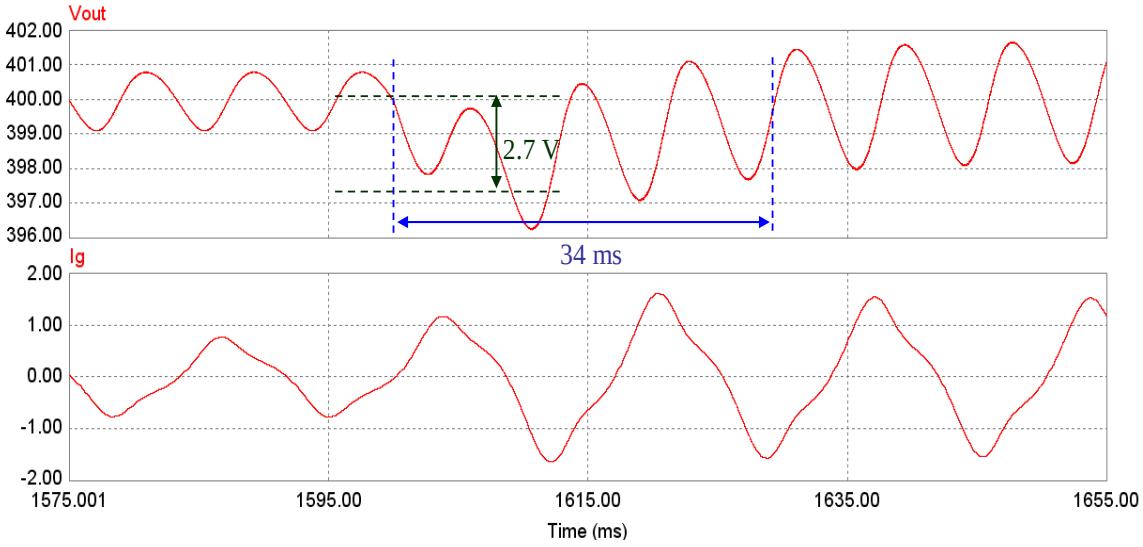


Fig. 4.11. The transient response of output voltage and input line current waveform without notch filter, load changes from 50 % to 100 %.

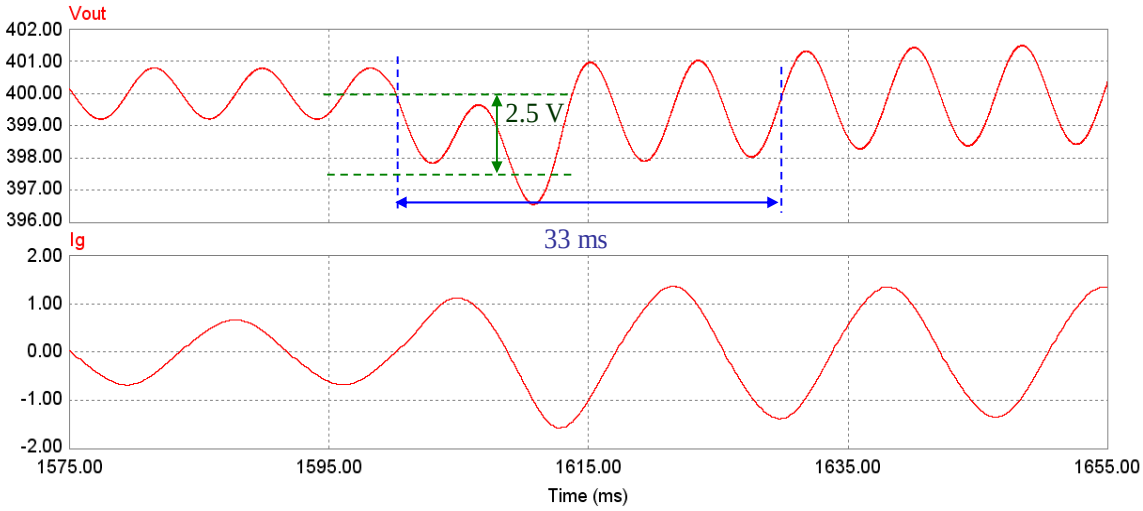


Fig. 4.12. The transient response of output voltage and input line current waveform with notch filter, load changes from 50 % to 100 %.

4.2.3 Design of Load Adaptive Gain Scheduling

From previous section discuss, added notch filter can increase voltage loop bandwidth and maintain the input line current low THD and high PF. But on different load conditions, the dynamic characteristics of the boost AC-DC converter have also different. Therefore, an adaptive control scheme is given to address different load variations for maintaining a stable and fast dynamic response. The load adaptive control scheme applies a look-up table to

estimate the modified gain, and the modified gain is determined by using linear interpolation method [29].

$$\alpha = \alpha(m) + \frac{\alpha(m+1) - \alpha(m)}{i_{\text{out}}(m+1) - i_{\text{out}}(m)} \cdot (i_{\text{out}} - i_{\text{out}}(m)) \tag{4-49}$$

$$\beta = \beta(m) + \frac{\beta(m+1) - \beta(m)}{i_{\text{out}}(m+1) - i_{\text{out}}(m)} \cdot (i_{\text{out}} - i_{\text{out}}(m)). \tag{4-50}$$

The look-up table of the modified factor of the digital PI controller is shown in Table 4.1 The digital PI controller with load adaptive gain scheduling can be modified as

$$C(z) = \alpha \cdot K_v \cdot \frac{z - \beta \cdot A_v}{z - 1}. \tag{4-51}$$

TABLE 4.1
LOAD LOOK-UP TABLE

Load (%)	10	30	50	70	90
i_{out} (A)	0.025	0.075	0.125	0.175	0.225
α	1	1.036.	1.072	1.108	1.114
β	1	1.0005	1.001	1.0015	1.002

Fig. 4.13 and Fig. 4.14 show the transient responses of output voltage without and with the load adaptive control scheme. In Fig. 4.13, the transient time is 43 ms from 10 W to 50 W and 30 ms from 60 W to 100 W, these reveal when without load adaptive control scheme, dynamic response of the output voltage is different at different load conditions change. Applied the adaptive control scheme, Fig. 4.14 shows the transient time is maintained 30 ms from 10 W to 50 W and 30 ms from 60 W to 100 W, the dynamic responses become optimal at different load conditions change after adding the load adaptive scheme.

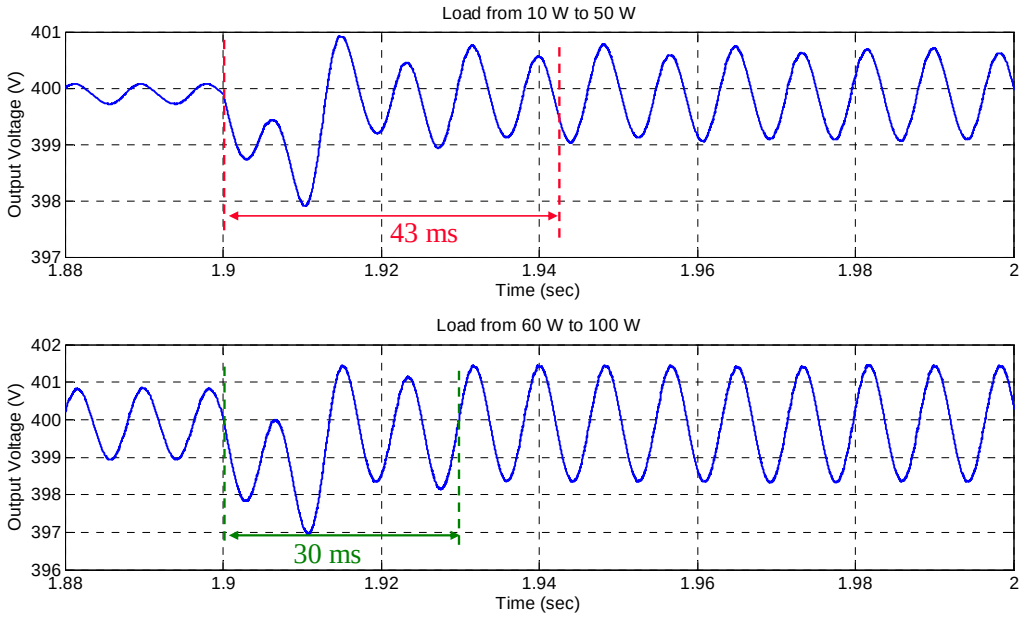


Fig. 4.13. The transient responses of output voltage without load adaptive gain adjustment, load changes from 10 W to 50 W and 60 W to 100 W.

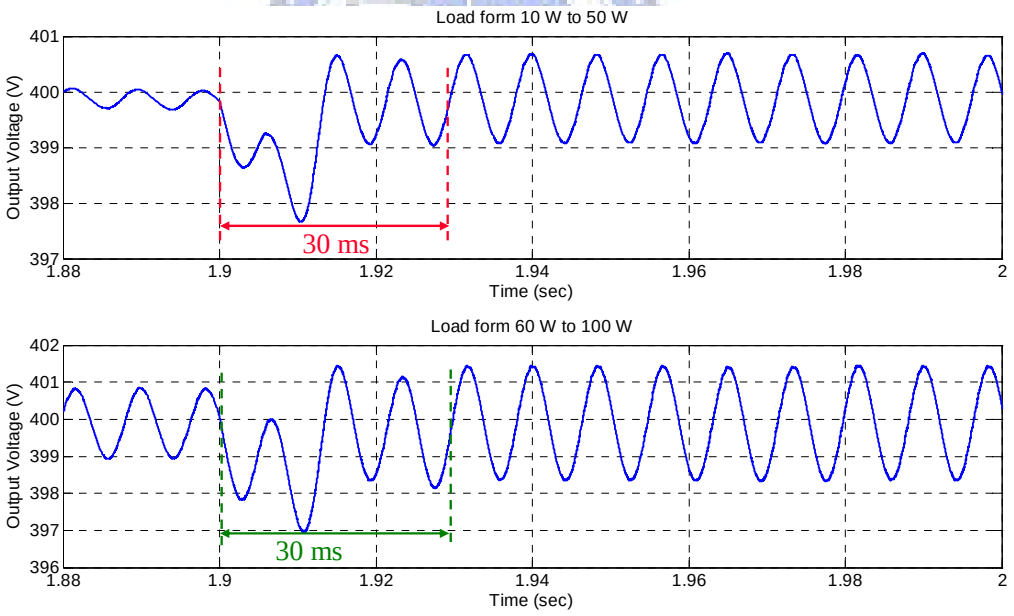


Fig. 4.14. The transient responses of output voltage with load adaptive gain adjustment, load changes from 10 W to 50 W and 60 W to 100 W.

Chapter 5

Implementing Mixed-Signal CRM PFC and Experimental Results Analysis

5.1 Laboratory Setup

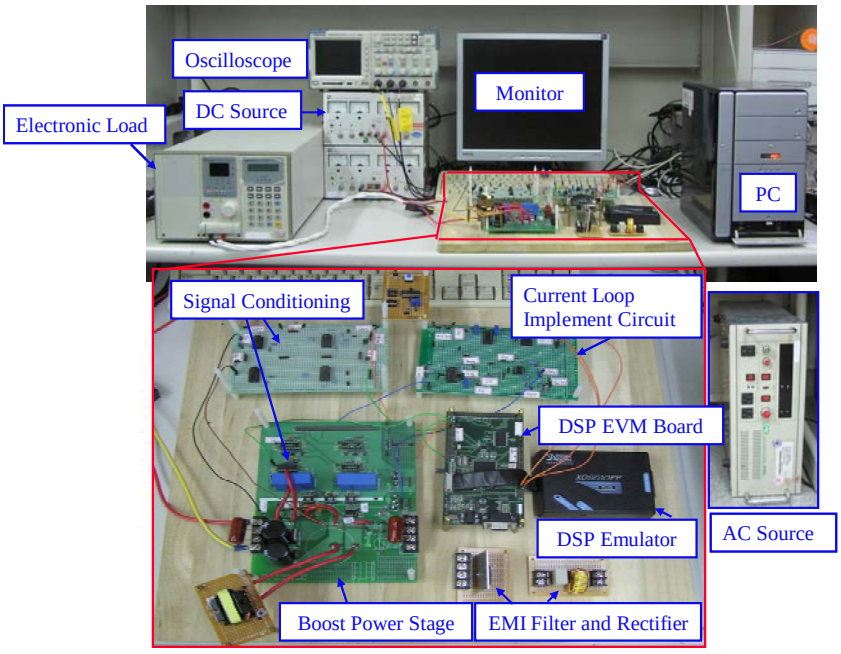


Fig. 5.1. The experimental board of mixed-signal CRM PFC AC-DC converter.

5.1.1 Development of Current Control Loop with L6561

In the previous chapters, the analog current control loop mainly includes four parts: current loop comparator, ZCD comparator, RS flip-flop, and gate driver. To implement the inner loop of the CRM controller, this thesis selects a CRM PFC control IC of ST Microelectronics, L6561. The block diagram of L6561 is shown in Fig. 5.2 and Table 5.1 shows the pin description and operating ranges of this control IC [30]-[32].

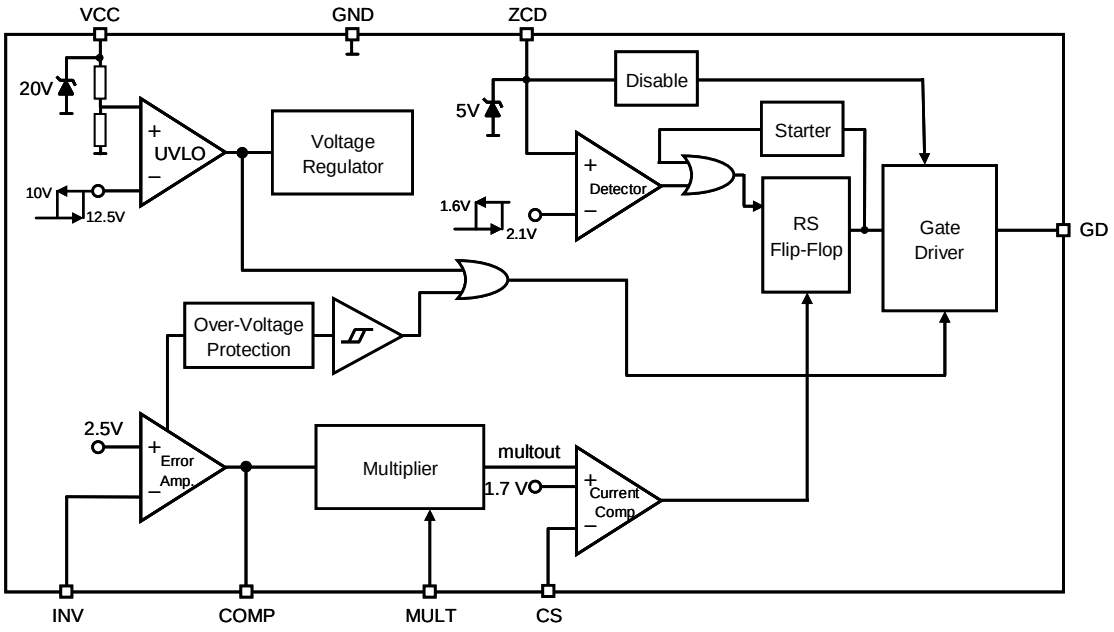


Fig. 5.2. The block diagram of L6561.

TABLE 5.1
PIN DESCRIPTION AND OPERATING RANGES

Pin	Symbol	Function	Electrical Characteristics
1	**INV**	Inverting input of the error amplifier	-0.3 V ~ 7 V
2	**COMP**	Output of error amplifier	2.25 V ~ 5.8 V
3	**MULT**	Input of multiplier stage	-0.3 V ~ 3.5 V
4	**CS**	Input to the current comparator.	-0.3 V ~ 1.8 V
5	**ZCD**	Zero current detector input	-10 mA ~ 50 mA
6	**GND**	Ground	0 V
7	**GD**	Gate driver output	-700mA ~ 700mA
8	**VCC**	Supply voltage of driver and control circuits	11 V ~ 18 V

The voltage control part in L6561 is needless and hence has to be removed. The voltage control is composed by an error amplifier and a multiplier with a gain equal to 0.6 at typical operating condition. Because of the protection mechanism on the error amplifier output which limits the error amplifier output voltage should be higher than 2.25 V and eliminating the effect of the multiplier gain, the error amplifier can not be floated. The relationship between the input sides and the output of the multiplier is provided as follow

$$V_{multout} = V_{multin} \cdot (V_{comp} - 2.5) \cdot 0.6 \qquad (5\text{-}1)$$

To eliminate the effect of multiplier gain, the error amplifier is connected as an inverting amplifier and let the multiple value of (V_{comp} − 2.5) and 0.6 equal to 1 from (5-1).

5.1.2 Development of Voltage Control Loop with DSP

For implementing the control algorithms, there are one periodic interrupt for control and one aperiodic interrupt for communication in the DSP as shown in Fig. 5.3. The period interrupt with 5 kHz sampling rate performs the ADC synchronization, notch filter executing, voltage compensator, and load adaptive gain adjustment.

The flow chart of the interrupt service routine (ISR) is shown in Fig. 5.4. The synchronous sampling techniques are applied for sensing the output voltage, rectified line voltage, and load current. If the sensed output feedback voltage is higher than the regulated value, the current command is directly set as zero to protect the system. If the sensed output feedback voltage is in the normal value, the voltage control algorithms will be executed.

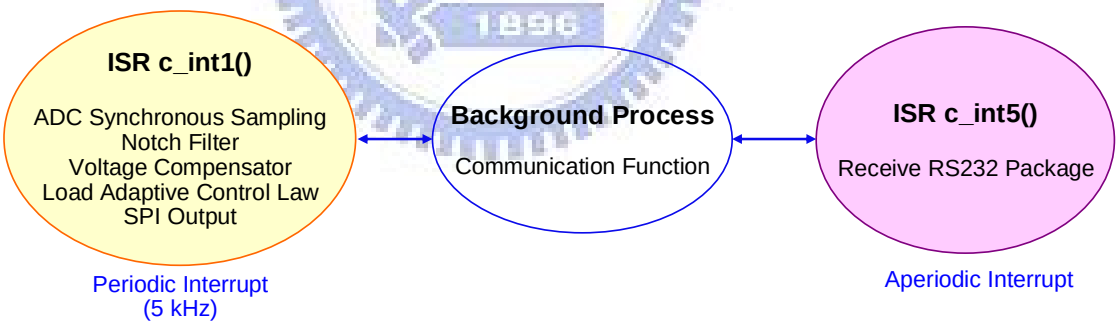


Fig. 5.3. Interrupt configuration in the DSP controller.

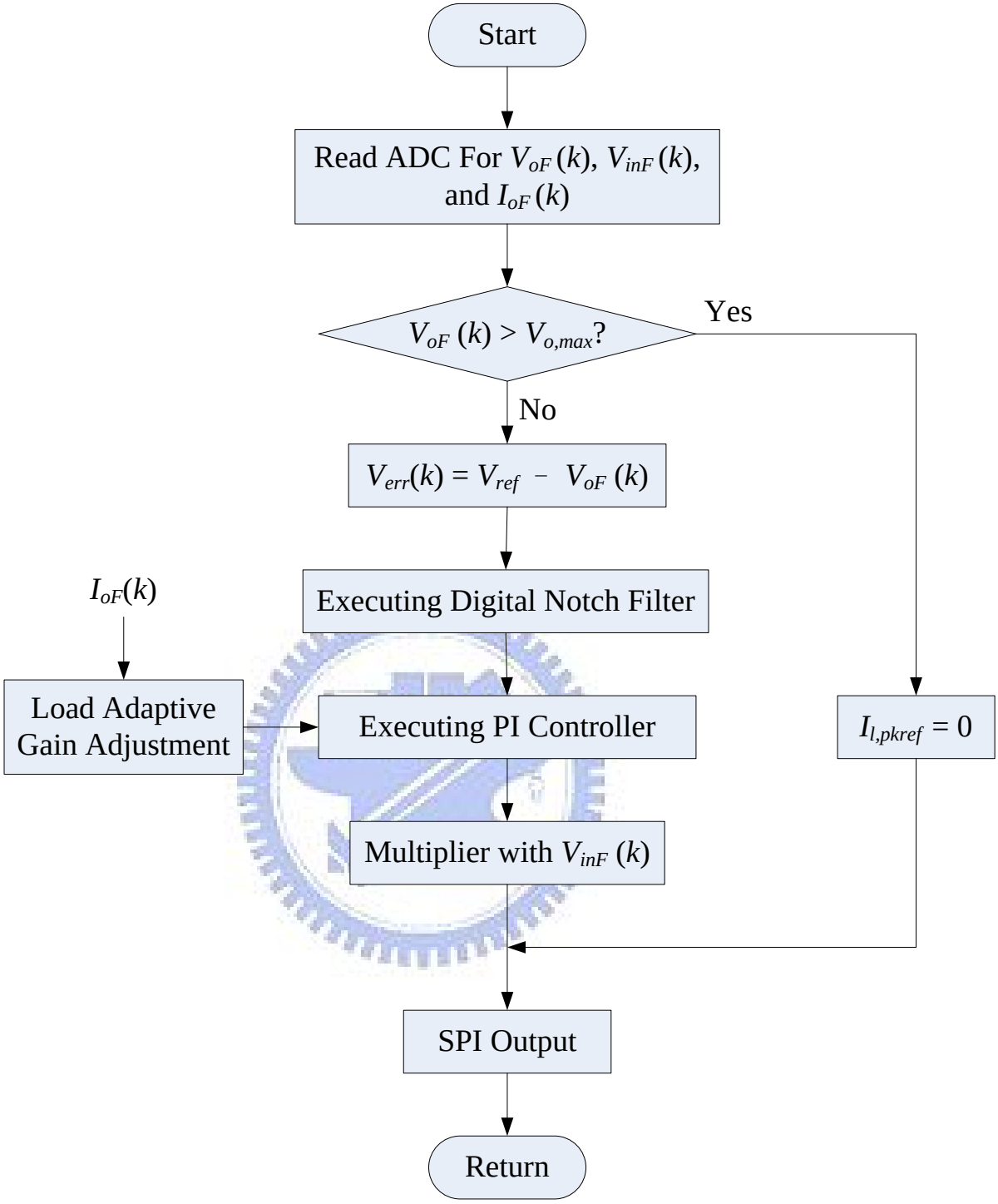


Fig. 5.4. The flowchart of voltage loop control.

5.2 Analysis of Experimental Results

5.2.1 Analysis of Steady-State Experimental Results

Fig. 5.5 shows the input line voltage and output voltage simulation waveforms. The experimental results reveal that the output voltage maintains at 400 V and the output voltage ripple caused by line voltage as shown in Fig. 5.6.

Fig.5.7 is shown the simulation results of the rectified line voltage and inductor current at 80 W. Fig. 5.8 show the rectified line voltage and inductor current waveforms at 80 W. Fig. 5.9 shows the line voltage and line current simulation waveforms at 80 W output power. Fig. 5.10 is shown that the line voltage and line current are in phase, power factor is 0.99, and THD is 5.1 %.

Fig. 5.11 shows the simulation results of the output voltage and output current waveforms when the output load varies from 50 W to 100 W. The experimental results reveal that the output voltage drops 5 V and the transient time is about 120 ms as shown in Fig. 5.12.

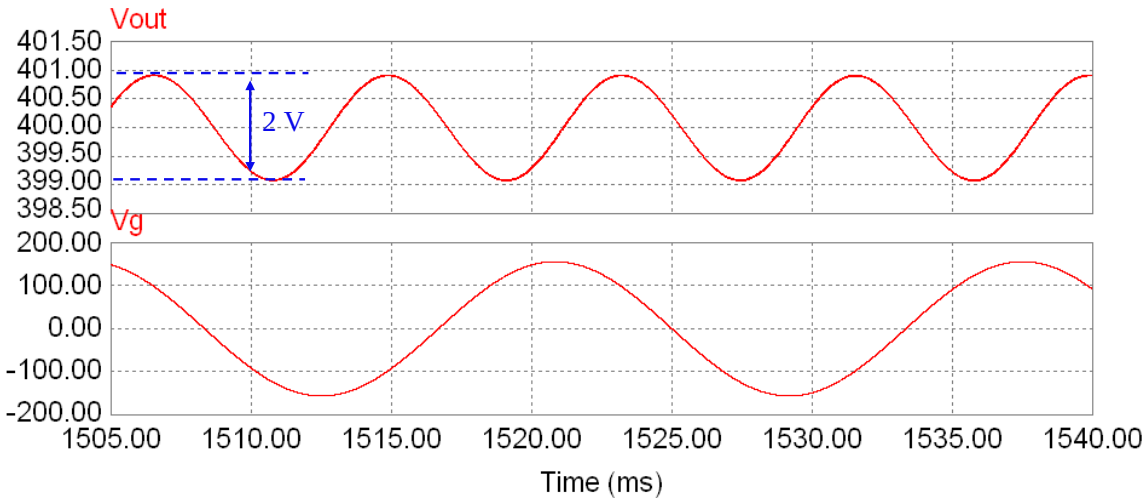


Fig. 5.5. The line voltage and output voltage simulation waveforms.

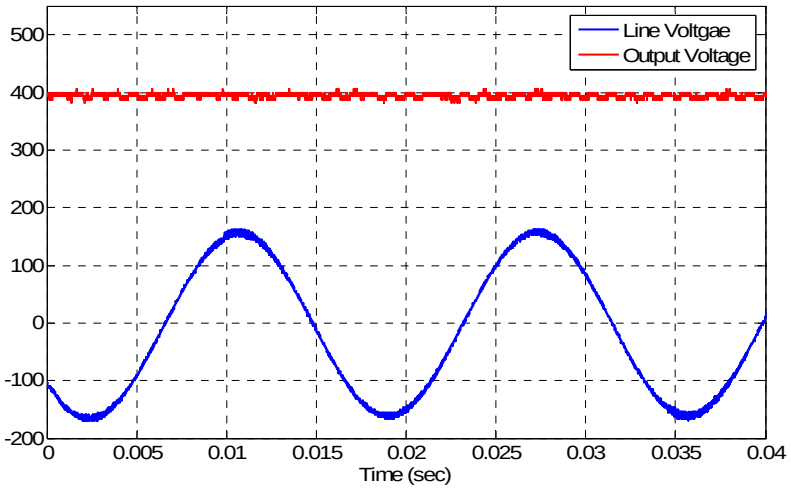


Fig. 5.6. The experimental results of line voltage and output voltage.

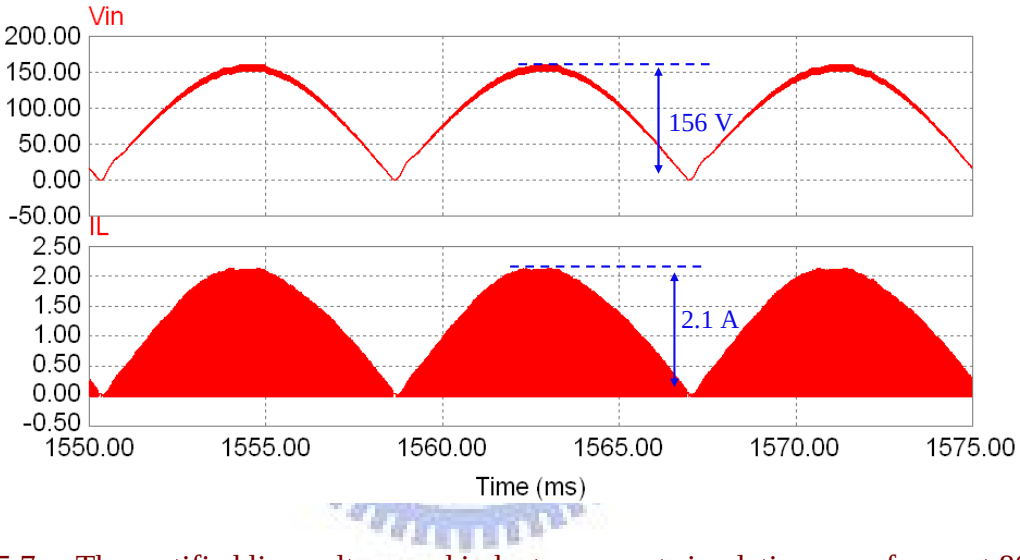


Fig. 5.7. The rectified line voltage and inductor current simulation waveforms at 80 W.

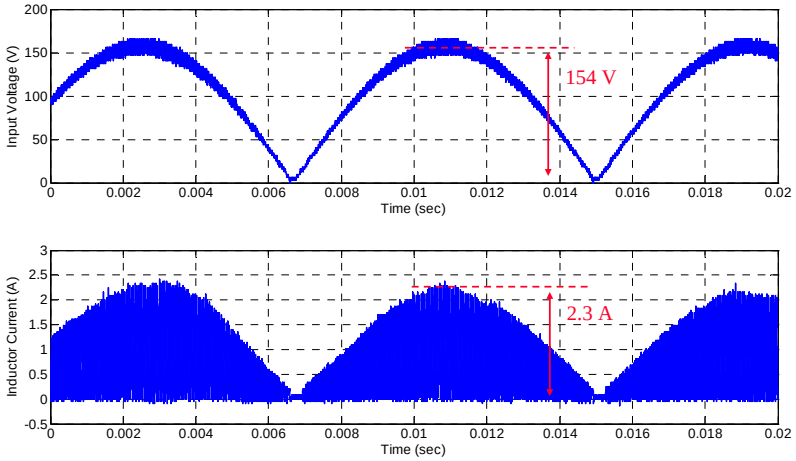


Fig. 5.8. The rectified line voltage and inductor current experimental waveforms at 80 W.

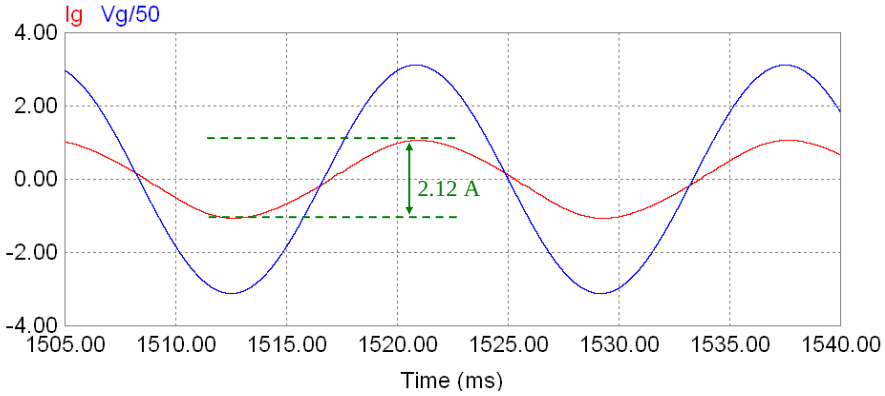


Fig. 5.9. The line voltage and line current simulation waveforms in 80 W load condition.

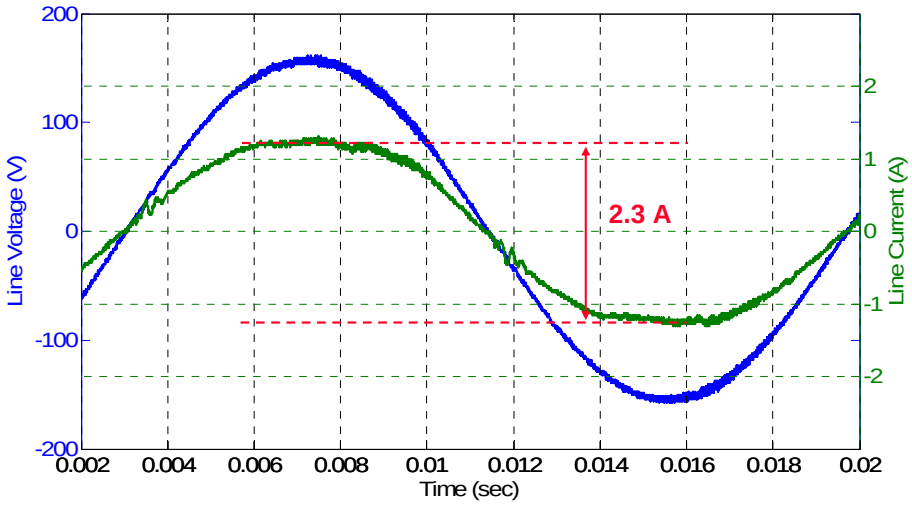


Fig. 5.10. The experimental results of line voltage and line current waveforms at 80 W load condition.

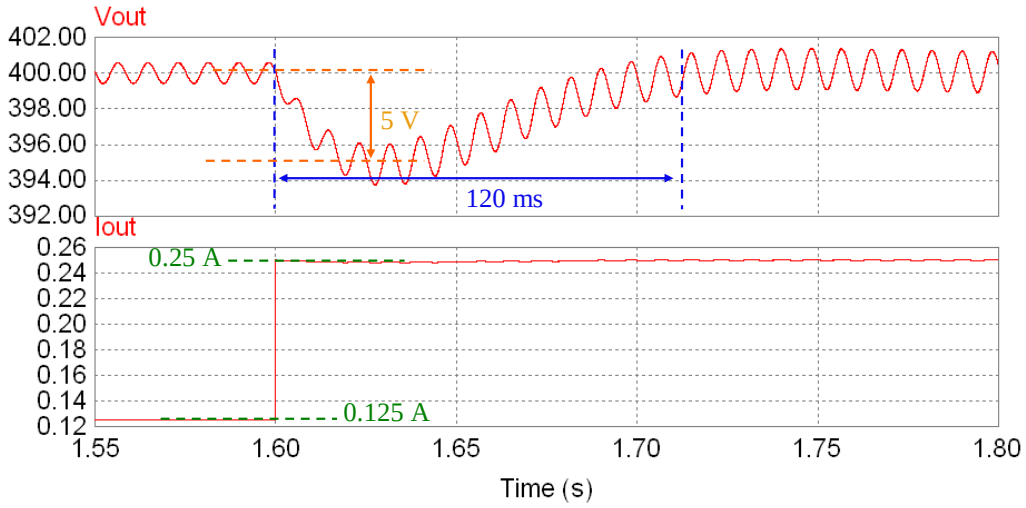


Fig. 5.11. The output voltage and output current simulation waveforms when output load varies from 50 W to 100 W.

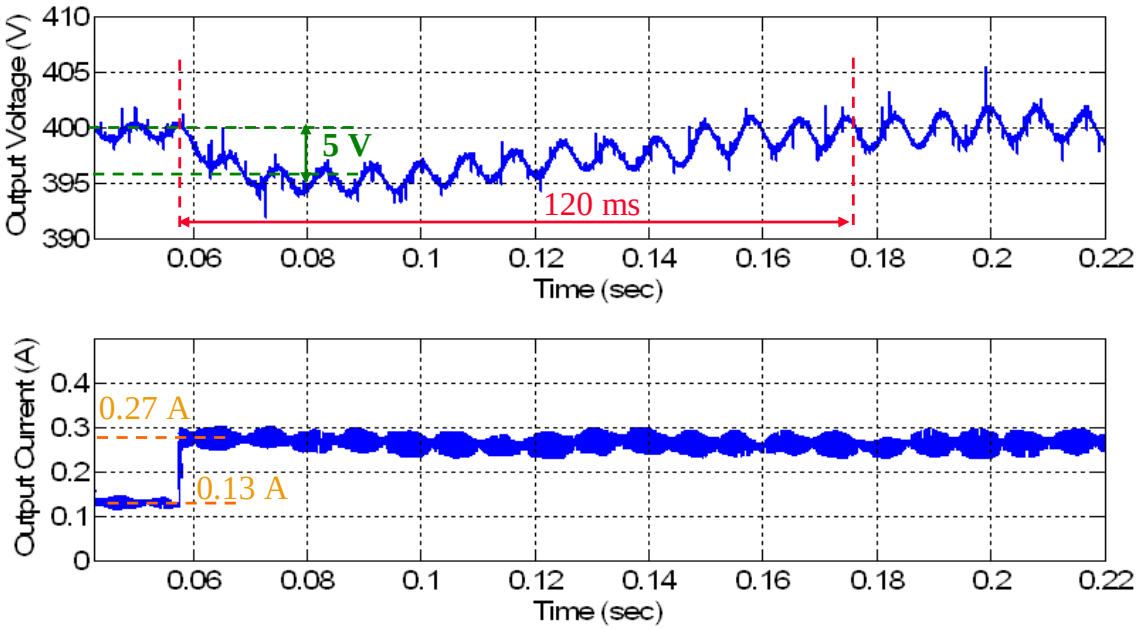


Fig. 5.12. The experimental results of the output voltage and output current when output load varies from 50 W to 100 W.

5.2.2 Analysis of Experimental Results with Notch Filter

Fig. 5.13 shows the experimental results of output voltage and line current waveforms when load varies from 50 W to 100 W and the voltage loop bandwidth is 30 Hz without notch filter. Under this condition, the transient time of output voltage is 22 ms and line current THD is 12 %. Fig. 5.14 shows the experimental results of output voltage and line current waveforms when load varies from 50 W to 100 W and the voltage loop bandwidth is 30 Hz with notch filter. The transient time is still 23 ms and the line current THD is improved to 6 %. This design flow makes the line current match the regulation. Fig. 5.15 and Fig. 5.16 compare the line current PF and THD without and with notch filter.

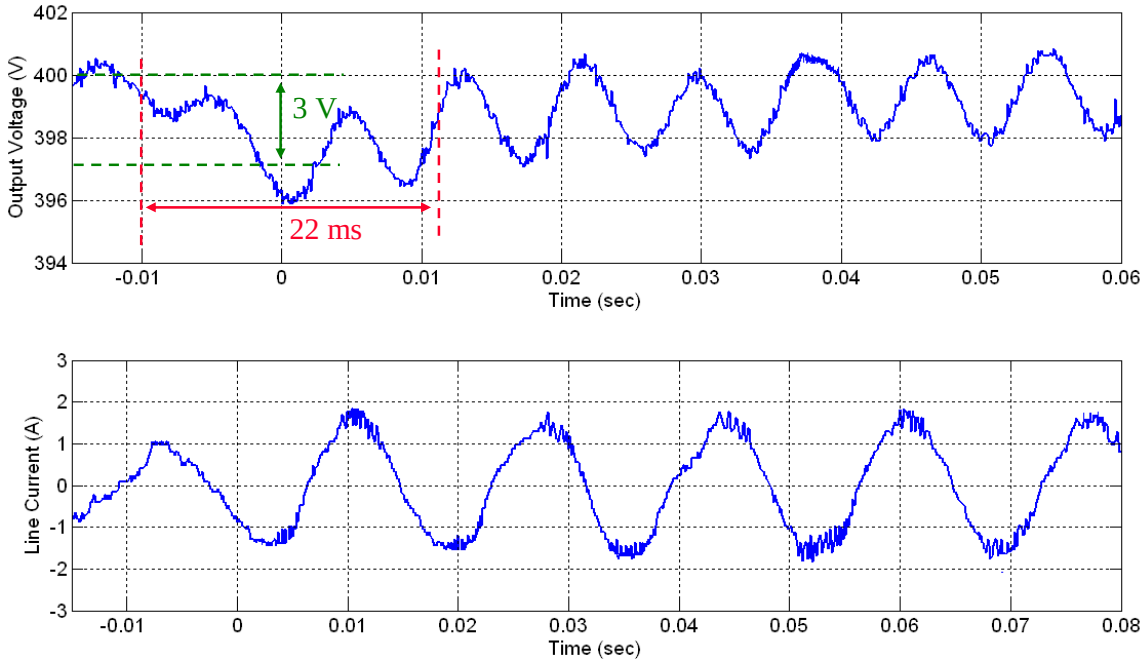


Fig. 5.13. The experimental results of output voltage and line current waveforms when load varies from 50 W to 100 W and the voltage loop bandwidth is 30 Hz without notch filter.

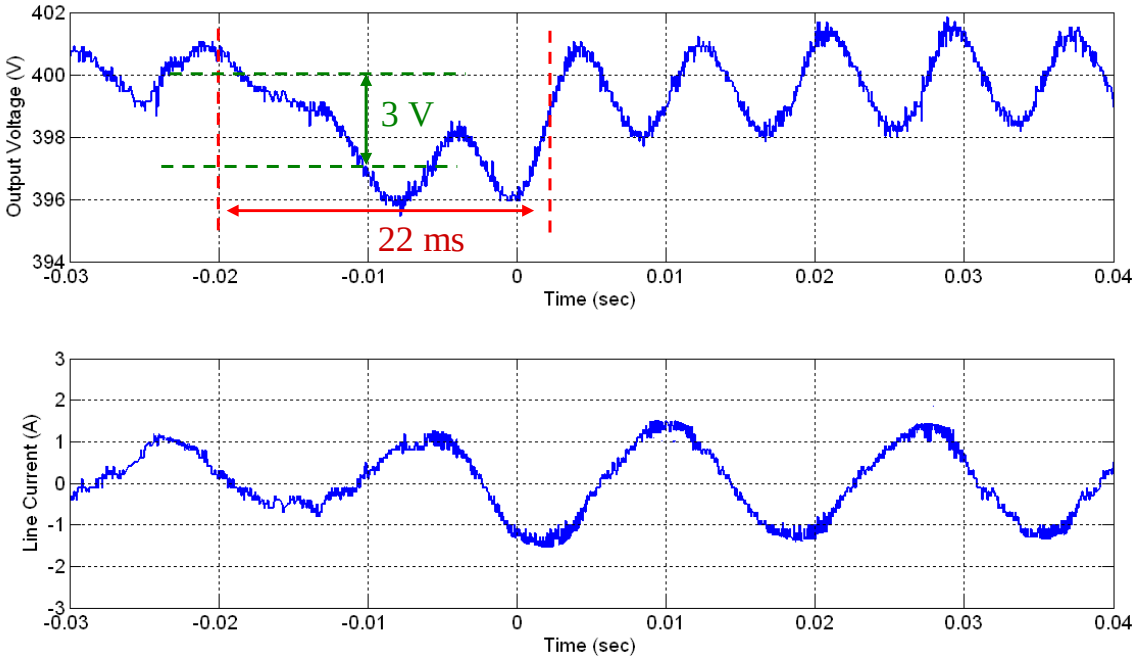


Fig. 5.14. The experimental results of output voltage and line current waveforms when load varies from 50 W to 100 W and the voltage loop bandwidth is 30 Hz with notch filter.

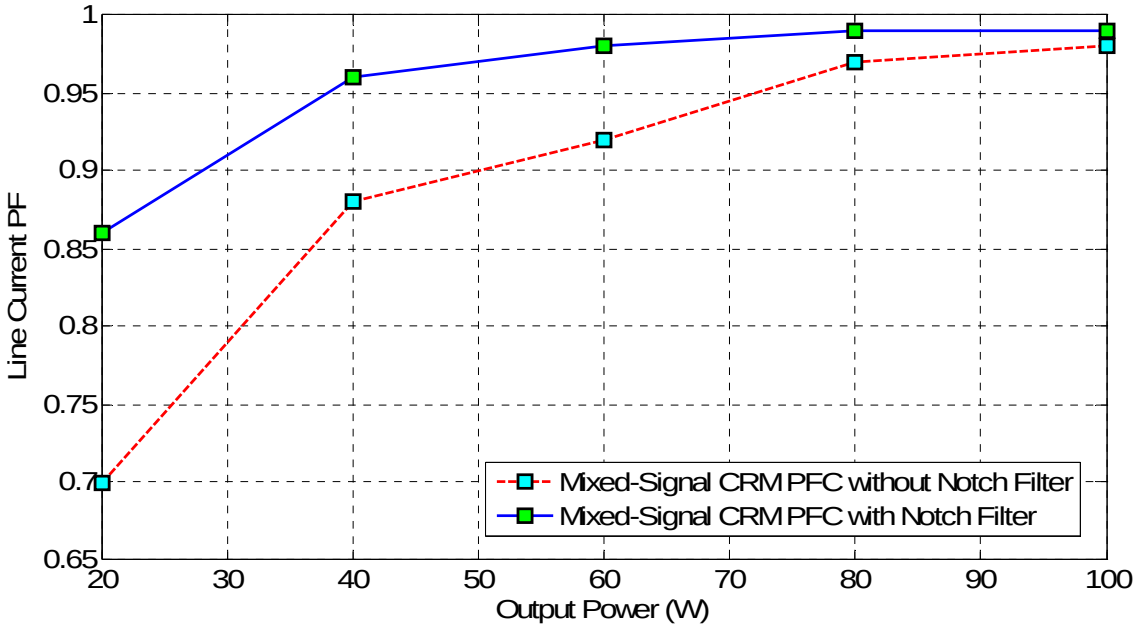


Fig. 5.15. Comparing the line current PF without and with notch filter.

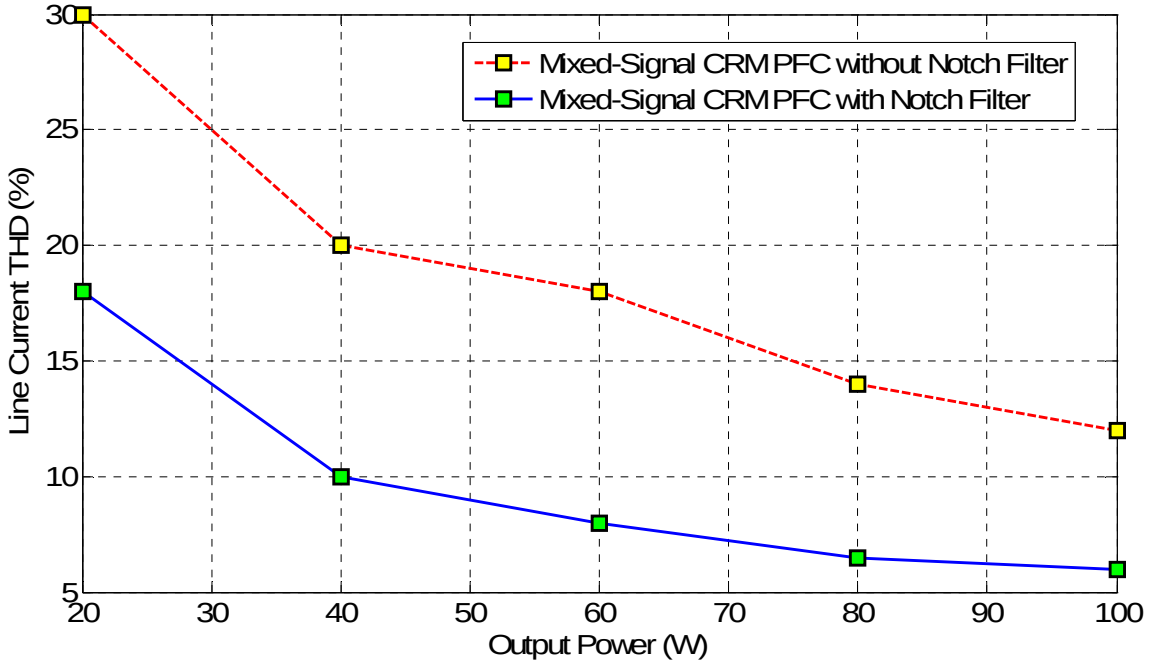


Fig. 5.16. Comparing the line current THD without and with notch filter.

5.2.3 Analysis of Experimental Results with Load Adaptive Adjustment

Fig. 5.17 shows the experimental results of output voltage dynamic responses when load varies from 10 W to 50 W and 60 W to 100 W without load adaptive control law. The recovery time is 38 ms from 10 W to 50 W and 22 ms from 60 W to 100 W. Added the load adaptive control law, the transient times are both 22 ms from 10 W to 50 W and from 60 W to 100 W as shown in Fig. 5.18. And so on, the dynamic responses become the same at different load conditions change.

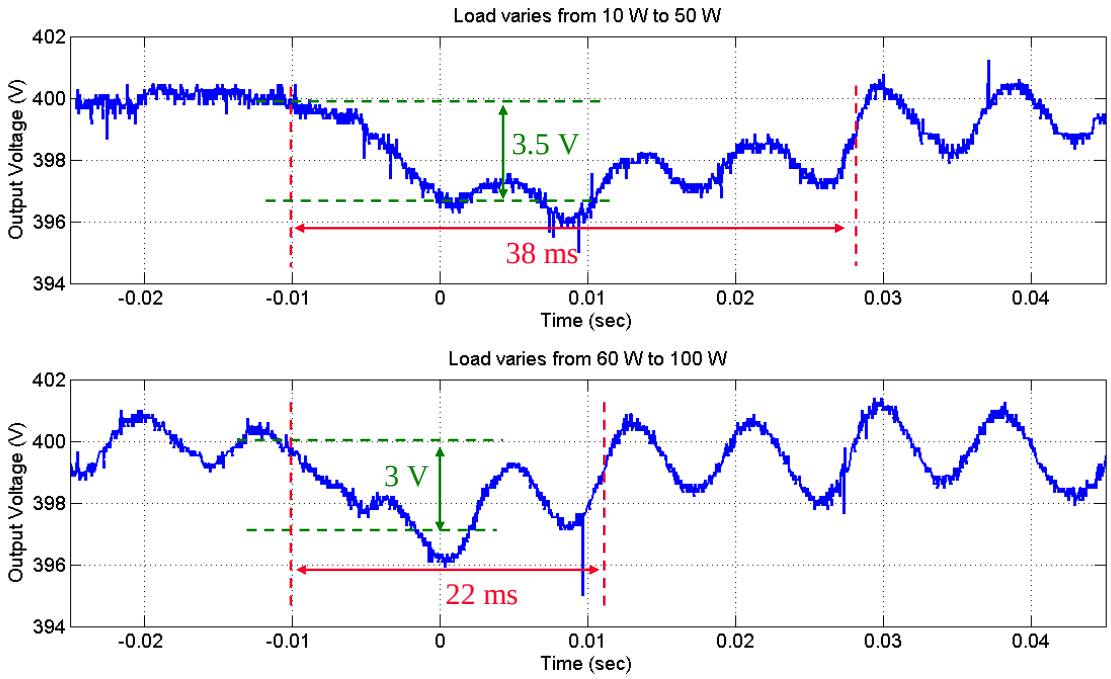


Fig. 5.17. The experimental results of output voltage transient responses without load adaptive control scheme, load changes from 10 W to 50 W and 60 W to 100 W.

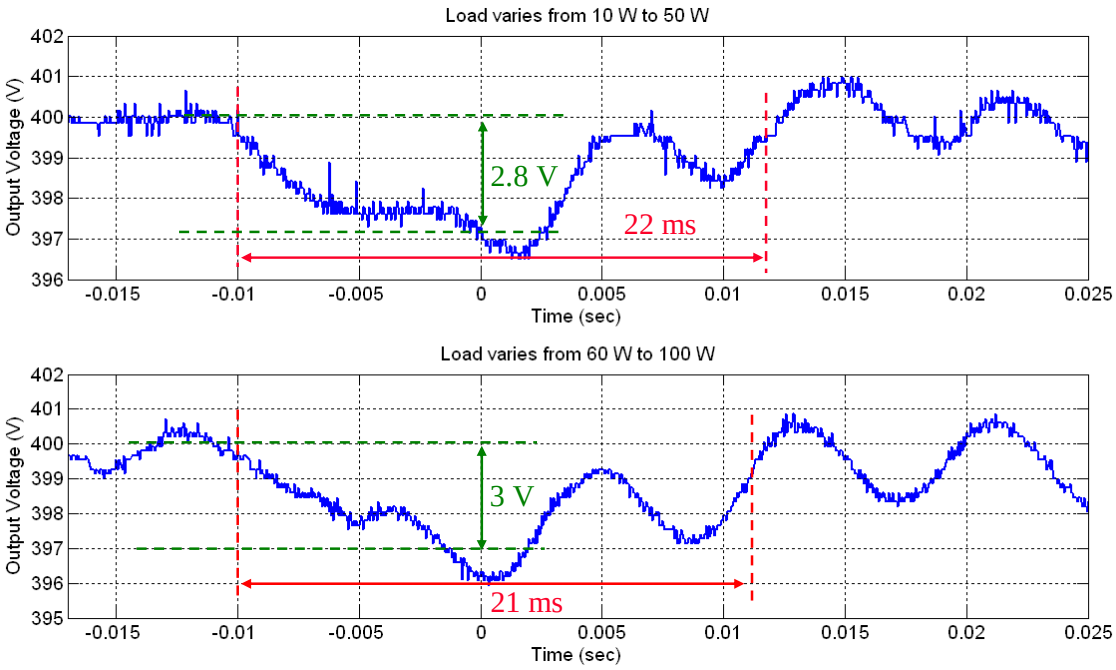


Fig. 5.18. The experimental results of output voltage transient responses with load adaptive control scheme, load changes from 10 W to 50 W and 60 W to 100 W.

Chapter 6

Conclusions

This thesis utilized PSIM simulation to analyze the control architecture of the mixed-signal CRM PFC. It focuses on the specifications of the sub circuit implementation such as analog current comparator, zero-current-detector comparator, sampling rate, and the bit resolutions of ADC and DAC. From the design procedure in chapter 3, the specifications of each sub circuit are as follows: the hysteresis band of analog current comparator is 50 mV, the reference voltage of ZCD comparator is 1.6 V, the sampling rate is 5 kHz, the bit resolutions of output voltage feedback and rectified line voltage feedback ADCs are both 8-bit, and the bit resolution of DAC is 10-bit. Under these conditions, PF and THD of the mixed-signal CRM PFC circuit are 0.99 and 4.6 % at rated power.

The thesis implements the mixed-signal CRM PFC AC-DC converter by ST Microelectronics CRM PFC IC, L6561, and DSP EVM board, TMS320LF2407A. The transient time of transient response from 50 W to 100 W can be reduced to 23 ms and the line current PF and THD are 0.99 and 6 % at rated power by adding digital notch filter. By applying the load adaptive gain adjustment, the transient times of dynamic responses from 10 W to 50 W and 60 W to 100 W are 22 ms and 21 ms. Therefore, the dynamic responses are the same on different load conditions. This load adaptive gain adjustment can make the dynamic responses stable and fast on different load conditions.

According to above conclusions with both the PSIM simulation and experimental results verifying to achieve proposed performances, the design of the mixed-signal CRM PFC AC-DC converter can be easily implemented and verified by referring this thesis.

Reference

[1] K. Rustom and I. Batarseh, "Recent advances in single-stage power factor correction," *IEEE Industrial Technology*, vol. 2, pp. 1089-1095, Dec. 2003.

[2] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: a survey," *IEEE Trans. on Power Electronics*, vol. 18, pp. 749-755, May 2003.

[3] L. Rossetto, G. Spiazzi, and P. Tenti, "Control techniques for power factor correction converters," *Power Electronics and Motion Control Conf. Proc.*, 1994..

[4] J. Sebastian, M. Jaureguizar, and J. Uceda, "An overview of power factor correction in single-phase off-line power supply systems," *IEEE IECON Conf. Rec.*, vol. 3, pp. 1688-1693, Sept. 1994.

[5] J. B. Williams, "Design of feedback loop in unity power factor AC to DC converter," *IEEE PESC Conf. Rec.*, vol. 2, pp. 959-967, Jun 1989.

[6] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. on Industrial Electronics*, vol. 50, no. 5, pp. 962-981, Oct. 2003.

[7] 宋自恆, 林慶仁, "功率因數修正電路之原理與常用元件規格," 新電子科技雜誌第217期, 2004年4月號

Review of Mixed-Signal Control Schemes

[8] R. Zane and D. Maksimovic, "A mixed-signal ASIC power-factor-correction (PFC) controller for high frequency switching rectifiers," *IEEE PESC Conf. Rec.*, pp. 117-122, Jul. 1999.

[9] L. T. Jakobsen and A. E. Andersen, "Comparison of two different high performance mixed signal controllers for DC/DC converters," *IEEE Compel Workshop*, July 2006.

[10] M. Chen, A. Mathew, and J. Sun, "Mixed-signal control of single-phase PFC based on a nonlinear current control method," *IEEE PESC Conf. Rec.*, June 2006.

[11] A. Prodic and D. Maksimovic, "Mixed-signal simulation of digitally controlled switching converters," *Proc. IEEE COMPEL*, pp. 100-104, June 2002.

CRM PFC Circuits

[12] J. S. Lai and D. Chen, "Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode," *IEEE APEC Conf. Proc.*, pp. 267-273, March, 1993.

[13] J. Turchi, Power factor correction stages operating in critical conduction mode, ON Semiconductor, Appl. Note AND8123, Sep. 2003.

[14] M. Gotfryd, "Limits in boost power factor corrector operating in border-line mode," *IEEE Trans. on Power Electronics*, vol. 18, pp. 1330-1335, Nov. 2003.

Analog Current Loop Circuits Design

[15] D. S. Chen and J. S. Lai, "A study of power correction boost converter operating at CCM-DCM mode," *IEEE SECON Conf. Rec.*, Apr. 1993.

[16] A. Abramovitz, "Effect of the ripple current on power factor of CRM boost APFC," *IEEE IPEMC Conf. Rec.*, pp. 1-4, Aug. 2006.

[17] L. Huber, B. T. Irving, and M. M. Jovanovic, "Line current distortions of DCM/CCM boundary boost PFC converter," *IEEE APEC Conf. Proc.*, pp. 702-708, Feb. 2008.

[18] C. Bridge and L. Balogh, *Understanding interleaved boundary conduction mode PFC converters*, Fairchild Power Seminars, 2008-2009.

Digital Voltage Loop Circuits Design

[19] L. Balogh, *A practical introduction to digital power supply control*, TI Unitrode Design Seminars, 2004-2005.

[20] S. Buso and P. Mattavelli, "Digital Control in Power Electronics," *Morgan & Claypool Publishers*, pp. 27-29, 2006.

[21] M. Xie, "Digital Control for Power Factor Correction," Master thesis, Virginia Tech, 2003.

Control Loop Modeling

[22] C. Adragna, Control loop modeling of L6561-baded TM PFC, STMicroelectronics, Appl. Note AN1089, Mar. 2000.

[23] R. B. Ridley, *Average small-signal analysis of the boost power factor correction circuit*, VPEC Seminar, 1989.

[24] M. Shen, Z. Qian, and M. Chen, "Analysis and average modeling of critical mode boost PFC converter," *IEEE PEDS Conf. Proc.*, vol. 1, pp. 138-141, Oct. 2001.

Voltage Control Loop Design

[25] A. Prodic, J. Chen, R. W. Erickson, and D. Maksimovic, "Digitally controlled low-harmonic rectifier having fast dynamic responses," *IEEE APEC Conf. Proc.*, pp. 476-482, 2002.

[26] S. Buso and P. Mattavelli, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. on Power Electronics*, vol. 13, no. 5, Sep. 1998.

[27] K. Hirano, S. Nishimura, and S. Mitra, "Design of digital notch filters," *IEEE Trans. Commun.*, vol. 22, no. 7, pp. 964-970, Jul. 1974.

[28] M. Ilic and D. Maksimovic, "Digital Average Current-Mode Controller for DC–DC

Converters in Physical Vapor Deposition Applications," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1428-1436, May 2008.

[29] K. J. Astrom and B. Wittenmark, *Adaptive Control*, 2nd ed. Reading, MA: Addison Wesley, 1994.

CRM PFC IC

[30] C. Ortmeyer and C. Adragna, Design tips for L6561 power factor corrector in wide range, STMicroelectronics, Appl. Note AN1214, Dec. 2000.

[31] C. Adragna, L6561 enhanced transition mode power factor corrector, STMicroelectronics, Appl. Note AN966, Mar. 2003.

[32] "Power factor corrector," STMicroelectronics, Datasheet, June 2004.

[33] "Design and apply to power factor correction circuit using SG6961," System General, Appl. Note AN6961.

[34] "Power-factor controller IC for high power factor and active harmonic filter," Infineon Technologies, Datasheet, Version 2.1, Feb. 2005.

[35] M. Herfurth and W. Frank, TDA4863-technical description, Infineon Technologies, Appl. Note AN-PFC-TDA4863-1, Version 1.2, Oct. 2003.

[36] W. Frank, Getting started with TDA4863, Infineon Technologies, Appl. Note AN-PFC-TDA4863-2, Version 1.0, April. 2002.

Vita

Ming-Hau Chan was born in Taichung, Taiwan, R.O.C, in 1985. He received the university degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C, in 2007. He is currently pursuing the M.S. degree at institute of electrical and control engineering in National Chiao Tung University, Hsinchu, Taiwan, R.O.C. His research interests are analog circuit design and digital control techniques for PFC AC/DC converter.

姓名: 詹茗皓

性別: 男

生日: 中華民國 74 年 4 月 13 日

論文題目: 中文: **具負載適應增益調適混合信號控制之邊界模式功率因數修正交-直流轉換器**

英文: **Design of a Load Adaptive Gain Adjustment Mixed-Signal Critical Mode PFC AC-DC Converter**

學歷:

1. 民國 96 年 6 月　　國立交通大學電機工程學系畢業
2. 民國 98 年 10 月　　國立交通大學電機及控制工程研究所碩士班