國立交通大學

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碩士論文

可切換頻帶式低雜訊放大器之設計

Design of Band Switchable Low Noise Amplifiers

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可 切 換 頻 帶 式 低 雜 訊 放 大 器 之 設 計

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摘　　要

兩個低雜訊放大器 (LNA) 被設計應用於超寬頻 (UWB) 與全球互運的微波存取 (Wi-MAX)。所提出的應用於 UWB 無線接收機之雙頻帶低雜訊放大器有兩個可切換的頻帶。 此低雜訊放大器分別可以操作在 3.1-5GHz 和 6-10.6GHz。 此設計包含了一個輸入匹配電路，兩個共源級放大器和使用來量測之輸出緩衝器。 並且分析輸入匹配電路設計步驟[9]，此對我們設計輸入匹配電路很重要。提出之低雜訊放大器擁有兩個使用 NMOS 當切換電容開關之負載以用來得到更好的品質因數(Q)。 此低雜訊放大器當使用 1.8V 電源供應器並且消耗功率 22.46mW 時分別提供 10.8dB 和 16.8dB 之增益與 6.2dB 和 6.5dB 之雜訊指標在 3.25-5.6GHz 和 6-10.4GHz。基於 UWB 可切換頻帶式低雜訊放大器之開關電路我們設計一個新的應用於四個頻帶之 Wi-MAX 低雜訊放大器之開關電路。此低雜訊放大器分別可以操作在 2.3GHz, 2.5GHz, 3.5GHz 和 5.8GHz。此提出之低雜訊放大器是由一個寬頻的輸入匹配電路, 一個 NMOS 連接到地之開關電路, 一個共源級放大器和使用來量測之輸出緩衝器構成。模擬結果表現此增益分別為 10.1dB, 11.1dB, 13.5dB 和 15.3dB 在 2.3GHz, 2.5GHz, 3.5GHz 和 5.8GHz。此雜訊指標分別為 4dB, 3.5dB, 2.8dB 和 3.4dB 在 2.3GHz, 2.5GHz, 3.5GHz 和 5.8GHz。 此功率消耗為 11.5mW 在一個 1.5V 之電源供應器下。此低雜訊放大器也使用台積電 0.18 微米互補式金氧半導體科技。

Design of Band Switchable Low Noise Amplifiers

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ABSTRACT

Two band switchable low noise amplifiers (LNA) are designed for ultrawideband (UWB) and Worldwide Interoperability for Microwave Access (Wi-MAX) applications. The proposed dual-band LNA for UWB wireless receiver has two switchable bands. This LNA can operate at both 3.1-5GHz and 6-10.6GHz frequency bands. The design consists of a input matching circuit, two cascode common-source amplifiers and an output buffer for measurement. Moreover, we give a procedure to analyze the input matching circuit [9], which is important for input matching design. The proposed LNA is designed with two loadings of switched capacitors which use NMOS in order to make high quality factor (Q). The LNA gives 10.8dB and 16.8dB gain, 6.2dB and 6.5dB noise figure at 3.25-5.6GHz and 6-10.4GHz frequency band while consuming 22.46mW through a 1.8V supply using the TSMC 0.18 μm CMOS technology. Based on the switch circuit of band switchable UWB LNA the new switch circuit is also designed for of band switchable Wi-MAX LNA. The LNA operates at 2.3GHz, 2.5GHz, 3.5GHz and 5.8GHz. The proposed LNA consists of a wideband input matching circuit, a NMOS connected to ground switch circuit, a common-source amplifiers and an output buffer for measurement. The simulation result shows that the gain is 10.1dB, 11.1dB, 13.5dB and 15.3dB at 2.3GHz, 2.5GHz, 3.5GHz and 5.8GHz, respectively. NF is 4dB, 3.5dB, 2.8dB and 3.4dB at 2.3GHz, 2.5GHz, 3.5GHz and 5.8GHz, respectively. The power consumption is 11.5mW with 1.5V power supply. The LNA also uses TSMC 0.18 μm CMOS technology.

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Chapter 1

Introduction

In this chapter, we will introduce the background of UWB and Wi-MAX. Moreover, we introduce the corresponding RF transceiver. Finally motivation, contribution and proposed design methodology.

1.1 UWB

UWB system has became one of the most popular technologies which can transmitting the data that has high data rate and low power over a wideband spectrum, since the UWB technology is defined for low power wireless communications in February, 2002 [1]. However, the agreement of IEEE UWB standard (IEEE 802.15.3a [2]) has not been completely defined by two main proposed solutions, multi-band-orthogonal frequency division multiplexing (MB-OFDM) and direct sequence UWB (DS-UWB), that are both permitted to transmit in the band between 3.1GHz-10.6GHz for MB-OFDM and 3.1GHz-9.6GHz for DS-UWB. The bandwidth of MB-OFDM is shown in Fig. 1.1(a). The band of OFDM-UWB extends from 3176MHz to 10552MHz. The bandwidth of DS-UWB is with Low-Band and High-Band which is shown in Fig. 1.1(b) is from 3100MHz to 4900MHz and 6000MHz to 9700MHz. For UWB, we should avoid using the U-NII band and the band for WLAN, because the band of U-NII and WLAN cover the group 2 of OFDM-UWB. On the other hand. In DS-UWB, the band of 4900MHz to 6000MHz is not using, too. The thesis focuses on how to switch the band to achieve the UWB application.

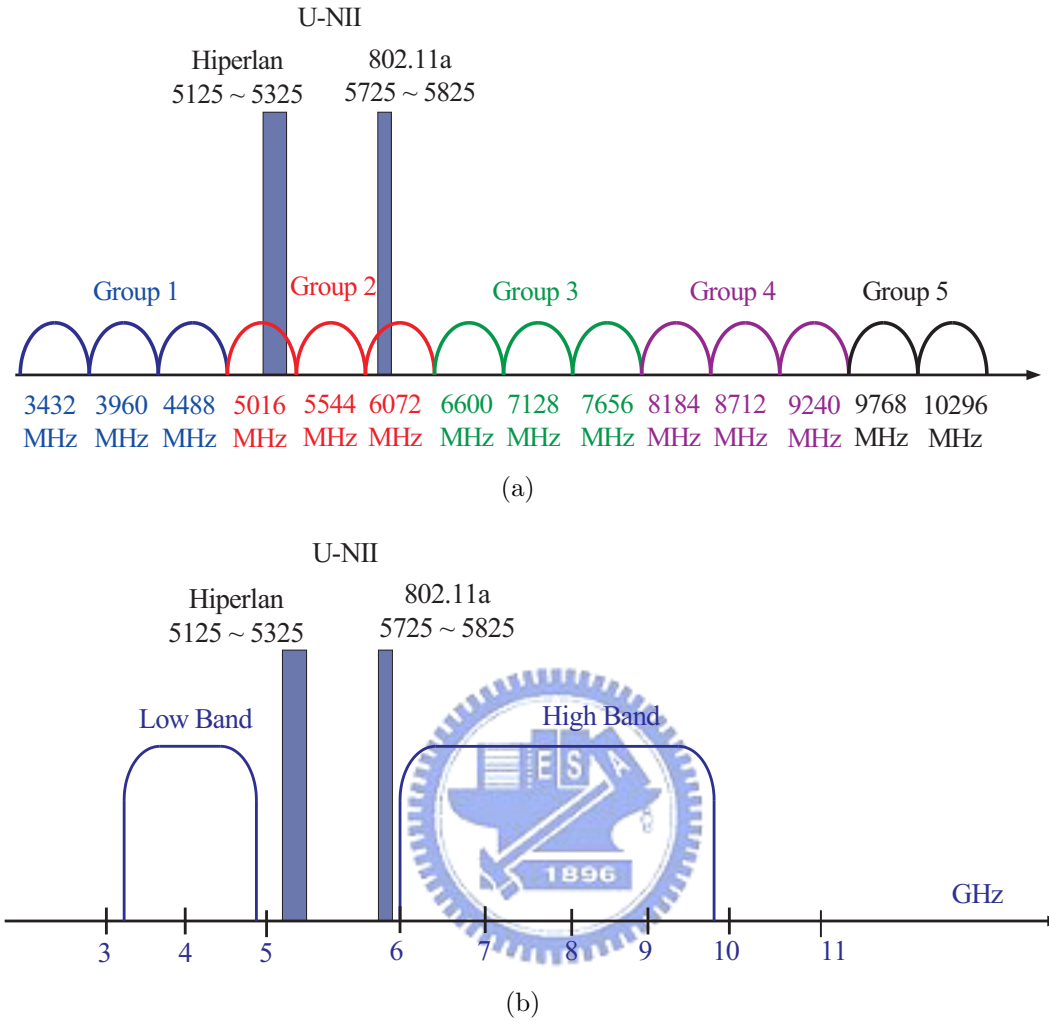


Figure 1.1: Bandwidth of UWB: (a) Band Groups of MB-OFDM. (b) Low Band and High Band of DS-UWB.

1.2 Wi-MAX

The Wi-MAX system is a larger coverage area, high data rate and low-power consumption wireless communication. In 2009 the Wi-MAX equipment sales are expected to hit 3 billion US dollars [3]. There are two types for Wi-MAX standards, i.e. fixed and mobile broadband data services. The later is more popular in recent years. For the IEEE 802.16e standard, the bandwidth is from 2GHz to 11GHz. The frequency bands of Wi-MAX are different in different

countries. For example, American uses 2.3GHz, 2.5GHz, and 5.8GHz, and Taiwan uses 2.3GHz and 2.5GHz. The 3.5GHz and 5.8GHz are used in fixed Wi-MAX systems. So in order to achieve all the requirement for those applications, the band switchable topology is desired. The thesis also discusses how to design band switchable LNA to fit the application of the multi-band Wi-MAX.

1.3 Transceiver

In communication system, one of the most popular transceiver architecture is the direct-conversion transceiver, because it does not need the image-rejection band-pass filter, and it only has two mixers and one local oscillator (LO). The direct-conversion transceiver architecture is shown in Fig. 1.2. It is known that the direct-conversion transceiver is similar to homodyne or zero-IF receiver. It receives the signals from antennas, and amplifies the signals by the LNA. It demodulates the signals by mixing them with the LO signals. After the demodulation, the frequency of the signals is down to be the baseband that can be used by analog-to-digital-converter (ADC). When the signals are converted to be digital, the digital-signal-process (DSP) can process the signals. The direct-conversion transceiver also transmits the signals from the DSP. The signals that from DSP is converted to be analog using digital-to- analog converter (DAC). The mixer also modulates the signals to high frequency band. The power amplifier (PA) amplifies and transmits the signal to antennas. Note that the signals created by LO is synthesized in the desired frequency carrier. They provide the quadrature phase signal for the quadrature mixer, because the two sideband of RF spectrum has the different information, the I and Q channels are needed. The low-pass filter is used to extracted desired signal. The filter also can be implemented with on-chip active circuits. The performance of receiver impacts the baseband signal, amplification, signal converting, and channel flitting, which are critical issues for transceiver design.

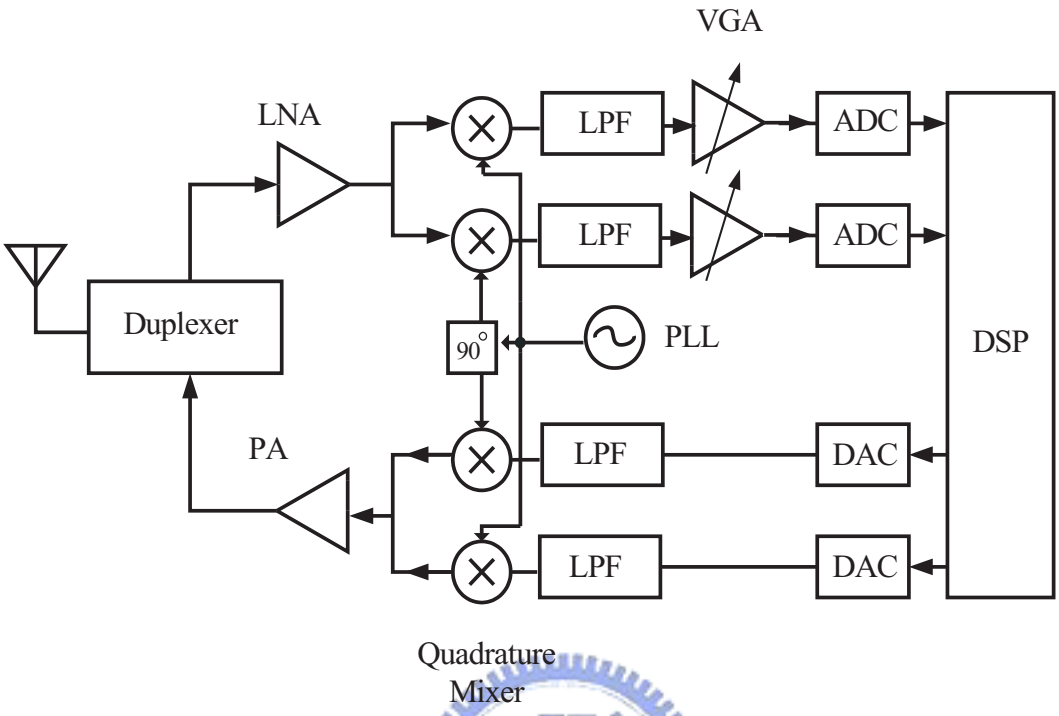


Figure 1.2: The Transceiver of direct-conversion transceiver.

1.4 Motivation and Contribution

In recent years, the market of wireless communication becomes large. For example, the cell phone and Bluetooth wireless headset. The requirements of wireless communication prefer low power, high speed and low cost, where the CMOS technology satisfies with these requirements. The CMOS technology has the advantages of low cost, integration, and increasing performance by scaling [4, 5]. In wireless communication, the transceiver is an important part which contains LNA, mixer, phase locked loops (PLL) and filter. LNA is the first stage of transceiver; its design determines the level noise and sensitivity of transceiver. In addition LNA should provide enough gain and very low noise contribution. Hence LNA is one of the most critical components in transceiver design.

As introduced in Sec. 1.1, UWB technology has become the solution of low cost, low power, high speed for wireless communication. In recent years, there

were some proposed UWB LNA topologies, e.q. [17][22][23]. In [17], the authors designed the 3.1GHz-10.6GHz wideband LNA for UWB receiver by common-gate input matching circuit. In [22], the authors also designed the wideband LNA for UWB by using three stage common-source amplifier and its bandwidth was from 3GHz to 6GHz. In [23], the authors optimized gain, noise, linearity and return losses of LNA for UWB applications. In UWB systems, the wideband input impedance matching is a crucial design challenge. There were some excellent wideband input impedance matching solutions proposed in [9] and [10]. In [10], the authors gave the broadband input matching. However we need to have the accurate transformer parameters. But the standard devices of TSMC 0.18μm does not include the transformer parameters. In [9], the authors used the topology in UWB LNA design is actually the Chebyshev filter. Although the topology also achieves the input matching, it needs four inductances. The inductance costs a lot of area. In our proposed design, we use the topology that contains a conventional source-degeneration input matching, an inductor shunted in input RF path and a capacitor seriesed in input RF path [9], because it does not need to exact transformer parameters and the number of inductances is one fewer than the Chebyshev filter. Then we present the analysis of input matching circuit for our designs. It is worth to emphasize the input matching analysis did not appear in conventional work. Our proposed analysis procedure can help a lot in adjusting the parameters used in input matching circuit.

Because the bandwidth of UWB is overlapping with other technology, e.g. WLAN, there should be some methods to avoid bandwidth overlapping. There are two solutions to avoid this. One is using switching-band, and another is using notch filter [16]. Because the quality factor (Q) in integrated circuit (IC) is in general low, the notch filter of IC does not good enough for UWB design. Although in [16], the authors used active notch filter to avoid low Q, it used more power. Another method is using switching band. The benefits of using switching band are that it do not need much device to achieve the application requirements and the noise of the other band can be removed because we do not use two bands simultaneously [6].

In recent years, various types of switches for switching narrow band LNA were proposed, e.q. [11][12][15]. In [11], the authors used PMOS as a switch in the load of LNA. However the mobility of PMOS is much lower than NMOS. Thus, its turn on resistance is large, which leads to a small quality factor and a low gain. In [12], the authors changed the passive device value by switching inductor. However the switching inductor needs large area. Although in [15], the authors used NMOS-based switch, its gain was not good enough.

To overcome these drawback, hence we use NMOS as switch. The large resistor can reduce the parasitic capacitance. Due to reduction of the parasitic capacitance, the size of the switch can be larger, which leads to a lower r_{on}. Thus the gain is larger when switch is on.

As introduced in Sec. 1.2, the Wi-MAX technology also prefer the solution of low cost, low power, high speed and larger coverage area. But Wi-MAX was different bands for different countries and different applications. Because there are four bands in Wi-MAX standards, using notch filter is too difficult to achieve the application requirements because it needs too many components to cut the bandwidth of the frequency that not in the application. In recent years, there were some proposed Wi-MAX LNA [13][18][19][24]. In [13], the authors were wideband band Wi-MAX LNA for 2GHz-11GHz, it was distorted by other interference. In [18], the authors used the notch filter to get the three bands of WI-MAX and WLAN, but noise was not good and it used five inductance. In [19], the authors were a LNA of band scalable receiver in 65nm CMOS for Wi-MAX. In [24], the authors were low power design for Wi-MAX LNA using capacitive cross coupling. In the thesis, we also proposed a band switchable LNA of Wi-MAX applications to reduce the other interference signal and uses all bands of Wi-MAX applications.

1.5 Thesis Organization

This thesis discusses about the LNA in UWB and Wi-MAX standards that all need the band switchable topology. The proposed LNA design used TSMC

0.18um CMOS technology. In this thesis we introduced two major topics: "A band switchable UWB LNA" and "A band switchable Wi-MAX LNA". In Chapter 2, we will discuss theoretical MOSFET noise model and noise theory. The classical theory of linearity and analysis of S-parameters, is presented in Sec. 2.2 and Sec. 2.3. Sec. 2.4 introduces some fundamentals of conventional LNA. In Chapter 3, a band switchable UWB LNA was proposed. The analysis of input matching circuit is presented in Sec. 3.2. The switch circuit topology of the LNA was discussed in Sec. 3.3. Also some design methodologies and layout consideration and trade-off are discussed here. The layout graph was presented in Sec. 3.6. The measurement and simulation result of the LNA was discussed in Sec. 3.7. Finally the second modified circuit was designed to achieve better performance in this chapter. In Chapter 4, a band switchable Wi-MAX LNA is proposed. The switch circuit in the LNA improves the circuit in Chapter 3. By connecting the loading capacitors to ground, we can remove one capacitor from the switch circuit in Sec. 3.3. Another contribution is to achieve the application of multi-band Wi-MAX. The simulation result of the LNA is discussed in Sec. 4.5. Conclusion and future work was given in Chapter 5.

Chapter 2

Background of LNA Design

In this chapter, the significant parameter, S-parameter is discussed in Sec. 2.1, the noise in MOSFET is introduced in Sec. 2.2. In Sec. 2.3 we discuss the linearity of LNA. Finally we analyze the noise of Complementary Metal-Oxide-Semiconductor (CMOS) and introduce various design of LNA in Sec. 2.4.

2.1 S-parameters

In radio-frequency (RF) design, The S-parameters are parameters for performance measurement. However the network that has many ports is too complicated to describe the characteristic of the network. Hence we usually use the two-port network that can be easily extended to the n-port network to describe the characteristic of system.In the system or network with two ports as illustrated in Fig.2.1, we often use the parameters including the y-parameters, h-parameters, and z-parameters to describe the systems in the analog design. Those parameters are expressed as follows:

$H - parameters$:

$$V_1 = h_{11}I_1 + h_{12}V_2, \tag{2.1}$$

$$I_2 = h_{21}I_1 + h_{22}V_2, \tag{2.2}$$

where

$$h_{11} = \frac{V_1}{I_1}|_{V_2=0},$$
$$h_{12} = \frac{V_1}{V_2}|_{I_1=0},$$
$$h_{21} = \frac{I_2}{I_1}|_{V_2=0},$$
$$h_{22} = \frac{I_2}{V_2}|_{I_1=0},$$

$Y - parameters$:

$$I_1 = y_{11}V_1 + y_{12}V_2,$$
$$I_2 = y_{21}V_1 + y_{22}V_2,$$

where

$$Y_{11} = \frac{I_1}{V_1}|_{V_2=0},$$
$$Y_{12} = \frac{I_1}{V_2}|_{V_1=0},$$
$$Y_{21} = \frac{I_2}{V_1}|_{V_2=0},$$
$$Y_{22} = \frac{I_2}{V_2}|_{V_1=0},$$

$Z - parameters$:

$$V_1 = Z_{11}I_1 + Z_{12}I_2, \tag{2.3}$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2, \tag{2.4}$$

where

$$Z_{11} = \frac{V_1}{I_1}|_{I_2=0},$$
$$Z_{12} = \frac{V_1}{I_2}|_{I_1=0},$$
$$Z_{21} = \frac{V_2}{I_1}|_{I_2=0},$$
$$Z_{22} = \frac{V_2}{I_2}|_{I_1=0}.$$

All the parameters of the networks are related to the total voltage and the total currents at both two ports. Hence the accuracy of the voltages and currents is demanded to obtain accurate the parameters. However in radio-frequency design the h, y, z-parameters cannot be measured, due to the following reasons,

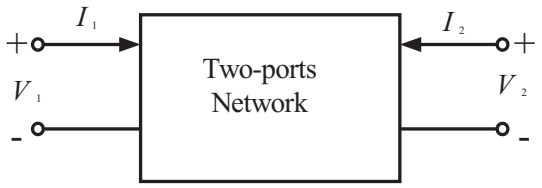


Figure 2.1: The two-ports network.

- Short and open network are difficult to obtain in the radio-frequency, since the coupling effect of capacitance and inductance, and the transmission line effect.
- The high frequency circuit is sensitive to the impedance and may lead to unstable or fail to work well when the terminal is open or short.
- The measured total voltage and the total current are not accurate in radio frequency due to coupling effect of capacitance and inductance.

Hence we need the parameters excluding h, y, z-parameters to describe the characteristic of the network. Let us explain this as follows. Let use add the transmission line in the two-port network as shown in Fig. 2.2, where E_{i1} is the wave voltage transmitted from the input port to the network, E_{r1} is the wave voltage reflected from the network to the input port, E_{i2} is the wave voltage transmitted from the output port to the network, and E_{r2} is the wave voltage reflected from the network to the output port. The voltage and current can be expressed as follows

$$V_1 = E_{i1} + E_{r1}, \tag{2.5}$$

$$V_2 = E_{i2} + E_{r2}, \tag{2.6}$$

$$I_1 = \frac{E_{i1} - E_{r1}}{Z_o}, \tag{2.7}$$

$$I_2 = \frac{E_{i2} - E_{r2}}{Z_o}, \tag{2.8}$$

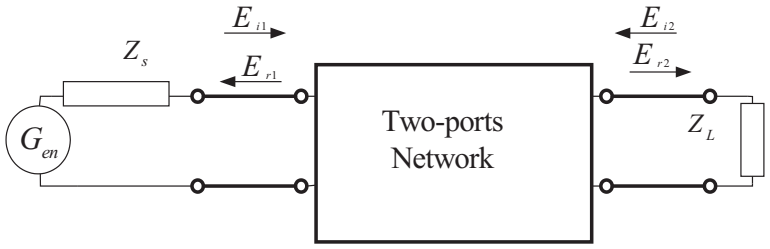


Figure 2.2: The two-ports network inserted in to a transmission line.

where Z_o is the characteristic impedance of the transmission line. Then we derive E_{r1} and E_{r2} in terms of the other parameters from the equation by replacing the total voltage and total current, so we derive the reflected traveling waves E_r which depends on the incident traveling voltage waves Ei by rearranging Eqs.(2.5)-(2.8), which leads to

$$E_{r1} = f_{11}E_{i1} + f_{12}E_{i2}, \tag{2.9}$$

$$E_{r2} = f_{21}E_{i1} + f_{22}E_{i2}, \tag{2.10}$$

where f_{11}, f_{12}, f_{21} and f_{22} are the new parameters of this network related to traveling voltage waves. Eqs.(2.9)-(2.10)is similar to that h-parameters in Eqs.(2.1)-(2.2), but they can also be expressed in other from like z-parameters in Eqs(2.3)-(2.4). By dividing the both sides of these equations by $\sqrt{Z_o}$, we can reexpress Eqs.(2.9)-(2.10) by

$$\frac{E_{r1}}{\sqrt{Z_o}} = \frac{f_{11}E_{i1}}{\sqrt{Z_o}} + \frac{f_{12}E_{i2}}{\sqrt{Z_o}}, \tag{2.11}$$

$$\frac{E_{r2}}{\sqrt{Z_o}} = \frac{f_{21}E_{i1}}{\sqrt{Z_o}} + \frac{f_{22}E_{i2}}{\sqrt{Z_o}}. \tag{2.12}$$

Let us define the following parameters

$$a_2 = \frac{E_{i2}}{\sqrt{Z_o}}, \qquad a_1 = \frac{E_{i1}}{\sqrt{Z_o}}, \tag{2.13}$$

$$b_2 = \frac{E_{r2}}{\sqrt{Z_o}}, \qquad b_1 = \frac{E_{r1}}{\sqrt{Z_o}}, \tag{2.14}$$

Let us define $s_{11} = f_{11}$, $s_{12} = f_{12}$, $s_{21} = f_{21}$, $s_{22} = f_{22}$, and Eqs.(2.11)-(2.12) are reexpressed as follows

$$b_1 = s_{11}a_1 + s_{12}a_2,$$
$$b_2 = s_{21}a_1 + s_{22}a_2,$$

where

$$s_{11} = \frac{b_1}{a_1}|_{a_2=0},$$
$$s_{12} = \frac{b_1}{a_2}|_{a_1=0},$$
$$s_{21} = \frac{b_2}{a_1}|_{a_2=0},$$
$$s_{22} = \frac{b_2}{a_2}|_{a_1=0}.$$

and s_{11}, s_{12}, s_{21} and s_{22} are called as the scattering parameters or simply S-parameters. As shown in Eqs.(2.13)-(2.14) the unit of s_{11}, s_{12}, s_{21} and s_{22} is the square root of power. Hence the S-parameters use the power of traveling wave rather than total voltage and total current at the ports at the radio-frequency. The two-port network for S-parameters is shown as Fig. 2.3.

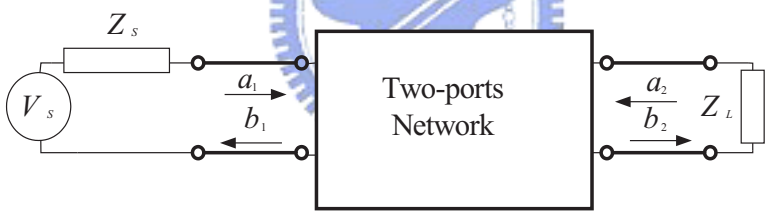


Figure 2.3: The two-ports network for S-parameters.

2.1.1 Multiple-Port Networks

As discussed in Sec. 2.1, let us derive the S-parameters of multiple-port network. For multiple-port network, the S-parameters for two-port network is not enough to measure the power transmission. To represent the S-parameters of multiple-port network, we usually use S-parameter matrix for this propose. Assume a multiple-port network has n ports, and every transmission line is lossless as shown in Fig. 2.4, where a_j is the incident traveling wave, and b_i is the reflected traveling wave. As the theory discussed in Sec. 2.1, the incident and reflected traveling

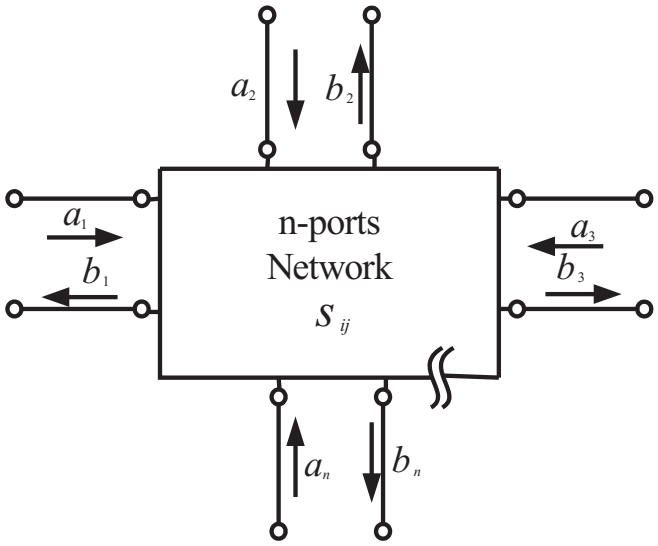


Figure 2.4: The N-ports network for S-parameters.

waves are related by

$$b_i = \sum_{i=j}^{n} s_{ij} a_j \quad for \quad i = 1, 2, 3, ..., n \quad , \tag{2.15}$$

where s_{ij} is the transmission coefficient that performs forward transmission from the jth port to the ith port when $i > j$, with all other ports impedance matched. s_{ij} is the transmission coefficient that performs reverse transmission from the jth port to the ith port when $i < j$, with all other ports impedance matched, and s_{ij} is the reflection coefficient that reflects from the ith port when $i = j$, with all other ports impedance matched. Therefore we can rearrange Eq.(2.15) as

$$\begin{aligned} b_1 &= s_{11}a_1 + s_{12}a_2 + s_{13}a_3 + ... + s_{1n}a_n, \\ b_2 &= s_{21}a_1 + s_{22}a_2 + s_{23}a_3 + ... + s_{2n}a_n, \\ &\vdots \\ b_n &= s_{n1}a_1 + s_{n2}a_2 + s_{n3}a_3 + ... + s_{nn}a_n. \end{aligned} \tag{2.16}$$

Represent Eq.(2.16) using matrix form Eq.(2.17) as follows

$$\begin{bmatrix} b_1 \\ b_2 \\ . \\ . \\ . \\ b_3 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & . & . & . & s_{1n} \\ s_{21} & s_{22} & . & . & . & s_{2n} \\ . & . & . & . & . & . \\ . & . & . & . & . & . \\ . & . & . & . & . & . \\ s_{n1} & s_{n2} & . & . & . & s_{nn} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ . \\ . \\ . \\ a_3 \end{bmatrix}, \tag{2.17}$$

which can be used in the multiple-port network.

2.1.2 Smith Chart

In order to solve transmission problem in radio-frequency signal, complex calculation is required. However the complex calculation is not intuitively to design the circuit of RF system. Hence a graphical solution is proposed by Philip H. Smith. The solution is called Smith chart that helps the designer to design circuit more intuitively. Before introducing the Smith chart, let us discuss the input impedance matching first, because an important application of Smith chart is input impedance matching. To design an LNA, the input impedance matching is necessary, because it helps to achieve the maximum power transfer requirement. An ideal input impedance matching means the load impedance of input is set to the complex conjugate of the input impedance. For example, the input matching impedance of $a + jb$ is $a - jb$. However the input impedance that we usually use in communication system is 50 ohm. Thus the complex conjugate impedance is also 50 ohm. Then we define the reflection coefficient, Γ, i.e. $s_{ij}(i = j)$, that is used in the impedance matching expressed as

$$\Gamma = \frac{Z - Z_o}{Z + Z_o}, \tag{2.18}$$

where Z_o is the characteristic impedance of a lossless transmission line. Eq.(2.18) can also be expressed by

$$\Gamma = \Gamma_r + j\Gamma_i = |\Gamma| e^{(j\theta_\Gamma)}, \tag{2.19}$$

where Γ_r and Γ_i are real part and imaginary part of the reflection coefficient, respectively. Γ is the ratio of signal reflected from input load to input port. In

addition the ideal condition for input matching is that Γ equals to zero. Because the load impedance usually has real part and imaginary part, we define the load impedance of the transmission line by $Z = R + jX$. Replacing Z by $R + jX$, Eq.(2.18) can be rewritten as

$$\Gamma = \frac{Z/Z_o - 1}{Z/Z_o + 1} = \frac{z-1}{z+1},$$

where

$$z = \frac{Z}{Z_o} = \frac{R}{Z_o} + j\frac{X}{Z_o} = r + jx, \tag{2.20}$$

and z is called normalized load impedance and r and x is the normalized load resistance and reactance, respectively. By rearrange Eq.(2.20) z can be described by

$$\begin{aligned} z &= \frac{1+\Gamma}{1-\Gamma} = \frac{1+|\Gamma|e^{(j\theta_\Gamma)}}{1-|\Gamma|e^{(j\theta_\Gamma)}} = r + jx \\ &= \frac{1+\Gamma_r+j\Gamma_i}{1-\Gamma_r-j\Gamma_i} = \frac{(1-\Gamma_r^2)-\Gamma_i^2+j2\Gamma_i}{(1-\Gamma_r)^2+\Gamma_i^2}. \end{aligned} \tag{2.21}$$

From Eq.(2.20) and Eq.(2.21), where

$$r = \frac{(1-\Gamma_r^2)-\Gamma_i^2}{(1-\Gamma_r)^2+\Gamma_i^2}, \tag{2.22}$$

and

$$x = \frac{2\Gamma_i}{(1-\Gamma_r)^2+\Gamma_i^2}. \tag{2.23}$$

Eqs.(2.22)-(2.23) are equations of circles. Thus we can draw circles on the Γ-plane. From the constant-r circle equation in Eq.(2.22), we have

$$\begin{aligned} & r[(1-\Gamma_r)^2+\Gamma_i^2] = (1-\Gamma_r^2)-\Gamma_i^2, \\ \Rightarrow\ & (1+r)\Gamma_r^2 - 2r\Gamma_r + (1+r)\Gamma_i^2 = 1-r, \\ \Rightarrow\ & \Gamma_r^2 - \frac{2r}{1+r}\Gamma_r + \left(\frac{r}{1+r}\right)^2 + \Gamma_i^2 = \frac{1-r}{1+r} + \left(\frac{r}{1+r}\right)^2, \\ \Rightarrow\ & \left(\Gamma_r - \frac{r}{1+r}\right)^2 + \Gamma_i^2 = \frac{1}{(1+r)^2}, \end{aligned}$$

where the center is $[r/(1+r), 0]$ and radius is $1/(1+r)$. Similarly from the constant-x circle equation in Eq.(2.23), we have

$$\begin{aligned} & x[(1-\Gamma_r)^2 + \Gamma_i^2] = 2\Gamma_i, \\ \Rightarrow\ & 1 - 2\Gamma_r + \Gamma_r^2 - \frac{2}{x}\Gamma_i + \Gamma_i^2 + \left(\frac{1}{x}\right)^2 = \left(\frac{1}{x}\right)^2, \\ \Rightarrow\ & (\Gamma_r - 1)^2 + \left(\Gamma_i - \frac{1}{x}\right)^2 = \left(\frac{1}{x}\right)^2, \end{aligned}$$

where the center is $[1, 1/x]$ and radius is $1/|x|$. The constant-r circles and the constant-x circles on the Γ-plane are shown in Fig. 2.5(a) and Fig. 2.5(b),which is called Smith chart.

Combining with the two circles, the Smith chart is shown in Fig. 2.6. We can get the reflection coefficient by pointing the impedance of the load $(r + jx)$ on the Smith chart or get the impedance of the load by pointing the reflection coefficient $(\Gamma = \Gamma_r + j\Gamma_i)$. As discussed before the perfect matching is at the point that reflection coefficient (Γ) is zero. When the normalized load resistance and reactance are 1 and 0, the actually resistance and reactance are Z_o and 0, respectively. In addition on the upper half plane of the Smith chart it always give the positive reactance. Hence it has the characteristic of the inductance. Similarly the lower half plane has the characteristic of the capacitance as shown in Fig. 2.7.

The Smith chart also has the admittance type, i.e. $Y = 1/z = g + jb$, where Y is the admittance of the load, g and b are the normalized load conductance and susceptance, respectively. The admittance Smith chart is shown in Fig. 2.8.

Similarly the lower half plane has the characteristic of the capacitance and the upper half plane has the characteristic of the inductance as shown in Fig. 2.9. In order to achieve impedance matching we can parallel and seriatim connect the lossless passive devices such as inductance and capacitor to match the impedance. However the combined impedance-admittance Smith chart is usually preferred, because using the admittance Smith chart to describe parallel connection of passive device is easier than impedance Smith chart. Hence by combining

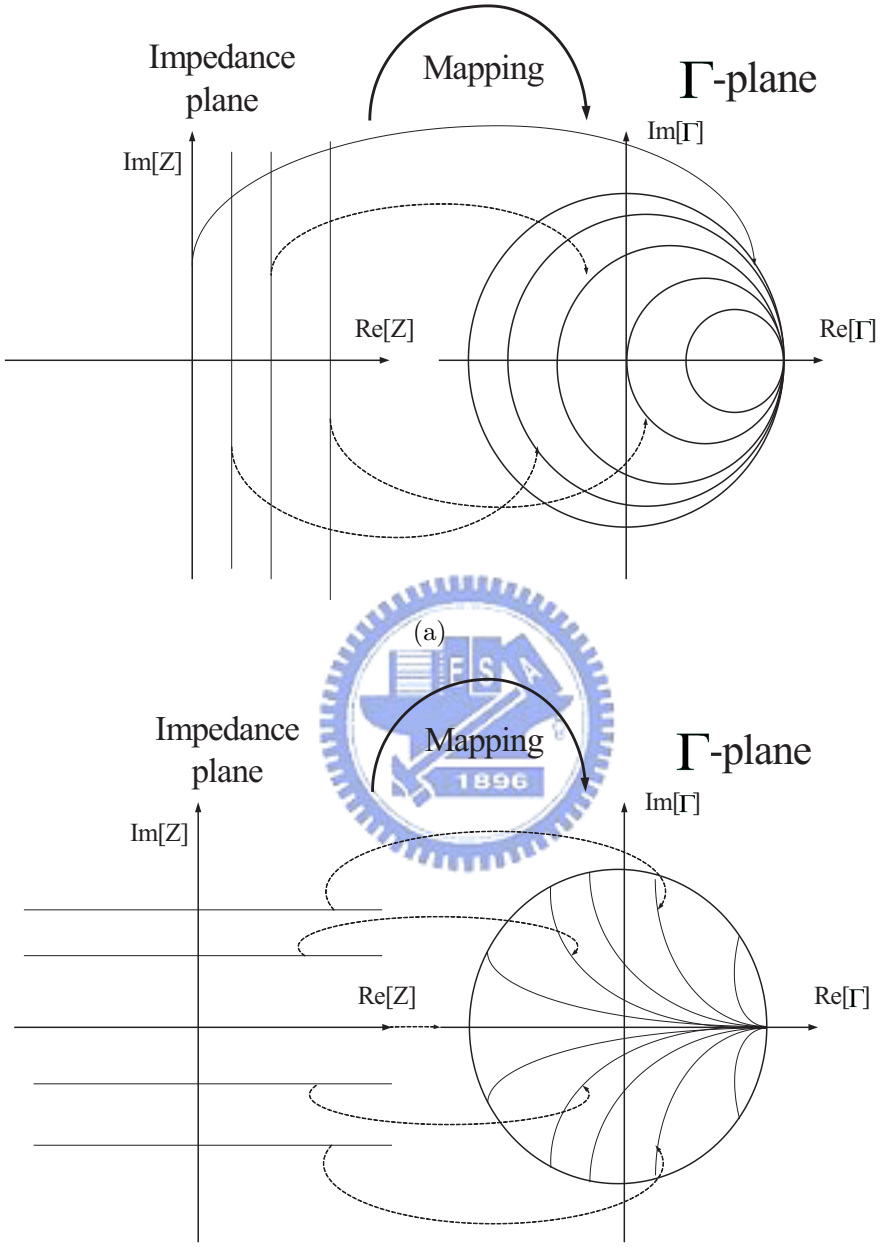


Figure 2.5: Mapping Smith chart from impedance plane: (a)constant-r. (b)constant-x.

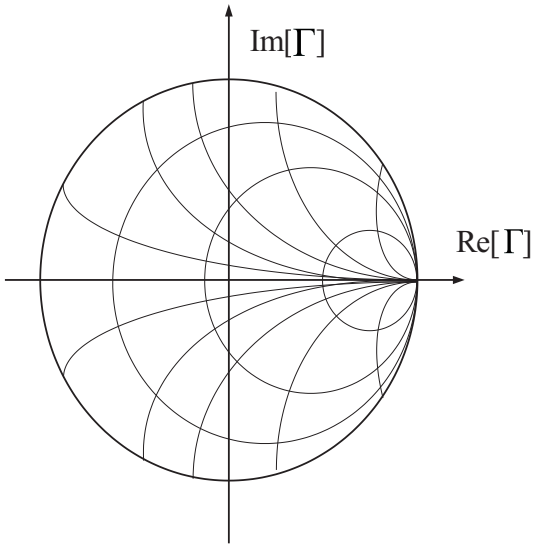


Figure 2.6: Smith chart.

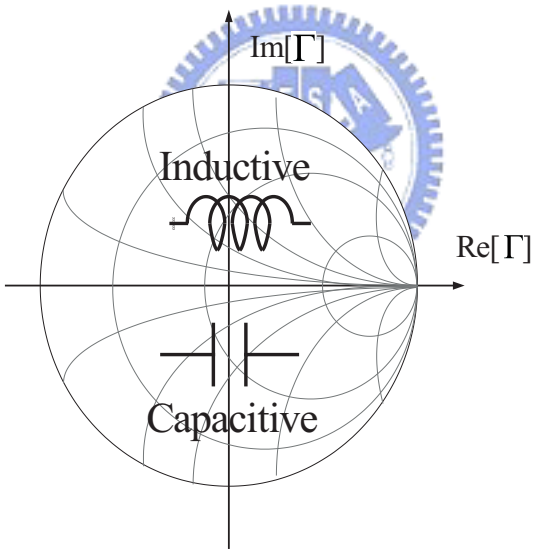


Figure 2.7: The characteristic of Smith chart.

the impedance Smith chart and admittance Smith chart, the Smith chart is drawn in Fig. 2.10. The characteristic of parallel and seriatim connected devices are shown in Fig. 2.11.

From the Smith chart, we can achieve the matching by series and parallel connection of inductance and capacitor. Note that the center of the Smith chart

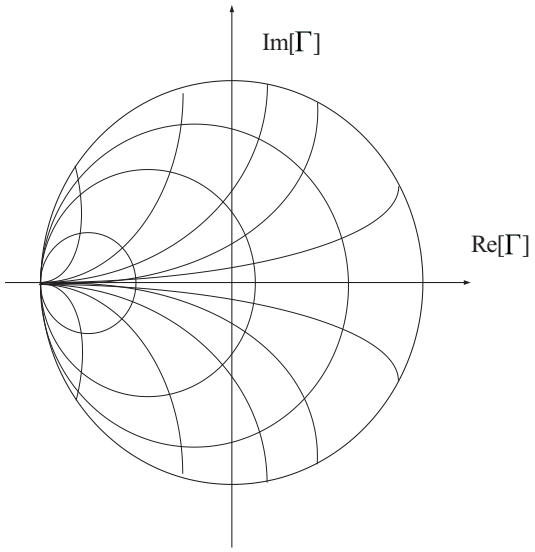


Figure 2.8: admittance Smith chart.

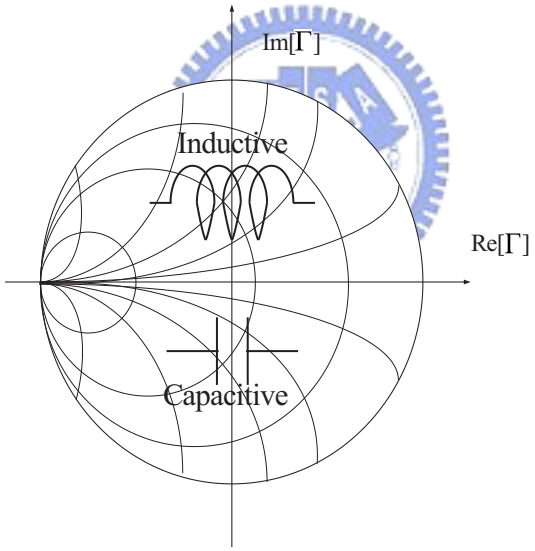


Figure 2.9: The characteristic of admittance Smith chart.

is the goal to reach. However there are many possible solutions for one matching condition. In addition the matching network usually uses lossless components like inductance, capacitor, transformer and transmission line, because lossy component like resistor leads to loss of power and induces noise. And it wastes the energy.

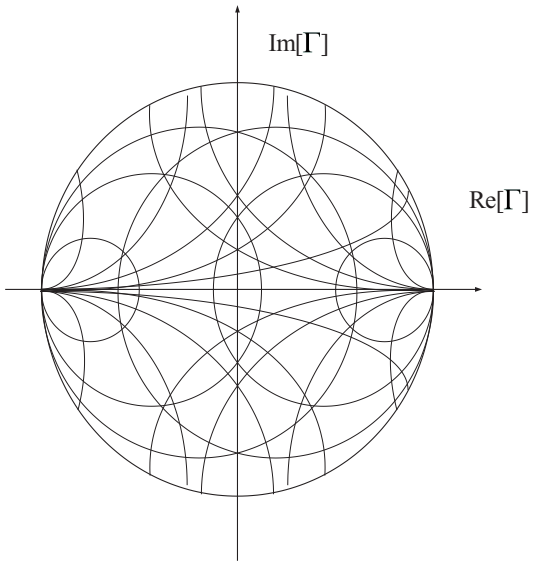


Figure 2.10: The combined impedance-admittance Smith chart.

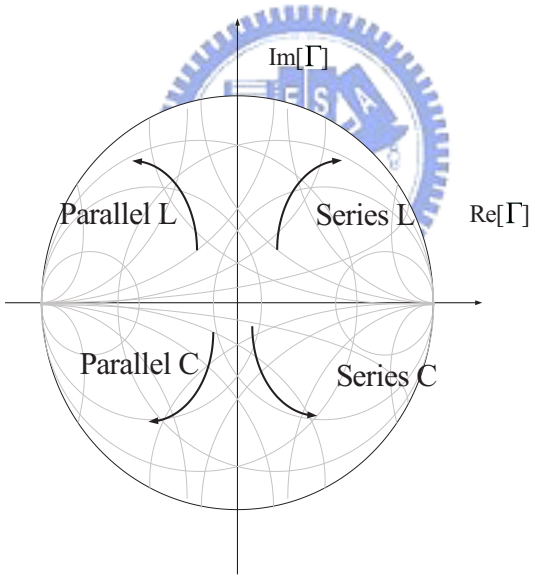


Figure 2.11: The series or parallel of the inductance or capacitor of Smith chart.

2.2 Noise in MOSFET

The noise in Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a significant issue for LNA design, because in LNA design MOSFET device will contribute the most noise when compared to the components such as inductance

and capacitor. Hence the analysis of noise for MOSFET is important for LNA. In order to analyze noise, the noise model of MOSFET is needed. Important parameters to analyze noise are input-referred noise, signal-to-noise ratio, and noise figure [6]. Let us discuss the noise source in LNA design as follows:

2.2.1 Flicker Noise

One of the noises in the MOSFET is flicker noise that arises from the channel of MOSFET. The effect is due to that the interface of the oxide-silicon in the MOSFET traps the charges. The noise density of flicker noise in the gate can be presented by

$$\overline{v_n^2} = \frac{K}{WLC_{ox}f} \tag{2.24}$$

where K is the process-dependent constant [6]. From Eq.(2.24), the flicker noise is small in high frequency. Hence in radio-frequency design the flicker noise is not a significant issue.

2.2.2 Thermal Noise

The thermal noise is produced by the thermal agitation of the charge carriers. The thermal noise is from the resistance in the circuit such as the resistor, the channel resistance of MOS and the gate resistance of MOS. It depends on the absolute temperature (T). The higher the absolute temperature is, the larger the thermal noise is. So the thermal noise can be described by $P_{av} = kT\triangle f$, where $\triangle f$ is the noise bandwidth per hertz and k is Boltzmann's constant. In the normal temperature ($25C^{\circ}$), the noise power per Hz is $1.38 \times 10^{-23} \times 293\ (25C^{\circ}) = 4 \times 10^{-18}\ mW = -174\ dBm$. The value of -174 dBm is also called the noise floor, because it is like floor below the signal. In addition the thermal noise is as a random distributed signal, and it is Gaussian white distributed. The thermal noise can be described in form of voltage square by

$$\overline{v_n^2} = 4kTR\triangle f \tag{2.25}$$

where R is the resistance as shown in Fig. 2.12 . We can also get the thermal noise in form of current square described by $\overline{i_n^2} = 4kT(1/R)\triangle f$ from Eq.(2.25).

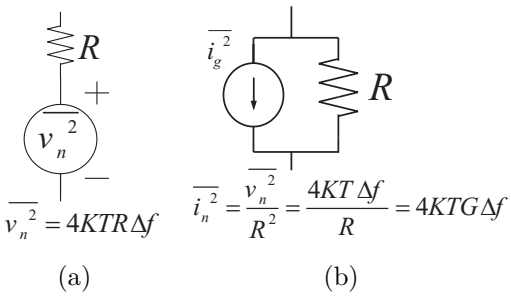


Figure 2.12: A thermal noise model: (a) voltage type, (b) current type.

2.2.3 Drain Noise

The drain noise is the channel noise of MOSFET that is from the voltage control resistor of MOS channel. It can be described by

$$\overline{i_d^2} = 4kT\gamma g_{d0}\triangle f,$$

where the g_{d0} is the drain conductance of the device when V_{DS} is zero , and γ is a bias dependent factor that is unity when V_{DS} is zero. In the long channel device, γ decreases toward a value of 2/3 in saturation. But in short channel device, γ is greater than 2/3. Hence the γ can be larger by using more advanced technology process, because of use of the short channel. The model of drain Noise can be as illustrated in Fig. 2.13. The noise current source is connected between the drain and source of MOS. [7]

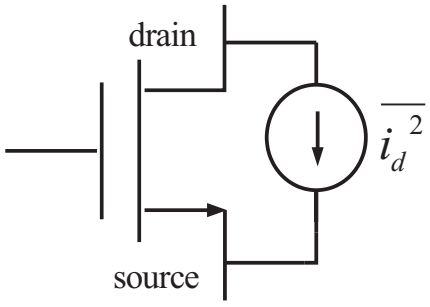


Figure 2.13: Drain noise model.

2.2.4 Gate Noise

Besides channel noise, other significant noise source is the gate noise, which is due to the channel charge with thermal agitation. Because the channel voltage variation couples to the gate directly, the gate terminal produces a noise source. This noise can be neglected at low frequencies, but it still affects the noise performance at radio frequencies due to the coupling. The gate noise can be expressed as

$$\overline{i_g^2} = 4kT\delta g_g \triangle f, \tag{2.26}$$

where g_g is conductance of noise source given by

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}, \tag{2.27}$$

δ is the coefficient of gate noise. The value of δ is 4/3 for long-channel devices. Eq.(2.27) obtained with assumption that the MOS working in saturation mode. The noise source has two models i.e. current model and voltage model. The noise model of gate noise in the MOS is shown in Fig. 2.14, where the g_g connects between the gate and source, and the resistor (r_g) is connected series with the parasitic capacitor (C_{gs}). The gate noise depends on the frequency. The higher

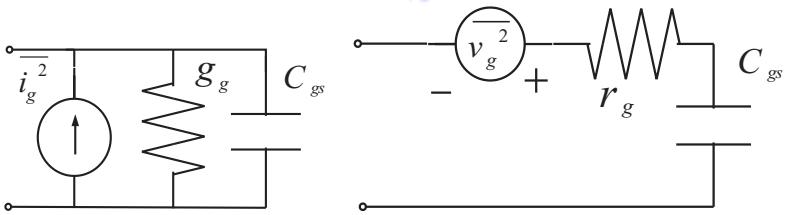


Figure 2.14: The gate noise model: (a)voltage type. (b)current type.

the frequency is, the larger the noise is. Because the gate noise is correlated to the drain noise, we use the correlation coefficient to describe the correlation. The correlation coefficient can be expressed as

$$c = \frac{\overline{i_g \cdot i_d^*}}{\sqrt{\overline{i_g^2} \cdot \overline{i_d^2}}} = 0.395j.$$

This case is for long channel device that has the correlation coefficient with value $0.395j$. Using the correlation coefficient, we can re-express Eq.(2.26) by

$$\overline{i_g^2} = 4kT\delta g_g(1-|c|^2)\triangle f + 4kT\delta g_g|c|^2\triangle f, \tag{2.28}$$

where the first item is the uncorrelated gate noise and the second item is the gate noise correlated to drain noise.

2.2.5 Noise Figure

The noise figure (NF) is an important specification for LNA design. In analog circuit design we usually use the signal-to-noise-ratio (SNR) to describe the noise performance of a circuit. It is defined as the ratio of the total signal power to the total noise power as described by

$$SNR = \frac{the\ \ total\ \ signal\ \ power}{the\ \ total\ \ noise\ \ power}. \tag{2.29}$$

In RF design the parameter that describes the noise performance is the noise figure, because of its computation convenience and the tradition. Since there are different definitions for noise figure, we choose the most popular definition here. The definition of the noise figure is

$$10\log_{10}(F),$$

where F is the noise factor, which is the input SNR over the output SNR expressed by

$$F = \frac{SNR_{in}}{SNR_{out}}, \tag{2.30}$$

where SNR_{out} and SNR_{in} are the signal-to-noise-ratio measured at the output and the input, respectively. Note that the noise factor is always larger than 1. Because if the system is ideal noiseless, it means the noise contribution is zero. Hence SNR_{out} is equal to SNR_{in}, and the noise factor is the minimum value of 1. When the noise factor is the minimum, the noise figure also has the minimum value of 0 dB, but it is unlikely to achieve the noise performance of noise figure of 0 dB because there is always noise in the circuit. To analyze the noise factor,

we usually calculate the total output noise due to the source and the total output noise, because from Eq.(2.30), the noise factor can be re-expressed as

$$\begin{aligned} noise\ \ factor &= \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{S_{in}}{S_{out}}\frac{N_{out}}{N_{in}} = \frac{N_{out}}{GN_{in}} \\ &= \frac{total\ \ output\ \ noise}{total\ \ output\ \ noise\ \ due\ \ to\ \ input}, \end{aligned} \tag{2.31}$$

where $G = S_{out}/S_{in}$ is the gain of LNA, so we can get the noise factor by calculating the total output noise due to the source and the total output noise. Hence calculating noise factor can be easier, and we will use the rule in Sec. 2.4.

Another critical specification of system dependent on noise figure is the sensitivity, which is the minimum signal level able to be detected with acceptable signal-to-noise-ratio. In order to calculate the sensitivity, we re-express the noise factor as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{P_{sig}/P_{R_s}}{SNR_{out}},$$

where P_{R_s} is the source resistance noise power per Hz, and P_{sig} is the input signal power per Hz. Hence $P_{sig} = P_{R_s} \cdot F \cdot SNR_{out}$. P_{sig} is the unit bandwidth signal power. Thus to get the full bandwidth signal power we integrate the unit bandwidth signal power over the bandwidth. Hence for the flat channel, $P_{sig,tot} = P_{R_s} \cdot F \cdot SNR_{out} \cdot B$, where B is the bandwidth of the channel, $P_{sig,tot}$ is the total signal power of the bandwidth. Usually the unit of power is dBm, so we replace the milliwatt with dBm. Hence we can get the total signal power expressed as $P_{in,min}|_{dBm} = P_{R_s}|_{dBm/Hz} \cdot NF|_{dB} \cdot SNR_{out}|_{dB} \cdot 10\log_{10}(B)$, where $P_{in,min}$ is the minimum total signal power level that can achieve the minimum requirement of signal-to-noise-ratio. If our circus has the conjugate input matching, P_{RS} is the noise floor, -174 dBm per Hz. By replacing P_{RS} with noise floor, the minimum total signal power level is $P_{in,min} = -174dBm/Hz + NF + 10\log_{10}(B) + SNR_{min}$. Hence the overall bandwidth noise floor of the system is the sum of the first three items, and we can increase the sensitivity by decreasing the bandwidth [6].

2.2.6 Noise factor in cascaded circuits

In order to get the total noise factor in the system, we should analyze the noise factor in the cascaded circuit, because the system usually consists of multiple stages. From Eq.(2.31), the noise factor is

$$F = \frac{1}{G}\frac{N_{out}}{N_{in}},$$

where $N_{out} = N_a + GN_{in}$, and N_a is the noise contribution of the circuit. For a two-stage circuit we define G_1 be the gain of the first-stage circuit, G_2 be the gain of the second-stage circuit, N_1 be the noise contribution of the first-stage circuit, and N_2 be the noise contribution of the second-stage circuit as shown in Fig. 2.15, respectively. The amplifier not only amplifies the signal from the input but also the noise from the input. Hence the first stage amplifies the noise and signal, the output noise is $N_1 + G_1N_{in}$. Similarly the output noise of the second stage is $N_2 + G_2(N_1 + G_1N_{in})$. So the final noise factor is the output noise over the input noise multiplied by the total gain given by

$$F = \frac{1}{G}\frac{N_{out}}{N_{in}} = \frac{N_2 + G_2N_1 + G_1G_2N_{in}}{G_1G_2N_{in}} = 1 + \frac{N_1}{G_1N_{in}} + \frac{N_2}{G_1G_2N_{in}}$$

$$= F_1 + \frac{F_2 - 1}{G_1}, \tag{2.32}$$

where

$$F_1 = 1 + \frac{N_1}{G_1N_{in}} \text{ and } F_2 = 1 + \frac{N_2}{G_2N_{in}},$$

Based on the noise factor of the two-stage cascaded circuit in Eq.(2.32), we can achieve the noise factor of the N-stage cascaded circuit shown in Fig. 2.16.

The noise factor of the N-stage cascade circuit can be expressed as

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \cdots + \frac{F_n - 1}{G_1G_2 \cdots G_{n-1}}, \tag{2.33}$$

where F_1 is the noise factor of the first stage, F_2 is the noise factor of the second stage and so on. From Eq.(2.33) if the gain of the first stage is large enough, the other items excluding F_1 can be neglected, and the total noise factor is equal to

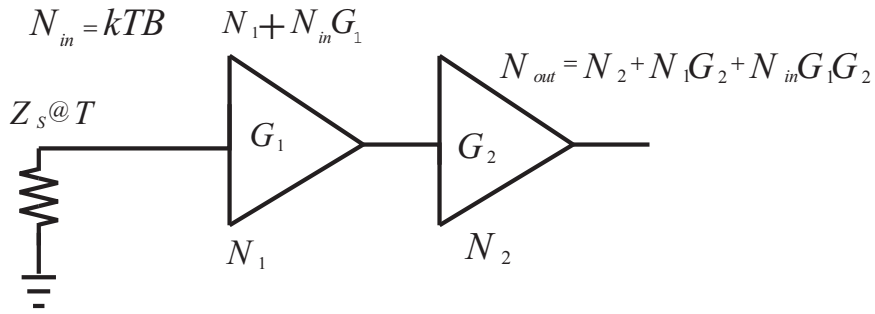


Figure 2.15: cascade noise model.

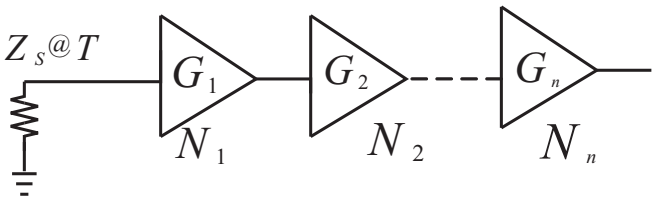


Figure 2.16: N-stage noise model.

the first stage noise factor. In other words, the total noise factor is dominated by the first stage noise factor if G_1 is large enough. This is why the first stage of transceiver is called low noise amplifier.

2.3 Linearity

The linearity is defined by the superposition. If the input signal is x and the output signal is y, they should have two characteristics. One is additivity, another is homogeneity. That is if $y_1 = f(x_1)$, $y_2 = f(x_2)$, $ay_1 + by_2 = f(ax_1) + f(bx_2)$, a and b can be any value of constant. If any system does not follow the rule, it is nonlinearity system. However most system in natural is nonlinear system. But in RF design we expect that all the systems are linear, because the linear system can be solved more easily. Hence the LNA design should take care of the linearity. By the way the linearity of system is also limited by the mixer design. If the signal passes thought the nonlinear system as shown in Fig. 2.17, the system can product many harmonics, so the output signal can be expressed as

$$V_{out} = a_1V_{in} + a_2V_{in}^2 + a_3V_{in}^3 + \cdots,$$

where V_{out} is output voltage, V_{in} is input voltage, $a_1, a_2, a_3...$ are the coefficients. By replacing V_{in} by the sinusoidal signal, $V_{in} = A\cos\omega t$, the nonlinear output can be re-expressed as

$$\begin{aligned} V_{out} &= a_1 A\cos\omega t + a_2 A^2\cos\omega t^2 + a_3 A^3\cos\omega t^3 + \cdots \\ &= a_1 A\cos\omega t + \frac{a_2 A^2}{2}(\cos 2\omega t + 1) + \frac{a_3 A^3}{4}(\cos 3\omega t + 3\cos\omega t) + \cdots \\ &= \frac{a_2 A^2}{2} + \left[a_1 A + \frac{3a_3 A^3}{4}\right]\cos\omega t + \frac{a_2 A^2}{2}\cos 2\omega t + \frac{a_3 A^3}{4}\cos 3\omega t + \cdots \end{aligned} \quad (2.34)$$

where $a_2 A^2/2$ is the DC offset, $\cos\omega t$ is the fundamental frequency signal that we want, and the other items are the harmonic terms. Because the harmonic terms

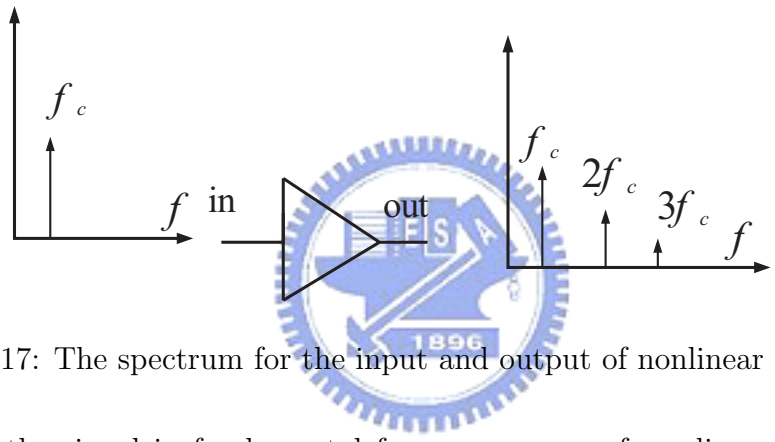


Figure 2.17: The spectrum for the input and output of nonlinear amplifier.

can distort the signal in fundamental frequency, we prefer a linear system. In order to get non-distortional signal, the design of linearity is taken seriously. To describe the linearity performance, P_{1dB} and IIP_3 are usually used in RF design. The P_{1dB} can be regarded as the gain compression of the system. The output and input signal usually have the linearity when the input signal is not too large, but when the input signal is too large, the linearity rule breaks. From Eq.(2.34) the signal gain can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{[a_1 A + \frac{3a_3 A^3}{4}]\cos\omega t}{A\cos\omega t} = a_1 + \frac{3a_3 A^3}{4}, \quad (2.35)$$

where a_3 is usually smaller than 0, so the gain can decrease to 0 when the input signal is too large. Hence we define the input value at the gain compressed $1dB$ point as P_{1dB}. From Eq.(2.35) the 1-dB gain compression point is described by

$20\log|a_1|-1dB = 20\log|a_1+(3/4)A^2_{1-dB}a_3|$. So the point is $A_{1-dB} = \sqrt{0.145|\frac{a_1}{a_3}|}$, we can draw it on the output and input transform plot as shown in Fig.2.18. Other factor that affect the linearity is the intermodulation distortion. When the

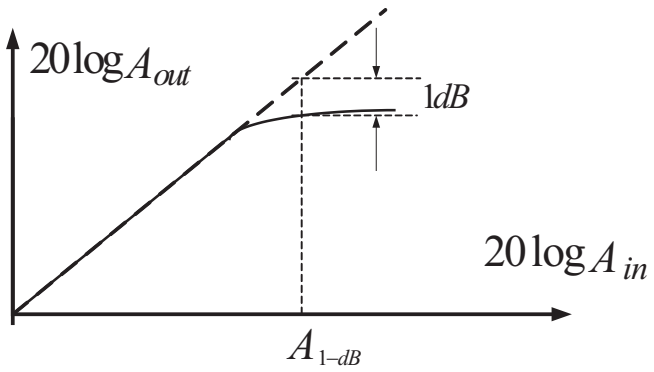


Figure 2.18: Definition of the 1-dB compression point.

system has the two or more interference sources as shown in Fig. 2.19. As the sum of two input interference is $V_{in} = A_1\cos\omega_1 t + A_2\cos\omega_2 t$, the output can be expressed as

$$V_{out} = a_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) + a_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 + a_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 + ...$$

Because the calculation is too complex, we list the items in different angular frequency in Tab. 2.1. Because the 3^{rd}-order harmonic may be directly located in

Frequency(ω)	harmonic
$\omega_1 \pm \omega_2$	$a_2A_1A_2\cos(\omega_1+\omega_2)t + a_2A_1A_2\cos(\omega_1-\omega_2)t$
$2\omega_1 \pm \omega_2$	$\frac{3a_3A_1^2A_2}{4}\cos(2\omega_1+\omega_2)t + \frac{3a_3A_1^2A_2}{4}\cos(2\omega_1-\omega_2)t$
$2\omega_2 \pm \omega_1$	$\frac{3a_3A_2^2A_1}{4}\cos(2\omega_2+\omega_1)t + \frac{3a_3A_2^2A_1}{4}\cos(2\omega_2-\omega_1)t$
ω_1, ω_2	$[a_1A_1 + \frac{3a_3A_1^3}{4} + \frac{3a_3A_1A_2^2}{2}]\cos\omega_1 t + [a_1A_2 + \frac{3a_3A_2^3}{4} + \frac{3a_3A_1^2A_2}{2}]\cos\omega_2 t$

Table 2.1: The harmonic of different ω.

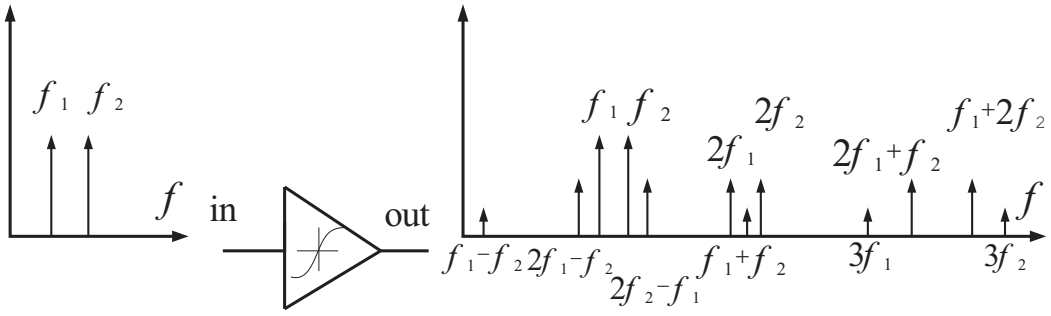


Figure 2.19: The spectrum of the nonlinear circuit with two tone input.

the channel, the signal in the desired channel is distorted. Hence in order to describe the nonlinearity due to interference, we define the input 3^{rd}-order intercept point (IIP_3) be the input signal level at the point that the 3^{rd}-order intermodulation distortion equals to the input signal excluding the gain compression as shown in Fig. 2.20. When the input signal is at IIP_3, it means that the power in

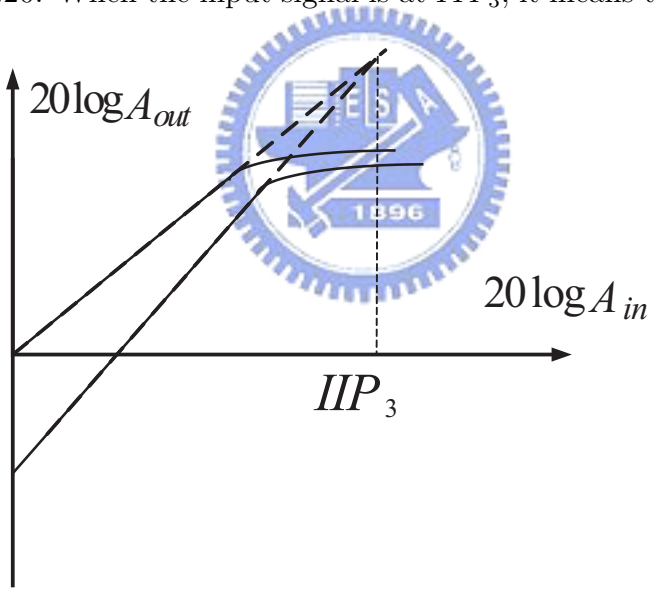


Figure 2.20: Definition of the IIP_3 point.

fundamental frequency is the minimum acceptable value, because the distortion and the signal are at the same level.

2.4 LNA Architectures

In this section we discuss about some basic LNA architectures that are usually used in the RF design. From sections in Chapter 2, the LNA design cares about power gain (s_{21}), noise figure (NF), linearity (P_{1dB}, IIP_3), and reflection coefficient (s_{11}), but those are trade-off parameters. Hence the design of LNA is to get the balance of all the parameters.

In LNA design, one of the critical design issues is the reflection coefficient, because it represents the amount of signal power reflected in the input stage. Since communication systems usually choose the 50 ohm to be the input impedance value. (50 ohm has the properties of low loss and high power transfer rate), the input impedance of LNA should be designed to be 50 ohm.

In basic amplifier design, there are two types of topology that are usually used. One is common source amplifier, the other is common gate amplifier. There are some topologies of input impedance matching for LNA including common source amplifier with shunt input resistor, common gate amplifier, shunt-series amplifier, and inductive source degeneration as shown in Fig. 2.21.

The first one technique is common source amplifier with shunt input resistor as shown in Fig. 2.21(a), where 50-ohm the resistor connects the input directly to get the perfect input impedance matching, but the noise contribution is the worst, because the added input resistor contributes the noise that equals to the source noise. Also the added input resistor attenuates the input signal as well, and the attenuated power can contributes the noise. Because the bad noise performance of the architecture, it is difficult to apply it to the general RF receivers that demand good input impedance matching.

The second one is shown in Fig. 2.21(b), where the common gate amplifier that uses the common gate stage as the input terminal. The input impedance of the common gate can be calculated by $1/(g_m + g_{mb}) = 50\Omega$, where g_m is transconductance of the input stage, g_{mb} is the back-gate transconductance of the input stage, they are all designed to achieve the input impedance of 50 ohm. By noise analysis the noise factor can be expressed as $F = 1 + \frac{\gamma}{\alpha}$ when the

input impedance is matched, where α is the ratio of the device g_m and drain conductance g_{d0} when $V_{DS} = 0$, and γ is the coefficient of the channel thermal noise [6]. For the short-channel device α is always smaller than one and γ is greater than one. For long channel devices γ is 2/3 and α is 1. By replacing γ and α with the values in the long channel devices the noise factor is $F = 1 + \frac{\gamma}{\alpha} \geq \frac{5}{3} = 2.2\ (dB)$. Hence the common gate amplifier architecture of LNA can achieve the minimum noise figure value of $2.2dB$.

The third LNA architecture is shunt-series amplifier that achieves the input impedance matching and output impedance matching by the series and shunt feedback resistors as shown in Fig. 2.21(c). The shunt-series amplifier architecture always have high power consumption compared to others under similar noise performance. However the shunt-series amplifier architecture can be used in some wideband LNA designs, because it is easy to get the wideband impedance matching. But for narrow band LNA design the shunt-series amplifier architecture is not popular, due to its high power dissipation.

The fourth LNA architecture is the inductive source degeneration LNA as shown in Fig. 2.21(d). The inductances connect to the source and gate of the input stage. In the input impedance the inductive source degeneration contributes a real term as we will show later. And it also has the opportunity to achieve the best noise performance, because it also achieve the noise match [20]. However since the inductances are sensitive to the frequency, the inductive source degeneration is utilized in narrow band LNA design. The wideband input matching circuit will still contain the inductive source degeneration architecture as will be introduced in Chapter 3. The inductive source degeneration LNA is discussed in the following subsection.

2.4.1 The Analysis of Inductive Source Degeneration LNA

The well known method, inductive source degeneration LNA [8], to optimize the noise performance was proposed by Thomas H. Lee and Derek K. Shaeffer in 1997. The inductive source degeneration cascode LNA and the input stage noise model are shown in Fig. 2.22 and Fig. 2.23. The cascode topology has high isolation

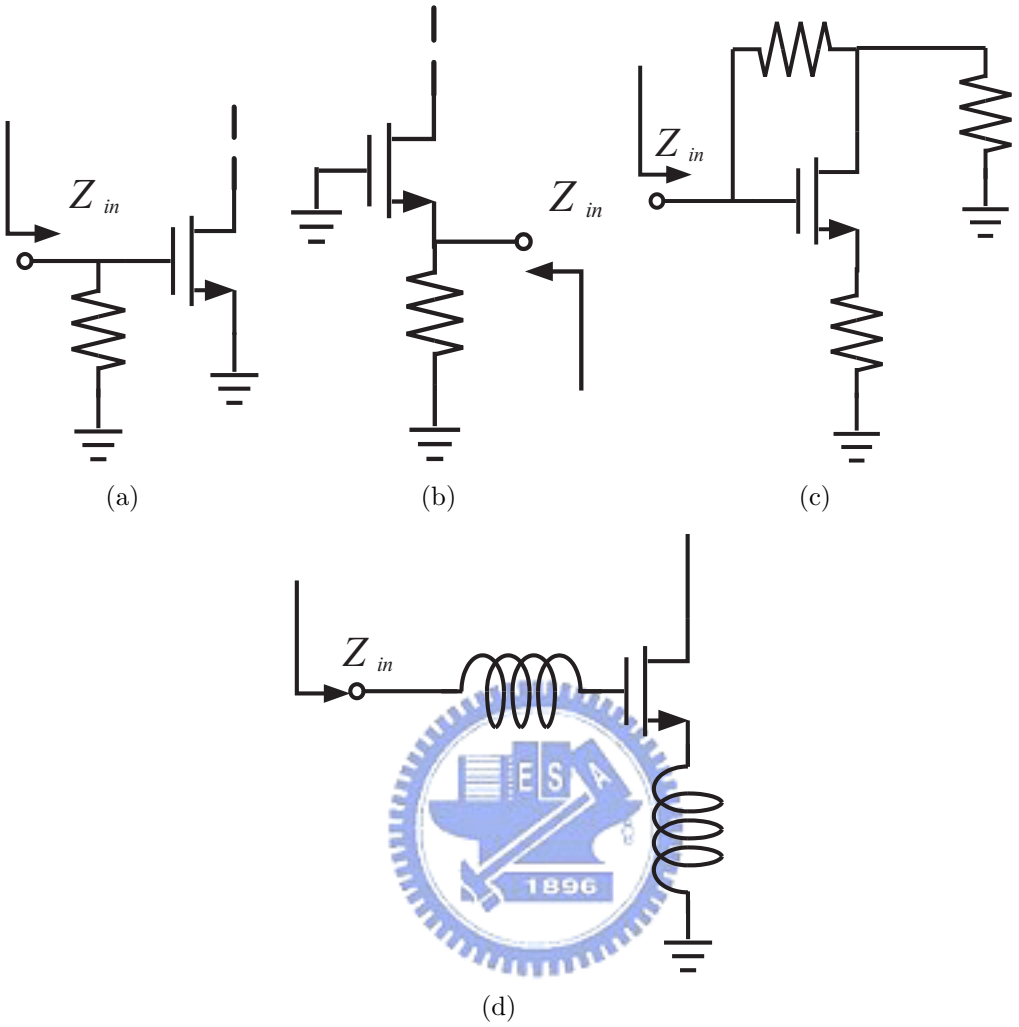


Figure 2.21: The LNA architecture: (a) common source amplifier with shunt input resistor. (b) common gate amplifier. (c)shunt-series amplifier. (d)inductive source degeneration.

property between the input and output. Since the most important influence on input impedance and noise performance is the input stage, we discuss the input stage noise factor in this section.

The input matching of this circuit is distributed by

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} = \omega_T L_s \quad \left(at \ \ \omega = \omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \right), \tag{2.36}$$

where $\omega_T L_s = g_m / C_{gs}$, C_{gs} is the parasitic capacitance of the input stage, L_s is the

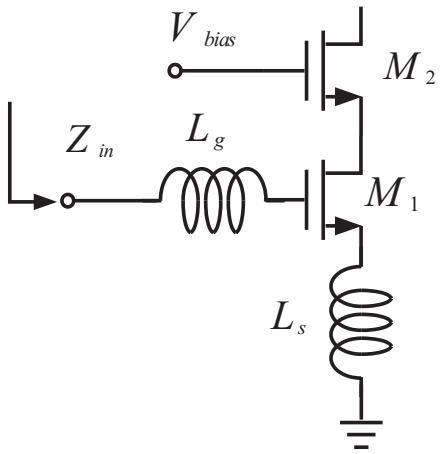


Figure 2.22: The cascode LNA architecture.

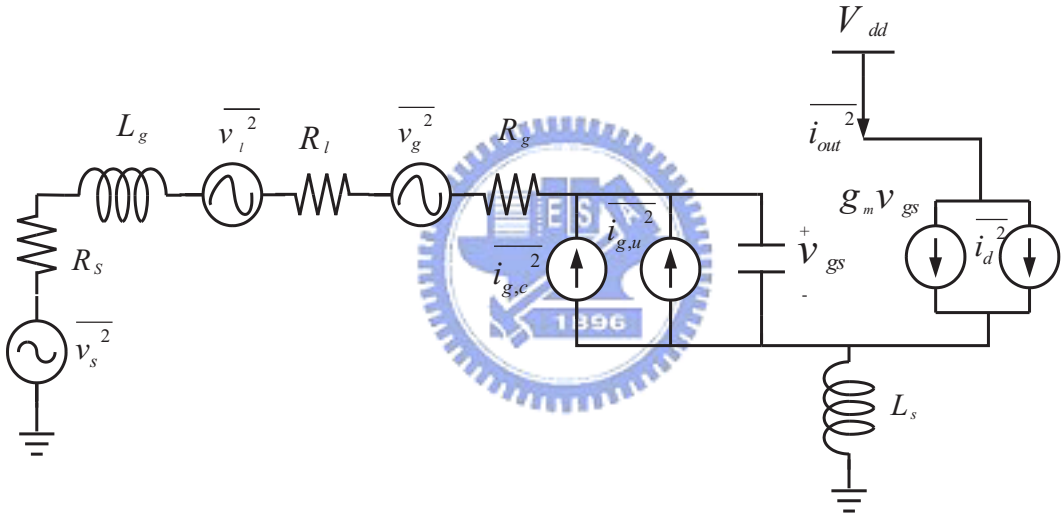


Figure 2.23: The noise model of inductance source degeneration LNA.

source degeneration inductance, L_g is the gate inductance, g_m is transconductance of the input stage. The input impedance Z_{in} is equal to the multiplication of L_s and ω_T at resonant frequency. This value is designed to be 50 ohm for input matching. From Fig. 2.23 R_g is the gate resistor of the input stage and R_l is the parasitic resistor of the gate inductance, R_g contributes the noise, called $\overline{v_g^2}$ and R_l also contributes the noise, called $\overline{v_l^2}$. The current noise source $\overline{i_d^2}$ is the channel thermal noise of the input NMOS, $\overline{i_{g,u}^2}$ and $\overline{i_{g,c}^2}$ are the gate noise that are correlated and uncorrelated term, respectively. In the analysis we neglect

the noise contribution of next stage, because the input stage gives sufficient gain of LNA. From Eq.(2.30) the noise factor is the total output noise over the total output noise due to the source. Hence in order to get the total output noise when the amplifier is driven by a 50-ohm source we calculate the transconductance of the input stage first. Because the output current is proportional to the voltage on C_{gs} and the input stage takes the form of a series-resonant network, G_m can be expressed as

$$G_m = g_m Q_{in} = \frac{g_{m1}}{\omega_o C_{gs}(R_s + \omega_T L_S)} = \frac{\omega_T}{\omega_o R_s(1 + \frac{\omega_T L_s}{R_s})} = \frac{\omega_T}{2\omega_o R_s}, \tag{2.37}$$

where Q_{in} is the effective Q of the amplifier input circuit. Define 50-ohm source noise power density is $S_{src}(\omega_o)$. From Eq.(2.37), the output noise power density due to the 50-ohm source ($S_{a,src}(\omega_o)$) can be expressed as

$$S_{a,src}(\omega_o) = S_{src}(\omega_o)G_m^2 = \frac{4kT\omega_T^2}{\omega_o^2 R_s(1 + \frac{\omega_T L_S}{R_s})^2}. \tag{2.38}$$

Similarly the output noise power density due to R_g and R_l is

$$S_{a,R_l,R_g}(\omega_o) = \frac{4kT(R_l + R_g)\omega_T^2}{\omega_o^2 R_s^2(1 + \frac{\omega_T L_S}{R_s})^2}. \tag{2.39}$$

Then the most important noise contributor of the LNA is the channel current noise of the input MOS device, so we calculate $\overline{i_d}$ by expressing the power spectral density of the source, one can derive that the output noise power density from the source given by

$$S_{a,i_d}(\omega_o) = \frac{\overline{i_d^2}/\triangle f}{(1 + \frac{\omega_T L_S}{R_s})^2} = \frac{4kT\gamma g_{do}}{(1 + \frac{\omega_T L_S}{R_s})^2}.$$

The noise power density of the correlating part of the gate noise to drain noise is

$$S_{a,i_d,i_g,c}(\omega_o) = \kappa S_{a,i_d}(\omega_o) = \frac{4kT\kappa\gamma g_{do}}{(1 + \frac{\omega_T L_S}{R_s})^2},$$

where

$$\kappa = \left[1 + |c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 + \frac{\delta\alpha^2}{5\gamma}|c|^2,$$

$$Q_L = \frac{1}{\omega_o R_s C_{gs}},$$

and

$$\alpha = \frac{g_m}{g_{do}}.$$

The noise power density of the uncorrelated part of the gate noise is expressed as

$$S_{a,i_d,u}(\omega_o) = \zeta S_{a,i_d}(\omega_o) = \frac{4kT\zeta\gamma g_{do}}{(1+\frac{\omega_T L_S}{R_s})^2},$$

where

$$\zeta = \frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q_L^2).$$

Because the noise contribution of the drain noise is from the first device M_1, which is part of $S_{a,i_d}(\omega_o)$. So it is appropriate to define the contribution of M_1 be

$$S_{a,i_d,M_1}(\omega_o) = \chi S_{a,i_d}(\omega_o) = \frac{4kT\chi\gamma g_{do}}{(1+\frac{\omega_T L_S}{R_s})^2}, \tag{2.40}$$

where

$$\chi = \kappa + \zeta = 1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1+Q_L^2). \tag{2.41}$$

Hence by adding the total output noise in Eqs.(2.38)-(2.40), dividing it by the total output noise due to the input in Eq.(2.38), the total noise factor can be derived as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma\chi g_{do} R_s \left(\frac{\omega_o}{\omega_T}\right)^2,$$

By replacing

$$g_{do}Q_L = \frac{g_m}{\alpha}\frac{1}{\omega_o R_s C_{gs}} = \frac{\omega_T}{\alpha\omega_o R_s},$$

the noise factor can be re-expressed as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma\chi}{\alpha Q_L}\left(\frac{\omega_o}{\omega_T}\right). \tag{2.42}$$

Finally Eq.(2.41) gives that χ is part of Q_L^2, and Eq.(2.42) shows that the noise factor is the part of χ over Q_L. Hence there is a particular Q_L to minimize F.

Chapter 3

Band Switchable UWB LNA Design

In this chapter, we will present the dual-band Switchable UWB LNA. First we discuss the consideration in the UWB switchable LNA design in Sec. 3.1. Second the important circuit for wideband input matching is presented in Sec. 3.2. In Sec. 3.3 we propose the new topology of the switch circuit. In addition, an output buffer for measurement is discussed in Sec. 3.4. In Sec. 3.5 all the circuits discussed in Secs. 3.2 - 3.4 are extended and used in the UWB switchable LNA. Secs. 3.6 and 3.7 discuss the layout consideration and the microphotograph of tape out chip. The measurement of this chip is shown in Sec. 3.8. We further improve the band switchable UWB LNA and show the result in Sec. 3.9. The layout and measurement of the improved band switchable UWB LNA are shown in Sec. 3.10 and Sec. 3.11, respectively.

3.1 Consideration for UWB Switchable LNA

The design considerations for UWB LNA are mainly in input return loss, power gain and noise figure (NF), linearity (P_{1dB}, IIP_3) and power consumption, but there are some trade-off between these important parameters. In order to get great input return loss, the wideband input matching is necessary. However in UWB systems, the wideband input impedance matching is a crucial design challenge. There were some excellent wideband input impedance matching solutions

proposed in [9] and [10]. The wideband input impedance matching in [9] and [10] are discussed in Sec. 3.2. However because the wideband input matching and the wideband noise matching [20] cannot achieve at the same time, there is a trade-off between the wideband input matching and the wideband noise matching [20]. The power gain is related to the power consumption and input return loss. Usually as the power gain is higher, the power consumption is larger, because the given energy is larger. Also the power gain is higher when the input return loss is lower, because lower input return loss means more signal power is transferred to the circuit. The linearity is most influenced by the output stage, because the signal power is the largest in the output stage. Hence the output buffer for measurement need to consider both the linearity and the output impedance matching. It is worth to emphasize that the power gain is also contributed from the output buffer, because the buffer increases the output current. Bandwidth is also an important parameter in the UWB switchable LNA. As discussed in Sec. 1.1, in order to avoid the 5-6GHz band in UWB, we should use the switch circuit. The classical switch circuit was proposed in [11]. In Sec. 3.3 we will discuss the switch circuit in [11]. Furthermore we will propose a new switch circuit used in LNA load in Sec. 3.3.

3.2 Wideband Input Matching

Some popular UWB input matching topology for LNA design are shown in Fig. 3.1 [9]and Fig. 3.4 [10]. In Fig. 3.1 the wideband input matching utilizes the transformer as the series feedback and the capacitive as the shunt feedback. And the feedback produces the real part of the input impedance for matching. The topology contributes two resonance frequencies at different frequency, respectively. In the high frequency, we can adjust the resonate frequency by properly choosing the drain inductor (L_d) and the load capacitance (C_L). It means the source of the two input transistors is connected to the ac ground, so the small signal circuit is shown in Fig. 3.2. We can derive the input impedance as

$$Z_{in,H} = j\omega L_g + \frac{1}{j\omega(C_{gs}+C_{gd})} + \frac{M \cdot g_m}{C_{gs}+C_{gd}},$$

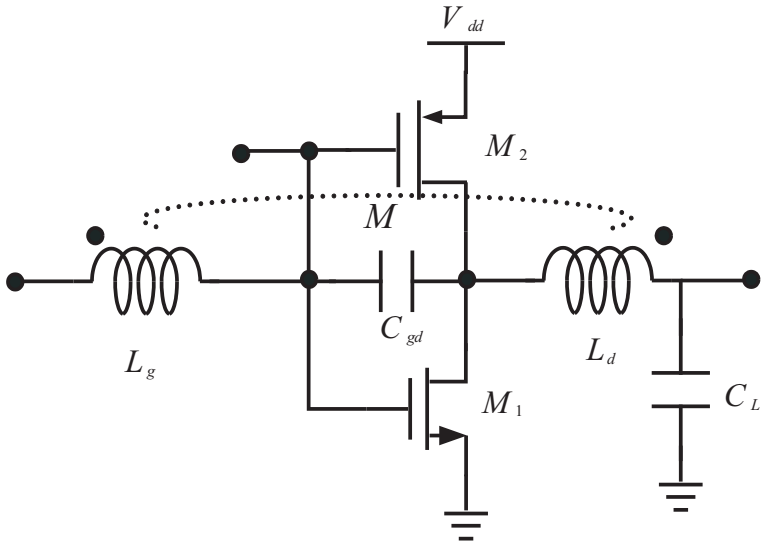


Figure 3.1: The dual feedback wideband matching.

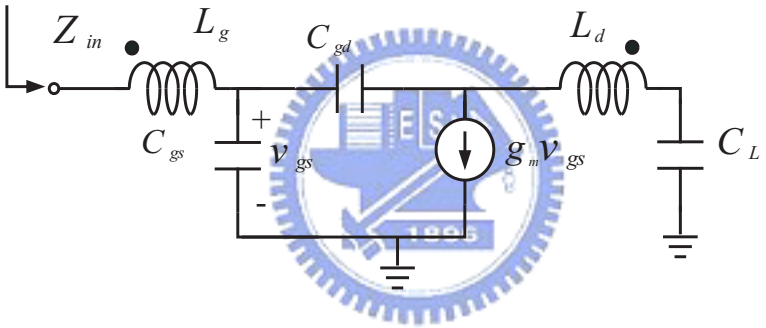


Figure 3.2: The small signal circuit of dual feedback circuit at high frequency.

where M is mutual inductance between the windings and the real part is contributed by the transformer and the resonance frequency expressed as

$$f_H = \left(2\pi\sqrt{L_d C_L}\right)^{-1} = \left(2\pi\sqrt{L_g(C_{gs}+C_{gd})}\right)^{-1}.$$

The real part is designed to be 50 ohm and the imaginary part is designed to be 0 ohm. In low frequency the small signal circuit is shown in Fig. 3.3, the input impedance can be expressed as

$$Z_{in,L} = j\omega L_g + \frac{1}{j\omega(C_{gs}+C_{gd}) + \frac{1}{R_{eq}+1/j\omega C_{eq}}}, \tag{3.1}$$

where $R_{eq} = (C_{gd}+C_L)/(g_m C_{gd})$ and $j\omega C_{eq} = j\omega C_{gd} g_m r_{ds}$, and the real part of input impedance is the capacitive feedback. From Eg.(3.1), in low frequency the

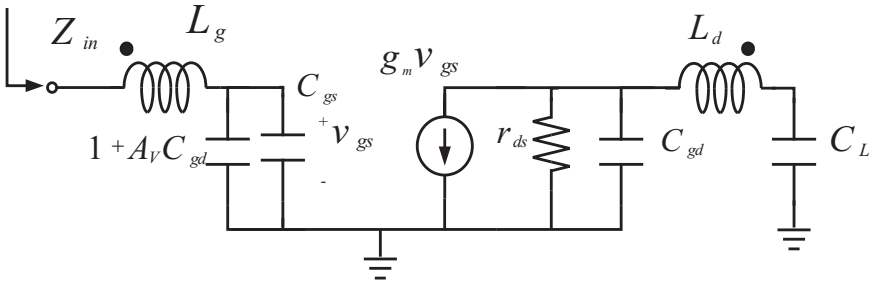


Figure 3.3: The small signal circuit of dual feedback circuit at low frequency.

influence of the load impedance capacitive and the capacitive feedback dominate the input impedance. Due to the high voltage gain, the Miller capacitance C_{eq} that dominates the imaginary part will appear. Hence the input circuit uses L_g to cancel the imaginary part. In addition the real part is designed to be 50 ohm and the imaginary part is designed to be 0 ohm in low frequency. Its resonance frequency is $f_L = \left(2\pi\sqrt{L_g C_{eq}}\right)^{-1}$. The topology gives the broadband input matching and good noise matching [20]. However we need to have the accurate transformer parameters. But the standard devices of TSMC 0.18μm does not include the transformer. Hence it is difficult to obtain M.

Another commonly used topology in UWB LNA design is the Chebyshev filter as shown in Fig. 3.4 [10]. As discussed in Sec. 2.4, Z_{in} is

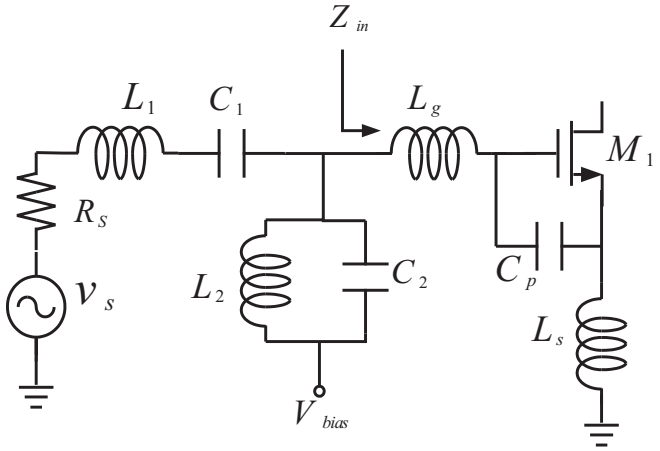


Figure 3.4: The Chebyshev filter for wideband matching.

$$s(L_g + L_s) + \frac{1}{s(C_{gs} + C_p)} + \omega_T L_s, \tag{3.2}$$

where $\omega_T = g_m/(C_{gs} + C_p)$. We can redraw Fig. 3.4 from Eq.(3.2) by replacing the transistor (M_1) with the resistor and the parasitic capacitors. Then the new graph is shown in Fig. 3.5. In general the real part of the input impedance

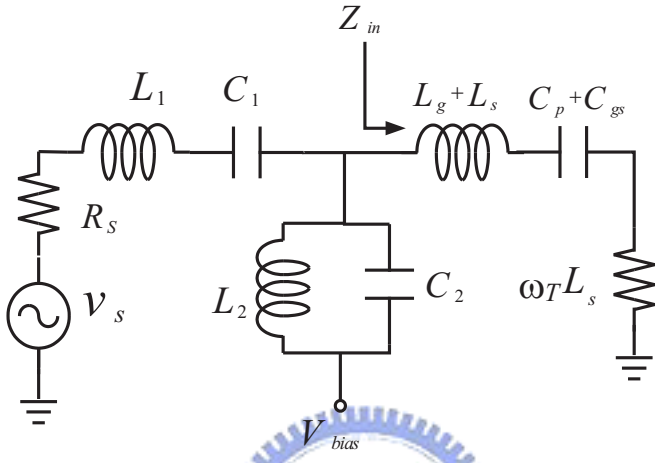


Figure 3.5: The Chebyshev filter for passive device.

is set to be 50 ohm, and other inductances and capacitors contribute different resonance frequency. Although the topology also achieves the input matching and noise matching [20], it needs four inductances. The inductance cost a lot of area and cost. In CMOS IC design, the cost is an important issue in business. Hence in this thesis we do not choose this solution for wideband input matching.

In this thesis we use the topology that contains a conventional source-degeneration input matching, an inductor shunted in input RF path and a capacitor seriesed in input RF path as shown in Fig. 3.6[9], because it does not need exact transformer parameters and the number of inductance is one fewer than the Chebyshev filter. As discussed in Sec. 2.4 from Eq.(2.36) the input impedance can be expressed as

$$s(L_g + L_s) + \frac{1}{s(C_{gs} + C_c)} + \omega_T L_s,$$

where $\omega_T = g_m/(C_{gs} + C_c)$. The impedance consists of one resistor, one inductance, and one capacitor. Hence we can redraw the circuit of input matching. The input matching circuit is shown as Fig. 3.7. In high frequency the induc-

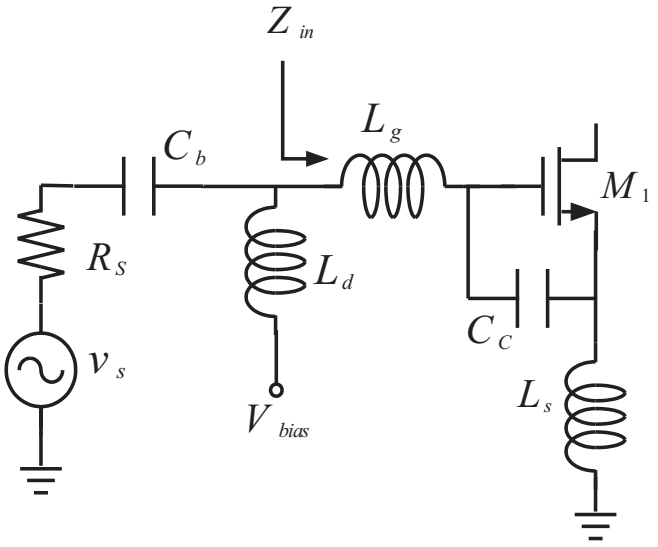


Figure 3.6: The input matching for UWB LNA.

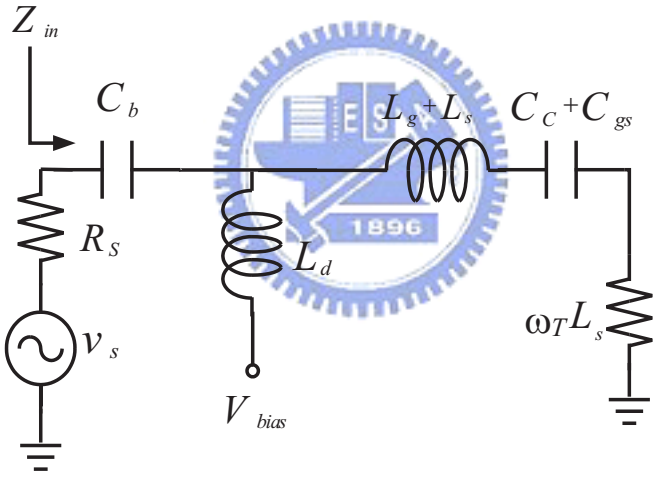


Figure 3.7: The input matching of passive device for UWB LNA.

tor shunted in input RF path, i.e. L_d, is approximately as open, because the impedance of inductance is proportional to frequency. Hence the circuit acts like an inductive source degeneration circuit. Note that the equivalent capacitance is the series connection of $(C_{gs} + C_c)$ and C_b. Hence the input impedance is expressed as

$$s(L_g + L_s) + \frac{1}{s((C_{gs}C_b + C_cC_b)/(C_{gs} + C_c + C_b))} + \omega_T L_s,$$

where $\omega_T L_s$ is set to be 50 ohm. The resonance frequency for high frequency is

$$\omega = \sqrt{\frac{1}{(L_g + L_s)((C_{gs}C_b + C_cC_b)/(C_{gs} + C_c + C_b))}}. \tag{3.3}$$

For low frequency the input impedance can be expressed as

$$\frac{1}{sC_b} + \left[sL_d // \left(s(L_g + L_s) + \frac{1}{s(C_{gs} + C_c)} + \frac{g_m L_s}{C_{gs}} \right) \right]. \tag{3.4}$$

Define $L = L_g + L_s$, $C = C_{gs} + C_c$ and $R = g_m L_s / C_{gs}$, Eq.(3.4) can be rewritten as

$$\frac{1}{sC_b} + \left[sL_d // \left(sL + \frac{1}{sC} + R \right) \right]. \tag{3.5}$$

Eq.(3.5) can be rearranged as

$$\begin{aligned}
&\frac{1}{sC_b} + \left[sL_d // \left(sL + \frac{1}{sC} + R \right) \right] \\
&= \frac{1}{sC_b} + \left(\frac{1}{1/sL_d + 1/(sL + 1/sC + R)} \right) \\
&= \frac{1}{sC_b} + \left(\frac{sL_d(sL + 1/sC + R)}{sL + 1/sC + R + sL_d} \right) \\
&= \frac{1}{sC_b} + \left(\frac{sL_d(s^2LC + sCR + 1)}{s^2LC + s^2L_dC + sCR + 1} \right) \\
&= \frac{s^2LC + s^2L_dC + sCR + 1 + s^2L_dC_b(s^2LC + sCR + 1)}{sC_b(s^2LC + s^2L_dC + sCR + 1)}.
\end{aligned} \tag{3.6}$$

Then we design the impedance to be 50 ohm. Thus design Eq.(3.6) is 50, .i.e. letting

$$\frac{s^2LC + s^2L_dC + sCR + 1 + s^2L_dC_b(s^2LC + sCR + 1)}{sC_b(s^2LC + s^2L_dC + sCR + 1)} = 50. \tag{3.7}$$

Replacing s by $j\omega$, Eq.(3.7) can be rearranged by

$$\begin{aligned}
&\frac{-\omega^2LC - \omega^2L_dC + j\omega CR + 1 - \omega^2L_dC_b(-\omega^2LC + j\omega CR + 1)}{j\omega C_b(-\omega^2LC - \omega^2L_dC + j\omega CR + 1)} = 50 \\
\Rightarrow &\frac{\omega^2(-LC - L_dC) + j\omega CR + 1 + \omega^4(L_dC_bLC) - j\omega^3L_dC_bCR - \omega^2L_dC_b}{-j\omega^3LCC_b - j\omega^3L_dCC_b - \omega^2CRC_b + j\omega C_b} = 50 \\
\Rightarrow &\frac{\omega^4(LCL_dC_b) - j\omega^3L_dC_bCR + \omega^2(-LC - L_dC - L_dC_b) + j\omega CR + 1}{-j\omega^3(LCC_b + L_dCC_b) - \omega^2CRC_b + j\omega C_b} = 50
\end{aligned}$$

Hence we can express the equation as

$$\begin{aligned}&\omega^4(LCL_dC_b) - j\omega^3 L_dC_bCR + \omega^2(-LC - L_dC - L_dC_b) + j\omega CR + 1\\ &= -j\omega^3 50(LCC_b + L_dCC_b) - \omega^2 50CRC_b + j\omega 50C_b. \end{aligned} \tag{3.8}$$

From Eq.(3.8) the real part of Eq.(3.8) can be rearranged as

$$\omega^4(LCL_dC_b) + \omega^2(-LC - L_dC - L_dC_b) + 1 + \omega^2 50CRC_b = 0. \tag{3.9}$$

Define X to be ω^2. Eq.(3.9) is given by

$$X^2(LCL_dC_b) - X(LC + L_dC + L_dC_b - 50CRC_b) + 1 = 0.$$

Hence X is

$$\frac{LC + L_dC + L_dC_b - 50CRC_b \pm \sqrt{(LC + L_dC + L_dC_b - 50CRC_b)^2 - 4LCL_dC_b}}{2LCL_dC_b}.$$

Because we want to get 50 ohm at low frequency, we choose smaller X as

$$\frac{LC + L_dC + L_dC_b - 50CRC_b - \sqrt{(LC + L_dC + L_dC_b - 50CRC_b)^2 - 4LCL_dC_b}}{2LCL_dC_b}.$$

Hence the resonance frequency for low frequency is given by

$$\sqrt{\frac{LC + L_dC + L_dC_b - 50CRC_b - \sqrt{(LC + L_dC + L_dC_b - 50CRC_b)^2 - 4LCL_dC_b}}{2LCL_dC_b}}. \tag{3.10}$$

In a word, according to Eq.(3.3) we first design the input impedance in high frequency by adjusting L_g, L_s, C_C, C_b and M_1 in the inductive source degeneration circuit. Then according to Eq.(3.10) we design the input impedance in low frequency by adjusting L_d. Finally the two band results in a wideband input matching. The procedure to determine the parameters is follows:

1. At high frequency we first design the size M_1 to get $\omega_T L_s$=50. Then design L_g, C_C, C_b to let the imaginary part of input impedance to be zero from Eq.(3.3).

2. After designing high frequency, according to Eq.(3.10) we design L_d to get the input matching at low frequency.

When we use the ideal devices to implement the input matching network the method is exact, because it uses basic circuit rule. We can easy to get two frequencies that matching to be 50 ohm. For no ideal devices such as TSMC 0.18μm model, this is not absolutely exact, because there are many no ideal conditions such as parasitic capacitance and parasitic resistance. Hence we cannot easy to get the input matching, but we still can use the method to simulate circuit. After some tuning, the input matching can also be achieved by the method.

3.3 Switch Circuit Topology

3.3.1 LC-tank

The proposed LNA belongs to LC-tank amplifiers. The classical LC-tank amplifier can be found in [8] shown in Fig. 3.8. Let the loading impedance of the LC-tank be Z_L. The voltage gain of this classical LC-tank amplifier is $g_m Z_L$. Hence it can produce different resonance frequency and different voltage gain by changing the corresponding capacitance, which is contained in Z_L. The impedance of

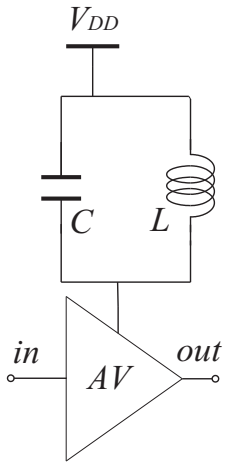


Figure 3.8: The classical LC-tank amplifier.

loading is expressed as

$$Z_L = \frac{1}{sC + 1/(sL)} = \frac{sL}{1 + s^2CL}, \tag{3.11}$$

where L is the inductance of loading and C is the capacitance of loading. Replacing s by $j\omega$ Eq.(3.11) can be rewritten as

$$Z_L = \frac{j\omega L}{1 - \omega^2 CL}. \tag{3.12}$$

From Eq.(3.12) the maximum impedance at the frequency given by

$$\omega = \frac{1}{\sqrt{LC}}.$$

Hence we can produce different resonance frequency and different voltage gain by changing the capacitance, which is contained in Z_L.

3.3.2 Switch Load

In recent years, various types of switches for switching narrow band LNA were proposed [11][12]. The one using PMOS as a switch in the load of LNA is as shown in Fig. 3.9(a). However the mobility of PMOS is much lower than NMOS. Because the turn on resistance of MOS is expressed as

$$r_{on} = \frac{L}{\mu_n W(V_{GS} - V_T - V_{DS})}. \tag{3.13}$$

Thus, its turn on resistance is large, which leads to a small quality factor and a low gain. The other method to change the passive device value is implementing switched inductor as shown in Fig. 3.9(b). In addition, the above two schemes are proposed for narrow band systems. But this topology leads to lager area because it needs two inductors. To overcome the above drawback, the proposed switched capacitor amplifier place the PMOS in Fig. 3.9(a) with a NMOS and adds a resistor R_1 as shown in Fig. 3.10(a), which consists of switched capacitors C_1, C_2, an inductor L_1 in parallel and a resistor R_1. Because NMOS has lower r_{on} than PMOS, NMOS has larger gain than PMOS when switch is on. Hence we use NMOS as switch. The large resistor (R_1) can reduce the parasitic capacitance.

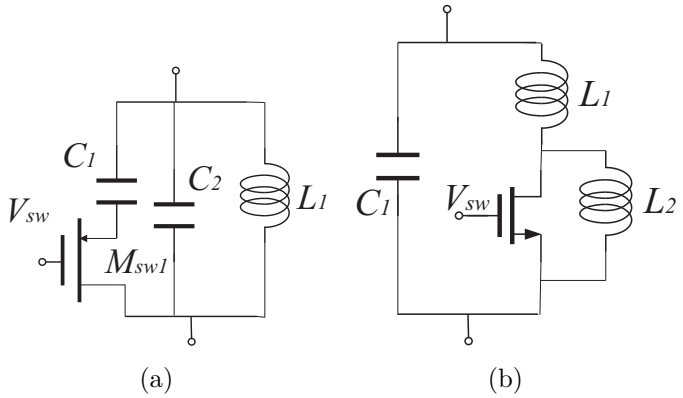


Figure 3.9: The load of (a) switched capacitor using PMOS [11] (b) switched inductor [12].

That is if we do not have R_1, the equivalent capacitance, C_{eq}, is that C_1 series C_{gs} when the switch is off. If we have R_1, C_{eq} is that C_{gs} and C_{gd} series C_1 and C_2 when the switch is off. Hence the parasitic capacitance is reduced from C_{gs} to C_{gs} and C_{gd} series. Due to reduction of the parasitic capacitance, the size of the switch can be larger, which leads to a lower r_{on}. Thus the gain is larger when switch is on. From Fig. 3.10(b) when M_{sw1} is turned off, the equivalent

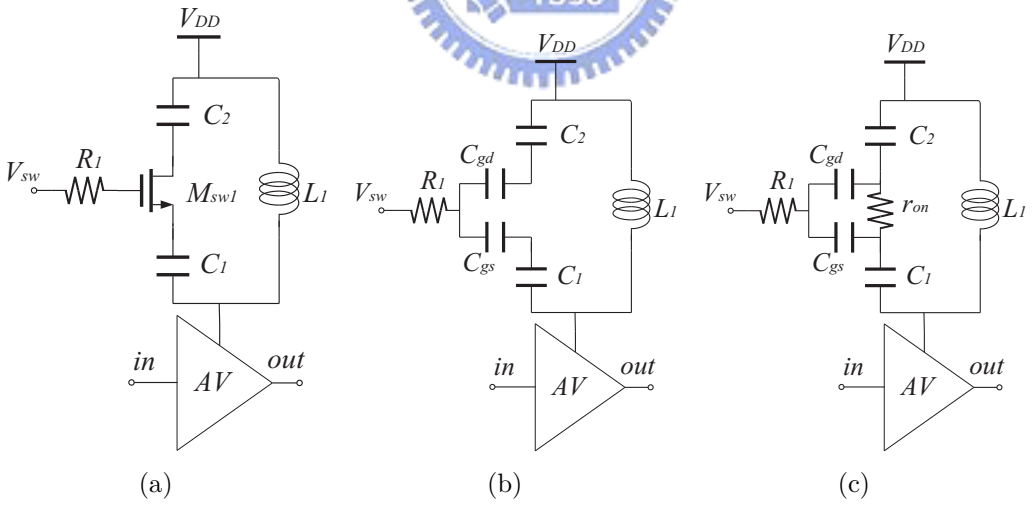


Figure 3.10: The proposed switched capacitor amplifier: (a) The proposed circuit. (b) Condition for M_{sw1} off. (c) Condition for M_{sw1} on.

capacitance is the parasitic capacitor of M_{sw1}, i.e. C_{gs} and C_{gd} series C_1 and C_2, because of R_1. By designing that $C_1, C_2 \gg C_{gs}, C_{gd}$, the equivalent capacitance,

C_{eq}, is that C_{gs} series C_{gd} given by

$$C_{eq} = \frac{C_{gs}C_{gd}}{C_{gs} + C_{gd}}.$$

On the contrary, from Fig. 3.10(c) when M_{sw1} is turned on, the equivalent capacitance is that r_{on} series C_1 and C_2. From Eq.(3.13) r_{on} is low resistance, because we use NMOS and R_1. Because r_{on} is a low resistance, r_{on} can be neglected. Hence the equivalent capacitance is

$$C_{eq} = \frac{C_1C_2}{C_1 + C_2}.$$

That is

$$C_{eq} = \begin{cases} \frac{C_{gs}C_{gd}}{C_{gs} + C_{gd}}, & M_{sw1} \text{ is off.} \\ \frac{C_1C_2}{C_1 + C_2}, & M_{sw1} \text{ is on.} \end{cases}$$

Thus the circuit can satisfy the resonance of the load at two different frequencies by turning M_{sw1} on or off. The resonant frequency is

$$\omega = \frac{1}{\sqrt{L_1C_{eq}}}.$$

The size of M_{sw1} trades off between C_{gs}, C_{gd} and r_{on}. In UWB switchable LNA design the critical design challenge is the range switchable of band, because it demands wider frequency. In our design the widest range is 5.6GHz (10.6GHz-5GHz), because we use cascade topology, which generates two resonate frequencies. This will be discussed in Sec. 3.5. Hence we simulate the three types of switch band circuit for 10.6GHz and 5GHz. The three switch band circuits are PMOS-based switch, NMOS-based switch and NMOS-based switch with large resistor as shown in Fig. 3.11. The simulation result is shown in Fig. 3.12. From Fig. 3.12 we can find the one who has the largest impedance at the low band is the NMOS-based switch with large resistor. This is because its r_{on} is smallest, and the Q is largest at the low band. The low r_{on} is due to high mobility of NMOS and the size of switch. The PMOS-based switch is smallest at the low band, due to its low mobility. However at high band the largest impedance is

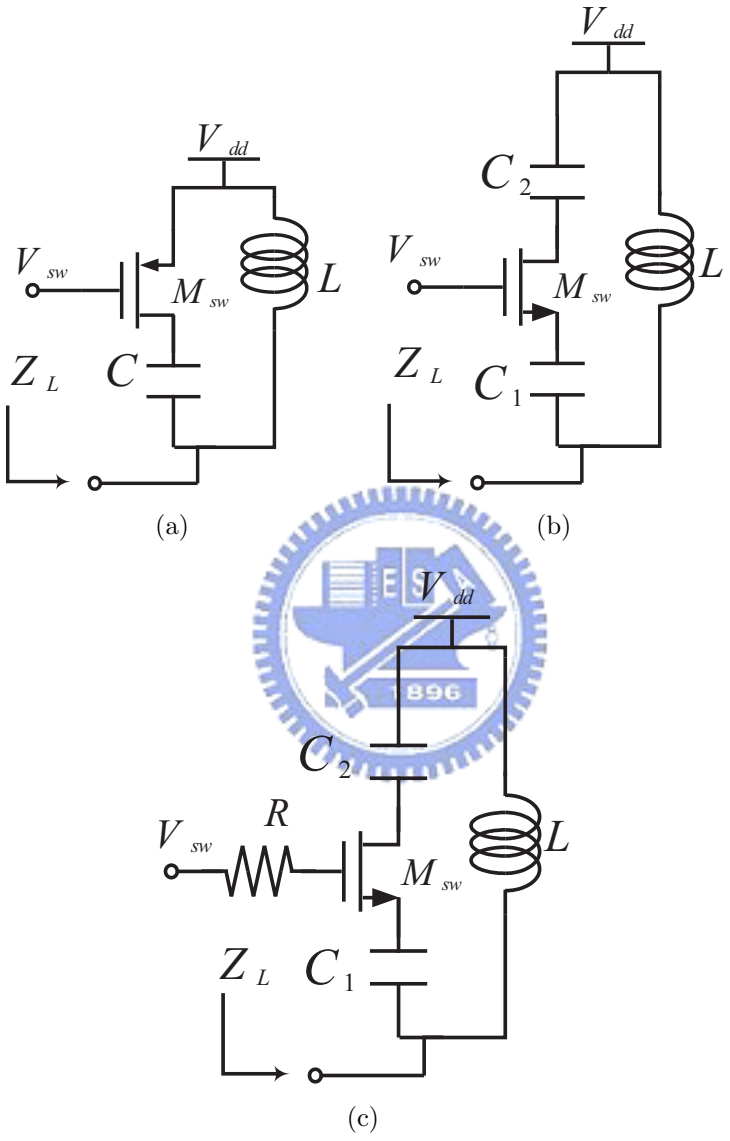
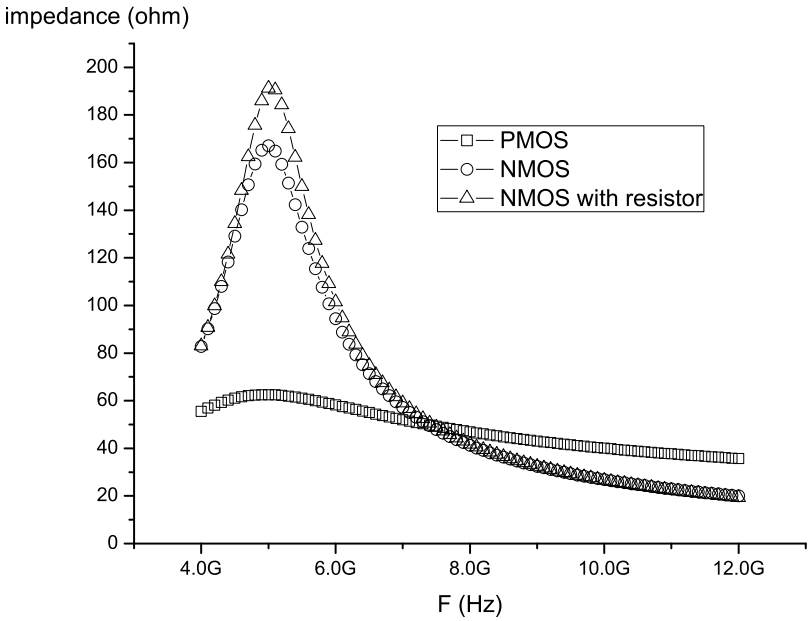
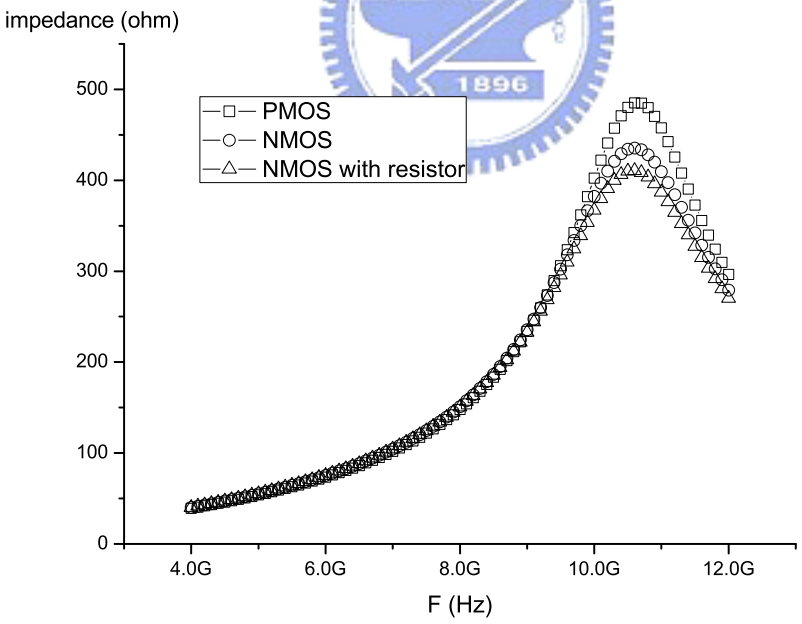


Figure 3.11: The three types of switch band circuit: (a) PMOS-based switch. (b) NMOS-based switch. (c) NMOS-based switch with large resistor.



(a)



(b)

Figure 3.12: The impedance of three types switch band circuit: (a) at low frequency, (b) at high frequency.

PMOS-based switch. This is because its mobility is smallest and it looks like as ideal open switch. This implies that at the low band the gain of NMOS-based switch with large resistor is the largest and that of the PMOS-based is the smallest. At the high band the gain of NMOS-based switch with large resistor is the smallest and that of the PMOS-based is the largest. From Fig. 3.12 we can find the impedance of every switch is larger at high band than at low band. Hence the gain of low band is lower than high band. Thus in order to fit specification, the gain of low band is a more important issue. Hence we choose the NMOS-based switch with large resistor as our switch band circuit to increase the gain of low band .

3.4 Output Buffer

In the section we discuss how to get the output impedance matching for the UWB Switchable LNA. In the LNA we use the output buffer for output impedance matching as shown in Fig. 3.13, because output buffer has the designable output impedance. This characteristic helps the output impedance to match 50 ohm. Fig. 3.13 show a typical output buffer. We replace the current source (I_b) with a

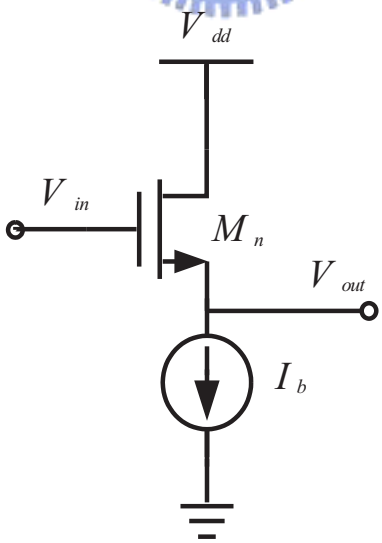


Figure 3.13: The output buffer for measurement.

NMOS, because the resistance of current source is infinite and the resistance of NMOS that looks into the drain terminal is large. The small signal model is shown in Fig. 3.14, where V_o and I_o is the test source to derive the output impedance, r_{ob} is the output resistance of current source NMOS, r_o is the output resistance of M_n, C_{gs} is the parasitic capacitance of M_n, and g_m is the transconductance of M_n. From Kirchoff's current law (KCL) we can express KCL as

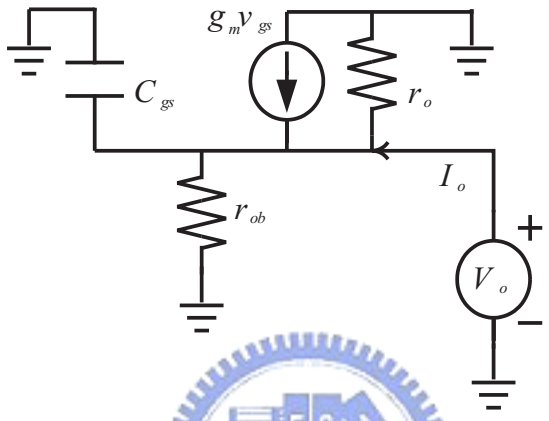


Figure 3.14: The small signal circuit of output buffer.

$$\frac{V_o}{1/(sC_{gs})} + \frac{V_o}{r_o} + \frac{V_o}{r_{ob}} = -g_m V_o + I_o,$$
$$V_o \left(\frac{1}{1/(sC_{gs})} + \frac{1}{r_o} + \frac{1}{r_{ob}} + \frac{1}{1/g_m} \right) = I_o$$

Hence the output impedance (Z_{out}) is expressed as

$$Z_{out} = \frac{V_o}{I_o} = \frac{1}{sC_{gs}} \| r_o \| r_{ob} \| \frac{1}{g_m}.$$

Because r_o and $r_{ob} \gg 1/g_m$, r_o and r_{ob} can be neglected. Hence Z_{out} can be re-expressed as

$$Z_{out} = \frac{1}{sC_{gs}} \parallel \frac{1}{g_m}.$$

In addition there is a DC-blocking capacitor (C_b) series at the output terminal in order to avoid DC current, thus the actual Z_{out} is expressed as

$$Z_{out} = \left(\frac{1}{sC_{gs}} \parallel \frac{1}{g_m} \right) + \frac{1}{sC_b}. \tag{3.14}$$

Hence we design $1/gm$ is equal to be 50 ohm and the imaginary part (C_b, C_{gs}) approach zero at the band that we want. And the voltage gain of the output buffer can be derived. From Fig. 3.14 because r_{ob} is too large, r_{ob} can be neglected. Hence the Fig. 3.14 can be redrew as show in Fig. 3.15. From Fig. 3.15

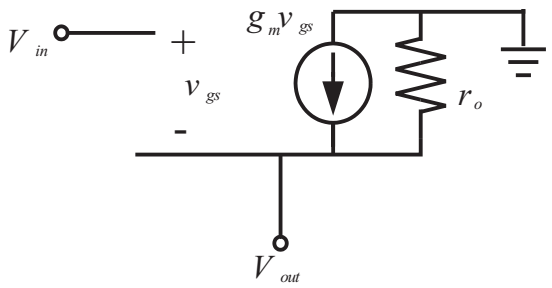


Figure 3.15: The small signal circuit of output buffer for deriving gain.

$$\frac{V_{out}}{r_o} = g_m v_{gs} \text{ and } v_{gs} = V_{in} - V_{out}$$

Hence the voltage gain of output buffer is expressed as

$$AV = \frac{V_{out}}{V_{in}} = \frac{g_m r_o}{1 + g_m r_o} \approx 1$$

Finally the voltage gain of output is equal to be 1 when $g_m r_o \gg 1$.

3.5 The UWB Switchable LNA

3.5.1 Cascoded Amplifier with LC-Tank Load

In this thesis, no matter the switch is on or off, the loading of the LNA acts like an LC-tank. One of the most popular technologies of the LNA is the cascode amplifier with LC-tank as shown in Fig. 3.5.1, because it reduces the Miller effect on input transistor M_1 to attain high-frequency performance. The loading with LC-tank is mostly applied to narrow-band systems because of its prominent frequency-selective characteristics. Its voltage gain A is given by

$$A(s) = -g_{m1} \frac{s g_{m2} r_{o1} r_{o2} L}{s^2 g_{m2} r_{o1} r_{o2} LC + sL + g_{m2} r_{o1} r_{o2}},$$

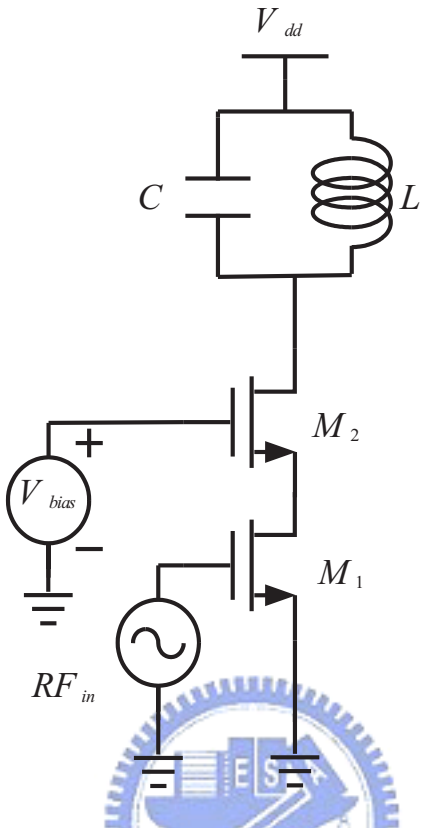


Figure 3.16: Cascode amplifier.

where g_{m1} is the transconductance of M_1, r_{o1}, r_{o2} are the output impedance of the transistors (M_1 and M_2), and the inductor L, capacitor C are the loading of the LC-tank.

3.5.2 Cascade Amplifier with LC-Tank Load

We use cascade amplifier to generate two frequency bands. In the cascade circuit as shown in Fig.3.17 the first stage amplifier with LC-tank resonated loading contributes the power gain of low frequency, and the second stage amplifier contributes the power gain of the high frequency. Therefore, the wide bandwidth and high power gain can be achieved by two stages LC-tank amplifiers.

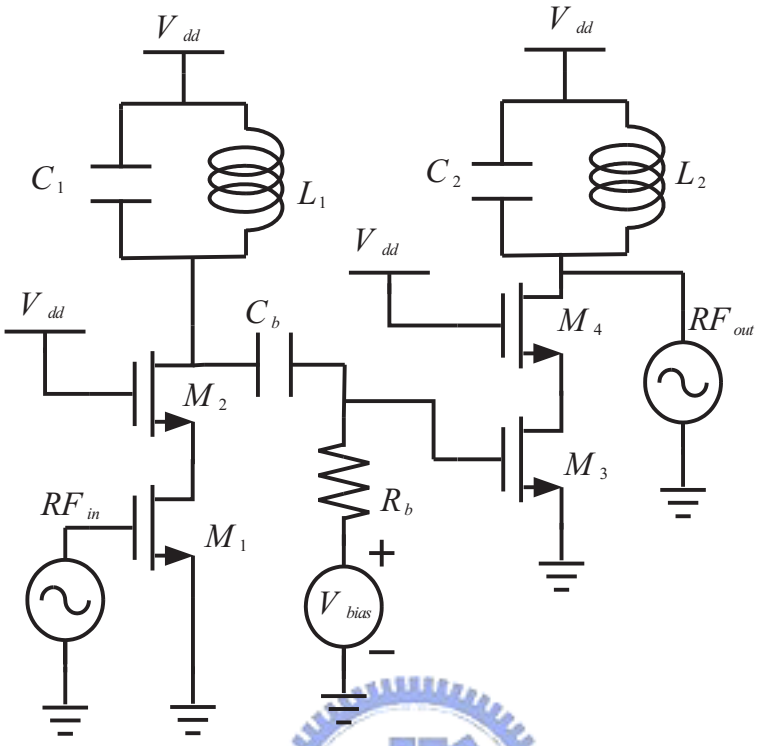


Figure 3.17: Cascade amplifier.

3.5.3 Proposed Dual-band Low Noise Amplifier

The proposed dual-band LNA is shown in Fig.3.18 which consists of the input matching network that is implemented by the Butterworth Filter [9] (consisting of L_d, L_g, L_s, C_c and C_{gs1}) ; the two stages of cascode amplifiers (containing M_1, M_2, M_3, and M_4) ; the switch capacitance loading of the amplifiers (consisting of L_1, L_2, M_{sw1}, C_3, C_4 and M_{sw2}) ; the output buffer (consisting of M_6 and M_7); the three DC blocking capacitors (consisting of C_b); RF chocks (consisting of R_1, R_2 and R_b). V_{sw1} and V_{sw2} are the control voltage source of the switch capacitance loading. When V_{sw1} and V_{sw2} are both 1.8, it is in the low frequency mode. On the contrary when both the voltages are 0, it is in the high frequency mode. Given an operation frequency, we can achieve this frequency by adjusting the size M_{sw1} and M_{sw2} when they are off. On the other hand, when M_{sw1} and M_{sw2} are on, the size of M_{sw1} and M_{sw2} will affect the resistance of the switch capacitance loading. The first stage cascode amplifier contributes the lower frequency power

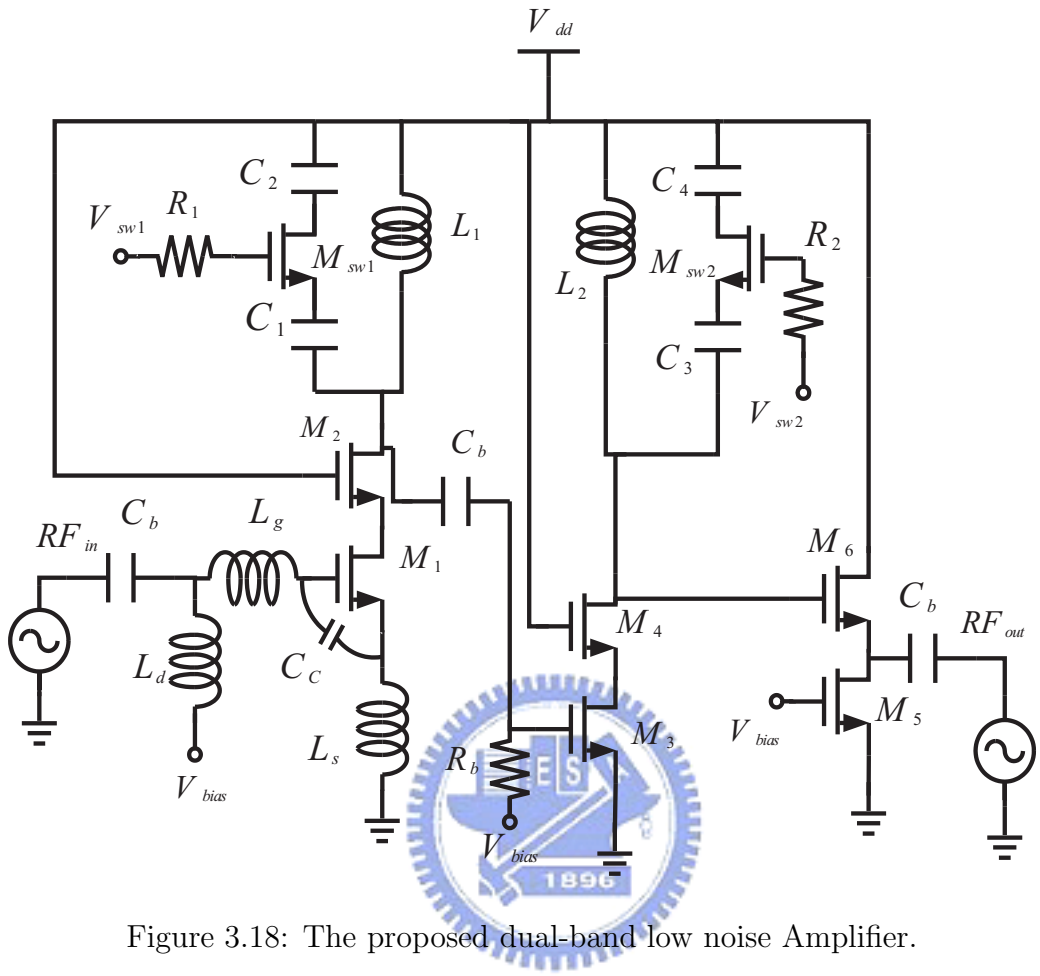


Figure 3.18: The proposed dual-band low noise Amplifier.

gain, where the lower frequency band is 3.1GHz to 6GHz. The second cascode stage amplifier contributes the higher frequency power gain, where the higher frequency band is 5GHz to 10.6GHz. The size of M_1 trades off between the input matching and the noise figure of the LNA.

3.6 Consideration of Layout

The layout of band switchable UWB LNA is shown in Fig. 3.19. The band switchable UWB LNA chip is fabricated in CMOS process with TSMC 0.18-μm. It uses a single poly layer and six layers of metal (1P6M). The capacitors are metal-insulator-metal (MIM) capacitors, the inductances are thick-metal inductor and the resistors are high sheet HRI P-poly resistors without silicide,

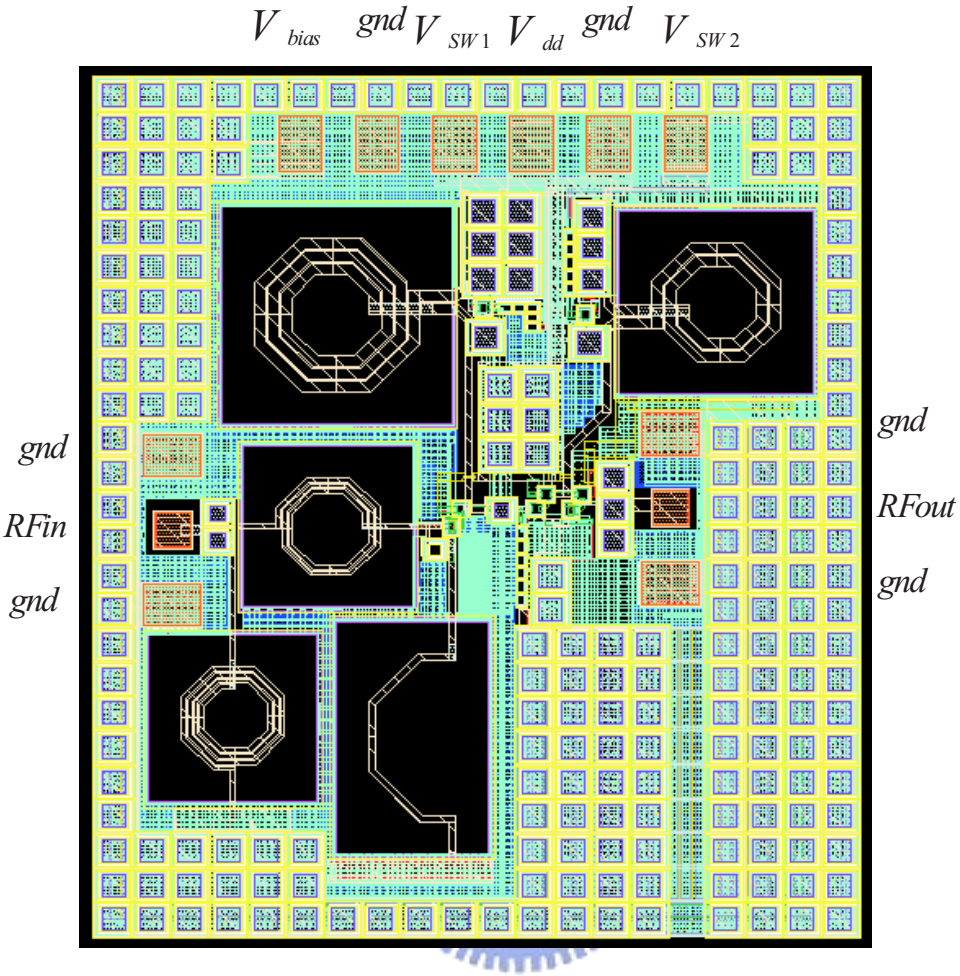


Figure 3.19: The layout of band switchable UWB LNA.

respectively. All MOS devices are the NMOS with triple-well technique. The inductances are at a reasonable distance from the other devices of circuit that prevents the interference and mutual inductance with circuit working. The pads of RFin and RFout are located in opposite direction, because it increases the isolation between the input and output. All DC pads are located in the top of the layout, because the bottom of the layout is ready for the pads that used by mixer. Because all the body terminal of devices is connected to ground, we need a wide ground plane. We use the low resistive metal-1 material to be the wide ground plane, because it is low loss. In addition it can also minimize the noise effect of substrate on the system.

The signal direction is uni-direction, because we do not want the signal returns close to its input. If the signal returns too close to its input the feedback will interfere with the circuit. The RFin and RFout ports used the standard Ground-Signal-Ground (GSG) configuration for measurement, and the DC port used standard Power-Ground-Power-Power-Ground-Power (PGPPGP) configuration[21]. Two of the DC ports are used to be the switch control ports as shown in Fig. 3.19. The other two ports are DC biasing voltage and power supply, respectively. Signal paths are as short as possible, because we want to decrease the transmission line effect. The total chip area is 1.17mm × 1mm. The size relates to the number of inductance. The empty area is filled by by-pass capacitor to stabilize the biasing voltage.

3.7 Microphotograph of Chip

The microphotograph of band switchable UWB LNA is shown in Fig. 3.20 that is fabricated in the TSMC 0.18μm CMOS process technology. The die area is 1.17mm × 1mm with the bonding pads.

3.8 Measurement Result of Band Switchable UWB LNA

The measurement results of the proposed band switchable UWB LNA is using the 4-Port Network Analyzer (Agilent 5230A), Noise Figure Analyzer (Agilent N8975A) and Signal Generator (Agilent E8247C) that supported by National Chip Implementation Center (CIC) [21]. The simulation results are using Agilent Advance Design System (ADS) 2006A simulator. At low band mode simulation results and measurement results are itemized as follows:

- S-parameters
  Fig. 3.21: S_{11}

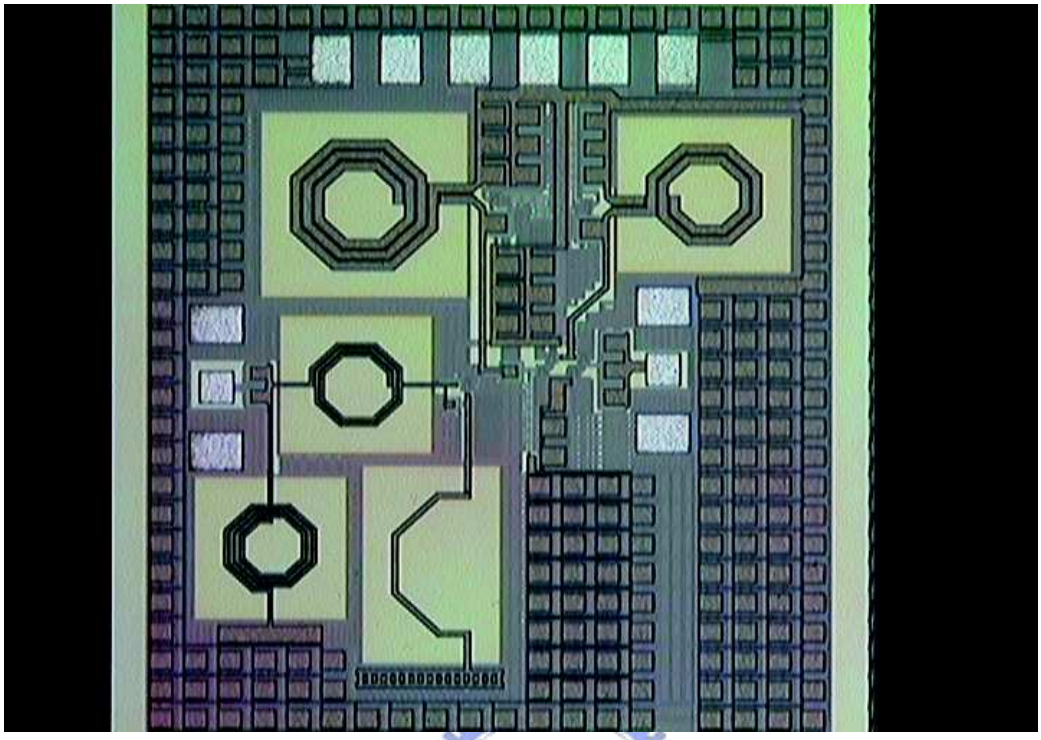


Figure 3.20: The chip photo of band switchable UWB LNA.

Fig. 3.22: S_{21}

Fig. 3.23: S_{22}

- Noise Figure

  Fig. 3.24: NF

- P_{1dB}

  Fig. 3.25: P_{1dB} of measurement

  Fig. 3.26: P_{1dB} of simulation

- IIP_3

  Fig. 3.27: IIP_3 of measurement

  Fig. 3.28: IIP_3 of simulation

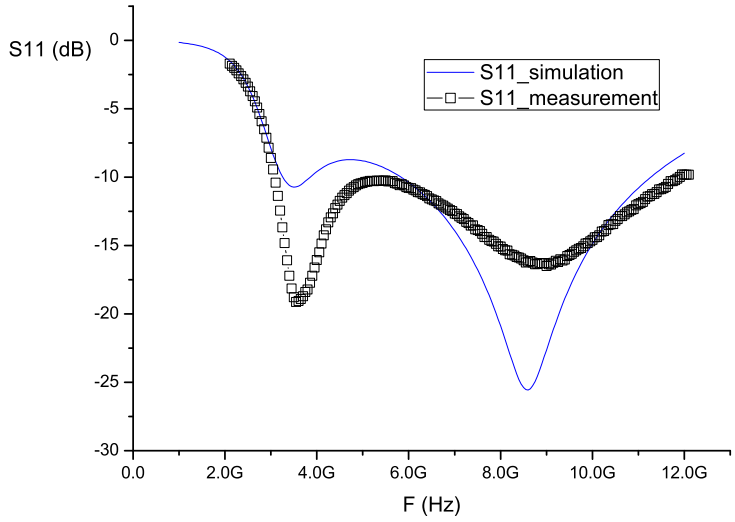


Figure 3.21: The S_{11} parameter of band switchable UWB LNA at low frequency.

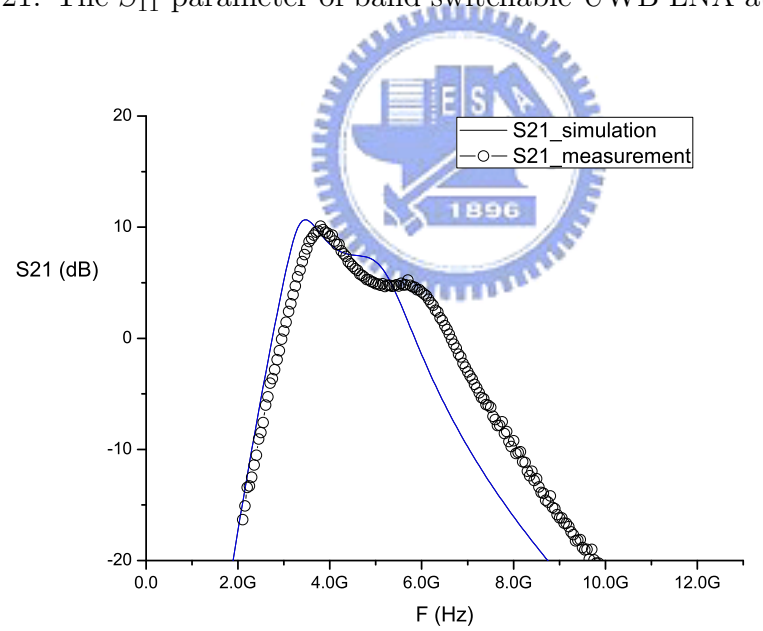


Figure 3.22: The S_{21} parameter of band switchable UWB LNA at low frequency.

At high band mode simulation results and measurement results are itemized as follows:

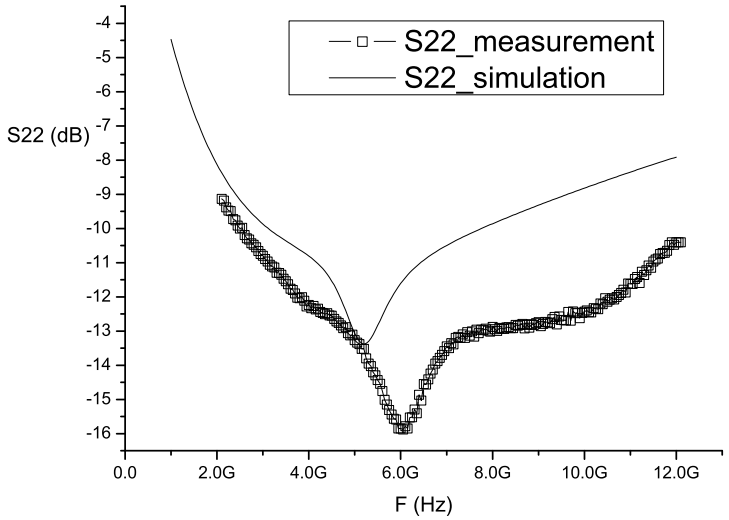


Figure 3.23: The S_{22} parameter of band switchable UWB LNA at low frequency.

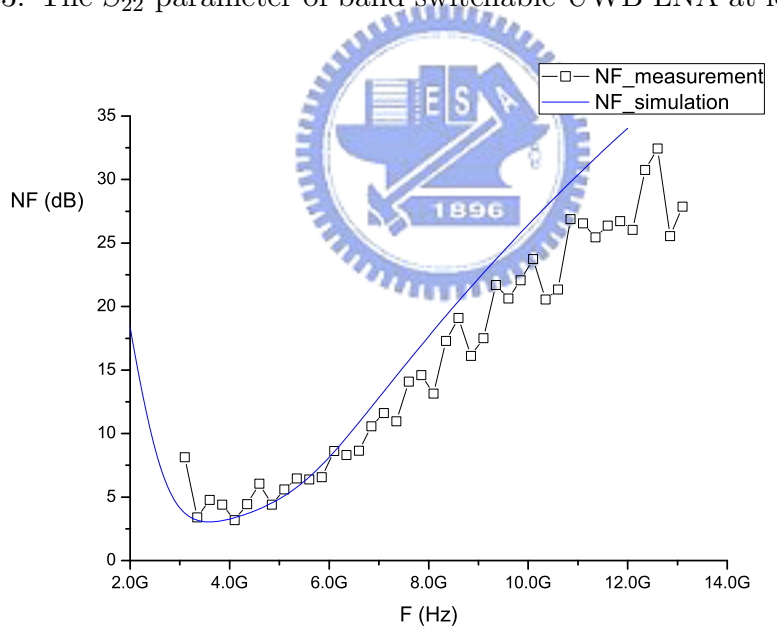


Figure 3.24: The NF parameter of band switchable UWB LNA at low frequency.

- S-parameters

  Fig. 3.29: S_{11}

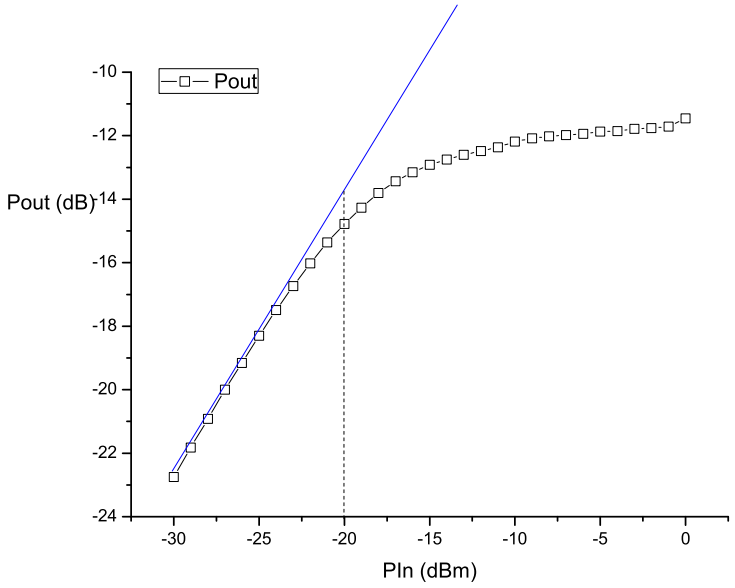


Figure 3.25: The P_{1dB} parameter of band switchable UWB LNA at low frequency for measurement.

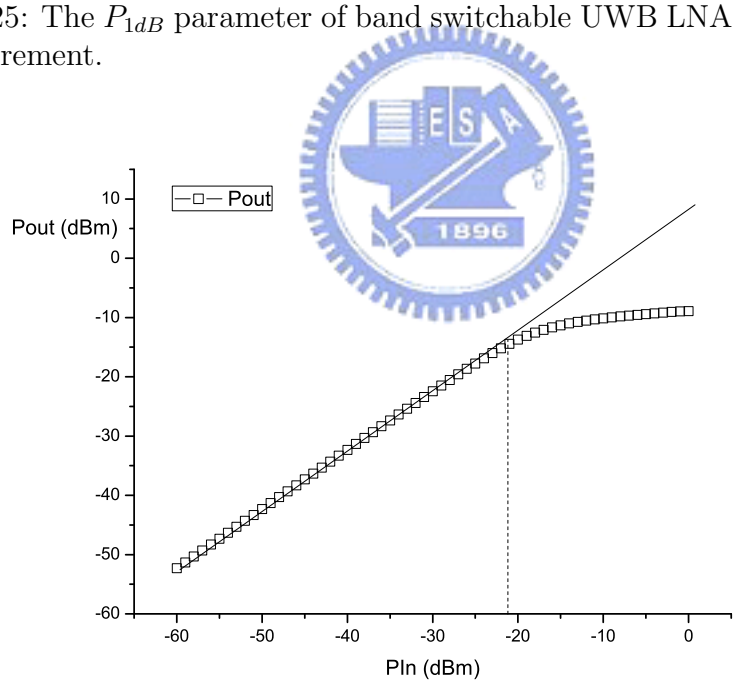


Figure 3.26: The P_{1dB} parameter of band switchable UWB LNA at low frequency for simulation.

Fig. 3.30: S_{21}

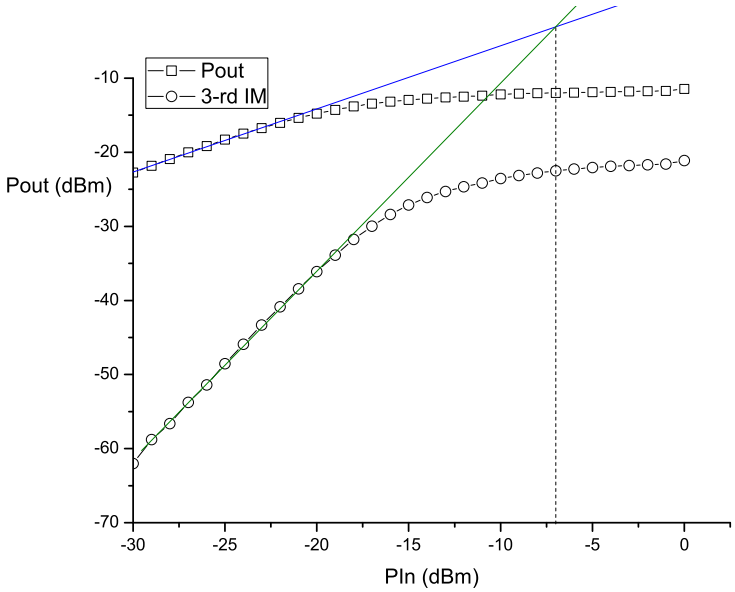


Figure 3.27: The IIP_3 parameter of band switchable UWB LNA at low frequency for measurement.

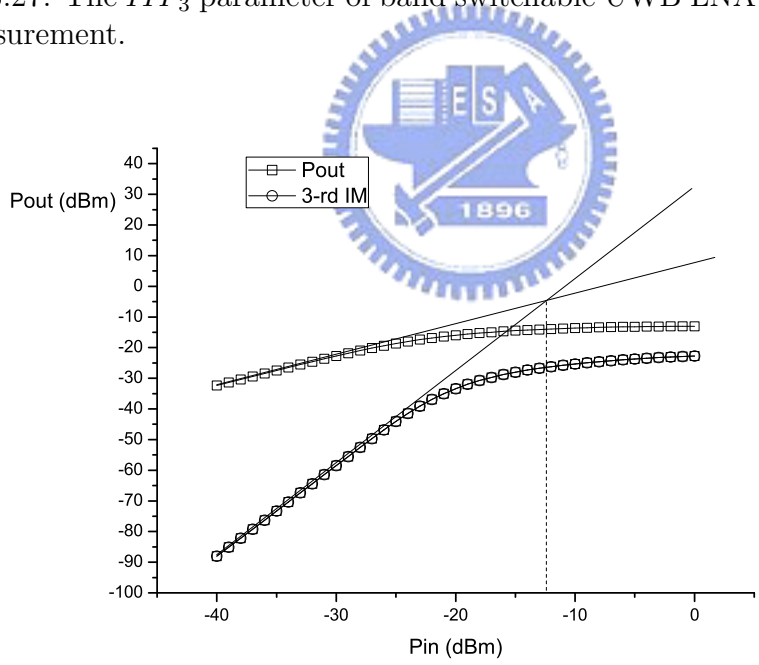


Figure 3.28: The IIP_3 parameter of band switchable UWB LNA at low frequency for simulation.

Fig. 3.31: S_{22}

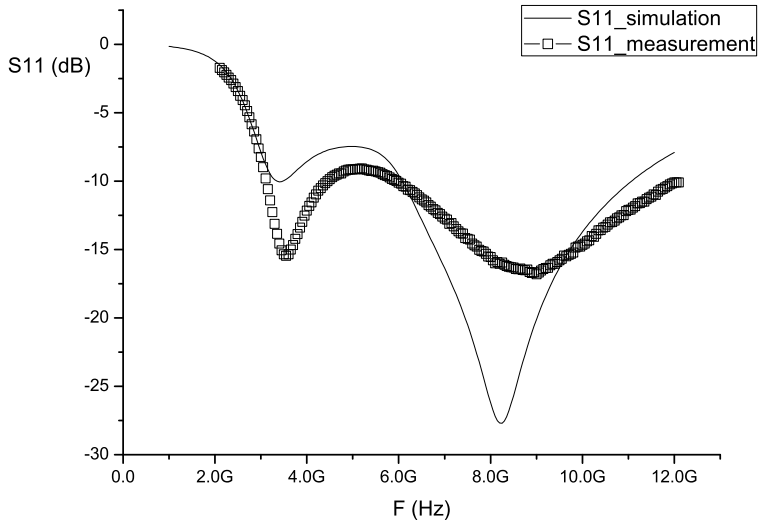


Figure 3.29: The S_{11} parameter of band switchable UWB LNA at high frequency.

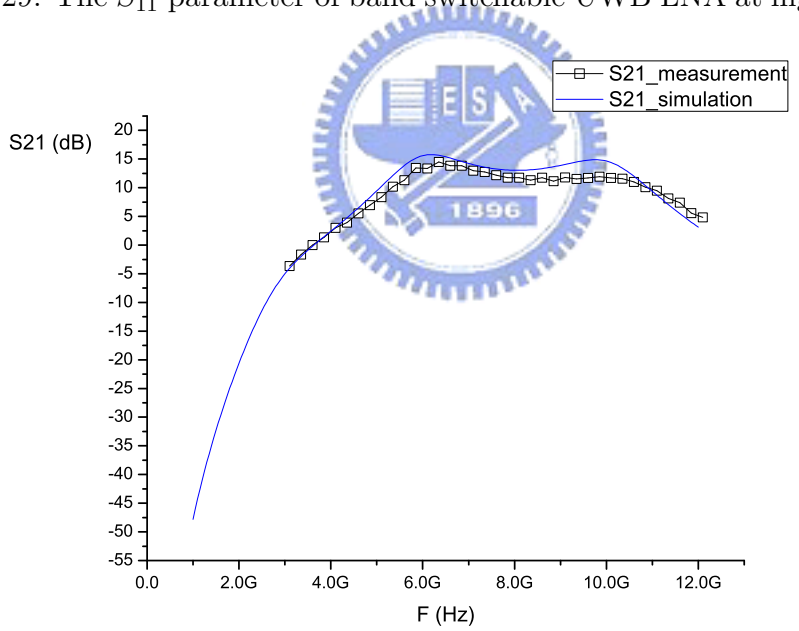


Figure 3.30: The S_{21} parameter of band switchable UWB LNA at high frequency.

- Noise Figure

  Fig. 3.32: NF

- P_{1dB}

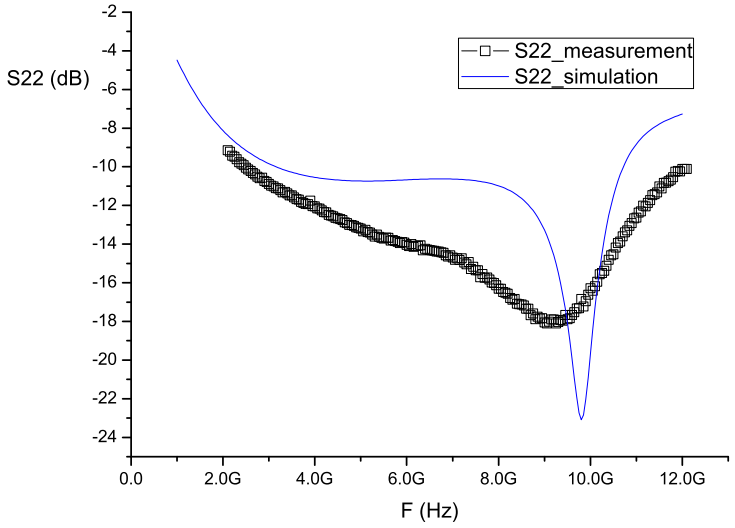


Figure 3.31: The S_{22} parameter of band switchable UWB LNA at high frequency.

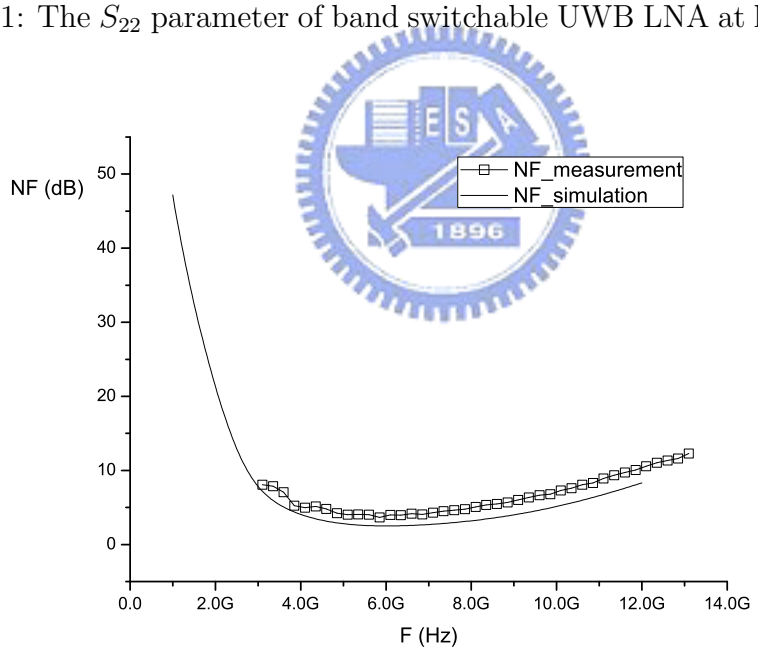


Figure 3.32: The NF parameter of band switchable UWB LNA at high frequency.

Fig. 3.33: P_{1dB} of measurement

Fig. 3.34: P_{1dB} of simulation

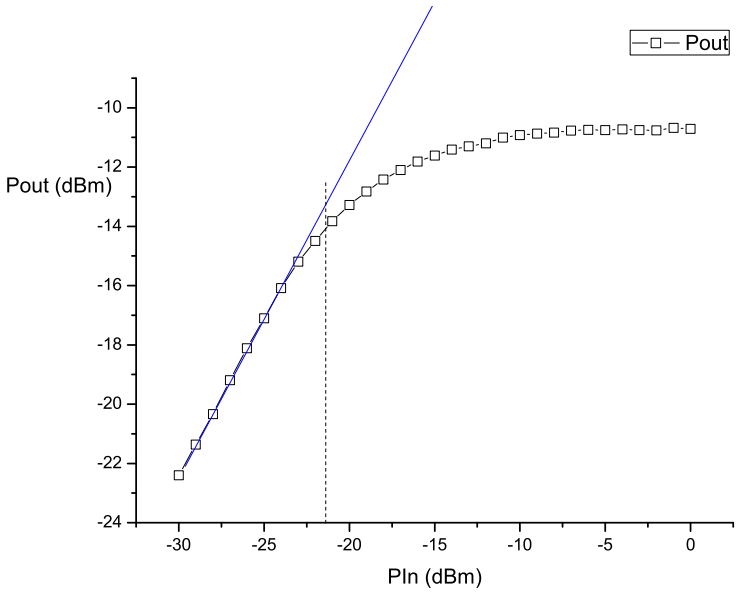


Figure 3.33: The P_{1dB} parameter of band switchable UWB LNA at high frequency for measurement.

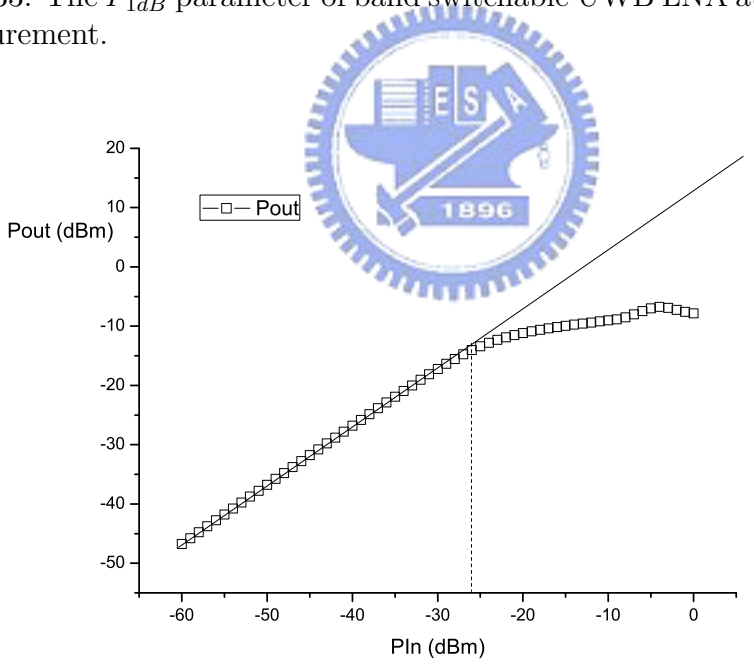


Figure 3.34: The P_{1dB} parameter of band switchable UWB LNA at high frequency for simulation.

- IIP_3

  Fig. 3.35: IIP_3 of measurement

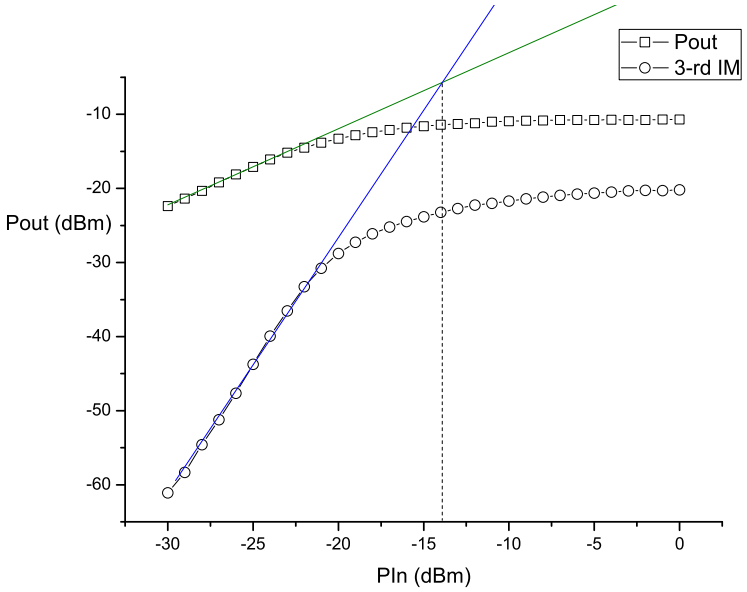


Figure 3.35: The IIP_3 parameter of band switchable UWB LNA at high frequency for measurement.

Fig. 3.36: IIP_3 of simulation

3.8.1 Discussion

Finally measurement and simulation results are listed as Tab. 3.1 and Tab. 3.2, respectively. The total power of measurement and simulation pass through a 1.8 V power supply are 28.62mW and 18.54mW, respectively. The comparison is shown in Tab. 3.3. The simulation power consumption is lower than others, but the power gain approximate the power gain of [22] and the power gain of [15] that also used switch capacitor topology. Note that [15] is simulation result and the gain of [16] is maximum voltage gain. The noise figure of [16] is minimum noise figure. However we see that the power consumption of measurement is large and the bandwidth in low band is narrower than simulation results. Hence we redesigned it in next section.

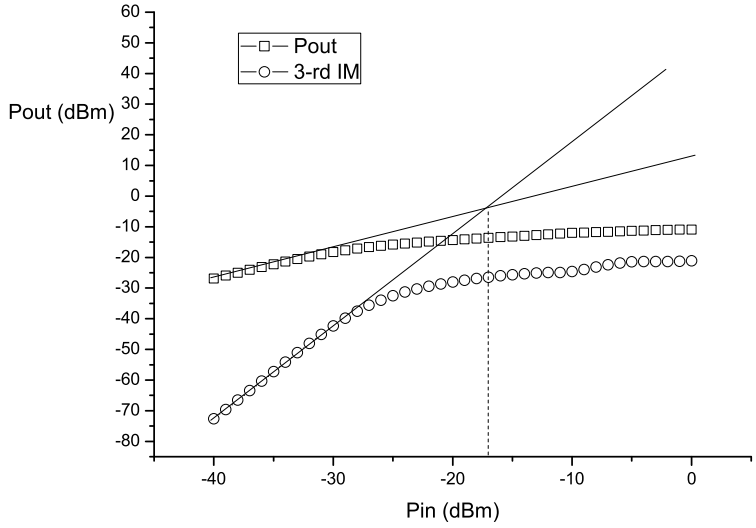


Figure 3.36: The IIP_3 parameter of band switchable UWB LNA at high frequency for simulation.

3.9 Improved Band Switchable UWB LNA

From the measurement result shown in Sec. 3.8, we can find the bandwidth of low band is smaller than simulation result. The bandwidth in fabricated chip only is 1GHz that is half of the simulation result. In addition the power consumption is large than simulation result. The reduced bandwidth is due to the low power gain in the second stage and the parasitic resistance in via that connect the switch NMOS and capacitors. In order to reduce the parasitic resistance we use more via. In addition, we improve the lower power gain by adding the gain tunable bias. We separate the bias voltage terminal in the second stage from all bias voltage terminals. Thus the bias voltage terminal of the second stage is independent. Thus we can tune the gain in the second stage by controlling the bias voltage terminal in the second stage. The large power consumption is due to the MOS variation in process, because we can get the simulation result by adding DC current. However there are different DC conditions for individual stages in MOS variation in process. Hence we separate all bias voltage terminals, because

Technology	TSMC 0.18um	
Topology	Switch-Capacitor	
Specification	Low	High
Supply Voltage	1.8 V	1.8 V
S_{11}	< -10.4 dB	<-10 dB
S_{22}	< -11 dB	< -14 dB
Power Gain	7.5dB - 10.5dB	11.2dB - 14dB
NF	3.4dB - 4.9dB	3.1dB - 6.8dB
P_{1dB}	-20 dBm	-22 dBm
IIP_3	-8 dBm	-16 dBm
BW(GHz)	3.4-4.4	6-10.6
Power	28.62 mW	28.62 mW

Table 3.1: The measurement result of band switchable UWB LNA.

the tunable bias circuit helps us to get the DC condition for every stage.

3.10 Layout of Improved Band Switchable UWB LNA

As discussed in Secs. 3.6 and 3.9, the layout is added the pads for different stages. As shown in Fig. 3.37. The chip is fabricated in CMOS process with TSMC 0.18μm. It uses 1P6M. The total chip area is 1.15mm $\times$ 1.02mm.

Technology	TSMC 0.18um	
Topology	Switch-Capacitor	
Specification	Low	High
Supply Voltage	1.8 V	1.8 V
S_{11}	< -8.8 dB	< -9.56 dB
S_{22}	< -9.98 dB	< -10.68 dB
Power Gain	6.9dB - 10.6dB	12dB - 15.7dB
NF	3dB - 4.8dB	2.5dB - 5.9dB
P_{1dB}	-21 dBm	-26 dBm
IIP_3	-12 dBm	-17 dBm
BW(GHz)	3.1-5	6-10.6
Power	18.54 mW	18.54 mW

Table 3.2: The simulation result of band switchable UWB LNA.

3.11 Microphotograph of Improved Band Switchable UWB LNA

The microphotograph of improved band switchable UWB LNA is shown in Fig. 3.38 that is fabricated in the TSMC 0.18μm CMOS process technology. And the die area is 1.15mm $\times$ 1.02mm with the bonding pads.

3.12 Measurement Result of Improved Band Switchable UWB LNA

As discussed in Sec. 3.8, using identical instrument to measure. At low band mode measurement results of improved LNA are itemized as follows:

- S-parameters

  Fig. 3.39: S_{11}

  Fig. 3.40: S_{21}

  Fig. 3.41: S_{22}

Paper	Topology	Techno-logy	BW (GHz)	S_{11} (dB)	S_{22} (dB)	S_{21} (dB)	NF (dB)	Power (mW)
This work simulation	Switch Capacitor	CMOS 0.18um	3.1-5	< -8.8	< -9.98	6.9-10.6	3-4.8	18.54
			6-10.6	< -9.56	< -10.68	12-15.7	2.5-5.9	18.54
This work measurement	Switch Capacitor	CMOS 0.18um	3.4-4.4	<-10.4	<-11	7.5-10.5	3.4-4.9	28.62
			6-10.6	<-10	<-14	11.2-14	3.1-6.8	28.62
[15]†	Switch Capacitor	CMOS 0.18um	3.1-4.8	<-8.9	<-8.3	5.6-8.4	4.1-4.9	24.8
			6-8.1	<-9.4	<-9.7	9-11.1	3.8-4.1	24.8
			8.1-10.3	<-8.4	<-10.1	8.1-10.3	4.1-4.8	24.8
[16]	Notch Filter	CMOS 0.13um	3-5	<-10	N/A	19.4‡	3.5*	31.5
[17]	4-stages common-source	CMOS 0.18um	3-10.6	<-9	<-13	15.9-17.5	3.1-5.7	33.2
[22]	3-stages common-source	CMOS 0.18um	3-6	<-12.2	<-10.1	13.5-15.8	4.7-6.7	59.4
[23]	Cascode	UMC 0.13um	2.2-9	<-9.2	<-10	11.3	3.9-4.6	30

†: simulation result. ‡:maximum voltage gain. ∗:minimum NF.

Table 3.3: The performance comparison of band switchable UWB LNA.

- Noise Figure
  Fig. 3.42: NF
- P_{1dB}
  Fig. 3.43: P_{1dB}
- IIP_3
  Fig. 3.44: IIP_3

At high band mode measurement results of improved LNA are itemized as follows:

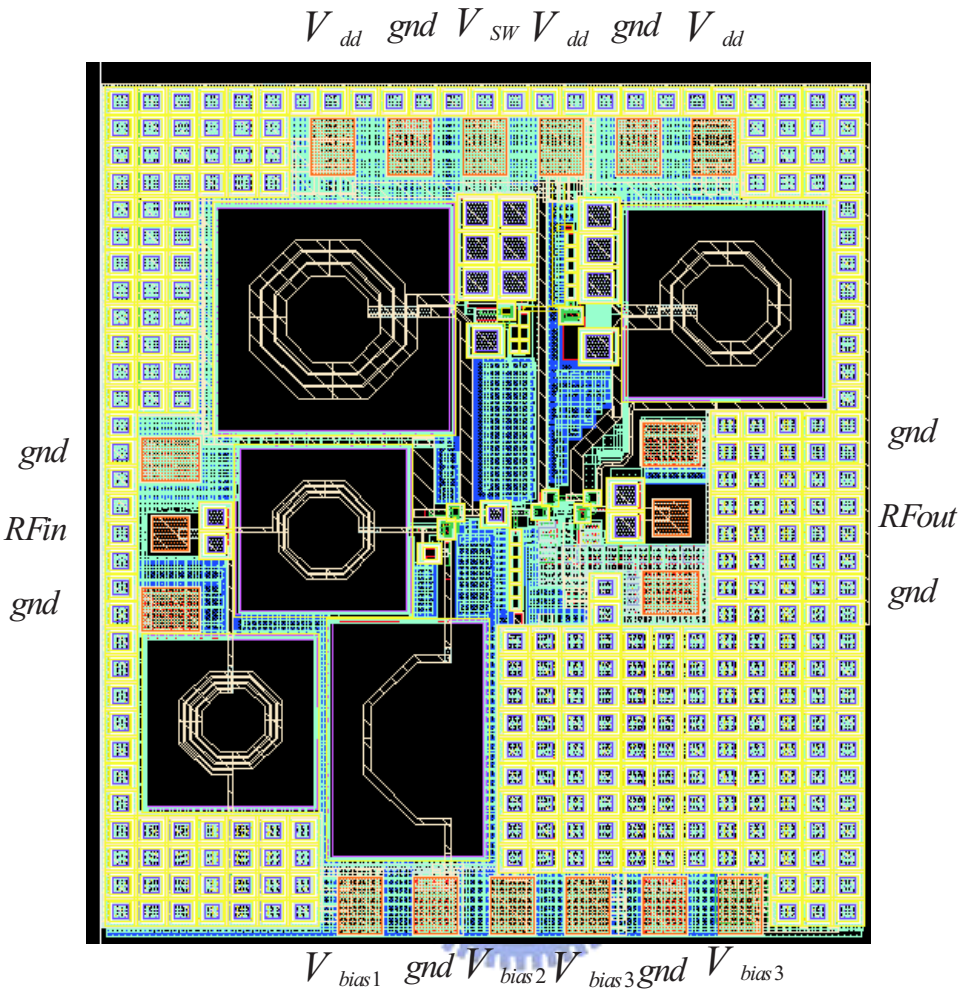


Figure 3.37: The layout of improved band switchable UWB LNA.

- S-parameters

  Fig. 3.45: S_{11}

  Fig. 3.46: S_{21}

  Fig. 3.47: S_{22}

- Noise Figure

  Fig. 3.48: NF

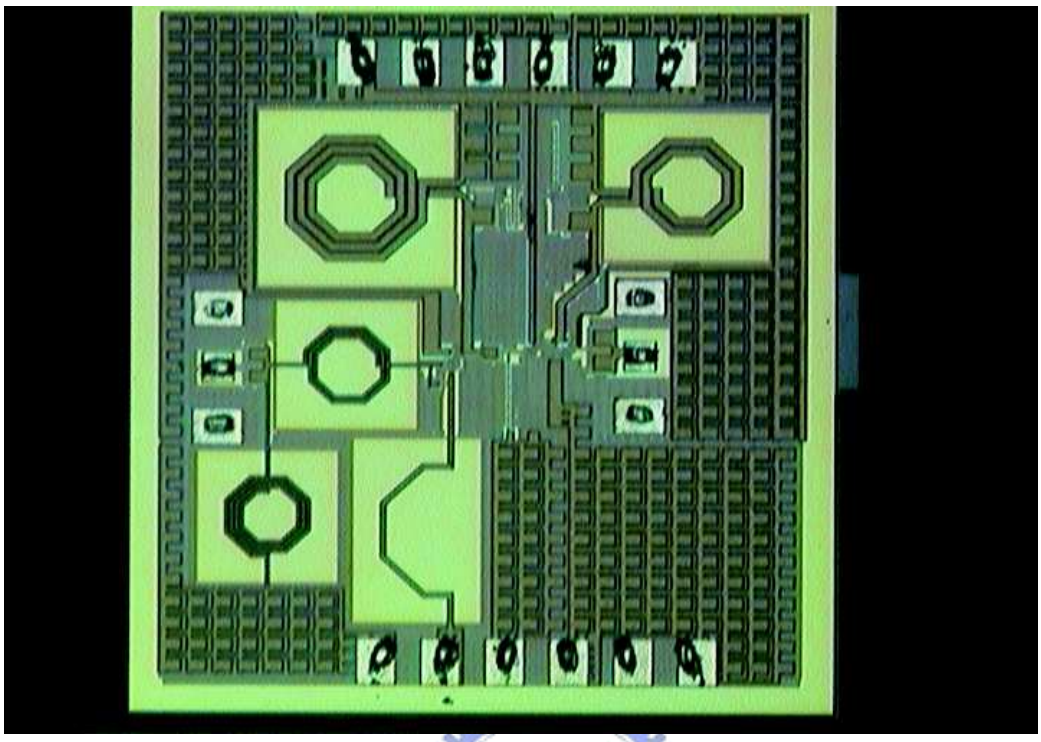


Figure 3.38: The chip photo of improved band switchable UWB LNA.

- P_{1dB}

  Fig. 3.49: P_{1dB}

- IIP_3

  Fig. 3.50: IIP_3

3.12.1 Discussion

Finally the results are list as Tab. 3.4. The comparison is shown in Tab. 3.5. The total power of measurement pass through a 1.8 V power supply are 22.46mW. The improved power consumption is lower than others. The improved noise figure is lower than [22]. The improved gain is higher than [22]. Note that [15] is simulation result and the gain of [16] is maximum voltage gain. The noise figure of [16] is minimum noise figure.

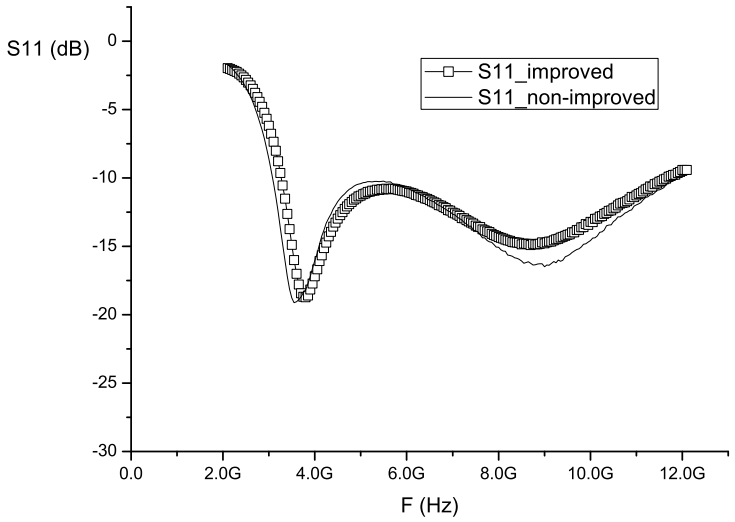


Figure 3.39: The S_{11} parameter of improved band switchable UWB LNA at low frequency.

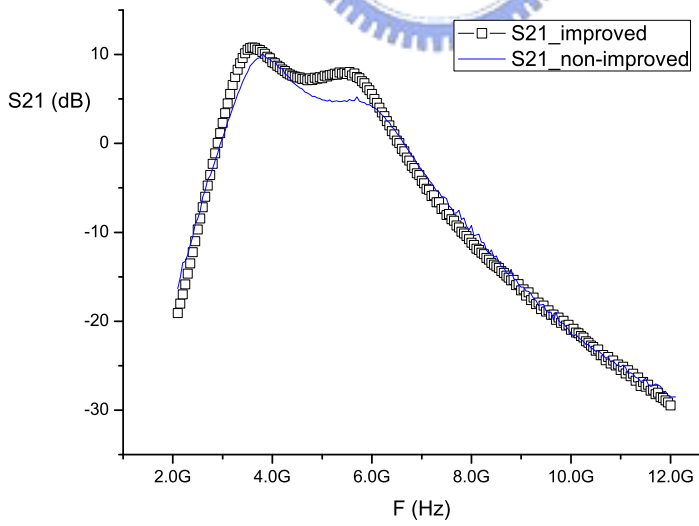


Figure 3.40: The S_{21} parameter of improved band switchable UWB LNA at low frequency.

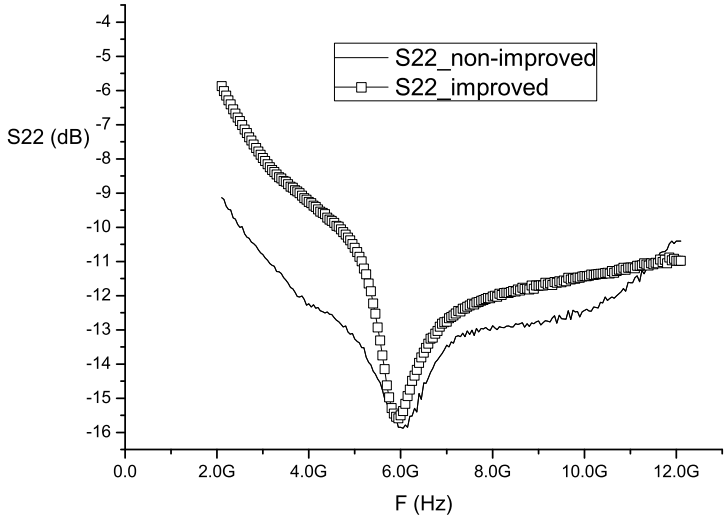


Figure 3.41: The S_{22} parameter of improved band switchable UWB LNA at low frequency.

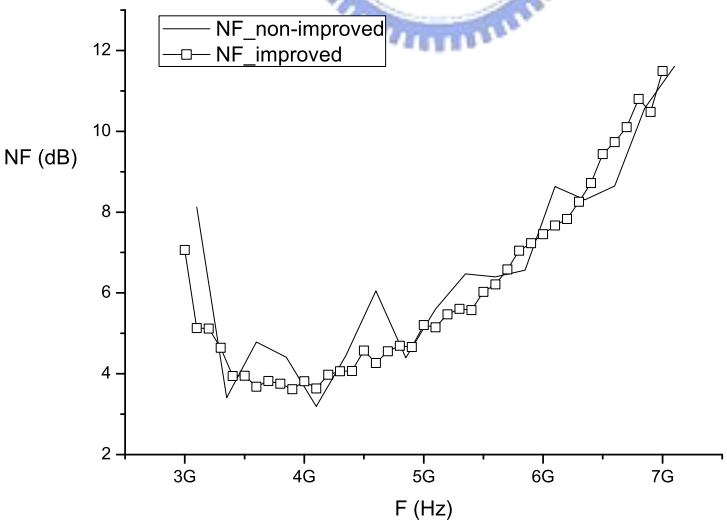


Figure 3.42: The NF parameter of improved band switchable UWB LNA at low frequency.

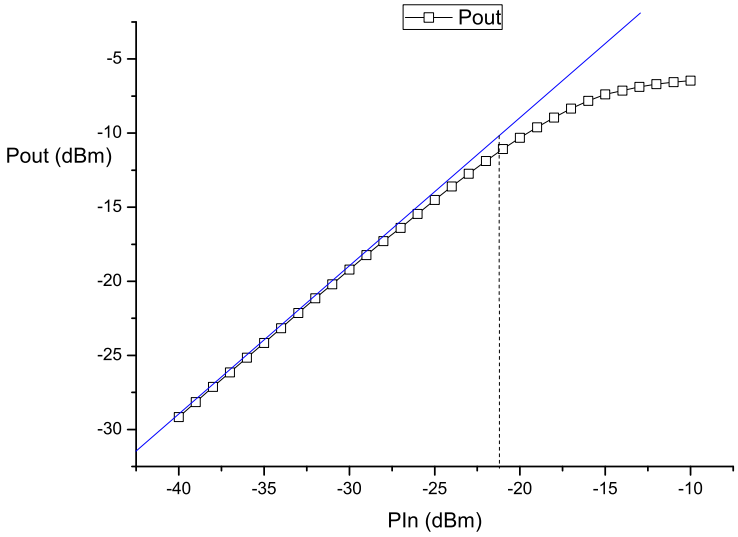


Figure 3.43: The P_{1dB} parameter of improved band switchable UWB LNA at low frequency for measurement.

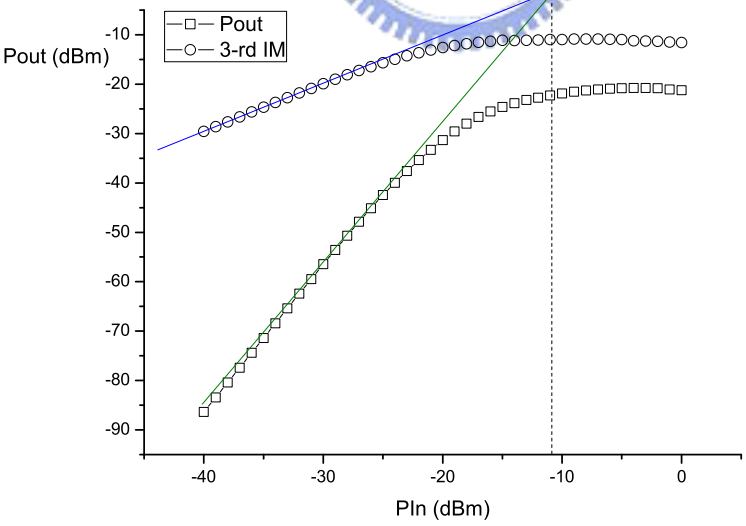


Figure 3.44: The IIP_3 parameter of improved band switchable UWB LNA at low frequency for measurement.

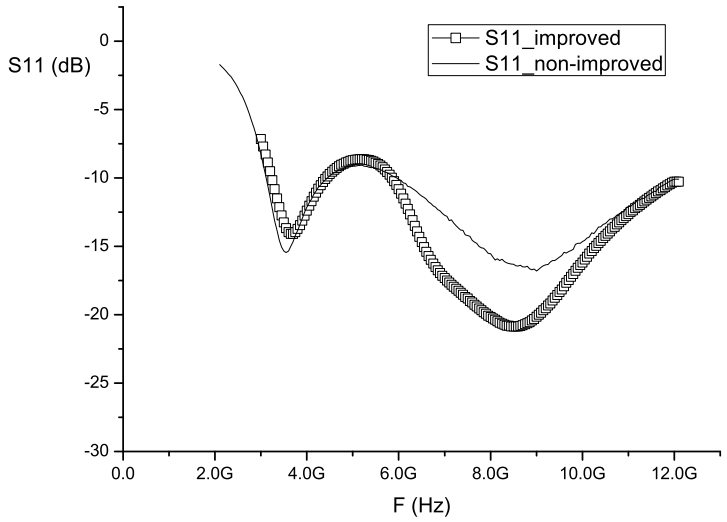


Figure 3.45: The S_{11} parameter of improved band switchable UWB LNA at high frequency.

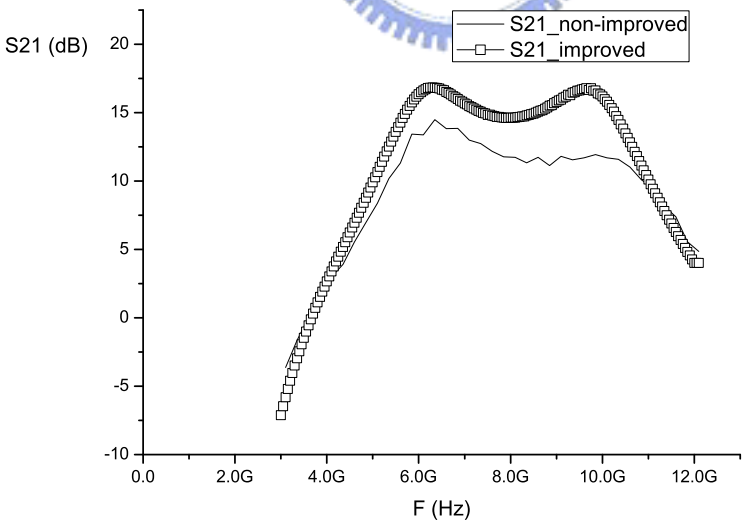


Figure 3.46: The S_{21} parameter of improved band switchable UWB LNA at high frequency.

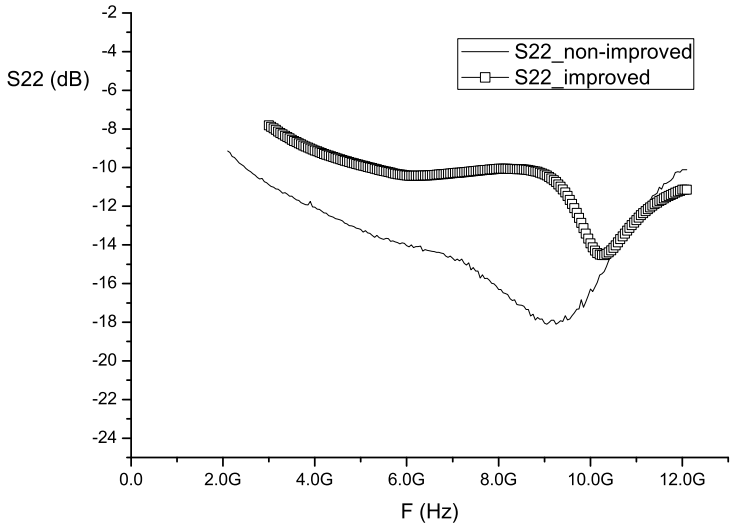


Figure 3.47: The S_{22} parameter of improved band switchable UWB LNA at high frequency.

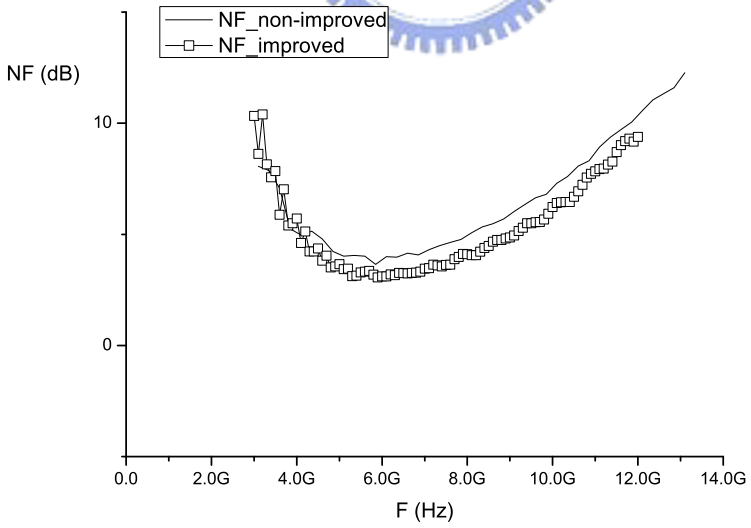


Figure 3.48: The NF parameter of improved band switchable UWB LNA at high frequency.

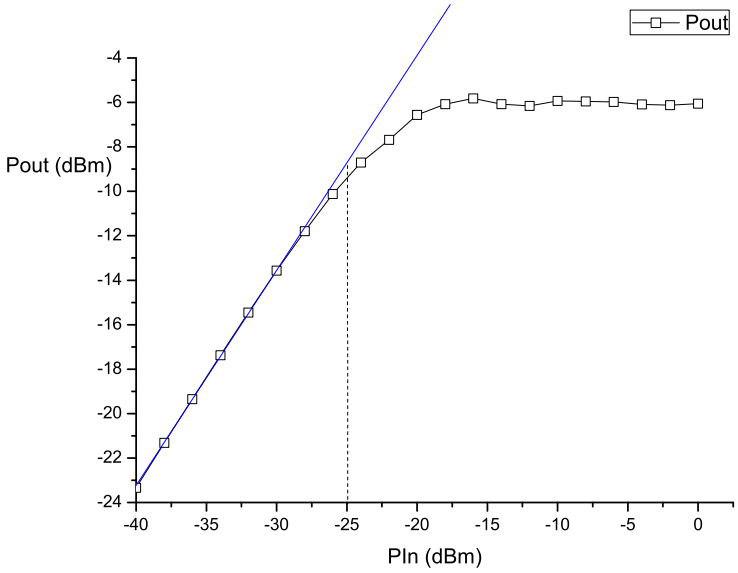


Figure 3.49: The P_{1dB} parameter of improved band switchable UWB LNA at high frequency for measurement.

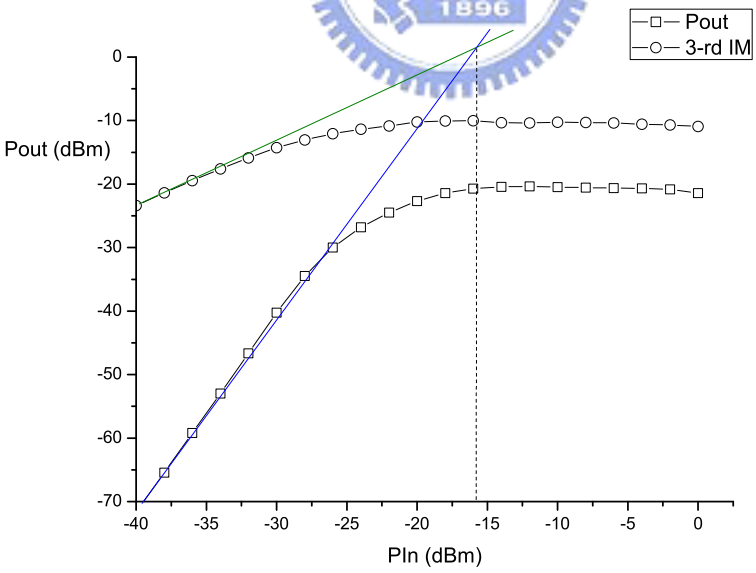


Figure 3.50: The IIP_3 parameter of improved band switchable UWB LNA at high frequency for measurement.

Technology	TSMC 0.18um	
Topology	Switch-Capacitor	
Specification	Low	High
Supply Voltage	1.8 V	1.8 V
S_{11}	< -9.6 dB	<-10.8 dB
S_{22}	< -8.4 dB	< -10.4 dB
Power Gain	7.5dB - 10.8dB	13.8dB - 16.8dB
NF	3.6dB - 6.2dB	3.1dB - 6.5dB
P_{1dB}	-22 dBm	-25 dBm
IIP_3	-11 dBm	-16 dBm
BW(GHz)	3.25-5.6	6-10.4
Power	22.46 mW	22.46 mW

Table 3.4: The measurement result of improved band switchable UWB LNA.

Paper	Topology	Technology	BW (GHz)	S_{11} (dB)	S_{22} (dB)	S_{21} (dB)	NF (dB)	Power (mW)
This work improved measurement	Switch Capacitor	CMOS 0.18um	3.25-5.6	< -9.6	< -8.4	7.5-10.8	3.6-6.2	22.46
			6-10.4	< -10.8	< -10.4	13.8-16.8	3.1-6.5	22.46
This work non-improved measurement	Switch Capacitor	CMOS 0.18um	3.4-4.4	<-10.4	<-11	7.5-10.5	3.4-4.9	28.62
			6-10.6	<-10	<-14	11.2-14	3.1-6.8	28.62
[15]†	Switch Capacitor	CMOS 0.18um	3.1-4.8	<-8.9	<-8.3	5.6-8.4	4.1-4.9	24.8
			6-8.1	<-9.4	<-9.7	9-11.1	3.8-4.1	24.8
			8.1-10.3	<-8.4	<-10.1	8.1-10.3	4.1-4.8	24.8
[16]	Notch Filter	CMOS 0.13um	3-5	<-10	N/A	19.4‡	3.5*	31.5
[17]	4-stages common-source	CMOS 0.18um	3-10.6	<-9	<-13	15.9-17.5	3.1-5.7	33.2
[22]	3-stages common-source	CMOS 0.18um	3-6	<-12.2	<-10.1	13.5-15.8	4.7-6.7	59.4
[23]	Cascode	UMC 0.13um	2.2-9	<-9.2	<-10	11.3	3.9-4.6	30

†: simulation result. ‡:maximum voltage gain. ∗:minimum NF.

Table 3.5: The performance comparison of improved band switchable UWB LNA.

Chapter 4

Band Switchable Wi-MAX LNA Design

In this chapter, we will present the Band Switchable Wi-MAX LNA. First we discuss the consideration in the Wi-MAX switchable LNA design in Sec. 4.1. Second the circuit for wideband input matching is presented in Sec. 4.2. In Sec. 4.3 we propose the new improved topology of the switch circuit from Sec. 3.3. And an output buffer for measurement is discussed in Sec. 4.4. All the circuits discussed in Secs. 4.2 - 4.4 combine the Band Switchable Wi-MAX LNA in Sec. 4.5. Finally the simulation result of this circuit is shown in Sec. 4.6.

4.1 Consideration for Wi-MAX Switchable LNA

In general the conventional Wi-MAX LNAs are wideband LNA [1][2] for example 2-11GHz [1] and 2-6GHz [2]. However the frequency bands of Wi-MAX are different in different country. Thus there is no need to use the whole band of Wi-MAX. That is, different frequency band can use different LNA with narrow band so that we have advantages including

1. Reducing the input noise.

2. Restraining the interference from other bands.

It can reduce the input noise then raises the input SNR. Because if the LNA is whole band, all the noise in the whole band will be included in the system

as shown in Fig. 4.1. Hence the total noise is not decreased and all the noise including out of desired band will be amplified by the LNA. Hence we should use better filters to remove the noise at back-end. Another benefit is it can restrain

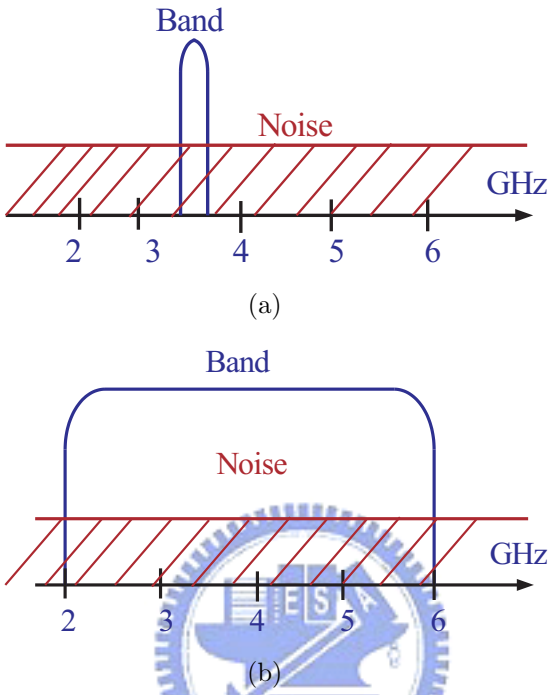


Figure 4.1: The input frequency is 3.5GHz, and noise is in two condition: (a) narrow band, (b) wideband.

the interference from other bands. If using the whole band LNA, all other signals will be received as shown in Fig. 4.2. But those signals are not in the desired band. They will interfere with the our desired signal. Also, the harmonics of those unwanted signals also distort our the desired signal. As discussed in Sec. 2.3, not only the 3-rd intermodulatoin but also 5-th and 7-th intermodulatoin can distort desired signal. Hence the switch band LNA is desired.

4.2 Wideband Input Matching

As discussed in Sec. 2.1, we need input matching circuit to get input matching. However the switch bands is 4 bands (2.3GHz, 2.5GHz, 3.5GHz, 5.8GHz), thus using switchable input matching circuit is too complex. The switch can product

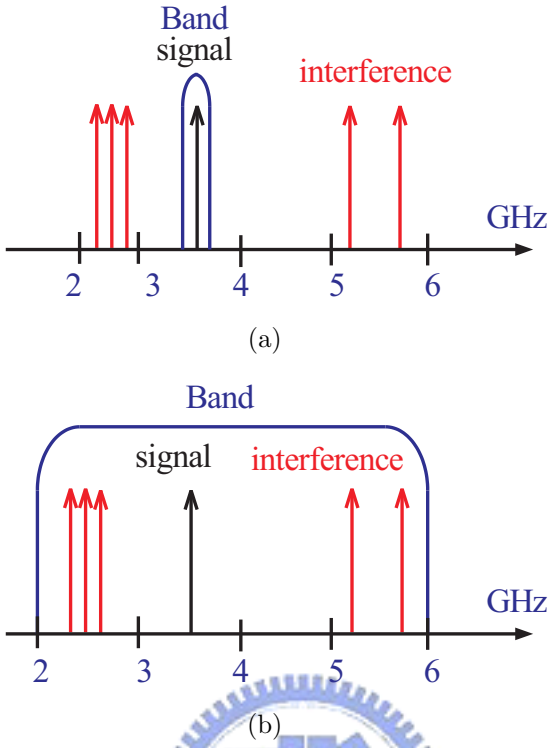


Figure 4.2: The input frequency is 3.5GHz, and the interferences are in two condition: (a) narrow band, (b) wideband.

the noise, because it is a noise source. The noise can influence our noise performance directly, hence we use the wideband input matching circuit as discussed in Sec. 3.2. The wideband matching circuit that we chose is shown in Fig. 4.3. But the design frequency is different, in this circuit the band we used is 2.3GHz to 5.8GHz. Hence we redesign the wideband matching circuit. In a word, according to Eq.(3.3) we first design the input impedance in 5.8GHz by adjusting L_g, L_s, C_C, C_b and M_1 in the inductive source degeneration circuit. Then according to Eq.(3.10) we design the input impedance in 2.3GHz by adjusting L_d. Finally the two band results in a wideband input matching.

4.3 Switch Circuit Topology

As discussed in Sec. 3.3, we already have a good switch band circuit. In this section we improve our switch band circuit again. From Fig. 3.11(c) , we remove

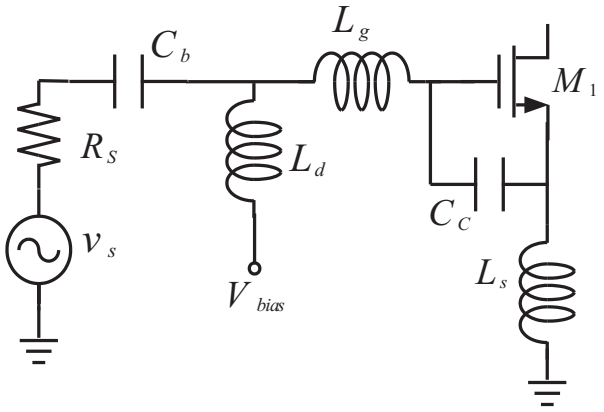


Figure 4.3: The input matching for Wi-MAX LNA.

the capacitor that connects to V_{dd}, then connects the source of switch NMOS to ground as shown in Fig. 4.4, where C is the switched capacitor.

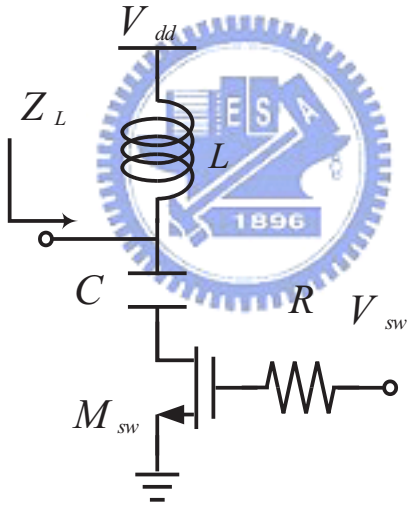


Figure 4.4: The switch circuit of Wi-MAX LNA.

The benefit is this circuit saves a capacitor and reduces the size of loading capacitor, because now the loading capacitor is C when switch MOS is on. Hence the equivalent capacitance is C when M_{sw} is on. However the conidtion is the same with Fig. 3.11(c) when M_{sw} is off. Hence the equivalent capacitance is

$$C_{eq} = \frac{C_{gs}C_{gd}}{C_{gs} + C_{gd}},$$

when M_{sw} is off. That is

$$C_{eq} = \begin{cases} \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}}, & M_{sw} \text{ is off.} \\ C, & M_{sw} \text{ is on.} \end{cases}$$

The resonant frequency is

$$\omega = \frac{1}{\sqrt{LC_{eq}}}.$$

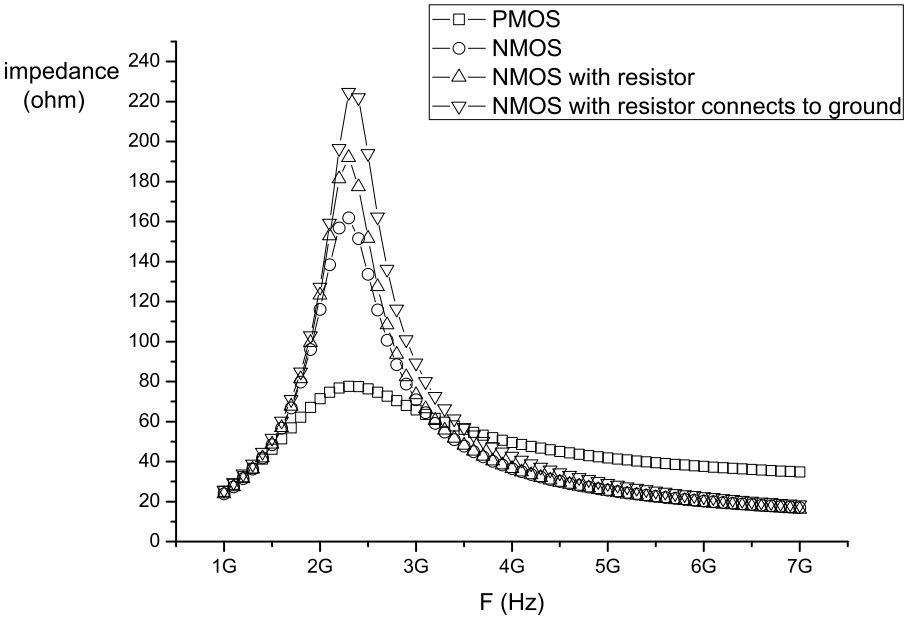
The impedance of the band switch circuit shown in Fig.4.4 and Fig.3.11 are shown in Fig .4.5. The largest impedance at low frequency is the NMOS-based with large resistor connects to ground. This is because its r_{on} is smallest, and the Q is largest at the low band. The low r_{on} is due to high mobility of NMOS and the size of switch. This implies that at the low band the gain of NMOS-based switch with large resistor connects to ground is the largest and that of the PMOS-based is the smallest. At the high band the gain of NMOS-based switch with large resistor connects to ground and the gain of NMOS-based switch with large resistor are both the smallest. This is because the condition is the same. As discussed in Sec. 3.3 the PMOS-based switch is the largest. From Fig. 4.5 we can find the impedance of every switch is larger at high band than at low band. Hence the gain of low band is lower than high band. Thus in order to fit specification, the gain of low band is a more important issue. Hence we choose the NMOS-based with large resistor connects to ground as our switch band circuit to increase the gain of low band .

4.4 Output Buffer

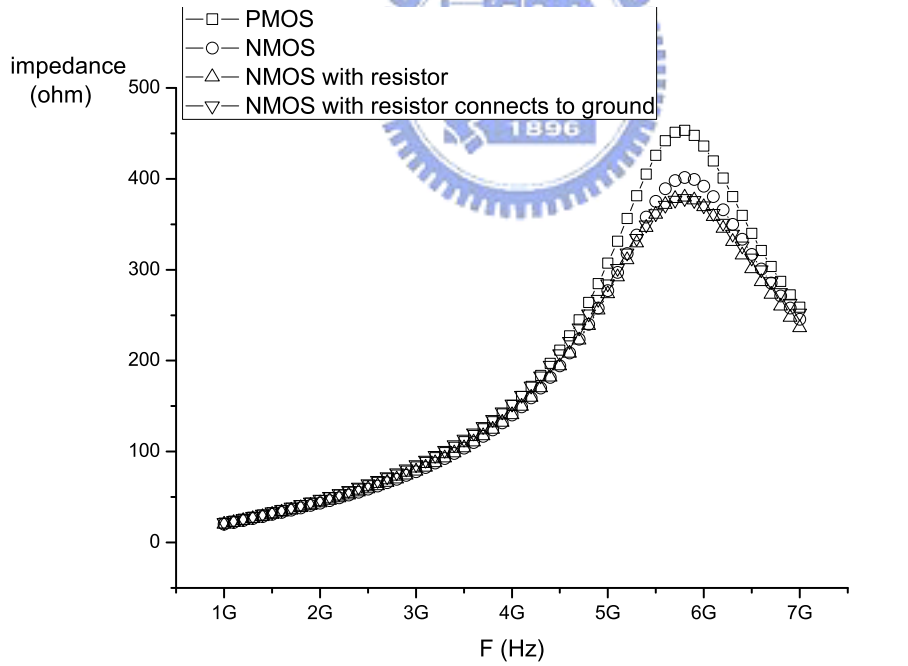
As discussed in Sec. 3.4, we use buffer to achieve output matching. From Eg.(3.14), the output impedance is

$$Z_{out} = \left(\frac{1}{sC_{gs}} \parallel \frac{1}{g_m}\right) + \frac{1}{sC_b},$$

Hence we design $1/gm$ is equal to be 50 ohm and the imaginary part (C_b, C_{gs}) approach zero at the band that we want.



(a)



(b)

Figure 4.5: The impedance of four types switch band circuit: (a) at low frequency, (b) at high frequency.

4.5 Band Switchable Wi-MAX LNA

As discussed in Sec.3.5, we use the cascode LNA topology, because it reduces Miller effect on input transistor M_1 to attain high-frequency performance. However we do not need the cascade LNA topology, because the Wi-MAX LNA we designed is a narrow band LNA. Hence the power of next stage is saved. And we use 1.5 voltage for power supply to reduce power consumption of band switchable Wi-MAX LNA.

The proposed Wi-MAX LNA is shown in Fig.4.6 which consists of the input matching network that is implemented by the Butterworth Filter [9] (consisting of L_d, L_g, L_s, C_c and C_{gs1}) ; the one stage amplifier (containing M_1 and M_2) ; the switch capacitance loading of the amplifiers (consisting of L, M_{sw1}, C_1, C_2, C_3, M_{sw2} and M_{sw3}) ; the output buffer (consisting of M_3 and M_4); the three DC blocking capacitors (consisting of C_b); R_1, R_2 and R_3 are resistor that reduce parasitic capacitance of switch. V_{sw1}, V_{sw2} and V_{sw3} are the control voltage source of the switch capacitance loading. First when V_{sw1}, V_{sw2} and V_{sw3} are all 0, it is in the 5.8GHz mode. Second when V_{sw1}, V_{sw2} and V_{sw3} are 0, 0, and 1.5, it is in the 3.5GHz mode. Third when V_{sw1}, V_{sw2} and V_{sw3} are 0, 1.5, and 1.5, it is in the 2.5GHz mode. Finally when V_{sw1}, V_{sw2} and V_{sw3} are 1.5, 1.5, and 1.5, it is in the 2.3GHz mode. Given an operation frequency, we can achieve this frequency by adjusting the size M_{sw1}, M_{sw2} and M_{sw3} when they are off. On the other hand, when M_{sw1}, M_{sw2} and M_{sw3} are on, the size of M_{sw1}, M_{sw2} and M_{sw3} will affect the resistance of the switch capacitance loading. The size of M_1 trades off between the input matching and the noise figure of the LNA.

4.6 Simulation Result

As discussed in Sec. 3.8, the simulator is ADS 2006A. Simulation results are itemized as follows:

- S-parameters

  Fig. 4.7: S_{11}

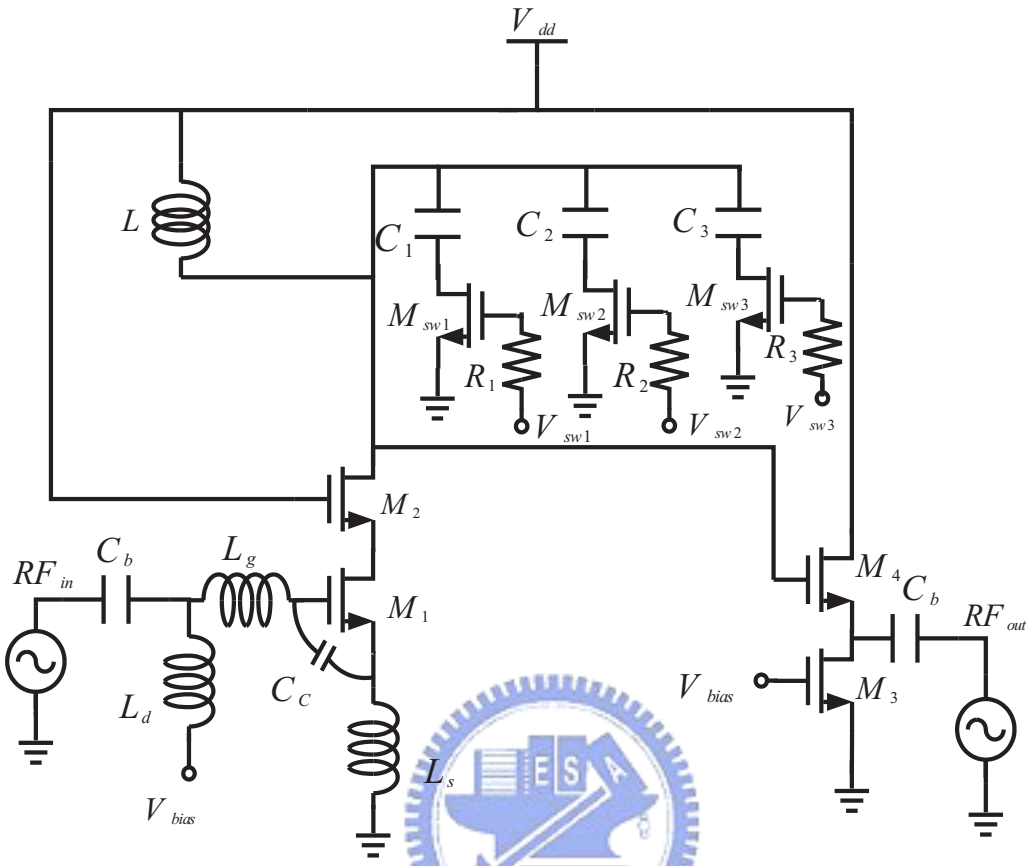


Figure 4.6: The proposed Wi-MAX low noise Amplifier.

Fig. 4.8: S_{21}

Fig. 4.9: S_{22}

- Noise Figure

  Fig. 4.10: NF

- P_{1dB}

  Fig. 4.11: P_{1dB} at 2.3GHz

  Fig. 4.12: P_{1dB} at 2.5GHz

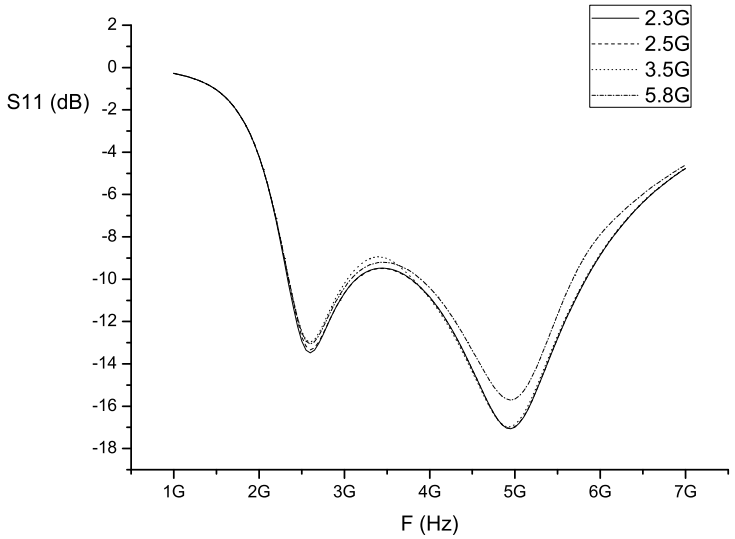


Figure 4.7: The S_{11} parameter of band switchable Wi-MAX LNA.

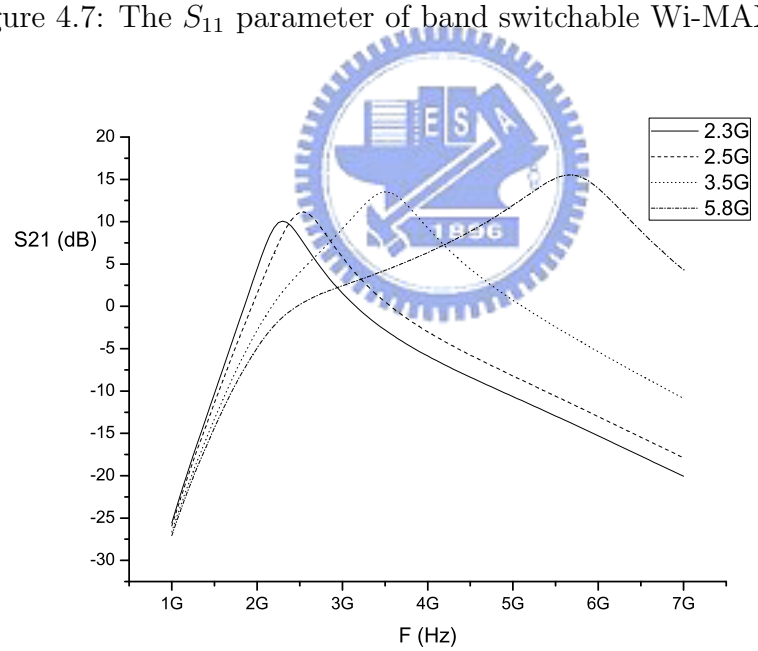


Figure 4.8: The S_{21} parameter of band switchable Wi-MAX LNA.

Fig. 4.13: P_{1dB} at 3.5GHz

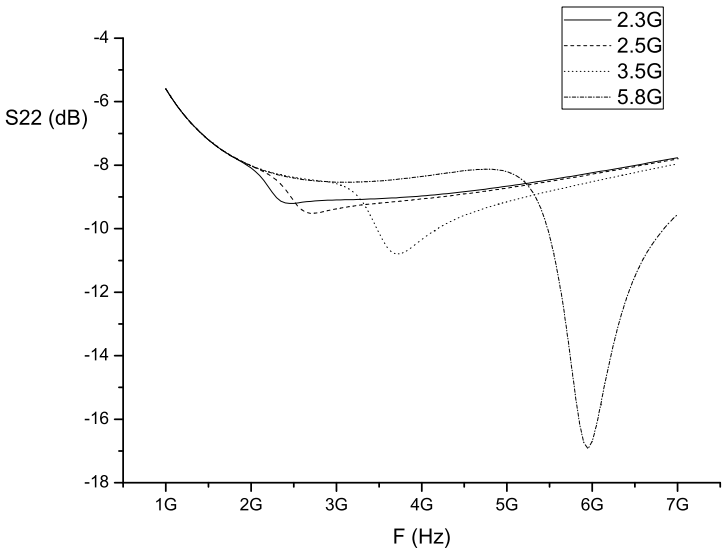


Figure 4.9: The S_{22} parameter of band switchable Wi-MAX LNA.

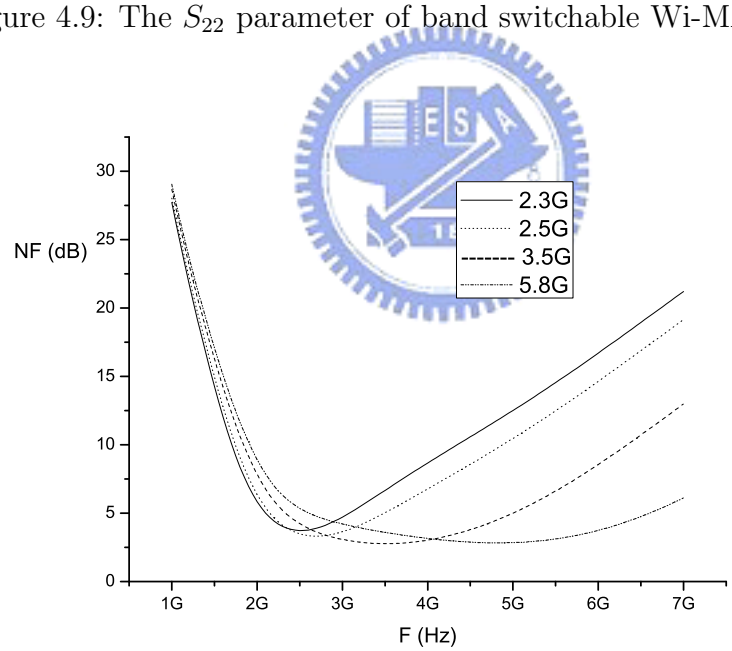


Figure 4.10: The NF parameter of band switchable Wi-MAX LNA.

Fig. 4.14: P_{1dB} at 5.8GHz

- IIP_3

  Fig. 4.15: IIP_3 at 2.3GHz

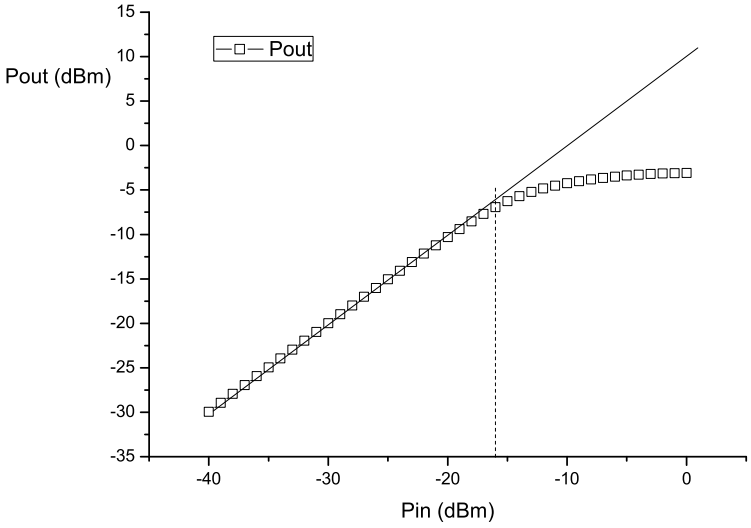


Figure 4.11: The P_{1dB} parameter of band switchable Wi-MAX LNA at 2.3GHz.

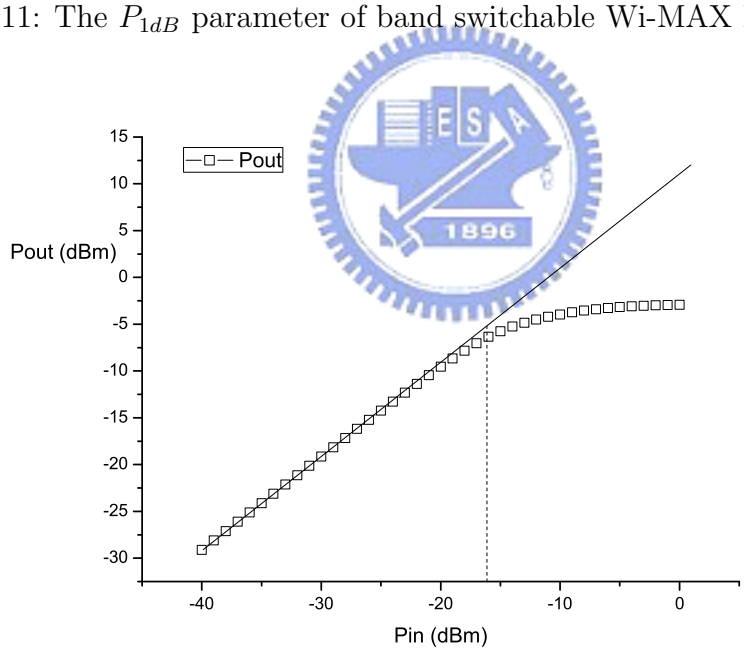


Figure 4.12: The P_{1dB} parameter of band switchable Wi-MAX LNA at 2.5GHz.

Fig. 4.16: IIP_3 at 2.5GHz

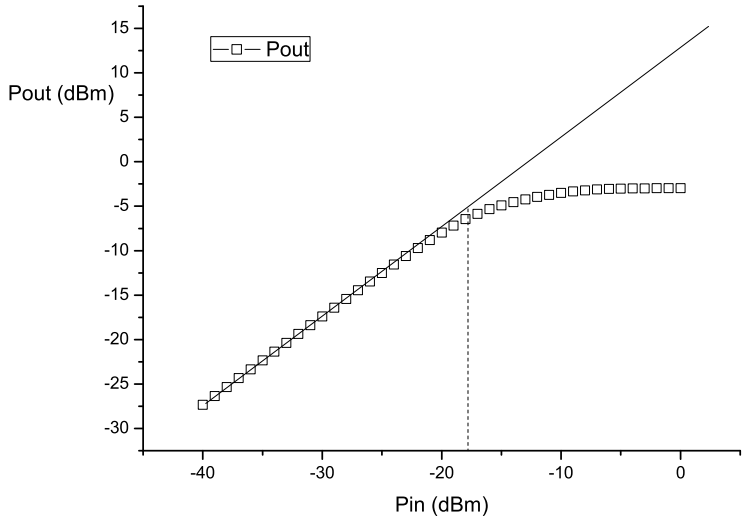


Figure 4.13: The P_{1dB} parameter of band switchable Wi-MAX LNA at 3.5GHz.

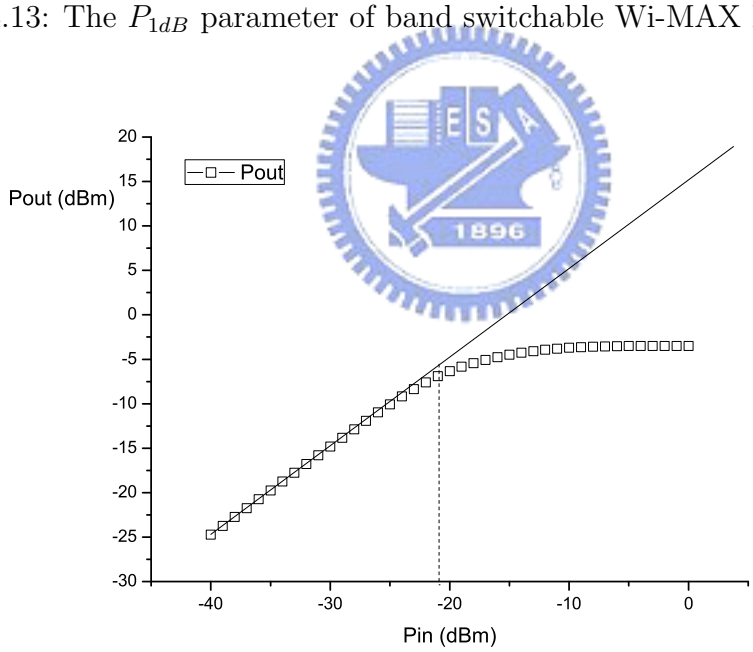


Figure 4.14: The P_{1dB} parameter of band switchable Wi-MAX LNA at 5.8GHz.

Fig. 4.17: IIP_3 at 3.5GHz

Fig. 4.18: IIP_3 at 5.8GHz

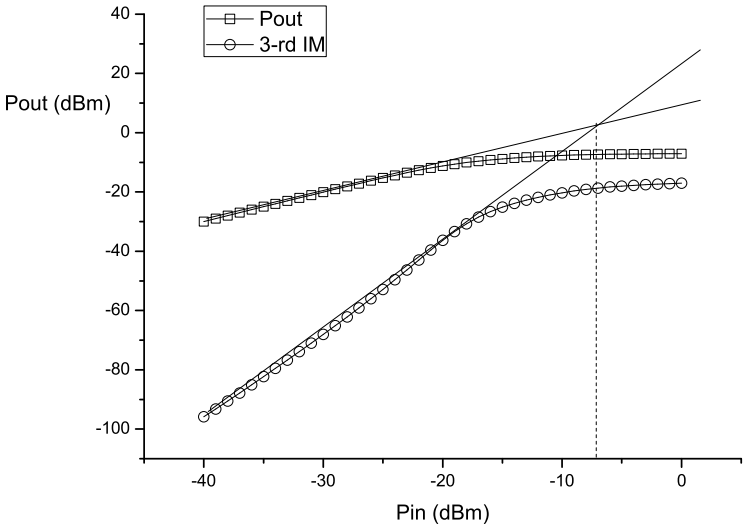


Figure 4.15: The IIP_3 parameter of band switchable Wi-MAX LNA at 2.3GHz.

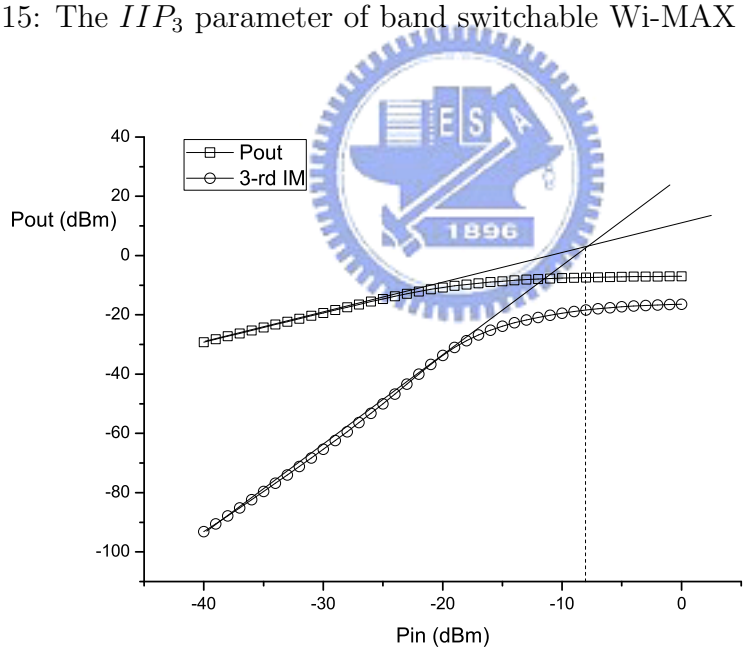


Figure 4.16: The IIP_3 parameter of band switchable Wi-MAX LNA at 2.5GHz.

4.6.1 Discussion

Finally the results are list as Tab. 4.1. The comparison is shown in Tab. 4.2. The total power of simulation pass through a 1.5 V power supply are 11.5mW.

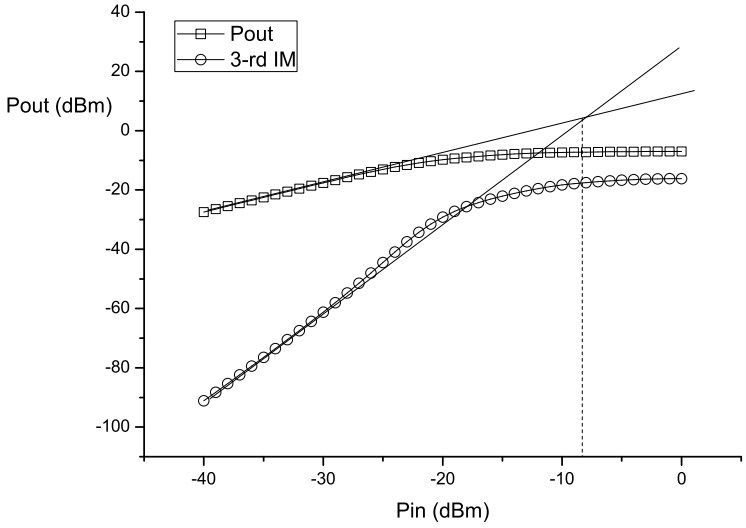


Figure 4.17: The IIP_3 parameter of band switchable Wi-MAX LNA at 3.5GHz.

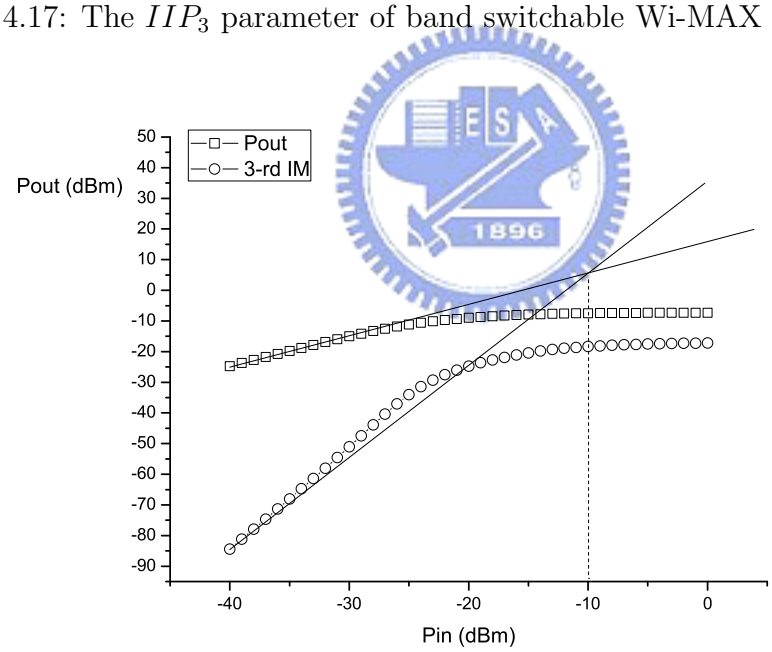


Figure 4.18: The IIP_3 parameter of band switchable Wi-MAX LNA at 5.8GHz.

The simulation power consumption is lower than others of Tab. 4.2, however the power gain is largest except for [24]. [18], [13], [24] are simulation results. [19] is measurement result. The gain of [24] is voltage gain. The gain of [19] is

transconductance gain.

Technology	TSMC 0.18um			
Topology	Switch-Capacitor			
Specification	2.3GHz	2.5GHz	3.5GHz	5.8GHz
Supply Voltage	1.5 V	1.5 V	1.5 V	1.5 V
S_{11}	-9.2 dB	-12.7dB	-9 dB	-10.2dB
S_{22}	-9 dB	-9dB	-10dB	-15.2 dB
Power Gain	10.1 dB	11.1dB	13.5dB	15.3dB
NF	4dB	3.5dB	2.8dB	3.4dB
P_{1dB}	-16 dBm	-16 dBm	-18dBm	-21dBm
IIP_3	-7 dBm	-8 dBm	-8dBm	-10dBm
Power	11.5 mW	11.5 mW	11.5 mW	11.5 mW

Table 4.1: The simulation result of band switchable Wi-MAX LNA.

Paper	Topology	Techno-logy	BW (GHz)	S_{11} (dB)	S_{21} (dB)	NF (dB)	IIP_3 (dBm)	Power (mW)
This work simulation	Switch Capacitor	CMOS 0.18um	2.3	< -9.2	10.1	4	-7	11.5
			2.5	<-12.7	11.1	3.5	-8	11.5
			3.5	< -9	13.5	2.8	-8	11.5
			5.8	< -10.2	15.3	3.4	-10	11.5
[18]	Notch	CMOS 0.18um	2.4	< -10.79	11.79	3.89	-3	13.5
			3.5	< -10.41	11.7	4.03	-2.1	13.5
			5.2	< -13.56	10.06	3.73	-0.4	13.5
[19]*	transcon-ductance	CMOS 65nm	2.4-2.7	< -10	28mS†	2.9	-13	14.8
[13]	Current-reuse	CMOS 0.18um	2-11	< -9.9	10.8-12.1	3.6	-10	14.3
[24]	capacitive cross-coupling	CMOS 0.13um	0.2-6.2	< -10	10.5‡	2.62-2.85	-2.7	2.23

†: transconductance gain. ‡: voltage gain. ∗: measurement result.

Table 4.2: The performance comparison of band switchable Wi-MAX LNA.

Chapter 5

Summy

5.1 Conclusions

In this thesis, we proposed a architecture for band switchable UWB LNA and band switchable Wi-MAX LNA. We designed a band switchable UWB LNA using NMOS-based switch with large resistor. The LNA was implemented in TSMC 0.18μm technology and was taped out. The measurement results showed that the LNA has power gain of 10.6dB for low band and 14dB for high band. The band switchable UWB LNA has noise figure of 3.4-4.9dB for low band and 3.1-6.8dB for high band. The total power consumption is 28.62mW. Moreover, in the second taped out chip, we also improved this LNA. The improved band switchable UWB LNA has power gain of 10.8dB for low band and 16.8dB for high band. The improved band switchable UWB LNA has noise figure of 3.6-6.2dB for low band and 3.1-6.5dB for high band. The total power consumption was reduced to 22.46mW. Furthermore, a band switchable Wi-MAX LNA using a NMOS-based switch connected to ground was proposed. This LNA also used TSMC 0.18μm technology. The pre-simulation results showed that power gain are 10.1dB for 2.3GHz, 11.1dB for 2.5GHz, 13.5dB for 3.5GHz and 15.3dB for 5.8GHz. The noise figure are 4dB for 2.3GHz, 3.5dB for 2.5GHz, 2.8dB for 3.5GHz and 3.4dB for 5.8GHz. The power consumption is 11.5mW with a 1.5V power supply. The proposed architectures can achieve higher gain under same power consumption compared to [15], [16] and [18].

5.2 Future Work

In the future work, we can move the low band frequency of the improved band switchable UWB LNA to 3.1GHz-5GHz by adding the capacitance in the second stage of the switch capacitor. Also, we would like to implement the proposed Wi-MAX LNA in TSMC 0.18μm technology and tape out.

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