國 立 交 通 大 學

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博 士 論 文

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摘　要

本論文主要研究方向為：對於目前應用於先進深次微米元件之各項技術所製作之金氧半場效電晶體(MOSFET)元件，進行其特性與可靠度(reliability)的探討。為解決超薄閘極氧化層(gate oxide)的漏電流問題，將引進氮化氧化層(nitrided oxide)與具有高介電常數(high-k)之材料來取代傳統閘極氧化層；且為進一步提升元件效能，將使用應變矽鍺(strained SiGe)材料作為元件之通道層(channel)；而為了改善高介電常數材料二氧化鉿(HfO_2)之薄膜特性，將使用不同之通道表面處理方法。因此，本論文將分為三大部分來進行探討：第一部份將針對具有超薄氮化閘極氧化層之n型深次微米金氧半場效電晶體，探討其熱電子劣化(hot-electron degradation)對可靠度之影響，以及其低頻跳動雜訊(flicker noise)之特性分析；第二部分針對具有經過一氧化二氮退火(N_2O-annealed)之超薄氮化矽(SiN)閘極介電層與應變矽鍺通道層之p型金氧半場效電晶體，研究其電應力壓迫(stressing)劣化機制與應

變矽鍺通道層厚度對元件特性的影響；第三部分則將探討不同表面處理對超薄二氧化鉿閘極介電層薄膜特性的影響。

對於多種具有超薄(等效氧化層厚度為 1.6 nm)氮化閘極氧化層之 0.13 μm n型金氧半場效電晶體，研究其因熱電子引起電子捕捉(electron trapping)所造成之元件劣化行為，我們發現經由多種氮化技術如氮化矽/二氧化矽堆疊(Si_3N_4/SiO_2 stack)、一氧化氮退火氮化(NO nitridation)與電漿氮化(plasma nitridation)等所形成之超薄氮化閘極介電層，將導致比傳統閘極氧化層有較嚴重的因熱電子所引起之元件劣化現象，而此熱電子劣化行為主要是因為氮加入於超薄閘極介電層中所造成之電子陷阱(electron trap)產生，而非由介面狀態(interface state)的產生所主導，此機制亦經由綜合各方面的實驗結果而獲得證實。因為將具有氮化閘極氧化層的元件於熱電子應力壓迫後，僅發現臨界電壓(threshold voltage)的正向漂移，並無發現嚴重的次臨界電壓擺幅值(subthreshold swing)變大現象，且閘極漏電流變小，由直流電流電壓(DCIV)量測所得到之I_b–V_{cb}特性曲線斜率亦無明顯變化，而臨界電壓對應力壓迫時間(stress time)所得之次方值(exponent, n~0.3)很小等，皆可說明元件因熱電子引起之電子捕捉即為造成元件劣化的主要原因。此外，實驗結果也顯示了於超薄氧化層中加入氮成分，將使閘極氧化層更易有熱電子劣化現象而產生嚴重的可靠度問題。而於多種氮化技術中，我們也發現電漿氮化的方式所造成的熱電子劣化效應較小，所以對於未來具有超薄氮化閘極氧化層之奈米元件的應用深具潛力。

我們亦對於傳統二氧化矽、氮化矽/二氧化矽堆疊、一氧化氮退火氮化與電漿氮化等多種超薄閘極氧化層(等效氧化層厚度為 1.6 nm)之 0.15 μm n 型金氧半場效電晶體，研究其低頻跳動雜訊特性，並發

現對於所有具有經過氮化處理之閘極氧化層元件，其跳動雜訊皆明顯的增加。其主因是來自於因氮的加入使得氧化層中電子陷阱增加所造成，因為電子陷阱的增加將提高電子捕捉/逃離(trapping/detrapping)的機率，而此正是造成低頻跳動雜訊的主要機制。另外對於電漿氮化氧化層元件，發現經熱電子應力壓迫後，其跳動雜訊並無顯著的影響，原因為熱電子應力壓迫時，雖有電子陷阱產生但亦伴隨著電子捕捉的發生，因此電子陷阱產生所引起的電子捕捉/逃離現象較為不明顯。然而當氧化層發生崩潰(breakdown)時，雖然因為崩潰為氧化層中產生大量缺陷而形成電流導通路徑(conduction path)所造成，因而導致其跳動雜訊明顯增強，但氮化氧化層增強的幅度卻較傳統氧化層和緩。此外，也發現雜訊頻率指標(frequency index of the noise spectrum)將隨著閘極偏壓而改變，且亦與氧化層的電子缺陷有很密切的關係，而熱載子劣化與氧化層崩潰都將造成傳統氧化層與氮化氧化層的雜訊頻率指標變小。綜合此低頻跳動雜訊的特性來看，電漿氮化技術所製作之氮化氧化層因具有較佳的薄膜品質，使未來奈米元件在類比與高頻電路應用上亦表現了其可行性的潛力。

另一方面，我們成功地結合了應變矽鍺通道與超薄一氧化二氮退火(N_2O-annealed)之氮化矽閘極介電層，製作出p型金氧半場效電晶體。此元件具有厚度為 50 nm的$Si_{0.85}Ge_{0.15}$通道層，與等效氧化層厚度為 3.1 nm的一氧化二氮退火之氮化矽閘極介電層，且由實驗結果顯示此元件亦有表現不錯的開/關與輸出特性。此外，透過數種不同的量測方式，我們將針對該元件的可靠度進行分析，所使用的方法有應力壓迫引發漏電流(SILC)、汲極雪崩熱載子(DAHC)注入、通道熱載子(CHC)注入以及負偏壓溫度不穩定性(NBTI)等。比較各個方法所得之分析結果後發現，對於元件的長時間劣化行為來說，因為在應力壓迫

後僅發現很微小的劣化現象，因此可以確信經一氧化二氮退火之氮化矽閘極介電層具有極佳的薄膜品質。此外，我們亦發現熱載子劣化比負偏壓溫度不穩定性的劣化較為嚴重，其中又更以通道熱載子應力壓迫所造成的劣化為所有劣化行為中最劇烈的。同時我們也發現介面狀態的產生即為導致熱載子所引發劣化現象的主要機制，而對於負偏壓溫度不穩定性的劣化則主要是由電子捕捉行為所主導。

進一步地，我們發現應變矽鍺通道層的厚度對於具有應變矽鍺通道，與超薄一氧化二氮退火氮化矽閘極介電層之p型金氧半場效電晶體特性有很大的影響，若將應變矽鍺通道層厚度控制在小於 15 nm 以下，我們將可獲得極佳的元件特性，如次臨界電壓擺幅值為 68 mV/dec 、介面狀態密度為 1×10^{11} $eV^{-1}cm^{-2}$、較小的接面(junction)漏電流大小以及比傳統矽通道元件高過 50%大小的電洞遷移率(hole mobility)等，而此結果亦表示使用經一氧化二氮退火之氮化矽薄膜作為閘極介電層將與應變矽鍺通道層之間可獲得極佳的介面品質，進而提升元件的特性與效能。

最後我們探討了不同的沈積前(pre-deposition)表面處理方法對二氧化鉿閘極介電層電性的影響，而表面處理方法有氫氟酸浸潤(HF-dipped)、氨氣退火氮化(NH_3-annealed)與快速高溫氧化(RTO-treated)等三種。 由實驗結果可知，經過氨氣退火氮化表面處理後具有較佳的二氧化鉿薄膜特性，原因為其漏電流較低，且具有較小的等效氧化層厚度(EOT)，以及適度大小的遲滯寬度(hysteresis width)。相對的，快速高溫氧化處理雖然因為可獲得較厚的等效氧化層厚度而有效的降低漏電流，但卻有相當嚴重的遲滯效果。另外，我們亦針對初始反相偏壓(initial inversion bias)、溫度與量測頻率等對遲滯效果的影響，對所有經過不同表面處理方法所製作的薄膜進行研

究。結果顯示，遲滯寬度將隨著量測時的初始反相偏壓增加而變大，而隨著量測溫度升高而變小，但卻不易受量測頻率的影響而有很大的改變。並且綜合我們的實驗結果，亦可發現遲滯寬度大小對於初始反相偏壓與溫度皆呈指數型關係，而此關係亦可用一個一般性的經驗式來表現，此經驗式可表示為$C(T)\cdot\exp(R_V V_{inv})$的形式。再者，我們發現陷阱輔助穿遂(trap-assisted tunneling)效應為所有薄膜的導通電流機制，因為其電流密度在低電壓時比起在高電壓時對溫度的改變有較劇烈的變化，而根據陷阱輔助穿遂模型，我們亦萃取了所有相關的參數並表列比較之。

Advanced Deep Sub-Micron MOSFETs with Ultra-Thin High-k Gate Dielectrics and Strained SiGe Channel

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A Dissertation

Department of Electronics Engineering and Institute of Electronics

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Abstract

We have investigared the device characteristics and the reliability of the MOSFETs fabricated by advanced deep sub-micron technologies. To reduce the intolerable leakage current of the ultra-thin gate oxide, the nitrided oxides and high-k gate dielectrics are introduced to place the conventional gate oxide; the strained SiGe layer is applied to be the device channel for enhancing the device performance; various surface treatments are performed to improve the quality of high-k HfO_2 film. Hence, our studies are focused on three main topics. Firstly, we have investigated the effects of hot-carrier degradation on device reliability and the low-frequency flicker noise characteristics for the deep sub-micron nMOSFETs with ultra-thin nitrided gate oxides. Secondly, the degradation mechanism of high voltage stressing and the channel thickness effect on device characteristics for the deep sub-micron pMOSFETs with ultra-thin N_2O-annealed SiN gate dielectric and strained $Si_{0.85}Ge_{0.15}$ channel have been studied. Finally, we have also investigated the effect of pre-deposition surface

treatment on the electrical characteristics for the ultra-thin HfO_2 gate dielectrics.

We have investigated the device degradation caused by the hot-electron-induced electron trapping in various ultra-thin (EOT = 1.6 nm) nitrided gate oxides for 0.13 μm nMOSFETs. It has been found that the nitrogen-incorporated gate dielectrics by a variety of popular techniques including Si_3N_4/SiO_2 (N/O) stack, NO annealing, and plasma nitridation result in enhanced hot-electron-induced device degradations as compared to the conventional gate oxide counterpart. The exacerbated hot-electron degradations are attributed to the electron trap generation in the ultra-thin gate dielectric rather than the interface state generation as a result of nitrogen incorporation, and the mechanism has also been confirmed by several aspects: the positive shift of threshold voltage, the insignificant variation of subthreshold swing, the reduction of gate leakage current, no slope change of the I_b-V_{cb} curves for DCIV measurement, and a small exponent value (n ~ 0.3) of ΔV_t versus stress time after the nitrided gate oxide devices were stressed. Moreover, the nitrogen incorporation into the ultra-thin gate oxide has been demonstrated to be more vulnerable to the hot-electron degradation as considering the long-term reliability issues, and the plasma nitridation has been shown to be the most promising technique of ultra-thin gate oxide nitridation for the sub-100nm device applications.

The low-frequency flicker noise of the 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal oxide, Si_3N_4/SiO_2 (N/O) stack, NO oxynitride, and plasma nitrided oxide has been demonstrated. We have found that the nitrogen incorporation in the ultra-thin gate oxide will increase the flicker noise by introducing more electron traps. It is due to the fact that the low-frequency flicker noise is mainly generated by the trapping/detrapping of channel electrons with the interface states and the electron traps. However, the nitrogen incorporation can improve the device immunity against the hot-carrier degradation in the flicker noise because the hot-electron-induced

electron trapping may suppress the effective electron traps for generating flicker noise. Moreover, moderate increase of noise level is observed when the nitrided oxide is suffering breakdown comparing with the thermal oxide even though a significant amount of electron traps are created when oxide breakdown occurs. We also found that the frequency index of the noise spectrum is varied with the gate bias and it is strongly related to the oxide traps. Hot-carrier degradation and oxide breakdown may lower the frequency index for both thermal oxide and nitrided oxide devices. For considering the flicker noise characteristics, the plasma nitrided oxide has been demonstrated its potential for sub-100 nm MOSFET devices in analog and RF applications because of its higher oxide quality.

The pMOSFET with 50-nm thick $Si_{0.85}Ge_{0.15}$ channel and ultra-thin (EOT=3.1 nm) N_2O-annealed SiN gate dielectric has been shown to have well-performing on/off and output characteristics. Several methodologies for the device reliability characterization, such as stress-induced leakage current (SILC), drain avalanche hot-carrier (DAHC) injection, channel hot-carrier (CHC) injection and negative bias temperature instability (NBTI), have been used and the results are compared. In terms of the long-term degradation, the excellent quality of the N_2O-annealed SiN gate dielectric can be firmly obtained because only negligible degradations have been found after stressing no matter which technique was employed. Even so, the experimental results have been compared and we found that the HC degradation is worse than the NBTI degradation and the channel hot-carrier (CHC) stressing is the worst case for all kinds of reliability testing. Meanwhile, we have also verified that the interface state generation is the dominant mechanism responsible for the HC-induced degradation while the electron trapping dominates the device degradation for the NBTI stressing.

We also have found that the thickness of SiGe channel has a great impact on the

device characteristics. With controlling the SiGe layer thickness thinner than 15 nm, the device depicts a subthreshold swing of 68 mV/dec, the interface state density of 1×10^{11} $eV^{-1}cm^{-2}$, acceptable junction leakage, and more than 50% hole mobility improvement comparing to the Si channel device. Therefore, high quality interface between the gate dielectric and the strained SiGe channel can be achieved by using the N_2O-annealed SiN gate dielectric and the device performance can be improved.

Finally, we have investigated the effects of various pre-deposition surface treatments, such as HF dipping (HF-dipped), NH_3 surface nitridation (NH_3-annealed), and rapid thermal oxidation (RTO-treated), on the electrical properties of HfO_2 gate dielectrics. The NH_3-annealed technique is far superior to the others because the dielectric subjecting to the NH_3 surface nitridation possesses a tremendously reduced leakage current, the lowest equivalent oxide thickness (EOT), and a moderate hysteresis width. In contrast, the RTO-treated preparation can only effectively reduce the leakage current by its resultant increased physical thickness and displays considerably severe hysteresis. The dependence of hysteresis on the initial inversion bias (V_{inv}), temperature, and frequency are also investigated for all splits. The hysteresis width increases upon increasing the initial inversion bias and decreasing the temperature, but it is rather insensitive to the measuring frequency. Our experimental results indicate that the hysteresis width depends exponentially on both the initial inversion bias and the temperature, and it can be described well by a general empirical relationship with the form $C(T)\cdot\exp(R_vV_{inv})$. In addition, the conduction currents through the dielectrics are probably dominated by trap-assisted tunneling (TAT) because the current densities display stronger temperature dependence at low voltage than they do at higher voltages. Based on the trap-assisted tunneling model, the corresponding parameters have been extracted and are presented.

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Contents

Abstract (Chinese) i

Abstract (English) vi

Acknowledgment (Chinese) x

Contents xii

Table Captions xv

Figure Captions xvi

Chapter 1 Introduction

1.1 An Overview of the Background and the Motivation 1

1.1.1 MOSFETs with Ultra-Thin Nitrided Gate Oxide 2

1.1.2 Strained SiGe Channel MOSFETs 3

1.1.3 Ultra-Thin HfO_2 Gate Dielectric 4

1.2 Organization of the Thesis 5

References 9

Chapter 2 Hot-Electron-Induced Electron Trapping in 0.13 μm nMOSFETs with Ultra-Thin (EOT = 1.6 nm) Nitrided Gate Oxide

2.1 Introduction 20

2.2 Device Fabrication and Characteristics Measurement 21

2.3 Results and Discussion 22

2.3.1 *I–V* Characteristics 22

2.3.2 CHE and SHE Stressing 24

2.3.3 DCIV Measurement 27

2.3.4 Device Lifetime 28

2.4 Summary 29

References 30

Chapter 3 Flicker Noise Characteristics of 0.15 μm MOSFETs with Ultra-Thin (EOT = 1.6 nm) Nitrided Gate Oxide

3.1 Introduction 61
3.2 Device Fabrication and Characteristics Measurement 62
3.3 Results and Discussion 63
3.4 Summary 67
References 69

Chapter 4 Reliability of Strained SiGe Channel pMOSFETs with Ultra-Thin (EOT = 3.1 nm) N_2O-Annealed SiN Gate Dielectric

4.1 Introduction 81
4.2 Device Fabrication and Characteristics Measurement 83
4.3 Results and Discussion 84
4.3.1 *C–V* and *I–V* Characteristics of pMOSFETs 84
4.3.2 CVS and CCS for pMOSCAPs 85
4.3.3 HC and NBTI Stressing for pMOSFETs 86
4.4 Summary 88
References 90

Chapter 5 Channel Thickness Effect on Strained SiGe Channel pMOSFETs with Ultra-Thin (EOT=3.1 nm) N_2O-Annealed SiN Gate Dielectric

5.1 Introduction 112
5.2 Device Fabrication and Characteristics Measurement 113
5.3 Results and Discussion 114
5.3 Summary 117

References 119

Chapter 6 Electrical Characteristics of Thin HfO_2 Gate Dielectrics Prepared Using Different Pre-Deposition Surface Treatments

6.1 Introduction 132
6.2 Device Fabrication and Characteristics Measurement 134
6.3 Results and Discussion 135
6.3.1 TEM and XPS Analysis 135
6.3.2 *C–V* and *I–V* Characteristics 136
6.3.3 Hysteresis 137
6.3.4 Conduction Mechanism 140
6.4 Summary 142
References 144

Chapter 7 Conclusions and Suggestions of Further Study

7.1 Conclusions 166
7.2 Suggestions of Further Study 171

Vita (Chinese)

Publication List

Table Captions

Chapter 6

Table. 6.1. Values of A, B, ln(A/B), R_v, and E_h under the conditions of V_{inv} = +3 V at T = 300 K. The terms A and B are proportionality constants, R_v is the reciprocal voltage constant, and E_h is the activation energy.

Table. 6.2. Values of E_a, qV_{IL}, ϕ_1, ϕ_2, and ϕ_t for all samples at V_g = +1 V. The term E_a is the activation energy, V_{IL} is the voltage across the interfacial layer, ϕ_1 is the barrier height between the Si substrate and the interfacial layer, ϕ_2 is the barrier between the interfacial layer and HfO_2, and ϕ_t is the effective energy of the electron traps with respect to the conduction band edge of the HfO_2 layer.

Figure Captions

Chapter 2

Fig. 2.1. Gate current densities as a function of gate voltage for four different gate dielectrics, and all devices have the same equivalent oxide thickness (EOT) of 1.6 nm.

Fig. 2.2. Linear (V_d = 0.05 V) I_d–V_g characteristics of nMOSFETs (W/L = 10/0.13 μm) with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

Fig. 2.3. Transconductance versus gate overdrive ($V_g - V_t$) of nMOSFETs (W/L = 10/0.13 μm) with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

Fig. 2.4. Substrate current versus gate voltage of nMOSFETs (W/L = 10/0.13 μm) with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

Fig. 2.5. Linear (V_d = 0.05 V) I_d–V_g characteristics of nMOSFETs (W/L = 10/0.13 μm) with an EOT of 1.6 nm thermal and plasma nitrided gate oxide before and after CHE ($V_g = V_d$ = 1.8 V) stressing for 10^4 seconds.

Fig. 2.6. Gate leakage currents of nMOSFETs (W/L = 10/0.13 μm) with an EOT of 1.6 nm plasma nitrided gate oxide before and after CHE ($V_g = V_d$ = 1.8 V) stressing for 10^4 seconds.

Fig. 2.7. Threshold voltage shift and transconductance reduction as a function of gate voltage with substrate biases of 0 V and –2 V for the 0.13 μm nMOSFET with an EOT of 1.6 nm plasma nitrided gate oxide after being stressed under SHE injection for 10^4 seconds. The source and drain are grounded.

Fig. 2.8. Threshold voltage shifts as a function of substrate bias for the 0.13 μm

nMOSFETs with various gate dielectrics (EOT = 1.6 nm) after SHE stressing for 10^4 seconds. The source and drain are grounded.

Fig. 2.9. Schematic band diagram and electron conduction path of n-channel MOSFET as stressed under different substrate bias conditions.

Fig. 2.10. Fig. 2.10. (a) Cross-sectional view and measurement setting of four-terminal n-channel MOSFET used in the DCIV measurement. (b) Base current versus collector-base voltage (I_b–V_{cb}) for five interface trap distributions, curve-# (drain, channel, source): curve-0 (0, 0, 0), curve-1 (nonuniform, 0, 0), curve-2 (0, uniform, 0), curve-3 (0, nonuniform, 0), and curve-4 (nonuniform, nonuniform, 0).

Fig. 2.11. Base currents measured by four-terminal DCIV method of the 0.13 μm nMOSFETs with an EOT of 1.6 nm plasma nitrided gate oxide before and after CHE and SHE stressing for 10^4 seconds.

Fig. 2.12. Threshold voltage shift as a function of stress time of the 0.13 μm nMOSFETs with various gate dielectrics (EOT = 1.6 nm) under SHE stressing (V_g = 2.2 V, V_{sub} = –1.5 V) for 10^4 seconds. The source and drain are grounded.

Fig. 2.13. Device lifetimes as a function of drain voltage for the 0.13 μm nMOSFETs with various gate dielectrics (EOT = 1.6 nm) under CHE stressing (V_g = V_d).

Chapter 3

Fig. 3.1. Linear (V_d = 0.1 V) I_d–V_g characteristics of 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

Fig. 3.2. Transconductance versus gate overdrive ($V_g - V_t$) of 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

Fig. 3.3. Low-frequency S_{Vg} noise power spectra versus frequency at linear operation ($V_g - V_t$ = 1.0 V and V_d = 0.1 V) for 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

Fig. 3.4. Low-frequency S_{Vg} noise power spectra (f = 100 Hz) versus gate overdrives ($V_g - V_t$) at linear operation (V_d = 0.1 V) for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after hot-carrier stressing ($V_g = V_d$ = 2.3 V for 1000 seconds).

Fig. 3.5. Low-frequency S_{Vg} noise power spectra (f = 100 Hz) versus gate overdrives ($V_g - V_t$) at saturation operation (V_d = 1 V) for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after hot-carrier stressing ($V_g = V_d$ = 2.3 V for 1000 seconds).

Fig. 3.6. Gate currents versus stress time for 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics stressed at V_g = 3.3 V.

Fig. 3.7. Low-frequency S_{Vg} noise power spectra (f = 100 Hz) versus gate overdrives ($V_g - V_t$) at linear operation (V_d = 0.1 V) for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after oxide breakdown (V_g = 3.3 V).

Fig. 3.8. The frequency index of noise spectrum, γ, versus gate voltages for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after hot-carrier stressing ($V_g = V_d$ = 2.3 V for 1000 seconds) and oxide breakdown (V_g = 3.3 V).

Chapter 4

Fig. 4.1. The schematic device cross-section and process flow of device fabrication.

Fig. 4.2. The capacitance–voltage (*C*–*V*) characteristics of the pMOSFET with 50 nm $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed SiN (EOT=3.1 nm) gate dielectric. The equivalent oxide thickness (EOT) of 3.1 nm is extracted from the accumulation capacitance.

Fig. 4.3. The current–voltage (*I*–*V*) characteristics of the pMOSFET with 50 nm $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed SiN (EOT=3.1 nm) gate dielectric. The inset shows the fitting of Fowler-Nordheim (FN) tunneling with an effective barrier height of 1.8 eV.

Fig. 4.4. The I_d–V_g and G_m characteristics of SiGe pMOSFET (W/L=10/0.5 μm) with N_2O-annealed SiN gate dielectric.

Fig. 4.5. The I_d–V_d characteristics of SiGe pMOSFET (W/L=10/0.5 μm) with N_2O-annealed SiN gate dielectric with various gate overdrives (V_g–V_t) from 0 to –2 V.

Fig. 4.6. The *C*–*V* characteristics of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric for various CVS conditions.

Fig. 4.7. The leakage current versus the stress time of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric under the constant voltage stress (CVS).

Fig. 4.8. The *C*–*V* characteristics of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric for various CCS conditions.

Fig. 4.9. The leakage current versus the stress time of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric under the constant current stress (CCS).

Fig. 4.10. The I_d degradation versus the stress time of HC and NBTI stressing for the

SiGe pMOSCAP with N_2O-annealed SiN gate dielectric.

Fig. 4.11. The G_m degradation versus the stress time of HC and NBTI stressing for the SiGe pMOSCAP with N_2O-annealed SiN gate dielectric.

Fig. 4.12. The threshold voltage shift (ΔV_t) versus the stress time for the SiGe pMOSCAP with N_2O-annealed SiN gate dielectric.

Fig. 4.13. The charge pumping currents of the devices before and after being stressed at HC and NBTI (RT) stressing.

Fig. 4.14. The enlargement of the charge pumping currents shown in Fig. 4.13.

Fig. 4.15. Comparison of the interface state generation (ΔN_{it}) which are extracted from the increase of charge pumping currents for the HC and NBTI (RT) stressing.

Fig. 4.16. The I_d degradation versus the stress time for the channel-hot-carrier stressing under various bias conditions of $V_g = V_d = -4.5$, –5, and –5.3 V.

Fig. 4.17. The G_m degradation versus the stress time for the channel-hot-carrier stressing under various bias conditions of $V_g = V_d = -4.5$, –5, and –5.3 V.

Fig. 4.18. The threshold voltage shift (ΔV_t) versus the stress time for the channel-hot-carrier stressing under various bias conditions of $V_g = V_d = -4.5$, –5, and –5.3 V.

Chapter 5

Fig. 5.1. SIMS profiles of the SiGe channel in-situ doped with phosphorus.

Fig. 5.2. The *C*–*V* characteristics of the pMOSFETs with different SiGe channel thickness.

Fig. 5.3. The I_d–V_g characteristics of the pMOSFETs with different SiGe channel

thickness.

Fig. 5.4. The I_d–V_d characteristics of the pMOSFETs with different SiGe channel thickness.

Fig. 5.5. The charge pumping currents of the the pMOSFETs with different SiGe channel thickness.

Fig. 5.6. The interface state density determined by the charge pumping technique and the subthreshold swing of pMOSFETs with different SiGe channel thickness.

Fig. 5.7. The gate-induced-drain-leakage (GIDL) of the pMOSFETs with different SiGe channel thickness.

Fig. 5.8. The junction leakage of the pMOSFETs with different SiGe channel thickness.

Fig. 5.9. The transconductance of the Si channel pMOSFET and the SiGe channel MOSFETs with different SiGe layer thickness.

Fig. 5.10. The effective hole mobility of the Si channel pMOSFET and the SiGe channel MOSFETs with different SiGe layer thickness.

Chapter 6

Fig. 6.1. TEM pictures of the cross sections for the HfO_2 films with different surface treatments. (a) HF-dipped. (b) NH3-annealed. (c) RTO-treated.

Fig. 6.2. The XPS spectra of the HfO_2 films with different surface treatments.

Fig. 6.3. The capacitance–voltage (*C*–*V*) characteristics of NMIS capacitors prepared by applying the three different surface treatment processes. The equivalent oxide thickness (EOT) was determined by measuring the

maximum accumulation capacitance.

Fig. 6.4. The plot of the leakage current as a function of gate voltage for each sample.

Fig. 6.5. The cumulative distribution of leakage currents at V_g = –2.5 V for capacitors formed by using the three different surface treatment processes.

Fig. 6.6. Normalized *C*–*V* curves with different sweeping voltages for each sample: (a) HF-dipped, (b) NH_3-annealed, and (c) RTO-treated samples. Initial inversion biases (V_{inv}) are +1, +2, and +3 V, and the accumulation bias (V_{acc}) is –3 V.

Fig. 6.7. The dependence of hysteresis width on the inversion bias (V_{inv}) during *C*–*V* measurement. The reciprocal voltage constant (R_v) is obtained from the slope of the fitted line.

Fig. 6.8. The plot of hysteresis as a function of the reciprocal of temperature. The activation energy (E_h) for each sample is ca. 0.092 eV.

Fig. 6.9. The plot of hysteresis as a function of the *C*–*V* measuring frequency.

Fig. 6.10. The plot of leakage current as a function of gate voltage as the temperature was varied from 20 to 125 ºC. (a) HF-dipped, (b) NH_3-annealed, and (c) RTO-treated samples.

Fig. 6.11. The Arrhenius plot of leakage currents at V_g = 1.0 V and V_g = 2.5 V. The activation energy (E_a) increases as the temperature decreases.

Chapter 7

Fig. 7.1. The schematic device structure of the advanced sub-100 nm SOI MOSFETs with strained layer channel, metal S/D, high-k gate dielectric,

and metal gate electrode.

Chapter 1

Introduction

1.1 An Overview of the Background and the Motivation

As predicted by the ITRS **[1]**, the thickness of the gate oxide should be unavoidably less than 1.5 nm for the purpose of gaining performance and eliminating deleterious short channel effects when the channel length of the CMOS devices continuously shrinks below 100 nm. With such thin gate oxide, the intolerable large direct tunneling current **[2]** and severe boron penetration **[3]** will become the most severe problems. Many techniques for introducing nitrogen into ultra-thin gate oxide have been demonstrated being capable of considerably alleviating these issues **[4]–[10]**. On the other hand, the velocity saturation **[11]**, ballistic effect **[12]–[15]**, and the increase of I_{off} leakage current **[16]** may eventually limit the driving capability and device performance with the gate length scaling to the sub-100 nm regime. Hence, the strained layer **[17]–[20]** are applied to be the device channel for further enhancing the performance of the deep sub-micron device because of the higher carrier mobility **[21]**, **[22]**. Moreover, the ultra-thin high-k gate dielectrics are recently paid more attention and extensively studied in order to further reduce the leakage current of the tunneling gate oxide **[23]–[26]**.

Therefore, we are interesting in electrical characteristics and reliability of the deep sub-micron MOSFETs fabricated with advanced technologies of ultra-thin nitrided gate oxide, strained SiGe channel, and ultra-thin high-k gate dielectrics.

1.1.1 MOSFETs with Ultra-Thin Nitrided Gate Oxide

It is well-known that the nitridation of thermal oxide has been studied for over three decades because of the higher dielectric constant and strength, smaller radiation-induced damages, and enhanced endurance under high-field stress, and numerously various techniques of nitridation have been published, such as oxidation of nitrogen-implanted silicon substrate **[27]**, thermal nitridation with N_2 annealing **[28]**, NH_3 annealing **[29]**, N_2O annealing **[30]**, **[31]**, and NO annealing **[32]**, **[33]**, JVD nitridation **[34]**, remote plasma nitridation (RPN) **[35]**, **[36]**, decoupled plasma nitridation (DPN) **[37]**, reoxidation of nitrided oxide **[38]**, Si_3N_4/SiO_2 (N/O) stack **[39]**, **[40]**. Many researches have been aggressively conducted in reducing the direct tunneling current and improving the boron penetration by incorporating nitrogen into the sub-2 nm gate oxide **[8]**, **[41]**, **[42]**. However, thermal nitridation process requires higher temperature to incorporate sufficient nitrogen concentration into the gate oxide **[4]**, and high process temperature makes device integration more difficult as the technology scales down continuously to the sub-100 nm regime.

On the other hand, device degradation by hot-carrier stressing is one of the most important reliability issues for short channel MOSFETs, because device characteristics will be degraded by interface-state generation and transconductance reduction **[43]**. For worse cases, hot-carrier stressing may damage gate oxide to cause oxide breakdown **[44]**. Although the improvement of hot-carrier reliability achieved by nitrided oxide has been reported **[45]–[47]**, controversial issues are also arisen. Nitrogen incorporation induced positive fixed oxide charges and electron traps are the main concerns for nitrided oxides. Carrier injection and trapping in the gate oxide and transconduction degradation by Coulomb scattering make the hot-carrier degradation still be a significant reliability issue for devices with ultra-thin nitrided gate oxide **[48]**,

[49]. In addition, the low-frequency flicker noise has been regarded as an important consideration in analog and RF device applications **[50]**, and it has also been reported to be another problem for the nitrided gate oxide **[51]**, **[52]**. Because the flicker noise is believed to be caused by the fluctuation in the number of carriers and/or in carrier mobility which are induced by electron trapping/detrapping through the oxide traps and the mobility scattering when electrons are transporting through the surface channel of MOSFETs **[53]**, the additional electron traps induced by the nitrogen incorporation may enhanced the noise level.

Therefore, for the deep sub-micron MOSFETs with ultra-thin nitrided gate oxides, the device degradation of hot-carrier stressing and the flicker noise characteristics should be further investigated.

1.1.2 Strained SiGe Channel MOSFETs

It has been demonstrated that the strained layer as the channel may dramatically improve the device performance because of the higher carrier mobility **[17]–[22]**. The strained SiGe channel device, especially for pMOSFET, is, however, more attractive since SiGe has higher bulk carrier mobility than Si **[11]**, the offset of valence band with respect to Si substrate leads to the quantum confinement effect of holes **[21]**, **[54]**, and the induced compressive strained in the SiGe channel would further enhance the channel hole mobility when the SiGe layer is directly on the Si substrate **[21]**, **[55]**. Moreover, the SiGe device has several attractive merits in device fabrication because of the capability of selective deposition on Si substrate, the completely comparable process with the conventional Si device, and the low activation temperature due to the high dopant activation rate **[56]**.

On the other hand, several drawbacks for the SiGe channel device have also been

proposed **[54]**, **[57]–[59]**. For example, the lattice mismatch between SiGe and Si interface may induce dislocations, the Ge segregation and atom-induced scattering may degrade the mobility, and lacking a high quality gate insulator for MOS applications. Hence, low temperature process and Si capping layer have to be developed for fabricating SiGe MOSFETs **[60]**. Additionally, ultra-thin silicon nitride (SiN) has been reported as the promising alternative of gate dielectric for the SiGe channel MOSFETs **[61]**. Although SiN film usually shows a considerable amount of fixed oxide charges, electron traps, and the interface states to degrade the device performance, N_2O-annealing has been proposed to improve the film quality and the interface **[62]**.

However, the device characteristics of the SiGe channel MOSFET with N_2O-annealed SiN gate dielectric have not been demonstrated yet so far. Therefore, for deep sub-micron MOSFET applications, the film quality of the ultra-thin N_2O-annealed SiN gate dielectric and the strained SiGe channel, the electrical characteristics, and the device reliability still need further extensive study.

1.1.3 Ultra-Thin HfO_2 Gate Dielectric

The high-k metal oxide insulators have been shown to be capable of significantly suppressing the gate leakage current for the same equivalent oxide thickness (EOT) with conventional SiO_2-based gate oxides because of their greater physical thickness. The high-k materials therefore have attracted considerable attention as the promising candidate for the ultra-thin gate dielectrics when the gate oxide thickness is scaled down to below 1.5 nm, such as TiO_2 **[63]**, Ta_2O_3 **[64]**, Al_2O_3 **[65]**, ZrO_2 **[66]**, HfO_2 **[67]**, La_2O_3 **[68]**, Y_2O_3 **[69]** and Pr_2O_3 **[70]**. Among these candidates, HfO_2 not only have relatively high dielectric constant and wide band gap **[71]** but also displays

impressive thermal stability when it directly contacts with the silicon substrate **[72]**. Therefore, HfO_2 film seems to be a good alternative gate dielectric for the generation of sub-1.5 nm gate oxide, and the excellent electrical properties have also been demonstrated **[73]**. However, the formation of the interfacial layer and the degradation of mobility are still the challenging issues of the MOSFETs with HfO_2 gate dielectric, and recently the Hf silicate and nitrogen incorporation are extensively studied to overcome these issues **[74]–[76]**. Moreover, oxide traps existing in high-k gate dielectrics have been demonstrated as another concerning issue because of the threshold voltage instability **[77]** and the reliability degradation **[78]**.

To improve the interface quality, pre-deposition surface treatment should be a viable approach and it may also suppress the formation of the interfacial layer. For example, surface nitridation can provide better thermal stability and reliability because of the excellent barrier for interfacial reaction and dopant diffusion and the effective reduction of leakage current **[79]**, and the surface oxidation can be an effective method for reducing the leakage current and improving the quality of the interface **[80]**. However, both techniques have disadvantages. Nitrogen incorporation may induce extra oxide charges in the gate dielectric to cause a shift in the flat-band voltage. On the other hand, the low dielectric constant of the forming SiO_2 layer may increase the EOT and then limit the gate oxide scaling.

Therefore, the electrical characteristics of the ultra-thin HfO_2 gate dielectrics with different surface treatments have to be further investigated and compared.

1.2 Organization of the Thesis

Three main topics are investigated and discussed in this dissertation. First, the

effect of hot-electron-induced electron trapping on device reliability and the low-frequency flicker noise characteristics for the deep sub-micron nMOSFETs with ultra-thin nitrided gate oxides are investigated. Second, the device degradation mechanism and the channel thickness effect on device characteristics for the deep sub-micron strained SiGe channel pMOSFETs with ultra-thin N_2O-annealed SiN gate dielectric are studied. Third, the electrical characteristics of the ultra-thin HfO_2 gate dielectrics prepared using various pre-deposition surface treatments are compared and discussed. This dissertation is also divided into seven chapters.

In Chapter 1, a brief overview of the background and the motivation are introduced. Three main advanced technologies for deep sub-micron MOSFETs are reviewed and we also discuss the most important issues for each technology.

In Chapter 2, the hot-electron degradation of the 0.13 μm nMOSFETs with various ultra-thin gate oxides (EOT = 1.6 nm), including thermal oxide, Si_3N_4/SiO_2 stack, NO oxynitride, and plasma nitrided oxide, are investigated. Severe hot-electron degradations under both channel hot-electron and substrate hot-electron injections are observed for the nitrided oxide devices comparing with the thermal oxide device. We also found that the main mechanism responsible for the hot-electron degradation should be dominated by the electron trap generation rather than the interface state generation in the ultra-thin nitrided gate oxides.

In Chapter 3, we investigated the low-frequency flicker noise characteristics of the 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) gate oxides of thermal oxide, Si_3N_4/SiO_2 stack, NO oxynitride, and plasma nitrided oxide subjecting to the hot-carrier stressing and the occurrence of oxide breakdown. The nitrogen incorporation in the ultra-thin gate oxide may increase the noise level by introducing electron traps but improve the device immunity against the hot-carrier degradation in the flicker noise. Comparing with the thermal oxide device, moderate increase of the

noise level for the nitrided oxide devices is observed when oxides are suffering breakdown. We also found that the frequency index of the noise spectrum is varied with the gate bias and decreased by hot-carrier degradation and oxide breakdown.

In Chapter 4, we have fabricated the pMOSFETs with 50-nm thick strained $Si_{0.85}Ge_{0.15}$ channel and ultra-thin (EOT = 3.1 nm) N_2O-annealed SiN gate dielectric and investigated the device degradations of the hot-carrier and the negative-bias temperature-instability stressing. The excellent quality of the ultra-thin N_2O-annealed SiN gate dielectric is obtained. The experimental results indicate that the hot-carrier degradation is worse than the NBTI degradation and the channel hot-carrier stressing is the worst case for all kinds of reliability testing. We have also verified that the interface state generation should be the main mechanism responsible for the hot-carrier degradation while the electron trapping dominates the device degradation for the NBTI stressing.

In Chapter 5, we have fabricated the strained $Si_{0.85}Ge_{0.15}$ channel pMOSFETs with ultra-thin (EOT = 3.1 nm) N_2O-annealed SiN gate dielectric and different channel thickness of 5, 15, and 30 nm. We have found that the thickness of SiGe channel has a great impact on the device characteristics. The thinner SiGe channel devices have been demonstrated to have higher interface quality, better device performance, lower leakage current, and higher mobility than the 30 nm SiGe channel device.

In Chapter 6, we have investigated the electrical characteristics of ultra-thin HfO_2 gate dielectrics with various pre-deposition surface treatments, such as HF dipping, NH_3 surface nitridation, and rapid thermal oxidation. The NH_3 nitridation technique has been shown to be superior to other surface treatment techniques. The dependence of hysteresis on the initial inversion bias, temperature, and frequency are also investigated. The hysteresis width is found to be increased with increasing the initial inversion bias and decreased with the temperature, and it is insensitive to the

measuring frequency. The experimental results also indicate that the hysteresis width is exponentially dependent on both the initial inversion bias and the temperature and can be described by an empirical relationship in the form $C(T)\cdot\exp(R_v V_{inv})$. The trap-assisted tunneling is also verified as the dominant conduction mechanism of the ultra-thin HfO_2 gate dielectrics.

In Chapter 7, we conclude our results and summarize the main conclusions in a list, and the suggestions for further studies are also discussed.

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Chapter 2

Hot-Electron-Induced Electron Trapping in 0.13 μm nMOSFETs with Ultra-Thin (EOT = 1.6 nm) Nitrided Gate Oxide

2.1 Introduction

The incorporation of nitrogen into the gate oxide has become a viable approach to reduce the intolerably high standby power consumption and overcome boron penetration when the gate oxide of continues to scale down below 2 nm because it provides a physically thicker film with the same electrical equivalent oxide thickness (EOT) for reducing tunneling current and simultaneously suppressing the boron diffusion effectively **[1]–[4]**. In the past, a variety of techniques including thermal nitridation **[5]–[17]**, jet vapor deposition (JVD) nitride **[18]–[22]**, remote plasma nitridation (RPN) **[23]–[28]**, decoupled plasma nitridation (DPN) **[29]**, **[30]**, and stacked nitride/oxide **[31]–[40]** have been studied extensively and shown to be beneficial in alleviating the above-mentioned problems. Despite these encouraging results, however, the impacts of nitrogen incorporation on the long-term reliability characteristics of the fabricated devices are still controversial. Some groups have studied that the introduction of nitrogen did cause significant reliability degradation in terms of charge trapping **[41]–[45]** and hot-carrier immunity**[46]–[56]**, while the others asserted the improved robustness against hot-carrier degradation by employing various nitridation techniques **[8]**, **[57]–[69]**. In this study, we demonstrate that the

gate dielectrics of 1.6nm EOT with nitrogen incorporation in deep sub-micron nMOSFETs will become less robust against hot-electron striking even though it has been shown that the ultra-thin oxides in direct tunneling regime have better hot-carrier reliability for nMOSFETs **[70]–[74]**. Several nitrogen incorporation techniques are employed in this work, including stacked Si_3N_4/SiO_2 (N/O), NO annealing, and plasma nitridation. It is clearly observed that 0.13 μm nMOSFETs with ultra-thin nitrided gate oxides (EOT = 1.6 nm) depict much severe degradations under both channel hot-electron (CHE) and substrate hot-electron (SHE) injections as compared to the device with conventional ultra-thin gate oxide. Meanwhile, it is found that the main mechanism which is responsible for the hot-electron degradation should be dominated by the electron trap generation rather than the interface state generation in the ultra-thin nitrided gate dielectrics after the long-term hot-electron stressing.

2.2 Device Fabrication and Characteristics Measurement

After active region definition, wafers were split to receive various gate dielectric preparation recipes, including thermal oxidation (i.e., control), Si_3N_4/SiO_2 (N/O) stack, NO-annealed oxide, and thermal oxide with plasma nitridation. Thermal oxide was grown by wet oxidation in catalysis oxidation chamber at 800°C; Si_3N_4/SiO_2 stack was made of a 0.8-nm bottom thermal oxide at 800°C followed nitridation in a high-density remote helicon-based nitrogen discharge at 450°C and a 1.4-nm high-quality nitride film deposited by low-pressure chemical-vapor-deposition (LPCVD) using gas sources of SiH_4 and NH_3 at 800°C; NO-annealed oxide was achieved with annealing the pre-grown thermal oxide at 800°C in the NO ambient; Plasma nitridation was implemented with exposing the thermal oxide to a decouple

plasma source at 550°C, 20 mTorr, in N_2 ambient followed by rapid thermal annealing (RTA) at 1050°C for 10 seconds. All of these gate dielectrics were carefully designed to have the same equivalent oxide thickness (EOT) of approximately 1.6 nm, as identified by *C–V* measurements. After deposition and patterning of a 150 nm un-doped polysilicon film, arsenic dopants were implanted with the energy of 5 KeV for simultaneous gate electrode doping and shallow source/drain junction formation. For dopant activation, all wafers were annealed by rapid thermal annealing (RTA) in N_2 gas ambient for 30 sec. Subsequently, cobalt salicide, PSG, and metallization were performed to complete the device fabrication.

The current–voltage (*I–V*) characteristics were measured by using a Keithley 4200 semiconductor characterization system. Two hot-carrier stressing methods, i.e., CHE and SHE injections, were used for evaluating the device reliability. The indicators of reliability degradation are the reduction of driving current, $\Delta I_d/I_d$ at $V_g = V_d = 1$ V, and transconductance, $\Delta G_m/G_m$ at the peak value, as well as threshold voltage shift (ΔV_t). Moreover, the variation of interface states will be monitored by the Direct–Current Current–Voltage (DCIV) method before and after the devices being stressed at CHE and SHE injections.

2.3 Results and Discussion

2.3.1 *I–V* Characteristics

The results of gate leakage current for various ultra-thin gate oxides are shown in **Fig. 2.1**. Consistent with the previous reports **[26]**, **[28]**, **[31]**, **[36]**, **[75]–[83]**, the gate leakage currents are reduced for all gate oxides with nitrogen incorporation, and

both N/O stack and plasma nitrided gate dielectrics are almost one order of magnitude lower than that of the thermal oxide with the same EOT value of 1.6 nm. The reduction of leakage currents are due to the increase of physical thickness which is achieved by increasing the dielectric constant for the nitrided oxides **[84]**, **[85]**. **Figure 2.2** demonstrates the linear I_d–V_g characteristics for 0.13 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics. Obviously, we can see that all devices have an almost identical subthrethold swing (S ~ 81 mV/dec), and the threshold voltages are displayed slightly negative shifts for the nitrided oxide devices as compared to the thermal oxide counterpart because of the nitrogen-induced positive charges in the gate dielectrics **[30]**, **[38]**, **[47]**, **[52]**, **[65]**, **[67]**, **[86]–[91]**. From this viewpoint, NO nitridation technique is the worst because the largest shift of threshold voltage has been observed. In addition, the transconductance versus the gate overdrive (V_g–V_t) for all devices are shown in **Fig. 2.3**. With respect to the control device with thermal gate oxide, the devices with N/O stack and plasma nitrided gate dielectrics show slight peak degradation of G_m at low gate bias which is attributed to the loss of mobile inversion electrons caught by the additional traps and the consequent Coulomb scattering **[35]**, **[47]**, **[92]–[96]**. The transconductance is, however, enhanced at high gate voltage regime, which has been reported to be caused by several possible factors: high interfacial nitrogen concentration may induce residual tensile stress at the interface **[94]**, **[97]**, **[98]**, nitrogen incorporation at the interface may reduce the acceptor-like interface states near and above the conduction edge **[94]**, **[95]**, **[99]**, and the electron trapping at the interface traps may screen the surface scattering through Coulomb shielding **[35]**, **[95]**, **[100]–[102]**. On the other hand, for the device with NO oxynitride, the severe G_m degradation should be due to higher level of nitrogen pile-up near the bottom interface via NO annealing **[30]**, **[52]**, **[93]**, **[94]**, **[100]**, which can also explain the result revealed in **Fig. 2.2**.

2.3.2 CHE and SHE Stressing

For the deep sub-micron devices with conventional ultra-thin gate oxide, it has been shown that the worst hot-carrier stress condition switches from $V_g = V_d/2$ (maximum I_{sub}) to $V_g = V_d$ **[103]–[107]**, and the device degradation is also enhanced by the valence-band electron tunneling when the oxide thickness shrinks down to the direct tunneling regime **[105]**. For the 0.13 μm nMOSFETs with ultra-thin nitrided gate oxides, as shown in **Fig. 2.4**, similar flat curves of substrate current versus gate voltage (I_b–V_g) are also obtained, so the worst condition of $V_g = V_d$ was used to monitor the degradations of our devices for hot-carrier stressing. Although the interface state generation has been demonstrated to be the main cause of the hot-carrier degradation for ultra-thin gate oxide devices **[72]**, **[104]**, **[105]**, **[108]**, the situation is, however, quite different for the devices with ultra-thin nitrided gate dielectrics. **Figure 2.5** indicates that almost no degradation was observed for the thermal oxide device with an EOT value of 1.6 nm, and this result is consistent with the previous works **[70]–[74]**. On the other hand, a slightly larger increase of threshold voltage (ΔV_t = 6 mV) is presented even though almost unchanged subthreshold swing was also observed for the plasma nitrided oxide device after being stressed under $V_g = V_d$ = 1.8 V (CHE) for 10^4 seconds. According to the results that nitrided oxide is very resistive to the interface state generation **[47]**, **[49]**, **[52]–[54]**, **[57]–[59]**, **[62]**, **[63]**, **[67]**, we, then, speculate that the electron trapping should be the dominating mechanism of the hot-electron degradation for the ultra-thin nitrided oxide device. Moreover, **Fig. 2.6** displays that the gate leakage current of the plasma nitrided oxide is slightly decreased after the CHE stressing. This trend is opposite to the results shown in other works, in which the increase of gate current has been

demonstrated if the gate oxide and the interface are damaged **[74]**, **[106]**, **[108]–[115]**. Therefore, the reduction of gate leakage current is believed to be due to the local electric field lowering induced by the electrons trapped in the gate dielectric **[109]**, **[116]**.

Figure 2.7 depicts the ΔV_t and $\Delta G_m/G_m$ versus gate voltage as a function of substrate bias (V_{sub}) under SHE stressing for the 0.13 mm nMOSFET with plasma nitrided gate oxide. We can clearly see that only negligible degradation has been found even when the gate voltage is up to 2.6 V when V_{sub} was fixed at 0 V (i.e. constant voltage stress, CVS). For the case of SHE stressing under V_{sub} = –2 V, however, the ΔV_t as well as $\Delta G_m/G_m$ are significantly enhanced with the increase of gate voltage. Note that the channel of device is strongly inverted for all applied gate voltages ($V_g > V_t = 0.38$ V). Thus, the electron injection into the gate dielectric which degrades threshold voltage (positive shift) and transconductance should be dominated by the substrate bias rather than the gate voltage. These results imply that the degradation must be strongly related to the energy of electrons flowing through the gate dielectric because electrons will gain energy from the substrate bias injection. Interestingly, V_t and G_m degradations are shown in a similar trend which indicates that V_t shift and G_m reduction may be enhanced by the same degradation mechanism, i.e. the electron trapping in the gate dielectric. In addition, the shifts of threshold voltage as a function of substrate bias under SHE stressing for various gate dielectrics are shown in **Fig. 2.8**. It can be seen that nitrogen-incorporated gate dielectrics depict poorer immunity against SHE stressing. When the substrate bias becomes more negatively than –1 V, all but the control device with thermal oxide show a drastic increase in threshold voltages. These sudden increases in the threshold voltages imply that electron trapping should be the dominant mechanism which is responsible for the aggravated device degradation for all nitrided gate oxide devices. Based on the

discussion abovementioned, we illustrate a schematic band diagram and electron conduction path for the devices stressed at different bias conditions, i.e., constant voltage stress (CVS), channel hot electron (CHE) injection, and substrate hot electron (SHE) in **Fig. 2.9**. For conventional CVS, i.e. V_{sub} = 0 V, the channel electrons, i.e., cold carriers, have a higher probability to directly tunnel into the gate without entering the conduction band of the oxide when the thickness of gate dielectric lies in the direct tunneling regime (EOT = 1.6 nm in our cases). Therefore, only negligible stress-induced degradation has been observed when the gate voltage is lower than 2.6 V as shown in **Fig. 2.7**. When a larger gate voltage is applied, a small fraction of electrons in the high-energy tail may tunnel into the conduction band of the gate dielectric and cause the dielectrics damaged via interaction with the dielectric network. Since the kinetic energy of the electrons in the tail of the energy distribution will increase with increasing the substrate bias, the degradation becomes accordingly more apparent.

It has ever been reported that electron trapping will dominate the dielectric degradation instead of the interface state generation for the gate oxide with heavily nitridation **[41]**, **[52]**, **[57]–[59]**, **[62]**, **[117]**, **[118]**. The link of the electron trap creation to the nitrogen incorporation has also been investigated **[119]–[121]**. It was shown that the bonds of paramagnetic electron trap precursors introduced by the nitrogen incorporation can be easily broken by the impact of the high energy electrons to create the electron traps. Therefore, the presence of trapped electrons in the gate dielectric may not only reduces the gate leakage current by locally electric field lowering **[109]**, **[116]**, but also leads to threshold voltage shift. Meanwhile, transconductance will also be degraded due to the loss of channel electrons and the consequent Coulomb scattering with capturing electrons within the gate dielectric **[35]**, **[47]**, **[92]–[96]**.

2.3.3 DCIV Measurement

In despite of the fact that charging pumping method is a very useful technique to characterize the interface quality, high gate leakage in the direct tunneling regime will cause the charge pumping measurement become unreliable, and more complicate analyzing approaches have to be developed **[122]–[126]**. Another technique for evaluating the interface quality as the Direct-Current Current-Voltage (DCIV) method has also been proposed **[127]–[134]**. Because gate bias of the DCIV measurement is biased at near the flat-band condition, the gate leakage component can be suppressed. **Figure 2.10** is the cross-sectional view of the four-terminal DCIV measurement. Regarding the source, substrate, and drain of the nMOSFET as the emitter, base, and collector of the parasitic BJT structure, respectively, the base current, I_b, is mostly attributed to the recombination current with the recombination process through the defects in the base region and the interface traps. Therefore, if excess interface states are generated during device stressing, I_b will be significantly increased with varying the slope as displayed in the curve-#2, 3, and 4 for different distribution situations. The base currents as a function of collector-base voltage (V_{cb}) measured by the four-terminal DCIV method of the 0.13 μm nMOSFETs with an EOT of 1.6 nm plasma nitrided gate oxide before and after CHE and SHE stressing for 10^4 seconds are shown in **Fig. 2.11**. Note that the slopes of I_b–V_{cb} curves are almost unchanged for both CHE and SHE stressing except slightly increase of the base currents. The parallel increase of I_b should be due to raising the effective gate bias by electron trapping in the gate dielectric after the hot-electron stressing. Again, we confirm that the mechanism responsible for the degradation is the electron trap generation rather than the interface state generation. As discussed previously, we speculate that all of these

degradations are closely related to the precursors of paramagnetic electron traps formed by nitrogen incorporation in the ultra-thin nitrided gate oxides even though the thickness is in the direct tunneling regime.

2.3.4 Device Lifetime

Figure 2.12 is the degradation of threshold voltage versus stress time for the SHE injection biased at V_g = 2.2 V and V_{sub} = –1.5 V for 10^4 seconds. Considering the device lifetime defined as ΔV_t = 10 mV, obviously the thermal oxide device has superior reliability lifetime than all devices with nitrded gate oxides. **Figure 2.12** also shows that the ΔV_t exhibits a power law dependence on the stress time, and the exponent number, n, is extracted to be approximately 0.3 for all devices. Consistent with previous reports **[60]**, **[135]–[138]**, it reveals that charge trapping should dominate the hot-carrier degradation for a smaller exponent (0.15–0.3) is obtained. On the other hand, 0.13 μm nMOSFETs with nitrogen-incorporated gate dielectrics also display their lifetimes are more than two orders of magnitude lower than the counterpart with thermal gate oxide after CHE stressing are shown in **Fig. 2.13**. For ten-year device operation, the optimum operating voltage could be as high as 1.5 V for the device with thermal oxide. By comparison, all of the nitrogen-incorporated devices show a lower operating voltage of only about 1.3 V. Consequently, these results clearly indicate that deep sub-micron nMOSFETs with ultra-thin nitrided gate oxides would be more vulnerable to the hot-electron-induced electron trapping in the gate dielectric as considering the long-term reliability issues. However, both **Fig. 2.12** and **Fig. 2.13** depict that plasma nitrided oxide has superior hot-carrier reliability than the nitride/oxide stack and the NO oxynitride gate dielectrics. Therefore, plasma nitridation will be concerned as the most promising technique of forming the

ultra-thin nitrided gate oxide for the sub-100 nm device applications.

2.4 Summary

Although nitrogen incorporation into ultra-thin gate oxide could reduce gate leakage current effectively, the nitrided oxide will introduce the positive oxide charges to cause threshold voltage shift and transconductance degradation. Moreover, the nitrided oxides result in enhanced hot-electron-induced device degradations of the significant threshold voltage shift, the transconductance degradation, and the drain current reduction comparing with the conventional thermal gate oxide. In this study, we have also found that electron trap generation rather than the interface state generation should be the main hot-electron degradation mechanism for the deep sub-micron devices with ultra-thin nitrided gate oxide because of the observed results of the positive shift of threshold voltage, the insignificant variation of subthreshold swing, the reduction of gate leakage current, no significant slope changes of the I_b-V_{cb} curves for DCIV measurement, and a small exponent value (n ~ 0.3) of the ΔV_t versus stress time plot. Therefore, the hot-electron-induced electron trapping in the ultra-thin nitrided gate oxide could eventually become a severe long-term reliability concern (CHE and SHE) for the sub-100nm technologies, and the plasma nitridation has be shown to be the most promising technique for the ultra-thin nitrided gate oxide applications.

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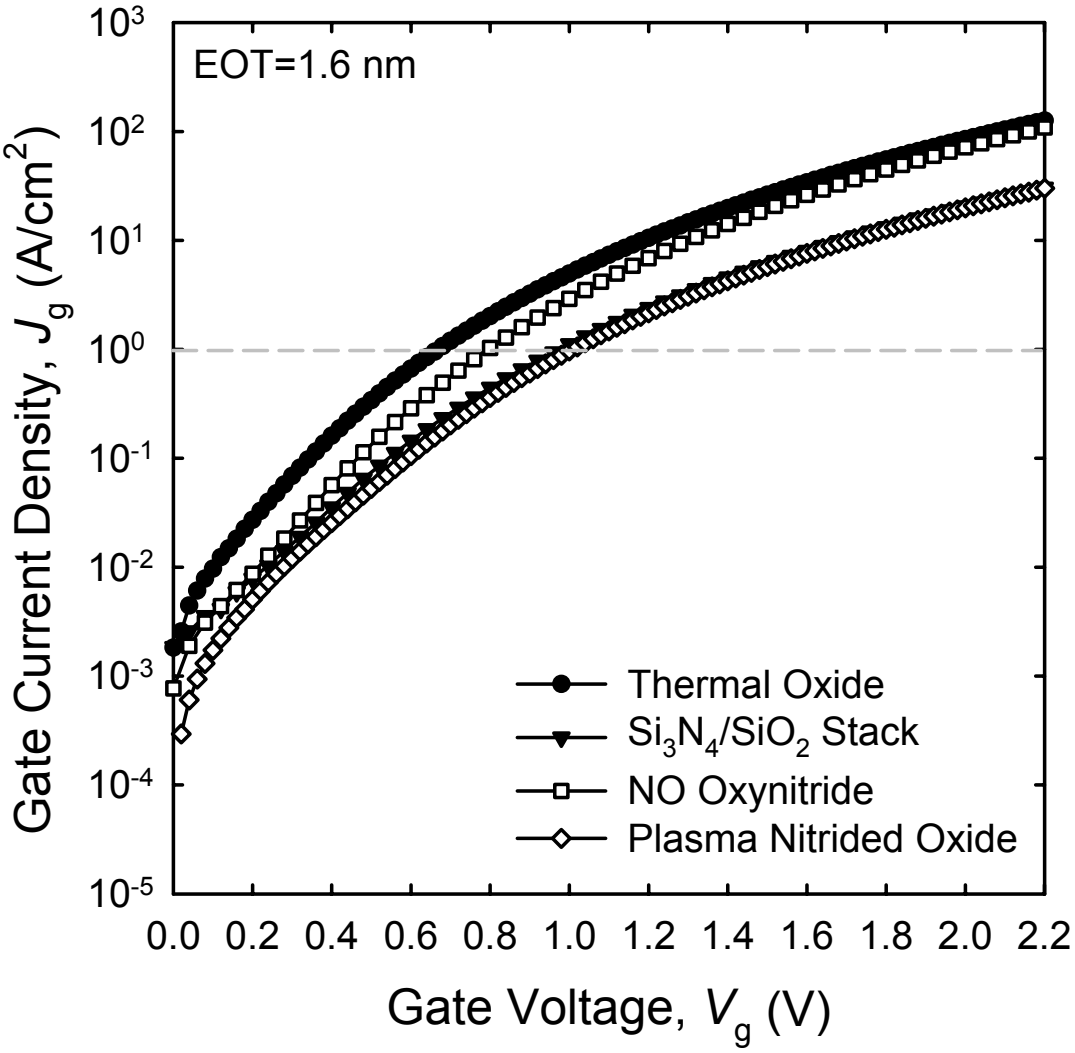


Fig. 2.1. Gate current densities as a function of gate voltage for four different gate dielectrics, and all devices have the same equivalent oxide thickness (EOT) of 1.6 nm.

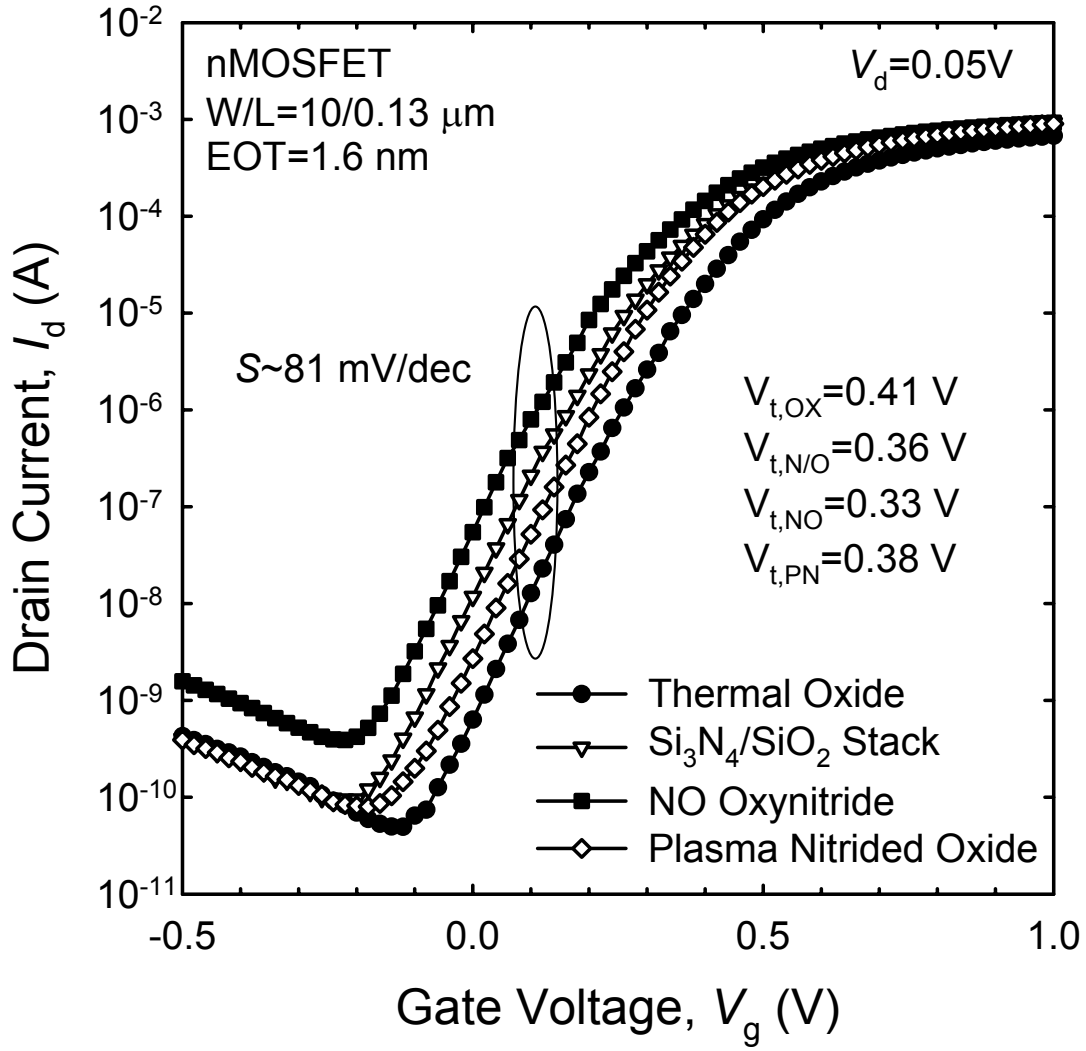


Fig. 2.2. Linear (V_d = 0.05 V) I_d–V_g characteristics of nMOSFETs (W/L = 10/0.13 μm) with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

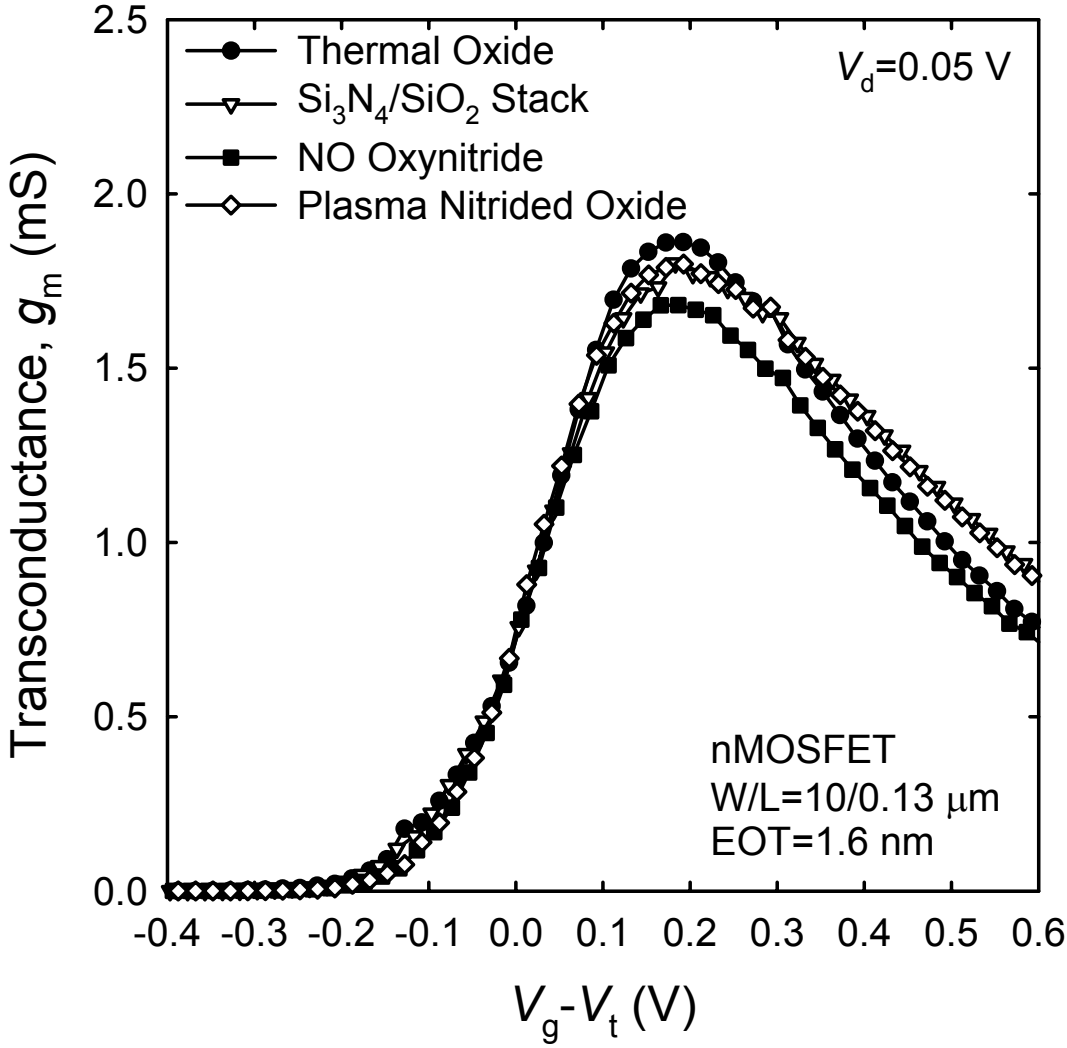


Fig. 2.3. Transconductance versus gate overdrive ($V_g - V_t$) of nMOSFETs (W/L = 10/0.13 μm) with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

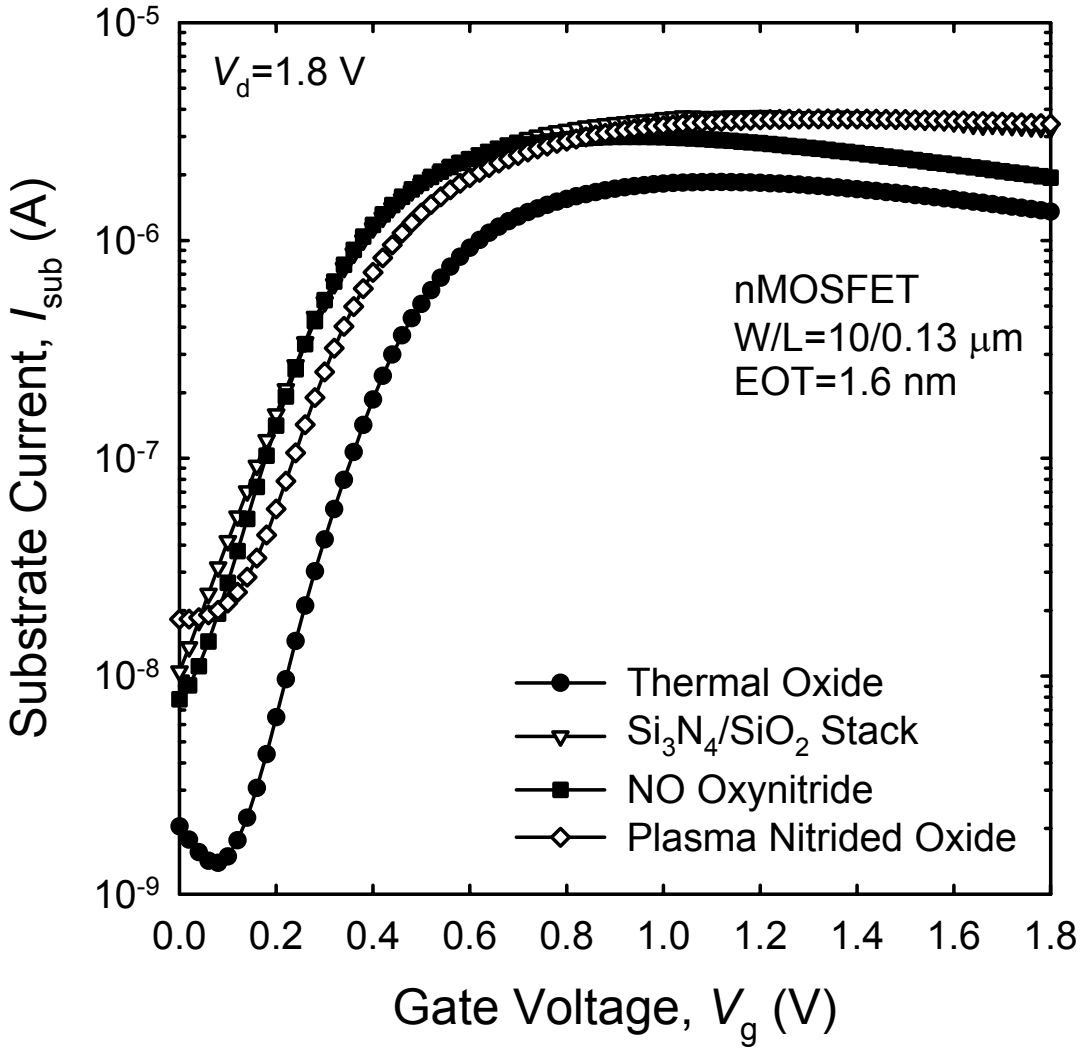


Fig. 2.4. Substrate current versus gate voltage of nMOSFETs (W/L = 10/0.13 μm) with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

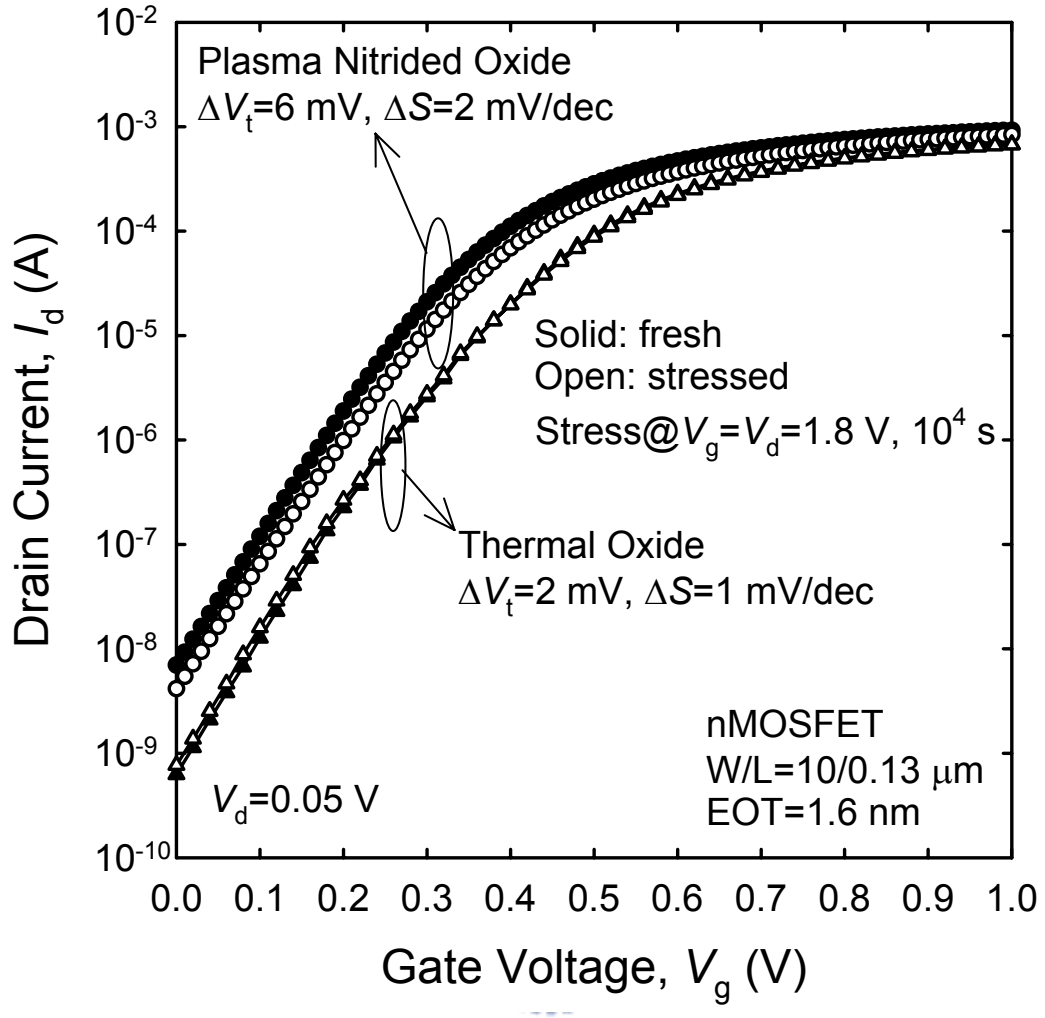


Fig. 2.5. Linear (V_d = 0.05 V) I_d–V_g characteristics of nMOSFETs (W/L = 10/0.13 μm) with an EOT of 1.6 nm thermal and plasma nitrided gate oxide before and after CHE (V_g = V_d = 1.8 V) stressing for 10^4 seconds.

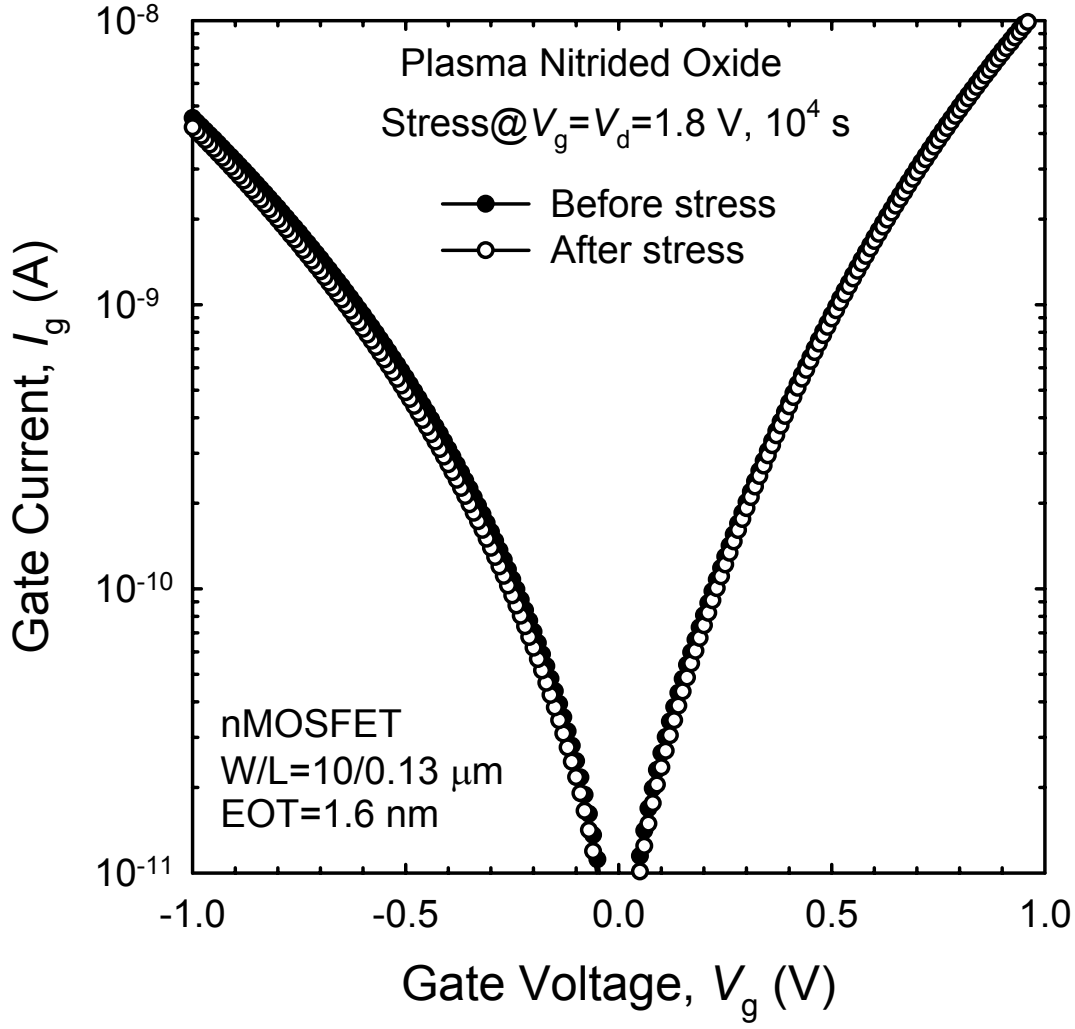


Fig. 2.6. Gate leakage currents of nMOSFETs (W/L = 10/0.13 μm) with an EOT of 1.6 nm plasma nitrided gate oxide before and after CHE (V_g = V_d = 1.8 V) stressing for 10^4 seconds.

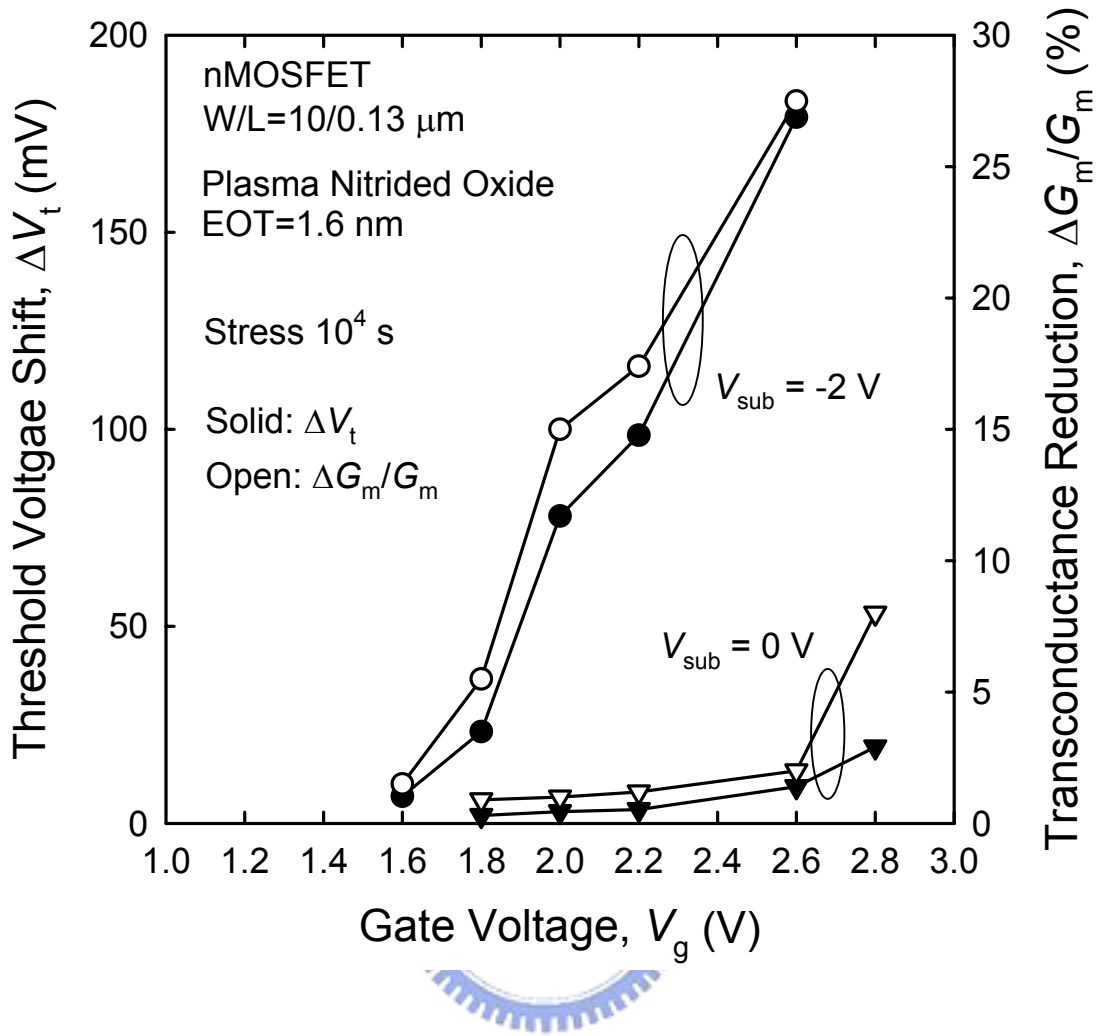


Fig. 2.7. Threshold voltage shift and transconductance reduction as a function of gate voltage with substrate biases of 0 V and –2 V for the 0.13 μm nMOSFET with an EOT of 1.6 nm plasma nitrided gate oxide after being stressed under SHE injection for 10^4 seconds. The source and drain are grounded.

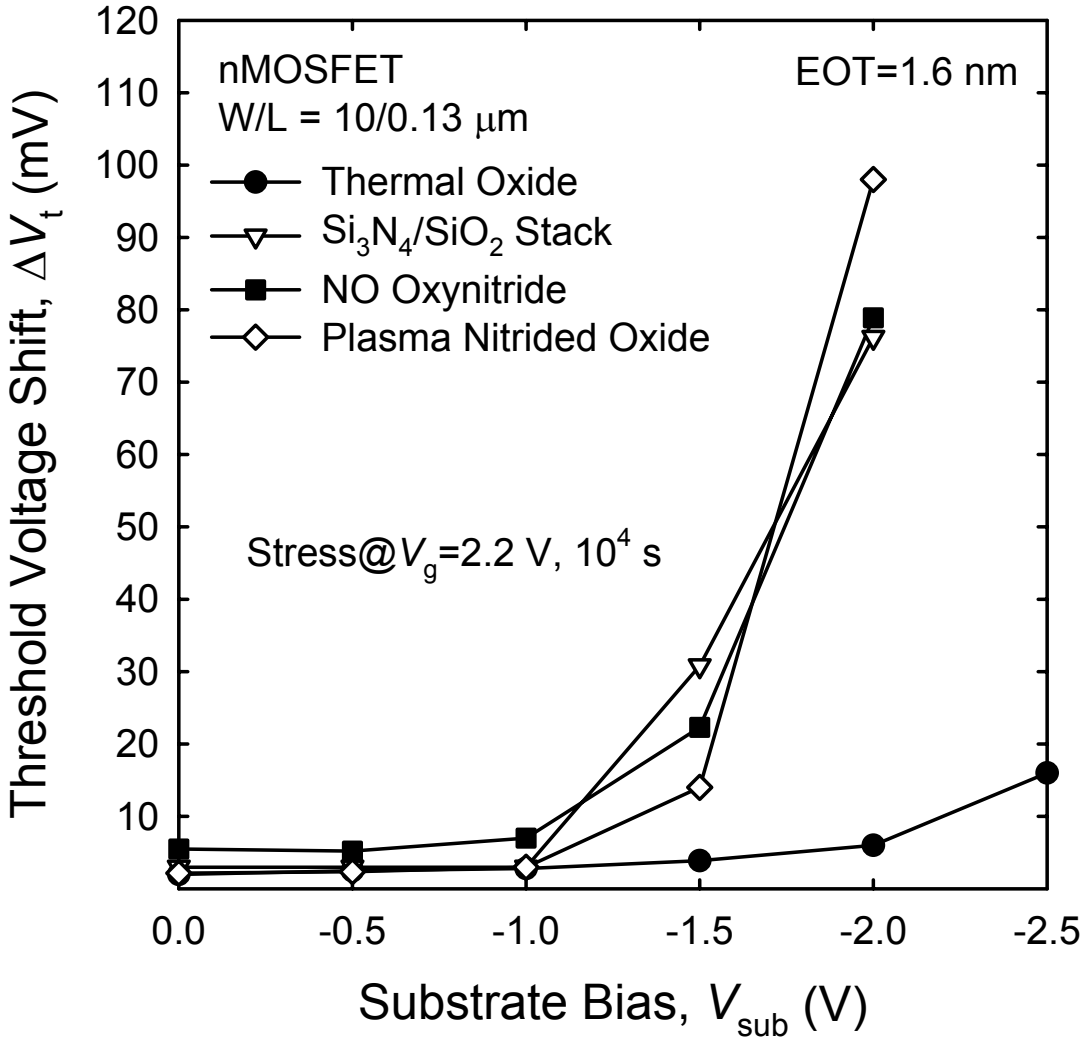


Fig. 2.8. Threshold voltage shifts as a function of substrate bias for the 0.13 μm nMOSFETs with various gate dielectrics (EOT = 1.6 nm) after SHE stressing for 10^4 seconds. The source and drain are grounded.

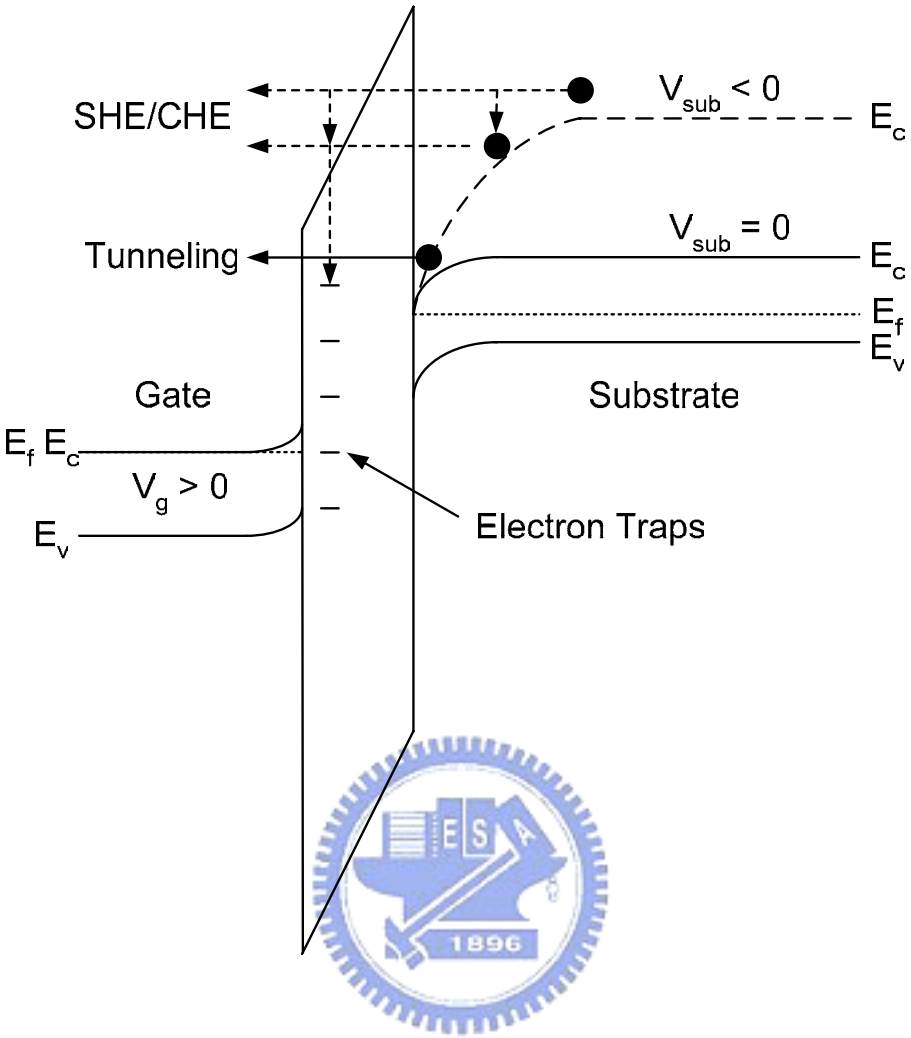


Fig. 2.9. Schematic band diagram and electron conduction path of n-channel MOSFET as stressed under different substrate bias conditions.

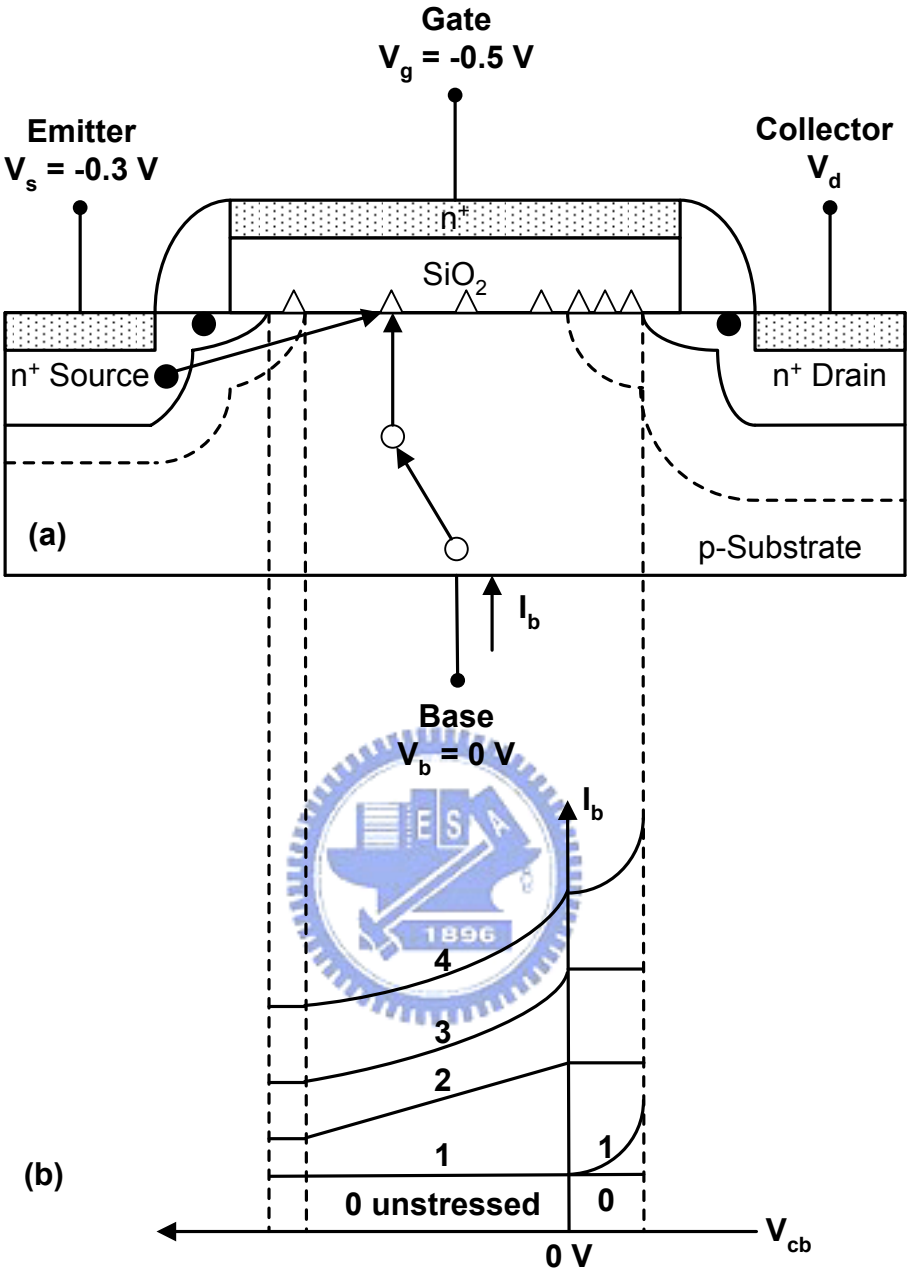


Fig. 2.10. (a) Cross-sectional view and measurement setting of four-terminal n-channel MOSFET used in the DCIV measurement. (b) Base current versus collector-base voltage (I_b–V_{cb}) for five interface trap distributions, curve-# (drain, channel, source): curve-0 (0, 0, 0), curve-1 (nonuniform, 0, 0), curve-2 (0, uniform, 0), curve-3 (0, nonuniform, 0), and curve-4 (nonuniform, nonuniform, 0).

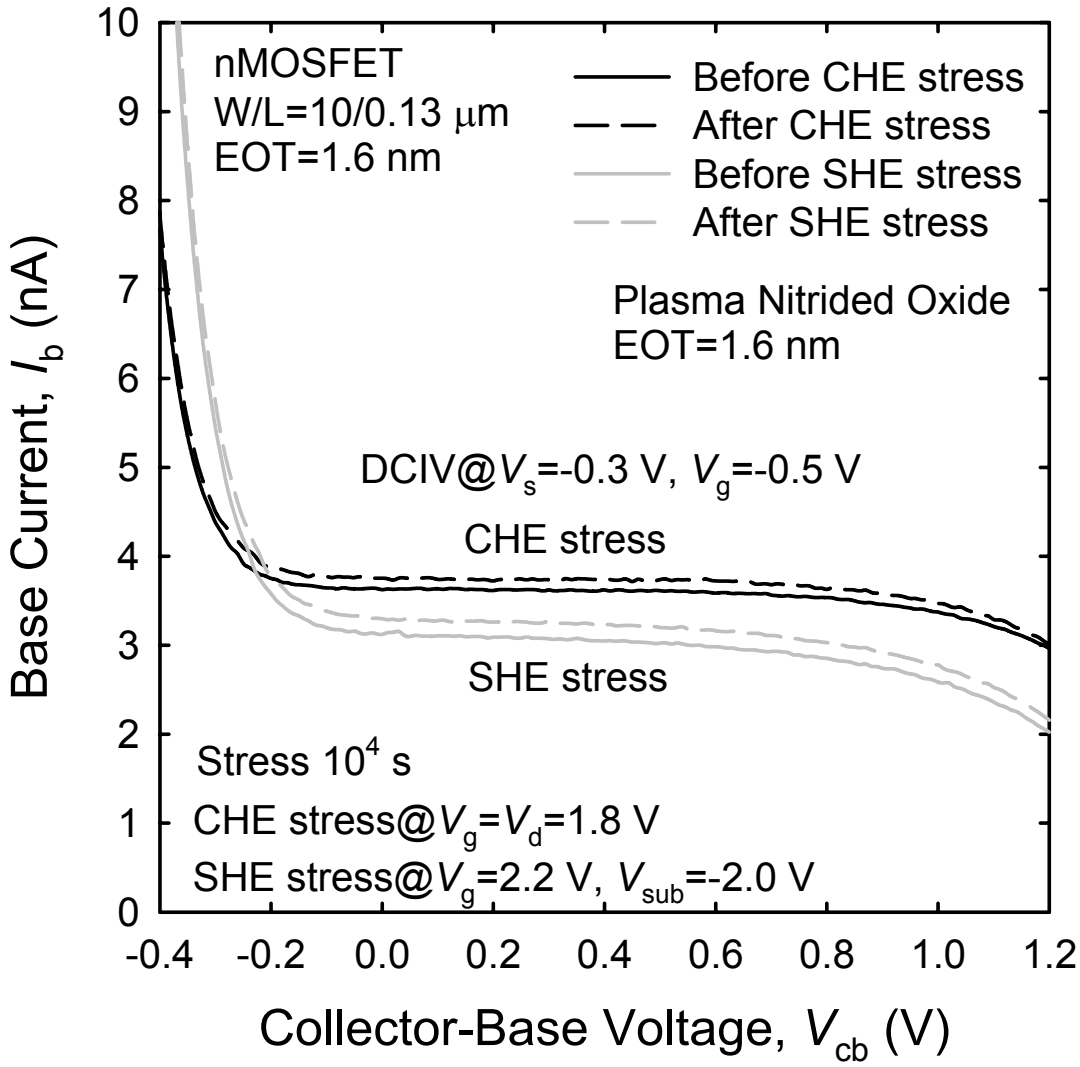


Fig. 2.11. Base currents measured by four-terminal DCIV method of the 0.13 μm nMOSFETs with an EOT of 1.6 nm plasma nitrided gate oxide before and after CHE and SHE stressing for 10^4 seconds.

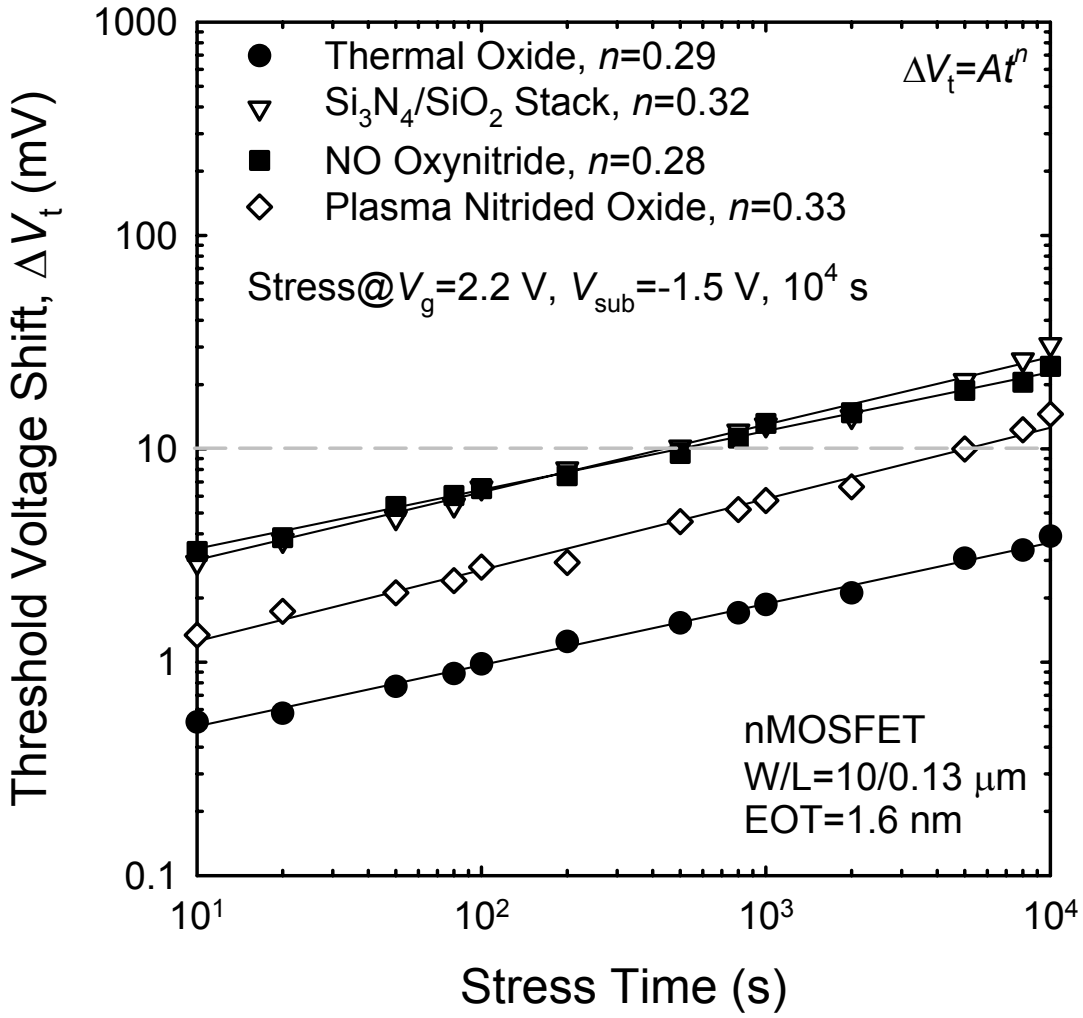


Fig. 2.12. Threshold voltage shift as a function of stress time of the 0.13 μm nMOSFETs with various gate dielectrics (EOT = 1.6 nm) under SHE stressing (V_g = 2.2 V, V_{sub} = –1.5 V) for 10^4 seconds. The source and drain are grounded.

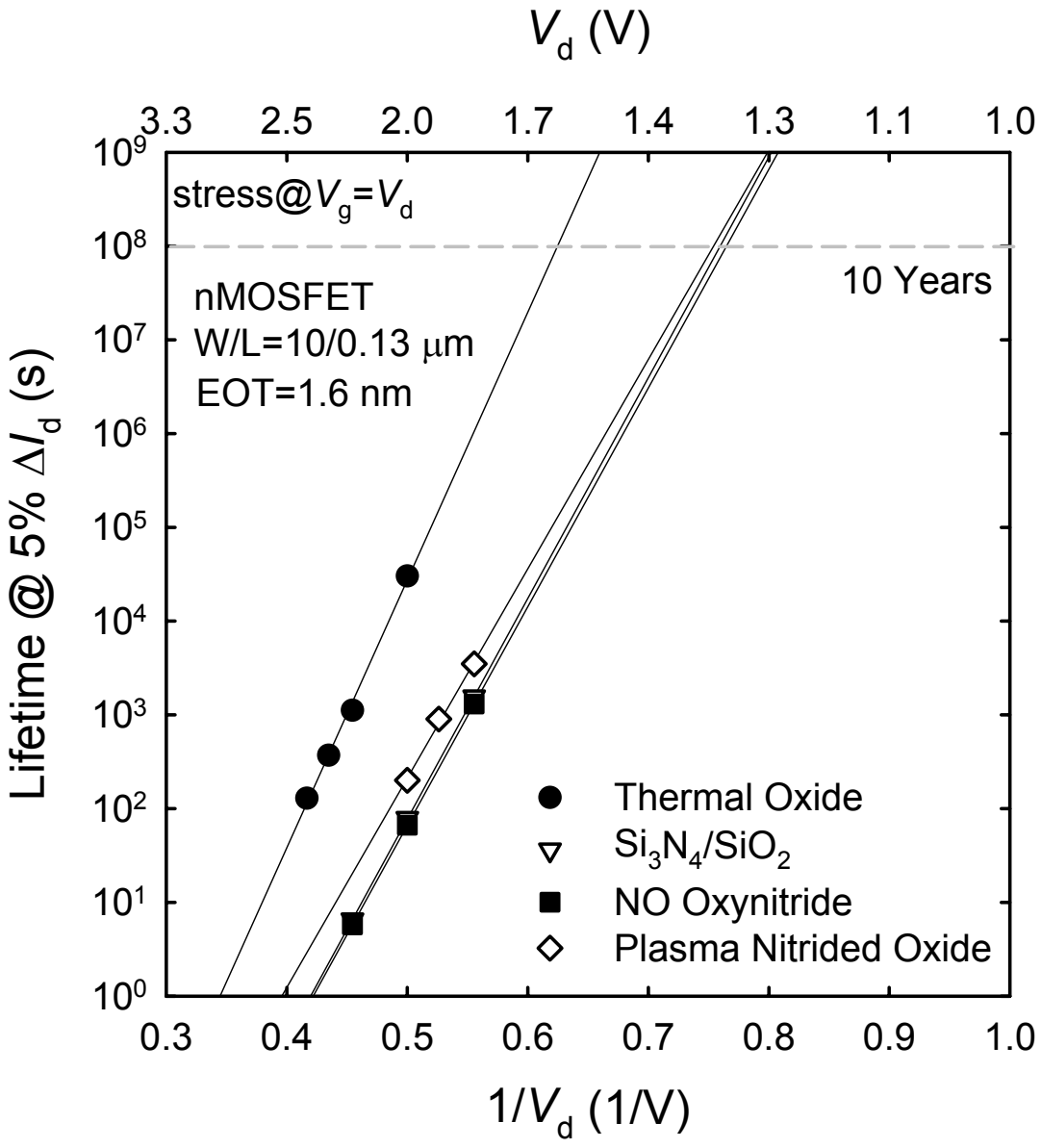


Fig. 2.13. Device lifetimes as a function of drain voltage for the 0.13 μm nMOSFETs with various gate dielectrics (EOT = 1.6 nm) under CHE stressing ($V_g = V_d$).

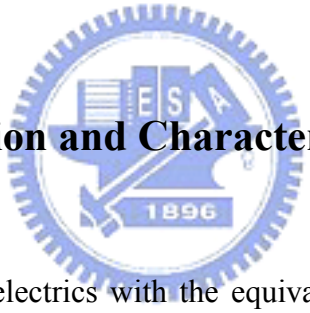
Chapter 3

Flicker Noise Characteristics of 0.15 μm MOSFETs with Ultra-Thin (EOT=1.6 nm) Nitrided Gate Oxide

3.1 Introduction

Nowadays, for aggressive progress of CMOS devices in analog and RF applications, the low-frequency (LF) noise of MOSFETs, i.e. the so-called flicker noise or 1/*f* noise, has been extensively studied **[1]**, **[2]**, because a low-frequency noise spectrum can be up-converted into a high-frequency (HF) spectrum around the carrier frequency. According to the previous reports, the flicker noise is believed to arise from the fluctuation in the number of carriers and/or in carrier mobility, which are induced by electrons trapping/detrapping through the traps and the mobility scattering when the carriers are transporting through the surface channel of MOSFETs **[3]**, **[4]**. Therefore, the flicker noise can act as a powerful vehicle in characterizing the quality of gate oxide near and at the SiO_2/Si interface and the reliability of devices **[5]**, **[6]** because its magnitude is intimately correlated to the surface roughness of channel **[7]**, the scaling of device geometry **[8]**, the plasma charging damage and breakdown (BD) in gate oxide **[9]**, **[10]**, and the hot-carrier (HC) induced degradation **[11]–[13]**. On the other hand, the nitrogen incorporation into gate oxide may induce the additional electron traps in the gate dielectric and reduce the mobility for a low gate bias **[14]**, **[15]**, and many research reports have indicated that the flicker noise has

become another potential problem for the nitrided gate oxides **[16]–[20]**. Hence, we investigated the characteristics of the flicker noise of 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) nitrided gate oxide subjecting to the hot-carrier (HC) stressing and the occurrence of oxide breakdown (BD). We found that the nitrogen incorporation in the ultra-thin gate oxide will increase the flicker noise by introducing electron traps but improve the device immunity against the hot-carrier degradation in the flicker noise. Moreover, the noise level is increased moderately for the nitrided oxide device comparing with the thermal oxide device when the oxides are suffering breakdown. We also found that the frequency index of the noise spectrum is dependent on the gate bias and will be decreased by hot-carrier degradation and oxide breakdown.



3.2 Device Fabrication and Characteristics Measurement

Various ultra-thin gate dielectrics with the equivalent oxide thickness (EOT) of 1.6 nm were formed after being defined the active region, including thermal oxidation, Si_3N_4/SiO_2 stack, NO-annealed oxide, and plasma nitrided oxide. After depositing and patterning of a 150 nm un-doped polysilicon film, arsenic dopants were implanted with the energy of 5 KeV for simultaneous gate electrode doping and shallow source/drain junction formation. All wafers were annealed by rapid thermal annealing (RTA) in N_2 gas ambient for 30 seconds for dopant activation. Subsequently, cobalt salicidation process was performed to improve the contact resistance. Finally, the process of standard back-end metallization completed the device fabrication.

The equivalent oxide thickness (EOT) of 1.6 nm was characterized by the capacitance–voltage (*C–V*) measurement with considering the quantum mechanical

effect. The low-frequency flicker noise measurement was performed by using the instruments set, including HP4156, HP35670A Dynamic Signal Analyzer, and BTA 9812 Noise Analyzer, before and after the hot-carrier stressing and the breakdown of gate oxide. Meanwhile, the output noise power spectrum density would be extracted in the low-frequency range between 10 Hz and 10 kHz.

3.3 Results and Discussion

The linear I_d–V_g characteristics of 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics, including thermal oxide, Si_3N_4/SiO_2 stack, NO oxynitride, and plasma nitrided oxide, are shown in **Fig. 3.1**. All devices depict an almost identical subthreshold swing (S) with a value of 80 mV/dec, and it implies that the qualities of these gate dielectric interfaces are similar. Meanwhile, obvious negative shift in threshold voltage (V_t) is observed for all of the devices with nitrided gate oxide. It is well-known that this tendency is closely related to the nitrogen-related positive charges. **Figure 3.2** shows the transconductances (g_m) of all devices versus the gate overdrive ($V_g - V_t$). It can be seen that the nitrogen incorporation not only results in the degradation of transconductance in low gate voltages which is caused by increasing the Coulomb scattering from additional oxide charges but also enhances the g_m in high gate voltages because of the less mobility degradation, and these results are consistent with the previous reports **[16]**. Hence, the largest V_t shift and the severe G_m degradation of the NO oxynitride device indicate that NO nitridation should introduce higher level of nitrogen into the gate dielectric than other nitridation techniques.

The results of gate voltage noise power spectrum (S_{Vg}) for all devices at the linear

operation ($V_g - V_t$ = 1.0 V and V_d = 0.1 V) are demonstrated in **Fig. 3.3**. Because S_{Vg} is obtained by S_{Id}/g_m^2, we can normalize the effects of various drain currents and transconductances for all devices. The reason why we characterize the flicker noise in linear region rather than in the saturation region is that the device can provide a uniform carrier distribution in the channel, and this condition simplifies the analysis of flicker noise. **Figure 3.3** depicts that once nitrogen has been incorporated into gate oxide, the increase of flicker noise can be clearly observed. It has been reported that nitrided oxide has higher noise level comparing with thermal oxide because oxide traps also contribute to the flicker noise in addition to the interface states **[18]**, and the noise level is strongly dependent on the techniques of nitridation **[16]–[20]**. This is attributed to the presence of the nitrogen-related interfacial electron traps in the gate dielectric at energies near the conduction band edge **[17]**. These traps can not only cause the fluctuation in the number of electrons in the channel by electrons trapping/detrapping through the traps but also modulate the scattering rate of mobility when they capture electrons **[19]**. Therefore, the devices with nitrided gate oxide show higher flicker noise than the thermal oxide counterpart. Besides, the frequency index of noise spectrum, γ, seems to be lowered with the amount of incorporated nitrogen, so the value of γ should be correlated with the electron traps. Similar speculation is also made in the previous study **[18]**. According to the results displayed in **Figures 3.1**, **3.2** and **3.3**, the plasma nitrided oxide has been shown to have superior oxide and interface quality over the Si_3N_4/SiO_2 stack and the NO oxynitride.

For the deep sub-micron device with thermal gate oxide, it has been demonstrated that the worst hot-carrier stress condition switches from $V_g = V_d/2$ to $V_g = V_d$ **[21]** and the interface state generation is the main cause of the hot-carrier degradation **[21]**, **[22]**. On the other hand, hot-electron-induced electron trapping is proposed to be the dominant degradation mechanism of the hot-electron injection for the ultra-thin

nitrided oxide devices **[23]**, **[24]**. Thus we stressed all devices at $V_g = V_d = 2.3$ V for 1000 seconds and investigated the effect of hot-carrier degradation on the flicker noise. **Figure 3.4** and **Figure 3.5** display the low-frequency S_{Vg} noise power spectra of thermal oxide and plasma nitrided oxide devices before and after hot-carrier (HC) stressing in linear and saturation operation modes, respectively. Obviously, the noise levels increase with the gate voltages for both devices whether operated in linear or saturation mode because of the increase of channel electrons with gate bias. The device with thermal gate oxide exhibits, however, significant increase of the flicker noise for hot-carrier degradation, but only slight changes are observed for the devices with plasma nitrided gate oxide. We believe that the drastic increase of noise for the thermal oxide device is attributed to the generation of the interface states and oxide traps **[21]**, **[22]**, **[25]**. While for the nitrided oxide device, the insignificant flicker noise variation arises from two factors. Firstly, it has been shown to have better hot-carrier immunity **[26]**. Secondly, the electron trapping in the nitrided gate oxide is the primary mechanism for hot-carrier degradation **[23]**, **[24]**, so the increase of electron traps which are available for generating flicker noise is not significant. Hence, the hot-carrier degradation contributes less impact on the flicker noise for the nitrided oxide device. Moreover, comparing results shown in **Fig. 3.4** and **Fig. 3.5**, the fresh noise level and the increment by hot-carrier stressing are higher in linear operation than in saturation operation for both devices. It is due to the fact that the channel is pinch-off away from the drain when device is in saturation mode. Only portion of electrons in the channel have probability to interact with interface and generate flicker noise, and the hot-carrier induced interface states and oxide traps has less impact on channel electrons because the damage region is only restricted to near the drain side for the hot-carrier stressing. Therefore, the flicker noise will become an important issue when device is operating in linear mode especially for analog and RF

applications **[27]**, **[28]**.

The variations of gate currents with stress time for all devices stressed at V_g = 3.3 V are shown in **Fig. 3.6**. Although the Si_3N_4 stack and the plasma nitrided oxide show similar breakdown characteristics to the thermal oxide, the NO oxynitride is easier to be breakdown than other counterparts. It is speculated to be caused by introducing more positive oxide charges and electron traps in the gate dielectric for NO nitridation. Once the oxide is breakdown, i.e. I_g increases abruptly, stressing process is interrupted immediately and then flicker noise measurement is performed. **Figure 3.7** is the results of low-frequency flicker noise before and after oxide breakdown (BD) for thermal oxide and plasma nitrided oxide devices with a stress voltage of V_g = 3.3V. When oxide breakdown is occurred, the noise level is observed to be increased moderately for the device with plasma nitrided oxide and it is significantly enhanced for the device with thermal oxide. In addition, the increment of noise level is higher for oxide breakdown comparing with the results of hot-carrier stressing. According to the model of the oxide breakdown **[29]–[31]**, a considerable amount of electron traps may be generated to construct the conduction path through the gate oxide. Therefore, more excess electron traps are contributing to the trapping/detrapping process for channel electrons and consequently enhance the flicker noise. Moreover, the frequency index of noise spectrum, γ, has been shown to be fluctuated with the gate bias and this observation is strong related to the electrons capturing/emission of the oxide traps **[18]**. Similar results are also obtained in our study which is demonstrated in **Fig. 3.8** for both the thermal oxide and plasma nitrided oxide devices before and after hot-carrier stressing and oxide breakdown. The frequency index is around 1.0–1.2 for fresh devices and it is decreased when devices are degraded either by hot-carrier degradation or even worse by oxide breakdown. Even though the variation of frequency index with gate voltage is also speculated to be corresponding to the

distribution of oxide traps **[18]**, we believe, however, further investigation is still needed for mechanism characterization with respect to the relationship between frequency index of noise spectrum and electron traps. Finally, according to previous results, the plasma nitrided oxide has been shown its potential for analog and RF applications with sub-100 nm devices because of the comparable noise level to thermal oxide, better immunity for enhancing flicker noise by hot-carrier degradation, and moderate increase of noise level after oxide breakdown.

3.4 Summary

We have found that the nitrogen incorporation in the ultra-thin gate oxide will not only induce the positive oxide charges to cause threshold voltage shift and transconductance degradation but also increase the flicker noise by introducing electron traps in nitrided oxide. It is due to the fact that the low-frequency flicker noise is mainly generated by trapping/detrapping of channel electrons with the interface states and the electron traps. However, nitrogen incorporation can improve the device immunity against the hot-carrier degradation in the flicker noise because the hot-electron-induced electron trapping may suppress the generation of flicker noise. Although a considerable amount of electron traps are created to enhance the flicker noise when oxide breakdown is occurred, moderate increase of noise level is observed when the nitrided oxide is suffering breakdown comparing with the thermal oxide. We also found that the frequency index of noise spectrum is varied with the gate bias and it is strong related to the oxide traps. Moreover, the frequency index will be lowered by hot-carrier degradation and even worse by oxide breakdown for both thermal oxide and nitrided oxide devices. For considering the characteristics of flicker

noise, the plasma nitrided oxide has been shown to be the most promising candidate of the ultra-thin nitrided oxide for sub-100 nm MOSFET devices in analog and RF applications.

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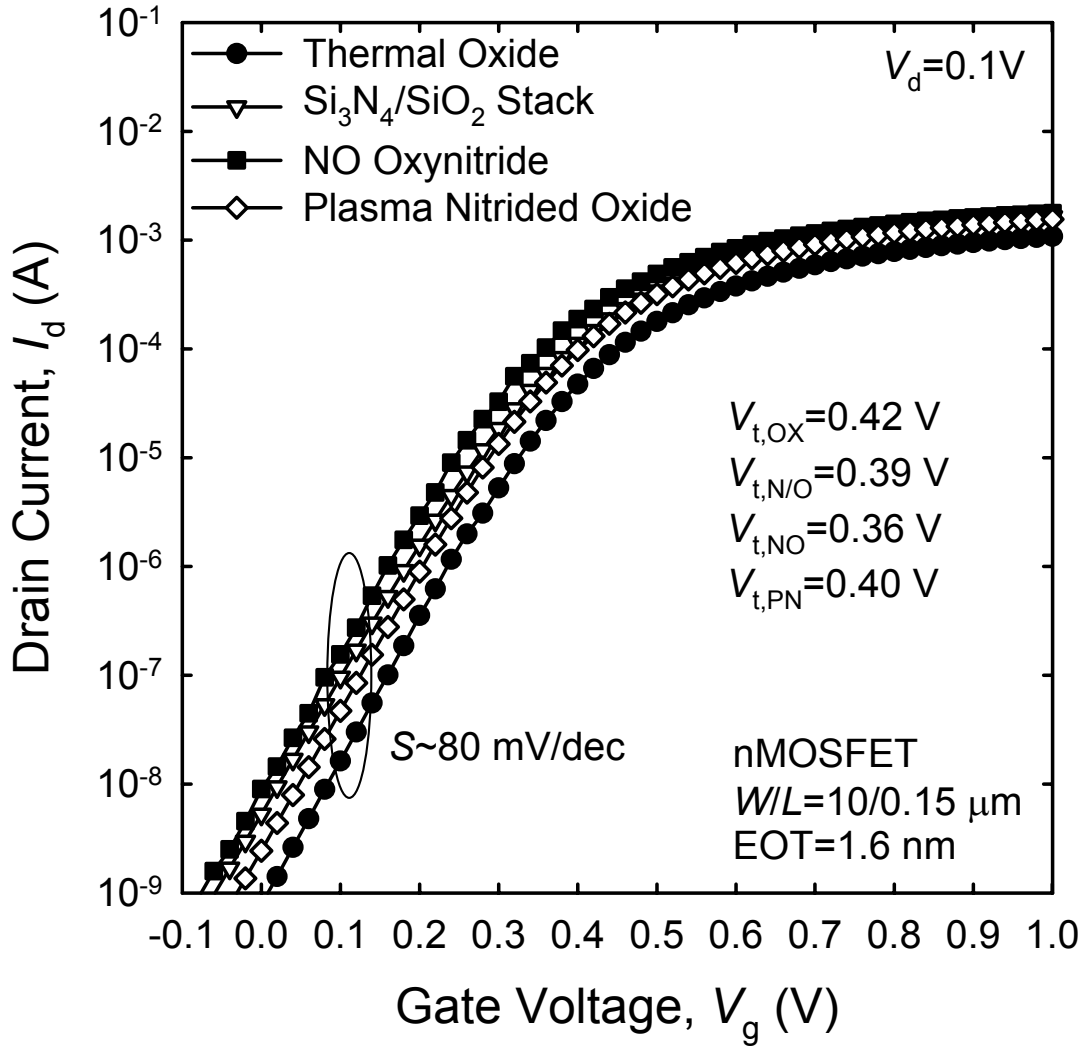

Fig. 3.1. Linear (V_d = 0.1 V) I_d–V_g characteristics of 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

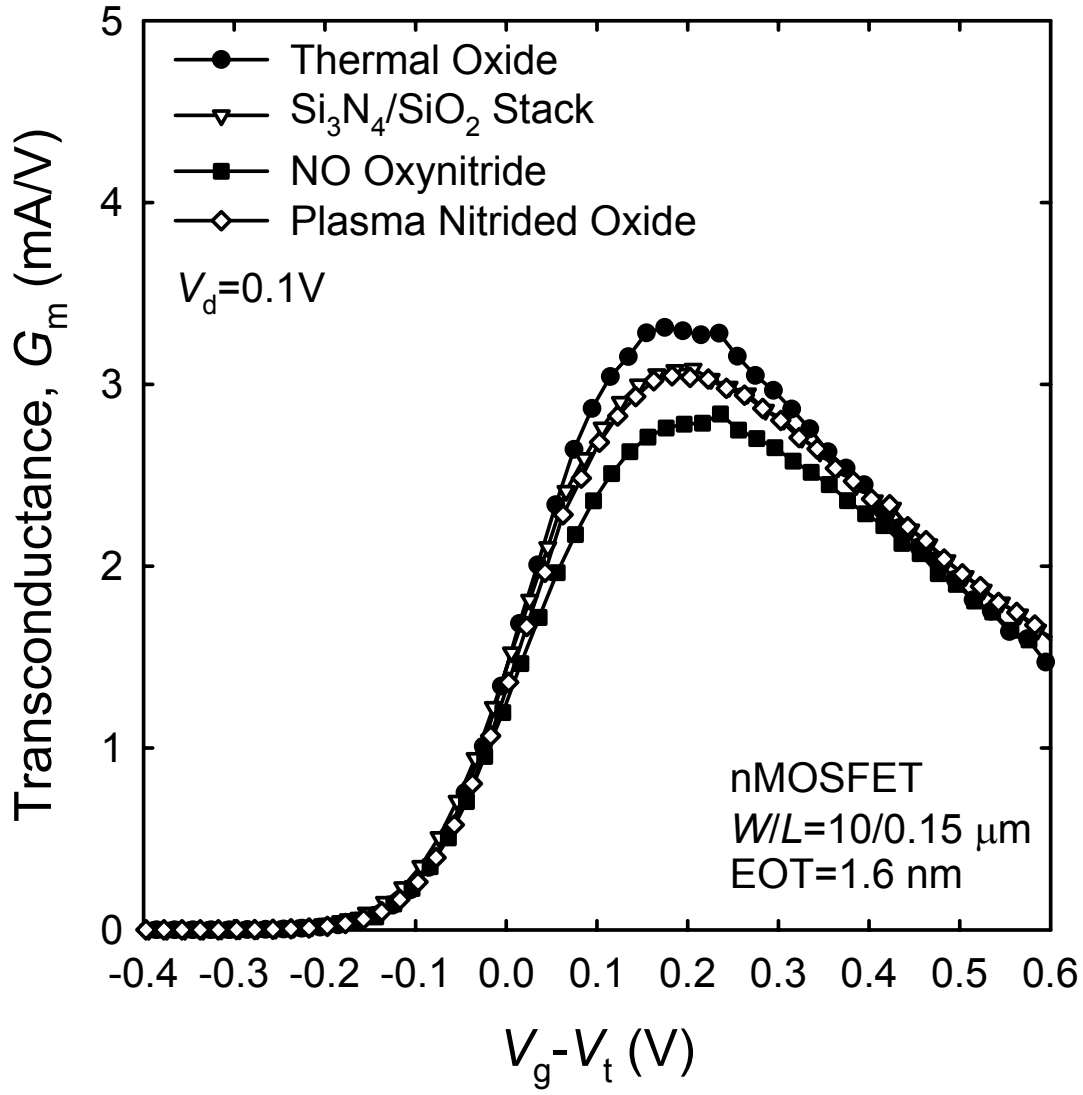

Fig. 3.2. Transconductance versus gate overdrive ($V_g - V_t$) of 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

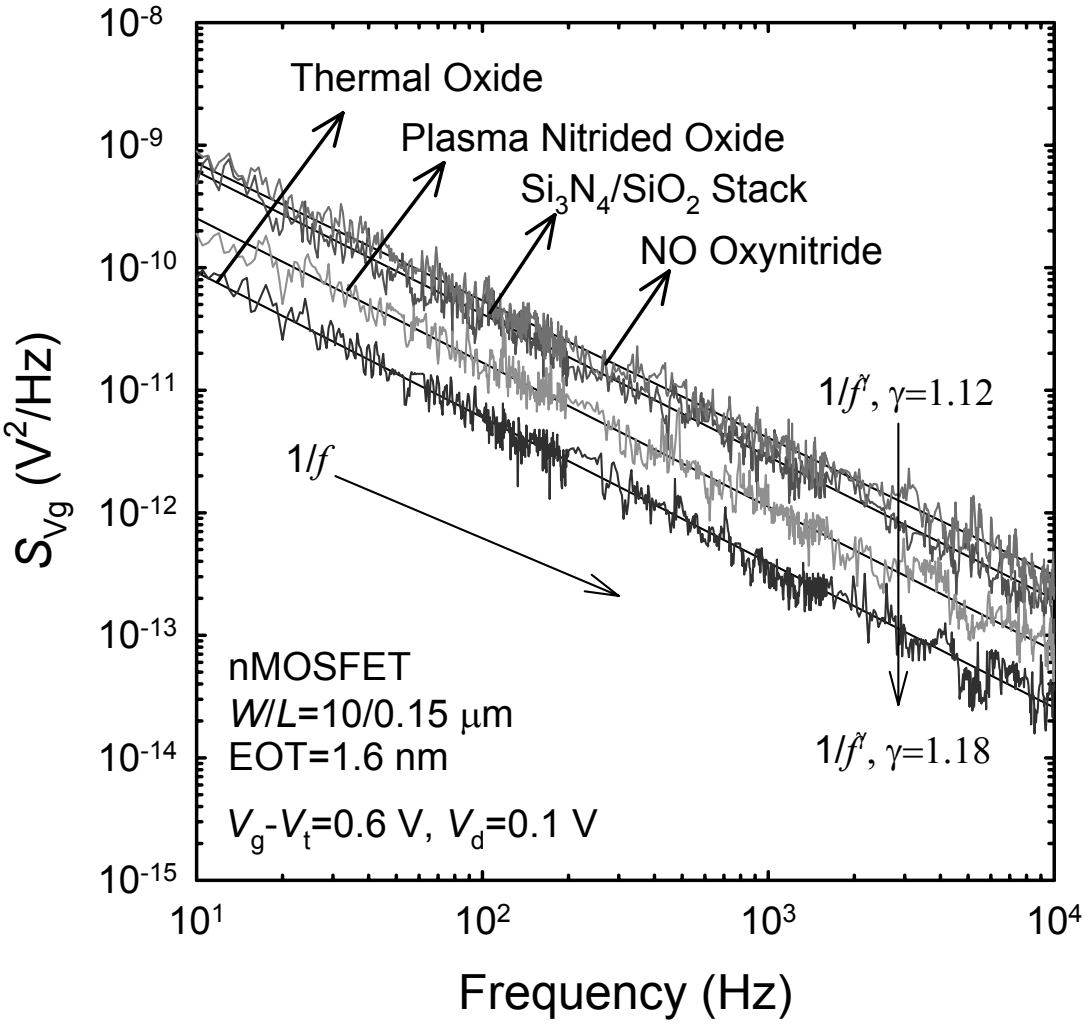

Fig. 3.3. Low-frequency S_{Vg} noise power spectra versus frequency at linear operation ($V_g - V_t$ = 1.0 V and V_d = 0.1 V) for 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics.

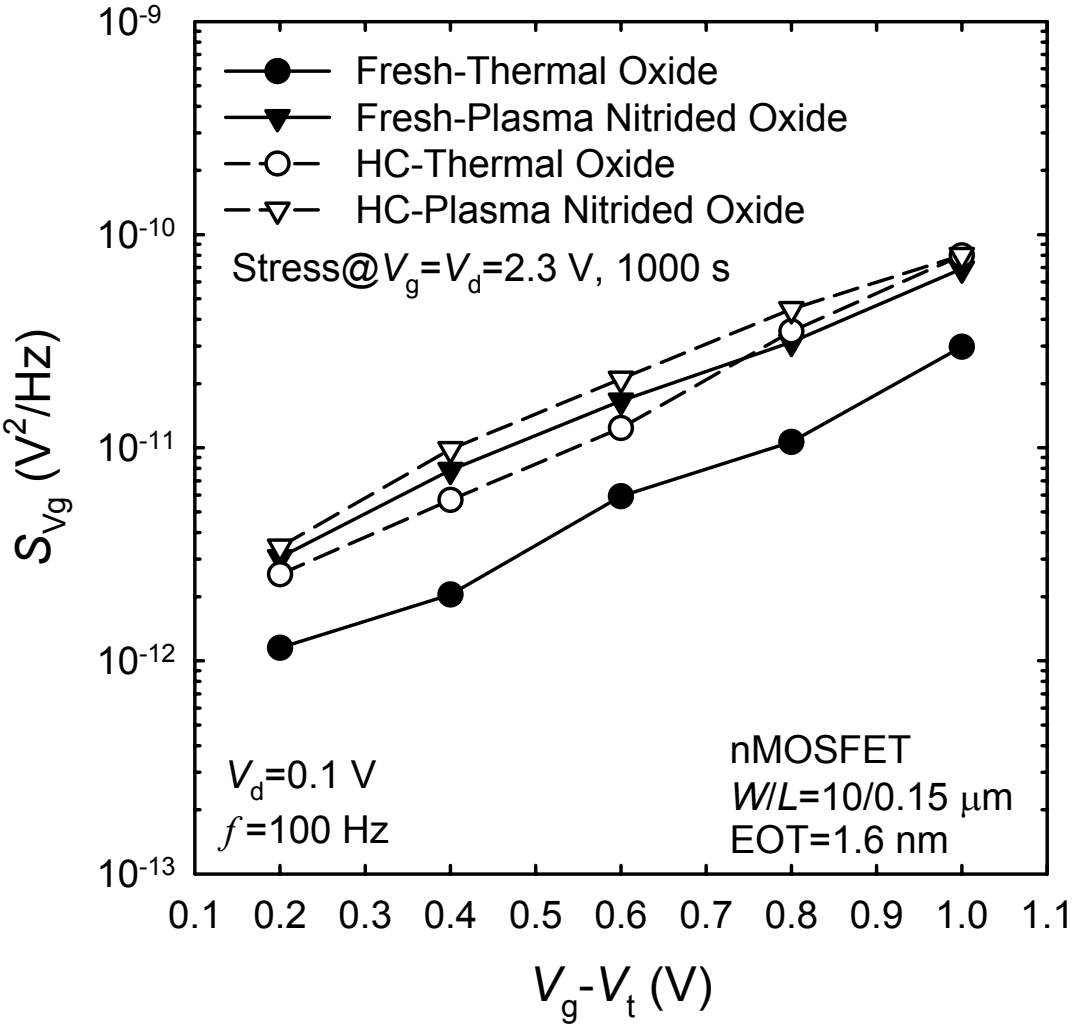

Fig. 3.4. Low-frequency S_{Vg} noise power spectra (f = 100 Hz) versus gate overdrives ($V_g - V_t$) at linear operation (V_d = 0.1 V) for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after hot-carrier stressing ($V_g = V_d$ = 2.3 V for 1000 seconds).

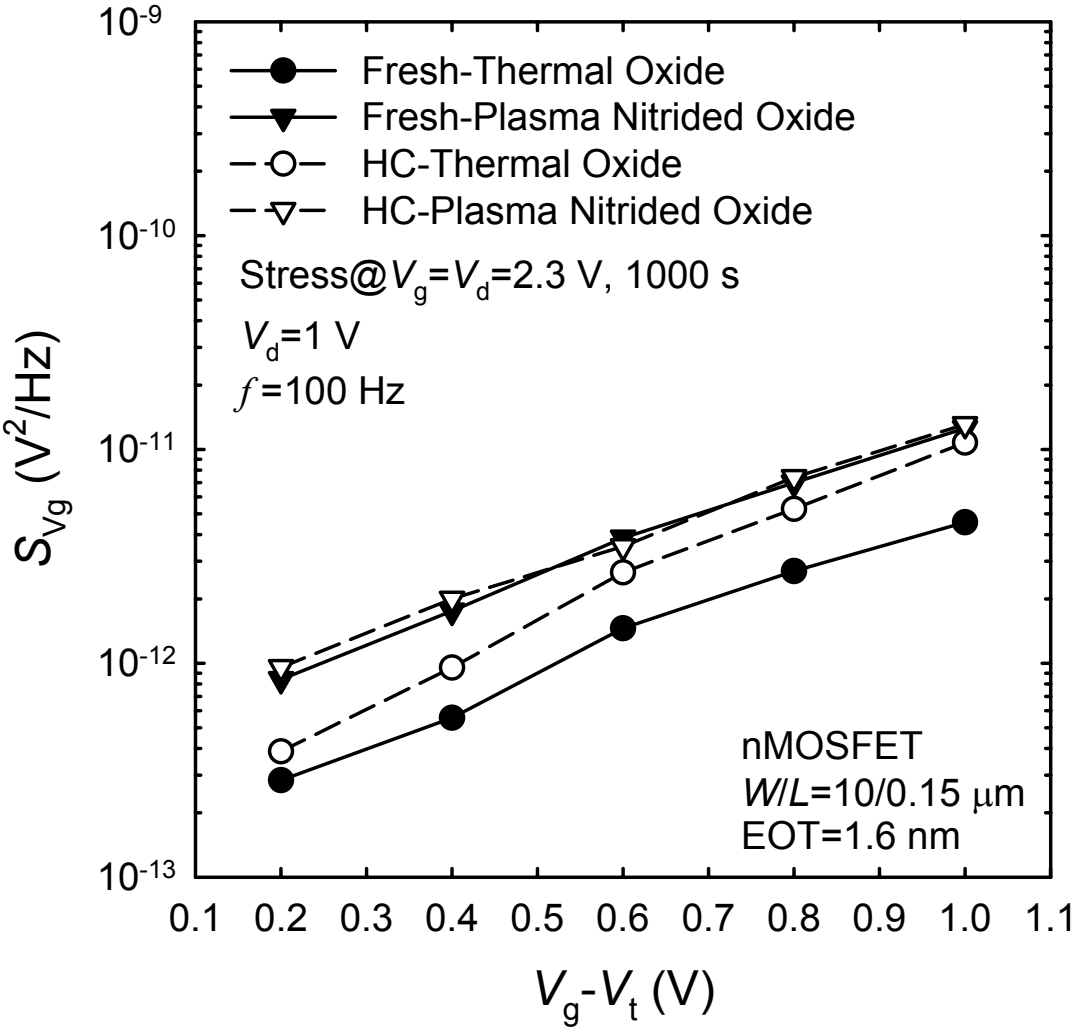

Fig. 3.5. Low-frequency S_{Vg} noise power spectra (f = 100 Hz) versus gate overdrives ($V_g - V_t$) at saturation operation (V_d = 1 V) for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after hot-carrier stressing ($V_g = V_d$ = 2.3 V for 1000 seconds).

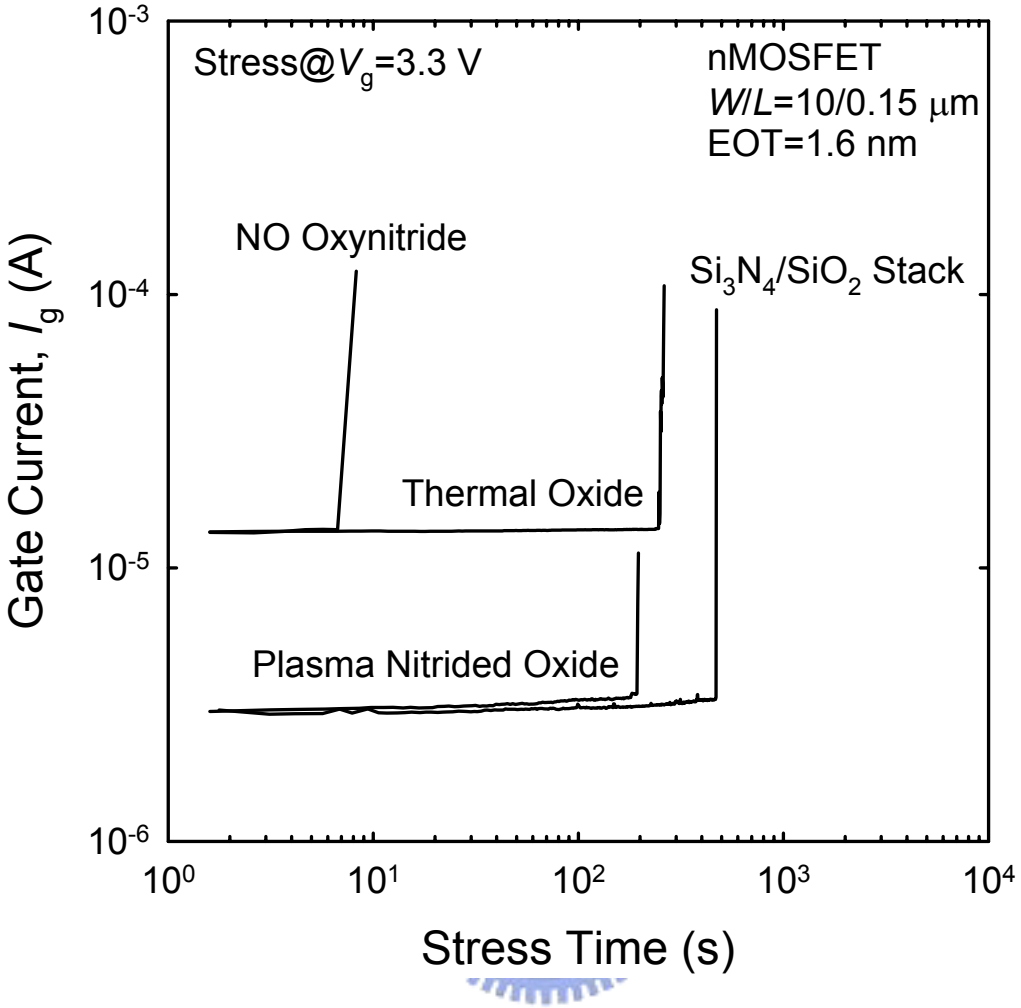

Fig. 3.6. Gate currents versus stress time for 0.15 μm nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate dielectrics stressed at V_g = 3.3 V.

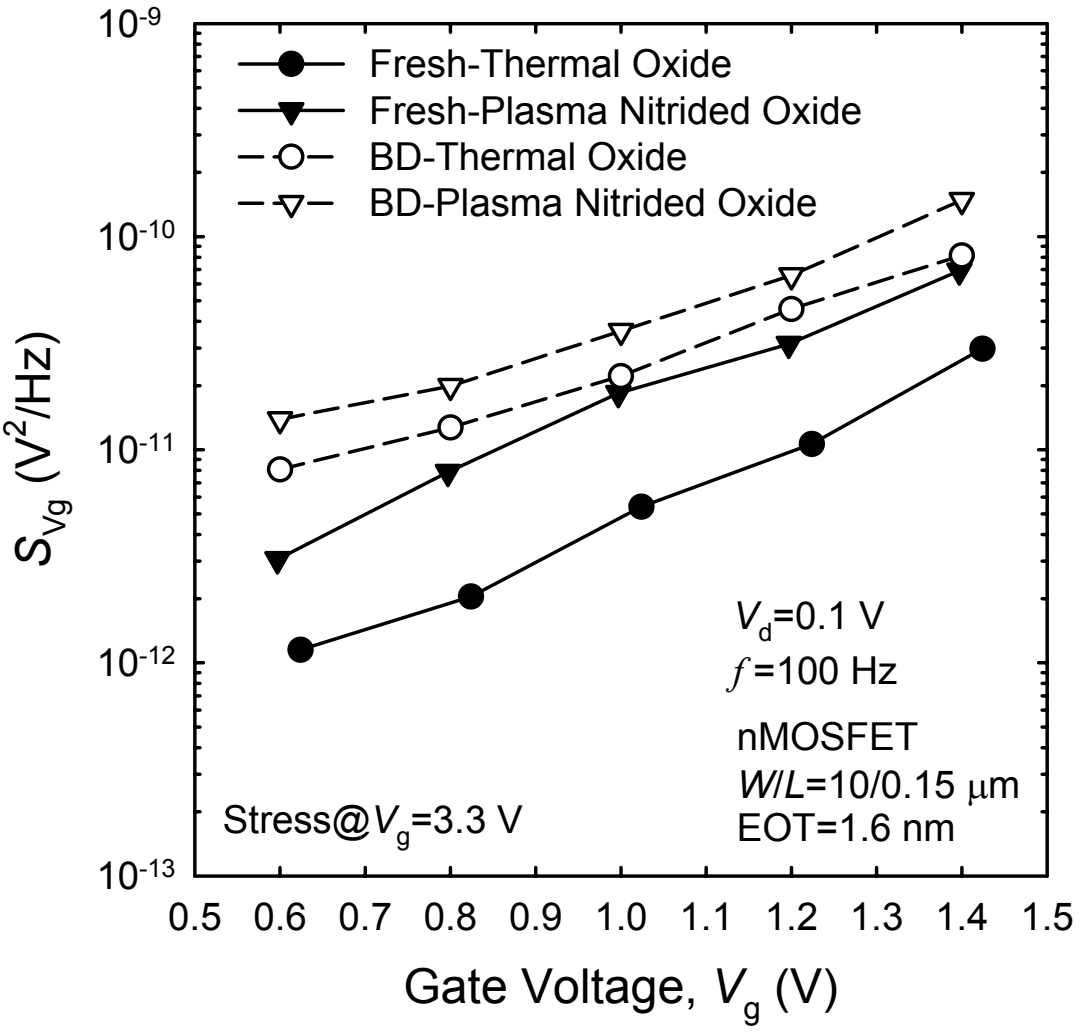

Fig. 3.7. Low-frequency S_{Vg} noise power spectra (f = 100 Hz) versus gate overdrives ($V_g - V_t$) at linear operation (V_d = 0.1 V) for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after oxide breakdown (V_g = 3.3 V).

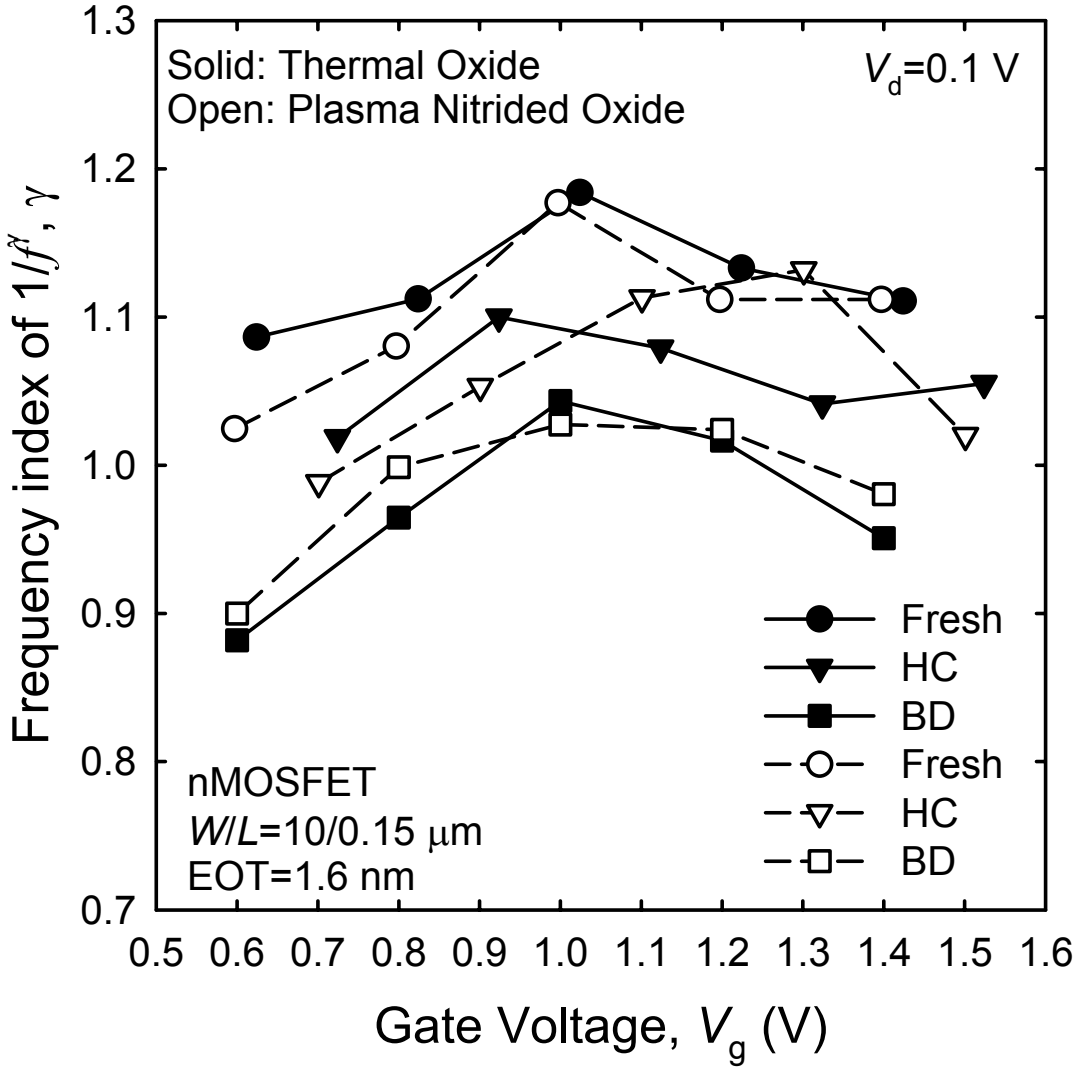

Fig. 3.8. The frequency index of noise spectrum, γ, versus gate voltages for 0.15 μm nMOSFETs with ultra-thin (EOT = 1.6 nm) thermal and plasma nitrided gate oxides before and after hot-carrier stressing (V_g = V_d = 2.3 V for 1000 seconds) and oxide breakdown (V_g = 3.3 V).

Chapter 4

Reliability of Strained SiGe Channel pMOSFETs with Ultra-Thin (EOT = 3.1 nm) N_2O-Annealed SiN Gate Dielectric

4.1 Introduction

The strained SiGe layer as the channel of the deep sub-micron MOSFETs has been extensively studied recently for improving the performance of device **[1]**, **[2]**. In addition to the fact that the bulk carrier mobility of the SiGe layer is higher than that of the Si layer, the compressive strain of SiGe layer **[3]–[5]** and the quantum confinement effect induced by the offset of valence band between SiGe and Si **[6]** are both lead to the enhancement of hole mobility when the SiGe layer is deposited directly on the Si substrate. Consequently, the performance of pMOSFET devices is predictably increased by using the SiGe channel **[7]–[9]**. Moreover, the SiGe devices have several attractive merits in device fabrication. Firstly, the SiGe layer can be selectively deposited on the Si substrate by a chemical vapor deposition (CVD) system. Secondly, the process of device fabrication is completely comparable to the conventional Si devices. Finally, the high dopant activation rate of SiGe is beneficial to form the shallow junction in source and drain, and the process with low thermal budget can be realized **[10]**.

In spite of the advantages mentioned above, the lattice mismatch between SiGe and Si interface will induce the formation of dislocations in the deposited SiGe film

and the Ge-induced scattering in the SiGe layer will degrade the carrier mobility **[6]**. Besides, lacking a high quality gate insulator is another concerned issue of the SiGe MOSFETs because Ge precipitates will be formed at the SiO_2/SiGe interface when the SiGe layer is thermally oxidized to grow the gate oxide and the quality of gate oxide will be deteriorated. Therefore, thermal oxidizing a Si capping layer **[11]** or direct depositing on the SiGe substrate **[12]**, **[13]** has become the most appropriate method to form the gate insulator of the SiGe channel MOSFETs. However, the high temperature oxidation process may cause the relaxation of the strained SiGe layer. Because the temperature of dielectric deposition is generally much lower than that of thermal oxidation and the relaxation problem can be effectively prevented, the silicon nitride (SiN) has been reported as the promising candidate of the gate dielectric for the SiGe channel MOSFETs **[12]**, **[13]**. Although the dielectric constant of SiN is larger than that of conventional SiO_2 and the boron penetration from the p^+ poly-Si gate can be effectively suppressed by using the SiN gate dielectric, the excess oxide charges and interface states introduced by the SiN gate dielectric cause the shift of threshold voltage and degrade the device performance. Therefore, N_2O-annealing has been proposed to improve the quality of the SiN gate dielectric and the SiN/Si interface **[14]**, **[15]**.

For concerning the reliability of device, the hot-carrier (HC) degradation has been extensively investigated for the conventional Si channel devices with non-nitrided and nitrided gate oxides **[16]–[21]**. The oxide charges and the interface states may be generated by the hot-carrier stressing **[20]**, **[21]**. In addition, the effect of negative-bias temperature-instability (NBTI) has also been reported as another degradation issue dominating the device reliability because the interface state generation and the oxide charge formation will be induced by the electrochemical reaction at the interface when the device is stressed at high voltage and high

temperature **[22]–[25]**. Although many studies have subjected to the Si and SiGe channel MOSFETs with SiN-related gate dielectric **[12]**, **[13]**, **[16]**, **[17]**, the electrical characteristics and the reliability of the SiGe channel devices with N_2O-annealed SiN gate dielectric still need extensive study. In this paper, therefore, we fabricated pMOSFETs with $Si_{0.85}Ge_{0.15}$ channel and ultra-thin N_2O-annealed SiN gate dielectric, and investigated the device degradations of the hot-carrier and negative-bias-temperature-instability stressing.

4.2 Device Fabrication and Characteristics Measurement

The pMOSFETs with $Si_{0.85}Ge_{0.15}$ channel and ultra-thin N_2O-annealed SiN gate dielectric were fabricated on 6-inch (100) orientated Si substrate for our experiments. After performing the standard local oxidation of silicon (LOCOS) process, we selectively deposited 50 nm $Si_{0.85}Ge_{0.15}$ epitaxy layer on the Si substrate in an ultra-high vacuum chemical vapor deposition (UHVCVD) system at 550 ºC. The SiGe layer was in-situ doped with phosphorus. After being cleaned by the RCA process, the SiN gate dielectric was deposited in a low pressure chemical vapor deposition (LPCVD) system with dichlorosilane (DCS, SiH_2Cl_2) and NH_3 at 780 ºC and then annealed immediately by using the rapid thermal annealing (RTA) at 900 ºC in N_2O ambience for 30 seconds. Sequentially, the gate electrode was formed by depositing the 150 nm undoped poly-Si film in an LPCVD system and patterning by using lithography and etching process. The source/drain was carried out by following the processes of the source/drain extension implantation (BF_2 with a dosage of 1×10^{14} cm^{-2} at an energy of 10 keV), oxide spacer formation (LPCVD TEOS oxide), the self-aligned gate and source/drain implantation (BF_2 with a dosage of 5×10^{15} cm^{-2} at

an energy of 20 keV), and the dopant activation (RTA at 900 ºC in N_2 ambience for 30 seconds). Finally, we completed the device fabrication by processing the standard back-end-of-line (BEOL) contact and metallization for all wafers. The schematic device cross-section and process flow of the device fabrication are also illustrated in **Fig. 4.1**.

The electrical characteristics of the capacitance-voltage (*C–V*) and the current-voltage (*I–V*) characteristics were measured by using the Agilent 4284 LCR meter and the Keithley 4200 semiconductor characterization system, respectively. The reliability of devices was investigated by evaluating the degradations of the drain current (ΔI_d), transconductance (ΔG_m), and threshold voltage (ΔV_t) when they were stressed under the hot-carrier (HC) and the negative-bias-temperature-instability (NBTI) stressing. Additionally, the density of interface state (N_{it}) was extracted from the charge pumping current (I_{CP}) which was obtained by using the charge pumping technique with a constant base level ($V_{g,base}$) and varied pulse amplitudes ($V_{g,peak}$).

4.3 Results and Discussion

4.3.1 *C–V* and *I–V* Characteristics of pMOSFETs

Figure 4.2 shows the capacitance-voltage (*C–V*) characteristics of the pMOSFET with $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed SiN gate dielectric. The equivalent oxide thickness (EOT) of 3.1 nm shown in **Fig. 4.2** is extracted from the accumulation capacitance (C_{acc}) of the high frequency (100 kHz) *C–V* curve. There is no hysteresis observed, implying that the ultra-thin N_2O-annealed SiN gate dielectric has only an insignificant amount of oxide traps. Besides, the capacitance at strong inversion is

slightly lower than that at strong accumulation, which is mainly due to the poly depletion effect (PDE). On the other hand, the leakage current of the N_2O-annealed SiN gate dielectric, as shown in **Fig. 4.3**, is more than two orders of magnitude lower than that of the conventional thermal oxide with the same EOT **[26]**. This is caused by the thicker physical thickness of the SiN layer because the dielectric constant of SiN is higher than that of SiO_2. Moreover, the well-fitted straight line in the Fowler-Nordheim (J/E_{eff}^2 versus $1/E_{eff}$) characteristics shown in the inset of **Fig. 4.3** demonstrates that the conduction mechanism of the gate current is dominated by the Fowler-Nordheim (FN) tunneling with an effective barrier height of 1.8 eV.

The characteristics of I_d and G_m versus V_g are demonstrated in **Fig. 4.4**. The threshold voltage (V_t) of –1.87 V and the subthreshold swing (S) of 125 mV/dec are also presented. **Figure 4.5** displays the I_d–V_d curves with various gate overdrives (V_g–V_t) from 0 to –2 V for the same device. Apparently, **Figures 4.4** and **4.5** depict that the pMOSFET with SiGe channel and ultra-thin N_2O-annealed SiN gate dielectric has well-performed on/off and output characteristics.

4.3.2 CVS and CCS for pMOSCAPs

The *C–V* characteristics of pMOSCAPs before and after being stressed under various conditions of constant voltage stress (CVS) are shown in **Fig. 4.6**. Because the *C–V* curves remain almost unchanged after stressing, it indicates that the CVS has negligible effects on the *C–V* characteristics even the gate voltage is up to 5.3 V and no polarity dependence is observed. **Figure 4.7** displays the variations of leakage currents with constant voltage stressing bias conditions which is so-called the stress-induced leakage current (SILC). Although only a slight increase of the current density with the stressing time was observed, the degradation at the negative gate

voltage regime, however, is slightly larger than that at the positive gate voltage regime. Because the stress-induced leakage current is dominated by the trap-assisted-tunneling (TAT) **[27]**, **[28]**, the polarity dependence of SILC reveals that the traps generated in the gate dielectric during the stressing process should be close to the gate electrode. Moreover, similar results are also obtained for various conditions of constant current stress (CCS) as shown in **Fig 4.8** and **Fig. 4.9**.

4.3.3 HC and NBTI Stressing for pMOSFETs

Figure 4.10 displays the degradation of drain currents (ΔI_d) versus stress time when devices are stressed with the hot-carrier (stressed at $V_g=V_d$, the channel-hot-carrier (CHC), and $V_g=2V_d/3$, the drain-avalanche-hot-carrier (DAHC)) and the negative-bias-temperature- instability (stressed at room temperature (RT) and 100 ºC) stressing. Obviously, the degradation of HC stressing is much severe than that of NBTI stressing, and the CHC stressing has been shown to be the worst case. Similar results, as shown in **Fig. 4.11**, are also observed for the degradation of transconductance (ΔG_m). Because the trends of ΔI_d and ΔG_m are almost identical, the same mechanism should be responsible for the hot-carrier degradations of drain current and transconductance. However, the variations both for I_d and G_m are moderate when the devices are stressed with the NBTI stressing at 100 ºC as compared with the counterparts at room temperature. This can be explained by the self-recovery effect of the high temperature NBTI degradation **[29]**. Moreover, the shift of threshold voltages (ΔV_t) with the stress time is plotted in **Fig. 4.12**. Interestingly, all values of ΔV_t are positive for all stressing conditions and follow a power law with the stress time in the form of $\Delta V_t = At^n$, indicating that electron trapping in the gate dielectric and/or at the interface is occurred during the stressing

process. According to the previous report **[30]**, for a small value of n ($n < 0.2$) means that the degradation of V_t should be dominated by the electron trapping in the gate oxide while ΔV_t should be caused by the interface state generation for a large value of n ($n > 0.3$ in our case). Therefore, we believe that the interface state generation is responsible for the hot-carrier degradation and the electron trapping in the gate dielectric dominates the NBTI reliability degradation for the pMOSFET with $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed SiN gate dielectric.

The interface state density variation accompanying with stressing using the charge pumping (CP) technique are shown in **Fig. 4.13**. The charge pumping currents (I_{CP}) are increased after the devices are stressed, and this confirms the generation of excess interface states. In addition, **Fig. 4.14**, the enlargement of **Fig. 4.13**, also depicts slightly positive shifts of the I_{CP} curves. Again, the occurrence of electron trapping which has been observed after stressing is obviously consistent with the results of ΔV_t. Comparing the interface state generation (ΔN_{it}) for all stressing conditions in **Fig. 4.15**, the hot-carrier stressing, especially the CHC stressing, shows higher ΔN_{it} than the NBTI stressing. It demonstrates that the generated interface states play the most important role in the hot-carrier degradation for the device reliability. Nevertheless, it is worth to notice that the result of charge pumping measurement for the NBTI stressing at 100 ºC is not shown here because of its insignificant degradation due to the self-recovery effect.

The degradations for the different bias conditions of $V_g = V_d = -4.5$, -5, and -5.3 V were further investigated even though the CHC stressing has been shown to be the worst case for the hot-carrier degradation. The results of ΔI_d, ΔG_m, and ΔV_t are shown in **Fig. 4.16**, **Fig. 4.17**, and **Fig. 4.18**, respectively. Although the drain currents are degraded with increasing the stressing time and applying voltages, the ΔG_m tends to saturate when the device was stressed under higher voltages for a longer time. It is

quite different from the case of stressing at $V_g = V_d = -4.5$ V which the degradations of I_d and G_m are increased monotonically with the stress time. From the shifts of threshold voltage induced by the hot-carrier stressing as well as the results shown in Fig. 4.16, positive shifts of V_t are only occurred at the beginning for the stressing voltages of –5 and –5.3 V and then the ΔV_t tends to be negative. It means that the electron trapping dominates the device degradation at the initial stage of the channel-hot-carrier stressing and then the hole trapping is enhanced to mainly degrade the device characteristics for a longer time stressing **[31]**, **[32]**.

4.4 Summary

We have successfully fabricated pMOSFETs with selectively 50 nm epitaxial $Si_{0.85}Ge_{0.15}$ channel and ultra-thin (EOT = 3.1 nm) N_2O-annealed SiN gate dielectric. No significant as-deposited oxide traps have been observed in the N_2O-annealed SiN gate dielectric and the FN tunneling has been demonstrated as the conduction mechanism responsible for the gate leakage current with an effective barrier height of 1.8 eV. Besides, the device also shows well-performed on/off and output characteristics. For the reliability concern, insignificant degradation has been found when the capacitors were stressed under the constant voltage (or current) stressing. This means that a good quality of gate dielectric can be obtained by the N_2O-annealed SiN film. On the other hand, the polarity dependence of SILC reveals that the oxide traps generated during the stressing process should be more close to the gate electrode. Moreover, we have studied the effect of hot-carrier and negative-bias-temperature instability stressing on the SiGe channel pMOSFETs with ultra-thin N_2O-annealed SiN gate dielectric. It is found that the hot-carrier degradation is more severe than the NBTI degradation and the channel-hot-carrier stressing is regarded as the worst case

of device degradation. According to the power law relationship of ΔV_t versus stress time as well as the results of charge pumping measurement, we have demonstrated that the interface state generation is the predominant factor for the HC degradation while the electron trapping dominates the degradation of device characteristics for the NBTI stressing. Although the electron trapping has been found to occur at the initial stage of the high voltage CHC stressing, the hole trapping will eventually dominate the degradation when the device is stressed for a longer time.

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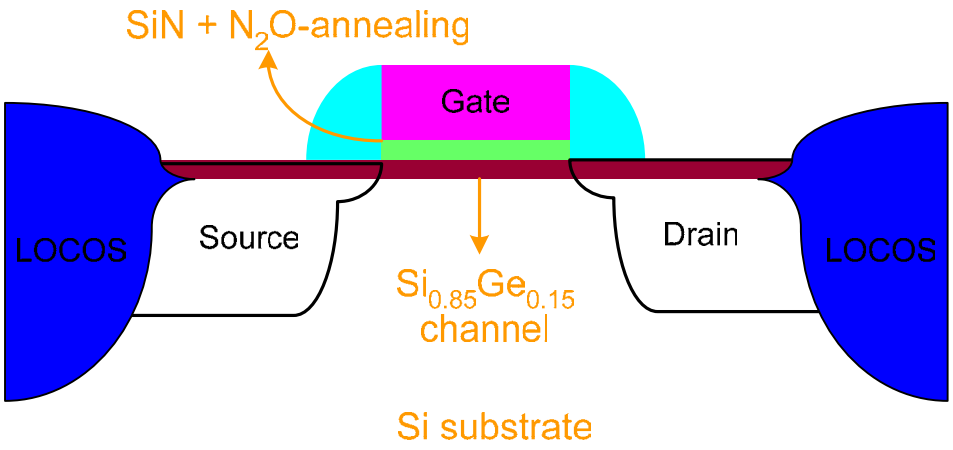

- LOCOS Isolation
- UHVCVD Selective In-Situ Doped Epitaxy $Si_{0.85}Ge_{0.15}$ Channel
- LPCVD SiN Deposition
  RTA N_2O-Annealing
- LPCVD Undoped Poly-Si Deposition
- Source/Drain Formation
- RTA Dopant Activation
- Contact and Metallization
  Forming Gas Annealing

Fig. 4.1. The schematic device cross-section and process flow of device fabrication.

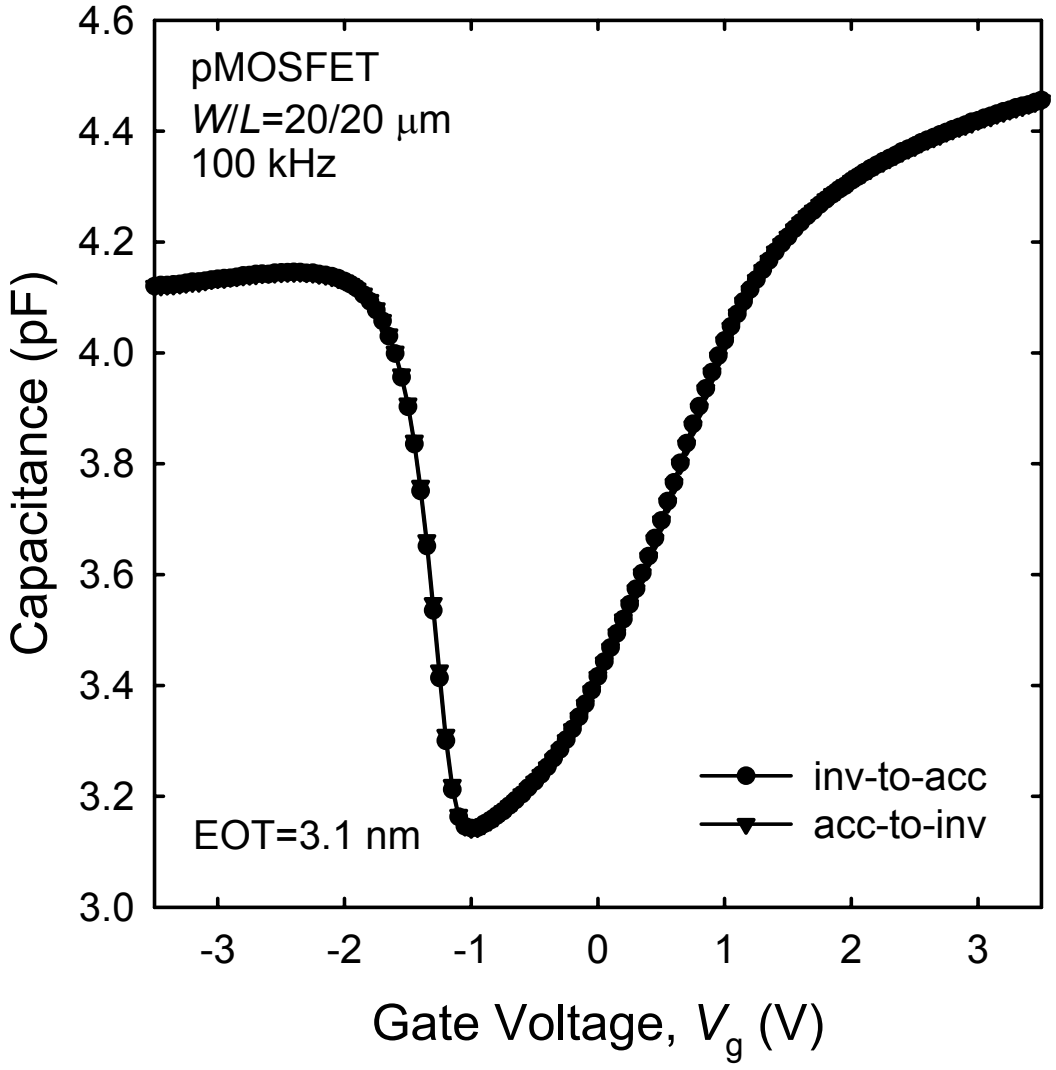

Fig. 4.2. The capacitance–voltage (*C–V*) characteristics of the pMOSFET with 50 nm $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed SiN (EOT=3.1 nm) gate dielectric. The equivalent oxide thickness (EOT) of 3.1 nm is extracted from the accumulation capacitance.

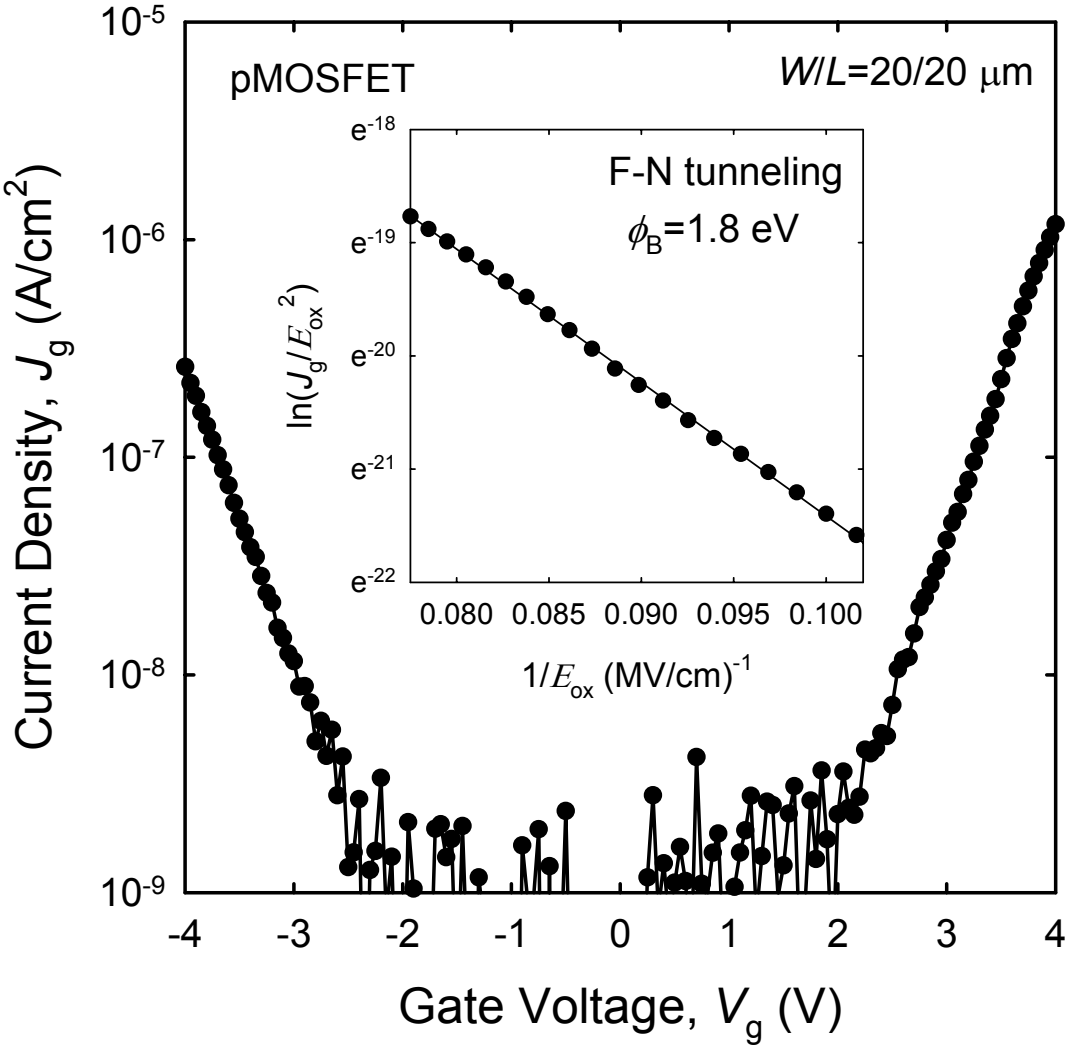

Fig. 4.3. The current–voltage (*I–V*) characteristics of the pMOSFET with 50 nm $Si_{0.85}Ge_{0.15}$ channel and N_2O-annealed SiN (EOT=3.1 nm) gate dielectric. The inset shows the fitting of Fowler-Nordheim (FN) tunneling with an effective barrier height of 1.8 eV.

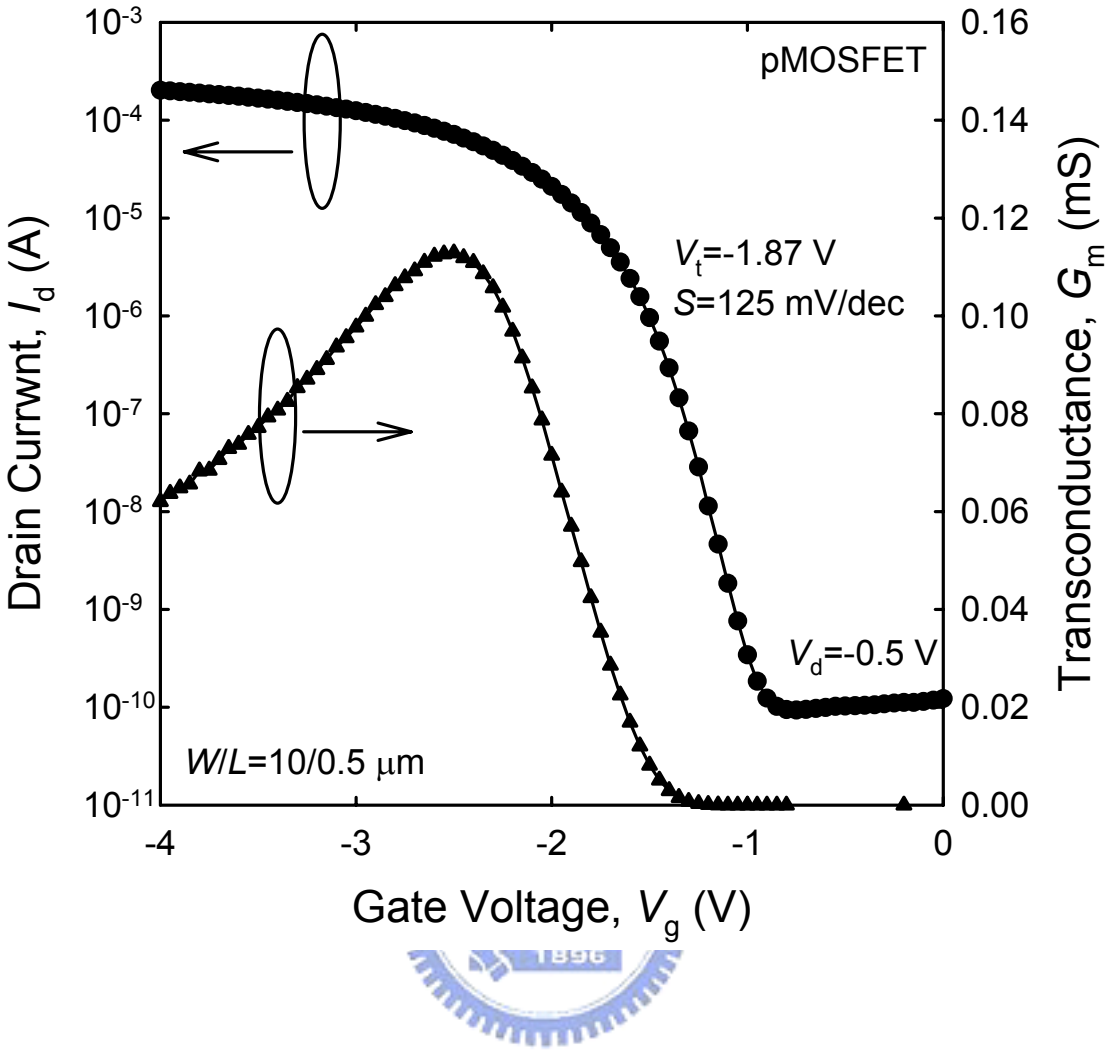

Fig. 4.4. The I_d–V_g and G_m characteristics of SiGe pMOSFET (W/L=10/0.5 μm) with N_2O-annealed SiN gate dielectric.

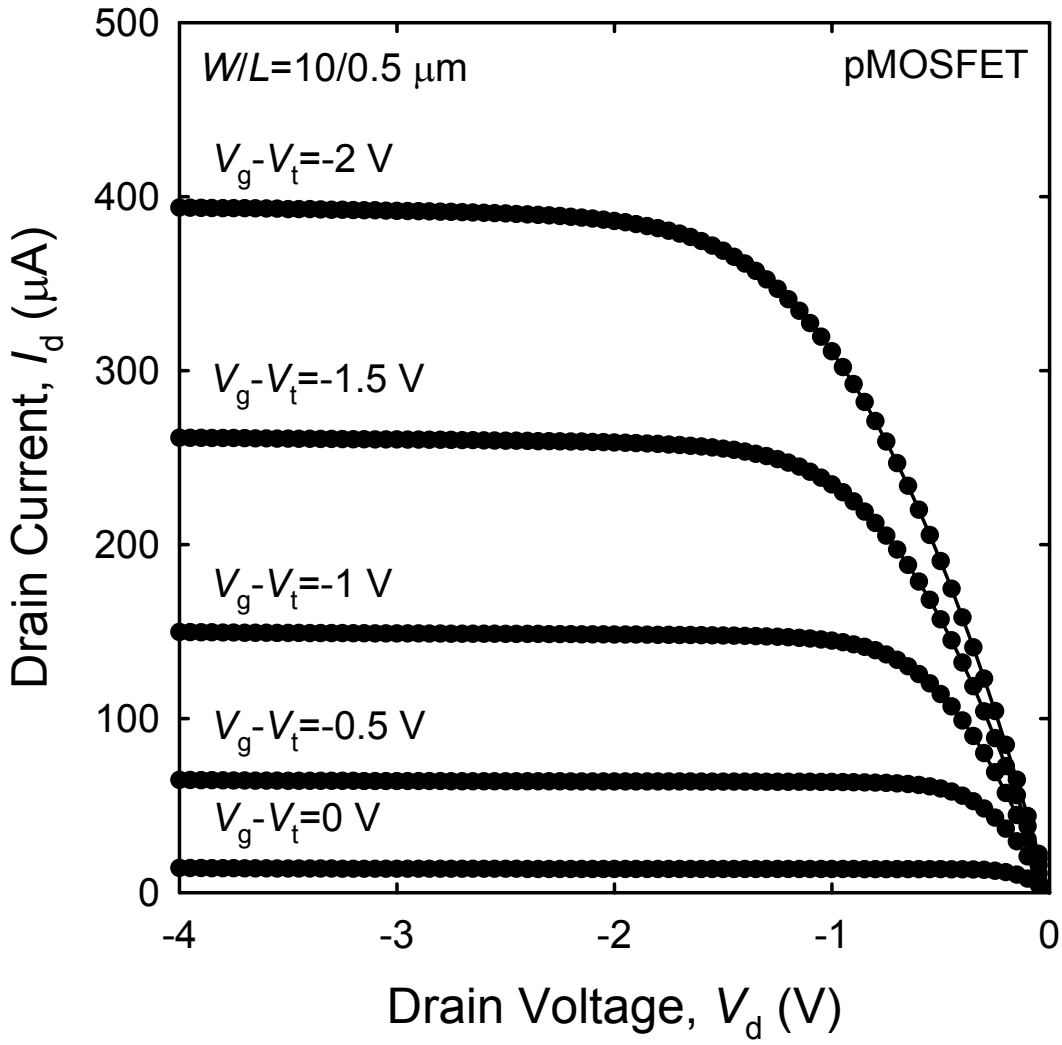

Fig. 4.5. The I_d–V_d characteristics of SiGe pMOSFET (W/L=10/0.5 μm) with N_2O-annealed SiN gate dielectric with various gate overdrives (V_g–V_t) from 0 to –2 V.

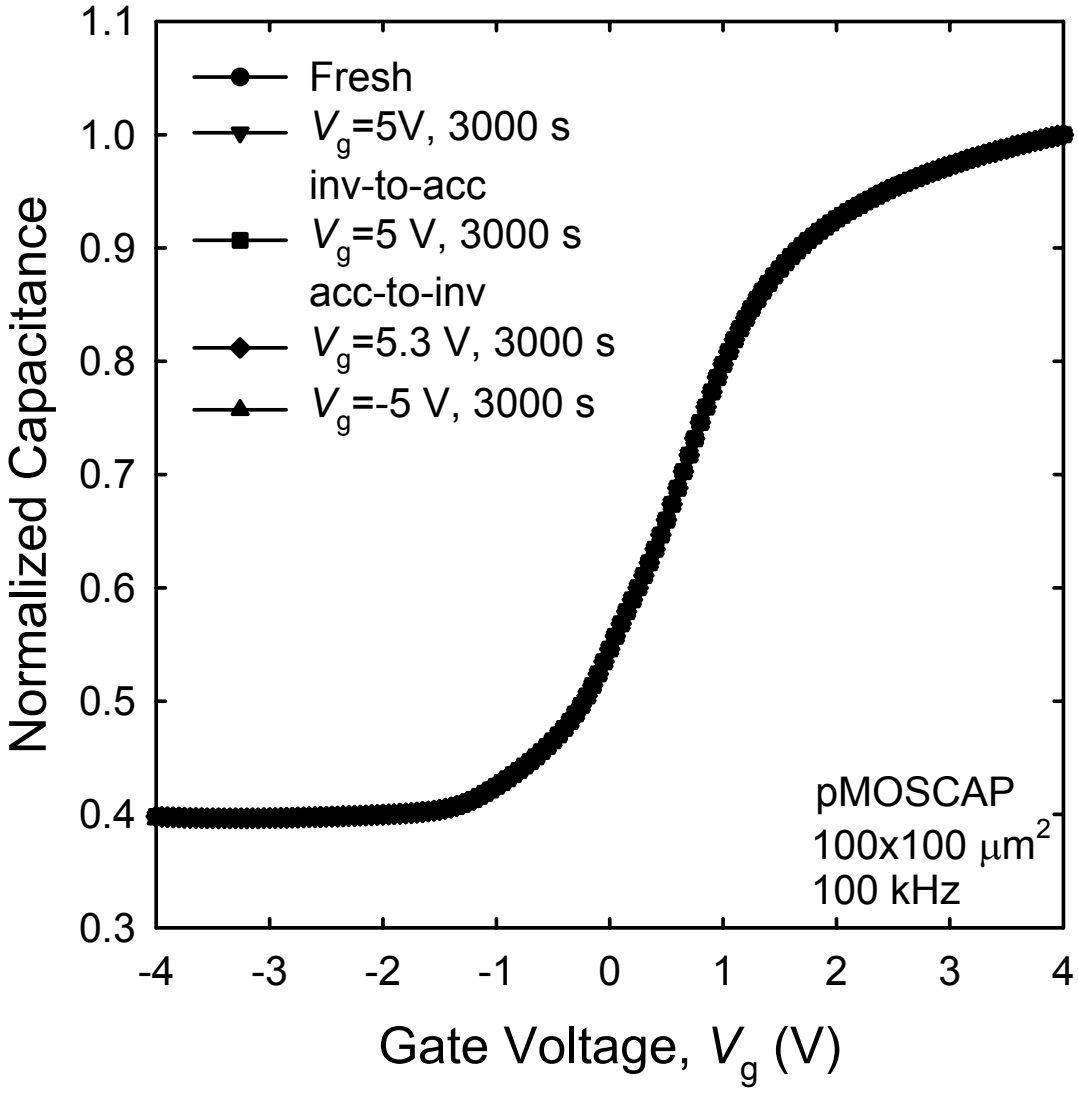

Fig. 4.6. The *C–V* characteristics of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric for various CVS conditions.

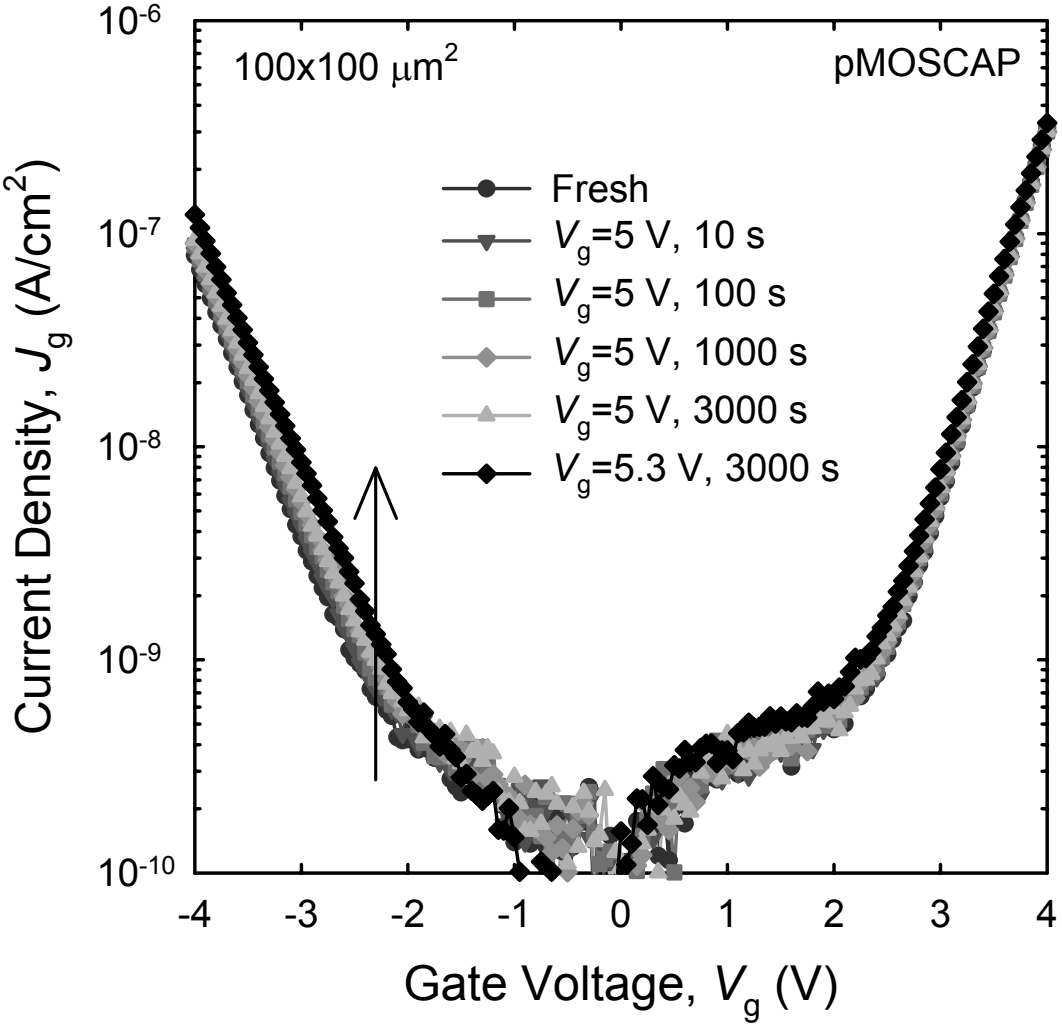

Fig. 4.7. The leakage current versus the stress time of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric under the constant voltage stress (CVS).

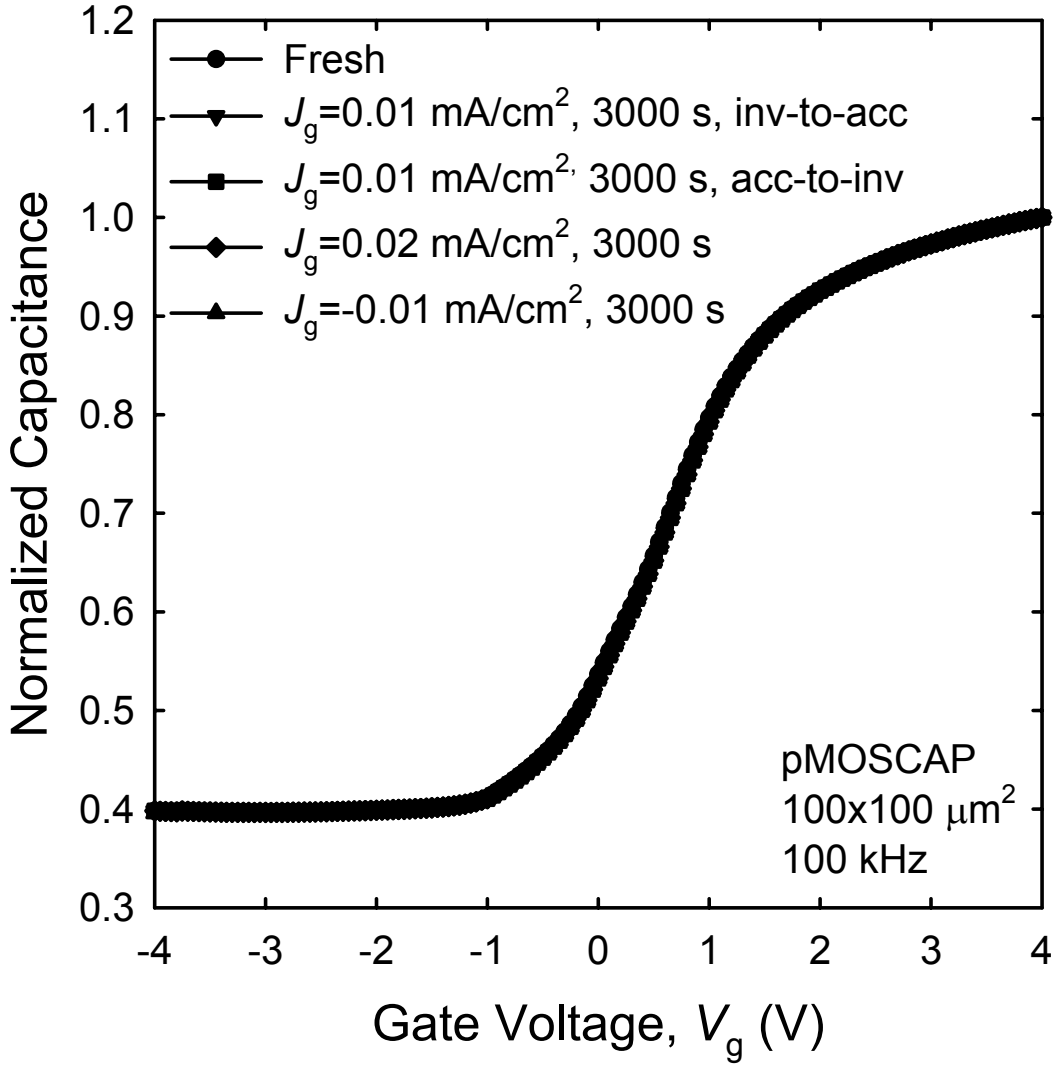

Fig. 4.8. The *C–V* characteristics of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric for various CCS conditions.

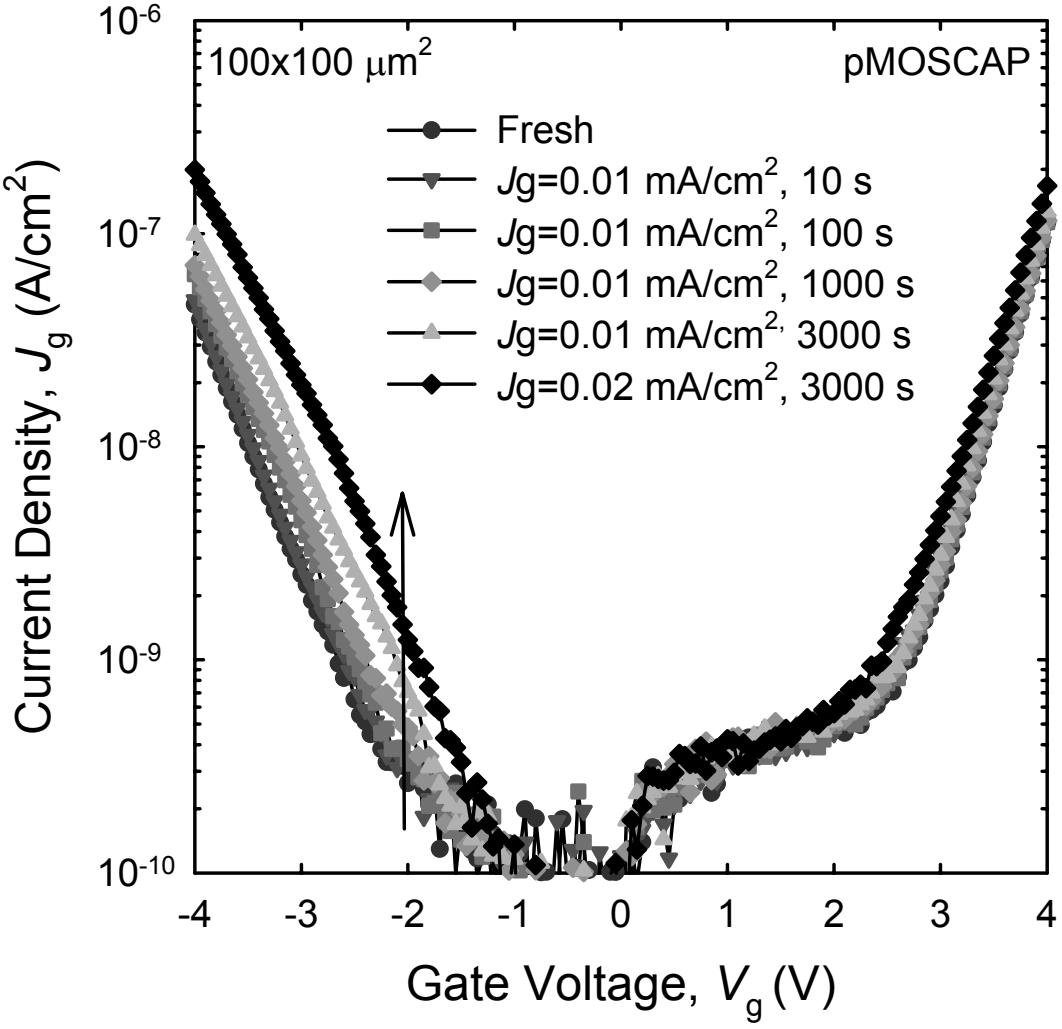

Fig. 4.9. The leakage current versus the stress time of SiGe pMOSCAP with N_2O-annealed SiN gate dielectric under the constant current stress (CCS).

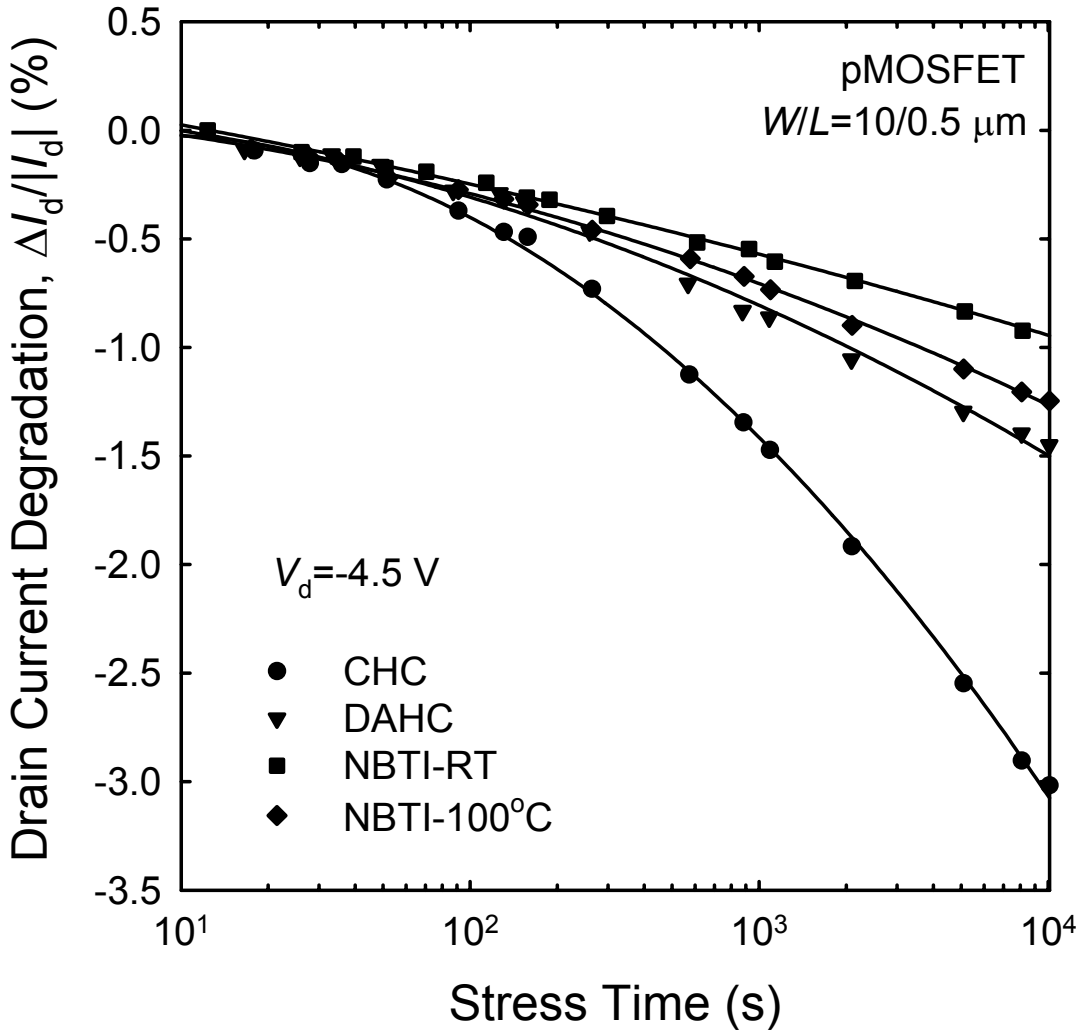

Fig. 4.10. The I_d degradation versus the stress time of HC and NBTI stressing for the SiGe pMOSCAP with N_2O-annealed SiN gate dielectric.

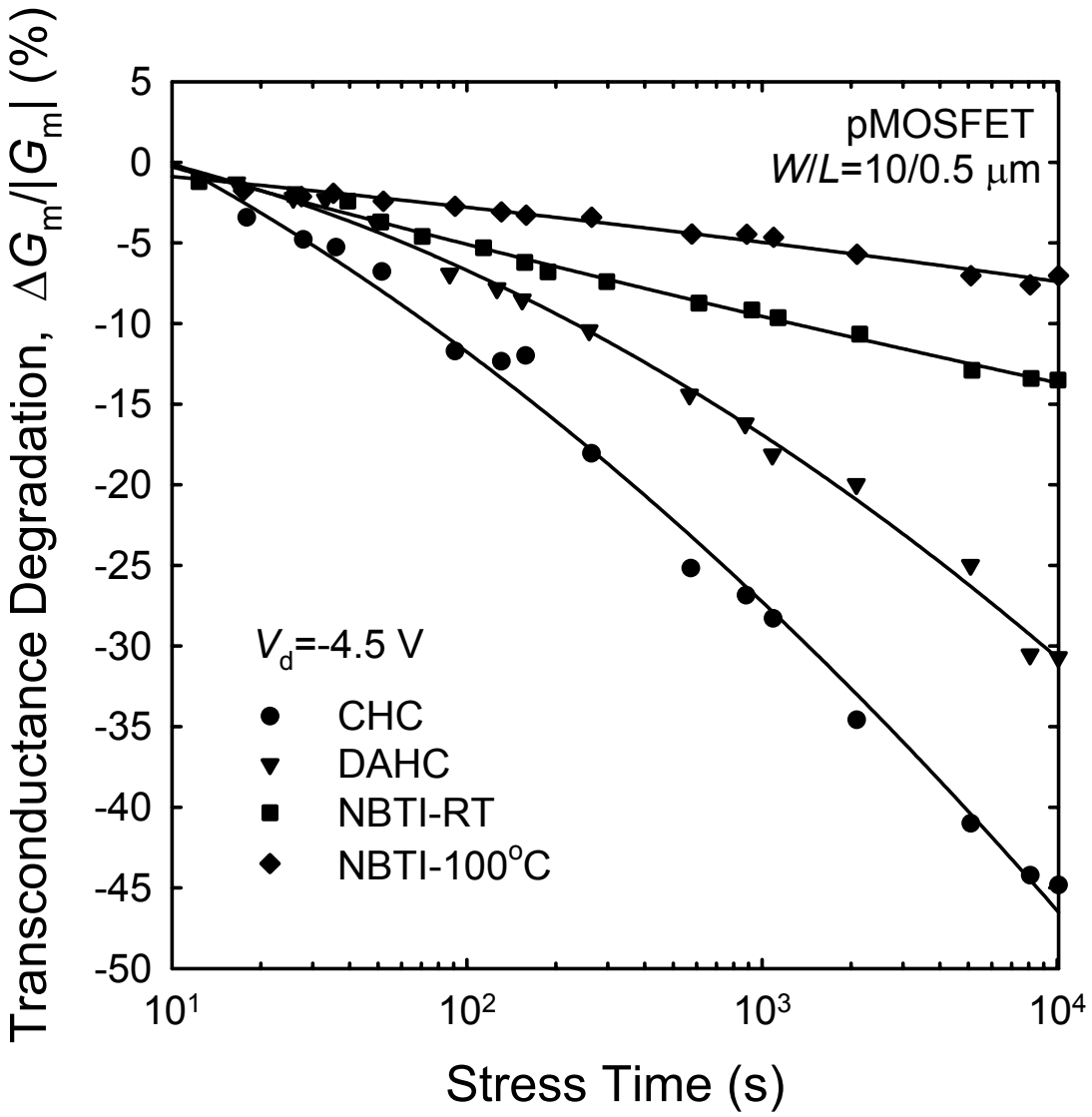

Fig. 4.11. The G_m degradation versus the stress time of HC and NBTI stressing for the SiGe pMOSCAP with N_2O-annealed SiN gate dielectric.

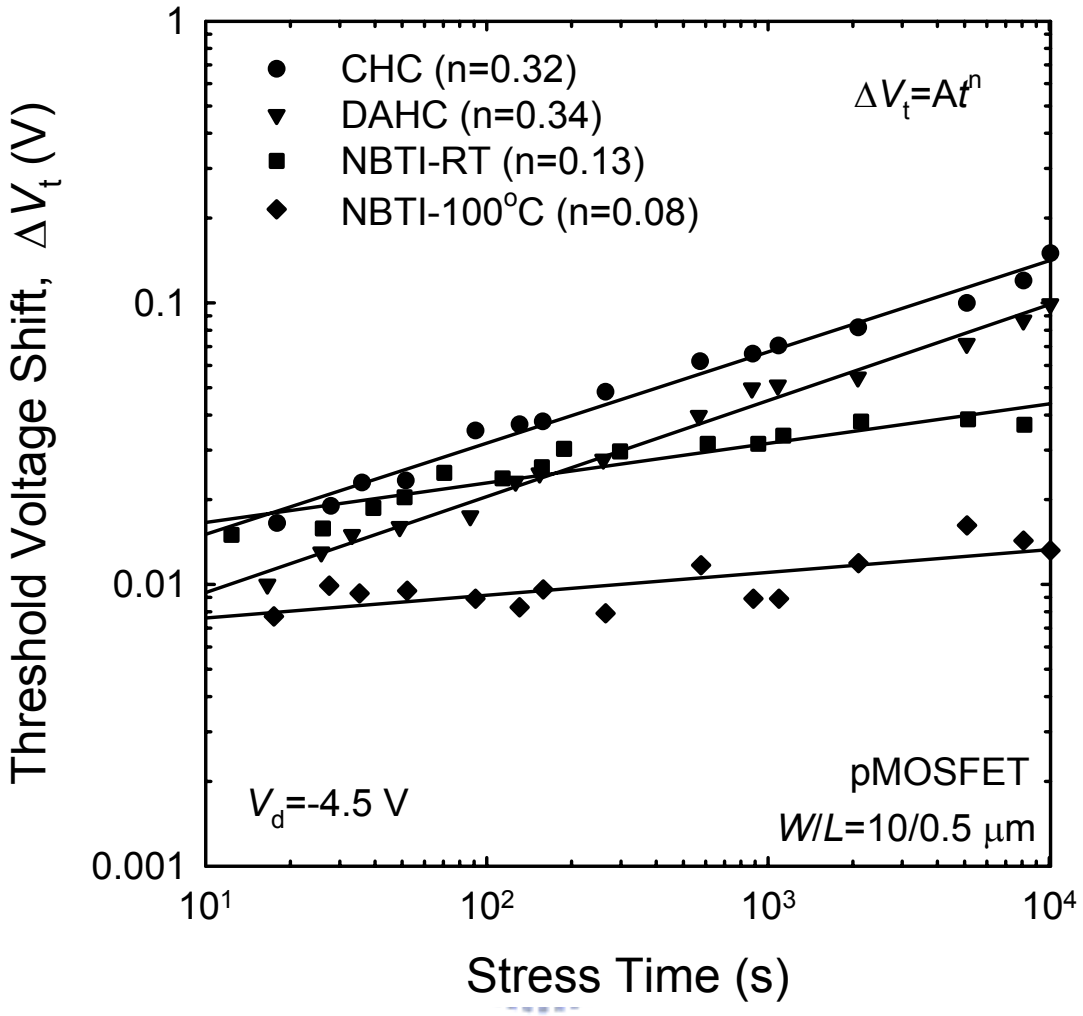

Fig. 4.12. The threshold voltage shift (ΔV_t) versus the stress time for the SiGe pMOSCAP with N_2O-annealed SiN gate dielectric.

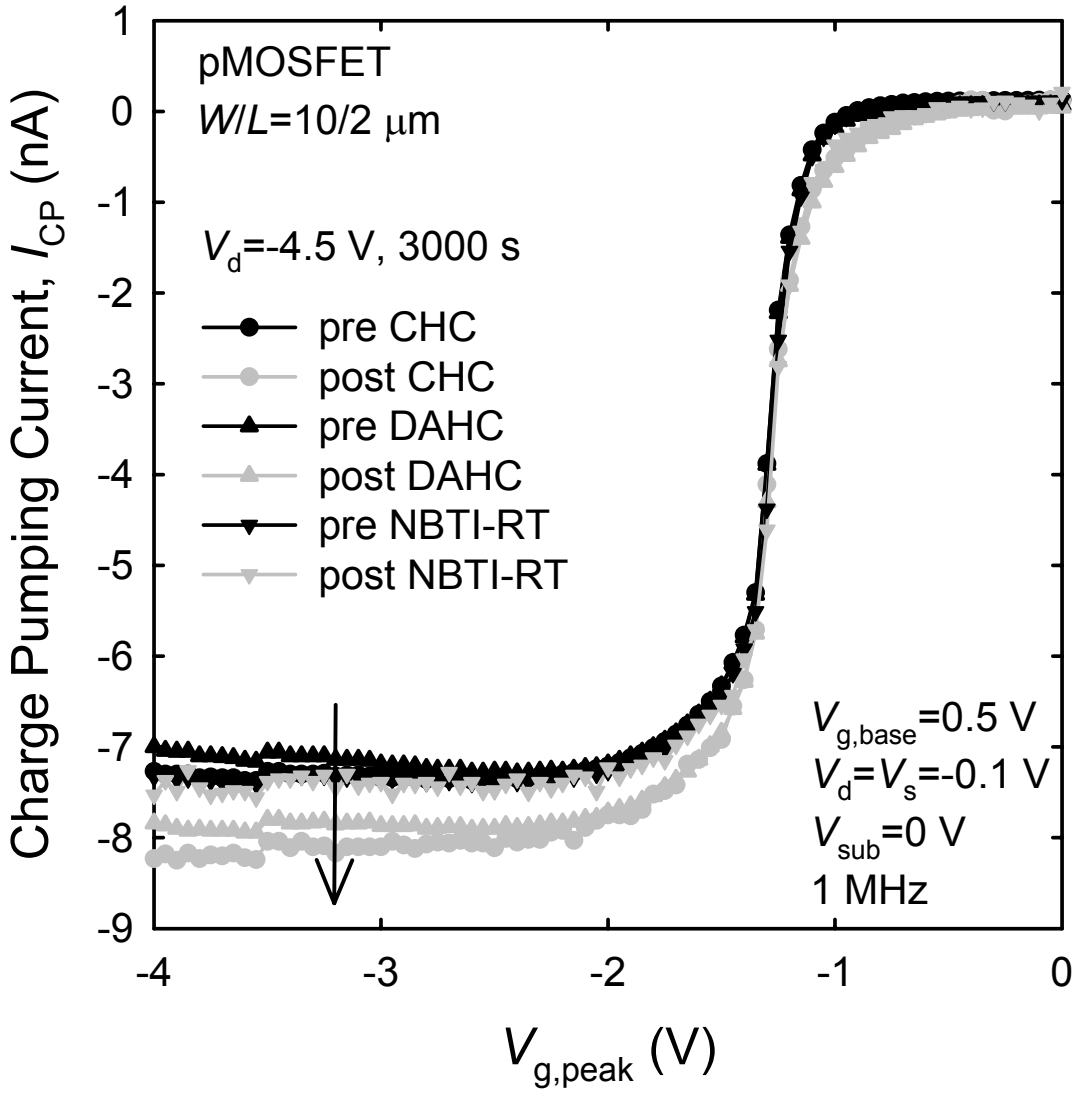

Fig. 4.13. The charge pumping currents of the devices before and after being stressed at HC and NBTI (RT) stressing.

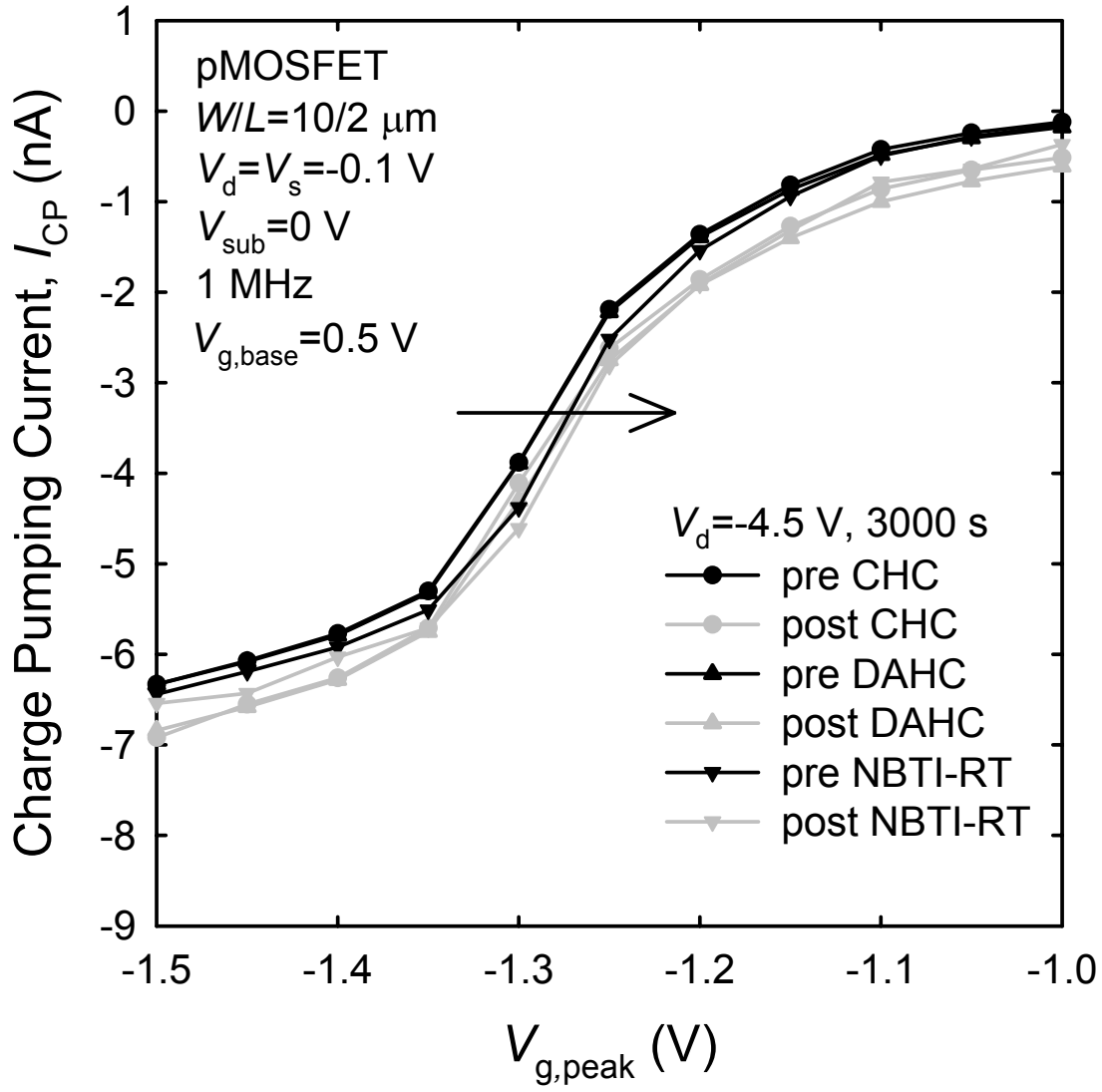

Fig. 4.14. The enlargement of the charge pumping currents shown in Fig. 4.13.

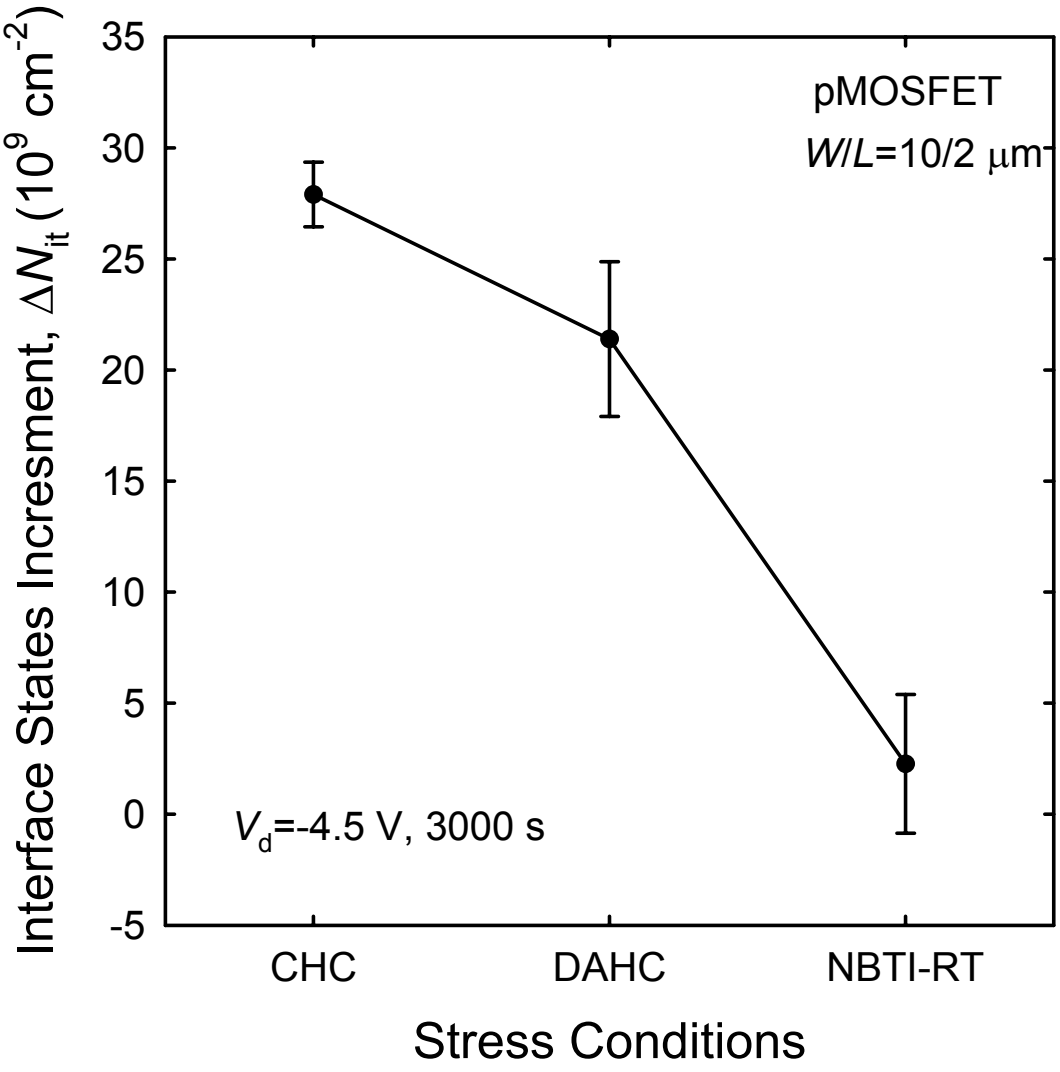

Fig. 4.15. Comparison of the interface state generation (ΔN_{it}) which are extracted from the increase of charge pumping currents for the HC and NBTI (RT) stressing.

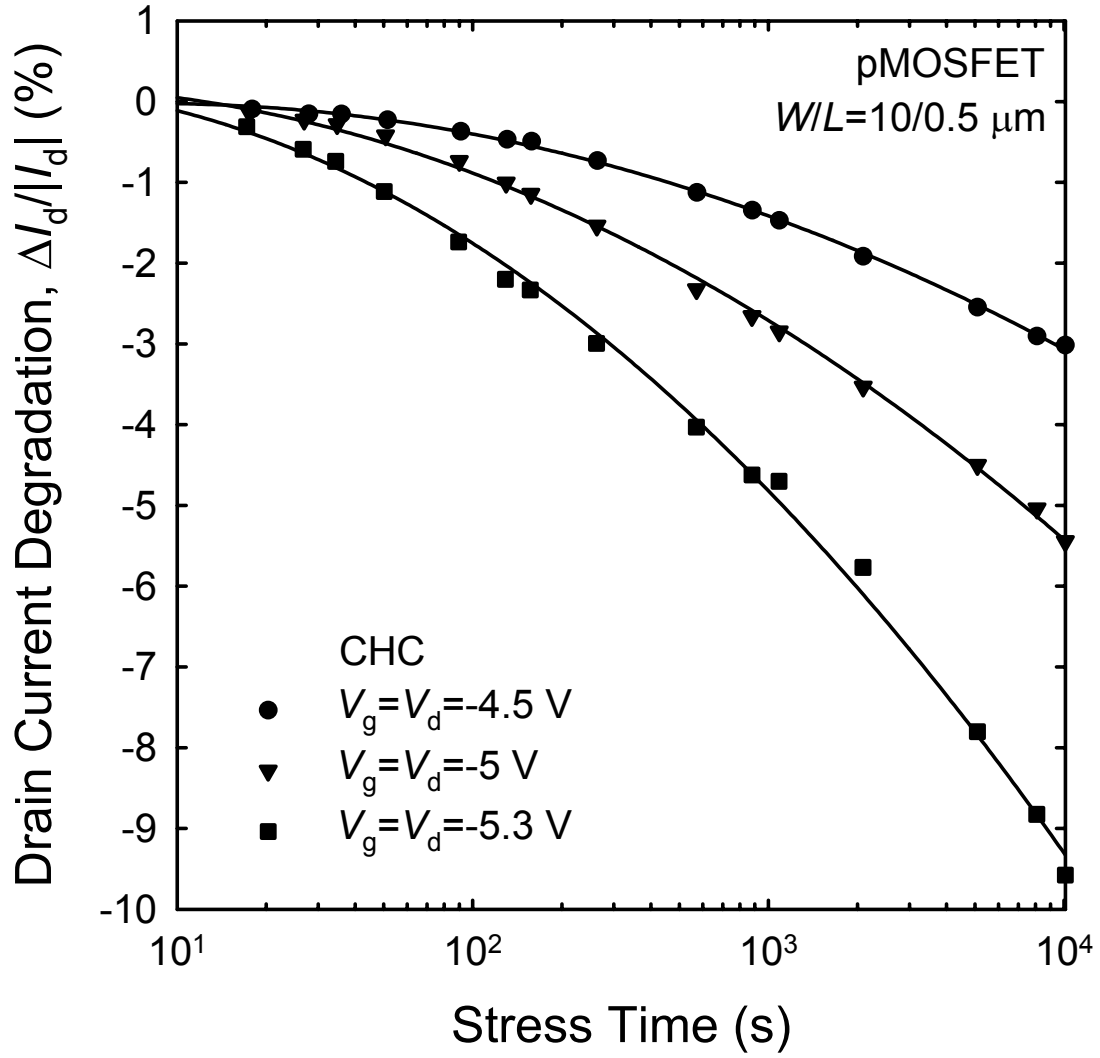

Fig. 4.16. The I_d degradation versus the stress time for the channel-hot-carrier stressing under various bias conditions of $V_g = V_d = –4.5$, –5, and –5.3 V.

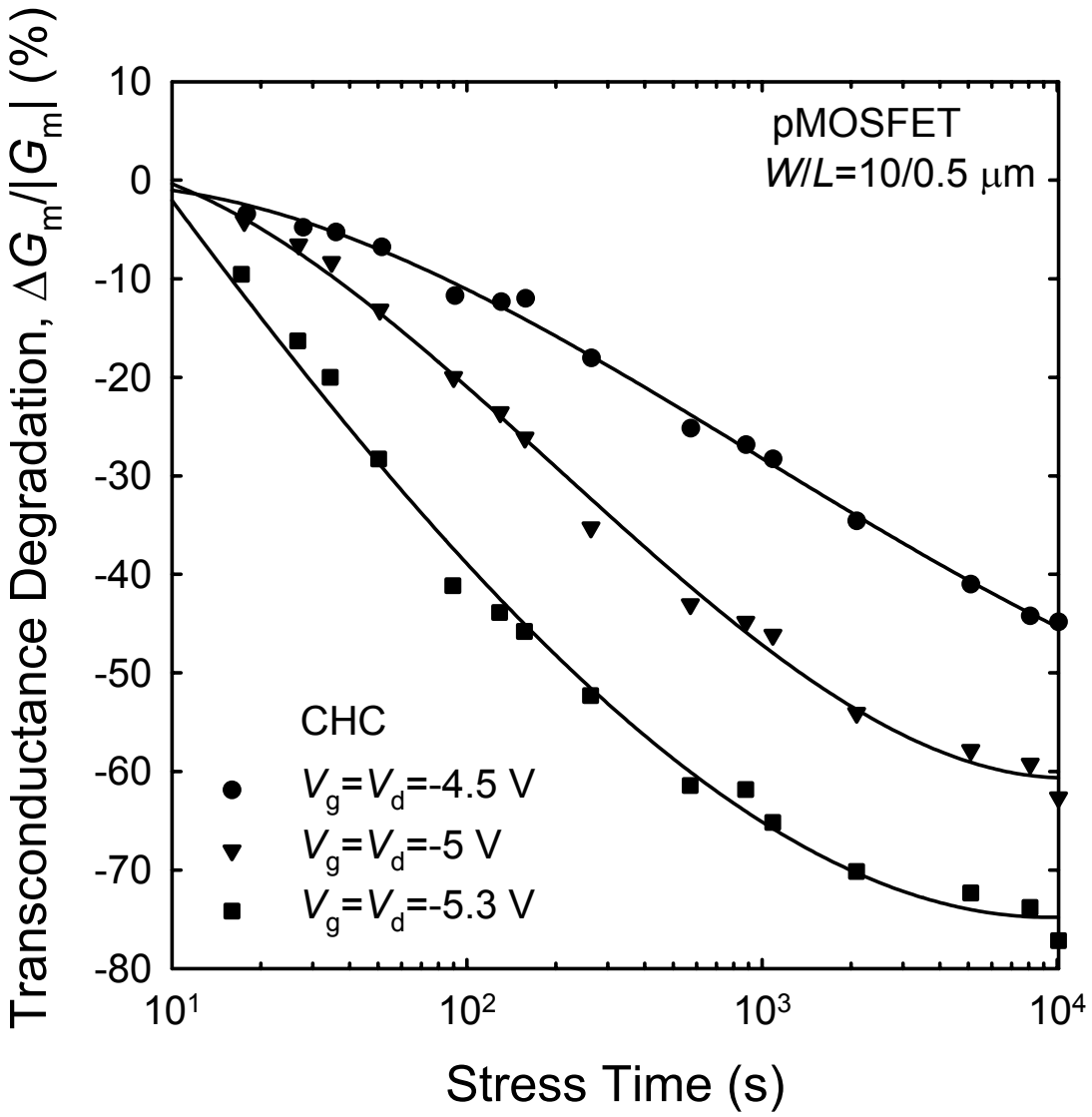

Fig. 4.17. The G_m degradation versus the stress time for the channel-hot-carrier stressing under various bias conditions of $V_g = V_d = –4.5$, –5, and –5.3 V.

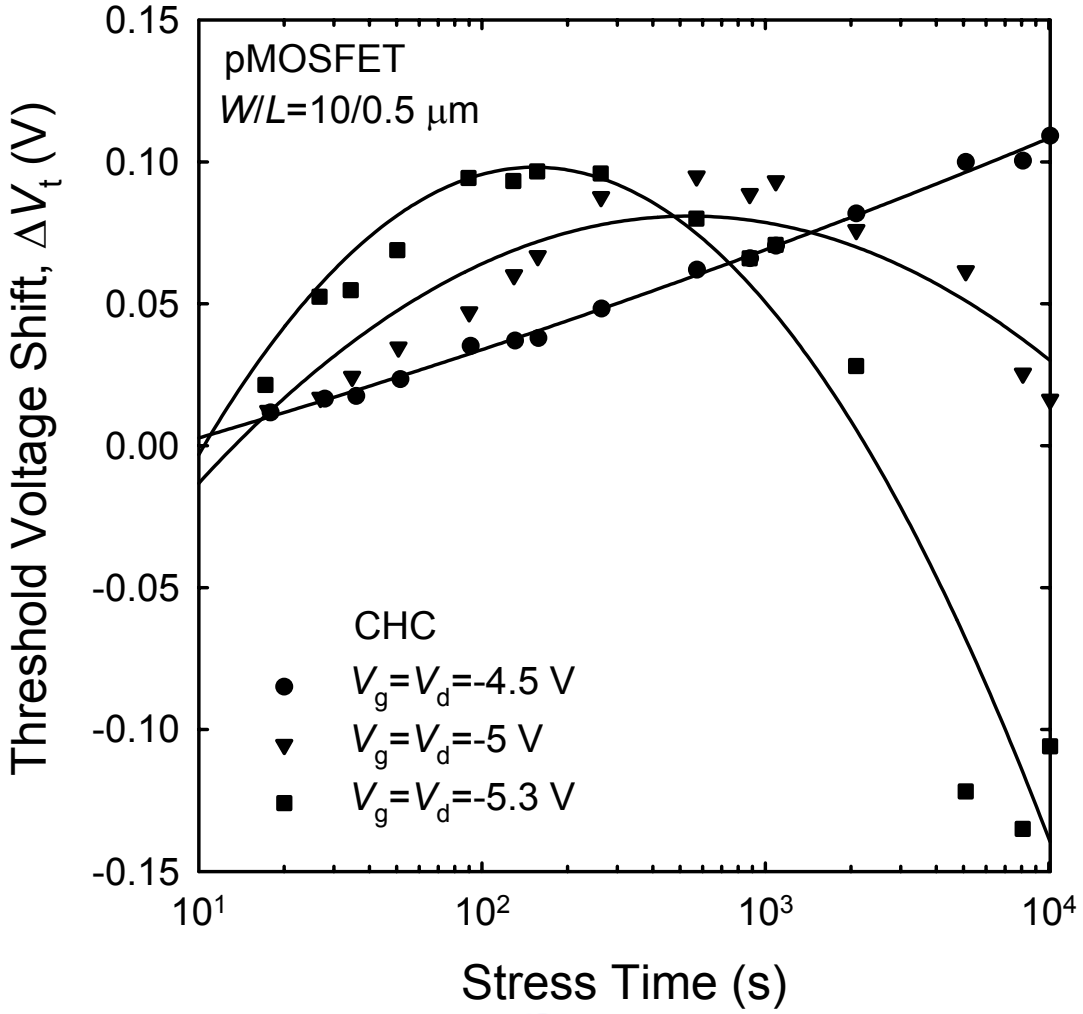

Fig. 4.18. The threshold voltage shift (ΔV_t) versus the stress time for the channel-hot-carrier stressing under various bias conditions of V_g = V_d = –4.5, –5, and –5.3 V.

Chapter 5

Channel Thickness Effect on Strained SiGe Channel pMOSFETs with Ultra-Thin (EOT = 3.1 nm) N_2O-Annealed SiN Gate Dielectric

5.1 Introduction

To enhance the performance of pMOSFETs, the silicon germanium (SiGe) layer has been introduced into the channel of pMOSFETs because (a) it has higher bulk carrier mobility than that of bulk Si, (b) the offset of valence band between SiGe and Si substrate leads to the quantum confinement effect of holes which also contributes the increase of hole mobility **[1]**, and (c) the hole mobility is further enhanced when the SiGe layer is deposited on top of Si substrate due to the induced compressive strained in the SiGe channel **[2]**, **[3]**. Although the SiGe channel devices have abovementioned advantages, however, the gate oxide formed by the conventional thermal oxidation process will cause Ge precipitates at the interface between SiGe and oxide, which will deteriorate the quality of gate oxide **[4]**. Therefore, one appreciable approach to prepare the gate dielectric for SiGe channel devices is using the deposition technique at lower temperature which can also prevent the relaxation of the strained SiGe layer. Recently, the ultra-thin silicon nitride (SiN) has been reported as the possible alternative of gate dielectrics for the SiGe channel pMOSFETs **[4]**, **[5]** owing to the advantages of suppressing the boron penetration, a larger dielectric constant, and better hot-carrier hardness **[6]**. Unfortunately, SiN films usually contain

a large amount of fixed oxide charges, which can cause the threshold voltage shift, and increase the interface state density to degrade the device performance **[7]**. Hence, N_2O-annealing has been reported to improve the qualities of the SiN layer and the SiN/Si interface by forming an oxygen-enriched interface (OI-SiN) **[8]**. In this paper, we employed the low temperature (800 ºC) N_2O-annealed SiN gate dielectric for fabricating the SiGe channel pMOSFETs. According to the results of electrical characteristics, we found an excellent interface quality, a considerably low subthresthold swing, and significant hole mobility improvement can be achieved for the SiGe channel pMOSFETs with the ultra-thin N_2O-annealed SiN gate dielectric.

5.2 Device Fabrication and Characteristics Measurement

The devices were fabricated on 6-inch (100) orientated Si wafers. After the standard LOCOS isolation being fabricated, the $Si_{0.85}Ge_{0.15}$ epitaxial layers with various thicknesses of 5, 15 and 30 nm were selectively deposited on top of the Si substrates by ultra-high vacuum chemical vapor deposition (UHVCVD) at 550 ºC. The SiGe layers were in-situ doped with phosphorus and the doping concentrations were 9×10^{17}, 1×10^{18}, and 4×10^{18} cm^{-3} for the thickness of 5, 15, and 3 nm, respectively according to the results of SIMS analysis shown in **Fig. 5.1**. After being cleaned by RCA process, the ultra-thin SiN gate dielectrics were deposited by low pressure CVD (LPCVD) furnace with dichlorosilane (DCS) and NH_3 at 780 ºC, and the rapid thermal annealing (RTA) at 800 ºC for 30 seconds in N_2O ambience immediately followed. The undoped 150 nm poly-Si deposition were performed by LPCVD furnace with silane (SiH_4) at 620 ºC and patterned by using lithography and etching process as the gate electrode. Then, the self-aligned source/drain extension

was implanted with BF_2 by a dosage of 1×10^{14} cm^{-2} at 10 keV. An oxide spacer was formed by etching isotropically the low temperature TEOS oxide (LTO), and the self-aligned gate and source/drain implantation were performed by implanting BF_2 with a dosage of 5×10^{15} cm^{-2} at 20 keV. After the substrate contact being defined and implanted to improve the body contact, the dopant activation by RTA at 900 ºC in N_2 ambience for 30 seconds was carried out. Then, the devices were passivated with 500 nm LTO oxide followed by a standard back-end-of-line (BEOL) contact and metallization processes. Finally the devices were annealed in a furnace with the forming gas at 400 ºC for 30 minutes before the electrical characteristics measurements.

The capacitance–voltage (*C–V*) characteristic of each capacitor was measured using an HP4284 LCR meter. The equivalent oxide thickness (EOT) of the gate dielectrics was obtained from the strong accumulation capacitance (EOT=$\varepsilon_{SiO_2}/C_{acc}$). The current–voltage (*I–V*) characteristics were measured by using a Keithley 4200 semiconductor characterization system.

5.3 Results and Discussion

Figure 5.2 shows the *C–V* characteristics of pMOSFETs with different strained SiGe channel thickness. The smaller value EOT of approximately 3.1 nm was obtained for the devices with thinner SiGe channels of 5 and 15 nm. The 30 nm SiGe channel device, however, depicts higher EOT value (3.5 nm). It is speculated that the faster deposition rate of SiN layer may be induced by the poor quality and/or the high strain energy of a thicker SiGe channel. In addition, the distortion of *C–V* curve for

the 30 nm SiGe channel device indicates more interface states did exist at the SiN/SiGe channel interface, and the shift of flat-band voltage (V_{fb}) is probably not only due to the higher oxide charges and interface states but also due to a slightly heavier doping concentration in the thicker SiGe channel which was evidenced by the SIMS profiles.

The I_d–V_g and I_d–V_d characteristics are shown in **Fig. 5.3** and **Fig. 5.4**. The threshold voltages of the devices with thinner strained SiGe channel (5 and 15 nm) are almost identical and they are smaller than that of the 30 nm SiGe channel device because of their smaller V_{fb} and lighter channel doping concentration. In addition, the subthreshold swing of as low as 68 mV/dec can also be realized in the devices with 5 and 15 nm stained SiGe channel. As strained SiGe channel increases up to 30 nm, the subthreshold swing increases drastically. On the other hand, the thin SiGe channel devices demonstrate higher driving currents than the 30-nm SiGe channel device for various overdrive gate biases (V_g–V_t) as well as **Fig. 5.4** shows. **Figure 5.5** depicts the results of charge pumping measurement for extracting the interface state density (the extracted interface state density is shown in **Fig. 5.6**). Obviously, the charge pumping current (I_{cp}) of the 30-nm SiGe channel device is much higher than that of the counterparts, and it means that the 30-nm SiGe channel device has a poor interface because the charge pumping current is proportional to the amount of interface states. The negative shift of the I_{cp} for the 30-nm SiGe channel device also indicates that positive charges are induced in the gate dielectric. These results are consistent with the information obtained from the C–V and I_d–V_g curves for the 30-nm SiGe channel device. **Figure 5.6** illustrates the comparison of the interface state density (N_{it}) extracted by charge pumping technique and the subthreshold swing (S) for all samples. From the I_{cp} data previously shown in **Fig. 5.5**, it is expected that the device with 30 nm SiGe channel may show nearly one order of magnitude higher N_{it} than the other

devices. Besides, N_{it} and S show almost identical trends, and this is in a good agreement with the well-known results, i.e. the lower the interface state density, the lower the subthreshold swing. We believe that the significant increases in subthreshold swing and the interface state density should come from the increase of the dislocation density in the devices with 30 nm SiGe channel thickness **[9]**. Therefore, we can conclude that with the combination of the sufficiently thin (<30 nm) strained SiGe channel layer and ultra-thin N_2O-annealed SiN gate dielectric, we can obtain a pMOSFET with excellent ON/OFF switching characteristics and performance.

Figure 5.7 and **Fig. 5.8** show the results of the gate-induced drain leakage (GIDL) and the junction leakage for all devices, respectively. We can clearly see that for the thinner SiGe channel devices, the GIDL and the junction leakage are almost the same and both are one order of magnitude lower than that for 30 nm strained SiGe channel device. These results further strengthen our previous speculation that a higher dislocation density in 30 nm SiGe channel layer is the culprit of the degraded characteristics.

The normalized transconductance ($G_m \times T_{ox}$) characteristics of all splits are shown in **Fig. 5.9**. The $G_m \times T_{ox}$ characteristics are almost identical for 5 and 15 nm SiGe channel devices and they are not only higher than that of the Si channel device due to the compressive strain but also superior than that of the device with 30 nm channel thickness because of their lower interface state and dislocation density at low gate voltages. However, at high gate voltages, the $G_m \times T_{ox}$ of the 30 nm SiGe channel pMOSFET becomes larger because higher level of carrier trapping at the interface traps may screen the surface scattering through coulombic shielding at high gate bias **[7]**, **[10]–[13]**. The effective hole mobility for all devices are also shown in **Fig. 5.10**. As expected **[14]**, **[15]**, the mobility improvement is clearly observed for all SiGe

devices with respect to the Si channel device owing to the fact that the induced compressive strain and the quantum confinement of holes in the SiGe channel are both helpful for improving the hole mobility. Because N_2O-annealing may introduce oxygen into the interface to form an oxygen-enriched interface **[8]**, it may also probably cause oxidation of SiGe layer near the interface. Consequently, the hole mobility will be additionally enhanced with slightly increasing the Ge content of the SiGe channel **[16]**, **[17]**. For the devices with the SiGe channel thinner than 15 nm, significant hole mobility improvement (more than 50 % enhancement as compared to the Si channel device) can be achieved in the linear operation; while the device with 30 nm SiGe channel suffers the mobility degradation in the low voltage regime due to the higher interface defect density and bulk dislocation density and gains slight enhancement of the hole mobility in the high voltage regime owing to the screening effect on the surface scattering. Besides, the mobility of the 5 nm SiGe channel device is slightly larger than that of the 15 nm SiGe channel counterpart which is due to the higher surface compressive strain for the thinner strained SiGe layer. Therefore, taking into account the relatively high leakage current and poor subthreshold swing, the thickness of the strained SiGe channel should be optimized less than 30 nm.

5.4 Summary

We have investigated the electrical properties of the strained $Si_{0.85}Ge_{0.15}$ pMOSFETs with various SiGe channel thickness of 5, 15, and 30 nm and the ultra-thin N_2O-annealed SiN gate dielectric. A thin EOT of 3.1 nm and an excellent subthreshold swing of 68 mV/dec have been obtained for the devices with 5 and 15

nm SiGe channel, and the density of interface state and dislocation are also shown even lower than that of the 30 nm SiGe channel device which are supported by the GIDL and junction leakage measurements. Moreover, with respect to the thinner SiGe channel devices, the 30 nm SiGe channel pMOSFET has been demonstrated having degradation in transconductance at low gate voltages because of its higher density of interface state and dislocation; at high gate voltages, the transconductance is, however, improved because of the screening effect on the surface scattering. On the other hand, the enhancement in the effective hole mobility caused by the compressive strain and the quantum confinement effect for all SiGe channel pMOSFETs as compared with the Si channel device has also been displayed. Finally, we have proposed the well-performed pMOSFETs with suitably thin (<30 nm) SiGe channel and ultra-thin N_2O-annealed SiN gate dielectric and also demonstrated their potential for the advanced sub-100 nm device technology and applications.

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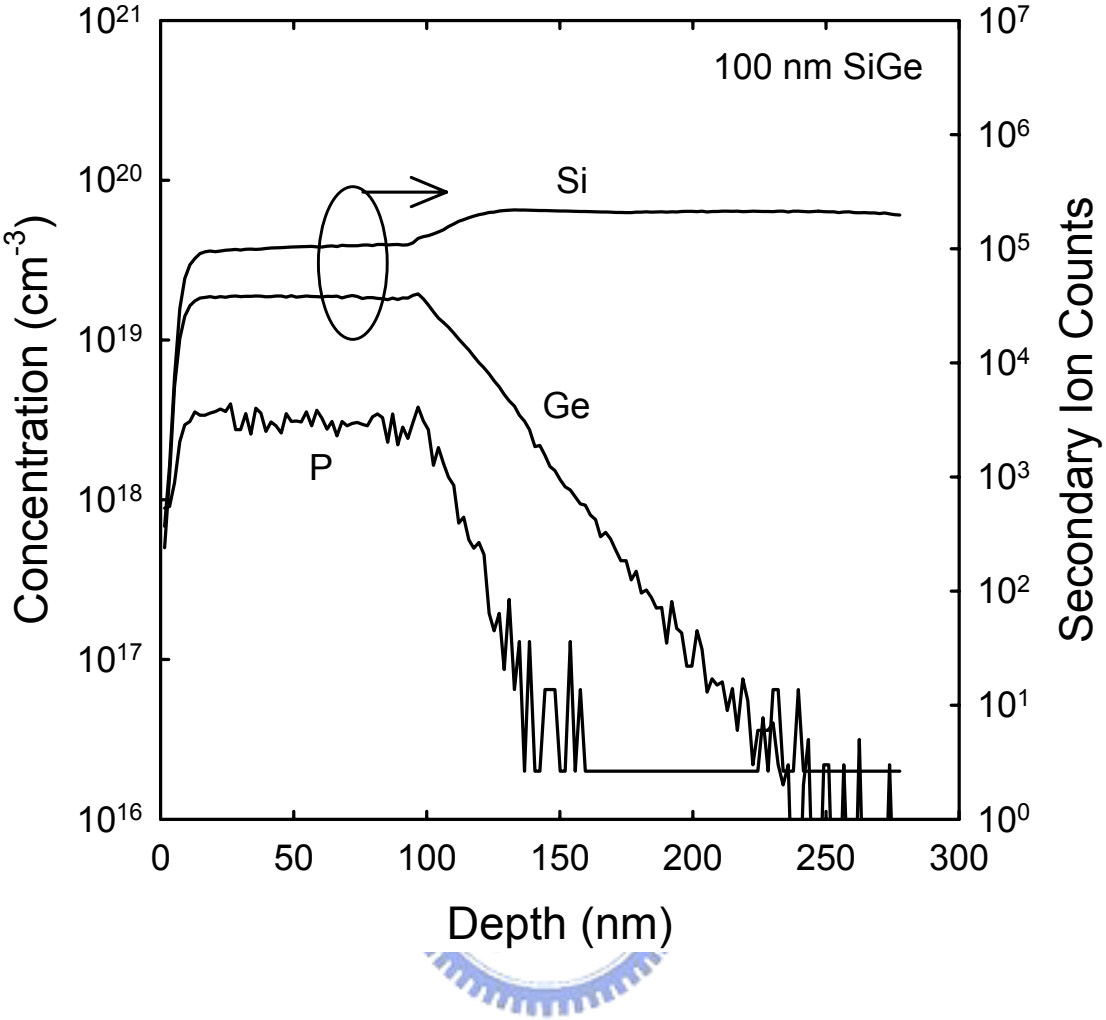

Fig. 5.1. SIMS profiles of the SiGe channel in-situ doped with phosphorus.

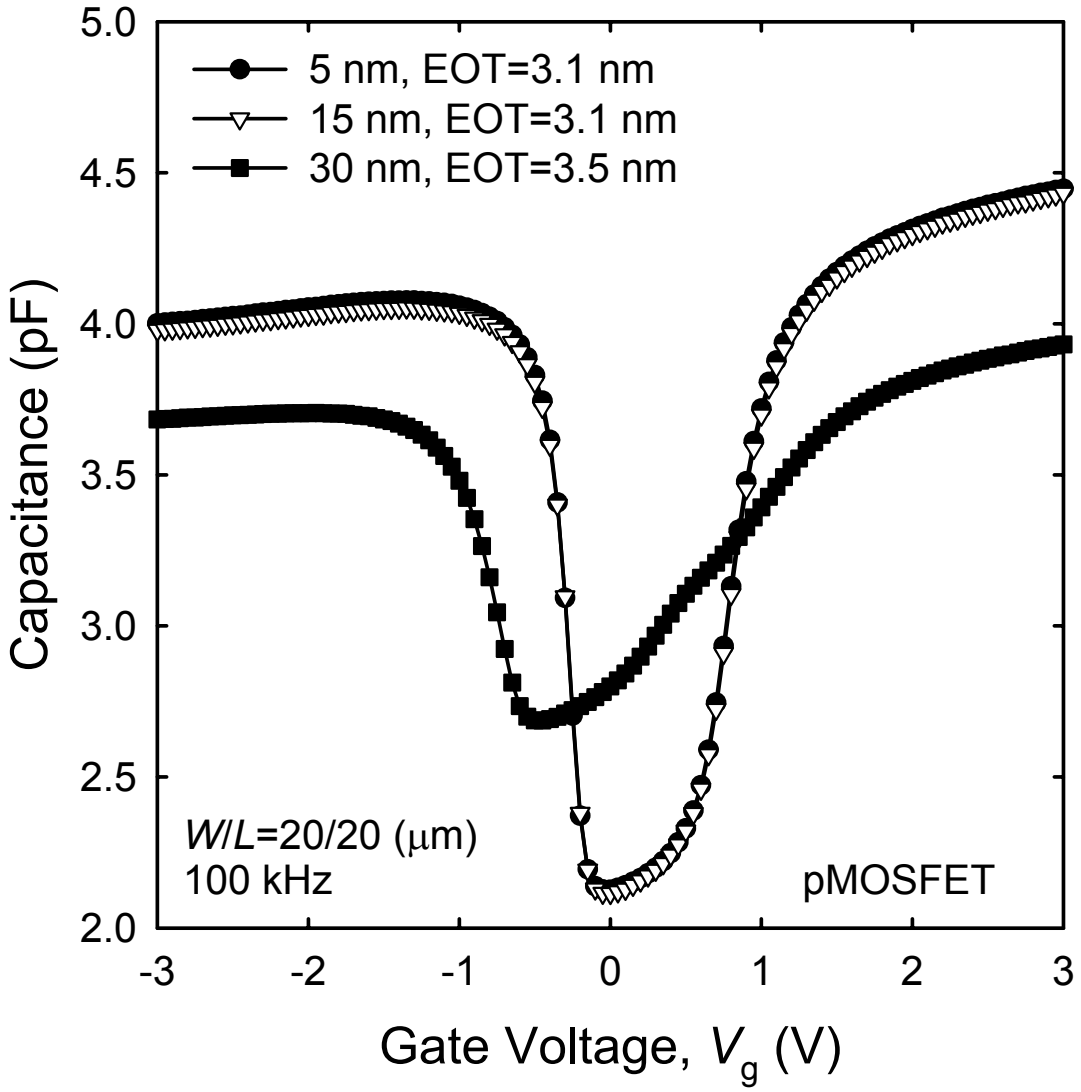

Fig. 5.2. The *C–V* characteristics of the pMOSFETs with different SiGe channel thickness.

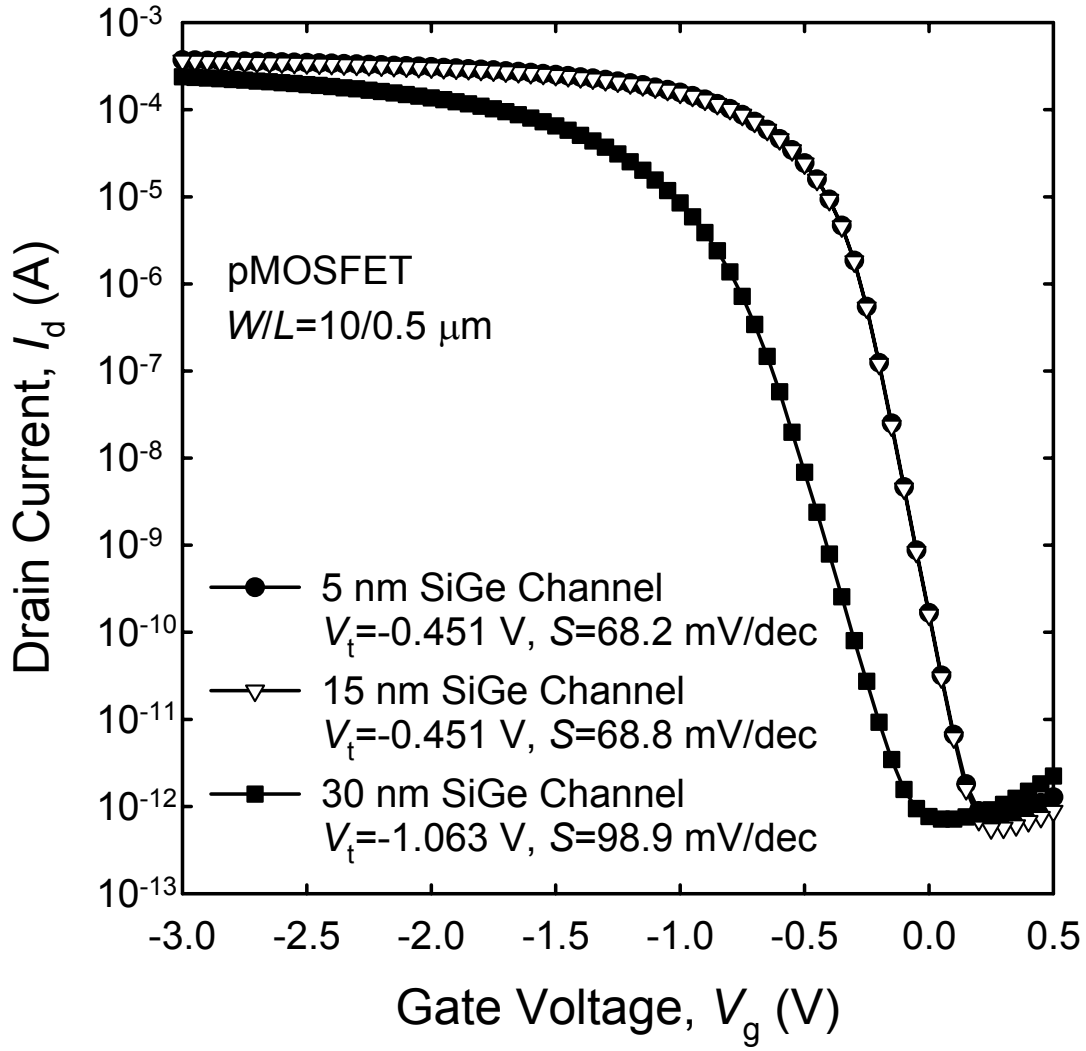

Fig. 5.3. The I_d–V_g characteristics of the pMOSFETs with different SiGe channel thickness.

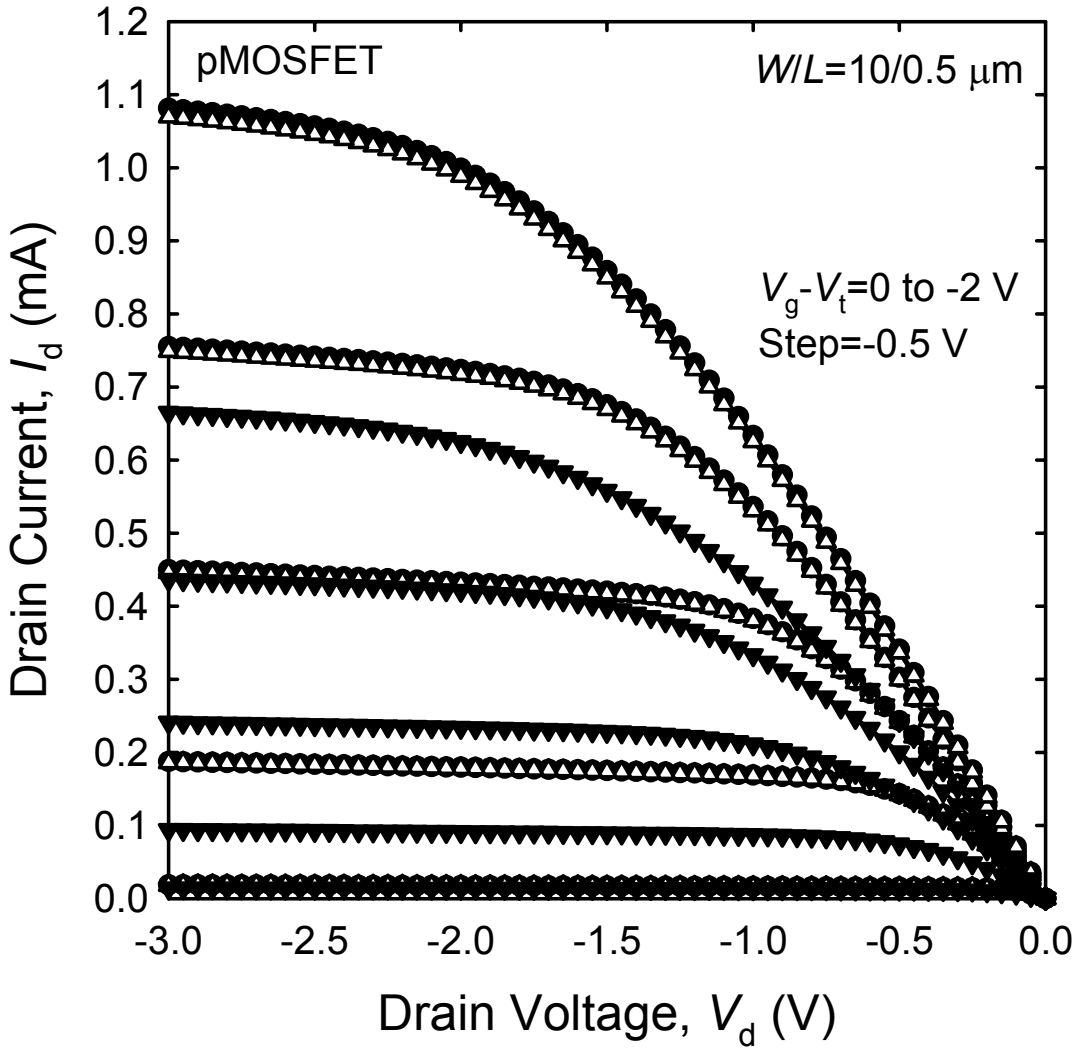

Fig. 5.4. The I_d–V_d characteristics of the pMOSFETs with different SiGe channel thickness.

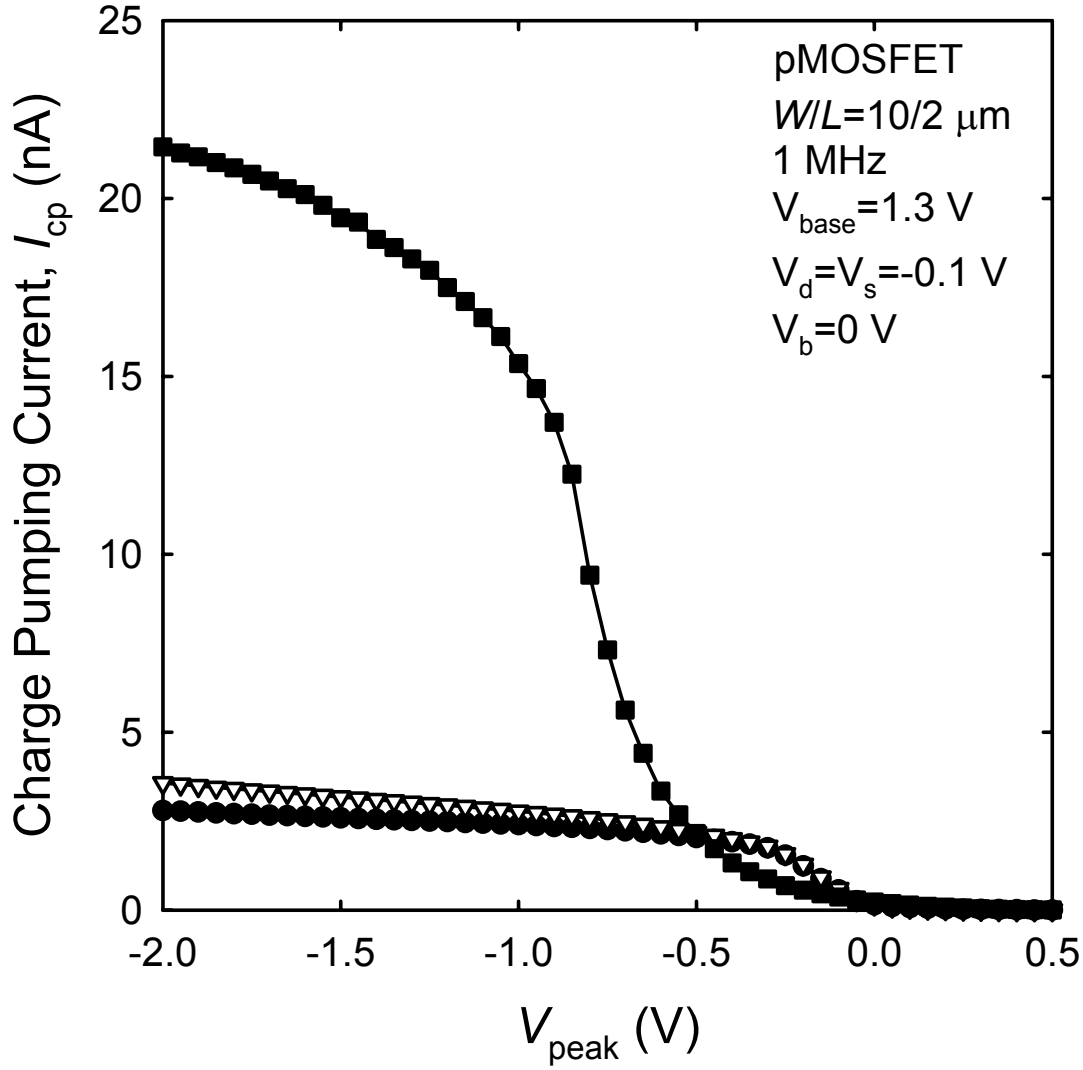

Fig. 5.5. The charge pumping currents of the the pMOSFETs with different SiGe channel thickness.

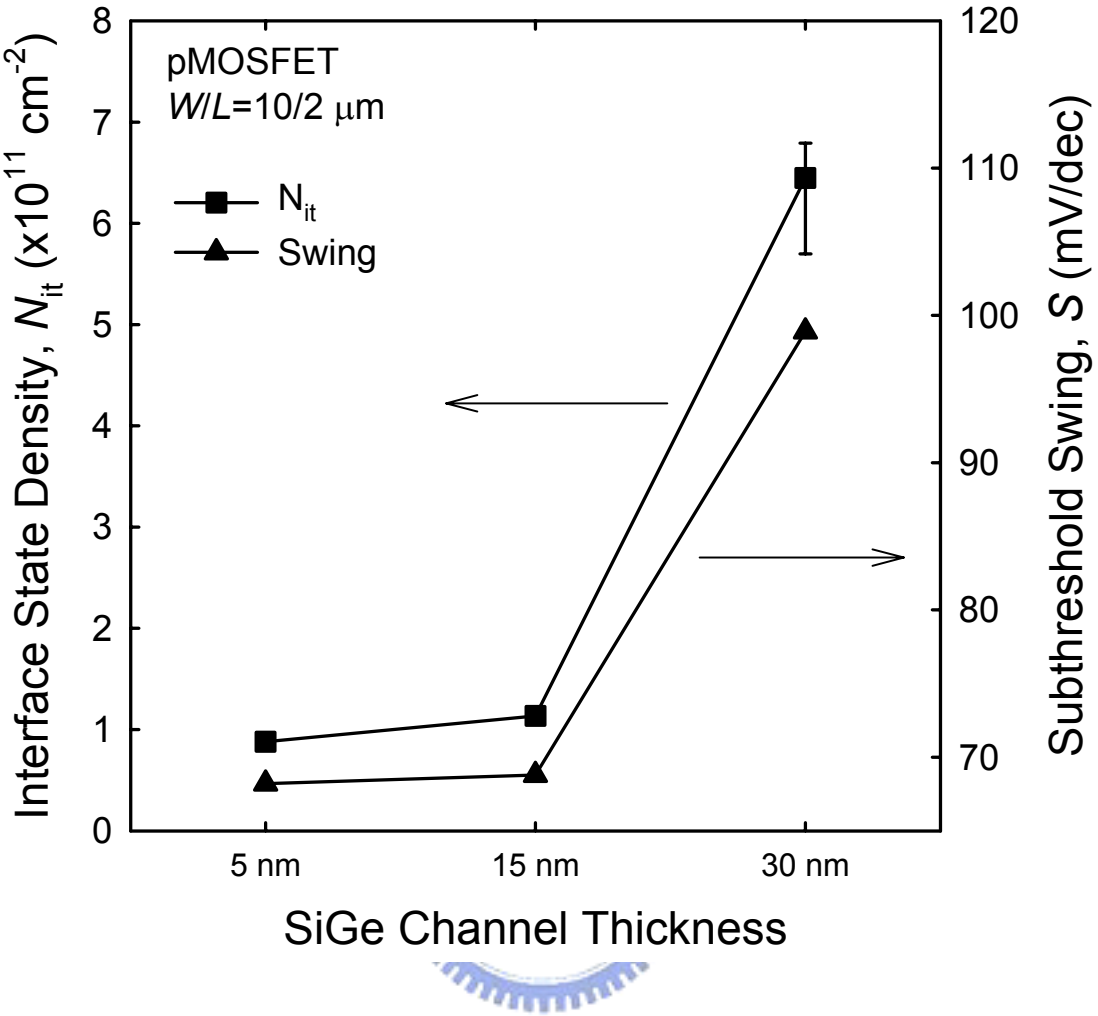

Fig. 5.6. The interface state density determined by the charge pumping technique and the subthreshold swing of pMOSFETs with different SiGe channel thickness.

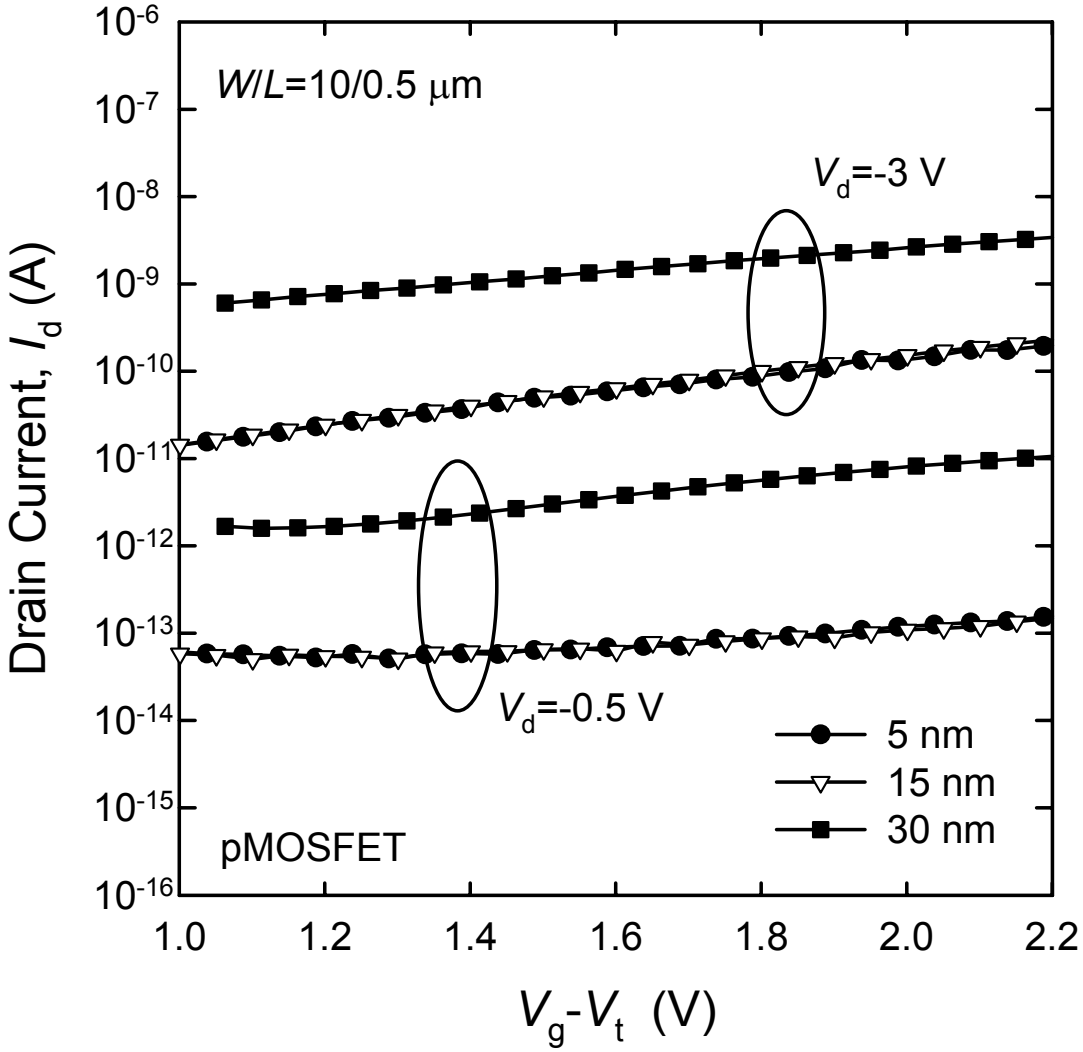

Fig. 5.7. The gate-induced-drain-leakage (GIDL) of the pMOSFETs with different SiGe channel thickness.

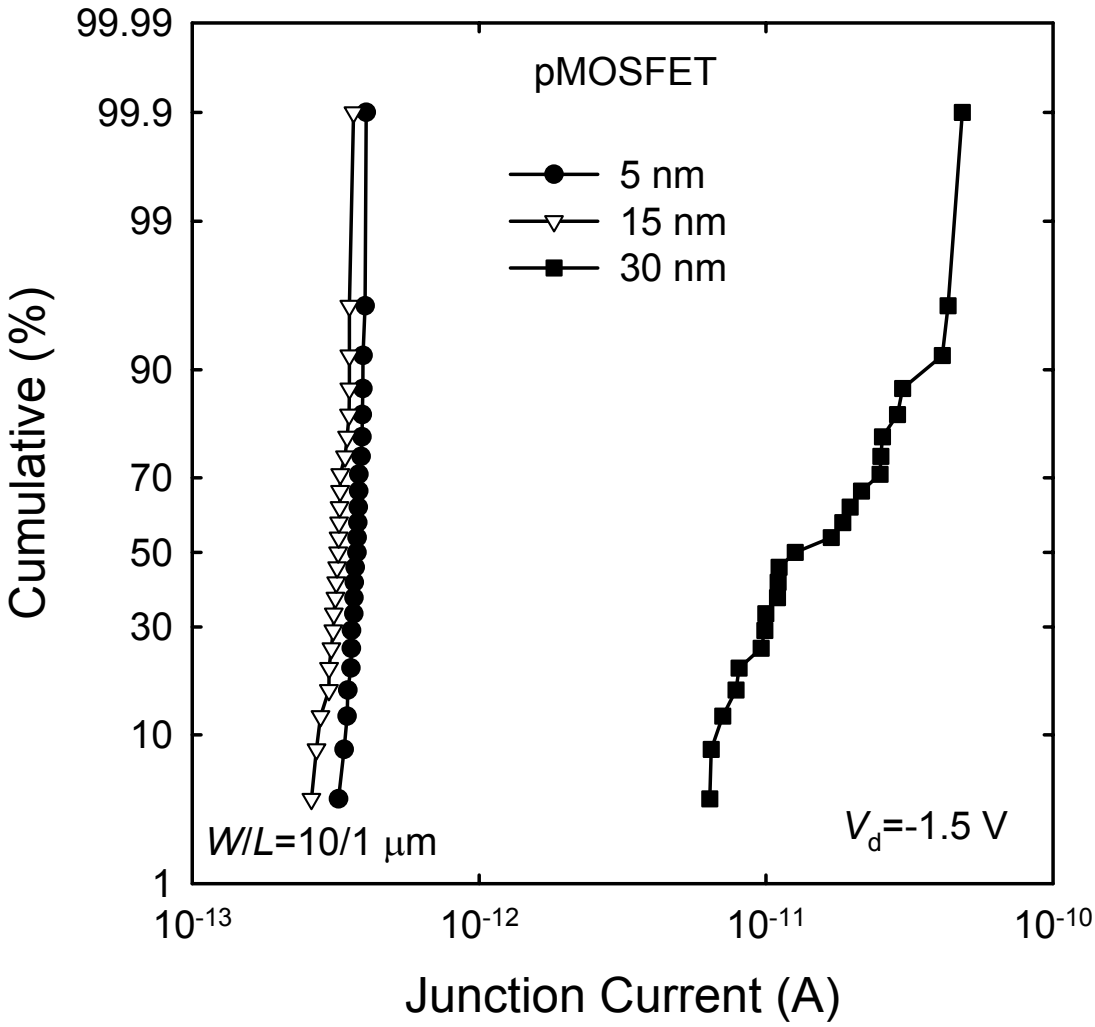

Fig. 5.8. The junction leakage of the pMOSFETs with different SiGe channel thickness.

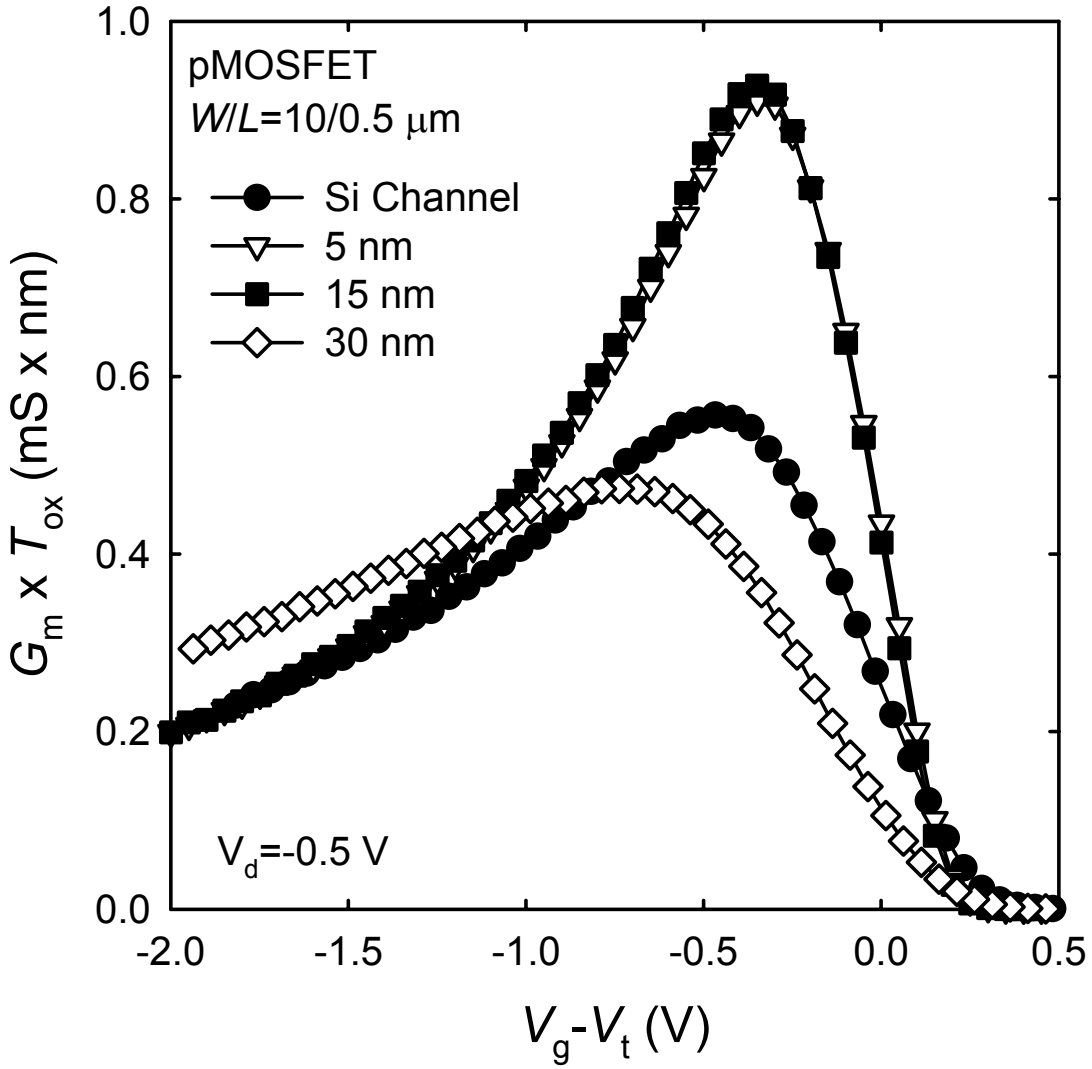

Fig. 5.9. The transconductance of the Si channel pMOSFET and the SiGe channel MOSFETs with different SiGe layer thickness.

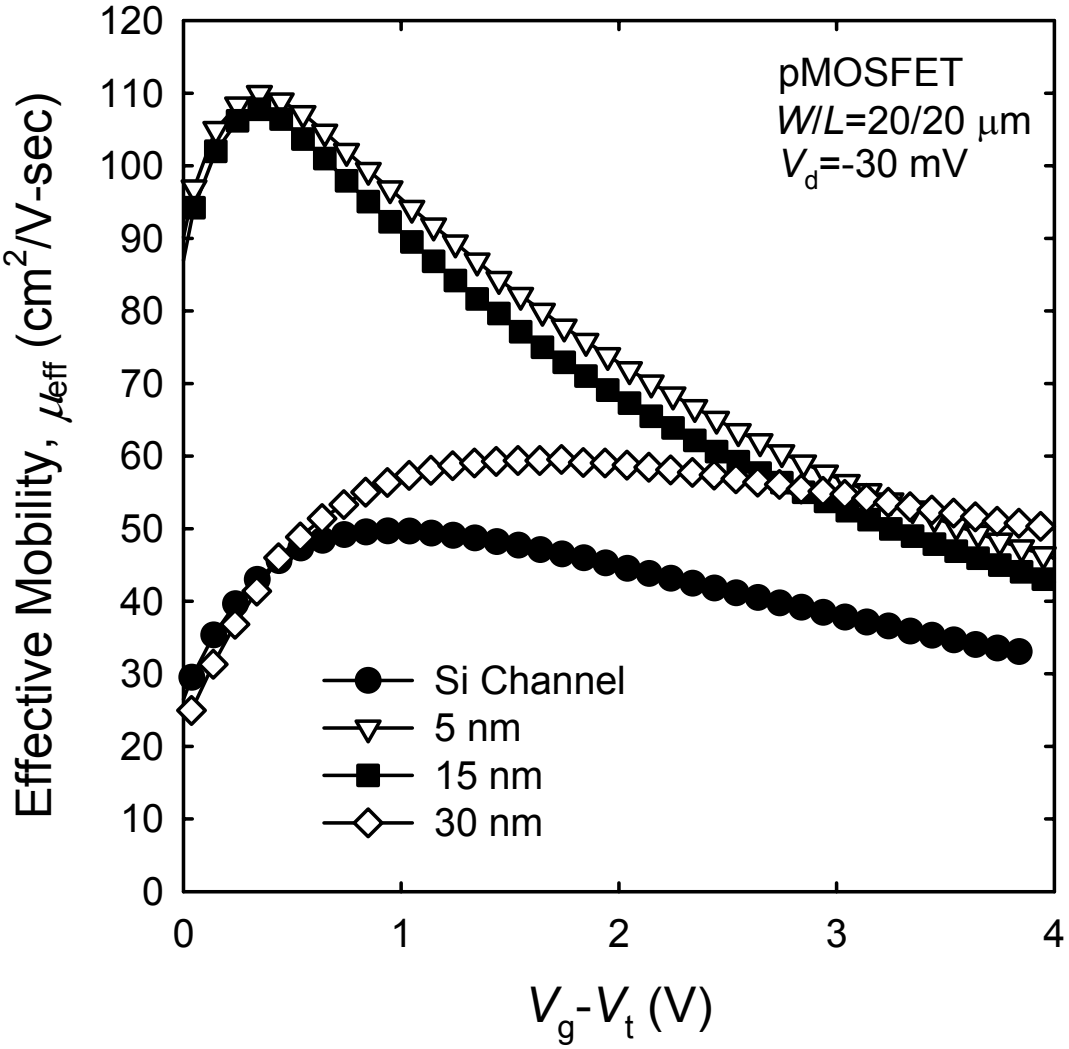

Fig. 5.10. The effective hole mobility of the Si channel pMOSFET and the SiGe channel MOSFETs with different SiGe layer thickness.

Chapter 6

Electrical Characteristics of Ultra-Thin HfO_2 Gate Dielectrics Prepared Using Different Pre-Deposition Surface Treatments

6.1 Introduction

As the gate oxide thickness of metal–oxide–semiconductor (MOS) devices is scaled down to below 1.5 nm **[1]**, the tunneling current through gate dielectrics and their reliability become serious problems **[2]**. Therefore, high-dielectric-constant (high-k) materials, such as the ZrO_2-based **[3]**, HfO_2-based **[4]**, and Al_2O_3-based **[5]** metal oxide insulator, have received considerable attention as alternative dielectric materials. These metal oxide insulators are able to significantly suppress the leakage current relative to that of traditional SiO_2-based dielectrics having the same equivalent oxide thickness (EOT) because of their greater physical thickness. Among these candidates, HfO_2 and its silicate not only have relatively high dielectric constants and wide band gaps but they also have been demonstrated to display impressive thermal stability when in contact with the silicon substrate **[6]**. Therefore, HfO_2-based insulators are promising candidates for the generation of sub-1.5-nm gate dielectrics. Although several groups have demonstrated in recent years the excellent electrical properties of MOS capacitors featuring HfO_2-based gate dielectrics **[7]–[9]**, there still remain many challenging issues, such as the formation of the interfacial layer and the degradation of mobility in MOSFET devices, that require further investigation.

Recently, traps existing in high-k gate dielectrics have been demonstrated as another issue of concern because their presence can cause threshold voltage instability **[10]** and degradation in their reliability **[11]**.

To provide a high-quality interface, surface treatment — e.g., forming an SiO_2, SiON, or SiN layer — is a viable approach toward eliminating the formation of an excessively thick interfacial layer. Surface nitridation can not only result in a good barrier for interfacial reaction and dopant diffusion but it also can alleviate the issue of leakage current without increasing the equivalent oxide thickness; in addition, it can also provide better thermal stability and reliability **[12]**, **[13]**. Forming a SiO_2 layer by thermal oxidation or chemical oxidation beneath an HfO_2 film has also been reported as an effective method for reducing the leakage current and improving the quality of the interface **[14]**. Despite the advantages mentioned above, however, both techniques have their drawbacks. For example, nitrogen incorporation may induce extra oxide charges in the gate dielectric and then cause a shift in the flat-band voltage **[13]**. On the other hand, the low-k character of the SiO_2 layer would inevitably cause an increase in the EOT and seriously limit the gate oxide scaling. In this study, therefore, we have investigated and compared the electrical characteristics of capacitors having HfO_2 gate dielectrics that have been deposited onto the silicon substrate using different surface treatments (HF-dipped, NH_3-annealed, and RTO-treated). After measuring the capacitance–voltage (C–V) and current–voltage (I–V) characteristics, the values of the equivalent oxide thickness (EOT), flat-band voltage (V_{fb}), hysteresis, and leakage current can be extracted. Moreover, we have also investigated the dependence of hysteresis on the magnitude of the initial inversion bias (V_{inv}), temperature, and measuring frequency. We have found that the hysteresis width varies exponentially with respect to both the initial inversion bias and temperature, but it remains less sensitive to the measuring frequency. Interestingly,

this bias-and-temperature-dependent hysteresis behavior can be described in the form $C(T)\cdot\exp(R_v V_{inv})$. Finally, we have deduced that the mechanism responsible for the current conduction in these gate dielectrics involves trap-assisted tunneling (TAT); we have also calculated the corresponding parameters of this model, which are presented.

6.2 Device Fabrication and Characteristics Measurement

We fabricated n-type metal–insulator–silicon (NMIS) capacitors that have standard LOCOS isolation on p-type (100)-oriented 15–25 ohm-cm silicon substrates. After cleaning using the RCA process, we split the wafers into three different groups with each one being subjected to a different surface treatment processes prior to HfO_2 deposition: i.e., either the HF-dipped, NH_3-annealed, or RTO-treated process. The HF-dipped wafers were prepared by immersing the wafers in a dilute HF (100:1) solution and then drying them directly without rinsing in DI water. The NH_3 annealing process was performed by subjecting the wafers to a pure NH_3 atmosphere at 800 °C for 60 min in an LPCVD system. The RTO treatment process was performed by placing the wafers in a rapid thermal oxidation (RTO) system, featuring an O_2 source, at 800 °C for 30 s, followed by in situ N_2 annealing at 1000 °C for 30 s. The HfO_2 films were deposited by atomic vapor deposition (AVD) using an AIXTRON Tricent® system at a substrate temperature of 500 °C. To improve the film quality, all of the samples were subjected to post-deposition annealing (PDA) under N_2 at 600 °C for 30 s. A 200-nm layer of polycrystalline silicon (poly-Si) was deposited successively by LPCVD, and then it was patterned by lithography and etching processes to form the gate electrode. Dopant activation by rapid thermal annealing (RTA) at 900 °C for 30 s under an N_2 atmosphere was followed by poly-Si gate

implantation of As using a dosage of 3×10^{15} cm^{-2} at 20 keV. Finally, the reverse side of each substrate was coated with a 500-nm-thick Al layer to achieve a conductive contact for electrical measurements.

The capacitance–voltage (C–V) characteristic of each capacitor was measured using an HP4284 LCR meter. The equivalent oxide thickness (EOT) of the gate dielectrics was obtained from the strong accumulation capacitance (EOT = $\varepsilon_{SiO_2}/C_{acc}$) and the hysteresis was determined by the shift of the flat-band voltage (V_{fb}). The current–voltage (I–V) characteristics were measured by using a Keithley 4200 semiconductor characterization system; from these measurements, it became possible to examine the leakage current and the conduction mechanism.

6.3 Results and Discussion

6.3.1 TEM and XPS Analysis

Figure 6.1 shows the cross sections of the HfO_2 films with different surface treatments. Form the TEM pictures, we can evaluate the thickness of the interfacial layers (IL) for all samples after completing fabrication process, and they are about 1.5, 1.2 and 2.0 nm for the HF dipping, NH_3 nitridation, and RTO annealing surface treatments, respectively. The obtained thinner interfacial layer for the NH_3-annealed sample is due to the fact that SiN_x is a good barrier against atom diffusion than the other interfacial layer materials **[15]**, **[16]**. Consequently, the formation of interfacial layer can be suppressed by blocking the oxygen diffusion into the interface. The spectra of XPS analysis for all samples are shown in **Fig. 6.2**. Obviously, the peak of binding energy is independent of the surface treatments. It reveals that the surface

treatment process will not cause the variation of the HfO_2 composition.

6.3.2 *C–V* and *I–V* Characteristics

The electrical characteristics of NMIS capacitors with respect to their various surface treatments are shown in **Figs. 6.3** and **6.4**. **Figure 6.3** displays the high-frequency (100 kHz) *C–V* curves. All of the splits depict the presence of positive charges in the dielectrics because negative shifts in flat-band voltages (V_{fb}) are clearly observed when compared to the ideal values of V_{fb}, which have been determined by simulation **[17]**. The equivalent oxide thicknesses extracted from each maximum accumulation capacitance (EOT = $\varepsilon_{SiO_2}/C_{acc}$) are 3.4, 3.2, and 3.9 nm for the capacitors prepared using the HF-dipped, NH_3-annealed, and RTO-treated surface treatment processes, respectively. According to previous reports, the interfacial layer for the HF-dipped sample is hafnium-silicate-like **[18]**, **[19]**, for the NH_3-annealed sample it is SiN_x **[15]**, and for the RTO-treated one it is SiO_2 **[20]**. The fact that we obtained the lowest value of EOT for the NH_3-annealed sample suggests that SiN_x is the most effective of the three in suppressing the growth of an interfacial layer. This finding might be attributed to the fact that SiN_x is much more dense barrier against atom diffusion than are the other interfacial layer materials **[15]**, **[16]**. A larger negative shift in V_{fb} indicates, however, that more positive charges are induced upon introducing the nitrogen atoms into the gate dielectric **[13]**, **[21]**. **Figure 6.4** exhibits the characteristics of the leakage currents as a function of voltage. The magnitudes of the leakage currents for the samples subjected to pre-deposition NH_3 nitridation and RTO surface treatments are more than one order of magnitude lower than that of the HF-dipped sample. **Figure 6.5** displays the distributions of leakage currents at a voltage of –2.5 V. Obviously, all of the distributions are quite uniform, which implies

the resultant trend in the values of the leakage current is not a specific case. In the case of the RTO surface-treated sample, the increase in physical thickness can account for the dramatic reduction in leakage current, but such an argument does not explain the reduction of leakage current obtained in the case where NH_3 surface treatment was performed because the value of the EOT of the NH_3-annealed dielectric is even lower. We speculate that the effectiveness of SiN_x in blocking oxygen diffusion is helpful in improving the quality of the overlying HfO_2 thin film by reducing the density of electron traps (or oxygen vacancies). Therefore, NH_3 surface treatment not only can suppress the growth of an interfacial layer but also result in the reduction of the leakage current of the gate dielectric **[12]**, **[13]**, **[15]**.

6.3.3 Hysteresis

Figure 6.6 demonstrates the hysteresis behavior of the capacitors formed using the different substrate surface treatment procedures; the hysteresis width is defined by the flat-band voltage shift (ΔV_{fb}). We observe clearly that the hysteresis width depends strongly on the sweeping voltage; it increases upon raising the initial inversion bias (V_{inv}). It is believed that a higher initial inversion bias (inversion-to-accumulation) would lead to more electrons being injected from the inversion layer and becoming trapped in the gate dielectric and, as a consequence, this process would result in a larger positive shift in the flat-band voltage. These results are consistent with the results of a previous study reported by Morioka *et al* **[22]**. The curves in the opposite direction (accumulation-to-inversion) were observed, however, to be rather insensitive to the sweeping bias. This trend reveals that these traps are more likely to be located near the Si substrate and can be detrapped easily during upon sweeping in the opposite direction. These kinds of traps are referred to as the inner-interface states

existing between the HfO_2 layer and the interfacial layer beneath it **[22]**, **[23]**. The hysteresis widths measured under the conditions of V_{acc} = –3 V and V_{inv} = +3 V are 0.35, 0.4, and 0.8 V for the HF-dipped, NH_3-annealed, and RTO-treated samples, respectively. As we discussed above, the reason for the larger hysteresis width observed for the RTO-treated capacitor, relative to its counterparts, is due to the higher density of electron traps at the HfO_2/SiO_2 interface. On the other hand, the positive charges present in the SiN_x layer are not as efficient at trapping at the inner-interface and, therefore, we observed only a slight increase in the hysteresis width.

The relationship between the hysteresis and the initial inversion bias is shown in **Fig. 6.7**. Interestingly, the hysteresis follows an exponential law with V_{inv} in the form $A \cdot \exp(R_v V_{inv})$, where R_v is defined as a reciprocal voltage constant. The NH_3-annealed and RTO-treated samples not only display larger hysteresis, but they also possess higher values of R_v relative to that of the HF-dipped sample. Because the hysteresis is caused primarily by the electrons trapped in the gate dielectric, the value of R_v should, therefore, be strongly dependent on the number of electron traps. According to this result, we infer that the hysteresis is caused mainly by filling of the as-fabricated traps because the inversion charge density varies exponentially with the surface potential **[24]**. This conclusion agrees well with our experimental results. On the other hand, the hysteresis is also a function of temperature, as illustrated in **Fig. 6.8**. We observe that the hysteresis decreases as the temperature is elevated. There are two reasons to explain this observation. Firstly, since the capture cross section of the electron traps would decrease at higher temperatures **[10]**, **[25]**, the electrons would not be trapped as easily upon elevating the temperature. Secondly, at higher temperatures, the trapped electrons in the gate dielectric would have a higher probability of escaping from the trap sites and, hence, the hysteresis becomes less

significant. The activation energy (E_h) extracted from the Arrhenius plot is almost identical (ca. 0.092 eV) for each sample. Therefore, we speculate that the hysteresis behavior in high-k materials is predominated essentially more by the number of electron traps rather than by the energy distribution of the electron traps because the temperature has the same effect (it causes electrons to detrap from the trap sites) on the hysteresis of each sample. The number of electron traps in the gate dielectric, however, is very sensitive to the fabrication process followed. These results can be verified by our experimental data. From the results presented in **Figs. 6.7** and **6.8**, we describe the hysteresis behavior as follows:

At a given temperature, the hysteresis width can be written as

$$hysteresis\ width = A \cdot \exp(R_v V_{inv}) \tag{6.1}$$

while at a given inversion bias, it can be described as

$$hysteresis\ width = B \cdot \exp(E_h / kT) \tag{6.2}$$

where A and B are constants that depend strongly on the surface treatment process that was employed. Under conditions of V_{inv} = +3 V at T = 300 K, we should obtain the same hysteresis width from both **Eqs. (6.1)** and **(6.2)**. Thus, we can obtain

$$A \cdot \exp(3R_v) = B \cdot \exp(E_h / 0.026), \tag{6.3}$$

and then

$$E_h = 0.026 \ln(A / B) + 0.078 R_v . \tag{6.4}$$

Apparently, as **Eq. (6.4)** states, the value of E_h follows a linear relationship with respect to R_v. **Table 6.1** summarizes the data obtained for the values of A, B, ln(A/B), R_v, and E_h for all of the samples. The values of E_h in **Table 6.1** derived from **Eq. (6.4)** coincide quite well with those extracted from the experimental data in **Fig. 6.8**. Hence, we conclude that the hysteresis behavior in Hf-based high-k materials can be modeled appropriately by

$$hysteresis\ width = C(T) \cdot \exp(R_v V_{inv}) \tag{6.5}$$

where $C(T)$ is an exponential function of temperature related to an activation energy.

Figure 6.9 presents the results of analyzing the hysteresis as a function of the C–V measuring frequency. We observe that, for each sample, the hysteresis width changes insignificantly upon increasing the frequency (from 5 kHz to 1 MHz). This finding indicates that the electron traps that are responsible for the hysteresis behavior can be classified as slow traps in the gate dielectric, as has been reported previously **[26]**, because the electrons are not trapped easily when measured at higher frequencies.

6.3.4 Conduction Mechanism

The mechanisms previously reported for the leakage currents in MIS capacitors that have high-k gate dielectrics are Fowler–Nordheim tunneling (FN) **[27]**, trap-assisted tunneling (TAT) **[28]**, and Poole–Frenkle emission (PF) **[7]**, **[29]**, **[30]**. So far, the dominating mechanism is still an issue under debate because the conduction mechanism for the high-k films might be process dependent; this phenomenon explains why different conclusions have been drawn by different groups. Nevertheless, we have investigated (shown in **Fig. 6.10**) our experimental data of leakage currents, which are temperature dependent (20–125 °C). In an attempt to clarify the dominant current conduction mechanism in our films, in **Fig. 6.11** we have plotted the leakage currents as a function of reciprocal temperature for two different applied voltages. Clearly, the leakage currents are more strongly dependent on temperature at low voltage, with a weaker dependence observed at higher voltage. This trend is quite consistent with the results described from previous studies **[28]**. Therefore, we believe that the conduction mechanism in our samples is also be dominated by trap-assisted tunneling (TAT) at low gate biases ($V_g < 2$ V).

According to the trap-assisted tunneling model in the low-voltage range **[28]**, the gate current density should be defined by the expression

$$J_g \sim \exp[(qV_{IL} - \phi_1 + \phi_2 + \phi_t)/kT] \sim \exp(-E_a/kT) \tag{6.6}$$

where V_{IL} is the voltage across the interfacial layer, ϕ_1 is the barrier height between the Si substrate and the interfacial layer, ϕ_2 is the barrier between the interfacial layer and HfO_2, ϕ_t is the effective energy of the electron traps with respect to the conduction band edge of the HfO_2 layer, and E_a is the activation energy. Consequently, the effective electron trap energy, ϕ_t, can be extracted from the activation energy, which is obtained from the slope of the Arrhenius plot of the leakage current if the values of V_{IL}, ϕ_1, and ϕ_2 are given.

For a stacked gate dielectric, it is well-known that

$$1/C_T = 1/C_{hk} + 1/C_{IL} \tag{6.7}$$

where C_T is the total accumulation capacitance, C_{hk} is the capacitance of the HfO_2 film, and C_{IL} is the capacitance of the interfacial layer. Hence, we can derive the equation

$$\frac{EOT}{\varepsilon_{ox}} = \frac{t_{hk}}{\varepsilon_{hk}} + \frac{t_{IL}}{\varepsilon_{IL}} = \frac{t_{hk}}{\varepsilon_{hk}}\left(1 + \frac{\varepsilon_{hk} t_{IL}}{\varepsilon_{IL} t_{hk}}\right), \tag{6.8}$$

where ε_{ox}, ε_{hk}, and ε_{IL} are the dielectric constants of SiO_2, HfO_2, and the interfacial layer, respectively, and t_{hk} and t_{IL} are the thicknesses of the HfO_2 and interfacial layers, respectively. The values of t_{hk} and ε_{hk} can be obtained by considering the TEM analysis, C–V measurements, and quantum mechanical effects (in our case, $t_{hk} \sim 6.5$ nm and $\varepsilon_{hk} \sim 18$). Because the stacked gate voltage, V_{stack}, is almost equal to the applied gate voltage, V_g, under positive bias ($V_{stack} = V_g - V_{fb} - \psi_s \sim V_g$), we can derive the voltages across the HfO_2 and interfacial layers further, as follows:

$$V_{hk} = V_g \Big/ \left(\frac{\varepsilon_{hk} t_{IL}}{\varepsilon_{IL} t_{hk}} + 1\right) \tag{6.9}$$

$$V_{IL} = V_g \Big/ \left(\frac{\varepsilon_{IL} t_{hk}}{\varepsilon_{hk} t_{IL}} + 1 \right) \tag{6.10}$$

where V_{hk} is the voltage across the HfO_2 layer. As we mentioned above, the interfacial layers of the HF-dipped, NH_3-annealed, and RTO-treated samples are Hf-silicate-like, SiN_x, and SiO_2, respectively. Therefore, the values of ϕ_1 can be assumed to be 1.5 eV **[31]**, 2.4 eV **[32]**, and 3.2 eV, respectively, for these three kinds of interfacial layers. Additionally, because the conduction band barrier height of HfO_2 on an Si substrate is 1.5 eV **[31]**, the value of ϕ_2 can be determined by the expression $\phi_1 - 1.5$ eV. From **Eqs. (6.5)**, **(6.7)** and **(6.9)**, therefore, we obtain effective electron trap energies of 0.541, 0.546 and 0.437 eV for the HF-dipped, NH_3-annealed and RTO-treated samples, respectively. **Table 6.2** summarizes the extracted data for all of the samples.

6.4 Summary

We have studied the influence that different pre-deposition surface treatments have on the electrical characteristics of HfO_2 gate dielectrics. We have found that NH_3-annealed surface treatment not only can result in a decrease in the equivalent oxide thickness but it also significantly reduces the leakage current. In contrast, the RTO-treated process is also able to reduce the leakage current, but it increases the EOT because of its greater physical thickness. We have also investigated the dependence of hysteresis on the initial inversion bias (V_{inv}), temperature, and frequency. Our results indicate that the hysteresis width depends exponentially on both the temperature and the initial inversion bias, but it is rather insensitive to the measuring frequency. The relationship between the reciprocal voltage constant, R_v, and the activation energy, E_h, obviously is linear, and the hysteresis of our gate

dielectrics is described well by an empirical relationship of the form $C(T)\cdot\exp(R_v V_{inv})$. In addition, we have found that the electron traps in the gate dielectrics fall in the category of slow traps and that they should play a key role in the hysteresis behavior: a large number of electron traps present in a gate dielectric results in a larger hysteresis width. Moreover, the NH_3-annealed surface treatment increases the hysteresis width only slightly when compared to that of the Hf-dipped sample, while the RTO-treated sample exhibits a considerably larger hysteresis width. We believe that more electron traps exist at the inner-interface between the HfO_2 and SiO_2 layers. Finally, we have observed that the leakage currents exhibit a stronger temperature dependence at low voltage than they do at higher voltage. Therefore, we believe that the conduction mechanism for each sample at a low gate bias is dominated by trap-assisted tunneling. We have also extracted the corresponding parameters for the TAT model and have presented the data for all splits. In conclusion, we believe that surface nitridation is the most promising method of pre-deposition surface treatment of HfO_2 gate dielectrics for improving the electrical characteristics in terms of EOT, leakage current, and hysteresis.

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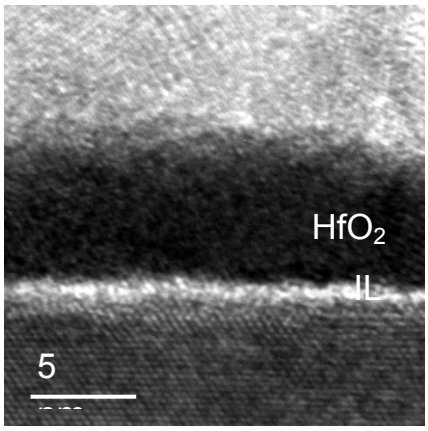
Table 6.1. Values of A, B, ln(A/B), R_v, and E_h under the conditions of V_{inv} = +3 V at T = 300 K. The terms A and B are proportionality constants, R_v is the reciprocal voltage constant, and E_h is the activation energy.

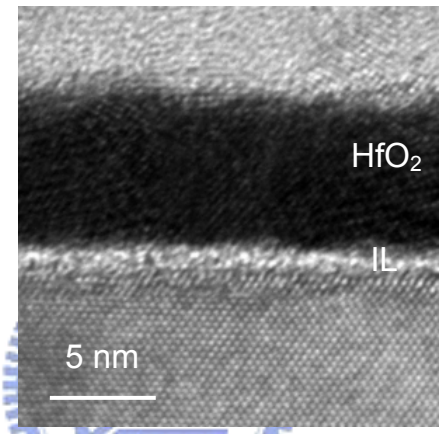
$E_h = 0.026\ln(A/B) + 0.078R_v$					
Surface Treatments	A	B	ln(A/B)	R_v (1/V)	E_h (eV)
HF-dipped	0.150	8.74×10^{-3}	2.843	0.274	0.095
NH_3-annealed	0.151	1.40×10^{-2}	2.378	0.336	0.088
RTO-treated	0.200	2.15×10^{-2}	2.230	0.435	0.092

Table 6.2. Values of E_a, qV_{IL}, ϕ_1, ϕ_2, and ϕ_t for all samples at V_g = +1 V. The term E_a is the activation energy, V_{IL} is the voltage across the interfacial layer, ϕ_1 is the barrier height between the Si substrate and the interfacial layer, ϕ_2 is the barrier between the interfacial layer and HfO_2, and ϕ_t is the effective energy of the electron traps with respect to the conduction band edge of the HfO_2 layer.

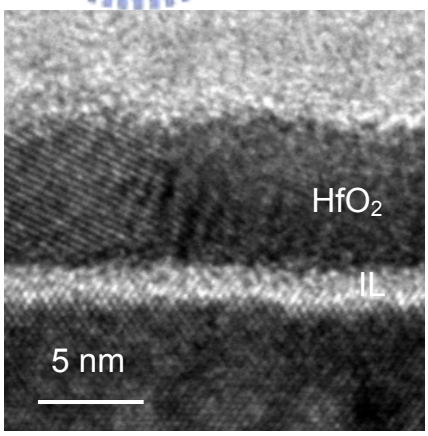
$E_a = -(qV_{IL} - \phi_1 + \phi_2 + \phi_t)$ (eV)					
Surface Treatments	E_a	qV_{IL}	ϕ_1	ϕ_2	ϕ_t
HF-dipped	0.384	0.575	1.5	0.0	0.541
NH_3-annealed	0.405	0.549	2.4	0.9	0.546
RTO-treated	0.433	0.630	3.2	1.7	0.437



(a) HF-dipped



(b) NH_3-annealed



(c) RTO-treated

Fig. 6.1. TEM pictures of the cross sections for the HfO_2 films with different surface treatments. (a) HF-dipped. (b) NH3-annealed. (c) RTO-treated.

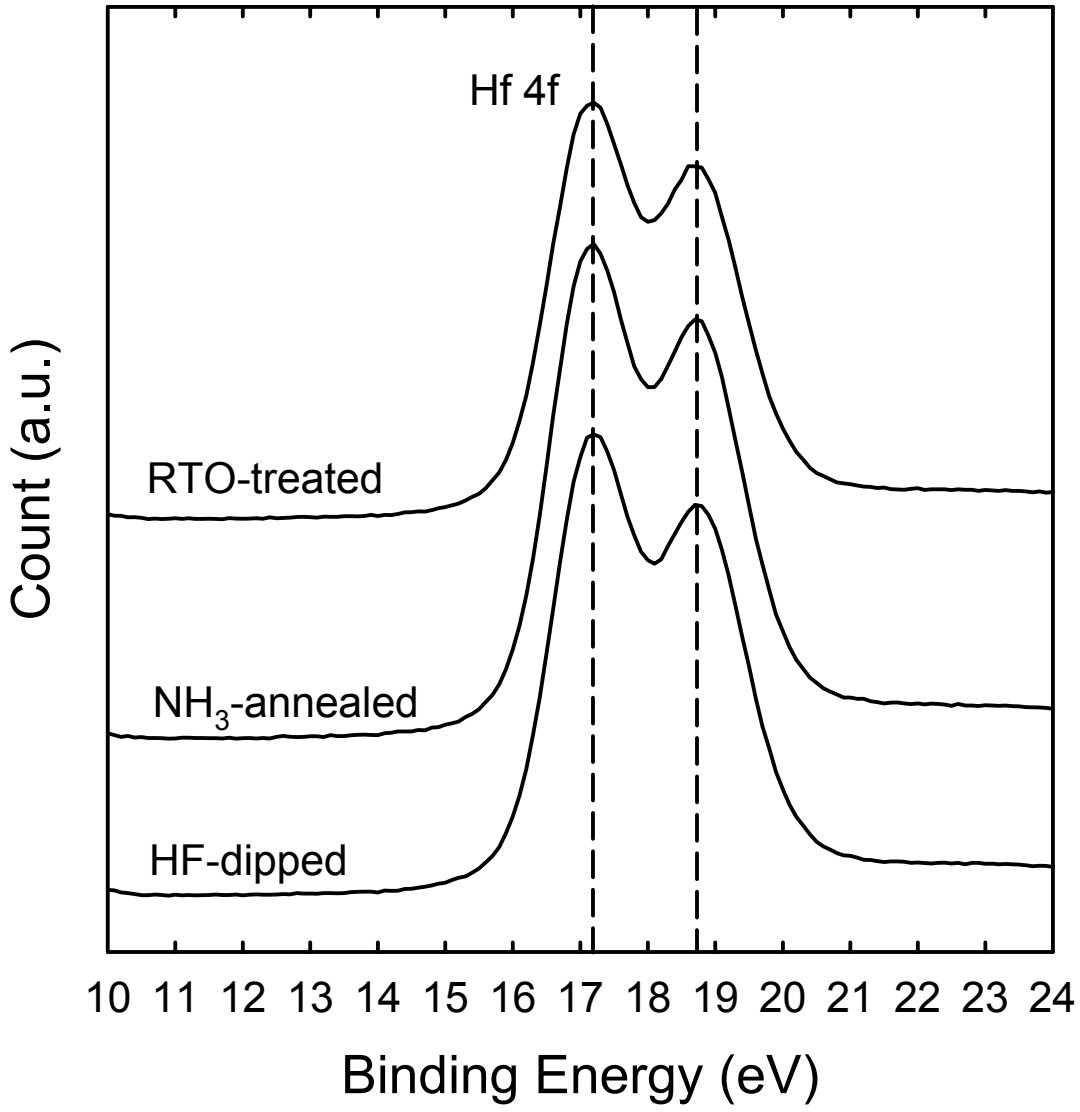


Fig. 6.2. The XPS spectra of the HfO_2 films with different surface treatments.

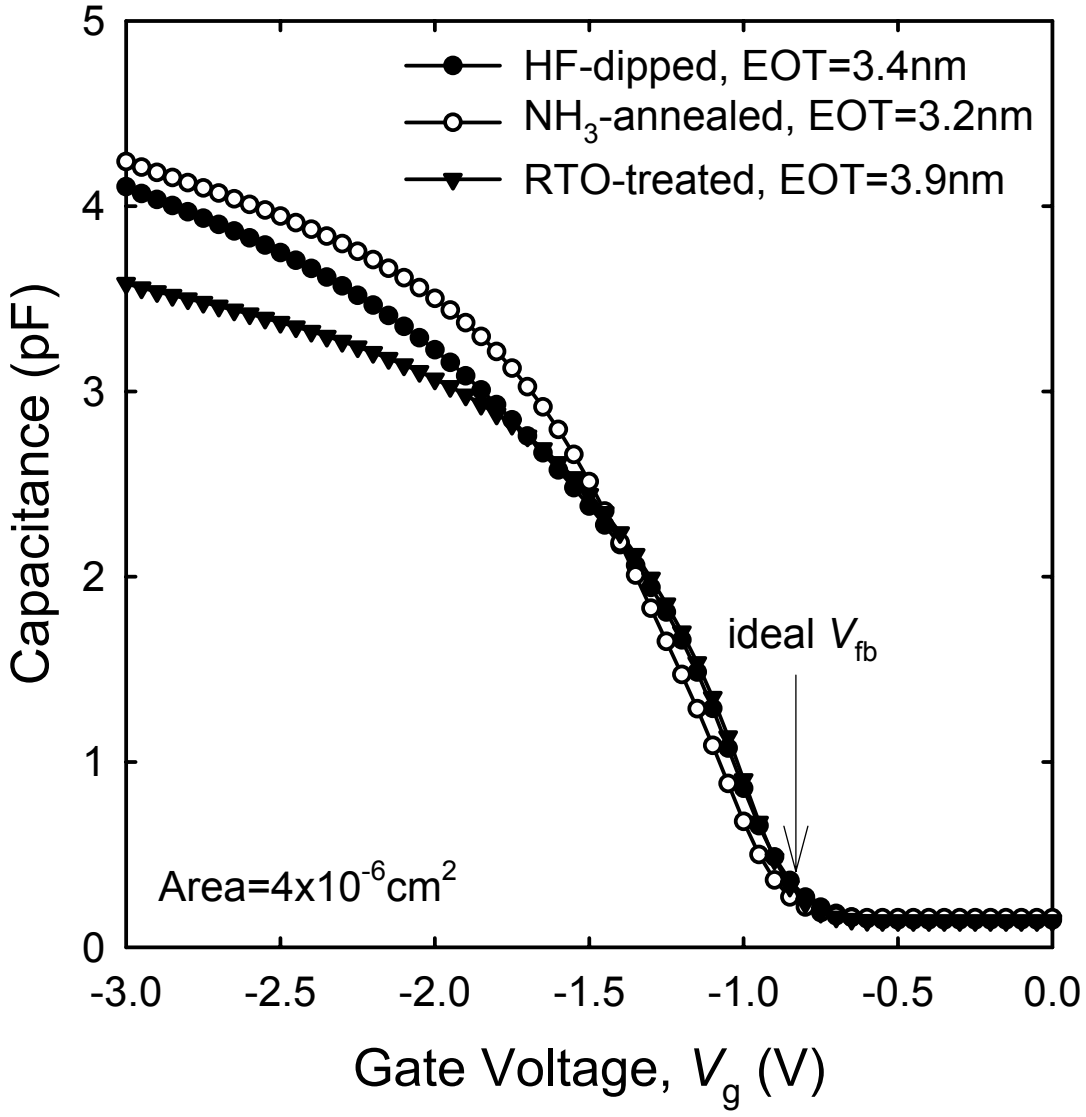


Fig. 6.3. The capacitance–voltage (C–V) characteristics of NMIS capacitors prepared by applying the three different surface treatment processes. The equivalent oxide thickness (EOT) was determined by measuring the maximum accumulation capacitance.

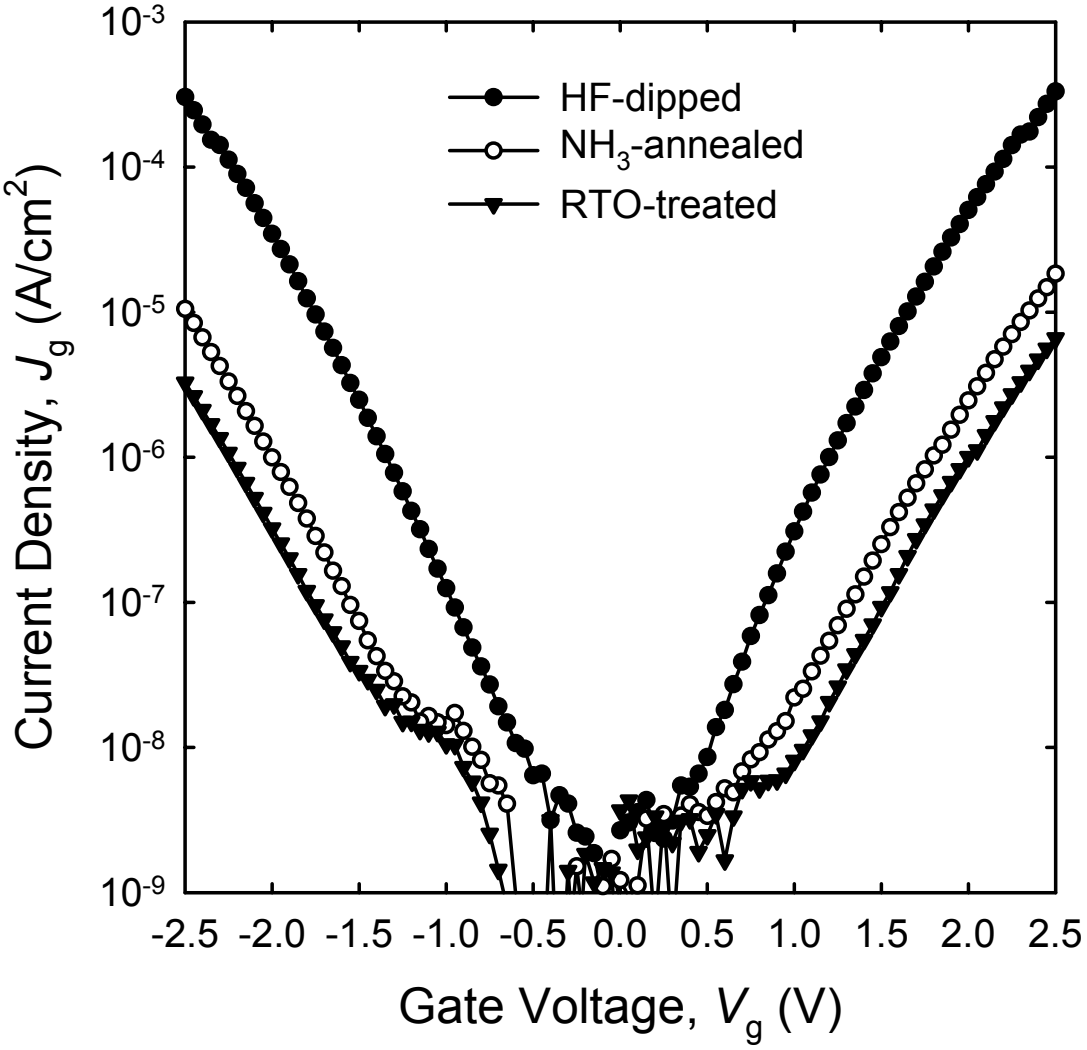


Fig. 6.4. The plot of the leakage current as a function of gate voltage for each sample.

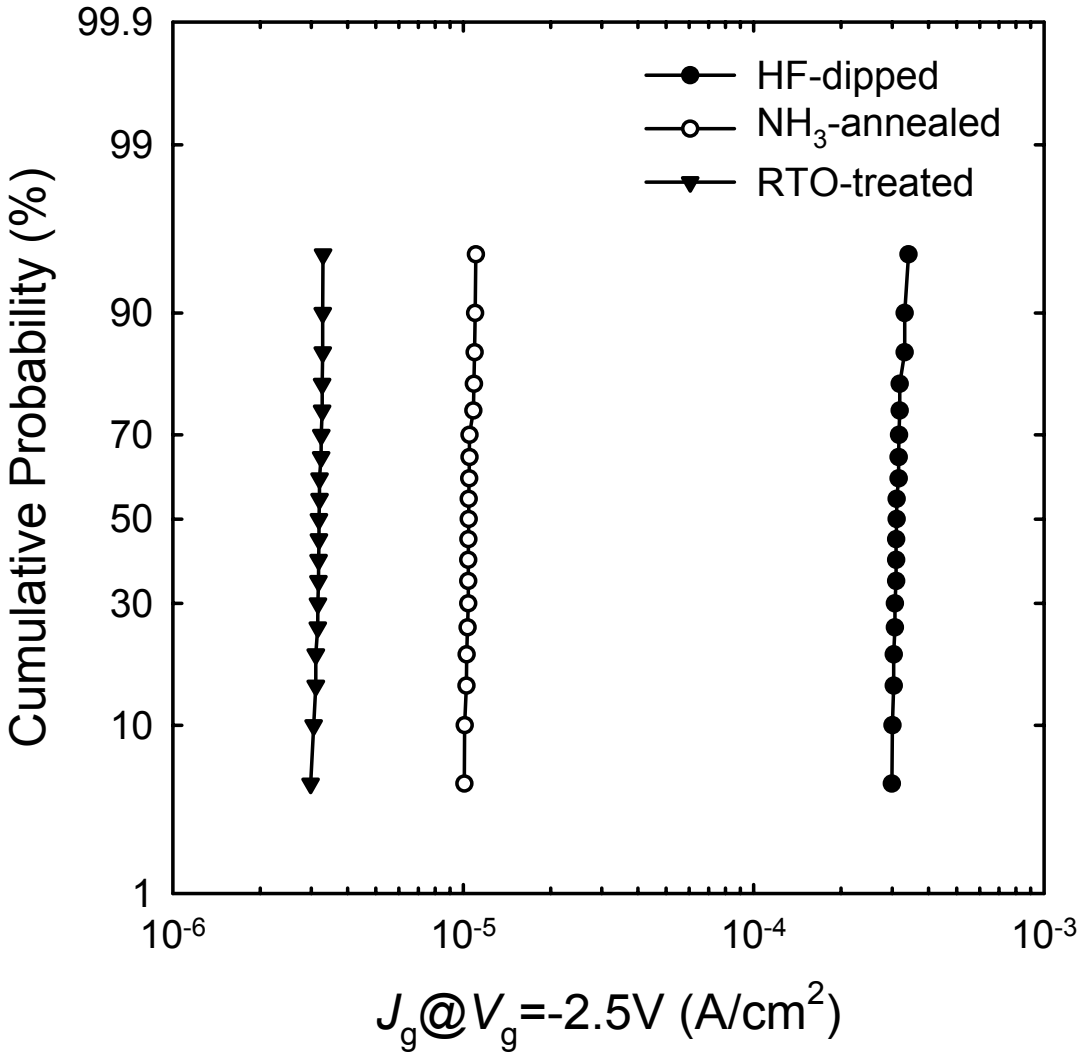


Fig. 6.5. The cumulative distribution of leakage currents at V_g = –2.5 V for capacitors formed by using the three different surface treatment processes.

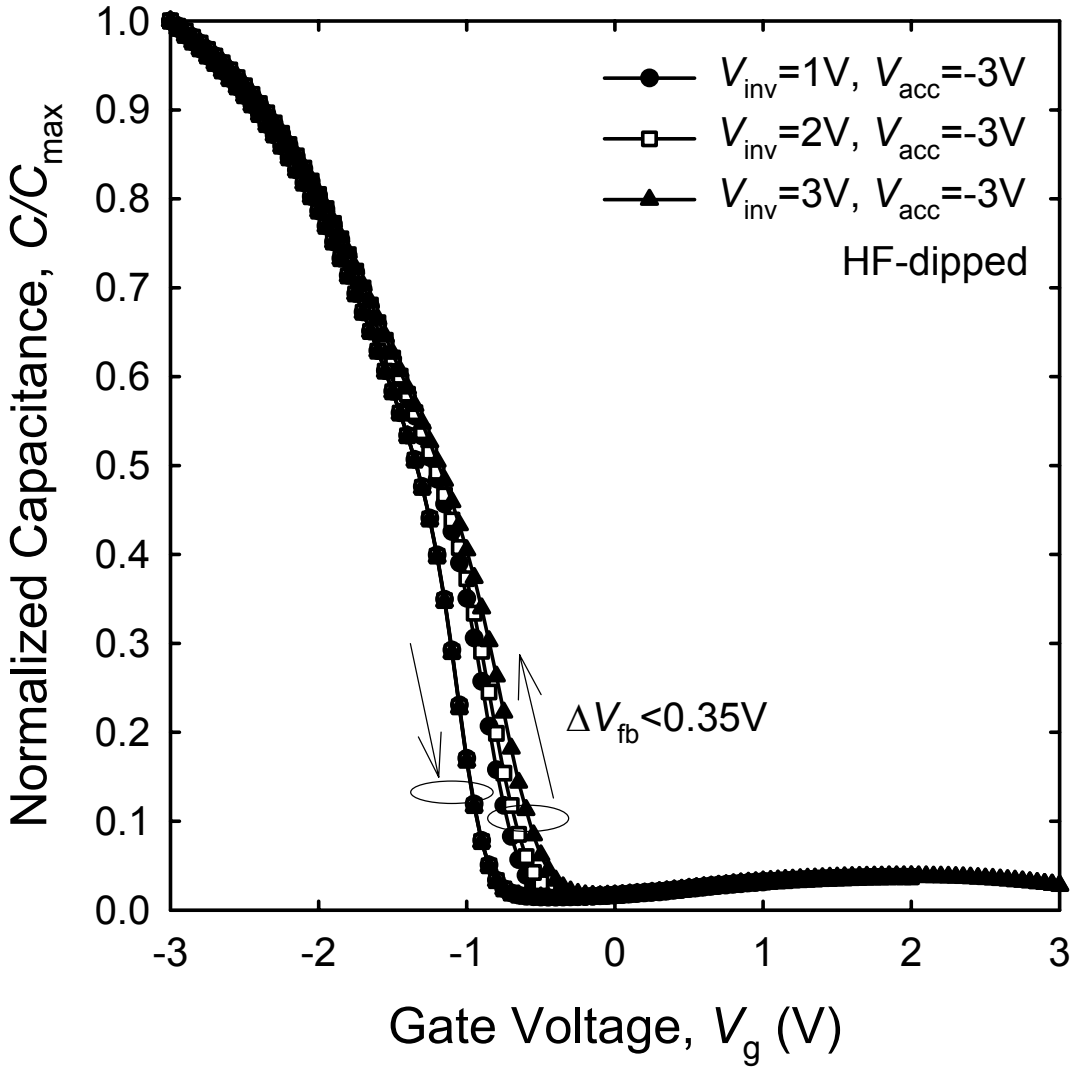


Fig. 6.6(a). Normalized C–V curves with different sweeping voltages for the HF-dipped sample. The initial inversion biases (V_{inv}) are +1, +2, and +3 V, and the accumulation bias (V_{acc}) is –3 V.

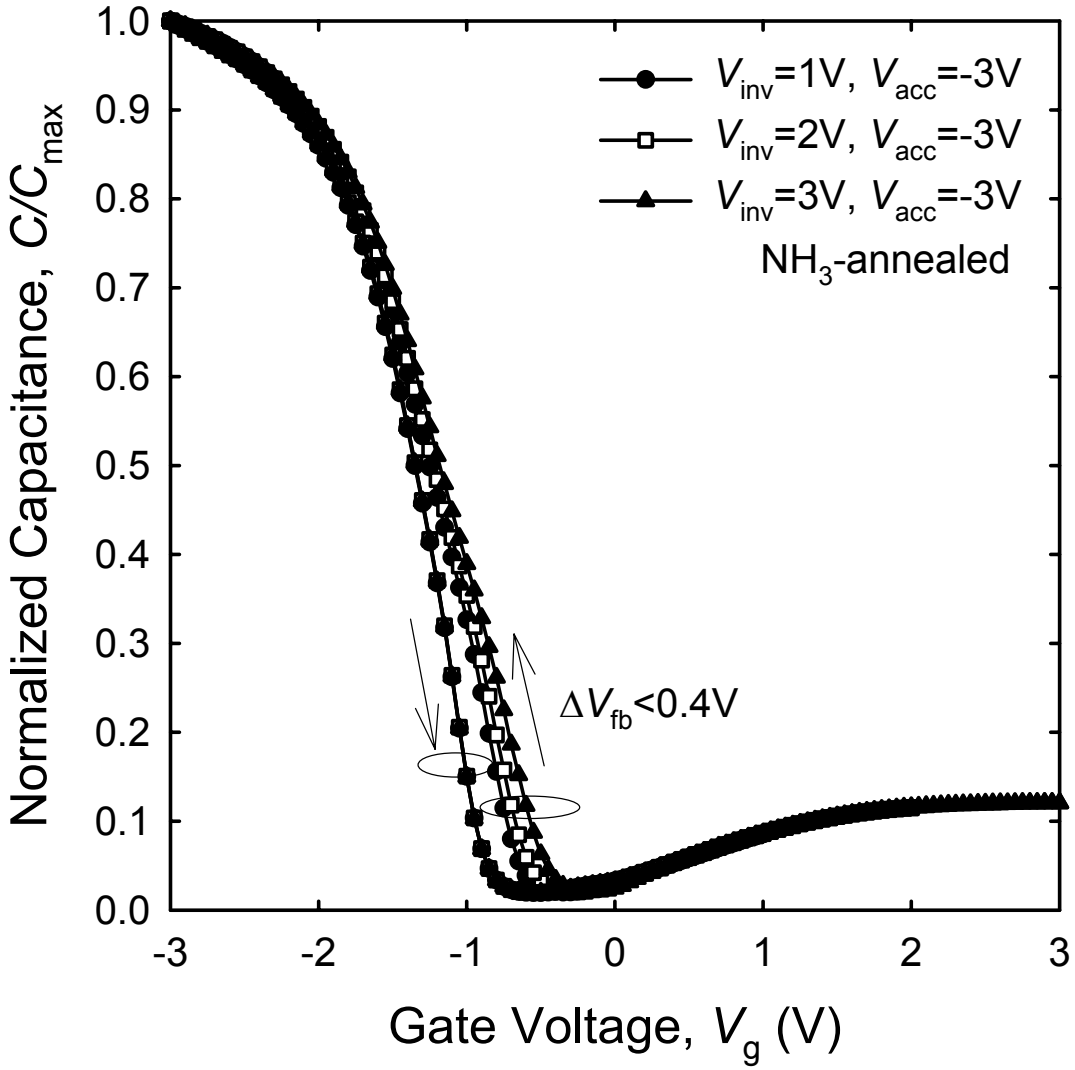


Fig. 6.6(b). Normalized C–V curves with different sweeping voltages for the NH_3-annealed sample. The initial inversion biases (V_{inv}) are +1, +2, and +3 V, and the accumulation bias (V_{acc}) is −3 V.

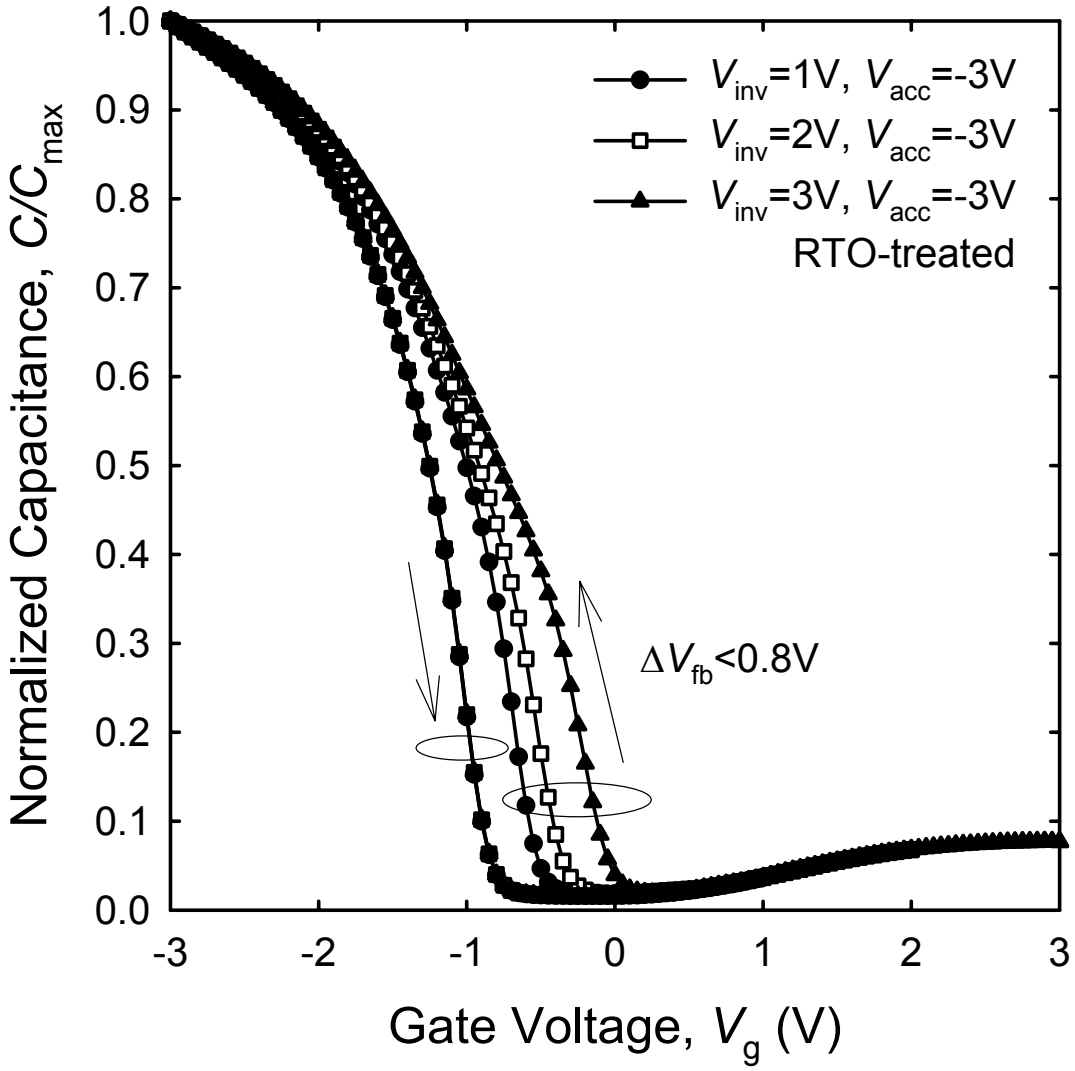


Fig. 6.6(c). Normalized C–V curves with different sweeping voltages for the RTO-treated sample. The initial inversion biases (V_{inv}) are +1, +2, and +3 V, and the accumulation bias (V_{acc}) is –3 V.

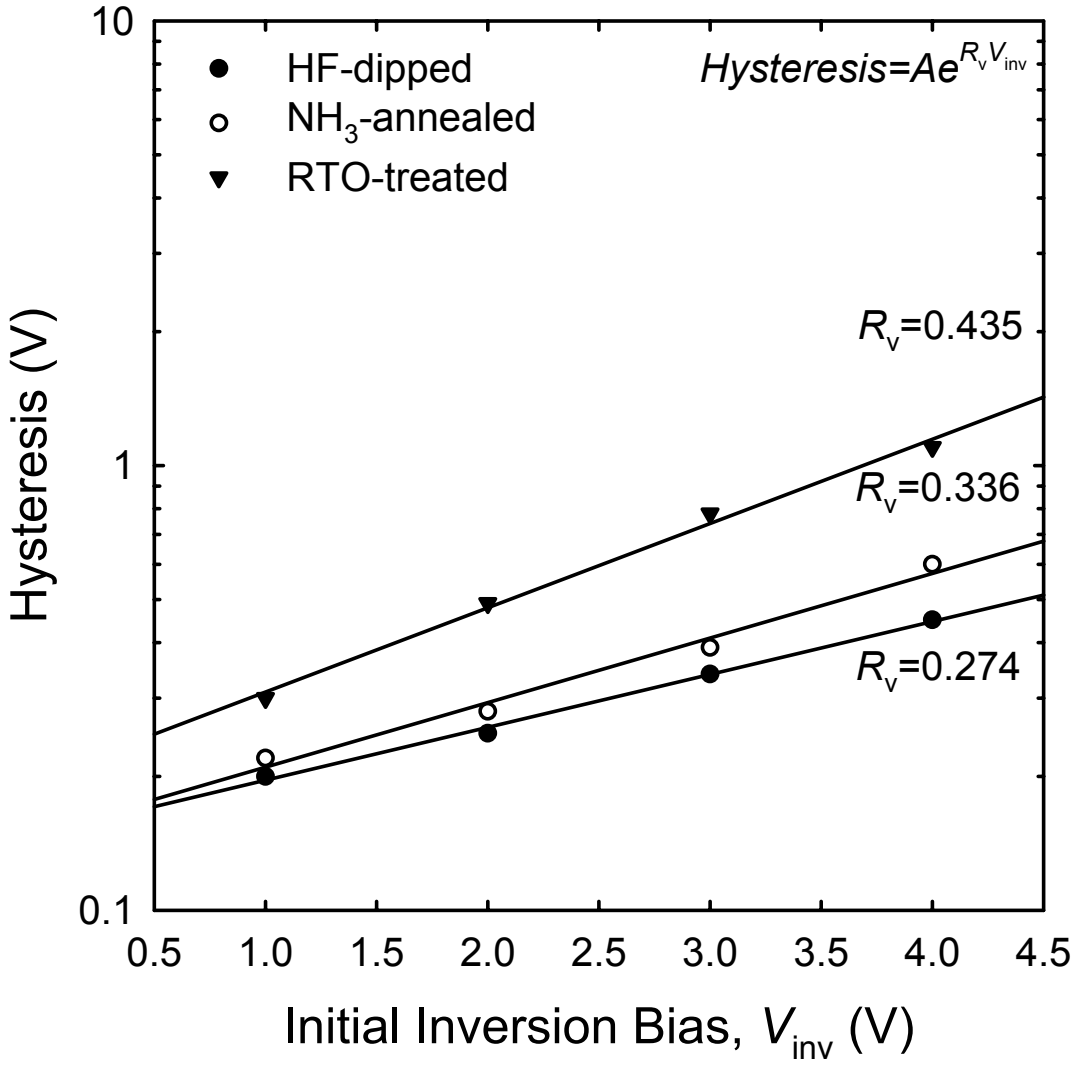


Fig. 6.7. The dependence of hysteresis width on the inversion bias (V_{inv}) during C–V measurement. The reciprocal voltage constant (R_v) is obtained from the slope of the fitted line.

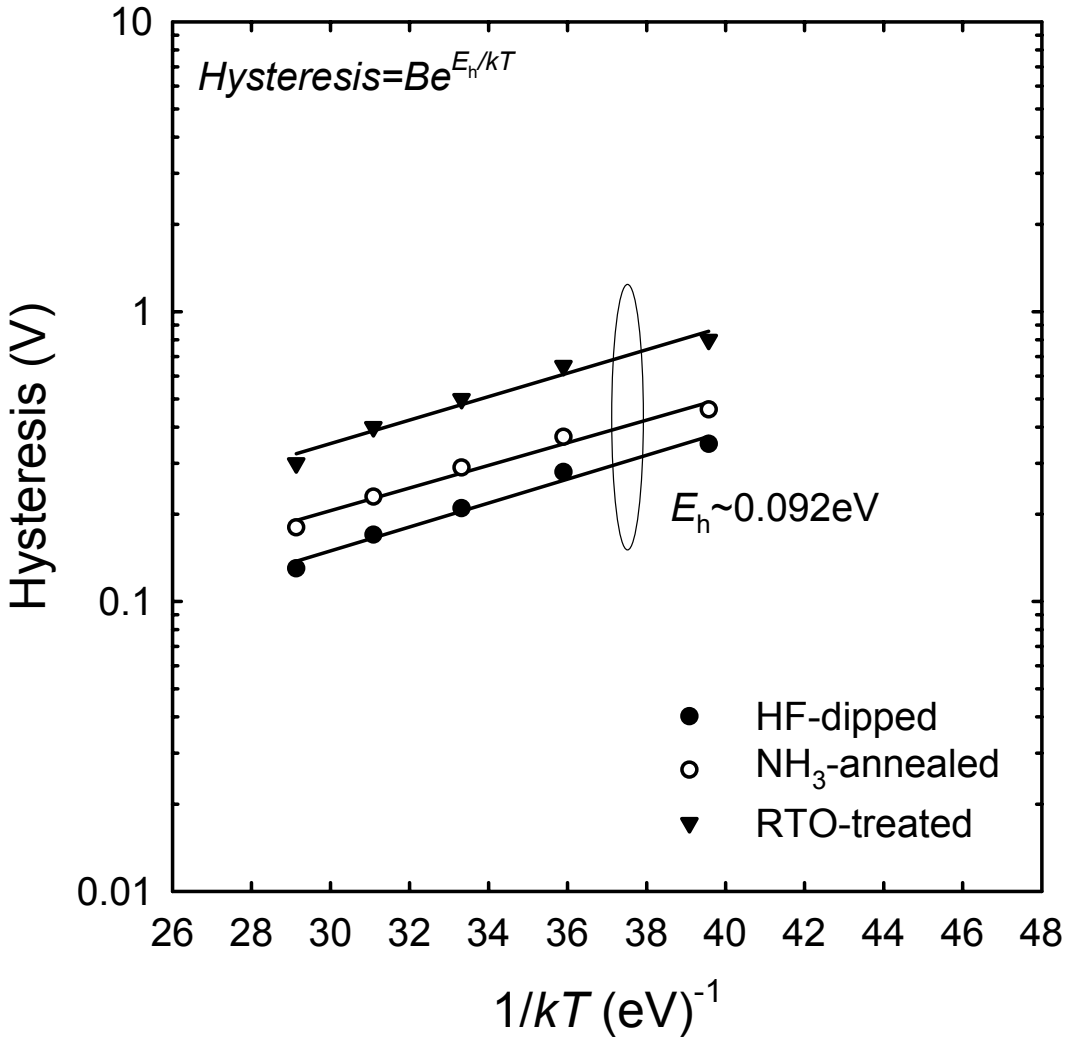


Fig. 6.8. The plot of hysteresis as a function of the reciprocal of temperature. The activation energy (E_h) for each sample is ca. 0.092 eV.

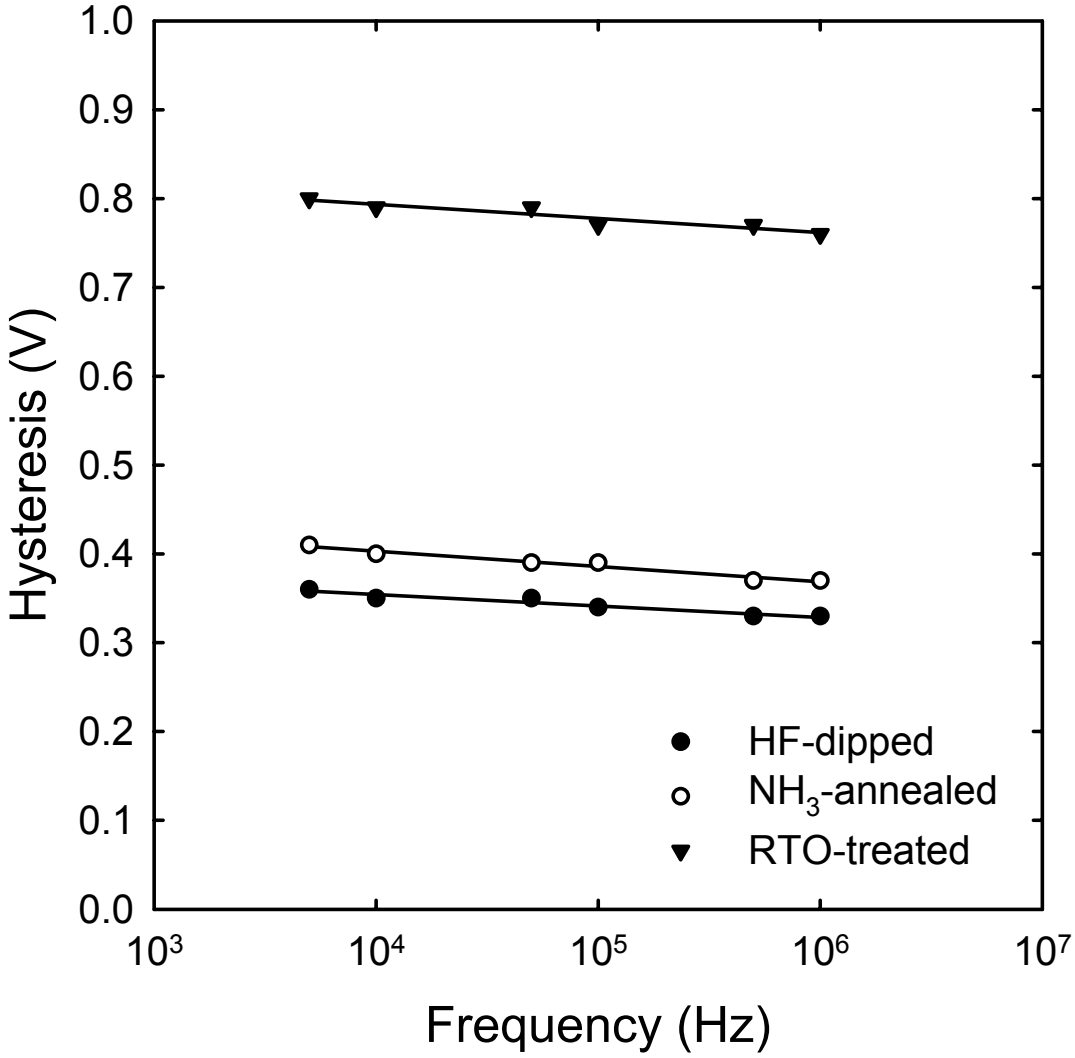


Fig. 6.9. The plot of hysteresis as a function of the *C–V* measuring frequency.

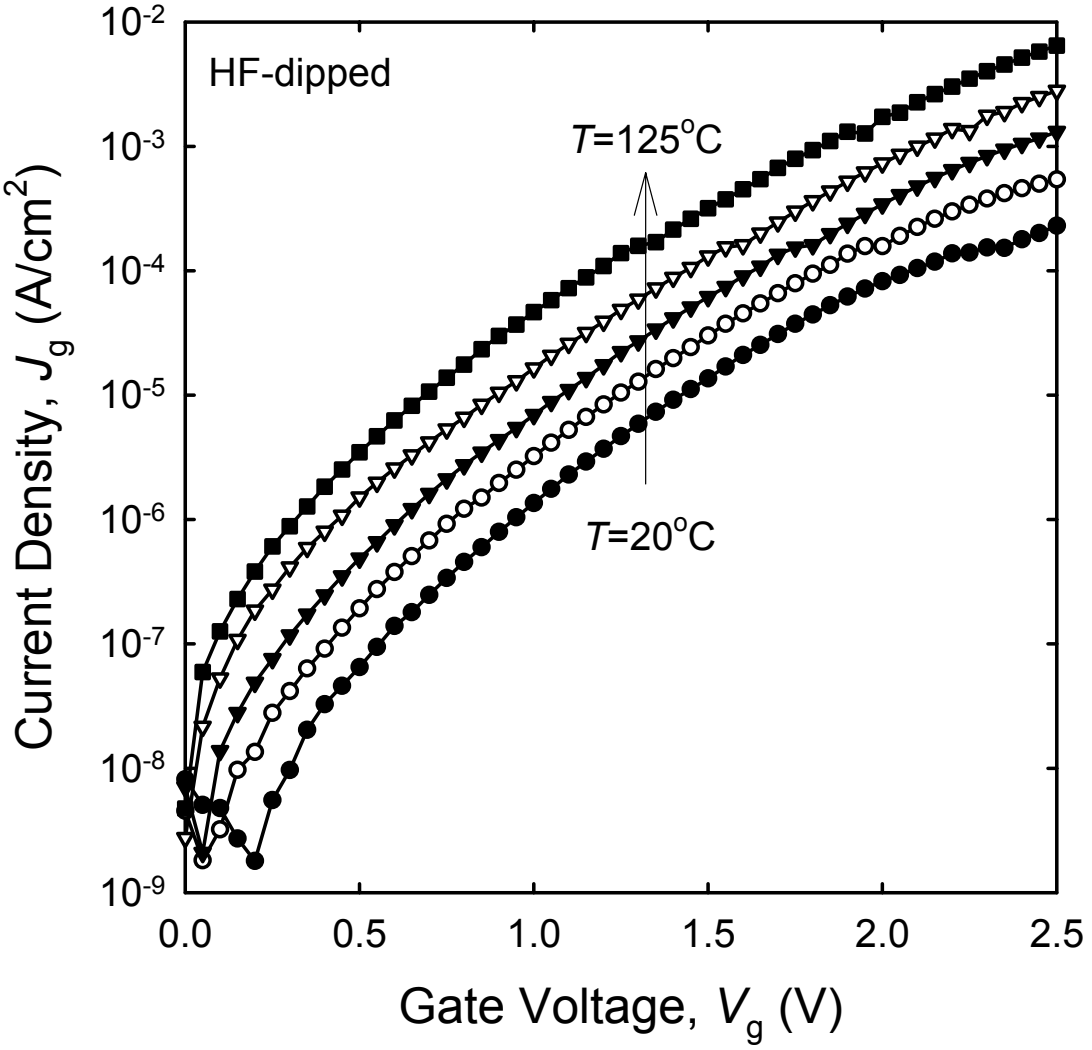


Fig. 6.10(a). The plot of leakage current as a function of gate voltage for the HF-dipped sample as the temperature was varied from 20 to 125 ˚C.

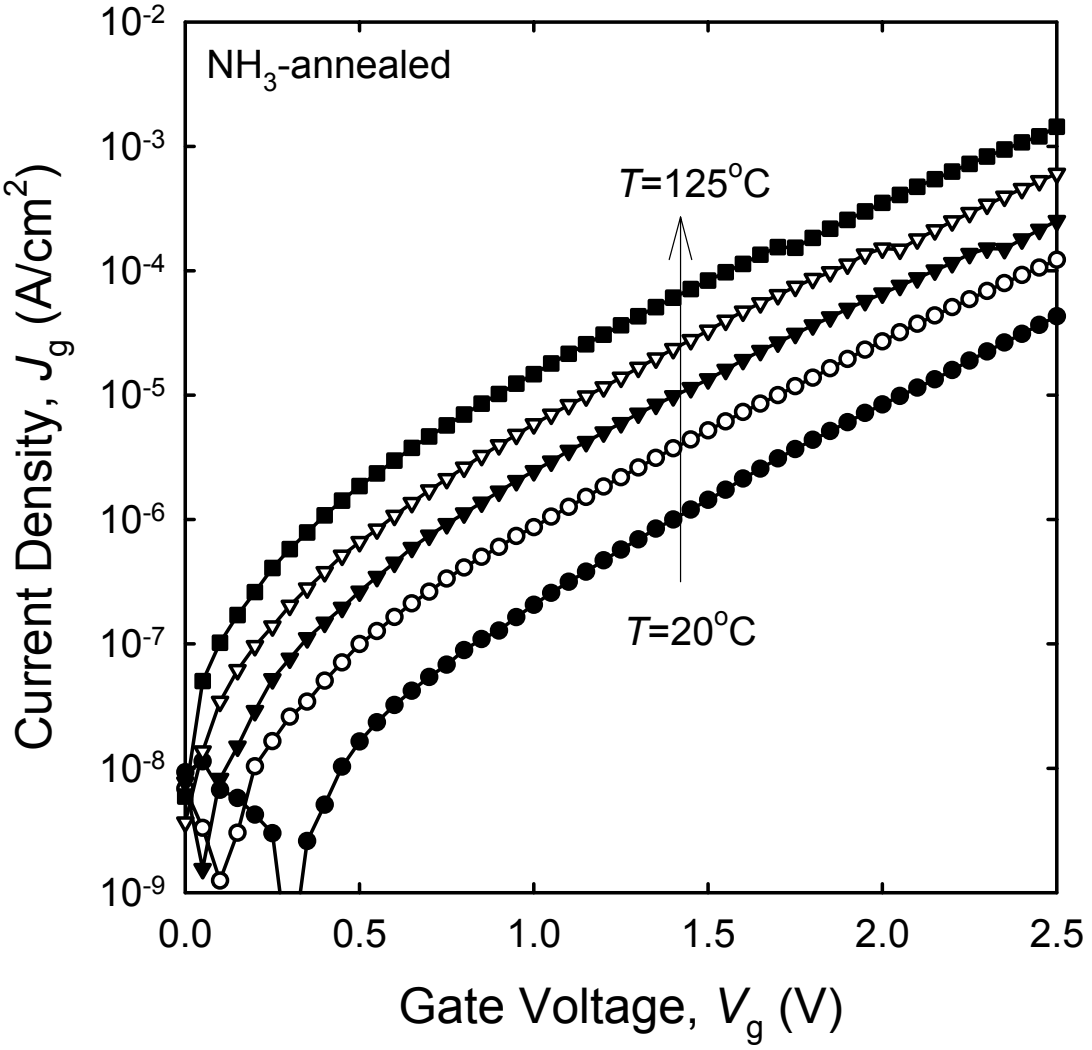


Fig. 6.10(b). The plot of leakage current as a function of gate voltage for the NH_3-annealed sample as the temperature was varied from 20 to 125 ˚C.

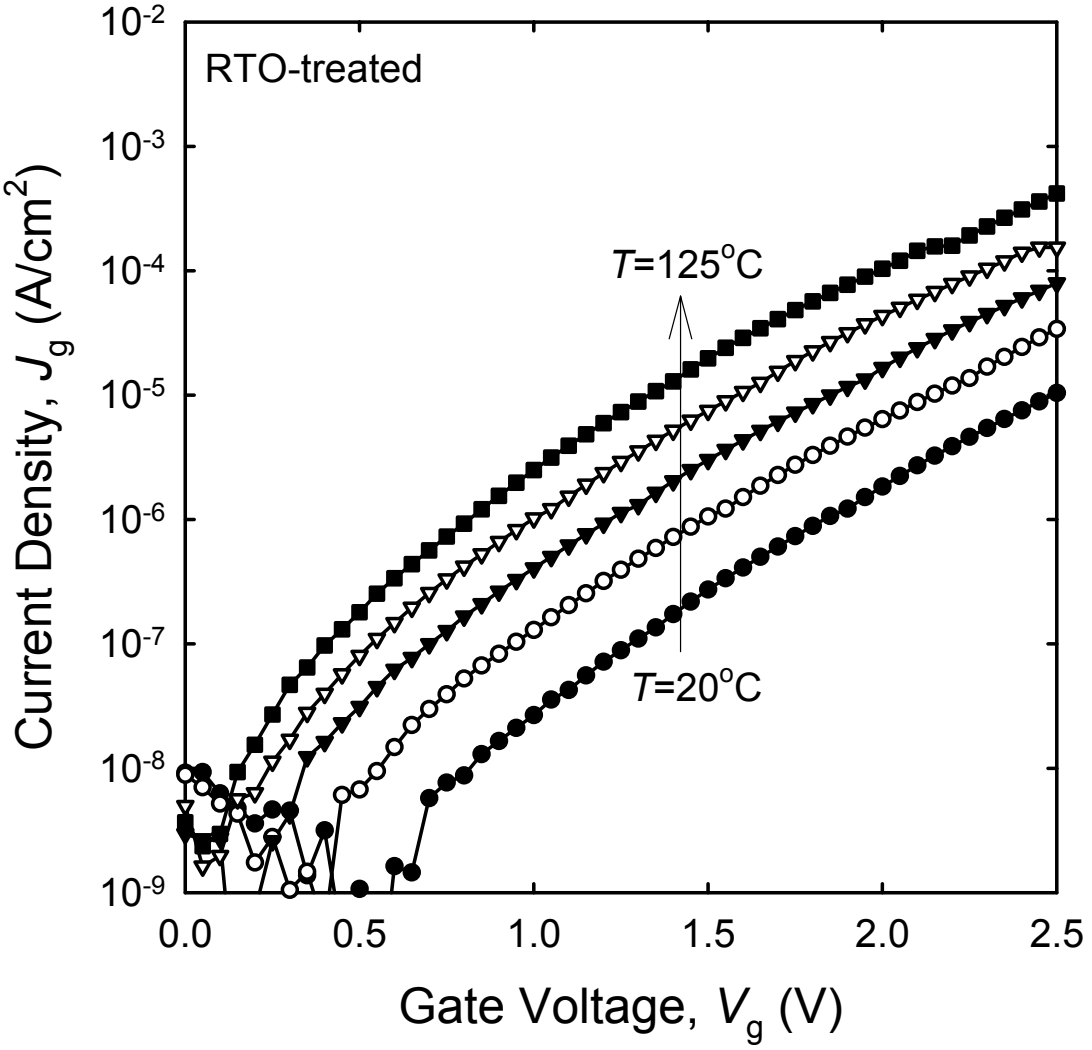


Fig. 6.10(c). The plot of leakage current as a function of gate voltage for the RTO-treated sample as the temperature was varied from 20 to 125 ˚C.

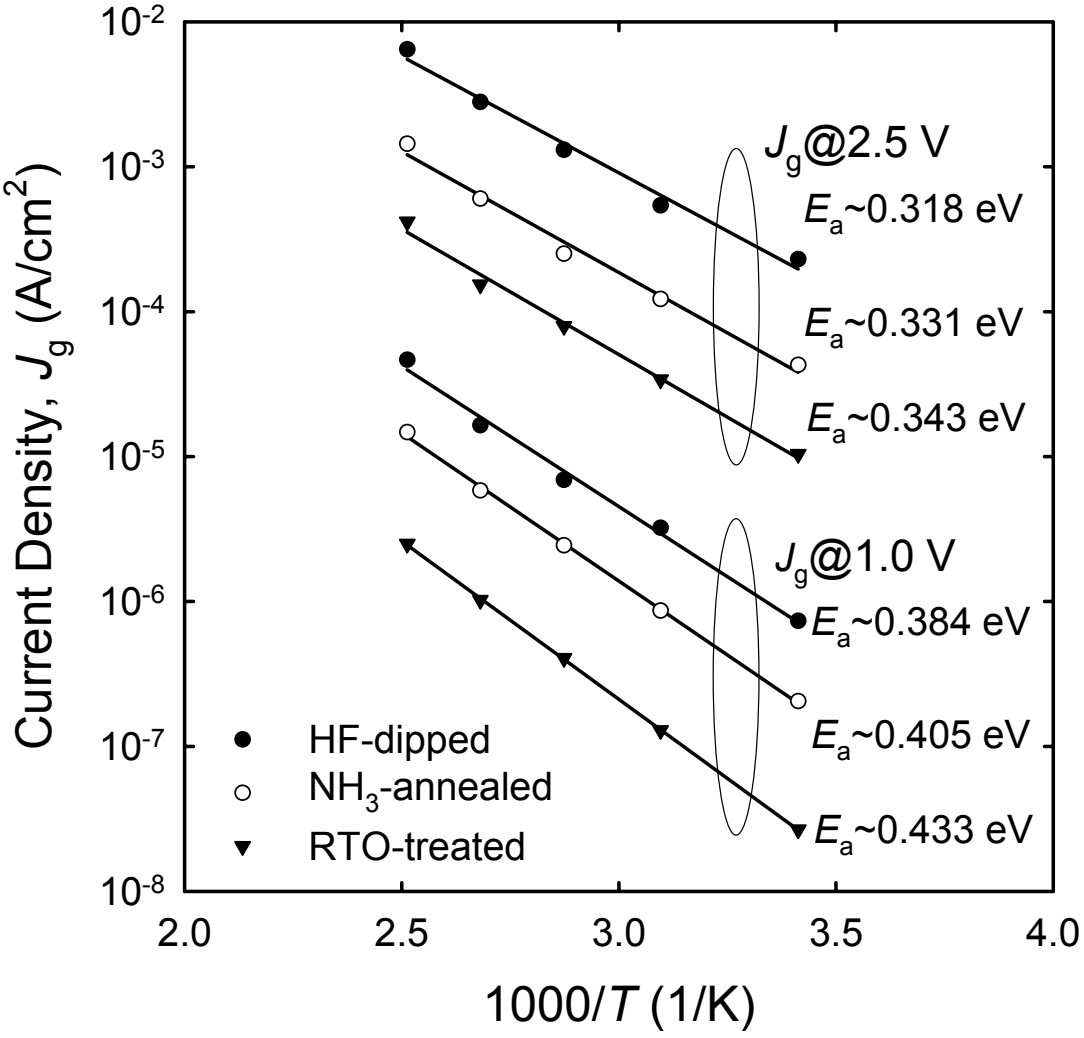


Fig. 6.11. The Arrhenius plot of leakage currents at V_g = 1.0 V and V_g = 2.5 V. The activation energy (E_a) increases as the temperature decreases.

Chapter 7

Conclusions and Suggestions for Further Study

7.1 Conclusions

We have investigated the hot-carrier degradation, reliability, and flicker noise characteristics of the deep sub-micron nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate oxides, including thermal oxide, Si_3N_4/SiO_2 stack, NO oxynitride, and plasma nitrided oxide. Next, the reliability and the channel thickness effect of the deep sub-micron pMOSFETs with ultra-thin (EOT = 3.1 nm) N_2O-annealed SiN gate dielectric and strained $Si_{0.85}Ge_{0.15}$ channel have been studied. Finally, we have also investigated the electrical characteristics of the ultra-thin HfO_2 gate dielectrics with different pre-deposition surface treatments of HF dipping, NH_3 nitridation and RTO annealing. In conclusion, we summarize the results and discussions in the following list.

For the deep sub-micron nMOSFETs with various ultra-thin (EOT = 1.6 nm) gate oxides:

1. Nitrogen incorporation into ultra-thin gate oxide could reduce gate leakage current effectively, but it also introduces the positive oxide charges to cause threshold voltage shift and transconductance degradation and induces the electron traps to enhance the flicker noise.
2. The nitrided oxides result in enhanced hot-electron-induced device degradations, such as significant threshold voltage shift, transconductance

degradation, and drain current reduction comparing with the thermal oxide. The electron trap generation rather than the interface state generation should be the main mechanism of the hot-electron degradation for the deep sub-micron nMOSFET with ultra-thin (EOT = 1.6 nm) nitrided gate oxide because of the observations of the positive shift of threshold voltage, the insignificant variation of subthreshold swing, the reduction of gate leakage current, no significant slope changes of the I_b-V_{cb} curves for DCIV measurement, and a small exponent value (n ~ 0.3) of the ΔV_t versus stress time plot after the hot-carrier stressing. Therefore, the hot-electron-induced electron trapping in the ultra-thin nitrided gate oxide could eventually become a severe long-term reliability concern (CHE and SHE) for the sub-100nm technologies.

3. The low-frequency flicker noise is mainly generated by electron trapping/detrapping with the interface states and the electron traps. Because of the electron traps induced by incorporating nitrogen into oxide, the nitrided oxides demonstrate a higher flicker noise than the thermal oxide. However, nitrogen incorporation can improve the device immunity against the hot-carrier degradation in the flicker noise since the hot-electron-induced electron trapping may suppress the generation of flicker noise. On the other hand, a considerable amount of electron traps are created to enhance the flicker noise when oxide breakdown is occurred, and moderate increase of noise level is observed for the nitrided oxide as compared with the thermal oxide.
4. The frequency index of noise spectrum is varied with the gate bias and it is strong related to the oxide traps. Moreover, the frequency index will be lowered by hot-carrier degradation and even worse by oxide breakdown for

both thermal oxide and nitrided oxide devices.

5. For considering the hot-carrier reliability and the characteristics of flicker noise, the plasma nitridation should be the most promising technique for the ultra-thin nitrided gate oxide applications, and the plasma nitrided oxide should be the promising candidate of the ultra-thin nitrided oxide for sub-100 nm MOSFET devices in analog and RF applications.

For the deep sub-micron pMOSFETs with ultra-thin (EOT = 3.1 nm) N_2O-annealed SiN gate dielectric and strained $Si_{0.85}Ge_{0.15}$ channel:

1. A good quality of gate dielectric can be obtained by the N_2O-annealed SiN film because no significant as-deposited oxide traps are observed in the N_2O-annealed SiN gate dielectric. The conduction mechanism responsible for the gate leakage current should be dominated by the FN tunneling with an effective barrier height of 1.8 eV. Moreover, the strained SiGe channel device with ultra-thin N_2O-annealed SiN gate dielectric shows well-performed on/off and output characteristics.
2. Insignificant degradation has been found when the capacitors with ultra-thin (EOT = 3.1 nm) N_2O-annealed SiN gate dielectric are stressed under the constant voltage (or current) stressing. The polarity dependence of SILC reveals that the oxide traps generated during the stressing process should be more close to the gate electrode.
3. The device reliability of hot-carrier degradation and NBTI stressing has been investigated. The hot-carrier degradation is more severe than the NBTI stressing and the channel-hot-carrier stressing is regarded as the worst case of device degradation. According to the power law relationship of ΔV_t versus stress time as well as the results of charge pumping measurement, the interface

state generation should be the predominant factor for the HC degradation while the electron trapping may dominate the degradation of device characteristics for the NBTI stressing. On the other hand, although the electron trapping occurs at the initial stage of the high voltage CHC stressing, the hole trapping eventually dominates the degradation when the device is stressed for a longer time.

4. To investigate the channel thickness effect of the strained $Si_{0.85}Ge_{0.15}$ pMOSFETs with ultra-thin N_2O-annealed SiN gate dielectric, the devices with various SiGe channel thickness of 5, 15, and 30 nm have been fabricated. A thin gate dielectric with EOT of 3.1 nm and an excellent subthreshold swing of 68 mV/dec are obtained for the devices with 5 and 15 nm SiGe channel, and the density of interface state and dislocation are also even lower than that of the 30 nm SiGe channel device because of their lower GIDL and junction leakage currents.
5. Comparing with the thinner SiGe channel devices, the 30 nm SiGe channel device degrades the transconductance at low gate voltages because of its higher density of interface state and dislocation and improves, however, the transconductance at high gate bias because of the screening effect on the surface scattering. On the other hand, all SiGe channel pMOSFETs, comparing with the Si channel device, show the enhancement in the effective hole mobility which is due to the compressive strain and the quantum confinement effect of the strained SiGe channel.
6. The pMOSFETs with thin (<30 nm) SiGe channel and ultra-thin N_2O-annealed SiN gate dielectric are well-performed and show their potential for the advanced sub-100 nm device technology and applications.

For the ultra-thin HfO_2 gate dielectrics with different pre-deposition surface treatments:

1. The NH_3-annealed surface treatment not only results in a decrease in the equivalent oxide thickness but also significantly reduces the leakage current. In contrast, the RTO-treated process is able to reduce the leakage current but increases the EOT because of its greater physical thickness.
2. The hysteresis width of HfO_2 gate dielectric is exponentially dependent on both the temperature and the initial inversion bias and insensitive to the measuring frequency without regarding the surface treatments. The relationship between the reciprocal voltage constant, R_v, and the activation energy, E_h, is linear, and the hysteresis width could be described well by an empirical relationship of the form $C(T)\cdot\exp(R_v V_{inv})$.
3. The electron traps in the HfO_2 gate dielectrics fall in the category of slow traps and they should play a key role in the hysteresis behavior because more electron traps result in a larger hysteresis width. The NH_3-annealed surface treatment increases the hysteresis width slightly comparing with the Hf-dipped sample, while the RTO treatment exhibits a considerably larger hysteresis width because of more excess electron traps at the inner-interface between the HfO_2 and SiO_2 layers.
4. The leakage currents exhibit stronger temperature dependence at low voltage than at higher voltage. Therefore, the conduction mechanism at low gate bias should be dominated by the trap-assisted tunneling. All of the corresponding parameters for the TAT model are extracted and presented for all samples.
5. The surface nitridation should be the most promising method of pre-deposition surface treatment for improving the EOT, the leakage current and the hysteresis of the ultra-thin HfO_2 gate dielectric.

7.2 Suggestions of Further Study

To further improve and enhance the performance of MOSFET devices, several well-known advanced technologies have to be applied and need further investigation:

1. SOI substrate: to reduce the operation voltage for low voltage and low power applications, and double gate and multiple-channel devices, such as FINFET, can be performed.
2. Strained layer channel: to enhance the channel mobility of carrier and improve the driving capability.
3. S/D with metal silicide: to reduce the sheet resistance and contact resistance of S/D and improve the output characteristics.
4. High-k gate dielectric: to reduce the gate leakage current and enhance the gate capacitance.
5. Metal gate: to eliminate the poly depletion effect and lower the gate resistance and the propagation delay can be reduced.

Although these technologies have been well-known studied and the combination of these technologies have also been realized, we believe that it is the first time to propose that an advanced high performance device may combine all of these technologies for the sub-100 nm device applications. We call it "The advanced sub-100 nm SOI MOSFETs with strained layer channel, metal S/D, high-k gate dielectric, and metal gate electrode," and the device structure is demonstrated in **Fig. 7.1**. Notice that, in this device, we use pure metal instead of silicide metal to form the source and drain. To achieve this device, however, many hard obstacles still have to be overcome so far especially for the process integration. Eventually, we believe that

it will be realized in the near future.

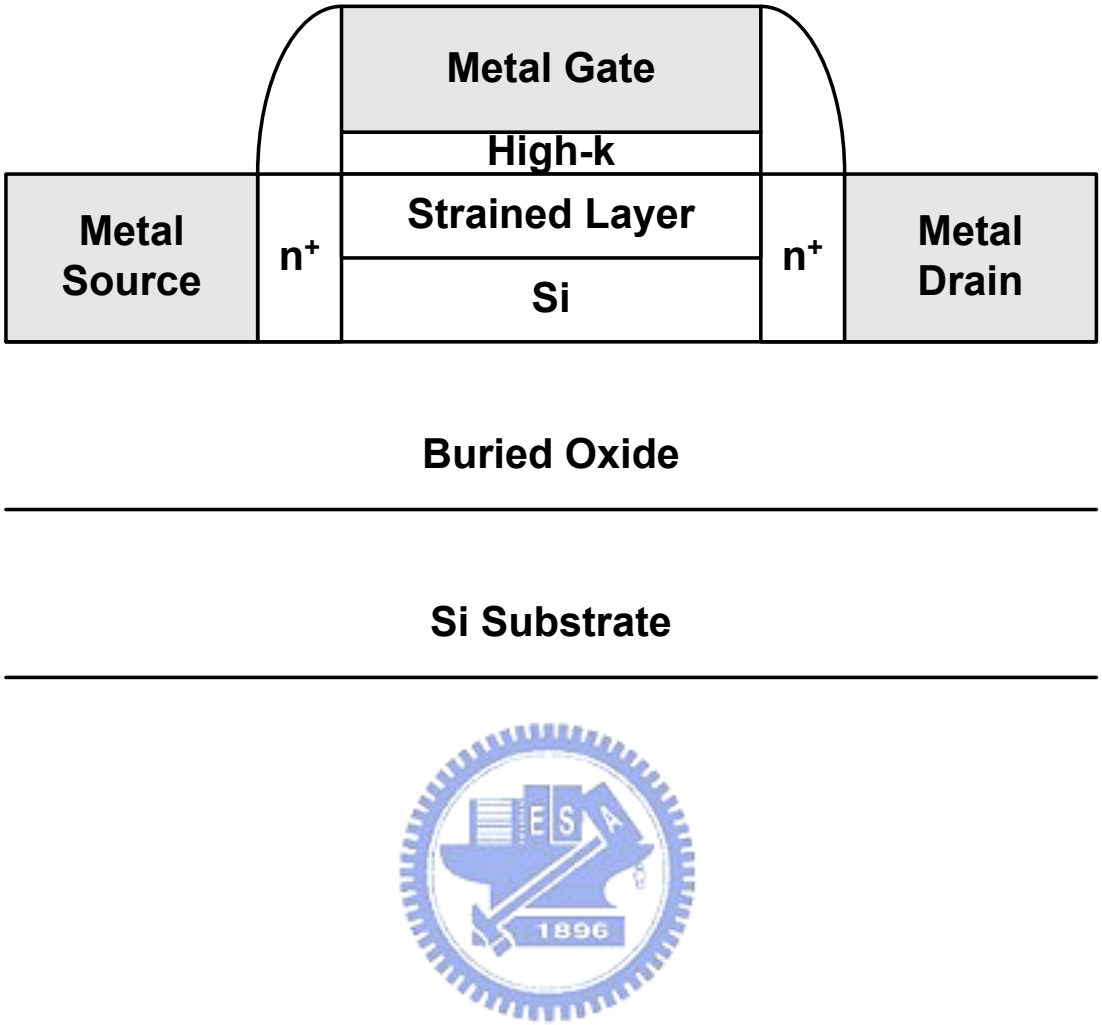


Fig. 7.1. The schematic device structure of the advanced sub-100 nm SOI MOSFETs with strained layer channel, metal S/D, high-k gate dielectric, and metal gate electrode.

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(Advanced Deep Sub-Micron MOSFETs with Ultra-Thin High-k Gate Dielectrics and Strained SiGe Channel)

Publication List

International Journal

1. **Ching-Wei Chen**, Chao-Hsin Chien, Tsu-Hsiu Perng, Ming-Jui Yang, Jann-Shyang Liang, Peer Lehnen, Bing-Yue Tsui, and Chun-Yen Chang, "Electrical characteristics of thin HfO_2 gate dielectrics prepared using different pre-deposition surface treatments," *Jpn. J. Appl. Phys.*, vol. 44, no. 1A, p. 87, 2005.
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4. **Ching-Wei Chen**, Chao-Hsin Chien, Yi-Cheng Chen, Shih-Lu Hsu, and Chun-Yen Chang, "Deep sub-micron strained $Si_{0.85}Ge_{0.15}$ channel pMOSFETs with ultra-thin N_2O-annealed SiN gate dielectric," *Jpn. J. Appl. Phys.*, vol. 44, no. 9, p. L278, 2005.
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