國立交通大學

電控工程研究所

碩士論文

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運用在積分三角類比數位轉換器

Power Consumptions Model and Model-based

Design Optimization for Sigma-Delta Modulators

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摘要

傳統的積分三角類比數位轉換器系統設計是一個相當耗時的工作，需要不斷的嘗試各種系統參數，以達到所需要的解析度以及功率消耗要求。本篇論文分析了積分三角類比數位轉換器的主要雜訊來源與非線性特性所造成的失真問題。藉由分析推導出的失真功率模型、雜訊功率模型及絕對功率消耗模型，並以訊號對雜訊和失真比(SNDR)來當作我們的設計規格，以做最佳化的設計。此最佳化設計意指在某特定系統規格下，找到一組最佳化的系統參數，使得類比數位轉換器的功率消耗最小以及訊號對雜訊和失真比最大，並節省龐大制定系統參數的時間成本。最後我們將針對已發表的設計結果來做驗證的工作。雖然現今已存在相當多行為模擬工具以自動化制定系統參數，但相較之下，本論文所提出的數學式最佳化方法將快上許多。

Power Consumptions Model and Model-based Design Optimization for Sigma-Delta Modulators

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ABSTRACT

The conventional sigma-delta ADC system design is a time consuming process and needs much trials and errors with system parameters(GBW, OSR and Bit…etc) to meet the specific specifications(signal bandwidth, SNDR). This paper analyze the mainly noise sources and nonlinear distortions. Utilizing the noise power models, nonlinear distortion power models and accurate power consumption models derived in this paper, and the assigned signal to noise and distortion ratio (SNDR) to be the design goal, we can forward to do design optimization under the specific specifications. Design optimization means that under the specific specifications, we find a set of optimal design parameters such that the power consumption of ADCs is minimum and SNDR is maximum, and reduce the huge time-cost to set up the circuit specifications. Finally, design optimization is tested against a published design result. Although design automation issues have been partially addressed by recent behavior- simulation–based methods, yet such methods can be slower than our analytical approach far.

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Symbols

V_{LSB}	Quantizer step size
V_{OS}	Maximum output swing of op-amp
OSR	OverSampling Ratio
$k_{\Sigma\Delta}$	Order of the Sigma-Delta modulator
B	Number of bits in the quantizer
f_S	Sampling Frequency
f_B	Signal Bandwidth
V_{ref}	Reference Voltage of the quantizer
A_0	Finite Gain of OTA
f_{in}	Frequency of the input signal
ϕ_i	ith phase of a nonoverlap clock
A_{in}	Amplitude of input signal
σ_{jit}	standard deviation of clock jitter
C_S	Sampling capacitor
C_I	Integrating capacitor
C_L	Load capacitor of OTA
C_{gate}	The loading capacitors of CMOS logic gates
C_{Switch}	The gate capacitances of all CMOS transmission gates

C_{OX}	The capacitance per unit area of the gate oxide
V_S	Input signal plus feedback DAC signal
τ_1	Time constant of input branch
σ_{VS}	Standard deviation of V_S
τ_2	Time constant of integrator output settling
a_i	gain coefficient of i th integrator
η	percentage of the bottom plate parasitic
T	Absolute temperature
R_{Switch}	Switch ON resistance
N	quantizer levels
G_m	Amplifier transconductance
Pr()	Probability of some condition
k	Boltzmann's constant (1.38×10^{-23}) J/K
α	OTA noise factor
$Erf[]$	Error Function
I_{OTA}	Total current of the OTA
I_{BASE}	Base current of each transistor of the input differential pair of OTA
K_{OTA}	The ratio of the total current of the OTA to this bias current
f_{cl2}	The GBW of the OTA
V_{reff}	The overdrive voltage of the transistor of the input differential pair of OTA
ε_0	The permittivity of free space

1.
Introduction

1.1 Current Status and Background

The sigma-delta modulator based on switched-capacitor circuits is well suited for high resolution medium-to-low-speed applications such as digital audio [1-2][3-6], voice codec [7], and DSP chip. Recently, with the popularity of the portable devices, the low power devices became a very important topic [4]. To reduce power consumption is to extend the life of the battery and to bring the convenience to the users. Design optimization towards minimal power consumption is popular with the high-speed low-power applications of the ΣΔ modulator [8-14]. ΣΔ ADCs have been frequently applied to higher signal bandwidth, and low power consumption designs. For example, in xDSL [15-16], WiMAX [17-18] and WLAN [19] applications, signals up to several MHz must be handled. When signal bandwidth increased, the power dissipation will increased too. Both of them are trade of specification, so how to reduce power consumption and increase resolution were important issue of Sigma-Delta A/D converters design.

1.2 Motivation and Aims

The power consumption of the Sigma-Delta A/D converters is important in all kinds of application. So it is difficult that how to design can get the better power consumption. We propose a power consumption model to estimate the power consumption in the discrete time ΣΔ ADCs design. Generally, the OTA (Operational Transconductance Amplifier) are the components consuming the most power in SDM [5]. The OTA power consumption model also the most difficult to estimate cause it has three system parameters (GBW, SR and DC-gain) in this power consumption model. Since significantly increasing the sampling rate

and reduce power consumption is difficult [4], designers seek DC-gain in order to achieve low power consumption and high-linearity. Due to the complexity with OTA, the papers about OTA noise and distortion can't directly offer an efficient method to obtain optimum DC-gain in low power consumption required. How to choice an optimum equilibrium of power consumption and resolution is important to designers. To propose the design optimization for ΣΔ modulators, we need a complete set of important nonideality models and the power consumption model. The performance of the ΣΔ ADCs is usually expressed in terms of SNR and SNDR. Circuit designers must take into consideration the nonidealities and decide the circuit and system parameters to meet the desired specifications. A design optimization procedure is proposed to meet design specifications while minimizing power consumption. In a ΣΔ modulator, common causes for harmonic distortions are nonlinear finite DC-gain, settling error, nonlinear capacitances, quantizer nonlinearity, nonlinear switch resistance and unit-DAC mismatch. OTA are the critical part of the ΣΔ modulators and its nonidealities such as nonlinear finite DC-gain and settling error may produce distortions and noise significantly. With these models for design optimization, we can increase the automation and reduce complexity in the single-loop ΣΔ ADCs design.

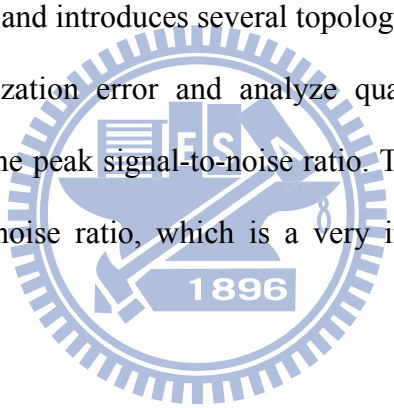
1.3 Organization

This work is organized as follows. In Chapter 2, systematic studies of fundamental theory and various architectures of ΣΔ modulator are presented first. The total noise power of Sigma-Delta Modulator has a brief introduction in Chapter 3. The accurate power consumption models is derived in Chapter 4. A design optimization scheme is proposed in Chapter 5.. Conclusions and future works are presented in Chapter 6.

2.
Fundamental Theorems and Architectures of Sigma-Delta Modulators

Before we establish the OTA gain distortion model of ΣΔ modulators, several important theorems and concepts must be known, such as Nyquist sampling theorem, quantization error and the two most critical techniques in a ΣΔ modulator: oversampling and noise shaping. All topologies of ΣΔ modulators are based on these two techniques. There also have some parameters we must to understand, such as OSR, SNR, and SNDR …etc. This chapter starts from fundamental theorems, and introduces several topologies of ΣΔ modulators.

We will illustrate quantization error and analyze quantization noise in an ideal A/D converter and then derives the peak signal-to-noise ratio. The resolution of an A/D converter is determined by signal-to-noise ratio, which is a very important specification in an A/D converter.



2.1 Nyquist Sampling Theorem

In an analog-to-digital converter, the analog signal from external environment must be converted to discrete-time signal by sampling. However, the sampling rate (fs) and signal bandwidth (f_B) must follow the Nyquist sampling theorem in (2.1):

$$f_S \geqq 2f_B \qquad (2.1)$$

The sampling rate must be higher or equal to twice of signal bandwidth in order to prevent from aliasing. We will illustrate the phenomenon of aliasing by Fig. 2.1. Fig. 2.1(a) and (b) are the spectrums of signal and sample function respectively; from fig. 2.1(c), when sampling rate is twice higher than signal bandwidth, the signal after sampling has no aliasing and it can be perfectly reconstructed by using low pass filters. However, in Fig. 2.1(d), when the

sampling rate is lower than twice of signal bandwidth, aliasing will appear in the signal after sampling. The signal having aliasing is difficult to reconstruct to original signal, like Fig. 2.1(e).

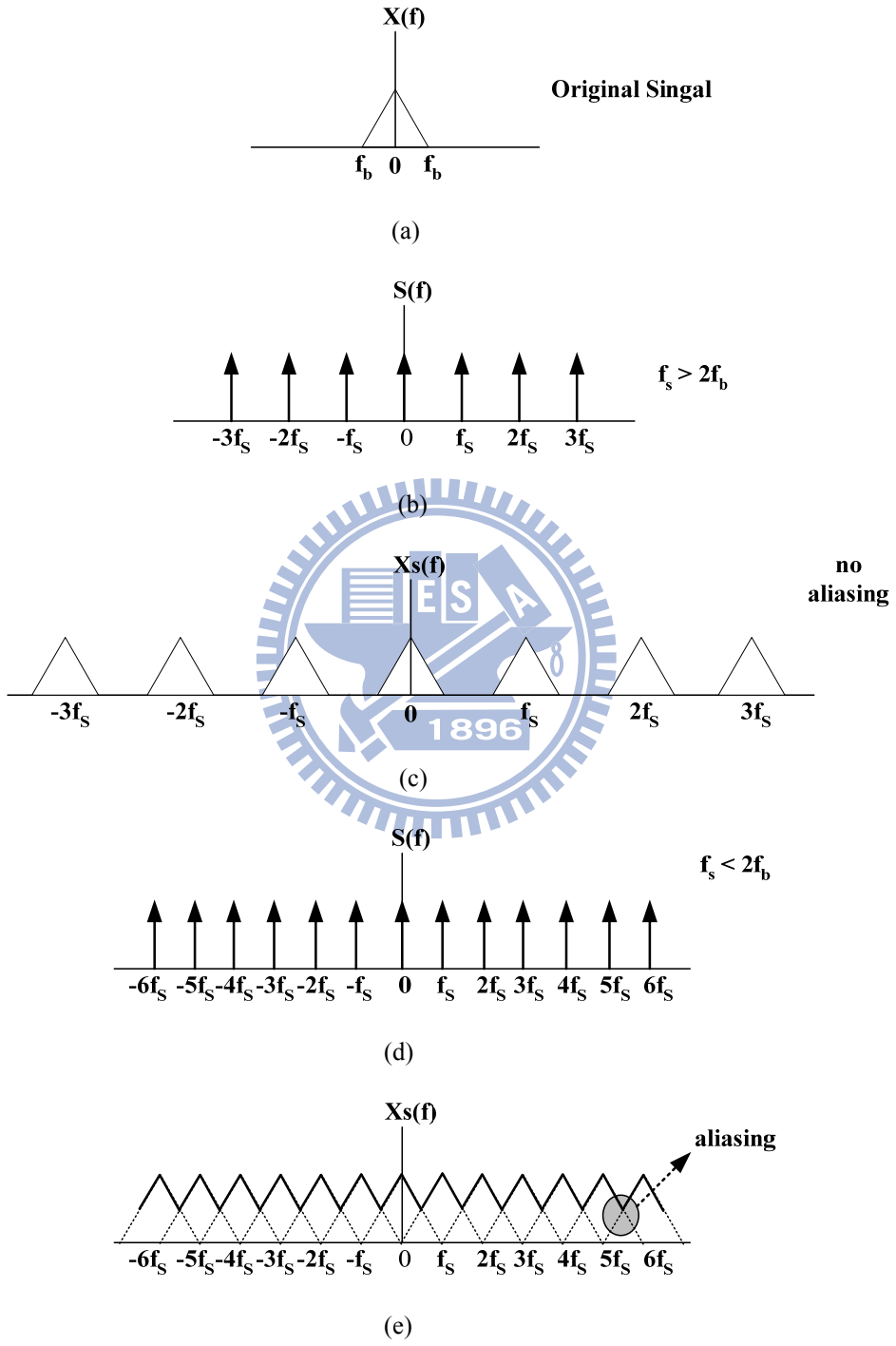


Fig. 2.1（a）Original signal spectrum（b）Sample function when fs > 2fB（c）Signal spectrum that' sampled by (b)（d）Sample function when fs < 2fB（e）Signal spectrum that sampled by (d)

2.2 Quantization noise and Peak SNR

We can get a discrete-time signal by sampling a continuous-time signal, and this sampled signal can be converted to digital signal. Quantization will appear in this process, the basic concept of quantization is to classify the original signal to different levels according to its level to determine the bit number of this signal, as shown in Fig. 2.2

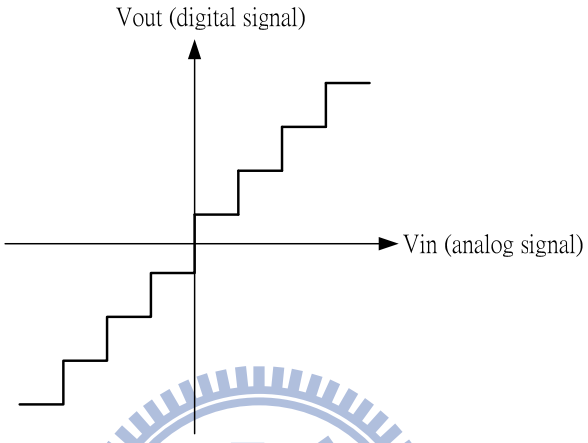
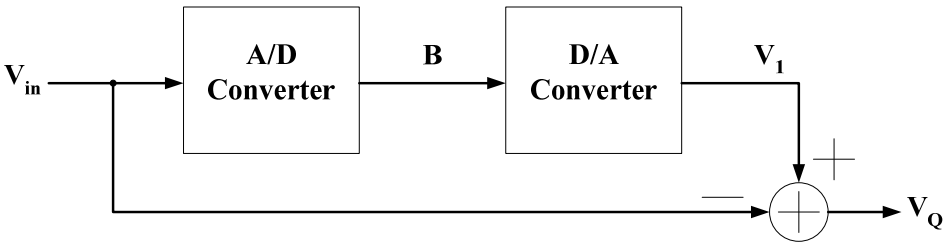


Fig. 2.2 Quantization process

It will have quantization error even in an ideal analog-to-digital converter. As shown in Fig .2.3, we convert the digital signal B to analog signal V_1 by a D/A converter, and then the signal V_1 is subtracted by input signal Vin. The result is the quantization error V_Q, as in (2.2) [20].

$$V_Q = V_{in} - V_1 \qquad (2.2)$$



Quantization noise $V_Q = V_{in} - V_1$

Fig. 2.3 Quantization error caused by A/D converter

The range of quantization error is limited in $\pm V_{LSB}/2$ (as in Fig. 2.4), and we assume the probability density function of quantization error is uniformly distributed between $\pm V_{LSB}/2$ and its mean is zero, as shown in Fig. 2.5. From this assumption, we can easily get the quantization noise power $V_{Q(rms)}^2$ in (2.3).

$$V_{Q(rms)}^2 = \int_{-\infty}^{\infty} x^2 \cdot f_Q(x) \cdot dx = \frac{1}{V_{LSB}} \int_{-VLSB/2}^{VLSB/2} x^2 \cdot dx = \frac{V_{LSB}^2}{12} \quad (2.3)$$

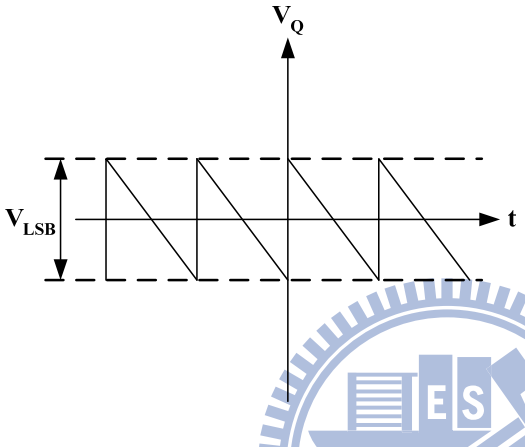


Fig. 2.4 Quantization error range

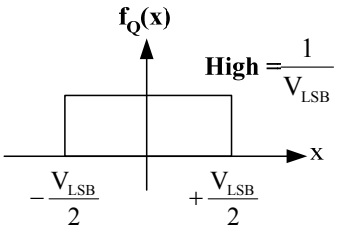


Fig. 2.5 P.D.F of quantization error

From (2.3) we can know the quantization noise power is proportional to square of V_{LSB}, and V_{LSB} can be represented as in (2.4). Therefore, we can say that the quatization noise will reduce by increasing quantization bit number.

$$V_{LSB} = \frac{FS}{2^B} \quad (2.4)$$

FS=Full scale = $V_{ref+} - V_{ref-}$　　B：Quantization bit number

Assume that input signal is sinusoidal, expressed as $V_{in}(t) = A \sin\omega t$, so the input signal power $V_{in(rms)}^2$ is as （2.5）. In （2.5）, we define the amplitude of input signal is the full scale of reference voltage, and from (2.3), (2.4) and (2.5), the peak SNR(Peak Signal-to-Noise Ratio) can be derived as in (2.6).

$$V_{in(rms)}^2 = \frac{1}{T} \int_{-T/2}^{T/2} (A \cdot \sin \omega t)^2 \cdot dt = \frac{A^2}{2} = \frac{(2A)^2}{8} = \frac{FS^2}{8} \quad (2.5)$$

$$PSNR = 10 \log\left(\frac{V_{in(rms)}^2}{V_{Q(rms)}^2} \right) = 6.02B + 1.76 \text{ dB} \quad (2.6)$$

(2.6) is the result obtained by Nyquist sampling rate. From (2.6), we can know that each additional bit number in quantizer increases 6dB in SNR. In Nyquist A/D converters, increasing the resolution of quantizer (decrease V_{LSB}) while reducing the quantization noise is a general method to reach higher SNR, but this method is sensitive to mismatches of analog device. Therefore, the general Nyquist A/D converter is not easily to implement with high resolution.

2.3 Techniques of Sigma-Delta Modulator

ΣΔ A/D converters are based on oversampling and noise shaping to reach high resolution. Oversampling means the sampling rate is much higher than Nyquist rate, about 8~512 times in general applications. The goal of oversampling is to expand quantization noise to wider range. It can reduce the quantization noise in signal bandwidth and increase the DR (Dynamic range) of input signal. Noise shaping is a technique that moves noise to high frequency, which is done by using discrete time filter and feedback technique. After noise shaping, the noise in high frequency can be filtered out by a digital filter [21].

2.3.1 Oversampling Technique

First, we made the assumption that quantization noise is a uniform distribution in sampling spectrum so its mean is zero and is a white noise [22]. The system in Fig. 2.6 just has oversampling function and does not have noise shaping effect. If a A/D converter is sampled in Nyquist rate, then the quantization noise is uniform distributed between $\pm f_B$; if it is sampled by oversampling technique, then quantization noise is uniform distributed between$\pm$ $f_{S2}/2_s$, which is much larger than f_B. As shown in Fig. 2.7, if the signal bandwidth is between $\pm f_B$, then quantization noise in this bandwidth will be reduced by using oversampling technique, which will raise PSNR significantly.

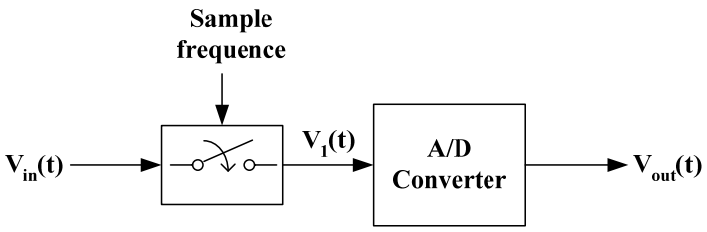


Fig. 2.6 Sampling system

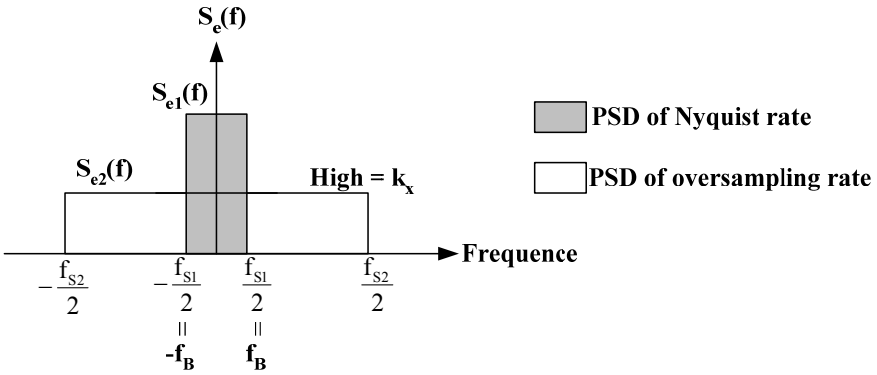


Fig. 2.7 Noise distribution after sampling

In the condition of oversampling, the PSD (Power Spectrum Density) of quantization noise is as $S_{e2}(f)$ in Fig. 2.7 and can be represented as:

$$k_x^2 = \frac{V_{LSB}^2}{12 \cdot f_s} = S_{e2}^2(f) \qquad (2.7)$$

From (2.7) we can estimate the quantization noise in $2f_B$ after oversampling

$$P_Q = \int_{-f_B}^{f_B} k_x^2 \cdot df = \frac{2f_B}{f_S} \cdot \frac{V_{LSB}^2}{12} = \frac{FS^2}{12 \cdot 2^{2B} \cdot OSR} \qquad (2.8)$$

In (2.8), we define a parameter OSR (Oversampling Ratio) as

$$OSR = \frac{f_S}{2f_B} \qquad (2.9)$$

Finally, we can get PSNR from (2.5) and (2.8)

$$PSNR = 10 \log\left(\frac{P_{signal}}{P_Q}\right) = 6.02B + 1.76 + 10 \log(OSR) \qquad (2.10)$$

From (2.10), we can find that doubling OSR will increase 3dB in PSNR, which is about 0.5 bit increase in resolution. Although oversampling can reduce quantization noise, it is difficult

to reach high SNR when using a low bit quantizer. For example, if we need a 16bit A/D converter, then SNR must be equal to 98dB, if the signal bandwidth is 20KHz, then the sampling rate must equal to $2 \times 10^9 \times 20\text{KHz}$, it is impossible to implement. Because at such high frequency, quantization noise is no longer a white noise, it is correlated with input signal. So there is not only oversampling technique, we must add noise shaping technique also, if we want to achieve high resolution.

2.3.2 Noise Shaping

We can model a general ΣΔ modulator and its linear model as shown in Fig. 2.8.

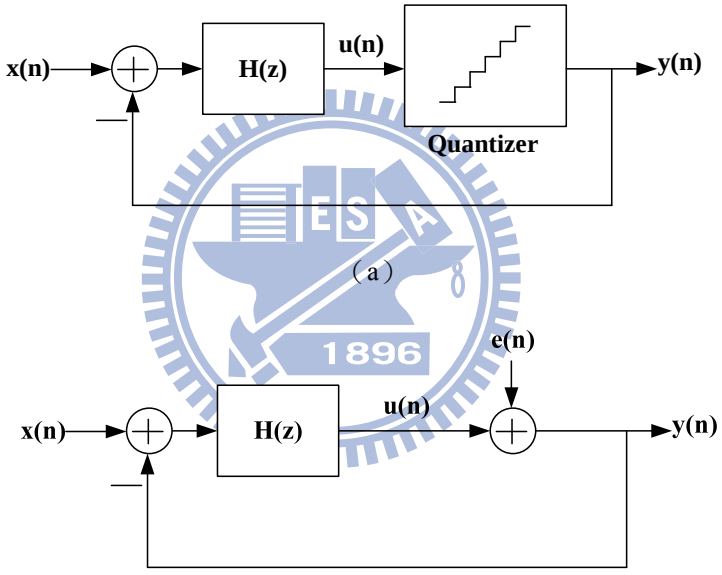


Fig. 2.8 (a) General ΣΔ modulator (b) Linear model with quantization noise

From Fig. 2.8(a), we can derive output Y(z) as (2.11)

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \qquad (2.11)$$

and define Signal Transfer Function S_{TF} and Noise transfer function N_{TF} as

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \qquad (2.12)$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \qquad (2.13)$$

where H(z) is the transfer function of a discrete time filter. There have two important meanings in (2.12), (2.13). If we want to obtain highest SNR, S_{TF} must be equal to 1, that means the input signal can transfer to output without attenuating; and N_{TF} (z) must be equal to 0, because the quantization noise will not affect output SNR.

In order to make N_{TF} (z) be a high pass filter, so at DC(z = 1), N_{TF} must be 0, and z = 1 is a pole of H(z), so the transfer function H(z) of the discrete filter is as

$$H(z) = \frac{1}{Z-1} = \frac{Z^{-1}}{1-Z^{-1}} \qquad (2.14)$$

Substitute (2.14) into (2.12) and (2.13), we can get

$$S_{TF}(z) = \frac{1}{z} \qquad (2.15)$$

$$N_{TF}(z) = 1 - \frac{1}{z} \qquad (2.16)$$

And we substitute z with $e^{j\frac{2\pi f}{fs}}$, then we can plot $|S_{TF}(f)|^2$ and $|N_{TF}(f)|^2$ in frequency domain, as Fig. 2.9. We can find $|N_{TF}(f)|^2$ also increases with frequency, and $|S_{TF}(f)|^2$ is always equal to 1, if we choose signal bandwidth in low frequency, then we can get highest signal power and lowest noise power, from this figure we see that quantization noise is moved to higher frequency significantly, this is the noise shaping effect.

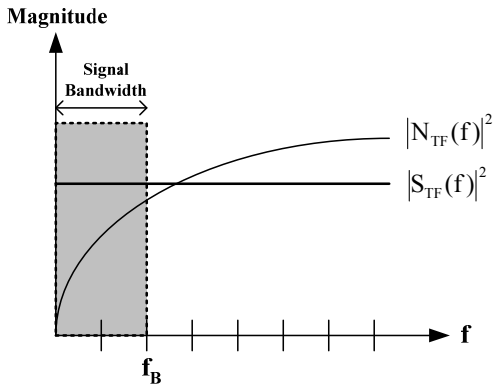


Fig. 2.9 Noise shaping

After noise shaping, we can filter out the noise in high frequency by using digital filter, and we will illustrate its architecture more detail in the next chapter.

2.4 Architectures of Sigma-Delta Modulator

Before we introduce various architectures of ΣΔ modulators, we must to realize the basic architecture of a general ΣΔ A/D converter. Fig. 2.10 is a complete block diagram of a ΣΔ A/D converter [20], and we can divide it into two different parts. First part is the ΣΔ modulator. The main function of this part is doing oversampling and noise shaping to the input analog signal. Second part is the decimation filter. The main function of this part is to remove noise in high frequency and down sampling the sampling frequency to base band frequency.

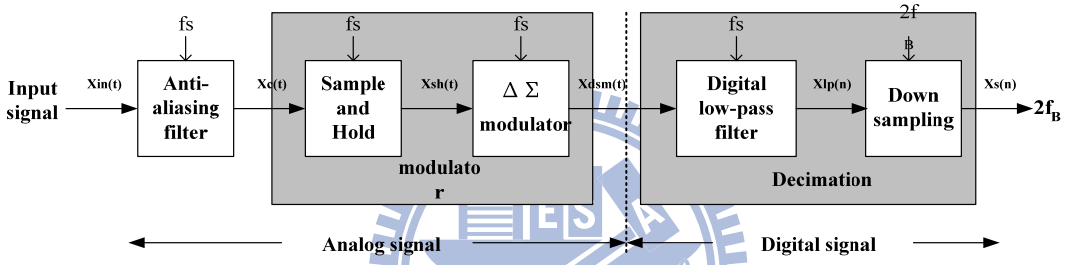


Fig. 2.10 Block diagram of ΣΔ A/D converter

First, the input signal Xin(t) pass an Anti-aliasing filter, the 3dB frequency of this filter is about few times of Nyquist frequency, so signal and noise out of Nyquist frequency is filtered roughly, and this signal goes into the ΣΔ modulator after goes through a S/H circuit. However, in the circuits implement situation, the sample and hold function is included in the circuits of ΣΔ modulator, so the signal Xc(t) will pass this modulator and produces a high speed data code Xdsm(n), because of noise shaping, the quantization noise will appear in high frequency. Finally, we must filter the noise in high frequency and reduce the sampling frequency to Nyquist frequency by a decimator, and passes the digital signal to the output [20].

In this chapter, we will focus on the architectures of ΣΔ modulator, because that the noise model and optimal method is focus on this part, we must understand the theorem,

benefits and drawbacks of each kinds of ΣΔ modulators. In addition, the implement of decimator is very typical [23, 24]. In today's technology, DSP processors are also used to replace decimators, so we will introduce this part roughly.

2.4.1 First-Order Sigma-Delta Modulator

We recall that H(z) in (2.14) is $\frac{Z^{-1}}{1-Z^{-1}}$, substitute it into Fig. 2.8, then we can get a first-order ΣΔ modulator; Analyze transfer function H(z) from time-domain, it indicates that output signal m(t) is obtained by adding the delayed input signal n(t-1) and the delayed output signal m(t-1), so we can express a complete first-order ΣΔ modulator as Fig. 3.2.

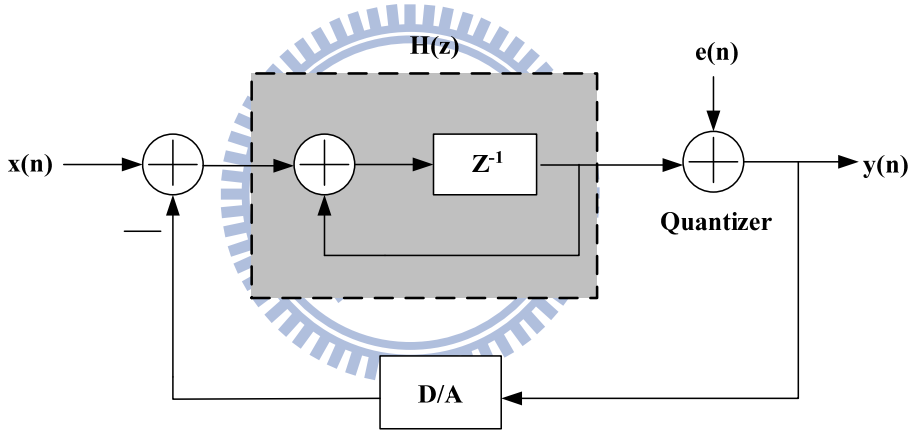


Fig. 2.11 First-order ΣΔ modulator

H(z) in Fig. 2.11 is indicated the effects of delay and accumulation, this is equivalent with an integrator in circuit design, so the three circuits components of ΣΔ modulator are integrator, quantizer and DAC in the feedback path. A first order ΣΔ modulator's output can represent as

$$Y(z) = z^{-1}X(z) + (1-z^{-1})E(z) \qquad (2.17)$$

From (2.17) we can find the signal transfer function is as a delay function, and noise transfer function is as a high pass filter, moves the noise to high frequency. In order to derive PSNR of first order ΣΔ modulator, we must get the magnitude of $N_{TF}(z)$ and $S_{TF}(z)$ in the frequency

domain, so we substitute z with $e^{j2\pi \cdot f/f_s}$, and get $|S_{TF}(f)|$ and $|N_{TF}(f)|$ respectively as:

$$|S_{TF}(f)| = |z^{-1}| = |e^{-j2\pi \cdot f/f_s}| = 1 \qquad (2.18)$$

$$N_{TF}(f) = 1 - e^{-j2\pi \cdot f/f_s} = \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi \cdot f/f_s}$$

$$\Rightarrow \quad |N_{TF}(f)| = 2 \cdot \sin(\frac{\pi f}{f_s}) \qquad (2.19)$$

So the quantization noise in base band $\pm f_B$ can obtain by (2.7) and (2.19)

$$P_Q = \int_{-f_B}^{f_B} S_e^{\,2}(f) \cdot |N_{TF}(f)|^2 df = \int_{-f_B}^{f_B} \frac{V_{LSB}^{\,2}}{12 \cdot f_s} \cdot \left[2\sin\left(\frac{\pi f}{f_s} \right) \right]^2 \cdot df \qquad (2.20)$$

Because that f_B is much lower than f_s, so $\sin(\pi f/f_s)$ is approximate equal to $(\pi f/f_s)$, and P_Q is as

$$P_Q = \frac{V_{LSB}^{\,2} \pi^2}{36} \cdot (\frac{1}{OSR})^3 = \frac{FS^2 \cdot \pi^2}{36 \cdot 2^{2B} \cdot OSR^3} \qquad (2.21)$$

From (2.5) and (2.21), if we have the maximum signal power, then PSNR is as (2.22)

$$PSNR = 10 \log(\frac{P_{signal}}{P_Q}) = 10 \log(\frac{3}{2} 2^{2B}) + 10 \log[\frac{3}{\pi^2} (OSR)^3]$$

$$= 6.02B + 1.76 - 5.17 + 30 \log(OSR) \qquad (2.22)$$

From (2.22), we find that each octave of OSR, PSNR will increase 9dB, increase 1.5 bit in resolution. Compare (2.22) with (2.10) that only has oversampling effect; we can find that 1st order noise shaping increases the performance of ΣΔ modulator.

2.4.2 Single-Loop Second-Order Sigma-Delta Modulator

When the discrete time filter in Fig. 2.8 is replaced by two cascade integrator, then it is a second order ΣΔ modulator, output of the first integrator is only connecting with the input of the second integrator, it is shown in Fig. 2.12

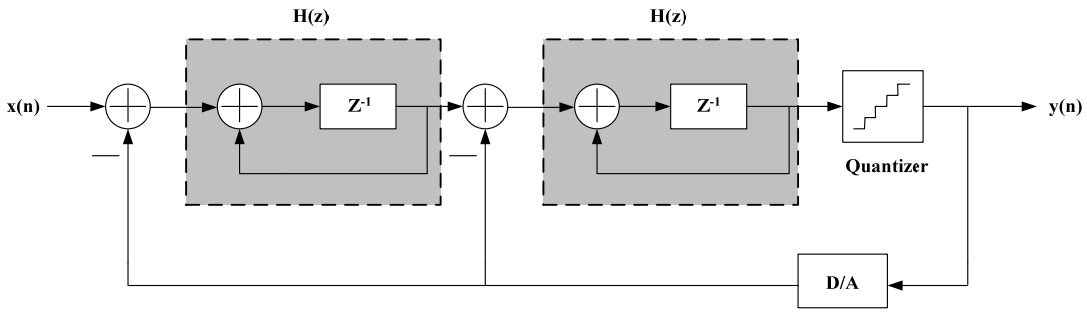


Fig. 2.12 Single loop second order ΣΔ modulator

Then the output of it can easily be derived as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \quad (2.23)$$

where S_{TF} and N_{TF} is as

$$S_{TF}(z) = z^{-2} \quad (2.24)$$

$$N_{TF}(z) = (1- z^{-1})^2 \quad (2.25)$$

Using the same method in (2.19) (2.20), we can obtain

$$|S_{TF}(f)| = 1 \quad (2.26)$$

$$|N_{TF}(f)| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \quad (2.27)$$

$$P_Q = \frac{V_{LSB}{}^2 \cdot \pi^4}{60 \cdot OSR^5} = \frac{FS^2 \cdot \pi^4}{2^{2B} \cdot 60 \cdot OSR^5} \quad (2.28)$$

So finally, PSNR of the second order ΣΔ modulator is as

$$PSNR = 10\log\left(\frac{P_{signal}}{P_Q}\right) = 10\log\left(\frac{3}{2}2^{2B}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

$$= 6.02B + 1.76 - 12.9 + 50\log(OSR) \quad (2.29)$$

In the single loop second order architecture, each octave of OSR can increase PSNR by 15 dB, it is equivalent to 2.5 bit in resolution. If we compare (2.29), (2.27) with $|NTF(f)|=1$ that without noise shaping, as Fig. 2.13, we can find that in our needed signal bandwidth, the quantization noise is highest when $|NTF(f)|=1$, and that with second order noise shaping is

smallest among this figure [20].

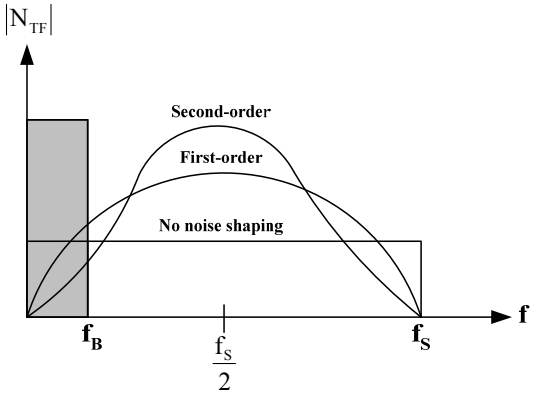


Fig. 2.13 Comparison of noise shaping techniques

2.4.3 Single-Loop High Order Sigma-Delta Modulator

Fig. 2.14 is a single loop high order ΣΔ modulator, from the derivation in Section 2.4.1 and Section 2.4.2, we can get the quantization noise P_Q in signal bandwidth is as

$$P_Q = \frac{V_{LSB}^2}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{OSR}\right)^{2L+1}, \text{L : order} \qquad (2.30)$$

and its PSNR is

$$PSNR = 6.02B + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \qquad (2.31)$$

In the application of high order ΣΔ modulator, (6L+3)dB increases in SNR when OSR is octave, so PSNR can be raised by increasing the order of the system, especially at large oversampling ratio. But sometimes in high order architecture, the performance will be worsen than result predicted by (2.29), because of the stability problem, it will make less effective noise shaping function, so the quantization noise will not be suppressed completely.

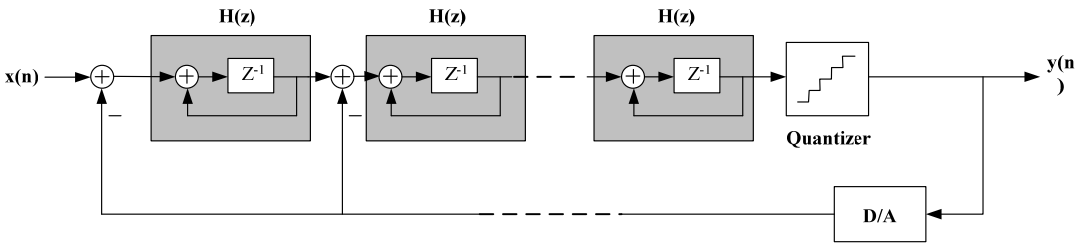


Fig 2.14 Single-loop high order ΣΔ modulator

2.4.4 Interpolative Sigma-Delta Modulator

Interpolative is a kind of high order ΣΔ modulator, it changes connection of some stages, adds some feed forward paths and feedback paths in order to suppose more aggressive noise shaping effect, Fig. 2.15 is a four-order interpolative architecture ΣΔ modulator [16].

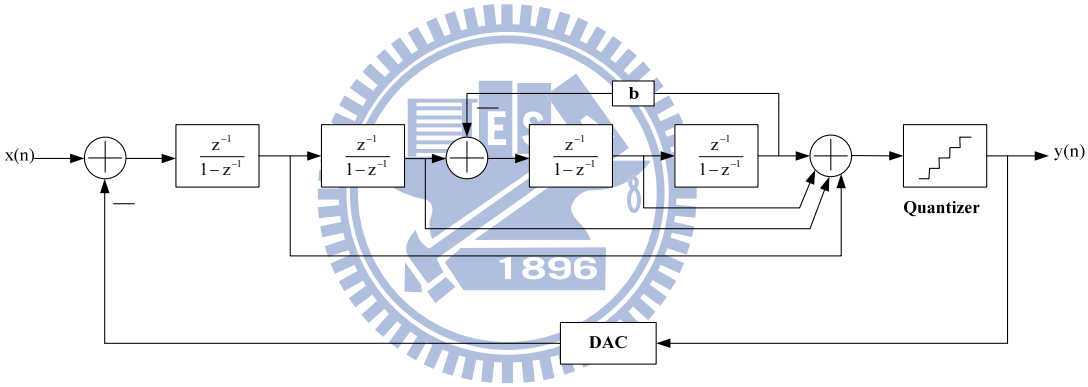


Fig. 2.15 Four-order interpolative architecture

This architecture also has stability problem, when the order L increases, each integrator produces one pole, and when the order is higher, poles of this system will also increase, and it will cause unstable situation, so the range of integrator gain will be limited; if the range of integrator gain is small, oscillation will appear in the circuits. Another is the considerations of clock control, when we use SC (switched-capacitor) to implement the integrator, each integrator needs two clocks to control its operation, and we will need more clock to control the integrator when the order of system increases, it will produce more problems.

2.4.5 MASH Architecture

MASH (Multi-stage noise shaping) architecture is also called cascade architecture, which is a method that cascades several low order loops modulator in order to get high order noise shaping effect. The fundamental ideal of MASH is delivering quantization noise of front stage to input of next stage, and combining the digital outputs of all the stages with proper transfer function in digital domain, only the quantization noise of last stage will appear at the output, and the orders of N_{TF} is the same with total orders in the cascade $\Sigma\Delta$ modulator. Fig 2.16 is a three-order cascade $\Sigma\Delta$ modulator, its is the combination of a second-order and first-order $\Sigma\Delta$ modulator, so also called 2-1 cascade architecture.

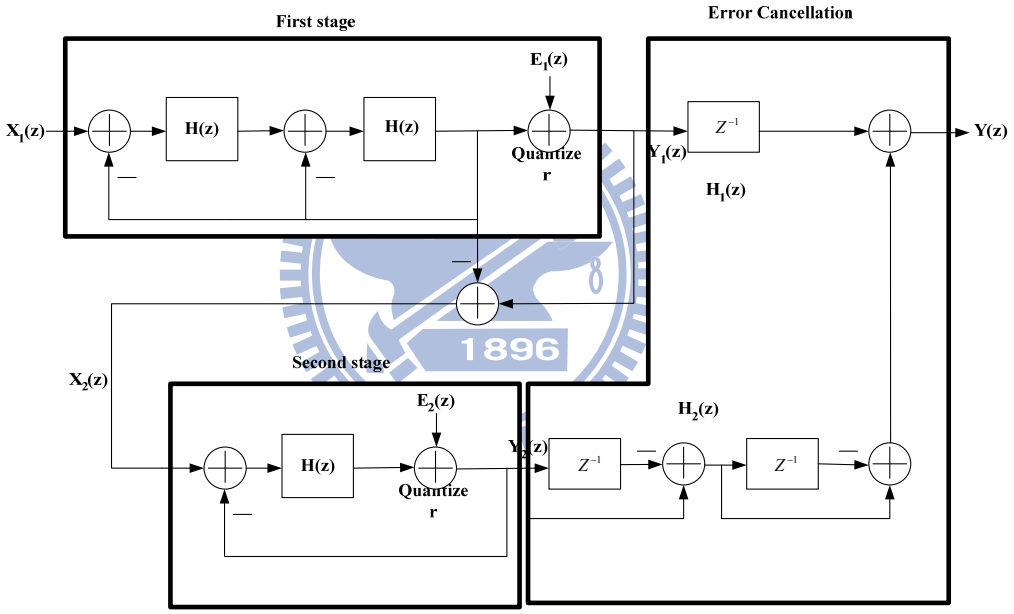


Fig. 2.16 2-1 architecture MASH $\Sigma\Delta$ modulator

From Fig. 2.16, we can derive the first stage output $Y_1(z)$ can be represented as

$$Y_1(z) = z^{-2}X_1(z) + (1-z^{-1})^2E_1(z) \quad (2.32)$$

Output of second stage $Y_2(z)$ is as

$$Y_2(z) = z^{-1}X_2(z) + (1-z^{-1})E_2(z) \quad (2.33)$$

and overall output of MASH $Y(z)$ is as

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \quad (2.34)$$

and we can say that second stage input $X_2(z)$ is almost the same with $E_1(z)$, in order to

eliminate first stage quantization noise $E_1(z)$, from (2.32) ~ (2.34), we can define the error cancellation functions $H_1(z)$ and $H_2(z)$ as

$$H_1(z) = z^{-1} \quad (2.35)$$

$$H_2(z) = (1-z^{-1})^2 \quad (2.36)$$

From (2.32)~(2.36), $E_1(z)$ can be eliminated, and second stage quantization noise $E_2(z)$ is shaped by third-order noise shaping function, and the MASH output Y(z) is as

$$Y(z) = z^{-3}X_1(z) + (1-z^{-1})^3E_2(z) \quad (2.37)$$

The most significant advantage of this architecture is that stability is not an issue, because it is composed by several low-order systems, and the quantization noise will not be amplified stage by stage, so its stability is good. Most important, the noise shaping function is equivalent as high order ΣΔ modulator, so it is popular in recent publications [25, 26]. However, there also have some drawbacks of this topology; it is sensitive to the circuits' imperfections, such as finite DC gain of OTA, variance of integrator gain due to capacitor mismatch and non-zero switch resistance. These are all practical considerations when we design a MASH architecture ΣΔ modulator [27].

2.4.6 Multi-bit Quantizer Sigma-Delta Modulator

The demands of high resolution and high bandwidth ADC are more and more in recent years. In a high signal bandwidth, OSR of ΣΔ ADC can't be too high, and the peak SNR of a ΣΔ modulator with such limited OSR can't satisfy of high resolution applications, if we use higher order architecture, then the performance will degrade due to instability. So the most general method to increase performance is to use multibit quantizer. The most obvious advantage of using multibit quantizer is that the distance between quantizer level V_{LSB} in (2.4) is much smaller due to increasing of B, and according to (2.3), the power of quantization noise is attenuated. Fig. 2.17 is the results of theoretical peak SNR of ΣΔ modulator versus oversampling ratio, with different order and quantizer bits, it is noted that peak SNR of the

same OSR is increase 6 dB with each additional bit number in quantizer, and at low OSR, low order higher bit number architecture has equivalent performance as high order architecture. This result is usable for high bandwidth applications, and the power consumption of digital circuit in ΣΔ modulator is reduced due to lower sampling rate [28].

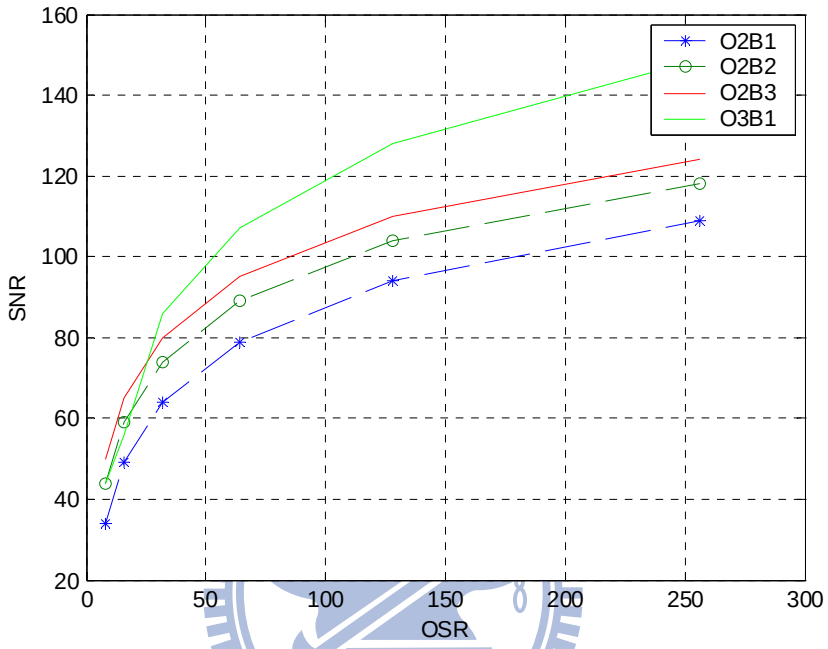


Fig. 2.17 SNR vs. OSR with different quantizer bit number

Because of using multi-bit quantizer, so we also need to use multi-bit DAC(Digital-to Analog Converter) to transfer the digital output to analog signal, and feed it back to integrator. The most significant disadvantage is the non-linearities introduced by multi-bit DAC can degrade the performance of ΣΔ converter, like Fig. 2.18. It is a linear model of multi-bit ΣΔ modulator, where E(Q) and E(D) represent the quantization noise and feedback DAC noise respectively. The values of these capacitor elements in DAC will not equal to ideal values that we need, it is due to process variation, typical value of mismatch in modern CMOS technology is about 0.05% ~ 0.5%. In recent years, so many researches are make efforts on reduce DAC noise due to mismatch, such as trimming [21], Dynamic element matching(DEM)[29, 30], although trimming is effective, but it has a expensive production step. So, DEM becomes more and more popular because of its efficiency and cheaper cost.

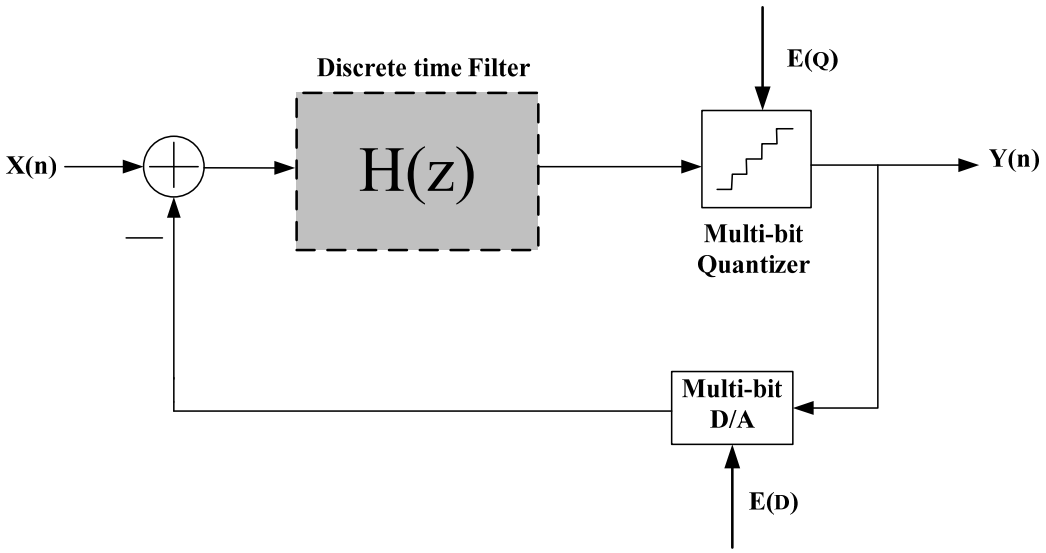


Fig. 2.18 Multi-bit architecture

2.4.7 Multi-bit Sigma-Delta Modulator use DEM Technique

Dynamic element matching is a different approach to decrease the DAC noise, it is used to improve the linearity of pure DACs [31], but now it is most used in inner DAC of multi-bit ΣΔ modulator. A DAC with DEM technique is illustrated in Fig. 2.19, 2^B bits thermometer code is put into the element selection logic block, and the function of element selection logic is try to select DAC elements in such way let the errors introduced by DAC average to zero for several operation periods. Because the DEM block is located in feedback loop, so its delay must be very small prevent to degrade the performance of ΣΔ converter, therefore the algorithm used in the DEM block must be simple. There are several techniques of DEM, such as Randomization [32], Clocked Averaging (CLA) [3], Individual Level Averaging (ILA) [33], Data Weighted Averaging (DWA) [3], Randomization is the first approach to use DEM technique in ΣΔ ADC, and DWA offers a good performance to reduce DAC error, in this section, an overview introduction of these two algorithms will be presented, and the operation principle of them will be explained.

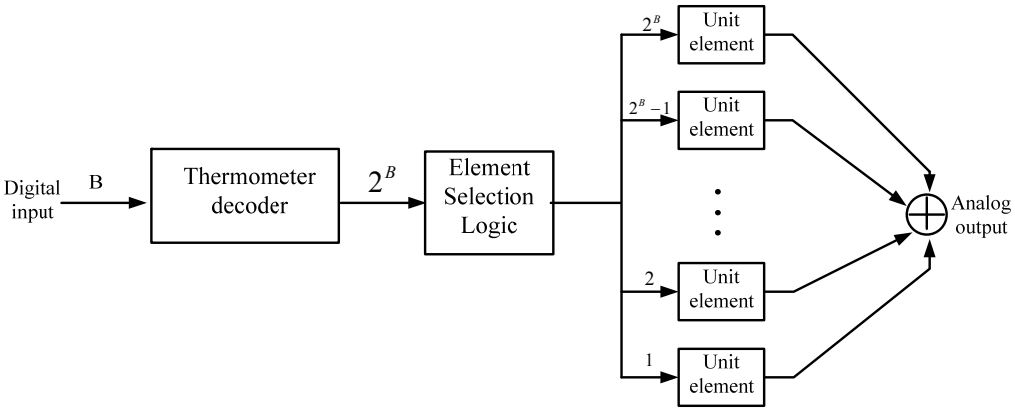


Fig. 2.19 A B-bit DAC with DEM technique

2.4.8 Decimator

In ΣΔ A/D converter, digital decimator is used to process digital signal of the quantizer output, the high speed data word after oversampling modulation can't be used directly. Because there have original signal and quantization noise among it, so the main function of decimator is to convert the oversampled B-bit output words of the quantizer at a sampling rate of fs to N-bit words at Nyquist rate of input, and removes the noise out of signal band. In order to prevent the noise introduced by other frequency, the decimator filter must have very flat signal pass-band, and sharp transition region and enough signal attenuation in stop band. Two-stage decimator is used in a general situation, because that single stage decimator is difficult to convert sampling rate to Nyquist rate in 1 time and without degrading SNR. In the first stage, we can down-sample the sample frequency to 2~4 times of Nyquist frequency, and in the second stage, we can use IIR or FIR filter that have high linearity [21]. For a large OSR, multi-stage decimator is used.

2.4.9 Performance Metrics for a ΣΔ Modulator

In order to understand the performance merits used to specify the behavior of ΣΔ modulator, several specifications concerning the performance are discussed [34].

- **Signal to Noise Ratio:** The SNR of a data converter is the ratio of the signal power to the

noise power, measured at the output of the converter for a certain input amplitude. The maximum SNR that a converter can achieve is called the peak SNR.

- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for a certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.
- **Dynamic Range at the input:** The DR_i is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is determined by the noise floor of the converter.
- **Dynamic Range at the output:** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic range at the output DR_o, which is exactly equal to peak SNR.
- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also includes the distortion components and can be calculated from (2.6) as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{2.38}$$

- **Overload Level:** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 2.17. This figure shows the SNR and SNDR of the $\Sigma\Delta$ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently, the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the

modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specifications are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 2.20 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

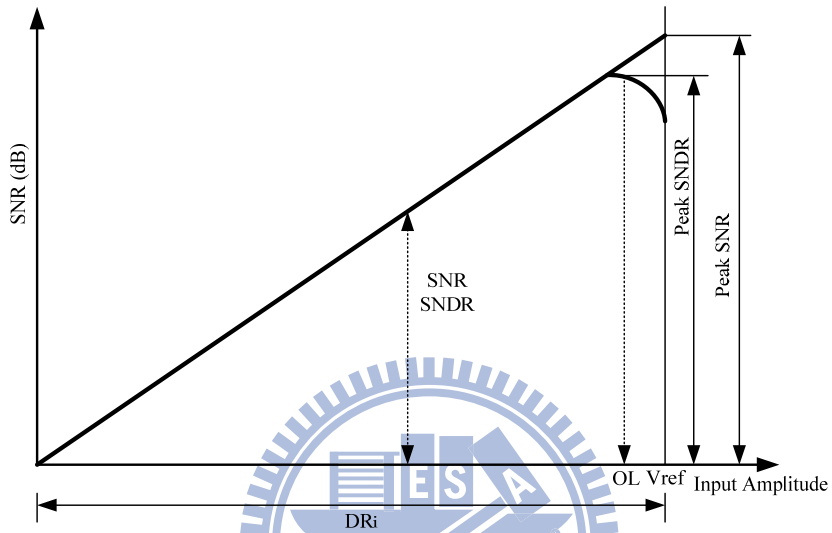


Fig. 2.20 Performance characteristic of a $\Sigma\Delta$ converter

3.
Models of Sigma-Delta Modulator Noises Power

Proposing an optimization algorithm for searching design parameters which maximize ΣΔ ADC SNR while minimize power consumption, is one of the primary purposes of this paper. Related model completeness determines success of this goal. The ΣΔ modulator nonidealities are categorized into five parts in this chapter; finite OTA gain error, thermal noise, settling error, multi-bit DAC noise, and jitter noise. All nonideality models are expressed in noise power form, which can directly add to ideal quantization noise power. All noise power models discussed in the following are based on the integrator scheme, consumption model is presented as the last part of this chapter.

3.1 Clock Jitter Effects

As both the signal bandwidth and the required output SNR increase, clock jitter problems become more obvious. Jitter is usually defined as a random variation in clock signal period around the ideal value, and the value of jitter can be reasonably assumed as a Gaussian random variable with zero mean and standard deviation σ_{jit}. If there is some variation in clock high time, the input signal will be sampled at the wrong instant and receive a consequent voltage error. For a sinusoidal input signal with maximum amplitude A_i and frequency f_{in}, if it is sampled by a clock which has a jitter variation, then the voltage error is [35]:

$$\Delta V \cong 2\pi \cdot f_{in} \cdot A_i \cos(2\pi \cdot f_{in} \cdot t)\Delta T \qquad (3.1)$$

where ΔT is the variation of clock period with standard deviation σ_{jit}. Then the jitter

noise power becomes:

$$P_{jitt} = \frac{(2\pi \cdot f_{in} \cdot A_i)^2}{2} \cdot \frac{\sigma_{jit}^{\ 2}}{OSR} \qquad (3.2)$$

We consider the worst case in this work. That f_{in} and A_{in} are replaced by f_B and V_{ref} respectively.

Before discussing power consumption modeling, we summarize the nonideality modeling as follows. The leakage noise due to finite OTA gain can be considered as an additional quantization noise, so the total quantization noise will be higher than theoretical quantization noise, appearing at D2 in Fig. 4.9. All other nonidealities are modeled at D1 in Fig. 3.1, because we have modeled them as input-referred noise in the integrator input.

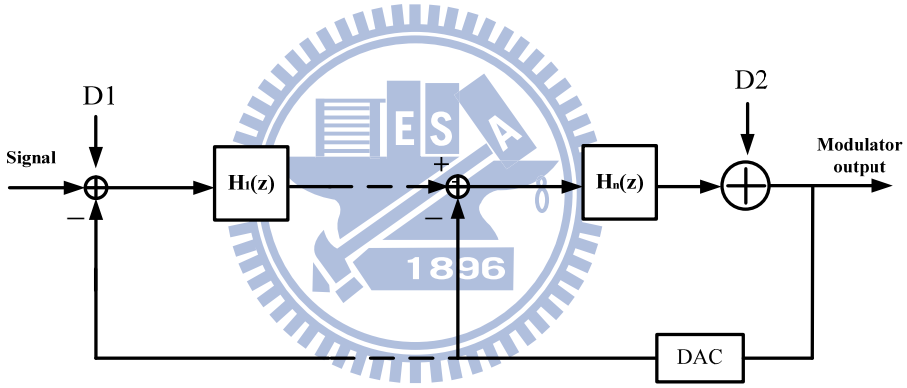


Fig. 3.1 Main nonidealities sources in the ΣΔ modulator

3.2 Thermal noise (Switch circuits)

There are three thermal noise sources in the ΣΔ modulator, in MOS switches, OTAs and reference voltage. We will analyze them separately as follows. For a fully differential implementation, the in band switch thermal noise during the sampling phase results in output noise power [36]

$$P_{sw1} = \frac{1}{OSR} \cdot \left(\frac{4kT}{C_S} \right) \qquad (3.3)$$

where k is Boltzman constant and T is the absolute temperature. Additional thermal noise is introduced by the switches during the integration phase, resulting in the output noise

power [34]

$$P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{4kT}{C_S} \right) \qquad (3.4)$$

Since the thermal noise voltages introduced during these two phases are uncorrelated, the total output switches thermal noise power from the switched capacitor integrator is

$$P_{sw} = P_{sw1} + P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{8kT}{C_S} \right) \qquad (3.5)$$

Half of P_{sw} is from the input branch, and the other half is from the DAC branch.

3.3 Finite OTA Gain Error

Finite OTA Gain is an important error when we analyze a real integrator. Typical value of OTA gain is about 50 ~ 80 dB in modern CMOS technology. For a general single-loop n th order $\Sigma\Delta$ modulator with finite OTA gain A_0, the modified quantization noise is expressed as [36]:

$$P_{Q(\text{mod.})} \cong \frac{\Delta^2}{12} \cdot \left[\frac{\pi^{2n}}{(2n+1) \cdot OSR^{2n+1}} + \left(\frac{a_1}{A} \right)^2 \cdot \frac{\pi^{2n-2} \cdot n}{(2n-1) \cdot OSR^{2n-1}} \right]$$

$$= P_Q + P_{AV} \qquad (3.6)$$

where P_Q is the original quantization noise, and Δ is the quantizer step size. The P_{AV} in (3.6) is due to finite OTA gain, and can be considered as an additive quantization noise power. It can be verified using (3.6) that, for a single-loop topology, $A = 50$ dB is sufficient to avoid SNR degrades, in the sense that a higher A_0 would not significantly reduce $P_{Q(\text{mod.})}$.

3.4 Multi-bit DAC noise

There are several advantages in using a multi-bit structure. One is that when the quantization step Δ decreases, quantization and settling noise reduce. Another is that a multi-bit structure improves stability and provides a higher overload level and more aggressive noise shaping function. However, due to CMOS process variations, there can be mismatches in the 2^B unit capacitors C_u of a B-bit DAC shown in Fig. 4.4. Assume that each unit capacitor distribution is Gaussian [37] around a nominal value. Let the normalized capacitance be

$$c_i = \frac{C_i}{\sum_{k=1}^{2^B} C_k}, \qquad 1 \le i \le 2^B \tag{3.7}$$

where C_i is the capacitance of the ith unit capacitor. Define the deviation of c_i as $e_i = c_i - c_m$, where

$$c_m = \frac{\sum_{i=1}^{2^B} c_i}{2^B} \tag{3.8}$$

Then voltage error caused by unit capacitor mismatches is given by [34]

$$e_{dac}(k) = V_{ref}\left(\sum_{i=1}^{x(k)} e_i - \sum_{i=x(k)+1}^{2^B} e_i\right) \tag{3.9}$$

where $x(k)$ represents the number of 1's in the feedback thermometer code at the time step k. The $e_{dac}(k)$ can be treated as an additive Gaussian noise in the $\Sigma\Delta$ modulator feedback path, the variance of which is

$$\begin{aligned}\sigma^2[e_{dac}] &= V_{ref}^{\,2}\left(x(k)\cdot\sigma^2[e_i] + (2^B - x(k))\cdot\sigma^2[e_i]\right) \\ &= V_{ref}^{\,2}\cdot 2^B\cdot\sigma^2[e_i] = V_{ref}^{\,2}\cdot 2^B\cdot\sigma_{cap}^{\,2}\end{aligned} \tag{3.10}$$

where σ_{cap} is the standard deviation of unit capacitor. Assuming the $e_{dac}(k)$ is also white, the average DAC noise power at the modulator output becomes

$$P_{dac} = \frac{1}{OSR} \cdot \mathrm{V_{ref}}^2 \cdot 2^B \cdot {\sigma_{cap}}^2 \qquad (3.11)$$

Apparently the dominating factor is B, since P_{dac} increases exponentially with respect to B. In order to reduce DAC error due to unit capacitor mismatch, several techniques have been proposed. The most efficient among these is the Data Weighted Averaging (DWA) [33], and it is shown in [38] that the DWA effect is a first-order noise shaping of the DAC noise. If the DWA is employed, the average DAC noise power at the modulator output is modified to be

$$P_{dac}(DWA) \cong \mathrm{V_{ref}}^2 \cdot 2^B \cdot {\sigma_{cap}}^2 \cdot \frac{\pi^2}{3 \cdot OSR^3} \qquad (3.12)$$

Equations (3.11) and (3.12) will be used to estimate the DAC noise power in the optimization process.

3.5 Settling noise

The settling error will produce settling noise and settling distortion, but settling distortion produced in large nonlinearity, the input signal settling in partial slewing about 50%. As mentioned above, the settling noise will vary large. So we only consider about settling noise in this paper.

In this section, the settling noise model [39] is a mathematical model what has no need to run behavior simulation. Settling noise is produced by non-idealities in OTA what causes nonlinear transfer characteristics. This nonlinearity is approximated by a nonlinear fitting which takes into account the time-domain distribution of SC integrator input $V_s(n)$ described in Fig. 4. The variance of $V_s(n)$ in second-order $\Sigma\Delta$ is $\sigma_{VS} = 1.4 \cdot \mathrm{V_{ref}}/2^B$ [39], but it is not exact enough to use. Because in different parameters $V_{ref} = 0.5 \cdot FS$ (Full Scale)、A_{in}、B and different stage of $\Sigma\Delta$, the variance will be change. In part I. there needs to find a variance equation from the parameters mentioned above.

3.5.1 Variance equation of V_S

A typical time domain histogram distribution of $v_s(n)$ is shown in Fig. 3.2.

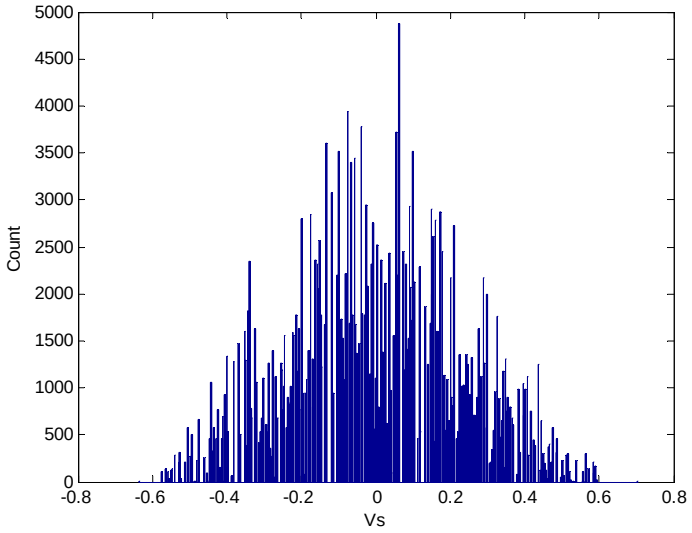


Fig. 3.2 Histogram distribution of $V_s(n)$.

The result is close to a Gaussian distribution. Therefore, we assume V_S is Gaussian distributed with a zero mean, and extensive simulations suggest that the relation between standard deviation $\sigma_{VS} \propto V_{LSB} = FS/2^B$ (Quantizer step size), and we suppose $2^B \cdot \sigma_{VS} / V_{ref}$ is a function of A_{in}、V_{ref} and polynomial $P_\alpha(B) = \sum_{n=0} \alpha_n \cdot B^n$ and $P_\beta(B) = \sum_{n=0} \beta_n \cdot B^n$ in (3.13).

$$2^B \cdot \sigma_{VS} / V_{ref} = P_\alpha(B) \cdot V_{ref} + P_\beta(B) \cdot A_{in} \tag{3.13}$$

We can use behavior simulation to find matrix function in (3.14) and using least-square solution to approximate $P_\alpha(B)$ and $P_\beta(B)$ in each B.

$$\begin{bmatrix} V_{ref1} & A_{in1} \\ \vdots & \vdots \\ V_{refN} & A_{inN} \end{bmatrix} \times \begin{bmatrix} P_\alpha(B) \\ \\ P_\beta(B) \end{bmatrix} = \begin{bmatrix} 2^B \cdot \sigma_1 / V_{ref1} \\ \vdots \\ 2^B \cdot \sigma_N / V_{refN} \end{bmatrix} \tag{3.14}$$

Finally we can calculate coefficients of $P_\alpha(B)$ and $P_\beta(B)$ in (3.15), but coefficient of

$P_\alpha(B)$ and $P_\beta(B)$ in different stage of ΣΔ are not the same. It has to calculate coefficients of each stage of ΣΔ.

$$\begin{bmatrix} \alpha_0 & \beta_0 \\ \vdots & \vdots \\ \alpha_N & \beta_N \end{bmatrix} = \begin{bmatrix} 1^0 & \cdots & 1^N \\ \vdots & \ddots & \vdots \\ N^0 & \cdots & N^N \end{bmatrix}^{-1} \times \begin{bmatrix} P_\alpha(1) & P_\beta(1) \\ \vdots & \vdots \\ P_\alpha(N) & P_\beta(N) \end{bmatrix} \tag{3.15}$$

Assume that the quantizer bit number is less than 6 in optimization module, the coefficients of $P_\alpha(B)$ and $P_\beta(B)$ are in TABLE 3.1.

		1st-order ΣΔ		2nd-order ΣΔ Mash 2-1, Mash 2-2	
α_0	β_0	2.6700	-1.9925	-5.5696	5.7689
α_1	β_1	-3.1090	2.7998	14.2976	-13.0144
α_2	β_2	1.5341	-1.5182	-9.7848	8.8548
α_3	β_3	-0.3820	0.3968	2.9032	-2.6518
α_4	β_4	0.0471	-0.0501	-0.3980	0.3674
α_5	β_5	-0.0023	0.0025	0.0207	-0.0193

TABLE 3.1 Coefficient of polynomial

3.5.2 Settling noise power of integration phase

Behavioral descriptions for settling errors are well known [40, 41]. The settling error during the sampling phase is:

$$\varepsilon_1 = V_S \cdot \exp(-\frac{T}{2 \cdot \tau_1}) \tag{3.16}$$

The settling error only consider of the error in integration phase, because $\tau_1 << \tau_2$. Then minimum ε_2 that occurs in linear settling will large than ε_1.

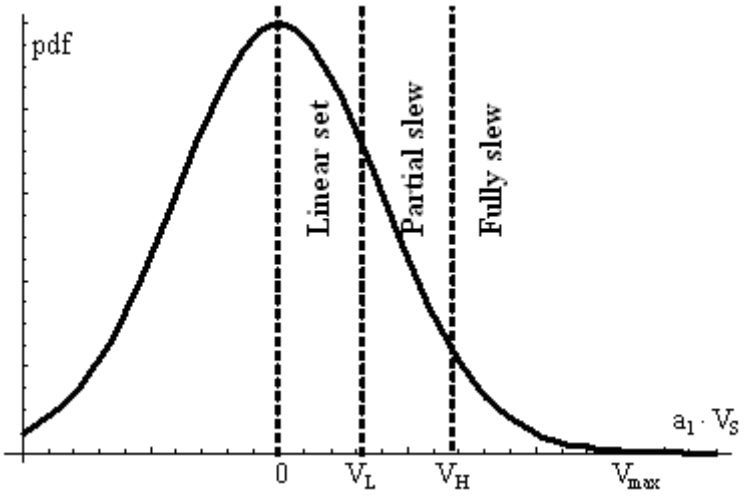


Fig. 3.3 Three types of settling conditions in integration phase

The settling error ε_2 during the integration phase can be divided into three cases:

Linear settling:

$$\varepsilon_2 = a_1 \cdot V_S \cdot \exp(-\frac{T}{2 \cdot \tau_2}), \text{ when } \quad 0 < |a_1 \cdot V_S| < V_L \tag{3.17}$$

Partial slewing:

$$\varepsilon_2 = SR \cdot \tau_2 \cdot \text{sgn}(V_S) \cdot \exp(\frac{a_1 \cdot |V_S|}{SR \cdot \tau_2} - \frac{T}{2\tau_2} - 1), \text{ when } \quad V_L < |a_1 \cdot V_S| < V_H \tag{3.18}$$

Fully slewing:

$$\varepsilon_2 = a_1 \cdot V_S - SR \cdot \text{sgn}(a_1 \cdot V_S) \cdot \frac{T}{2}, \text{ when } \quad V_H < |a_1 \cdot V_S| < V_{max} \tag{3.19}$$

In fig. 3.3, the boundary voltage $V_L = SR \cdot \tau_2$ 、 $V_H = (\frac{T}{2} + \tau_2) \cdot SR$ and $V_{max} = a_1 \cdot (V_{ref} + A_{in})$. The parameter SR is the slew rate of OTA, a_1 is a constant produced by charge sharing effect, and $\tau_2 = \frac{1 + 2\pi \cdot GBW \cdot R_S \cdot C_S}{2\pi \cdot GBW}$ is the charging time constant in the integration phase, with GBW being the equivalent gain bandwidth in the integration phase.

There are three settling conditions depending on the absolute value of V_S. The full slewing case is not considered here because it is not significant. From (3.17) and (3.18) it can be verified that V_S at end of each integration interval can be written as

$$V_S(T)=\begin{cases} a_1\cdot V_S(1-\beta) \ ; & |a_1\cdot V_S|\le V_L \\ a_1\cdot V_S(1-\dfrac{V_L}{|a_1\cdot V_S|}\beta e^{-1}e^{|a_1\cdot V_S|/V_L}) \ ; & |a_1\cdot V_S|>V_L \end{cases} \tag{3.20}$$

where $\beta=\exp(-T/2\tau_2)$

From (16), the settling error of integration phase can be expressed as:

$$\varepsilon_2(V_S)=\begin{cases} a_1 V_S\beta \ ; & |a_1 V_S|\le V_L \\ a_1\,\mathrm{sgn}(V_S)V_L\beta e^{-1}e^{|a_1V_S|/V_L} \ ; & |a_1V_S|>V_L \end{cases} \tag{3.21}$$

To analyze the effect of the nonlinear error (3.21), it is approximated by the polynomial.

$$p_i(V_S)=\alpha_1 V_S+\alpha_3 {V_S}^3+\alpha_5 {V_S}^5 \tag{3.22}$$

Then, least square method is applied and a cost function is defined to be

$$C=\int_0^{V_H}\left[\varepsilon_2(V_S)-p_i(V_S)\right]^2\times W(V_S)\,dV_S \tag{3.23}$$

$W(V_S)$ is a Gaussian weighting function. With the method above, the coefficients in (3.23) for C to be minimum can be found to be

$$\begin{bmatrix}\alpha_1\\ \alpha_3\\ \alpha_5\end{bmatrix}=\begin{bmatrix} \int_0^{V_{max}}W(V_S){V_S}^2dV_S & \int_0^{V_{max}}W(V_S){V_S}^4dV_S & \int_0^{V_{max}}W(V_S){V_S}^6dV_S \\ \int_0^{V_{max}}W(V_S){V_S}^4dV_S & \int_0^{V_{max}}W(V_S){V_S}^6dV_S & \int_0^{V_{max}}W(V_S){V_S}^8dV_S \\ \int_0^{V_{max}}W(V_S){V_S}^6dV_S & \int_0^{V_{max}}W(V_S){V_S}^8dV_S & \int_0^{V_{max}}W(V_S){V_S}^{10}dV_S \end{bmatrix}^{-1}$$

$$\times\begin{bmatrix} \int_0^{V_L}W(V_S)\beta{V_S}^2\,dV_S+\int_{V_L}^{V_H}W(V_S)V_L\beta e^{-1}e^{|V_S|/V_L}V_S\,dV_S \\ \int_0^{V_L}W(V_S)\beta\cdot{V_S}^4\,dV_S+\int_{V_L}^{V_H}W(V_S)V_L\beta e^{-1}e^{|V_S|/V_L}{V_S}^3\,dV_S \\ \int_0^{V_L}W(V_S)\beta\cdot{V_S}^6\,dV_S+\int_{V_L}^{V_H}W(V_S)V_L\beta e^{-1}e^{|V_S|/V_L}{V_S}^5\,dV_S \end{bmatrix} \tag{3.24}$$

The integrated boundary V_H or V_L in (3.24) will be changed to V_{max} if and only if V_H or V_L is large than V_{max}.

With coefficients α_1, α_3 and α_5 in (3.24) determined, the next step for calculating settling noise power is to determine the ${V_s}^3(f)$ in (3.26) and ${V_s}^5(f)$ in (3.27) by

using $V_s(f)$. The power spectral density of $v_s(n)$ is expressed as

$$h_e(f) = |Vs(f)| = \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi \cdot f}{f_s}) \right]^2 \tag{3.25}$$

$$h_{e3}(\mathrm{f}) = h_e(f) \otimes h_{e2}(f) \tag{3.26}$$

$$h_{e5}(f) = h_{e3}(f) \otimes h_{e2}(f) \tag{3.27}$$

Then the expected value of the height of PSD of settling noise of integration phase can be defined as

$$E\{h(f)\} = \alpha_1 E\{h_{e1}\} + \alpha_3 E\{h_{e3}\} + \alpha_5 E\{h_{e5}\} \tag{3.28}$$

3.5.3 Dependence with settling noise and quantization noise

The mathematical settling noise model produce by quantization noise model, so it might be calculated the quantization noise reduplicative. In (3.28), we can know that the settling noise is a linear combination of vectors h_{e1}、h_{e3} and h_{e5}. The settling noise and quantization noise signal will mixed together in (3.29), so power spectral density of each of them in (3.31) is including $S_Q(f)$、$S_S(f)$ 、$S_{SQ}(f)$ and $S_{QS}(f)$[41].

$$N_{Q+S}(t) = V_s(t) + \alpha_1 \cdot V_s(t) + \alpha_3 \cdot V_s^{\,3}(t) + \alpha_5 \cdot V_s^{\,5}(t) \tag{3.29}$$

Assume that $S_{QS}(jw)$ and $S_{SQ}(jw)$ isn't equal to zero, the total noise power in (3.30) of settling noise and quantization noise is the sum of noise in baseband.

$$\begin{aligned} S_{Q+S}(f) &= \Im\{\ \mathrm{E}[\ N_{Q+S}(\tau), N_{Q+S}(\tau + t)\ ]\ \} \\ &= S_Q(f) + S_{QS}(f) + S_{SQ}(f) + S_S(f) \end{aligned} \tag{3.30}$$

The quantization noise is $P_Q = \int_0^{f_B} S_Q(j\omega) df$, so the settling noise power is not only the settling noise $S_S(j\omega)$ in baseband, it must addition the dependent parts $S_{QS}(j\omega)$ and

$S_{SQ}(j\omega)$ in baseband in (3.31).

$$P_{\text{set}} = \int_0^{f_B} S_S(f) + S_{QS}(f) + S_{SQ}(f)\ df \tag{3.31}$$

The dependent part $S_{QS}(f)$ is equal to $S_{SQ}(f)$ complex conjugate in (3.32).

$$S_{QS}(f) = (S_{SQ}(f))^* = h_e(f) \cdot (h(f))^* \tag{3.32}$$

When quantization noise and settling noise are independent, the settling noise is $S_S(f)$.

The other noise P_{AV} (Finite OTA leakage noise)、P_{sw} (Switch thermal noise)、P_{dac} (Multi-bit DAC noise) and P_{jitter} (Jitter noise) are white gaussian noise. We assume that the noises power are independence of each other, because each of than produced by difference source and did not influenced with other noises. So the noises power P_{AV}、P_{sw}、P_{dac} and P_{jitt} could be added.

4.
Models of Sigma-Delta Modulator Power Consumption

In order to estimate the power dissipation of ΣΔ modulator, we drive the power dissipation equation of the circuit. Our goal is effective to estimate the absolute value of the power because the relative power estimate model [42] in (4.1) was a disadvantage when designer realize circuit. Typically, ΣΔ ADC power consumption is categorized into static and dynamic parts.

$$P \sim GBW \cdot C_{eq} \tag{4.1}$$

The static power is created by static current and dynamic power is created by carrier charge and discharge of capacitors. Why we add the dynamic part, but the power model in (4.1) only consider with the static part. Because when the quantizer bit number B increase, the static power will decrease and the dynamic power will increase in TABLE 4.1. So the dynamic power can't always be neglected.

B	1	2
GBW (MHz)	65	31
SR (V/us)	272.271	129.852
C_S (pF)	2	2
Static power (mW)	19.84	9.83
Dynamic power (mW)	2.14	3.31
P_{sw} (dB)	-110.414	-110.414
P_{set} (dB)	-97.8094	-97.809

TABLE 4.1 power dissipation between Static part and Dynamic part in different bit

4.1 Static Power Consumption

The static power dissipation in a ΣΔ modulator is mainly from OTA and comparator. In this section, the supply current of OTA and comparator is a constant value. But it has no use in our

optimization model. How to link up the relationship between power model and system parameters is important.

4.1.1 OTA power model

Building the power consumption model of OAT is very a complex topic, because the integrator depends on five system parameters($k_{\sum\Delta}$ 、 A_0 、 C_S 、 GBW and SR). The power consumption in (4.2) is easily to understand, but the parameter in (4.2) must be transformed into system parameter.

$$POW_{OTA} = k_{\sum\Delta} \cdot I_{OTA} \cdot V_{DD} = k_{\sum\Delta} \cdot K_{OTA} \cdot I_{BASE} \cdot V_{DD} \tag{4.2}$$

In (4.2), K_{OTA} is the total number of current branches of OTA and I_{BASE} is the OTA base current. The parameter K_{OTA} depends on the architecture of OTA. When DC gain A_0 increase, the OTA must cascade more stage in Fig. 4.1 and K_{OTA} will increased with DC gain in (4.3), because the A_0 will increased with total stage number N_{stage}.

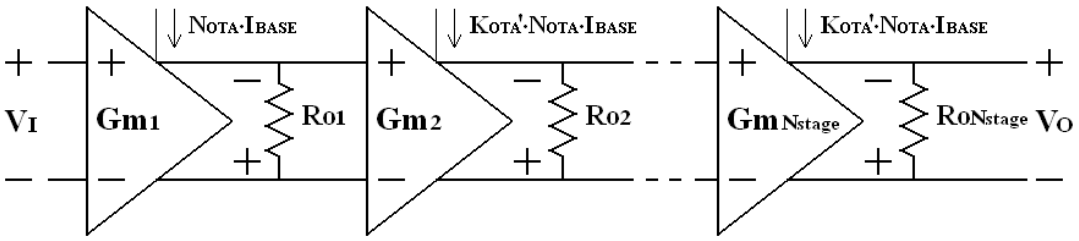


Fig. 4.1 Structure of OTA

$$K_{OTA} = N_{\mathrm{OTA}} \cdot \left(1 + \left(\mathrm{N}_{\mathrm{stage}} - 1\right) \cdot K_{OTA}'\right) \tag{4.3}$$

The parameter K_{OTA}' in Fig. 4.1 is the ratio value of current branches and N_{OTA} is the ratio between bias circuit and current mirror of OTA., suppose the currents are equal in $2 \sim N_{stage}$ stages and K_{OTA}' is less than or equal to 2, K_{OTA}' will be decided by system

parameter SR and GBW in (4.4).

$$K_{OTA}' = \frac{SR}{C_{eq} \cdot I_{BASE}} \tag{4.4}$$

If all transistor width will increase when the base current I_{BASE} increases, we suppose that the trans-conductance parameter $\mathrm{K} = 0.25 \cdot \alpha^2 \cdot \mathrm{I_{BASE}}$ then trans-conductance of each stage is $\mathrm{G_{m1}} = 2\sqrt{\mathrm{K} \cdot \mathrm{I_{BASE}}}$ and $\mathrm{G_{m2}} = \ldots = \mathrm{G_{mN}} = \alpha \cdot \mathrm{K_{OTA}} \cdot \mathrm{N_{OTA}} \cdot \mathrm{I_{BASE}}$. Then A_V can be calculated in (4.5).

$$A_V = G_{mN} \cdot R_{oN} = \frac{\alpha \cdot I}{(\lambda_p + \lambda_n) \cdot I} = \frac{\alpha}{\lambda_p + \lambda_n} \tag{4.5}$$

Assume that the DC gain A_V of each stage was the same, N_{stage} could be compute in (4.6).

$$N_{stage} = \left\lceil log_{10}(A_0) \Big/ log_{10}(A_V) \right\rceil - \xi_0 \tag{4.6}$$

Finally, we observe that I_{BASE} is a function of C_{eq} and GBW in (4.7), C_{eq} is a close loop equivalent capacitive load in (4.8).

$$I_{BASE} = \frac{2\pi \cdot C_{eq} \cdot GBW}{N_{OTA} \cdot \alpha \cdot A_V^{(N_{stage} - \xi_1)}} \tag{4.7}$$

$$\mathrm{C_{eq}} = \left(1 + \frac{\mathrm{C_L}}{\mathrm{C_I}}\right)\left(\mathrm{C_P} + \mathrm{C_S} + 2^{\mathrm{B}} \cdot \mathrm{C_u}\right) + \mathrm{C_L}$$

(4.8)

The parameters ζ_0 and ζ_1 will changed when using different amplifier in first stage or first two stages. The parameter values of ξ_0 and ξ_1 by some amplifiers in TABLE 4.2.

	ξ_0	ξ_1
Folded-Cascode amplifier	0	2
Telescope amplifier	1	1
Two-Stage amplifier	0	1

TABLE 4.2 Value of ζ_0 and ζ_1 in different amplifier

In Fig. 4.2 shows the power dissipation of the actual OTA and OTA power model with consider parasitic capacitors and without consider parasitic capacitors, the parasitic capacitors in (4.8) is $C_L = \mathrm{N}_{\mathrm{OTA}} \cdot C_L'$. In fact the parasitic capacitors could not be estimated before the OTA designed, we can only suppose the value of C_L' before designed. The actual OTA GBW is influenced by parasitic capacitors, so the GBW can't rise unlimited. The actual OTAGBW must limits by dominant pole. Fig. 4.2 shows that the differences of power between actual OTA and OTA power model with consider parasitic capacitors are not large at low frequencies.

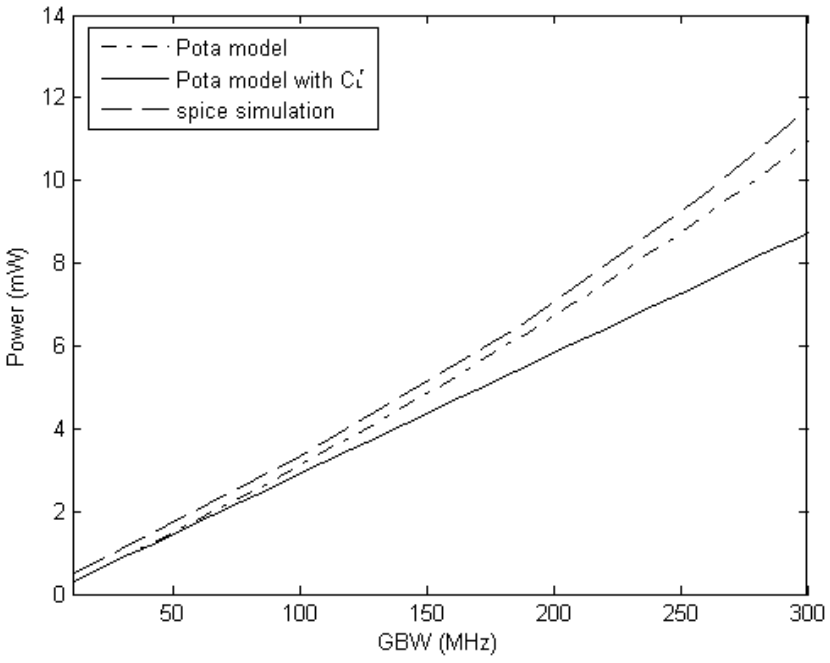


Fig. 4.2 Simulation of OTA power model

4.1.2 Comparator power model

The comparator power model shown in (4.9) is only depends on bit number, the supply current of comparator I_{comp} can not be calculated by system parameters. So it should be design a comparator before optimization simulation.

$$POW_{comp} = 2^{\mathrm{B}} \cdot I_{comp} \cdot V_{DD} \tag{4.9}$$

In (4.9), comparator power in quantizer is only a function with system parameter B, the parameter I_{comp} must decide by designer.

The first integrator is the most important in terms of noise. Hence, all succeeding integrators are normally scaled down progressively to reduce the power consumption and die area. Consider that the sum of the relative scaling factors used in all the integrators of the $\Sigma\Delta$ modulator is $k_{\Sigma\Delta}$. Then the static power consumption equals $k_{\Sigma\Delta} \cdot POW_{OTA}$, where $k_{\Sigma\Delta}$ is proportional to the order n of the $\Sigma\Delta$ modulator. From (4.2) and (4.10), the total static power consumption is:

$$\begin{aligned} POW_{static} &= POW_{OTA} + POW_{comp} \\ &= \left(k_{\Sigma\Delta} \cdot K_{OTA} \cdot I_{BASE} + 2^{B} \cdot I_{comp}\right) \cdot V_{DD} \end{aligned} \tag{4.10}$$

Since the static power consumption relates to $k_{\Sigma\Delta}$、B、A_V、C_{eq}、SR and GBW they are important system parameters t determined in the design flow.

4.2 Dynamic Power Consumption

In this section, we discuss dynamic power consumption. Dynamic power includes switch power、DAC power and digital power. All of them depend on dynamic signal $\mathrm{f_s} = 2 \cdot \mathrm{f_B} \cdot \mathrm{OSR}$ and capacitor of each other.

4.2.1 Switch power model

The CMOS switch is shown in Fig. 4.3, assume that the number of CMOS transmission gate in Sigma-Delta Modulator is N_{Switch}. The PWO_{Sw} in (4.11) is the total power dissipation of switch circuits.

$$POW_{SW} = N_{Switch} \cdot C_{Switch} \cdot f_s \cdot V_{DD}^{\ 2} \tag{4.11}$$

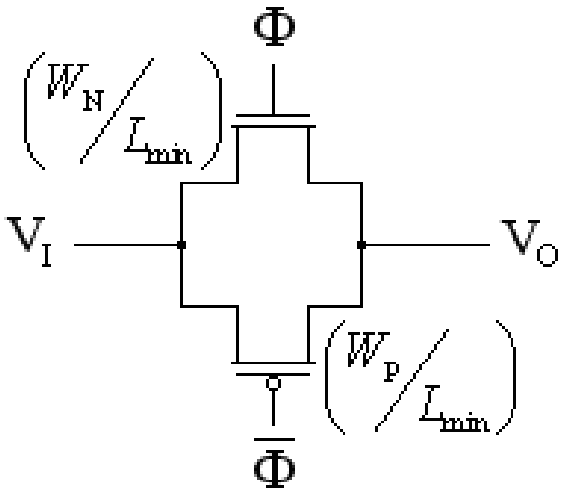


Fig. 4.3 CMOS transmission gate

When the switches turn on or turn off, it must charge and discharge carriers to the gate of CMOS switch. Those carriers loss accumulate a huge power dissipation of sigma-delta. So it must be estimated in our power model. It is easily to calculate capacitor C_{Switch} of each switch gate in (4.12).

$$\begin{aligned} C_{Switch} &= C_{NMOS} + C_{PMOS} \\ &= L_{\min} \cdot (W_P + W_N) \cdot C_{OX} \end{aligned} \tag{4.12}$$

But our power must link the relationship system parameters and power dissipation, unfortunately C_{Switch} is not the system parameter, it has no use in optimization model. But it can be transform to system parameter R_{Switch} in (4.13) (4.14) (4.15).

$$R_N = \frac{1}{\mu_n \cdot C_{OX} \cdot \left(W_N / L_{min}\right) \cdot \left(V_{DD}/2 - V_I - V_{tn}\right)} \tag{4.13}$$

$$R_P = \frac{1}{\mu_p \cdot C_{OX} \cdot \left(W_P / L_{min}\right) \cdot \left(V_{DD}/2 - V_I - |V_{tp}|\right)} \tag{4.14}$$

Suppose $\mu_p \cdot W_P = \mu_n \cdot W_N$, PMOS the resister R_P could be calculated in (4.13), the resistor of CMOS transmission gate is the parallel resistance with R_P and R_P.

$$\begin{aligned} R_{Switch} &= \frac{1}{\mu_n \cdot C_{OX} \cdot \left(W_N / L_{min}\right)\left(V_{DD} - V_{tn} - |V_{tp}|\right)} = \frac{L_{min}^{\ 2}}{\mu_n \cdot C_{NMOS} \cdot \left(V_{DD} - V_{tn} - |V_{tp}|\right)} \\ &= \frac{L_{min}^{\ 2}}{\mu_n \cdot C_{NMOS} \cdot \left(V_{DD} - V_{tn} - |V_{tp}|\right)} = \frac{\left(\mu_n^{\ -1} + \mu_p^{\ -1}\right) \cdot L_{min}^{\ 2}}{C_{Switch} \cdot \left(V_{DD} - V_{tn} - |V_{tp}|\right)} \end{aligned} \tag{4.15}$$

Form (4.11) the total capacitor $C_{Switch} = \left(1 + \mu_p / \mu_n\right) \cdot C_{NMOS}$. The value of C_{Switch} is inversely proportional to the switch-on resistance R_{Switch} [43] in (4.16).

$$C_{Switch} = \frac{\left(\mu_n^{\ -1} + \mu_p^{\ -1}\right) \cdot L_{min}^{\ 2}}{R_{Switch} \cdot \left(V_{DD} - V_{tn} - |V_{tp}|\right)} \tag{4.16}$$

Parameter $N_{Switch} = 8 \cdot k_{\Sigma\Delta} \cdot 2^B$ is the number of total switches, so we define the relative switch power as

$$\begin{aligned} POW_{SW} &= N_{Switch} \cdot C_{Switch} \cdot f_s \cdot V_{DD}^{\ 2} \\ &= 2 \cdot N_{Switch} \cdot \frac{\left(\mu_n^{\ -1} + \mu_n^{\ -1}\right) \cdot L_{min}^{\ 2}}{\left(V_{DD} - V_{tn} - |V_{tp}|\right) \cdot R_{Switch}} \cdot V_{DD}^{\ 2} \cdot f_B \cdot OSR \end{aligned} \tag{4.17}$$

4.2.2 DAC power model

DAC power is the total carrier loss in feedback loops, the unit feedback capacitor C_u will be charged in sampling phase and those carriers on C_u will be discharged in integration phase.

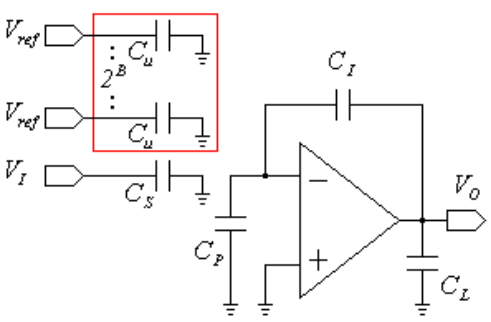


Fig. 4.4 Sampling phase

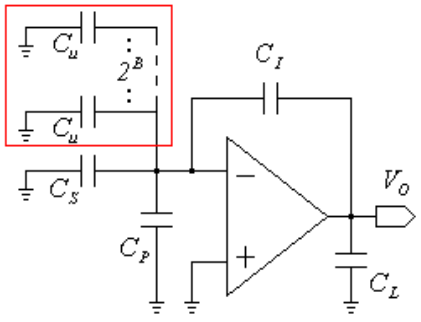


Fig. 4.5 Integration phase

We estimate the power consumption of multi-bit DAC in the multi-bit sigma-delta converter. The multi-bit DAC is shown in Fig. 4.4 and Fig. 4.5. It is composed of switches and unit feedback capacitors. At first, we consider charge and discharge for a unit feedback capacitor in sampling phase and integration phase. Assume that the periods of charge and discharge both are $T/2$, the average current I_u of unit feedback capacitor and power consumption P_u of a unit capacitor in (4.18)(4.19).

$$I_u = C_u \, dV_u / dt \tag{4.18}$$

$$\begin{aligned} P_u &= \frac{1}{T}\int_0^{T/2} V_{ref} \cdot I_u dt - \frac{1}{T}\int_{T/2}^{T} V_{ref} \cdot I_u dt \\ &= \frac{1}{T}\int_0^{T/2} V_u \cdot C_u \cdot \left(dV_u / dt \right) dt - \frac{1}{T}\int_{T/2}^{T} V_u \cdot C_u \cdot \left(dV_u / dt \right) dt \\ &= \frac{1}{T}\int_0^{V_{ref}} V_u \cdot C_u dV_u - \frac{1}{T}\int_{V_{ref}}^{0} V_u \cdot C_u dV_u \\ &= \frac{1}{T} C_u \cdot {V_{ref}}^2 = f_S \cdot C_u \cdot {V_{ref}}^2 \end{aligned} \tag{4.19}$$

The power dissipation of total feedback carriers in is $POW_{DAC} = N_{DAC} \cdot P_u$. It's a function of full scale $FS = V_{ref}/2$ and N_{DAC} what is the number of total unit feedback capacitor $C_u = C_S / 2^B$ in (4.20). The parameter N_{DAC} in signal ended sigma-delta modulator

is $k_{\Sigma\Delta} \cdot 2^B$, but our model is fully differential sigma-delta modulator, the value of N_{DAC} must be double $N_{DAC} = 2 \cdot k_{\Sigma\Delta} \cdot 2^B$. The DAC Power is not depends on B, because $N_{DAC} \cdot C_u = 2 \cdot k_{\Sigma\Delta} \cdot C_S$ in (4.19).

$$POW_{DAC} = \frac{1}{4} N_{DAC} \cdot C_u \cdot FS^2 \cdot f_S$$

$$= k_{\Sigma\Delta} \cdot C_S \cdot FS^2 \cdot f_B \cdot OSR \tag{4.20}$$

4.2.3 Digital power model

Digital power in (4.21) is including clock generator circuit power, dynamic element matching circuit power and the logic circuit power in quantizer. In this paper, we use CMOS logic to design the logic circuit. Parameter N_{gate} is total number of logic gate when the quantizer is only 1 bit and the parasitic capacitor C_{gate} is the average capacitor of total logic gates. In this section the parasitic capacitors could not be transfer to system parameters. So the digital circuit must design before optimization simulation.

Considering a CMOS inverter with the load capacitor C_{gate} are shown in Fig. 4.6, the capacitor C_{gate} namely the channel capacitor in MOSFET. The length to width ratio of M_P and M_N is (W_P/L_{min}) and (W_N/L_{min}), we can calculate channel capacitor C_{PMOS} in (4.21) and C_{NMOS} in (4.22).

$$C_{PMOS} = W_P \cdot L_{min} \cdot C_{OX} \tag{4.21}$$

$$C_{NMOS} = W_N \cdot L_{min} \cdot C_{OX} \tag{4.22}$$

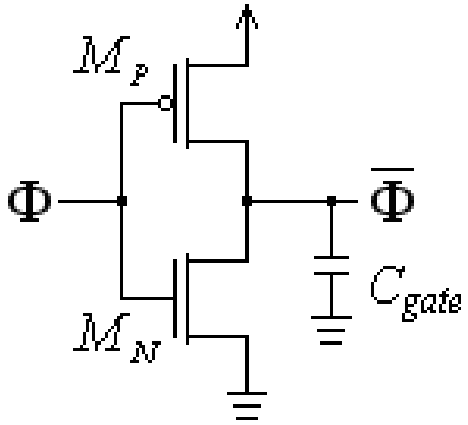


Fig. 4.6 CMOS logic inverter

Giving a periodic square-wave Φ to inverter input node. When Φ changed from high level voltage to low level voltage at $t = 0$, the C_{PMOS} charge and C_{NMOS} discharge. The total carrier $Q_{H\to L}$ in (4.23)

$$Q_{H\to L} = V_{DD} \cdot (C_{PMOS} + C_{NMOS}) \tag{4.23}$$

In reverse case Φ changed from low level voltage to high level voltage at $t = T/2$, the C_{PMOS} discharge and C_{NMOS} charge. The power dissipation $Q_{L\to H}$ in (4.24)

$$Q_{L\to H} = V_{DD} \cdot (C_{PMOS} + C_{NMOS}) \tag{4.24}$$

The average current I_{avg} in 1 clock cycle of this inverter could be calculated in (4.25), we can find the power dissipation of this inverter in (4.26).

$$\begin{aligned} I_{avg} &= \frac{1}{T} \cdot (Q_{H\to L} + Q_{L\to H}) \\ &= \frac{2}{T} \cdot V_{DD} \cdot (C_{PMOS} + C_{NMOS}) \end{aligned} \tag{4.25}$$

$$P_{INV} = I_{avg} \cdot V_{DD} = 2 \cdot (C_{PMOS} + C_{NMOS}) \cdot f_S \cdot V_{DD}^{\ 2} \tag{4.26}$$

From (4.26), the load capacitor $C_{gate} = 2 \cdot (C_{PMOS} + C_{NMOS})$, assumed that C_{gate} is the average of each logic gate capacitor and C_{gate} of all logic gates are the same, the digital circuit power could be calculated in (4.21)

$$POW_{digital} = 2^{B} \cdot N_{gate} \cdot C_{gate} \cdot V_{DD}{}^{2} \cdot 2 \cdot f_B \cdot OSR \tag{4.21}$$

In TABLE 4.3 is the relationship between total power models and system parameters, when the power depend on less parameter like POW_{comp} and $POW_{digital}$. So those power models both needed to design circuit to get the parameters N_{gate} 、 C_{gate} and I_{comp} before optimization.

	POW_{OTA}	POW_{comp}	POW_{SW}	POW_{DAC}	$POW_{digital}$
OSR	-	-	↑	↑	↑
f_B	-	-	↑	↑	↑
C_S	↑	-	-	↑	-
R_{Switch}	-	-	↑	-	-
B	-	↑	↑	-	↑
GBW	↑	-	-	-	-
SR	↑	-	-	-	-
A_0	↑	-	-	-	-
$k_{\Sigma\Delta}$	↑	-	↑	↑	-
FS	-	-	-	↑	-

TABLE 4.3 Relationship between power models and system parameters

5.
Design Optimization of Sigma-Delta ADCs Design

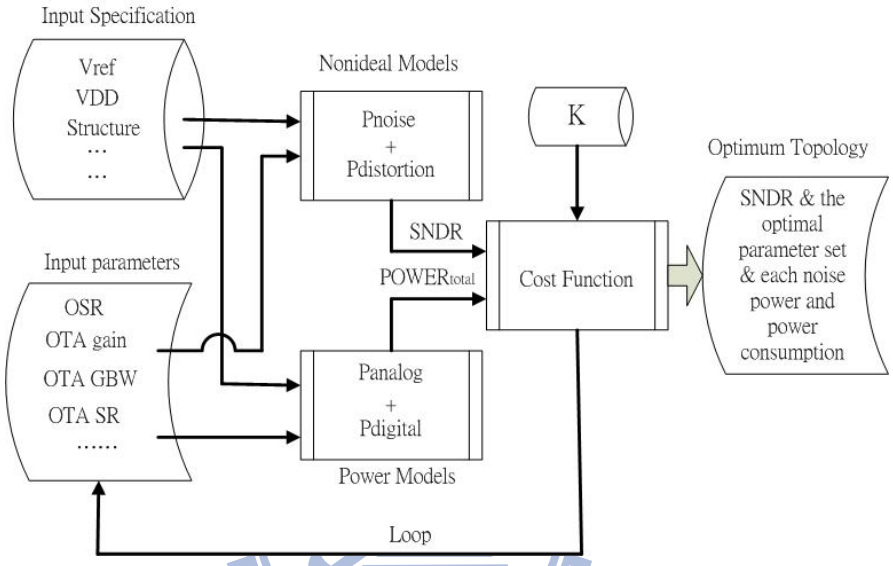


Fig. 5.1 Flow of the proposed optimization for the ΣΔ modulator Model-based design

In section VI, we propose a design optimization flow to help designers reach an optimal design quickly as Fig. 5.1. The input signal bandwidth (Hz) and the output signal *SNDR* (dB) are treated as design specifications. We modify the figure-of-merit (FOM) [44] function by multiplying a variable K to the SNDR term of FOM and inverse it, to become our Cost Function. In Fig. 1 the Cost Function is expressed by

$$CF = \left(K \cdot SNDR_{dB} + 10\log\left(\frac{f_B}{POWER_{total}} \right) \right)^{-1} \tag{5.1}$$

$SNDR$ is defined as (5.1). Where P_{total_noise} and $P_{total\_distortion}$ are sum of all major noises and distortions in SDM listed in TABLE I.

P_Q	Quantization noise
P_{AV}	Finite OTA leakage noise
P_{jitt}	Jitter noise
P_{set}	Settling noise
P_{sw}	Switch thermal noise
P_{OTA}	OTA thermal noise
P_{dac}	Multi-bit DAC noise
$HD3_{NFDCG}$	third harmonic distortion of Nonlinear Finite-DC-Gain
$HD5_{NFDCG}$	fifth harmonic distortion of Nonlinear Finite-DC-Gain
$HD2_{DAC}$	second harmonic distortion of of Nonlinear Capacitance
$HD3_{DAC}$	third harmonic distortion of of Nonlinear Capacitance
$HD4_{DAC}$	fourth harmonic distortion of of Nonlinear Capacitance

TABLE 5.2 The representation of each noise in our models

The constant *K* serves as the relative weighting between SNDR and $POWER_{total}$. Typically, if we prefer high resolution designs, we set K higher and SNDR plays a more important role than $POWER_{total}$. On the other hand, if we prefer low power designs, we can set K lower. parameters of σ_{cap}, V_{ref} and some circuit device dimensions parameter (ex: μ_n, C_{ox}, etc) depend on the technology, so they are set before the design optimization.

6.
Conclusions and Future Works

In order to increase the speed and low power of circuit design for ΣΔ ADCs, this paper offers an efficient optimization method. The power estimation is presented for sigma-delta converter with a certain accuracy and bandwidth specification. The power consumptions model offers designer to find the dominant power dissipation part and how to reduce it.. Our proposed method has acceptable accuracy and nice speed, and the flexibility can be enhanced by building more nonlinearity models for different circuit structures.

Further, in order to estimation the noises power, it must consider the noise power dependency issue. In this paper only consider the dependency problem between setting noise and quantization noise. The power has a slight disadvantage that the digital power and comparator power must design before optimization.

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