國立交通大學

電控工程研究所

碩士論文

模組化非線性運算放大器增益所產生之

諧波失真與模組設計最佳化運用在積分

三角類比數位轉換器

Modeling Harmonic Distortions Caused by Nonlinear Op-Amp DC-Gain and Model-based Design Optimization for Sigma-Delta Modulators

研 究 生：謝智隆

指導教授：陳福川　教授

中 華 民 國 九 十 八 年 九 月

模組化非線性運算放大器增益所產生之諧波失真與

模組最佳化在離散時間積分三角類比數位轉換器

Modeling Harmonic Distortions Caused by Nonlinear Op-Amp DC-Gain and Model-based Design Optimization for Sigma-Delta Modulators

研 究 生：謝智隆　　Student：Chih-Lung Hsieh

指導教授：陳福川　　Advisor：Fu-Chuang Chen

國 立 交 通 大 學

電 控 工 程 研 究 所

碩 士 論 文

A Thesis

Submitted to Department of Electrical and Control Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electrical and Control Engineering

September 2009

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 八 年 九 月

模組化非線性運算放大器增益所產生之諧波失真與模組最佳化在離散時間積分三角類比數位轉換器

研究生：謝智隆　　指導教授：陳福川 教授

國立交通大學

電控工程研究所

摘要

傳統的積分三角類比數位轉換器電路規格設計是一個相當耗時的工作，且需要不斷的嘗試各種電路規格，以達到所需要的解析度。本篇論文分析了各種不同架構的積分三角類比數位轉換器之主要雜訊來源與非線性特性所造成的失真問題。藉由分析推導出的失真功率模型、雜訊功率模型及絕對功率消耗模型，並以訊號對雜訊和失真比(SNDR)來當作我們的設計規格，以做最佳化的設計。此最佳化設計意指在特定系統規格下(如頻寬、訊號對雜訊和失真比)，找到一組最佳化的設計參數，使得類比數位轉換器的功率消耗最小以及訊號對雜訊和失真比最大，並節省龐大制定電路規格的時間成本。最後我們將針對已發表的設計結果來做驗證的工作。雖然現今已存在相當多行為模擬工具以自動化制定電路規格，但較之下，本論文所提出的最佳化方法將快上許多。

Modeling Harmonic Distortions Caused by Nonlinear Op-Amp DC-Gain and Model-based Design Optimization for Sigma-Delta Modulators

Student：Chih-Lung Hsieh　　Advisor：Dr. Fu-Chuang Chen

Institute of Electrical and Control Engineering

Nation Chiao Tung University

ABSTRACT

The conventional sigma-delta ADC design approach is a time consuming process and needs much trials and errors. This paper analyze the mainly noise sources and nonlinear distortions. Utilizing the noise power models, nonlinear distortion power models and accurate power consumption models derived in this paper, and the assigned signal to noise and distortion ratio (SNDR) to be the design goal, we can forward to do design optimization under the specific specifications. Design optimization means that under the specific specifications (signal bandwidth, SNDR), we find a set of optimal design parameters such that the power consumption of ADCs is minimum and SNDR is maximum, and reduce the huge time-cost to set up the circuit specifications. Finally, design optimization is tested against a published design result. Although design automation issues have been partially addressed by recent behavior- simulation–based methods, yet such methods can be slower than our analytical approach far.

誌謝 Acknowledgment

我要將此論文獻給

我親愛的母親-江麗金 女士

最疼我的父親-謝朝榮 先生

若沒有他們，我不可能有機會完成此篇論文，並且從交通大學碩士班畢業。此外，必須感謝指導教授陳福川博士兩年來嚴格的督促與指導，讓我學會做研究的方法與心態。另外，也要感謝口試委員林清安教授、洪浩喬教授與陳科宏教授對本篇論文所給予的建議與指導。

還要感謝實驗室文佑學長在我一年級時幫我打好深厚的研究基礎。感謝實驗室同瑞祺、武璋和學弟子恩、嘉昌陪我度過最後的學生生涯，並在研究上給予我很多幫助。感謝學弟們，謝謝你們在這兩年間帶給我的鼓勵和歡樂，我以後會很懷念晚上打棒球的日子。最後要謝謝這兩年在新竹唸書期間所有幫助過我的人，雖然無法一一列舉，但在這邊向大家致上最大的謝意。

Contents

Lists of Tables

Lists of Figures

List of Symbols

Symbols

VLSB	Quantizer step size
V_{OS}	Maximum output swing of op-amp
OSR	OverSampling Ratio
n	Order of the Sigma-Delta modulator
B	Number of bits in the quantizer
f_S	Sampling Frequency
f_B	Signal Bandwidth
V_{ref}	Reference Voltage of the quantizer
A_0	Finite Gain of OTA
f_{in}	Frequency of the input signal
A_{in}	Amplitude of input signal
$\sigma_{jit.}$	standard deviation of clock jitter
C_S	Sampling capacitor
C_I	Integrating capacitor
C_L	Load capacitor of OTA
C_{OX}	The capacitance per unit area of the gate oxide
V_S	Input signal plus feedback DAC signal
a_i	gain coefficient of i th integrator
R_{Switch}	Switch ON resistance
N	quantizer levels
gm1	Amplifier transconductance
$\sigma_{cap.}$	Mismatch of unit capacitance
k	Boltzmann's constant (1.38×10^{-23}) J/K

1
Introduction

1.1 Current Status and Background

Sigma-Delta A/D converters have become popular for high-resolution medium-to-low-speed applications such as digital audio [1][2], voice codec, and DSP chip. Recently, ΣΔ ADCs have been applied to higher bandwidth signals, and low power designs are frequently emphasized. For example, in ×DSL [3][4] applications, signals up to several MHz must be handled. Since significantly increasing the sampling rate is difficult, designers either seek to increase the order or the cascade stages [5][6], or employ multi-bit quantization [7][8], or both, in order to achieve the required dynamic range. DAC linearity can be improved due to process technology advances, making the multi-bit architecture more popular. The ΣΔ modulator design is a complex and time consuming process because many coupled design parameters must be determined. Coming up with an acceptable design is very difficult with increasing design specification demands, previously described. Even an acceptable design may not be the best one. We propose an optimization approach to increase automation and reduce complexity in the ΣΔ ADCs design.

1.2 Motivation and Aims

To propose the design optimization for many structures of ΣΔ modulators, we need a complete set of important nonideality models and the power consumption model. Some issues concerning ΣΔ modulator noise and error modeling appeared in [1][2][9]. The performance of the ΣΔ ADCs is usually expressed in terms of SNR and SNDR. Circuit designers must take into consideration the nonidealities and decide the circuit and system parameters to meet the desired specifications. A design optimization procedure is proposed

in [10] to meet design specifications while minimizing power consumption. However, it didn't consider the nonlinear distortions, so that the effectiveness of the proposed design optimization is limited. In this work, we discuss all the important nonlinear distortions, and incorporate relevant distortion powers into the optimization process in order to achieve more realistic designs.

In a ΣΔ modulator, common causes for harmonic distortions are nonlinear finite-OTA-gain, settling error, nonlinear capacitances, quantizer nonlinearity, nonlinear switch resistance and unit-DAC mismatch. Operational amplifiers (op-amps) are the critical part of the ΣΔ modulators and its nonidealities such as nonlinear finite-OTA-gain may produce distortions significantly.

The nonlinear finite-OTA-gain distortion is caused by the gain variation of op-amp. Currently, there are two major approaches for selecting op-amp DC-gains. The first approach is *ad hoc* based [11-13], which usually suggests setting DC-gain at a sufficiently large value, e.g. 70 dB, so that nonlinear distortion can be small enough. This can be too conservative, since the DC-gain can actually be smaller for certain applications. The other approach for selecting op-amp DC-gain requires intensive simulations and subsequent computations [9][14-15]. In this approach, time-consuming Spice simulation is first used to identify the nonlinear DC-gain curve of a specific op-amp design, and then magnitude of distortion is computed from the nonlinear curve identified. If the computed distortion is too large or too conservative (too small), the op-amp design has to be modified so that DC-gain can be adjusted. Then, one needs to carry out the aforementioned simulation and computation again. This iterative process would continue until a suitable DC-gain is determined. So the existing approaches are either not accurate enough or not time-efficient.

In this paper we propose an accurate and efficient approach for selecting op-amp DC-gain. An essential first step in our method is the creation of a general model for nonlinear op-amp DC-gain curves. The importance of this nonlinear DC-gain model is that it eliminates the

need for time-consuming Spice simulations described above. Then, the nonlinear DC-gain curve model can be employed to analytically derive the nonlinear distortion which appears at SDM output. Since the nonlinear distortion model is expressed in terms of DC-gain and other SDM parameters, it can be used to accurately compute the minimum required op-amp DC-gain such that the nonlinear distortion is kept under a tolerable value. The nonlinear DC-gain curve model and the nonlinear distortion model are verified by transistor level simulations. Their application to sigma-delta modulators is verified by behavior simulations.

Currently, the major approaches about SDM high-level optimization used MATLAB Simulink and related power models by simulated annealing or generic algorithm [16-17] to find a best parameters combination. Although they used different algorithm to reduce the searching time, it still spent much time in behavior simulation. In existing approaches, the optimization result can't indicate each noise power and the power consumption of each device (ex: op-amp, switch, decoder, etc), so designer is hard to analyze and correct the system. Differing with these approaches employ behavioral simulators to explore the design space, in order to find out the best combination of ΣΔ ADC architecture and circuit parameters. We proposed an optimization design for ΣΔ ADC based on analytic all typical architecture noise and power consumption with general math models. So that our model can list all noise power and each device power consumptions after each optimization. Designer can obtain the parameter they want and know how to correct the result. More importantly, our analytical models don't have behavior simulation, so our optimization time is not dependent on system cycles, but relate to CPU clock. It will make faster than other optimization design.

In this paper, we propose an optimization algorithm based on analytical models of noises, nonlinear distortions, and power consumptions. This algorithm searches the parameter space for a design parameter combination which meets signal to noise plus distortion ratio (SNDR)

requirement while minimizing power consumption. Main purposes of this paper are to propose a complete and general set of noise, nonlinear distortion and power models on all typical architecture.

1.3 Organization

This work is organized as follows. In Chapter 2 and Chapter 3, systematic studies of fundamental theory and various architectures of ΣΔ modulator are presented first. In Chapter 4, we discuss about different architecture of non-idealities noise and distortion models of SDM. In Chapter 5, we create of a general model for nonlinear op-amp DC-gain curves. In Chapter 6, we can be employed to analytically derive the nonlinear distortion which appears at SDM output by nonlinear DC-gain curve model and we use behaving and transistor level simulation to verify our model. We discuss the design optimization between MODEL-BASED and SIMULATION-BASED in Chapter 7. A design optimization scheme is proposed in Chapter 8. It essentially combines system and circuit level designs, and optimizes all design parameters at the same time. The optimization scheme is verified in Chapter 9, and various issues are discussed. Conclusions and future works are presented in Chapter 10.

2
Fundamental Theorems of Sigma-Delta Modulators

Before we establish the error models of ΣΔ modulators, several important theorems and concepts must be known, such as Nyquist sampling theorem, quantization error and the two most critical techniques in a ΣΔ modulator: oversampling and noise shaping. All topologies of ΣΔ modulators are based on these two techniques. There also have some parameters we must to understand, such as OSR, SNR, and SNDR …etc. This chapter starts from fundamental theorems, and introduces several topologies of ΣΔ modulators.

We will illustrate quantization error and analyze quantization noise in an ideal A/D converter and then derives the peak signal-to-noise ratio. The resolution of an A/D converter is determined by signal-to-noise ratio, which is a very important specification in an A/D converter.

2.1 Nyquist Sampling Theorem

In an analog-to-digital converter, the analog signal from external environment must be converted to discrete-time signal by sampling. However, the sampling rate (f_S) and signal bandwidth (f_B) must follow the Nyquist sampling theorem in (2.1):

$$f_S \geqq 2f_B \qquad (2.1)$$

The sampling rate must be higher or equal to twice of signal bandwidth in order to prevent from aliasing. We will illustrate the phenomenon of aliasing by Fig. 2.1. Fig. 2.1(a) and (b) are the spectrums of signal and sample function respectively; from fig. 2.1(c), when sampling rate is twice higher than signal bandwidth, the signal after sampling has no aliasing and it can be perfectly reconstructed by using low pass filters. However, in Fig.

2.1(d), when the sampling rate is lower than twice of signal bandwidth, aliasing will appear in the signal after sampling. The signal having aliasing is difficult to reconstruct to original signal, like Fig. 2.1(e).

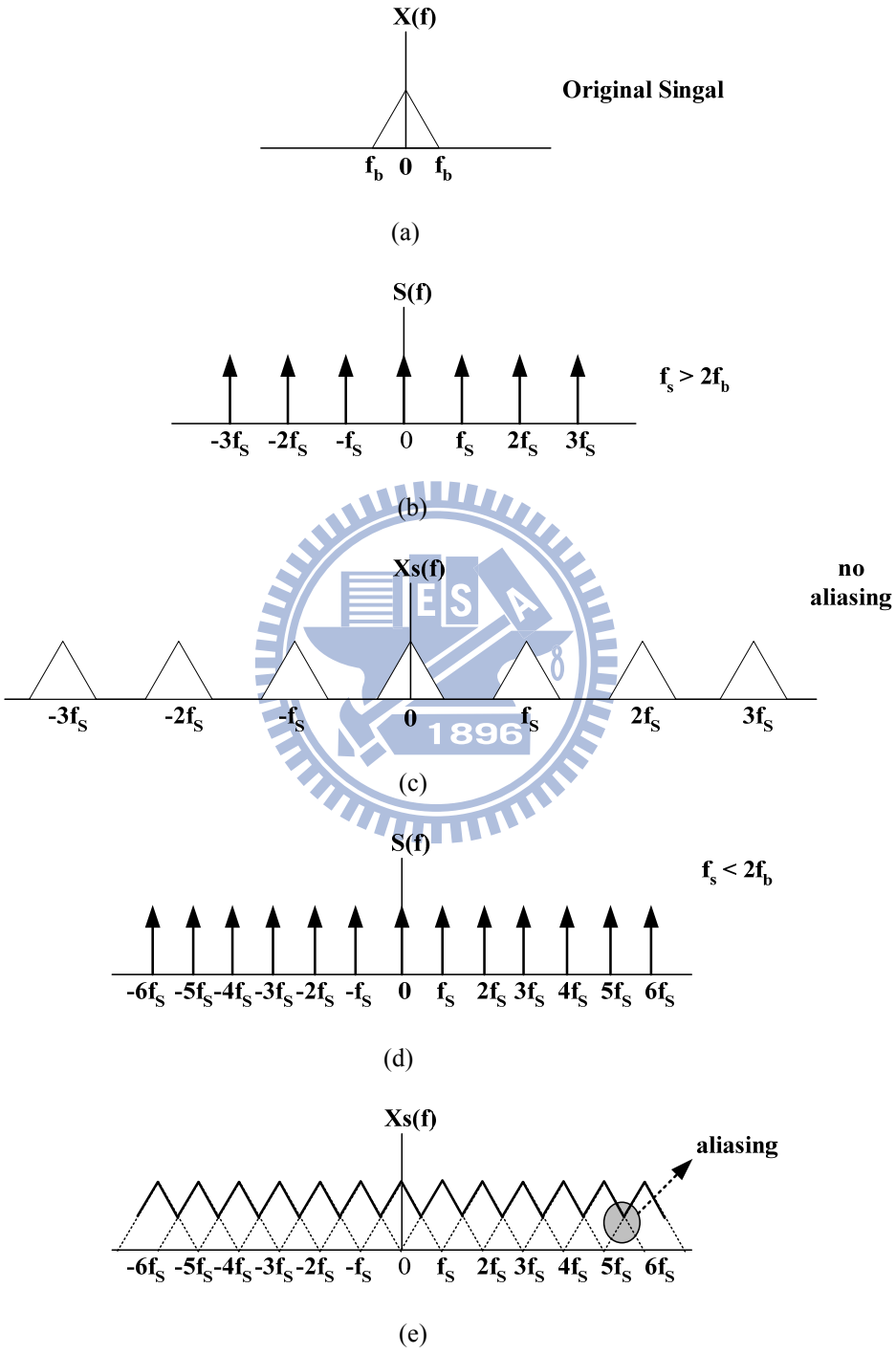


Fig. 2.1 (a) Original signal spectrum (b) Sample function when fs > 2fB (c) Signal spectrum that' sampled by (b) (d) Sample function when fs < 2fB (e) Signal spectrum that sampled by (d)

2.2 Quantization noise and Peak SNR

We can get a discrete-time signal by sampling a continuous-time signal, and this sampled signal can be converted to digital signal. Quantization will appear in this process, the basic concept of quantization is to classify the original signal to different levels according to its level to determine the bit number of this signal, as shown in Fig. 2.2.

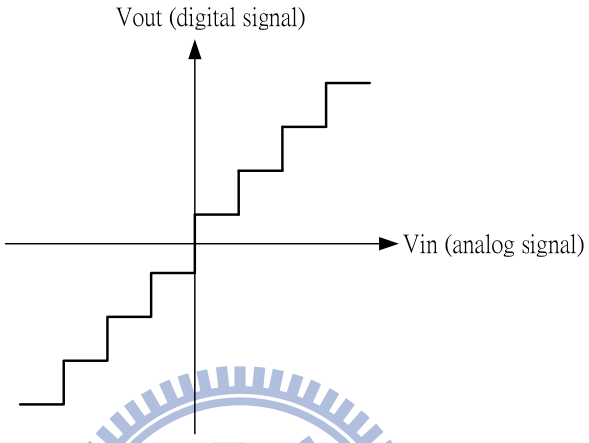
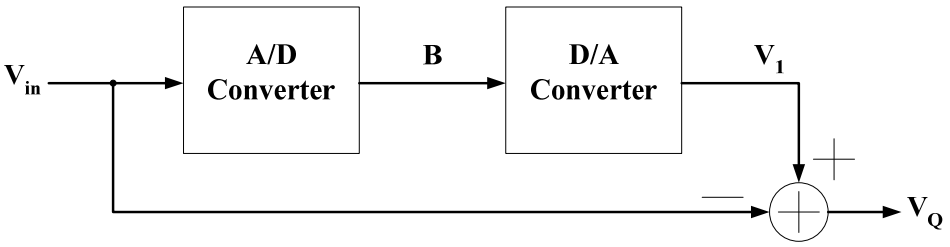


Fig. 2.2 Quantization process

It will have quantization error even in an ideal analog-to-digital converter. As shown in Fig .2.3, we convert the digital signal B to analog signal V_1 by a D/A converter, and then the signal V_1 is subtracted by input signal Vin. The result is the quantization error V_Q, as in (2.2) [18].

$$V_Q = V_{in} - V_1 \qquad (2.2)$$



Quantization noise $V_Q = V_{in} - V_1$

Fig. 2.3 Quantization error caused by A/D converter

The range of quantization error is limited in $\pm V_{LSB}/2$ (as in Fig. 2.4), and we assume the

probability density function of quantization error is uniformly distributed between $\pm V_{LSB}/2$ and its mean is zero, as shown in Fig. 2.5. From this assumption, we can easily get the quantization noise power $V_{Q(rms)}^2$ in (2.3).

$$V_{Q(rms)}^2 = \int_{-\infty}^{\infty} x^2 \cdot f_Q(x) \cdot dx = \frac{1}{V_{LSB}} \int_{-VLSB/2}^{VLSB/2} x^2 \cdot dx = \frac{V_{LSB}^2}{12} \quad (2.3)$$

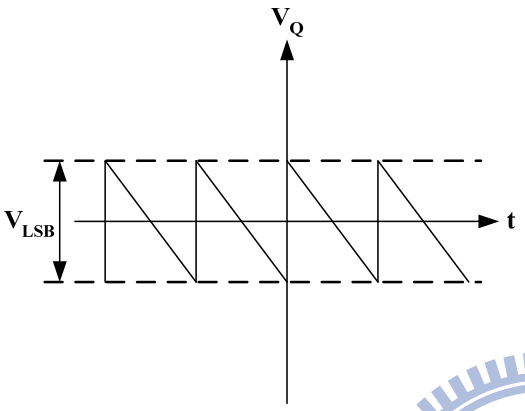


Fig. 2.4 Quantization error range

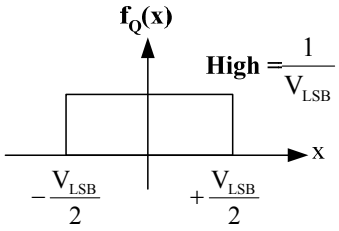


Fig. 2.5 P.D.F of quantization error

From (2.3) we can know the quantization noise power is proportional to square of V_{LSB}, and V_{LSB} can be represented as in (2.4). Therefore, we can say that the quatization noise will reduce by increasing quantization bit number.

$$V_{LSB} = \frac{FS}{2^B} \quad (2.4)$$

FS=Full scale = $V_{ref+} - V_{ref-}$　　B：Quantization bit number

Assume that input signal is sinusoidal, expressed as $V_{in}(t) = A \sin\omega t$, so the input signal power $V_{in(rms)}^2$ is as （2.5）. In （2.5）, we define the amplitude of input signal is the full scale of reference voltage, and from (2.3), (2.4) and (2.5), the peak SNR(Peak Signal-to-Noise Ratio) can be derived as in (2.6).

$$V_{in(rms)}^2 = \frac{1}{T} \int_{-T/2}^{T/2} (A \cdot \sin \omega t)^2 \cdot dt = \frac{A^2}{2} = \frac{(2A)^2}{8} = \frac{FS^2}{8} \quad (2.5)$$

$$PSNR = 10 \log \left(\frac{V_{in(rms)}^2}{V_{Q(rms)}^2} \right) = 6.02B + 1.76 \text{ dB} \quad (2.6)$$

(2.6) is the result obtained by Nyquist sampling rate. From (2.6), we can know that each

additional bit number in quantizer increases 6dB in SNR. In Nyquist A/D converters, increasing the resolution of quantizer (decrease V_{LSB}) while reducing the quantization noise is a general method to reach higher SNR, but this method is sensitive to mismatches of analog device. Therefore, the general Nyquist A/D converter is not easily to implement with high resolution.

2.3 Techniques of Sigma-Delta Modulator

ΣΔ A/D converters are based on oversampling and noise shaping to reach high resolution. Oversampling means the sampling rate is much higher than Nyquist rate, about 8~512 times in general applications. The goal of oversampling is to expand quantization noise to wider range. It can reduce the quantization noise in signal bandwidth and increase the DR (Dynamic range) of input signal. Noise shaping is a technique that moves noise to high frequency, which is done by using discrete time filter and feedback technique. After noise shaping, the noise in high frequency can be filtered out by a digital filter [19].

2.3.1 Oversampling Technique

First, we made the assumption that quantization noise is a uniform distribution in sampling spectrum so its mean is zero and is a white noise [20]. The system in Fig. 2.6 just has oversampling function and does not have noise shaping effect. If a A/D converter is sampled in Nyquist rate, then the quantization noise is uniform distributed between $\pm f_B$; if it is sampled by oversampling technique, then quantization noise is uniform distributed between$\pm f_{S2}/2_s$, which is much larger than f_B. As shown in Fig. 2.7, if the signal bandwidth is between $\pm f_B$, then quantization noise in this bandwidth will be reduced by using oversampling technique, which will raise PSNR significantly.

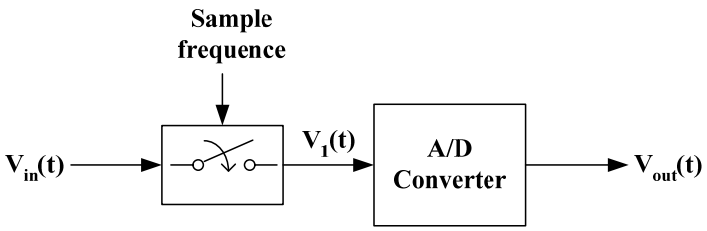


Fig. 2.6 Sampling system

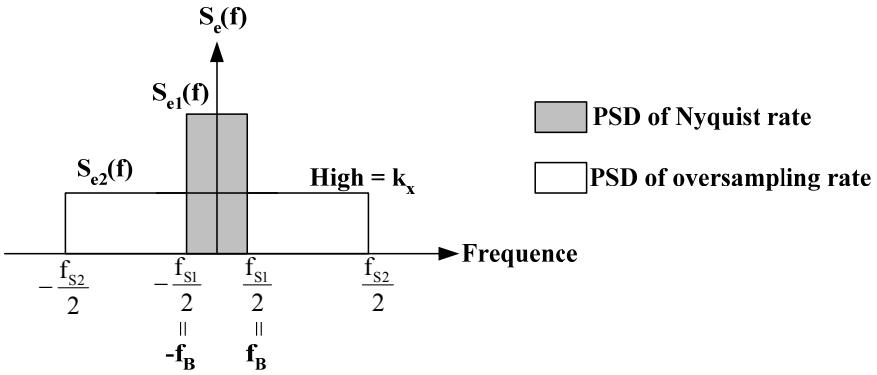


Fig. 2.7 Noise distribution after sampling

In the condition of oversampling, the PSD (Power Spectrum Density) of quantization noise is as $S_{e2}(f)$ in Fig. 2.7 and can be represented as:

$$k_x^2 = \frac{V_{LSB}^2}{12 \cdot f_s} = S_{e2}^2(f) \qquad (2.7)$$

From (2.7) we can estimate the quantization noise in $2f_B$ after oversampling

$$P_Q = \int_{-f_B}^{f_B} k_x^2 \cdot df = \frac{2f_B}{f_s} \cdot \frac{V_{LSB}^2}{12} = \frac{FS^2}{12 \cdot 2^{2B} \cdot OSR} \qquad (2.8)$$

In (2.8), we define a parameter OSR (Oversampling Ratio) as

$$OSR = \frac{f_s}{2f_B} \qquad (2.9)$$

Finally, we can get PSNR from (2.5) and (2.8)

$$PSNR = 10 \log\left(\frac{P_{signal}}{P_Q}\right) = 6.02B + 1.76 + 10 \log(OSR) \qquad (2.10)$$

From (2.10), we can find that doubling OSR will increase 3dB in PSNR, which is about 0.5 bit increase in resolution. Although oversampling can reduce quantization noise, it is

difficult to reach high SNR when using a low bit quantizer. For example, if we need a 16bit A/D converter, then SNR must be equal to 98dB, if the signal bandwidth is 20KHz, then the sampling rate must equal to $2 \times 10^9 \times 20\text{KHz}$, it is impossible to implement. Because at such high frequency, quantization noise is no longer a white noise, it is correlated with input signal. So there is not only oversampling technique, we must add noise shaping technique also, if we want to achieve high resolution.

2.3.2 Noise Shaping

We can model a general ΣΔ modulator and its linear model as shown in Fig. 2.8.

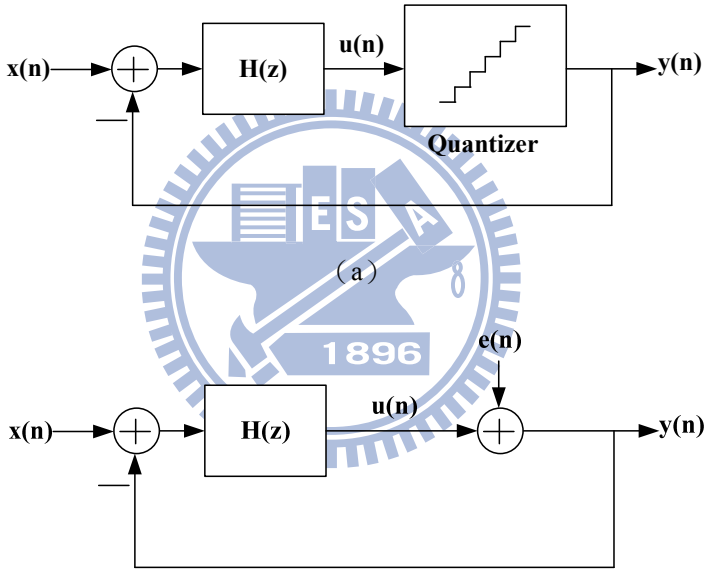


Fig. 2.8 (a) General ΣΔ modulator (b) Linear model with quantization noise

From Fig. 2.8(a), we can derive output Y(z) as (2.11)

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \qquad (2.11)$$

and define Signal Transfer Function S_{TF} and Noise transfer function N_{TF} as

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \qquad (2.12)$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \qquad (2.13)$$

where H(z) is the transfer function of a discrete time filter. There have two important meanings in (2.12), (2.13). If we want to obtain highest SNR, S_{TF} must be equal to 1, that means the input signal can transfer to output without attenuating; and N_{TF} (z) must be equal to 0, because the quantization noise will not affect output SNR.

In order to make N_{TF} (z) be a high pass filter, so at DC(z = 1), N_{TF} must be 0, and z = 1 is a pole of H(z), so the transfer function H(z) of the discrete filter is as

$$H(z) = \frac{1}{Z-1} = \frac{Z^{-1}}{1-Z^{-1}} \qquad (2.14)$$

Substitute (2.14) into (2.12) and (2.13), we can get

$$S_{TF}(z) = \frac{1}{z} \qquad (2.15)$$

$$N_{TF}(z) = 1 - \frac{1}{z} \qquad (2.16)$$

And we substitute z with $e^{j\frac{2\pi f}{fs}}$, then we can plot $|S_{TF}(f)|^2$ and $|N_{TF}(f)|^2$ in frequency domain, as Fig. 2.9. We can find $|N_{TF}(f)|^2$ also increases with frequency, and $|S_{TF}(f)|^2$ is always equal to 1, if we choose signal bandwidth in low frequency, then we can get highest signal power and lowest noise power, from this figure we see that quantization noise is moved to higher frequency significantly, this is the noise shaping effect.

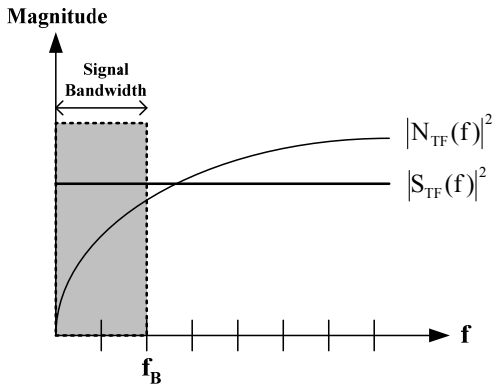


Fig. 2.9 Noise shaping

After noise shaping, we can filter out the noise in high frequency by using digital filter, and we will illustrate its architecture more detail in the next chapter.

3
Architectures of Sigma-Delta Modulator

Before we introduce various architectures of ΣΔ modulators, we must to realize the basic architecture of a general ΣΔ A/D converter. Fig. 3.1 is a complete block diagram of a ΣΔ A/D converter [18], and we can divide it into two different parts. First part is the ΣΔ modulator. The main function of this part is doing oversampling and noise shaping to the input analog signal. Second part is the decimation filter. The main function of this part is to remove noise in high frequency and down sampling the sampling frequency to base band frequency.

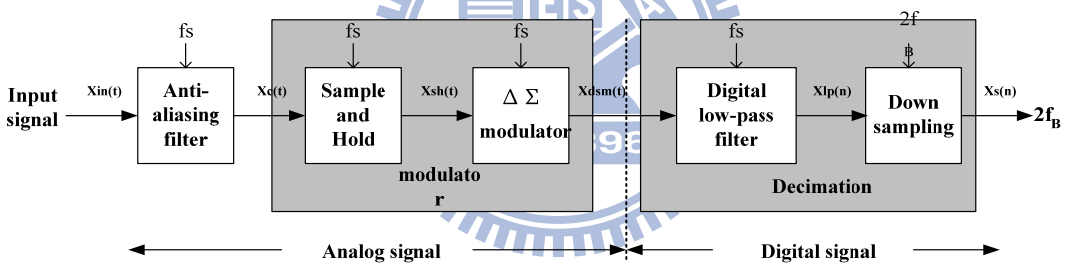


Fig. 3.1 Block diagram of ΣΔ A/D converter

First, the input signal Xin(t) pass an Anti-aliasing filter, the 3dB frequency of this filter is about few times of Nyquist frequency, so signal and noise out of Nyquist frequency is filtered roughly, and this signal goes into the ΣΔ modulator after goes through a S/H circuit. However, in the circuits implement situation, the sample and hold function is included in the circuits of ΣΔ modulator, so the signal Xc(t) will pass this modulator and produces a high speed data code Xdsm(n), because of noise shaping, the quantization noise will appear in high frequency. Finally, we must filter the noise in high frequency and reduce the sampling frequency to Nyquist frequency by a decimator, and passes the digital signal to

the output [18].

In this chapter, we will focus on the architectures of ΣΔ modulator, because that the noise model and optimal method is focus on this part, we must understand the theorem, benefits and drawbacks of each kinds of ΣΔ modulators. In addition, the implement of decimator is very typical [21][22]. In today's technology, DSP processors are also used to replace decimators, so we will introduce this part roughly.

3.1 First-Order Sigma-Delta Modulator

We recall that H(z) in (2.14) is $\frac{Z^{-1}}{1-Z^{-1}}$, substitute it into Fig. 2.8, then we can get a first-order ΣΔ modulator; Analyze transfer function H(z) from time-domain, it indicates that output signal m(t) is obtained by adding the delayed input signal n(t-1) and the delayed output signal m(t-1), so we can express a complete first-order ΣΔ modulator as Fig. 3.2.

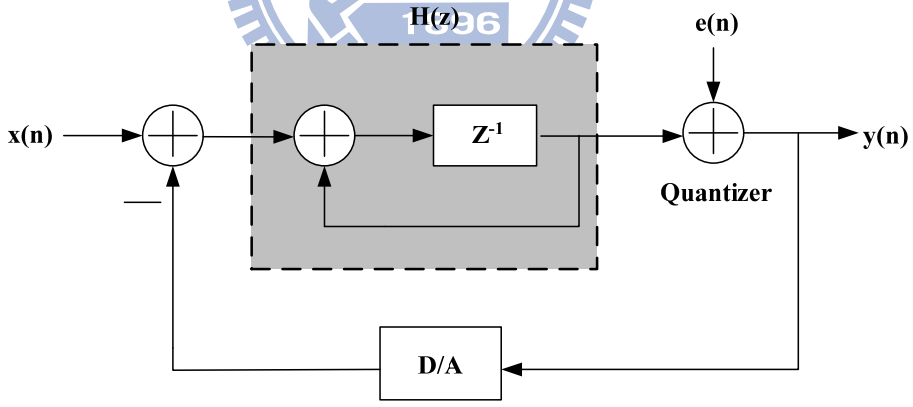


Fig. 3.2 First-order ΣΔ modulator

H(z) in Fig. 3.2 is indicated the effects of delay and accumulation, this is equivalent with an integrator in circuit design, so the three circuits components of ΣΔ modulator are integrator, quantizer and DAC in the feedback path.

A first order ΣΔ modulator's output can represent as

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \qquad (3.1)$$

From (3.1) we can find the signal transfer function is as a delay function, and noise transfer function is as a high pass filter, moves the noise to high frequency. In order to derive PSNR of first order ΣΔ modulator, we must get the magnitude of $N_{TF}(z)$ and $S_{TF}(z)$ in the frequency domain, so we substitute z with $e^{j2\pi \cdot f/f_s}$, and get $|S_{TF}(f)|$ and $|N_{TF}(f)|$ respectively as:

$$|S_{TF}(f)| = |z^{-1}| = |e^{-j2\pi \cdot f/f_s}| = 1 \qquad (3.2)$$

$$N_{TF}(f) = 1 - e^{-j2\pi \cdot f/f_s} = \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi \cdot f/f_s}$$

$$\Rightarrow \quad |N_{TF}(f)| = 2 \cdot \sin(\frac{\pi f}{f_s}) \qquad (3.3)$$

So the quantization noise in base band $\pm f_B$ can obtain by (2.7) and (3.3)

$$P_Q = \int_{-f_B}^{f_B} S_e{}^2(f) \cdot |N_{TF}(f)|^2 df = \int_{-f_B}^{f_B} \frac{V_{LSB}{}^2}{12 \cdot f_s} \cdot \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \cdot df \qquad (3.4)$$

Because that f_B is much lower than f_s, so $\sin(\pi f/f_s)$ is approximate equal to $(\pi f/f_s)$, and P_Q is as

$$P_Q = \frac{V_{LSB}{}^2 \pi^2}{36} \cdot (\frac{1}{OSR})^3 = \frac{FS^2 \cdot \pi^2}{36 \cdot 2^{2B} \cdot OSR^3} \qquad (3.5)$$

From (2.5) and (3.5), if we have the maximum signal power, then PSNR is as (3.6)

$$PSNR = 10 \log(\frac{P_{signal}}{P_Q}) = 10 \log(\frac{3}{2} 2^{2B}) + 10 \log[\frac{3}{\pi^2}(OSR)^3]$$

$$= 6.02B + 1.76 - 5.17 + 30 \log(OSR) \qquad (3.6)$$

From (3.6), we find that each octave of OSR, PSNR will increase 9dB, increase 1.5 bit in resolution. Compare (3.6) with (2.10) that only has oversampling effect; we can find that 1st order noise shaping increases the performance of ΣΔ modulator.

3.2 Single-Loop Second-Order Sigma-Delta Modulator

When the discrete time filter in Fig. 2.8 is replaced by two cascade integrator, then it is a second order ΣΔ modulator, output of the first integrator is only connecting with the input of the second integrator, it is shown in Fig. 3.3

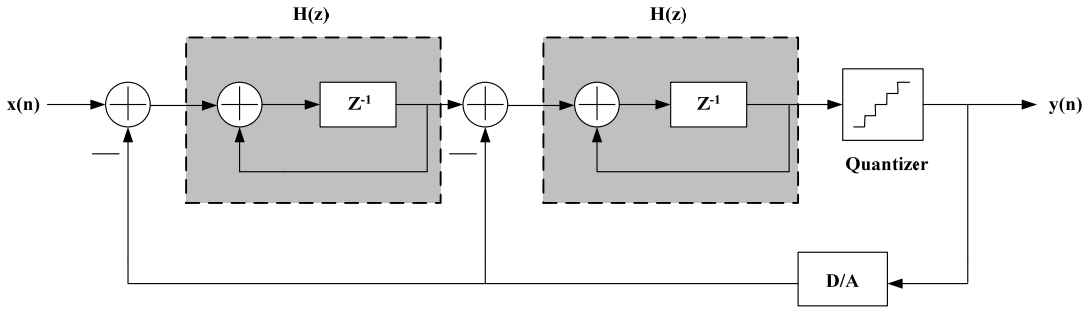


Fig. 3.3 Single loop second order ΣΔ modulator

Then the output of it can easily be derived as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \qquad (3.7)$$

where S_{TF} and N_{TF} is as

$$S_{TF}(z) = z^{-2} \qquad (3.8)$$

$$N_{TF}(z) = (1- z^{-1})^2 \qquad (3.9)$$

Using the same method in (3.3) (3.4), we can obtain

$$\left|S_{TF}(f)\right| = 1 \qquad (3.10)$$

$$\left|N_{TF}(f)\right| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \qquad (3.11)$$

$$P_Q = \frac{V_{LSB}{}^2 \cdot \pi^4}{60 \cdot OSR^5} = \frac{FS^2 \cdot \pi^4}{2^{2B} \cdot 60 \cdot OSR^5} \qquad (3.12)$$

So finally, PSNR of the second order ΣΔ modulator is as

$$PSNR = 10\log\left(\frac{P_{signal}}{P_Q}\right) = 10\log\left(\frac{3}{2}2^{2B}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

$$= 6.02B + 1.76 - 12.9 + 50\log(OSR) \quad (3.13)$$

In the single loop second order architecture, each octave of OSR can increase PSNR by 15 dB, it is equivalent to 2.5 bit in resolution. If we compare (3.13), (3.11) with $|NTF(f)|=1$ that without noise shaping, as Fig. 3.4, we can find that in our needed signal bandwidth, the quantization noise is highest when $|NTF(f)|=1$, and that with second order noise shaping is smallest among this figure [18].

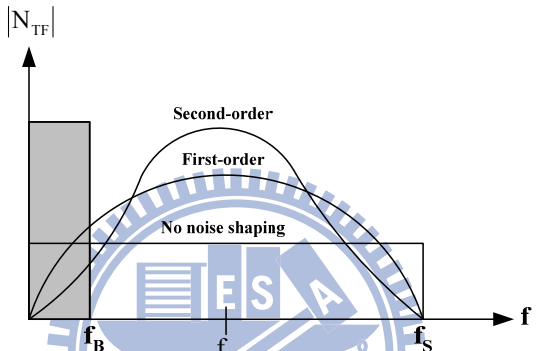


Fig. 3.4 Comparison of noise shaping techniques

3.3 Single-Loop High Order Sigma-Delta Modulator

Fig. 3.5 is a single loop high order ΣΔ modulator, from the derivation in Section 3.1 and Section 3.2, we can get the quantization noise P_Q in signal bandwidth is as

$$P_Q = \frac{V_{LSB}^2}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{OSR}\right)^{2L+1} \quad , L: \text{order} \quad (3.14)$$

and its PSNR is

$$PSNR = 6.02B + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \quad (3.15)$$

In the application of high order ΣΔ modulator, (6L+3)dB increases in SNR when OSR is octave, so PSNR can be raised by increasing the order of the system, especially at large oversampling ratio. But sometimes in high order architecture, the performance will be

worsen than result predicted by (3.13), because of the stability problem, it will make less effective noise shaping function, so the quantization noise will not be suppressed completely.

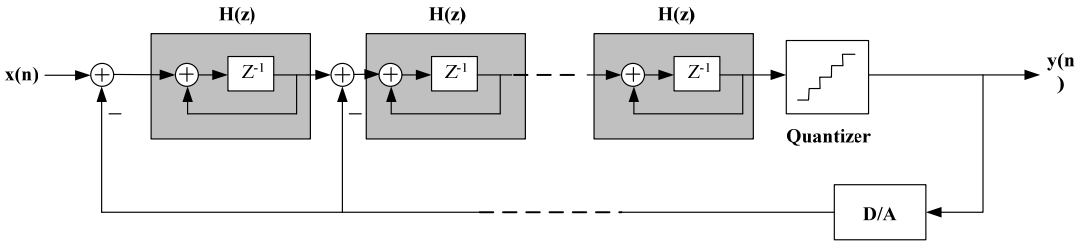


Fig 3.5 Single-loop high order ΣΔ modulator

3.4 Interpolative Sigma-Delta Modulator

Interpolative is a kind of high order ΣΔ modulator, it changes connection of some stages, adds some feedforward paths and feedback paths in order to suppose more aggressive noise shaping effect, Fig. 3.6 is a four-order interpolative architecture ΣΔ modulator [23].

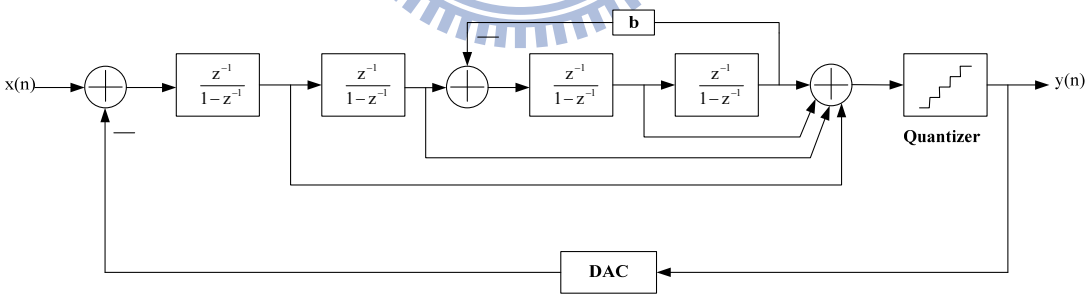


Fig. 3.6 Four-order interpolative architecture

This architecture also has stability problem, when the order L increases, each integrator produces one pole, and when the order is higher, poles of this system will also increase, and it will cause unstable situation, so the range of integrator gain will be limited; if the range of integrator gain is small, oscillation will appear in the circuits. Another is the considerations of clock control, when we use SC (switched-capacitor) to implement the integrator, each

integrator needs two clocks to control its operation, and we will need more clock to control the integrator when the order of system increases, it will produce more problems.

3.5 MASH Architecture

MASH (Multi-stage noise shaping) architecture is also called cascade architecture, which is a method that cascades several low order loops modulator in order to get high order noise shaping effect. The fundamental ideal of MASH is delivering quantization noise of front stage to input of next stage, and combining the digital outputs of all the stages with proper transfer function in digital domain, only the quantization noise of last stage will appear at the output, and the orders of N_{TF} is the same with total orders in the cascade ΣΔ modulator. Fig 3.7 is a three-order cascade ΣΔ modulator, its is the combination of a second-order and first-order ΣΔ modulator, so also called 2-1 cascade architecture.

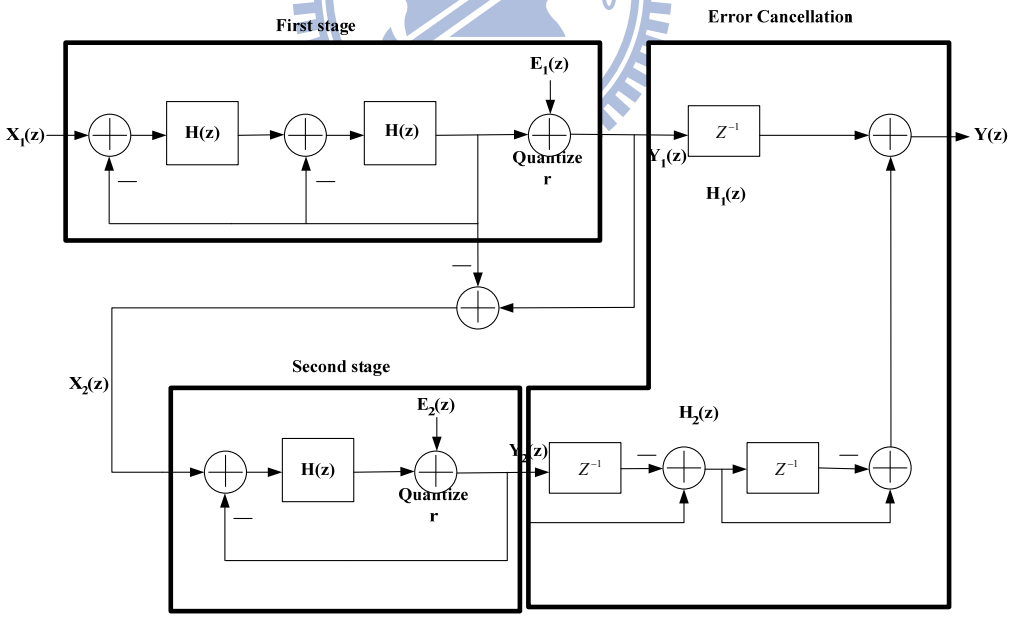


Fig. 3.7 2-1 architecture MASH ΣΔ modulator

From Fig. 3.7, we can derive the first stage output $Y_1(z)$ can be represented as

$$Y_1(z) = z^{-2}X_1(z) + (1-z^{-1})^2E_1(z) \quad (3.16)$$

Output of second stage $Y_2(z)$ is as

$$Y_2(z) = z^{-1}X_2(z) + (1-z^{-1})E_2(z) \quad (3.17)$$

and overall output of MASH Y(z) is as

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \quad (3.18)$$

and we can say that second stage input $X_2(z)$ is almost the same with $E_1(z)$, in order to eliminate first stage quantization noise $E_1(z)$, from (3.16) ~ (3.18), we can define the error cancellation functions $H_1(z)$ and $H_2(z)$ as

$$H_1(z) = z^{-1} \quad (3.19)$$

$$H_2(z) = (1-z^{-1})^2 \quad (3.20)$$

From (3.16)~(3.20), $E_1(z)$ can be eliminated, and second stage quantization noise $E_2(z)$ is shaped by third-order noise shaping function, and the MASH output Y(z) is as

$$Y(z) = z^{-3}X_1(z) + (1-z^{-1})^3E_2(z) \quad (3.21)$$

The most significant advantage of this architecture is that stability is not an issue, because it is composed by several low-order systems, and the quantization noise will not be amplified stage by stage, so its stability is good. Most important, the noise shaping function is equivalent as high order ΣΔ modulator, so it is popular in recent publications [4][6]. However, there also have some drawbacks of this topology; it is sensitive to the circuits' imperfections, such as finite DC gain of OTA, variance of integrator gain due to capacitor mismatch and non-zero switch resistance. These are all practical considerations when we design a MASH architecture ΣΔ modulator [3].

3.6 Multi-bit Quantizer Sigma-Delta Modulator

The demands of high resolution and high bandwidth ADC are more and more in recent years. In a high signal bandwidth, OSR of ΣΔ ADC can't be too high, and the peak SNR of a ΣΔ modulator with such limited OSR can't satisfy of high resolution applications, if we use higher order architecture, then the performance will degrade due to instability. So the most general method to increase performance is to use multibit quantizer. The most

obvious advantage of using multibit quantizer is that the distance between quantizer level V_{LSB} in (2.4) is much smaller due to increasing of B, and according to (2.3), the power of quantization noise is attenuated. Fig. 3.8 is the results of theoretical peak SNR of ΣΔ modulator versus oversampling ratio, with different order and quantizer bits, it is noted that peak SNR of the same OSR is increase 6 dB with each additional bit number in quantizer, and at low OSR, low order higher bit number architecture has equivalent performance as high order architecture. This result is usable for high bandwidth applications, and the power consumption of digital circuit in ΣΔ modulator is reduced due to lower sampling rate [24].

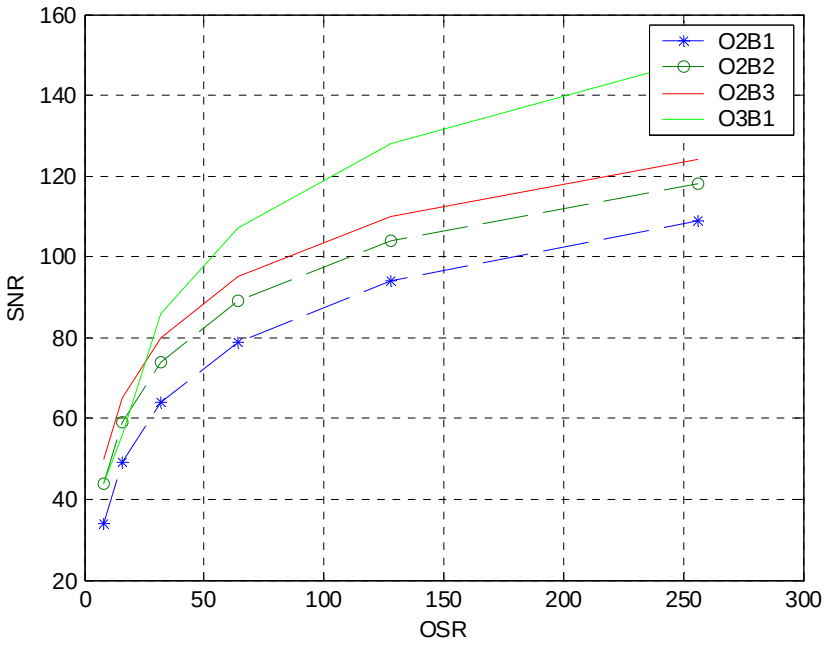


Fig. 3.8 SNR vs. OSR with different quantizer bit number

Because of using multi-bit quantizer, so we also need to use multi-bit DAC(Digital-to Analog Converter) to transfer the digital output to analog signal, and feed it back to integrator. The most significant disadvantage is the non-linearities introduced by multi-bit DAC can degrade the performance of ΣΔ converter, like Fig. 3.9. It is a linear model of multi-bit ΣΔ modulator, where E(Q) and E(D) represent the quantization noise and feedback DAC noise respectively. The values of these capacitor elements in DAC will not equal to ideal values that we need, it is due to process variation, typical value of mismatch

in modern CMOS technology is about 0.05% ~ 0.5%. In recent years, so many researches are make efforts on reduce DAC noise due to mismatch, such as trimming [19], Dynamic element matching (DEM)[8][25], although trimming is effective, but it has a expensive production step. So, DEM becomes more and more popular because of its efficiency and cheaper cost.

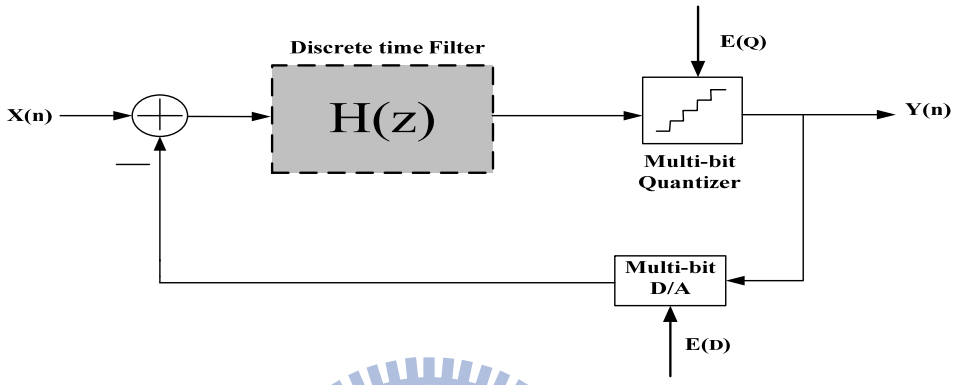


Fig. 3.9 Multi-bit architecture

3.7 Multi-bit Sigma-Delta Modulator use DEM Technique

Dynamic element matching is a different approach to decrease the DAC noise, it is used to improve the linearity of pure DACs [26], but now it is most used in inner DAC of multi-bit ΣΔ modulator. A DAC with DEM technique is illustrated in Fig. 3.10, 2^B bits thermometer code is put into the element selection logic block, and the function of element selection logic is try to select DAC elements in such way let the errors introduced by DAC average to zero for several operation periods. Because the DEM block is located in feedback loop, so its delay must be very small prevent to degrade the performance of ΣΔ converter, therefore the algorithm used in the DEM block must be simple. There are several techniques of DEM, such as Randomization [27], Clocked Averaging (CLA) [26], Individual Level Averaging (ILA) [28], Data Weighted Averaging (DWA) [29], Randomization is the first approach to use DEM technique in ΣΔ ADC, and DWA offers a good performance to reduce DAC error, in this section, an overview introduction of these two algorithms will be presented, and the operation

principle of them will be explained.

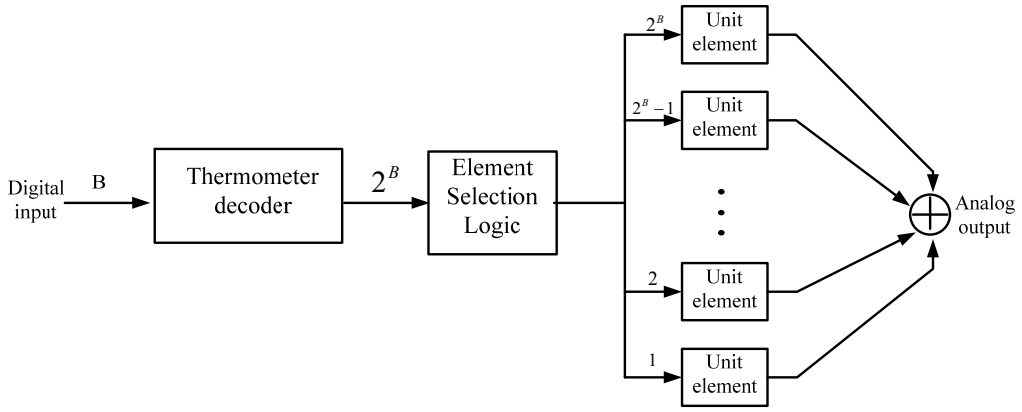


Fig. 3.10 A B-bit DAC with DEM technique

3.7.1 Randomization Technique

The main operation principle of randomization is that the element selection logic performs as a randomizer. In each clock period, the randomizer selects DAC elements randomly to generate the output of DAC. If the randomizer is ideal, then the DAC noise will become uncorrelated with each other. Simulation results show that randomization DEM technique reduces the noise floor from DAC error by several dB, but it still be a white noise in low frequency. Fig. 3.12 is the output spectrum of a second-order ΣΔ modulator with a 0.1% capacitor mismatch, it is notable that the noise floor of randomization DEM is lower than that without any calibration technique in the feedback DAC.

3.7.2 Data Weighted Averaging (DWA)

DWA is a efficiently method to reduce DAC mismatch noise, it uses one register to remember the capacitor last time used, and always points to the first unused unit capacitor in this clock, so DWA rotates through all the unit capacitors such that all capacitors are used at the maximum possible rate. From this algorithm, each elements is used the same number of times in long interval, this ensures that the errors caused by the DAC average to zero

quickly. In Fig. 3.11, it is a 4-bit DAC and the shaded boxes are the number of 1's in the thermometer code. Assumes that the input codes sequence is 8, 8, 10, 9, 10, 10, 11, 11, 12, 11, 14, 11, 14, 13, 12, 15... Fig. 3.12 is the simulation results of a third order ΣΔ modulator, we can see that without DEM has highest noise floor and DWA works as a first order noise shaping function of DAC noise, ideal DAC only with quantization noise has third-order noise shaping.

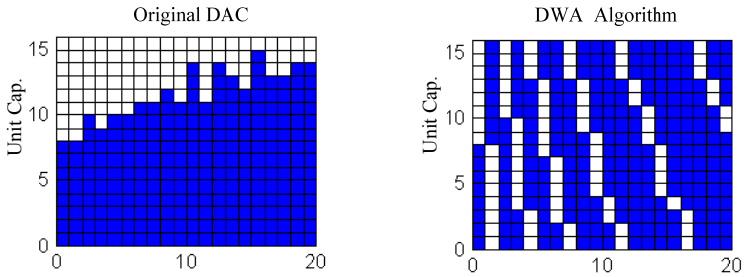


Fig. 3.11 Operation principle of the DWA algorithm

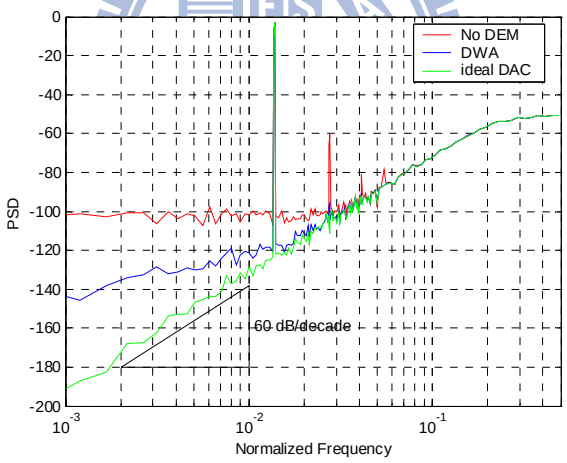


Fig. 3.12 Output spectrum with three kinds of DAC

Another consideration is the sub-ADC(quantizer) of the ΣΔ modulator, we usually use Flash A/D as the multi-bit quantizer because of its high speed, but Flash A/D has a significant disadvantage is that the number of comparators of it is proportional to 2^B. That means a 6 bit quantizer needs 64 comparators, the occupied area of comparator may not much, but in modern SOC applications, the problems of power and area are important, so it becomes one limitation of multi-bit quantization.

ΣΔ A/D converter is attractive for high resolution application, for higher signal bandwidth, we increase system order to raise SNR, but it still have stability problem. So people develop MASH and multi-bit architecture to improve its performance. Finally, we classify they into low order, high order, MASH and multi-bit four kinds of architecture, and compare their advantage and disadvantage as Fig. 3.13 [30]

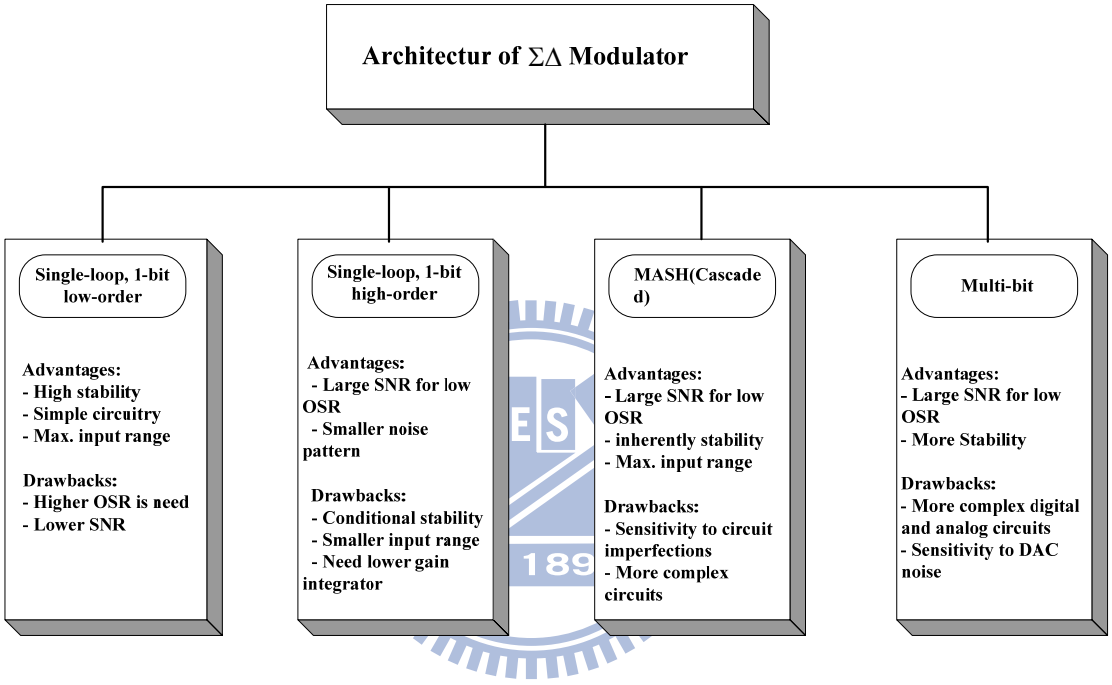


Fig. 3.13 Comparison of ΣΔ modulator architectures

3.8 Decimator

In ΣΔ A/D converter, digital decimator is used to process digital signal of the quantizer output, the high speed data word after oversampling modulation can't be used directly. Because there have original signal and quantization noise among it, so the main function of decimator is to convert the oversampled B-bit output words of the quantizer at a sampling rate of fs to N-bit words at Nyquist rate of input, and removes the noise out of signal band.

In order to prevent the noise introduced by other frequency, the decimator filter must have very flat signal pass-band, and sharp transition region and enough signal attenuation in stop band. Two-stage decimator is used in a general situation, because that single stage decimator is difficult to convert sampling rate to Nyquist rate in 1 time and without degrading SNR. In the first stage, we can down-sample the sample frequency to 2~4 times of Nyquist frequency, and in the second stage, we can use IIR or FIR filter that have high linearity [19]. For a large OSR, multi-stage decimator is used.

3.9 Performance Metrics for a ΣΔ Modulator

In order to understand the performance merits used to specify the behavior of ΣΔ modulator, several specifications concerning the performance are discussed [15].

- **Signal to Noise Ratio:** The SNR of a data converter is the ratio of the signal power to the noise power, measured at the output of the converter for a certain input amplitude. The maximum SNR that a converter can achieve is called the peak SNR.
- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for a certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.
- **Dynamic Range at the input:** The DRi is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is determined by the noise floor of the converter.
- **Dynamic Range at the output:** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic

range at the output DR_o, which is exactly equal to peak SNR.

- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also includes the distortion components and can be calculated from (2.6) as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{3.22}$$

- **Overload Level:** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 3.14. This figure shows the SNR and SNDR of the ΣΔ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently, the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specifications are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 3.14 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

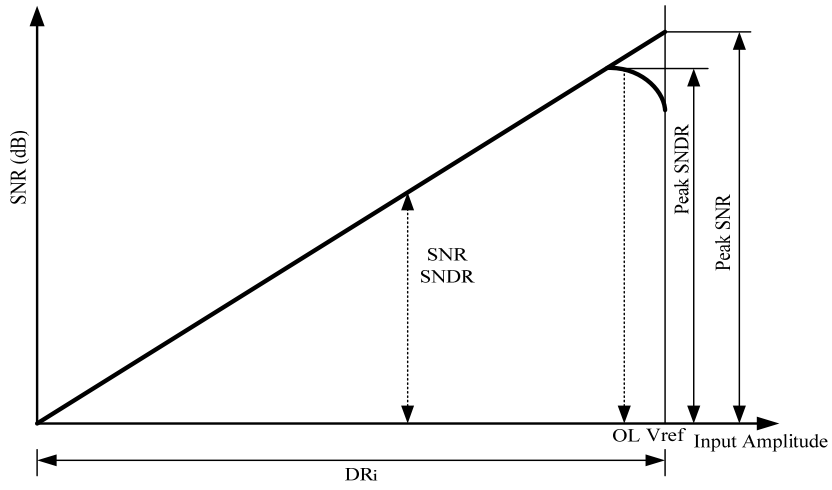


Fig. 3.14 Performance characteristic of a ΣΔ converter

4

Discuss About Different Architecture of Non-idealities Noise and Distortion Models

Proposing an optimization algorithm for searching design parameters which maximizes ΣΔ ADC SNDR, while minimizing power consumption is one of the primary purposes. Model completeness determines success of this goal. The ΣΔ modulator major nonidealities are finite OTA gain error, thermal noise, settling error, multi-bit DAC noise, and jitter noise. All nonideality models in our model are expressed in noise power forms.

Our model can include all SDM typical architectures where all noises are dominated by the first integrator in the chain. And some noises or distortion (quantization noise [30], finite gain error [30], settling error [9] and nonlinear DC-gain distortion [31]) may change in different system structure which related to order number or system feedback value see as Fig. 4.1. Furthermore, thermal noise [30], multi-bit DAC noise [32], jitter noise [1] and DAC distortion are independent of system architecture.

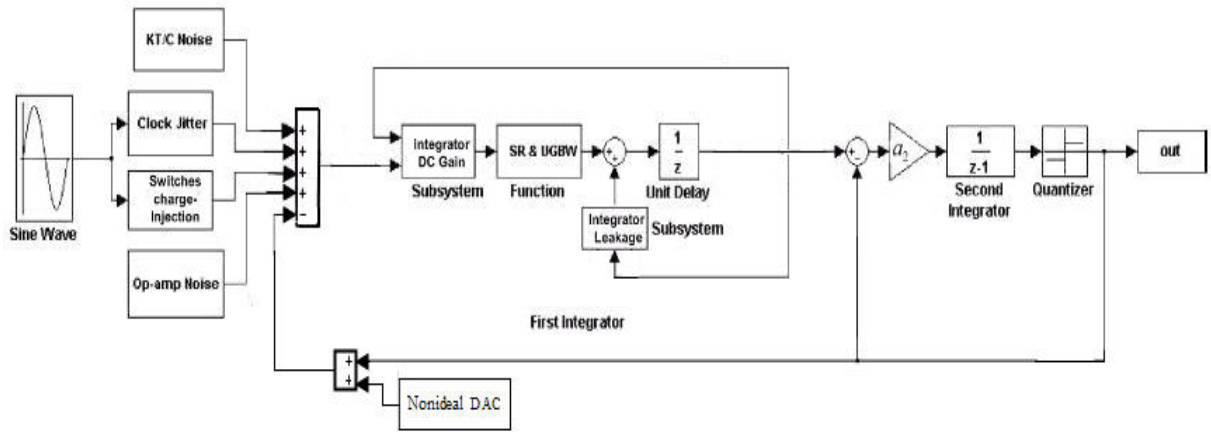


Fig. 4.1 SDM nonideal model

5
Op-amp Non-Linear Gain Curve

5.1 DC-gain Distortion Can Be Severe

A second order SDM with OSR = 20, V_{OS} = 0.6, a 3-bit quantizer, a 1V sinusoidal input signal, and a relatively small DC-gain A_O = 50db, will see a severe DC-Gain distortion at about -61dB, which easily dominates other noises and distortions, e.g. quantization noise (-81 dB) and DAC distortion (-76 dB, without DEM), and results in a poor SNDR at 60 dB.

5.2 Modeling Nonlinear DC-gain Curves

It is well known that the output resistance of op-amp output-stage-transistors is dependent on the output voltage V_o. This dependency results in nonlinear op-amp DC-gain when V_o changes, as is shown in Fig. 5.1. A typical nonlinear DC-gain curve can be approximated by the polynomial:

$$A_V(V_o) = A_0(1 + q_2V_o^2 + q_4V_o^4) \tag{5.1}$$

where $A_V(V_o)$ is the nonlinear DC-gain of op-amp, and A_O is the maximum DC-gain when V_o is in the neighborhood of 0V.

It is well known that $|V_{GSQ}|$ of the output-stage transistors and the maximum DC-gain A_O are the only two parameters which can affect the shape of the nonlinear curves $A_V(V_o)$. It is also well known that maximum output swing V_{OS} and $|V_{GSQ}|$ have germane relation with each other. Since V_{OS} makes much more sense for practical designers, we replace $|V_{GSQ}|$ by V_{OS}, and in the rest of this paper V_{OS} and A_O are the only two parameters which affect

$A_V(V_o)$. In order to demonstrate the effects of V_{OS} and A_O on $A_V(V_o)$, Spice op-amp simulations in Fig. 5.2(a), (b) respectively show the effects that A_O and V_{OS} can have on the shape of DC-gain curves.

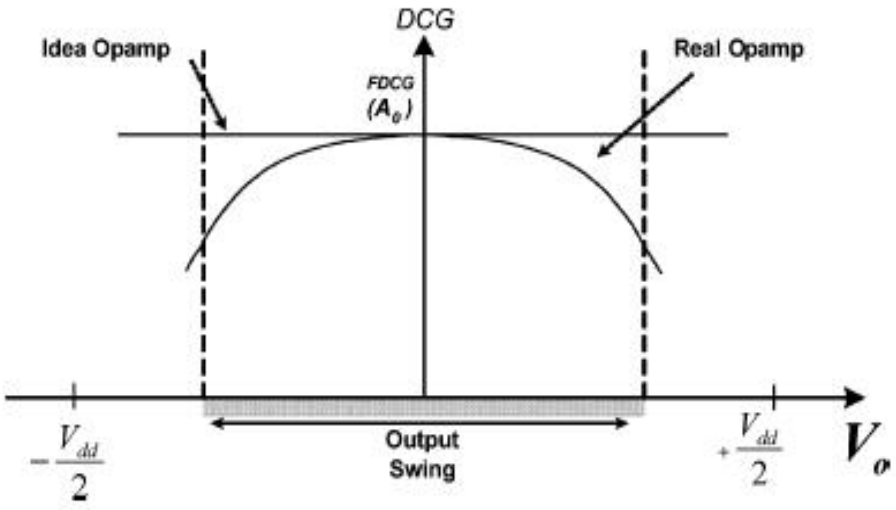
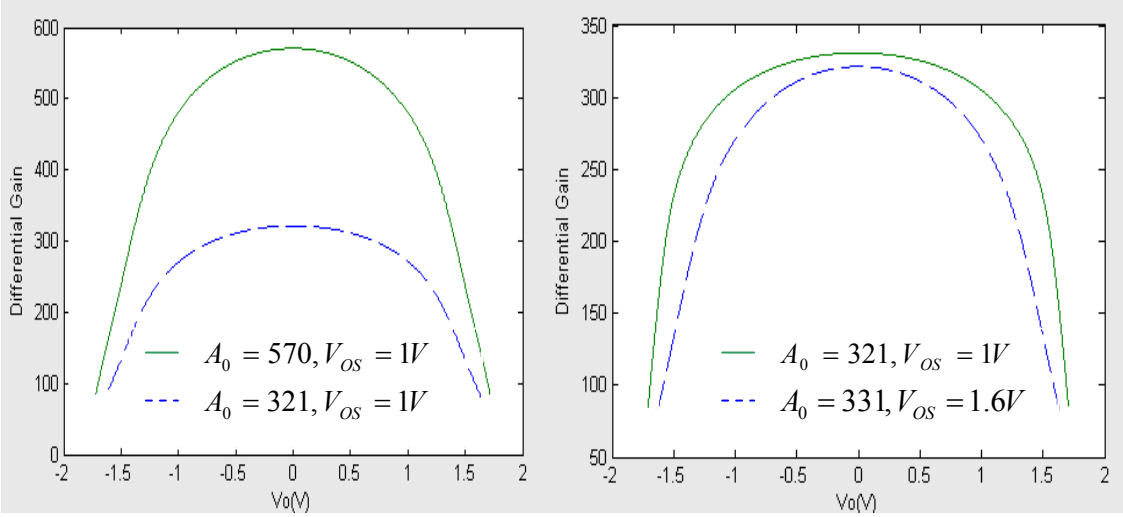


Fig. 5.1 DCG curve versus output voltage with the rail to rail voltage of VDD



(a) (b)

Fig. 5.2 (a) Two nonlinear DC-gain curves with identical V_{OS} but different A_O
(b) Two nonlinear DC-gain curves with similar A_O but different V_{OS}

In order to model the nonlinear gain $A_V(V_o)$, we tried various combination of A_O and V_{OS} to create a set of representative curves for the family of nonlinear DC-gain curves.

Then, we endeavored to find out suitable q_2 and q_4 such that (5.1) can reasonably fit all of these curves. After intensive tries and errors, we come up with the q_2 and q_4 in (5.1) to be

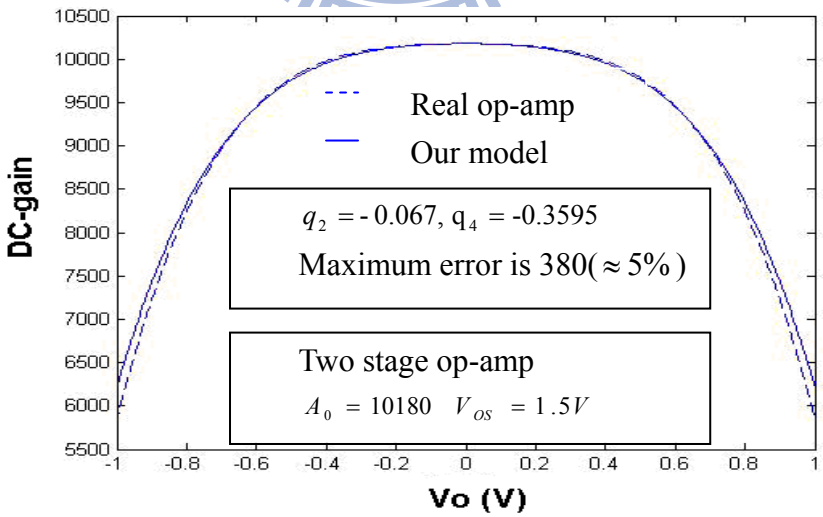
$$q_2 \equiv -9 \cdot \left(\frac{A_O^{0.01}}{(1+V_{OS})^{2.6}}\right)^2 \tag{5.2}$$

$$q_4 \equiv -6 \cdot \left(\frac{A_O^{0.0001}}{(1+V_{OS})^{0.83}}\right)^4 \tag{5.3}$$

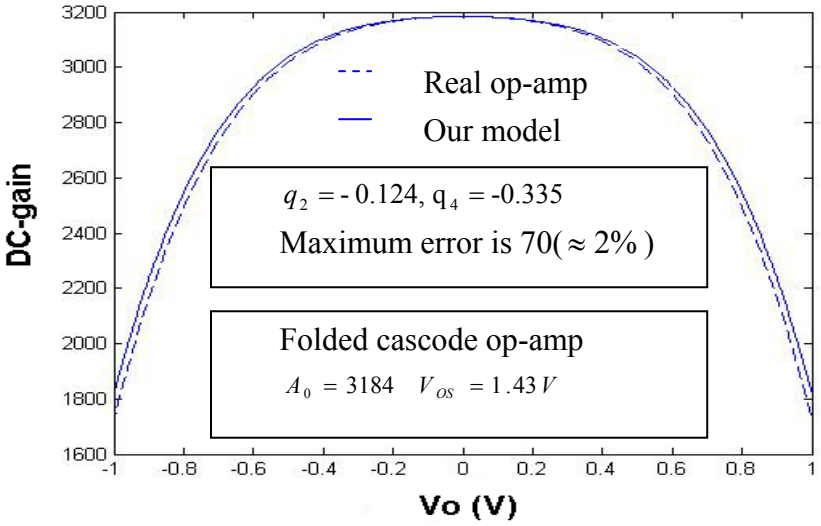
Although the q_2 and q_4 are obtained from tries and errors, the searching and testing time for them is more than one year. We are confident that the model (5.1) – (5.3) is sufficiently general and accurate, as is verified in the next subsection.

5.3 Verifying Nonlinear DC-Gain Curve Model

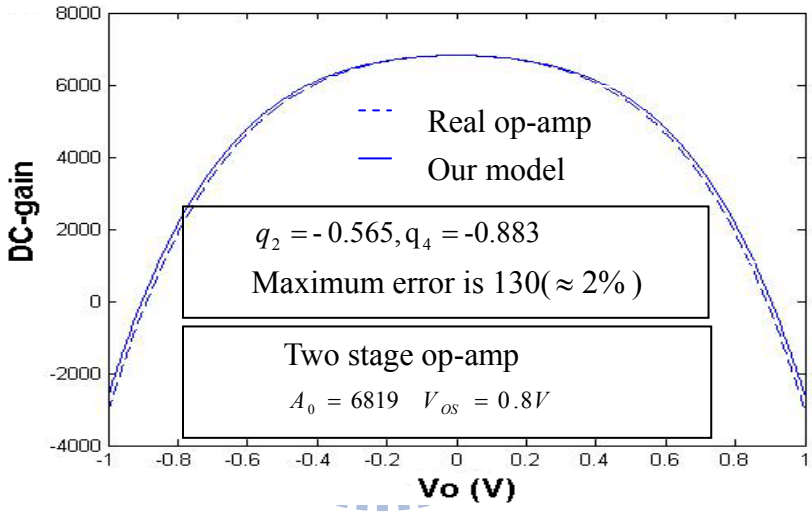
Comparisons of DC-gain curves from real op-amps and from our model (5.1) – (5.3) are shown in Fig. 5.3. The comparisons are



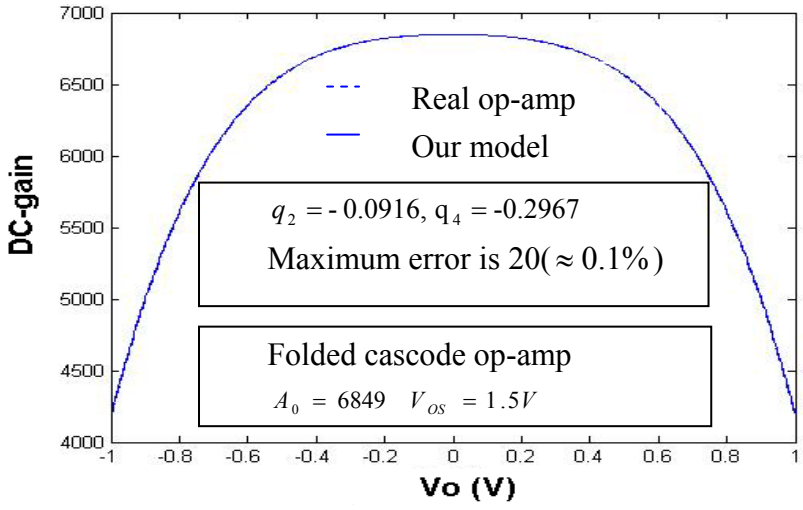
(a)



(b)



(c)



(d)

Fig. 5.3 Comparisons between op-amp nonlinear DC-gain curves from real op-amp and from our model

deliberately planed to cover various op-amp structures and representative points in op-amp parameter space. The sub-figures in Fig. 5.3 are cross-related as follows:

1. (a) and (c) are two-stage op-amps, and (b) and (d) are folded cascode op-amps.
2. (a) and (b) have large difference in the values of A_O .
3. (c) and (d) differs mainly in V_{OS} .

For the four cases presented in Fig. 5.3, the errors between op-amp nonlinear DC-gain curves from real op-amps and from our model range from 0.1% to 5%. This demonstrates that our model (5.1) – (5.3) is sufficiently general and accurate.

6

SDM DISTORTION DUE TO THE NONLINEAR DC-GAIN OF THE OPERATIONAL AMPLIFIER

In section 6, we analyze the op-amp nonlinear DC-gain phenomenon, and obtain a nonlinear DC-gain model (5.1) – (5.3). In this section, based on the model (5.1) – (5.3), we want to derive a nonlinear distortion model for all architecture SDM output distortions caused by nonlinear DC-gain in op-amps. Fig.6.1 shows the block diagram of an ideal SDM for single-loop 2nd. We will first discuss the property of V_S which is the input to the first integrator. Then the transfer characteristics of the integrator are analyzed, based on which the SDM nonlinear DC-gain distortion model is derived. Distortion models for other SDM structures can be obtained following the approach in this section.

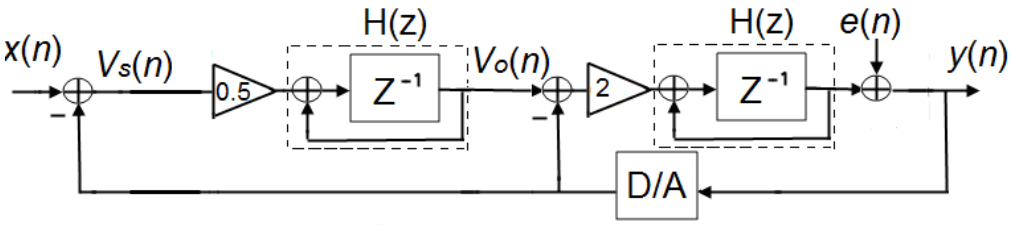


Fig. 6.1 Single-loop second-order ΣΔ modulator

6.1 Properties of V_S

In Fig. 6.1, the SC integrator input V_S can be expressed without the noise part as

$$V_S(z) = (1 - z^{-n_{order}})X(z) \tag{6.1}$$

Where n_{order} is SDM feedback stage number. To analyze the signal part, with

$x(n) = A_{in}\sin(wnT)$, we perform inverse z-transform to (6.1), and one obtains

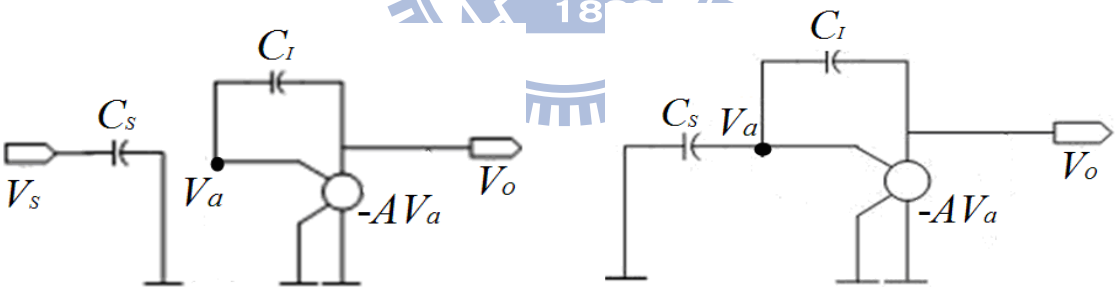
$$V_S(nT) = A_{in}\sin(wnT) - A_{in}\sin(w(n-n_{order})T)\cdot u(w(n-n_{order})T)$$
$$\approx A_{in}\cdot\sin(\frac{n_{order}\times\pi}{OSR})\cdot\cos(wnT) \quad (6.2)$$

Then, the amplitude of V_S can be approximated as

$$|A_{VS}| = |V_S(n_{order}\cdot nT)| = |A_{in}\sin(n_{order}\cdot wnT)| \cong n_{order}\cdot A_{in}\cdot w\cdot T \quad (6.3)$$

6.2 Transfer Characteristics of the First Integrator

The sampling phase and integration phase of a switch capacitor integrator are shown in Fig. 6.2. In the following discussion, signals $V_O((n+1/2)T)$, $V_O((n-1/2)T)$ and $V_s(nT)$ will be respectively denoted by V_O^+, V_O^- and V_S. Suppose settling problem is ignored, which requires separate treatment. Then, the sampling phase is ideal, and the input/output characteristics of the integration phase can be completely described by the following three equations



(a) Sampling phase (b) integration phase

Fig. 6.2 Switch-capacitor integrator with nonlinear DC-gain op-amp

$$A_V(V_O) = A_O(1+q_2V_O^{\ 2}+q_4V_O^{\ 4}) \quad (6.4)$$

$$V_O^{\pm} = -A_V(V_O^{\pm})\cdot V_a^{\pm} \quad (6.5)$$

$$C_I\cdot(V_o^+ - V_a^+) - C_S\cdot V_a^+ = C_I\cdot(V_o^- - V_a^-) + C_S\cdot V_S \quad (6.6)$$

Substituting (6.4) and (6.5) into (6.6), one obtains the following expression

$$
\begin{aligned}
&V_O^+ - V_O^- \\
&= K_S \cdot \{1 + \frac{1}{A_O} \cdot [q_2 \cdot ((V_O^+)^2 + (V_O^+)(V_O^-) + (V_O^-)^2) + (q_4 - {q_2}^2) \cdot ((V_O^+)^4 \\
&+ (V_O^+)^3 (V_O^-)^1 + (V_O^+)^2 (V_O^-)^2 + (V_O^+)^1 (V_O^-)^3 + (V_O^-)^4)] + \cdots \frac{1}{{A_O}^\infty}\} \cdot V_S
\end{aligned}
\tag{6.7}
$$

where K_S is C_S / C_I. The problem with (6.7) is that the integrator output $V_O^{\pm}$ also appears at right-hand-side of (6.7). However, since $V_O^{\pm}$ can be shown to relate to V_S in (6.2) as follows

$$
V_O^{\pm} \approx -\frac{K_S}{1 + \frac{1 + K_S}{A_O}} \cdot \frac{1}{\sqrt{4 - \frac{4 \cdot K_S}{A_O}} \cdot \sin\frac{wT}{2}} \cdot \{A_{VS} \cdot \sin\left(w(n \pm \frac{1}{2})T\right)\} \tag{6.8}
$$

the $V_O^{\pm}$ and V_S at right-hand side of (6.7) can be substituted by (6.8) and (6.2), and take its nonlinear term resulting in

$$
\begin{aligned}
V_O^+ - V_O^- = K_S \cdot \frac{1}{A_O} \{ & \frac{3}{4 - \frac{4K_s}{A_O}} \cdot \left(\frac{K_S}{1 + \frac{1 + K_S}{A_O}} \right)^2 \cdot {A_{VS}}^2 \cdot q_2 \cdot \cot^2(\frac{1.5708}{OSR}) \cdot \sin^2(wnT) \\
& + \frac{5}{(4 - \frac{4K_S}{A_O})^2} \cdot \left(\frac{K_S}{1 + \frac{1 + K_S}{A_O}} \right)^4 \cdot {A_{VS}}^4 \cdot (q_4 - {q_2}^2) \cdot \cot^4(\frac{1.5708}{OSR}) \cdot \sin^4(wnT) \\
& + \frac{10}{(4 - \frac{4K_S}{A_O})^2} \cdot \left(\frac{K_S}{1 + \frac{1}{A_O}} \right)^4 \cdot {A_{VS}}^4 \cdot (q_4 - {q_2}^2) \cdot \cot^2(\frac{1.5708}{OSR}) \cdot \cos^2(wnT) \cdot \sin^2(wnT) \\
& + \frac{1}{(4 - \frac{4K_S}{A_O})^2} \cdot \left(\frac{K_S}{1 + \frac{1}{A_O}} \right)^4 \cdot {A_{VS}}^4 \cdot (q_4 - {q_2}^2) \cdot \cos^4(wnT)\} \cdot \\
& \{A_{in} \sin(wnT) - A_{in} \sin(w(n - n_{order})T) \cdot u((n - n_{order})T)\}
\end{aligned}
\tag{6.9}
$$

Equation (6.9) can be used to compute nonlinear DC-gain distortions appearing at 1st integrator output.

6.3 Nonlinear DC-gain Distortions at SDM Output

It is known that if the gain of the behind integrator equals one, i.e. $C_{S2}/C_{I2} = 1$, the same distortions appearing at 1st integrator output would appear at SDM output. Otherwise, some modification is needed on distortions at SDM output. Suppose behind integrator gain equals one. Then, the 3rd harmonic magnitudes in DC-gain disotritons can be computed from (6.9) as follows

$$A_{\sin\_3} = K_S \cdot \frac{1}{A_O} \cdot \frac{1}{16} \cdot \{[\frac{-12}{4-\frac{4K_S}{A_O}} \cdot \cot^2(\frac{1.5708}{OSR}) + \frac{4}{4-\frac{4K_S}{A_O}}]$$
$$\cdot [\frac{K_S}{1+\frac{1+K_S}{A_0}}]^2 \cdot A_{VS}{}^2 \cdot A_{in} \cdot q_2 + [\frac{-25}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^4(\frac{1.5708}{OSR})$$
$$+ \frac{10}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^2(\frac{1.5708}{OSR}) + \frac{3}{(4-\frac{4K_S}{A_O})^2}]$$
$$\cdot [\frac{K_S}{1+\frac{1+K_S}{A_0}}]^4 \cdot A_{VS}{}^4 \cdot A_{in} \cdot (q_4 - q_2{}^2)\} \cdot \left[1 - \cos(\frac{n_{order} \cdot \pi}{OSR})\right] \tag{6.10}$$

$$A_{\cos\_3} = K_S \cdot \frac{1}{A_O} \cdot \frac{1}{16} \cdot \{[\frac{-12}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^2(\frac{1.5708}{OSR}) - \frac{4}{(4-\frac{4K_S}{A_O})^2}] \cdot$$
$$[\frac{K_S}{1+\frac{1+K_S}{A_0}}]^2 \cdot A_{VS}{}^2 \cdot A_{in} \cdot q_2 + [\frac{-15}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^4(\frac{1.5708}{OSR})$$
$$- \frac{10}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^2(\frac{1.5708}{OSR}) + \frac{5}{(4-\frac{4K_S}{A_O})^2}]$$
$$\cdot [\frac{K_S}{1+\frac{1+K_S}{A_0}}]^4 \cdot A_{VS}{}^4 \cdot A_{in} \cdot (q_4 - q_2{}^2)\} \cdot \left[\sin(\frac{n_{order} \cdot \pi}{OSR})\right] \tag{6.11}$$

$$A_{\sin\_5} = K_s \cdot \frac{1}{A_O} \cdot \frac{1}{16} \cdot \{[\frac{5}{(4-\frac{4K_s}{Ao})^2} \cdot \cot^4(\frac{1.5708}{OSR}) - \frac{10}{(4-\frac{4K_s}{Ao})^2} \cdot \cot^2(\frac{1.5708}{OSR}) + \frac{1}{(4-\frac{4K_s}{Ao})^2}] \cdot [\frac{K_s}{1+\frac{1+K_s}{A_0}}]^4 \cdot {A_{vs}}^4 \cdot A_{in} \cdot (q_4 - {q_2}^2)\} \cdot \left[1 - \cos(\frac{n_{order} \cdot \pi}{OSR})\right] \quad (6.12)$$

$$A_{\cos\_5} = K_s \cdot \frac{1}{A_O} \cdot \frac{1}{16} \cdot \{[\frac{5}{(4-\frac{4K_s}{Ao})^2} \cdot Cot^4(\frac{1.5708}{OSR}) - \frac{10}{(4-\frac{4K_s}{Ao})^2} \cdot Cot^2(\frac{1.5708}{OSR}) + \frac{1}{(4-\frac{4K_s}{Ao})^2}] \cdot [\frac{K_s}{1+\frac{1}{A_0}}]^4 \cdot {A_{vs}}^4 \cdot A_{in} \cdot (q_4 - {q_2}^2)\} \cdot \sin(\frac{n_{order} \cdot \pi}{OSR}) \quad (6.13)$$

Then the powers of the 3rd and 5th harmonic distortions are

$$HD3_{NFDCG}(dB) = 10\log\frac{({A_{\sin\_3}}^2 + {A_{\cos\_3}}^2)}{2} \quad (6.14)$$

$$HD5_{NFDCG}(dB) = 10\log\frac{({A_{\sin\_5}}^2 + {A_{\cos\_5}}^2)}{2} \quad (6.15)$$

The model (6.10)-(6.15) indicates that the DC-gain distortions at SDM output are related to C_I, C_S, A_{in}, A_O, V_{OS} and OSR. Some qualitative properties about how each parameter can affect distortion magnitude are obtained from (6.10)-(6.15) and listed in TABLE 6.1.

	$C_I \uparrow$	$C_S \uparrow$	$A_{in} \uparrow$	$A_O \uparrow$	$V_{OS} \uparrow$	OSR$\uparrow$
Distortion magnitude	↓	↑	↑	↓	↓	↓

TABLE 6.1 The relationship between the each parameter and the harmonic distortions

Some quantitative investigation based on (6.10)-(6.15) shows that A_O and OSR are the most influential parameters on SDM DC-gain distortions. Therefore, an interesting example about how (6.10)-(6.15) can be utilized is that if the four parameters are fixed at A_{in} = 1v, V_{OS} = 0.8, C_S = 1pF and C_I = 2pF , then (6.10)-(6.15) can be employed to determine the minimum A_O and OSR required so that the DC-gain distortion can be kept under certain value. The results of single-loop 2nd are tabulated in TABLE 6.2.

HD3 distortion power(dB)	HD5 distortion power(dB)	A_O	OSR
-70	-80	≧1000	≧16
-90	-100	≧3000	≧64
-110	-120	≧6400	≧256

TABLE 6.2 Minimum required A_O and OSR

Due to loop shaping, the DC-gain nonlinearity in the second integrator degrades the performance to a much lesser extent, allowing a more relaxed design [33]. Therefore, only the DC-gain distortion caused by first integrator is considered in this paper.

6.4 Behaving Model Simulation Results

We use a calculable behavior model to verify our SDM nonlinear DC-gain distortion model. The z-domain transfer function of a delayed integrator of sigma-delta modulator is

$$H(z) = g \cdot \frac{z^{-1}}{1-\alpha \cdot z^{-1}} \tag{6.16}$$

$$\alpha = 1 - \frac{K_s}{A_0 \sum_{i=0}^{\infty} \beta_i V_o^{2i}} \cong 1 - \frac{K_s}{A_0}\left(1 - \sum_{i=0}^{\infty} \beta_i V_o^{2i}\right) \tag{6.17}$$

$$g = \frac{K_s}{1 + \frac{1}{A_0 \sum_{i=0}^{\infty} \beta_i V_o^{2i}}} \cong K_s \cdot (1 - \frac{1 + K_s}{A_0}(1 - \sum_{i=0}^{\infty} \beta_i V_o^{2i})) \tag{6.18}$$

where g and α are the integrator gain and leakage [34]. Then, one can place the nonlinear DC-gain behavior model (6.16) into the complete sigma delta modulator behavior simulation scheme. The diagram is shown in Fig. 6.3.

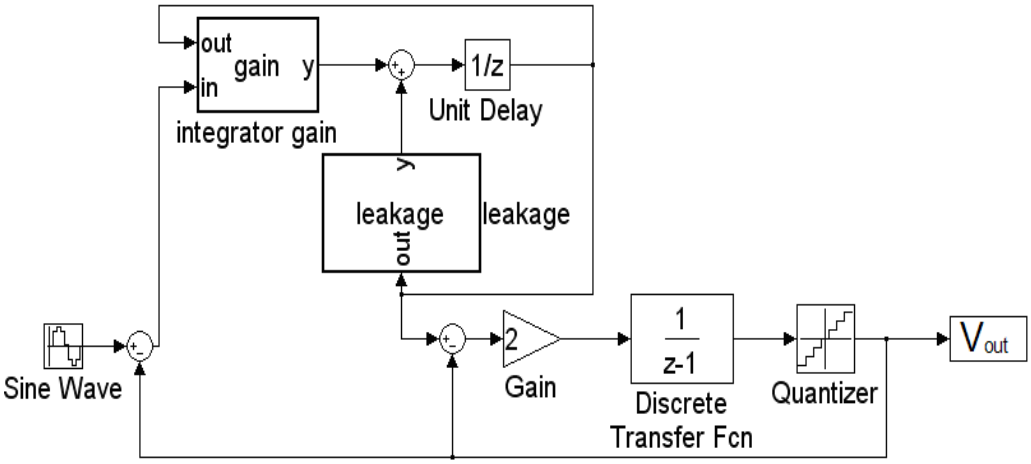


Fig. 6.3 Second-order SDM behavior model with nonlinear DC-gain

The behavior simulations are conducted for two different cases. The SDM output FFTs are shown in Fig. 6.4. The comparisons between simulation results and theoretical results are shown in TABLE 6.3, TABLE 6.4 and TABLE 6.5. The results from both simulation cases are very close to those obtained from our DC-gain distortion model.

A_o = 60db, V_{os} = 1.5	Theoretic (dB)	Simulink(db)
$A_{in} = 0.8$	HD3=-93.1 HD5=-106.72	HD3=-92.55 HD5=-102.2
$A_{in} = 1$	HD3=-84.34 HD5=-97.031	HD3=-83.11 HD5=-94.43
$A_{in} = 1.5$	HD3=-67.75 HD5=-79.42	HD3=-67.58 HD5=-80.28

TABLE 6.3 Comparison of theoretic result and behavior simulation of Case A.

$A_o = 50db, V_{os} = 1$	Theoretic (dB)	Simulink(db)
$A_{in} = 0.8$	HD3=-75.12 HD5=-89.59	HD3=-77.6 HD5=-85.1
$A_{in} = 1$	HD3=-66.59 HD5=-79.9	HD3=-67.05 HD5=-77.28
$A_{in} = 1.5$	HD3=-50.31 HD5=-62.29	HD3=-50.62 HD5=-62.75

TABLE 6.4 Comparison of theoretic result and behavior simulation of Case B.

$A_o = 60db, V_{os} = 1.5$	Theoretic (dB)	Simulink(db)
$A_{in} = 0.8$	HD3=-61.18 HD5=-75.9	HD3=-64.76 HD5=-71.39
$A_{in} = 1$	HD3=-52.73 HD5=-66.23	HD3=-53.61 HD5=-63.4
$A_{in} = 1.5$	HD3=-36.54 HD5=-48.62	HD3=-35.81 HD5=-47.01

TABLE 6.5 Comparison of theoretic result and behavior simulation of Case C.

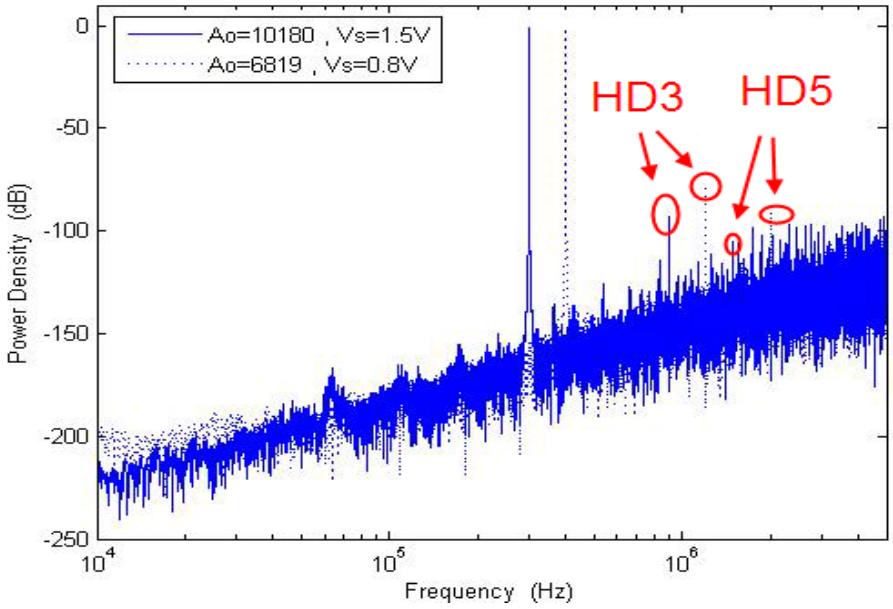


Fig. 6.4 The modulator's output PSD

6.5 Transistor Level Simulation Results

The proposed model serves as a powerful tool for analyzing nonlinear DC-gain distortion for sigma delta modulators. In order to verify the accuracy of our model at transistor level,

the circuit of a general integrator has been realized using classical two-stage architecture in Spice.

The specifications of the op-amp are A_O =80dB, V_{OS} =±1.5V, K_S =1, and the sinusoidal input frequency is 10k. Integrator output FFT is shown in Fig. 6.5. The total harmonic distortion (THD) is mainly determined by the third harmonic distortion (HD3) and the fifth harmonic distortion (HD5). It is indicated in Fig. 6.5 that HD3 and HD5 are -56.9dB and -67.3dB respective, and the HD3 and HD5 generated from our model are -63.9dB and -73.5978dB respective. The theoretical results and simulation results are close, and are listed in TABLE 6.6.

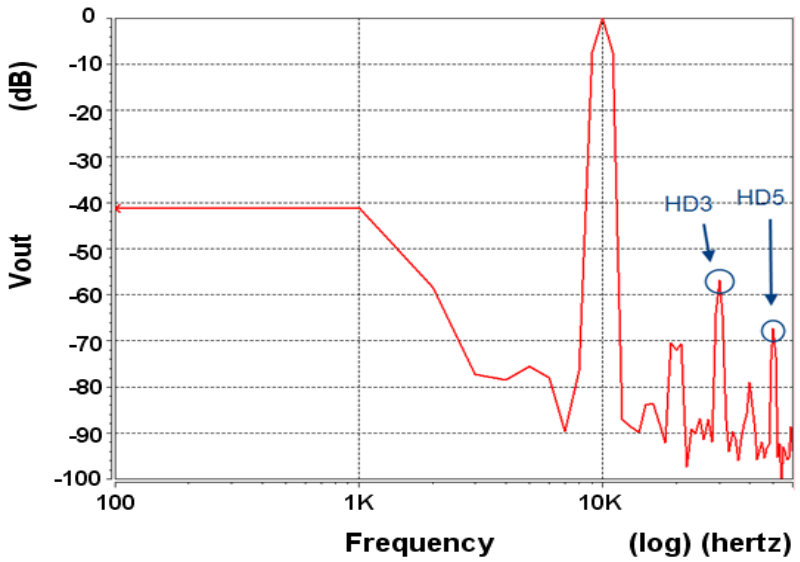


Fig. 6.5 Spice simulation FFT Results with K_S =1, A_O =80dB, V_{OS} =1.5V, and F_{in}=10k

	Theoretic (dB)	Spice simulation (dB)
HD3	-63.9	-56.9
HD5	-73.5978	-67.3

TABLE 6.6 Comparison of theoretic result and Spice simulation

7
THE DESIGN OPTIMIZATION BETWEEN MODEL-BASED AND SIMULATION-BASED

The optimization algorithm design basically searches through the entire parameter space to find a best set of design parameters see as Fig. 7.1 which minimum the Cost Function. By minimum the Cost Function we can increase signal to noise plus distortion ratio (SNDR) (7.1) or dynamic range (DR) and reduce power consumption at the same time. We can know SNDR plays an important role in design optimization.

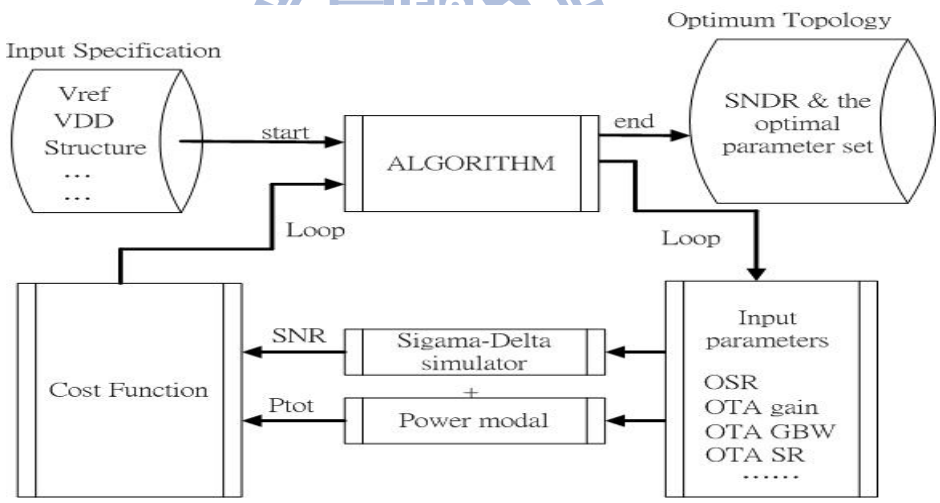


Fig. 7.1 Proposed design optimization for the $\Sigma\Delta$ modulator design

$$SNDR = \frac{P_{signal}}{P_{total\_noise} + P_{total\_distortion}} \tag{7.1}$$

where P_{total_noise} and $P_{total\_distortion}$ are total noise power and total distortion power in SDM

7.1 How to Generate SNDR of Simulation-based SDM Approach and Run OPTIMIZATION

SNDR is an important part in design optimization. To compute SNDR in Simulation-based SDM design optimization, designers should model all SDM noise block for behavior simulation like [9] and then use FFT (Fast Fourier Transform) to simulation data in order to find out whole system power spectral density (PSD) see as Fig. 7.2 and then integrate in band noise power and search harmonic distortion. In Fig. 7.2, we can see the noise and distortion may combine numerous noise and distortion. Designer can not realize which noise or distoertion dominating the system.

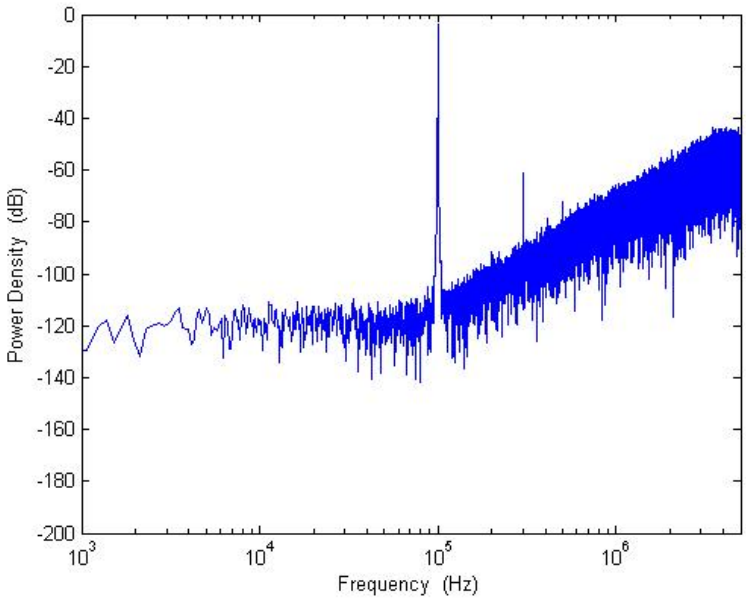


Fig. 7.2 The modulator's output PSD

It is well known a parameter set of SDM behavior simulation may need numerous minute, but the parameter searching space of optimization may have thousands combinations. So it will cause many time to run behavior simulation and find a best parameters combination. Using different algorithm of simulation-based SDM design optimization is the most popular method to overcome simulation time issue. Althought using algorithm could decrease

searching space of optimization, it may cause optimization result not accuracy enough. And designer had no ideal to correct the input parameter after each optimization because simulation-based design optimization can not separate each noise and distortion in PSD or list each noise and distortion power magnitude.

7.2 How to Generate SNDR of Model-based SDM Approach and Run OPTIMIZATION

In this paper, we propose a complete Model-based design optimization approach. In Model-based SDM design, we analyze all major noises and distortions into mathematics model. We can compute each noise and distortion power at SDM output (ex: quantization noise [30], thermal noise [30], jitter noise [1], DC-Gain Distortion [31], settling Distortion [35], etc) and we added each noise and distortion power to represent total noise power (7.2) and total distortion power (7.3) for computing SNDR of Model-based approach.

$$P_{total\_noise} = P_{quantization\_noise} + P_{thermal\_noise} + P_{jitter\_noise} + .. \quad (7.2)$$

$$P_{total\_distortion} = P_{DC-Gain\_distortion} + P_{settling\_distortion} + ... \quad (7.3)$$

And the detail and dependency of these noises we will discuss in next section.

Our model is more time-efficient because our model does not need any behavior simulation. And this approach could list each noise and distortion power magnitude so that designers could depend on their requirement to correct the input parameter after each optimization result.

7.3 Comparisons With These Two Optimization Schemes

7.3.1 Model-based V.S. Simulation-based

Our optimization model includes all principal noise models. Compared with Simulation-based optimization models, our model can list each noise power after each

optimization. Then, designer can easier find out which parameters decrease the SNDR or increase power consumption. Our model can tell designer how to correct the dominating parameters or improve circuit for minimum Cost Function. In our model, designer can know which noise and distortion dominate this system. Base on this result, designer can make devices easier design for relaxing input parameter (ex: op-amp DC-gain and SR) which are not dependent on the dominative noise and distortion. So there are many circuit improvements between resolution and power issues which depend on designer requirement.

7.3.2 Speed

In previous optimization simulations used behavior simulation by different algorithm to do optimization. Because the transient time of behavior simulation depends on system cycles, it may take long time to find the best parameter combination. In this paper, we provide all typical architecture noise, distortion and power models in mathematics, so we do not need any behavior simulation. If our theoretical models are employed to compute SNDR, it takes only 0.17 second. And the transient time of optimization depends on CPU frequency. Compare with a second order SDM with oversampling ratio of 24, sampling frequency of 9.6 MHz in behavior simulation, our model can be hundreds times faster. The results with 1024, 8192 and 16384 cycles are tabulated in TABLE 7.1.

Number Of Cycles	Simulation Time (T)	T/0.17sec
1024	4 min 45sec	1676
8192	35 min 41 sec	12594
16384	1hr 3 min 24 sec	22376

TABLE 7.1 SIMULATION TIMES FOR THE PROPOSED MODELS

8

Design Optimization of Sigma-Delta ADCs Design

8.1 Design Optimization

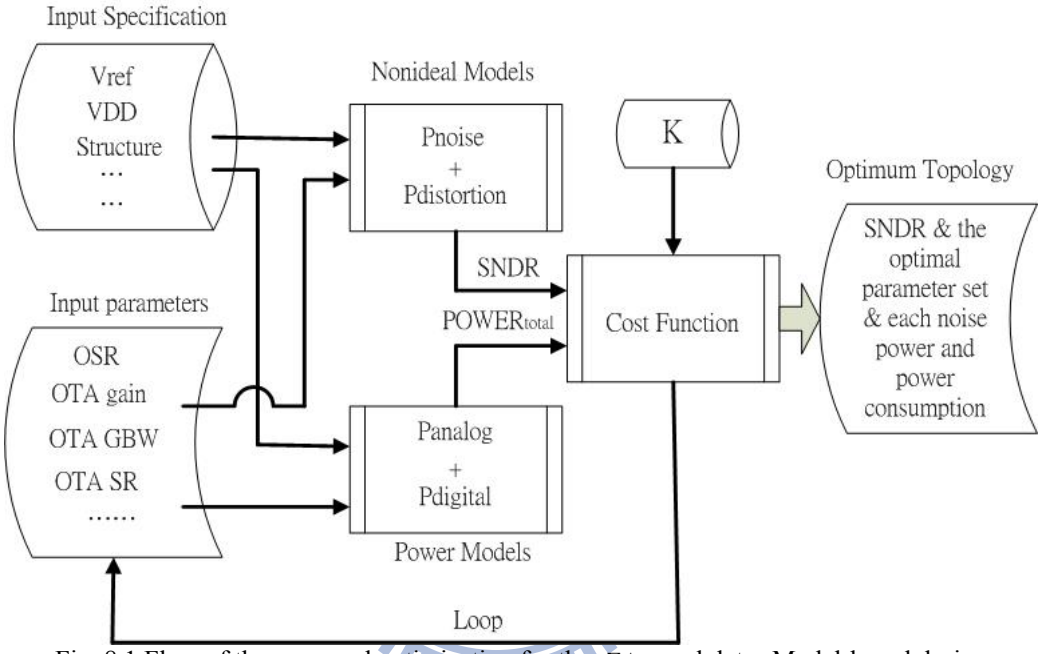


Fig. 8.1 Flow of the proposed optimization for the ΣΔ modulator Model-based design

In section VI, we propose a design optimization flow to help designers reach an optimal design quickly as Fig. 8.1. The input signal bandwidth (Hz) and the output signal *SNDR* (dB) are treated as design specifications. We modify the figure-of-merit (FOM) [36] function by multiplying a variable K to the SNDR term of FOM and inverse it, to become our Cost Function. In Fig. 8.1 the Cost Function is expressed by

$$CF = \left(K \cdot SNDR_{dB} + 10\log\left(\frac{f_B}{POWER_{total}} \right) \right)^{-1} \tag{8.1}$$

$SNDR$ is defined as (7.1). Where P_{total_noise} and $P_{total\_distortion}$ are sum of all major noises and distortions in SDM listed in TABLE 8.1.

P_Q	Quantization noise
P_{AV}	Finite OTA leakage noise
P_{jitt}	Jitter noise
P_{set}	Settling noise
P_{sw}	Switch thermal noise
P_{OTA}	OTA thermal noise
P_{dac}	Multi-bit DAC noise
$HD3_{NFDCG}$	third harmonic distortion of Nonlinear Finite-DC-Gain
$HD5_{NFDCG}$	fifth harmonic distortion of Nonlinear Finite-DC-Gain
$HD2_{DAC}$	Second harmonic distortion of of Nonlinear Capacitance
$HD3_{DAC}$	third harmonic distortion of of Nonlinear Capacitance
$HD4_{DAC}$	fourth harmonic distortion of of Nonlinear Capacitance

TABLE 8.1 The representation of each noise in our models

The constant K serves as the relative weighting between SNDR and $POWER_{total}$. Typically, if we prefer high resolution designs, we set K higher and SNDR plays a more important role than $POWER_{total}$. On the other hand, if we prefer low power designs, we can set K lower. The representation of each parameter in our models is in Table 8.2. The parameters of σ_{cap}, V_{ref} and some circuit device dimensions parameter (ex: μ_n, C_{ox}, etc) depend on the technology, so they are set before the design optimization.

8.2 Design Parameters Discussions

All noise power models discussed in the following are based on the integrator scheme, as shown in Fig. 8.2. In Fig. 8.2, C_u is the unit capacitor whose capacitance is $C_S/2^B$. And the representation of each parameter in our model is shown as TABLE 8.2.

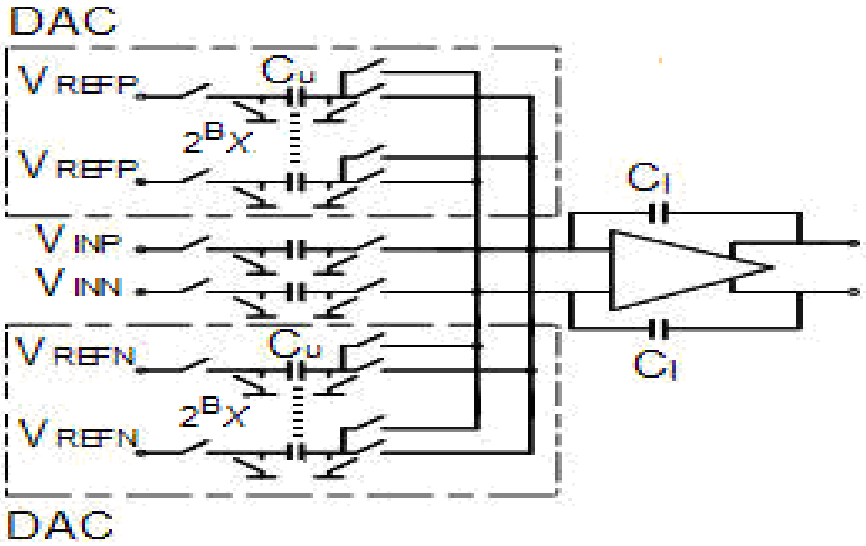


Fig. 8.2 Integrator and the DAC branches

B	Bit number
OSR	Oversampling ratio
C_S	First stage integrator sample capacitance
C_{eq}	Close loop equivalent capacitive load
GBW	Op-amp gain bandwidth
SR	Op-amp gain Slew-Rate
σ_{jit}	standard deviation of clock jitter
R_{Switch}	Switch ON resistance
Vos	Op-amp output swing
A_O	Op-amp DC-gain
A_{in}	Input signal amplitude

TABLE 8.2 The representation of each parameter in our models

	$B\uparrow$	$OSR\uparrow$	$R\uparrow$	$GBW\uparrow$	$C_S\uparrow$	$SR\uparrow$	$\sigma_{cap}\uparrow$	$A_{in}\uparrow$	$V_{OS}\uparrow$	$A_0\uparrow$
P_Q	↓	↓	—	—	—	—	—	—	—	—
P_{AV}	↓	↓	—	—	—	—	—	—	—	↓
P_{dac}	↑	↓	—	—	—	—	↑	—	—	—
P_{jitter}	—	↓	—	—	—	—	—	↑	—	—
P_{sw}	—	↓	—	—	↓	—	—	—	—	—
P_{op}	—	↓	↓	↓	—	—	—	—	—	↓
P_{set}	↓	↑	↑	↓	↑	↓	—	↑	—	—
HD_{NFDCG}	—	↓	—	—	↑	—	—	↑	↓	↓
HD_{DAC}	↑	—	—	—	—	—	↑	↑	—	—

TABLE 8.3 Summary of noise and distortion-power and power-rating when design parameters increase

TABLE 8.3 summarizes the above discussions. Basically we identify *B*, *OSR*, *R*, *GBW*, C_S and *SR* as the optimization process design parameters. TABLE 8.3 shows qualitatively how distortion and power are affected when a particular design parameter increases, and it reveals that the ΣΔ ADC design task is a very complex one.

9
Optimization Simulation Results

In order to demonstrate the accuracy and pfracticability of our method, the two published design cases [3, 37] are compared with our theoretical results in this section. The parameter searching space is specified to be

- OSR : 24 ~ 120
- B : 1 ~ 4
- A_0 : 50dB~90dB
- SR: 100 V/μs ~ 300 V/μs
- GBW : 200 MHz ~ 500 MHz
- A_{in} : 0.4V ~ 1V
- C_S : 1 pF ~ 3 pF

9.1 ΣΔ ADC for ADSL-CO Applications

Compare with the design of [3], the design optimization algorithm uses the same specifications as those in [3]. They are:

- Peak $SNDR$: 78 dB
- Signal bandwidth : 276 kHz

The V_{REF} is set at 1 V for a 1.8 V power supply in 0.18-μm CMOS technology. The matching of capacitor σ_{cap} is set at 0.04% for the MIM capacitance. The results published in [3] and those obtained from our methodology are all listed in Table 9.1, which includes two design optimization results corresponding to K=2 with and without DEM. TABLE 9.2 lists the all noise and distortion power for theoretic calculation. Due to DEM is employed in this case, P_{dac} in TABLE 9.2 is decreased much and DAC distortion is eliminated. We assume DEM power is $0.5\times POW_{digital}$.

circuit parameters	Ref [3]	K=2	K=2 DEM	Unit
B	3	1	3	-
OSR	96	120	120	-
Cs	1.7	1	2	Pf
C_{eq}	7.64	7	8	Pf
A_0	55	80	90	dB
Vos	0.8	0.8	0.8	V
GBW	400	200	200	MHz
SR	500	100	100	V/μs
R_{Switch}	300	300	300	Ω
σ_{jit}	9	9	9	Ps
A_{in} at peak SNDR	0.75	1	1	V
n	2	2	2	-
SNDR [3]	78	-	-	dB
Our model SNR	79.19	88.2269	101.406	dB
Our model SNDR	76.5158	86.3616	101.317	dB
$SNDR$ (SIMULINK)	76.65	87.59	99.8	dB
Our model POW_{total}	39.22	7.198	13.8	mW

TABLE 9.1 Comparisons of our design results with those in [3]

Nonlinearities Power	Ref [3]	K=2	K=2 DEM	Unit
P_Q	-109.05	-101.85	-113.89	dB
P_{AV}	-135.14	-151	-173.04	dB
P_{sw}	-96.926	-95.590	-98.601	dB
P_{jit}	-130.28	-128.75	-128.75	dB
P_{op}	-116.29	-127.45	-135.46	dB
P_{set}	-155.63	-127.38	-174.24	dB
P_{dac}	-78.75	-85.74	-116.13	dB
$HD3_{NFDCG}$	-89.890	-105.57	-115.45	dB
$HD5_{NFDCG}$	-103.7	-117.83	-127.73	dB
$HD2_{DAC}$	-80.095	-88.308	-	dB
$HD3_{DAC}$	-91.751	-99.807	-	dB
$HD4_{DAC}$	-105.98	-113.88	-	dB

TABLE 9.2 The corresponding noise powers for the design parameters listed in TABLE 9.1

Discussion:

1. According to TABLE 9.2, we can know three bits SDM without DEM may cause severe DAC noise (-78 dB) and DAC distortion (-80 dB). And these dominative noise and distortion also cause whole system SNDR scale-down. Due to DAC noise and distortion are major dependent of bit number and OSR, so the result of our optimization design K=2 without DEM decreases bit number and increases OSR to make lower DAC noise (-85.74 dB), distortion (-88 dB) and higher SNDR (86.36 dB). The other way is adding DEM circuit to SDM, it is well known DEM circuit can make DAC noise decreased and DAC distortion eliminated. So the SNDR of our optimization design K=2 with DEM can reach about 101.317 dB. In design of [3] case, we offer two different ways to designer to increase system resolution.

2. Due to DAC noise and distortion are major dependent of bit number and OSR. Some input parameters do not need so tough like GBW and SR. If GBW and SR set too high, the op-amp can consume too much power. So the result of our optimization design K=2 without DEM relax GBW and SR to save power consumption from 39.22mw to 7.198mw. Although settling noise may be increasing about -127.38 dB for relaxing GBW and SR. Compare with DAC noise (-85.74 dB) and distortion (-88 dB), the increasing settling noise is still not be an important role of SNDR. It is well known DEM circuit may also consume more power. Our optimization design K=2 with DEM list that the total power consumption is 13.8mw. It is higher than our model K=2 without DEM, but lower than [3]. So designer could relax GBW and SR, and then add DEM circuit for higher resolution and lower power.

9.2 ΣΔ ADC for 14-bit 2.2-MS/s

Compare with the design of [37], the design optimization algorithm uses the same specifications as those in [37]. They are:

- Peak *SNDR* : 72 dB
- Signal bandwidth : 500 kHz

The results published in [37] and those obtained from our methodology are all listed in TABLE 9.3, which includes two design optimization results corresponding to K=0.5 without DEM and K=10 with DEM. TABLE 9.4 lists the all noise and distortion power for theoretic calculation.

circuit parameters	Ref [37]	K=0.5	K=0.01 DEM	Unit
B	5	1	1	-
OSR	24	120	24	-
Cs	1.32	1	1	Pf
C_{eq}	7.2376	7	7	Pf
A_0	58	80	80	dB
Vos	0.8	0.8	0.8	V
GBW	1000	200	200	MHz
SR	475	100	100	V/μs
R_{Switch}	100	300	300	Ω
σ_{jit}	9	9	9	Ps
A_{in} at peak SNDR	0.55	1	0.9	V
n	2-2	2-2	2-2	-
SNDR [37]	72	-	-	dB
Our model SNR	76.237	88.32	90.361	dB
Our model SNDR	76	86.4233	89.644	dB
SNDR (SIMULINK)	77.7	87.83	88.87	dB
Our model POW_{total}	207.615	21.6784	19.6878	mW

TABLE 9.3 Comparisons of our design results with those in [37]

Nonlinearities Power	Ref [37]	K=0.5	K=0.01 DEM	Unit
P_Q	-128.864	-167.68	-104.78	dB
P_{AV}	-168.111	-214.95	-166.02	dB
P_{sw}	-89.8069	-95.59	-88.601	dB
P_{jit}	-126.957	-128.75	-122.67	dB
P_{op}	-110.67	-127.45	-120.46	dB
P_{set}	-230	-127.38	-358.86	dB
P_{dac}	-78.75	-85.74	-101.18	dB
$HD3_{NFDCG}$	-92.0368	-105.57	-95.94	dB
$HD5_{NFDCG}$	-108.601	-117.83	-108.95	dB
$HD2_{DAC}$	-97.478	-88.308	-	dB
$HD3_{DAC}$	-114.404	-99.807	-	dB
$HD4_{DAC}$	-133.885	-113.88	-	dB

TABLE 9.4 The corresponding noise powers for the design parameters listed in TABLE 9.3

Discussion:

1. Compare with the design of [37]. The result of our optimization is almost the same as previous discussion, but we use different weighting value K in this application. We prefer low power design at K=0.01 with DEM, so we can see that the total consumption power is 19.6878 mw lower than the other two case without DEM.

10
Conclusions and Future Works

In order to increase the speed of circuit design for ΣΔ ADCs, this paper offers an efficient optimization method to obtain the most suitable circuit specifications. All the nonlinearity power also can be obtained after a complete optimization, and the dominating nonlinearity power can be reduced by adjusting the design specifications. Our proposed method has acceptable accuracy and nice speed, and the flexibility can be enhanced by building more nonlinearity models for different circuit structures.

Further, in order to reduce the time-cost for optimization, the algorithm efficiently search the entire design parameters space to find the parameter set which satisfies the specifications must to be established.

References

[1] B. E. Boser and B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1298-1308, Dec. 1988.

[2] S. R. Norsworthy, I. G. Post and H. S. Fetterman, "A 14-bit 80-kHz Sigma-Delta A/D Converter: Modeling, Design, and Performance Evaluation," *IEEE J. Solid-State Circuits*, vol. 24, pp. 256-266, April. 1989.

[3] R. Gaggl, A. Wiesbauer, G. Fritz, C. Schranze, P. Pessel, "A 85-dB Dynamic Range Multibit Delta-Sigma ADC for ADSL-CO Applications in 0.18-μm CMOS," *IEEE J. Solid-State Circuit*s, vol. 38, pp. 1105-1114, Jul. 2003.

[4] R. d. Rio, J. M. Rosa, B. P. Verdu, et al, "Highly Linear 2.5-V CMOS $\Delta\Sigma$ Modulator for ADSL+," *IEEE Trans. Circuits Syst. I*, vol. 51, pp. 47–62, Jan. 2004.

[5] O. Oliaei, P. Clément and P. Gorisse, "A 5-mW Sigma–Delta Modulator with 84-dB Dynamic Range for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 37, pp. 2-10, Jan. 2002.

[6] K. Vleugels, S. Rabii and B. Wooley, "A 2.5-V Sigma-Delta Modulator for Broadband Communication Applications," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1887-1899, Dec. 2001.

[7] J. Grilo, I. Galton, K. Wang and G. Montemayor, "A 12-mW ADC Delta-Sigma Modulator With 80dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," *IEEE J. Solid-State Circuits*, vol. 37, pp. 271-278, March 2002.

[8] R. Miller and S. Petrie, "A Multibit Sigma-Delta ADC for Multimode Receivers," *IEEE J. Solid-State Circuits*, vol. 38, pp. 475-482, March 2003.

[9] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *IEEE Trans. Circuits Syst. I*, vol. 50, pp. 352-364, March 2003.

[10]國立交通大學電機與控制工程研究所, C. H. Chung, "Optimization Designs of Sigma-Delta ADCs via Nonideality and Power Analyses", Jun, 2005.

[11]A. Mahmoodi and D. Joseph, “Optimization of Delta-Sigma ADC for Column-Level Data Conversion in CMOS Image Sensors,” IEEE Instrumentation and Measurement Technology Conference Proceedings, pp.1-6, May. 2007.

[12]M. Webb, Hua Tang, “Analog Design Retargeting by Design Knowledge Reuse and Circuit Synthesis**,”** IEEE International Midwest Symposium on Circuits and Systems, pp.892-895, May 2008.

[13]H. Zare-Hoseini and L. Kale, “On the Effects of Finite and Nonlinear DC-Gain of the Amplifiers in Switched-Capacitor ΔΣ Modulators,” IEEE International Symposium on Circuits and Systems, Vol.3, pp.2547-2550, May 2005.

[14]A. Banerjee, S. Chatterjee, A. Patra and S. Mukhopadhyay, ”An Efficient Approach to Model Distortion in Weakly Nonlinear Gm-C Filters,” IEEE International Symposium on Circuits and Systems, pp.1312-1315, May 2008.

[15]Y. Geerts, WMC. Sansen, “Design of multi-bit Delta-Sigma A/D converters,” Kluwer Academic Publishers, 2002

[16]K. Franchen and G. G. E. Gielen, “A High-Level Simulation and Synthesis Environment for ΣΔ Modulators,” *IEEE Trans. Comput.-Aided Des. Integr. Circuit Syst.*, vol. 22, no 8, pp. 1049-1061, Aug. 2003.

[17]J. Ruiz-Amaya, J. M. de la Rosa, F. V. Fernandez, F. Medeiro, R. del Rio, B. Perez-Verdu, and A. Rodriguez-Vazquez, “High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time ΣΔ Modulators Using SIMULINK-Based Time-Domain Behavioral Models,” *IEEE Trans. on Circuit and Systems*, vol. 52, no. 9, pp. 1795-1810, Sep. 2005.

[18]D. A. Johns and K. Martin, *Analog Integrated Circuit Design.* John Wiley & Sons, Inc., 1997.

[19]S. D. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters–Theory, Design, and Simulation*. Piscataway, NJ：IEEE Press, 1997.

[20]B. Razavi, *Design of Analog CMOS Integrated Circuit,* McGraw-Hill series in electrical and Computer engineering, McGraw-Hill, 2001.

[21]S. B. Nerurkar, K. H. Abed, R. E. Siferd, V. Venugopal, “Low power sigma delta decimation filter,” in *Proc.*

IEEE Int. Symp. Circuits and Systems, vol. 1, pp. 647-650, Aug. 2002.

[22]K. Y. F. Mok, A. G. Constantinides, P. Y. K. Cheung, "A VLSI decimation filter for sigma-delta A/D Converters," in *Proc. IEEE Int. Conf. Advanced A-D and D-A Conversion Techniques and their Applications*, pp. 36-41, Jul 1994.

[23]Chao, S. Nadeem, W. Lee, and C. Sodini, "A Higher Order Topology for Interpolative Modulators for Oversampling A/D Converters," *IEEE Trans. Circuits Syst.*, Vol. 37, No 3, pp. 309–318, March 1990.

[24]V. Peluso, M. Steyaert and W. M. C. Sansen, *Design of low-voltage low-power CMOS delta sigma A/D Converters*, Kluwer Academic Publishers, 1999.

[25]M. Rebeschini, N. R. Van Bavel, P. Rakers, R. Greene, J. Caldwell, and J. R. Haug, "A 16-b 160-kHz CMOS A/D Converter Using Sigma-Delta Modulation," *IEEE J. Solid-State Circuit,* vol. 25, pp. 431-440, April 1990.

[26]Van de Plassche, R. J. and Goedhart, D., "A monolithic 14-bit D/A converter," *IEEE J. Solid-State Circuits*, pp. 552–556, January 1997.

[27]Carley, L. R., "A noise-shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, pp. 267–273, April 1989.

[28]Chen, F. and Leng, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, pp. 453–460, April 1995.

[29]Baird, R. T. and Fiez, T. S., "Linearity enhancement of multibit A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II,* vol. 42, pp. 753–762, December 1995.

[30]F. Medeiro, A. P. Verdu, A. R. Vazquez, *Top-Down Design of High Performance Sigma-Delta Modulators.* Kluwer academic publishers, 1999.

[31]F. C. Chen and C. L Hsieh, " Modeling Harmonic Distortions Caused by Nonlinear Op-Amp DC-Gain for Switched-Capacitor Sigma-Delta Modulators," *IEEE Transactions on Circuits and Systems II*, 2009

[32]M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching Properties of MOS Transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1439, Oct. 1989.

[33]K. Abdelfattah, B. Razavi, "Modeling Op Amp Nonlinearity in Switched-Capacitor Sigma-Delta

Modulators,"IEEE Custom Integrated Circuits Conference (CICC), 2006

[34]H. Zare-Hoseini, I. Kale, and O. Shoaei, ”Modeling of Switched-Capacitor Delta-Sigma Modulators in SIMULINK,” *IEEE Trans. on instrumentation and measurement*. Vol. 54, Issue 4, pp.1646-1654, Aug 2005.

[35]F. Medeiro, B. Perez-Verdu, A. Rodriguez-Vazquez and J. L. Huertas, “Modeling OpAmp-Induced Harmonic Distortion for Switched-Capacitor sigma-delta Modulator Design,” in Proceedings of IEEE ISCAS, vol. 5, 1994, pp. 445-448

[36]R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters,* IEEE Press, A JOHN WILEY & SONS, INC, Publication, 2005.

[37]J.C. Morizio, I.M. Hoke, et al, ” 14-bit 2.2-MS/s sigma-delta ADCapos;s,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 968–976, Jul. 2000