國 立 交 通 大 學

電機與控制工程學系

碩 士 論 文

混合訊號前端積體電路應用於可攜式生醫訊號擷取系統

A CMOS Mixed-Signal Front-End IC for Portable Biopotential Acquisition System

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中華民國 九十八 年 六 月

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中文摘要

在人體所有的生理訊號中，其訊號振幅皆非常微弱，亦容易被受測者本身、量測環境及設備等因素所影響，故本論文提出適用於各種電生理訊號擷取之晶片設計。除了一般著重的低功率、低雜訊之外，同時提高共模訊號拒斥比(CMRR)與電源漣波拒斥比(PSRR)，並將整體多通道前端電路整合實現在單一晶片上，不需要任何外接元件，除了兼具成本與晶片面積效益，亦可降低因複雜的接線對生理訊號在量測時所造成的干擾，使後端處理及分析的訊號品質能夠更為精確。另外，在系統加入了數位控制介面，根據不同生理訊號的需求，利用數位訊號去控制選擇所要的訊號放大倍率與系統頻寬。

本論文所設計的生理訊號擷取晶片包含：截波穩定式儀表放大器(CHS-IA)、類比多工器、切換式電容低通濾波器(SC-LPF)、非重疊時脈產生器(Non-Overlapping Clock Generator) 、切換電容式可變增益訊號放大器(SC-VGA)及多級雜訊移頻三角積分類比/數位轉換器(MASH 2-1-1 tri-level ΣΔ ADC)等電路。整個電路設計使用 TSMC 0.18μm CMOS 1P6M 製程技術來實現，而整體晶片面積為 1.9198 × 1.9198 mm^2。由模擬結果顯示，在頻率 1024Hz 下，可獲得訊雜比 90 dB，16 位元解析度的效能。在操作電壓 1.8V 下，總消耗功率約 998μA。

關鍵字：生理訊號，腦電圖，截波穩定式儀表放大器，切換式電容低通濾波器，切換電容式可變增益訊號放大器，多級雜訊移頻三角積分類比/數位轉換器。

A CMOS Mixed-Signal Front-End IC for Portable Biopotential Acquisition System

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Abstract

Due to properties of low-amplitude and non-stationary, most of biomedical signals are easily influenced by examined persons, measured environment, and electronic devices. A novel analog circuit design is proposed in this thesis, which is suitable for various biomedical signal acquisitions. In addition to the consideration of low power and low noise, the multi-channel mixed-signal front-end integrated circuit (MSFEIC) is designed. This circuit is realized into a single chip without any external component. It can not only reduce the number of outer components, but also enhance a better signal-to-noise ratio enormously. In addition, to select system gain and bandwidth corresponding to different amplitude and frequency of biomedical signals, the controllable digital interface is also designed and integrated into MSFEIC.

In this thesis, MSFEIC design is composed of four chopper-stabilized instrumentation amplifiers (CHS-IA), a switched-capacitor variable gain amplifier (SC-VGA), a switched-capacitor low-pass filter (SC-LPF), a non-overlapping clock generator, and a cascaded 2-1-1 tri-level sigma-delta analog-to-digital converter (MASH 2-1-1 tri-level ΣΔ ADC). These circuits have been integrated into a single

chip of the total area of 1.9198×1.9198mm^2 by using TSMC 0.18μm CMOS Mixed-Signal RF General purpose MiM Al 1P6M 1.8&3.3V process. For the simulation results, the proposed chip can achieve 90 dB of SNR, 16-bit resolution at 1024Hz. The total power consumption is about 998μW under 1.8V supply.

Keyword: Biomedical signal, chopper-stabilized instrumentation amplifier(CHS-IA), switched-capacitor low-pass filter (SC-LPF), switched-capacitor variable gain amplifier (SC-VGA), MASH 2-1-1 tri-level ΣΔ ADC.

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Chapter 1 Introduction

1.1 Background

The medical application of science and microelectronic technology recently has made significantly advances, thus improving human quality of life. Biomedical instruments are crucial in modern life. The biomedical signal acquisition instrument has already developed years ago. However, the amplitude of the biomedical signals is all very weak. Biomedical signals are very easy to be influenced by testing environment and biomedical signals of the person who examined. These effects make recording biomedical signals become more and more difficult. Among them, the interferences of the testing environment are including the temperature and humidity of the electronic components, capacity effect of the pads, power supply variation, electromagnetic wave, digital noise, etc. The interferences of the biomedical signals are including electroencephalogram (EEG), electro-oculogram (EOG), electromyography (EMG), electrocardiogram (ECG), respiration, perspiration, etc. Therefore, we should amplify measured biomedical signals effectively and restrain noise by an analog front-end (AFE) circuit.

By a mixed-signal front-end (MSFE) circuit, the processed biomedical signals input a digital signal processor (DSP) and analyzed. Amplifying the measured signals and restraining noise play important parts of the biomedical signal acquisition system. Fig. 1-1 shows the typical setup for an EEG recording system which comprises the instrumentation amplifier (IA) as analog front-end (AFE), the programmable gain amplifier (PGA) for boosting the acquired EEG signal to levels for further analog signal processing [1]. Hence, the specification of analog front-end circuit affects the performance of the system directly.

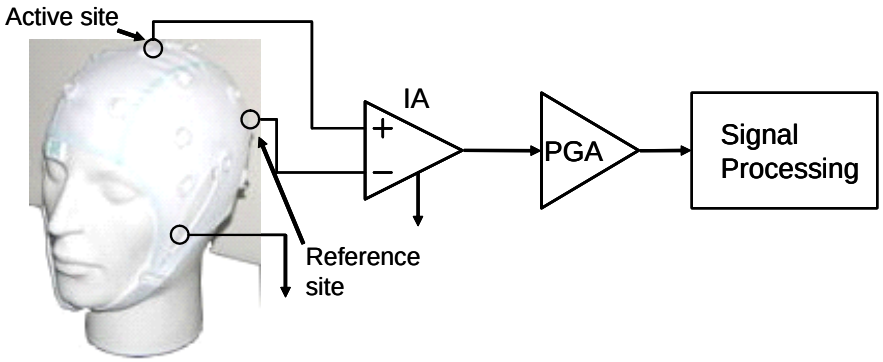


Fig. 1-1 Typical setup for EEG recording

The instrumentation amplifier [2][3][4][5] has already been used in the analog front-end circuit of the biomedical signals recording system widely. The greatest advantages are effective restraining noise such factors as the measuring environment, electrical electrode, etc. and amplifying the weak biomedical signals to observable signals. Therefore, noise interference cannot lead to the signals distortion. Since all biomedical signals are low frequency signals, and the frequency of the noise is usually higher than the biomedical signals, the circuit in this study has a low-pass filter after an instrumentation amplifier. The low-pass filter goes one step future to get rid of noise [5][6][7] to assure the quality of the signals.

This research is the first stage in the biomedical signal acquisition and analysis system, so the performance of gain and restraining noise is extremely important. Its result will influence the efficiency of the whole system. The first generation analog front-end circuit of the biomedical signal recording system has been developed in our laboratory, and has already been accepted by 2008 IEEE International Symposium on Circuits and Systems [8]. This research direction and achievement are received the affirmation by the international academia. We will be devoted to this future development of the research base on the research results.

1.2 Motivation

Medical treatment progresses more and more in recent years. Besides improving the medical technology that has already had, gradually paying attention to the important representative information of biomedical signals is sent out from our body each position. Examine and analyze these biomedical signals can go a step future to find out about the state of the body.

Giving an example of EEG, analyzing the potential signal of human brain is researched from Berger. Proposed in 1920. EEG is produced by many accumulated current of nerve cells under cerebral cortex. Through the research of decades, we can learn the state of mind of the persons who are examined EEG from the measured results [9][10]. Nevertheless, complicated EEG signals can be few processed to study. Computer operation is faster and faster in speed and the algorithms are progressing excellently in recent years, so processing measured EEG signals is enough for real-time. People pay attention to the discussion of human spiritual information gradually. The traditional EEG recording system is shown in Fig. 1-2. This system is composed of an international 10-20 electrode placement system as Fig. 1-3, a biomedical signal amplifier, an analog-to-digital converter (ADC), and a computer. Because the instrument of recording and analyzing is very bulky, it is very inconvenient to use. The difficult problems of reducing systematic volume and simplifying difficulty use of the system should be overcome.

Fig. 1-2 Traditional EEG recording system

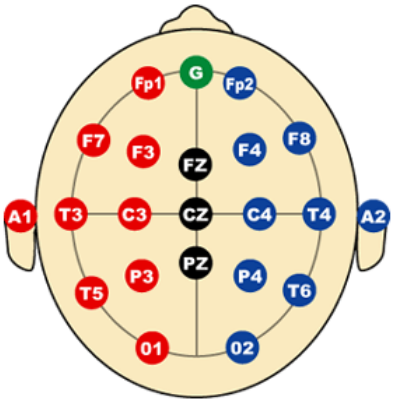
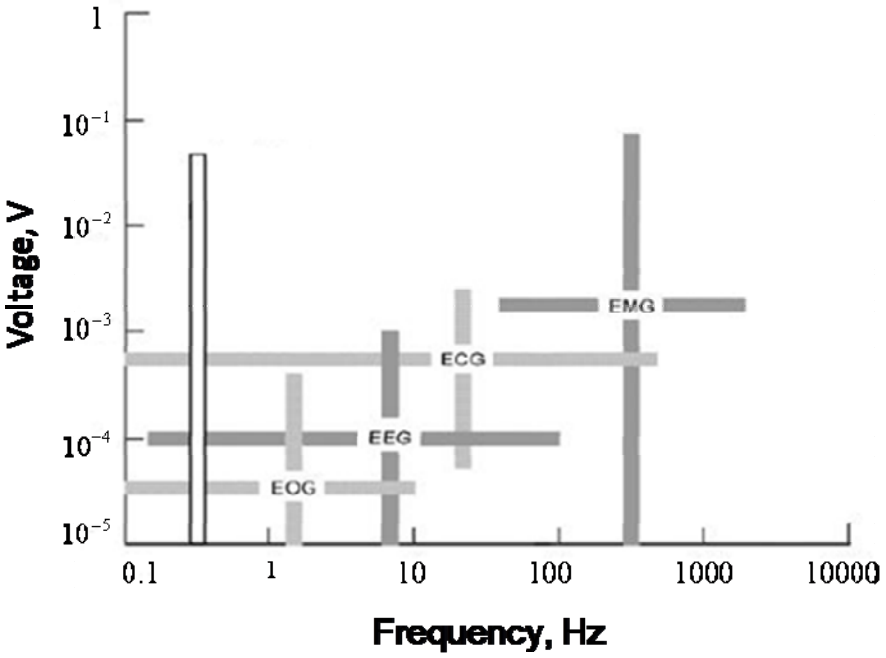


Fig. 1-3 International 10-20 electrode placement system

Generally, the commonly used biomedical signals of body have the characteristics illustrated in Fig. 1-4 and Table 1-1, including EEG, EOG, EMG, and ECG. Biomedical signals are all distributed over ultra-low amplitude and ultra-low frequency, so they are hard to process. For this reason, how to receive and amplify the real biomedical signals that are not distortion is an important issue in this study. Its frequency or amplitude is not a constant value even if it is the same kind of biomedical signals. So the signals must have different bandwidth and different voltage gain.



• Fig. 1-4 Biomedical signals: amplitude/frequency range

Table 1-1 The characteristics of biomedical signals

Biomedical signal	Amplitude distribution	Frequency distribution
EEG	1μV~100μV	DC~150Hz
ECG	100μV~10mV	0.01Hz~250Hz
EOG	10μV~10mV	DC~100Hz
EMG	10μV~10mV	20Hz~1kHz

Furthermore, the use of very large scale integrated circuits (VLSI) dominates medical electronics applications, which range from small, battery-powered electronic implants to room-filling diagnostic imaging systems [11]. As in other VLSI applications, the design and processing of the technology chosen for medical devices depends on the specific applications involved. Product complexity, size, sales volume, cost objectives, and available power source all play significant roles in the specific process [12]. The fabrication of VLSI may be based on the bipolar, CMOS or BiCMOS technologies. However, portable instruments and implantable products, where low power consumption is a necessity, primarily use CMOS devices. CMOS technology has become popular in the last few years for implementing complex circuits and systems. The integration of the AFE circuit and other processing units on the same chip has brought a new era in biomedical systems [13][14][15]. The cost of electronic instruments is proportional to their size, the number of devices and interconnections they contain. VLSI circuits have done a great deal to reduce size, components, and interconnections, and thus the cost of the products that contain them.

This study realized an AFE circuit design which is suitable for a portable biomedical signals recording system [2][16][17][18]. It combines the System-on-Chip (SoC) and needs no external components. It reduced the area and cost of the circuit effectively, in order to combine with DSP in the future. This study expanded the applications of the circuit. In addition, it has joined the digital controlling interface in the circuit. The user can choose the proper gain and bandwidth according to different characteristics of biomedical signals. The MSFE circuit can amplify biomedical signals to the range that can be observed and filter out the noise besides the bandwidth of biomedical signals. Consequently, the systematic structure could measure many kinds of biomedical signals.

1.3 Thesis Organization

The thesis is organized as follows. Chapter 2 describes the development of analog front end circuit for biomedical signal acquisition. Descriptions of MSFEIC design are in Chapter 3. Then the circuit performance and testing platform are presented in Chapter 4. Finally, a summary of this thesis research and future work is briefly concluded by Chapter 5.

Chapter 2

Architecture Survey

2.1 A CMOS IC for portable EEG acquisition systems

Rui Martins et al[2]. proposed a CMOS IC for portable EEG acquisition systems in 1998.Besides low power, the key design points are high common mode rejection ratio (CMRR) and very low noise. Minimum component count is also important to reduce system weight and volume. The system includes 16 instrumentation amplifiers, one 16-to-1 analog multiplexer, a microprocessor compatible digital interface, and an internal current/voltage reference source as shown in the block diagram of Fig. 2-1.

The basic functional block diagram of current feedback amplifiers is presented in Fig. 2-2. Analyzing the input branch of this figure, we conclude that high input impedance is guaranteed by two unity gain buffers. Utilizing the current feedback, by the ratio of input impedance and output impedance to determine voltage gain, and reach high CMRR.

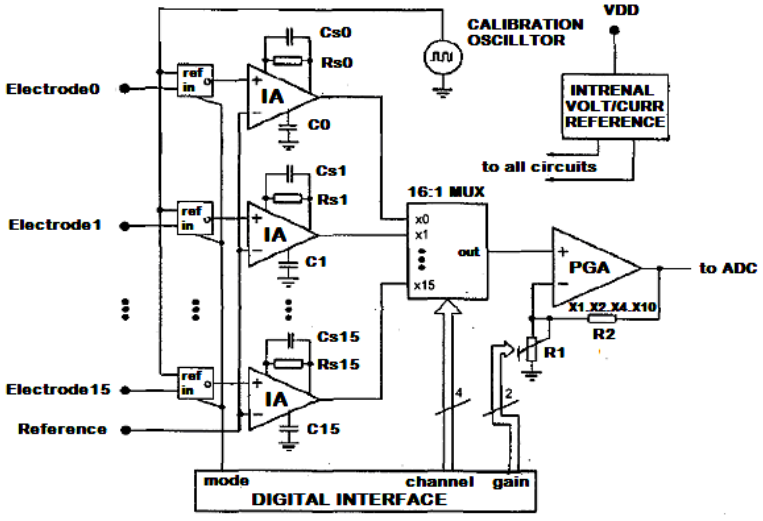


Fig. 2-1 IC block diagram [2]

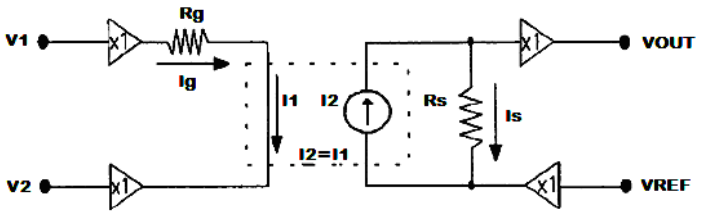


Fig. 2-2 Block diagram of an IA with current feedback [2]

Design the concept as the (2-1).

$$v_{out} = \frac{R_s}{R_g} \cdot (v_1 - v_2) + v_{ref} \tag{2-1}$$

But it is important to note that, contrary to the classical configuration with three operational amplifiers, there is no global feedback (from the output to the input) and that there is only one high impedance node, which simplifies the frequency compensation. Another advantage is the CMRR do not depend on any matching of resistor values. The resistor count is also reduced, saving chip area.

They implemented a CMOS variation of [19], as with this configuration only a reduced number of stacked transistors is necessary (improving dc behavior at low voltage power supply) and only two transistors at input are needed. Also, as PMOS transistors exhibit low flicker noise for the same area, we chose them to the input as shown in Fig. 2-3.

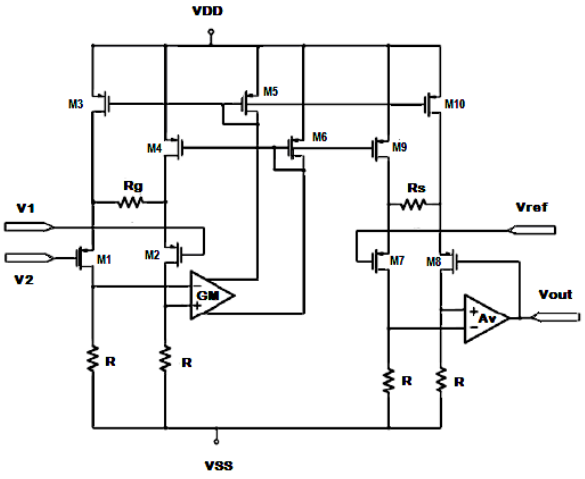


Fig. 2-3 Simplified IA circuit [2]

In order to realize high pass filter function, it was implemented using another feedback loop around the output circuit, as shown in Fig. 2-4. The complete circuit of the IA is shown in Fig. 2-5.

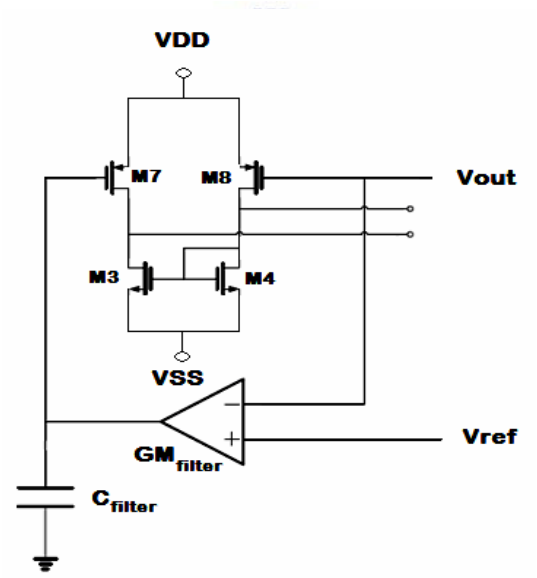


Fig. 2-4 Feedback look realizing the high pass filter function [2]

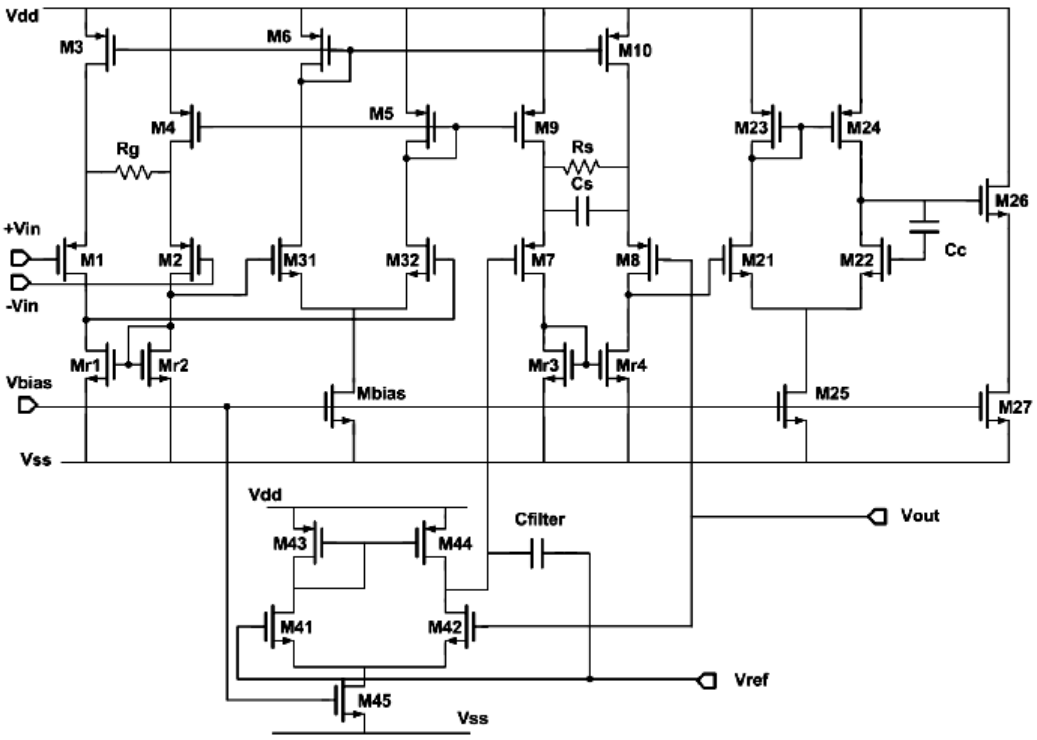


Fig. 2-5 Complete circuit of the IA [2]

2.2 A CMOS analog front-end (AFE) IC for portable EEG/ECG monitoring applications

K. A. Ng and P. K. Chan proposed a CMOS analog front-end (AFE) IC for portable EEG/ECG monitoring applications in 2005[20]. The proposed AFE system chip is shown in Fig. 2-6. A promising approach is the differential difference amplifier (DDA) based non-inverting IA [21][22], which has favorable properties such as simplicity and acceptable low power dissipation. Fig. 2-7 shows the basic DDA non-inverting amplifier.

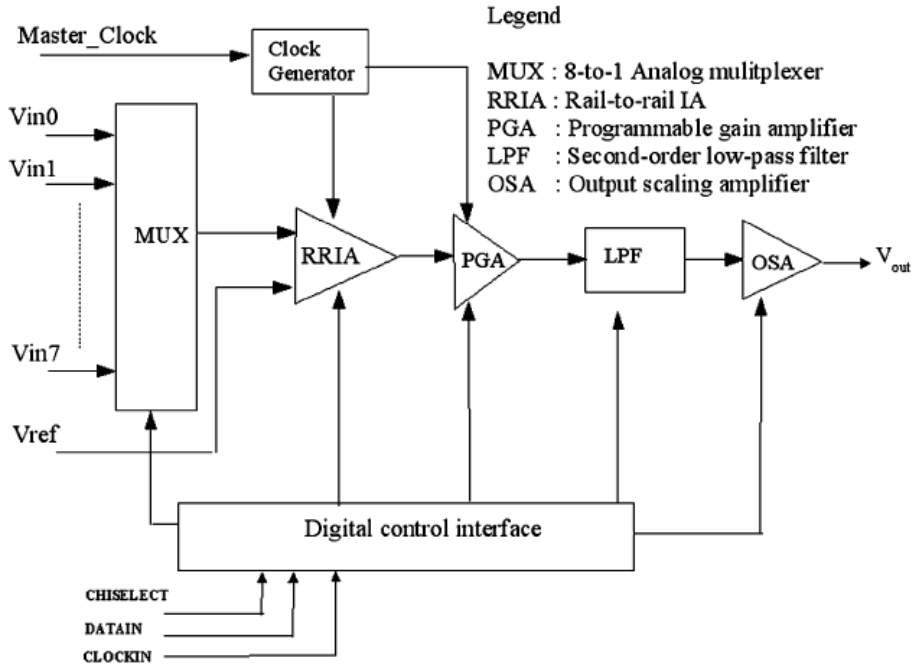


Fig. 2-6 System block diagram of the proposed AFE IC [20]

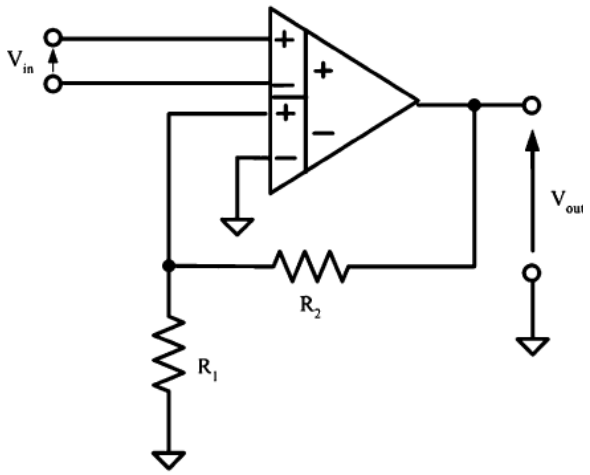


Fig. 2-7 Non-inverting DDA for use an IA [20]

The input and output relation of non-inverting DDA is defined as (2-2). The major advantage of the DDA non-inverting amplifier over the typical IA is it requires an active amplifier and two resistors to set the instrumentation gain. In this DDA-based design, the CMRR is related to the mismatch of the input ports. Mismatch between resistors R_1 and R_2 only affects the gain factor, but it does not degrade the CMRR of the amplifier.

$$V_{out} = V_{in} \times \left(\frac{R_2}{R_1} + 1 \right) \tag{2-2}$$

Fig. 2-8 is a circuit schematic of the PMOS differential-input chopper-stabilized differential difference amplifier (CHSDDA). It joined a chopper-stabilized skill in the circuit to reduce flicker noise and DC offset voltage.

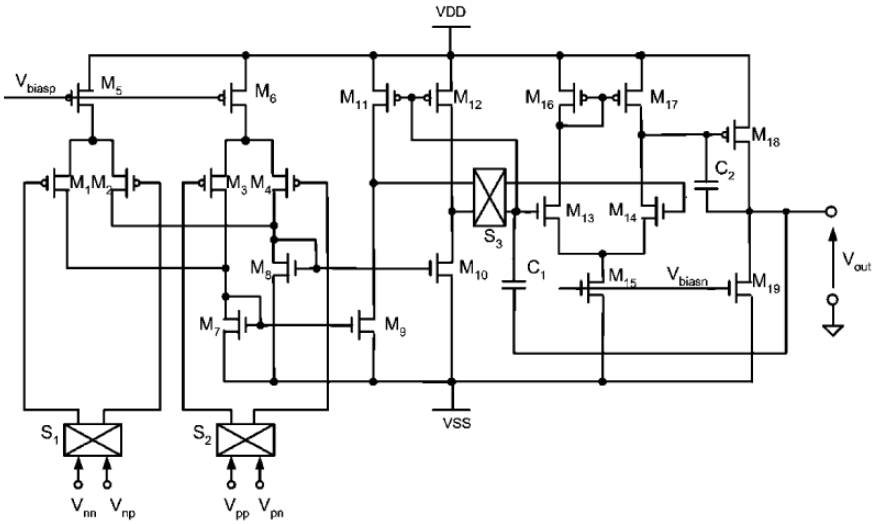


Fig. 2-8 Circuit schematic of the PMOS CHSDDA [20]

A new rail-to-rail input IA is proposed in Fig. 2-9, which shows the filtering circuits added to the basic chopper-stabilized DDA non-inverting amplifier for suppressing this input DC offset voltage. In this realization, two CHSDDAs are arranged in parallel configuration. Input pairs are NMOS and PMOS separately, guarantee to normal running of the circuit in any input common mode voltage. In addition, the circuit added an external RC band pass filter to eliminate noise outside the frequency bandwidth of biomedical signals.

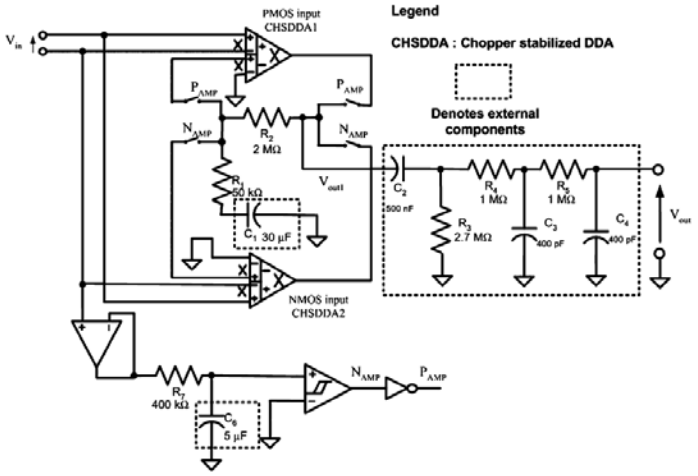


Fig. 2-9 Proposed rail-to-rail IA [20]

Fig. 2-10 shows the conceptual circuit block diagram of the chopper-stabilized DDA circuit. The two pairs of input differential voltage signals are modulated concurrently and translated to the current signals via the trans-conductance cells having identical trans-conductance gain of *Gm*.

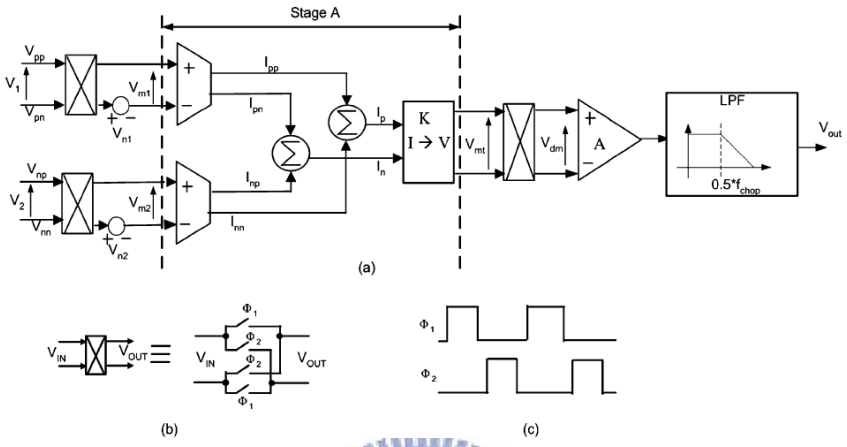


Fig. 2-10 CHSDDA and its associated clock for the chopping switches [20]

Because the chopper-stabilized circuit utilizes clock to control the switches, it could produce the high frequency noise. In order to reduce the influence, it must join a low pass filter used to except the switch noise.

The programmable gain amplifier (PGA) provides further amplification with respect to the output of the rail-to-rail IA. To prevent the input impedance of the amplifier from loading the band pass filter output of the rail-to-rail IA, a non-inverting configuration is used. Note that the first chopper-stabilized stage inside the PGA is derived from the CHSDDA by just removing one input differential port. By digitally connecting the resistors via CMOS switches, the amplifier provides programmable voltage gain.

2.3 Low-power Low-noise 8-channel EEG front-end ASIC for Ambulatory Acquisition Systems

Refet Firat Yazicioglu et al. proposed low-power low-noise 8-channel EEG front-end ASIC for ambulatory acquisition systems in 2006 [16]. Fig. 2-11 shows the architecture of the implemented 8-channel EEG readout front-end ASIC. Each channel of the ASIC consists of an instrumentation amplifier (IA), a spike filter (SF), a fixed gain stage, a variable gain amplifier (VGA) stage, and a channel buffer.

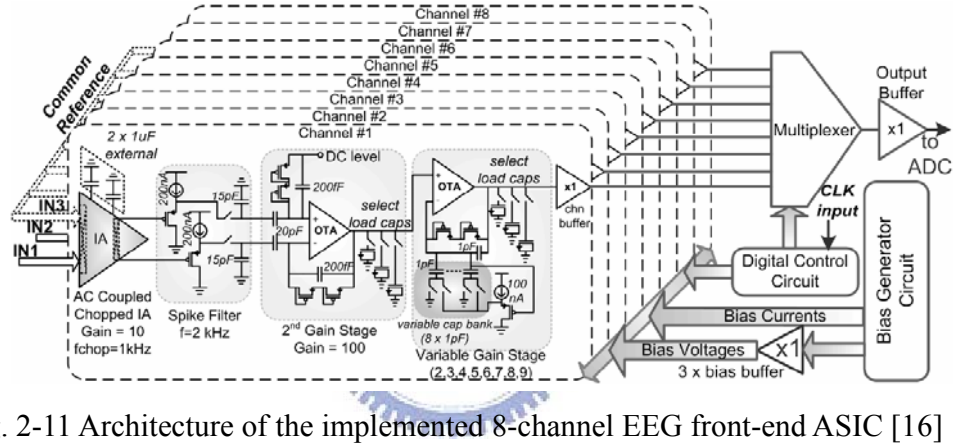


Fig. 2-11 Architecture of the implemented 8-channel EEG front-end ASIC [16]

The IA defines the noise level and CMRR of the channel, and filters the electrode offset. The second gain stage further amplifies the output of the IA and also serves as a differential to single-ended converter. The VGA is used to adjust the gain of the channels for different applications. A multiplexer, time multiplexes the output of each channel. Moreover, a bias generator and a digital control circuit generate the bias currents and digital signals for the ASIC, respectively.

Fig. 2-12 shows the implemented current feedback instrumentation amplifier (CFIA) architecture. The presented CFIA consists of only 4 main parallel branches to minimize the power dissipation, and the ratio of two resistors defines the gain (R2/R1). On the other hand, flicker noise and process related mismatches still put a limit on the minimum achievable power dissipation and CMMR. A commonly used technique to eliminate

flicker noise and to achieve high CMRR is called chopping [23]. However, conventional chopping amplifiers are inherently DC coupled devices. Fig. 2-12 shows the architecture of the implemented AC coupled chopped IA.

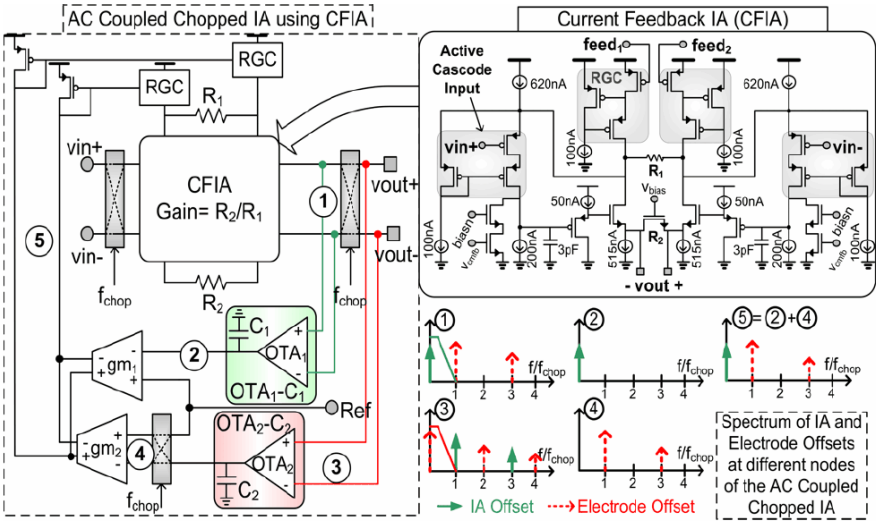


Fig. 2-12 CFIA architecture and the AC coupled chopped IA topology [16]

Fig. 2-13 shows the block diagram of the digital control circuit. It generates the necessary clock signals for the AC coupled chopped IA, the spike filter and the output multiplexer from a single clock input. Additionally, this block generates a sync-signal that can be used to synchronize the ASIC with an ADC. A non-overlapping clock generator supplies the chopping signal for the chopping switches of the AC coupled chopped IA.

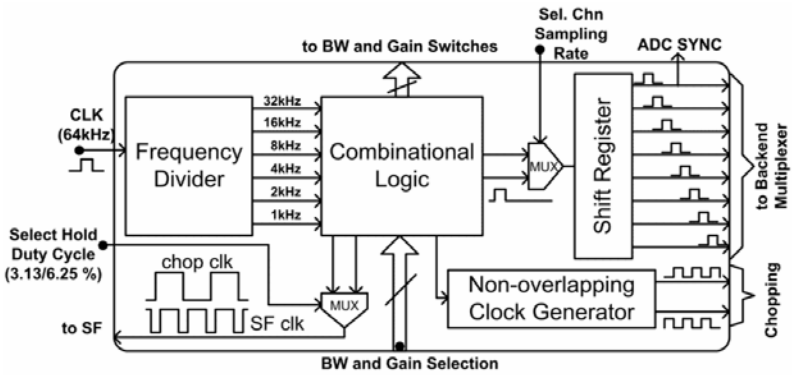


Fig. 2-13 Block diagram of the digital control circuit [16]

Refet Firat Yazicioglu et al. proposed a 60 uW 60 nV/$\sqrt{Hz}$ readout front-end for portable bio-potential acquisition systems in 2007 [6]. The architecture of the front-end acquisition system is shown as Fig. 2-14. The readout channel of the system consists of the AC coupled chopped instrumentation amplifier (ACCIA), a chopping spike filter (CSF) stage, a digitally programmable gain stage and an output buffer.

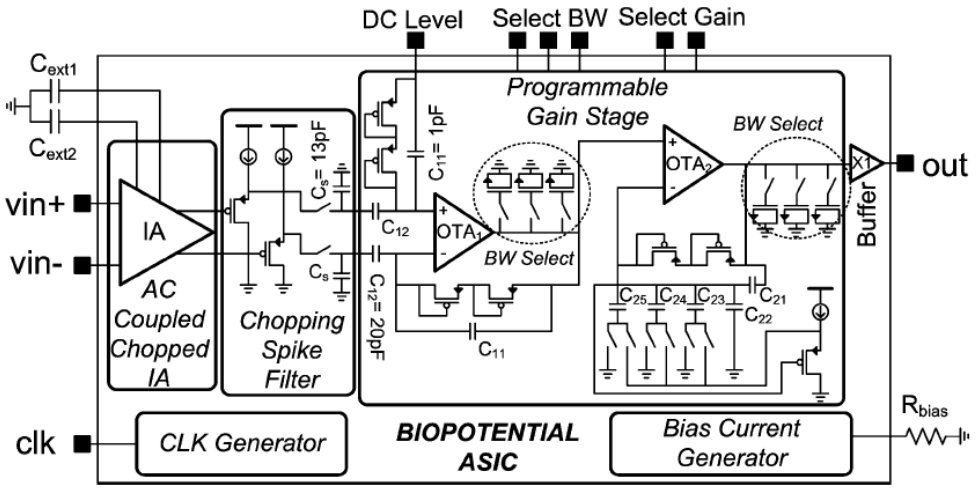


Fig. 2-14 Architecture of the bio-potential readout front-end for the acquisition of EEG, ECG, and EMG signals [6]

The concept of the ACCIA is shown in Fig. 2-15. DC input voltage which is the offset voltage is modulated by the input chopper and copied to the terminals of R_1. The voltage creates a current through R_1 which is copied to R_2 and defines the output voltage after demodulation by the output chopper. A trans-conductance stage *GM* with trans-conductance and low pass cut-off frequency f_p filters the DC component of the output and converts it into current. The transfer function of the architecture is as (2-3), assuming low pass cut-off frequency of the ACCIA $f_{LP,IA}$ is much larger than f_{chop} and $gmR_2 >> 1$.

$$\frac{V_{out}}{V_{in}}(s) = \frac{R_2}{R_1}\frac{s + 2\pi f_p}{s + gmR_2(2\pi f_p)} \tag{2-3}$$

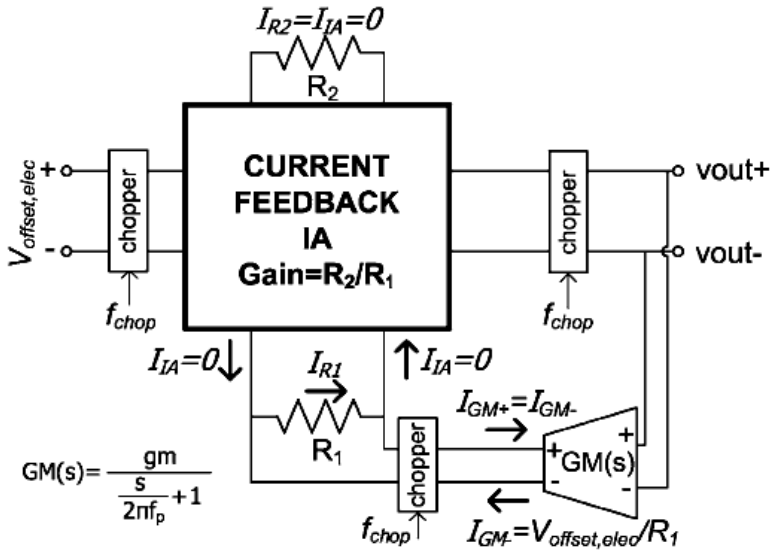


Fig. 2-15 Concept of the ACCIA [6]

On the other hand, the noise of the IA is only modulated by the output chopper. Therefore, the output noise power spectral density of ACCIA, S_{ACCIA}, can be expressed in terms of the output noise power spectral density of the IA, S_{IA}, as (2-4).

$$S_{ACCIA}(f)=\left(\frac{2}{\pi}\right)^2\sum_{\substack{n=-\infty\\ n=odd}}^{+\infty}\frac{1}{n^2}S_{IA}(f-nf_{chop})$$
$$\cong S_{IA,white}(f) \tag{2-4}$$

If $f_{LP,IA}>>f_{chop}$ and the flicker noise corner frequency of the current feedback IA is smaller than $f_{chop}/2$, $S_{IA,white}$ [23]. As a result, while flicker noise of the current feedback IA is eliminated by chopping, the electrode offset is filtered by the feedback loop implemented by *GM*. Fig. 2-16 shows the implementation of the concept presented Fig. 2-15. This architecture can eliminate flicker noise, and external circuit reduces the offset voltage is presented by electrode and IA. The GM is implemented by the OTA_2-C_{ext2} filter and the trans-conductance stage, gm_2. This results in an equivalent trans-conductance of $A_v\ gm_2$, where A_v is the voltage gain of OTA_2. By replacing gm of (2-8) with $A_v gm_2$ and f_p with $gm_{OTA2}/(A_v C_{ext2})$, high-pass cut-off frequency of the ACCIA, $f_{HP,ACCIA}$, is shown as (2-5).

$$f_{HP,ACCIA} = \frac{1}{2\pi} R_2 gm_2 \left(\frac{gm_{OTA2}}{C_{ext2}} \right) \tag{2-5}$$

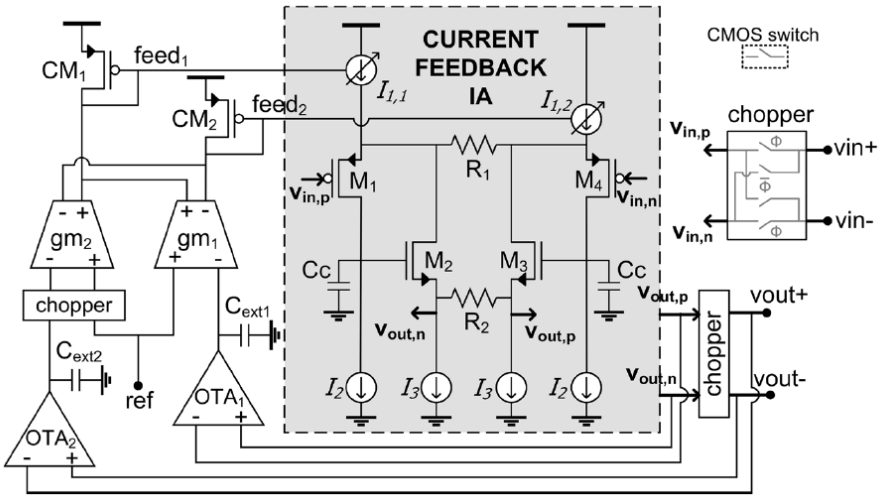


Fig. 2-16 ACCIA implemented circuit [6]

OTA_2 is implemented as a current mirror OTA as Fig. 2-17(a), where is reduced using a series parallel division of current [24]. The gm2 stage is implemented as a basic differential stage as Fig. 2-17(b), which acts as a voltage to current converter. The combination of the two feedback loops cancels both different electrode offset (DEO) and the IA offset.

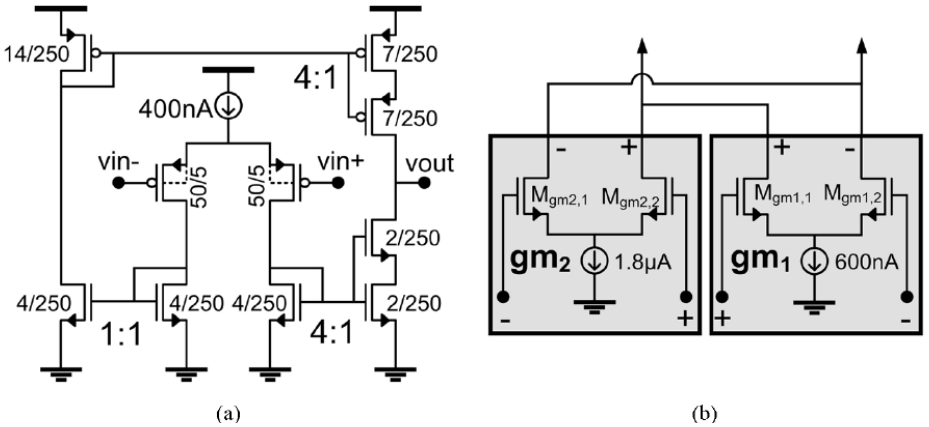


Fig. 2-17 Schematic of OTA [6]: (a) OTA_1-$C_{ext1}$and OTA_2-C_{ext2} implemented circuit (b) gm_1 and gm_2 implemented circuit

Fig. 2-18 shows the complete schematic of the implemented current feedback IA. All the current sources are implemented by paralleling the unit cascode current source, M_{SN1}, M_{SN2} for NMOS current sources and M_{SP1}, M_{SP2} for PMOS current sources. Current sources $I_{1,1}$ and $I_{1,2}$ are implemented by combining a fixed current source and a regulated cascade current mirror. R2 is implemented with a NMOS transistor so that the gain of the IA can be continuously adjusted. The source follower stages, which consist of transistors and act as level shifters in order to maximize the input-output voltage swing of the IA.

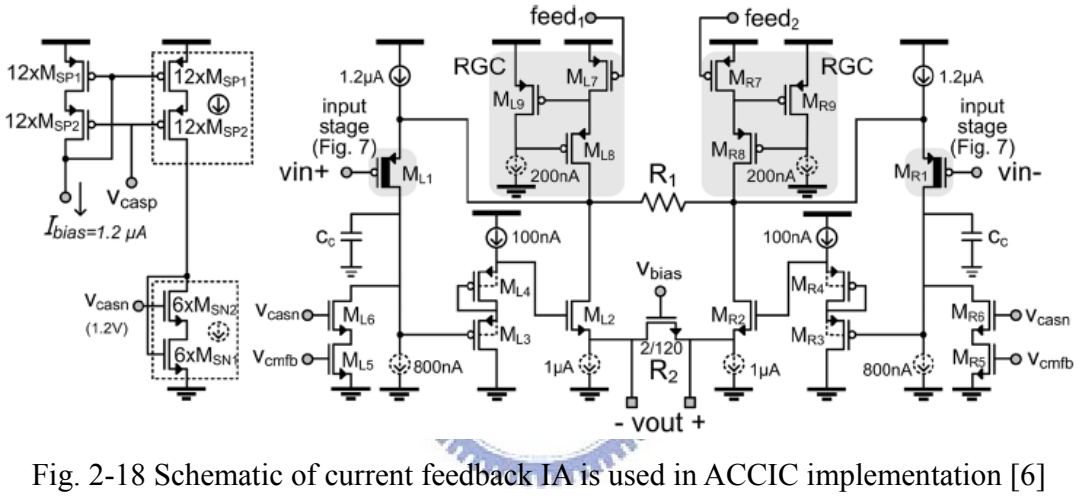


Fig. 2-18 Schematic of current feedback IA is used in ACCIC implementation [6]

Fig. 2-19 shows the implemented chopping spike filter (CSF) stage. Before the appearance of the chopping spike, output is sampled to the capacitor and during the presence of a chopping spike, switch S is opened and output is held on the capacitor.

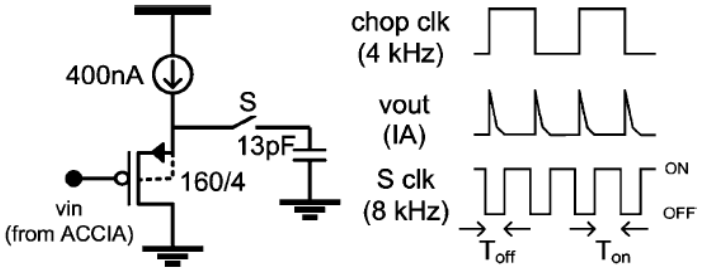


Fig. 2-19 Schematic of CSF and operation principle [6]

A continuous-time variable gain amplifier (VGA) stage with digitally controllable gain is shown as Fig. 2-20. Pseudo-resistors are used in order to set the DC level at the inverting node of the OTA. The VGA transfer function of the VGA is shown as (2-6).

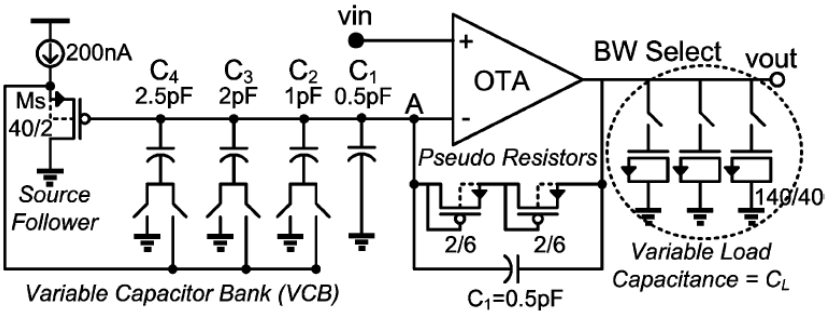


Fig. 2-20 Schematic of the VGA [6]

$$A_v(s) = \frac{\left\{1 + \frac{C_T}{C_1}\left[\frac{\left(s + \frac{1}{C_T R_{par}}\right)}{\left(s + \frac{1}{C_1 R_{eq}}\right)}\right]\right\}}{\left[s\left(\frac{C_T}{C_1}\frac{C_L}{gm_{OTA}}\right) + 1\right]} \qquad (2\text{-}6)$$

Chapter 3
A CMOS Mixed-Signal Front-End IC for Portable Biopotential Acquisition System

In this chapter, the critical issues of front-end circuit and complete mixed-signal front-end integrated circuit (MSFEIC) are presented. Section 3.1 shows the overview of MSFEIC architecture. Section 3.2 describes the critical issues of front-end circuit. Section 3.3 presents every stage of MSFEIC. The simulation results and summary are presented in Section 3.4 and 3.5, respectively.

3.1 System Architecture

This study aims to develop a bandwidth/gain tunable, low noise, low power and multi-channel mixed-signal front-end integrated circuit (MSFEIC) for patient's biomedical signals monitoring. It amplifies the measured signals and filters other noise and makes these signals become to the meaningful information. Because the biomedical signals distribute over the very weak amplitude and very low frequency, they must be processed by MSFEIC before input the digital signal processor (DSP) to analyze. MSFEIC is divided into four parts, that including instrumentation amplifier (IA), voltage amplifier, low-pass filter (LPF), and analog-to-digital converter (ADC).

However, the measured node of the biomedical signals is not only one node, so the MSFEIC is a multi-channel design to cooperate to measure conditions practically. The structure of the MSFEIC is shown as Fig. 3-1. It is composed of four chopper-stabilized instrumentation amplifier (CHS-IA), a four-to-one analog multiplexer, a switched-capacitor variable gain amplifier (SC-VGA), a switched-capacitor low-pass

filter (SC-LPF), a Multi-stAge-noise-SHaping 2-1-1 tri-level sigma-delta analog-to-digital converter (MASH 2-1-1 tri-level ΣΔ ADC). In addition, MSFEIC includes a digital controlling interface with a clock generator.

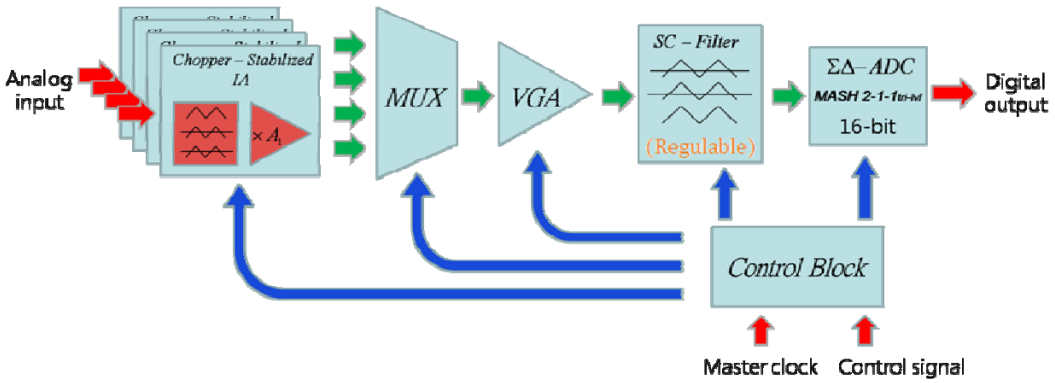


Fig. 3-1 The signal flow gragh of MSFEIC

In this structure of MSFEIC, the first stage CHS-IA initially amplifies the weak biomedical signals which are received by electrodes. It defines the noise performance of the front-end. A standard IA architecture is the three-opamp IA. However, the CMRR of the three-opamp IA depends on the matching of the resistors and the need for low output impedance amplifiers results in excessive power dissipation. Thus, three-opamp IA is convenient for low-power and low-noise front-ends.

A digitally programmable gain stage with selectable gain is used to adjust the gain of the readout for different biomedical signals. Conventional gain stages use either capacitor or resistive feedback topologies, where former has consumes excessive power. In this work, a switched-capacitor topology for variable gain amplifier is applied to MSFEIC, in which input signal amplification and output load drive are separated into two different phases. This SC-VGA technique relaxes the requirement for the bandwidth and the slew rate of the operational amplifiers employed. Thus, the power consumption can be reduced.

In the last decade or so many active filters with resistors and capacitors have been replaced with a special kind of filter called a switched-capacitor filter. The switched-capacitor filter allows for very sophisticated, accurate, and tuneable analog

circuits to be manufactured without using resistors. This is useful for several reasons. Chief among these is that resistors are very noisy, and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values. Moreover, it can also perform the operation of an anti-aliasing filter.

In a complete biomedical signal sensor circuit, that must includes a analog-to-digital (ADC) converter, the incorporation of an analog-to-digital converter (ADC) allows data communication with digital devices, targeted for ultimate system-on-chip approach, with the incorporation of a digital signal processor for full function.

3.2 Design Issues

3.2.1 Device Electronic Noise

Noise limits the minimum signal level that a circuit can process with acceptable quality. In particular, biomedical signals are very weak and susceptible to noise interference. Therefore, the input stage of biomedical signals acquisition circuit need to eliminate $1/f$ and popcorn noise. First of all, the need to analyze the form of noise.

Analog signals processed by integrated circuits are corrupted by two different type of noise: device electronic noise and environmental noise. We focus on device electronic noise here.

(1) Thermal Noise

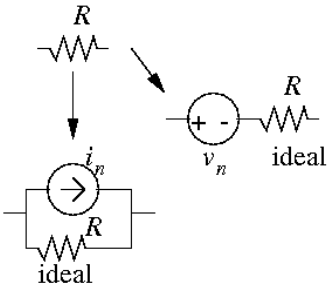


Fig. 3-2 Resistor noise model

Resistance is the most common source of noise, the random motion of electrons in conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. Thus, the spectrum of thermal noise is proportional to the absolute temperature. According to Nyquist theorem, the Effective noise power and one-sided spectral density:

$$P_{av} = kT\Delta f = \overline{v_n^2}/4R \tag{3-1}$$

$$S_v(f) = \overline{v_n^2}/\Delta f = 4kTR \qquad f \geq 0 \tag{3-2}$$

where $k = 1.38 \times 10^{-23}\ J/K$ is the boltzmann constant. Equation (3-2) shows that noise spectral density is independent of frequency; thus, it is called “white noise”, as shown in Fig. 3-3.

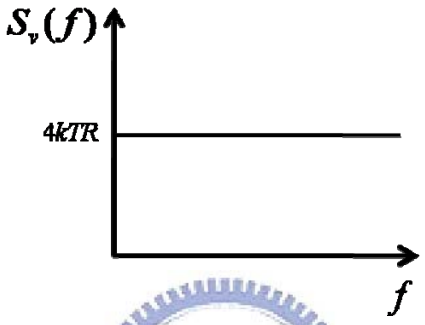


Fig. 3-3 Noise one-sided spectral density

MOS transistors also exhibit thermal noise. The most significant source is the noise generated in in the channel. It can be proved that for long-channel MOS devices operating in saturation, the channel noise can be modeled by a current source connected between the drain and source terminals as shown in Fig. 3-4.

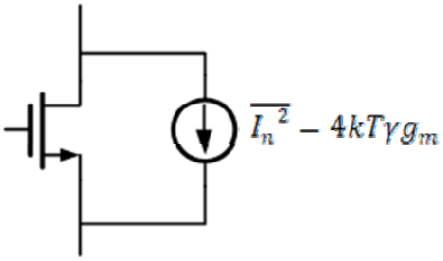


Fig. 3-4 Thermal noise of a MOSFET

(2) Flicker Noise ($1/f$ Noise)

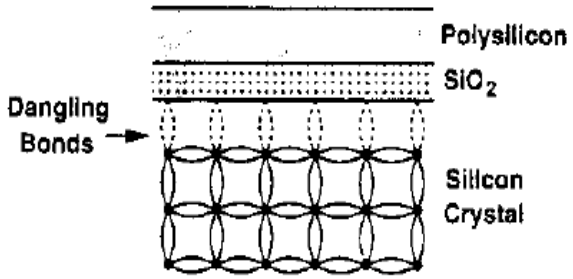


Fig. 3-5 Dangling bonds at the oxide-silicon interface [25]

The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since the silicon crystal reaches an end at this interface, many "dangling" bonds appear, giving rise to extra energy states. As charge carriers move at the interface , some are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current. In addition to trapping, several other mechanisms are believed to generate flicker noise.

Unlike thermal noise, the average power of flicker noise cannot be predicted easily. Depending on the "cleanness" of the oxide-silicon interface, flicker noise may assume considerably different values and as such varies from one CMOS technology to another. The flicker noise is modeled as a voltage source in series with the gate and given by

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{3-3}$$

where K is a process-dependent constant. As shown in Fig. 3-6, the noise spectral density is inversely proportional to the frequency.

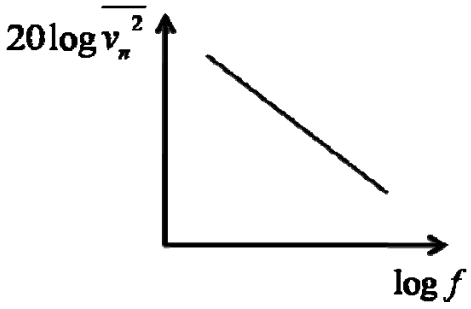


Fig. 3-6 Flicker noise spectrum

From the above discussion, in order to quantify the significance of $1/f$ noise with respect to thermal noise for a given device, we plot both spectral densities on the same axes (Fig. 3-7), and we can reduce noise "enough" by

1. Using "large" devices and good layout.
2. Trimming (bipolar).
3. Dynamic noise-cancellation (DNC) techniques.

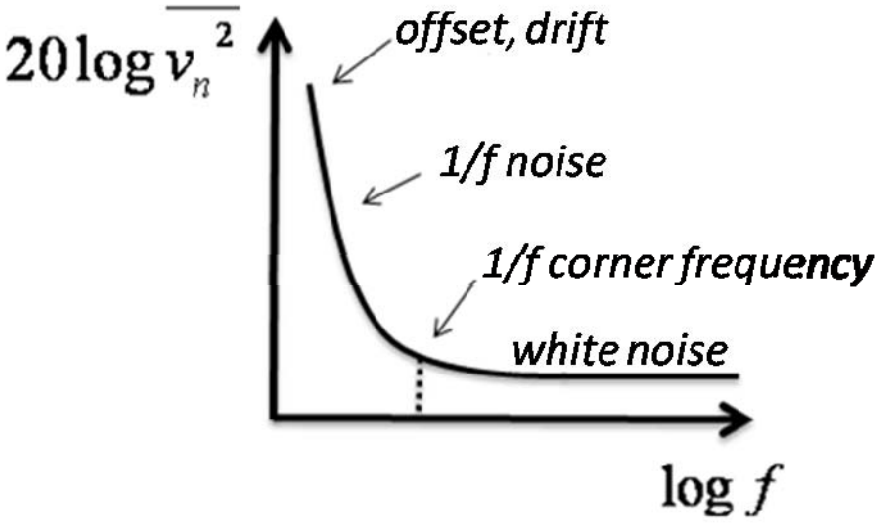


Fig. 3-7 Concept of noise

For this design, DNC is a good way to eliminate noise, one for the application of continuous-time, we use the chopper stabilization technique, because it has excellent long term stability, and no additional costs for testing.

3.2.2 Charge Injection

Charge injection occurs by channel charge when MOS switches turn off. From Fig. 3-8 we can see the channel charge flow out from the channel region of the transistor to the drain and source junctions. The channel charge of a transistor had zero drain-source voltage is given by (3-4).

$$Q_{ch} = WLC_{ox}V_{eff} = WLC_{ox}(V_{gs} - V_t) \tag{3-4}$$

And we derive voltage error due to charge injection is given by (3-5).

$$\Delta V = -\frac{1}{2}Q_{ch} \cdot \frac{1}{C_l + C_{ov}} \approx \frac{WLC_{ox}(V_{gs} - V_t)}{2C_l} \tag{3-5}$$

Switches connected to analog ground and virtual ground will cause signal -independent error because its turn-on voltage is constant. Besides these, switches connected to the signal will cause signal-dependent error which is changed with signal. Signal-dependent error is important because it truly affects resolution of the circuit. Therefore, How to reduce this kind of errors is the critical issue when we design switches of switched-capacitor circuit.

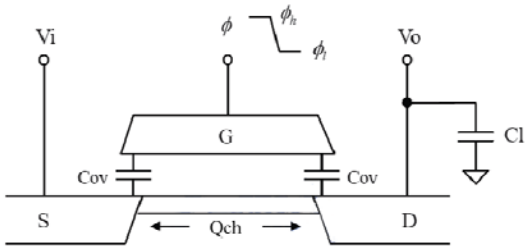


Fig. 3-8 Non-ideal effects of MOSFET switch.

3.2.3 Switch Body Effect

To alleviate the body effect on a CMOS switch, we may permanently connect the body of the MOSFET to its source. However, this arrangement is not applicable to some fabrication processes. Alternatively, we use an auxiliary structure as shown in Fig. 3-9.

As the schematic shows, *M*3 and *M*4 form the main switch, while *M*1 and *M*2 forms the auxiliary switch. When *clk* goes low, both *M*1 and *M*3 are shut off, and the body of *M*3 is tied to the highest voltage in the circuit (i.e., *Vdd*) through the PMOS transistor *M*5, in order to prevent latch-up. When the clock signal *clk* goes high, both the main and auxiliary switches are conducting, and the body of the PMOS transistor *M*3 is connected to its source rather than to *Vdd*. As a result, its body-to-source voltage (*Vbs*) is constantly set to zero, and the body effect is thus removed. Also, its on-resistance is signifi cantly lowered [30].

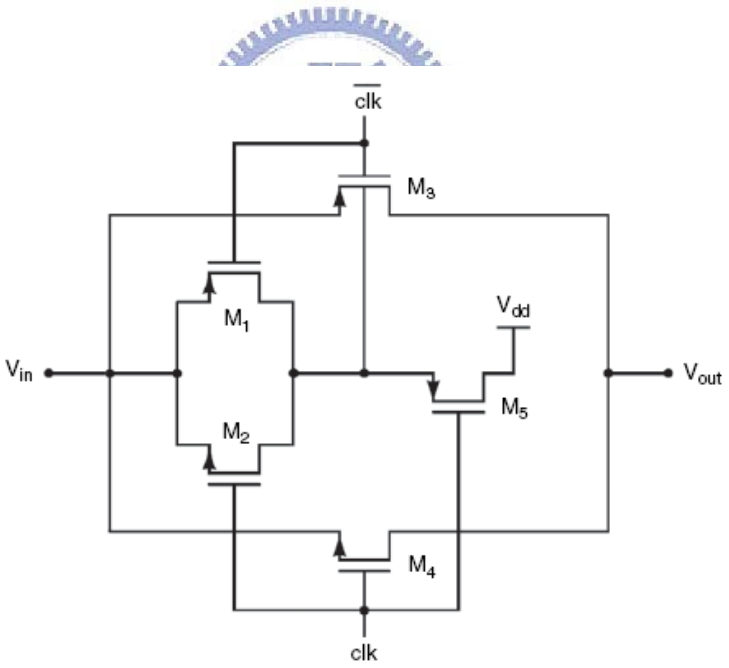


Fig. 3-9 CMOS switch configuration.

3.2.4 Analog Nonlinearities in Cascaded Modulator

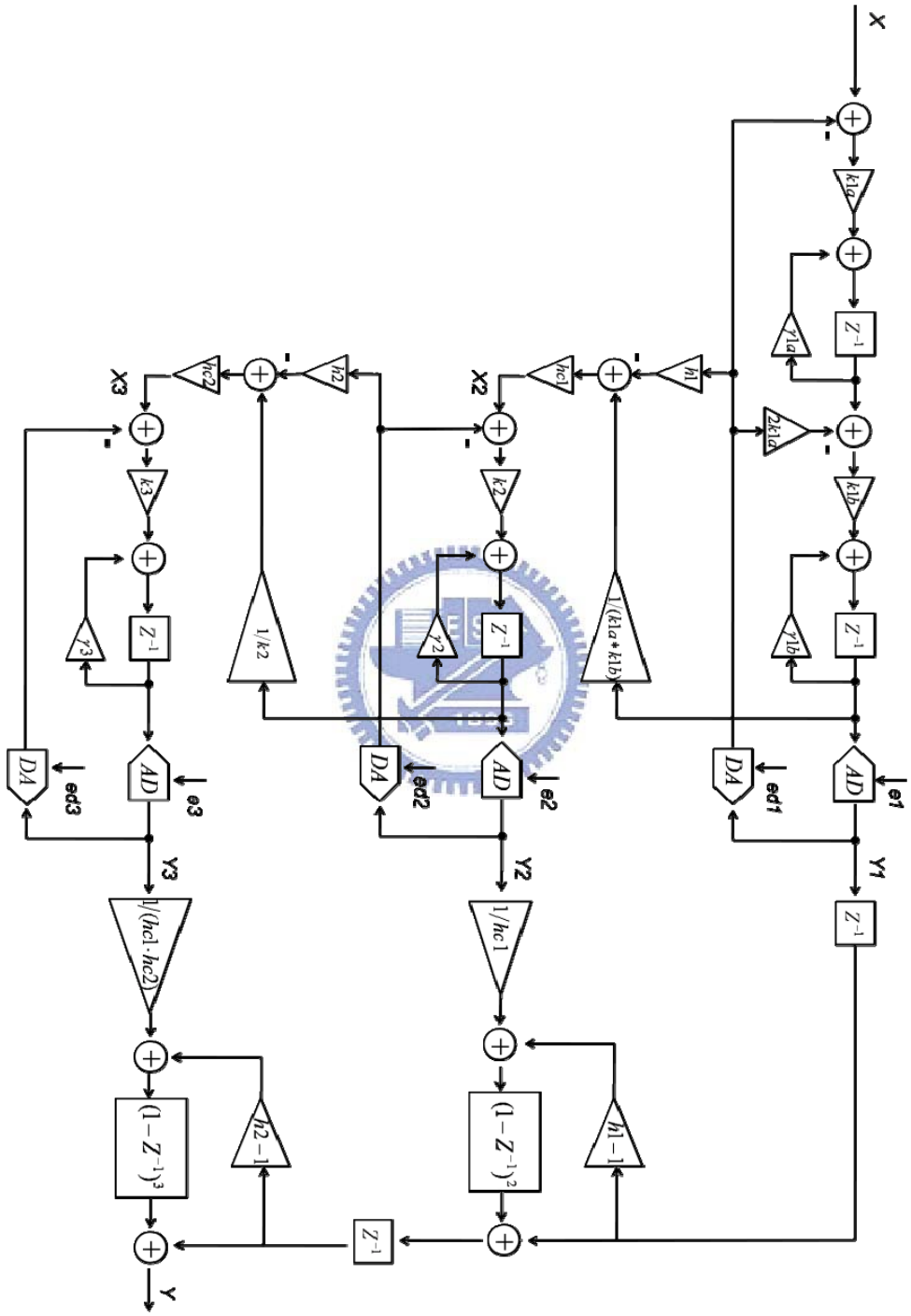


Fig. 3-10 A cascaded fourth-order (2-1-1) modulator general form with analog nonidealities.

Fig. 3-10 illusfrates A cascaded fourth-order (2-1-1) modulator with analog nonidealities. The DAC nonlinearities, *ed1, ed2*, and *ed3,* are represented as additive white noises, similar to the quantization error, at the corresponding feedback path of the modulator. The coefficients, γ1, γ2, and γ3, are referred to as the leakage factors of the integrators, respectively.

Ideally, the coefficients, γ1, γ2, and γ3, are all equal to unity, and the DAC errors, *ed1, ed2,* and *ed3,* are equal to zero. In reality, mismatches in the analog components make these coefficients vary slightiy from their ideal values, causing circuit non-linearities. Therefore, efforts need to be made to alleviate these circuit nonlinearities[26].

3.3 Circuit Design

The structure of MSFEIC is divided into four parts mainly (Fig. 3-11). The first stage is a chopper-stabilized instrumentation amplifier (CHS-IA), the second stage is a switched-capacitor variable gain amplifier (SC-VGA), the third stage is a switched-capacitor low-pass filter (SC-LPF), and the fourth stage is a cascaded fourth-order (2-1-1) sigma-delta analog-to digital converter (MASH 2-1-1 tri-level ΣΔ ADC). In addition, the circuit has four analog multiplexer to select signal paths and a digital control circuit to select different mode.

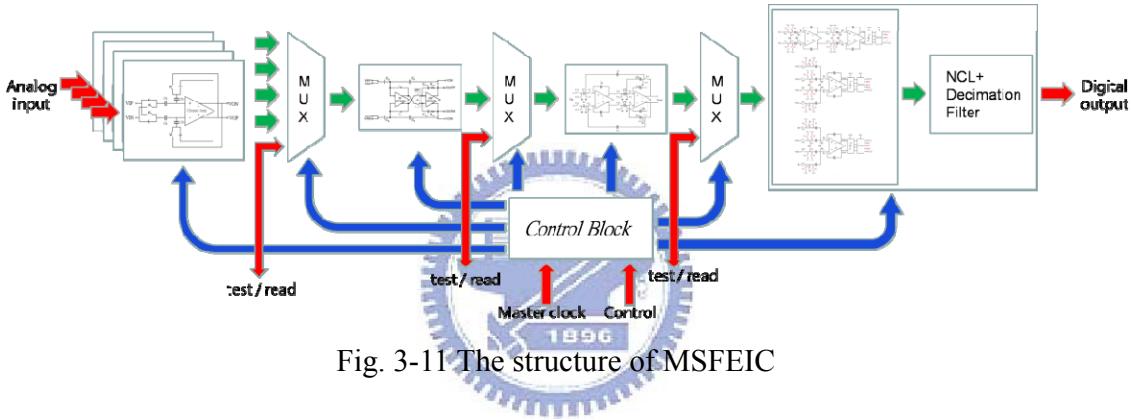
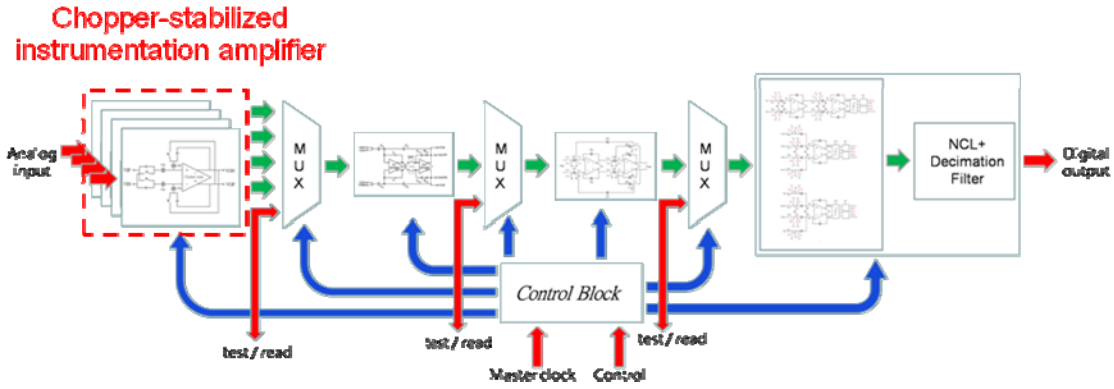


Fig. 3-11 The structure of MSFEIC

3.3.1 Chopper-Stabilized Instrumentation Amplifier (CHS-IA)



Biomedical signals are small-of the order of tens of μV-and reside at low bandwidths

that make them susceptible to excess noise. The chopper architecture circumvents the major issues of low power designs by using closed-loop feedback with specific timing constraints. To illustrate this concept, the proposed signal flow graph for an amplifier responding to a step is illustrated in Fig. 3-12. Feedback is a well-known technique to suppress distortion and increase precision in circuits. The implementation of feedback in this application, however, required a design paradigm. Input and feedback paths around the amplifier are conveyed as ac signals that were up-modulated to the chopper modulation frequency. The ac feedback ensures that all signals passing through the front-end of the amplifier are well above the $1/f$ corner for the transistors. Using ac modulation also allows for input and feedback signal chain scaling to be achieved with low-noise, on-chip capacitors as opposed to resistors that potentially draw excess power and add noise to the signal chain[27].

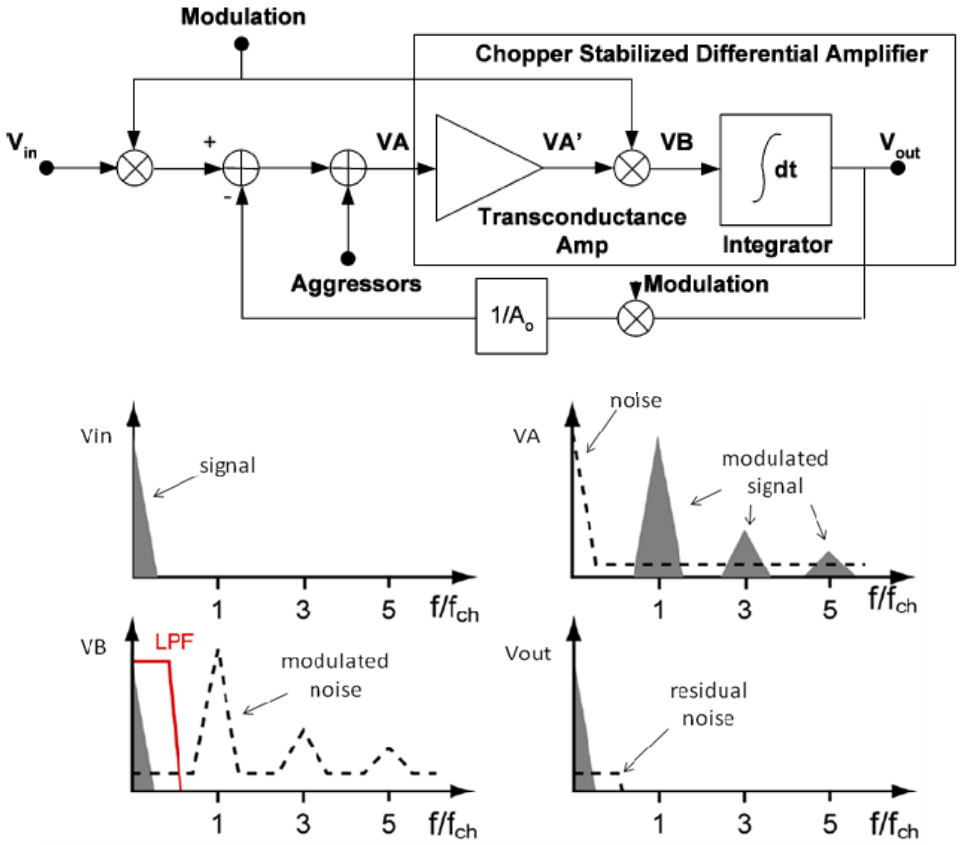


Fig. 3-12 The signal flow gragh of CHS-IA[27]

The chopper stabilization is an established technique for suppressing device electronic noises; the noises can be regarded as input refered noise, aggressor. At the input, a switch modulator translates input signal to the chopper frequency prior to entering the amplifier; and the chopper frequency must excess noise corner. After amplification, the signal is translated back to baseband, while shifting the noise up to the modulation frequency. Finally, the integrator filter out noise and retain the signal. The gain characteristics of the chopper-stabilized instrumentation amplifier are set by the input and feedback-switched capacitor networks. The amplifier summing node VA receives a differential signal input scaled by the capacitor C_{in} (Fig. 3-13), and the gain we set in CHS-IA is 26 dB.

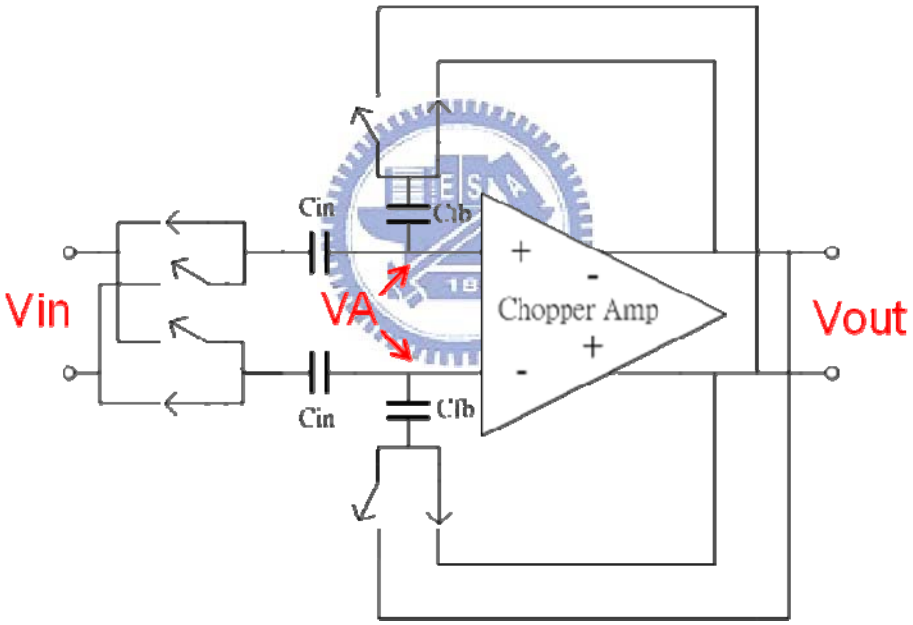


Fig. 3-13 The structure of CHS-IA

The structure of CHS-IA is shown as Fig. 3-13, the chopper modulator is composed of CMOS switch. To alleviate the body effect on a CMOS switch, we use the low body effect CMOS switch illustrated in section 3.2.3, the chopper amplifier in CHS-IA is a two stage amplifier with chopping switch[28], which is shown as Fig. 3-14.

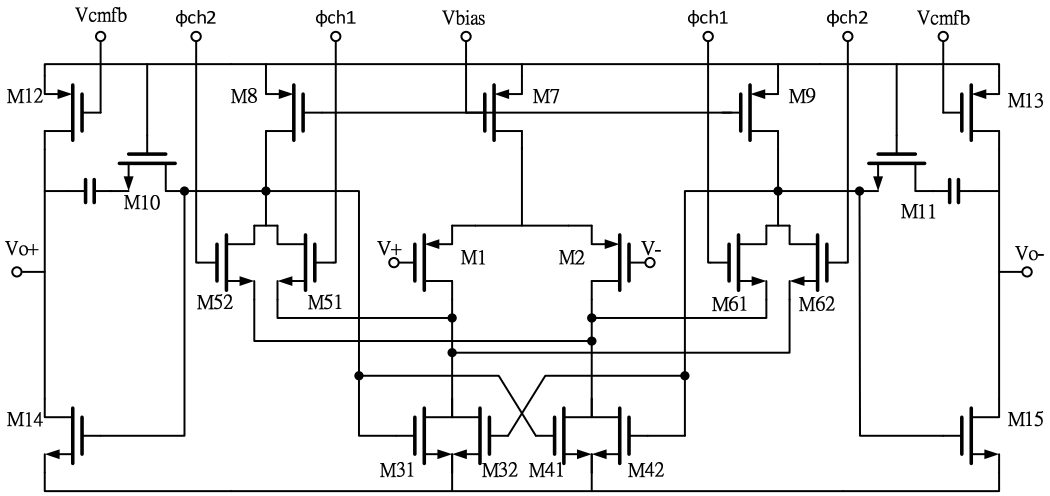


Fig. 3-14 Chopper amplifier (Two stage amplifier with chopper switch)[28]

The two stage amplifier illustrated in Fig. 3-14 is based on a fully differential folded-cascode p-type two-stage Miller-compensated configuration. with active load which also allows a large output swing. Since the opamp uses a two-stage structure and a compensation capacitor, the same switching arrangement cannot be used at the output. In fact, the compensation capacitance acts like a memory element that prohibits the opamp output to be chopped instantaneously. Instead, the output of the first stage is chopped as shown in Fig. 3-14 using two sets cascode transistors M51, M52 and M61, M62. Due to the differential structure, the common-mode output voltage of both stages needs to be regulated using common-mode feedback (CMFB). In order to avoid this extra CM amplifier, the CMFB circuit for the first stage has been replaced by the cross-coupled connection of transistors M31, M32, M41, and M42. For the second stage, a simple active CMFB circuit, shown in Fig. 3-15, is used. Although the signal characteristics are purely ac at node VA(input of chopper amplifier), the amplifier must have the proper dc biasing to ensure the appropriate amplification and demodulation of the signals. Thus, the pseudoresistor is used.

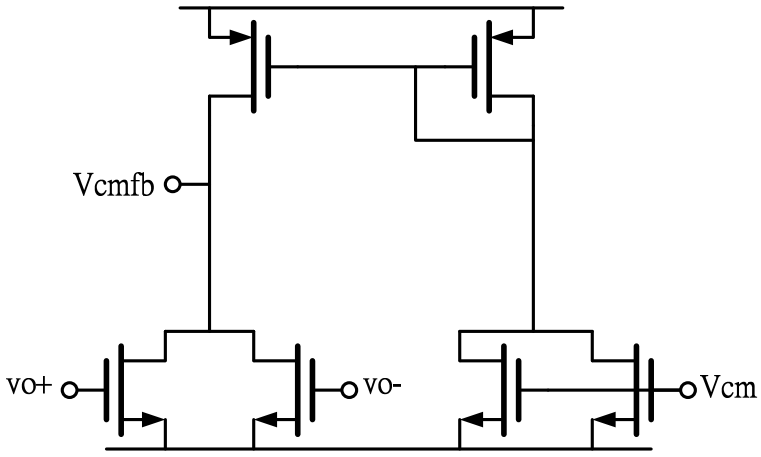


Fig. 3-15 Active CMFB

Pre-layout simulation

(1) Chopper Amplifier

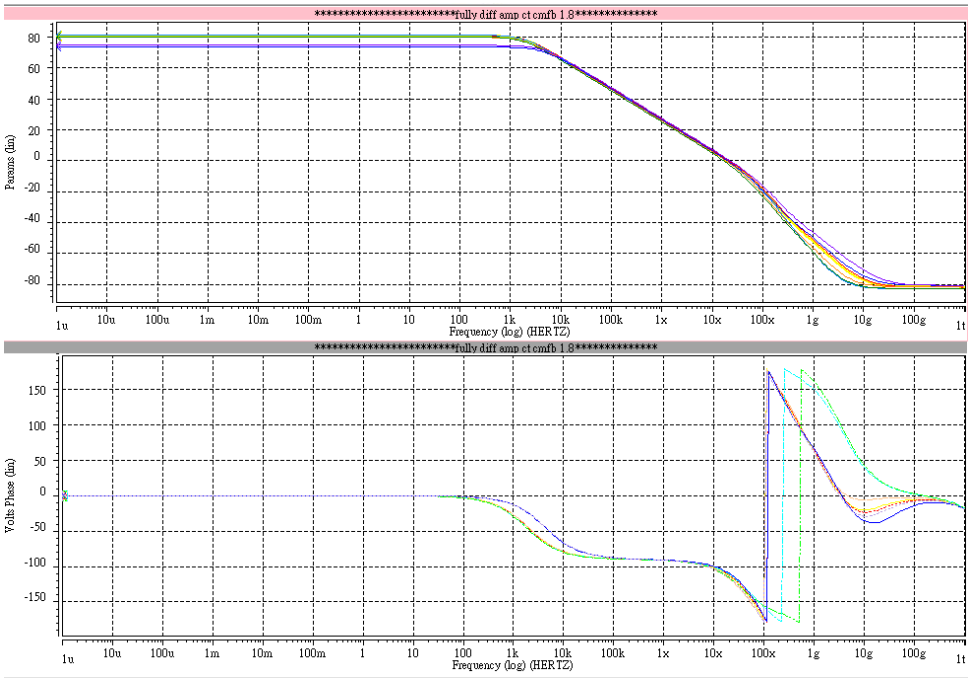


Fig. 3-16 Pre-layout simulation of chopper amplifier (Corners: TT, SS, FF, FS, SF Temperature: 0℃~100℃ Power supply: 1.8V±10%)

Gain > 73.4 dB

PM > 62.3°

(2) CHS-IA

Input testing signal

Input signal type: **sine wave**

Input signal frequency: **1.024 kHz** (the max frequency that system to process)

Input signal amplitude: **213 μV**

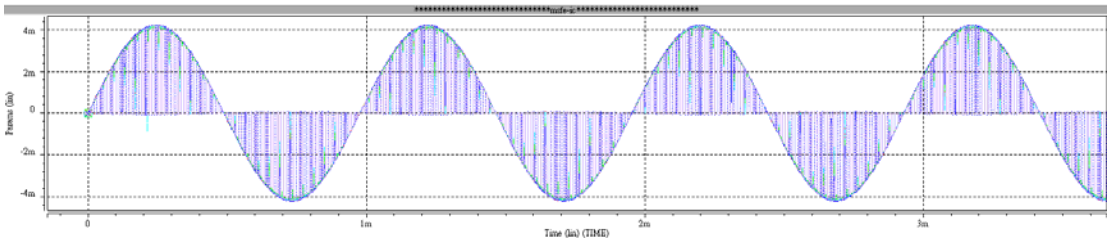


Fig. 3-17 The output of CHS-IA in time-domain (Corners: TT, SS, FF, FS, SF Temperature: 0℃~100℃ Power supply: 1.8V±10%)

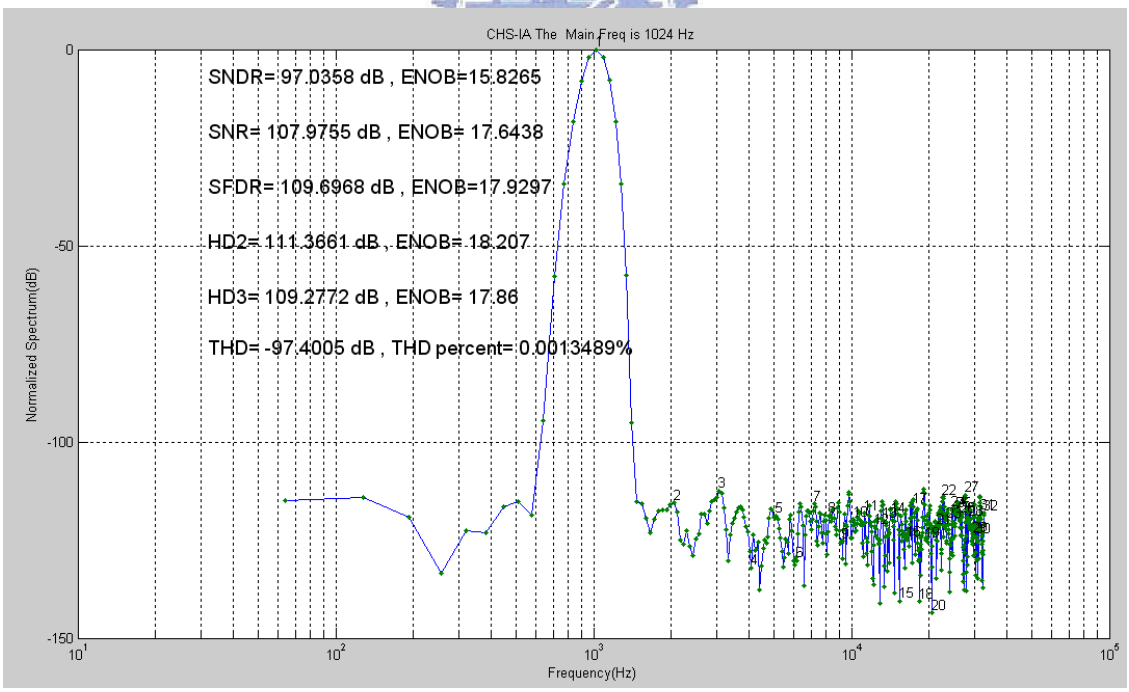
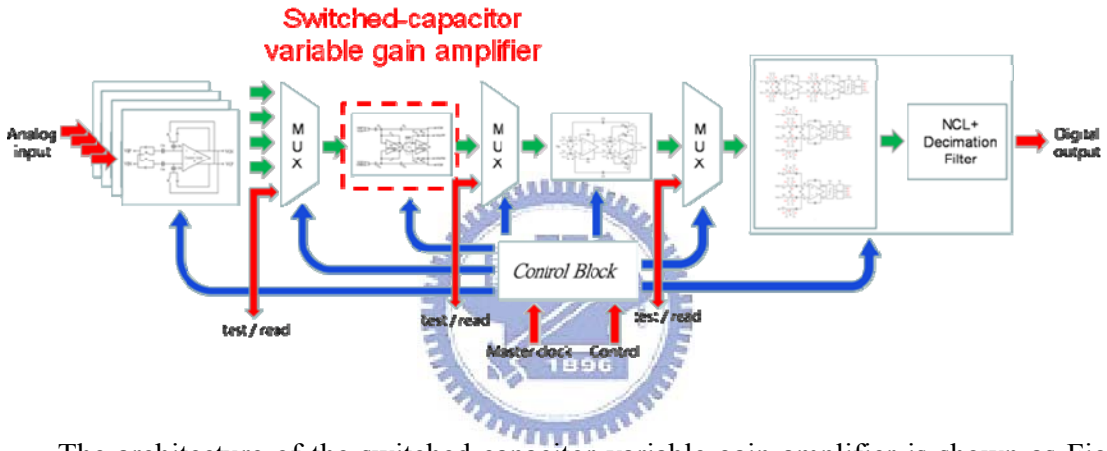


Fig. 3-18 The output of CHS-IA in frequency-domain (worst case)

SPEC	CHS-IA
Supply Voltage	1.8 V
Power Consumption	72.61 uW
Gain	26 dB
Nonlinearity	0.00135%
Sample Rate	65.536 Hz
Bandwidth	2 kHz

3.3.2 Switched-Capacitor Variable Gain Amplifier (SC-VGA)



The architecture of the switched-capacitor variable gain amplifier is shown as Fig. 3-19. SC-VGA is the second gain stage besides the CHS-IA. With the measured environment and signal amplitude at that time, SC-VGA amplifies the biomedical signals to the range easy to analyze. According to the different amplitudes of the biomedical signals, we utilized tunable digital interface to choose proper voltage gain.

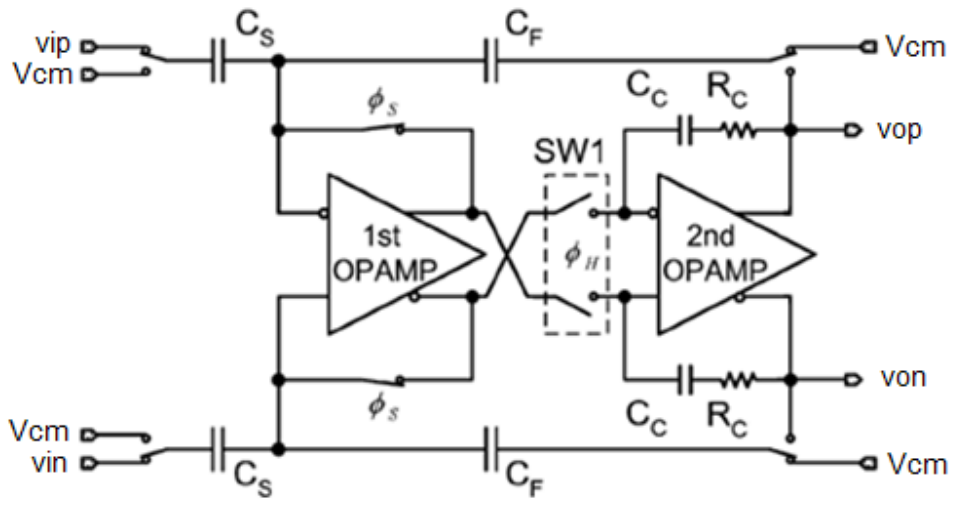


Fig. 3-19 The structure of SC-VGA[29]

Conventional gain stage is the use of resistor topology, gain is set by parallel feedback resistor and input resistor. However, resistance configuration will consume a large amount of power and generate additional noise. Therefore, capacitor topology become a better choice, but it's performance of power consumption is still not suitable for portable devices. In this design, we use switched-capacitor variable gain amplifier (SC-VGA)[29] to achieve signal amplification, and gain is set by parallel feedback capacitor C_F, in which input signal amplification and output load drive are separated into two different phases. This SC-VGA technique relaxes the requirement for the bandwidth and the slew rate of the operational amplifiers employed. Thus, the power consumption can be reduced[29]. The circuit configurations of the SC-VGA in sample phase Φ_S and hold phase Φ_H are shown in Fig. 3-20 and Fig. 3-21, respectively.

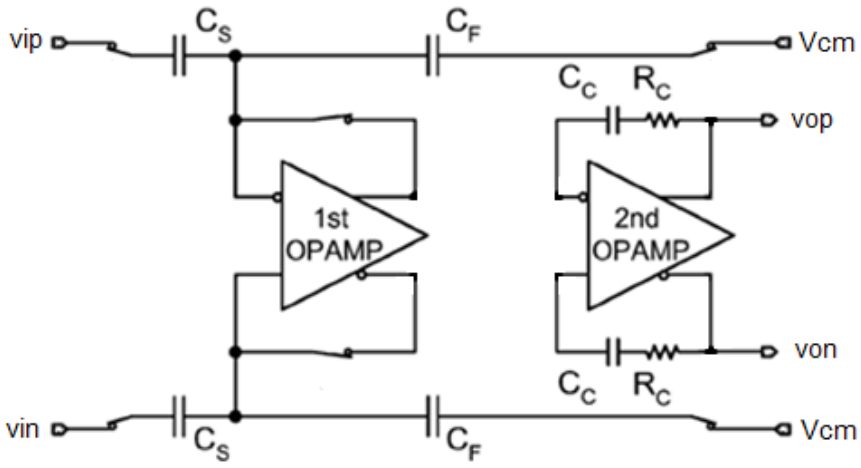


Fig. 3-20 SC-VGA in sample phase Φ_S

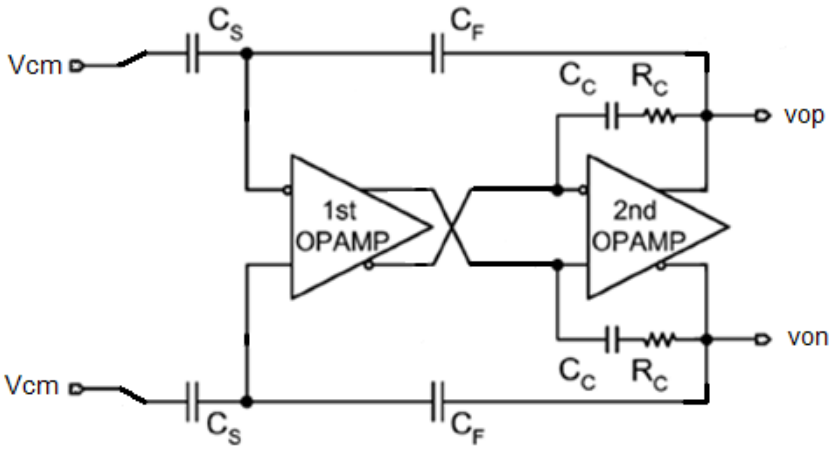


Fig. 3-21 SC-VGA in hold phase Φ_H

During phase Φ_S, as shown in Fig. 3-20, the first op-amp is reset and the input signal is sampled on C_S, At the same time, the second op-amp and compensation capacitor work together as a hold circuit for previously amplified signal in phase Φ_H. During phase Φ_H, as shown in Fig. 3-21, the first and second with C_S and C_F amplify the signal sampled on C_S previously phase Φ_S[29].

Next, the power reduction technique will be described, the bandwidth and slew rate of the hold circuit during Φ_S is given by

$$BW_{SC-VGA,\Phi_S} = \frac{g_{m2}}{2\pi C_L} \tag{3-6}$$

$$SR_{SC-VGA,\Phi_S} = \frac{I_2}{C_L} \tag{3-7}$$

where g_{m2} is the transconductance of the second op-amp, I_2 is the current consumed in the second op-amp, and C_L is the load capacitance. Those of the SC-VGA during Φ_H shown in Fig. 3-21 are given by

$$BW_{SC-VGA,\Phi_H} \approx \frac{g_{m2}}{2\pi C_L} \tag{3-8}$$

$$SR_{SC-VGA,\Phi_H} = \frac{I_1}{C_C} < \frac{I_2}{C_{Leff}+C_C} = \frac{I_2}{\beta C_L + C_C} \tag{3-9}$$

where $\beta = C_F/(C_F + C_S)$ is the feedback factor, C_c is the compensation capacitor as shown in Fig. 3-20 and Fig. 3-21, I_1 is the current consumed in the first op-amp. $C_{Leff} = \beta C_S$ is the effective load capacitance in Φ_H, and $C_S = C_L$ is assumed for simplify the analyses, also, Also, the phase margin of the two stage op-amp is assumed to be $45°$ in derivation of (3-8), which is described as

$$\frac{g_{m1}}{C_C} = \frac{g_{m2}}{C_{Leff}} \tag{3-10}$$

On the other hand, if the SW1 in Fig. 3-19 is always turned on, the bandwidth and slew rate of SC-VGA in the Φ_H are given by

$$BW'_{SC-VGA,\Phi_H} \approx \frac{\beta}{1+\beta} \cdot \frac{g_{m2}}{2\pi C_L} \tag{3-11}$$

$$SR'_{SC-VGA,\Phi_H} = \frac{I_1}{C_C} < \frac{I_2}{(1+\beta)\cdot C_L + C_C} < \frac{I_2}{(1+\beta)\cdot C_L} \tag{3-12}$$

and the phase margin of the two stage op-amp is assumed to be 45° in the derivation of (3-11), which is described as

$$\frac{g_{m1}}{C_C} = \frac{g_{m2}}{C_L + C_{Leff}} \tag{3-13}$$

the SC-VGA with switch1 (SW1) improve bandwidth as proportional to $1 + 1/\beta$. When $\beta < 1$ and $C_C \ll C_L$, $SR_{SC-VGA,\Phi_S} < SR_{SC-VGA,\Phi_H}$, which means the slew rate of the SC-VGA is limited by (3-7). The slew rate can be improved as proportional to $1 + \beta$[29]. As a result, the SC-VGA relaxes the requirement for the bandwidth and slew rate. Therefore, we use a simple structure to implement the op-amp of SC-VGA, as shown in Fig. 3-22.

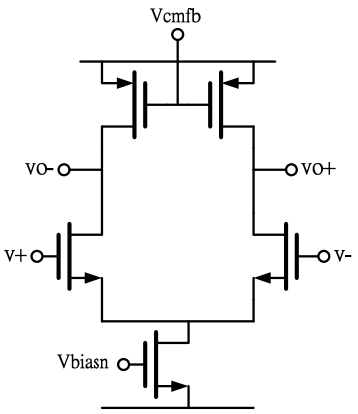


Fig. 3-22 The OPAMP used in SC-VGA

Pre-layout simulation

(1) Input testing signal:

Input signal type: **sine wave**

Input signal frequency: **1.024 kHz** (the max frequency that system to process)

Input signal amplitude: **4.1 mV**

Gain of SC-VGA: **46 dB**

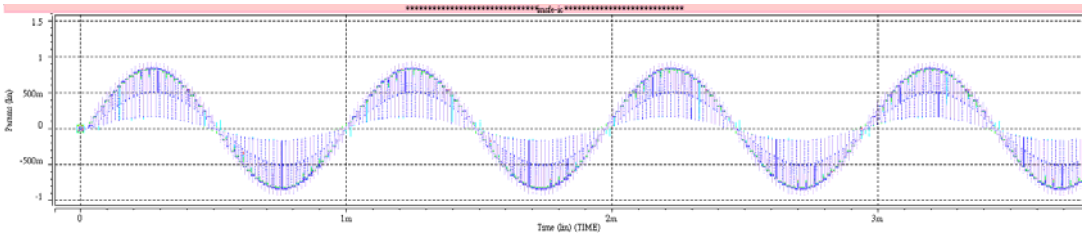


Fig. 3-23 The output of SC-VGA in time-domain (gain=46 dB) (Corners: TT, SS, FF, FS, SF Temperature: 0℃~100℃, Power supply:1.8V±10%)

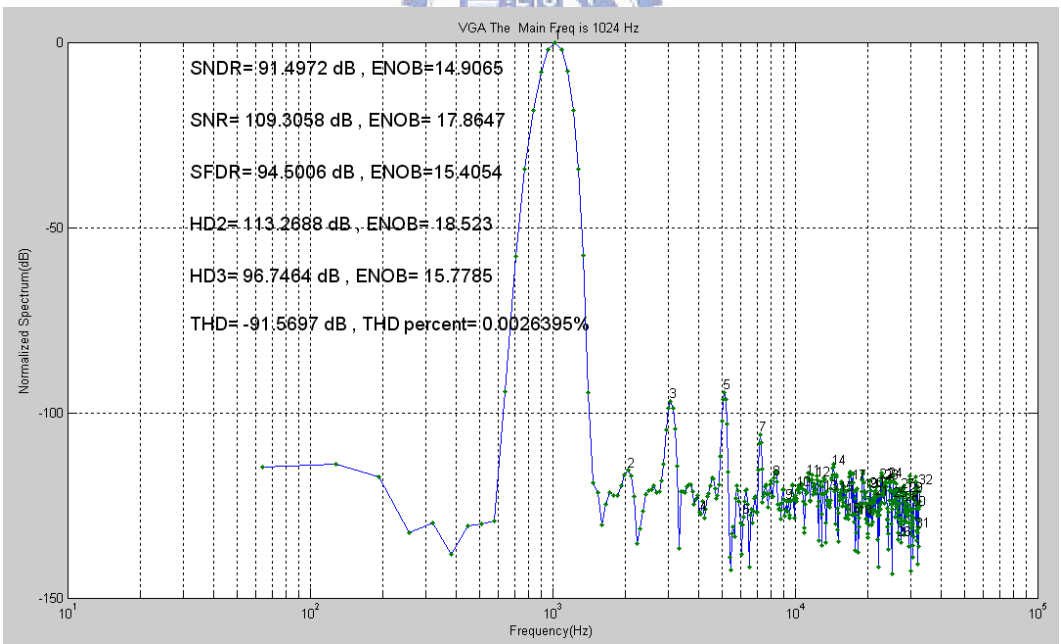


Fig. 3-24 The output of SC-VGA in frequency-domain (gain=46 dB) (worst case)

(2) Input testing signal:

Input signal type: **sine wave**

Input signal frequency: **1.024 kHz** (the max frequency that system to process)

Input signal amplitude: **8.2 mV**

Gain of SC-VGA: **40 dB**

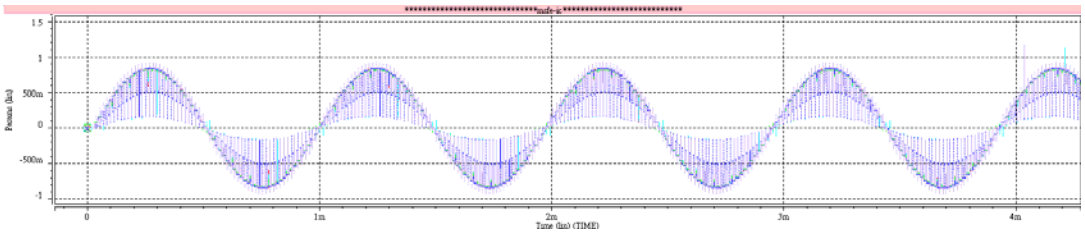


Fig. 3-25 The output of SC-VGA in time-domain (gain=40 dB) (Corners: TT, SS, FF, FS, SF Temperature: 0℃~100℃ Power supply: 1.8V±10%)

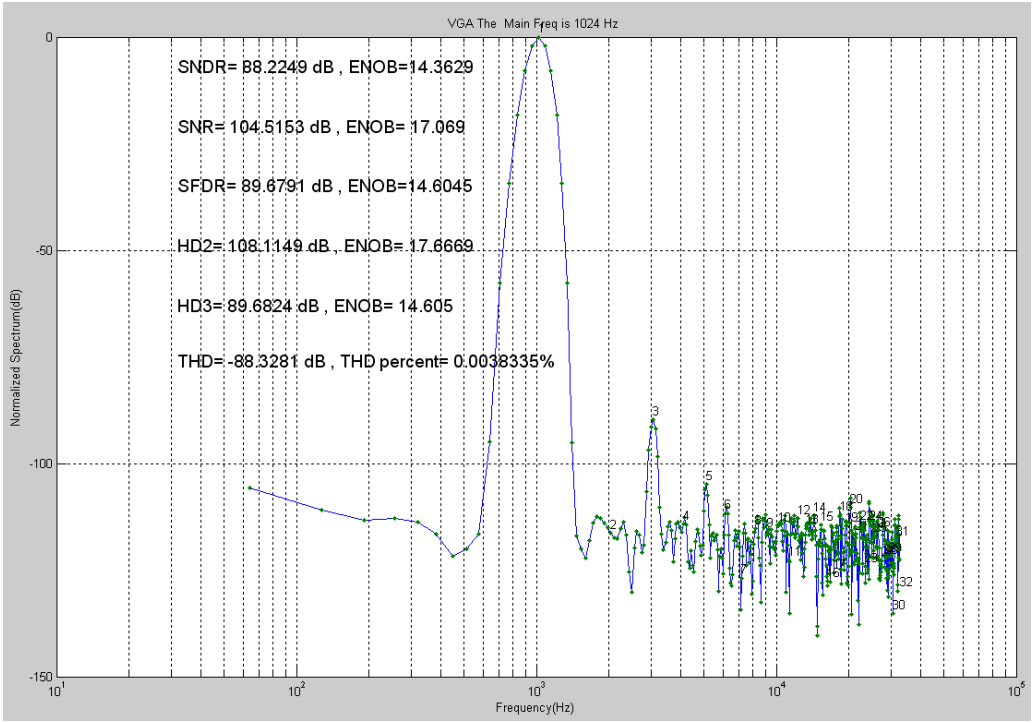


Fig. 3-26 The output of SC-VGA in frequency-domain (gain=40 dB) (worst case)

(3) Input testing signal:

Input signal type: **sine wave**

Input signal frequency: **1.024 kHz** (the max frequency that system to process)

Input signal amplitude: **16.4 mV**

Gain of SC-VGA: **34 dB**

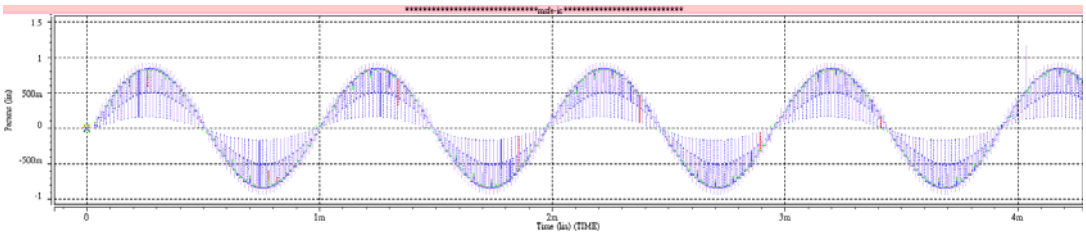


Fig. 3-27 The output of SC-VGA in time-domain (gain=34 dB) (Corners: TT, SS, FF, FS, SF Temperature: 0℃~100℃ Power supply: 1.8V±10%)

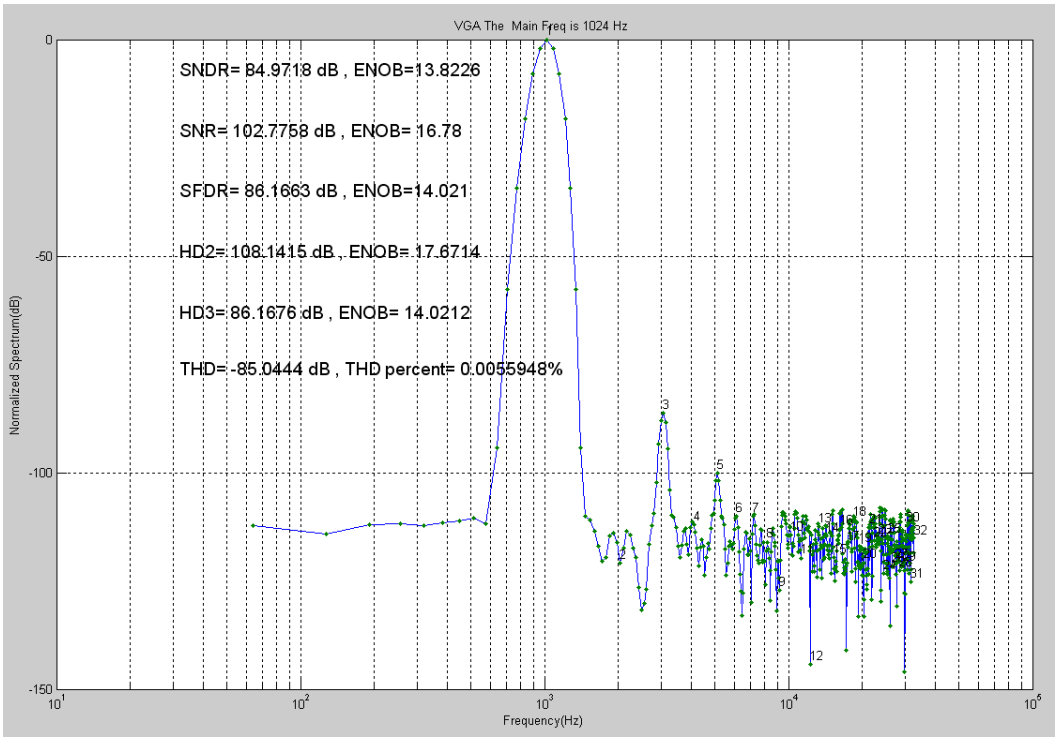
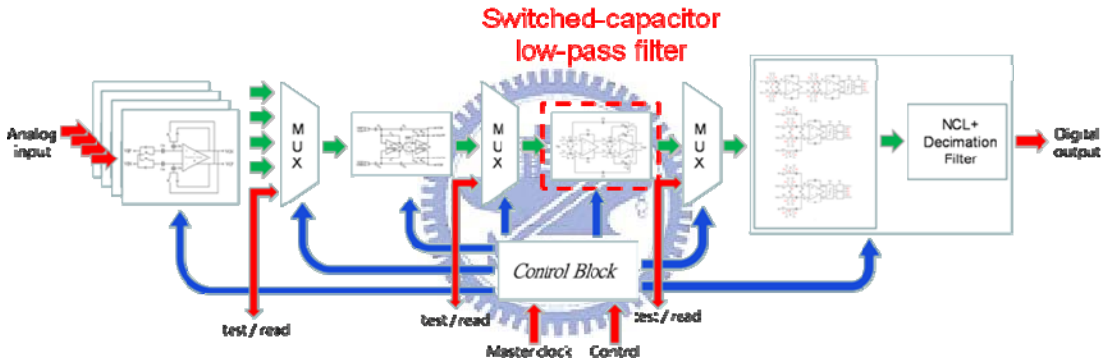


Fig. 3-28 The output of SC-VGA in frequency-domain (gain=34 dB) (worst case)

SPEC	SCVGA
Supply Voltage	1.8 V
Power Consumption	104 uW
Gain	34~46 dB
Nonlinearity	0.0056%
Sample Rate	65.536 kHz
Bandwidth	2 kHz
Gain Step	6 dB

3.3.3 Switched-Capacitor Low-Pass Filter (SC-LPF)



As the most common approach for realizing accurate and linear analog signal processing (ASP) in metal-oxide semiconductor (MOS) integrated technologies, switched-capacitor (SC) circuit techniques have dominated the design of high-quality monolithic filters since the 1980s. The incomparable technological adaptability shown by SC circuits has furthermore made them the competent candidate appropriate for a rich variety of applications. In this design, switched-capacitor low-pass filter (SC-LPF) is used to realize a low-pass filter and anti-aliasing filter. The structure of SC-LPF can be divided into two kinds of high-Q and low-Q filter, and that is suitable for application of high frequency and low frequency separately. Due to the biomedical signals are all low frequency signals, so we used the low-Q biquad filter to realize the filter.The signal flow gragh of SC-LPF is shown as Fig. 3-29.

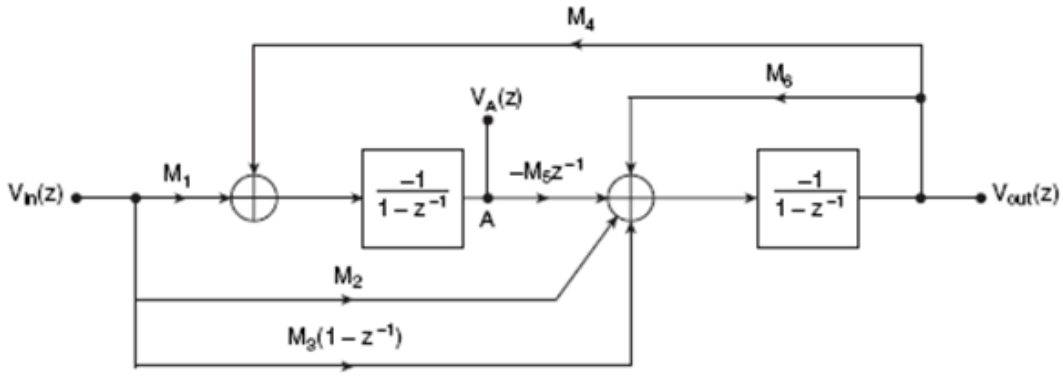


Fig. 3-29 The signal flow gragh of SC-LPF

The structure of SC-LPF is second-order biquad. As the graph shows, there are three forward paths and two feedback loops. Utilizing the Mason's rule, we can obtain the transferfunction, which is given by

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{(M_2+M_3)z^2+(M_1M_5-M_2-2M_3)z+M_3}{(M_6+1)z^2+(M_4M_5-M_6-2)z+1} \qquad (3\text{-}14)$$

The overall dc gain of this filter ($z = 1$) is thus given by

$$H(z)|_{z=1} = -\frac{(M_2+M_3)+(M_1M_5-M_2-2M_3)+M_3}{(M_6+1)+(M_4M_5-M_6-2)+1} = -\frac{M_1}{M_4} \qquad (3\text{-}15)$$

From Fig. 3-29, we can obtain the dc signal level at node A as follows:

$$V_A(z)|_{z=1} = \left[M_1 + \left(-\frac{M_1}{M_4}\right)M_4\right]\left(\frac{-1}{1-1^{-1}}\right) = \frac{0}{0} = ? \qquad (3\text{-}16)$$

The question mark in the preceding equation stands for uncertainty, which implies that the specified transfer function $H(z)$ cannot determine the dc signal level at node A.

Uncertainty essentially means flexibility, therefore a certain degree of freedom in choosing the values of M_1, M_4, and M_5 is obtained, and the nominal dc signal level at node A can be set at any value regardless of the three capacitance ratios[30].

Next, making use of the flexibility in choosing the values of M_1, M_4 and M_5, we obtain the following approximations (assuming $\omega_0 T << 1$):

$$M_4 \cong M_5 \cong \omega_0 T \cong Q \cdot M_6 \text{ and } Q \cong \frac{\sqrt{M_4 M_5}}{M_6} \qquad (3\text{-}17)$$

This indicates that the values of $\omega_0 T$ and Q can be determined by M_4, M_5, and M_6. That is, M_4, M_5, and M_6 determine the pole positions. By contrast, it can be found that the other capacitance ratios (M_1, M_2, and M_3) are responsible for the zero(s) only[30].

The implementation of SC-LPF is shown as Fig. 3-30, the switched-sharing is used. Although, switched-sharing can not only reduce the layout area but also save the dynamic power consumption.

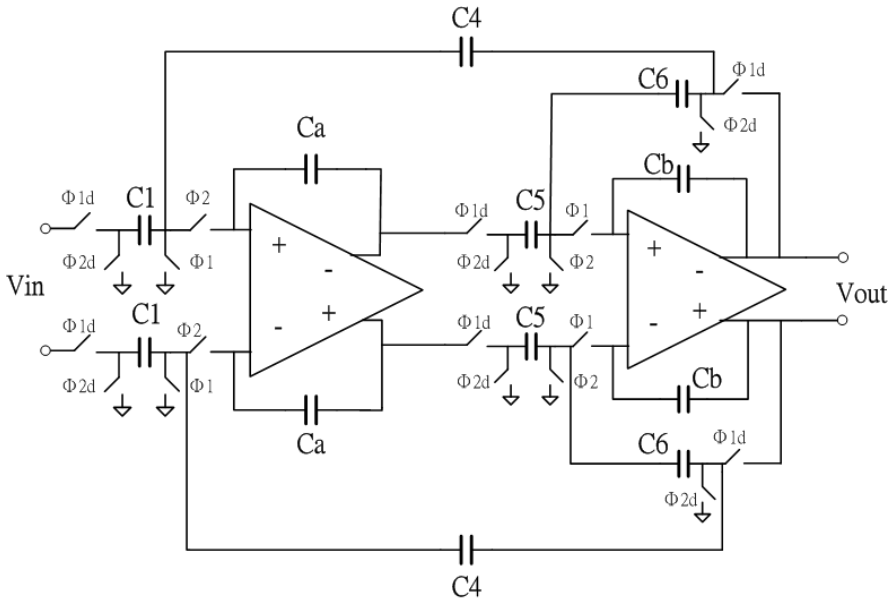


Fig. 3-30 Low-Q SC-LPF with switched-sharing

To prevent charge injection illustrated in section 3.2.2, the circuit is controlled by two phase non-overlapping clock Φ_1, Φ_2 and two delay phases Φ_{1d}, Φ_{2d}; mutual matching of four clocks can effectively reduce the influences of charge injection.

Pre-layout simulation

Input testing signal:

Input signal type: sine wave

Input signal frequency: 1.024 kHz (the max frequency that system to process)

Input signal amplitude: 0.82 V

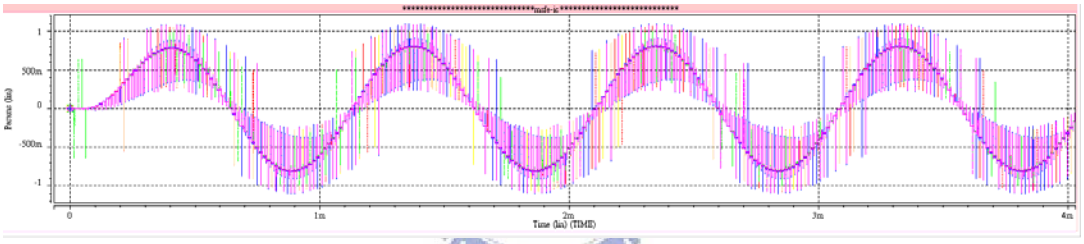


Fig. 3-31 The output of SC-LPF in time-domain (Corners: TT, SS, FF, FS, SF Temperature: 0℃~100℃ Power supply: 1.8V±10%)

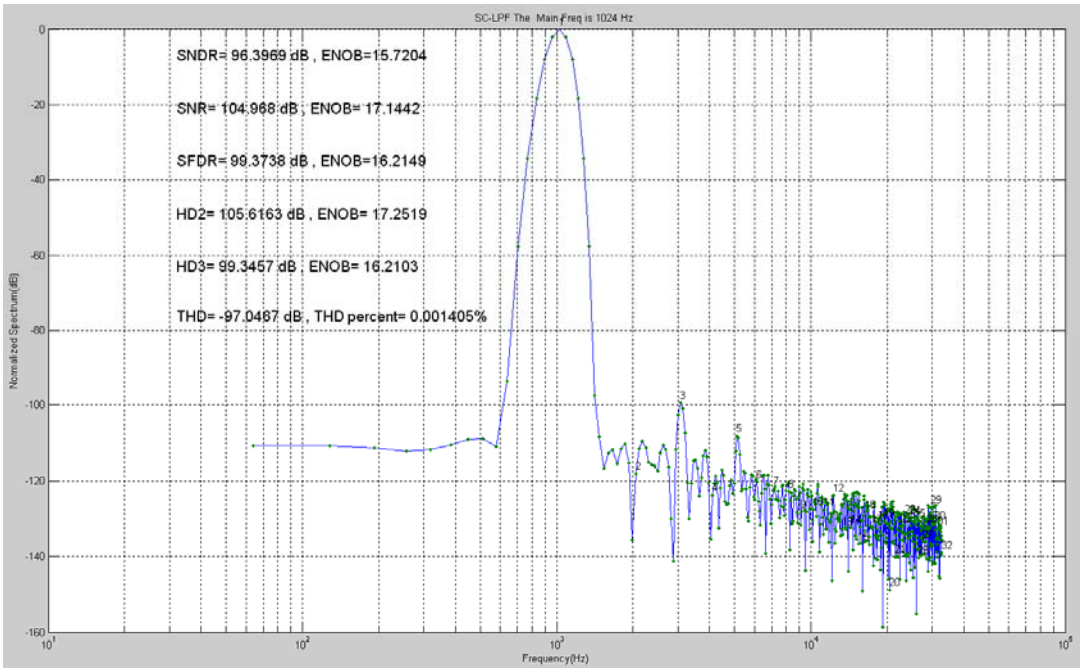
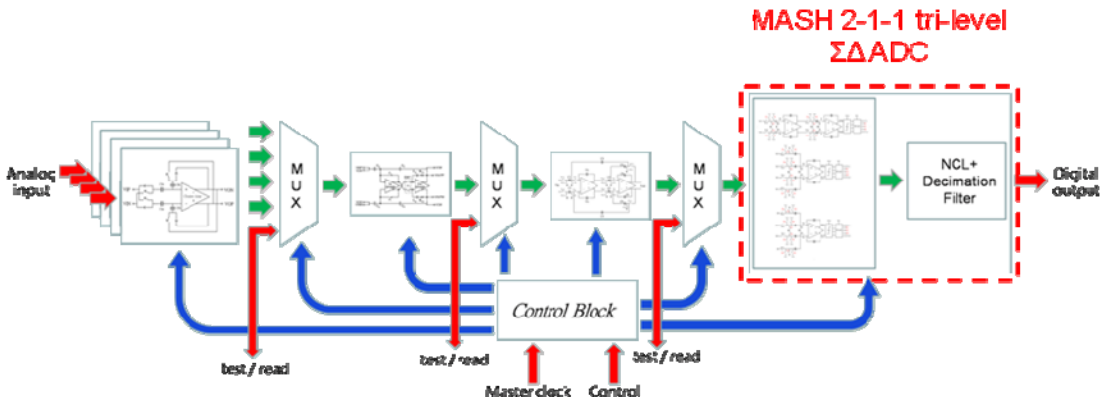


Fig. 3-32 The output of SC-LPF in frequency-domain (worst case)

SPEC	SCLPF
Supply Voltage	1.8 V
Power Consumption	124.48 uW
Gain	0 dB
Nonlinearity	0.001405%
Bandwidth	Sampling rate/32

3.3.4 MASH 2-1-1 tri-level ΣΔ Modulator



The growing trend in biomedical signal processing is to shift more signal processing from the analog to the digital domain. This implies that the analog-to-digital converter (ADC) is moved toward the front-end system with less analog preprocessing, which makes the performance requirement more stringent.

The target performance of an ADC has at least 90-dB signal-to-noise ratio (SNR) and 100-dB spurious-free dynamic-range (SFDR) with a bandwidth exceeding 1 kHz. This design presents a 16-b 2 kHz output-rate ADC, which achieves these performance and reduces power dissipation. This ADC development involves a key design issue. That is a sigma-delta modulator (SDM) topology feasible at a low oversampling ratio (OSR) of 32. This is important for integration with the decimation filter. The resulting sampling clock of 64 kHz makes digital switching noise easier to manage, and a cost-effective single-chip solution possible. Also, a lower sampling clock will relax speed requirements in the analog circuits, and hence reduce power dissipation. In this development, an architectural approach that combines merits of cascaded SDM structures and tri-level quantization makes all quantization noise sources negligible at 32 OSR. As a result, the entire noise budget can be given to analog noise sources to reduce analog power dissipation.

Cascaded SDM structures realize high-order noise shaping by cascading sigma-delta stages of second order or lower to avoid instability, and are suited for ADCs with low OSR. A common choice is fourth-order noise shaping implemented as a 2-1-1 cascaded SDM, as shown in Fig. 3-33

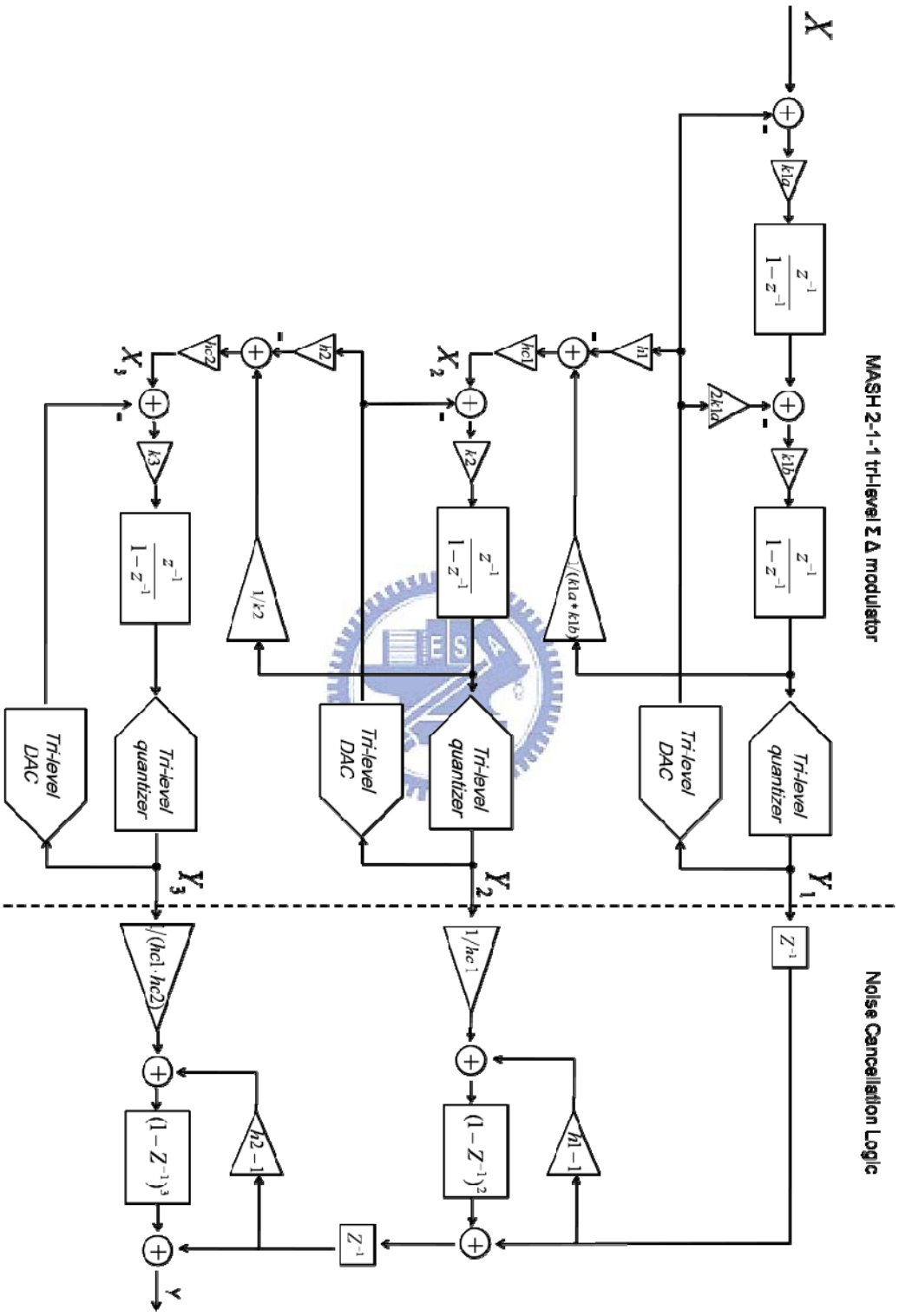


Fig. 3-33 MASH 2-1-1 tri-level ΣΔ modulator with noise cancellation logic

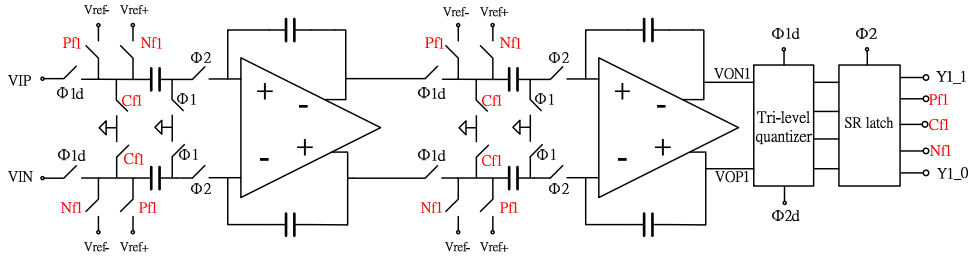
In a cascaded structure, the quantization noise of the preceding stage is extracted and fed to the following stage. As a result, the digital output of the following stage includes information of quantization noise for both the preceding stage and itself. By replicating the noise transfer function of the preceding stage in the noise cancellation logic (NCL), the quantization noise can be cancelled using the digital representation. Ideally, quantization noise of only the final stage suppressed by the total noise- shaping order appears at the SDM output, which is usually referred to as theoretical quantization noise (TQN)[31].

$$N_{TQN} = \frac{1}{(1+H)^3} \cdot \frac{1}{1+K_3 H} \cdot \frac{1}{h_{c1} h_{c2}} e_3 \qquad (3\text{-}18)$$

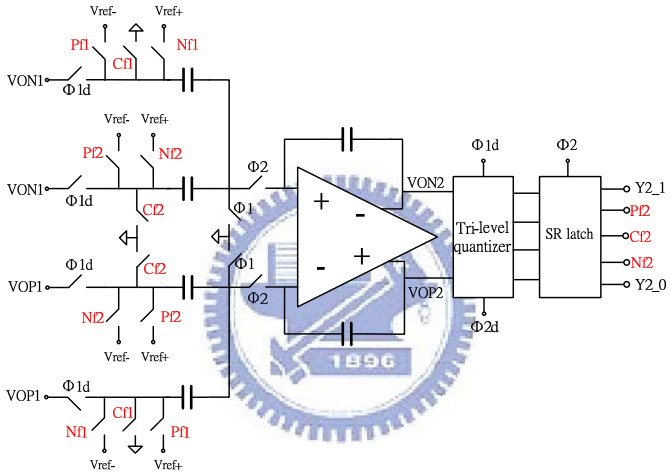
where H is the transfer function of integrator, e_3 is the quantization error of third stage. The implementation of MASH 2-1-1 tri-level ΣΔ modulator is shown as Fig. 3-34

ΣΔ Modulator

SDM 1st stage



SDM 2nd stage



SDM 3rd stage

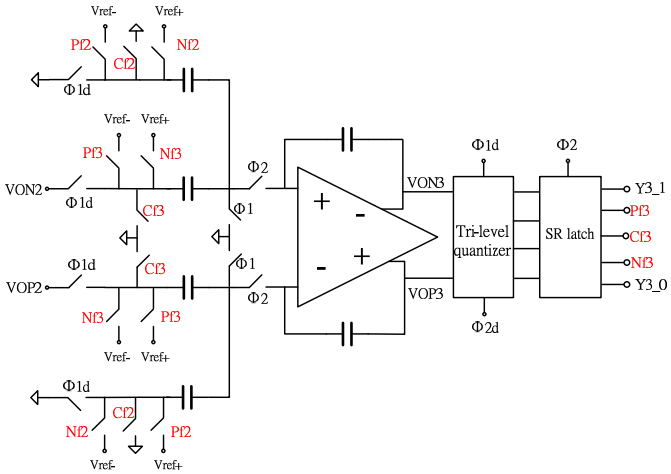


Fig. 3-34 The SC diagram of MASH 2-1-1 tri-level ΣΔ modulator

The fully differential SC increased signal dynamic range (DR), higher immunity to clock and charge feed-through, and rejection to the common-mode noise. The circuit is operated with two non-overlapping clock phases, in the phase ϕ_1 the sampling capacitors are charged, while in the phase ϕ_2 this charge is transferred to the integrating capacitors. In an SC system, the smallest capacitor usually generates the largest thermal noise. The size of the smallest capacitor needs to be determined according to the $\frac{kT}{C}$ equation, since the thermal noise injected at the input cannot be shaped. Their sizes need to be carefully selected to prevent significant SNR loss due to the thermal noise limitation. The relationship between the modulator's SNR and its input capacitor is given by

$$SNR = \frac{(2 \cdot V_{ref,pp})^2}{2} \cdot \frac{C_{in} \cdot OSR}{4kT} \tag{3-19}$$

where $V_{ref,pp}$ is the peak-to-peak value of the reference voltage V_{ref}, C_{in} is the input capacitance, k is the Boltzmann's constant (1.381×10^{-23} Joules/K), T is the temperatiire in Kelvin[32].

Conventionally, 1-b quantization has been used in the cascaded stages because of its inherent linearity. In this ADC, a signal-to-quantization-noise ratio (SQNR) substantially lower than the 90-dB SNR target is required. On the other hand, the use of the multibit quantizer requires dynamic element matching (DEM) algorithm to solve the nonlinear problem of multibit digital-to-analog converters (DACs). The DEM circuit usually consume considerable power and cost additional silicon area. Thus, we use the tri-level quantizer to meet the requirements. The structures of tri-level quantizer and SR-latch are shown as Fig. 3-35. Each stage use a tri-level quantizer and two SR-latch to generate the required output and feedback control signal.

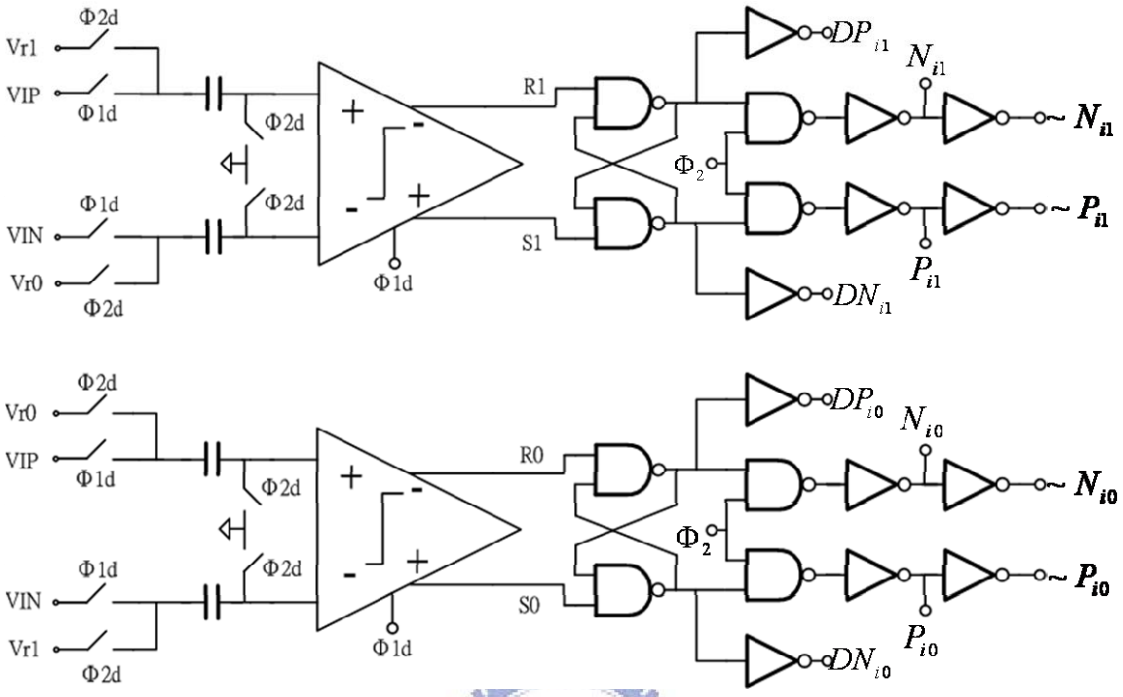


Fig. 3-35 Tri-level quantizer and SR-latch (i=1~3)

where Vr1=+Vref/3, Vr0=−Vref/3, the output and feedback signal of each stage are constituted by the output of two SR-latch as shown in Fig. 3-36

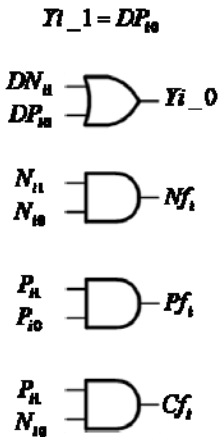


Fig. 3-36 The output and feedback control signal (i=1~3) of each stage

To meet the required DC gain. Thus, usually a two-stage amplifier is needed. Fig. 3-37 shows the used opamp[28]. It is based on a fully differential folded-cascode p-type two-stage Miller-compensated configuration. The second stage is a common-source amplifier with active load which also allows a large output swing (-1.77 V~+1.77 V).

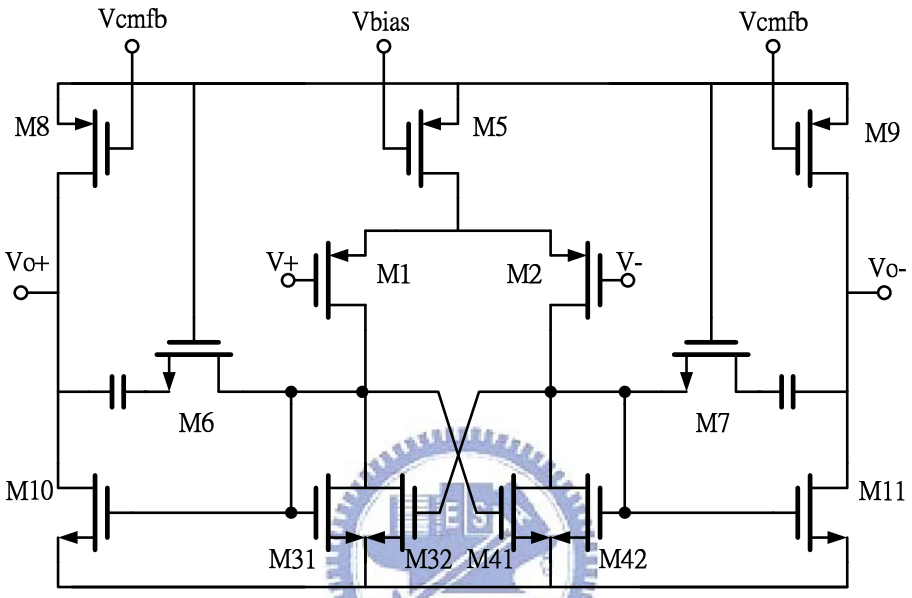


Fig. 3-37 Two stage operational amplifier

The performance of the modulator is greatiy influenced by the accuracy of its integrators, especially the one at the front input. The integrator's accuracy, defined by its fransient behavior, is govemed by the slew rate and unity-gain bandwidth of the amplifier. These two specifications are critical to the design of the modulator. The integrator's output is arranged to settle to its final value at half (50%) of the on-period of the clock, $T_s/2$. The difference between the integrator's output at the half of $T_s/2$ and its ideal value is defined as the integration error, ε, which limits the maximum accuracy that the modulator can achieve[38-39].

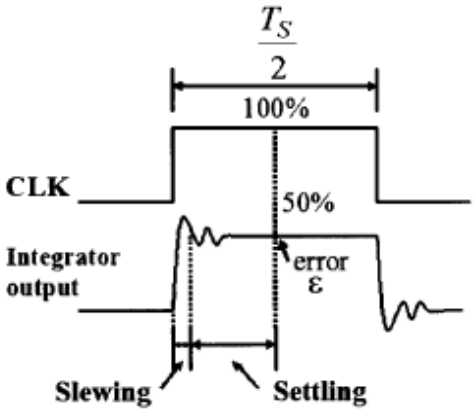


Fig. 3-38 The transient behavior for the modulator[26].

The amplifier's slew rate can be expressed as

$$SR = \frac{\Delta V \cdot 2f_s}{k_{SR}} \tag{3-20}$$

where ΔV is the maximum output of integrator, k_{SR} is the integrator's slewing factor in percent of $T_s/2$, and an equation associated with the amplifier's unity-gain bandwidth and its sampling frequency can be obtained as

$$f_u = \frac{\Delta V \cdot f_s}{\pi \cdot k_{ST} \cdot V_{ref}} \cdot ln\left(\frac{1}{\varepsilon}\right), \tag{3-21}$$

where f_u is the amplifier's unity-gain bandwidth in hertz, k_{ST} is the settling factor of the integrator in percent of $T_s/2$, and ε is the integration error.

The comparator is appropriate for high-speed and low-power applications, and it operates as follows. During the *reset* mode (i.e., Φ_{1d} is low), the outputs are connected to *VDD* through M9 and M10. When Φ_{1d} goes high, the comparator enters the *regenerative* mode and transistors M3–M8 form a positive feedback loop. As a result, the input difference voltage is amplified to a full-scale rail-to-rail output. Once the comparator makes a decision, the crosscoupled transistors M3,4 and M7,8 immediately shut down all the connections between *VDD* and *VSS*, thereby saving power. This process may be better understood by looking at Fig. 3-39: When in+ is high and in- is low, out- becomes low and out+ becomes high. As a result, M3 and M8 are on, whereas M4 and M7 are off and hence the comparator is turned off[33].

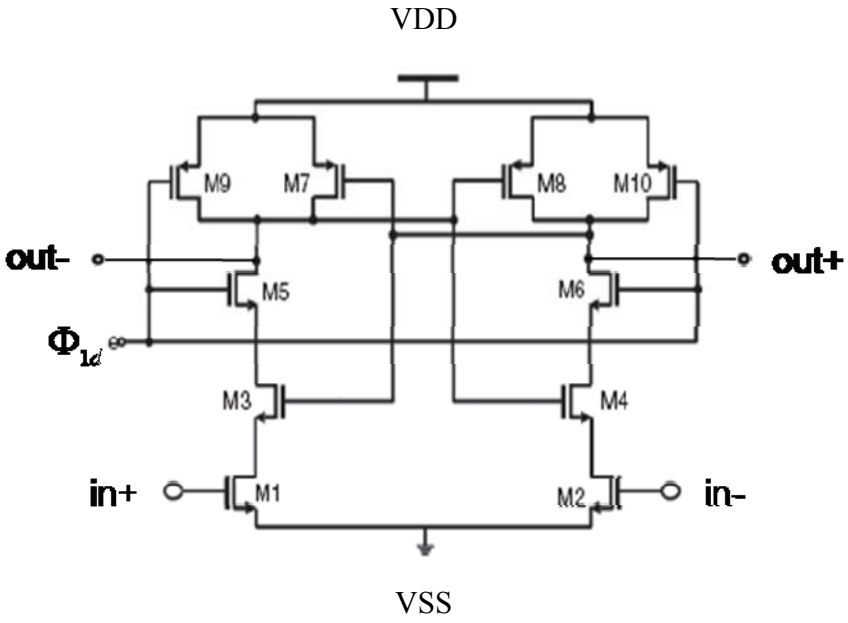


Fig. 3-39 Comparator[30]

Pre-layout simulation

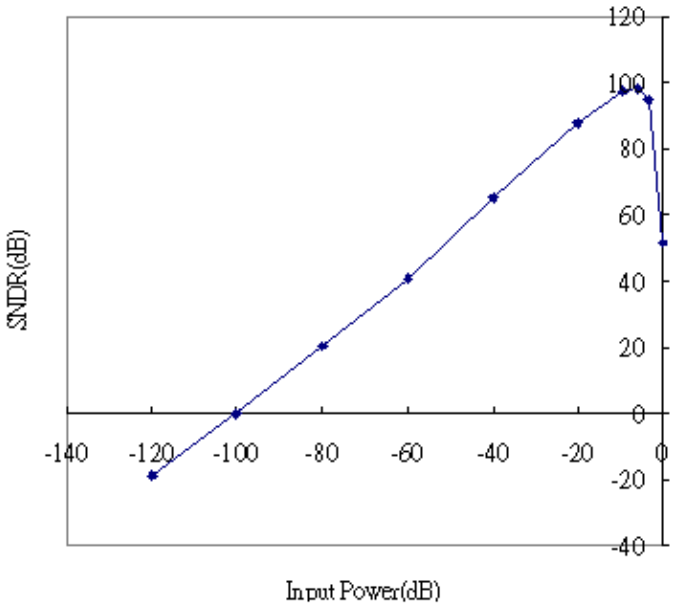


Fig. 3-40 Plot of simulated SNDR versus input level

Input testing signal:

Input signal type: sine wave

Input signal frequency: 1.024 kHz (the max frequency that system to process)

Input signal amplitude: 0.82 V

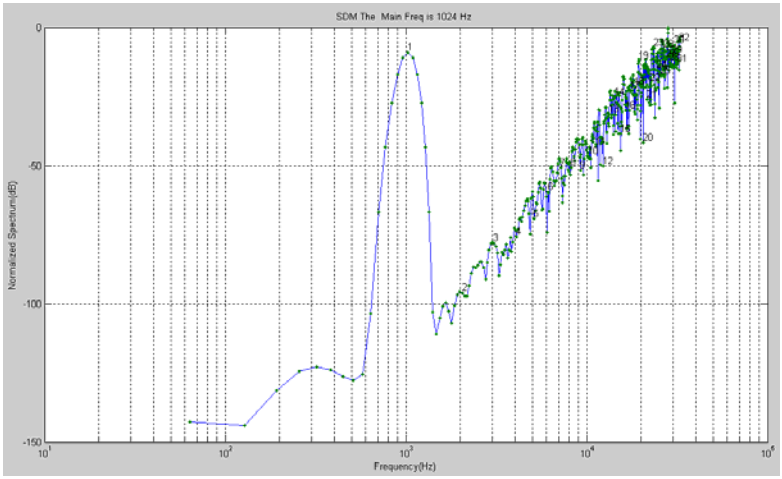


Fig. 3-41 Output PSD of MASH 2-1-1 tri-level ΣΔ modulator at 64 kHz sampling rate

SPEC	ΣΔ-ADC
Supply Power	1.8 V
Power Consumption	271.7 uW
Gain	0 dB
Sample Rate	65.536 kHz
Bandwidth	1.024 kHz
SNDR	95.1 dB
Resolution	16-bit

3.3.5 Digital Decimation Filter

Filtering noise which could be aliased back into the baseband is the primary purpose of the digital filtering stage. Its secondary purpose is to take the data stream that has a high sample rate and transform it into a 16-bit data stream at a lower sample rate. This process is known as decimation. Essentially, decimation is both an averaging filter function and a rate reduction function performed simultaneously. High resolution is achieved by averaging over 32 data points to interpolate between the coarse quantization levels of the modulator. The process of averaging is equivalent to lowpass filtering in the frequency domain. With the high frequency components of the quantization noise removed, the output sampling rate can be reduced to the Nyquist rate without aliasing noise into the baseband.

The simplest and most economical filter to reduce the input sampling rate is a "Comb-Filter", because such a filter does not require a multiplier. A multiplier is not required because the filter coefficients are all unity. This comb-filter operation is equivalent to a rectangular window finite impulse response (FIR) filter. By considering the case when the down-sampling factor can be expressed as

$$M = M_1 \cdot M_2 \cdot M_3 \tag{3-22}$$

and the comb transfer function as

$$H(z) = \left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^K = \left[\prod_{i=1}^{N}\frac{1}{M_i}\left(\frac{1-z^{-\prod_{j=1}^{i}M_j}}{1-z^{-\prod_{j=0}^{i-1}M_j}}\right)\right]^K;\ M_0 = 1 \tag{3-23}$$

In this design, for M=32 and N=3, we can select

$$M_1 = 4, M_2 = 4, M_3 = 2 \tag{3-24}$$

Using equation (3-22)~(3-23), we can modified comb filter $H_m(z)$ as

$$H_m(z) = H_1^{k1}(z)H_2^{k1}(z^4)H_3^{k3}(z^{16}) \tag{3-25}$$

where k_i is the number of the cascaded filters H_i. (H_2 and H_3 can be removed to the lower rate[34]). To improve the magnitude characteristic of the filter we use the cascaded cosine prefilter[35], [36] and sharpening technique[37] , we can obtain

$$H_{ShCCOS}(z) = H_1^{k_1}(z)Sh\left\{H_2^{k_2}(z^4)\right\}Sh\left\{H_3^{k_3}(z^{16})\right\}\times H_{COS}^{n_1}(z^8)H_{COS}^{n_2}(z^4). \tag{3-26}$$

where $$Sh\left\{H_i^{k_i}(z)\right\} = \left[H_i(z)\right]^{2k_i}\left\{3z^{-(M_i-1)k_i/2} - 2\left[H_i(z)\right]^{k_i}\right\} \tag{3-27}$$

we select $k_1 = 4, k_2 = k_3 = 2$ and $n_1 = 4, n_2 = 2$

$$H_{ShCCOS}(z) = H_1^4(z)Sh\{H_2^2(z^4)\}Sh\{H_3^2(z^{16})\}H_{COS}^4(z^8)H_{COS}^2(z^4)$$

(3-28)

finally, the signal flow gragh of digital decimation filter is shown as

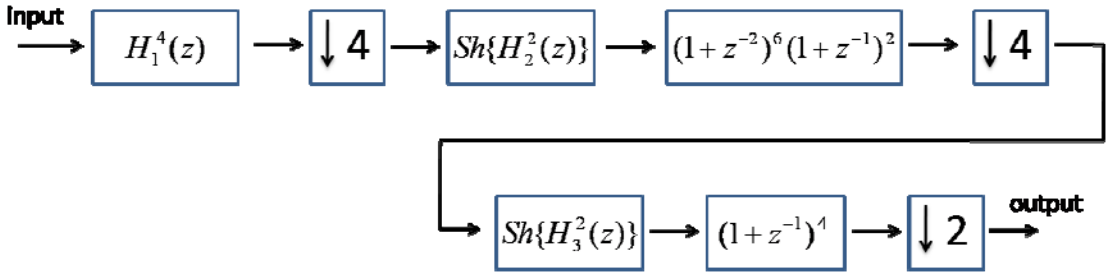
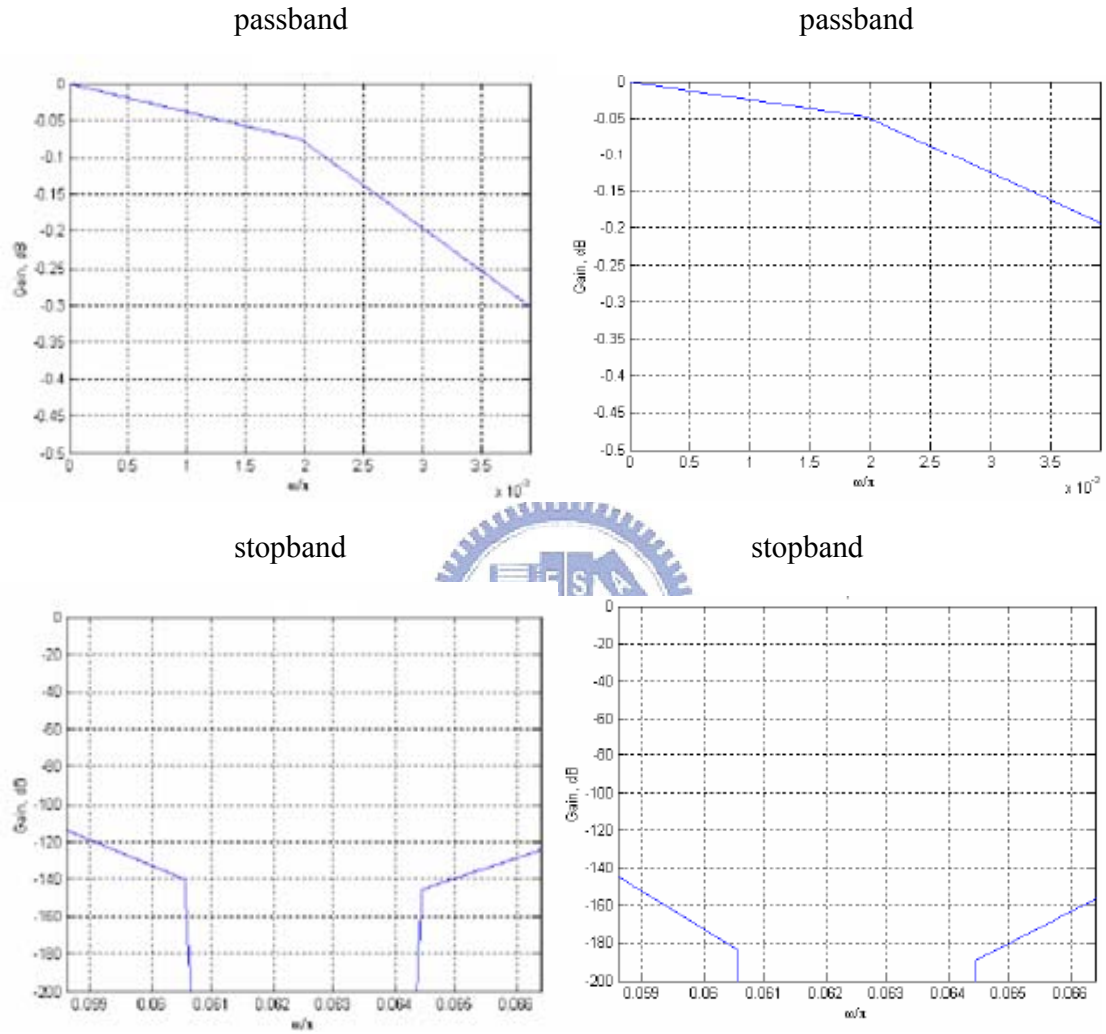


Fig. 3-42 Signal flow gragh of digital decimation filter

The corresponding magnitude response for decimation filter with cosin filter, sharpening technique and without cosin filter, sharpening technique, respectively, shown as Fig. 3-43 (a) and (b).



(a) (b)

Fig. 3-43 magnitude response of decimation filter[40]

3.3.6 Wide-Swing Constant-Gm Cascode Biasing Circuit

The architecture of the wide-swing constant-Gm cascade biasing circuit is shown as Fig. 3-44. It can be divided into three parts: The first part is a bias loop which is composed of high-swing cascode current mirror [41] to provide a stable current source. On the presupposition of low power consumption, the current mirror used about 1uA to drive the core circuit. The second part is a cascode bias which utilizes the current mirror to copy the current of bias loop and utilizes the cascode structure to bias voltage. The third part is a start-up circuit. Because this structure adopts the wide-swing and constant-Gm, the biasing circuit must add a start-up circuit to maintain the circuit in a correct state at any time. The concepts of the start-up circuit are low consumption and no effects on the biasing circuit. The start-up circuit will revise the voltage in order to maintain the biasing circuit in a normal operational state following the feedback during the biasing circuit only when the biasing circuit is operated abnormally.

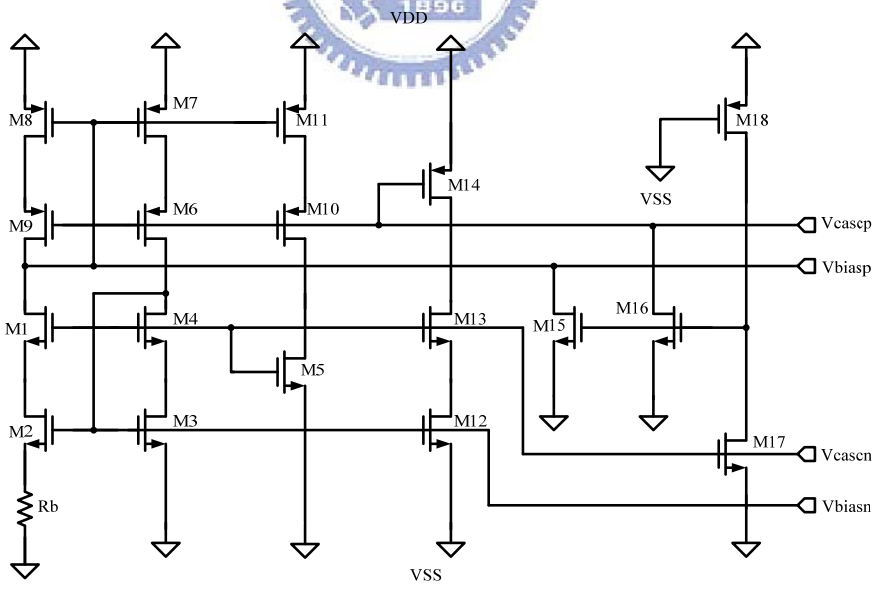


Fig. 3-44 The architecture of the biasing circuit.

Chapter 4
Chip Implementation, Verification and Test Platform

4.1 Design Flow

While design the suitable MSFEIC for acquiring biomedical signals, we observed the characteristics of the biomedical signals first, for example, different biomedical signals have different amplitude and frequency. Then we consulted other structures of the circuit proposed by other laboratories and the first generation AFEIC design to think that the drawbacks of design and practical applications. Revise and improve the drawbacks, and design more complete structure. And then we utilized HSPICE to design the circuit with transistor level and simulate the pre-layout simulation. After MSFEIC passed the pre-layout simulation, we utilized Laker tools to layout the circuits, verified the layout (Calibre DRC、LVS、PEX), and simulated the post-layout simulation. We checked the specification with conformability to improve the practicability of the MSFEIC. After the chip is manufactured, we will test the characteristic and analyze the different between the simulation and the result of testing. The design flow is shown as Fig. 4-1

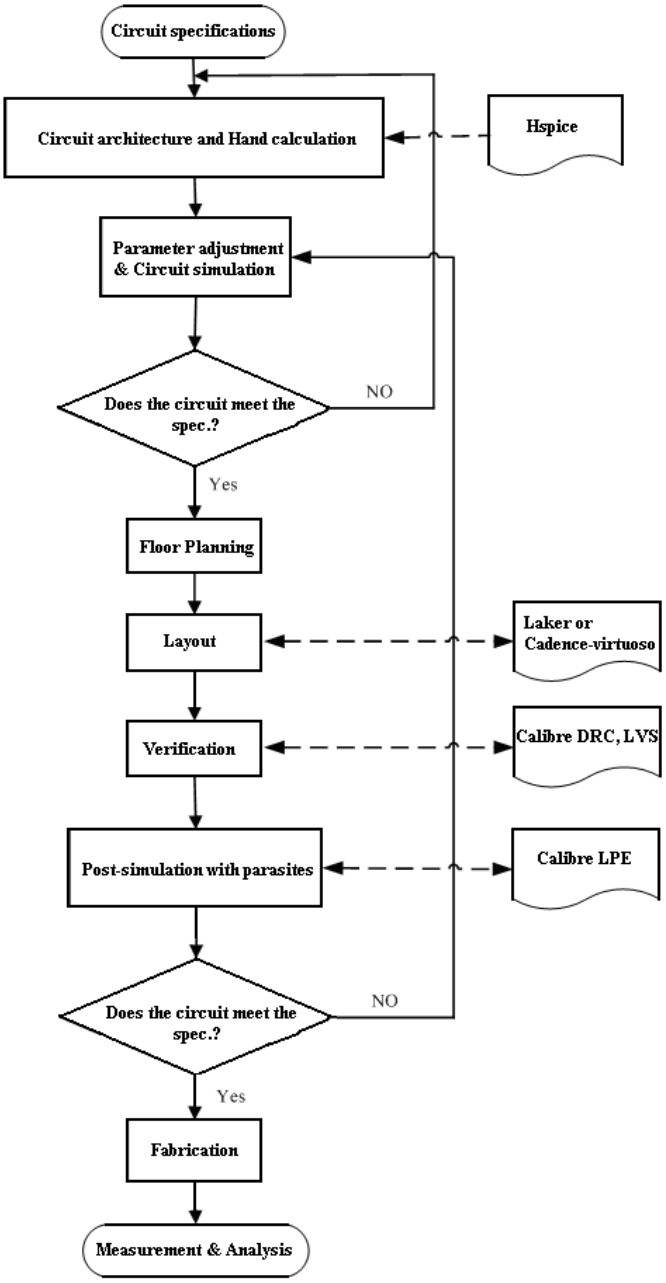


Fig. 4-1 Design flow

4.2 Layout Consideration and Implementation

Analog circuits have high processing sensitivity, so we must consider the place when layout the circuit. The fundamental consideration of analog circuit layout is matching, so it should add dummy cells to protect the elements in order to reduce errors in the VLSI process. In the core circuit parts, we used a guard ring to isolate the passive elements and to avoid the surrounding noise affecting the performance of the core circuit. Therefore, we used a double-layer guard ring in the layout to isolate the core analog circuit, digital controlling circuit, and passive elements (resistors and capacitors array).

The unit capacitor is 50fF and is cut the angle of 45 degrees neatly in this design. It is composed of two metal boards (M5, M6). We utilized the unit capacitor to arrange into a necessary capacitor array, and added dummy cells, and surrounded a guard ring with six contacts. The unit high P+ poly resistor with RPO is 5kΩ. We utilized the unit resistor to arrange into a necessary resistor array, and added dummy cells, and surrounded a guard ring with six contacts.

Fig. 4-2 is the complete MSFEIC layout containing electrostatic discharge (ESD) pads. The area of the core circuit is 1.9198×1.9198 mm^2. Due to the chip is composed of analog signals and digital signals circuit, layout needs to pay attention to the following notices.

(1) In order to avoid noise by the high frequency signals coupling to the analog circuit, we utilized resistors and capacitors to isolate the analog circuits and digital circuits.

(2) Separate the analog power supply and digital power supply and be distant from each other. The power supplies are used different pads to connect with outside to increase PSRR of the analog circuit.

(3) In the sensitive circuit, add one or more guard ring layers to protect the circuit from noise effects.

(4) If accuracy of resistors or capacitors is expected much, capacitors must use common centroid layout and resistors must use intersection layout.

(5) The differential input pairs, for example the differential input pair of OP, are possible symmetry in the layout.

(6) Choose the pads with ESD protection to reduce the effects of latch up.

(7) Add dummy cells around the passive elements to avoid the imperfect etching.

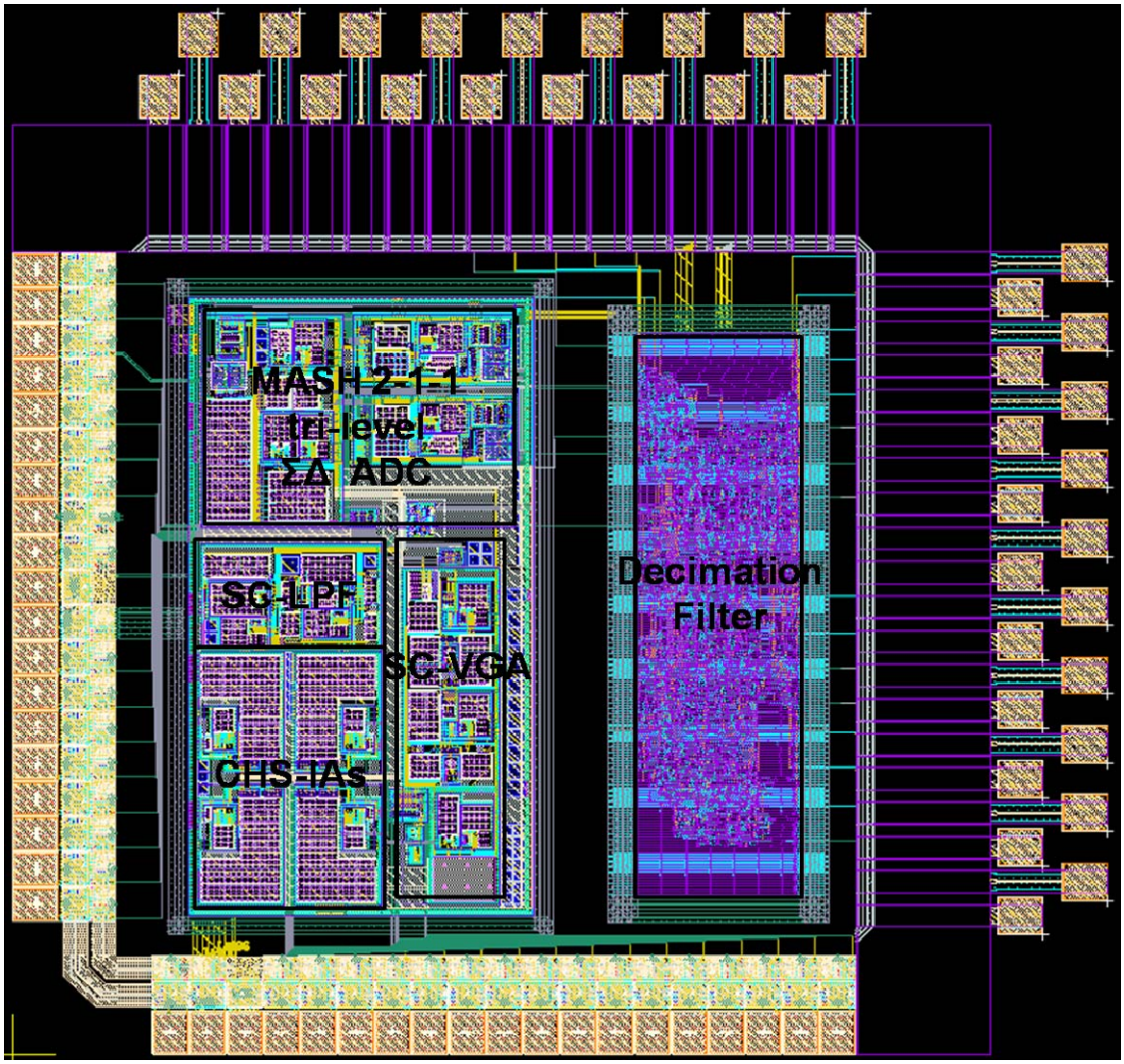


Fig. 4-2 Complete MSFEIC layout.

4.3 Post-Layout Simulation

System input testing signal:

Input signal type: sine wave

Input signal frequency: 1.024 kHz (the max frequency that system to process)

Input signal amplitude: 213 uV

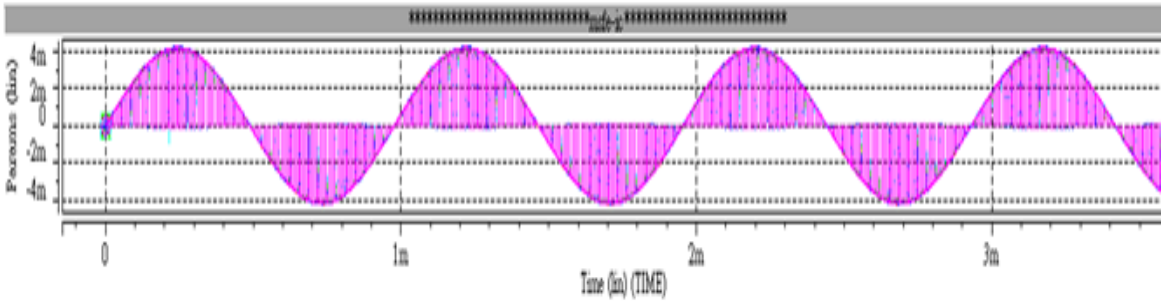


Fig. 4-3 output of CHS-IA

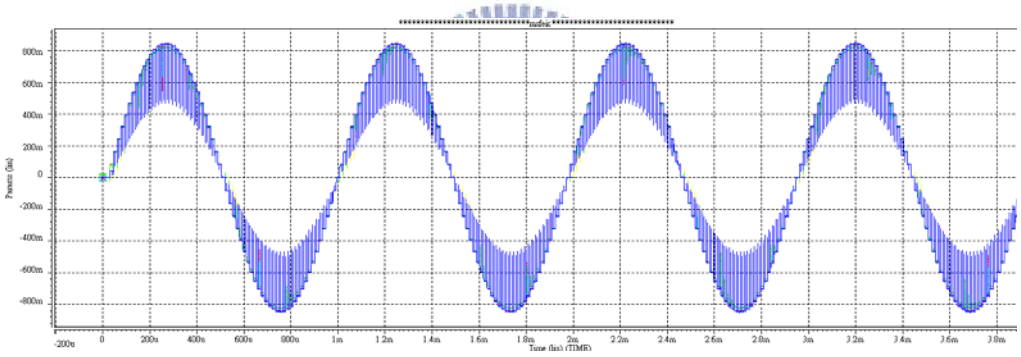


Fig. 4-4 output of SC-VGA for gain=72 dB

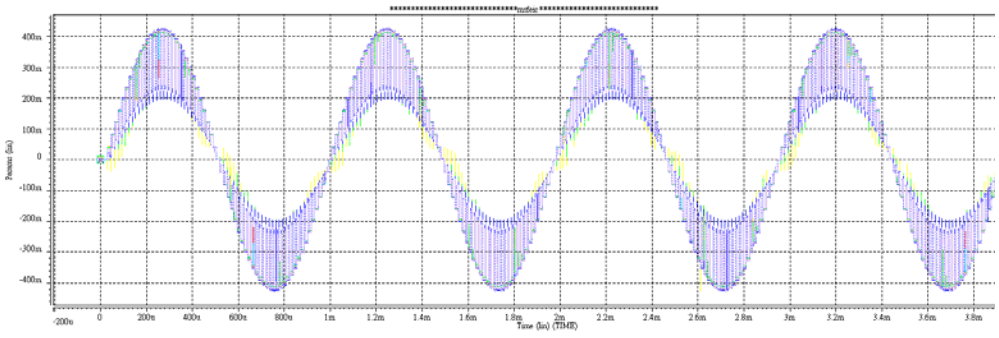


Fig. 4-5 output of SC-VGA for gain=66 dB

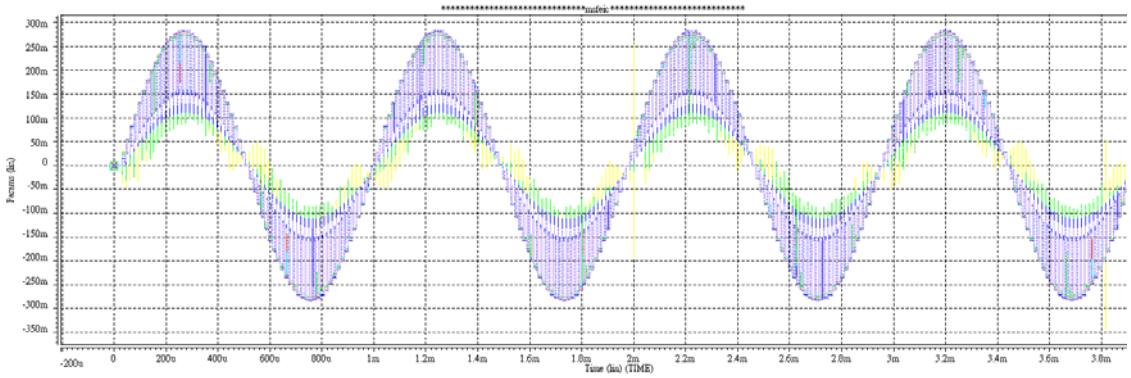


Fig. 4-6 output of SC-VGA for gain=60 dB

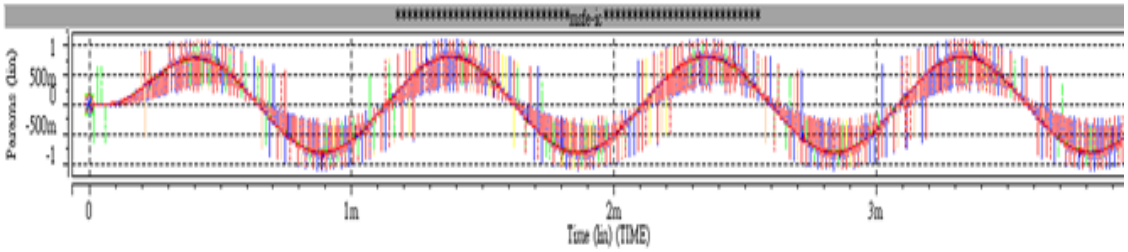


Fig. 4-7 output of SC-LPF

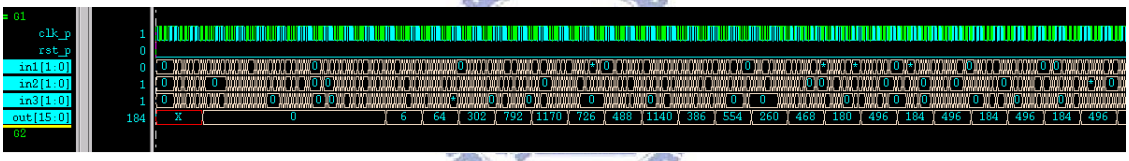


Fig. 4-8 output of MASH 2-1-1 tri-level ΣΔ-ADC

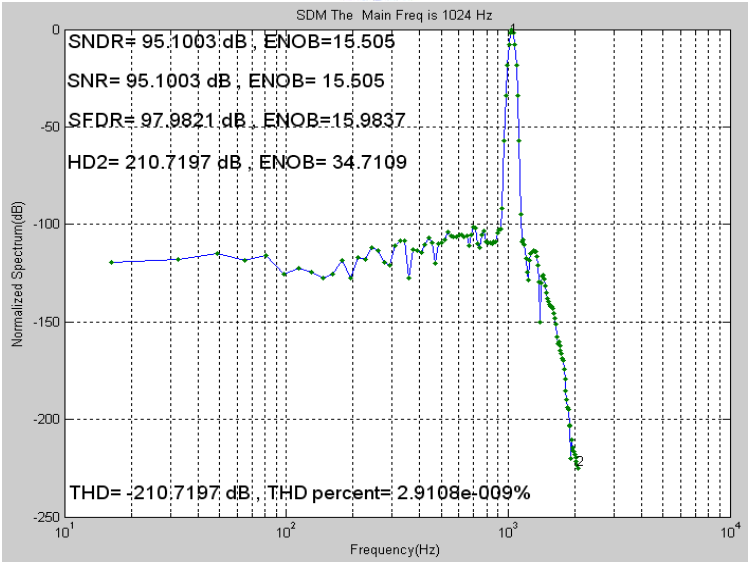


Fig. 4-9 PSD of system output

4.4 Specification Comparison

The specification of MSFEIC design in this thesis is shown as Table 1, Table 2, and Table 3 summarizes the comparison results among the proposed MSFEIC and the conventional designs. It can be seen that the proposed MSFEIC offers reasonable low power, high signal-to-noise ratio(SNR) performance. In terms of area size, the proposed four-channel MSFEIC is fully implemented with relative small size. Importantly, by integrating digital interface, the MSFEIC has the selectable system gain and bandwidth.

Table 1 The specification of MSFEIC.

Process Technology	**TSMC 0.18um 1P6M**	
	Pre-Simulation	**Post-Simulation**
Supply voltage	1.8V	1.8V
DC Gain (Max.)	72dB	71.5dB
CMRR (DC~1 kHz)	> 140dB	> 136dB
PSRR+ (DC~1 kHz)	> 120dB	> 117dB
PSRR- (DC~1 kHz)	> 120dB	> 117dB
Bandwidth	Selectable	Selectable
Input Resistance	1.000e+20 Ω	1.000e+20Ω
ADC Resolution	16-bit	16-bit
Sampling Rate	65.536 kHz	65.536 kHz
Power consumption	Analog: 787.51uW Digital: 210.49 uW	Analog: 787.51uW Digital: 210.49 uW

spec	CHSIA	SCVGA	SCLPF	ΣΔ-ADC
Supply voltage	1.8 V	1.8V	1.8V	1.8V
Power consumption	72.61 uW	104uW	124.48uW	modulator 271.7 uW decimation 20uW
Gain	26 dB	34~46dB	0dB	0dB
nonlinearity	<0.00135%	<0.0056%	<0.001405%	-
Gain step	-	6 dB	-	-
Sample Rate	65.536 kHz	65.536 kHz	-	65.536 kHz
BandWidth	2 kHz	2 kHz	Sampling rate / 32	1.024 kHz
SNDR(dB)	-	-	-	95.1
Resolution	-	-	-	16bit

Table 2 The comparison MSFEIC (analog) with relevant papers.

Parameter	**Ref [1] TIM 1998**	**Ref [2] ESSCIRC 2006**	**Ref [3] JSSC 2007**	**The 1st circuit ISCAS 2008**	**This Work**
Technology	2.4um CMOS	0. 5um CMOS	0.5um CMOS	0.35um CMOS	0.18um CMOS
Supply Voltage (V)	+/- 4.5	3	3	+/- 1.5	1.8
No. of Channel	16	8	1	1	4
Core Area (mm^2)	24	12	1.95	0.268	0.406
Mid-Band Gain (dB)	Up to 74	66-79	51.82 - 67.96	52.66 - 80.45	60-72
Current Consumption per Channel (uA)	520	92.6	20	47.468	71.6
Power Consumption per Channel (uW)	292.5	100	60	150.7682	128.95
Input Referred Noise (uVrms)	1.39	0.93	< 0.7	2.417	<0.06
Bandwidth (Hz)	0.3 - 150	Selectable	Selectable	Selectable	Selectable
CMRR (dB)	99	130	> 120	145	136
PSRR+ (dB)	40 @10Hz	N/A	80 @50Hz	131 @50Hz	117 @50Hz
PSRR- (dB)	N/A	N/A	78 @50Hz	118 @50Hz	117 @50Hz

Table 3 The comparison ΣΔ-ADC with relevant papers.

parameter	**IEEE, 2001 [4]**	**ESSCIRC, 2002 [5]**	**ISSCC, 2005 [6]**	**ESSCIRC, 2006 [7]**	**ISCAS, 2008 [8]**	**Previous generation**	**This work**
topology	2nd	2nd	2nd	2nd	2nd	2nd	4th
Signal type	Audio	ADSL	WCDMA	Audio	GSM	biosignal	biosignal
BW (Hz)	8k	300k	1.94M	312k	100k	1.25k	1.024k
OSR	64	96	20	16	128	256	32
SNDR (dB)	49.7	82	63	65	85.7	60	95
Technology (um, V)	0.6 , 3.3	0.18 , 1.8	0.09 , 1.2	0.09 , 0.6	0.18 , 1.8	0.18 , 1.5	0.18 , 1.8
Size ($\mathbf{mm^2}$)	N/A	N/A	0.2	2.2	N/A	0.3	0.252
Power (mW)	6.996	9	1.2	7.2	4.2	0.98	0.291
FOM (uW/step)	27.33	1.1	1.17	3.52	0.26	0.96	0.004135

$$FOM = \frac{Power_{modulator}}{2^{ENOB}}$$

4.5 Test Platform Design

The architecture of testing the chip is shown as Fig. 4-10. Its purpose confirms that whether the chip can operate correctly or not. Test the performances of amplification, filter, and eliminating noise in the MSFEIC. The equipments of testing the chip include function generators, an oscilloscope, power supplies, etc. The testing step is as following.

(1) Adjust the power supply to proper voltage supply, and connect to the analog voltage supply (0/1.8V), digital voltage supply (0/1.8V), and ESD voltage supply (0/1.8V). In order to avoid 60Hz noise with power supply, we must add a capacitor and a resistor to filter the noise.

(2) Input the simulated biomedical signal sine wave, which is produced by the function generator, to the CHS-IA.

(3) Input voltage to digital selected input of the multiplexer to pass a channel which we want to analyze.

(4) Set the sampling frequency of SC-LPF by the function generator producing a suitable clock.

(5) Input voltage to digital selected input of the decoder to choose appropriate voltage gain by passing the resistor switch.

(6) Connect the output of SC-VGA to an oscilloscope to observe the output wave of the MSFEIC.

(7) Outputs of the multiplexer and decoder have pins. If the multiplexer or decoder is failure, input the signals to the output of the multiplexer or decoder to test other analog circuits.

(8) Calculate the various specifications utilizing logical analyzer and computer

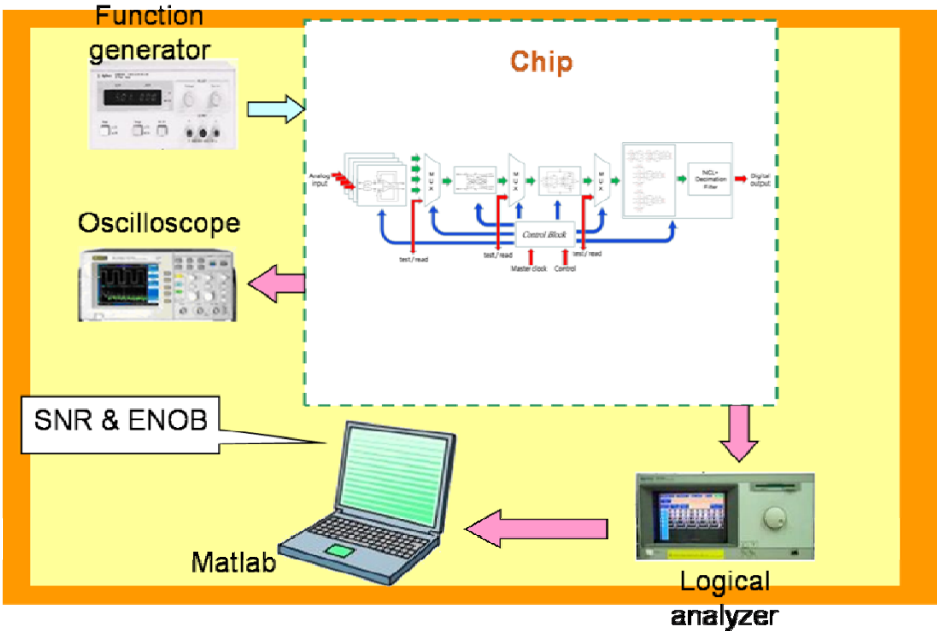


Fig. 4-10 Test Platform

Chapter 5 Conclusions

5.1 Conclusion

The study realized a tunable bandwidth/gain circuit design of multi-channel biomedical signals acquisition. Focus on low power consumption and low noise. The MSFEIC is integrated on a chip, that is SoC, and it has advantages of low cost and size. It is conducive to integrate the embedded biomedical system. The feature of MSFEIC is that utilized the characteristic of self-circuit to reduce additional circuit design and area. Multi-channel design shared a SCFLP and a PGA to reduce the area of the circuit, SCFLP utilized different clock frequency to select different bandwidth of the system, and SC-VGA utilized different CMOS switches in parallel capacitor to select different gain ratio.

5.2 Future Work

The thesis has had superiority in the biomedical signals recording system according to the result of the MSFEIC post-layout simulation. However, the MSFEIC is still worth improving further in the future. For example, reduce the phase delay in the SC-LPF, consume lower power, use battery to supply the power of MSFEIC, integrate with digital signal processing circuit, etc.

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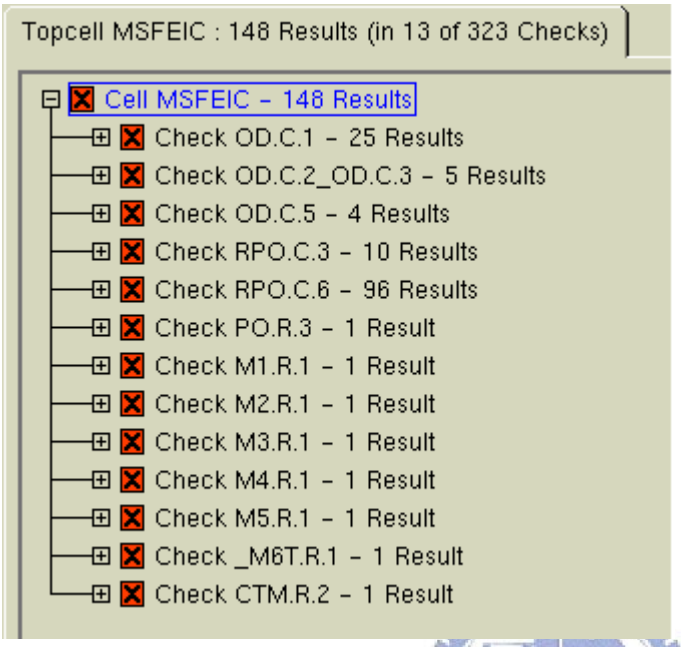
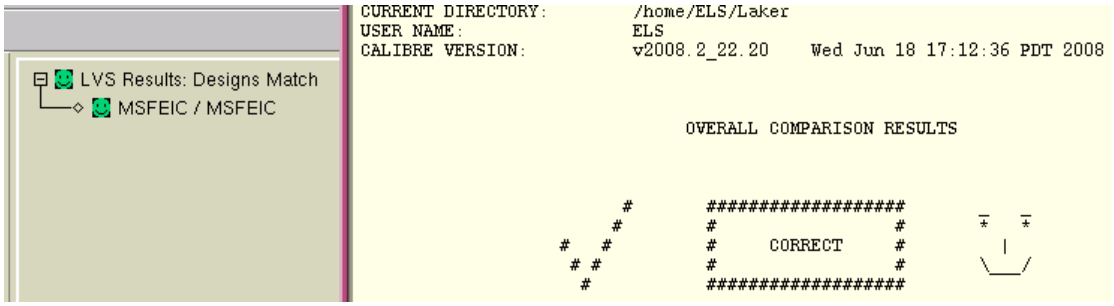
Appendix

A. DRC Verification



上表為 DRC report 的錯誤訊息表，其中 OD.S.1 & OD.C.1 & OD.C.5 & RPO.C.3 & RPO.C.6 為 IO PAD 中的假錯，CTM.R.2 為電容假錯，可忽略。而 PO.R.3 & M1.R.1 & M2.R.1 & M4.R.1 & M5.R.1 & _M6T.R.1 是因為使用 CIC 的 cell based design 所以佈局中的 cell 還未放入佈局中，所以會造成 poly 和各層 metal 的錯誤，其也為假錯。

B. LVS Verification



C. Tapeout Review Form (for Full-Custom IC)

Tapeout review form 的用意在提醒設計者在設計、模擬、佈局、佈局驗證及 tapeout 時具備設計理念及了解應注意事項,希望能藉此提昇晶片設計的成功率及達到完整的學習效果。因此,請指導教授及設計者確實檢查該晶片設計過程是否已注意本表格之要求,並在填寫確定後簽名,若審查時發現設計內容與 Tapeout Review Form 之填寫不符,很可能遭取消該晶片下線製作資格。可參考本表後所附範例確實填寫。

專題名稱:A CMOS Mixed-Signal Front-End IC for Portable Biopotential Acquisition System

Top Cell 名稱:MSFEIC

製程名稱:TSMC 0.18 UM CMOS Mixed Signal RF General Purpose MiM AI 1P6M 1.8&3.3V

1 電路概述

1-1. 工作電壓:1.8V

1-2. 工作頻率:65.536kHz

1-3. 功率消耗:類比:978uW total:998uW

1-4. 是否使用 CIC 提供之 ARM CPU IP? NO

使用 CPU 之種類為何?(ARM7TDMI or ARM926EJ)

1-5. 此電路架構於貴實驗室是否第一次設計?是(接 2-1) v 否(接 1-5-1)

1-5-1. 此電路之前不 work 或 performance 不好的原因為何?

1-5-2. 對之前的錯誤作何種修改?

2　電路模擬考量

2-1.　已用 SS, SF, TT, FS, FF 中哪些不同狀態之 spice model 模擬?_____

SS, SF, TT, FS, FF_____

2-2.　已模擬過電壓變動+/-10%中哪些情況對電路工作之影響?_____YES

2-3.　如何考量溫度變異之影響?_____已測試過溫度變異對整體電路的影響(0 度~90 度)_____

2-4.　如何考量電阻、電容製程變異之影響?_____加入 dummy 及使用對稱佈局法以減少變異影響_____

2-5　模擬時是否加入 IO PAD、Bonding wire 的效應及考量測試儀器之負載等影響?_YES_____

2-6　是否作 LPE 及 post layout simulation?_YES　使用的軟體為

__Laker&Calibre&Hspice

3　Power Line 佈局考量

3-1.　Power Line 畫多寬?_____>5um_____

3-2.　是否考量 power line current density?_____YES_____

3-3.　是否考量 Metal Line 之寄生電阻、電容?_____YES_____

4　DRC, LVS

4-1.　是否有作 whole chip 的 DRC 及 LVS?_____YES_____

4-2.　除了 PAD 上 DRC 的錯誤之外, 內部電路及與 PAD 連接的線路是否有錯?__NO__

錯誤原因為何?_____

4-3.　在作 LVS 的過程中, PIN 腳及元件是否 match?__YES___ 不 match 的原因為何?_____

4-4.　檢查 PAD 與 PAD 間是否有移位、短路或斷路的現

象?_____YES_____

5　類比-混合訊號電路佈局考量(類比-混合訊號電路設計者填寫)

5-1　佈局對稱性及一致性考量

5-1-1　OP(Comparator) Input Stage 是否對稱?_____YES_____

5-1-2　OP(Comparator) Input Stage 是否對稱?____YES_____

5-1-3　佈局中對稱元件是否使用 dummy cell 技巧?____YES_____

5-1-4　對稱電容是否採用同心圓佈局?___YES_____

5-1-5　對稱單位電容四周是否切成 45 度斜角?_____YES_____

5-1-6　對稱電容的單位面積是否一致?___YES_____

單位電容面積多大?___7.399_____um x____7.399____um

單位電容值多大?___0.05_____pF

5-1-7　電阻採用哪一材質製作?___P+ high poly resistor with RPO

單位電阻值多大?_____1k Ohm_____

5-2　電路雜訊佈局考量

5-2-1　是否將 Analog 及 Digital 的 power line 分開?_____YES

5-2-2　Analog area 是否用 guard ring 隔絕?_____YES_____

5-2-3　Digital area 是否用 guard ring 隔絕?_____YES_____

5-2-4　對於 sensitive line 是否使用 shield 的技巧?_____

YES_____

5-2-5　Analog guard ring 及 shield 是否接至乾淨之電位?___YES__

5-2-6　是否將 sensitive line 儘量縮短及避免跨越

noise(clock)line?___YES__

5-2-7　電容的上下極板是否接對?_____YES_____

6　MEMS 設計考量(MEMS 設計者填寫)

6-1 請簡述所進行之後製程：

_____

6-2 後製程操作地點：

_____

6-3 下線者目前是否有操作該製程設備之合法授權?_____若目前無操作該製程設備之合法授權，是否可在晶片取回前得到合法授權?_____

6-4 下線者是否有使用該製程設備之經驗?_____

6-5 是否有該後製程之製程參數（壓力、溫度、流量、……）?_____

6-6 之前是否有成功實現過該後製程?_____

6-7 Layout 違反 design rule 的部分是否會影響微結構本身或元件操作？

___

6-8 Layout 之蝕刻孔尺寸是否足以讓結構懸浮?_____

6-9 元件驅動電壓範圍?_____

7 RF Circuit 電路佈局考量（ RF 操作頻段設計者填寫）:

7-1 電路規格適用何種系統? _____

7-2 說明被動元件模型的來源 _____

7-3 模擬軟體（可不只一種)? _____

7-4 系統整合 chip 裡之各個 block 是否曾下過線且量測符合預期規格(chip 為系統整合者回答,並說明製程梯次代號)?_____

7-5 佈局考量：

7-5-1 元件佈局方式是否與模型提供者所提供的佈局一致? _____

7-5-2 接地與電壓源是否均勻? _____

7-5-3 元件與拉線的電流承載能力考量? _____

7-5-4　拉線是否過長過細? _____

7-5-5　PAD 的佈局是否配合量測上之考量? _____

7-5-6　PAD 與 Bond-wire 的效應是否考量? _____

7-6 DRC 驗證過程中, 部分錯誤若為特殊考量, 請說明

_____

_____

_____

_____

_____

_____

7-7 LVS 驗證過程中, 電感電容或其他特殊元件的比對是否做過處理, 請說明_____

_____

_____

_____

_____

_____

7-8 量測方式為 on wafer, on PCB or in package? 並說明量測時應該注意事項與量測地點

_____

_____

_____

_____

_____

_____

8 PAD Replacement 考量(使用 TSMC I/O PAD 設計者填寫)

8-1 個人設計的 Cell 名稱(cell-name)未與 TSMC 所提供之任一 Pad Cell 名稱相同_____

8-2 採用 Create Instance 方式加入 I/O Pad，未用 Copy 或 Flatten 破壞

Instance 的結構_____

8-3 由 IC Core 部份拉線到 Pad 只拉到最邊緣部分，未過於覆蓋 Pad_____

9. 使用 ARM926EJ or ARM7TDMI CPU IP

9-1. 若有使用 ARM926EJ /ARM7TDMI CPU IP，請提供以下訊息以便向 ARM 原廠申請 Design ID。

使用的 CPU 種類（ARM926EJ or ARM7TDMI）:_____

使用的 metal layers 的層數:_____

佈局中 ARM926EJ /ARM7TDMI Macro 的 cell name:_____

這個晶片是否為修訂版本(revision,也就是之前曾下線過相同晶片)?_____

若是修訂版本，前一次下線的晶片編號:_____

修訂版本的原因是?(例如修正 bug)_____

10 其他考量

10-1 是否考量測試時的輸出量測點?_____YES_____

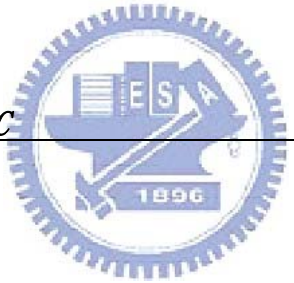
10-2 是否考量電路之可修改性(如用 laser cut 設備)_____YES_____

D. Tapeout Review Form (for Cell-Based IC)

Tapeout review form 的用意在提醒設計者在設計、模擬、佈局、佈局驗證及 tapeout 時具備設計理念及了解應注意事項,希望能藉此提昇晶片設計的成功率及達到完整的學習效果。因此,請指導教授及設計者確實檢查該晶片設計過程是否已注意本表格之要求,並在填寫確定後簽名,若審查時發現設計內容與 Tapeout Review Form 之填寫不符,很可能遭取消該晶片下線製作資格。可參考本表後所附範例確實填寫。

9. 晶片概述：

1-1 專題名稱：A CMOS Mixed-Signal Front-End IC for Portable Biopotential Acquisition System



1-2 Top Cell 名稱： *MSFEIC*

1-3 使用 library 名稱：

___ CIC_CBDK90

v CIC_CBDK18

CBDK 版本: CBDK018_TSMC_Artisan_v2.0

是否使用 Core Cell: *v* 若有使用 Core Cell 型號: □hvt □rvt □lvt

Core Cell 有無更改 Cellname: *NO* (建議保留勿更改)

是否使用 IO: *v* 若有使用 IO, 採用形式是 : □Linear v Staggered

1-4 是否使用 CIC 提供之 Memory？ *NO* 若使用 Memory, 是否已上傳 spec 檔: ____

使用 Memory 之種類為何？ _____

1-5 是否使用 CIC 提供之 ARM CPU IP？ *NO* (若為 Yes, 請務必填寫第 9 項)

使用 CPU 之種類為何？(ARM7TDMI or ARM926EJ) _____

1-6 工作頻率： *65,536kHz*

1-7 功率消耗： 數位: *20uW* *total: 998uW*

1-8 晶片面積： *1.919* X *1.919*

9. 設計合成：

2-1. 使用之合成軟體？ Synopsys design compiler

2-2. 是否加入 boundary condition：

v input drive strength、*v* input delay、*v* output loading、*v* output delay

2-3. 是否加入 timing constraint：

v specify clock (sequential design)

v max delay、*v* min delay (combinational design)

2-4. 是否加入 area constraint？ *NO*

2-5. 合成後之 report 是否有 timing violation？

NO 有 setup time violation、*NO* 有 hold time violation

2-6. 合成後之 verilog 是否含有 assign 描述？ *NO*

2-7. 合成後之 verilog 是否含有 *cell* 之 instance name？ *NO*

2-8. 合成後之 verilog 是否含有反斜線 \ 之 instance name 或 net name？ *NO*

9. 可測試性設計(前瞻性晶片必填)：

3-1. 使用之設計軟體？ DFT compiler

3-2. 使用之 ATPG 軟體？ TetraMAX

3-3. 使用 Embedded memory 數量: SRAM 0 ，ROM 0

Memory 大小:

測試方法: BIST ，or 其他測試方法

若使用 BIST,其 Test Algorithm 為何?

同時有多個 memory，是否共用 BIST controller ，BIST controller 數量

3-4. Scan Chain Information

Flip-Flop 共有多少個？ 772

Scan chain 的數量共有多少條？ 1

Scan chain length (Max.) ？ 14131.805

3-5. Uncollapsed fault coverage 是否超過 90% ？ yes ，為多少？ 98.34%

ATPG pattern 的數目為多少？ 32

註：若使用 Synopsys TetraMAX 來產生 ATPG pattern，請使用 set faults -fault_coverage 指令指定 TetraMAX 產生 fault coverage information

若使用 SynTest TurboScan 之 asicgen 來產生 ATPG pattern，請以 atpg pessimistic fault coverage 的值為準

9. 佈局前模擬

4-1. gate level simulation 是否有 timing violation？

___ 有 setup time violation、___ 有 hold time violation

9. 實體佈局

5-1. 使用之 P&R 軟體？ ___ Apolo、 *v* SOC Encounter

5-2. power ring 寬度？ *8um* 是否已考量 current density(1mA/1um)？ *yes*

5-3. 是否考慮 output loading？ *yes*

5-4. 是否加上 Clock Tree？ *yes*

5-5. 是否加上 Corner pad？ *yes*

5-6. IO Buffer 間是否加上 IO Filler: *yes* IO Filler 寬度: *24* um（建議至少需 12um 寬）

5-7. 是否加上 Core Filler？ yes

5-8. 是否上加 Bonding Pad？ *yes*

以下(A-1)為使用 Apollo 者才須回答

A-1. 是否執行 Fill Notch and Gap 步驟？ _____

以下(S-1 至 S-2)為使用 SOC Encounter 者才須回答

S-1. power ring 上是否有 overlap vias？ _____

S-2. 是否確定 IO Row 和 Corner Row 互相貼齊？ _____

9. 佈局後模擬

6-1. 是否做過 post-layout gate-level simulation？ *yes*

STA(static timing analysis) 軟體？ *ncverilog*

6-2. 是否做過 post-layout transistor-level simulation？ *yes*

6-3. 已針對以下環境狀態模擬： *v* SS、 *v* TT、 *v* FF

6-4. 晶片取得時將以何種方式進行測試？將此晶片所需的直流電路接好，使用波形產生器產生不同的弦波輸入此晶片中，觀察其輸出，再用邏輯分析儀將其輸出值抓出，再代回 matlab 中分析其輸出的時域

值和頻域值是否正確。分析其解析度、有效 bit 數和線性度(INL & DNL)。

6-5. 模擬時是否考量輸出負載影響？ ___*yes*___ 若有輸出負載是: ___*20*___ pF（建議至少需 20pF）

9. DRC/LVS 驗證

7-1. 是否有 DRC 錯誤？ ___*yes*___ 錯誤原因: OD.C.1 OD.C.5 RPO.C.3 RPO.C.6 以上四個為 io pad 的假錯 ; CTM.R.2 為電容假錯; PO.R.3 M1.R.1 M2.R.1 M4.R.1 M5.R.1 M6T.R.1 等的錯誤為數位電路部分，所有的 cell 還未填入，所以會有此些 density 的問題。

驗證 DRC 軟體？ ___*calibre*___

是否有不作 DRC 的區域？ ___*NO*___

7-2. 是否有 LVS 錯誤？ ___*NO*___

驗證 LVS 軟體？ ___*calibre*___

是否有非 CIC 提供的 BlackBox？ ___*yes*___

9. MT Form 填寫

8-1. 是否填上 ___ 系所單位、___ 設計者姓名、___ 聯絡電話(與手機）、___ 日期

8-2. 是否填上晶片上傳目錄？ _____

8-3. 是否填上檔案名稱？ _____

8-4. 是否寫上 top cell name？ _____

9. 使用 ARM926EJ or ARM7TDMI CPU IP

9-2. 若有使用 ARM926EJ /ARM7TDMI CPU IP，請提供以下訊息以便向 ARM 原廠申請 Design ID。

使用的 CPU 種類（ARM926EJ or ARM7TDMI）:_____

使用的 metal layers 的層數:_____

佈局中 ARM926EJ /ARM7TDMI Macro 的 cell name:_____

這個晶片是否為修訂版本(revision,也就是之前曾下線過相同晶片)?_____

若是修訂版本，前一次下線的晶片編號:_____

修訂版本的原因是?(例如修正 bug) _____