Chapter 1

Introduction

Technologies for fabricating high device cutoff frequency f_T, maximum oscillation frequency f_{max}, low frequency (1/f) as well as microwave noise, power efficiency and low intermodulation would be desired for wireless communication applications. Silicon germanium hetero-junction bipolar transistor (SiGe HBT), with its nature potential, would be capable of providing such performances. Several researches have been done to develop the SiGe HBT devices for obtaining higher performance. However, there were still many unknown in the physical origins of the device operation and it could impact the applications of the SiGe HBT in RF and analog circuit design.

In this research, the device behaviors involving the physics of the collector region and the corresponding fabrication technology were dedicated which could induced potential impacts on analog and RF circuit design critically. First, in chapter 2, a efficient approach for estimating the transit time composition have been developed and reported. The transit time composition could be qualitatively decoupled by this approach based on the calibrated SIMS doping profile and MEDIDI simulation results

of the HBT device. It was also found that the collector region could alternate the device characteristics more significantly as the vertical dimension was continuous scaled down to 0.18 μm BiCMOS generation. It suggested that the device behaviors dependent on the collector region should be worth to studied.

Next, in chapter 3, the bias dependency of r_B and the associated influences on the RF characteristics was discussed, as well as the improving strategies. In section 2.1, the current dependent characteristics of the base resistance r_B was illustrated. Next, in section 2.2, the techniques and associated information involved corresponding to the vertical current spreading and crowding effect would be described including the measurement results and the deduction and identification of the associating physical model. Third, in section 2.3, the theoretic deduction on the base dependent behavior of r_B discussed in 2.2 was presented. The associated deductions were also identified by device simulation in section 2.3. In section 2.4, the impacts resulting from the current dependent r_B behavior on the RF characteristics of the modern HBT devices in various geometry and collector doping profile based on the measurement results were reported. Moreover, for accurately verification in numerical way, the mathematical relations of f_T and f_{max} based on the proper device RF model should be required. In section 2.5, the derivation details of the mathematical relations based on the RF HBT model with the emitter resistance was illustrated. Furthermore, the RF characteristic

impacts from the bias dependent behaviors of r_B described in section 2.4 were verified by the numerical approaches associated with the measurement results which were applied to verify the scheme of the impacts. Finally, in section 2.6, the impact of the current dependency of r_B on the device noise characteristics would be discussed

In addition, deep trench (DT) isolation technology has been widely applied in several applications in modern VLSI fabrication to improve the device breakdown, reliability and isolation performance. [1] – [2]. However, limited literatures have discussed the characteristic deviations between DT and NDT devices (without DT structures), especially for RF applications. In chapter 4, the impacts of the DT structure on the RF characteristics of SiGe HBT including the cutoff frequency, maximum oscillation frequency, RF noise characteristics and two tone performance which were key indexes for RF IC design were studied discussed. Several experiments have been done for this study. First, SiGe HBT devices with and without DT structure were fabricated with various doping profiles. Next, standard DC and RF measurements were applied to obtain accuracy device parameters for further analysis. Finally, the T-SUPREM 4 simulation was applied to identify the physics involved in the study.

Further more, in traditional integrated circuit, the operation speed of the active devices could be a dominant item, which limited the circuit capability. With the

enlarging complexity of the integrated circuit, longer interconnection lines associated with larger parasitic capacitance could be created and this could become another speed limiting issue in SOC design. In chapter 5, a novel, low cost and efficient approaches that could successfully improve the physical and electrical capability of the low-K dielectric material adopted in the copper comparable backend system would be reported. Finally, a conclusion of this research will be made in chapter 6 along with the potential contribution and corresponding future works.