Chapter 1 Introduction

1.1 Background and motivation

A wideband receiver is constructed where its radio frequency (RF) covers 78.3-113.1GHz and its intermediate frequency (IF) bandwidth is set to 34.8GHz. Instantaneous detection of the intended electromagnetic spectra is therefore ensured with this maximized IF bandwidth, thus allows the exploration of the anisotropy of the cosmic microwave background radiation (CMBR) in the millimeter-wave frequency range; or more specifically, the inverse-Compton scattering of the photons by hot electrons in the galaxy clusters, also known as Sunyaev-Zel'dovich (SZ) effect.

As shown in Fig. 1-1, the incoming signal is first fed into two cryogenic amplifier modules with each has 70.90Kelvin noise temperature and 20dB gain at 20Kelvin ambience. To ensure stability, cryogenic isolators have been incorporated into these amplifiers. The cryogenic WiseWave-FDB1001 mixer made by WiseWave Technologies (now Ducomun Technologies) is then used to down-convert, with 5.7dB conversion loss, the signal to (quasi) DC-34.8GHz. Of course, it is possible using a room-temperature mixer instead, but that will require the precision insertion of a hermetically-sealed millimeter-wave waveguide between the front-end cryogenic amplifier and this room-temperature mixer, and the attenuation along this long waveguide will also be pronounced. Four separate bands can now be extracted by the use of amplifiers, filters, and another three mixers, each with 8.7GHz IF bandwidth and the LO frequency is fixed at 17.4GHz, 17.4GHz and 26.1GHz, respectively. The reason for not using an 8.7GHz LO for down-converting in the second band is because this LO is bordering the IF band, thus any residual LO at IF output is hard to remove; by contrast, a 17.4GHz LO can be easily taken off afterward.
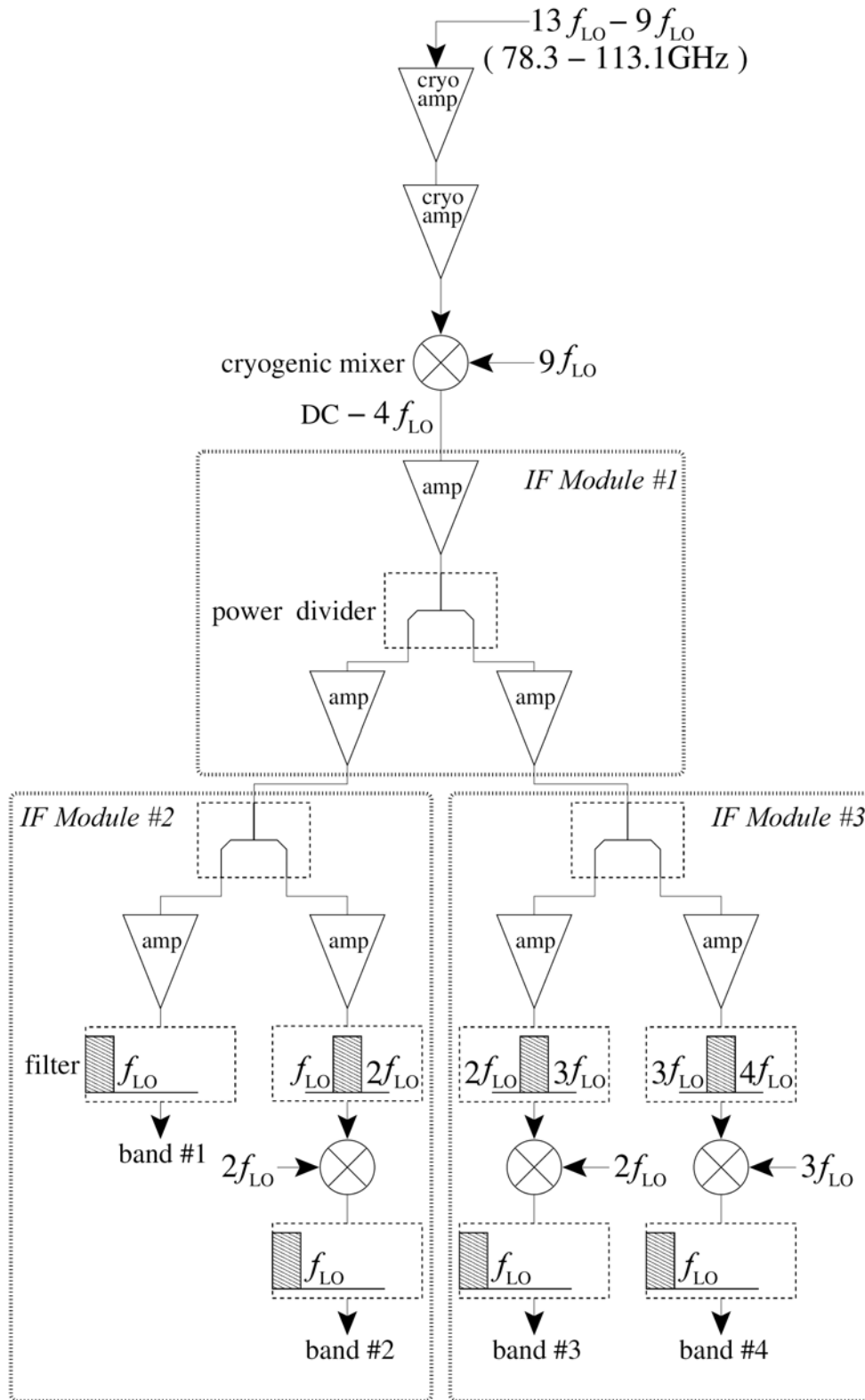
Fig. 1-1 Schematic of the wideband millimeter wave receiver. With f_{LO} = 8.7GHz, the incoming 78.3-113.1GHz signal will be amplified and down-converted to DC-34.8GHz, which is split into four separate bands of equal bandwidth, as indicated by the shaded areas.

1.2 Thesis Organization

This thesis is focusing on one type of RF circuit: the wide-IF-band mixer, where it can be divided into two categories, i.e., the fundamental mixer and its sub-harmonic counterpart, which will be discussed in the following. For the convenience of circuit design, the mixer can be further divided into small constituting blocks, thus allowing a step-by-step analysis. Both simulated and measured results will be presented at the end of Chapter 2. The shortcomings and undesired properties of the mixers will then be explained and discussed in Chapter 3, which also contains the tentative conclusion and the future work. Meanwhile, we are working on the development of the theory for explaining the characteristics of our mixer, and this will be done by this summer; the design of the W-band mixer is also in schedule.
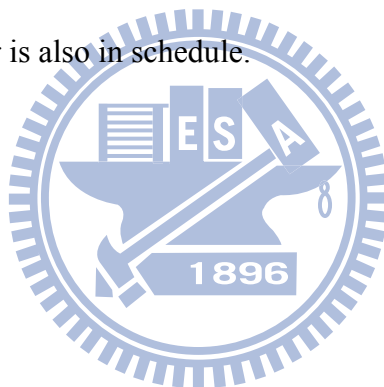
Chapter 2
Wide-IF-Band CMOS Mixers for Millimeter-Wave Applications

2.1 Introduction

Nowadays, the growing amount of blossomed information flow has increased the aspiration for much wider bandwidth in order to achieve higher efficiency, which makes inevitable the development of wideband devices. One of the largely ignored so far but highly potential lands is the mixers with wideband intermediate frequency (IF). As with the 60GHz wideband system already demonstrated viable by different for-profit companies, the 78.3-113.1GHz (W-band) is expected to be the next goldmine, and cutting-throat battlefield too, as the number of journal papers on W-band circuits designed by world-leading universities keeps piling up steadily. Therefore, we aim to begin with the millimeter-wave wide-IF-band mixer, and the experience acquired from such efforts will then help us to accomplish our own W-band mixer design.

Although the double-balanced circuit configuration had appeared in microwave and millimeter-wave applications for many years, but not all the techniques that developed for improving the mixer's performance at low frequency or even a few GHz are applicable at tens of GHz. Besides, most of the reported active wideband transistor mixers have their proclamation illustrated by shifting the LO frequency across the intended wide RF bandwidth while retaining their IF bandwidth relatively small, so they are in fact wide-RF-band but narrow-IF-band mixers. All these means developing these wide-IF-band mixers demands some particular attention to details.

In this thesis, we are going to design the RF and IF mixers, as indicated in Fig. 2-1. The mixer on top of the figure is the RF mixer that is used to down-convert the 78.3-113.1GHz signal; the other three mixers are all IF mixers that can down-convert the 8.7-17.4, 17.4-26.1 and 26.1-34.8GHz signal, respectively. Our research plan is to complete the design of three IF mixers first and then their modified versions (sub-harmonic mixers) that have better performance and relaxed system constraints. Finally, we will move onto the design of the W-band mixer, with the experience gained from designing the IF mixers.
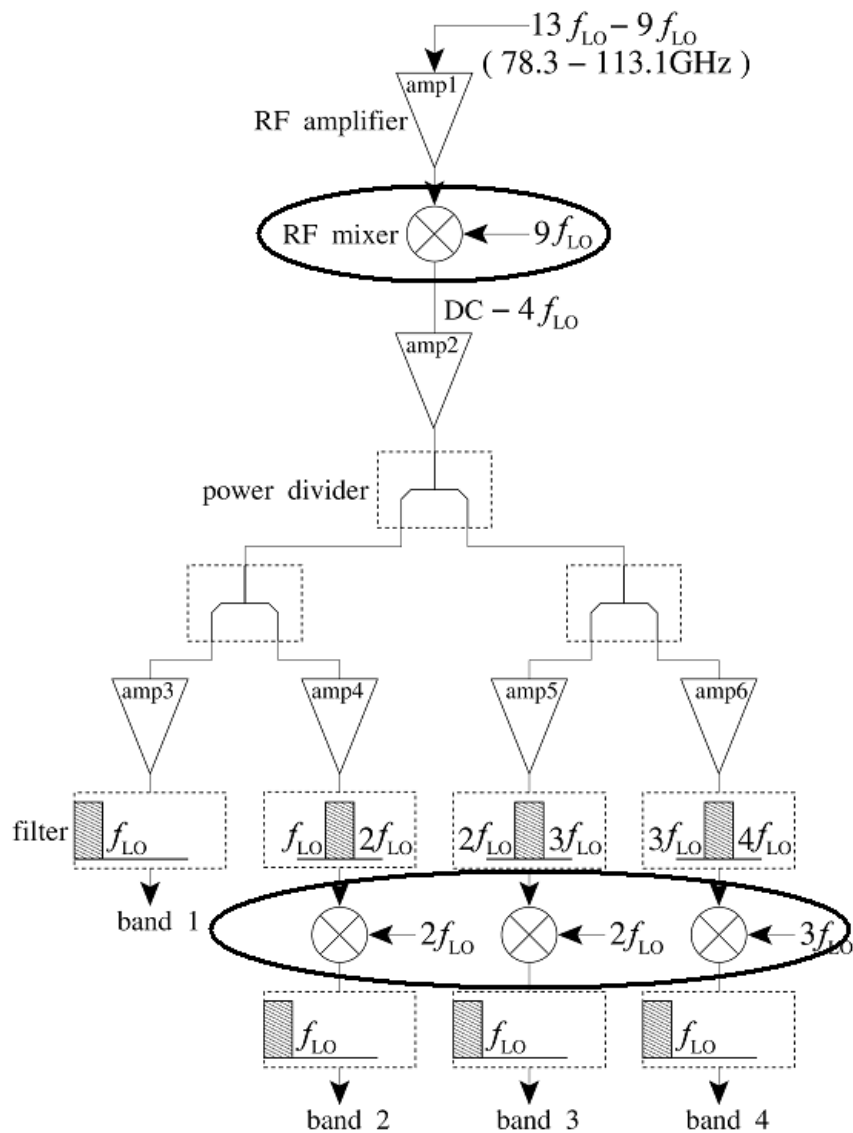
Fig. 2-1 Schematic of the wide-band receiver. Our objective mixers are indicated by black circles.

2.2 Wide-IF-band mixer design

Fig. 2-2 is the schematic of proposed wide-IF-band mixer circuit and it can be divided into three parts: input RF circuit, mixing core, and output IF circuit. Since the balun plays an important role in both the RF circuit and mixing core, it will be discussed first.
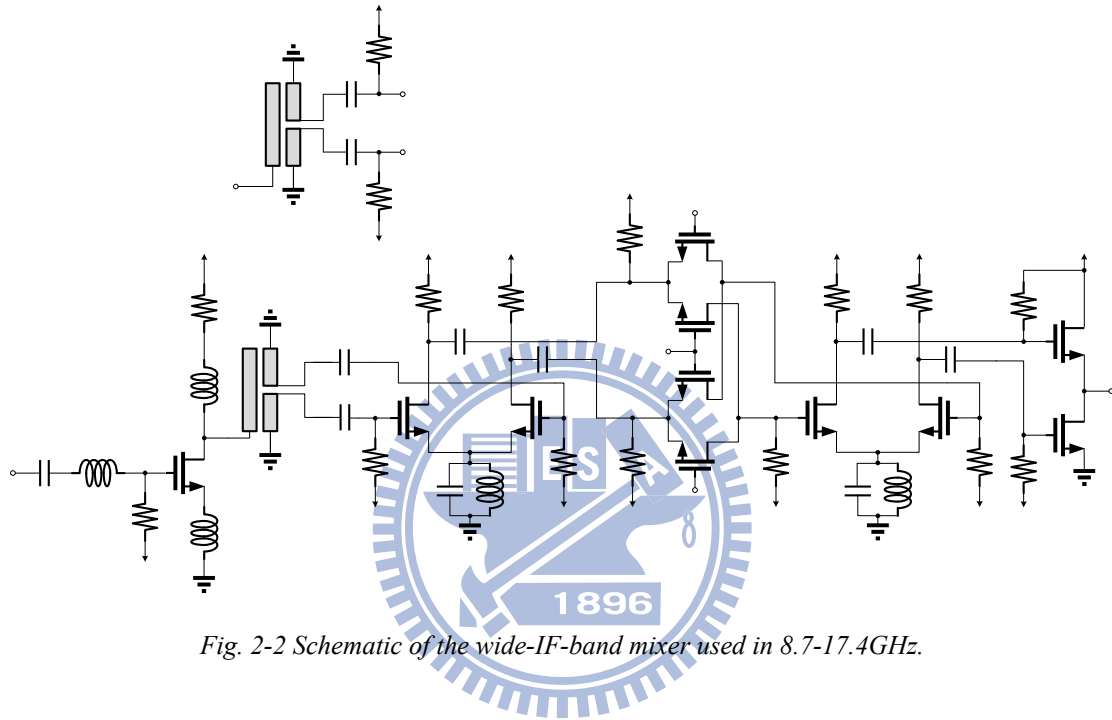

Fig. 2-2 Schematic of the wide-IF-band mixer used in 8.7-17.4GHz.

A. LO balun

There are two baluns used in this mixer, one is in the input RF circuit to transform the single-ended RF signal into its differential-mode counterpart, and the other is in the mixing core to produce the balanced LO signals. For wideband purpose, we use the Marchand balun in our research [8], which has its S-parameters arranged in Eq. (2-1) where C is the coupling coefficient; Z_0 is the 50Ω system impedance; and Z_1 is the arbitrary loading impedance which may be different Z_0 [13]. When Z_1 happens to be 50Ω, the S-parameter can be simplified as Eq. (2-2), and we can see that S_{11} is zero when C is -4.8dB. In any case, S_{21} and S_{31} will be whatever equal magnitude but 180°

out-of-phase [9], [10]. Fig. 2-3 shows the schematic and layout of our proposed

broadside-coupled balun and Fig. 2-4 is the simulated results.

$$
\begin{bmatrix}
\dfrac{1-C^2(\dfrac{2Z_1}{Z_0}+1)}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} & \dfrac{j2C\sqrt{1-C^2}\sqrt{\dfrac{Z_1}{Z_0}}}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} & \dfrac{-j2C\sqrt{1-C^2}\sqrt{\dfrac{Z_1}{Z_0}}}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} \\[4ex]
\dfrac{j2C\sqrt{1-C^2}\sqrt{\dfrac{Z_1}{Z_0}}}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} & \dfrac{1-C^2}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} & \dfrac{j2C^2\sqrt{\dfrac{Z_1}{Z_0}}}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} \\[4ex]
\dfrac{-j2C\sqrt{1-C^2}\sqrt{\dfrac{Z_1}{Z_0}}}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} & \dfrac{j2C^2\sqrt{\dfrac{Z_1}{Z_0}}}{1+C^2(\dfrac{2Z_1}{Z_0}-1)} & \dfrac{1-C^2}{1+C^2(\dfrac{2Z_1}{Z_0}-1)}
\end{bmatrix}
\tag{2-1}
$$

$$
\begin{bmatrix}
\dfrac{1-3C^2}{1+C^2} & \dfrac{j2C\sqrt{1-C^2}}{1+C^2} & \dfrac{-j2C\sqrt{1-C^2}}{1+C^2} \\[3ex]
\dfrac{j2C\sqrt{1-C^2}}{1+C^2} & \dfrac{1-C^2}{1+C^2} & \dfrac{2C^2}{1+C^2} \\[3ex]
\dfrac{-j2C\sqrt{1-C^2}}{1+C^2} & \dfrac{2C^2}{1+C^2} & \dfrac{1-C^2}{1+C^2}
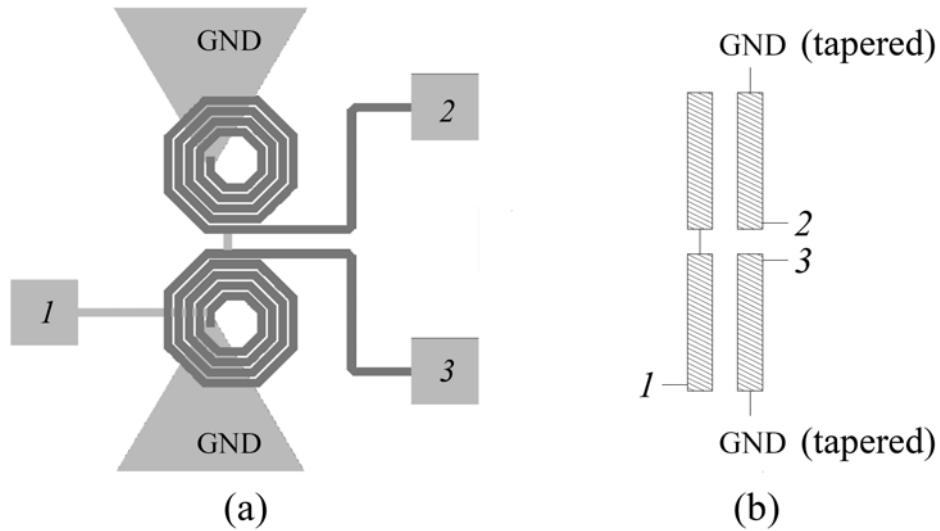\end{bmatrix}
\tag{2-2}
$$

7

Fig. 2-3 Proposed broadside-coupled Marchand balun with minimum connecting line between the spirals. (a) Layout. (b) Schematic.
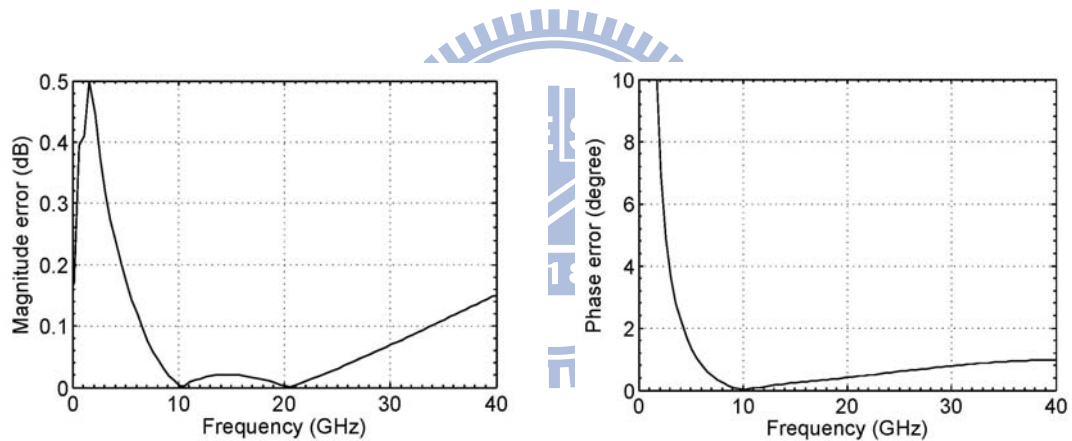

Fig. 2-4 Simulated output magnitude and phase errors of the balun. (a) Output magnitude error. (b) Output phase error.

Since the output of the balun in our mixer is connected to the transistor's gate, which is not 50Ω but close to 0.13pF, the mixer's input reflection coefficient will be highly frequency-dependent [14], as that shown in Fig. 2-5. Of course, by inserting *R-L* circuit between the balun's output ports, a matched S_{11} can indeed be obtained over a wide bandwidth for capacitive loading; however, this lossy matching method will cause the signal attenuation. Therefore, to achieve good RF input return loss, we

insert a single stage transistor circuit in front of the balun, as which can also provide a
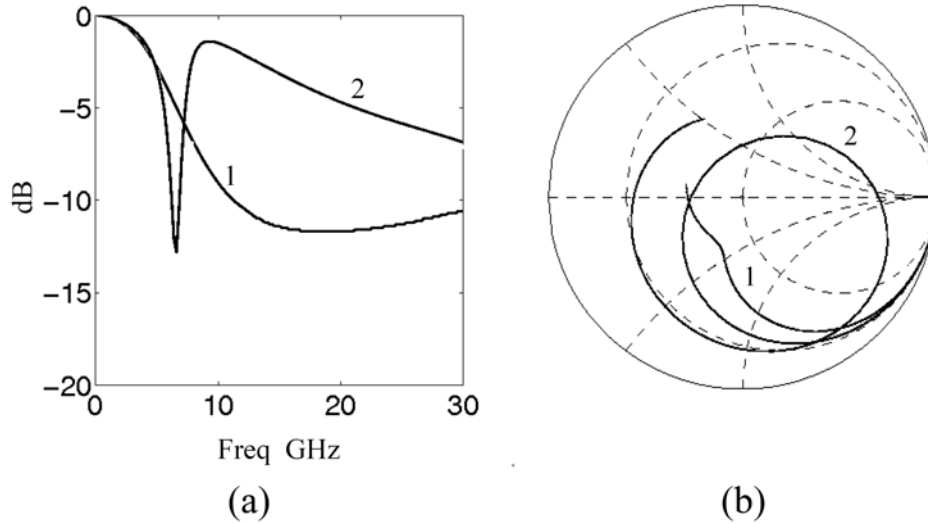
moderate gain [5].

Fig. 2-5 Simulated input reflection coefficient of the balun. (a) Curve 1 is with 50Ω loading for both port 2 and port 3; curve 2 is with each output port connected to a 130fF capacitor. (b) The corresponding curves in the Smith chart.

For the LO port, however, the insertion of additional transistors is not appropriate

as they can be easily driven into saturation by the LO signals. What we do is to

modify the LO balun layout so as to shift the matched point to our desired

narrowband LO frequency. Following is the mathematical explanation, Eq. (2-3) is S_{11}

of Eq. (2-1), as its numerator sets to zero and apply Z_L as $1/sC_{gs}$, we can find out the

relation between C and the frequency at zero return loss, which is derived as Eq. (2-4).

It shows that we can adjust C to make the unbalanced port match to 50Ω at our

desired frequency (LO frequency), and the matched frequency rises as C rises, and

vice versa.

$$S_{11} = \frac{1 - C^2(\frac{2Z_L}{Z_o} + 1)}{1 + C^2(\frac{2Z_L}{Z_o} - 1)} \tag{2-3}$$

$$1 - C^2(\frac{2Z_L}{Z_o} + 1) = 0 \text{, when } Z_L = \frac{1}{sC_{gs}}$$

$$\Rightarrow \frac{2}{sC_{gs}Z_o} = \frac{1 - C^2}{C^2}$$

$$\Rightarrow s = \frac{2}{C_{gs}Z_o}\frac{C^2}{1 - C^2} \cong \frac{2C^2}{C_{gs}Z_o} \cdot (1 + C^2), \quad \because 0 < C < 1 \tag{2-4}$$

B. Input RF circuit

As shown in Fig. 2-6, the input RF circuit starts with a single-stage transistor with source and gate inductors. By fine tuning their inductance, wideband input matching can be achieved [5]. The power gain of this common-source stage affords to compensate for the insertion loss of the succeeding balun [11], [12], [13].

The balanced signals out of the balun are fed to the trans-conductance stage and then into the mixing core. By find-tuning the source LC of the RF differential pair, any residual common-mode signal out of the balun (due to its poor out-band performance) can be easily suppressed while the differential-mode signal can still be amplified. In other words, this stage has good common mode rejection ratio (CMRR) for the RF signals. It should be noted that since the output impedance of the conventional current source (using p-type transistors) decreases rapidly as frequency increases, the current-source approach cannot be used in our application. By contrast, the LC tank can easily achieve high impedance and therefore is more appropriate here. With its resonance frequency set at 17GHz, this LC tank can have a peak impedance of 1kΩ. Likewise, the use of active loading on the drain branch is avoided; the
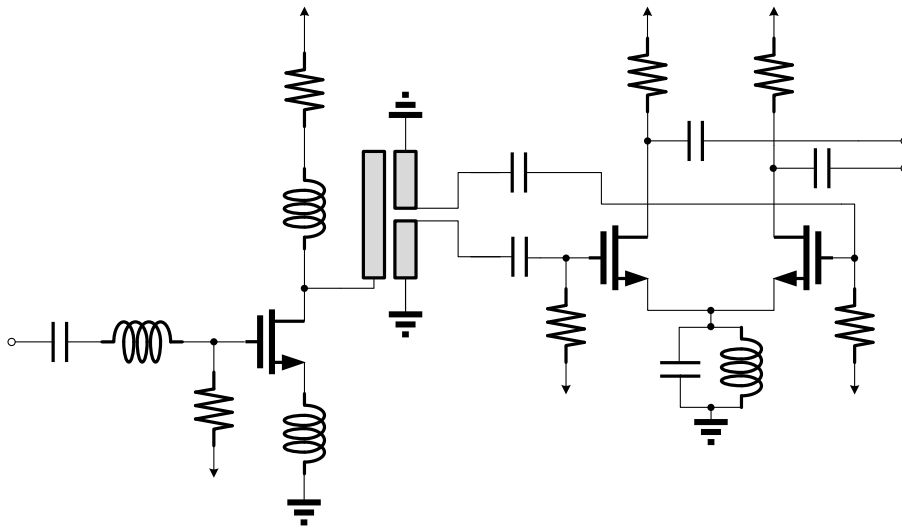
resistive bias scheme is preferred instead.

Fig. 2-6 Schematic of the input RF circuit.

C. Mixer core

Since the RF band is adjacent to the IF band in the mixer, the double-balanced configuration, shown in Fig. 2-7, is used to improve the RF-IF port isolation to avoid the RF-IF leakage. For high linearity purpose, resistive biasing scheme is adopted where the mixing transistor can be modeled as mainly a variable resistor (modulated by the applied LO signal). Being less frequency-dependent, this mixer is also expected to be wideband. In the simulation, though a much larger conversion gain exists with non-zero drain bias, discernible conversion gain variation over the whole 8.7GHz IF bandwidth can be observed. Resistive mixer, on the other hand, tends to have constant conversion gain, and is more straightforward in terms of biasing. Furthermore, we set the voltage of mixing transistor's drain and source to the gate bias of other stages to curtail two dc blocking capacitors.
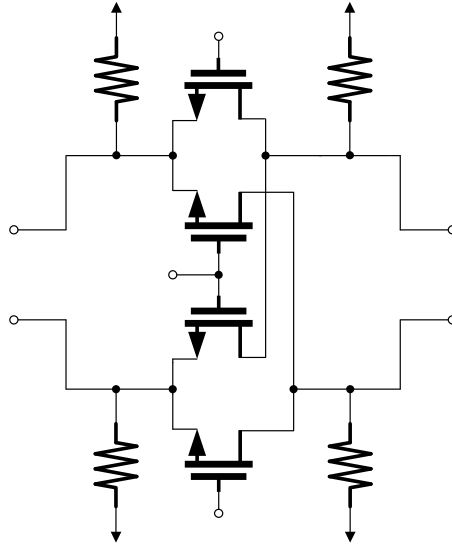
Fig. 2-7 Schematic of the mixer core.

D. Output IF circuit

As expected, the output IF circuit also needs to have a high CMRR value in DC-8.7GHz. Though the passive balun is used for the input RF circuit, this type of balun tends to take too much chip area for low frequency applications, not to mention that this passive balun fails to function around zero frequency. Therefore, we use a differential-pair followed by two n-type transistors in-cascade [17], [18], as shown in Fig. 2-8. The *LC*-tank is capable of providing large impedance at 8.7GHz while the in-cascade transistors can suppress the low-frequency common-mode signals, as best illustrated in Fig. 2-9.
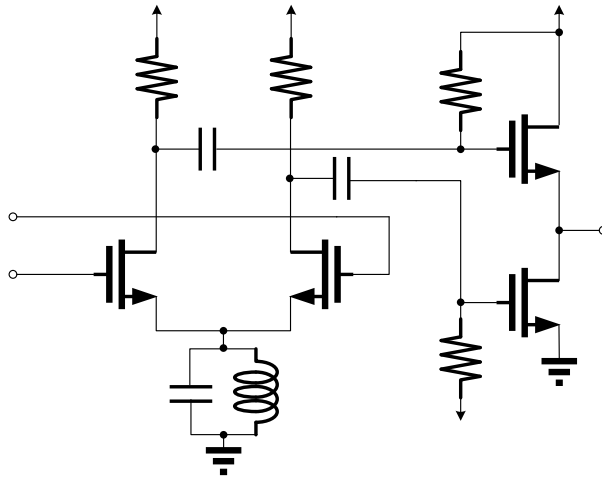
Fig. 2-8 Schematic of the output IF circuit.
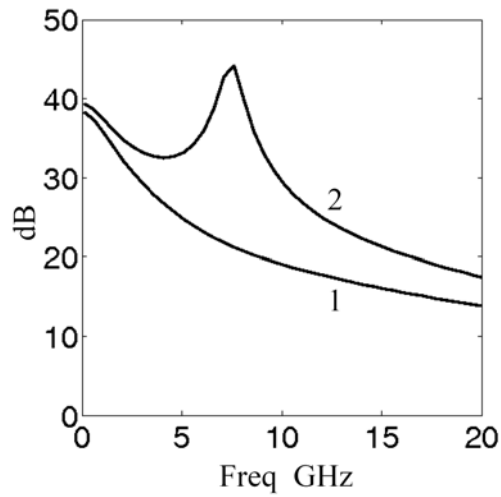
Fig. 2-9 CMRR of the output IF circuit. Curve 1 is the simulated CMRR of the in-cascade transistors,

curve 2 is the CMRR of overall IF circuit, i.e., differential-pair plus the in-cascade.

2.3 Simulated and measured results

This mixer is designed with TSMC 0.18um mixed-signal/RF CMOS process, chip size 1.098×0.968 um^2, power consumption 31mW. Fig. 2-10(a) is its layout and Fig.2-10(b) is the chip photograph.
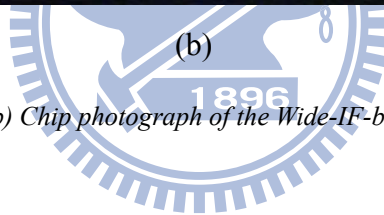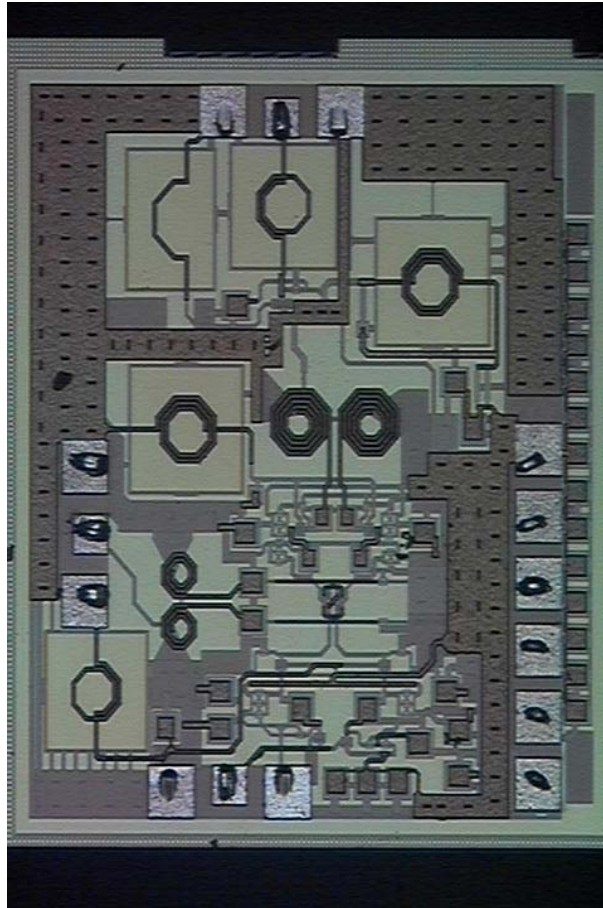

(a)

(b)
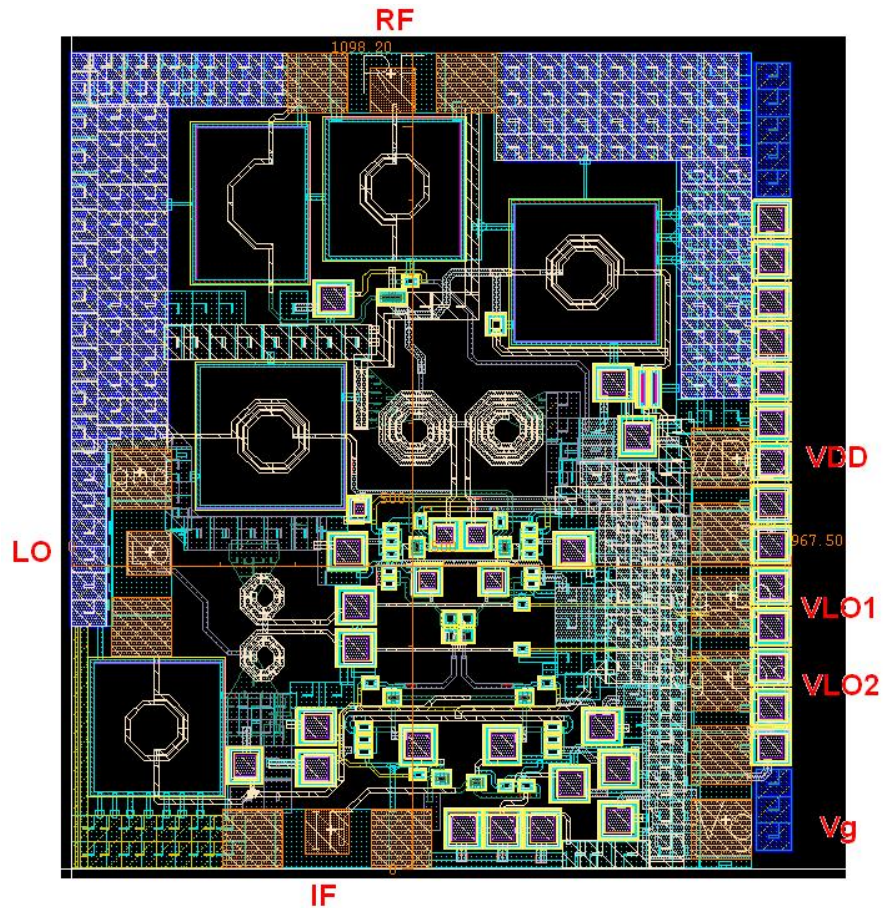
Fig. 2-10 (a) Layout (b) Chip photograph of the Wide-IF-band 8.7-17.4GHz mixer.

We deliver on-wafer measurement in Chip Implementation Center (CIC), which provides probe stations, network analyzers (HP8510C), spectrum analyzers (Agilent E4407B), signal generators, and power supplies. Fig. 2-11 shows the arrangement of DC and RF probes, one 6-pin DC probe and three 3-pin RF probes with pitch both are 100um are required for this circuit, and Fig. 2-12, 2-13, and 2-14 are the measured arrangement of S-parameter, conversion gain, and IIP3 respectively.
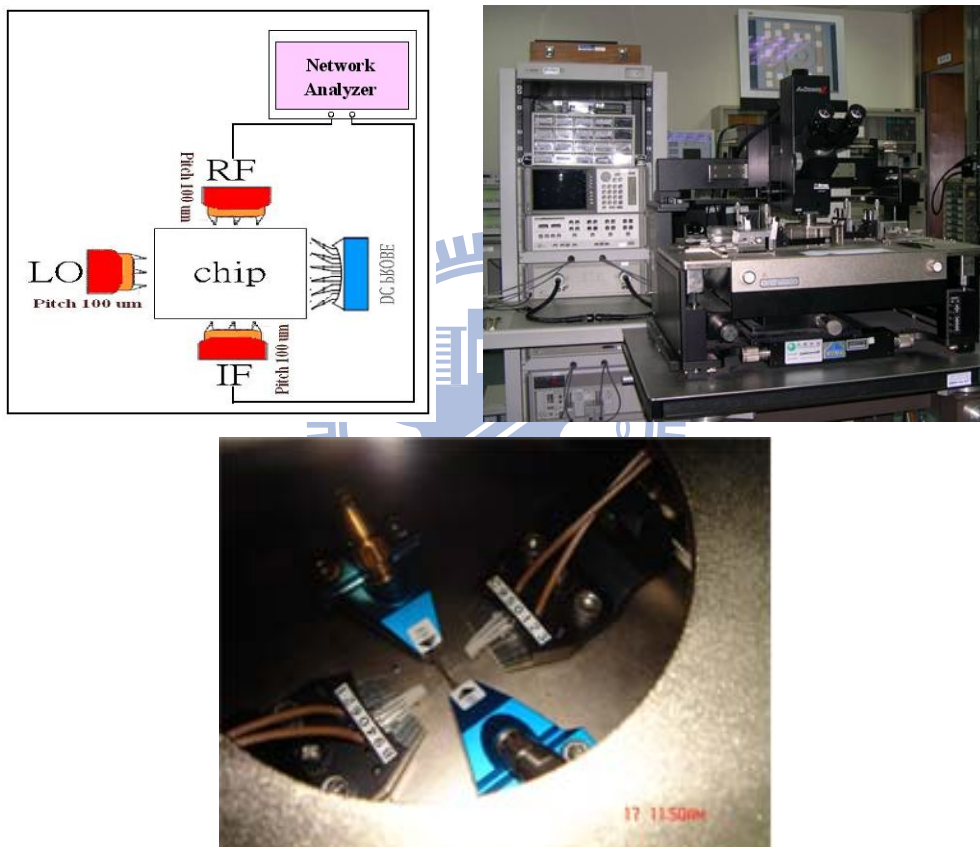
15
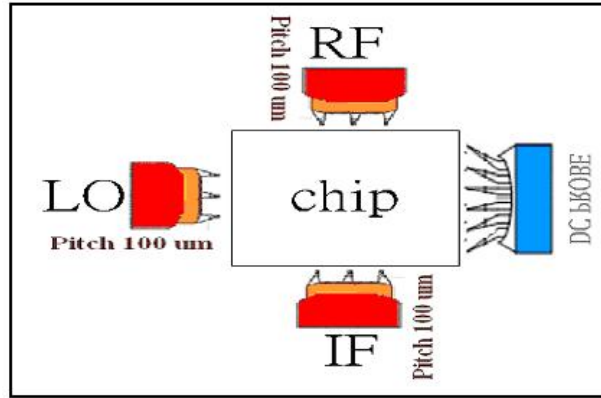
Fig. 2-11 Arrangement of DC and RF probes.

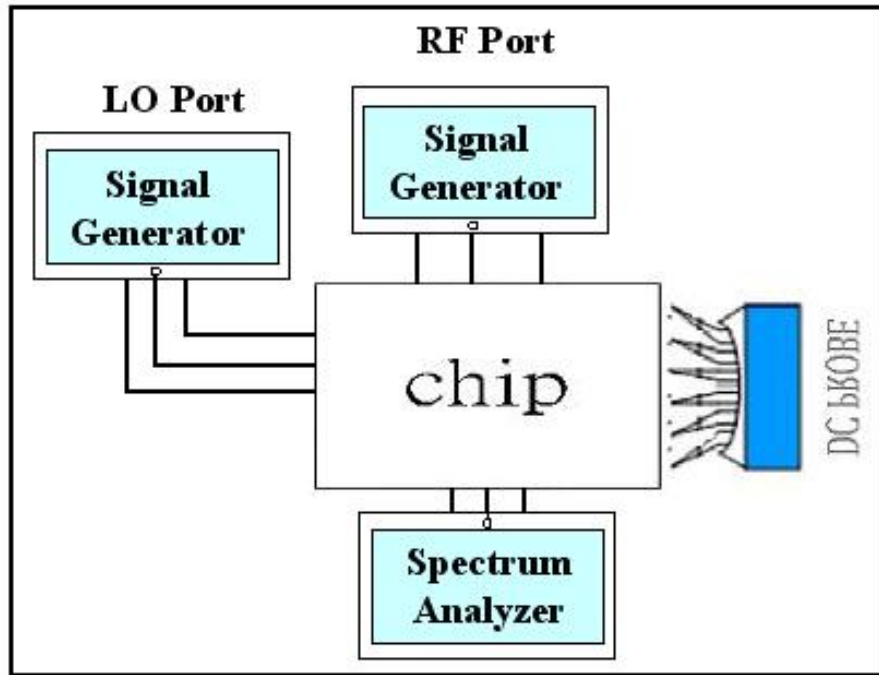*Fig. 2-12 The measured arrangement of S-parameter.*

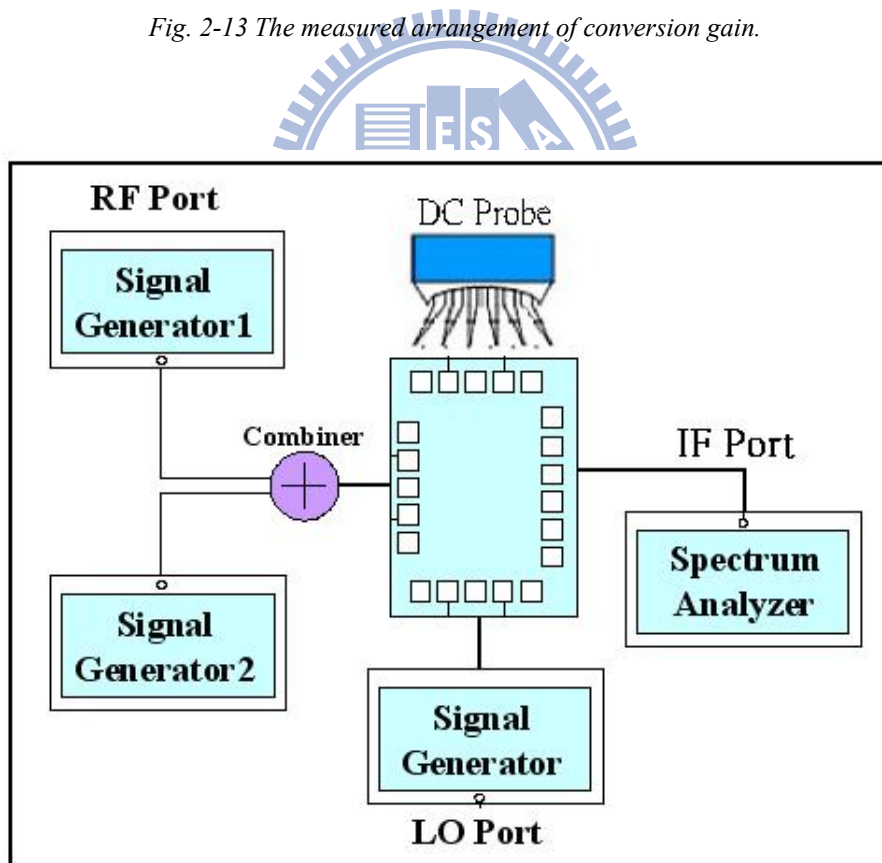*Fig. 2-13 The measured arrangement of conversion gain.*

Fig. 2-14 The measured arrangement of IIP3.

As shown in Fig. 2-15, the simulated and measured RF port return loss are below -10dB in 8.7-17.4GHz, and both the LO and IF ports have their simulated and measured return loss less than -10dB within the intended bandwidth, as shown in Fig. 2-16 and Fig. 2-17.
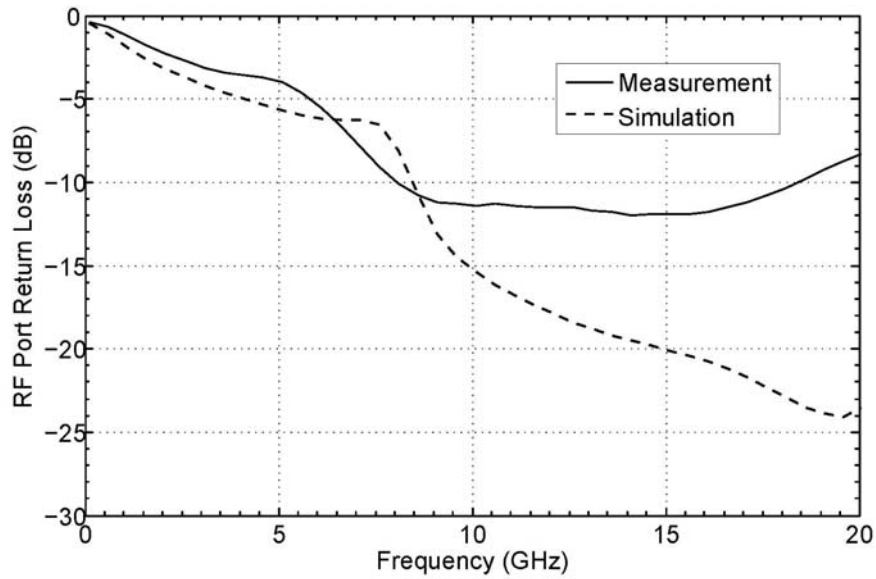

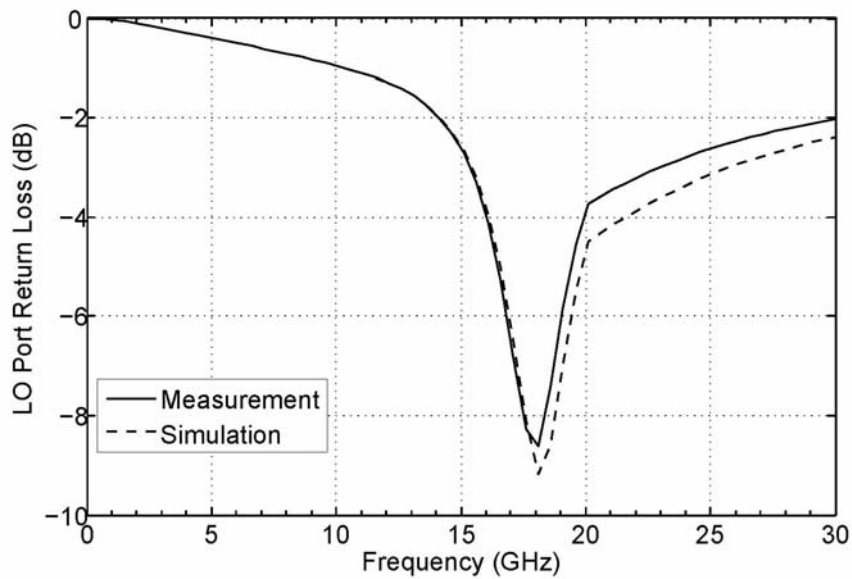*Fig. 2-15 RF port return loss where the RF signal is 8.7-17.4GHz.*

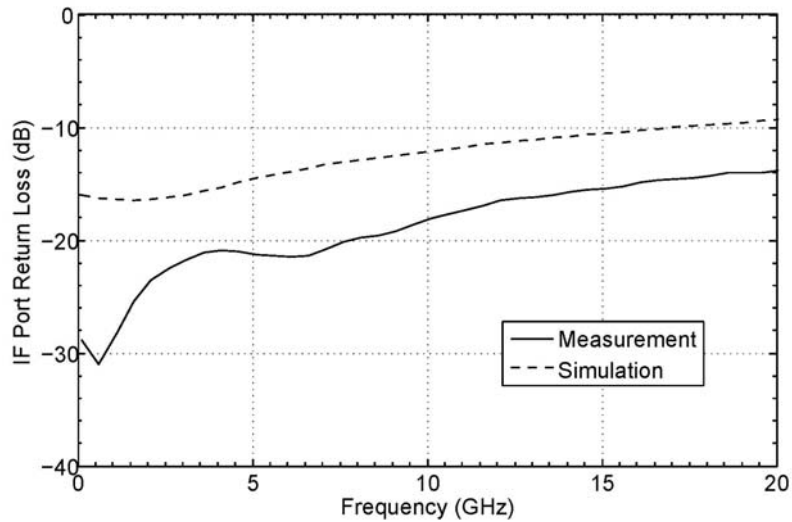*Fig. 2-16 LO port input return loss where the LO is fixed at 17.4GHz.*

Fig. 2-17 IF port return loss for IF equals to DC-8.7GHz.

Fig. 2-18 shows the simulated and measured conversion gain. The simulated result exhibits an average 5dB conversion gain, and gain variation less than 2dB within the intended RF bandwidth, but the measured result decreases 5dB at the lower end and 3dB at the higher end of RF bandwidth. We will discuss this discrepancy between simulation and measurement letter. Fig. 2-19 (a) and (b) are the input 1dB compression point (IP1dB) when RF frequency fixed at 15 and 17GHz respectively.
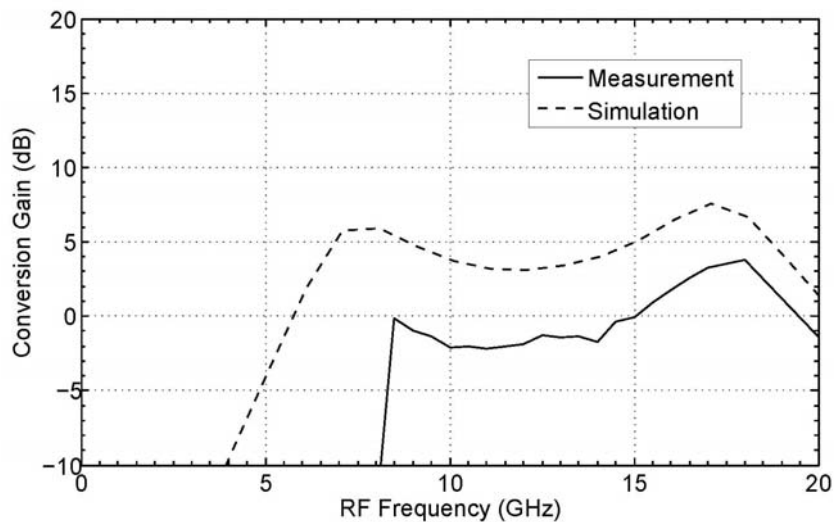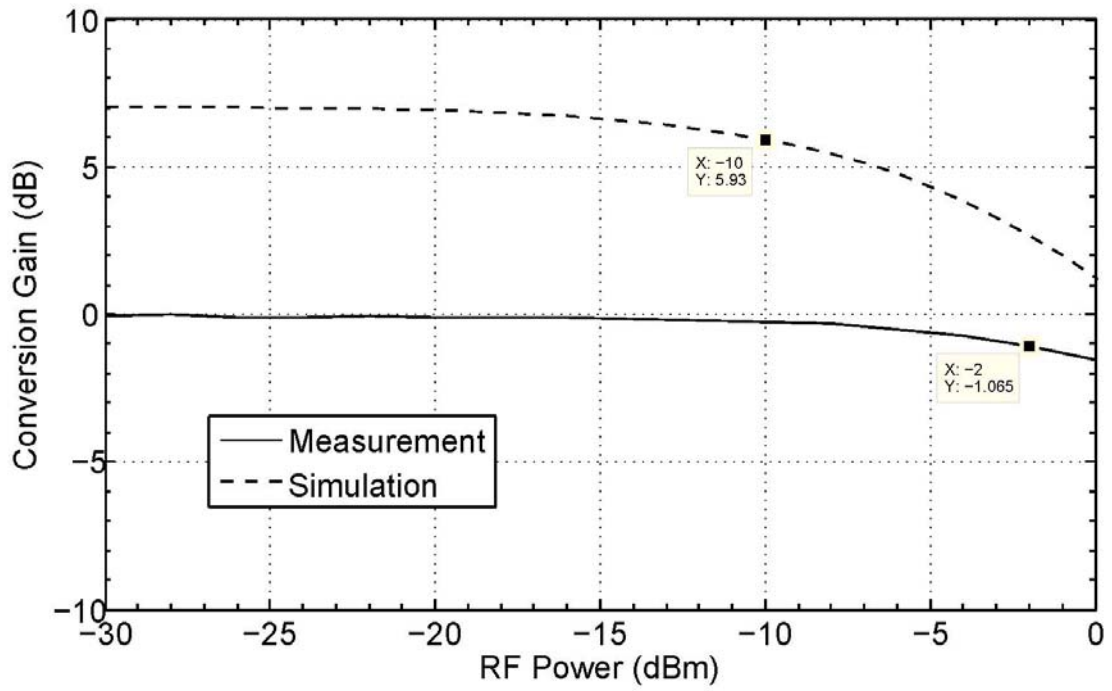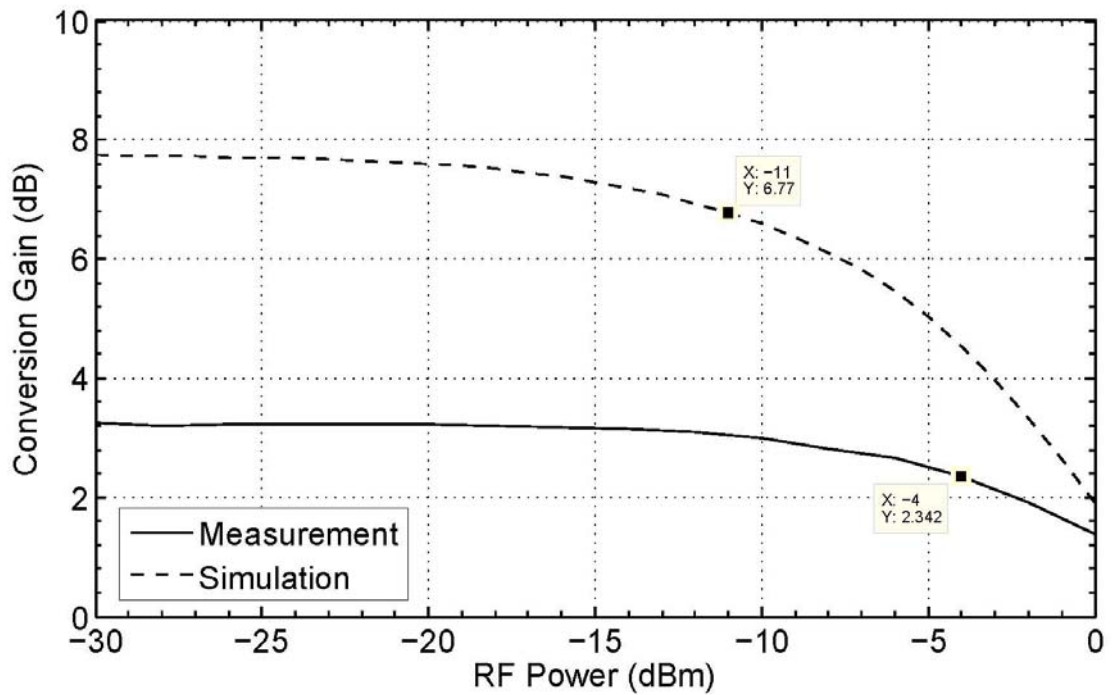

Fig. 2-18 Conversion gain versus RF frequency with LO fixed at 17.4GHz.

(a)

(b)

Fig. 2-19 P1dB of the 8.7-17.4GHz mixer where RF frequency fixed at (a) 15GHz. (b) 17GHz.

The comparison of simulated and measured results is shown in Table 2-1; they have obvious difference on conversion gain. We think the inconsistent is due to the loss of connecting lines, since the operating frequency is up to 18GHz, thus the connecting lines may decay the signal power dramatically. Therefore, the measured conversion gain are largely degraded against the simulated result.

Table 2-1 Comparison of the 8.7-17.4GHz Mixer's simulated and measured results.

	Simulation	Measurement
Process	TSMC 0.18um CMOS	
RF Bandwidth	8.7-17.4GHz	8.7-17.4GHz
Supply Voltage(V)	1.8V	2.3V
IF Bandwidth	DC-8.7GHz	DC-8.7GHz
RF input return loss	< -10dB	< -10dB
LO input return loss	< -10dB	< -8dB
IF input return loss	< -10dB	< -10dB
Conversion Gain	3dB	-2-4dB
P1dB	-11dBm@17GHz	-4dBm@17GHz
Power	31mW	60mW

2.4 Wide-IF-band mixers at higher band

As shown in Fig. 15, the two mixers for operating at higher bands (17.4-26.1 and 26.1-34.8GHz) have similar circuit configuration as that of the first one (8.7-17.4GHz) and the LO ports are modified to have 50Ω input impedance in their respective LO frequency. However, some design techniques are used to maintain their conversion gain. For instance, after the RF balun, additional inductors are added to be in parallel with the gate capacitor of 0.13 pF so as to boost the incoming RF signal. For a similar reason, a small series inductor is also inserted to the input of the RF balun. The inductors on the drain bias branch of the IF differential pair is used to improve the gain flatness.
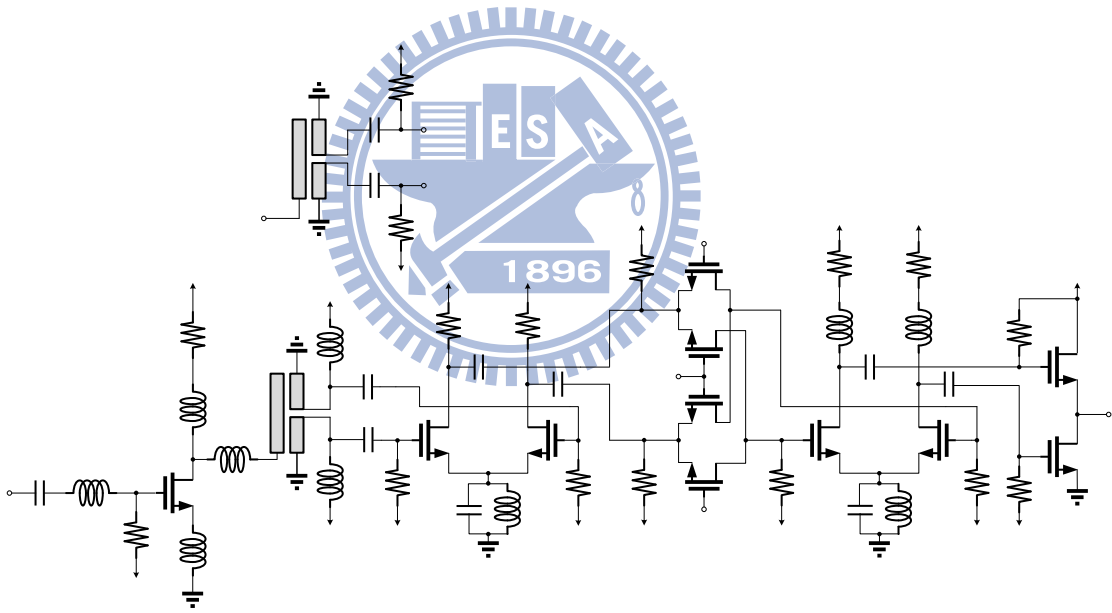

Fig. 2-20 Total schematic of the wide-IF-band mixer at higher band.

2.5 Simulated results of the 17.4-26.1GHz mixer

This mixer is designed with TSMC 0.13um mixed-signal/RF CMOS process, chip size 1.344×0.947 um^2, power consumption 30mW. Fig. 2-21 is its layout. As shown in Fig. 2-22, the simulated RF port return loss are below -10dB in 17.4-26.1GHz, and both the LO and IF ports have their return loss less than -10dB within the intended bandwidth, as shown in Fig. 2-23 and Fig. 2-24.
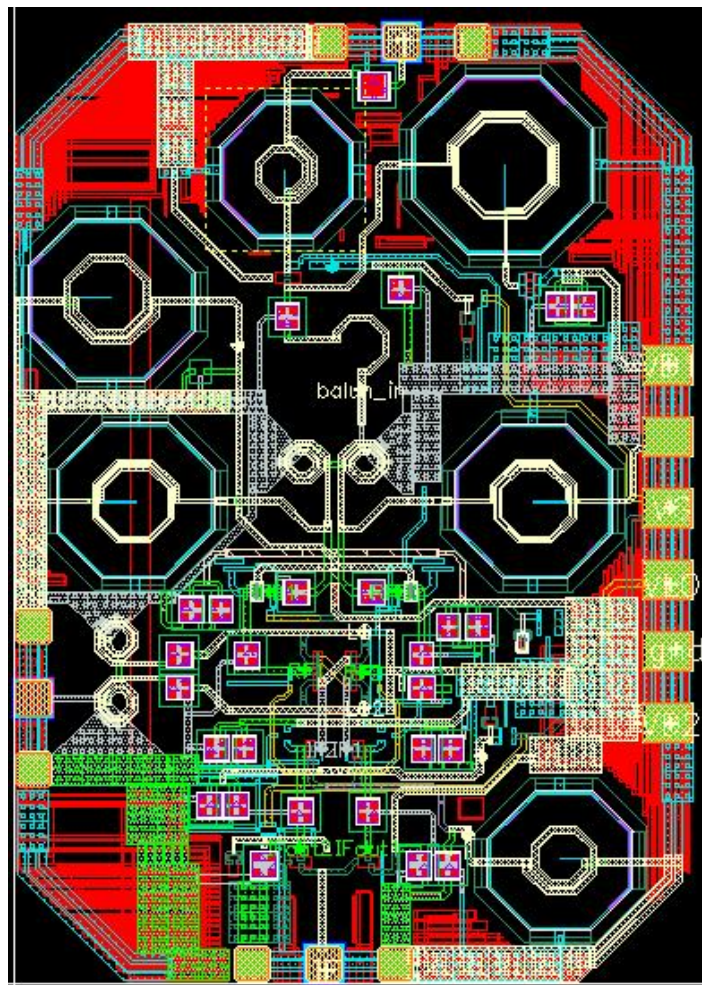

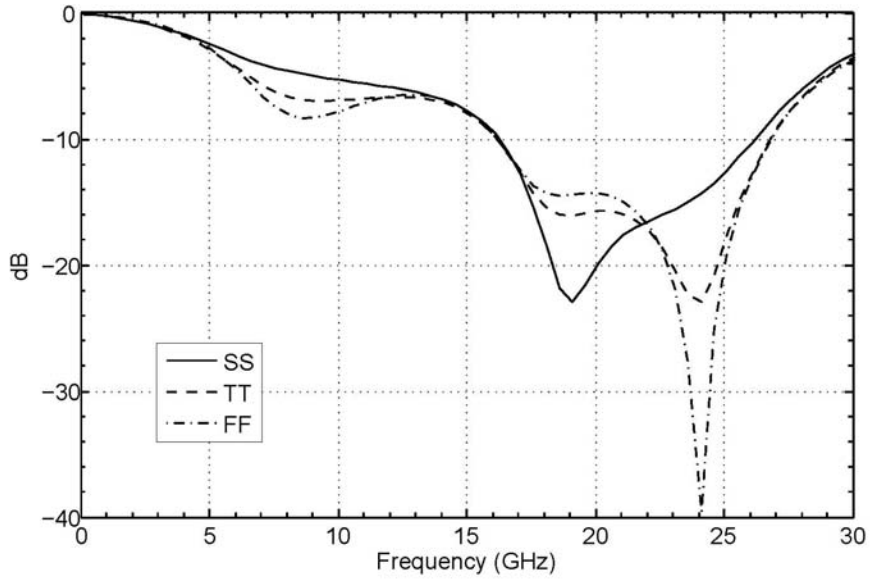*Fig. 2-21 Layout of the Wide-IF-band 17.4-26.1GHz mixer.*

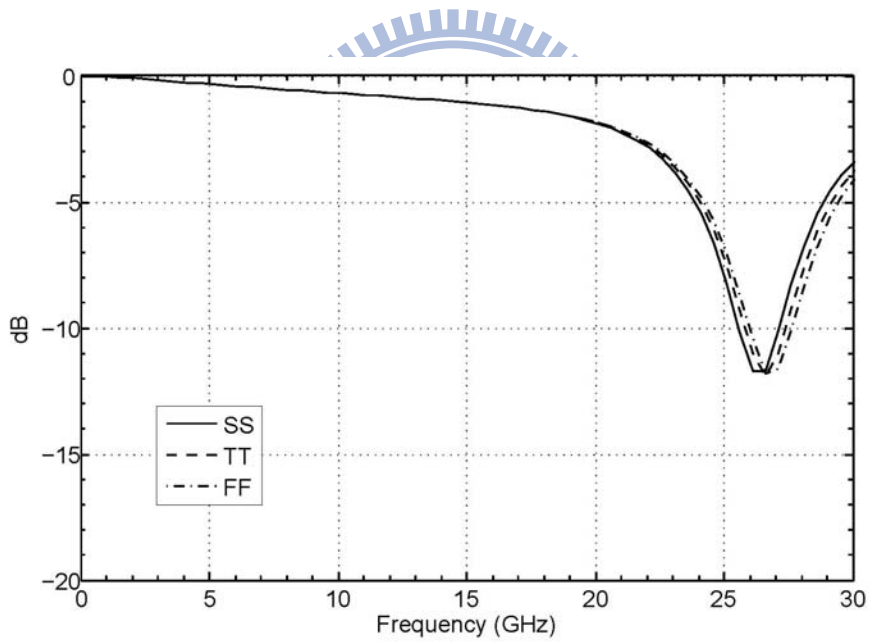*Fig. 2-22 RF port return loss where the RF signal is 17.4-26.1GHz.*

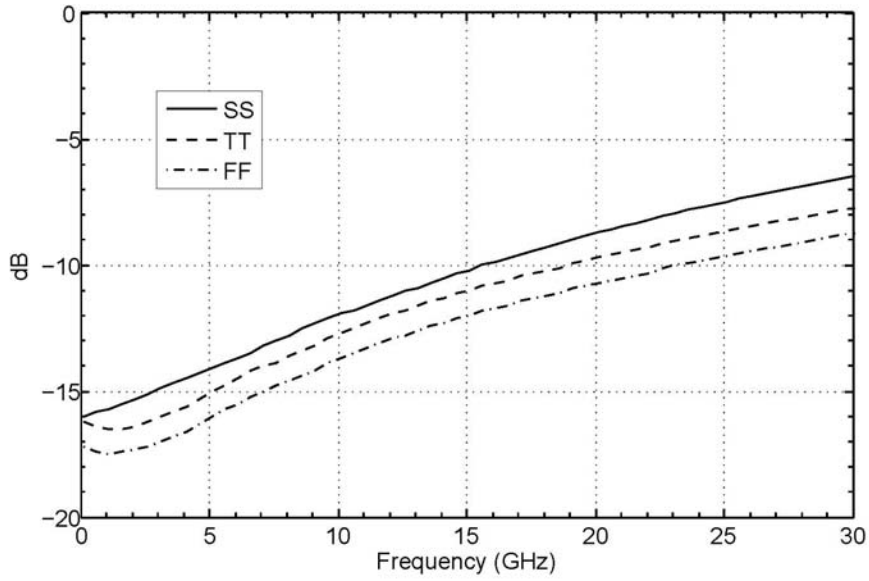*Fig. 2-23 LO port input return loss where the LO is fixed at 26.1GHz.*

Fig. 2-24 IF port return loss for IF equals to DC-8.7GHz.

Fig. 2-25 shows the simulated conversion gain where the variation is less than 3dB within the intended RF bandwidth. Three corner (TT、FF、SS) are employed in the simulation. All the simulated results are acceptable. These performances are all listed in the Table 2-2.
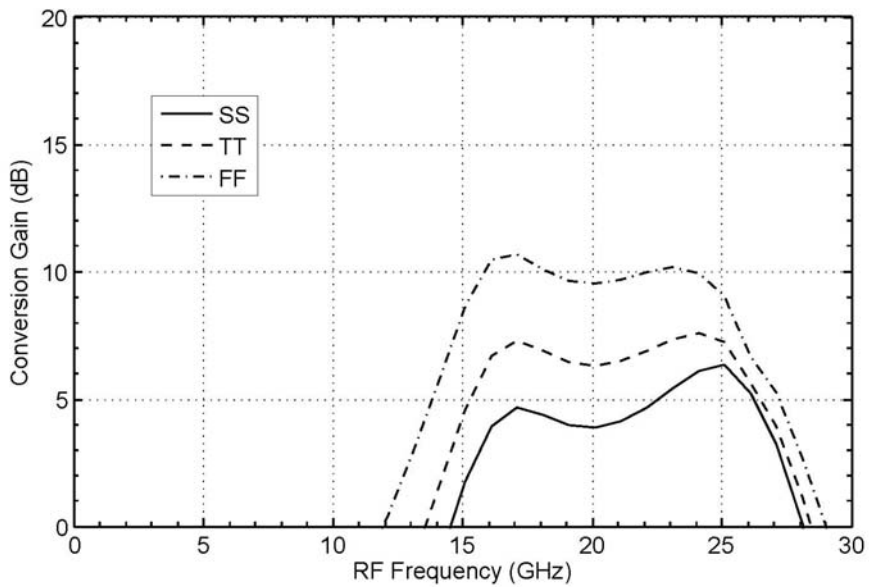
Fig. 2-25 Conversion gain versus RF frequency with LO fixed at 26.1GHz.

Table 2-2 simulated results of the 26.1-34.8GHz Mixer.

	Simulation
Process	TSMC 0.13um CMOS
RF Bandwidth	17.4-26.1GHz
Supply Voltage(V)	1.5V
IF Bandwidth	DC-8.7GHz
RF input return loss	< -10dB
LO input return loss	< -10dB
IF input return loss	< -10dB
Conversion Gain	4dB
Power	30mW

## 2.6 Simulated and measured results of the 26.1-34.8GHz mixer

This mixer is designed with TSMC 0.13um mixed-signal/RF CMOS process, chip size 1.438×1.063 um^2, power consumption 28mW. Fig. 2-26(a) is its layout and Fig.2-26(b) is the chip photograph. We deliver on-wafer measurement in CIC whose instruments are stated previously, the DC and RF probes and measured arrangement are similar as well.
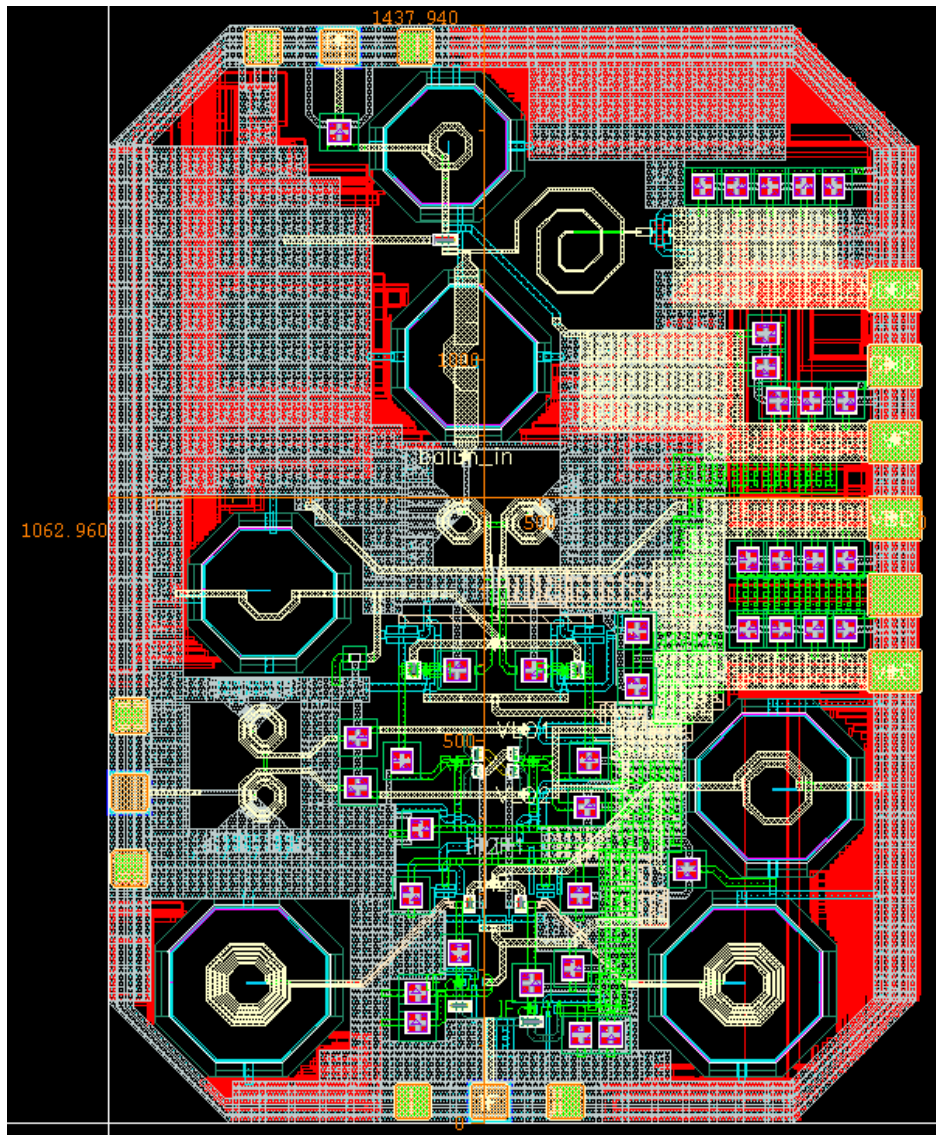
(a)
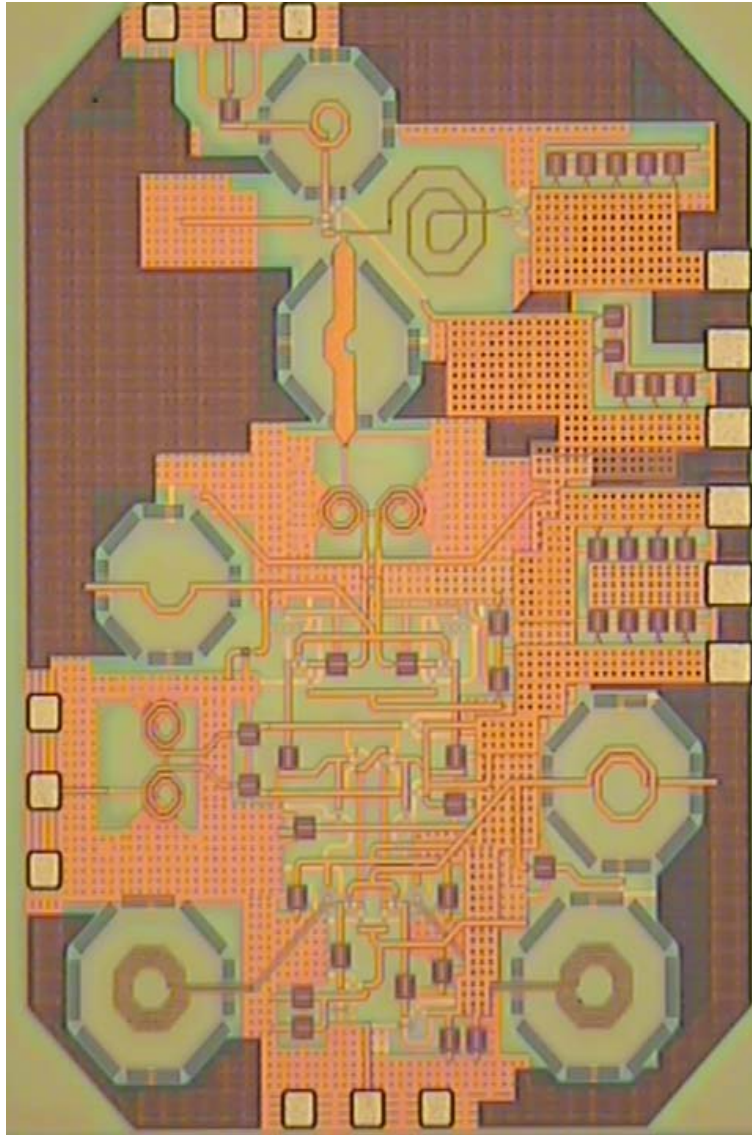
(b)

Fig. 2-26 (a) Layout (b) Chip photograph of the Wide-IF-band 26.1-34.8GHz mixer.

As shown in Fig. 2-27, the RF port return loss is under -10dB for 26.1-34.8GHz in simulation, but the measurement result is -6dB at worst, we will discuss this deviation letter. Fig. 2-28 and Fig. 2-29 show that the LO and IF ports' return loss which are all below -10dB within the intended bandwidth.
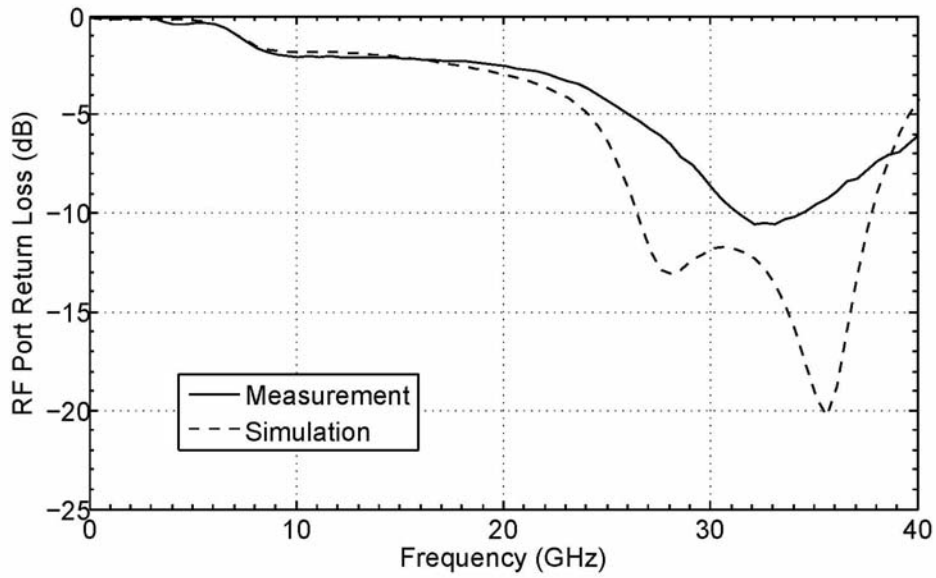
Fig. 2-27 RF port return loss where the RF signal is 26.1-34.8GHz.
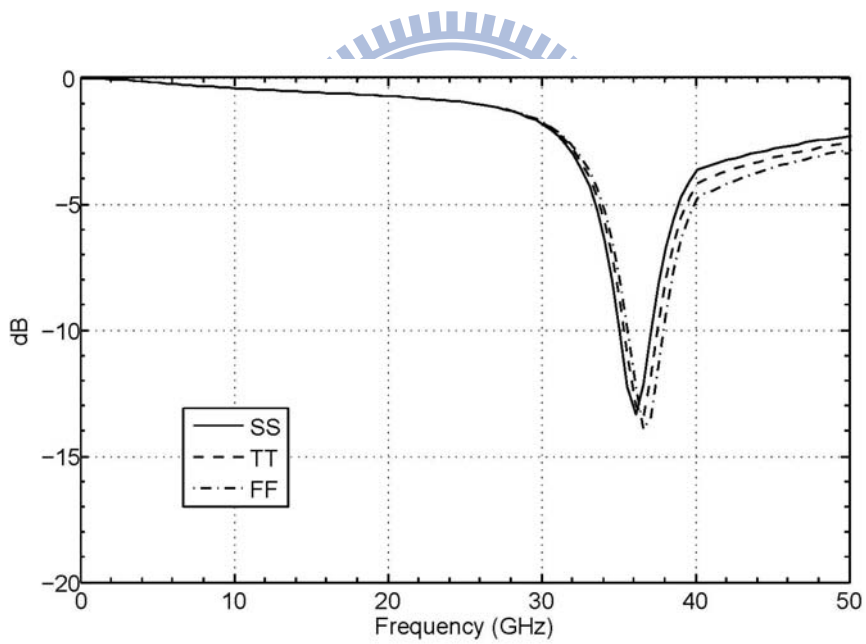
Fig. 2-28 LO port input return loss where the LO is fixed at 34.8GHz.
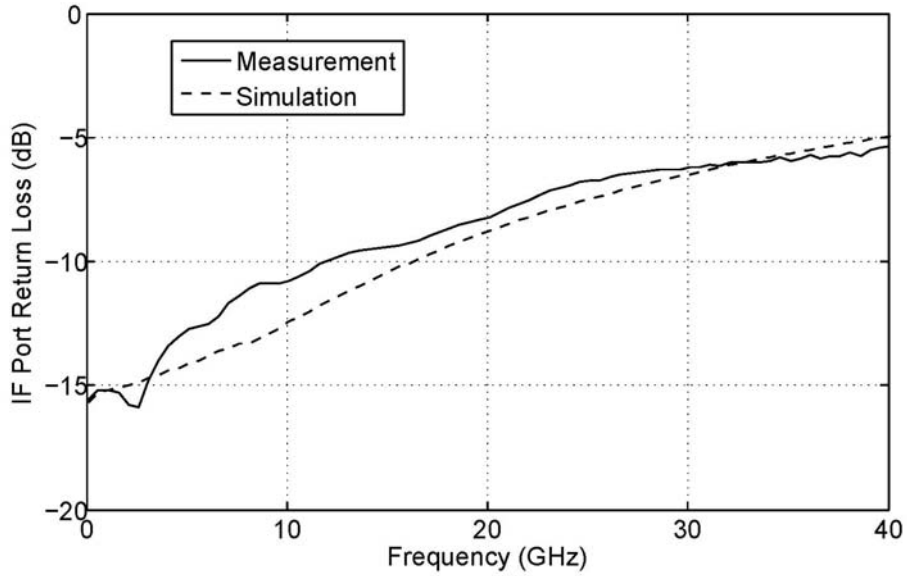
Fig. 2-29 IF port return loss for IF equals to DC-8.7GHz.

Fig. 2-30 shows the simulated and measured conversion gain. The simulated result exhibits an average 3dB conversion gain, and gain variation less than 1dB within the intended RF bandwidth, but the measured result collapses at the lower end and decays 3dB at the higher end of RF bandwidth. We will discuss this discrepancy between simulation and measurement letter.

Fig. 2-30 Conversion gain versus RF frequency with LO fixed at 34.8GHz.

The comparison of simulated and measured results is shown in Table 2-3. The first discrepancy between them appears on RF input return loss, and we consider that it's because the source inductor of the first transistor. Since its inductance is so small that the process doesn't provide in the existed model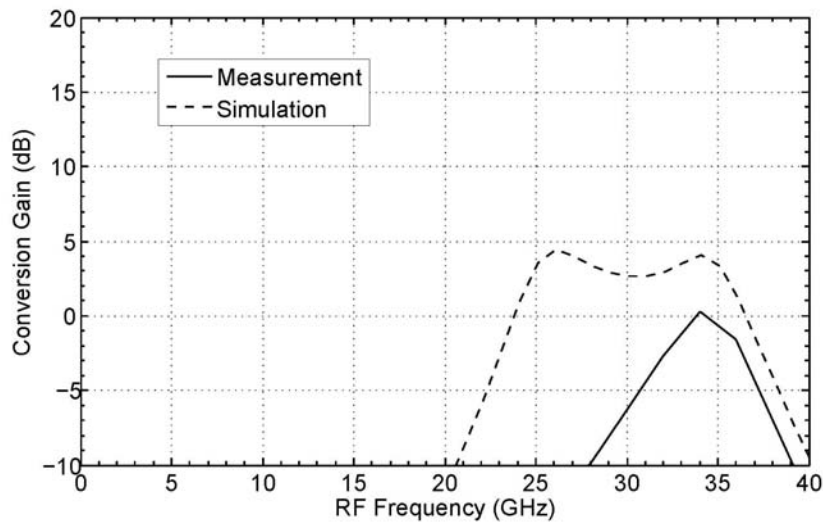, we must fabricate this inductor using EM tools (ADS Momentum and sonnet), and the set-up on the substrate exploiting in EM simulation may exist some inaccuracy, thus influences the inductance and finally degrades the RF input return loss.

Conversion gain is the second inconsistent point, and we think it's primarily due to the poor input matching which reduces the power pumps into the circuit and then affects the available power on the output port. Moreover, since the operating frequency is up to 35GHz, thus the connecting lines may decay the signal power dramatically. For these two reasons, the measured conversion gain are largely degraded against the simulated result.

Table 2-3 Comparison of the 26.1-34.8GHz Mixer's simulated and measured results.

	Simulation	Measurement
Process	TSMC 0.13um CMOS	
RF Bandwidth	26.1-34.8GHz	26.1-34.8GHz
Supply Voltage(V)	1.5V	1.5V
IF Bandwidth	DC-8.7GHz	DC-8.7GHz
RF input return loss	< -10dB	< -6dB
LO input return loss	< -10dB	--
IF input return loss	< -10dB	< -10dB
Conversion Gain	3dB	-10-0dB
Power	28mW	20mW

2.7 Wide-IF-band sub-harmonic mixer design

A. Mixer circuit design

Since the mixer used to down-convert the highest IF band requires the LO frequency to be 34.8GHz, designing the corresponding LO circuit, especially the 34.8GHz power amplifier, will be very difficult. Hence, we would like to modify the mixer circuit to lessen the LO burden, and the most straightforward approach is the use of sub-harmonic mixer which needs only 17.4GHz LO frequency. We exploit the same stages as previous mixers just different on wiring in the mixer core, but due to the large number of mixing transistors (eight!) and the required 90-degree LO phase, a double-balanced sub-harmonic mixer still needs to use large LO power and takes large chip area. By contrast, single-balanced sub-harmonic mixer in this frequency range will require less LO power and occupy a smaller area. The poor RF-IF port isolation for the single-balanced mixer could be improved by inserting additional components, like the $\lambda/4$ open and short transmission lines, or series or shunt LC tanks.

B. Simulated results of the double-balanced sub-harmonic mixer

This mixer is designed with UMC 90nm Logic & Mixed-Mode CMOS process, chip size 1.272×0.906 um^2, power consumption 37mW. Fig. 2-31 is its layout. As shown in Fig. 2-32, the RF port return loss is under -10dB for 26.1-34.8GHz, and the LO and IF ports' return loss are all below -10dB within the intended bandwidth. Fig. 2-33 shows the simulated conversion gain where the variation is less than 3dB within the intended RF bandwidth. The simulated results are acceptable. These performances

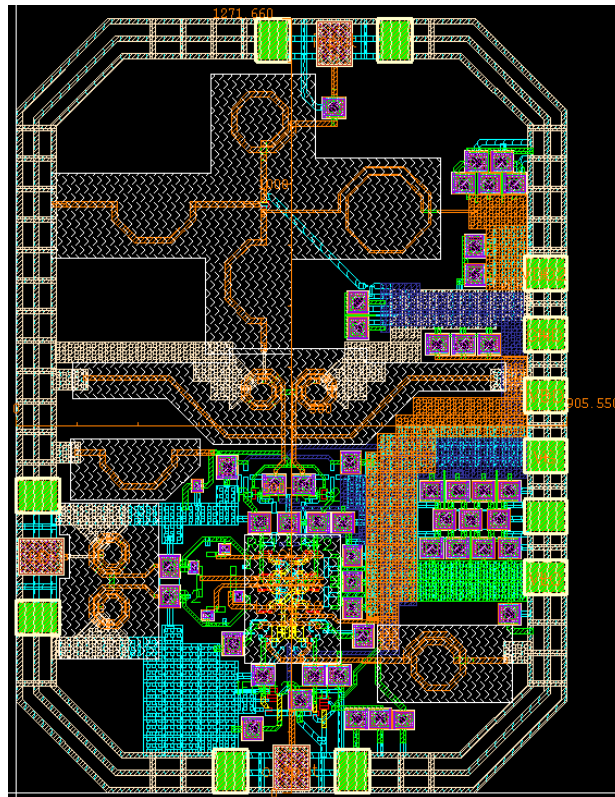are all listed in the Table 2-4.

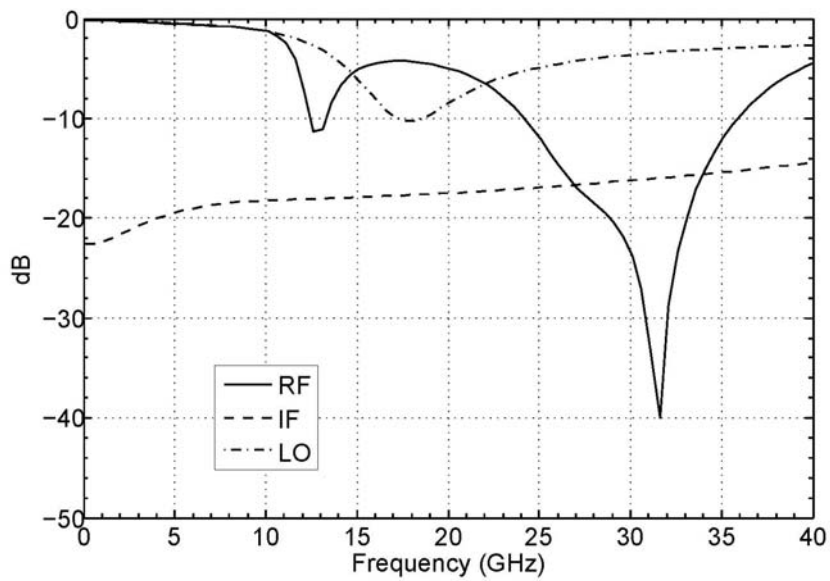*Fig. 2-31 Layout of the Wide-IF-band double-balanced sub-harmonic mixer.*

Fig. 2-32 RF, IF and LO port return loss where the RF signal is 26.1-34.8GHz, LO fixed at 17.4GHz

and IF equals to DC-8.7GHz.

33

Fig. 2-33 Conversion gain versus RF frequency with LO fixed at 17.4GHz.

Table 2-4 simulated results of the double-balanced sub-harmonic Mixer.

	Simulation
Process	UMC 90nm CMOS
RF Bandwidth	26.1-34.8GHz
Supply Voltage(V)	1.5V
IF Bandwidth	DC-8.7GHz
RF input return loss	< -10dB
LO input return loss	< -10dB
IF input return loss	< -10dB
Conversion Gain	4dB
Power	37mW

C. Simulated results of the single-balanced sub-harmonic mixer

This mixer is designed with TSMC 0.13um mixed-signal/RF CMOS process, chip size 1.29×1.26 um^2, power consumption 42mW. Fig. 2-34 is its layout. As shown in Fig. 2-35, the RF port return loss is under -10dB for 26.1-34.8GHz, and the LO and IF ports' return loss are all below -10dB within the intended bandwidth. Fig. 2-36 shows the simulated conversion gain where the variation is less than 3dB within the intended RF bandwidth. The simulated results are acceptable. These performances are all listed in the Table 2-5.

Fig. 2-34 Layout of the Wide-IF-band single-balanced sub-harmonic mixer.

Fig. 2-35 RF, IF and LO port return loss where the RF signal is 26.1-34.8GHz, LO fixed at 17.4GHz and IF equals to DC-8.7GHz.
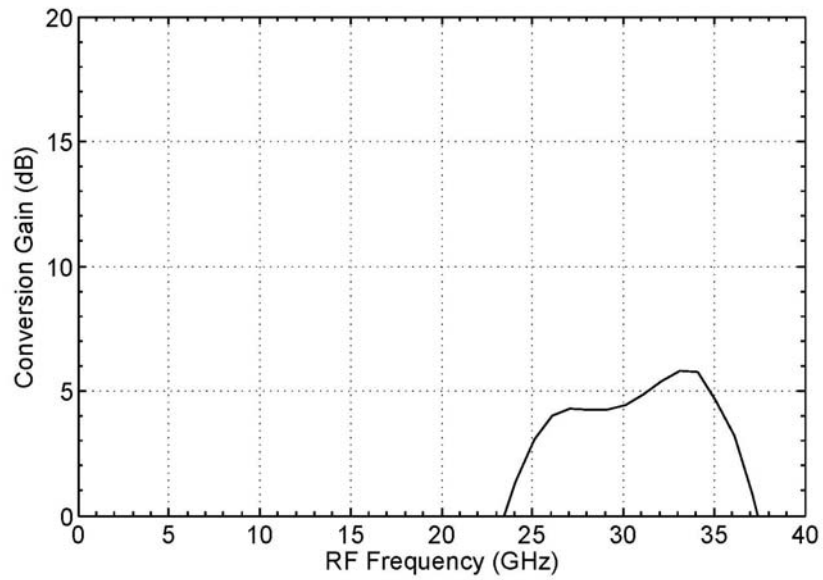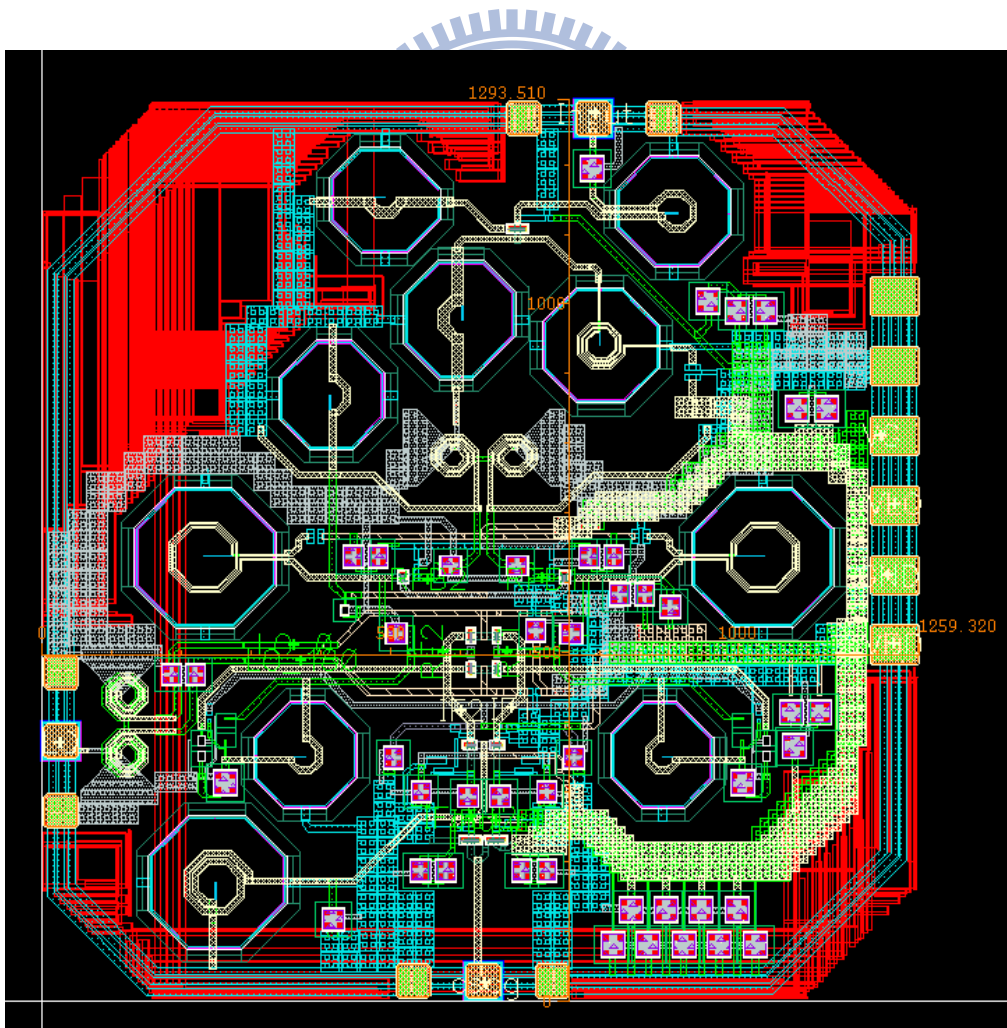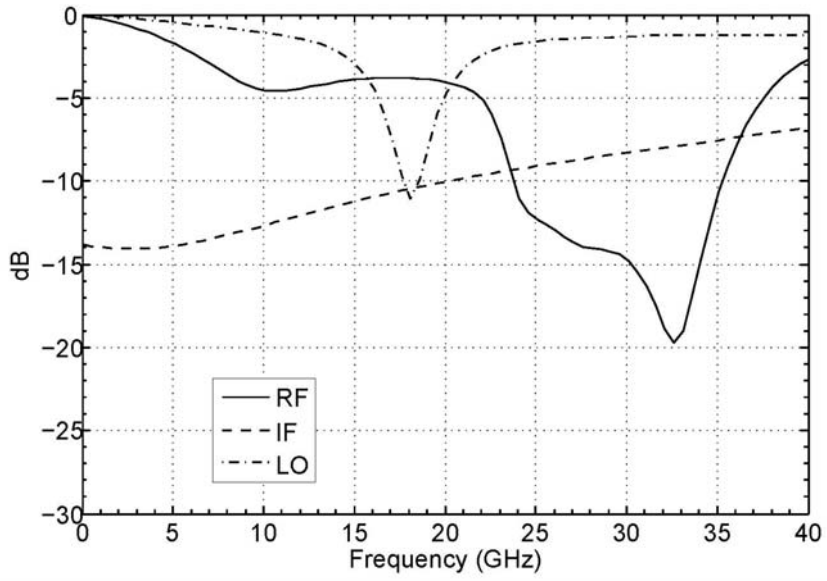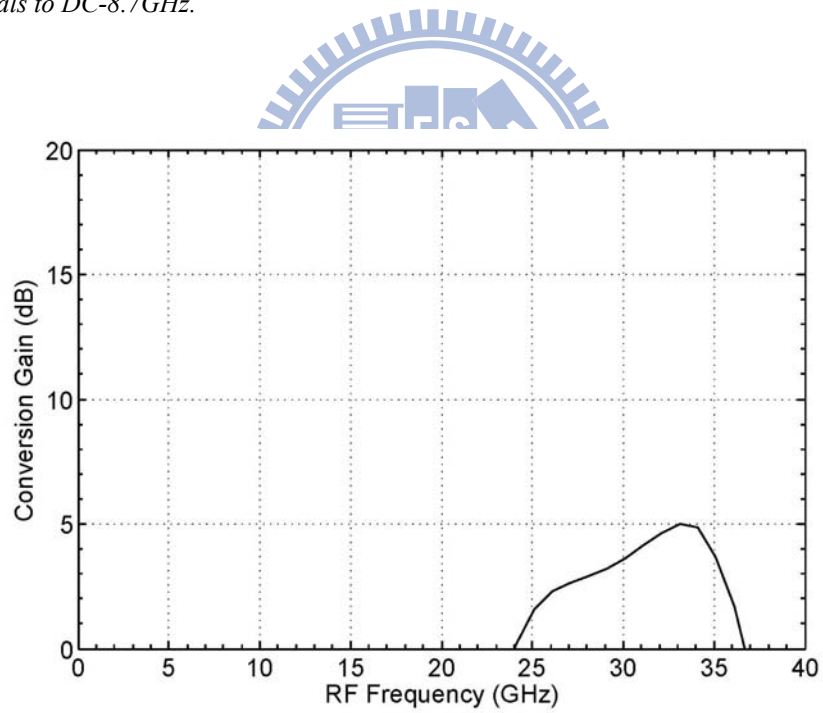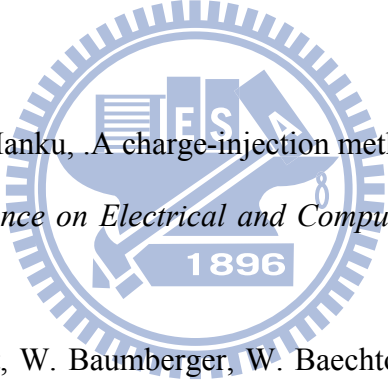

Fig. 2-36 Conversion gain versus RF frequency with LO fixed at 17.4GHz.

Table 2-5 simulated results of the single-balanced sub-harmonic Mixer.

	Simulation
Process	TSMC 0.13um CMOS
RF Bandwidth	26.1-34.8GHz
Supply Voltage(V)	1.5V
IF Bandwidth	DC-8.7GHz
RF input return loss	< -10dB
LO input return loss	< -10dB
IF input return loss	< -10dB
Conversion Gain	3dB
Power	42mW

2.8 Reference

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Chapter 3

Discussion on Inconsistency between Simulation and Measurement

3.1 Introduction

In this chapter, we are going to discuss the inconsistent between simulation and measurement of the two measured mixers. There may be some factors that result in the discrepancies, but our purpose is to find the decisive one. Furthermore, since the factor of inconsistent may be different, we will discuss these two mixers in separate paragraphs, chapter 3.2 is the 8.7-17.4GHz mixer, chapter 3.3 is the 26.1-34.8GHz mixer, and chapter 3.4 is our conclusion. In the discussion, we first think extensively to assume various possibilities and then examine each possibility through simulation to make sure which one is the source of the inconsistent.

3.2 The 8.7-17.4GHz mixer

The simulated and measured results are shown on Fig. 3-1 to 3-4, the variation of input and output matching can be easily achieved by slightly tuning the matching inductors (the gate and source inductor of the first transistor) or the power supply voltage. Hence we believe that this inconsistent is due to process variation and corner selection. Furthermore, though the input and output matching are not fit the simulated results, yet they both satisfy the system specification, namely -10dB, so we must concentrate on the problem of conversion gain. The measured conversion gain suffers from about 6dB degradation at 8.7GHz, lower (RF) frequency end, and about 4dB degradation at 17.4GHz, higher (RF) frequency end. Obviously, the conversion gain

in the lower RF frequency end decreases more than the higher ones, in other words, the higher IF frequency decreases more than the lower ones; this point may provide some clue on our inspection.
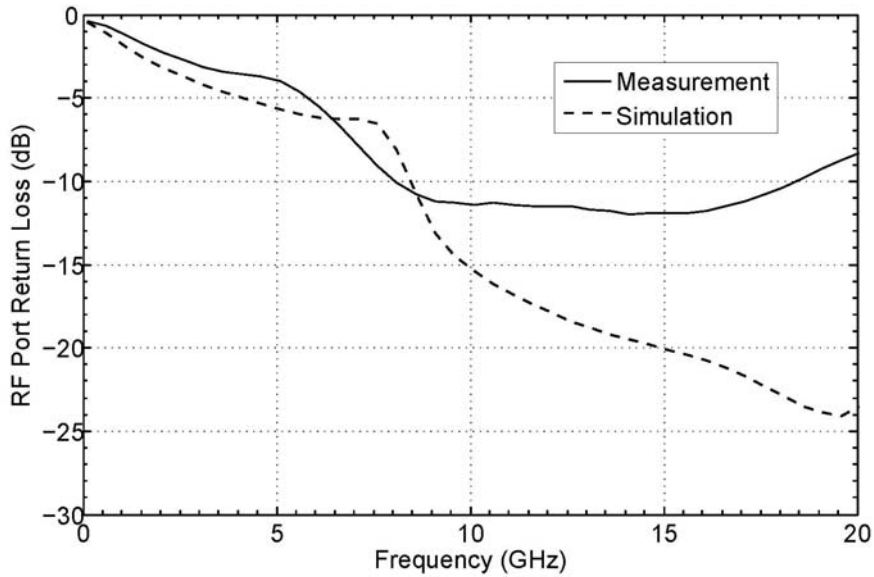

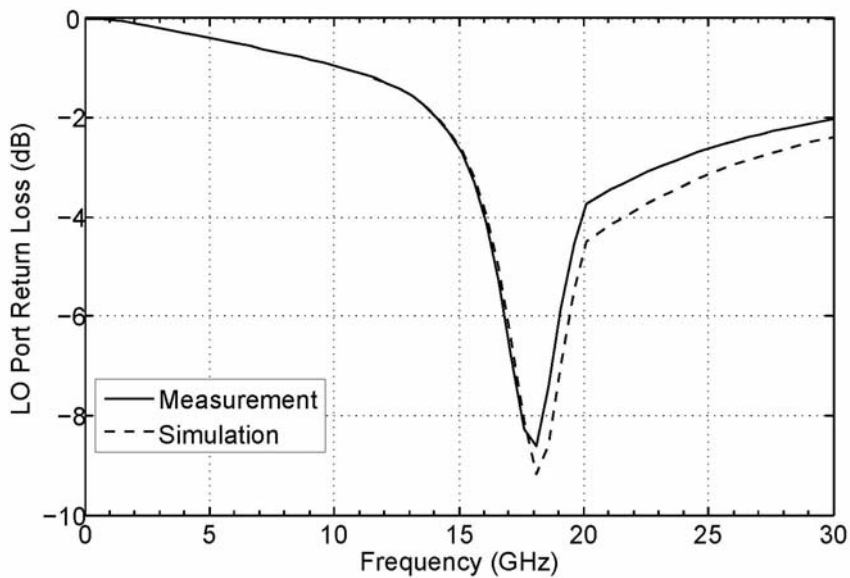*Fig. 3-1 RF port return loss where the RF signal is 8.7-17.4GHz.*

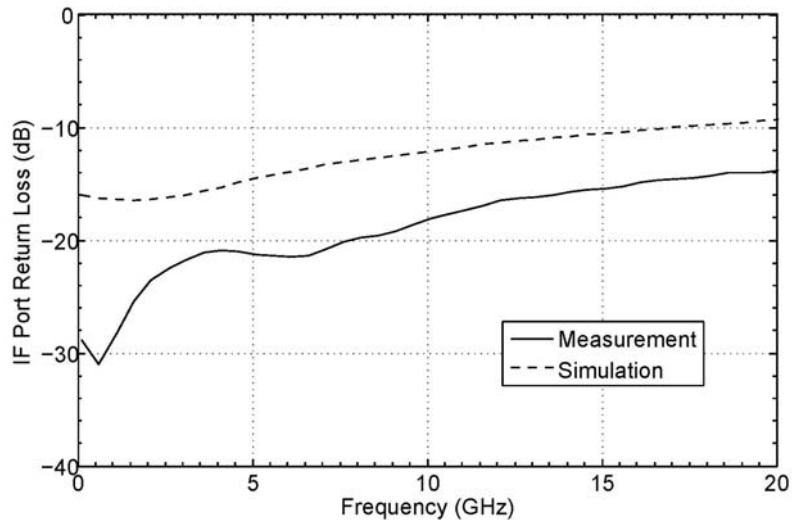*Fig. 3-2 LO port return loss where the LO signal is fixed at 17.4GHz.*

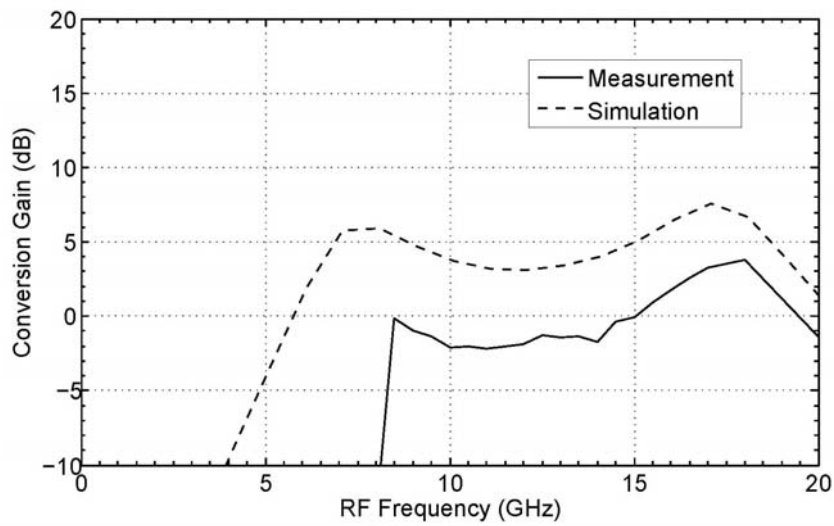*Fig. 3-3 IF port return loss where the IF signal is DC-8.7GHz.*

Fig. 3-4 Conversion gain versus RF frequency with LO fixed at 17.4GHz.

A. The inductor series with *LC*-tank

The first assumption is on the inductor series with *LC*-tank of RF and IF differential pairs, if the *LC*-tank's ground not be treated well, it can be seem as series with a small inductor, and it's the practical case in our floor plan as plot in Fig. 3-5. Though we utilize differential pair as amplifier stage that the source of transistors is a virtual ground, but if the signal on the transistor's gate is not perfectly differential, that is, 180 degrees out-of-phase, the small inductor may be seem by transistors' source and then influenced its gain.
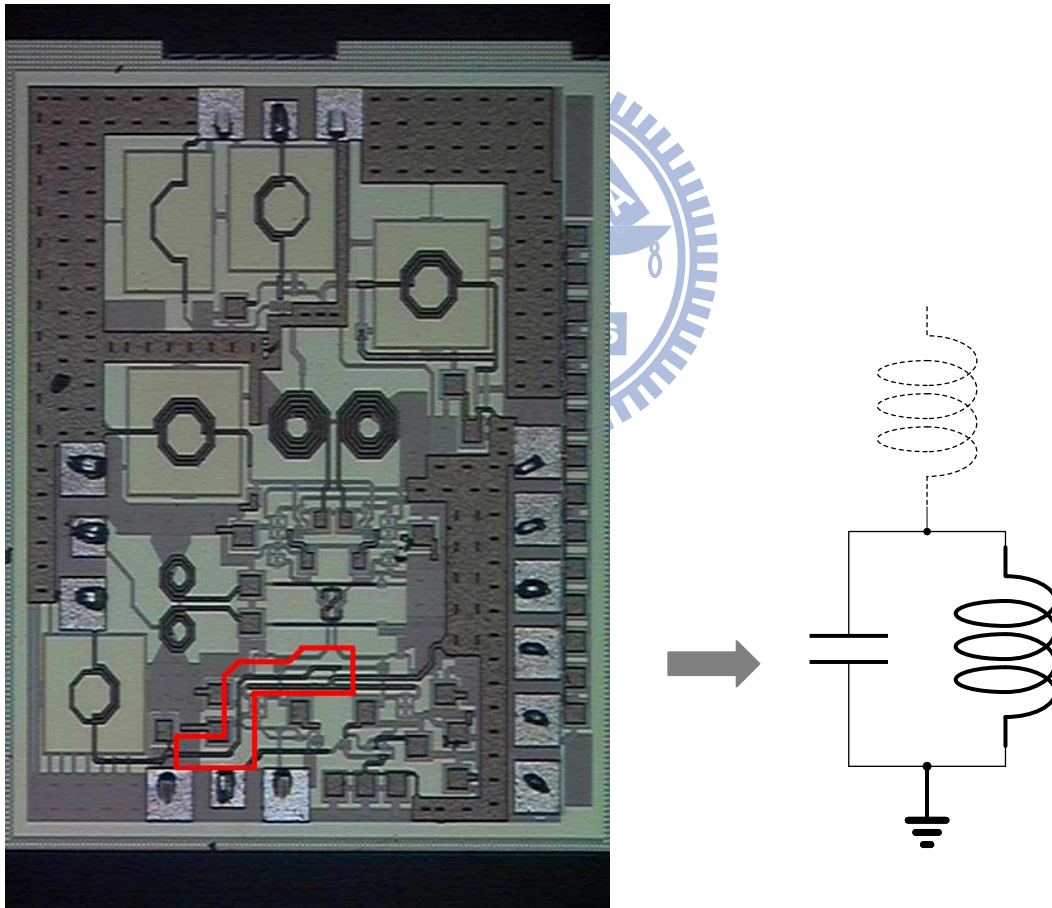

Fig. 3-5 Schematic of the inductor series with LC-tank.

To verify our suspicion, we inspect the gain response of the differential pair when its input signal has 10% variation from fully differential; the test structure is depicted in Fig. 3-6. All the elements' parameters are the same with the IF differential pair since the conversion gain decrease mostly on the higher RF frequency end, which is just the higher IF frequency end, and the series inductor in the source LC-tank will right reduce more gain on the higher frequency. Therefore we doubt that the inconsistent may occur on IF stage. Besides, the inductor series with LC-tank is about 0.3nH extracting from layout.
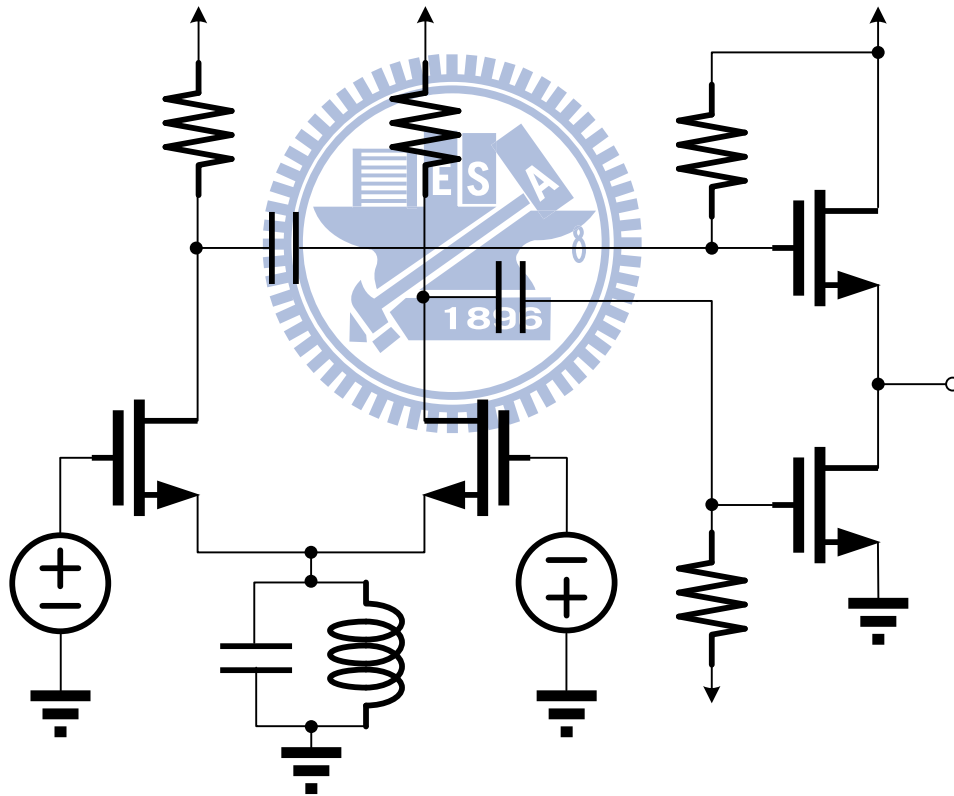

Fig. 3-6 Schematic of the test structure.

The simulation results are shown in Fig. 3-7, curve 1 is the conversion gain without input signal variation, curve 2 is that with 10% variation in magnitude, and curve 3 is that with 10% variation in phase. We can see that variation in phase influence more than magnitude on conversion gain, yet no matter magnitude error or phase error does not exhibit obvious degradation on conversion gain. Consequently from simulation results, we reject the possibility of the series inductor.
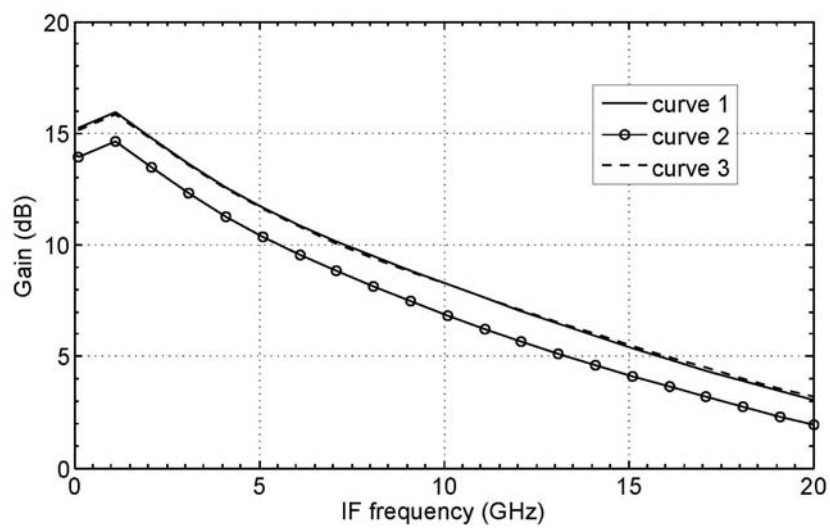

Fig. 3-7 Gain of the test structure within the series inductor in the LC-tank. Curve 1 is the gain without input signal variation, curve 2 is that with 10% variation in magnitude, and curve 3 is that with 10% variation in phase.

B. Mixer core bias

The following guess is on the mixer core bias. In the design strategy we set V_{ds} to 0V to extend mixing bandwidth, and choose V_{gs} close to transistor's threshold voltage, V_t, to enhance the conversion efficiency. However, the conversion gain flatness is very sensitive to the mixer core bias V_{gs}, namely V_{LO}, so we think it may be the source of the conversion gain degradation.

Fig. 3-8 shows the conversion gain versus RF frequency as V_{LO} equals to 0.6, 0.8, and 1.0V respectively. We can see that the conversion gain deviates severely when V_{LO} decreases from V_t at the lower RF frequency end, but sustains about the same at the higher RF frequency end, that is, we may supply improper bias on the mixer core so that it doesn't work correctly on the lower frequency end; accordingly we obtain the inconsistent conversion gain as measured.
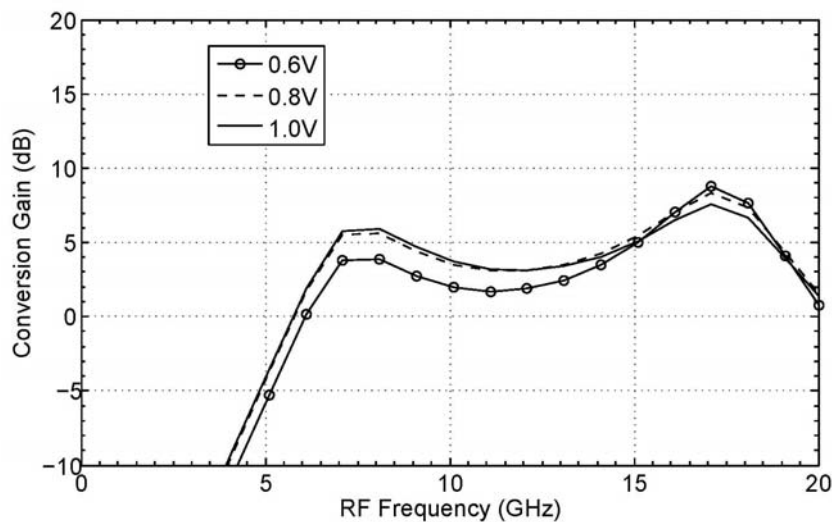

Fig. 3-8 Conversion gain versus RF frequency under VLO equals to 0.6, 0.8, and 1.0V respectively.

To confirm our dubitation, we conduct a re-measurement on this mixer. Instead of directly measured the conversion gain versus RF frequency using simulated bias, we first input an 8.7GHz signal and focus on the desired IF tone on the spectrum, and tune V_{LO} to obtain a set of bias that maximize its power spectrum, then redo it using 17.4GHz input iteratively to find the optimum V_{LO}. However we find out that the optimum V_{LO} doesn't differ from simulated value too much and so does the re-measured conversion gain. Besides, the influence of V_{LO} though can result in the gain inclines to the lower frequency end, but it cannot interpret the level shift of the overall gain, so we think this assumption still is not the answer of our problem.

C. Ground plane

At the time I come to the dead end, a classmate's research give me the inspiration. His low noise amplifier (LNA) also suffer from gain degradation, and he finally found that it's caused by ground plane of the whole circuit, especially that of common source stages. As simulation, software treats every ground node as ideal ground, but in the physical layout, we connect them to the real ground of RF probe via wide metals above 20μm, namely, ground plane. Though it's so wide but the residual inductive effect still results in source degeneration and leads to gain degradation.

The above-mentioned problem may occur on our circuit as well. Although we employ differential pair as amplifier stages that the virtual ground node prevent imperfect ground effect, but the input matching transistor and output common-source-common-drain transistors still suffer from it. In addition, the ground of Marchand balun is also likely to be a big problem.

To verify our suspicion, we add the ground plane to EM-simulation especially that of input matching transistor, output common-source-common-drain transistors,

and Marchand balun, the three parts we discussed previously, and simplify the RF signal path to minimize simulation time. Moreover, since the source *LC*-tank in RF and IF differential pairs are so close to LO balun that the large power LO signal may couple to them accidentally, they are delivered to EM-simulation too. The EM-simulated layout is shown in Fig. 3-9.
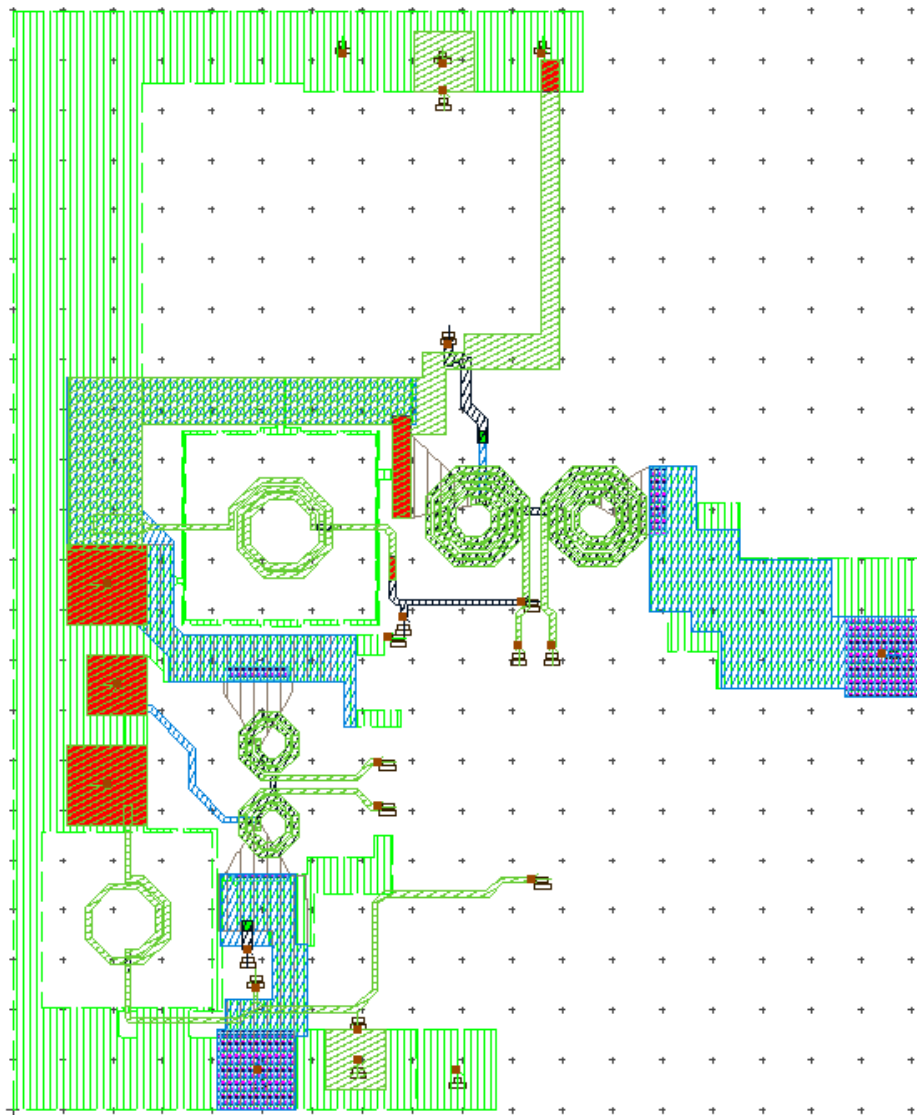

Fig. 3-9 EM-simulated ground plane, balun, and LC-tanks.

Applying the EM-simulated component to the circuit simulation, we find out that ground plane of input matching transistor, common-source-common-drain transistors, and *LC*-tanks don't produce obvious influence on the conversion gain. However, that of the two Marchand baluns' affect the circuit very much, especially the LO balun. This may be caused by asymmetrical ground plane that one terminal is problematic grounded by inductor's guard ring, which is not wide metal that ideally short to ground. Furthermore, the indirect LO balun's feed line and asymmetrical RF balun's ground plane also violet their balanced performance. The simulated LO and RF balun performance accompanied with and without ground plane is displayed in Fig. 3-10, we can realize the importance of ground plane from it. Eventually, the simulated conversion gain that cooperates with ground plane is shown in Fig. 3-11, it fits with the measured result very well so that we confirm the poor balanced performance that due to ground plane degrades overall conversion gain and results in the inconsistent.
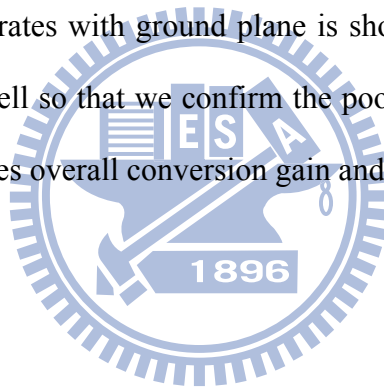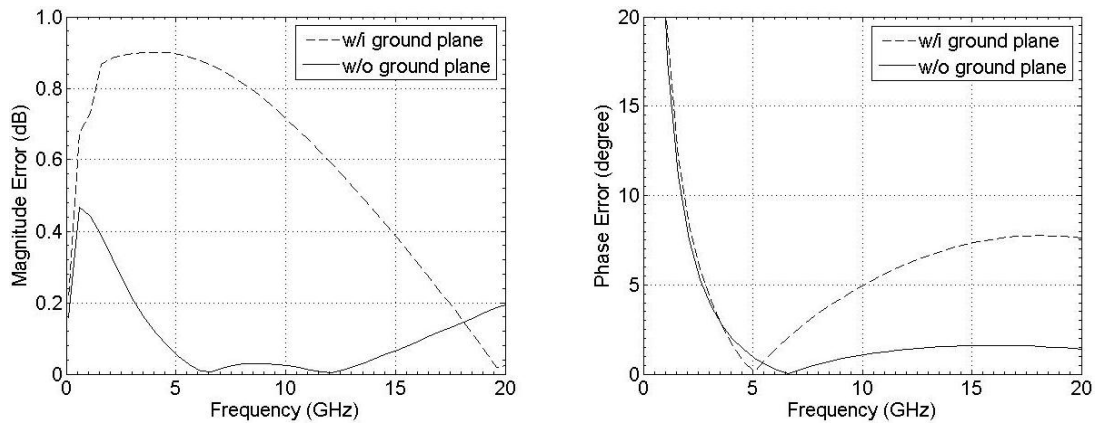
(a)
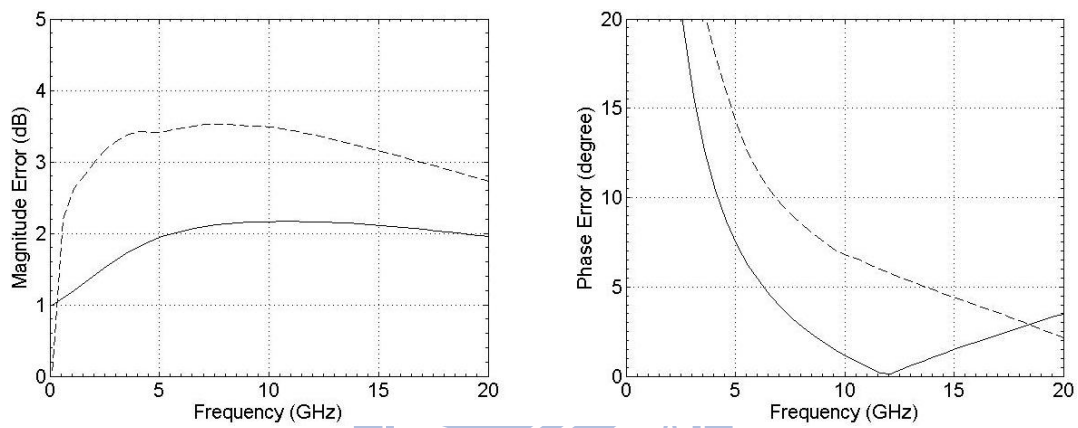
(b)

Fig. 3-10 balanced performance of Marchand balun within and without ground plane. (a) RF balun. (b)
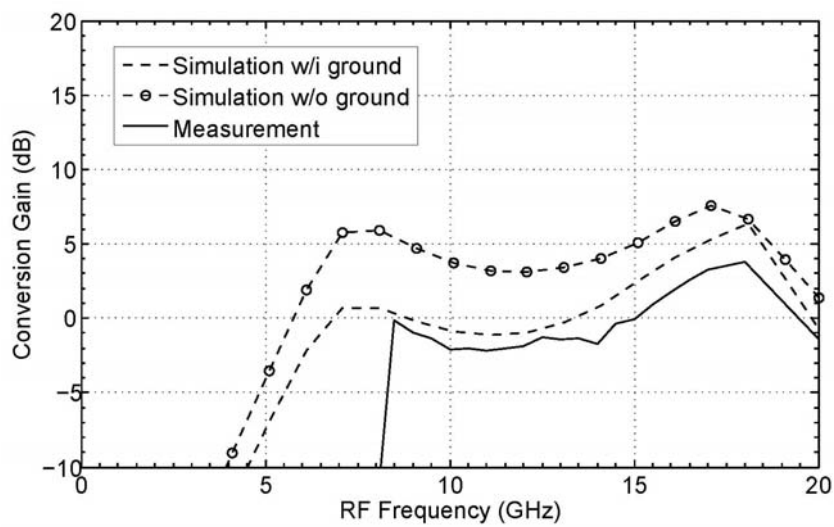
LO balun.

Fig. 3-11 Conversion gain versus RF frequency which is measured, simulated within ground plane, and

simulated without ground plane.

3.3 The 26.1-34.8GHz mixer

Fig. 3-12 to 15 shows the simulated and measured results of the 26.1-34.8GHz mixer. It has problems similar to the 8.7-17.4GHz mixer; they both suffer from gain degradation, especially on lower frequency end. In addition, its input matching also has serious shift that cannot be simply explained by process variation. Hence we will take these two problems into discussion in the following paragraph.
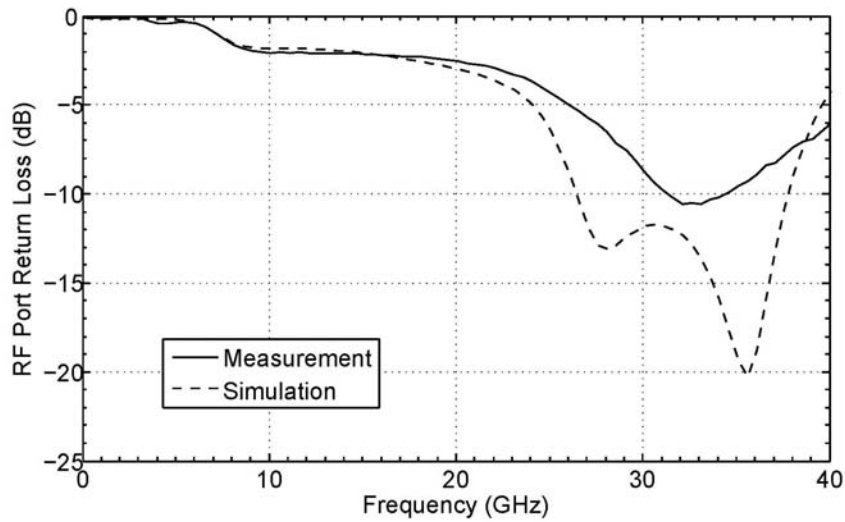

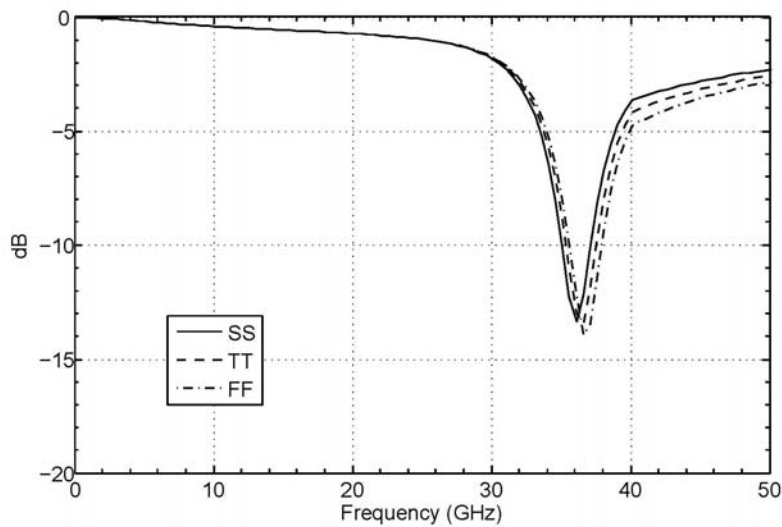*Fig. 3-12 RF port return loss where the RF signal is 26.1-34.8GHz.*

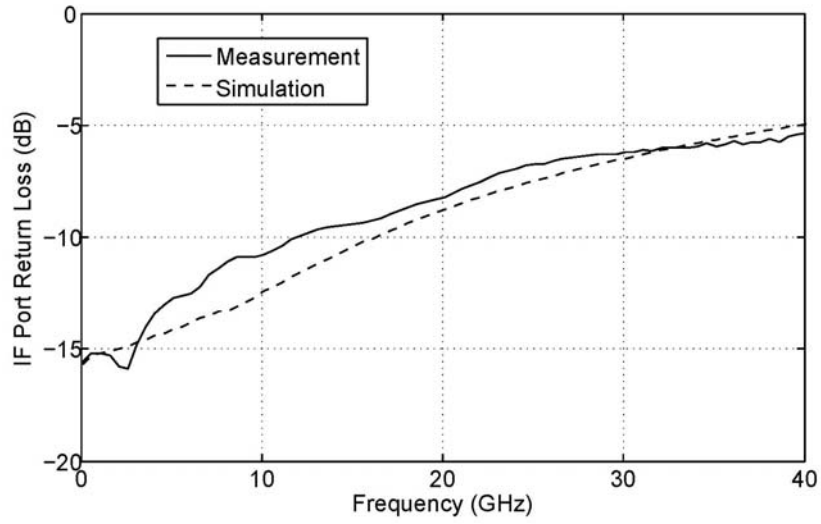*Fig. 3-13 LO port return loss where the LO is fixed at 34.8GHz.*

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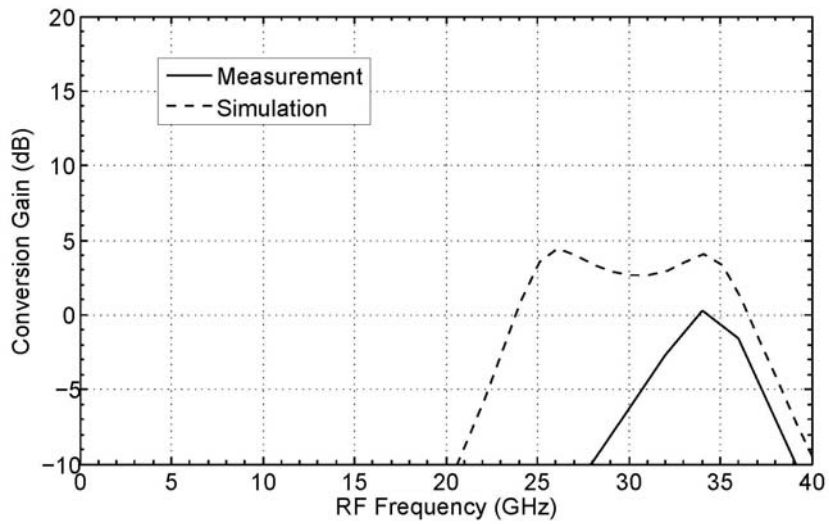*Fig. 3-14 IF port return loss where the IF signal is DC-8.7GHz.*

Fig. 3-15 Conversion gain versus RF frequency with LO fixed at 34.8GHz.

A. Ground plane and EM-simulation setup

As previous work, we realize that although ground plane exhibits severe problem on conversion gain, but it doesn't affect input matching so much, so there must be another factor existed in the shift of input matching. The most possible reason is occurred on our EM-simulation setup, so we re-verify our setup with TSMC's measured raw data and then re-EM-simulate the inductors in input matching stage. As a result, the input matching is shown in Fig. 3-16, and is very similar to measured ones. Besides, we will use this new setup in the following inspection as well.
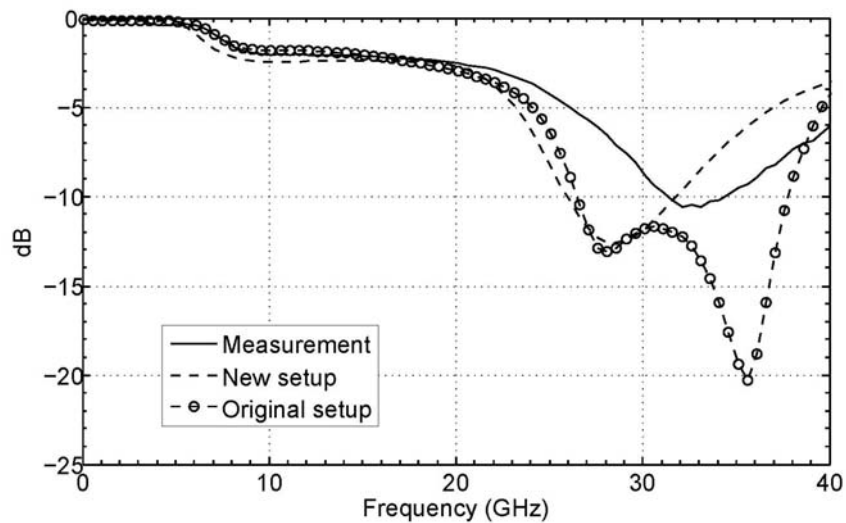

Fig. 3-16 RF port return loss which is measured, simulated with new EM-simulation setup, and simulated with original EM-simulation setup.

With experience acquired from the previous effort, we deliver the ground plane into EM-simulation directly, just as Fig. 13-17 shows, and find out that the problem occurs on the RF balun. The conversion gain simulated with ground plane is shown in Fig. 13-18, it fits with measured result very well; we first doubt that it's because the two peaking inductors, as described in the previous chapter, absorb power in the balun and violet its balance performance. Fig. 13-19 compares the balanced performance that cooperate with both ground plane and two peaking inductors with which without ground plane and the two peaking inductors are EM-simulated separately; however, the latter has a good performance but the former is nothing but a mess.
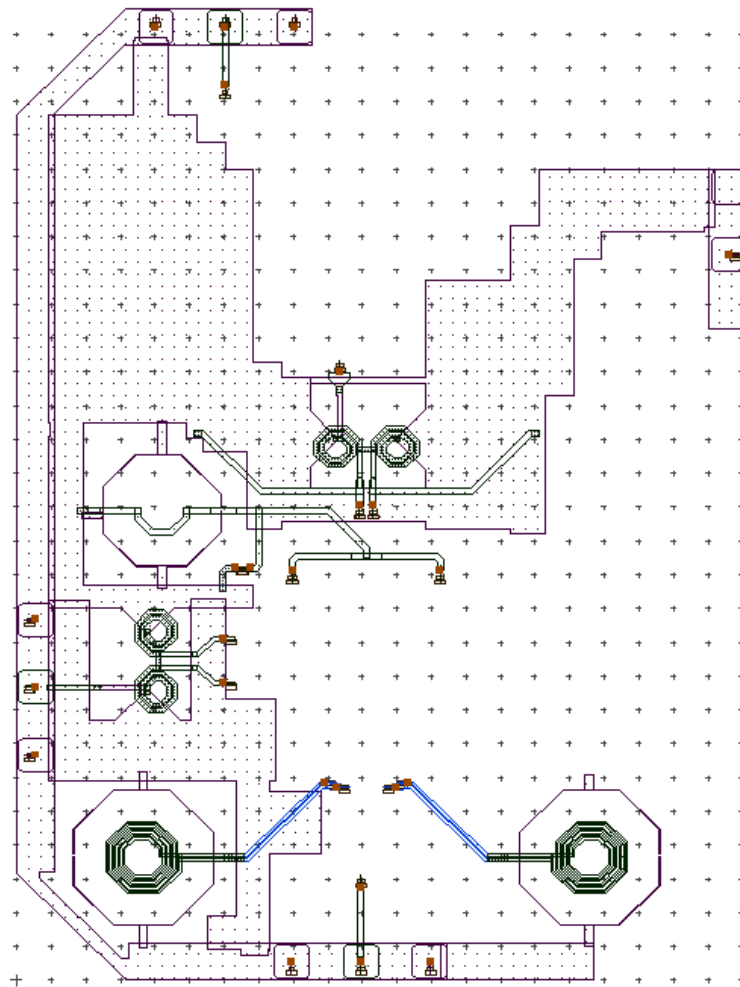

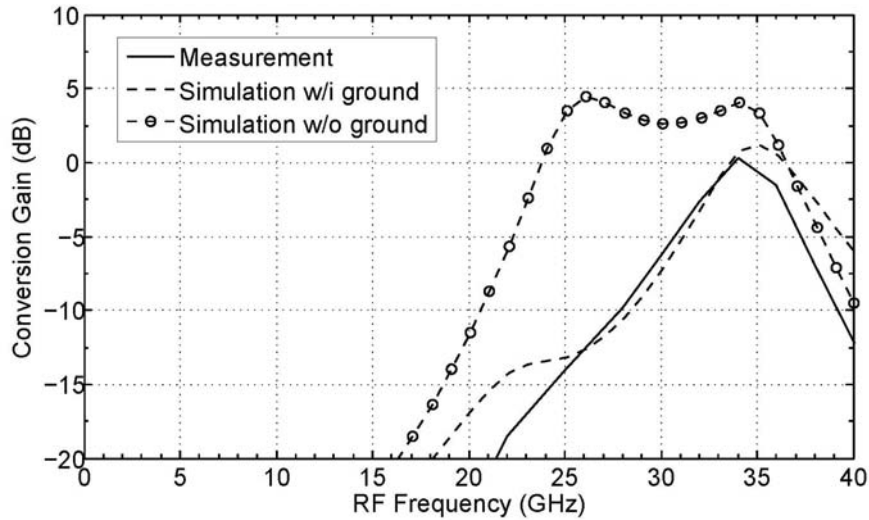*Fig. 3-17 EM-simulated ground plane.*

Fig. 3-18 Conversion gain versus RF frequency which is measured, simulated within ground plane, and simulated without ground plane.
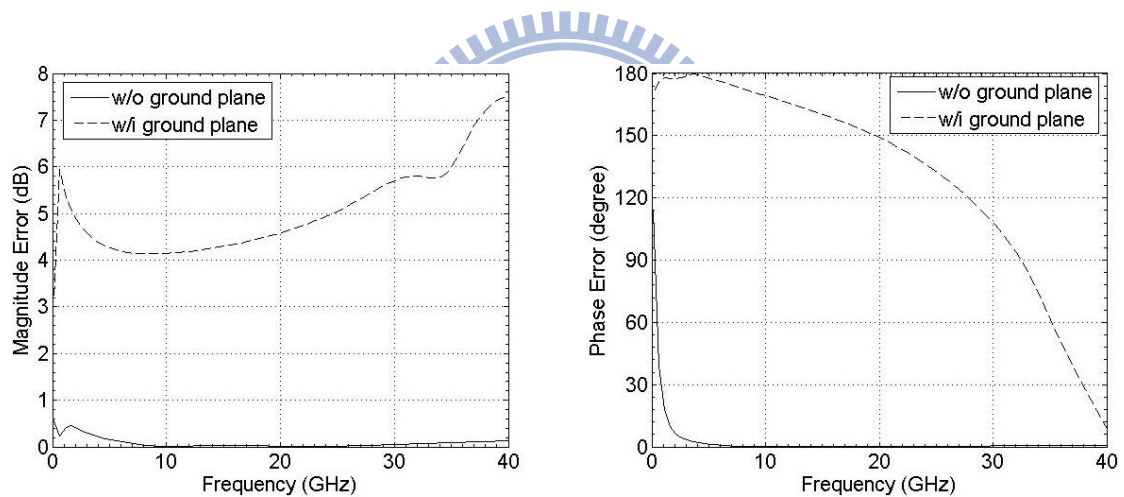

Fig. 3-19 balanced performance of Marchand balun within and without ground plane.

To go one step further, we EM-simulate the balun that with ground plane and without the two peaking inductors, as shown in Fig. 3-20, but surprisingly find that its performance is also very poor, as shown in Fig. 3-21. Tracing from layout, we realize that it must because the ground plane is not perfectly symmetrical that one is connected to RF pad's ground and another is connected to DC pad's so that their shape are not similar enough. Consequently, this point severely influences the balanced performance and then degrades overall conversion gain once again.
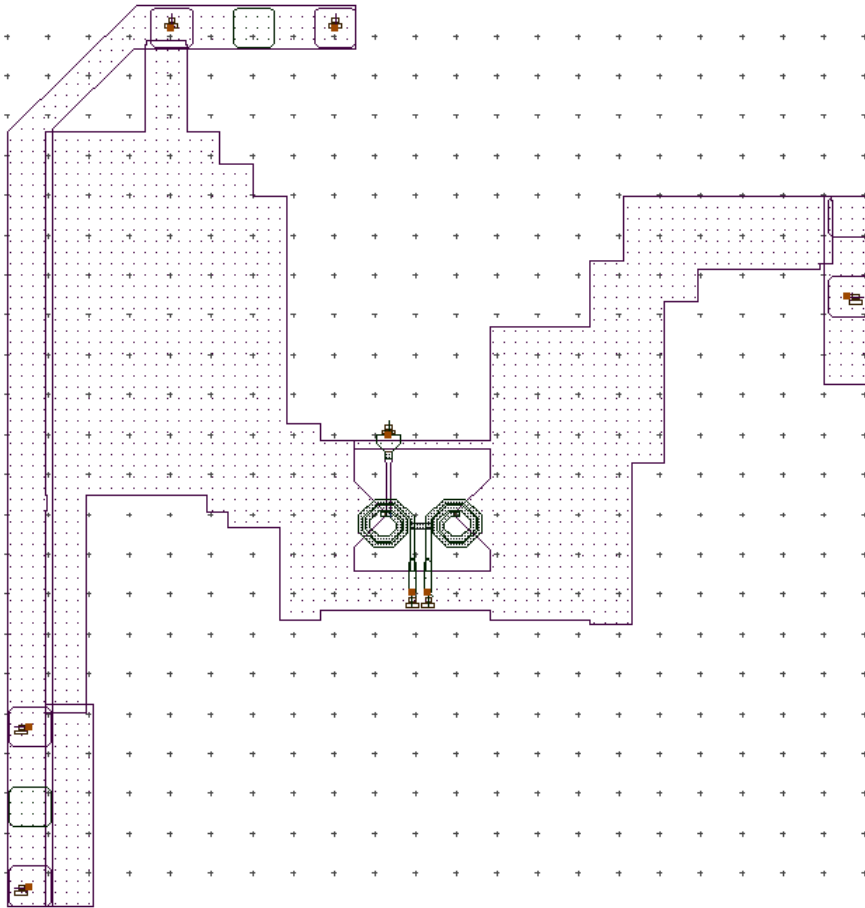
Fig. 3-20 EM-simulated RF balun within ground plane.
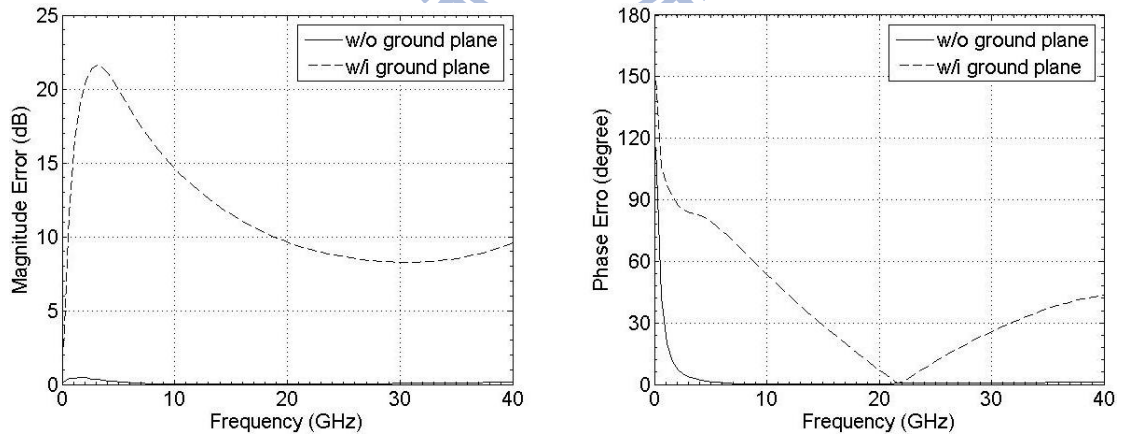
Fig. 3-21 balanced performance of Marchand balun within and without ground plane.

3.4 Conclusion

From the inspection on the problem of our mixers, we realize that the ground plane demands particular attention in details. It not only results in source degeneration that reduces the gain of amplifier stage but also is a decisive factor on passive component's performance. However, specific EM-simulation on ground plane or any other passive components require accurate substrate and software setup, so in the design flow, we must take them into the first step, and then exploit them to consider the influence of the whole ground.
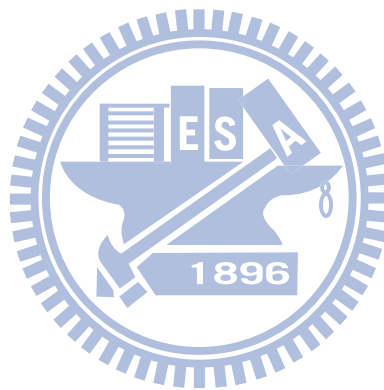
Chapter 4
Conclusion and Future Work

4.1 Conclusion

The thesis is made of several wide-IF-band circuits: they are the 8.7-17.4, 17.4-26.1 and 26.1-34.8GHz fundamental mixers, and the 26.1-34.8GHz double- and single-balanced sub-harmonic mixers. Both resistive biasing scheme and on-chip Marchand balun are employed in these circuits. By incorporating both the wideband matching and amplifying stages into the mixer circuit, we can easily achieve good port return loss, appropriate conversion gain, and moderate linearity. The double-balanced circuit configuration ensures excellent port-to-port isolation. From the measured results, we found that further performance improvement of our mixers, especially the conversion gain, can be made. Though the measured results of the 17.4-26.1GHz mixer and the two sub-harmonic mixers are not available yet at this time of thesis writing, they will be carried out in the summer. As from both simulation and measurement, our mixers exhibit superb wideband performance, and are better than those reported in journal papers or commercially available.

4.2 Future work

A. Theoretical analysis

For the wide-IF-band application, two components still need to be further analyzed; one is on the balun's input impedance and the other is the mechanism of the mixer core. As the S-parameters of Marchand balun shown in Eq. (2-1) are derived with the assumption that the two coupled lines have 90-degree electric length, which

is valid only for the central frequency [1]. When the balun is used in wideband applications, a comprehensive wideband S-parameter of Marchand balun will be needed. Since Marchand balun is composed of two quarter-wave coupled lines, we should start the wideband analysis with a single coupled line. The use of matrix multiplication of two such coupled lines result in the matrix of Marchand balun.

Inside the mixer core, the Gilbert cell is often simplified as a switch controlled by the LO signal. In reality, however, the Gilbert cell is far from a perfect on-off switch, thus the interpretation of Gilbert cell by a square function needs to be revised. This results in that proposed by Abidi [2], where two switching models are suggested: one is hard switching and the other soft switching. The difference between hard switching and soft switching depends on whether the LO signal can be modeled as square wave or sine wave, and the difference will affect the predicted the conversion gain, the IF bandwidth, and the noise performance of the mixer. On the other hand, the conversion matrix originally proposed by Kerr for solving the conversion gain of diode-mixer [3] is then extended and applied to the FET-mixer case [4]. Later, Stephen A. Mass proposed a GaAs MESFET mixer with low inter-modulation [5], where he claimed that, by using a passive MESFET as a time-varying resistor, a low inter-modulation mixer can be obtained. We now plan to analyze the passive transistor (under large LO modulation) using conversion matrix, in order to fully understand its characteristics.
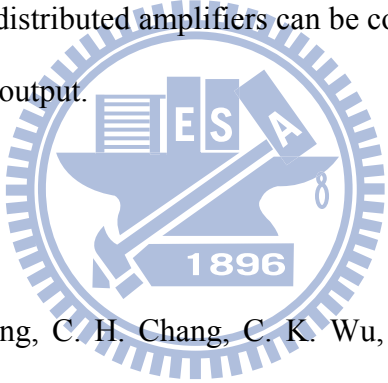
B. W-band wide-IF-band mixer design

The W-band mixer is used to down-convert the 78.3-113.1GHz incoming electromagnetic signals to DC-34.8GHz, with the LO frequency fixed at 78.3GHz. Though the absolute RF band is quite wideband, the relative bandwidth is in fact quite moderate due to its high operating frequency. Again, here we use the zero-biased

resistive mixing core to achieve the broad IF bandwidth of DC-34.8GHz. As the equivalent circuit of the transistor is mainly a variable resistor, this mixer will not only be wideband, but also capable of operating at very high frequency, i.e. 113.1GHz in this case. As the RF input transistor stage may not be able to provide positive gain for frequency higher than 100GHz in the 90nm CMOS case, a better approach might be to start the mixer circuit with the wideband Marchand balun, and then the mixer core (both are independent of the transistor's unit gain bandwidth).

The IF band of DC-34.8GHz, though much lower than the RF bandwidth, is in fact tantalizing and does pose a design challenge. At this moment, we are exploiting the possibility of designing a differential-to-single-ended distributed circuit. Alternatively, two separate distributed amplifiers can be connected to the output of the mixer core to allow dual IF output.

4.3 Reference

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