國 立 交 通 大 學

電信工程學系

碩 士 論 文

3–6 GHz 超寬頻低功率自順向基底偏壓
低雜訊放大器設計

3–6 GHz Ultra-Wideband Low-Power
Self-Forward-Body-Bias Low-Noise Amplifier

研 究 生：李振銘

指導教授：唐震寰　教授

中 華 民 國 九 十 八 年 七 月

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國 立 交 通 大 學

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A Thesis

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摘要

於本論文，我們提出一使用 0.18-μm TSMC CMOS 1P6M 製程應用於超寬頻低頻帶系統之低功率自順向基底偏壓低雜訊放大器。使用自順向基底偏壓技術，可以降低低雜訊放大器的供應電壓並且也可以節省額外的偏壓電路，而使我們的低雜訊放大器在兩個汲極-源極的電壓降之供應電壓為 1.06 V 為低功率消耗。而 LNA 電路裡的互補式架構與第二級直接耦合的方式也節省了額外所需的偏壓電路。由於提出的自順向基底偏壓技術對於雜訊指數有些許不好的影響，因此，我們針對此問題將先前提出的低雜訊放大器之雜訊指數做改善。在本論文的一些圖表中，所提出第一個的低雜訊放大器之量測數據顯示，在功率消耗 6.38 mW 且頻寬為 2.6 至 6.6 GHz，最大增益為 15.5 dB，輸入/輸出阻抗匹配之功率反射係數分別為低於-12 dB 及 -17dB，平均雜訊指數為 3.2 dB。而改善後的低雜訊放大器之量測結果顯示，在功率消耗 4.5 mW 且頻寬為 2.0 至 6.6 GHz 下，最大增益為 16.2 dB，輸入/輸出阻抗匹配之功率反射係數分別為低於-12 dB 及 -16dB，平均雜訊指數為 2.6 dB。

3–6-GHz Ultra-Wideband Low-Power Self-Forward-Body-Bias Low-Noise Amplifier

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Abstract

A low-power low-noise amplifier (LNA) implemented in 0.18-μm TSMC CMOS 1P6M technology utilizing a self-forward-body-biased (SFBB) technique is proposed for UWB low-frequency band system in this thesis. By using the SFBB techniques, it reduces supply voltage as well as saves additional biased circuits used in conventional FBB techniques, which leads to a low power consumption with low supply voltage of 1.06 V for two MOSFETs drain-to-source voltage drops. Using the complementary configuration and inter-stage direct coupling technique also saves the biased circuits. However, the self forward body bias technique will give rise to some noise figure degradation. Therefore, we proposed the second LNA to improve the noise figure of the preceding LNA in this thesis. The measurement result shows that the LNA 1 also presents a maximum power gain of 15.5 dB with a good input/output match (S_{11}< –12 dB/ S_{22}< -17 dB) and an average noise figure of 3.2 dB in the frequency range of 2.6–6.6 GHz while consuming power of 6.38 mW. And the measurement result shows that the NF-improved LNA presents a maximum power gain of 16.2ddB with a good input/output match (S_{11}< -12 dB/ S_{22}< -16 dB) and an average noise figure of 2.6 dB in the frequency range of 2.0–6.6 GHz while consuming power of 4.5 mW.

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李振銘　誌予

九十八年七月

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Chapter 1 *Introduction*

1.1 Background and Problems

Ultra-wideband (UWB) communication techniques have attracted great interests in both academia and industry in the past few years for applications in short-range and high-speed wireless mobile system. The Federal Communication Commission (FCC) has recently approved the 3.1GHz to 10.6GHz full-band for UWB deployment as shown in Figure 1.1. Two recent major proposals [1], [2] for the IEEE 802.15.3a propose that data rate of up to 400–480 Mbps can be obtained using only the low-frequency band (3–6 GHz) of UWB.

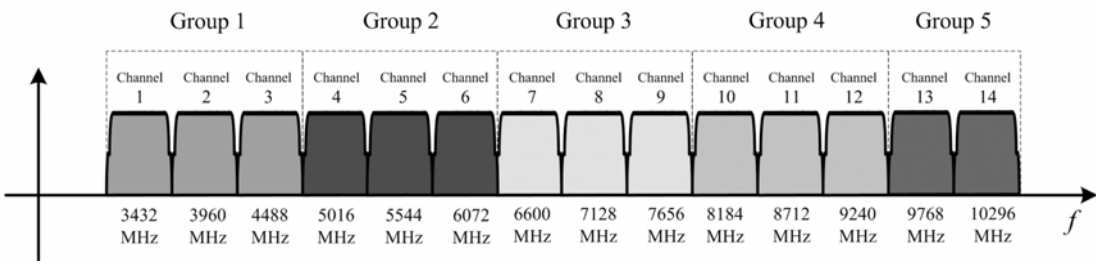


Figure 1.1 UWB Multi-Band OFDM Proposal

One of the most critical blocks in wireless receivers is the low-noise amplifier (LNA) because it needs to amplify the received weak signal. There are several common goals in the design of UWB LNA including the input impedance matching, low noise performance, low power consumption, small sizes, sufficient linearity, and enough power gain to overcome the noise of subsequent stages. Therefore, in the design of LNA, it has to find some ways of achieving these goals.

1.2 Related Works

Several CMOS UWB LNA design techniques have been reported for wideband communication applications, which include current-reused [3], input band-pass filter wideband matching [4], resistive feedback [5], common-gate configuration [6] and distributed architecture [7], etc. The current-reused LNA is composed of two common-source configuration stages under common-DC-current structure that can save power consumption effectively. However, its chip area is large since it usually contains numerous inductors for wideband purpose. In the input-band-pass-filter technique, the ladder band-pass filter is employed for wideband input impedance matching. However, at the input of LNA of this technique, the parasitical resistance of ladder filter would degrade the noise performance. The resistive feedback LNA increases the bandwidth of desired operation frequency at the cost of the gain. Therefore, the higher the gain is, the more amplifier stages we need which yield more consumption of DC power. A common gate (or the $1/g_m$ termination) amplifier has the highest potential to achieve the wideband input matching, good linearity, and input-output isolation, but it leads to lower gain and higher noise figure than using a common source amplifier. The well-developed distributed amplifier is known as its wide bandwidth, but it requires large power consumption and layout area that is not suitable for portable devices.

Here, LNA requires power consumption as lower as possible while achieving acceptable

performance. That may be very important for many potential applications, especially for portable device. In this thesis, we propose a low-power low-noise amplifier (LNA) utilizing self forward body bias (SFBB) technique for wideband applications. The threshold voltage of MOSFET can be lowered by means of SFBB/FBB technique, and then, with the same current amount, we need not the higher supply voltage (1.8 V) supplied in the conventional LNAs in 0.18-μm CMOS technology. The supply voltage of the proposed LNA is only 1.06 V for two drain-to-source voltage drops of MOSFET. With regard to the design of system, biasing the bulk of MOSFETs by the self-bias technique saves the DC power consumption as well since it doesn't need additional bias circuits.

1.3 Thesis Organization

The thesis is organized into five chapters including the introduction. Chapter 2 deals with the basic concepts of low noise amplifier design, and introduces the impedance matching and low noise design method of some popular LNA topologies with their comparison. Chapter 3 reviews the advanced low-power LNA design methods. In chapter 4, proposes low-power self-forward-body-bias UWB CMOS LNA, and the noise degradation resulted from the self-forward-body-bias technique is improved in the second LNA. In Chapter 5, conclusion is drawn.

Chapter 2 *Basic Concepts of Low-Noise Amplifier Design*

2.1 System Specifications of LNA

2.1.1 S-Parameters

Systems can be characterized in numerous ways. Usually, we use the well-known representations of impedance (Z), admittance (Y), hybrid (H), and cascade (ABCD) parameters matrix to characterize N-port network. However, in microwave design (or higher frequencies), it is quite difficult to obtain the parameters matrices mentioned above by providing short or open termination, since we can't measure the current at each port as it results in the reflected wave from short or open termination. For this reason, we must use Scattering Parameters, also called S-parameters, defined by the variables in terms of incident and reflected voltage waves with characteristic impedance, rather than port voltages or currents, to characterize the two-port network in LNA design [28]-[30].

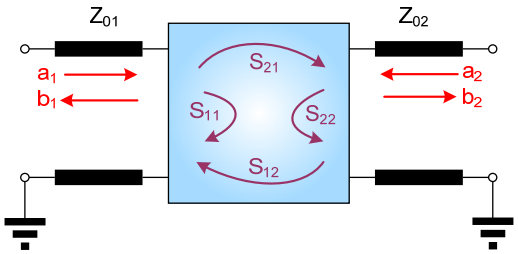


Figure 2.1 Two-port network with S-parameters.

Consider the two-port network for LNA shown in Figure 2.1, where Z_{0i} is the characteristic impedance of the port I, and V_i^+ and V_i^- represent the incident and reflected voltage waves at port i respectively. In order to obtain physically meaningful power relations in terms of wave amplitudes, we must define a new set of wave amplitudes as

$$a_i = V_i^+ / \sqrt{Z_{0i}} \ , \tag{2.1}$$

$$b_i = V_i^- / \sqrt{Z_{0i}} \ , \tag{2.2}$$

where a_i and b_i represents the normalized incident and reflected voltage wave by characteristic impedance (Z_{0i}) at port i respectively.

Then, the two-port S-parameters are defined as

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \tag{2.3}$$

where

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{\text{Port 2 is terminated.}}, \tag{2.4}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{\text{Port 1 is terminated.}}, \tag{2.5}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{\text{Port 2 is terminated.}}, \tag{2.6}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{\text{Port 1 is terminated.}}. \tag{2.7}$$

Thus, S_{11} and S_{22} are simply the input and output reflection coefficient respectively while we terminated another, and S_{12} and S_{12} is simply the forward gain and reverse isolation respectively.

.

2.1.2 Noise Figure (NF)

A useful representation of the noise effect of a system is the noise figure, usually denoted *F* or *NF*. The noise figure is a measure of the degradation in signal-to-noise ratio (SNR) that a system introduces. The noise factor is defined as

$$F \equiv \frac{SNR_{in}}{SNR_{out}} = \frac{\text{total output noise power}}{\text{output noise power due to input source}}\ , \tag{2.8}$$

and we usually represent the noise figure with logarithm defined as

$$NF(\text{dB}) = 10\log F. \tag{2.9}$$

The method for analyzing the effect of noise in MOSFET and the calculation of noise figure are illustrated in reference [28].

Figure 2.2 Cascade of system block diagram.

The overall noise figure of a cascade of systems depends on both the individual noise figures as well as their gains. The dependency on the gain results from the fact that, once the signal has been amplified, the noise of subsequent stages is less important. As a result, system noise figure tends to be dominated by the noise performance of the first several stages in a receiver. Consider the block diagram of Figure 2.2, where each F_n is the noise figure and each G_n is the gain. The total noise factor is the sum of these individual contributions, and is therefore given by

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{\prod_{n=1}^{N-1} G_n}. \tag{2.10}$$

2.1.3 Harmonics

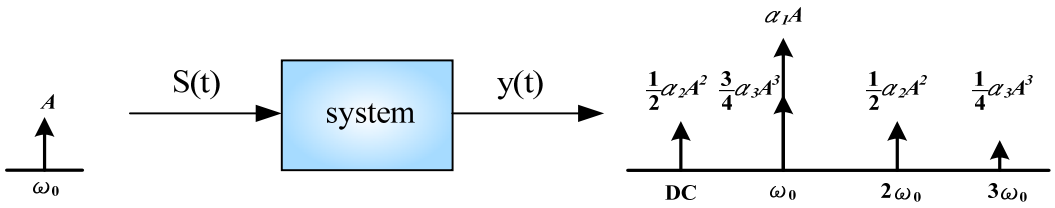


Figure 2.3 Frequency response of nonlinear system with one tone signal.

In wireless receiver, the low-noise amplifier usually can be approximately treated as linear system for processing small signal. In fact, it is nonlinear and the input-output relationship of a nonlinear system can be described by

$$y(t) = \alpha_1 S(t) + \alpha_2 S(t)^2 + \alpha_3 S(t)^3 + \cdots, \tag{2.11}$$

Here, as shown in Figure 2.3, S(t) is the input signal, and y(t) is the output signal. Using the function (2.11) with one tone signal at the input, $S(t) = A\cos\omega_0 t$, the output of the nonlinear system can be viewed mathematically as

$$y(t) = \alpha_1 A\cos\omega_0 t + \alpha_2 (A\cos\omega_0 t)^2 + \alpha_3 (A\cos\omega_0 t)^3 + \cdots$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega_0 t + \frac{\alpha_2 A^2}{2}\cos 2\omega_0 t + \frac{\alpha_3 A^3}{4}\cos 3\omega_0 t + \cdots \ . \tag{2.12}$$

As can be seen easily from (2.12), harmonic distortion is generated and is defined as the ratio of the amplitude of a particular harmonic to that of the fundamental. For example, third-order harmonic distortion (HD_3) is defined as the ratio of amplitude of the tone at $3\omega_0$ to that of the fundamental at ω_0, and is therefore given by

$$HD_3 = \frac{1}{4}\frac{\alpha_3}{\alpha_1}A^2. \tag{2.13}$$

2.1.4 1-dB Gain Compression Point (P1dB)

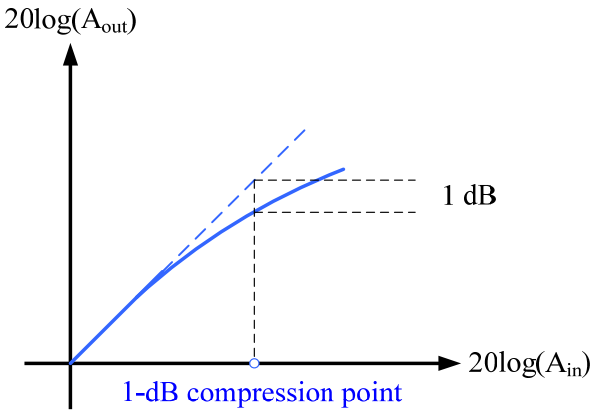


Figure 2.4 Definition of 1-dB compression point.

As can be seen easily from (2.12), for an amplifier, the output amplitude of the fundamental will not be given with a linear gain (α_1) when the input signal amplitude is large. We rewrite only the term of the fundamental as follows

$$y(t) = \left(\alpha_1 A + \frac{3}{4}\alpha_3 A^3\right)\cos\omega_0 t = \left(\alpha_1 + \frac{3}{4}\alpha_3 A^2\right) A\cos\omega_0 t. \tag{2.14}$$

At this point, from (2.14), α_3 is usually negative, and the gain will be compressed while the input signal amplitude exceeds some value. In RF circuits, this effect is quantified by the "1-dB compression point," defined as the input signal level that causes the linear small-signal gain to drop by 1 dB. It is depicted graphically in Figure 2.4. To calculate the 1-dB compression point, we can write from (2.14)

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{1\text{-}dB}^2\right| = 20\log|\alpha_1| - 1\text{dB}. \tag{2.15}$$

That is,

$$A_{1\text{-}dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.16}$$

2.1.5 Inter-Modulation

As more than one tone is applied to a nonlinear system, Inter-modulation (IM) arises. Assume that there are two strong interferers occurred at the input of the receiver, specified by $S(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$. The IM distortion can be expressed mathematically by applying $S(t)$ to (2.11)

$$y(t) = \alpha_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) + \alpha_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 + \alpha_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 + \cdots \quad (2.17)$$

Using trigonometric manipulations, we can find expressions for the second and the third-order IM products as follows

$$\omega_1 \pm \omega_2 : \alpha_2 A_1 A_2\cos(\omega_1 + \omega_2)t + \alpha_2 A_1 A_2\cos(\omega_1 - \omega_2)t \ , \quad (2.18)$$

$$2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 - \omega_2)t \ , \quad (2.19)$$

$$2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^2 A_1}{4}\cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^2 A_1}{4}\cos(2\omega_2 - \omega_1)t \ . \quad (2.20)$$

The output spectrum in frequency domain can be determined from (2.18)-(2.20) by evaluating its Fourier transform. In a typical two-tone test, $A_1 = A_2 = A$, there are two third-order IM products at $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ respectively, and then the output signal will be corrupted by one of the two, illustrated in Figure 2.5.

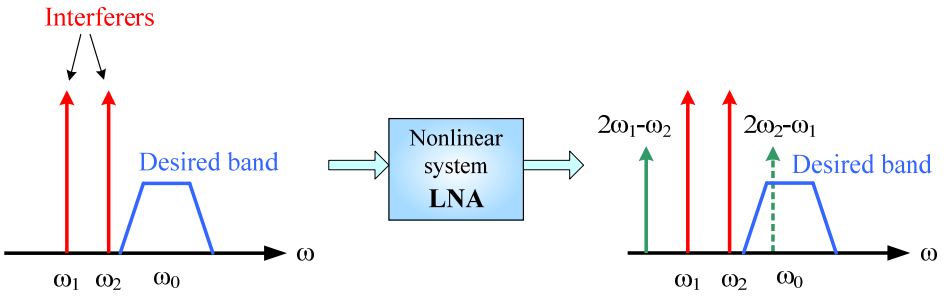


Figure 2.5 Inter-modulation in LNA (nonlinear system).

2.1.6 Third-Order Intercept Point (IP3)

The corruption of signals due to third-order IM of two nearby interferes is so common and so critical that a performance has been defined to characterize this behavior. Called the "third intercept point" (IP3), this parameter is measured by a two-tone test in which the input amplitude (A) is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant and equal to α_1. From (2.19) and (2.20), we note that as A increases, the fundamentals increase in proportion to A, whereas the third-order IM products increase in proportion to A^3. Plotted on a logarithmic scale in Figure 2.6, the third-order intercept point IP3 is defined to be the intersection of the two dotted lines elongated from linear region. Therefore, we can see that the amplitude of the input interferer at the third-order intercept point, A_{IP3}, is defined by the relation

$$20\log(\alpha_1 A_{IP3}) = 20\log\left(\frac{3}{4}\alpha_3 A_{IP3}^3\right). \tag{2.21}$$

From (2.21), we can solve for A_{IP3}:

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.22}$$

For 50-Ω systems, we define the input third-order intercept point (IIP3) as $\mathrm{IIP3} = \frac{1}{2}A_{\mathrm{IIP3}}^2/50$. (IIP3 is hence interpreted as the power level of the input interferer at the third-order intercept point).

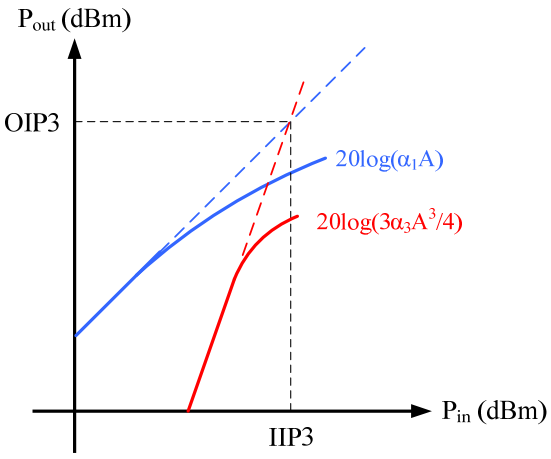
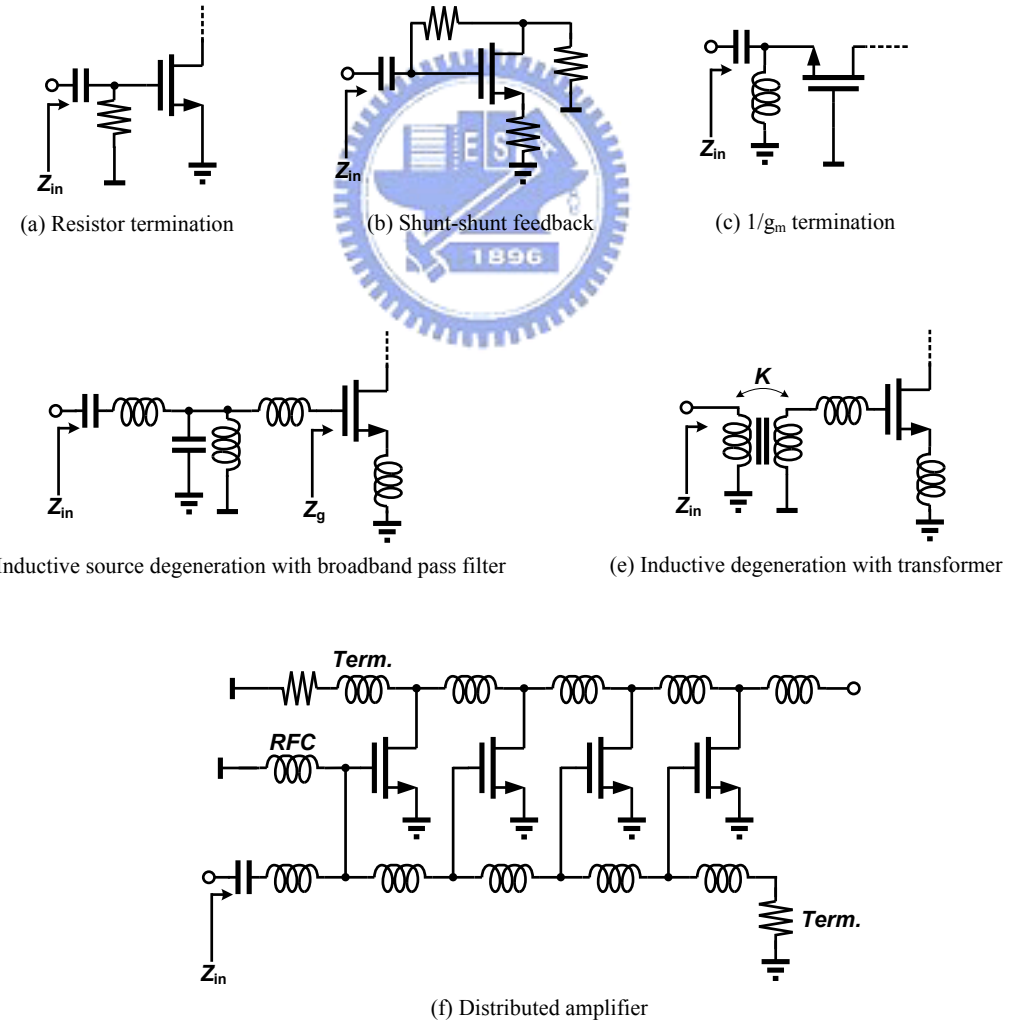


Figure 2.6 The input and output third order intercept point (IIP3 and OIP3).

2.2 Conventional Wideband Input Impedance Matching Architecture

In wireless receivers, low-noise amplifier is the first stage in the front-end RF circuits and is used to amplify the received weak signal with low noise figure and good input impedance match. However, a tradeoff among the input impedance match, die area, power consumption and noise figure of LNA should be carefully studied. There are several 50-Ohm input-matching architectures that have been explored in the conventional wideband CMOS LNA shown in Figure 2.7. In this section, we will introduce these architectures which can be achieved wideband input impedance match.



(a) Resistor termination

(b) Shunt-shunt feedback

(c) $1/g_m$ termination

(d) Inductive source degeneration with broadband pass filter

(e) Inductive degeneration with transformer

(f) Distributed amplifier

Figure 2.7 Conventional wideband input matching architectures of CMOS LNA.

2.2.1 Resistor Termination Architecture

Resistive termination architecture is the most straightforward approach to achieve the wideband 50-Ohm match at the input shown in Figure 2.8. The resistor R equal to R_S (=50 Ohm) is placed across the input terminal of the LNA to provide the wideband impedance match.

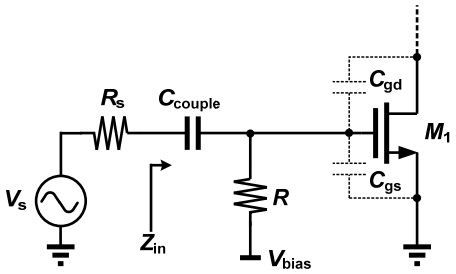


Figure2.8 Resistor termination architecture.

Usually, the input-matching bandwidth of this approach determined by the input capacitance of the transistor M_1 is very broad, due to the pole associated with the input at very high frequency. Unfortunately, the resistor R placed at the input not only adds thermal noise but also attenuates signal (by a factor of 2) ahead of the transistor. Consequently, the combination of these two effects generally produces unacceptably high noise figure. More formally, it is straightforward to establish the following lower bound on the noise figure of this circuit (neglecting gate current noise):

$$F \geq \frac{4KT/R_S+4KT/R+(4KT\mathrm{g}_{d0}/\mathrm{g}_m^2)/(R/2)^2}{4KT/R_S} = 2+\frac{4\gamma}{\alpha}\cdot\frac{1}{\mathrm{g}_m R}\ , \tag{2.23}$$

where $R_S = R$, $\alpha = g_m/g_{d0}$, g_{d0} is the drain-source conductance at zero V_{DS}, and γ is the channel thermal noise coefficient. Therefore, it seems that there is a tradeoff between the performance of the input impedance match and the noise figure.

Due to the high noise figure, the resistor termination architecture is not practical in most wireless application even though the input-matching bandwidth is very broad.

2.2.2 Shunt-Series Resistor Feedback Architecture

The resistor feedback technique is used to achieve a good input-match shown in Figure 2.9, [5], [8]. This technique unlike resistor terminating, it does not attenuate the signal by a noisy resistor before reaching the input (gate) of transistor and hence the noise figure is expected to be better than that of the case of resistor termination.

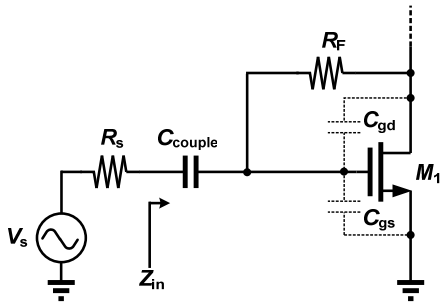


Figure 2.9 Shunt-series resistor feedback architecture.

However, not only the feedback resistor (R_F) continues to generate thermal noise of its own, but it also has no good input-output isolation. Furthermore, due to the negative-feedback, the gain will be sacrificed for bandwidth enhancement.

2.2.3 Common-Gate Architecture ($1/g_m$ Termination)

Using the common-gate configuration shown in Figure 2.9 can provide wideband input impedance match by designing $1/g_m$ that is equal to 50 Ohm, [6], [9], [10].

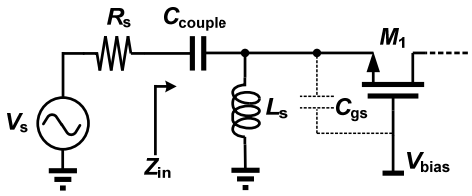


Figure 2.10 Common-gate architecture.

Similarly, the input-matching bandwidth of this approach is determined by the input capacitance of the transistor, but we can suppress the capacitive effect by means of parallel inductor L_S to enlarge wider input-matching bandwidth, and it provides the DC path for

transistor operating. The input impedance is given by

$$Z_{\text{in}} = \frac{1}{\text{g}_\text{m}} \parallel j\omega L \parallel \frac{1}{j\omega C_{gs}}. \tag{2.24}$$

The real part of the input impedance $1/g_m$ must be of 50 Ohm to provide the input match, and the g_m is limited to the value of 20m A/V^2. This value usually leads to lower gain than that of the other approaches and lightly high noise figure. However, common-gate architecture has the highest potential to achieve the wideband input impedance match, good linearity, and input-output isolation.

It is straightforward to establish the following lower bond on the noise figure of the common-gate amplifier (neglecting gate current noise):

$$F \geq \frac{4kTR_S + 4kT\gamma g_{do}/g_m^2}{4kTR_S} = 1 + \frac{\gamma}{\alpha}. \tag{2.25}$$

It is about 2.2dB for long-channel devices and perhaps as high as 4.8dB for short.

2.2.4 Inductive Source Degeneration with Broadband-Pass Filter

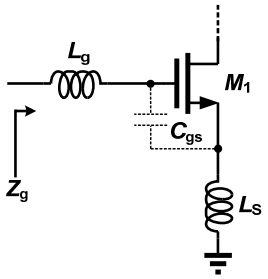


Figure 2.11 Inductive source degeneration architecture.

First, as shown in Figure 2.11, we must introduce the inductive source degeneration that can present a real input impedance to achieve input match without noisy resistor at only one frequency (at resonance) [28]. The input impedance is that of a series *RLC* network which has the following form,

$$Z_{\text{in}} = j\omega\left(L_{\text{g}+}L_{\text{s}}\right) + \frac{1}{j\omega C_{\text{gs}}} + \frac{\text{g}_m}{C_{\text{gs}}}L_{\text{s}}. \tag{2.26}$$

Consequently, the resistance is transformed from an inductor L_S, and it does not bring with the resistive thermal noise because a pure reactance is noiseless.

As a result, this architecture has the highest potential to achieve the narrow-band input impedance match with good noise performance. However, the inductor consumes more die area than would probably be consistent with an economical design.

At resonance, the gate-to-source voltage is Q times as large as the input voltage. The value of the quality factor Q is given by

$$Q = \frac{1}{\omega_0 C_{gs}(R_s+\omega_T L_s)}, \tag{2.27}$$

where ω_0 $(= 1/\sqrt{C_{gs}(L_g + L_s)})$ is the resonant frequency, and ω_T equals to g_m/C_{gs}. The overall stage trans-conductance G_m under this condition is therefore

$$G_m = g_{m1}Q = \frac{g_{m1}}{\omega_0 C_{gs}(R_s+\omega_T L_s)} = \frac{\omega_T}{2R_s\omega_0}. \tag{2.28}$$

In order to achieve wideband input impedance match, the ladder-*LC* filter is employed at the input of the amplifier shown in Figure 2.12 [4], [8]. For instance, there are some papers using Butterworth filter [11], Chebyshev filter or others. Therefore, this architecture can provide a wideband input impedance match without substantially adding thermal noise, but we must consider the issue of large die area almost consumed by numerous inductor.

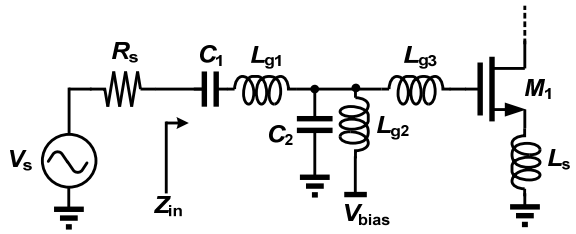


Figure 2.12 Inductive source degeneration with an input broadband-pass filter.

2.2.5 Inductive Source Degeneration with Transformer

To achieve the wideband input impedance match with low noise, the inductive source degeneration with broadband pass filter has been introduced already. However, due to this technique exploiting numerous inductors, the die area is always larger than that of other techniques. For this reason, the inductive source degeneration with transformer (or called the mutual inductor) architecture is developed to reduce die area for the wideband input impedance match shown in Figure 2.13.

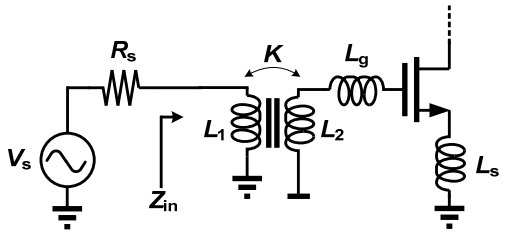


Figure 2.13 Inductive source degeneration with a transformer.

From Figure 2.13, the ideal coupling factor K is equal to constant unity, but this factor is dependent on frequency and smaller than unity actually. Then, K will be a function of frequency, and the input impedance may possibly have more than one resonant frequency to achieve the wideband input impedance match.

However, although this technique can save the die area efficiently, the implementation and modeling of mutual inductor (two coupling inductors) is so complicated due to effects of the parasitic capacitance between the one inductor and the other. Several examples of Layout of mutual inductor is shown in Figure 2.14.

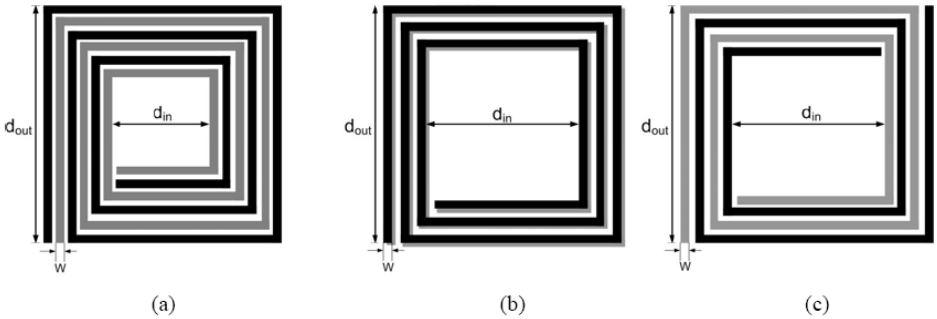


Figure 2.14 Layout of various mutual inductors. (a) Parallel (Shibata) configuration. (b) Overlay (Finlay) configuration. (c) Inter wound (Frlan) configuration.

2.2.6 Distributed Amplifier

Another architecture which can achieve very broadband input impedance match is the distributed amplifier shown in Figure 2.15. This technique, exploiting several inductors with the input capacitance of MOSFET forms equivalently a transmission-line model whose characteristic impedance is of 50Ω, and it is terminated by a 50-Ω resistor.

Although the architecture can achieve very broadband input impedance match, the numerous stages cause much power consumption. Consequently, this architecture is usually not practical for wireless portable devices.

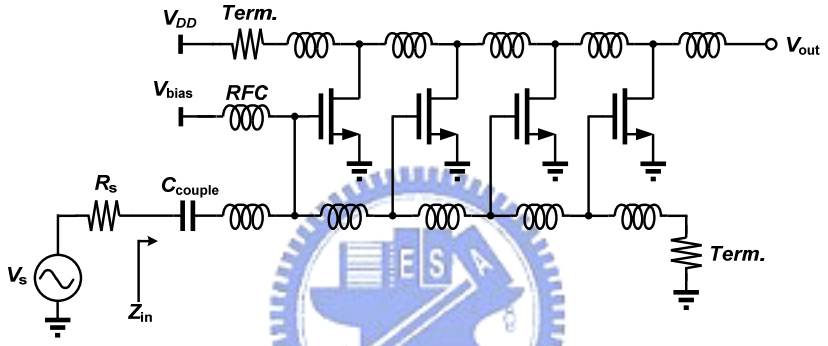
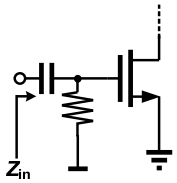


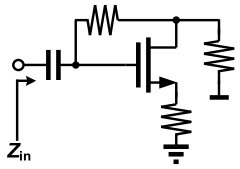
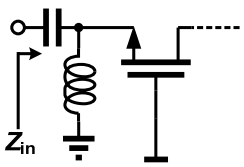
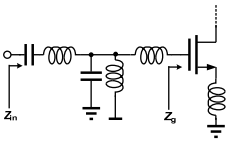
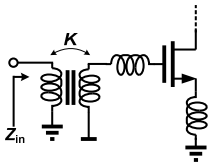
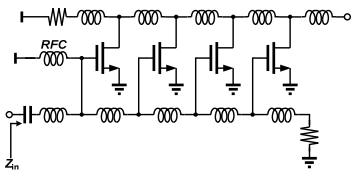
Figure 2.15 Distributed amplifier.

2.2.7 Comparison of Wideband Input Matching Architectures

The comparison of wideband input-matching architectures is shown in Table 2.1.

Table 2.1 Comparison of wideband input matching architectures

Input-matching architecture	Advantage	Drawback
 (a) Resistor termination	◆ Wideband input impedance match.	◆ High thermal noise.

 (b) Shunt-shunt feedback	◆ Wideband input impedance match. ◆ Wideband frequency response.	◆ High power dissipation. ◆ Poor reverse isolation. ◆ Feedback resistor gives rise to thermal noise.
 (c) $1/g_m$ termination	◆ Wideband input impedance match. ◆ Good linearity. ◆ Good reverse isolation. ◆ No Miller effect.	◆ Lower power gain. ◆ Higher noise figure.
 (d) Inductive source degeneration with broadband pass filter	◆ Wideband input-impedance match. ◆ Low noise figure. ◆ Good power gain.	◆ Large area.
 (e) Inductive degeneration with transformer	◆ Low noise figure. ◆ Good power gain.	◆ Hard to design. ◆ Complicated design.
 (f) Distributed amplifier	◆ The best wideband input-matching. ◆ Good frequency response.	◆ Large area ◆ High power consumption

2.3 Methods to Reduce Noise Figure of LNA

In order to obtain acceptable signal-to-noise ratio (SNR), noise figure should be performed as lower as possible in LNA design. There are several methods to reduce noise figure.

2.3.1 Gate-Drain Overlap Capacitance Neutralization Method

The negative feedback from the gate-drain overlap capacitance (C_{gd}) cannot be ignored in the high frequency, which leads to degradation of input impedance match, noise figure and gain. This feedback effect (called Miller effect) can be reduced using an inductor that mitigates the reactance of the parasitic capacitance C_{gd}.

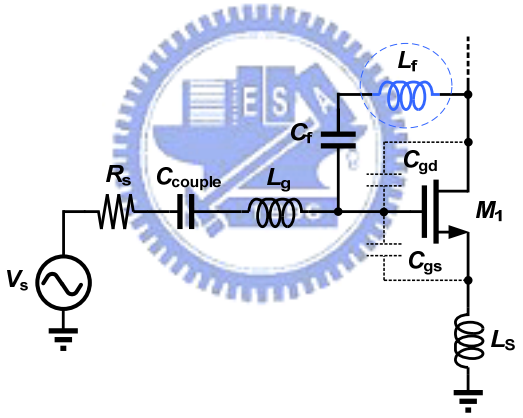


Figure 2.16 Gate-drain overlap capacitance neutralization.

2.3.2 Miller Effect Mitigation by Using Cascode Configuration

Although using the inductor can cancel the effect of the parasitic capacitance C_{gd}, it may not be necessary and suitable for on-chip implementations. That another technique can mitigate miller effect is using cascade configuration shown in Figure 2.17.

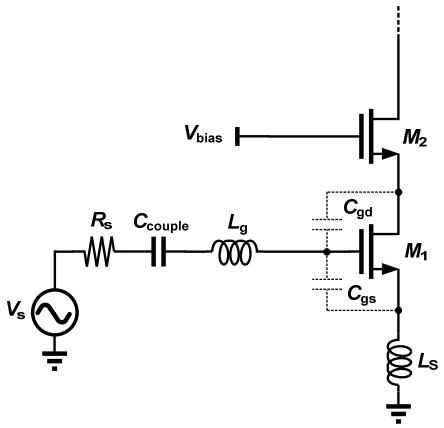


Figure 2.17 Miller effect mitigation by using cascode configuration.

2.3.3 Feed-Forward Thermal Noise Canceling Method

Figure 2.18 illustrates that cancel the channel thermal noise of M_1 with straightforward implementation using an ideal feed-forward voltage amplifier with a gain $-A_V$ $(A_V > 0)$ [13].

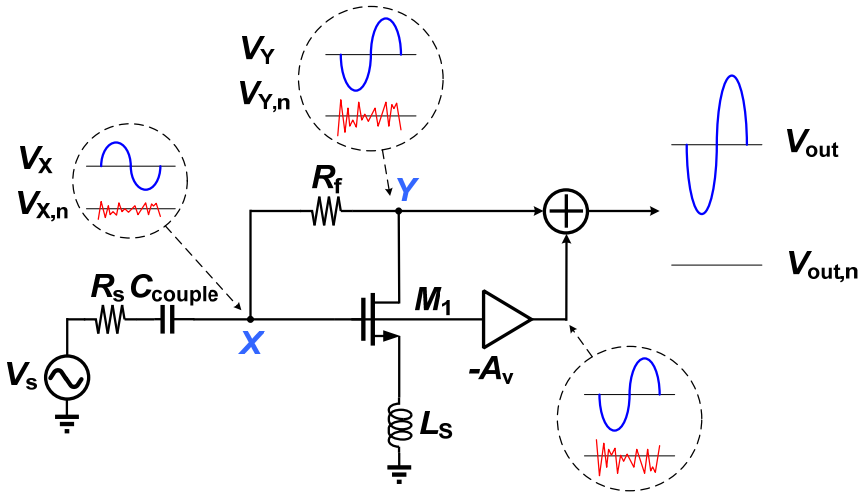


Figure 2.18 Feed-forward thermal noise canceling architecture

As can be seen from Figure 2.18, the input-matching device M_1 noise voltage at node X is in

terms of that of node Y

$$V_{\mathrm{X,n}} = V_{\mathrm{Y,n}} R_{\mathrm{S}}/(R_{\mathrm{S}} + R_{\mathrm{f}}). \tag{2.29}$$

The output noise voltage due to the noise of the matching device, $V_{out,n}$ is then equal to

$$\begin{aligned} V_{\mathrm{out,n}} &= V_{\mathrm{Y,n}} - V_{\mathrm{X,n}} A_V \\ &= V_{\mathrm{Y,n}}[1 - A_V R_{\mathrm{S}}/(R_{\mathrm{S}} + R_{\mathrm{f}})]. \end{aligned} \tag{2.30}$$

Thus, the output noise cancellation, $V_{out,n} = 0$, is achieved as the gain A_V equal to

$$A_V = 1 + R_{\mathrm{S}}/R_{\mathrm{f}}. \tag{2.31}$$

2.3.4 Input-Matching Device Thermal Noise Reduction Method by Using Mutual Inductor

Not only mutual inductor can achieve the wideband input match, but it also can provide reducing matching device thermal noise and peaking at the output. Due to the signal coupling feature of mutual inductor, we can exploit it with reverse-polarity coupling to cancel the input-matching device thermal noise, as illustrated in Figure 2.19 [15].

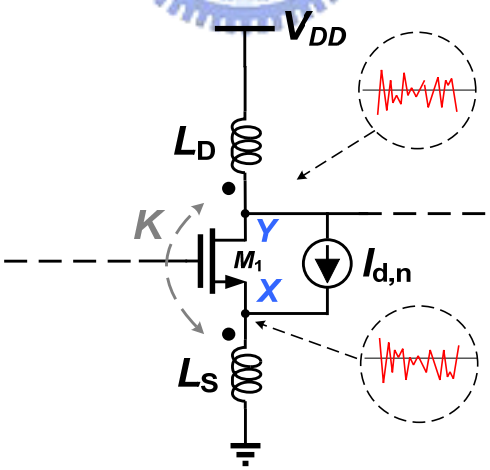


Figure 2.19 Thermal noise reduction using a mutual inductor

From Figure 2.19, the thermal noise voltage due to the input-matching device M_1 in magnitude at node X with self inductance is

$$V_{\mathrm{X,n}} = I_{\mathrm{d,n}} \frac{\omega L_S}{\sqrt{1+(\omega L_S g_{\mathrm{m}})^2}}, \tag{2.32}$$

and the thermal noise voltage in magnitude at node Y with self inductance is

$$V_{\mathrm{Y,n}} = -I_{\mathrm{d,n}}\omega L_D, \tag{2.33}$$

Thus, the output noise reduction is achieved

$$\begin{aligned} V_{\mathrm{out,n}} &= \alpha(K,N)V_{\mathrm{X,n}} + V_{\mathrm{Y,n}} \\ &= I_{\mathrm{d,n}}\left[\alpha(K,N)\frac{\omega L_S}{\sqrt{1+(\omega L_S \mathrm{g_m})^2}} - \omega L_D\right], \end{aligned} \tag{2.33}$$

where K is the coupling coefficient of the mutual inductor, and N is the turn ratio.

By proper design of parameters of L_S L_D and g_m, we can reduce the output thermal noise due to input-matching device M_1. Furthermore, input-matching purpose inductor L_S and output-peaking purpose L_D are fabricated together to form a mutual inductor, so it reduce the chip area efficiently. However, the implementation of mutual inductor is so complicated due to effects of the parasitic capacitance between the one inductor and the other.

2.3.5 Quality Factor (Q) of Inductor Enhancement Method

In order to achieve that gain and noise is not degraded by parasitic resistance of inductors at the input of LNA; we should require the high-Q inductor to improve the gain and noise figure shown in Figure 2.20.

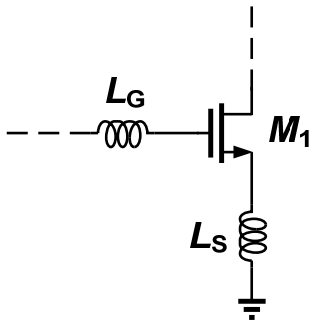


Figure 2.20 Inductive source degeneration architecture requires high-Q inductor.

A new implementation of high quality factor (Q) copper inductor on CMOS silicon substrate using a fully process is presented. The Q factor of such inductors depends on the

conductivity of metal layer and other parasitic components. Planner spirals can be of different shapes, i.e. square, hexagonal, octagonal and circular as shown in Figure 2.21.

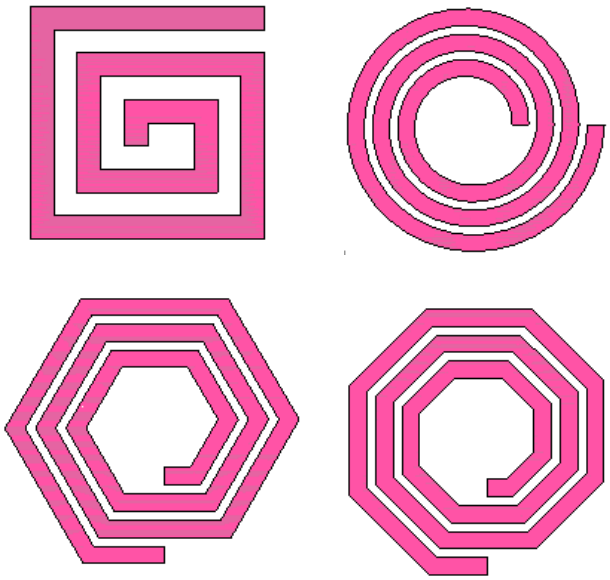


Figure 2.21 On-chip planner spiral inductors of different shapes

2.4 Considerations of LNA Design

In general, the following should be considered in LNA design:

a. Input- and Output-matching:

In wireless receiver, the component placed before LNA is usually the filter and antenna with characteristic impedance 50 Ω, so the input impedance of LNA must be matched to obtain high input/output return loss.

b. Low Noise Figure:

The noise figure of the entire receiver system is almost dominated by the first building block, LNA. Thus, noise figure of LNA is the most important parameter to evaluate the noise performance of the entire receiver system. And we should know that there is a tradeoff among the performance of the input match, noise figure and power consumption, etc.

c. Sufficient power gain and bandwidth:

The sufficient power gain of the LNA is also important, because not only it amplifies the receiver RF signal but it also compresses the noise contribution from the sequential stages. Thus, the design of LNA with an insufficient gain, the noise performance of the entire receiver system may not be excellent even if noise figure of LNA is small.

d. Low power consumption:

The power consumption is crucial to the designs of RF circuits, especially for portable device. Thus, no matter what RF circuits we design, the DC power should be consumed as lower as possible with acceptable performance.

Chapter 3 *Review of Low-Power LNA Designs*

3.1 Introduction

In LNA designs, that there are some low-power consumption techniques have been proposed, such as

a. Reduce or save supply current:

Current-reused technique,

Common-gate configuration with non-50-Ω input impedance technique,

Gain boost using mutual inductor technique.

b. Reduce supply voltage:

Forward body bias technique,

Dynamic-threshold voltage technique.

3.2 Current-Reused Technique

The current-reused LNA is composed of two common-source configuration stages under the common-current structure that can save the power consumption effectively, as shown in Figure 3.1. As can be seen from this Figure, in order to achieve the current-reused structure with two common-source configuration stages, we must exploit an inductor L_1 which is employed for passing the DC current and blocking the AC signal into the source of M_2, and then, we lead the signal to reach the gate of M_2 to achieve the second common-source configuration stage. Furthermore, not only does inductor L_1 block the signal into the source of M_2, but it also peaks the output of the first common-source configuration stage by cancelling the parasitic capacitance at the drain of M_1. And the bypass capacitor C_{ac} is used to avoid degrading the gain of the second common-source configuration stage due to the large impedance Z_x.

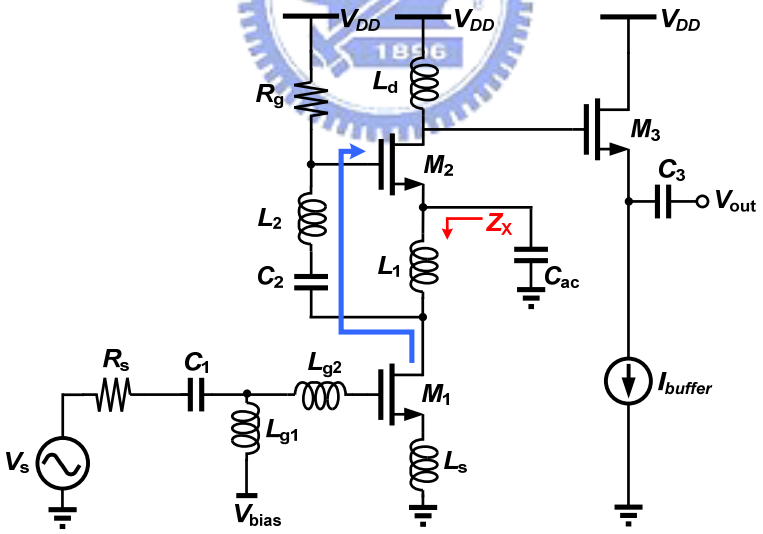


Figure 3.1 The current-reused LNA.

However, in order to achieve wideband input matching (L_{g1}, L_{g2} and L_S), signal blocking (L_1) and inductive peaking (L_d) network, we must use more than five inductors which result in large chip area.

3.3 Common-Gate Configuration with Non-50-Ω Input Impedance Technique

The common-gate architecture has the highest potential to achieve the wideband input impedance match. In the conventional common-gate LNA design, as shown in Figure 3.2(a), the resistance looking into the source terminal of M_1 is $1/g_m$, which should be equal to 50 Ω (g_m=20m A/V^2) to provide the wideband input impedance match.

At this point, we introduce an approach that can save half the power consumption of the conventional common-gate LNA. The low-power common-gate LNA is shown in Figure 3.2(b). In order to achieve low power consumption, we make the resistance looking into the source terminal of M_1, $1/g_m$, be equal to 70.7 Ω that can reduce half the current while $1/g_m$ is equal to 50 Ω, since we know that the $(1/g_m)^2$ is inversely proportional to the current I_d from the well-known relation given by

$$g_m = \sqrt{2\mu c_{ox}\frac{W}{L}I_d}. \tag{3.1}$$

Although we can reduce the power consumption by this method, it causes the input impedance mismatch with R_S (50 Ω). So the impedance must be transformed by incorporating the reactance component.

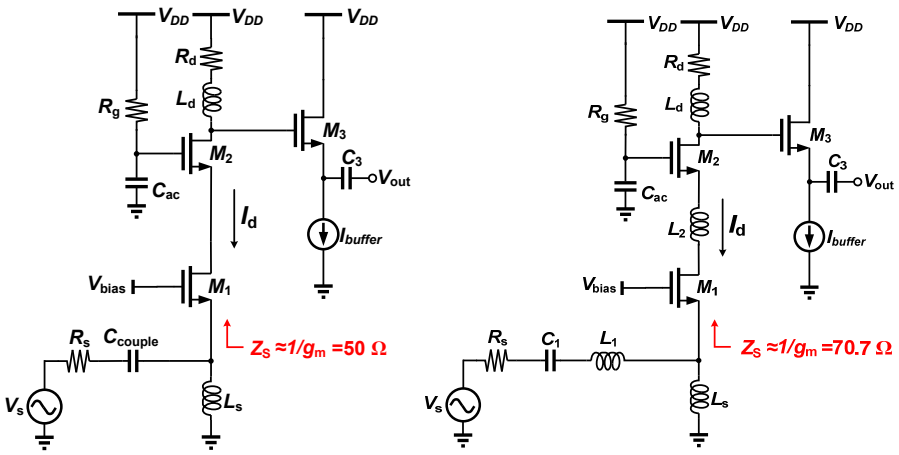


Figure 3.2 (a) Conventional, (b) Low-power, common-gate LNA

3.4 Gain Boost by Using Mutual Inductor Technique

In LNA design, we usually utilize the multistage architecture if the gain is inadequate to amplify the weak received signal. However, the multistage architecture will consume much DC power that is not suitable for the low-power applications.

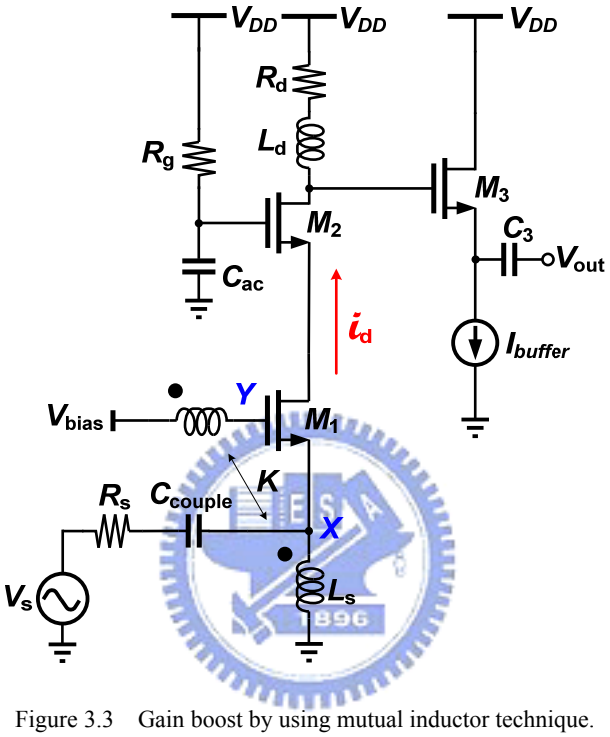


Figure 3.3 Gain boost by using mutual inductor technique.

For this reason, a gain boost approach that can increase the gain without any power consumption has been proposed by utilizing a mutual inductor, as shown in Figure 3.3. The mutual inductor is used to increase the gate-source small-signal voltage that converts high small-signal current to obtain the high gain. From Figure 3.3, assumed that mutual inductor is ideal, K=1, we can obtain v_Y=–v_X, thus v_{gs}=–2 v_X. It doubles the gate-source small-signal voltage compared with Figure 3.2 (a), and then the drain small-signal current would be double too. Therefore, it increases the gain without trans-conductor enhancement that may consume more power.

3.5 Forward Body Bias Technique

Most performances of LNA which include the gain, noise figure and I/O impedance matching, etc., are dependent on bias current. The higher gain and low noise figure we achieve, the larger current we require. For this reason, reducing the current to achieve low power consumption is not the best method.

In recent years, an approach that can achieve low power consumption by reduced supply voltage has been proposed [x], called the forward body bias (FBB). While a forward voltage biases the P-N junction between the bulk (or called the body) and source terminal of MOSFET, the P-N junction depletion region can be reduced, and then the minor carrier charge in the substrate can be attracted to create the channel under the lower gate-source and drain-source voltage than that of MOSFET without FBB.

We use the theoretical formula to explain why gate-source and drain-source voltage can be reduced maintaining the same current with FBB technique. The well-known threshold voltage formula is given by

$$V_t = V_{t0} + \gamma\left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}\right), \tag{3.2}$$

where V_{t0} is the threshold voltage at zero bulk-source voltage, ϕ_F the Fermi level deep in the bulk, and γ denotes the body effect coefficient. From (3.2), biasing the bulk-source P-N junction forwardly to reduce the P-N junction depletion region means that the threshold voltage can be reduced. Since the threshold voltage is reduced by using FBB, the gate-source and drain-source voltage can be lowered with the constant current, as known from the MOSFETs current equation

$$I_{\mathrm{d}} = \frac{1}{2}\mu_{\mathrm{n}}C_{\mathrm{ox}}\frac{w}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS}). \tag{3.3}$$

3.6 Dynamic-Threshold Voltage Technique

Although the FBB technique can reduce supply voltage to achieve low-power consumption, the voltage biased the bulk-source terminal requires an additional bias circuit (or called the voltage reference circuit) to supply it. The additional bias circuit consumes the DC power as well, so the FBB technique may not actually achieve low-power consumption. Therefore, the dynamic-threshold voltage approach that improves the FBB technique has been proposed. Since the gate-source bias voltage is always required to let MOSFET work as an amplifier, the bulk terminal can directly connect with the gate terminal to obtain bulk-source voltage that saves an additional bias circuit, as shown in Figure 3.4.

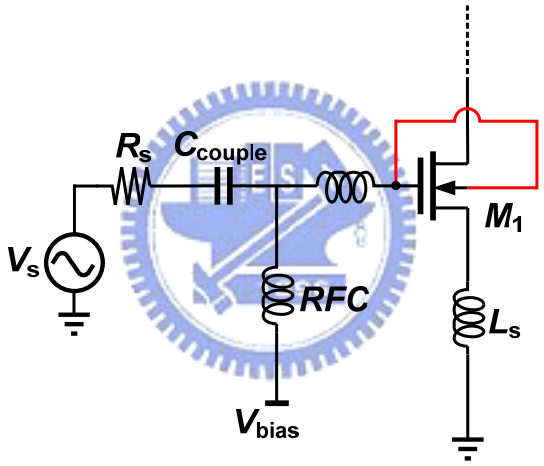


Figure 3.4 Low-power design with the dynamic-threshold voltage technique.

However, it has a troublesome issue with noise while using the dynamic-threshold voltage technique. Because, at the gate terminal in the first stage, the received weak signal has not amplified yet, the considerable thermal noise in the substrate will significantly degrade the noise figure if the bulk and gate terminal connect together in the first stage of LNA. Therefore, we proposed the self forward body bias technique in the next chapter that need not employ an additional bias circuit and doesn't degrade the noise figure significantly.

3.7 Comparison of Low-Power consumption Techniques

The comparison of low-power consumption technique is shown in Table 3.1.

Table 3.1 Comparison of low-power consumption techniques.

Low-power technique	Advantage	Drawback
Current-reused	◆ High gain. ◆ Low noise.	◆ Large area. ◆ Hardly design. ◆ Poor linearity.
Common-gate configuration with non-50-Ω input impedance	◆ Good linearity. ◆ Wideband input impedance matching.	◆ Low gain ◆ Noise figure degradation.
Gain boost using mutual inductor	◆ High gain. ◆ Wideband input impedance matching. ◆ Low noise.	◆ Hardly implement an mutual inductor.
Forward Body Bias	◆ High gain ◆ Wideband input impedance matching.	◆ Require an additional bias circuit.
Dynamic-Threshold voltage	◆ High gain ◆ Wideband input impedance matching.	◆ Thermal noise in the substrate significantly degrades noise figure.

Chapter 4 *Design of Low-Power Self-Forward-Body-Bias UWB LNA*

4.1 Introduction

A low-power UWB LNA we proposed is achieved by using self-forward bulk-source bias. And the forward bulk-source voltage in our design is obtained by means of the proposed ultra-low power self-bias that we don't need an additional bias circuit to supply the bulk terminal of MOSFET. However, the self forward body bias technique will give rise to some noise figure degradation. Therefore, we proposed the second LNA (LNA 2) to improve the noise figure of the preceding LNA (LNA 1) in this chapter. The measurement result shows that the LNA 1 has a gain of 12.5–15.5 dB from 2.6 to 6.6 GHz with a good input/output matching S_{11}<-10 dB and S_{22}<-17 dB and average noise figure of 3 dB while consuming power of 6.3 mW from 1.06 V voltage supply. And the measurement result of the LNA 2 shows that it has a gain of 13.5–16.2 dB from 2.0 to 6.6 GHz with a good input/output matching S_{11}<-10 dB and S_{22}<-16 dB and average noise figure of 2.4 dB while consuming power of 4.5 mW from 1.06 V voltage supply.

4.2 The Proposed Low-Power UWB LNA

The proposed low-power CMOS LNA for 3–6.5 GHz is show in Figure 4.1. It consists of two stages and the output buffer. The first stage using the complementary architecture amplifies the received weak signal with wideband input impedance matching and low noise figure, and the second stage employs the cascode architecture to compensate the gain at high frequency band of interest 3–6.5 GHz.

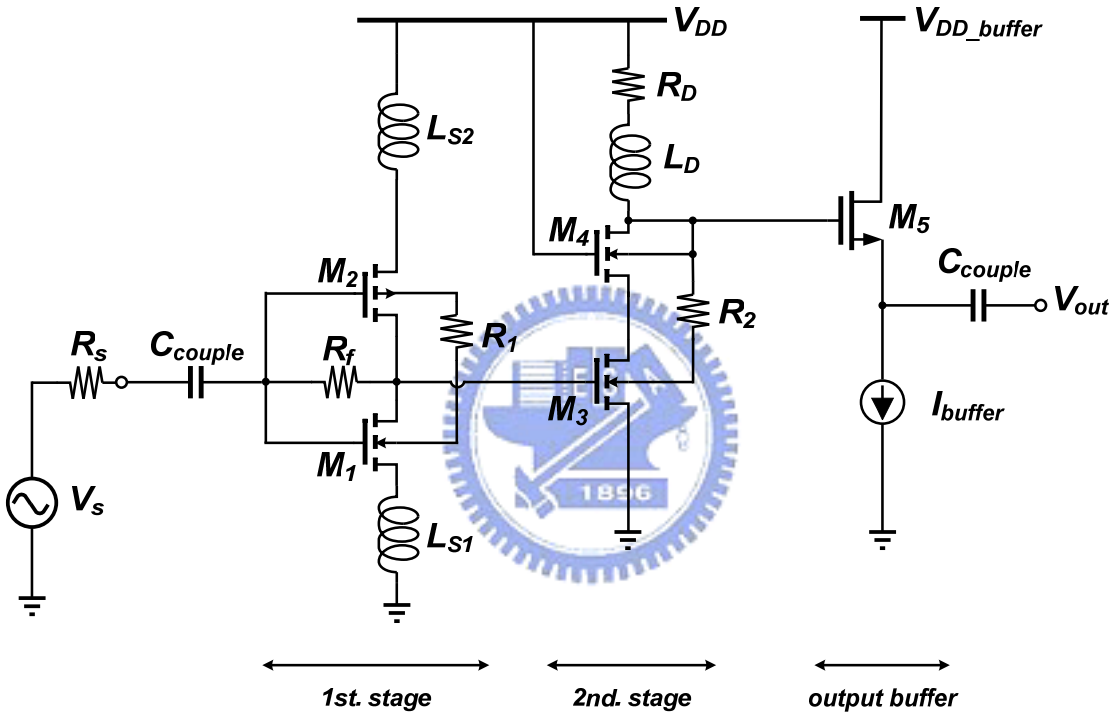


Figure 4.1 The proposed low-power SFBB UWB LNA.

The low-power technique in our LNA design is by means of self forward body bias (SFBB) which we first proposed. We will introduce and analysis the SFBB technique in this section.

4.2.1 Design of Input/Output Impedance Matching

In LNA design, the first stage has to provide impedance matching at the input. In order to achieve low noise and wideband impedance matching, we utilize a complementary architecture with two inductive source degenerations in parallel, as shown in Figure 4.2, and

the input small signal equivalent circuit is shown in Figure 4.3.

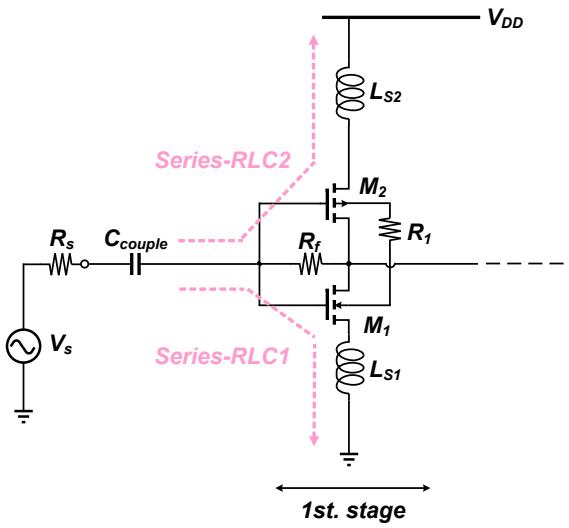


Figure 4.2 The first stage of the proposed low-power SFBB UWB LNA.

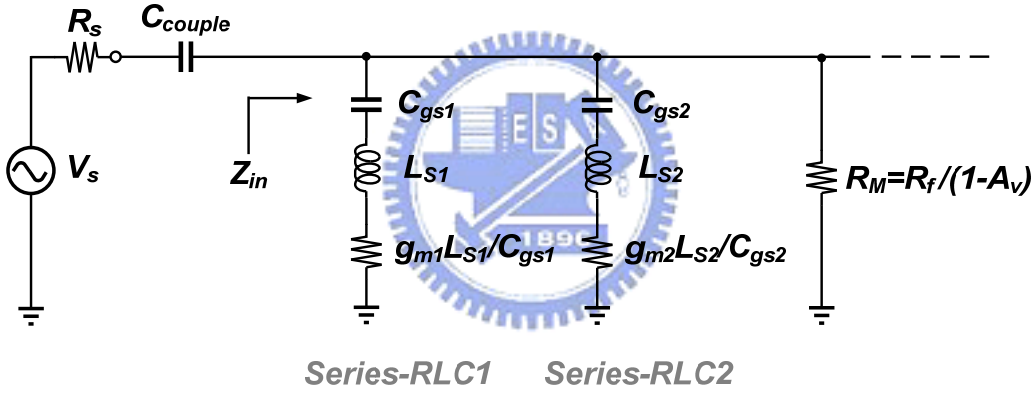


Figure 4.3 Equivalent circuit of the input impedance.

From Figure 4.3, that both the inductive source degenerations in parallel with different resonant frequencies design and with low Q factor can provide a wideband input matching in the first stage in our LNA design. Further, the resistance of the series-RLC1 and series-RLC2, $g_{m1}L_{S1}/C_{gs1}$ and $g_{m2}L_{S2}/C_{gs2}$, result from the transformation of the inductor and transistor. Therefore, both the resistances do not give rise to thermal noise, so the inductive source degeneration is a superior matching topology for low noise design. In addition to both the inductive source degenerations, there is a resistance, $R_M = R_f /(1-A_v)$ in across the input and ground due to Miller effect, which R_f is employed to supply gate-source self bias ,and A_v denotes the open loop gain in the first stage. Using this complementary architecture with two

inductive source degenerations and resistor feedback, the input impedance is

$$Z_{in} = \left(sL_{S1} + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_{S1}}{C_{gs1}}\right) || \left(sL_{S2} + \frac{1}{sC_{gs2}} + \frac{g_{m2}L_{S2}}{C_{gs2}}\right) || R_M \ ,$$

$$= \left[\frac{s^2L_{S1}L_{S2} + \frac{L_{S1}}{C_{gs2}} + \frac{sg_{m2}L_{S1}L_{S2}}{C_{gs2}} + \frac{L_{S2}}{C_{gs1}} + \frac{1}{s^2C_{gs1}C_{gs2}} + \frac{g_{m2}L_{S2}}{sC_{gs1}C_{gs2}} + \frac{sg_{m1}L_{S1}L_{S2}}{C_{gs1}} + \frac{g_{m1}L_{S1}}{sC_{gs1}C_{gs2}} + \frac{g_{m1}g_{m2}L_{S1}L_{S2}}{C_{gs1}C_{gs2}}}{s(L_{S1}+L_{S2}) + \frac{1}{s(C_{gs1}+C_{gs2})} + \frac{g_{m1}L_{S1}}{C_{gs1}} + \frac{g_{m2}L_{S2}}{C_{gs2}}}\right]$$

$$|| \ R_M \ ,$$

$$= \left[\frac{s^2L_{S1}L_{S2} + s\left(\frac{g_{m2}L_{S1}L_{S2}}{C_{gs2}} + \frac{g_{m1}L_{S1}L_{S2}}{C_{gs1}}\right) + \left(\frac{L_{S1}}{C_{gs2}} + \frac{L_{S2}}{C_{gs1}} + \frac{g_{m1}g_{m2}L_{S1}L_{S2}}{C_{gs1}C_{gs2}}\right) + \frac{1}{s}\left(\frac{g_{m2}L_{S2}}{C_{gs1}C_{gs2}} + + \frac{g_{m1}L_{S1}}{C_{gs1}C_{gs2}}\right) + \frac{1}{s^2}\left(\frac{1}{C_{gs1}C_{gs2}}\right)}{s(L_{S1}+L_{S2}) + \frac{1}{s(C_{gs1}+C_{gs2})} + \frac{g_{m1}L_{S1}}{C_{gs1}} + \frac{g_{m2}L_{S2}}{C_{gs2}}}\right]$$

$$|| \ R_M \ . \qquad (4.1)$$

Finally, the simulated and measured impedance matching response (S_{11}) of the first stage in our LNA design is depicted in Figure 4.4.

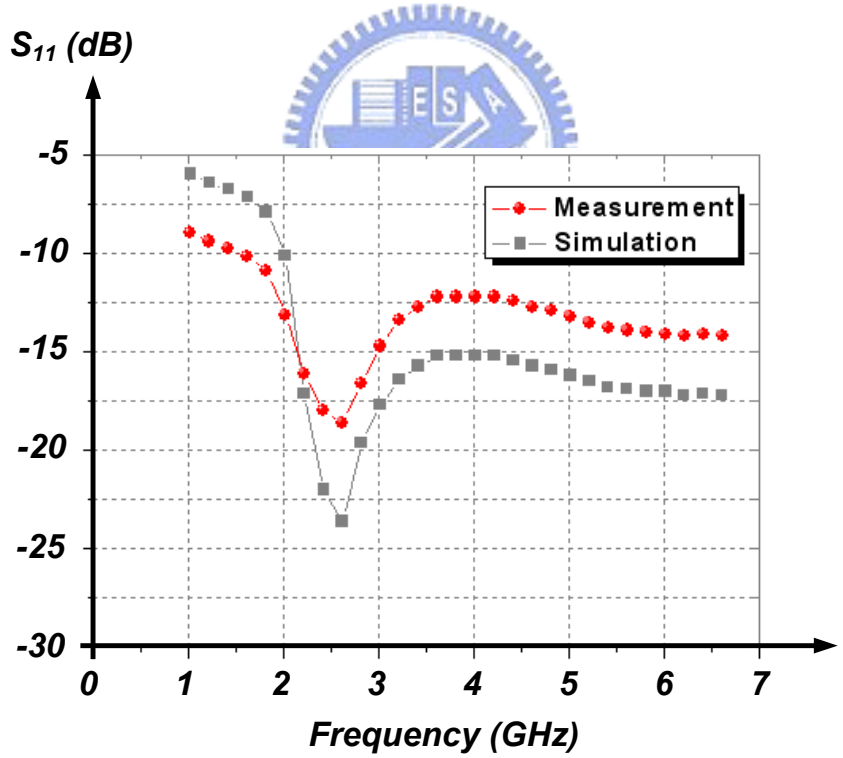


Figure 4.4 Simulated and measured input impedance matching (S_{11}).

4.2.2 Gain Bandwidth Extension

Although the first stage using complementary with two inductive degenerations can provide the wideband input impedance matching with low noise, it cannot provide the sufficient high frequency gain. Therefore, we have to incorporate the second stage that employs the cascode architecture with the inductive peaking to compensate the gain of high frequency in the band of interest as well as increase the inverse isolation, as shown in Figure 4.5.

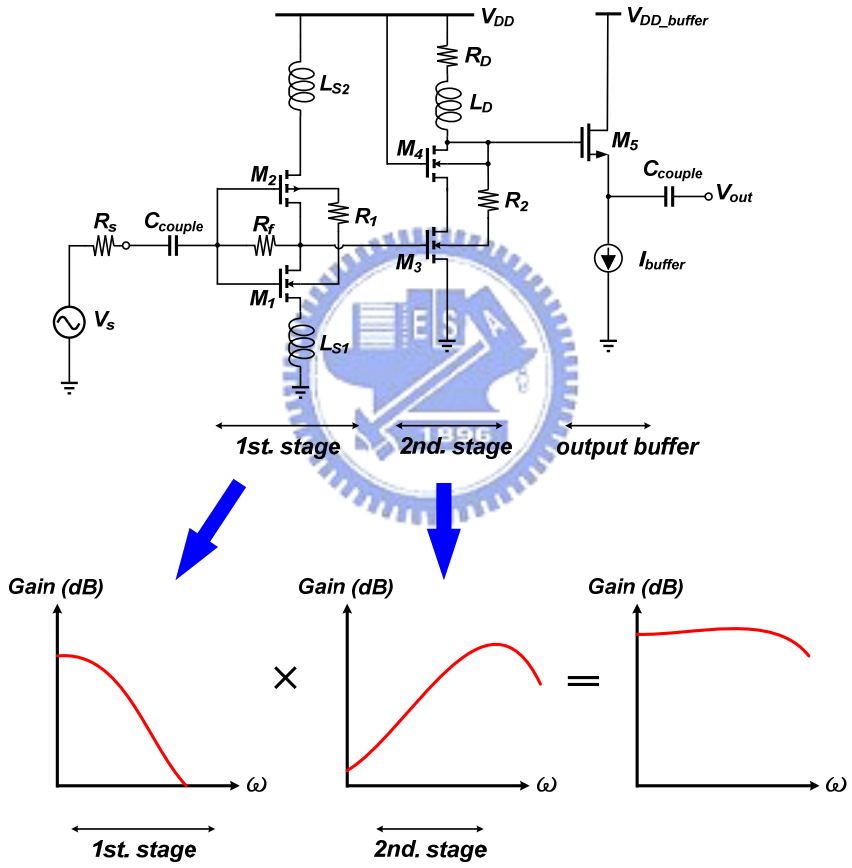


Figure 4.5 Frequency response of the proposed LNA.

The overall gain of the proposed LNA can be obtained by the product of the gain of the first and second stage. The gain of the first is

$$G_1 \approx \left[\frac{g_{m1}r_{o1}}{r_{o1}+R_{out1}+(1+g_{m1}r_{o1})sL_{S1}} + \frac{g_{m2}r_{o2}}{r_{o2}+R_{out1}+(1+g_{m2}r_{o2})sL_{S2}}\right] R_{out1}, \quad (4.2)$$

where

$$R_{\text{out1}} = R_F \| \frac{1}{j\omega\left(C_{gd1}+C_{db1}+C_{gd2}+C_{db2}\right)}, \tag{4.3}$$

and the gain of the second is

$$G_2 \approx -g_{m3}\left[(R_D + sL_D) \| \frac{1}{s(C_{gd5}+C_{gd4})}\right]. \tag{4.3}$$

4.2.3 Self Forward Body Bias (SFBB) Technique

The low-power technique in our LNA design is by means of self forward body bias (SFBB) which we first proposed. As can been from Figure 4.6, with a difference to conventional FBB technique [21], SFBB using an ultra-low power self bias approach improves the conventional FBB technique which needs additional bias circuit to supply the bulk terminal of MOSFET for obtaining a forward bulk-source bias.

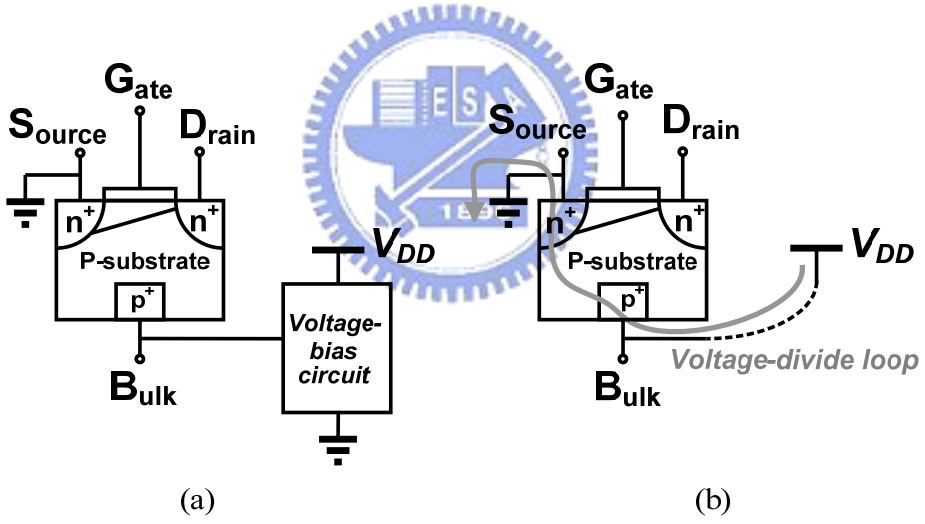


Figure 4.6 (a) Conventional FBB with additional bias circuit. (b) Self-FBB.

In the SFBB approach, as shown in Figure 4.6(b), we can achieve ultra-low power self-bias loop since the P-N junction (parasitic diode) between the bulk and source in the MOSFET is treated as a component in a voltage-divided loop, and only working within at its cut-off region, in which the P-N junction voltage is lower than the cut-in voltage $V_{cut,in}$ (typically about 0.5 V). The well-known P-N junction I-V characteristic equation is given by

$$I_{PN} = I_S\left(e^{\frac{V_{PN}}{\eta V_T}} - 1\right), \tag{4.4}$$

where η is the ideality factor, V_T is the thermal voltage, and I_S denotes the reverse-bias leakage current. Applying the cut-off region ($0 < V_{PN} < V_{cut,in}$), the current through the P-N junction is very small (about few μA) that leads a self-bias loop with ultra-low power consumption (about few μW).

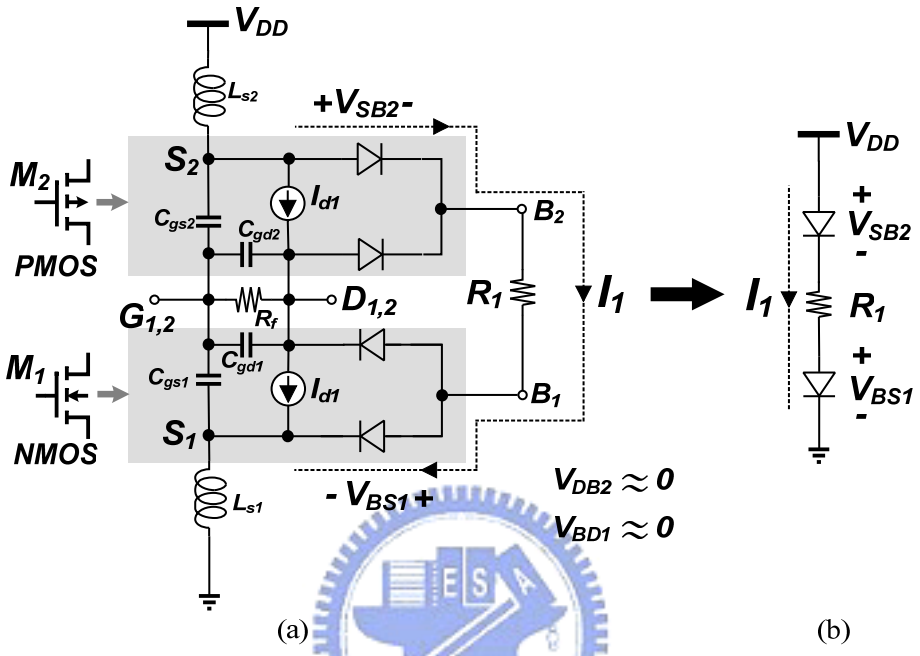


Figure 4.7 (a) The first stage with the MOSFET model. (b) Self-bias voltage-divided loop.

The ultra-low power self-bias loop employed in the two stages of the proposed LNA is analyzed and evaluated as follows. In Figure 4.7(a), the first stage using the complementary architecture that consists of an N-MOSFET and a P-MOSFET is shown. In order to provide the bulk-source P-N junction voltage (V_{BS1} and V_{SB2}) of both the transistors to form a voltage-divided loop with forward bias, a resistor R_1 is employed to connect the bulk terminal of M_1 and that of M_2. To be simple, the self-bias voltage-divided loop is individually shown in Figure 4.7(b). In the loop, R_1 is properly selected to yield the bulk-source P-N cut-off region, which can achieve ultra-low power self-bias loop. The formula of R_1 is derived as follows, which start with the voltage equation of the self-bias voltage-divided loop,

$$V_{DD} = V_{BS1} + V_{SB2} + I_1 R_1 \ . \tag{4.5}$$

According to (4.4), the loop current I_1 is expressed in terms of V_{BS1} or V_{SB2},

$$I_1 = I_{S1}\left(e^{\frac{V_{BS1}}{\eta V_T}} - 1\right), \tag{4.6}$$

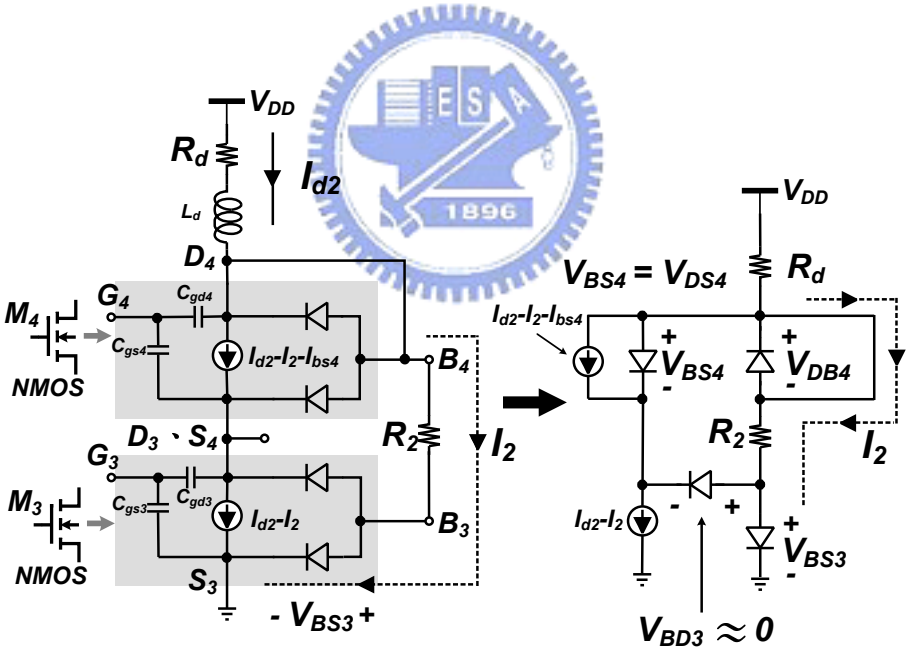
or $$I_1 = I_{S2}\left(e^{\frac{V_{SB2}}{\eta V_T}} - 1\right). \tag{4.7}$$

Here, I_{S1} and I_{S2} denote the reverse-biased leakage current of the bulk-source P-N junction of the N-MOSFET and P-MOSFET in the first stage respectively. Then, substituting (4.6) into (4.5), we obtain

$$V_{DD} = V_{BS1} + V_{SB2} + I_1 = I_{S1}\left(e^{\frac{V_{BS1}}{\eta V_T}} - 1\right)R_1, \tag{4.8}$$

thus,

$$R_1 = \frac{V_{DD} - V_{BS1} - V_{SB2}}{I_{S1}\left(e^{\frac{V_{BS1}}{\eta V_T}} - 1\right)}. \tag{4.9}$$



(a) (b)

Figure 4.8 (a) The second stage with the MOSFET model. (b) Self-bias voltage-divided loop.

The second stage uses the cascode architecture shown in Figure 4.8. Similarly, in order to form a self-bias loop, we exploit a resistor R_2 to connect between their bulk terminals. The principle and analysis method of the SFBB technique in the second stage is similar to that of the first stage, so we only show what the value of R_2 we need while the bulk-source P-N

junction voltage, V_{BS3}, is operating within cut-off region. And V_{BS4} is equal to V_{DS4} (about 0.45 V), so it also works within cut-off region.

$$R_2 = \frac{V_{DD} - I_{d2}R_d - V_{BS3}}{I_{S\_3}\left(e^{\frac{V_{BS3}}{\eta V_T}} - 1\right)}. \tag{4.10}$$

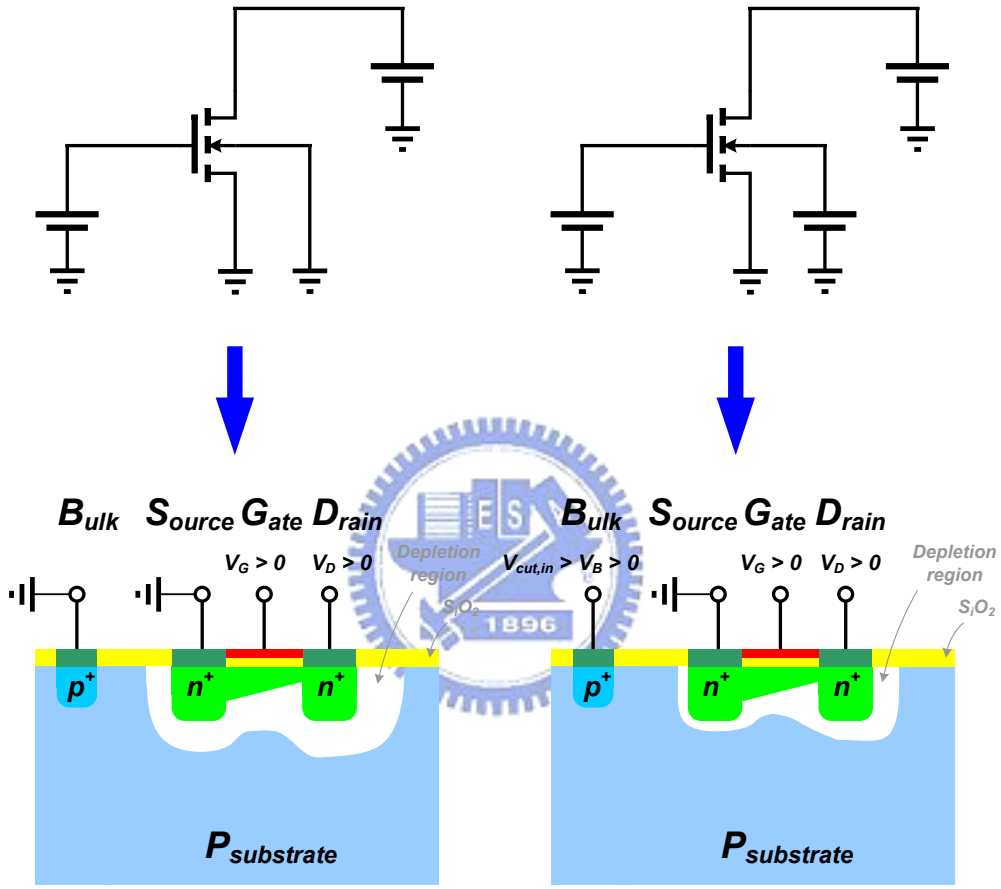


Figure 4.9 MOSFET (a) without forward body bias, (b) with forward body bias technique.

Finally, we have to explain why the threshold voltage and supply voltage can be lowered while we obtain the forward bulk-source bias. The N-MOSFET without and with forward body bias is shown in Figure 4.9(a) and Figure 4.9(b) respectively. As can be seen, if the P-N junction between the bulk and source terminal is biased by forward voltage, the depletion between N-channel and P-substrate will be narrower than that of without forward bias. Then, while the depletion is shrunk, the electron in the P-substrate is easier to be attracted than that

of N-MOSFET without forward bias under the same gate-source and drain-source voltage. Therefore, the threshold voltage V_t is reduced by means of forward bulk-source bias, and the formula of threshold voltage is given by

$$V_t = V_{t0} + \gamma\left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}\right), \tag{4.11}$$

where V_{t0} is the threshold voltage at zero bulk-source voltage, ϕ_F the Fermi level deep in the bulk, and γ denotes the body effect coefficient. And the gate-source and drain-source voltage can be lowered than that of N-MOSFET without forward bulk-source bias for the same current, as known from the MOSFETs current equation

$$I_{\mathrm{d}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{w}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS}). \tag{4.12}$$

And Figure 4.10 illustrates that the threshold voltage with forward bulk-source bias compares with that of zero bulk-source voltage by simulation. The threshold voltage V_{th1} of the MOSFET with V_{BS}=0 V is about 0.45 V; and that V_{th2} of the MOSFET with V_{BS}=0.45 V is about 0.35 V.

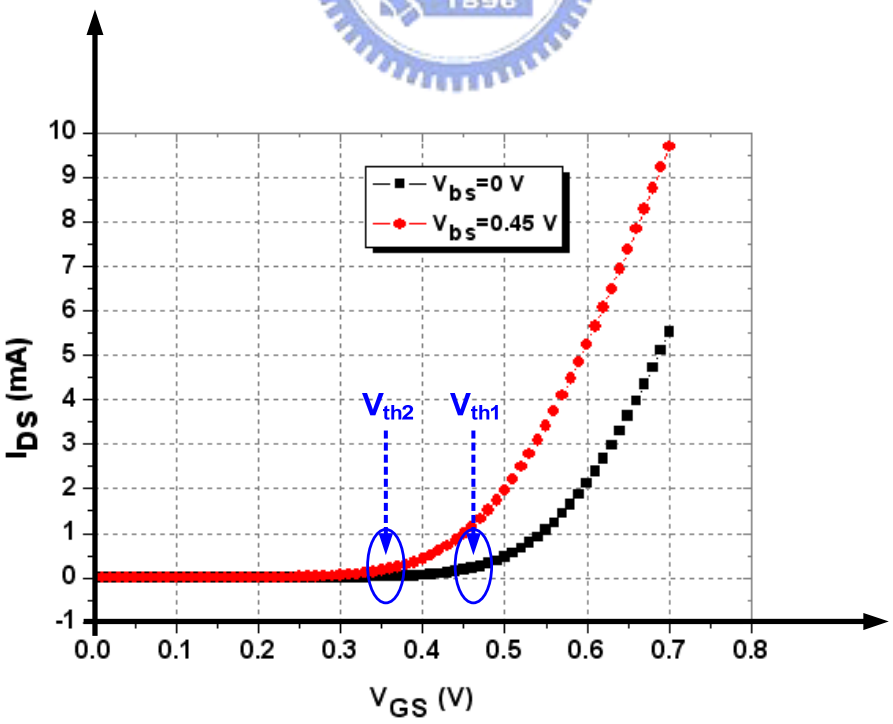


Figure 4.10 I-V curve of MOFSET for forward/zero bulk-source bias.

4.2.4 Noise Analysis of The Proposed LNA

Before analyze the noise figure of the proposed LNA (Figure 4.1), we have to draw the circuit with noise sources shown in Figure 4.11.

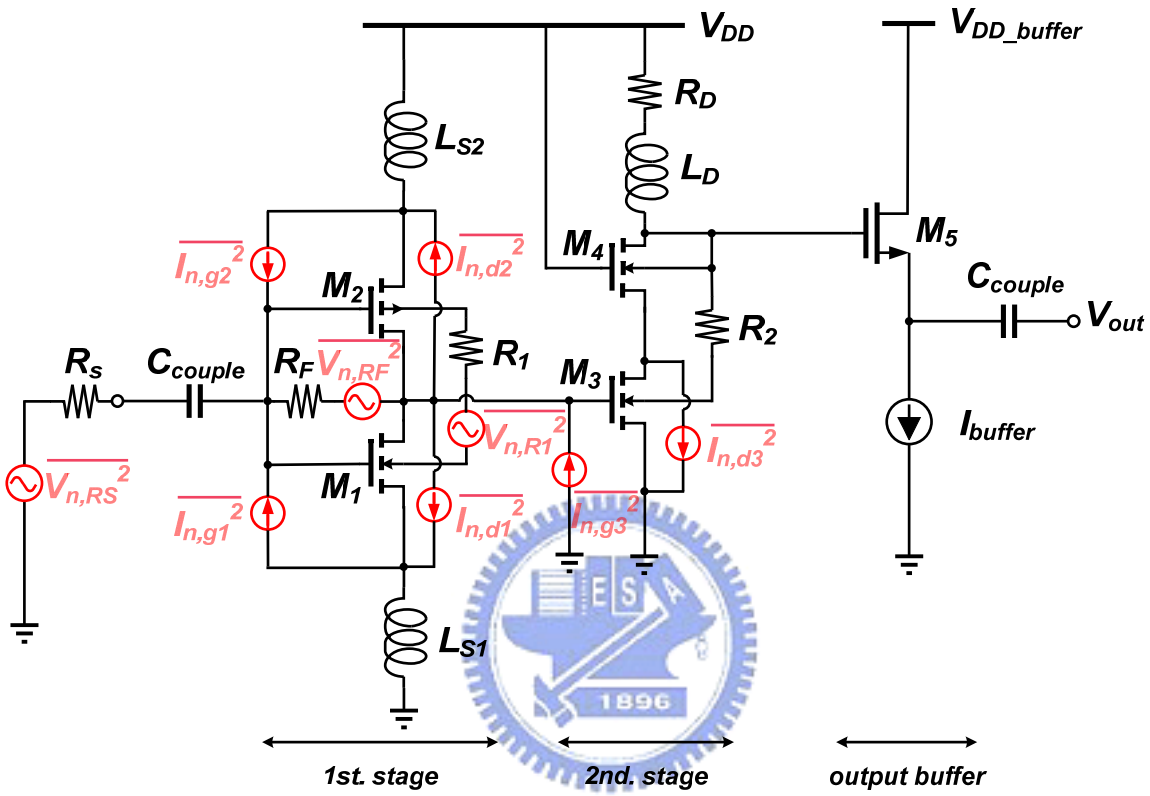


Figure 4.11 The proposed LNA with noise sources.

The noise factor is defined as:

$$F \equiv \frac{Total\ output\ noise}{Total\ output\ noise\ due\ to\ input\ source}. \tag{4.13}$$

As equation (4.12) shows that the noise factor equals to the ratio of total output noise and output noise due to source. The noise sources in the LNA contain the resistor thermal noise, channel thermal noise, induced gate noise (correlated and uncorrelated with channel thermal noise), gate resistive thermal noise and bulk thermal noise, etc. In order to simply estimate, we assume that the passive components are ideal without other parasitic effects. At the first, we start with the calculation of the output noise power spectrum density (PSD) due to the input source resistor R_S,

$$\overline{S_{n,R_s}{}^2} = 4kTR_s \left|\frac{Z_{in}}{Z_{in}+R_s}\right|^2 |G_1G_2|^2, \tag{4.14}$$

where Z_{in}, G_1 and G_2 are expressed in (4.1), (4.2) and (4.3) respectively. The noises PSD contributed by the part of the induced gate noise in M_1 and M_2 that are fully uncorrelated with the drain channel thermal noise:

$$\overline{S_{n,g,u,1}{}^2} = \frac{4kT\alpha\delta\omega^2 C_{gs1}^2}{5g_{m1}} \left|\left[\left(j\omega L_{S1}||\frac{1}{g_{m1}}\right)+(R_s||Z_{in2})\right]||\frac{1}{j\omega C_{gs1}}\right|^2 \left|g_{m1}R_{out1,2}\right|^2 |G_2|^2(1-|c|^2), \tag{4.15}$$

$$\overline{S_{n,g,u,2}{}^2} = \frac{4kT\alpha\delta\omega^2 C_{gs2}^2}{5g_{m2}} \left|\left[\left(j\omega L_{S2}||\frac{1}{g_{m2}}\right)+(R_s||Z_{in1})\right]||\frac{1}{j\omega C_{gs2}}\right|^2 \left|g_{m2}R_{out1,2}\right|^2 |G_2|^2(1-|c|^2), \tag{4.16}$$

where

$$Z_{in1} = sL_{S1} + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_{S1}}{C_{gs1}},$$

$$Z_{in2} = sL_{S2} + \frac{1}{sC_{gs2}} + \frac{g_{m2}L_{S2}}{C_{gs2}},$$

$$\alpha_1 = \frac{g_m}{g_{d0}},$$

$$c = \frac{\overline{I_{n,g}I_{n,d}{}^*}}{\sqrt{\overline{I_{n,g}{}^2}\,\overline{I_{n,d}{}^2}}},$$

$$R_{out1,2} = [r_{o1} + (1+g_{m1}r_{o1})j\omega L_{S1}]||[r_{o2} + (1+g_{m2}r_{o2})j\omega L_{S2}]||R_F||\frac{1}{j\omega C_{gs2}},$$

and δ and c are the induced gate noise coefficient and correlation coefficient. The output noise PSD due to correlated induced gate noise source and drain channel thermal noise source of M_1 and M_2:

$$\overline{s_{n,g,d,c,1}{}^2} = \left(\overline{s_{n,d,1}} + \overline{s_{n,g,c,1}}\right)^2$$

$$= \left(\overline{s_{n,d,1}{}^2} + \overline{s_{n,g,c,1}{}^2} + 2\overline{s_{n,d,1}}\,\overline{s_{n,g,c,1}}\right), \tag{4.17}$$

$$\overline{s_{n,g,d,c,2}{}^2} = \left(\overline{s_{n,d,2}} + \overline{s_{n,g,c,2}}\right)^2$$

$$= \left(\overline{s_{n,d,2}{}^2} + \overline{s_{n,g,c,2}{}^2} + 2\overline{s_{n,d,2}}\,\overline{s_{n,g,c,2}}\right), \tag{4.18}$$

where

$$\overline{s_{n,d,1}} = \sqrt{\frac{4kT\gamma g_{\mathrm{m1}}}{\alpha}}\left|R_{\mathrm{out1,2}}G_2\right|,$$

$$\overline{s_{n,g,c,1}} = -j|c|\sqrt{\frac{4kT\alpha\delta\omega^2C_{gs1}^2}{5g_{\mathrm{m1}}}}\left|\left[\left(j\omega L_{S1}||\frac{1}{g_{\mathrm{m1}}}\right)+(R_{\mathrm{s}}||Z_{in2})\right]||\frac{1}{j\omega C_{gs1}}\right|\left|g_{\mathrm{m1}}R_{\mathrm{out1,2}}||G_2\right|,$$

and

$$\overline{s_{n,d,2}} = \sqrt{\frac{4kT\gamma g_{\mathrm{m2}}}{\alpha}}\left|R_{\mathrm{out1,2}}G_2\right|,$$

$$\overline{s_{n,g,c,2}} = -j|c|\sqrt{\frac{4kT\alpha\delta\omega^2C_{gs1}^2}{5g_{\mathrm{m1}}}}\left|\left[\left(j\omega L_{S2}||\frac{1}{g_{\mathrm{m2}}}\right)+(R_{\mathrm{s}}||Z_{in1})\right]||\frac{1}{j\omega C_{gs2}}\right|\left|g_{\mathrm{m1}}R_{\mathrm{out1,2}}||G_2\right|.$$

Notice that, in (4.17) and (4.18), the power spectrum densities (PSDs), $\overline{s_{n,g,c,1}}^2$ and $\overline{s_{n,g,c,2}}^2$ should be absolutely positive. The output noise due to R_1, R_{sub1} and R_{sub2}:

$$\overline{s_{n,R_1,R_{\mathrm{sub1}},R_{\mathrm{sub2}}}}^2 = 4kT(R_1+R_{\mathrm{sub1}}+R_{\mathrm{sub2}})\left|\frac{\frac{1}{j\omega C_{CB1}}g_{mb1}+\frac{1}{j\omega C_{CB2}}g_{mb2}}{j\omega(L_{S2}+L_{S2})+R_1+\frac{1}{j\omega(C_{CB1}+C_{CB2})}}\right|^2\left|R_{\mathrm{out1,2}}\right|^2|G_2|^2. \quad (4.19)$$

The output noise due to R_F:

$$\overline{s_{n,R_F}}^2 = 4kTR_F\left|\frac{R_{out1,2}}{(R_S||Z_{in1}||Z_{in2})+R_F+R_{out1,2}}\right|^2|G_2|^2. \quad (4.20)$$

The noise contributed by the part of the induced gate noise in M_3 that is fully uncorrelated with the drain channel thermal noise:

$$\overline{S_{n,g,u,3}}^2 = \frac{4kT\delta\alpha_3 g_{\mathrm{m3}}\omega^2C_{gs3}^2}{5}\left|R_{\mathrm{out1,2}}\right|^2|G_2|^2. \quad (4.21)$$

The output noise due to correlated induced gate noise source and channel thermal noise source of M_3

$$\overline{s_{n,g,d,c,3}}^2 = \left(\overline{s_{n,d,3}}+\overline{s_{n,g,c,3}}\right)^2$$

$$= \left(\overline{s_{n,d,3}}^2+\overline{s_{n,g,c,3}}^2+2\overline{s_{n,d,3}}\,\overline{s_{n,g,c,3}}\right). \quad (4.22)$$

where

$$\overline{s_{n,d,1}} = \sqrt{\frac{4kT\gamma g_{\mathrm{m3}}}{\alpha}}|R_D+j\omega L_D|,$$

$$\overline{s_{n,g,c,3}} = -j|c|\sqrt{\frac{4kT\alpha\delta}{5g_{\mathrm{m3}}}}|G_2|.$$

Notice that, in (4.21), the power spectrum density (PSD) $\overline{s_{n,g,c,3}{}^2}$ should be absolutely positive. The thermal noise of the resistor R_D can be suppressed significantly by the gain of the preceding stages, so we neglect this calculation for it. Finally, according to (4.22), the noise factor of the proposed LNA can be expressed as

$$F = 1 + \frac{(4.15)+(4.16)+(4.17)+(4.18)+(4.19)+(4.20)+(4.21)+(4.22)}{(4.14)}. \quad (4.23)$$

4.2.5 Layout Consideration

In radio-frequency integrated circuit designs, not only is the well circuit design essential, but the layout is also considerable. The bad layout may give rise to the poor noise figure and/or the parasitic capacitance that degrades the gain significantly. Therefore, the metal line length, especially near the input, should be as short as possible to minimize the noise figure. In the vicinity of the input in our LNA design is shown in Figure 4.12. From this figure, we can see that the metal line length is short (< 50 μm) near the input pad.

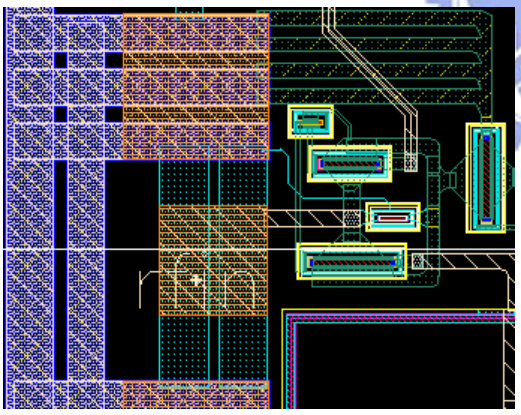


Figure 4.12 Layout near the input pad.

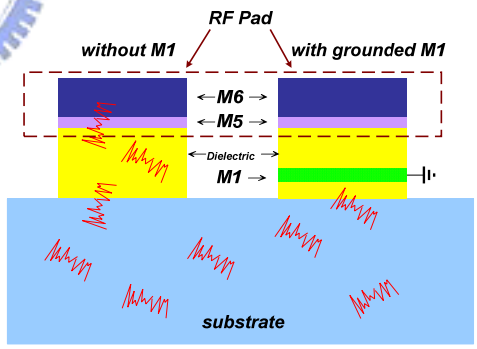


Figure 4.13 RF pad wi/wo the grounded metal-1 layer.

Another issue that also degrades the noise figure results from the input RF pad. As can be seen from Figure 4.13, a lot of thermal noise exists in the substrate that will be coupled to the input RF pad to degrade noise figure. To overcome this problem, we add the grounded metal-1 (M1) layer that will improve the noise figure efficiently.

4.2.6 Simulation and Measurement Result

The simulated results of the LNA with SFBB technique compare with that of the LNA without SFBB technique.

The simulated input impedance matching (S_{11}) with and without SFBB technique are shown in Figure 4.14 and Figure 4.15 respectively:

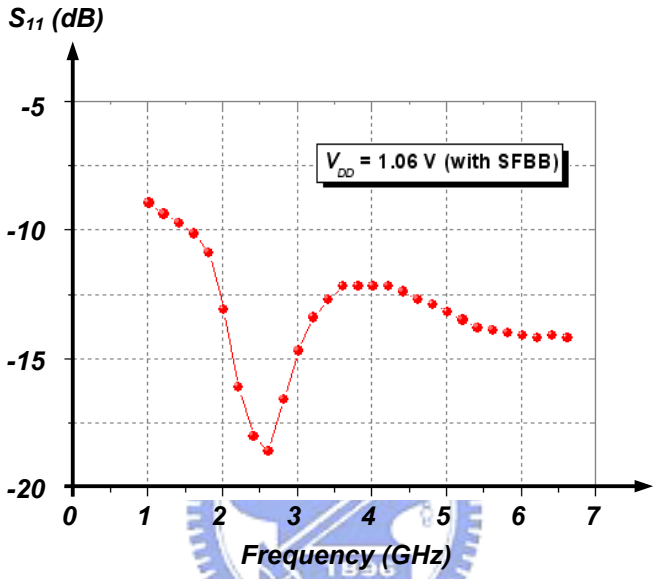


Figure 4.14 Simulated S_{11} (input impedance matching) with SFBB technique.

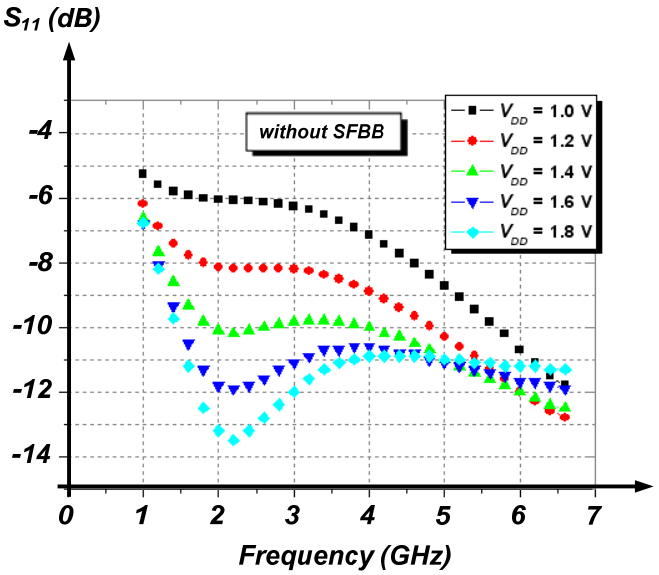


Figure 4.15 Simulated S_{11} (input impedance matching) without SFBB technique under different supply voltages.

The simulated reverse isolation (S_{12}) with and without SFBB technique are shown in Figure 4.16 and Figure 4.17 respectively:

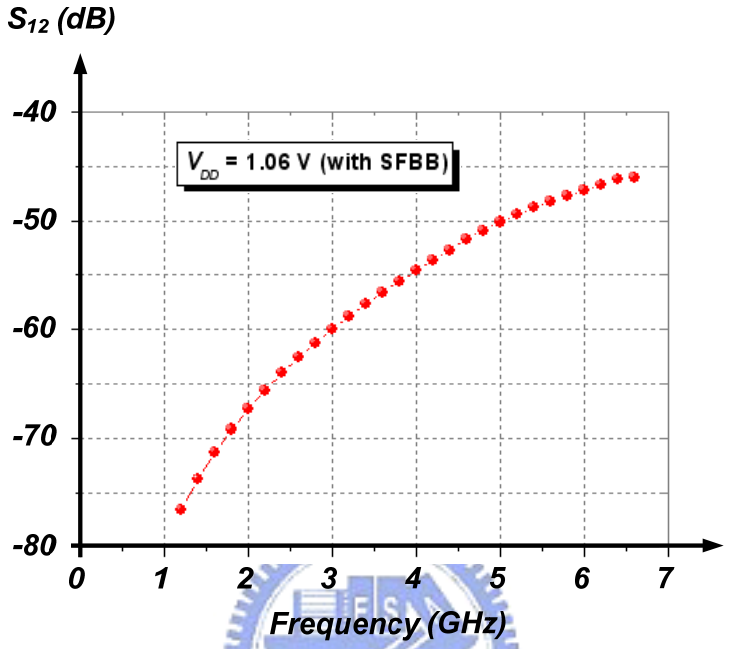


Figure 4.16 Simulated S_{12} (reverse isolation) with SFBB technique.

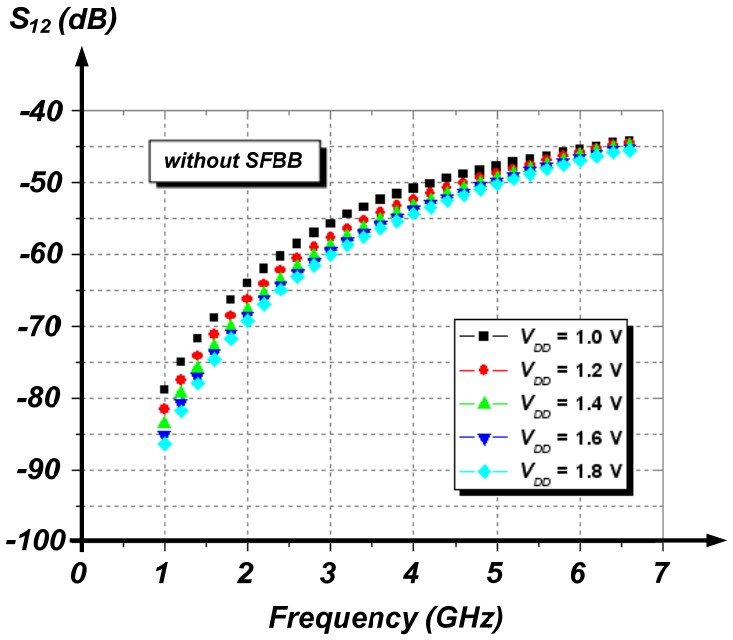


Figure 4.17 Simulated S_{12} (reverse isolation) without SFBB technique under different supply voltages.

The simulated gain (S_{21}) with and without SFBB technique are shown in Figure 4.18 and Figure 4.19 respectively:

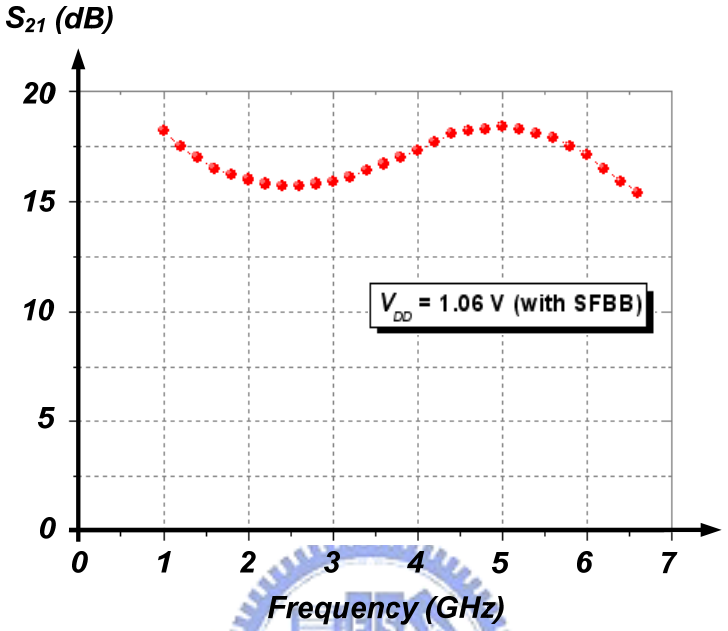


Figure 4.18 Simulated S_{21} (gain) with SFBB technique.

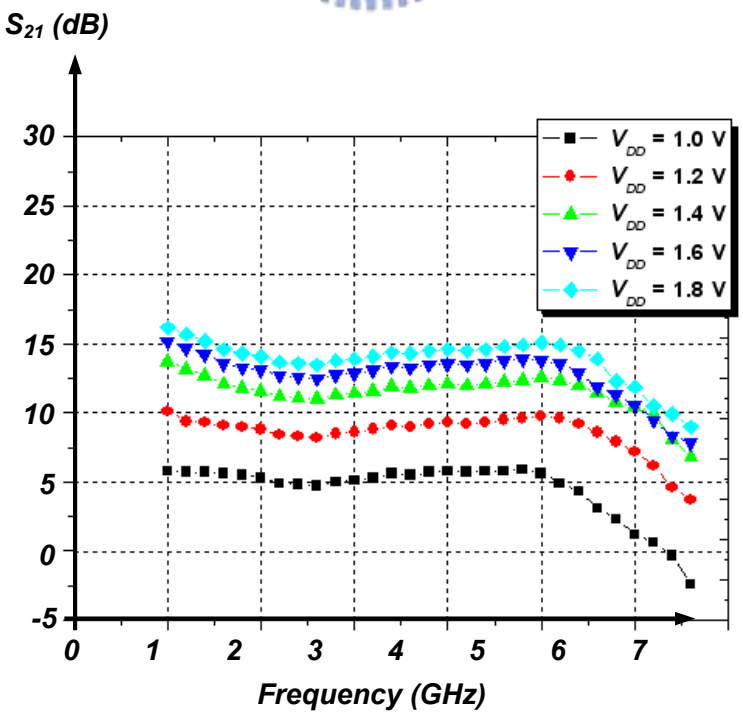


Figure 4.19 Simulated S_{21} (gain) without SFBB technique under different supply voltages.

The simulated output impedance matching (S_{22}) with and without SFBB technique are shown in Figure 4.20 and Figure 4.21 respectively:

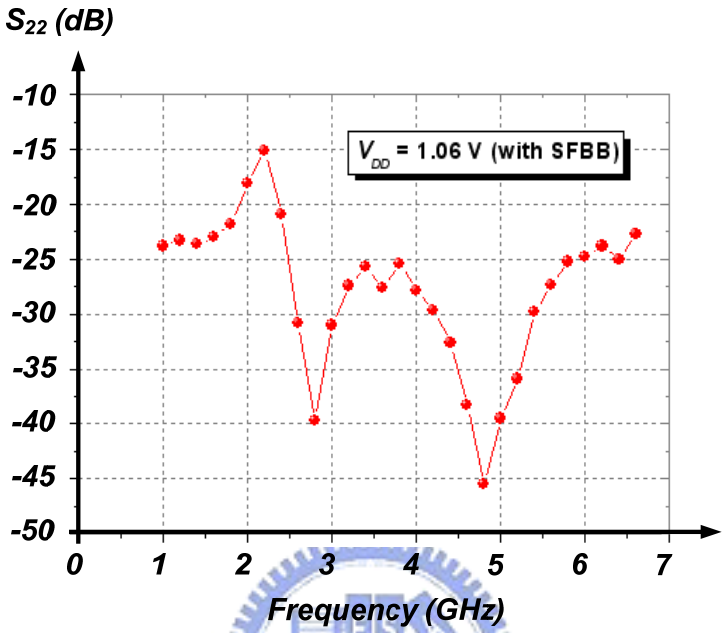


Figure 4.20 Simulated S_{21} (output impedance matching) with SFBB technique.

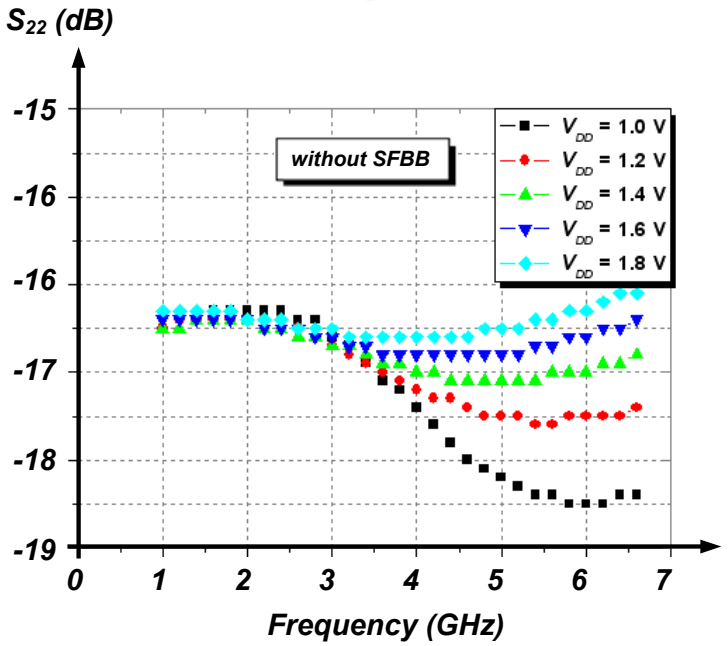


Figure 4.21 Simulated S_{22} (output impedance matching) without SFBB technique under different supply voltages.

The simulated noise figure (NF) with and without SFBB technique are shown in Figure 4.22 and Figure 4.23 respectively:

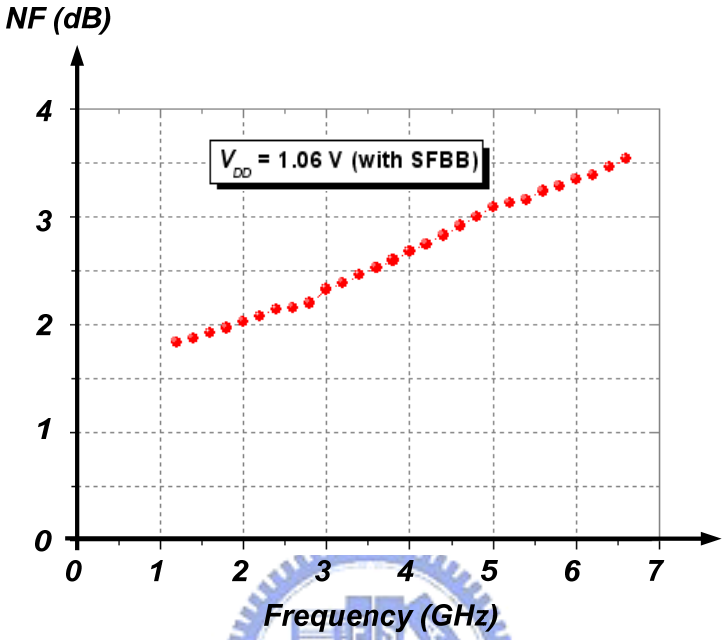


Figure 4.22 Simulated noise figure with SFBB technique.

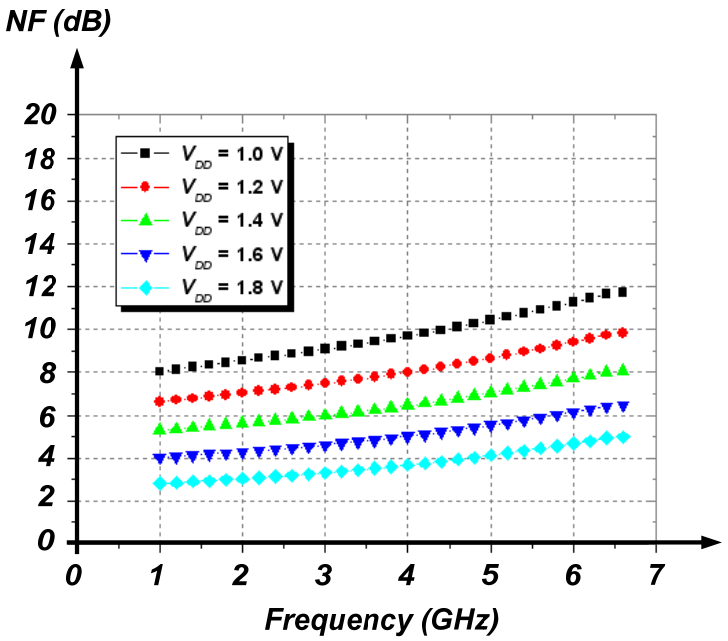


Figure 4.23 Simulated noise figure without SFBB technique under different supply voltages.

The simulated performance summary of with SFBB and without SFBB for different supply voltage is shown in Table 4.1.

Table 4.1 Simulated performance summary of wi/wo SFBB for different supply voltage.

	Supply voltage (V)	Power (mW)	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)
With SFBB	**1.06**	**3.8**	**1.0–6.6**	**< –12**	**15.2-18.2**	**2.2–3.6**
Without SFBB	1.0	1.9	1.0–5.4	< –6	3.0–6.1	8.8–11.7
	1.2	3.0	1.2–6.0	< –8	7.1–9.9	7.3–9.8
	1.4	4.5	1.4–6.1	< –10	9.5–12.6	5.8–8.0
	1.6	6.2	1.4–6.0	< –11	10.6–13.8	4.5–6.5
	1.8	8.1	1.4–6.0	< –12	12.3–15.1	3.2–5.0

The measured results of the LNA with SFBB technique compare with the simulated results.

The measured and simulated input impedance matching (S_{11}) of the proposed LNA is shown in Figure 4.24:

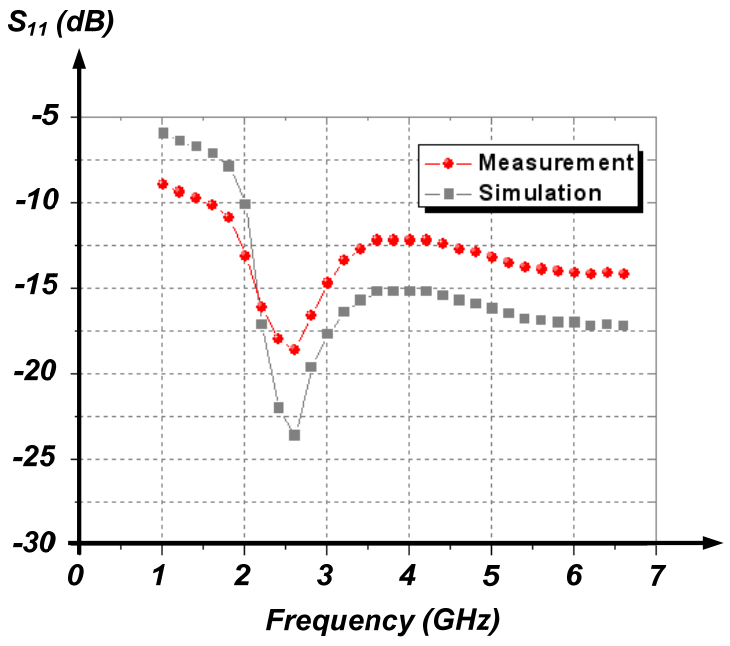


Figure 4.24 Measured and simulated S_{11} (input impedance matching) of the proposed LNA.

The measured and simulated output impedance matching (S_{22}) of the proposed LNA is shown in Figure 4.25:

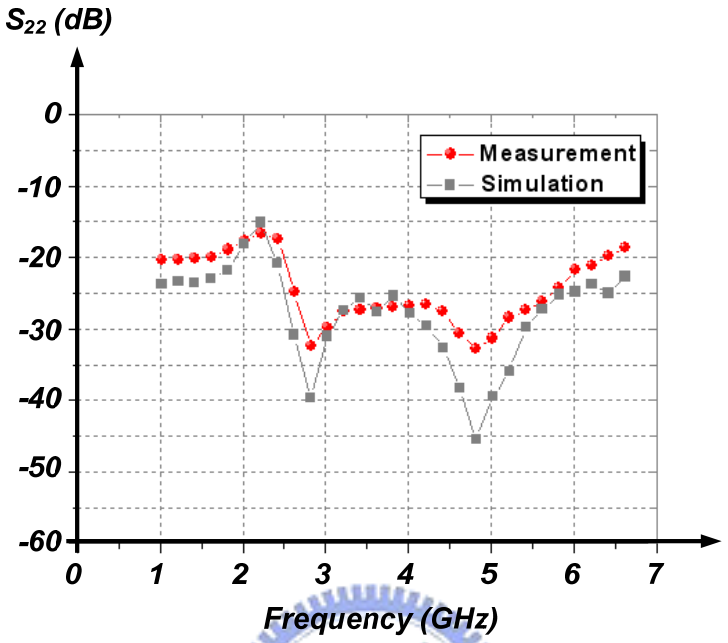


Figure 4.25 Measured and simulated S_{22} (output impedance matching) of the proposed LNA.

The measured and simulated gain (S_{21}) of the proposed LNA is shown in Figure 4.26:

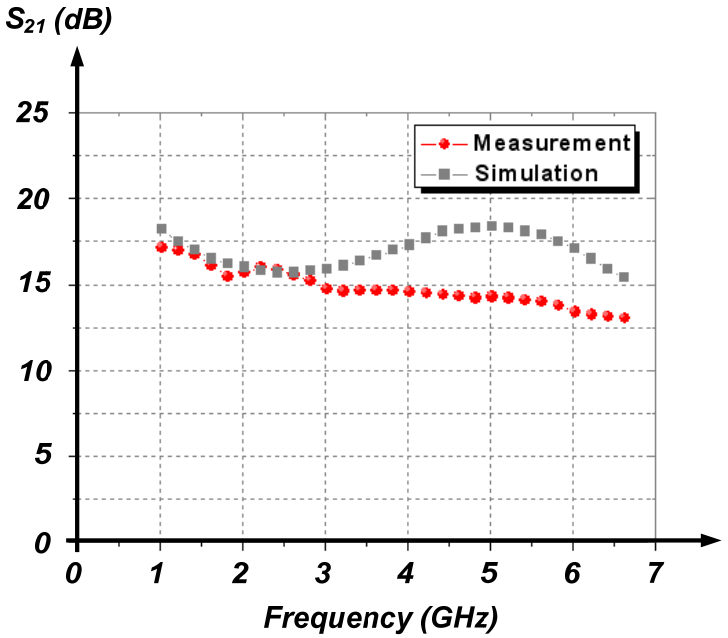


Figure 4.26 Measured and simulated S_{21} (gain) of the proposed LNA.

The measured and simulated reverse isolation (S_{12}) of the proposed LNA is shown in Figure 4.27:

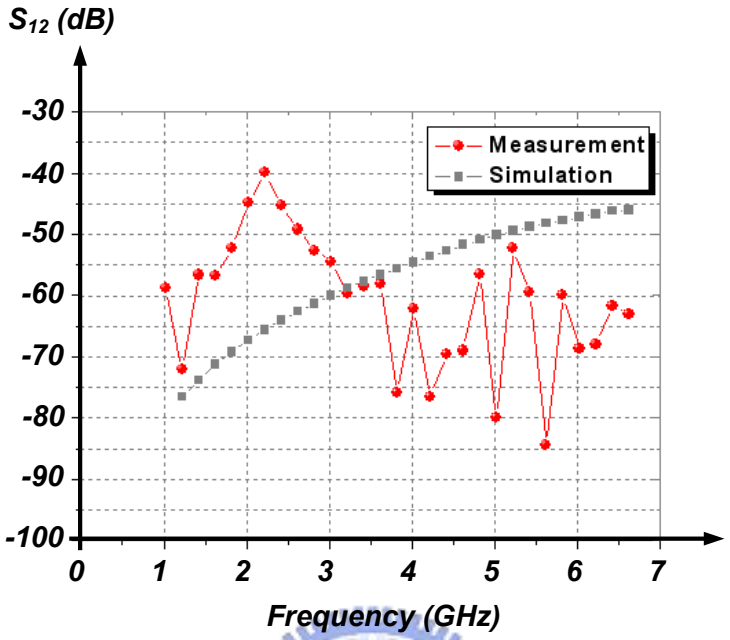


Figure 4.27 Measured and simulated S_{12} (reverse isolation) of the proposed LNA.

The measured and simulated noise figure (NF) of the proposed LNA is shown in Figure 4.28:

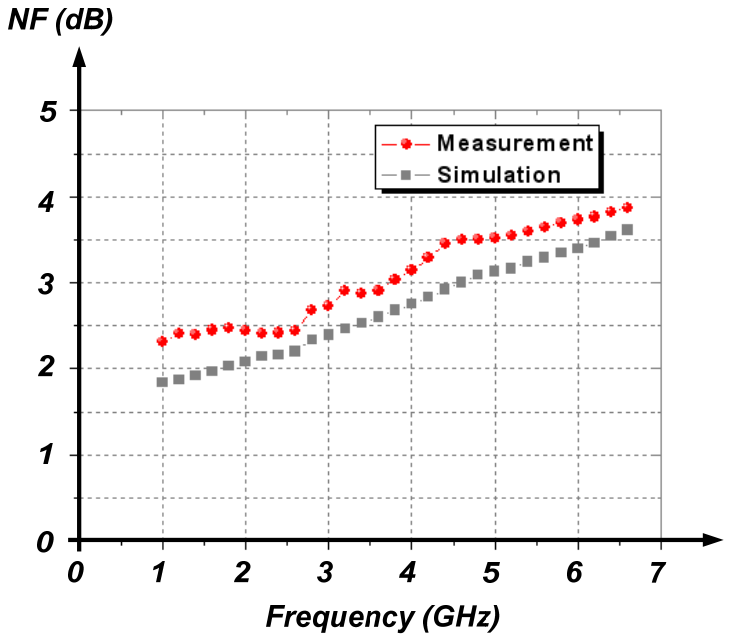


Figure 4.28 Measured and simulated NF (noise figure) of the proposed LNA.

The measured 3rd-order input intercept point (IIP3) at 4 GHz of the proposed LNA is shown in Figure 4.29:

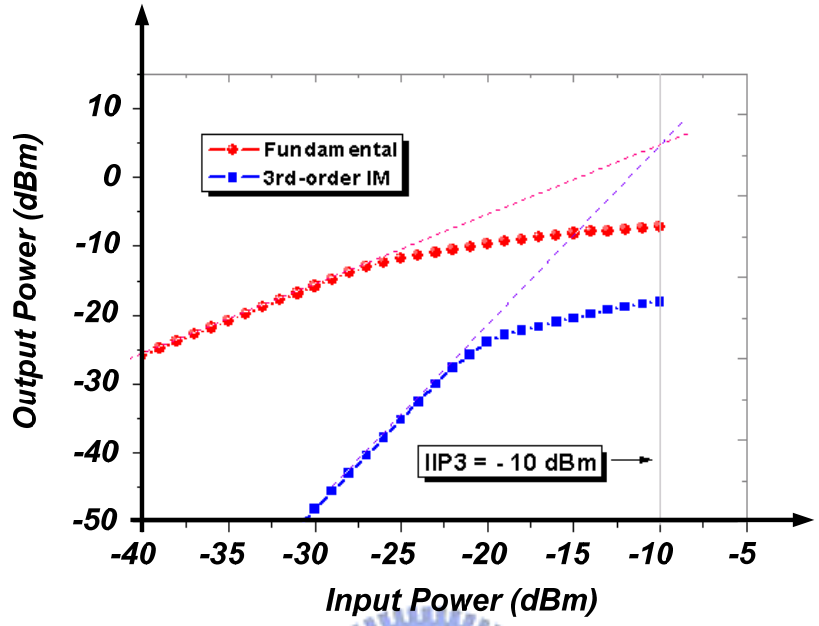


Figure 4.29 Measured third-order input intercept point (IIP3) at 4 GHz of the proposed LNA.

The measured 3rd-order input intercept point (IIP3) versus frequency of the proposed LNA is shown in Figure 4.30:

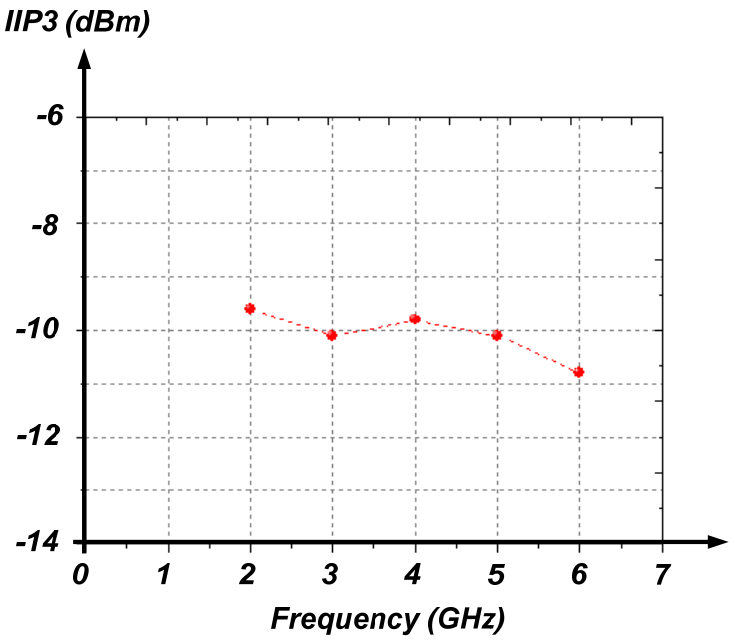


Figure 4.30 Measured third-order input intercept point (IIP3) versus frequency of the proposed LNA.

The measured 1-dB compression point (P1dB) at 4 GHz of the proposed LNA is shown in Figure 4.31:

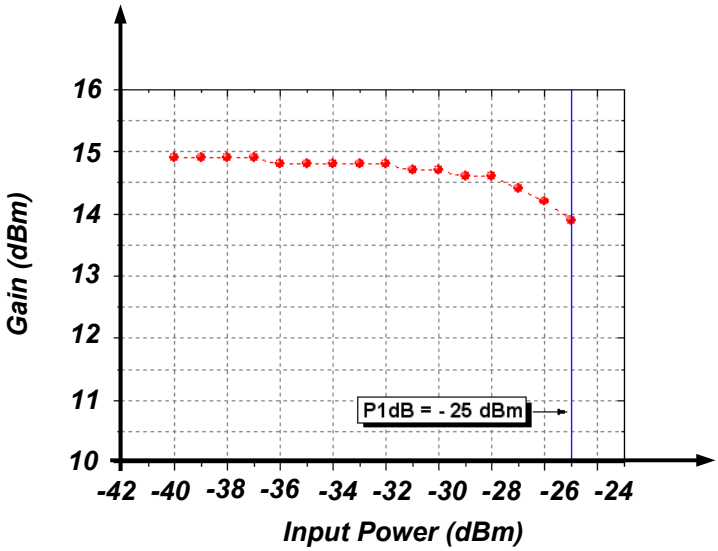


Figure 4.31 Measured 1-dB compression point (P1dB) at 4 GHz of the proposed LNA.

The performance summary of the proposed LNA and comparison with several papers that has been proposed and published is shown in Table 4.2.

Table 4.2 The performance summary of the proposed LNA and comparison with several papers.

Ref.	Tech.	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply voltage (V)	Power (mW)
This work	**0.18-µm CMOS**	**2.6–6.6**	**< –12**	**12.5-15.5**	**2.5–3.9**	**–10@ 4G**	**1.06**	**6.38**
[6]	0.18-µm CMOS	2–8.5	< –10	13*	4.1–4.8	–13.5@ 3 GHz	1.8	9.3
[16]	0.18-µm CMOS	3–5	< –10	13*	4.6–5	0.1 @ 4 GHz	1.8	14.6
[17]	0.18-µm CMOS	3–6	< –8.7	13.6*	3.6–5	–5 @ 4GHz	1.8	12.5
[18]	0.13-µm CMOS	2–4.6	< –10	9.5*	3.5–6.6	–0.8 @ 3 GHz	1.5	16.5
[19]	90-nm CMOS	0.1–8	< –10	16*	3.4–5.8	–9	1.4	16

* Maximum power gain.

The chip layout and microphotograph of the proposed LNA are shown in Figure 4.32(a) and Figure 4.32(b) respectively, and the chip area is 0.96 mm × 0.64 mm (0.61 mm^2).

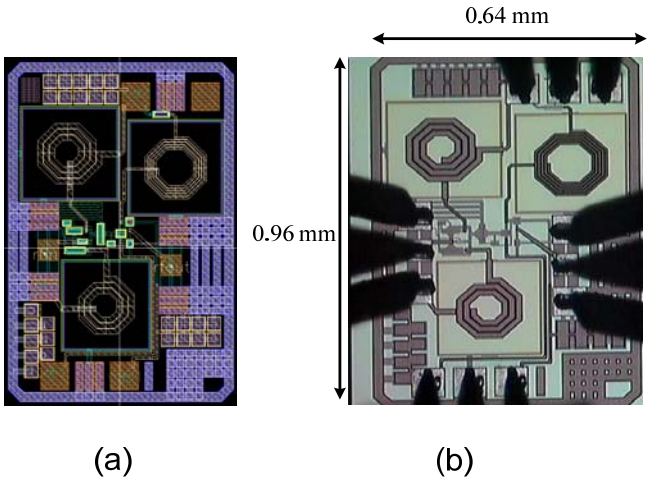


Figure 4.32 (a) Layout, (b) microphotograph of the proposed LNA.

4.3 Noise Improvement for The proposed LNA

In the preceding LNA design, **called the LNA 1 after here**, more substrate thermal noise will be coupled to MOSFET channel under the self forward bulk-source bias than that under zero bulk-source bias will, since the bulk-source depletion becomes narrow. And the complementary architecture also degrades the noise figure significantly, because there are two channel thermal noise sources and two induced gate noise sources in the first stage. For these issues, we have to find some ways to improve the noise performance.

4.3.1 Noise Improvement

Under the forward bulk-source bias, the depletion between the channel and substrate becomes narrower than zero bulk-source bias does. As shown in Figure 4.32, thermal noise contributed from the substrate will be coupled to channel more easily. Therefore, we utilize a capacitor that provides a path for the substrate thermal noise toward ground as well as does not affect the self voltage-divided loop.

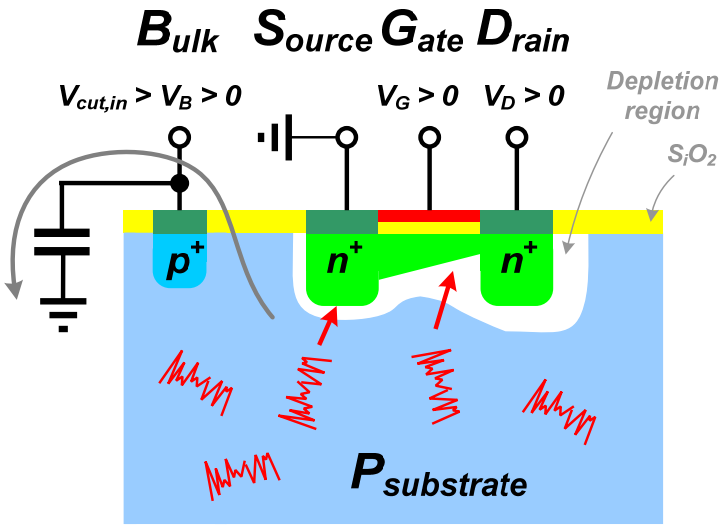


Figure 4.33 Reduce the noise contributed from the substrate.

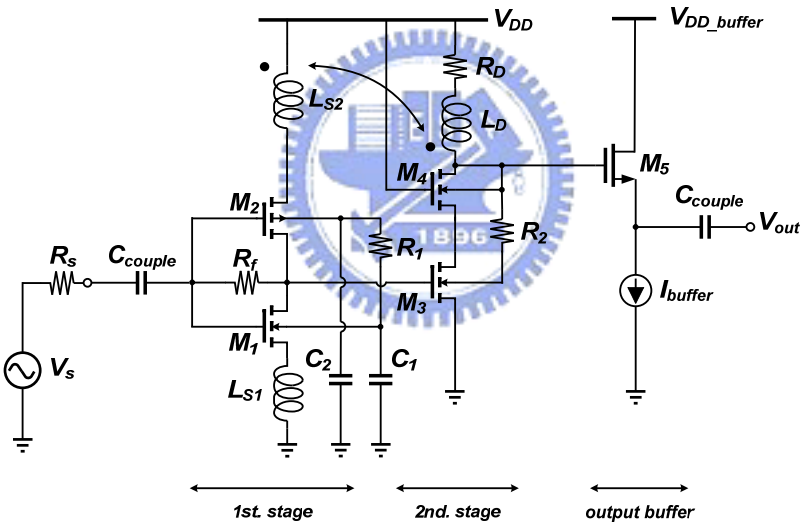


Figure 4.34 The proposed noise-improved LNA.

In order to suppress the noise contribution from the substrate and R_1, we employ two capacitances, C_1 and C_2, to provide the paths for these noise sources toward ground, as shown in Figure 4.33.

Another significant noise degradation results from the complementary architecture since there are two channel thermal noise sources and two induced gate noise sources in the first stage. To improve the noise degradation, we select to suppress the channel thermal noise contributed from M_2 by coupling both the inductors, L_{S2} and L_D.

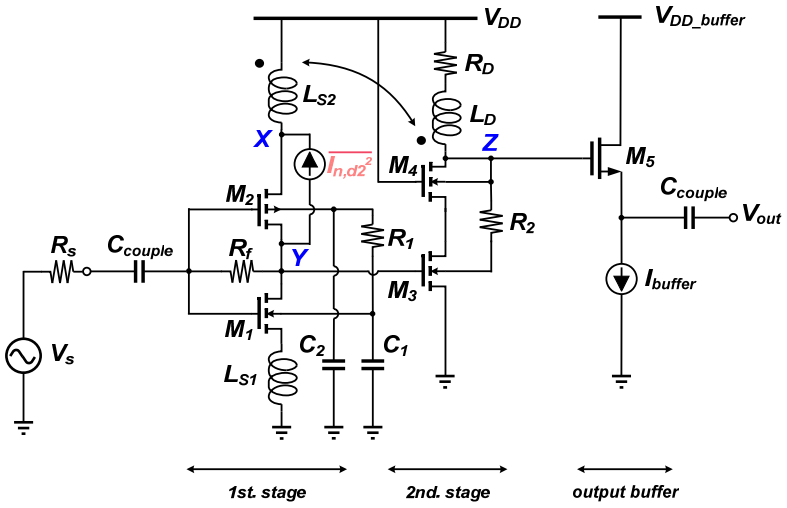


Figure 4.35 The proposed noise-improved LNA with equivalent channel thermal noise source .

From Figure 4.34, at the first, we assume that the channel thermal noise voltage at *X* contributed from M_2 is positive while negative at *Y* relatively. Thus, the noise voltage at *Z* which is resulted from the noise voltage at *Y* through the cascode stage path is given by

$$\overline{V_{n,z1}} \approx \sqrt{\frac{4kT\gamma g_{m2}}{\alpha}}\left[(j\omega L_{S1} g_{m1} r_{O1}) \| (j\omega L_{S2} g_{m2} r_{O2}) \| R_f\right] g_{m3}(R_D + j\omega L_D) \approx jA - B \qquad (4.24)$$

where *A* and *B* represent the imaginary and real part respectively.

At this point, in order to suppress the channel thermal noise contributed from M_2, we utilize another path, mutual inductor (L_{S2}, L_D), toward *Z* to reduce the noise with opposite polarity to that of (2.4). The channel thermal noise voltage contributed from M_2 through the mutual path at *Z* is negative while positive at *X* assumed above, which is given by.

$$\overline{V_{n,z2}} \approx \sqrt{\frac{4kT\gamma g_{m2}}{\alpha}}\left(\frac{1/g_{m2}}{1/g_{m2}+j\omega L_{S2}}\right)(-j\omega M) + \frac{K^2}{n^2}\sqrt{\frac{4kT\gamma g_{m2}}{\alpha}} R_D \approx -jC + D \qquad (4.25)$$

where *n*, *M*, and *K* denotes the turn ratio, mutual inductance and coupling coefficient, and *C* and *D* represent the imaginary and real part respectively.. Therefore, combining both the contrary noise voltage at point *Z* can achieve the noise suppression. Furthermore, using the mutual inductor can reduce the chip area effectively.

However, there is an issue while using this mutual inductor mentioned above. From Figure 4.34, the RF signal at point *X* and point *Y* are out of phase of that at point *Z*, and the second cascode stage that provides a negative voltage gain. Then, this loop forms a positive

feedback that the LNA may not stable to oscillate. Consequently, there is a tradeoff between the noise suppression and unstable condition. Thus, we separate both the inductor a little to avoid oscillating. The chip layout and microphotograph of the proposed LNA are shown in Figure 4.35(a) and (b) respectively, and the chip area is 0.99 mm × 0.47 mm.

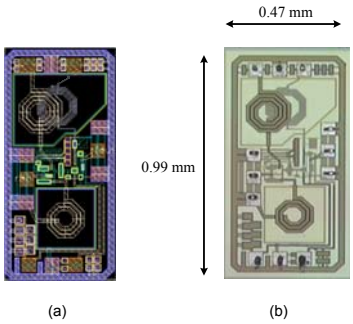


Figure 4.36 (a) Layout, (b) microphotograph of the proposed noise-improved LNA.

4.3.2 Measurement Result

The measured results of the noise-improved LNA, **called the LNA 2** with SFBB technique compare with that of the preceding LNA, **called the LNA 1**.

The measured noise figure (NF) of the proposed noise-improved LNA is shown in Figure 4.37:

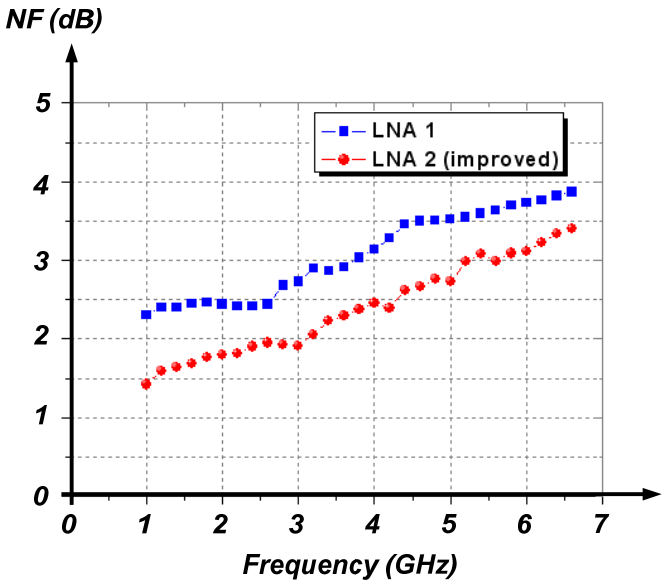


Figure 4.37 Measured NF of the proposed noise-improved LNA.

The measured S_{11} of the proposed noise-improved LNA is shown in Figure 4.38:

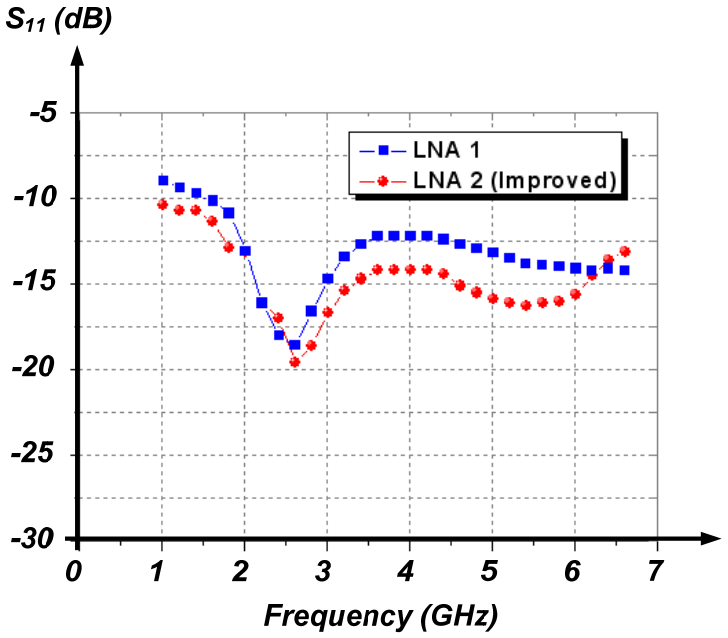


Figure 4.38 Measured S_{11} of the proposed noise-improved LNA.

The measured S_{22} of the proposed noise-improved LNA is shown in Figure 4.39:

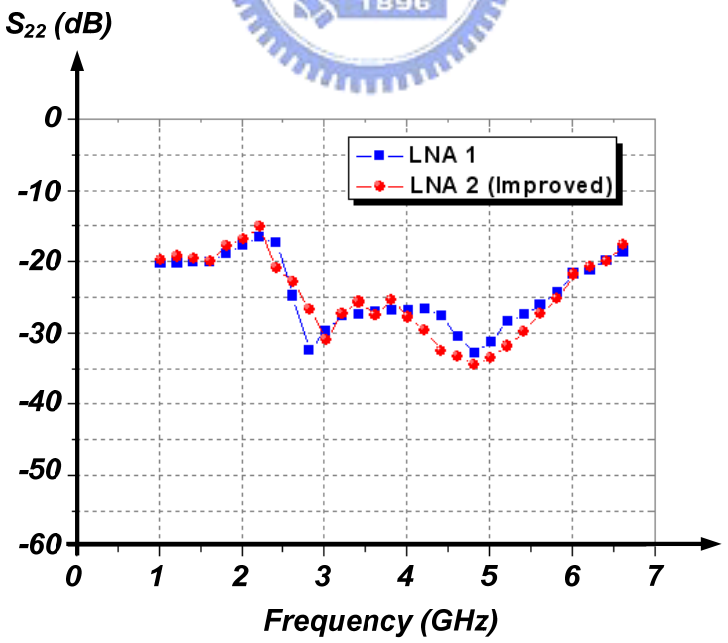


Figure 4.39 Measured S_{22} of the proposed noise-improved LNA.

The measured S_{21} of the proposed noise-improved LNA is shown in Figure 4.40:

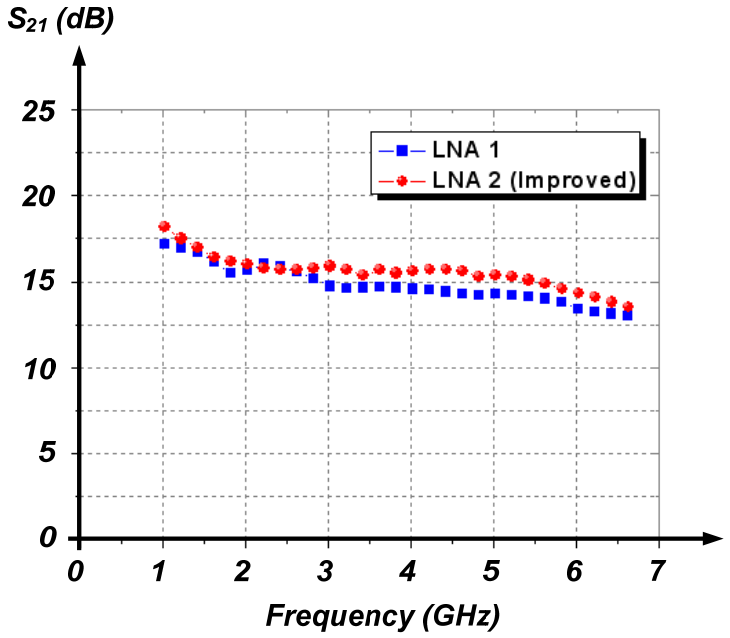


Figure 4.40 Measured S_{21} of the proposed noise-improved LNA.

The measured S_{12} of the proposed noise-improved LNA is shown in Figure 4.41:

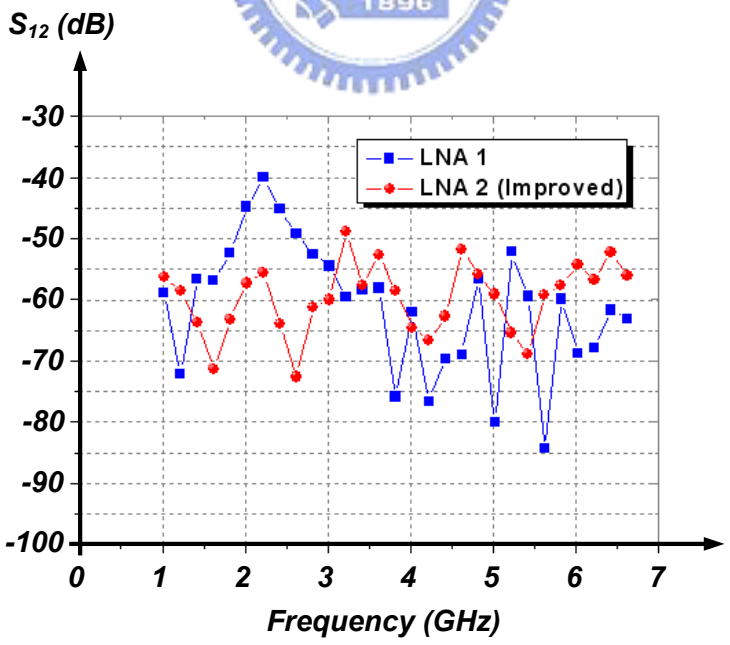


Figure 4.41 Measured S_{12} of the proposed noise-improved LNA.

The measured 3rd-order input intercept point (IIP3) at 4 GHz of the proposed noise-improved LNA is shown in Figure 4.42:

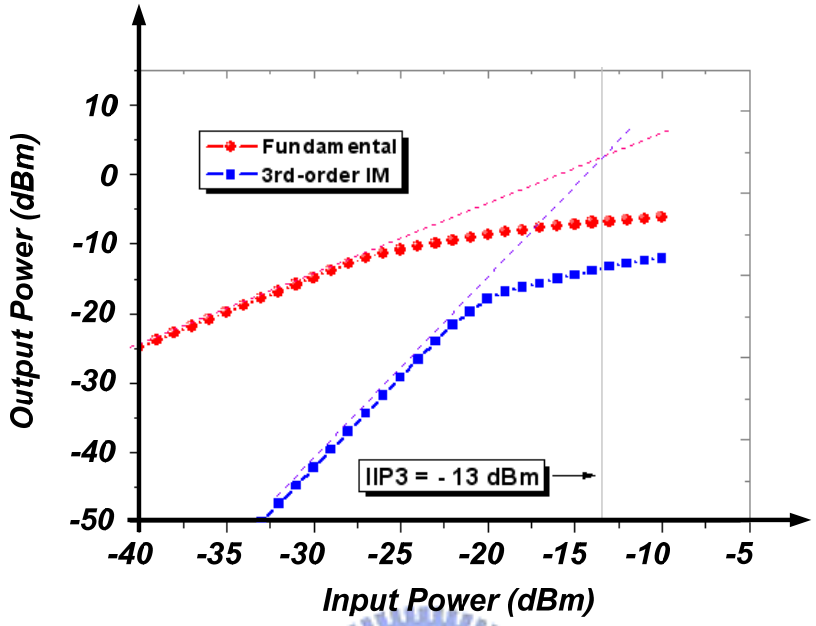


Figure 4.42 Measured IIP3 at 4 GHz of the proposed noise-improved LNA.

The measured third-order input intercept point (IIP3) versus frequency of the proposed noise-improved LNA is shown in Figure 4.43:

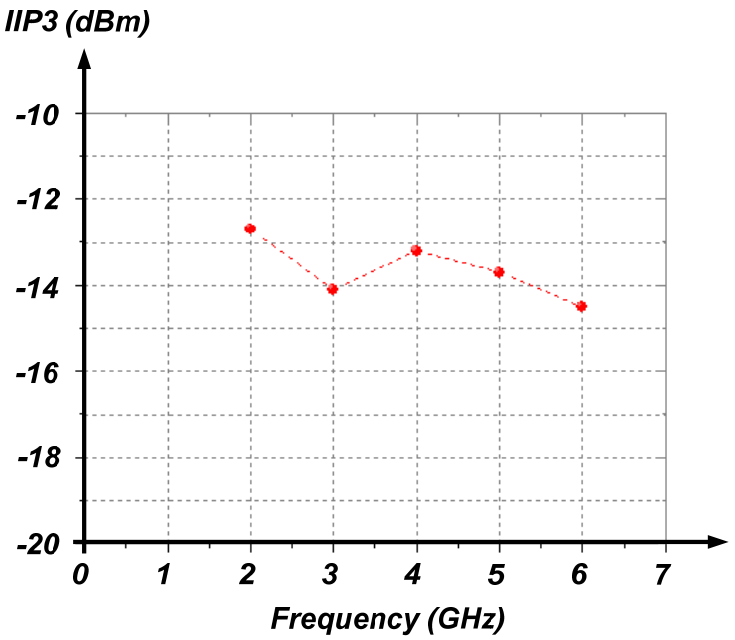


Figure 4.43 Measured third-order input intercept point (IIP3) versus frequency of the proposed noise-improved LNA.

The measured 1-dB compression point (P1dB) at 4 GHz of the proposed noise-improved LNA is shown in Figure 4.44:

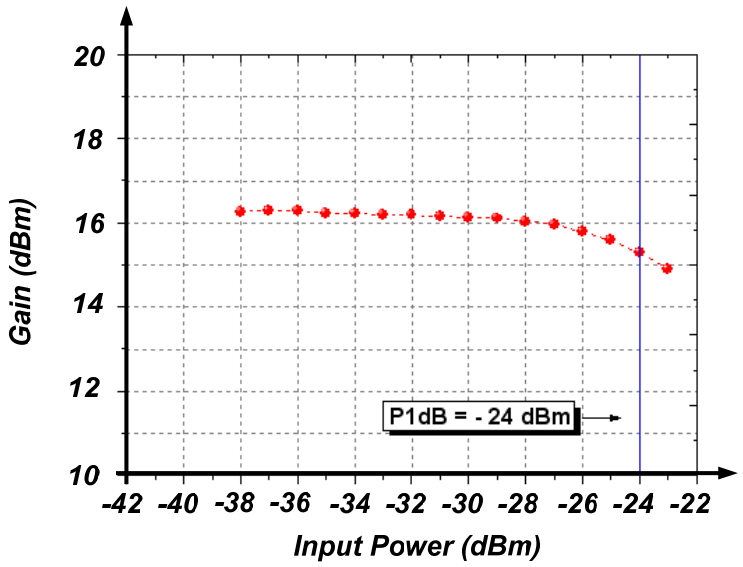


Figure 4.44 Measured third-order input intercept point (IIP3) at 4 GHz of the proposed noise-improved LNA.

The performance summary of the noise-improved LNA and comparison with several papers that has been proposed is shown in Table 4.3.

Table 4.3 The performance summary of the noise-improved LNA and comparison with several papers.

Ref.	Tech.	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply voltage (V)	Power (mW)
LNA 2 (Improved)	**0.18-µm CMOS**	**2.0–6.6**	**< –12**	**13–16**	**1.8–3.4**	**–13@ 4GHz**	**1.06**	**4.53**
LNA 1 (Preceding)	**0.18-µm CMOS**	**2.6–6.6**	**< –12**	**12.5–15.5**	**2.5–3.9**	**–10@ 4GHz**	**1.06**	**6.38**
[6]	0.18-µm CMOS	2–8.5	< –10	13*	4.1–4.8	–13@ 3 GHz	1.8	9.3
[16]	0.18-µm CMOS	3–5	< –10	13*	4.6–5	0.1 @ 4 GHz	1.8	14.6
[17]	0.18-µm CMOS	3–6	< –8.7	13.6*	3.6–5	–5 @ 4GHz	1.8	12.5
[18]	0.13-µm CMOS	2–4.6	< –10	9.5*	3.5–6.6	–0.8 @ 3 GHz	1.5	16.5
[19]	90-nm CMOS	0.1–8	< –10	16*	3.4–5.8	–9	1.4	16

* Maximum power gain.

Chapter 5 *Conclusion*

The low-power UWB LNA has been demonstrated in 0.18-μm CMOS 1P6M process. Low-power consumption is achieved by using a forward bulk-source bias (or called the forward body bias, FBB). And the forward bulk-source voltage in our design is obtained by means of the proposed ultra-low power self-bias that we don't need an additional bias circuit to supply the bulk terminal of MOSFET. However, the self forward body bias technique will give rise to some noise figure degradation. Therefore, we proposed the second LNA (LNA 2), to improve the noise figure of the preceding LNA (LNA 1). The measurement result shows that the LNA 1 has a gain of 12.5–15.5 dB from 2.6 to 6.6 GHz with a good input/output matching S_{11}<-10 dB and S_{22}<-17 dB and average noise figure of 3.2 dB while consuming power of 6.3 mW from 1.06 V voltage supply. The chip area is 0.96 mm × 0.64 mm. And the proposed noise-improved LNA 2 to improve the noise figure degraded lightly by the self-bias loop. The measurement result of the LNA 2 shows that it has a gain of 13.5–16.2 dB from 2.0 to 6.6 GHz with a good input/output matching S_{11}<-10 dB and S_{22}<-16 dB and average noise figure of 2.6 dB while consuming power of 4.5 mW from 1.06 V voltage supply. The chip area is 0.98 mm × 0.47 mm.

References

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