國 立 交 通 大 學

電信工程學系

碩 士 論 文

一個應用於-55˚C ~125˚C智慧型溫度感測器之

1.8V、12.9微瓦三角積分類比數位轉換器

A 1.8V 12.9uW Sigma-Delta A/D converter

for a -55˚C ~125˚C smart temperature sensor

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摘要

準確且低功率消耗的溫度感測元件在量測及生物醫學領域之應用是個不可缺少的元件，隨著積體電路(IC)的技術進步，一個新的溫度感測器已經被研究並發展，此新式的溫度感測器被命名為「智慧型溫度感測器」。本篇論文提出一個適用於智慧型溫度感測器後端介面之類比-數位轉換器。並經由台積電 0.18 微米製程實現了一個 12 位元並應用在類-直流(dc-like)頻段信號的積分-三角類比數位轉換器。

本篇論文提出的電路由前端的積分-三角類比數位調變器以及後端的 SINC 濾波器所組成。前端的積分三角調變器以 CIFF 架構來達成低電壓低功率的操作，並以 CDS 的技巧消去低頻雜訊，而後端的 SINC 濾波器具備了抑制電力線雜訊的特性。此篇電路在正常模式下之功率消耗維 12.917 微瓦、能量消耗維 0.646 微焦耳，而休眠狀態之功率消耗為 2.014 微瓦。本篇論文之電路架構適用於低功率、高解析度之溫度感測系統應用。

A 1.8V 12.9uW Sigma-Delta A/D converter for a -55˚C ~125˚C smart temperature sensor

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Abstract

Low power and accurate temperature sensing device is an essential element in many applications, such as biomedical system and instrumentation application. With the development of Integrated-Circuit(IC) technology, a new temperature sensing device has been developed. It has been named as ”Smart temperature sensor”. This thesis focuses on the design of the back-end interface of the smart temperature sensor. A sigma delta ADC with high resolution (12 bits) for dc-like signals is designed and implemented in TSMC 0.18um process.

The developed circuitry is composed of a sigma-delta modulator, which utilized CIFF architecture and CDS technique for low-power, low-voltage operation and low-frequency noise reduction, and a back-end SINC filter for line-noise attenuation. A power consumption of 12.917uw and energy consumption of 0.646uJ for each conversion in normal mode and 2.014uW power consumption in sleep mode is achieved. This design is suitable to the temperature sensing system for the low-power and high-resolution conditions.

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緊接著，謝謝嘉儀、智仁、江俊、品翰、秉勳、凱迪、明君、以及俊誼這八位學長在研究上及日常生活上對我的照顧；還要謝謝鎮宇、國哲、鼎國、燦杰四位同學以及學弟登政在我的課業及生活上的幫忙;平常在研究領域上的討論及切磋，讓我的基本觀念能夠更加的紮實。也謝謝文仲、維盈、舜婷、鄭綺等學弟妹們的支持與幫忙。最後還要特別謝謝大學同學偉琳、立夫、建霖、洛維、等人對我在專業領域上的幫助。有了各位的陪伴，才造就了這段充實、快樂、豐富的碩士班研究生活。這段日子的陪伴將永遠留在學生的記憶裡。

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我由衷感謝上述曾提攜或幫助過我的你們，誠心謝謝並祝福大家。

溫是瑜

November,11,2009 於新竹

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Chapter 1

Introduction

1.1 Motivation

In the development of human civilization, temperature sensing has been demanding and sustaining. Many reference temperature points, such as freezing and boiling point of water and the temperature of human body, has been found so that comparison between these fixed point can be made for temperature judgment. With the judgment temperature information, corresponding response can be made for the measuring system. Therefore, accurate temperature sensor, which sense and convert the temperature signal, is an essential element in many applications.

The resistance thermometer, such as Pt-100 and the thermistor, dominated the market of temperature sensors in the past five years. However, with the development of integrated circuit(IC) technology, the smart temperature sensor, which is a novel temperature sensing device, has been researched and developed. The smart temperature sensor integrates the front-end BJT or MOS sensing unit and the back-end analog-to-digital electrical interface.

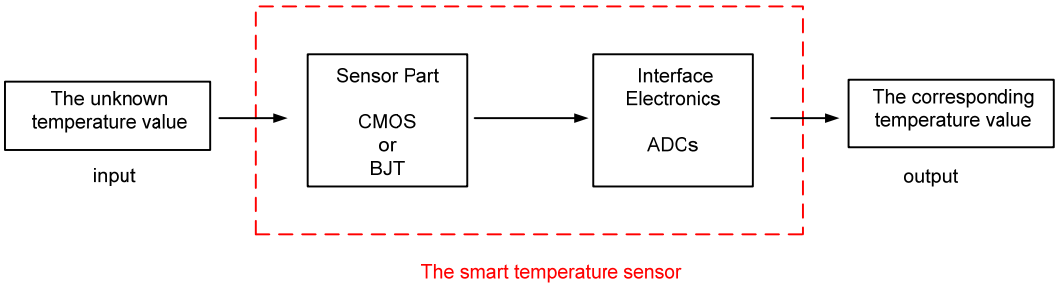


Fig.1-1 Architecture of the smart temperature

Here, both of it can easily be implemented in semi-conductor process. For the reasons, the smart temperature sensor is suitable for system-on-chip (SoC) application, which is the advantage of the new temperature sensing device than the conventional sensors.

In the system of smart temperature sensor, the analog-to-digital electrical interface, which determines the performance of the whole system, is a critical building block. A high performance A/D converter is needed for accurate converting the external analog temperature signal to digital voltage signal, which can be processed by the back-end digital systems. Here, the analog-to-digital electrical interface can be classified to three different types by the corresponding principle of conversion [1]. It is “frequency conversion”, “duty-cycle conversion” and “sigma-delta modulation”.

Previous researches indicated that the sigma-delta A/D converter has the best trade-off as the back-end A/D interface when comparing to frequency conversion or successive-approximation conversion [1]. In recent researches, accurate and wide sensing range smart temperature sensor with sigma-delta A/D as the electrical interface has been published [2]-[7].

In this paper, a 12bit sigma-delta A/D converter with 12.9uW power consumption and 0.646uJ energy consumption for each temperature conversion in Normal mode and 2.014uW power consumption in sleep mode is designed. It will be integrated into an advanced all CMOS temperature sensor system.

1.2 Organization

In Chapter 2, a brief introduction and an overview of analog-to-digital converters (ADCs) will be the beginning. After that, fundamental principle of first-order sigma-delta ADC for dc-like signal will be mentioned. Next, higher order architecture will be discussed. Finally, the performance metrics of sigma-delta modulator (SDM) will be the end of this chapter.

Chapter 3 describes the expectation and challenges of designing advanced all-CMOS smart temperature. The system level design consideration will be followed, which includes the analysis of power and energy issue of the back-end sigma-delta ADC, describes the system level design considerations, SDM topology selection and system parameter decision. The discussion of non-ideal effects, such as finite OP gain and thermal noise, ends this chapter.

The topic of Chapter 4 is design of the sub-circuits used for realizing the whole sigma-delta ADC. Transistor level design of the sigma-delta modulator which includes an OPAMP, a bias circuit, a 1-bit quantizer and a non-overlapped clock generator and the SINC filter will be discussed. Next, the layout level design will be followed. Finally, the system simulation result will be showed and compared with the related researches.

In Chapter 5, the testing environment and experimental result of the sigma-delta ADC is presented.

Chapter 6 ends the whole thesis. Brief conclusion and the future works will be arranged in this Chapter.

Chapter 2

Fundamental of Analog-to-Digital Conversions in Temperature Sensing Application

This chapter begins with a brief introduction and an overview of analog-to-digital converters (ADCs). The fundamental principle of first-order and higher-order sigma-delta ADC for dc-like signal will be followed. Finally, the performance metrics of sigma-delta modulator (SDM) ends this chapter.

2.1 A Brief Introduction of ADC

Despite real life signals that we meet in our daily life are analog signals, digital signals, which can easily be encoded and have the characteristic of low-distortion, are preferred to be used in many applications. For the reasons, analog-to-digital converters (ADCs), which convert real word signal to digital forms, are essential elements in our life.

In the process of signal conversion, the working principles of analog-to-digital converter can be classified to two major operations. The first one is the discretization in time, which can be called as sampling. After sampling, the second operation is the quantization in signal amplitude. A simplified block diagram of ADC can be shown as Fig.2.1

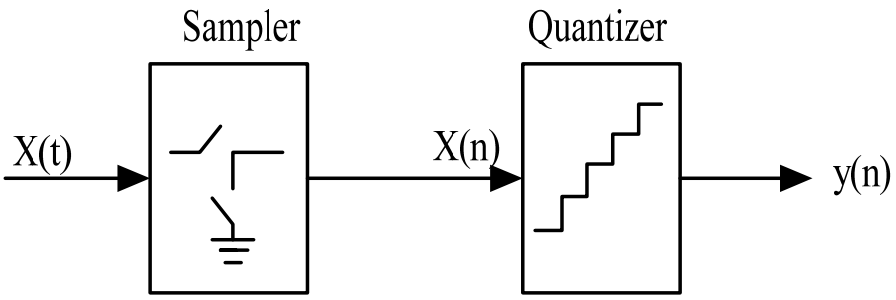


Fig.2.1 Simplified block diagram of ADC.

After analog-to-digital conversion, the signal transfer curve of analog-to-digital converter can be made, as shown in Fig.2.2.

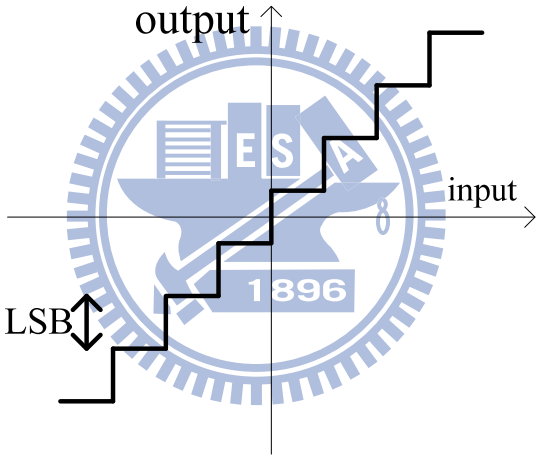


Fig2.2 Ideal transfer curve of ADC

For Fig.2.1, the LSB of an N bit ADC can be called as the quantization step and it can be written as $\Delta = {V_{ref}}/{2^N}$.

Since quantization happened in the process of conversion, quantization error e_q will exist. The relations between quantization error e_q and quantization step $\Delta = {V_{ref}}/{2^N}$ in correctly working situation can be written as:

$$-\frac{\Delta}{2} \le e_q \le \frac{\Delta}{2} \tag{2.1}$$

Here, an assumption is made that the quantization noise is a white noise. Therefore, the quantization error is uniformly distributed in the range of $\pm\frac{LSB}{2}$, as shown in Fig.2.3.

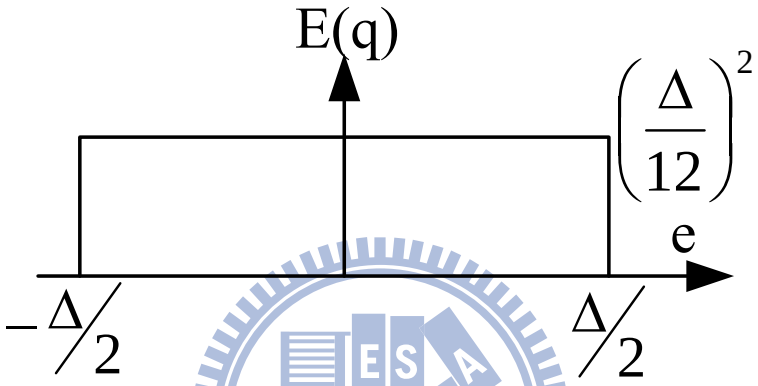


Fig.2.3 Power spectrum density of quantization error e_q

Therefore, the power of quantization error can be calculated as:

$$P_e = \int_{-\infty}^{\infty} e^2 \rho(e_q) de = \frac{\Delta^2}{12} \tag{2.2}$$

Next, the power of a sinusoidal wave can be derived as:

$$P_{in} = \frac{1}{2}\left(\frac{2^N \Delta}{2}\right)^2 = \frac{2^{2N}\Delta^2}{8} \tag{2.3}$$

where N is the bit number of the quantizer

With previous equations, the ideal signal-to-noise ratio (SNR) of an analog-to-digital converter can be derived as:

$$SNR_{peak} = 10\log\left(\frac{P_{in}}{P_e}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}}\right) = 10\log\left(2^{2N}\right) + 10\log\left(\frac{3}{2}\right) = 6.02N + 1.76(dB) \quad (2.4)$$

It can easily be realized that one bit resolution increasing will also increase 6.02dB in SNR.

For an analog-to-digital converter, the signal bandwidth and the system resolution are two important parameters. Trade-off between signal bandwidth, resolution and circuitry complexity always happen in the design of analog-to-digital converter. Corresponding ADC architecture is designed and developed for different bandwidth and resolution requirement, as depicted in Table 2.1.

Application	Resolution	Bandwidth	Architecture of ADCs
Microcontroller	Low-Med	Low-Med	Successive apprx, Algorithm, Cyclic
Dc, sensor application and LF. measurement	High	Low-Med	Dual-slope, Voltage-to-frequency, Incremental sigma-delta
Audio	High	Med	Successive apprx, Sigma-delta modulation
Video	Med-High	High	Flash, Pipeline, Low-OSR sigma-delta modulation
Telecommunication	Med	High	Flash, High-OSR sigma-delta modulation

Table 2.1 Corresponding ADC architectures for different resolution/bandwidth applications

After the brief introduction of ADCs, the A/D conversion principle of temperature sensing will be further introduced at next section.

2.2 A/D Conversions in Temperature Sensing Application

This section will briefly introduce the commonly used working principle of A/D conversions in temperature sensing. Frequency conversion will be described first, followed by duty-cycle and sigma-delta modulation [1]. Finally, a comparison between these conversions will be discussed.

2.2.1 Frequency Conversion

In frequency conversion A/D conversion, the outside analog temperature signal will be convert and founded in corresponding signal frequency. The principle can be interpreted by a simplified circuit diagram, as shown in Fig.2.4.

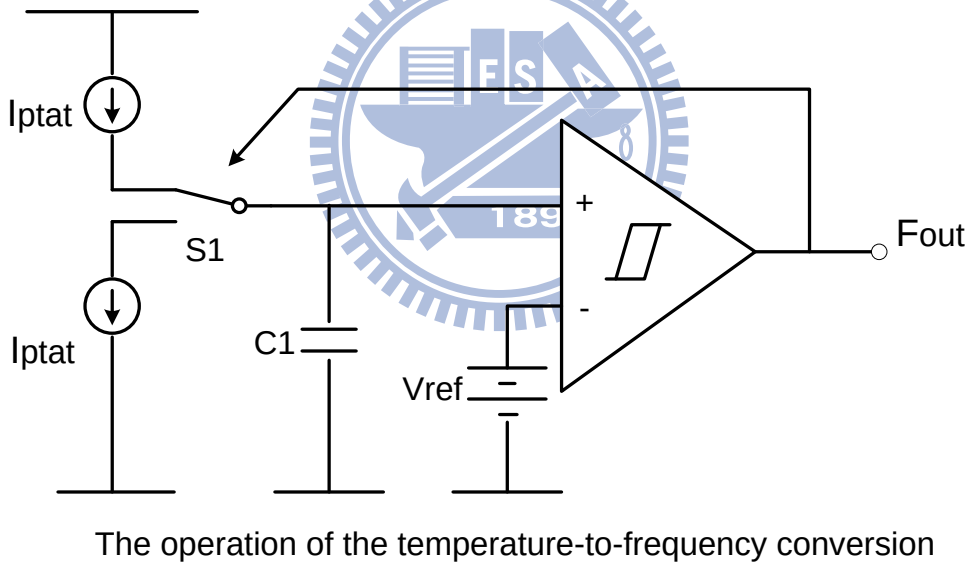


Fig.2.4 Simplified circuit architecture of frequency conversion ADC

In the process of conversion, two phases can be classified:

Phase I: Iptat charges C1. When the voltage on C1 reaches Vref+Vhyst, Fout switches to 0. Here, Vhyst is the hysteresis voltage of the comparator and Iptat is the positive-to-absolute-temperature current source.

Phase II: The charge on C1 starts to discharge. When the voltage on C1 reaches Vref-Vhyst, Fout switches to 1.

Finally, the output frequency can be calculated as:

$$F_{out} = \frac{2 \cdot I_{ptat}}{C1 \cdot V_{hyst}} \tag{2.5}$$

After previous derivation, it means that the temperature information can be found in signal frequency.

The advantages of frequency conversion are the simplicity of the circuitry. A ptat current generator, a hysteresis comparator and a capacitor is sufficient for the whole circuit. The frequency domain signal is easy to interpret by CPU or other digital systems.

Despite advantages of the circuitry, disadvantage of the circuitry is the poor accuracy. The output frequency signal is determined by Iptat(so does Rptat), C1 and Vhyst. These determination factors are all prompt to be influenced by process variation.

The overall comparison result between other conversions will be discussed at 2.2.4.

2.2.2 Duty-cycle Modulation

Duty-cycle modulation which is a method that will not be affected by absolute value of determination factor will be introduced in this section. The basic measurement principle of the duty-cycle modulation can be shown as Fig.2.5

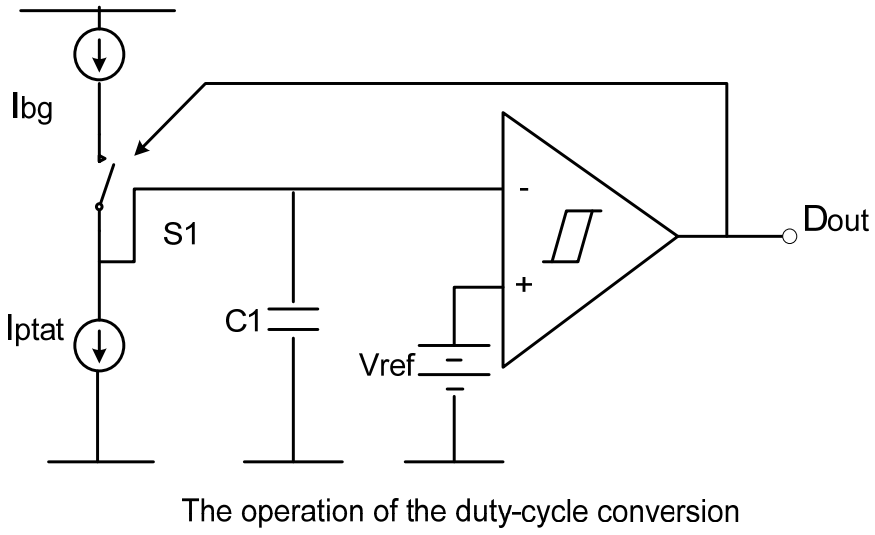


Fig.2.5 Simplified circuit architecture of duty-cycle modulation ADC

During a conversion period, as depicted in Fig.2.6, the bandgap current source Ibg charges C1 during T1 and the positive-to- absolute-temperature current source Iptat discharge C1 at the whole period T.

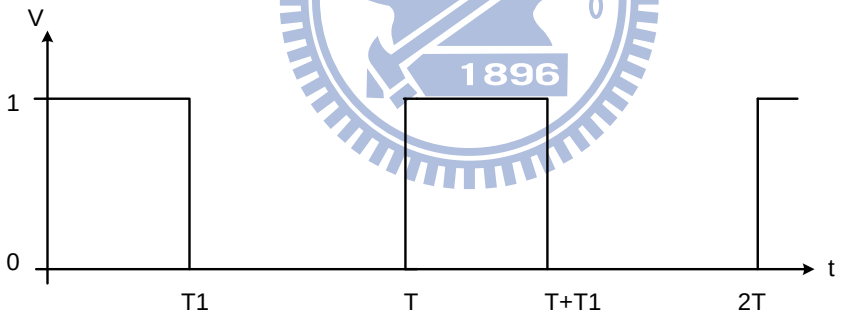


Fig.2.6 Conversion period of the duty-cycle modulation ADC

Since the charge on C1 at the end of each period is always the same for a constant temperature signal, the charged and discharged charge on C1 is equal during on period. Therefore, a derivation of the duty-cycle can be made:

$$T_1 \cdot I_{bg} = T \cdot I_{ptat} \tag{2.6}$$

Finally, the duty-cycle of the conversion can be calculated as:

$$D_{out} = \frac{T_1}{T} = \frac{I_{ptat}}{I_{bg}} \tag{2.7}$$

Since the ratio of Dout is positive to Iptat, It means that the temperature information can be interpreted by the duty-cycle of the ADC.

Process variation of Iptat and Ibg can be eliminated if both the current sources are derived from the same resistor. This is also the advantage of duty-cycle modulation ADC. Since the duty-cycle is not determined by absolute factors, higher accuracy can be obtained.

However, in realistic application, the duty-cycle clock may not synchronize with the system clock. Other circuitry is needed to overcome this problem. Therefore, the accuracy may be reduced.

2.2.3 Sigma-Delta Modulation

In incremental sigma-delta modulation, the temperature information can be converted to the digital word at the output of ADC. Here, the basic principle of the first order incremental sigma-delta ADC will be introduced and the architecture can be shown as Fig.2.7.

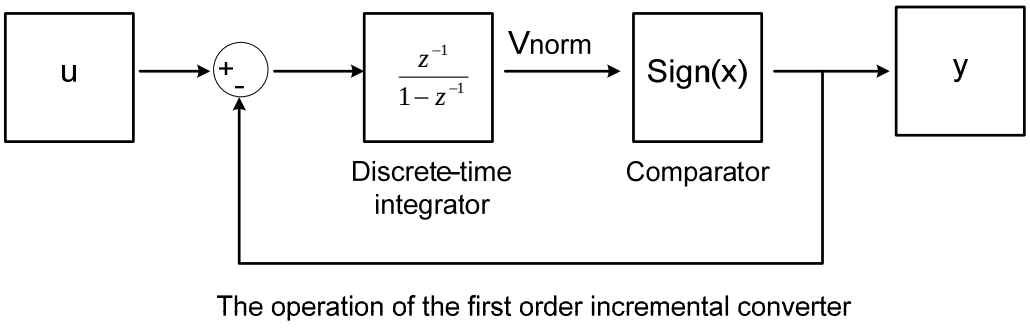


Fig.2.7 Simplified circuit architecture of incremental sigma-delta ADC

In Fig.2.7, all of the signals have been normalized to Vref. And we can derive that:

$$V_{norm}[n] = \sum_{i=0}^{n-1} (u[i] - y[i]) \tag{2.8}$$

With proper signal management, it can be ensured that $V_{norm} \in [1,-1]$. Next, in time step N, a derivation can be made that:

$$\left| \bar{u} - \frac{1}{N} \sum_{i=0}^{n-1} y[i] \right| \le \frac{1}{N} \tag{2.9}$$

where $\bar{u} = \overline{Vin} / Vref$

It shows that the error between the mean input value and $\frac{1}{N}\sum_{i=0}^{n-1} y[i]$ is bounded by $\frac{1}{N}$.

The digital output word can be defined as $Dout = \frac{1}{N}\sum_{i=0}^{n-1} y[i]$. And $\frac{1}{N}$ can be seen as the quantization error of the ADC. Thus, we can calculate that:

$$\frac{1}{N} = \frac{LSB}{2} = \frac{u_{\max}}{2^{nbit}} \tag{2.10}$$

$u_{\max}$ is the maximum normalized input voltage and $u_{\max} = 1$ in this case. Finally, we can derive that:

$$\frac{1}{N} = \frac{LSB}{2} = \frac{1}{2^{nbit}} \tag{2.11}$$

It means that to achieve n bit resolution, the ADC must operate through $N = 2^{nbit}$ cycles.

The advantage of sigma-delta modulation is that the output is determined by the ratio of capacitors, which eliminates process variation. Oversampling and Noise shaping techniques are also be utilized in sigma-delta modulation, higher accuracy can be obtained. The output digital word can be sent directly to the following digital systems or the outside word without other synchronization hardware.

However, as in eq.2.11, longer conversion cycle is needed for higher resolution requirement. In this situation, higher system frequency for adequate conversion time may occur. This does not meet the efficiency consideration. In other hand, lower conversion cycle is needed for the same resolution by using higher order architecture. Nevertheless, overloading situation may occur in higher order architecture without proper signal management.

After previous introductions of the commonly used conversion, comparison between them will be discussed in next section.

2.2.4 Comparison of Conversions

In this thesis, high accuracy requirement and better system integration for using deep-submicro process must be concerned. Here, classification of the previous conversions can be made by their sampling frequency, as depicted in Table 2.2.

Application	Architecture	
	Nyquist-rate ADC	Oversampling ADC
DC, sensor application and LF. measurement	Frequency conversion Duty-cycle modulation	Sigma-delta modulation

Table2.2 Classification list of the commonly used conversion in temperature sensing

Despite the simplicity of the two Nyquist-rate ones, there are limitations on high precision Nyquist-rate ADC design:

1. In deep-submicro CMOS process, it is hard to manufacture high precision passive analog element, such as resistor, that Nyquist-rate ADC relies so much.

2. Although there are methods to eliminate passive element variation for duty-cycle modulation, additional circuitry is needed to interpret the duty-cycle signal. Synchronization and locking problem may happen so the accuracy may be reduced.

3. Nyquist-rate ADC is easily suffered from the coupling interference of the high speed digital signal on system-on-chip (SOC) integrating environment. It means that the coupling noise suppression ability of Nyquist-rate ADC is worse when system integration is needed.

In contrast, oversampling-ADC has the following characteristics which make it suitable for such application.

1. The switch-capacitor architecture used in sigma-delta modulation is less sensitive to pulse-like switching noise coupled from digital part of the system due to the sample and hold characteristic.

2. Parameters in sigma-delta modulation are determined by capacitor-ratio in stead of the absolute value of it. Precise capacitor matching can be achieved by proper floorplan of layout.

3. Sigma-delta modulation utilizes the skill of oversampling and noise shaping. Therefore, higher SNR ratio can be achieved in signal band.

4. The digital output word of sigma-delta ADC can be used directly by the digital system without additional interpretation circuitry, which makes the system integration easier.

After comparison, the oversampling ADC is better for realization of high accuracy instrumentation application than the Nyquist-rate ones. Overloading situation of higher order sigma-delta architecture can be avoided by proper parameter chosen. Therefore, sigma-delta ADC is the chosen architecture for implementation in this thesis. The detailed analysis of the ADC in our application will be discussed in the following chapter.

Chapter 3

System Level Design Consideration

The design challenges and expectations of advanced all-CMOS smart temperature sensor will be discussed at this chapter. Next, power and energy consumption analysis will be followed, which describes system level design consideration of the sigma-delta ADC. Finally, discussion of non-idealities effects, such as finite OPAMP gain and thermal noise…, ends this chapter.

3.1 Design Challenges and System Specifications

In beginning, Contributions and challenges of designing advanced all-CMOS smart temperature sensor will be described at section 3.1.1. Next, specifications of the designed ADC will be introduced at section 3.1.2.

3.1.1 System Limitation and Design Issues

As described in section 2.2.4, the sigma-delta modulation has the best trade-off between accuracy, simplicity and circuit integration. So far, the smart temperature sensor with the best performance has also been implemented in sigma-delta modulation [6]. Table3.1 lists the performance of smart temperature sensors with sigma-delta modulation in recent researches [2] ~ [7].

Reference	Process	Range	Inaccuracy	Supply voltage	Power	ADC resolution	area
JSSC, 1996[2]	0.7um CMOS	-40°C ~120°C	$\pm 1.0°C$	2.2V~ 5.0V	55uW~ 125uW	8bits, first order SDM	$1.5mm^2$
JSSC, 1998[3]	0.6um CMOS	-50°C ~125°C	$\pm 1.5°C$	2.7V~ 5.5V	3.3mW~ 6.8mW	10bits, SAR ADC	$3.3mm^2$
ESSCIRC, 1999[4]	0.7um CMOS	-40°C ~127°C	$\pm 1.0°C$	3V~ 5.5V	300uW~ 550uW	10bits, first order CTSDM	$3.0mm^2$
JSSC, 2005[5]	0.5um CMOS	-50°C ~125°C	$\pm 0.5°C$	2.7V~ 5.5V	350uW~ 750uW	15.5bits, second order SDM	$2.5mm^2$
JSSC, 2005[6]	0.7um CMOS	-55°C ~125°C	$\pm 0.1°C$	2.5V~ 5.5V	187uW~ 412uW	16bist, second order SDM	$4.5mm^2$
ISCAS 2006[7]	0.25um TSMC	-55°C ~125°C	$\pm 1.0°C$	1.8V~ 3.3V	300uW~ 2.2mw	9bits,SDM	$1.0mm^2$

Table 3.1 Summary of researches of sigma-delta modulation smart temperature sensors

From table 3.1, it is clear that the temperature sensing range is wider, -55°C ~ 125°C sensing range is achieved, and the temperature inaccuracy is lower, $\pm 0.1°C$ inaccuracy is accomplished.

Despite the improvements in sensing range and inaccuracy, large semiconductor process is still used without corresponding process reducing. It will limit the integration between smart sensor and related systems in deep-submicro process, which have been a commonly used process in many industrial products. Therefore, an advanced all-CMOS smart temperature sensor, which can easily be implemented in deep-submicro process, is the design goal and contribution.

However, there are design challenges for deep-submicro all-CMOS smart temperature sensor design:

a. BJT element, which is commonly used for designing front-end sensing device, cannot be used for its poor parasitic performance in deep-submicro process.

b. In this situation, MOS element must be used for designing instead of the BJT element. However, high linearity MOS temperature sensing device is hard to design in deep-submicro process.

c. Due to the lower supply voltage in deep-submicro process, the design of high resolution back-end analog-to-digital electrical interface is difficult.

For the design challenges, a high linearity CMOS PTAT and reference generator has been designed in deep-submicro process and published at 2006 [8] by our design group as the solution for challenge a and b. Therefore, the topic of this thesis is to design a low power and energy consumption back-end A/D conversion circuit for the all-CMOS smart temperature sensor system.

3.1.2 ADC Design Concept and Specifications

In this project, two main specifications of the ADC can be determined:

a. Resolution Consideration:

The application temperature sensing range is from -55°C to 125°C and the temperature inaccuracy is set to ± 0.1°C for biomedical application and wide range environment measurement. The required resolution of the ADC can be calculated as:

$$2^{bit} > \frac{125-(-55)}{0.1} = 2^{10.81} \approx 2^{11} \tag{3.1}$$

It means that at least 11bits resolution is needed for the ADC

b. Signal Bandwidth Consideration:

In this application, the measured temperature signal can be seen unchanged during the whole process of conversion. Therefore, the signal bandwidth of the sigma-delta ADC is dc.

The other specifications such as sampling frequency and conversion time will be discussed detailed after selection of ADC architecture. Hence, only resolution and bandwidth specification is presented here. Next, there are design concepts of ADC in our application which make it suitable for temperature sensing applicaiton.

Here, the designed ADC must have the following characteristics:

a. Low-power and low-energy consumption must be concerned. It means that power and energy consumption must be minimized with the prerequisite of sufficient accuracy.
b. In this application, “one shot” type operation is needed. The ADC has to work normally when it needs to convert the temperature signal while power down after temperature conversion for power saving.

For the reasons, proper ADC architecture which is suitable for low-voltage and low-power consumption must be concerned and analyzed. Detailed discussion will be arranged at section 3.2.

3.2 Architecture Selection of Sigma-delta ADC

This section will discuss the architecture used in our designed Sigma-delta ADC. Proper circuit topology which is suitable for low-voltage and low-power sigma-delta modulator will be introduced. Followed by architecture selection of digital filters, two different types of digital filter will be discussed and compared.

3.2.1 Architecture Selection of Sigma-delta Modulator

From section2.2.3 and section2.2.4, we know that longer conversion cycle is needed for first order sigma-delta modulation with higher resolution. Thus, it may occur that the sampling frequency is much higher than system conversion time. Therefore, the conversion efficiency of first order sigma-delta modulation is lower and it is not suitable for higher resolution application. In practice, higher order architecture of sigma-delta modulation will be used to overcome this problem.

However, we know that there are several architectures of higher order sigma-delta modulator. Here, proper architecture which is suitable for low-voltage operation and low-power consumption must be analyzed.

The most general topology of sigma-delta modulator is the Cascade-Integrator with Feed-Back path (CIFB) architecture. Here, a second order CIFB sigma-delta modulator, as in Fig.3.1, will be discussed:

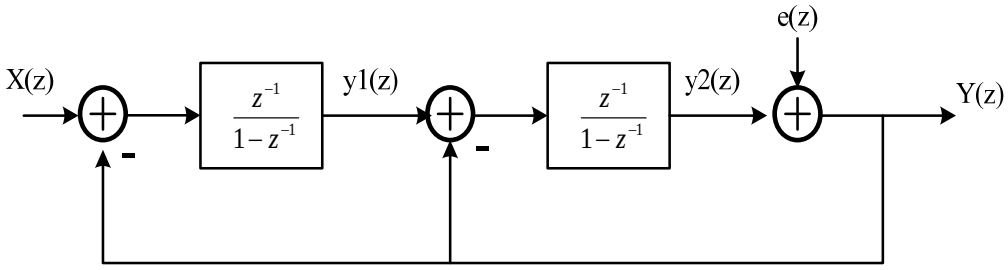


Fig.3.1 Architecture of second order CIFB sigma-delta modulator

The transfer function of this modulator can be derived as:

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 e(z) \tag{3.2}$$

Where the signal transfer function (STF) and noise transfer function (NTF) can be given by:

$$STF = z^{-2} \quad \text{and} \quad NTF = \left(1 - z^{-1}\right)^2$$

Next, the output of both integrators y1 and y2 can be presented as:

$$y1(z) = z^{-1}(1 - z^{-1})X(z) - z^{-1}(1 - z^{-1})e(z) \tag{3.3}$$

$$y2(z) = z^{-2}X(z) - z^{-1}(1 - z^{-1})e(z) \tag{3.4}$$

From eq.3.3 and eq.3.4, we know that both the output of the integrators is function of $X(z)$. It means that the output of the integrator will relate to input signal. In the situation, it can be observed that:

a. If the input signal is large, larger output amplitude may occur since the output is function of input. Next, higher slewing requirement is needed to the OPAMP, which is the critical element of integrator. Next, much power consumption is needed for CIFB sigma-delta modulator which makes it not suitable for low-power concerned application.

b. In temperature sensing application, wider stable input range is needed for wider sensing range. Nevertheless, overloading situation may easily occur in CIFB architecture sigma-delta modulator because it's larger amplitude at output of the integrator. It means that wide sensing range requirement is hard to be achieved by using CIFB architecture.

Due to the nature restriction of CIFB architecture, the other topology which is called the Cascade-Integrator with Feed-Forward path (CIFF) architecture sigma-delta modulator will be introduced [9]. The architecture of a second order CIFF architecture can be shown as Fig.3.2:

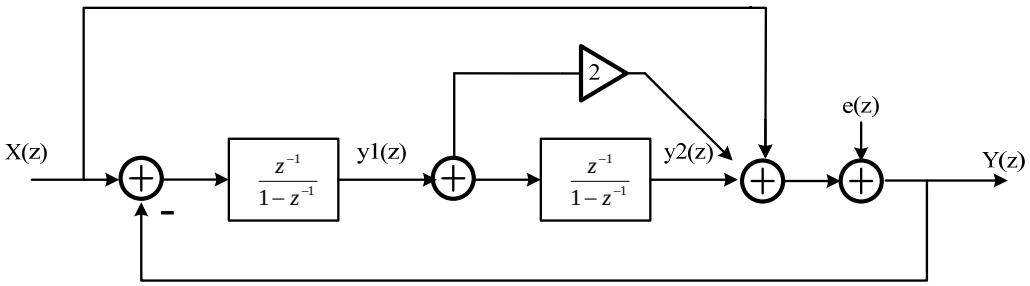


Fig.3.2 Architecture of second order CIFF sigma-delta modulator

Similarly, the transfer function of the CIFF modulator can be depicted as:

$$Y(z) = X(z) + (1 - z^{-1})^2 e(z) \tag{3.5}$$

where the signal transfer function (STF) and noise transfer function (NTF) is given by:

$$STF = 1 \quad \text{and} \quad NTF = \left(1 - z^{-1}\right)^2$$

The transfer function of integrator outputs y1 and y2 can be derived as:

$$y1(z) = -z^{-1}(1 - z^{-1})e(z) \tag{3.6}$$

$$y2(z) = z^{-2}e(z) \tag{3.7}$$

From eq.3.6 and eq.3.7, it can be observed that the integrator output does not contain input signal $X(z)$. After comparison between CIFB architecture, we can find that:

a. Since the integrator output contains only quantization error $e(Z)$, which is usually a smaller signal when comparing to $X(Z)$, lower amplitude at output of integrator can be achieved. Next, it can relax the slewing requirement of integrator. Hence, the power consumption of the modulator can be reduced.

b. Due to its lower output amplitude at integrator, this makes it suitable for low-voltage operation. Next, occurrence of overloading situation will also reduce. Wider stable input range can be achieved which makes it proper in sensing application.

c. Non-linearity and distortion effects can greatly be reduced because the loop filter does not process the input signals. Better performance of the modulator can be made.

From previous discussion, the Casacde-Integrator with Feed-Forward path (CIFF) architecture sigma-delta modulator is better for circuit implementation than the Cascade-Integrator with Feed-Back path (CIFB) one in our application. Therefore, the CIFF architecture will be used for the topology of sigma-delta modulator in this designed thesis.

3.2.2 Architecture Selection of Digital Filter

After the architecture selection of sigma-delta modulator, a proper digital filter which demodulates the bit-stream of sigma-delta modulator is the following

concerned issue. Here, there are two commonly used filter architecture in sensing application [10] ~ [12]. Discussion and comparison of the two architectures will be followed.

The first one is the Cascade-Integrators (CI) digital filter. The principle of a second order CIFF modulator with second order CI filter, as shown in Fig.3.3, will be discussed.

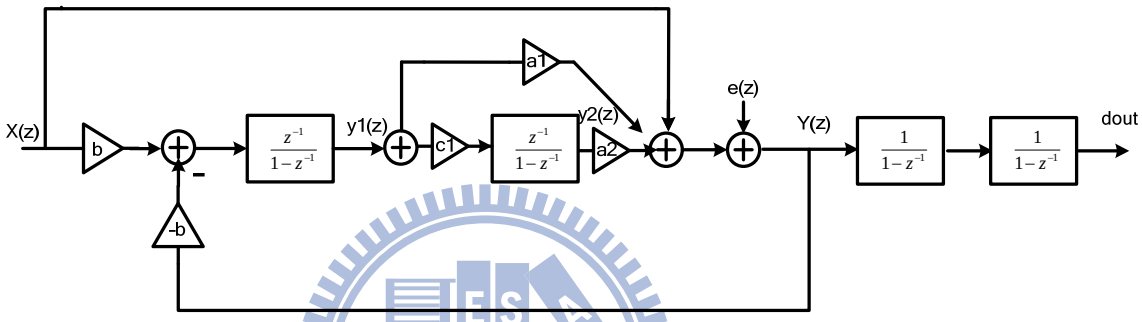


Fig.3.3 Architecture of second order CIFF modulator with second order CI digital filter

From Fig.3.3, the output of the first integrator V_{i1} in time step n can be derived:

$$\begin{aligned} &V_{i1}[0] = 0 \\ &V_{i1}[1] = b\left(Vin[0] - d_0 V_{ref}\right) \\ &.... \\ &V_{i1}[n] = b\sum_{k=0}^{n-1}\left(V_{in}[k] - d_k V_{ref}\right) \end{aligned} \tag{3.8}$$

where $d_k = \pm 1$ is the output of comparator at time step k

Similarly, the output of the second integrator V_{i2} in time step n can be calculated:

$$\begin{aligned} &V_{i2}[0] = 0 \\ &V_{i2}[1] = c1V_{i1}[0] + V_{i2}[0] = 0 \\ &V_{i2}[2] = c1V_{i1}[1] + V_{i2}[1] = c1\left(V_{i1}[1] + V_{i1}[0]\right) \\ &V_{i2}[n] = c1\sum_{l=0}^{n-1} V_{i1}[l] = c1b\sum_{l=0}^{n-1}\sum_{k=0}^{l-1}\left(V_{in}[k] - d_k V_{ref}\right) \end{aligned} \tag{3.9}$$

With proper signal management, we can make sure that $|v_{i2}| \le V_{ref}$. Next, we can derive that:

$$-\frac{2!}{(n-1)n}\frac{1}{c1b}V_{ref} < V_{in} - \frac{2!}{(n-1)n}V_{ref}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}d_k < +\frac{2!}{(n-1)n}\frac{1}{c1b}V_{ref} \tag{3.10}$$

Here, the output of the Cascade-Integrators (CI) output, which is the corresponding digital value of V_{in}, can be defined as:

$$dout = \frac{\hat{V}_{in}}{V_{ref}} = \frac{2!}{(n-1)n}\sum_{l=0}^{m-1}\sum_{k=0}^{l-1}d_k \tag{3.11}$$

Therefore, the quantization error can be depicted as:

$$\frac{1}{2^{nbit}} = \frac{2!}{(n-1)n}\frac{1}{c1b} = \frac{V_{LSB}}{2} \tag{3.12}$$

Finally, we can calculate that the needed conversion cycle n for $nbit$ resolution:

$$n_{bit} = \log_2(c1b\frac{(n-1)n}{2!}) \approx 2\log_2(n) + \log_2(c1b) - 1 \tag{3.13}$$

From eq.2.11, we can calculate the conversion cycle needed for 11bits resolution of a first order sigma-delta ADC is $n_{1st} = 2^{11} = 2048$. However, if we set $b = c1 = 1$ for fast calculation of the same resolution, the conversion cycle for second order CIFF modulator with second order CI filter is $n_{2nd} \approx 2^{\frac{11+1}{2}} = 64$. It can be found that the conversion cycle can greatly reduce for using higher order architecture, hence increase the conversion efficiency.

The second architecture is the SINC digital filter [10] ~ [12]. Recent researches reveal that the combination of n-th order modulator and (n+1)-th order SINC filter has the best trade-off between performance and circuit complexity. Here, a second order CIFF modulator with a third order SINC filter, as in Fig.3.4, will be discussed:

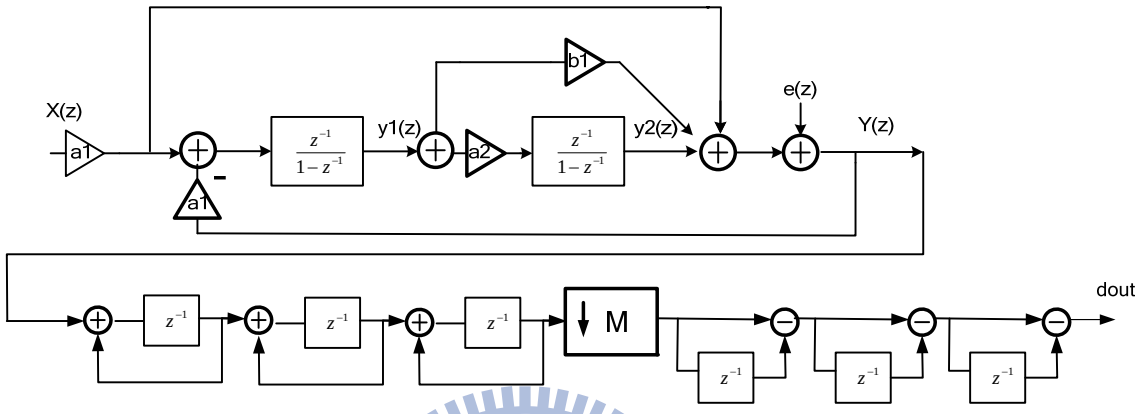


Fig.3.4 Architecture of second order CIFF modulator with third order SINC digital filter

First, the transfer function of the general front-end CIFF modulator can be derived as:

$$Y(z) = STF \cdot U(z) + NTF \cdot E(z) = U(z) + \frac{(1-z^{-1})^2}{D(z)} E(z) \qquad (3.14)$$

$$\text{where } D(z) = 1 - (2 - a1b1)z^{-1} + (a1a2 - a1b1 + 1)z^{-2}$$

Next, the transfer function of the third order SINC filter is:

$$H(z) = \frac{1}{M^3}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^3 \qquad (3.15)$$

where M is the down-sampling ratio

Finally, the transfer function of the whole ADC can be derived as:

$$
\begin{aligned}
d_{out} &= \frac{1}{M^3}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^3 \cdot Y(z) \\
&= \frac{1}{M^3}\left(\frac{1-z^{-N}}{1-z^{-1}}\right)^3 \cdot U(z) + \frac{1}{M^3}\frac{(1-z^{-M})^3}{(1-z^{-1})} \cdot \frac{1}{D(z)} \cdot e(z) \\
&= \overline{U}(z) + Q(z)
\end{aligned}
\tag{3.16}
$$

Here, $\overline{U}(z)$ is the output of the ADC and $Q(z)$ is the corresponding quantization error of the whole system. We can calculate the OSR needed of the ADC for quantization error $Q(z) \le \frac{LSB}{2} = \frac{1}{2 \cdot 2^{nbit}}$:

$$
OSR \ge \sqrt[2.5]{\frac{2^{n+1} \cdot \sqrt{6}}{a1 \cdot a2 \cdot U_{\max}} \sqrt{\frac{\left(\sum_{i=1}^{m} w_d[i]\right)^2}{\sum_{i=1}^{m} w_d[i]}}}
\tag{3.17}
$$

where w_d is the impulse response of $\frac{1}{D(z)}$ and $U_{\max}$ is the maximum allowable input value

If we set $a1 = a2 = 1$ for fast calculation of the same resolution, the OSR for second order CIFF modulator with third order SINC filter is $OSR = 128$. For third order SINC filter, minimum conversion cycle n needed is $n = 3 \cdot OSR = 3 \cdot 128 = 384$. Increasing of conversion efficiency can also be achieved in this architecture.

After discussion, we know that both the architecture of digital filter can be used for this application. In practice, the CIFF modulator with CI filter architecture can simply be implemented. In other hand, it is harder to implement the CIFF modulator with SINC filter one. However, if the low frequency noise that come from power

line is considered, only the SINC filter architecture can suppress the ac line noise instead of the CI one. In this accuracy concerned thesis, the noise that may cause performance reduction should be cared. Therefore, the SINC filter is the chosen one for circuit implementation. The n-th order CIFF modulator with (n+1)-th order SINC filter will be used in the following section of this thesis.

3.3 System Parameter Consideration

In this section, power and energy consumption issues will be considered. For previous section, we know that high order sigma-delta ADC architecture can indeed increase the conversion frequency. Correspondingly, power consumption may be higher since much number of integrators is used. Therefore, a fast analysis and estimation must be done for sigma-delta ADC order choosing for getting a best trade-off between power, accuracy, area and circuit-stability.

3.3.1 Coefficient Selection of the second order CIFF Modulator

From previous section, the second order architecture CIFF modulator with third order SINC filter is decided. In this section, coefficient selection of the second order modulation will be discussed for power consumption consideration.

First, a general second order CIFF sigma-delta modulator can be shown as Fig.3.5

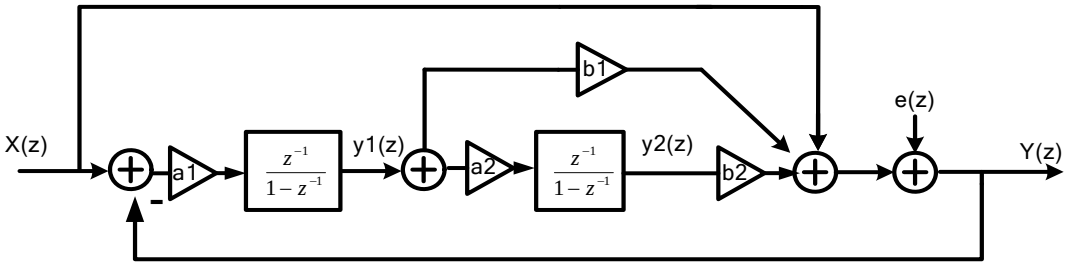


Fig.3.5 General architecture of second order CIFF sigma-delta modulator

Four tunable coefficients can be found, which are two integrator gain factor (a1, a2) and two summation factor (b1, b2). The transfer function of the general second order CIFF sigma-delta modulator can be derived as:

$$Y(z) = X(z) + \frac{\left(1 - z^{-1}\right)^2}{1 + (a1b1 - 2)z^{-1} + (a1a2b2 - a1b1 + 1)z^{-2}} e(z) \tag{3.18}$$

The STF and NTF are given by:

$$STF = 1 \quad \text{and} \quad NTF = \frac{\left(1 - z^{-1}\right)^2}{1 + (a1b1 - 2)z^{-1} + (a1a2b2 - a1b1 + 1)z^{-2}}$$

Next, by using the sigma-delta toolbox [12], NTF with optimized noise attenuation can be calculated. It can be shown as:

$$NTF_{opt}(Z) = \frac{(z-1)^2}{z^2 - 1.225z + 0.4415} \tag{3.19}$$

After comparison of eq.3.18 and eq.3.19, it can be observed that:

$$a1b1 = 0.775 \tag{3.20}$$

$$a1a2b2 = 0.2165 \tag{3.21}$$

In this power concerned project, lower power consumption can be achieved by reducing the output swing of the integrator (reduce the integrator gain factor a1, a2), as shown in Fig.3.6. If the output swing of the integrator can be smaller, relaxing slewing behavior can also be achieved, which reduces the power consumption of the integrator [14].

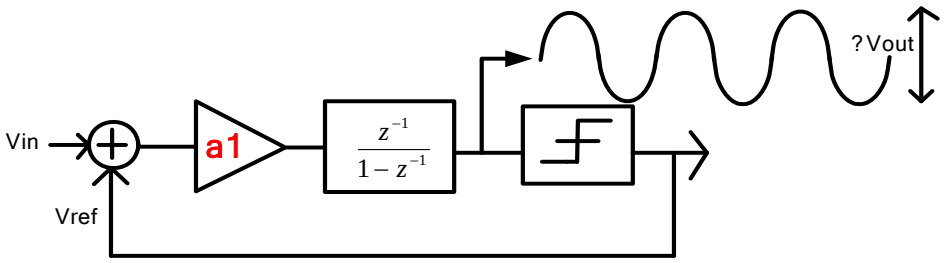


Fig.3.6 Simplified model between gain factor and integrator output amplitude

However, the smaller the integrator gain, the bigger the summation factor and that will cause the overloading situation. After simulations by matlab simulink [12], we choose a1=0.25 and b1=3 for the above requirement, signal scaling and capacitor matching. The coefficients of the CIFF modulator can be listed at Table 3.6.

Integrator Coefficients	Feed-Forward Coefficients
a1=0.25	b1=3
a2=1	b2=1

Table 3.2 Coefficients table of the designed CIFF sigma-delta modulator

Next, the modified NTF with the choosing parameter becomes:

$$NTF_{\mathrm{mod}}(Z) = \frac{(z-1)^2}{z^2 - 1.25z + 0.5} \tag{3.22}$$

The SNR of the modulator will not degrade significantly with slightly change the poles of the NTF.

With the above parameter, the OSR needed for the second order modulator can be calculated by eq.3.17 with $a1 = 0.25$, $a2 = 1$ and $U_{\max} = 1.4/1.8$. It can be calculated that the require OSR is:

$$OSR \geq 301 \tag{3.23}$$

Finally, an approximation of OSR is made in power of 2 for the convenience of clock synthesis in digital part. Therefore, the OSR for implementation in this thesis is:

$$OSR = 512 \tag{3.24}$$

Next, the sampling frequency for the dc-like system can be derived as [10]:

$$OSR = \frac{f_s}{2 \cdot f_B} = \frac{f_s}{f_n} \tag{3.25}$$

The frequency f_n, which will be designed for power line noise suppression, is the first notch frequency of the SINC filter. In this project, $f_n = 60Hz$ is chosen for the ac noise of Taiwan's power line. After calculation, the sampling frequency can be calculated as:

$$f_s = 60 \cdot 512 = 30.72 \times 10^3 \tag{3.26}$$

Next, the minimum conversion cycle needed for the SINC filter can be calculated as:

$$n = L \cdot OSR = 3 \cdot 512 = 1536 \tag{3.27}$$

Therefore, the conversion time needed for each temperature conversion is:

$$t_c(\text{conversion time}) = N \cdot f_s^{-1} = 1536 \cdot 1/30.72k = 50 \times 10^{-3} \tag{3.28}$$

3.3.2 Analysis of Power and Energy Issues

From eq.3.17, we can quickly calculate the needed $OSR = 512$ for the parameter in 3.3.1. Similar analysis can be made for third CIFF modulator with fourth order SINC filter and the needed $OSR = 256$.

In a sigma-delta ADC, the OPAMP dominates the power consumption of sigma-delta ADC and the Dynamic power consumption of registers dominates the power consumption of SINC filter. Therefore, the following analysis will focus on the two blocks and finally extended to the whole ADC.

a. power consumption of the sigma-delta modulator

As declare previously, the power consumption of the sigma-delta modulator is dominated by the OPAMP in the integrator. Next, we know that the power consumption of the OPAMP is proportional to its slewing behavior (power is proportional to $f_{samp}*C_{load}$).

Finally, the analysis result can be listed as Table 3.2: (X is the power needed for the first OPAMP of second order modulator)

modulator Order	**OSR for target resolution**	**Power Consumption**			
		1st OP	2nd OP	3rd OP	**Total**
2	512	X	0.3X	N/A	**1.3X**
3	256	0.5X	0.45X	0.4X	**1.35X**

Table 3.3 Power comparison table of second and third order modulators

b. Power consumption of the SINC filter

The power consumption of the filter is accordance with the dynamic power consumption of registers. Here, the capacitor loading is proportional to the length of

register. Recent research reveals that the minimum length of register needed without overflow for the filter is $B_{\min} = L \cdot \log_2 OSR + 1$[13]. Here, L is the order of the filter.

The analysis result can be listed as Table 3.3: (Y is the power needed for the third order SINC filter)

Filter Order	OSR for target resolution	Register Number	Power Consumption
3	512	28*3	**Y**
4	256	33*4	**0.78Y**

Table 3.4 Power comparison table of third and fourth order SINC filters

c. Energy consumption of the whole ADC for each temperature conversion

Since the system will enter sleep mode for power saving after each conversion, the energy consumption, instead of the power consumption, is the most important element for the performance of ADC. In the situation, longer conversion time is needed for higher order architecture. Finally, the analysis result can be listed as Table 3.4:

architecture	Modulator power	Filter power	Conversion Time	Energy Consumption
				Total
Mod2+Dig3	1.3X	Y	512*3*1/512	**3.9X+3Y**
Mod3+Dig4	1.35X	0.78Y	256*4*1/256	**5.4X+3.12Y**

Table 3.5 Energy consumption comparison table of ADCs

d. area and stability consideration

Here, assumptions is made that the area needed is dominated by the length of register in the digital part and the area of capacitor in the analog part. On the other hand, the stability can be determined by the order of the modulator. The simulation result can be made, as in Table 3.5: (A1 is the area needed of second order modulator, A2 is the area needed of third order SINC filter)

architecture	Circuit Stability	Chip Area
Mod2+Dig3	Better	A1+A2
Mod3+Dig4	Worse	2. 1A1+1.6A2

Table 3.6 Stability and area comparison table of ADCs

From Table 3.5, it can be found that the second order CIFF modulator with third order SINC filter has advantages both on area and stability than the other one.

After the analysis, second order sigma delta modulator with third order SINC filter will be chosen for circuit implementation in this thesis.

3.4 Non-idealities Consideration

Ideal circuit model and analysis has been made at previous sections. However, there are some non-ideal effects that may reduce the performance in realistic circuit implementation. These unavoidable effects can not be ignored and must be concerned. In this section, the analysis of the non-idealities will be made for achieving our requiring specification.

3.4.1 Effect of Finite OPAMP Gain

Finite gain effect of the OPAMP will affect the noise-transfer-function (NTF) of sigma-delta modulator, which also reduces the performance of the whole ADC. This section will discuss the effect of finite OPAMP gain and make fast gain requirement estimation for achieving system specification.

The architecture of a single-ended integrator can be shown as Fig.3.7.

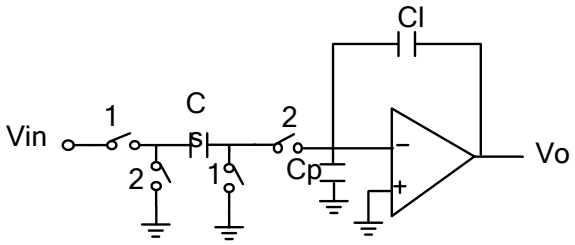


Fig.3.7 Circuit architecture of a single-ended integrator

The ideal transfer function of the integrator can be derived by assuming infinite gain of OPAMP. It can be depicted as:

$$H(z) = g \cdot \frac{z^{-1}}{1 - \alpha \cdot z^{-1}} \tag{3.31}$$

However, the OPAMP gain cannot be infinite in realistic implementation. In this situation, the transfer function will become:

$$H(z) = k_s \cdot \left(1 - \frac{1 + k_s + k_p}{A_0}\right) \cdot \frac{z^{-1}}{1 - \left(1 - \frac{k_s + k_p}{A_0}\right) \cdot z^{-1}} \tag{3.32}$$

where $k_s = C_s / C_I$ and $k_p = C_p / C_I$

To the sigma-delta modulator, the finite gain of OPAMP will slightly change the position of pole of NTF from unit circle. When the distance of the zero exceed about $\frac{\pi}{OSR} \cdot \frac{C_I}{C_S}$, the noise attenuation of NTF begins to degrade. After analysis, we can find that the degradation of NTF can be accepted when the gain of OPAMP $A_0 \geq OSR$. However, this is only a rough estimation of finite gain [15].

Further analysis can be made by Matlab toolbox. The finite gain effect model can be established into the sigma-delta modulator model, for more precision estimation [16]. The simulation result of a ramp input is show Fig.3.9.

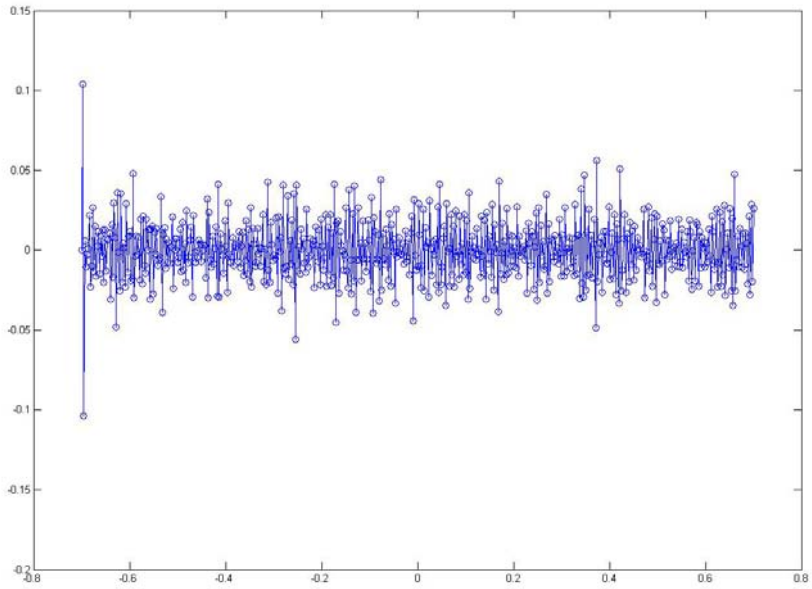


Fig 3.8 Output of the ADC for a ramp input (infinite OPAMP gain)

The X axis is the input voltage and Y axis is the quantization error (LSB). Here, the $V_{LSB} = \frac{2 \cdot V_{ref}}{2^{bit}} = \frac{2 \cdot 1.8}{2^{14}}$.

Next, the simulation result in finite gain situation will show:

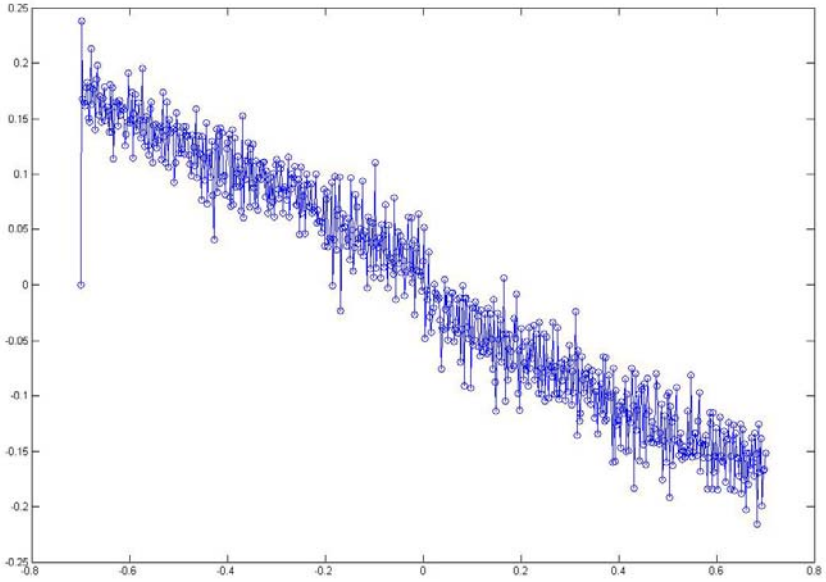


Fig.3.9 output of the ADC (40dB gain at first OPAMP and 40dB gain at second OPAMP)

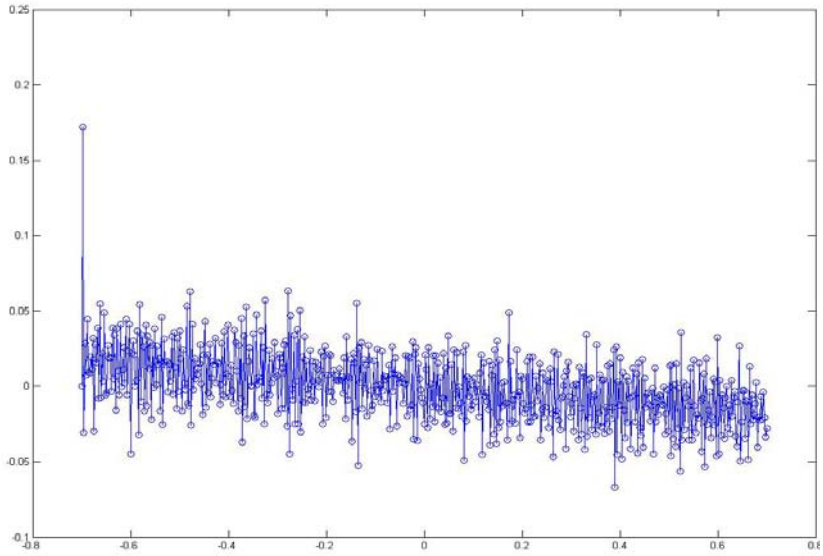


Fig.3.10 output of the ADC (60dB gain at first OPAMP and 40dB gain at second OPAMP)

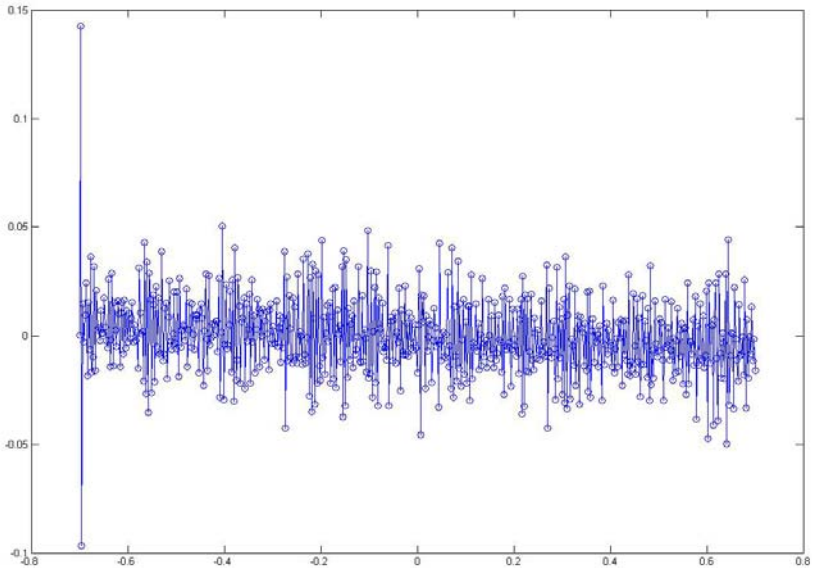


Fig.3.11 output of the ADC (60dB gain at first OPAMP and 60dB gain at second OPAMP)

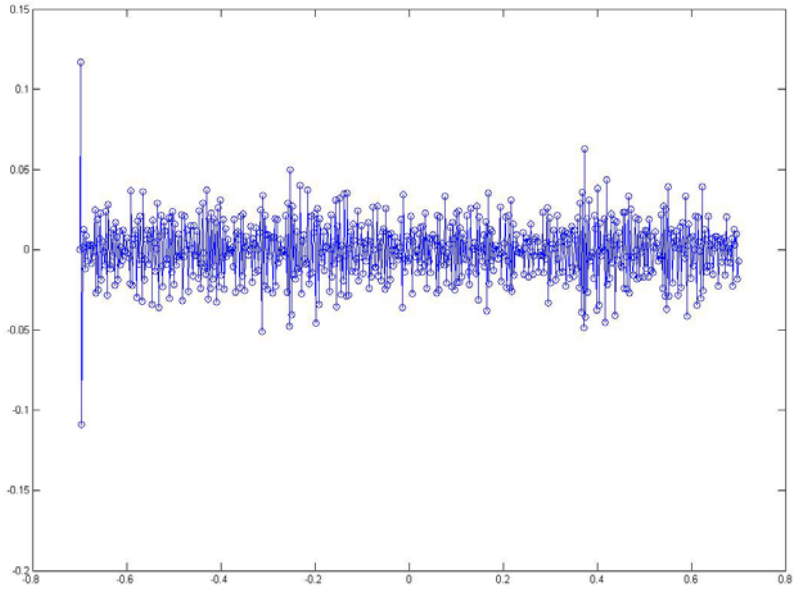


Fig.3.12 output of the ADC (80dB gain at first OPAMP and 80dB gain at second OPAMP)

The effects of finite gain can be observed from above simulation results. After simulation comparison, we chose 80dB gain at first OPAMP and 80dB gain at second OPAMP for a safe design margin.

3.4.2 Thermal Noise and Capacitor Sizing

In analog circuits, the thermal noise that comes from the passive and active elements will affect the whole performance. To sigma-delta modulator, the effect caused by thermal noise at the first integrator is most critical one. The architecture of the first integrator can be shown as Fig. 3.13.

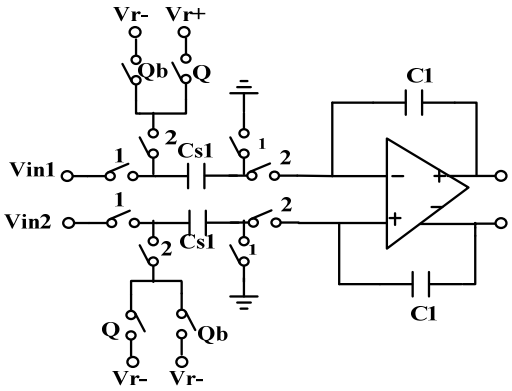


Fig. 3.13 Circuit architecture of the first integrator in sigma-delta modulator

The thermal noise caused by sampling capacitor and the OPAMP can be derived [15]:

$$v_{th} \approx \frac{4kT}{C_{s1}} \tag{3.29}$$

where k is the Boltzmann constant and T is the absolute temperature

Due to the oversampling characteristic, the noise in signal-band will become:

$$v_{th}' \approx \frac{v_{th}}{OSR} \tag{3.30}$$

For full scale input amplitude, the in-band noise must be attenuate 92dB, which is a conservative over-design in resolution specification, below the signal power. So we can calculate that:

$$\begin{aligned} v'_{th} &= \frac{v_{th}}{OSR} \le 10^{-9.2} \cdot (\frac{V_{DD}}{2})^2 \cdot \frac{1}{2} \\ \Rightarrow C_{s1} &\ge \frac{4kT}{10^{-9.2} \cdot (\frac{V_{DD}}{2})^2 \cdot \frac{1}{2} \cdot OSR} = 17.4246 \times 10^{-14} = 174.246(fF) \end{aligned} \tag{3.31}$$

Finally, $C_{s1} = 200\,fF$ is set for realistic implementation.

Here, simulation by Matlab Simulink [17] model can also be done, the established model can be shown as Fig.3.14:

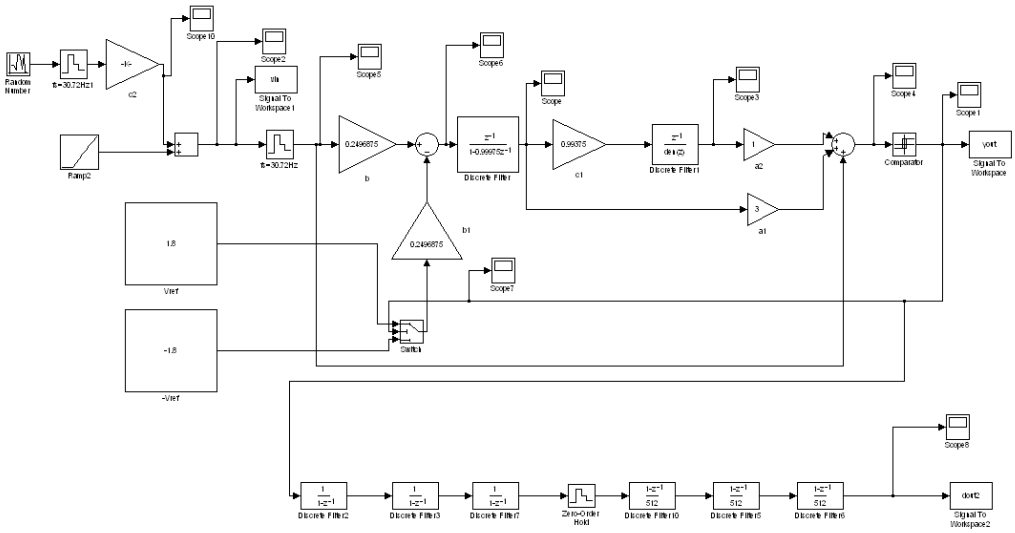


Fig.3.14 Matlab Simulink model of the designed sigma-delta ADC

The simulation result of a ramp input for infinite OPAMP gain can be shown as Fig.3.15:

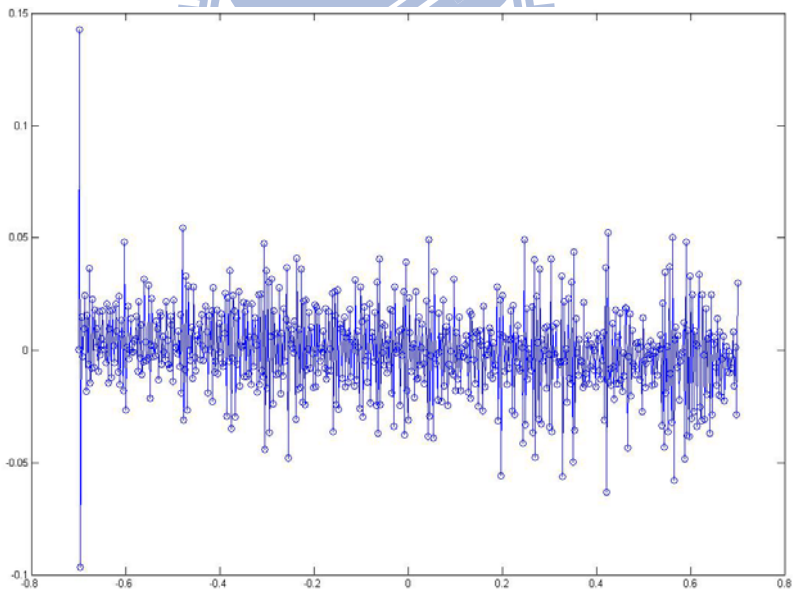


Fig.3.15 output of the ADC (for $C_{s1} = 200\,fF$ and with finite OPAMP gain)

3.4.3 Settling Behavior of OPAMP

To a switch-capacitor (SC) circuit, the settling behavior can be classified into two steps. The first step is called sampling and the second part is called integration,

as shown in Fig.3.16.

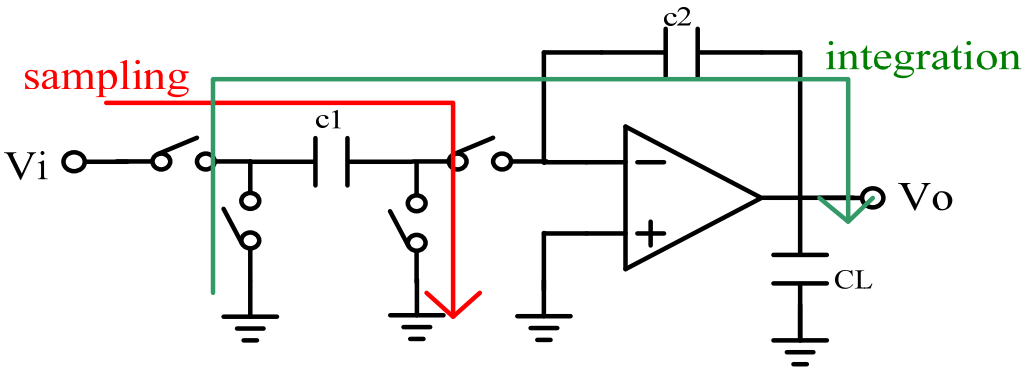


Figure 3.16 Sampling and integration period of a loop filter

The settling behavior can be shown as Fig.3.17. Slewing situation happen when a large input signal enters the loop and the OPAMP will charge the loading linearly. Next, when the differential input voltage is less than $\sqrt{2}V_{OV}$, the OPAMP will enter settling region and it will charge the loading exponentially.

Since there are bandwidth limitations in OPAMP, settling error will occur at the end of integration period. Therefore, analysis of settling behavior must be made when designing the OPAMP for performance consideration.

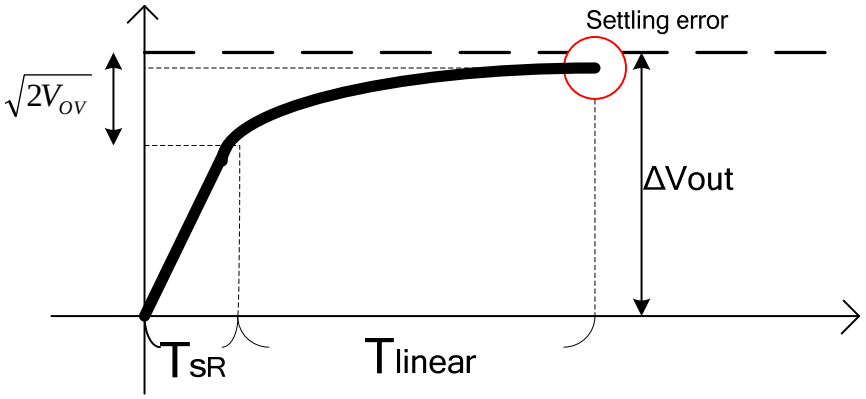


Figure 3.17 Settling behavior of OPAMP

In previous section, the non-ideal effects, which include finite OPAMP gain, thermal noise and settling behavior, has been presented. The detailed transistor level design will be discussed in next chapter.

Chapter 4

Circuit Implementation

In this chapter, sub-circuits designed for the sigma-delta modulator which includes a folded-cascode OPAMP, a mode-controllable bias circuit, a non-overlapped clock generator and 1bit quantizer will be introduced at beginning. After modulation introduction, the design of the SINC filter will be presented. Next, layout level design will be followed. Finally, system simulation and comparison with related research ends this chapter.

4.1 Design of the Sigma-delta modulator

From the discussion of section 3.3.1, a second order sigma-delta modulator is needed for this thesis. The designed fully differential sigma-delta modulator can be shown as Fig.4.1.

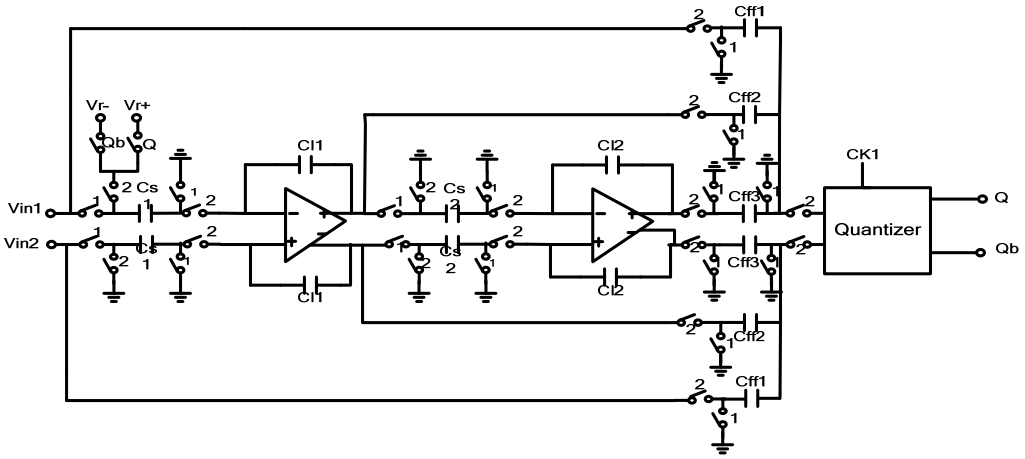


Fig.4.1 Architecture of the designed second order sigma-delta modulator

The CDS technique and dynamic CMFB circuitry is eliminated for easier representation. The detailed sub-circuits used will be discussed at the following section. The designed folded-cascode OPAMP and a mode-controllable BIAS circuit which control the working mode of the whole modulator will be first. Next, integrator with correlated double sampling (CDS) technique will be introduced for offset and low-frequency noise cancellation. Finally, discussion of non-overlapped clock generator, 1-bit quantizer and the common-mode feedback circuit will be arranged.

4.1.1 The Designed Folded-Cascode OPAMP in Sigma-delta Modulator

As discussed in section 3.4, there are non-idealities that affect performance of the ADC. From section 3.4.1, the gain requirement of the OPAMP can be determined preliminary.

Next, the architecture of OPAMP must be decided for further analysis. The conventional OPAMPs, which is two-stage OPAMP, folded-cascode OPAMP and telescope OPAMP, are candidates in our thesis. After comparison, the folded-cascode OPAMP can reduce the compensation capacitor when comparing to the two-stage OPAMP and has higher output swing can be achieved when comparing to the telescope OPAMP for the same gain requirement. Therefore, the conventional folded-cascode OPAMP is chosen for the implementation architecture in this thesis.

The architecture of the folded-cascode OPAMP is shown as Fig.4.1.

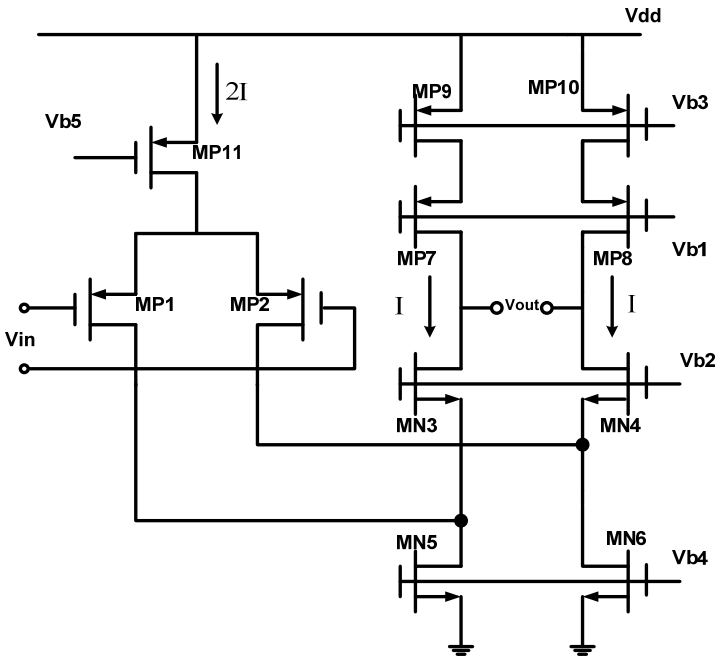


Fig.4.2 Architecture of the folded-cascode OPAMP

Next, the slewing behavior and settling behavior will be considered separately as discussed in section 3.4.3:

First, the slewing behavior will be considered. The slewing behavior will determine the output current of the OPAMP. From Fig.4.2, we can analyze the slewing behavior clearly.

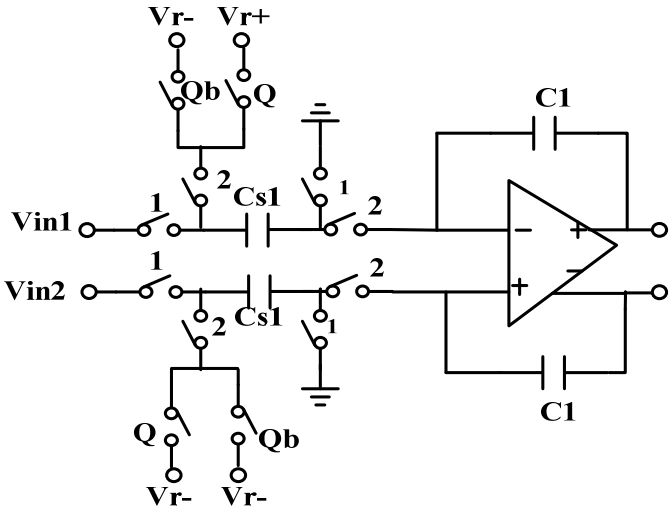


Fig.4.3 Feedback architecture of the integrator

In this design, we set 40% of a period for slewing. Hence, we can derive that:

$$I \geq \frac{Q}{t} = \frac{V_{dd} \cdot (C1 + Cs1 + Cp)}{\frac{1}{2} \cdot T \cdot \frac{2}{5}} = (0.8p + 0.3p + 0.2p) \cdot V_{dd} \cdot 5 \cdot f_{ck} \qquad (4.1)$$

Since we know that $V_{dd} = 1.8V$ and $f_{ck} = 30.72K$, we can calculate that:

$$I \geq (0.8p + 0.3p + 0.2p) \cdot V_{dd} \cdot 5 \cdot f_{ck} = 3.59424 \cdot 10^{-7} \approx 360n(A) \qquad (4.2)$$

We can observe that at least 360nA current is needed.

Secondly, the settling behavior will be considered. From Fig.4.2, we can derive the total time constant of the integrator and it can be shown as:

$$\tau_a = \frac{1}{2\pi \cdot f_u \cdot \beta} \qquad (4.3)$$

where f_u is the unit-gain frequency of the OPAMP and β is the feed-back factor

Next, we set 60% of a period for settling, we can calculate that:

$$t_{settle} \geq \tau_a \cdot nbit \cdot \ln 2 = \frac{1}{2\pi \cdot f_u \cdot \beta} \cdot nbit \cdot \ln 2 \qquad (4.4)$$

where $nbit$ is the required resolution of the system

After calculation, we can calculate that:

$$f_u \geq 264.75KHz \qquad (4.5)$$

Therefore, the OPAMP must meet the previous specification for achieving the required performance.

In this design, the aspect ratio of the OPAMP is listed as Table 4.1:

Aspect Ratio of Operational Amplifier			
No.	length	width	multi
M11	2um	0.25um	8
M1,M2	2um	0.25um	4
M3,M4	10um	0.50um	4
M5,M6	10um	0.50um	4
M7,M8	10um	2.50um	4
M9,M10	10um	2.50um	2

Table 4.1 Aspect ratio of the designed folded-cascode OPAMP

The reason why larger channel length is used for some transistors is that only hundreds of micro ampere is needed for the output current from eq.4.2. All the transistors in the designed OPAMP work on saturation region.

The performance summary of the OPAMP is listed as Table 4.2:

Technology / Supply voltage	TSMC 0.18um 1P6M / 1.8V
DC gain	≒76.886dB
Unity-gain Frequency	≒299.09KHz
Phase Margin	≒88.042°
Output Swing	0.338V~1.588V
Input Common-Mode Range	0.321V~1.192V
PSRR+ / PSRR-	54.574dB / 56.811dB
Bias Current(I)	≒400nA
Power consumption	≒5.213uW

Table 4.2 Specification table of the designed OPAMP

The specification of the designed OPAMP follows the derived ones as eq.4.2 and eq.4.5 with slightly overdesign for the convenience and realistic implementation. It can found that only 5.213uW is needed with the required specification. That makes the designed system much competitive.

4.1.2 The Designed BIAS Circuit in Sigma-delta Modulator

In section 3.1.2, it is mentioned that the “one shot” working type of ADC is needed for sensing application. In this thesis, a mode-selectable BIAS circuit is designed for the desired function. The architecture of the BIAS circuit is shown as Fig.4.3:

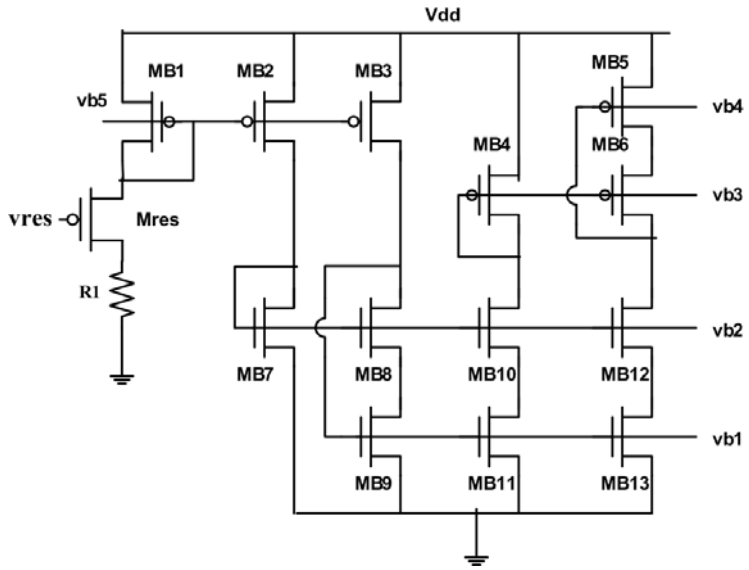


Fig.4.4 Architecture of the mode-controllable BIAS circuit

When the voltage Vres becomes high, the transistor Mres turn off so that the current of BIAS circuit becomes zero and so does the OPAMP circuit. The whole integrator is power down and enters the “sleep mode”. When the voltage becomes low, the BIAS circuit works normally and so does the OPAMP. The whole system converts the temperature signal and enters the “normal mode”. Since the integrator dominates the power consumption of the sigma-delta modulator, the method can greatly reduce the power in sleep mode.

The aspect ratio of the BIAS circuit is listed at Table 4.3:

Aspect Ratio of Bias Circuit			
No.	length	width	multi
MB1	2um	0.25um	1
MB2	2um	0.25um	5
MB3	2um	0.25um	2
MB4	10um	0.25um	2
MB5	10um	2.50um	1
MB6	10um	2.50um	2
MB7	10um	0.25um	1
MB8,MB10,MB12	10um	0.50um	2
MB9,MB11,MB13	10um	0.50um	1
R1	12M		

Table 4.3 Aspect ratio of the mode-controllable BIAS circuit

4.1.3 Correlated Double Sampling (CDS) Technique

In this application, the measured value must be absolutely accurate. Therefore, the offset voltage of the OPAMP, which comes from mismatch of the device, and flicker noise, will affect the system. Comparing with the chopping technique, the CDS technique has lower power consumption and can easier be implemented in discrete time sigma-delta modulator. The circuit architecture of integrator with CDS technique can be shown as Fig.4.4 [18]:

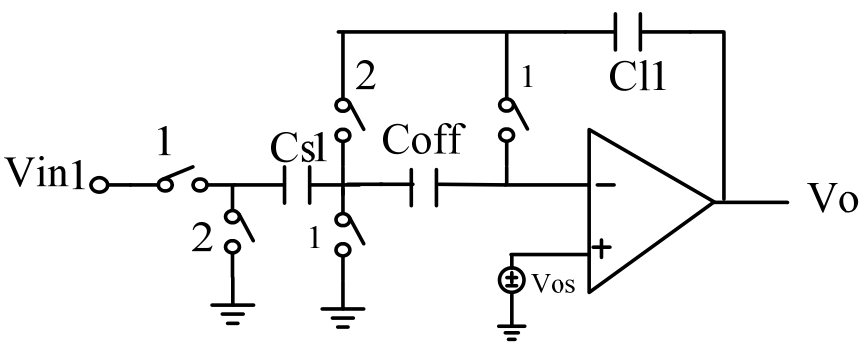


Fig.4.5 Integrator with CDS

Two phases can be classified for analysis the CDS technique can be classified:

At phase1, the circuit works on sampling mode, as in Fig.4.5:

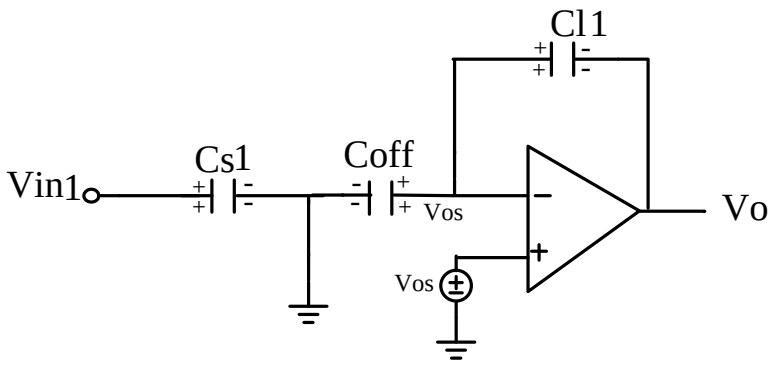


Fig.4.6 Architecture of CDS integrator at phase1

It can be calculated that at time step $t = nT$:

$$Q_{Cs1}(nT) = C_{s1} \cdot V_{in}(nT) \tag{4.6}$$

$$Q_{coff}(nT) = C_{coff} \cdot V_{os} \tag{4.7}$$

$$Q_{cl1}(nT) = C_{cs1} \cdot (V_{os} - V_{out}(nT)) \tag{4.8}$$

The charge on each capacitor can be calculated.

Next, the circuit works on integrating mode, as in Fig.4.6:

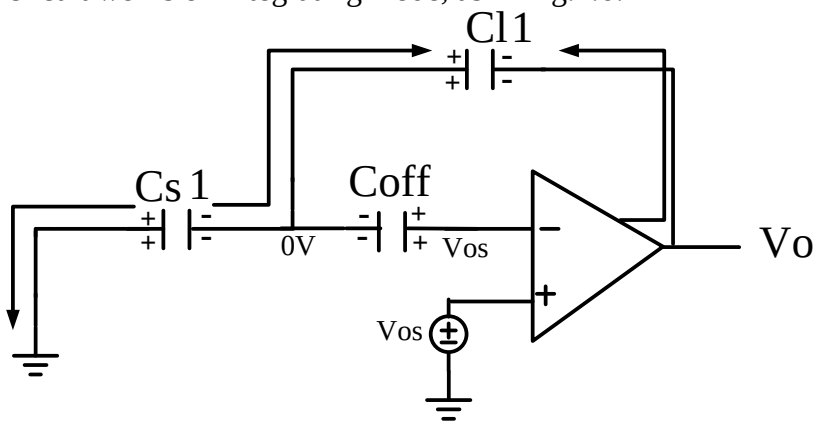


Fig.4.7 Architecture of CDS integrator at phase2

With charge redistribution, we can derive that at time step $t = nT + T/2$:

$$Q_{(Cl1)}\left(nT+\frac{T}{2}\right)=Q_{(Cl1)}(nT)-Q_{(Cs1)}(nT)$$

$$\Rightarrow C_{Cl1}\cdot\left(0-V_{out}\left(nT+\frac{T}{2}\right)\right)=C_{Cl1}\cdot\left(V_{os}-V_{out}(nT)\right)-C_{Cs1}\cdot V_{in}(nT)$$

$$\Rightarrow -C_{Cl1}\cdot V_{out}\left(nT+\frac{T}{2}\right)=C_{Cl1}\cdot V_{os}-C_{Cl1}\cdot V_{out}(nT)-C_{Cs1}\cdot V_{in}(nT) \quad (4.9)$$

Finally, at time step $t = nT + T$ (next sampling period). It can be derived that:

$$-C_{Cl1}\cdot V_{out}(nT+T)+C_{Cl1}\cdot V_{os}=C_{Cl1}\cdot V_{os}-C_{Cl1}\cdot V_{out}(nT)-C_{Cs1}\cdot V_{in}(nT)$$

$$\Rightarrow -C_{Cl1}\cdot V_{out}(nT+T)=-C_{Cl1}\cdot V_{out}(nT)-C_{Cs1}\cdot V_{in}(nT) \quad (4.10)$$

The Z-transform of eq.4.10 can be derived as:

$$-C_{Cl1}\cdot V_{out}(z)\cdot z=-C_{Cl1}\cdot V_{out}(z)-C_{Cs1}\cdot V_{in}(z)$$

$$\Rightarrow C_{Cl1}\cdot V_{out}(z)\cdot(z-1)=C_{Cs1}\cdot V_{in}(z) \quad (4.11)$$

Therefore, the transfer function of the CDS integrator can be written as:

$$\frac{V_{out}(z)}{V_{in}(z)}=\frac{1}{z-1}=\frac{z^{-1}}{1-z^{-1}} \quad (4.12)$$

From eq.4.12, it can found that the transfer function does not relate to the offset voltage Vos. The effect of low-frequency flicker noise in the integrator can also be eliminated with the CDS technique.

4.1.4 Dynamic CMFB Circuit

For fully-differential OPAMP circuit, a CMFB circuit must be used for settling the output common mode voltage of the integrator. A dynamic CMFB circuit is used here for its power-efficient property. The architecture of the dynamic CMFB can be shown as Fig.4.7:

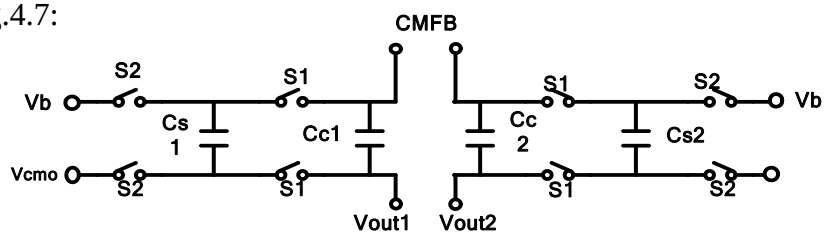


Fig.4.8 Architecture of the CMFB circuit

Here, Vcmo was set to the require output common mode voltage. The Switch connected to CMFB use CMOS switches and other switches use PMOS switch only.

4.1.5 1-bit Quantizer

A power-efficient 1 bit quantizer, which is composed of a comparator and a SR, is shown as Fig.4.8. When the CLK is high, the comparator with positive feedback quickly compares the input voltage and the comparison result is locked by the SR latch.

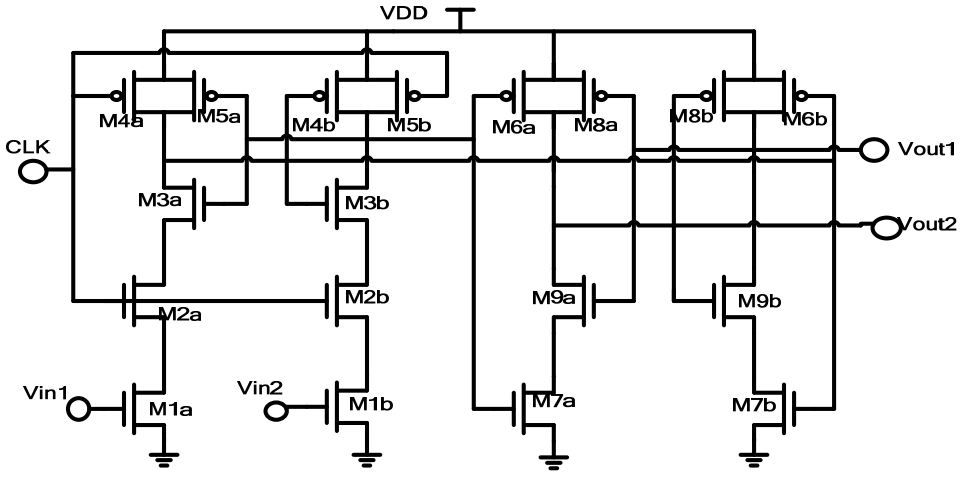


Fig.4.9 Architecture of 1-bit quantizer

4.1.6 Non-overlapped Clock Generator

The on-chip non-overlapped clock generator circuit is shown in Fig.4.9. Four non-overlapped clock signals, which are CK1_a, CK1, CK2_a and CK2, can be generated with one reference clock.

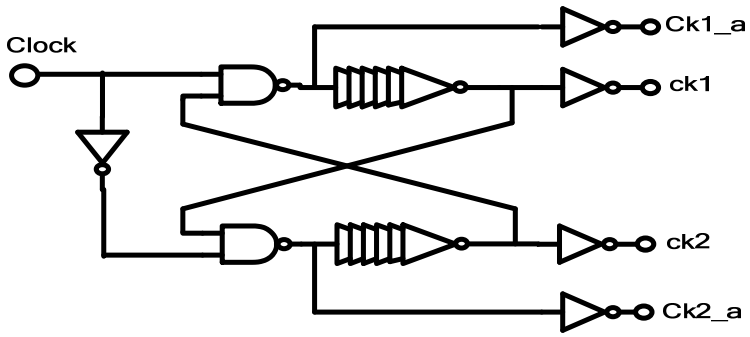


Fig.4.10 Architecture of the non-overlapped clock generator

The sub-circuits used for sigma-delta modulator has be introduces. The design of the SINC filter will be arranged at next section.

4.2 Design of the Digital SINC Filter

As the analysis of section 3.3.1, a third order SINC filter is needed for demodulating bit-streams of the sigma-delta modulator. Here, the detailed design will be presented.

The transfer function of a third order SINC filter can be written as:

$$H(z) = \frac{1}{M^3}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^3 \tag{4.13}$$

where M is the down-sampling ratio of the SINC filter

From eq.4.13, we can observe that the SINC filter has the properties of low-pass and down-sampling. The SINC filter is composed of the chains-of-integrators part (front-end) and the chains-of-comb filter part (back-end). Here, the minimum length of register needed without overflow can be calculated as [13]:

$$B_{\min} = L \cdot \log_2 OSR + 1 = 3 \cdot \log_2 512 + 1 = 28 \qquad (4.14)$$

Next, the signal flow diagram can be depicted as Fig.4.10:

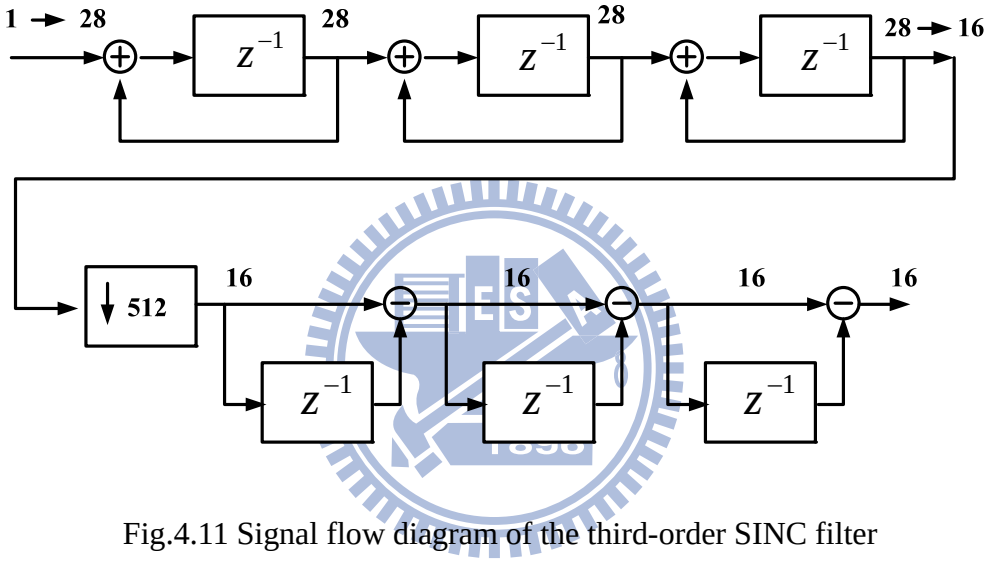


Fig.4.11 Signal flow diagram of the third-order SINC filter

For the corresponding resolution in this application, we reduce the length of register to 16 bits at the chains-of-comb filter part for the required resolution. The minimum conversion cycle and conversion time has also been derived in eq.3.27 and eq.3.28.

In realistic circuit implementation, the back-end comb filter can be simplified for area and power saving after proper analysis. The back-end comb filter part can be shown as Fig.4.11.

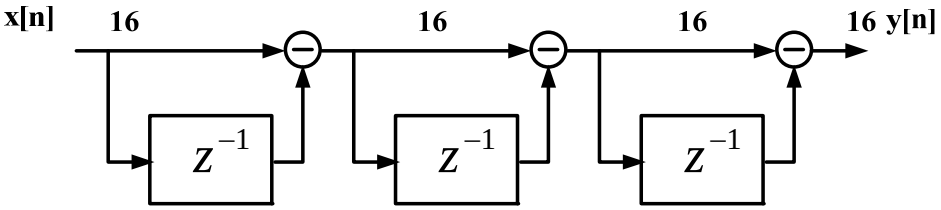


Fig.4.12 Architecture of the back-end comb filter

The transfer function of the comb filter is:

$$y[n] = x[n] - 3x[n-1] + 3x[n-2] - x[n-3] \qquad (4.15)$$

Next, we can recalculate it as:

$$y[n] = x[n] - x[n-1] - x[n-1] - x[n-1] + x[n-2] + x[n-2] + x[n-2] - x[n-3] \qquad (4.16)$$

For the lower operating frequency of the comb filter part, only one register for repeating using is needed. The signal flow diagram for implementing eq.4.16 can be shown as Fig.4.12:

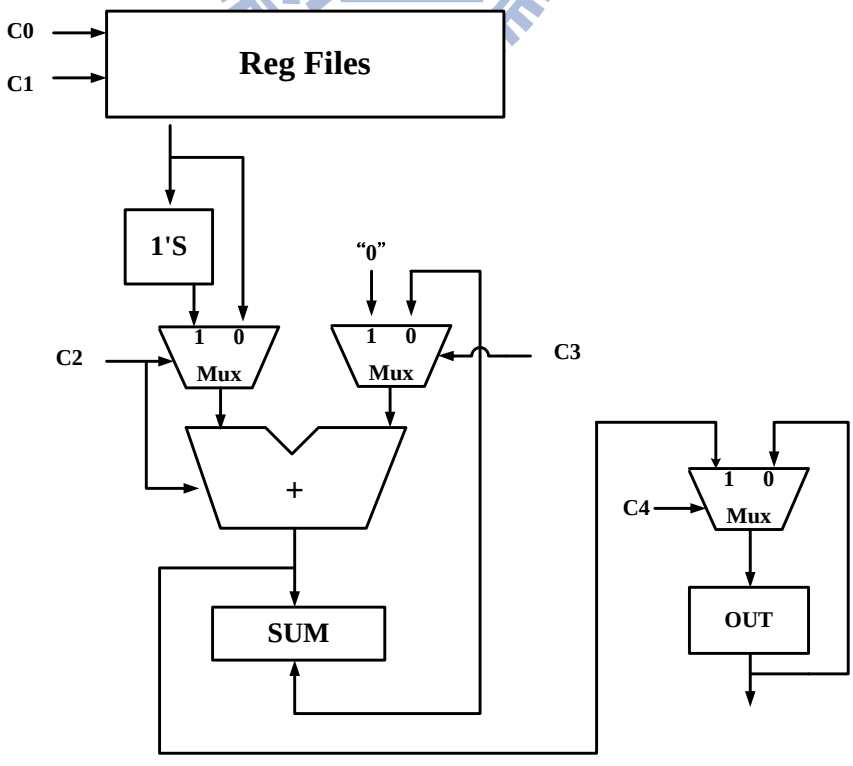


Fig. 4.13 Signal flow diagram of the simplified comb section

The working period is:

$$1st: x_N + \phi$$
$$2nd: 1st - \text{Reg}1$$
$$3rd: 2st - \text{Reg}1$$
$$4th: 3rd - \text{Reg}1$$
$$5th: 4th + \text{Reg}2$$
$$6th: 5th + \text{Reg}2$$
$$7th: 6th + \text{Reg}2$$
$$8th: 7st - \text{Reg}3$$

Finally, the hardware needed of the designed third order SINC filter can be listed as Table 4.4:

	Registers	Add / Sub
Sinc3 filter	28 bits*3 18bits *1	Add*3 Sub*1

Table 4.4 hardware summary of the filter

With the simplified method used, greatly reduction of hardware needed and area consumption is achieved.

After the design of modulator and filter, layout level design will be presented at next section.

4.3 Layout Level Design of the Sigma-delta ADC

The physical layout diagram of the designed ADC is shown as Fig.4.13. This circuit is fabricated in a 0.18um 1P6M 1.8V standard CMOS technology with MIM process.

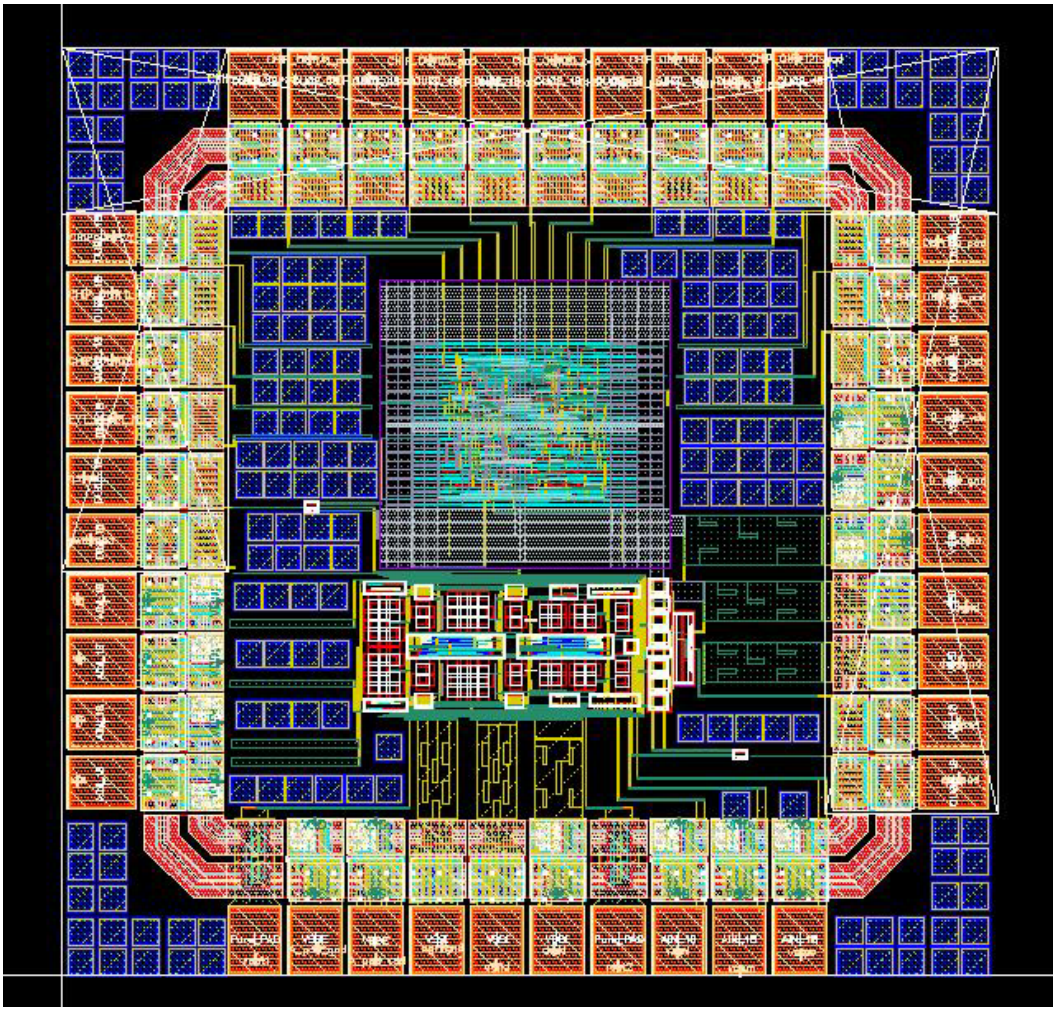


Fig.4.14 Layout diagram of the designed sigma-delta ADC

Variations of process, such as mismatch and parasitic effects, must be considered for better performance. Several principles of layout must be obeyed to reduce these effects:

(1) Symmetry layout of transistors and capacitor in modulator

(2) Multi-finger transistor to reduce the parasitic effects

(3) Dummy Cell to reduce the mismatch effects

The Chip size is $1.068\times1.063mm^2$ including ESD protection PAD and $0.391\times0.501mm^2$ for active area. The package type is S/B 40 pin, as shown in Fig.4.14.

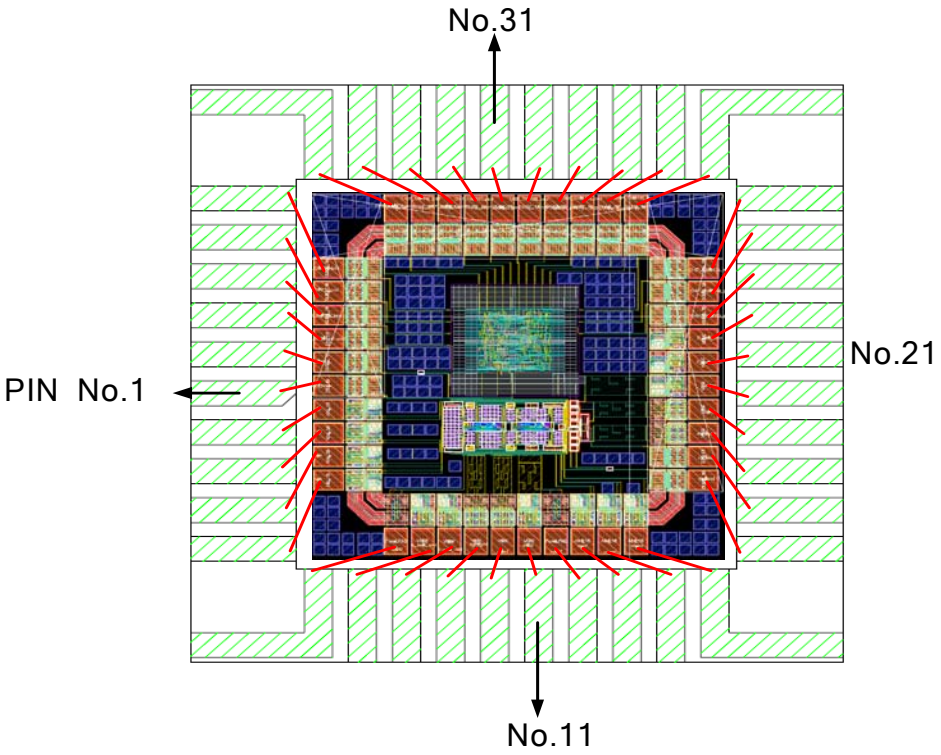


Fig.4.15 Diagram of chip with S/B 40 pin package

The pin assignment is listed as Table 4.5

Pin	Name	Description
1	pwd_pad	Sleep or Normal mode
2	vn	Differential input 2
3	vp	Differential input 1
4	vrp	Reference voltage2
5	vrn	Reference voltage1

6	rout1	Variable resistor 1
7	A_pad_gnd	Analog pad GND
8	A_pad_vdd	Analog pad VDD
9	agr_gnd	Analog guard ring gnd
10	agnd	Analog core GND
11	avdd	Analog core VDD
12	rout2	Variable resistor 2
13	vcmi	OP common voltage
14	vcom	CMFB voltage
15	vcmo	OP common voltage
16	qb_pad	SDM negative output
17	ck_pad	Clock input
18	dgr_gnd	Digital guard-ring power
19	dgnd	Digital core GND
20	dvdd	Digital core VDD
21	D_pad_gnd	Digital pad GND
22	D_pad_vdd	Digital pad VDD
23	CHIP_OUT[15]_pad	Digital output
24	CHIP_OUT[14]_pad	Digital output
25	CHIP_OUT[13]_pad	Digital output
26	CHIP_OUT[12]_pad	Digital output
27	CHIP_OUT[11]_pad	Digital output
28	CHIP_OUT[10]_pad	Digital output
29	CHIP_OUT[9]_pad	Digital output
30	CHIP_OUT[8]_pad	Digital output
31	CHIP_OUT[7]_pad	Digital output
32	CHIP_OUT[6]_pad	Digital output
33	CHIP_OUT[5]_pad	Digital output
34	CHIP_OUT[4]_pad	Digital output
35	CHIP_OUT[3]_pad	Digital output
36	CHIP_OUT[2]_pad	Digital output
37	CHIP_OUT[1]_pad	Digital output
38	CHIP_OUT[0]_pad	Digital output
39	EXT_RESET_N_pad	Register clear
40	q_pad	SDM positive output

Table 4.5 Pin assignment of the chip with S/B 40 pin package

4.4 System Simulation and Comparison

In this section, system simulation result of the sigma-delta modulator, digital SINC filter and the whole sigma-delta ADC will be presented. After all the simulation, comparison between related researches will be arranged.

4.4.1 Simulation Result of the Sigma-delta Modulator

Here, a low-frequency sine-wave is used as testing input for sigma-delta modulator. Simulation result of tt corner 25°C 8192-point fft for a 3.75Hz sine-wave input can be shown in Fig.4.16.

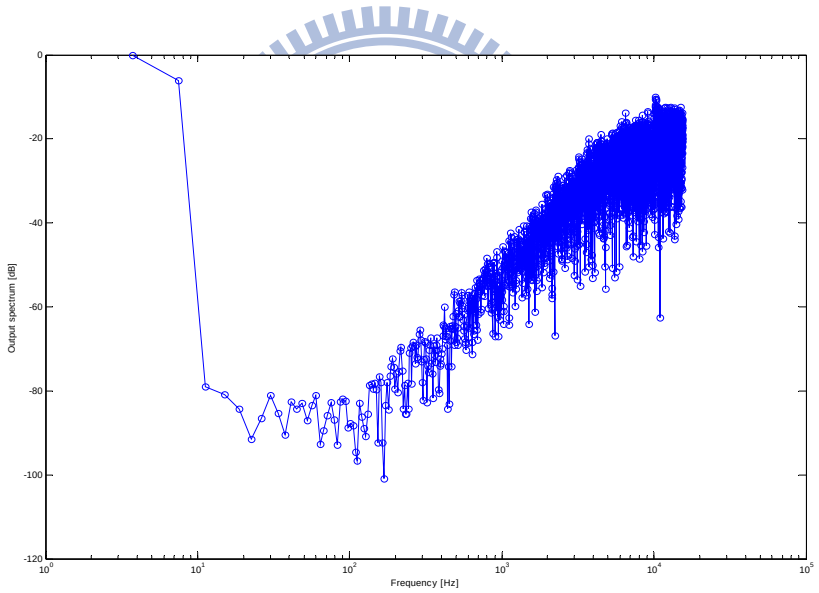


Fig.4.16 Simulation result of 8192 point fft at tt corner 25°C for a 3.75Hz sine wave

The fft shows that the simulated (signal-to-noise and Distortion ratio) $SNDR = 76.921dB$ and $ENOB = 12.485bit$. It meets the system specification of 11bit resolution.

Secondly, the simulation result of ff, ss, fs and sf corners fft for the same

condition can also be shown as Fig.4.17.

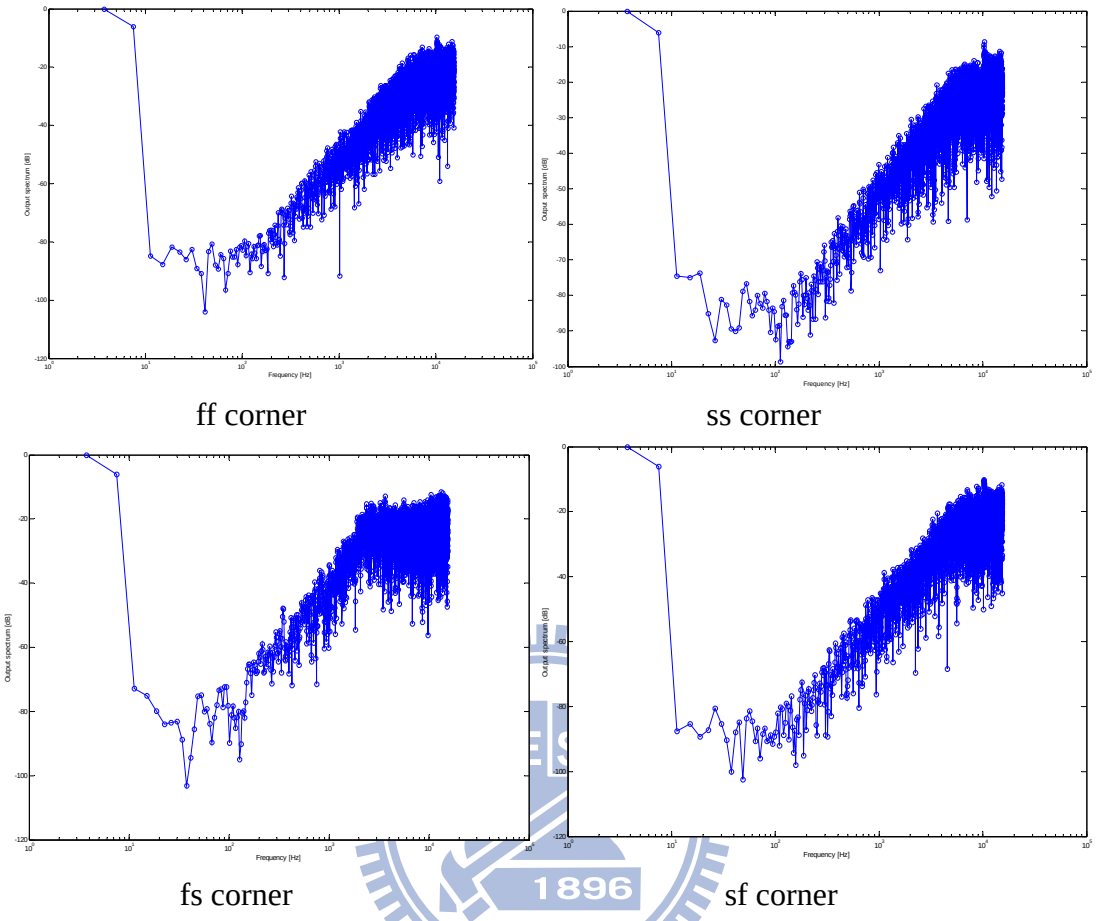


Fig.4.17 Simulation result of ff, ss, fs and sf corner 8192 point fft at 25°C

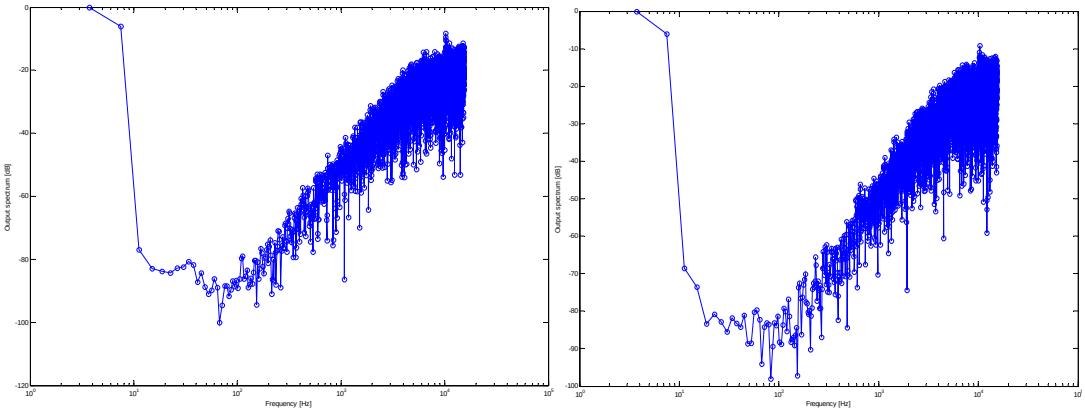
The summary of SNDR and ENOB for each corner is listed in Table 4.6:

Corner	SNDR (dB) / ENOB (bit)
tt	76.921 / 12.485
ff	78.565 / 12.758
ss	70.463 / 11.462
sf	79.102 / 12.847
fs	71.313 / 11.523

Table 4.6 SNDR / ENOB summary for all corners

Since the ADC will be used for wide range temperature sensing, the fft simulation

result for the extreme temperature value is shown as Fig.4.18.



125°C -55°C

Fig.4.18 Simulation result of 8192 point fft for extreme temperature values

The summary of SNDR and ENOB for different temperature is listed in Table 4.7:

temperature	SNDR (dB) / ENOB (bit)
-55°C	73.282 / 11.880
25°C	76.921 / 12.485
125°C	78.670 / 12.781

Table 4.7 SNDR / ENOB summary for different temperature values

It can be found that the sigma-delta modulator can meet the system specification at different corner and temperature values.

Finally, the post-layout simulation of the sigma-delta modulator is shown at Fig.4.19.

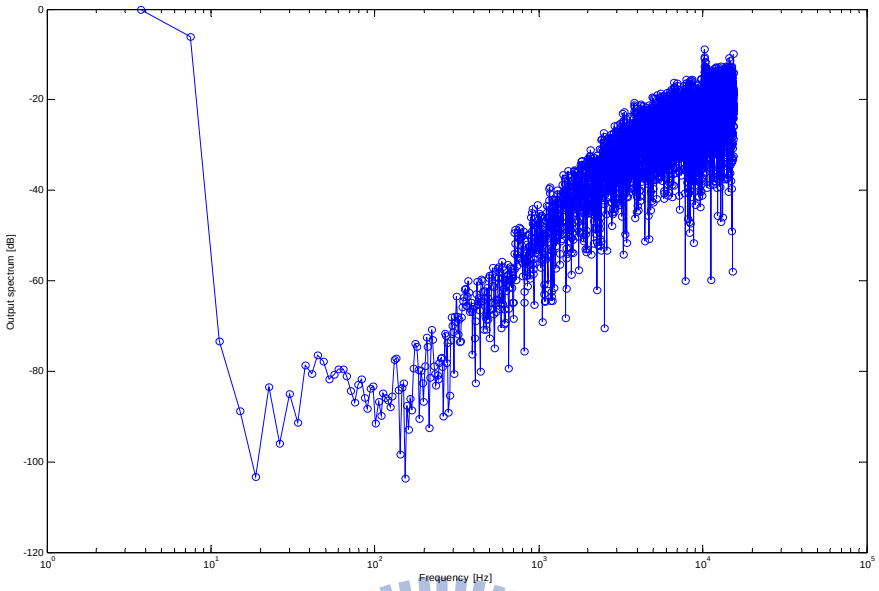


Fig.4.19 tt corner 25°C 8192-point 3.75 Hz-sine wave fft result (post-sim)

The fft shows that the simulated (signal-to-noise and Distortion ratio) $SNDR = 74.0893dB$ and $ENOB = 12.0148bit$ for post-layout simulation. It can also meet the system specification of 11bit resolution.

The summary of SNDR / ENOB and power dissipation for pre-layout simulation and post-layout simulation is listed in Table 4.8:

Simulation Result	Pre-sim	Post-sim
Input Frequency(Hz)	3.75	
SNDR(dB) / ENOB(bit)	76.9210 / 12.4850	74.0893 / 12.0148
Power Dissipation(uW)	12.165	12.578

Table 4.8 Performance summary of modulator for pre-sim and post-sim

Finally, the power consumption of the modulator in normal mode and sleep mode can be listed as table 4.9.

Mode	Normal	Sleep
Supply Voltage	1.8V	
Power Consumption	12.578uW	1.997uW

Table 4.9 Power consumption comparison of modulator at different mode

It can be observed that 84.123% power consumption can be saved at sleep mode. Therefore, greatly power saving can be achieved for the method used in this thesis.

4.4.2 Simulation Result of the Third Order SINC Filter

Here, we put the signal flow diagram, as in Fig.4.11, again for analysis conveniently.

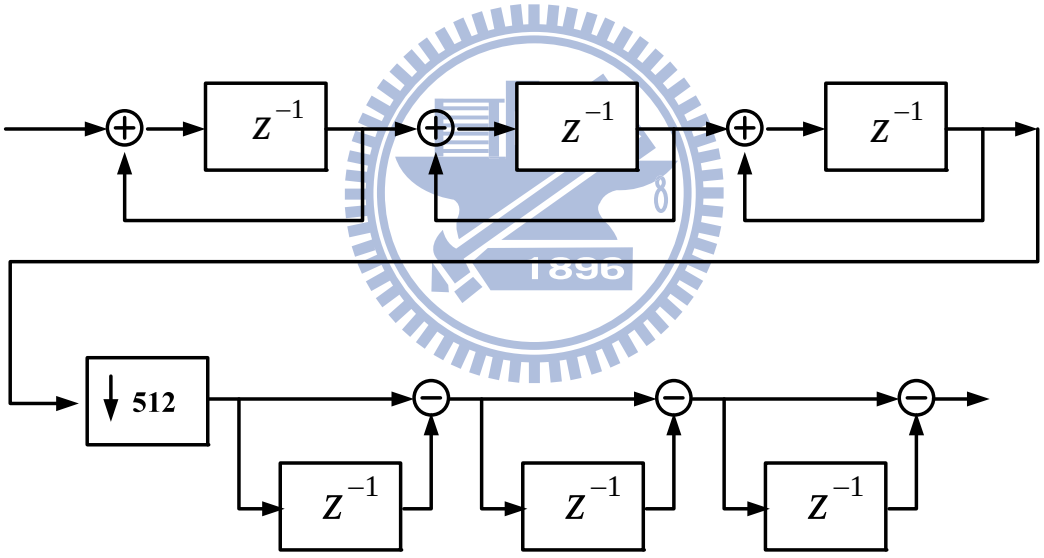


Fig.4.11 Signal flow diagram of the third-order SINC filter

The simulation result of third order SINC is shown in Fig.4.20

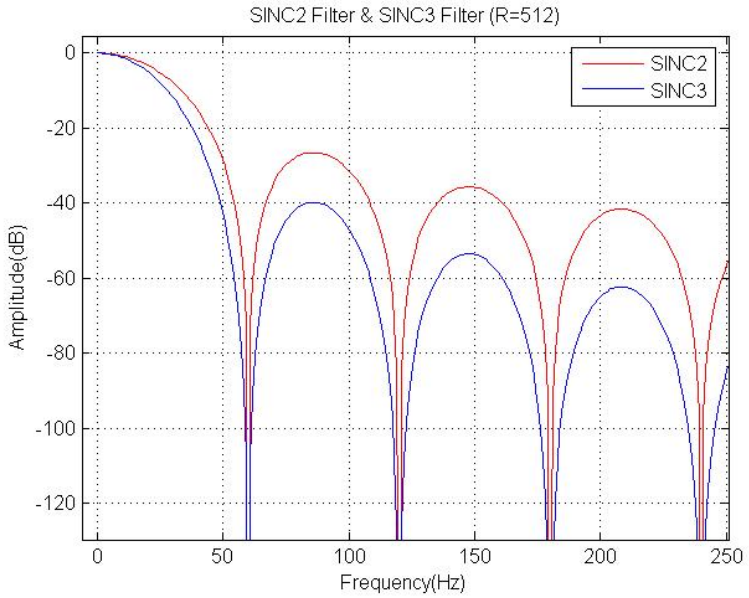


Fig.4.20 Frequency domain simulation of second and third order SINC filter

From, Fig.4.19, it is clear that the third order one can have better noise attenuation than the second order one.

The hardware implementation and power consumption of the SINC filter is listed in Table 4.10:

	Registers	Add / Sub	Gate Count	Power
Sinc3 filter	28 bits*3 18bits *1	Add*3 Sub*1	2437	0.339uW

Table 4.10 Hardware implementation summary of filter

In this thesis, power saving mechanism is also used in the designed filter by clock gating. The power consumption of the SINC filter in normal mode and sleep mode can be listed as table 4.11.

Mode	Normal	Sleep
Supply Voltage	1.8V	
Power Consumption	0.339uW	0.017uW

Table 4.11 Power consumption comparison of SINC filter at different mode

4.4.3 Simulation Result of the Designed Sigma-delta ADC

The DC input simulation is shown in Fig.4.21. In Fig.4.21, the X-axis is the input DC voltage and the Y-axis is the corresponding quantization error in LSB. The LSB for the system specification can be calculated as:

$$V_{LSB} = \frac{2 \cdot 1.8}{\frac{125-(-55)}{0.1}} = 0.002(V) \tag{4.17}$$

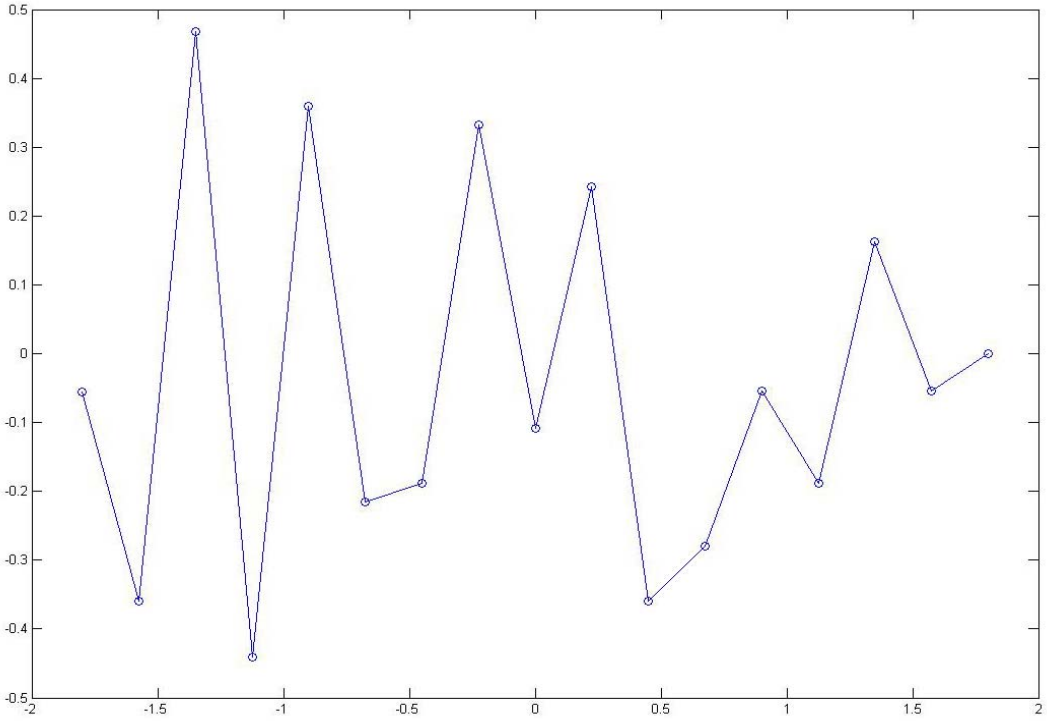


Fig.4.21 Input voltage (x-axis) V.S. quantization error (y-axis) diagram

It is clear that all the quantization $Q_{error} \le 0.5V_{LSB}$. Therefore, the designed ADC can meet our system specification

The simulation result of nanosim is shown in Fig.4.22 for co-simulation, the analog modulator and the digital filter, verification.

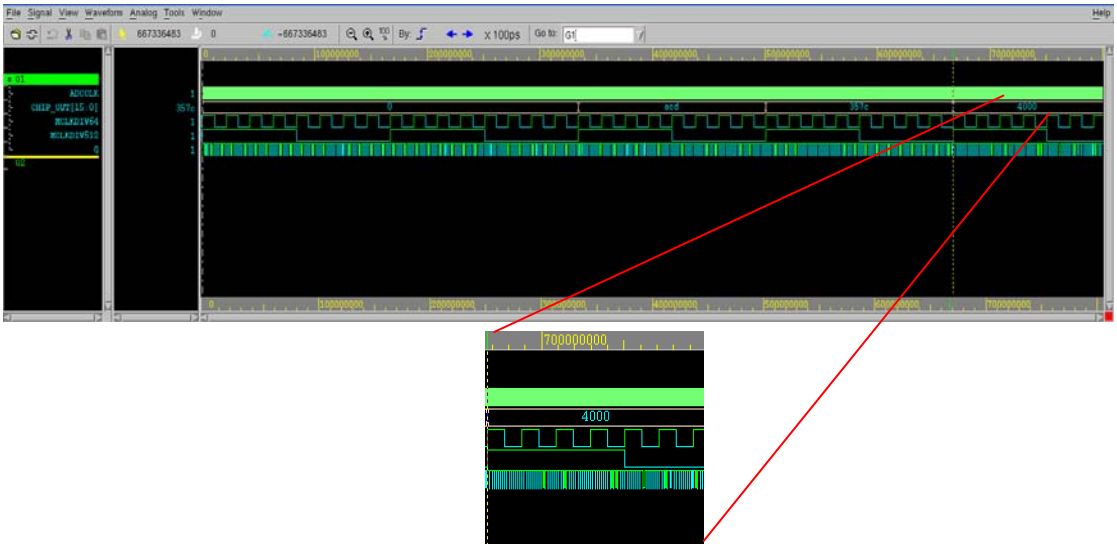


Fig.4.22 Nanosim simulation result of the ADC

In Fig.4.21, the input voltage is DC 0.9V. Since the reference voltage Vref is 1.8V, it means that the digital output is 0.5. In binary format, 0.5 can be presented as:

$$0.5_2 = \underset{4}{0.1}\underset{0}{0000}\underset{0}{0000}\underset{0}{0000} \qquad (4.20)$$

Therefore, the co-simulation function of the whole ADC is correct

Finally, the power consumption of the designed Sigma-delta ADC in normal mode and sleep mode can be listed as table 4.12.

Mode	Normal	Sleep
Conversion time	50ms	
Power Consumption	12.578uW+0.339uW =12.917uW	1.997uW+0.017uW =2.014uW
Energy Consumption	0.63uJ+0.016uJ =0.646uJ	Not needed

Table 4.12 Summary of power and energy consumption for the designed ADC

In normal mode, the power consumption of 12.917uW and 0.646uJ for each temperature conversion is achieved. On the other hand, only 2.014uW power consumption is needed in sleep mode. The power reduction rate is 84.048% in sleep mode for the proposed method.

4.4.4 Comparison with Related Researches

The simulation results of this thesis are all shown in previous section. In this section, the comparison result will be presented.

The performance comparison of Sigma-delta ADCs, which is used in smart temperature or instrumentation application in recent researches, is listed at Table 4.13.

Reference	Process	Resolution	Conversion time	Power	Energy (per-conv.)	Normalized Energy	N.Energy/resolution (uJ/dB)
JSSC, 2004[5]	0.5um CMOS	15.5bit	25ms	432.01uW ~880.42uW	10.80uJ ~22.01uJ	1.336uJ ~2.852uJ	0.0143~0.0305
JSSC, 2006[10]	0.6um CMOS	22bit	66.7ms	323.98uW 599.98uW	21.61uJ ~40.02uJ	1.945uJ ~3.6021uJ	0.0146~0.0272
ISCAS, 2008[19]	0.7um CMOS	12bit	200ms	212.50uW ~467.50uW	42.50uJ ~93.50uJ	2.81uJ ~6.183	0.0388~0.0855
This work	0.18um TSMC	12bit	50ms	12.917uW	0.65uJ	0.65uJ	0.0089

Table 4.13 Performance comparison table of sigma-delta ADC

From Table4.13, it is clear that the designed sigma-delta ADC has the lowest power and energy consumption than the other ones. Since the process used is different, Normalization in energy consumption is also done [18]. Lowest normalized energy consumption is achieved for the process normalization one. Next, we know that the resolution is determined with corresponding application.

Energy-per-resolution parameter is also made for resolution normalization. It can be found that the designed ADC has the lowest energy-per-resolution. Therefore, the designed sigma-delta ADC is highly competitive in temperature sensing and instrumentation application.

Circuit implementation, simulation and comparison have been presented in this chapter. Testing and measurement consideration will be discussed in next chapter.

Chapter 5

Testing Setup and Measurement

5.1 Testing Environment Setup

A testing setup for the fabricated chip is presented in this section. Fig.5.1 shows the die photo of the developed chip.

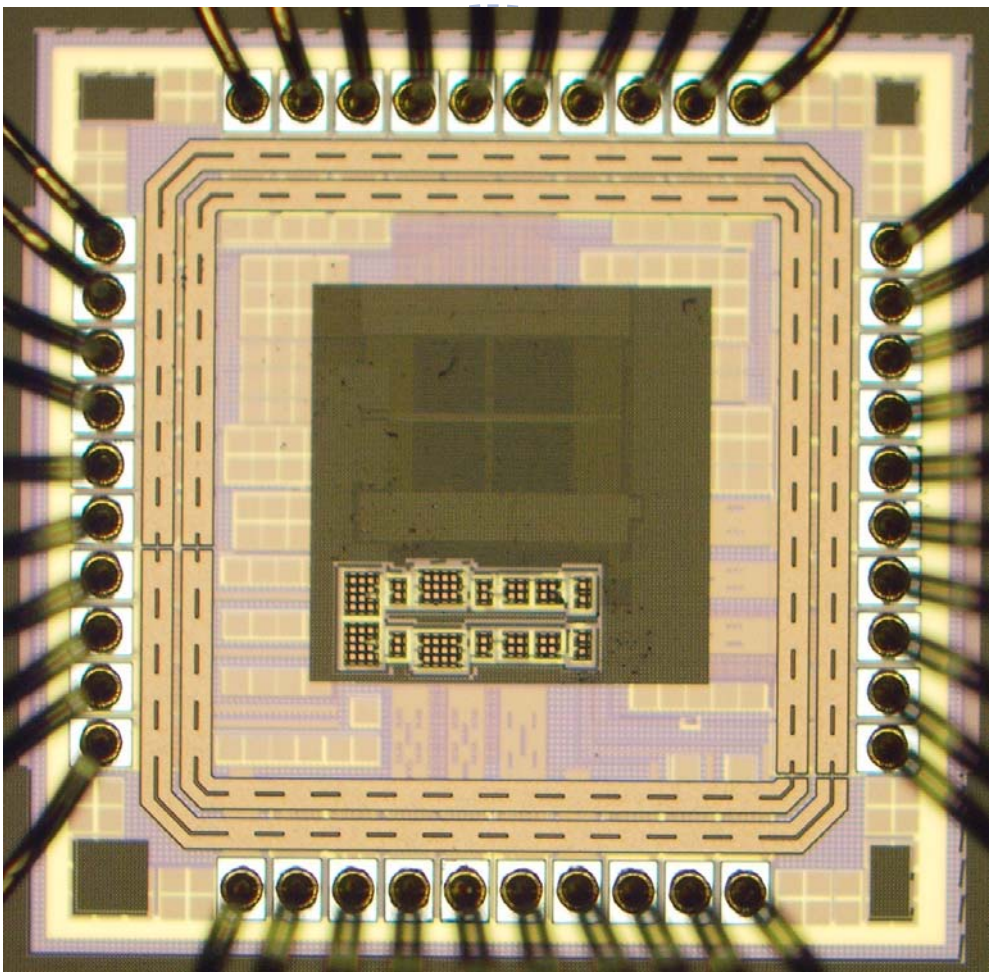


Fig.5.1 Die photo of the fabricated chip

Two measurements must be made for the fabricated chip:

(a) The SNR of the sigma-delta modulator

(b) The accuracy of the sigma-delta ADC.

The testing environment of (a) is shown in Fig.5.2.

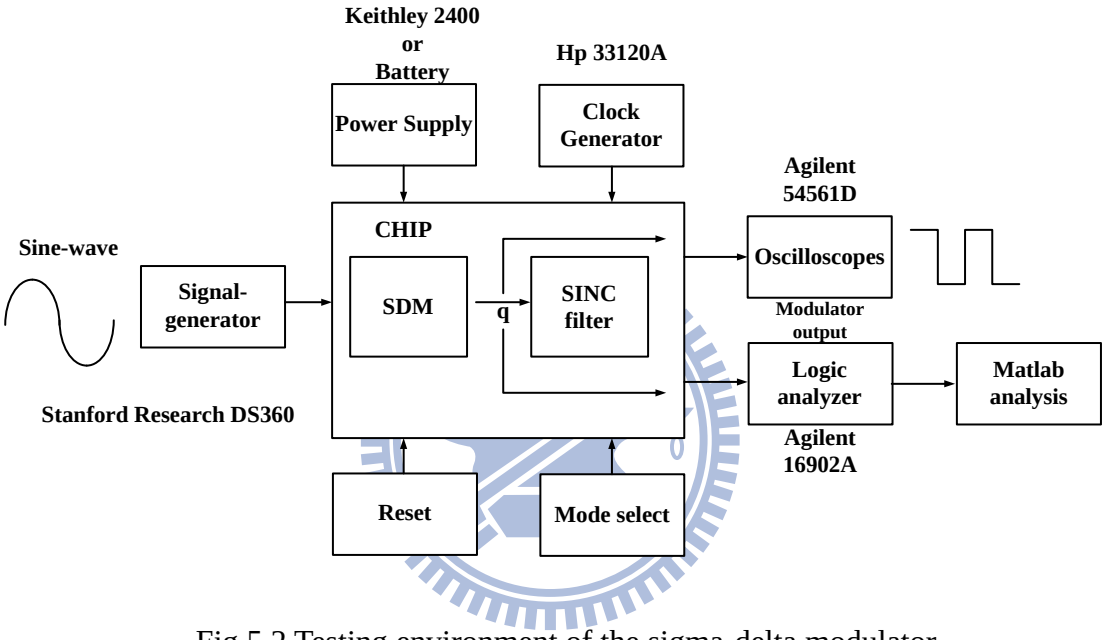


Fig.5.2 Testing environment of the sigma-delta modulator

It includes a low-distortion signal generator (Standford Research DS360), a low-frequency clock generator (Hp 33120A), a low noise power supply (Keithley 2400), a mix-signal Oscilloscopes (Agilent 54561D) and a logic analyzer (Agilent 16902A). Due to the slower frequency, a bread board is used for fast functional testing. The photo of testing environment is shown in Fig.5.3.

When testing the SNR of the sigma-delta modulator, a low-frequency sine-wave is given for input signal. Next, the output of the modulator can be shown in Oscilloscope and will be captured by logic analyzer at the same time. Finally, by using matlab for fft analysis, the SNR of the modulator will be calculated.

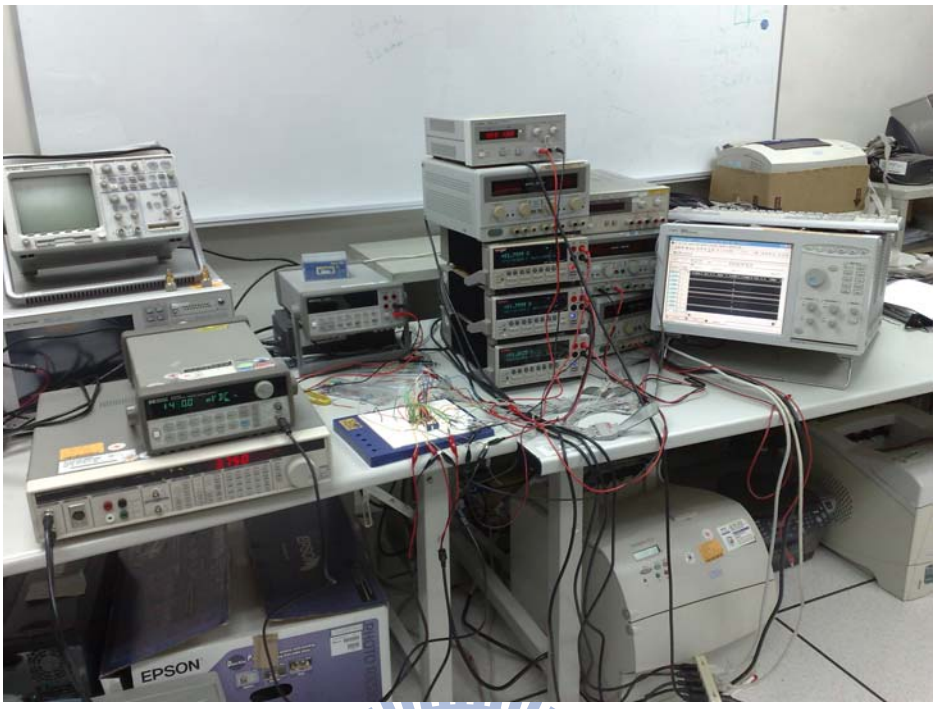


Fig.5.3 Photograph of the measurement environment

Next, measurement environment of (b) can be shown in Fig.5.4.

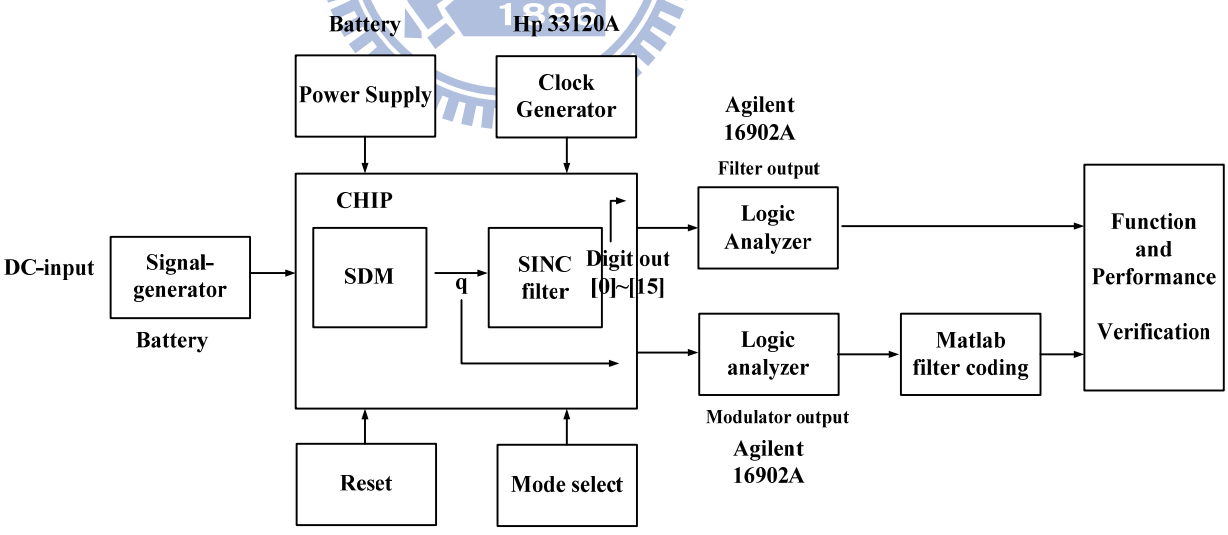


Fig.5.4 Testing environment of the sigma-delta ADC

Here, a dc input which comes from battery is given for input. Next, the output of the modulator (q) and the output of the ADC (Digit out[0]~[15]) will be captured by logic analyzer simultaneously. The function of the digital filter can be verified by

comparing the data of the logic analyzer and ideal out from matlab filter coding with q. Finally, accuracy of the ADC can be analyzed by comparing the dc input and output from logic analyzer.

5.2 Measurement Result

(a) Measurement result of the sigma-delta modulator

Fig.5.5 shows the measurement result of the fabricated chip with 1.875Hz input frequency.

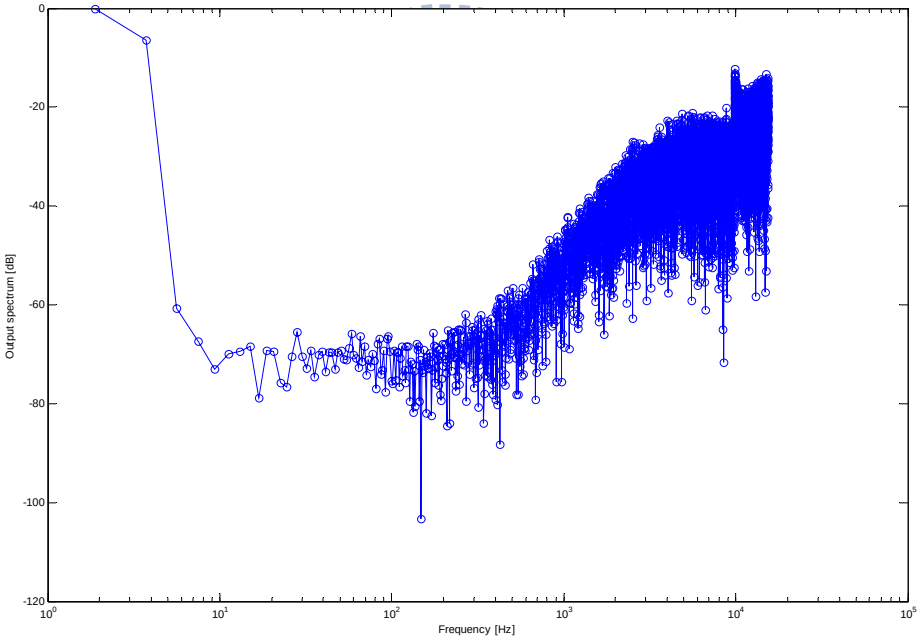


Fig.5.5 Measurement result of 1.875Hz sine wave

The fft shows that the measured $SNDR = 59.7664dB$ and $ENOB = 9.6356bit$. It can be found that degradation of the modulator occurs. In the testing environment, the noise which comes from the voltage supply may be the major cause since the sampling frequency of the developed circuit is slower.

Therefore, a measurement is made by using 1.8V battery as the voltage source which eliminates the noise of supply voltage. The measurement result for 1.875Hz input is shown in Fig.5.6.

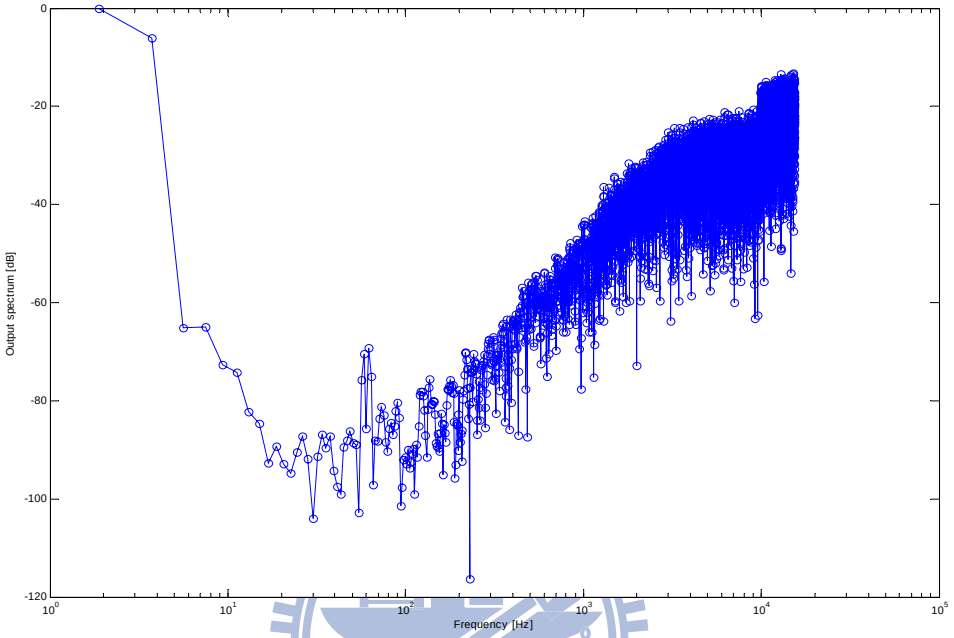


Fig.5.6 Measurement result of 1.875Hz sine wave (with battery)

The fft shows that the measured $SNDR = 64.7768dB$ and $ENOB = 10.4628bit$. The system specification of 10.81bit resolution is achieved.

(b) Measurement result of the sigma-delta ADC

The DC input simulation is shown in Fig.5.7. In Fig.5.7, the X-axis is the input DC voltage comes from battery and the Y-axis is the corresponding quantization error in LSB. The LSB for the system specification can be calculated as:

$$V_{LSB} = \frac{\frac{2 \cdot 1.8}{125-(-55)}}{0.1} = 0.002(V)$$

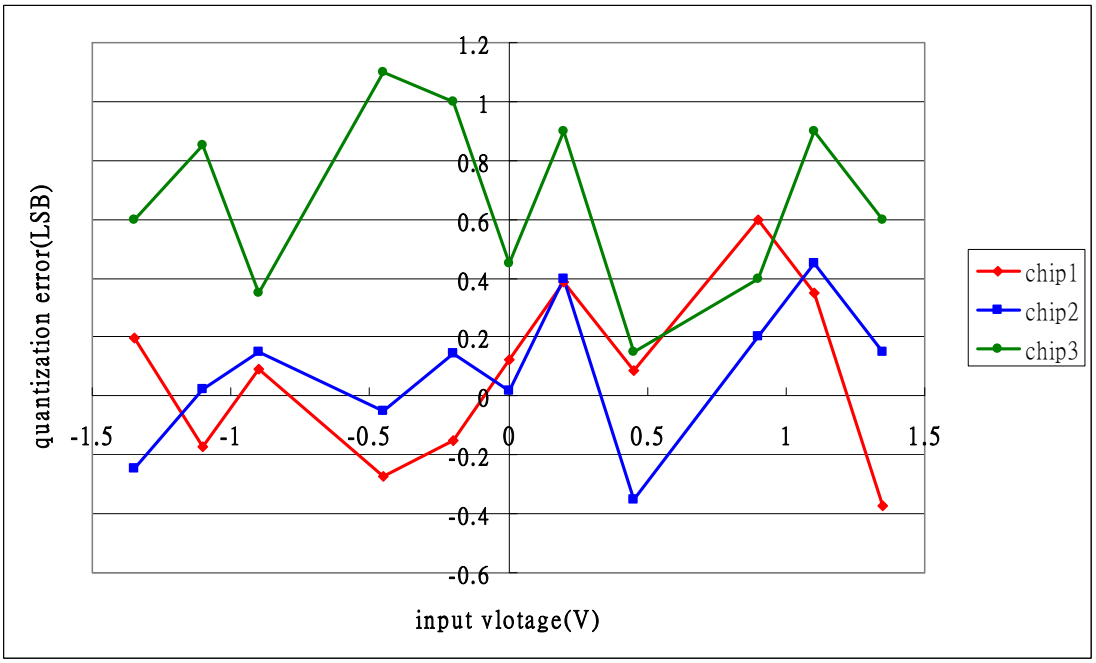


Fig.5.7 Input voltage (x-axis) V.S. quantization error (y-axis) diagram

It is clear that the quantization error of chip1 and chip2 can meet the specification of quantization $Q_{error} \le 0.5V_{LSB}$. In chip3, 0.5VLSB offset voltage occurs. Process variation between transistors in the OPAMP may cause the effect despite CDS technique is used in the developed circuit. However, system level trimming can be used for eliminating the effects since the offset voltage of each chip is fixed.

Finally, Table.5.1 shows the power consumption of the designed ADC. It can be separated by two parts: the analog part and the digital part:

(a) Power consumption of the analog block (modulator only)

Part	Analog Block(modulator only)	
Type	Post-layout Simulation	Measurement
Power consumption (Normal work mode)	10.59uW	12.042uW
Power consumption (Sleep mode)	0.013uW	0.016uW

Table.5.1 Power consumption of analog block

(b) Power consumption of the digital block (Analog clock generator + SINC filter + output buffer)

Part	Digital Block		
Type	Post-Sim (Without bread board loading)	Post-Sim (With bread board loading)	Measurement (With bread board loading)
Power consumption (Normal work mode)	2.327uW	39.8266uW	43uW
Power consumption (Sleep mode)	2.001uW	36.6071uW	41uW

Table.5.2 Power consumption of digital block

It can be found that the power consumption of analog part is nearly the same. Larger power consumption at digital part can be explained by post-layout simulation with bread board loading.

5.3 Summary

A summary of the developed sigma-delta ADC can be listed as Fig.5.3

Technology / Supply voltage	TSMC 0.18um 1P6M / 1.8V
Sampling frequency	30.72KHz
Absolute resolution	10.81bit
Power dissipation @Normal mode	55.042uW
Power dissipation @Sleep mode	41.016uW
Conversion time	50ms
Energy consumption (per conv.)	2.7574uJ
Chip size(core)/ (full chip)	$0.391 \cdot 0.501 mm^2$ /$1.068 \cdot 1.063 mm^2$

Table.5.3 Performance summary of the developed ADC

The circuit present in this thesis is the design and implemented of a low power sigma-delta ADC for temperature sensing application. Architecture analysis for low power issue is made in chapter3. In chapter4, transistor level design of each block is considered. The measurement result reveals that the developed ADC can meet the system specification and has the lowest energy consumption when comparing to recent researches [5]、[10]、[19].

Chapter 6

Conclusion and Future Works

6.1 Conclusion

This thesis describes the design and implementation of a low power and energy consumption sigma-delta ADC for advanced all CMOS smart temperature sensor. A low power second order CIFF architecture sigma-delta modulator which is composed of a mode selectable CDS integrator and a low power quantizer is designed. A simplified third order SINC filter is also implemented for demodulate the bit-streams of the front-end modulator.

The designed ADC is implemented in TSMC 0.18um process. The absolute accuracy of 11bit is achieved for the designed sigma-delta ADC which is sufficient for ±0.1°C accuracy from -55°C ~125°C temperature range. The front-end sigma-delta modulator can have 74.0893dB SNDR and it can also achieve the required specification even in wide temperature operation. With the CIFF architecture, low voltage operation and relaxing specification of OPAMP, which reduced the power consumption, can be achieved. The power consumption of 12.917uW and 0.646uJ energy dissipation for each conversion in Normal work mode is the lowest one between recent researches. On the other hand, only 2.014uW power consumption is needed in Sleep mode. 84.048% power reduction rate is achieved.

6.2 Future Work

The future work is to integrate the high linearity PTAT sensor part. A low power interface for connecting the sensor and ADC must be designed. High performance current-to-voltage circuitry and a preamplifier are needed in this design.

System level chopping and dynamic element matching (DEM) technique may be used for eliminating the offset voltage caused by process variation. The connection between front-end sensor and back-end ADC will continuously be made by out group. A low-power high accuracy smart temperature sensor with wide sensing range is expected to be implemented in the near future.

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