

# 應用於藍牙傳輸及液晶顯示器中間極驅動器之 資料轉換器設計

研究生：李尚勳

指導教授：洪崇智 教授

國立交通大學  
電信工程學系碩士班

## 摘要

在許多訊號處理的應用上，資料轉換器是對於整個系統的速度和精準度相當重要的一塊電路，資料轉換器又分為類比數位資料轉換器和數位類比資料轉換器兩個部份。在類比數位資料轉換器中三角積分類比數位轉換器傳統地被使用在低訊號頻帶和高解析度的儀器、聲音和音頻訊號的應用上。而數位類比轉換器則應用在液晶顯示器的驅動器上。

在這論文裡，連續時間三角積分類比數位轉換器的設計流程將被呈現，並且一個應用於100MHz取樣頻率和1MHz訊號頻帶的運算放大器連續時間三角積分類比數位轉換器被實現。此設計被製造於台積電 0.18 微米互補式金氧半導體製程。量測的訊號失真雜訊比為 53.8dB 而動態輸入範圍為 56dB。功率消耗在 1.8V 電源供給下為 10.2 毫瓦。

在這論文中，液晶顯示器的源極驅動器也將被實現，傳統的源極驅動器是以電阻串的形式完成，但有著許多問題需要克服，故提出一個全新的架構——轉換電容式數位類比轉換器來完成。此設計是使用台積電 0.35 微米半導體製程。

# Data converters for Bluetooth and LCD column driver applications

Student : Shang-Shiun Li

Advisor : Prof. Chung-Chih Hung

Department of Communication Engineering

National Chiao Tung University

Hsinchu, Taiwan

## Abstract

In many signal processing applications, the data converter is a critical building block limiting the accuracy and speed of the overall system. Data converters have two type, Analog-to-digital converter (ADC) and digital-to-analog converter (DAC). In the analog-to-digital converter, sigma-delta analog-to-digital converter is traditionally used in instrumentation, voice, and audio applications that are low signal bandwidth and high resolution. Digital-to-analog converters are applied to the column driver circuit to drive the LCD pannel

In this thesis, the design flow of the continuous-time (CT) modulator is presented and a 100MHz CT single-bit active-RC sigma-delta modulator with 1MHz signal bandwidth for Bluetooth application is implemented. The design has been fabricated by TSMC 0.18  $\mu\text{m}$  CMOS process. The measured SNDR is 53.8dB and the dynamic range is about 56dB. The power consumption is about 10.2mW at 1.8V supply.

Furthermore, a DAC circuit for LCD column driver application is also implemented. Historically, column drivers have employed the resistor string DAC to provide the analog voltage, but it has to overcome solve problems. There we have developed a complete new system using a linear DAC in the column driver. The DAC circuit has been design by TSMC 0.35  $\mu\text{m}$  process.

## 誌謝

隨著這份碩士論文的完成，兩年來在交大的求學生活也即將告一個段落，往後迎接著我的，又是另一段嶄新的人生旅程。本論文得以順利完成，首先，要感謝我的指導教授洪崇智老師在我兩年的研究生活中，對我的指導與照顧，並且在研究主題上給予我寬廣的發展空間。而類比積體電路實驗室所提供完備的軟硬體資源，讓我在短短兩年碩士班研究中，學習到如何開始設計類比積體電路，乃至於量測電路，甚至單獨面對及思考問題的所在。此外要感謝李育民教授和陳富強教授撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

另一方面，要感謝所有類比積體電路實驗室的成員兩年來的互相照顧與扶持。首先，感謝已畢業博士班學長羅天佑和博士班學長薛文弘、廖德文、陳宗益、陳家敏以及已畢業的碩士班學長林永州、楊文霖、夏竹緯、郭智龍、黃介仁、邱楓翔和張維欣在研究上所給予我的幫助與鼓勵，尤其是文弘學長和德文學長，由於他平時不吝惜的賜教與量測晶片時給予的幫助，使得我的論文研究得以順利完成。另外我要感謝黃聖文、許新傑和簡兆良等諸位同窗，透過平日與你們的切磋討論，使我不論在課業上，或研究上都得到了不少收穫。尤其是工四718實驗室的同學們，兩年來陪我一塊兒努力奮鬥，一起渡過同甘苦的日子，也因為你們，讓我的碩士班生活更加多采多姿，增添許多快樂與充實的回憶。此外也感謝學弟們陳伽維、許凱修、李人維、蔡湯唯、林均曄和蘇俊仁的熱情支持，因為你們的加入，讓實驗室注入一股新的活力與朝氣。

到這邊，特別要致上最深的感謝給我的父母及家人們，謝謝你們從小到大所給予我的栽培、照顧與鼓勵，讓我得以無後顧之憂地完成學業，朝自己的理想邁進，衷心感謝你們對我的付出。還有默默陪伴著我的許多朋友，感謝你們體諒我平時的忙碌，以及在背後不斷地鼓勵我、支持我，並在這段成長的路上與我相伴。

最後，所有關心我、愛護我和曾經幫助過我的人，願我在未來的人生能有一絲的榮耀歸予你們，謝謝你們。

李尚勳 于 交通大學工程四館 718 實驗室  
2009. 10. 14

# TABLE OF CONTENTS

	<u>Page</u>
ABSTRACT.....	I
ACKNOWLEDGEMENT.....	III
TABLE OF CONTENTS.....	IV
LIST OF FIGURES.....	VII
LIST OF TABLES.....	XI

	<u>Page</u>
<b>CHAPTER 1</b>	
<i>Introduction</i> .....	1
1.1 <i>Motivation</i> .....	1
1.2 <i>Thesis Organization</i> .....	3
<b>CHAPTER 2</b>	
<i>Basic Understanding of Sigma-Delta A/D Conversion</i> .....	6
2.1 <i>Performance Parameters</i> .....	6
2.1.1 <i>Signal-to-Noise Ratio (SNR)</i> .....	6
2.1.2 <i>Signal-to-Noise and Distortion Ratio (SNDR)</i> .....	7
2.1.3 <i>Spurious Free Dynamic Range (SFDR)</i> .....	7
2.1.4 <i>Dynamic Range (DR)</i> .....	7
2.1.5 <i>Effective Number of Bits (ENOB)</i> .....	8
2.1.6 <i>Overload Level (OL)</i> .....	8
2.2 <i>Sampling and Quantization</i> .....	9
2.3 <i>Oversampling</i> .....	15
2.4 <i>Noise shaping</i> .....	16
2.5 <i>First-order Sigma-Delta Modulator</i> .....	17
2.6 <i>Second-order Sigma-Delta Modulator</i> .....	20
2.7 <i>High-order Sigma-Delta Modulator</i> .....	22
2.8 <i>Summary</i> .....	23
<b>CHAPTER 3</b>	
<i>Continuous-Time Sigma-Delta Modulators</i> .....	24
3.1 <i>Discrete-Time Modulators V.S Continuous-Time Modulators</i> .....	24
3.2 <i>Transformation of a Discrete-Time to a Continuous-Time</i> .....	26
3.2.1 <i>Impulse-Invariant transformation</i> .....	26

3.3	<i>Non-idealities of Continuous-Time Modulators</i> .....	31
3.3.1	<i>Opamp's non-idealities in CT Integrators</i> .....	31
3.3.2	<i>Excess Loop Delay</i> .....	32
3.3.3	<i>Clock Jitter</i> .....	34
<b>CHAPTER 4</b>		
<i>A Continuous-Time Single-Bit Active-RC Sigma-Delta Modulator with 1MHz bandwidth</i> .....		
		<b>37</b>
4.1	<i>Introduction</i> .....	37
4.2	<i>Loop Filter Architecture</i> .....	38
4.2.1	<i>Architecture</i> .....	38
4.2.2	<i>Coefficients</i> .....	40
4.3	<i>System Level Analysis</i> .....	41
4.3.1	<i>RC Variation</i> .....	43
4.3.2	<i>Clock Jitter</i> .....	44
4.3.3	<i>Simulation Result</i> .....	45
4.4	<i>Circuit Level Implementation</i> .....	46
4.5	<i>Circuit Level Simulation Result</i> .....	55
4.6	<i>Summary</i> .....	57
<b>CHAPTER 5</b>		
<i>BACKGROUND OF LIQUID CRYSTAL DISPLAY</i> .....		
		<b>58</b>
5.1	<i>Liquid Crystal Display Structure</i> .....	58
5.1.1.	<i>Liquid Crystal</i> .....	58
5.1.2.	<i>Liquid Crystal</i> .....	60
5.2	<i>Driving Method in LCD</i> .....	62
5.2.1	<i>Gamma Correction</i> .....	62
5.2.2	<i>Driving Method</i> .....	63
5.2	<i>Periphery Circuit Block</i> .....	66
5.2.1	<i>Scan Driver Circuit</i> .....	68
5.2.2	<i>Data Driver Circuit</i> .....	69
<b>CHAPTER 6</b>		
<i>Basic Understanding of Digital-to-Analog Converter</i> .....		
		<b>71</b>
6.1	<i>Ideal D/A Converter</i> .....	72
6.2	<i>Performance Metrics</i> .....	73
6.2.1	<i>Static Performance</i> .....	73
6.2.1.1	<i>Offset Error</i> .....	73
6.2.1.2	<i>Gain Error</i> .....	74
6.2.1.3	<i>Differential Non-Linearity (DNL)</i> .....	74
6.2.1.4	<i>Integral Non-Linearity (INL)</i> .....	75

6.2.1.5 Monotonicity.....	76
6.2.2 Dynamic Performance.....	76
6.2.2.1 Settling Time.....	77
6.2.2.2 Glitch.....	78
6.3 DAC for LCD column driver.....	79
6.3.1 Resistor-String DAC.....	79
6.3.2 Charge-Redistribution DAC.....	80
6.4 Summary.....	81
<b>CHAPTER 7</b>	
<b>A LCD Column Driver Using a Switch Capacitor DAC.....</b>	<b>82</b>
7.1 Introduction.....	82
7.2 Column Driver Architecture.....	83
7.3 Cyclic Switched Capacitor DAC.....	84
7.4 Simulation Result.....	98
7.5 Summary.....	99
<b>CHAPTER 8</b>	
<b>Test Setup and Measurement Results.....</b>	<b>100</b>
8.2 Measuring Environment.....	100
8.2.1 Power Supply Regulator.....	102
8.2.2 Single-to-Differential Transformer.....	103
8.2.3 Reference Voltage Generator.....	104
8.5 Summary.....	109
<b>CHAPTER 9</b>	
<b>Conclusions and Future Works.....</b>	<b>110</b>
9.1 Conclusions.....	110
9.2 Future Works.....	111
<b>Bibliography.....</b>	<b>112</b>

# ***LIST OF FIGURES***

<u>Figure</u>	<u>Page</u>
Fig. 2.1 Performance of the SFDR.....	7
Fig. 2.2 Performance characteristic of a sigma-delta modulator.....	8
Fig. 2.3 The sampling spectral.....	9
Fig. 2.4 Aliasing phenomenon.....	10
Fig. 2.5 Analog-to-digital conversion.....	10
Fig. 2.6 M-step mid-rise quantizer (M is odd) (a) transfer curve (b) error function.....	12
Fig. 2.7 M-step mid-tread quantizer (M is even) (a) transfer curve (b) error function.....	12
Fig. 2.8 (a) Probability density function of quantization noise (b) power spectral density of quantization noise.....	14
Fig. 2.9 Power spectral density (a) without oversampling (b) with oversampling.....	15
Fig. 2.10 (a) A general noise-shaping delta-sigma modulator (b) Linear model of the modulator showing injected quantization noise.....	16
Fig. 2.11 A first-order lowpass sigma-delta modulator.....	18
Fig. 2.12 A second-order lowpass sigma-delta modulator.....	21
Fig. 2.13 Comparison with different noise shaping transfer functions .....	21
Fig. 2.14 The block diagram of the L-order sigma-delta modulator.....	22
Fig. 2.15 Empirical SQNR limit for 1-bit modulators of order N.....	23
Fig. 3.1 (a) A first order CTSDM (b) A first order DT SDM.....	25
Fig. 3.2 The loop filter representation for (a) DT modulator and (b) CT modulator.....	27
Fig. 3.3 DAC feedback pulse shapes (a) NRZ (b) RZ (c) HRZ.....	29
Fig. 3.4 A fully differential integrator with finite gain and bandwidth .....	32
Fig. 3.5 DAC feedback impulse response including Excess Loop Delay (a) NRZ (b) RZ (c) HRZ.....	33
Fig. 3.6 Continuous-Time $\Delta \Sigma$ modulator with zero-order loop compensation .....	34
Fig. 3.7 Model of the jitter-induced noise for NRZ feedback DAC.....	35

Fig. 3.8 Error sequence energy in different DAC shapes.....	36
Fig. 4.1 The architecture of CT $\Delta \Sigma$ modulator using feedback resistors .....	38
Fig. 4.2 Pole-zero plot and PSD of CRFB.....	39
Fig. 4.3 (a) Maximum out-of-band gain of the NTF versus the peak SNR (b) Input level versus the SNR in system level.....	42
Fig. 4.4 The system simulation of CT $\Delta \Sigma$ modulator using feedback resistors.....	42
Fig. 4.5 Simulated SNDR for -7dBFS input under the variation of the time constant.....	43
Fig. 4.6 Simulated SNDR for -7dBFS input under the effect of the clock jitter.....	44
Fig. 4.7 Behavior model simulation result.....	45
Fig. 4.8 Simplified block diagram of the CT third-order modulator....	46
Fig. 4.9 Folded cascode opamp with p-type input.....	47
Fig. 4.10 Frequency response of the Amplifier.....	48
Fig. 4.11 Schematic of CMFB circuit.....	50
Fig. 4.12 (a) A cross-coupled preamplifier and (b) Low-offset regenerative latch.....	51
Fig. 4.13 Simulation result of the comparator.....	52
Fig. 4.14 Active-RC integrator with current steering DAC.....	53
Fig. 4.15 Low-jitter clock generator.....	54
Fig. 4.16 Tuning circuit.....	55
Fig. 4.17 Simulated power spectral density of this work (a) TT (b) FF (c) SS corner.....	56
Fig. 4.18 Chip photo of this work using feedback resistors.....	57
Fig. 5.1 Phase variation of liquid crystal in different temperature	58
Fig. 5.2 Transparency of TN and STN in different voltage.....	60
Fig. 5.3 Cross section of LCD model.....	61
Fig. 5.4 The liquid crystal operates in normally white case: (a) light can pass and (b) light is blocked.....	62
Fig. 5.5 (a) The relationship between digital input codes and input voltage across liquid crystals and (b) the smooth curve between digital input codes and light transmission rate.....	63
Fig. 5.6 Inversion of LCD panel.....	64
Fig. 5.7 The operational waveform of direct driving method.....	66



Fig. 5.8	The operational waveform of AC modulation driving method....	66
Fig. 5.9	Block diagram of the LCD panel driver circuits.....	67
Fig. 5.10	The pixel layout structure of active matrix cell on LCD panel .....	68
Fig. 5.11	The block diagram of scanning driver.....	68
Fig. 5.12	RC (resister and capacitor) ladder of scanning line.....	69
Fig. 5.13	The block diagram of data driver.....	70
Fig. 6.1	Digital-to-analog conversion.....	71
Fig. 6.2	Block diagram if a n-bit DAC.....	72
Fig. 6.3	Non-ideal transfer curve with offset error.....	73
Fig. 6.4	Non-ideal transfer curve with gain error.....	74
Fig. 6.5	Non-ideal transfer function with INL and DNL error of DAC..	75
Fig. 6.6	A non-monotonic DAC.....	76
Fig. 6.7	Actual output signal and ideal output signal (dash) of a DAC .....	77
Fig. 6.8	Glitch output.....	78
Fig. 6.9	DAC using tree-like decoder.....	80
Fig. 6.10	DAC using digital decoder.....	80
Fig. 7.1	New column driver block diagram [5].....	83
Fig. 7.2	Stacked amplifier configuration.....	84
Fig. 7.3	Simplified schematic of lower DAC.....	85
Fig. 7.4	DAC output versus linear and LCD response [5].....	86
Fig. 7.5	DAC conversion sequence (a) $\phi 10$ and rest; (b) $\phi 20$ ; (c) $\phi 11$ ; .....	87
Fig. 7.6	Control signal timing.....	87
Fig. 7.7	DAC amplifier schematic.....	91
Fig. 7.8	Small signal representation of output stage with cascade Miller compensation [5].....	94
Fig. 7.9	Lower DAC simulation result.....	98
Fig. 7.10	Higher DAC simulation result.....	99
Fig. 8.1	Test setup.....	101
Fig. 8.2	Function generator hp 8656B for input signal.....	101
Fig. 8.3	Function generator ROHDE & SCHWARZ SML03 for clock.....	101
Fig. 8.4	Logic analyzer Agilent 16902A.....	102
Fig. 8.5	Power supply regulator.....	103

Fig. 8.6 Single-to-differential transformer.....103  
Fig. 8.7 Reference voltage generator.....104  
Fig. 8.8 PCB of the CT modulator.....105  
Fig. 8.9 (a) Pin configurations (b) Pin assignments of the CT modulator  
.....105  
Fig. 8.10 The die photo of the CT SDM.....106  
Fig. 8.11 Measured power spectral density of the CT modulator.....107  
Fig. 8.12 Post-simulation power spectral density of the CT modulator  
.....107  
Fig. 8.13 Dynamic range plot of the CT modualtor.....108



# ***LIST OF TABLES***

<u>Table</u>	<u>Page</u>
Table 2.1 Properties of quantizers in Figs 2.6 and 2.7.....	13
Table 3. 1 Comparison with the main advantages of CT and DT SDM .....	26
Table 3.2 S-domain equivalent for z-domain partial expansion .....	30
Table 4.1 Zero placement for minimum in-band noise .....	39
Table 4.2 Performance of the Amplifier .....	48
Table 4.3 Truth table of SR latch .....	52
Table 4.4 Performance summary of this work .....	56
Table 7.1 Performance of the Amplifier.....	98
Table 8.1 Measurement results of the CT modulator .....	108
Table 8.2 Comparison between DT SDM and the CT modulator .....	109

