CHAPTER 1
Introduction

1.1 Motivation

In many signal processing application, the data converter is a critical building block limiting the accuracy and speed of the overall system. Data converters have analog-to-digital converter (ADC) and digital-to-analog converter (DAC) two types.

Sigma-delta analog-to-digital converter (ADC) is traditionally used in instrumentation, voice, and audio applications that are low signal bandwidth and high resolution. In recent years, there has been a growing trend to move ADC towards the system front-end. This implies that more signal processing is shifted from analog domain to digital domain. Due to the scaling in VLSI technology, high performance digital systems can be realized. However, ADC has to provide higher dynamic range in the interface between analog and digital data. Therefore, sigma-delta ADC which can achieve high resolution with wide input bandwidth for wireless and wireline communication systems becomes more and more important [1] [2].

In sigma-delta ADC, the use of continuous-time (CT) loop filter provides several advantages over discrete-time (DT) implementations. Without critical slewing and settling issues, as in switched-capacitor

circuits, CT integrators are often promised to achieve better power-performance efficiency [3]. Moreover, CT integrators are praised for better noise immunity due to their inherent anti-aliasing filtering which are especially advantageous in RF receivers [4]. However, CT integrators are sensitive to process variation thereby require extra tuning circuit to adjust the time constant. DT integrators, on the contrary, set the pole-zero locations by capacitor ratios, which are highly accurate. Another advantage of using DT loop filter is that its signal transfer function and noise transfer function scale with the clock frequency which could be handy for a multi-standard system design. Alternative hybrid CT/DT loop filter approach tends to exploit the performance by keeping all the pros.

Liquid crystal displays (LCD) are expected to be the dominant technology for flat panel televisions. The main consideration of LCD performance is high resolution, wide view-angle, and high contrast ratio, etc. Besides, a current trend of LCD is low power, light weight, and small volume. LCD column driver is one of digital-to-analog converter's applications. Historically, column driver have employed a 64 or 256 element resistor string DAC to provide the analog voltage, as presented in Fig 1.1. A unity gain amplifier for each output has been incorporated in the larger displays to provide a low impedance output. But resistor string DAC has follow problems [5]:

- The inverse transfer curve is hardwired on each part, requiring a custom die for each type of LCD panel.
- The resistor string is not accurate enough. To obtain consistent voltages from die to die, 16 taps are brought out, wired together, and driven externally.
- The current in the resistor string is too high for mounting the die directly on the LCD glass.
- The die size becomes excessive for 10 bits per color.
- Supporting independent inverse transfer curves for each color increases the die size.

We have developed a complete new system using a linear DAC in the column driver. The linear DAC keeps the die size small as well as supporting additional features.

1.2 Thesis Organization

This thesis is organized into seven chapters.

Chapter 1 briefly introduces the motivation of the thesis.

Chapter 2 first explains the performance parameters of the sigma-delta A/D and describes the background of the sigma-delta A/D conversion. Then, the concepts and advantages of quantization, oversampling and noise shaping are introduced. Finally, the common

architectures of the sigma-delta modulator, single-loop and multi-stage, are illustrated and discussed.

Chapter 3 introduces the comparison of the CT and DT loop filter. Then, how to transform between the DT and the CT loop filter is described and the non-idealities of the CT modulator are explained.

Chapter 4 presents a continuous-time single-bit active-RC sigma-delta modulator for 1 MHz bandwidth. The design of the loop is illustrated, including the architecture and coefficients. The system and circuit level designs are introduced in detail. Non-idealities and important simulation results are included. Finally, in mixed-signal design, the considerations of the layout are discussed.

Chapter 5 introduces the LIQUID CRYSTAL DISPLAY, first, the structure of liquid crystal display is explained. Then we describe the driving method of liquid crystal display. Finally, we introduce the periphery circuit block slightly.

Chapter 6 first introduces the ideal DAC. Then explains the performance parameters of the DAC and describes the background of some different LCD column driver types.

Chapter 7 presents a LCD column driver using a switch capacitor DAC, first, we explain the problems of the R-string DACs. Then we describe the new architecture of LCD column driver and the operation of switch

capacitor DAC. Finally, we discuss the design of circuit about the DAC.

Chapter 8 presents the testing environment, including the components on the printed circuit board (PCB) and instruments. The measurement results of the continuous-time single-bit active-RC sigma-delta modulator for 1 MHz bandwidth is shown and summarized.

Finally, the conclusions and the future works of this thesis are summarized in Chapter 9.

CHAPTER 2
Basic Understanding of Sigma-Delta A/D Conversion

In this chapter, first, the performance parameters of the sigma-delta A/D are explained. Then we describe the background of the sigma-delta A/D conversion and introduce the concepts of quantization, oversampling and noise shaping. Finally, the tradeoffs of the various sigma-delta modulator architectures will be discussed.

2.1 Performance Parameters

There are commonly the most important performance parameters when sigma-delta A/D is compared. These performance parameters are described as follows:

2.1.1 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio of an A/D is the ratio of the signal power to the noise power over the interest band at the output of a converter. The theoretical value of SNR for sinusoidal inputs in a Nyquist rate A/D is given by

$$SNR_{max} = 6.02N + 1.76 \qquad (2.1)$$

The derivation of the equation (2.1) is described in section 2.3

2.1.2 Signal-to-Noise and Distortion Ratio (SNDR)

The signal-to-noise and distortion ratio of an A/D is the ratio of the signal power to the noise and all distortion power over the interest band at the output of a converter. In general, the SNDR is lower than SNR due to the distortion power.

2.1.3 Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is defined as the ratio of the signal power to the maximum distortion component in the range of interest, as shown in Fig. 2.1.

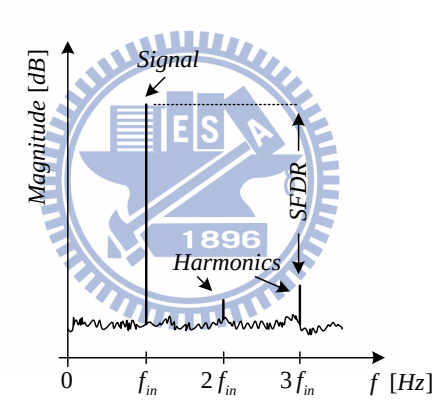


Fig. 2.1 Performance of the SFDR

2.1.4 Dynamic Range (DR)

The dynamic range of an A/D for sinusoidal inputs is defined as the ratio of the maximum signal power to the signal power for a small input which the SNR is unity [6].

2.1.5 Effective Number of Bits (ENOB)

Equation (2.2) relates the number of bits to the SNDR used in an A/D when the input signal is a sinusoidal.

$$ENOB = \frac{SNDR - 1.76}{6.02} bits \tag{2.2}$$

2.1.6 Overload Level (OL)

Overload level is defined as the maximum input sinusoidal signal which the structure still operates correctly. Usually, the maximum stable amplitude is at the 6dB reduction of the peak SNR.

The performance parameters discussed above are summarized in Fig. 2.2, where SNR_p are the peak SNR, respectively [7].

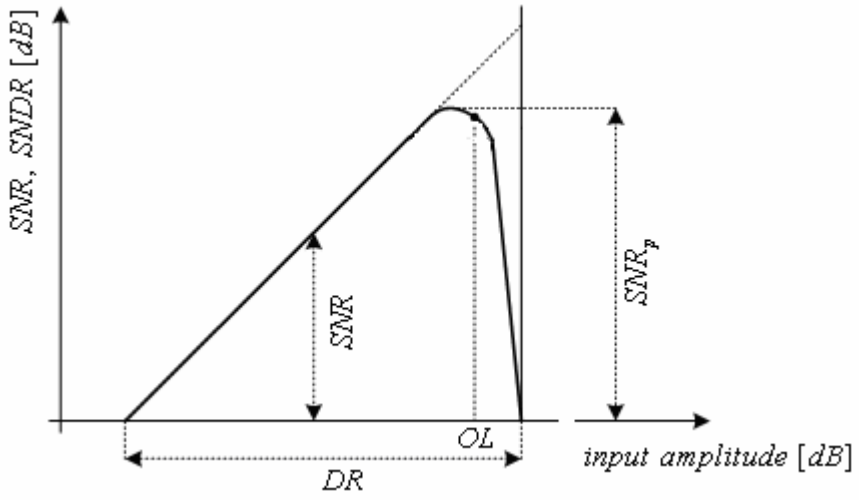


Fig. 2.2 Performance characteristic of a sigma-delta modulator

2.2 Sampling and Quantization

In order to properly interface the analog world which is composed of continuous-time signal (e.g. voice, audio or video) with the digital signal processor which can only process discrete-time signal, analog-to-digital conversion is required. We describe it into two basic operations: uniform sampling in time and quantization in amplitude.

Under the assumption that the signal information of the continuous input waveform $u(t)$ is contained in the signal band, i.e., $|f_{sig}| \leq f_B$, where f_B is defined as the signal bandwidth, the sampling in time is a completely invertible process. This is easily understood when considering a quantization in time as a periodization in frequency [8], which is illustrated in Fig. 2.1. There, the considered input signal is sampled at uniform time intervals T_S, the sampling time, or with a fixed frequency, f_S, resulting in a periodicity of the original signal

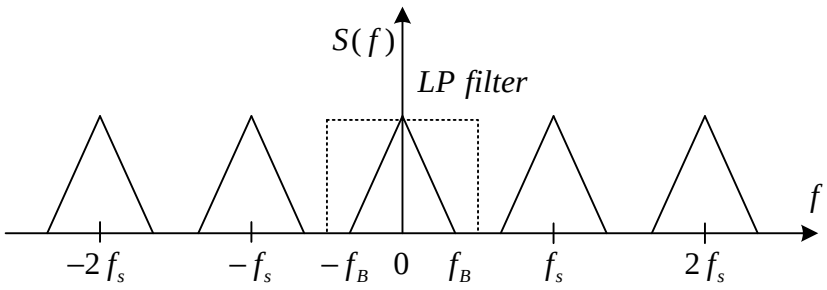


Fig. 2.3 The sampling spectral

spectrum at multiples of f_S. From Fig. 2.3 it is obvious that by sample

low-pass filtering, the original base-band spectrum can be reconstructed, provided that the sampling itself does not result in overlap or aliased regions. This is achieved when:

$$f_S \geq 2 f_B = f_N \tag{2.3}$$

which is known as the *Nyquist theorem*, where f_N is the *Nyquist frequency*. Otherwise, the aliasing maybe occur, as shown in Fig. 2.4. To assure a proper sampling operation, the condition in (2.3) is enforced by an analog filter preceding the sampling operation, called the *antialiasing filter* (AAF).

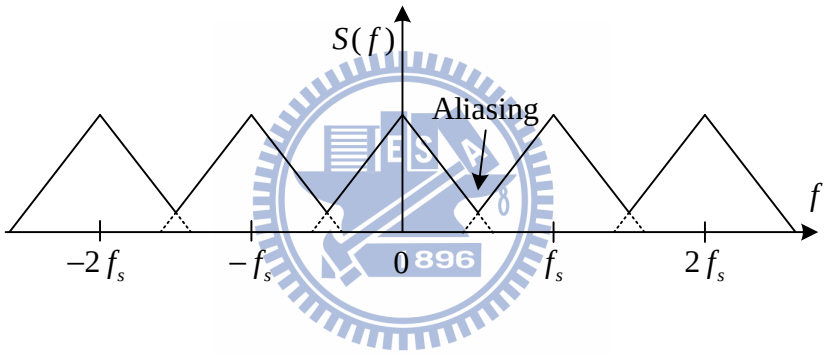


Fig. 2.4 Aliasing phenomenon

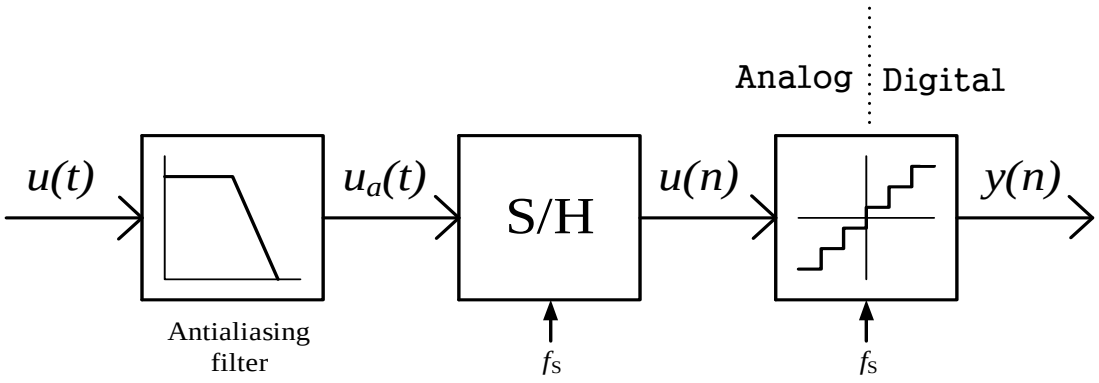


Fig. 2.5 Analog-to-digital conversion

The basic ADC structure is shown in Fig. 2.5. An ADC working with a sampling frequency of f_N is called a *Nyquist Rate* converter. But in real implementations, this results in a zero transition band for the filter to cut off the unwanted high frequency signals, making it hard to design. On the other hand, analog filters with a gentle roll in their transition band are less costly, easier to design; require less power, and smaller chip area while introducing less phase distortion. Therefore, many ADCs work with sampling rates higher than f_N , and one defines:

$$OSR = \frac{f_S}{2 f_N} \tag{2.4}$$

as the *oversampling ratio* of the ADC.

The process of quantization in amplitude encodes a continuous range of analog values into a set of discrete levels. The device which realizes the quantization is called a quantizer or ideal A/D converter. There are two types of the quantizers which are mid-rise and mid-tread [9], as shown in Figs. 2.6 and 2.7. In Fig. 2.6(a), the mid-rise quantizer has $u=0$ in a rise of v . On the other hand, $u=0$ occurs in the middle of a flat portion of the curve and hence it is called a mid-tread quantizer. In ideal both cases, the straight line $v=ku$ is the desirable A/D transfer curve, where the gain k of the quantizer is determined by the ratio of the step size to the adjacent input thresholds known as the least-significant bit size (LSB size or Δ). The deviation between the straight line $v=ku$ and the real A/D characteristic is called quantization error or quantization noise. Figs. 2.6 (b) and 2.7 (b) illustrate the quantization error e. In the range from $-M-1$ to $M+1$, the quantization error is within $\pm\Delta/2$.

This range is called no-overload input range and the difference between lowest and highest levels is named full scale (FS). Therefore, the FS is equal to

$$FS = \Delta \cdot 2^N \tag{2.5}$$

where N is quantizer resolution. Table 2.1 summarizes the quantizers of the Figs 2.6 and 2.7.

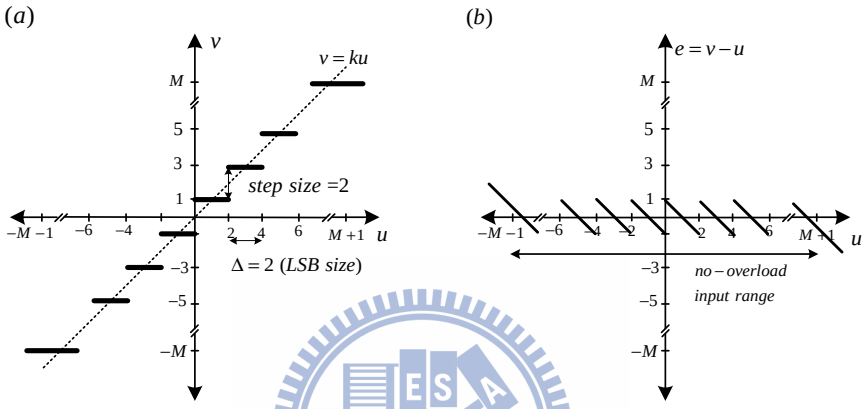


Fig. 2.6 M-step mid-rise quantizer (M is odd) (a) transfer curve (b) error function

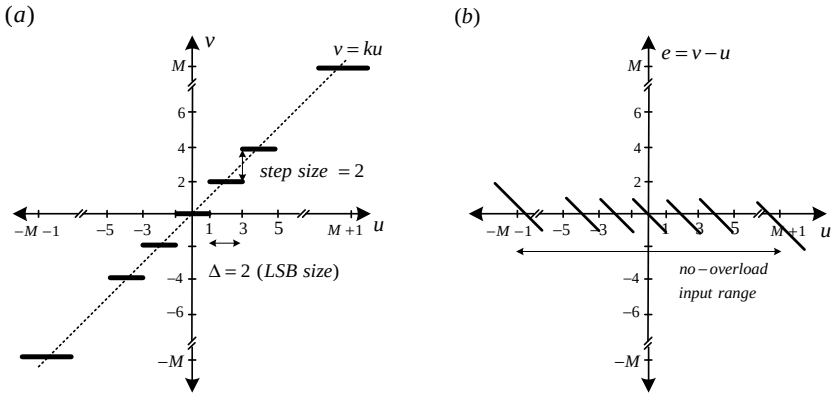


Fig. 2.7 M-step mid-tread quantizer (M is even) (a) transfer curve (b) error function

Table 2.1 Properties of quantizers in Figs 2.6 and 2.7

Parameter	Value
input step size (LSB size)	2
output step size	2
number of steps	M
number of levels	M+1
number of bits	$[\log_2(M+1)]$
no-overload input range	[-(M+1), M+1]
full-scale	2M
input thresholds	0, ±2, ….., ±(M-1), M odd ±1, ±3, ….., ±(M-1), M enen
output levels	±1, ±3, ….., ±M-, M odd 0, ±2, ±4….., ±M, M enen

The ideal quantizer is a deterministic device. The output v and hence the error q are fully determined by the input *y*. However, under certain circumstances, for example, if the input y stays within the non-overload input range of the quantizer, and changes by sufficiently large amounts from sample to sample so that its position within a quantization interval is essentially random, then it is permissible to assume that *q* is a white noise process with samples uniformly distributed between $-V_{LSB}/2$ and $+V_{LSB}/2$. The probability density function (PDF) and power spectral density (PSD) of the quantization noise are shown in Fig. 2.8.

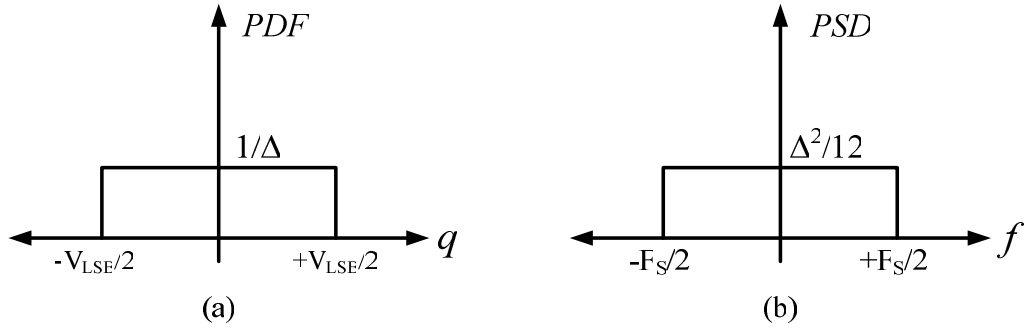


Fig. 2.8 (a) Probability density function of quantization noise (b) power spectral density of quantization noise

The impact of the quantization noise on the ADC's performance can be found by calculating its maximum signal-to-quantization-noise ratio (SQNR). This parameter is obtained by dividing the power of a sinusoidal input signal by the power of the quantization noise. The power of a sinusoidal signal is given by $Amp^2/2$, where Amp is the amplitude of the signal. The power of the quantization noise is given in (2.6).

$$\sigma_q^2 = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} q^2 dq = \frac{\Delta^2}{12} \tag{2.6}$$

To get the SQNR, Amp should be equal to half of the non-overload input range of the quantizer, which is $V_{Ref}+V_{LSB}/2$.

$$SQNR = \frac{\left(V_{Ref} + \frac{\Delta}{2}\right)^2}{\frac{\Delta^2}{12}} = \frac{\left(2^{N-1}\Delta\right)^2}{\frac{\Delta^2}{12}} = \frac{3}{2} 2^{2N} \tag{2.7}$$

(2.7) is expressed in dB, this becomes (2.8), which is widely used to assess the performance of the data converter.

$$SQNR\ [dB] = 10 \log_{10} SQNR = 6.02N + 1.76 \tag{2.8}$$

2.3 Oversampling

In (2.6), we calculate the power of quantization noise is to integrate the power spectral density over the full bandwidth. It is obvious that if the bandwidth of interest is much lower than the bandwidth which we interest, the resolution of the ADC can be improved by filtering the output to the desired bandwidth which reduces the total power of the quantization noise. This technique, illustrated in Fig. 2.9, is called oversampling.

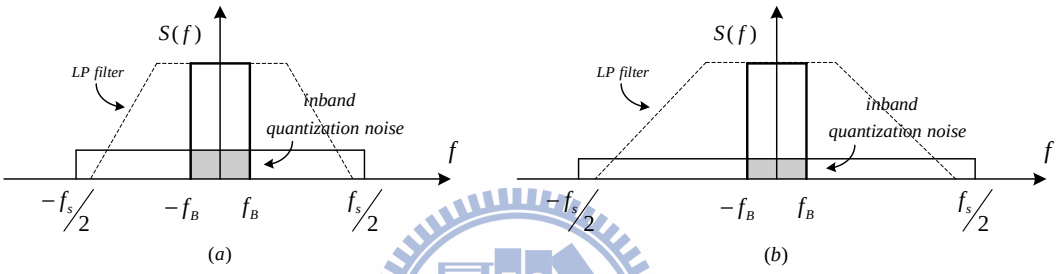


Fig. 2.9 Power spectral density (a) without oversampling (b) with oversampling

Due to the oversampling technique, the inband quantization noise is reduced. Consequently, the inband quantization noise power becomes

$$P_e = \frac{1}{f_s}\int_{-f_B}^{f_B} \sigma_e^2 df = \frac{\Delta^2}{12}\frac{2f_B}{f_s} = \frac{\Delta^2}{12}\frac{1}{OSR} \tag{2.9}$$

The SNR of a oversampling converters is as follows:

$$\begin{aligned} SNR_{max} &= 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(OSR) \\ &= 6.02N + 1.76 + 10\log(OSR) \end{aligned} \tag{2.10}$$

Compared to (2.10), the SNR is enhanced by 3dB with doubling OSR. Therefore, the oversampling gives a SNR improvement with the OSR at a rate of 3dB/octave, or 0.5bit/octave.[10]

2.4 Noise shaping

In section 2.3, we discuss that oversampling can used to trade speed for resolution of ADC. But the quantization noise also has a flat power spectral density over the full bandwidth $[-f_S/2, f_S/2]$. A more efficient way to use oversampling is to shape the spectral density such that most of the quantization noise power is outside the band of interest.

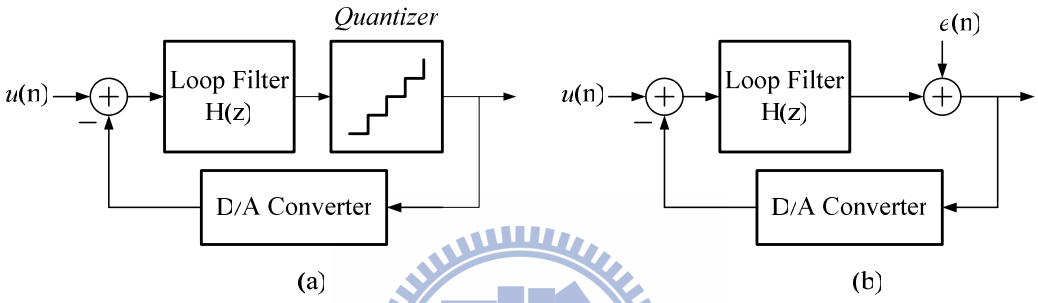


Fig. 2.10 (a) A general noise-shaping delta-sigma modulator (b) Linear model of the modulator showing injected quantization noise

A general noise shaping sigma-delta modulator (SDM) is shown in Fig. 2.10 (a), where $H(z)$ is loop filter. Assuming the input signal and the quantization noise are independent signals simplifying the analysis. The linear model of the modulator in z domain is shown in Fig. 2.10 (b). With this linear model, we can derive a STF and a NTF as defined

$$STF(z) \equiv \frac{V(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{2.11}$$

$$NTF(z) \equiv \frac{V(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.12}$$

According to (2.12), we can find out that the zeros of $NTF(z)$ is equal to the poles of $H(z)$. It means that when $H(z)$ go to infinity, $NTF(z)$

will be zero. In other words, by choosing $H(z)$ such that its magnitude is large in signal bandwidth, $STF(z)$ should approximate unity and $NTF(z)$ should be close zero over the same bandwidth. For the output signal, we can express it in linear combination of the input signal and the noise signal in (2.13), which are filtered by STF and NTF, respectively.

$$V(z) = STF(z)U(z) + NTF(z)E(z) \tag{2.13}$$

In general cases, the $STF(z)$ has all-pass or lowpass frequency response and the $NTF(z)$ has highpass characteristic. Based on (2.13), the inband quantization noise can be shaped to high frequency band and then it doesn't affect the input signal [11]. Therefore, the SNR can be improved effectively by using noise shaping.

2.5 First-order Sigma-Delta Modulator

In the previous section, we know that a first-order noise shaping, the $NTF(z)$ should have a zero at dc (i.e., z=1), that is a lowpass frequency response, equivalently $H(z)$ has a pole at dc. So the quantization noise has highpass characteristic. By letting $H(z)$ be a discrete-time integrator, the function is

$$H(z) = \frac{1}{z-1} \tag{2.14}$$

where $H(z)$ has a pole at dc (i.e., z=1). For this choice, the block diagram in z domain is shown in Fig. 2.11. In frequency domain, the $STF(z)$ is given by

$$STF(z) \equiv \frac{V(z)}{U(z)} = \frac{\frac{1}{z-1}}{1+\frac{1}{z-1}} = z^{-1} \tag{2.15}$$

and the $NTF(z)$ is given by

$$NTF(z) \equiv \frac{V(z)}{E(z)} = \frac{1}{1+\frac{1}{z-1}} = 1-z^{-1} \tag{2.16}$$

According to (2.13), the output signal becomes

$$V(z) = z^{-1} \cdot U(z) + (1-z^{-1}) \cdot E(z) \tag{2.17}$$

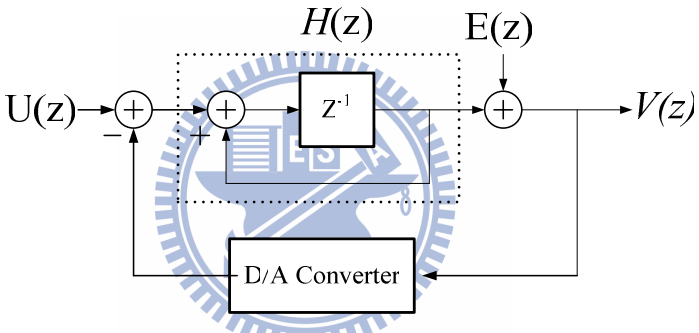


Fig. 2.11 A first-order lowpass sigma-delta modulator

We see that the input signal is just a delay through the input to the output, and the quantization noise is through a discrete-time differentiator (i.e., a high-pass filter) to the output. We are interesting in the magnitude of the noise transfer function, $|NTF(f)|$, we let $z = e^{j\omega T} = e^{j2\pi f/f_S}$ and get the following:

$$\begin{aligned} NTF(f) &= 1 - e^{-j2\pi f/f_S} \\ &= \frac{e^{j\pi f/f_S} - e^{-j\pi f/f_S}}{2j} \times 2j \times e^{-j\pi f/f_S} \\ &= \sin\left(\frac{\pi f}{f_S}\right) \times 2j \times e^{-j\pi f/f_S} \end{aligned} \tag{2.18}$$

Taking the magnitude of both sides, we have the high-pass function

$$|NTF(f)| = 2\sin(\frac{\pi f}{f_S}) \tag{2.19}$$

Now we can integrate the quantization noise power over the frequency bandwidth we interest as below

$$P_e = \int_{-f_B}^{f_B} S_e^2(f)|NTF(f)|^2 df$$

$$= \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_S}\left[2\sin\left(\frac{\pi f}{f_S}\right)\right]^2 df \tag{2.20}$$

When $f_B \ll f_S$ (i.e., OSR>>1), we can approximate $\sin(\frac{\pi f}{f_S})$ to be $(\frac{\pi f}{f_S})$, so we have

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_B}{f_S}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{2.21}$$

Now we can estimate the maximum SNR by assuming the input signal having maximum amplitude. We can obtain as

$$SNR_{max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{3}{\pi^2}(OSR)^3\right] \tag{2.22}$$
$$= 6.02N + 1.76 - 5.17 + 30\log(OSR)$$

We can double OSR, the SNR performance is improved by 9dB, i.e., 1.5bit/octave. Compared to (2.12), the SNR has the improvement of 1bit/octave.

2.6 Second-order Sigma-Delta Modulator

To realize a second-order sigma-delta modulator, the $NTF(z)$ should be a second-order highpass function. The block diagram of the modulator is shown in Fig. 2.12. For this modulator, the $STF(z)$ is given by

$$STF(z) = z^{-1} \tag{2.23}$$

and the $NTF(z)$ is given by

$$NTF(z) = \left(1 - z^{-1}\right)^2 \tag{2.24}$$

Similarly, we are interested in the squared magnitude of the $NTF(z)$. It is

$$\left|NTF(f)\right|^2 = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^4 \tag{2.25}$$

Using the same assumption OSR>>1, the quantization noise power over the frequency band of interest becomes

$$P_e = \int_{-f_B}^{f_B} S_e(f)\left|NTF(f)\right|^2 df = \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^4}{5}\right)\left(\frac{2f_B}{f_s}\right)^5 = \frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5 \tag{2.26}$$

Again, the SNR for this case is given by

$$\begin{aligned} SNR_{max} &= 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right] \\ &= 6.02N + 1.76 - 12.9 + 50\log(OSR) \end{aligned} \tag{2.27}$$

We can see that the second-order noise shaping can give an SNR improvement for 15 dB or 2.5 bits by doubling the OSR

Fig. 2.13 shows the noise-shaping curves compared with shape of zero-, first-, second- and third-order. The noise power decreases as the noise-shaping order increases over the band which we interest. But the out-of-band noise power increases for the higher-order modulators.

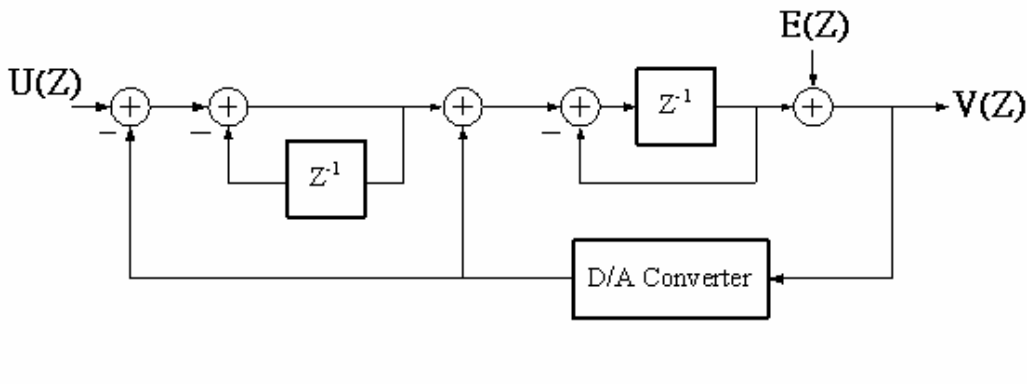


Fig. 2.12 A second-order lowpass sigma-delta modulator

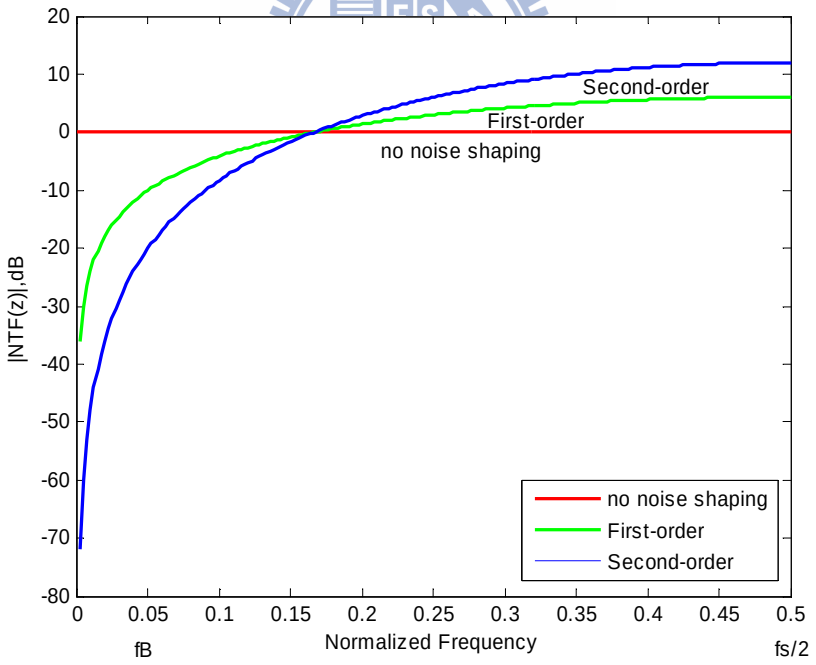


Fig. 2.13 Comparison with different noise shaping transfer functions

2.7 High-order Sigma-Delta Modulator

Fig. 2.14 shows the block diagram of the L-order sigma-delta modulator. As the first- and second-order SDM, the $NTF(z)$ of the L-order SDM should be chosen to have an L-order highpass function. This gives

$$NTF(z) = (1 - z^{-1})^{L} \tag{2.28}$$

We let $z = e^{j\omega T} = e^{j2\pi f / f_S}$ and get the magnitude response

$$|NTF(f)| = \left[2\sin\left(\frac{\pi f}{f_S}\right) \right]^{2} \tag{2.29}$$

Integrating the quantization noise power over the frequency band which we interest and using the approximation, we can get the result:

$$\begin{aligned} P_e &= \int_{-f_B}^{f_B} S_e^{\,2}(f)\,|NTF(f)|^2\,df \\ &= \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_S}\left[2\sin\left(\frac{\pi f}{f_S}\right)\right]^{2L} df \\ &= \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{2f_B}{f_S}\right)^{2L+1} = \frac{\Delta^2 \pi^{2L}}{12\,(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1} \end{aligned} \tag{2.30}$$

Again, assuming the maximum signal power is used, the maximum SNR for this case is given by

$$\begin{aligned} SNR_{max} &= 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{2L+1}{\pi^{2L}}(OSR)^{2L+1}\right] \\ &= 6.02N + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \end{aligned} \tag{2.31}$$

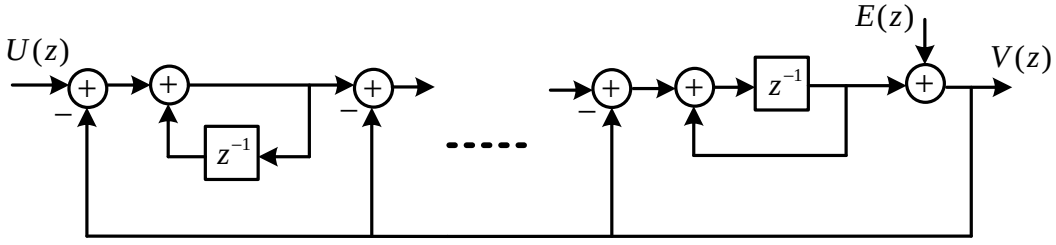


Fig. 2.14 The block diagram of the L-order sigma-delta modulator

From (2.32), the SNR performance can be improved by (6L+3) dB with doubling OSR, or at a rate of (L+0.5) bit/octave. However, higher than second-order SDM suffers from potential instability due to the accumulation of large signals in the integrators. Consequently, stability problems reduce the achievable resolution to a lower value than the equation (2.32). Fig. 2.15 shows the SQNR tradeoff between order and OSR.

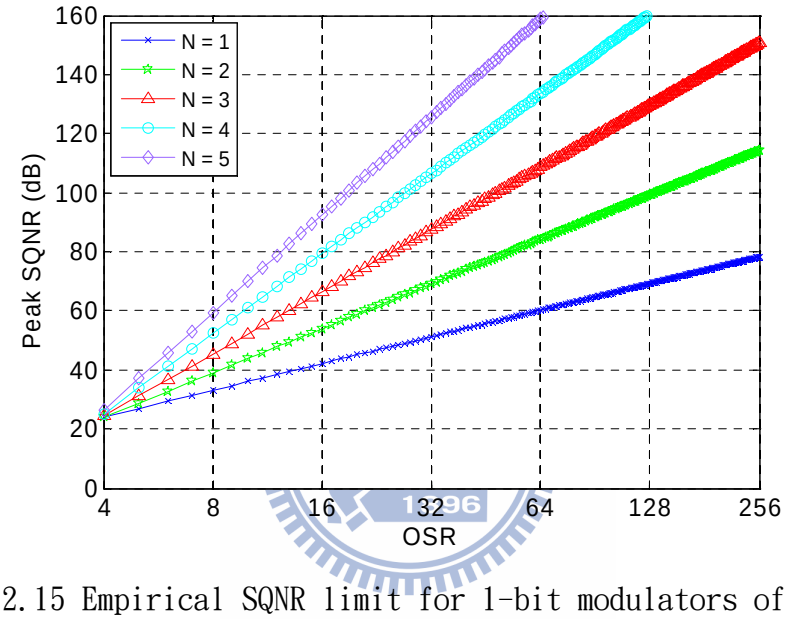


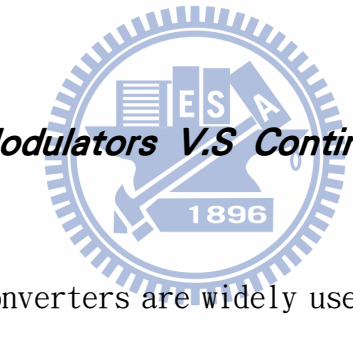
Fig. 2.15 Empirical SQNR limit for 1-bit modulators of order N

2.8 Summary

In this chapter, performance parameters of a sigma-delta modulator are first explained. Then, we introduce the basic concept of the SDM and the fundamental principles of how a modulator works are described. Through the use of oversampling and noise shaping, the SNR performance can be improved in the band of interest. Finally, the common architectures of the SDM, single-loop and multi-stage, are illustrated and discussed.

CHAPTER 3
Continuous-Time Sigma-Delta Modulators

In this chapter, we will show that the DT ΔΣ modulator loop filter function transform into CT ΔΣ modulator and the procedure to choose the feedback DAC pulse shapes. Besides, various non-idealities will affect the performance, even the stability of the CT ΔΣ modulator. These non-idealities, including finite OpAmp gain and gain-bandwidth, excess loop delay, element mismatch in the multi-bit feedback DAC and clock jitter, would be analyzed in detail.



3.1 Discrete-Time Modulators V.S Continuous-Time Modulators

Sigma-delta A/D converters are widely used in wireless and wireline communication system. In recent years, continuous-time (CT) sigma-delta A/D gains growing interest in wireless application for their lower power consumption and wider input bandwidth as compared to the discrete-time counterparts. In other words, the opamp of CT SDM can be relaxed at speed requirements or CT SDM can operate at higher sampling frequency. Moreover, CT SDM is praised for better noise immunity due to their inherent anti-aliasing filtering which are especially advantageous in RF receivers [4]. Besides, the absence of the switches makes CT SDM has less glitch and less digital switching noise.

DT SDM, on the contrary, is insensitivity to clock jitter and exact shape of opamp settling waveform as long as full settling occurs. Another advantage of DT SDM is that the integrator gain and transfer functions are accurately defined.

The main advantages of CT and DT SDM are summarized in Table3.1 and their block diagrams are shown in Fig. 3.1 [7] [9].

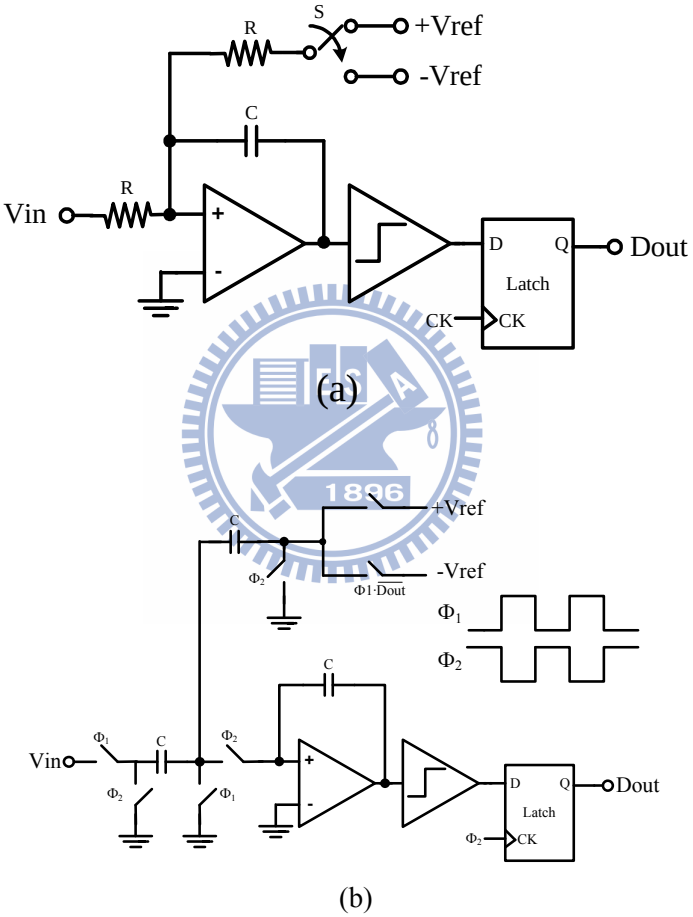


Fig. 3.1 (a) A first order CTSDM (b) A first order DT SDM

Table 3. 1 Comparison with the main advantages of CT and DT SDM

	Advantages
CT SDM	• Inherent anti-aliasing filter • Higher sampling frequency possible • Relaxed opamp speed requirements • Less glitch sensitive • Less digital switching noise • Lower simulation time (circuit level)
DT SDM	• Accurately defined integrator gains and transfer function by capacitor ratios • Transfer functions scaled with clock frequency • Low sensitivity to clock jitter • Low sensitivity to excess loop delay • Low sensitivity to DAC waveform • Lower simulation time (high level)

3.2 Transformation of a Discrete-Time to a Continuous-Time

3.2.1 Implus-Invariant transformation

In the previous section, we know why the CT SDM gains growing interest. Used sigma-delta toolbox [8], the DT loop filter can be obtained easily. By contrast, the loop filter design of a CT SDM is nontrivial because it has a strong dependence on the pulse shape of the feedback digital-to-analog converter (DAC). Fortunately, we can find a CT loop filter through the equivalent DT loop filter and transforming it to continuous-time.

In DT SDM, the sampling is at the front-end input while it is at the input of the quantizer in CT SDM, just like Fig. 3.2. But if they have

the same output sequences in the time domain for the same time instants, they can be considered equivalent.

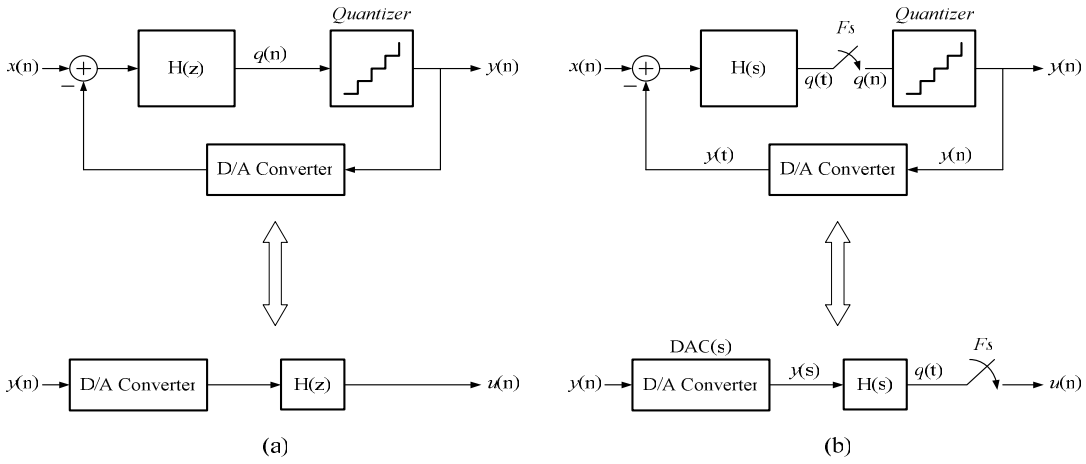


Fig. 3.2 The loop filter representation for (a) DT modulator and (b) CT modulator

As mentioned above, the two modulators are equivalent if their quantizers have the same inputs at each sampling instant, which means

$$x(n) = x(t)|_{t=nT_s} \tag{3.1}$$

This can be satisfied if their impulse responses are equal at each sampling instants. This results in the condition [11]

$$Z^{-1}\{H(z)\} = L^{-1}\{H_{DAC}(s)H(s)\}|_{t=nT_s} \tag{3.2}$$

or, in the time domain [12]

$$h(n) = [h_{DAC}(t) * h(t)]|_{t=nT_s} = \int_{-\infty}^{\infty} h_{DAC}(\tau) * h(t-\tau)d\tau|_{t=nT_s} \tag{3.3}$$

where $h_{DAC}(t)$ is the impulse response of the DAC. The transformation between CT and DT is called the impulse-invariant transformation, because it makes the open loop impulse response equal at the sampling times.

3.2.2 Synthesis of CTΔΣ Feedback DAC

To actually perform the Impulse Invariant Transformation, the continuous-time DAC feedback pulse shape has to be decided first. Different pulse shapes result in different transformations between the DT and CT modulators. We will shortly discuss their practical advantages. There are three commonly used rectangular DAC feedback pulses: non-return-to-zero (NRZ), return-to-zero (RZ) and half-delay-return-to-zero (HRZ) [12]. Their impulse responses are shown in Fig. 3.3. DACs with NRZ shapes provide constant output over a full period; DACs with RZ shapes produce constant valid output only from 0 to T/2 and DACs with HRZ produce a half clock cycle delayed version of RZ. The transfer function of NRZ, RZ and HRZ can be described by the same equation:

$$h_{DAC}(t)=\begin{cases}1, & \alpha \le t < \beta,\ 0 \le \alpha < \beta \le 1\\ 0, & otherwise\end{cases} \tag{3.4}$$

where α and β are feedback starting and ending times. So, the three rectangular DAC feedback pulses are

$$\begin{cases} NRZ & \alpha = 0, \quad \beta = 1 \\ RZ & \alpha = 0, \quad \beta = 0.5 \\ HRZ & \alpha = 0.5, \quad \beta = 0 \end{cases} \tag{3.5}$$

By the Laplace transform of (3.4), their responses in s-domain can be described as follows

$$H_{DAC}(s)=\frac{\exp(-\alpha s)-\exp(-\beta s)}{s} \tag{3.6}$$

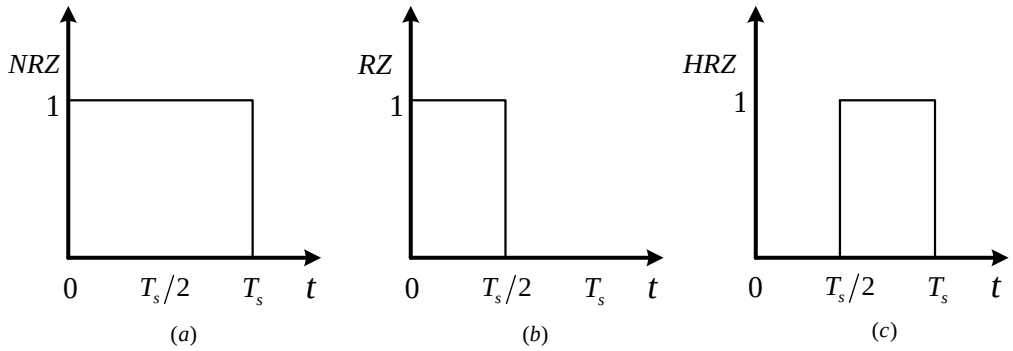


Fig. 3.3 DAC feedback pulse shapes (a) NRZ (b) RZ (c) HRZ

After determining the DAC feedback pulse shape and its response, impulse-invariant transformation can be used in following steps. First, we need to express the as a partial fraction expansion and then convert each partial fraction expansion from z-domain to s-domain. Finally, the can be derived by recombining the results.

Table 3.2 lists the results of impulse-invariant transformation between CT loop filters and DT loop filters for the commonly used DAC feedbacks [13]

Table 3.2 S-domain equivalent for z-domain partial expansion

z-domain partial fraction			s-domain equivalent
$\frac{z^{-1}}{1-z_k z^{-1}}$	NRZ	General z_k	$\frac{s_k}{z_k-1}\frac{1}{sT_s-s_k}$
		$z_k=1$	$\frac{1}{sT_s}$
	RZ	General z_k	$\frac{s_k}{z_k-z_k^{0.5}}\frac{1}{sT_s-s_k}$
		$z_k=1$	$\frac{2}{sT_s}$
	HRZ	General z_k	$\frac{s_k}{z_k^{0.5}-1}\frac{1}{sT_s-s_k}$
		$z_k=1$	$\frac{2}{sT_s}$
$\frac{z^{-2}}{(1-z_k z^{-1})^2}$	NRZ	General z_k	$\frac{(-s_k+1-1/z_k)sT_s-s_k^2}{(z_k-1)^2}\frac{1}{(sT_s-s_k)^2}$
		$z_k=1$	$\frac{1}{(sT_s)^2}-\frac{0.5}{sT_s}$
	RZ	General z_k	$\frac{\left[(0.5z_k^{-0.5}-1)s_k+1-z_k^{-0.5}\right]sT_s+(0.5z_k^{-0.5}-1)s_k^2}{(z_k-z_k^{0.5})^2}\frac{1}{(sT_s-s_k)^2}$
		$z_k=1$	$\frac{-1.5}{sT_s}+\frac{2}{(sT_s)^2}$
	HRZ	General z_k	$\frac{(-0.5z_k^{-0.5}s_k+z_k^{-0.5}-z_k^{-1})sT_s-0.5z_k^{-0.5}s_k^2}{(z_k^{0.5}-1)^2}\frac{1}{(sT_s-s_k)^2}$
		$z_k=1$	$\frac{-0.5}{sT_s}+\frac{2}{(sT_s)^2}$

3.3 Non-idealities of Continuous-Time Modulators

In this section, we will discuss non-idealities of CT modulators, including opamp in CT integrators, excess loop delay and clock jitter, are explained. These different non-idealities can cause different effects which are performance degradation or even making modulators unstable. Through understanding of these non-idealities and modeling their behaviors in system level simulations, we can analyze and overcome them in circuit level.

3.3.1 Opamp's non-idealities in CT Integrators

For an active-RC integrator shown in Fig. 3.4, the ideal transfer function is

$$\frac{V_{out}}{V_{in}} = -\frac{1}{sRC} \tag{3.7}$$

where R is the input resistor and C is the integration capacitor.

If OPAmp have finite DC gain A_0 and assume $A_0 >> 1$, the transfer function becomes

$$\frac{V_{out}}{V_{in}} \approx -\frac{1}{sRC + 1/A_0} \tag{3.8}$$

Considering the OPAmp finite DC gain, OPAmp unit gain bandwidth and only the dominant pole of the OPAmp, the transfer function becomes

$$\frac{V_{out}}{V_{in}} \approx -\frac{1}{s(1+\alpha \cdot f_s / GBW) + \alpha \cdot f_s / A_0} \tag{3.9}$$

where α is the scaling coefficient, f_s is sampling frequency while GBW and A_0

represent the gain bandwidth and the DC gain of the OPAmp, respectively.

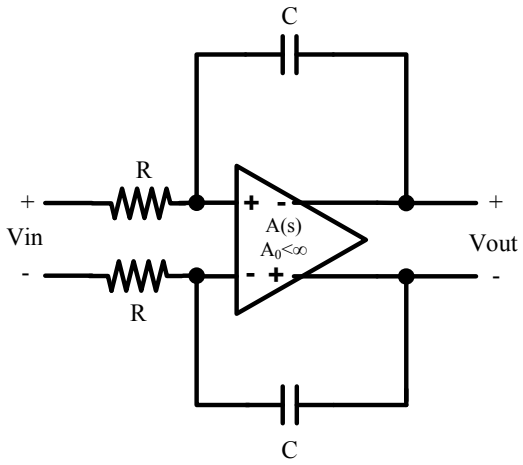


Fig. 3.4 A fully differential integrator with finite gain and bandwidth

Through the equation (3.9), we can analyze the requirement of the opamp in CT integrators in system level and design our OPAmp in circuit level.

3.3.2 Excess Loop Delay

When we synthesize the CT loop filter from a DT filter for a given feedback DAC waveform in the section 3.1.2, it is assumed that there is no delay time between the sampling instant of the loop filter output and the generation of new output digital codes. However, in the real circuits, due to the finite speed of transistors, this delay known as excess loop delay could not be zero. The excess loop delay usually consists of the delays introduced by the quantizer (including the dynamic element matching (DEM) logic if necessary), feedback DAC, and loop filter. Considering the feedback DAC, the impulse response of those three rectangular DAC pulses shown in Fig. 3.3 is changed to be that in Fig. 3.5.

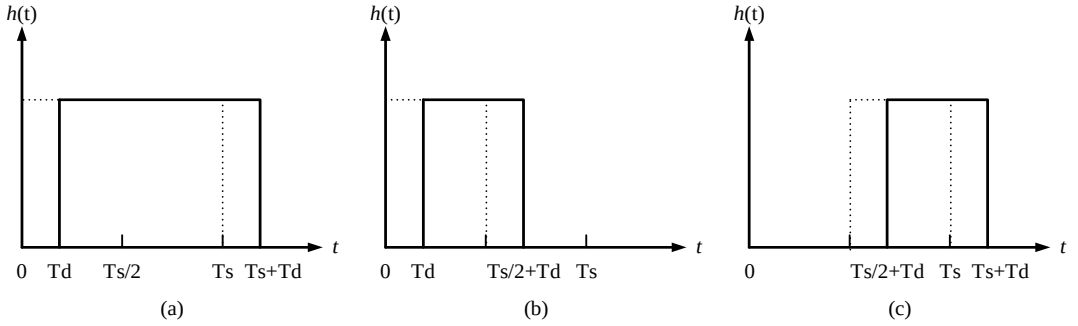


Fig. 3.5 DAC feedback impulse response including Excess Loop Delay (a) NRZ (b) RZ (c) HRZ

As analyzed in [13], if the falling edge of the DAC pulse exceeds the time instant, the order of the equivalent DT loop filter of the CT one is higher by one than under ideal conditions, which makes the CT modulator uncontrolled. The excess loop delay degrades the dynamic range of the modulator by reducing the effectiveness of the noise shaping as well as the maximum stable input signal swing. If the excess loop delay is too large compared with the clock period, the CT modulator will be unstable.

In order to compensate the excess loop delay, the RZ pulse can be used as the DAC waveform. As shown in Fig.3.5 (b), it can be seen that if the excess loop delay is smaller than half clock period, then the falling edge is still within the range, and hence the equivalent DT loop filter has the same order of the CT one. However, in most CT $\Delta\Sigma$ modulators, the NRZ DAC pulse is superior to the RZ (or HRZ) counterpart in terms of the clock jitter sensitivity issue. In addition, because the exact value of the excess loop delay is unknown while synthesizing the CT loop filter, the resulting CT modulator still cannot realize the same noise shaping as the DT target even using RZ DAC pulse.

While using NRZ DAC pulse, a common solution to the excess loop delay is to introduce a full clock delay in the feedback path to absorb the varying quantizer delay as well as the other delays, as shown in Fig. 3.6. However, due to this full clock delay, the impulse response of the CT loop at the sampling instant is zero. To compensate this response sample, an extra feedback branch is added directly to the quantizer input to make the total impulse response equivalent to the DT function [14]. Because the loop formed by the extra feedback branch doesn't include any integrator, we call it zero-order loop compensation.

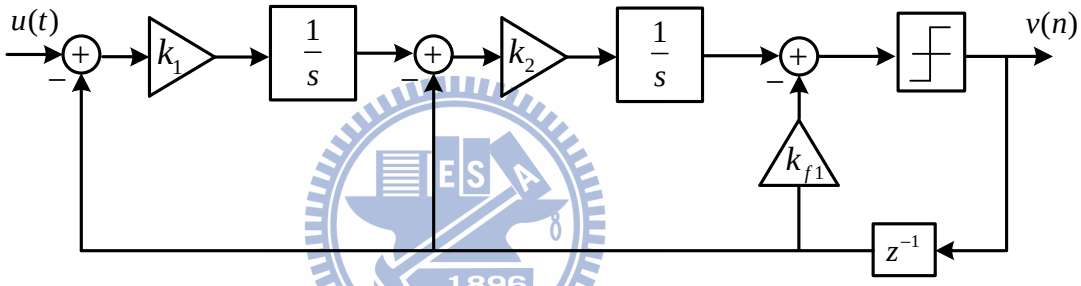


Fig. 3.6 Continuous-Time ΔΣ modulator with zero-order loop compensation

3.3.3 Clock Jitter

In the DT ΔΣ modulator, the continuous-time signal is sampled at the modulator input, so the sampling error caused by the clock jitter is directly added to the output without any attenuation. However, the sampling action in the CT ΔΣ modulator happens at the input of the quantizer, so the jitter-induced error is shaped by the loop filter before it appears at the output and hence may be negligible. But, the DAC output of the CT ΔΣ modulator is continuous, that is, the feedback signal affects the loop filter at all time instead of just at the sampling

instants. Therefore, the timing error of the feedback signal transition edges caused by the DAC clock jitter is equivalent to the feedback signal error itself. Because the DAC error also appears at the modulator output without any attenuation, the DAC clock jitter is one of the most important issues which should be considered while designing the CT ΔΣ modulator.

Fig. 3.7 shows the model of the jitter-induced noise for NRZ feedback DAC. In each sampling instant, the error area between ideal waveform and jittered waveform can be modeled as an equivalent error in the signal magnitude. In other words, the equivalent error can be expressed as follows

$$e(n) = \frac{\Delta A(n)}{T_s} = \left(v(n) - v(n-1)\right) \cdot \frac{\Delta t(n)}{T_s} \tag{3.15}$$

From (3.15), we can observe that if the difference between and is less, the clock jitter has lees effect upon the modulator performance. Therefore, the multi-bit quantizer has better jitter noise immunity.

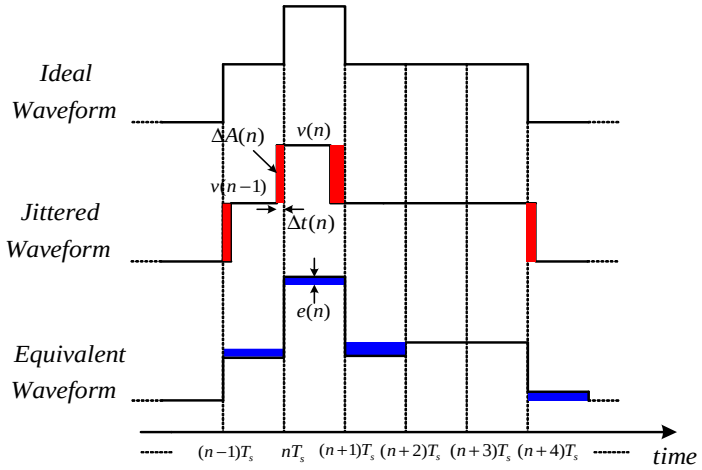


Fig. 3.7 Model of the jitter-induced noise for NRZ feedback DAC

DAC shape also affects the jitter sensitivity of CT modulators. This can be illustrated by Figure 3.7, where single-bit NRZ, RZ and HRZ feedback DAC shapes are described. In Fig. 3.8, the solid lines indicate the affected clock edges. In NRZ aspect, the NRZ DACs are only affected by clock jitter when the outputs change. On the contrary, the RZ and HRZ DACs suffer from the effect of the clock jitter in rising and falling edges of every clock cycle. They are more frequently affected than NRZ. So, the NRZ DAC is more resistant to the clock jitter. A good rule of thumb is that CT modulators employing RZ or HRZ DACs experience jitter noise about 6dB worse in the signal band than if NRZ DACs are used [12].

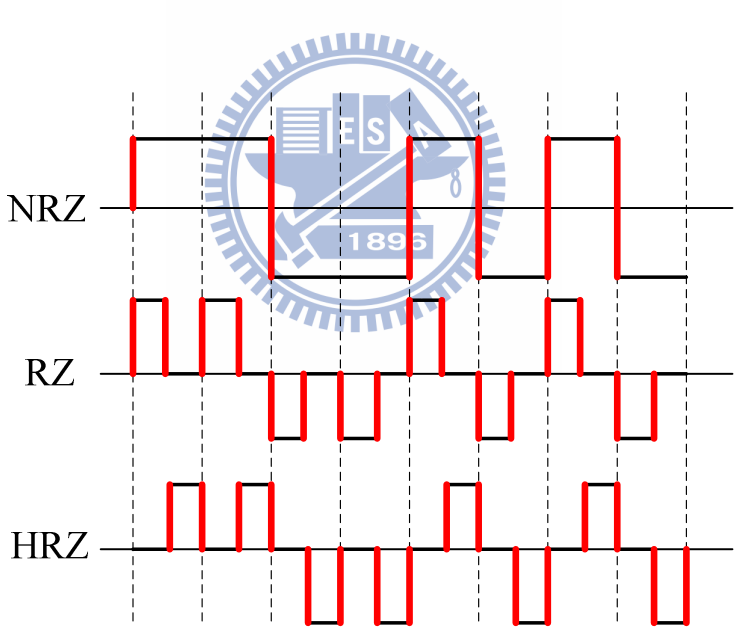


Fig. 3.8 Error sequence energy in different DAC shapes

CHAPTER 4
A Continuous-Time Single-Bit Active-RC Sigma-Delta Modulator with 1MHz bandwidth

In this chapter, we will implement a continuous-time single-bit active-RC sigma-delta modulator with 1MHz bandwidth. The system level and circuit level design of our first work is presented in detail, which includes the determination of the system level parameters, and the system level simulations with non-idealities. After that, the circuit blocks will be discussed, and the modulator is realized with a 0.18 μm CMOS technology and 1.8 V power supply voltage.

4.1 Introduction

The order of the loop filter is third and we use the architecture, cascade of resonators with distributed feedback (CRFB) [8], we can improve the bandwidth without increasing the order of the loop filter.

We use the active-RC type for all integrators. Due to the closed-loop operation, the active-RC integrator has better linearity than the gm-C integrator. However, because of the loading effect, the active-RC integrator requires an additional output buffer which consumes much power. This is a trade off between the two typical integrators.

Finally, the system and he system and circuit level implementations

are presented and the design considerations are explained. The chip is designed in TSMC 0.18 μm CMOS process and the chip size is 1.07mm x 1.12mm. This work achieves 53.8dB SNDR performance and consumes 10.2mW at 1.8V supply voltage.

4.2 Loop Filter Architecture

4.2.1 Architecture

We use cascade of resonators with distributed feedback (CRFB) for the loop filter of the CT third-order modulator, as shown in Fig. 4.1.

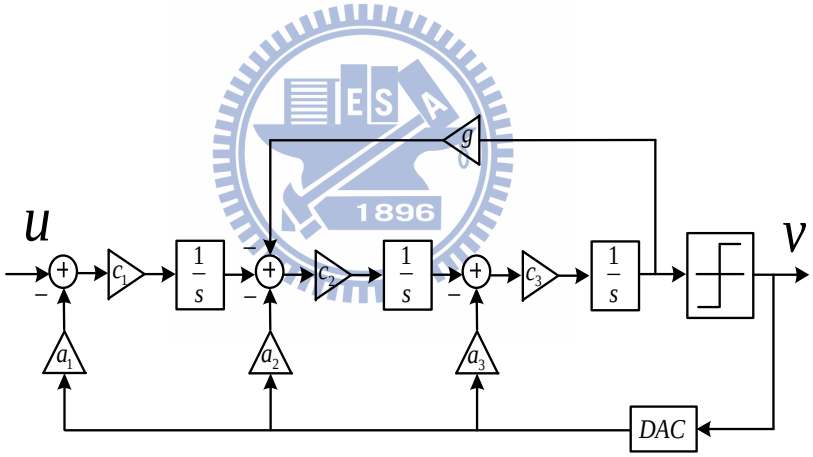


Fig. 4.1 The architecture of CT $\Delta\Sigma$ modulator using feedback resistors

The loop filter transfer function in Fig. 4.1 can be derived by

$$H(s)=\frac{u}{v}=\frac{a_3\cdot c_3\cdot s^2+(c_2\cdot c_3\cdot a_2)s+c_1\cdot c_2\cdot c_3\cdot a_1}{s^3+g\cdot c_2\cdot c_3} \tag{4.1}$$

The advantage of the architecture is capable of realizing NTF zeros as two conjugate complex pairs on the unit circle to obtain wider bandwidth.

For example, the pole-zero plot of the third-order architecture is illustrated in Fig. 4.2. In Fig. 4.2, we can observe that there are one zero at DC and two conjugate zeros on the unit circle as the described advantage. The power spectral density is shown in Fig. 4.2.

It is expected that even greater benefits can be obtained by optimizing the location of the zeros of higher-order NTF. The resulting values for the zeros are given in Table 4.1 for NTF with degrees from 1 to 8 [8].

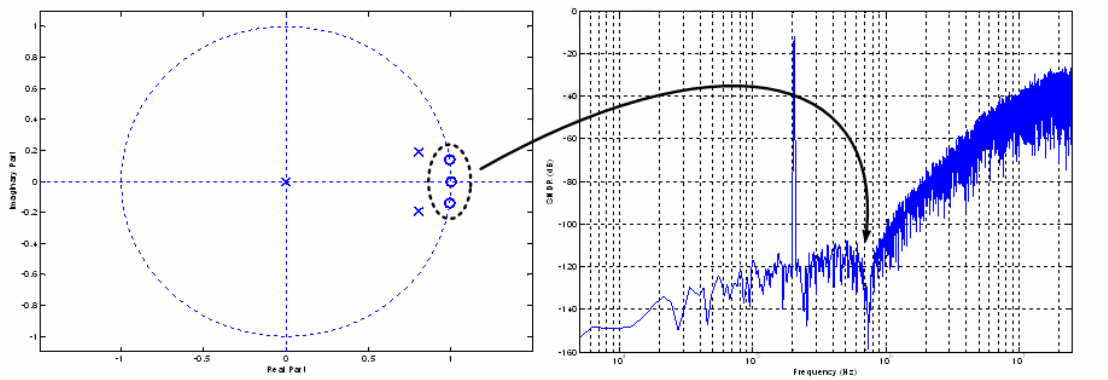


Fig. 4.2 Pole-zero plot and PSD of CRFB

Table 4.1 Zero placement for minimum in-band noise

N	Zero locations, normalized to bandwidth ω_B	SNR improvement
1	0	0 dB
2	$\pm 1/(\sqrt{3})$	3.5 dB
3	$0,\ \pm\sqrt{3/5}$	8 dB
4	$\pm\sqrt{3/7 \pm \sqrt{(3/7)^2 - 3/35}}$	13 dB
5	$0,\ \pm\sqrt{5/9 \pm \sqrt{(5/9)^2 - 5/21}}$	18 dB
6	$\pm 0.23862,\ \pm 0.66121,\ \pm 0.93247$	23 dB
7	$0,\ \pm 0.40585,\ \pm 0.74153,\ \pm 0.94911$	28 dB
8	$\pm 0.18343,\ \pm 0.52553,\ \pm 0.79667,\ \pm 0.96029$	34 dB

4.2.2 Coefficients

One of the most important designs in ΔΣ modulator is the system coefficients. Different system coefficients have different performance. Use sigma-delta toolbox [8], the DT loop can be obtained easily. For example, the *synthesizeNTF* function in sigma-delta toolbox is used to synthesize a noise transfer function (NTF) according to the order of the modulator, OSR and high frequency gain. And then we can obtain the signal transfer function (STF) and the loop filter function from the noise transfer function (NTF). The CT loop filter function can be derived by the impulse-invariant transformation, just like in section 3.2.

In our research, first, by using the *synthesizeNTF* function and designing the third-order lowpass modulator, where the OSR is 50 and high-frequency gain of the NTF is 1.7, the DT NTF can be derived by

$$NTF(z)=\frac{(z-1)(z^2-1.998z+1)}{(z-0.5932)(z^2-1.37z+0.5824)} \tag{4.2}$$

and the DT loop filter can be expressed as

$$H(z)=\frac{1.035(z^2-1.55z+0.6325)}{(z-1)(z^2-2z+1)} \tag{4.3}$$

Second, by applying impulse-invariant transformation in Matlab, the CT loop filter can be obtained by

$$H(s)=\frac{0.83s^2+0.38s+0.0864}{s^3+0.002s} \tag{4.4}$$

Finally, from (4.1), (4.5) and by assigning the initial values of the feedback coefficients $a_1 = 1$, $a_2 = 1$ and $a_3 = 1$, the CT coefficients can be acquired as

$$c_1 = 0.227, c_2 = 0.46, c_3 = 0.83, g = 0.0053 \quad (4.5)$$

This is not the only solution and many other more systemic methods proposed in [8] can also effectively resolve the coefficient issues.

4.3 System Level Analysis

As mentioned before, talking the non-idealities into account, we show how we determine the NTF. By the sigma-delta toolbox, the NTF can be easily derived according to the specifications. In this work, we design a third-order modulator, where the OSR is equal to 50 and the maximum out-of-band gain of the NTF is 1.7, as shown in Fig. 4.3. In Fig. 4.3 (a), we simulate the maximum out-of-band gain of the NTF versus the peak SNR in system level. Due to the stability issue, we can find that the maximum out-of-band gain of the NTF is limited. The plot of the input level versus the SNR is shown in Fig. 4.3 (b). Therefore, we choose that the maximum out-of-band gain of the NTF is equal to 1.7 and input level is equal to -7dBFS, so we get the peak SNR is 85dB.

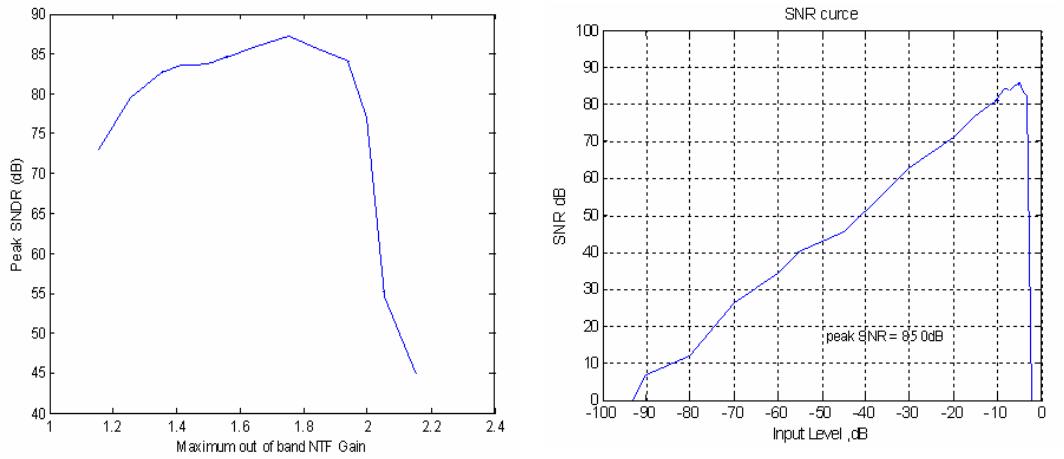


Fig. 4.3 (a) Maximum out-of-band gain of the NTF versus the peak SNR (b) Input level versus the SNR in system level

We show the output spectrum in this system level simulation of the modulator, which includes all the non-idealities except the thermal noise, as shown in Fig. 4.4. As a comparison, the ideal noise transfer function is also plotted in this figure.

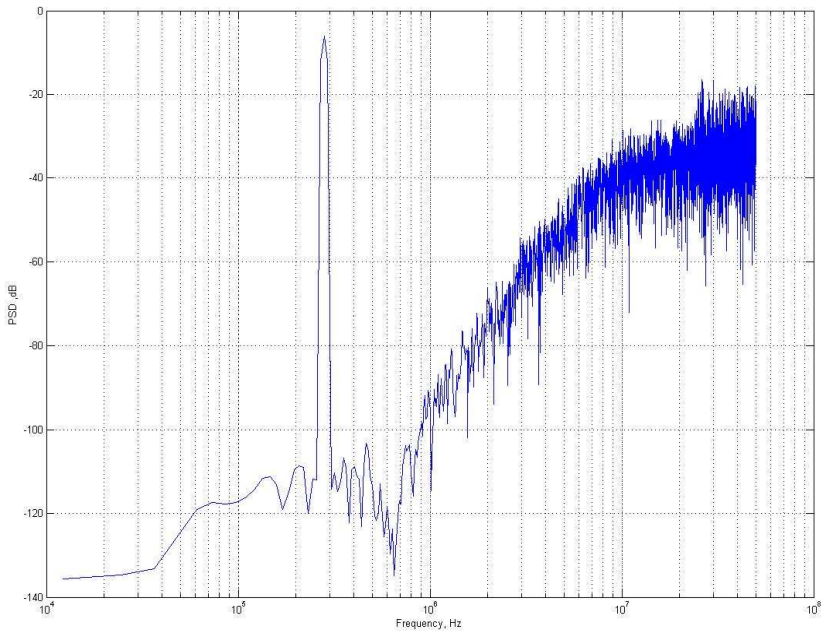


Fig. 4.4 The system simulation of CT ΔΣ modulator using feedback resistors

4.3.1 RC Variation

The variation of the RC time constant is one of the system imperfections in CT Σ Δ ADCs. In process variation, the actual value of resistors and capacitors can vary as large as ±20%. For CT ADCs, ±20% variation is enough to lead the system to unstable operation. Therefore, by analyzing the behavior model, the SNDR performance for -7BFS input under the variation of the time constant is shown in Fig. 4.5 we can find that a positive time constant variation can also make the system stable and achieve the 65dB SNDR performance. However, a negative time constant variation results in the unstable modulator instead. Consequently, additional tuning circuits vary the time constant of the CT Σ Δ ADCs and ensure the system in stable operation.

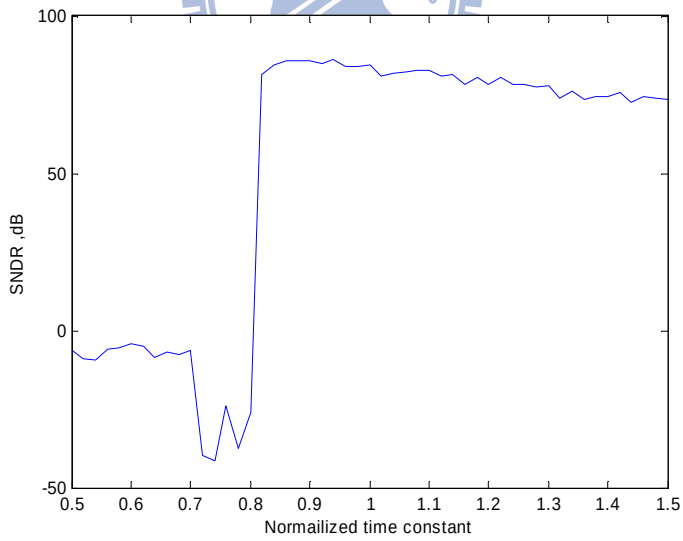


Fig. 4.5 Simulated SNDR for -7dBFS input under the variation of the time constant

4.3.2 Clock Jitter

Another the system imperfection in CT ΣΔ ADCs is clock jitter. The clock jitter arises from both the quantizer and the feedback DACs. Due to the noise shaping, the clock jitter noise at the quantizer only adds little noise to the modulator output. Nevertheless, the clock jitter in the feedback DACs generates unshaped noise. The noise can degrade the modulator performance sorely. Thereby, by the behavior model analysis, we can estimate the performance degradation generated by clock jitter noise. Fig. 6 shows the simulated SNDR for -7dBFS input under the effect of the clock jitter. If the 65dB SNDR performance wants to be achieved, the effect of the clock jitter should be smaller than 0.1% Ts. This can be accomplished by an additional preamplifier in the quantizer to improve speed.

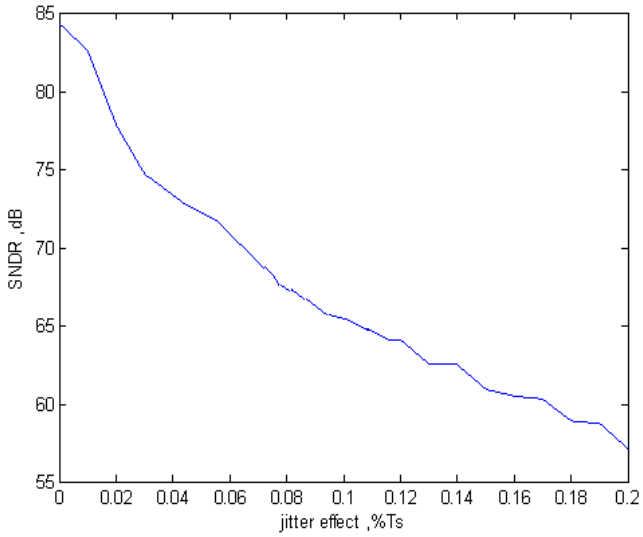


Fig. 4.6 Simulated SNDR for -7dBFS input under the effect of the clock jitter

4.3.3 Simulation Result

By the SIMULINK model, we can analyze different non-idealities to estimate the noise budget and achieve attainable performance.

The CT third-order sigma-delta modulator operates at 100MHz and the signal bandwidth is 1MHz. The oversampling ratio is equal to 50 and about non-idealities term, we assume the time constant variation and clock jitter, the whole behavior model simulation is shown in Fig. 4.7. For Fig. 4.7 the input sine wave is set to be -7dBFS at 140.38 kHz. The noise floor is around -100dB and the SNDR performance is about 66.6dB

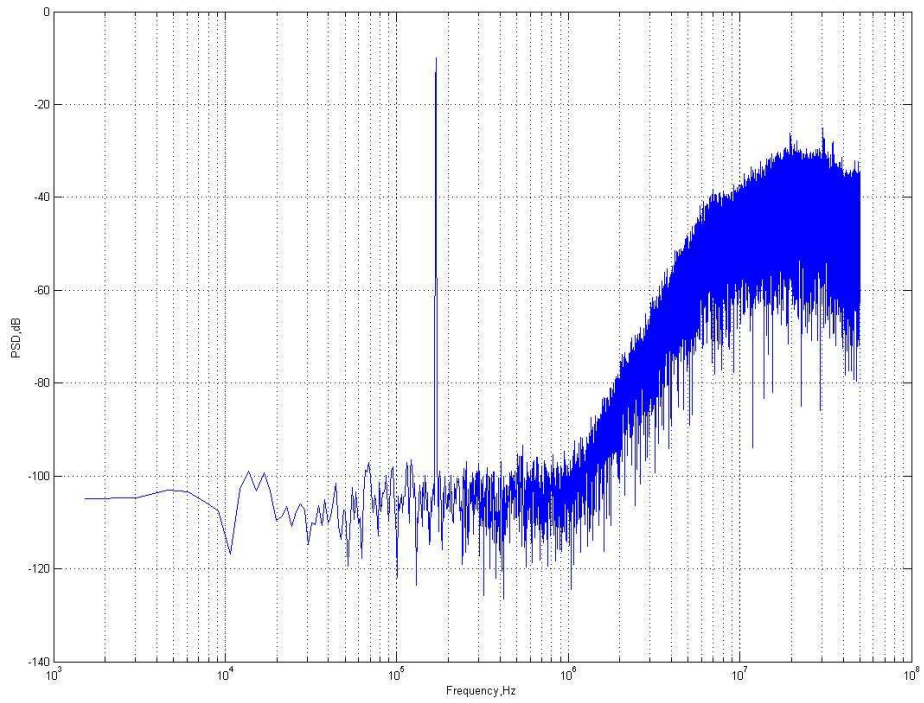


Fig. 4.7 Behavior model simulation result

4.4 Circuit Level Implementation

In this section, the circuit level implementation of the continuous-time single-bit active-RC sigma-delta modulator for Bluetooth is introduced in detail. The modulator is designed in a standard TSMC 0.18μm CMOS process with 1.8V supply voltage.

4.4.1 Loop Filter

Fig. 4.8 shows the simplified block diagram of the CT third-order modulator. The architecture of the three integrators uses the typical type, active-RC. Because of the closed-loop operation, the active-RC integrator has better linearity than the gm-C type. The single-bit quantizer is composed of the preamplifier, the regenerative latch and the SR latch which realizes the NRZ shape. The output of the quantizer is to control the switches of the current steering DACs which form the feedback loop.

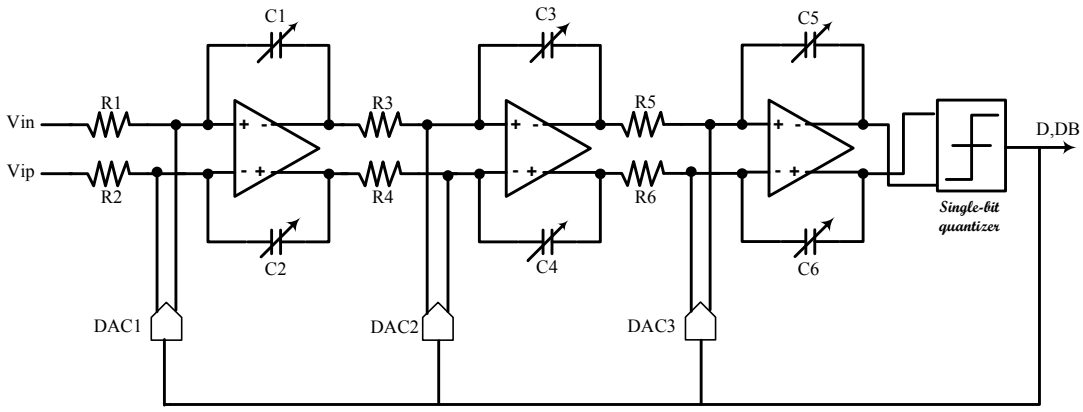


Fig. 4.8 Simplified block diagram of the CT third-order modulator

In the following subsection, other important analog parts are described and the design considerations are explained in detail.

4.4.2 Amplifier in active RC integrator

Due to the sampling frequency is 100MHz and the bandwidth is 1MHz, the opamp uses a folded-cascode opamps shown in Fig. 4.9 Compared with the two-stage opamps, folded-cascode opamps achieve the higher speed with the lower power consumption and compared with the telescopic opamps generates wider output swing. In order to ensure that the modulator is functional, we analyze the behavior model to know each opamps specification.

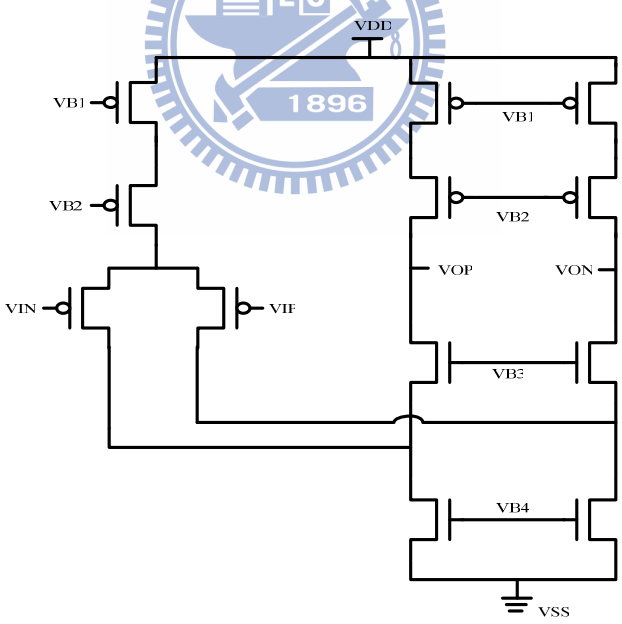


Fig. 4.9 Folded cascode opamp with p-type input

Fig. 4.10 shows the AC simulation results in TT, FF and SS corner and the performance of the telescopic opamp with gain boosting is summarized in Table 4.2

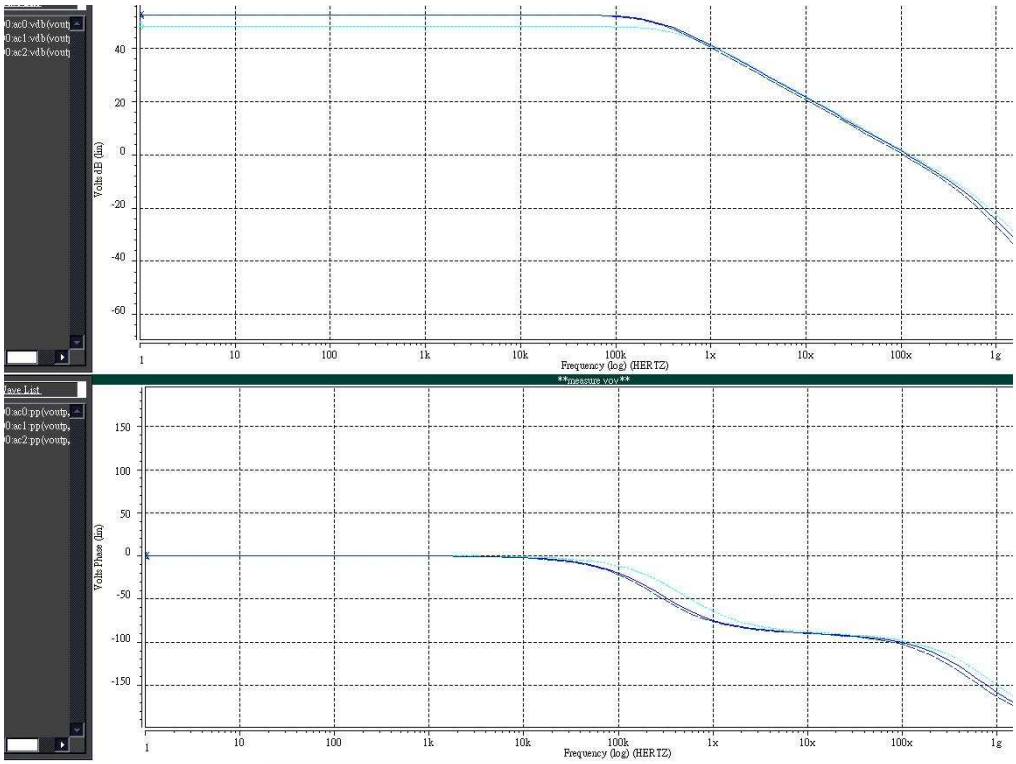


Fig. 4.10 Frequency response of the Amplifier

Table 4.2 Performance of the Amplifier

Simulation Results	Red Line TT @ 50° C	Blue Line FF @ 0° C	Green Line SS @ 100° C
Differential Gain	52.6 dB	48.3 dB	52.7 dB
Phase Margin	77.5°	79.9°	76.5°
Unity-Gain Frequency (5p)	118.3 MHz	124.5 MHz	105.9 MHz
Output Swing	1.1V		
Power Dissipation	2.57mW		

Fig. 4.11 shows the common-mode feedback (CMFB) circuit for the folded-cascode OpAmp. We first assume the two pairs have the same differential voltage, therefore, the current in Q1 will be equal to the current in Q3, while the current in Q2 will equal the current in Q4. This result is valid independent of the nonlinear relationship between a differential pair's input voltage and its large signal differential

drain currents. Now, letting the current in Q2 be denoted as $I_{D2} = I_B / 2 + \Delta I$, where I_B is the bias current of the differential pair and ΔI is the large signal current change in I_{D2} the current in Q3 is given by $I_{D3} = I_B / 2 - \Delta I$ and the current Q5 in is given by

$$I_{D5} = I_{D2} + I_{D3} = I_B / 2 + \Delta I + I_B / 2 - \Delta I = I_B \qquad (4.1)$$

Thus, as long as the voltage V_{outp} is equal to the negative value of V_{outn}, the current through diode-connected Q5 will not change even when large differential signal voltage are present. Since the voltage across diode-connected Q5 is used to control the bias voltages of the output stage of the OpAmp, this means that when no common mode voltage is present, the bias currents in the output stage will be the same regardless of whether a signal is present or not.

Next, we consider one thing, what happens when a common mode voltage other than zero is present. We first assume a positive common mode signal is present. This positive voltage will cause the currents in both Q2 and Q3 to increase, which causes the current in diode-connected o increase, which in turn causes its voltage to increase. This voltage is the bias voltage that sets the current levels in the n-channel current sources at the output of the OpAmp. Thus, both current sources will have larger currents pulling down to the negative rail, which will cause the common mode voltage to decrease, bring the common mode voltage back to zero. By this way, as long as the common mode loop gain is large enough, and the

differential signals are not as large as to cause transistors into turn-off, the common mode output voltage will be kept very close to ground [10].

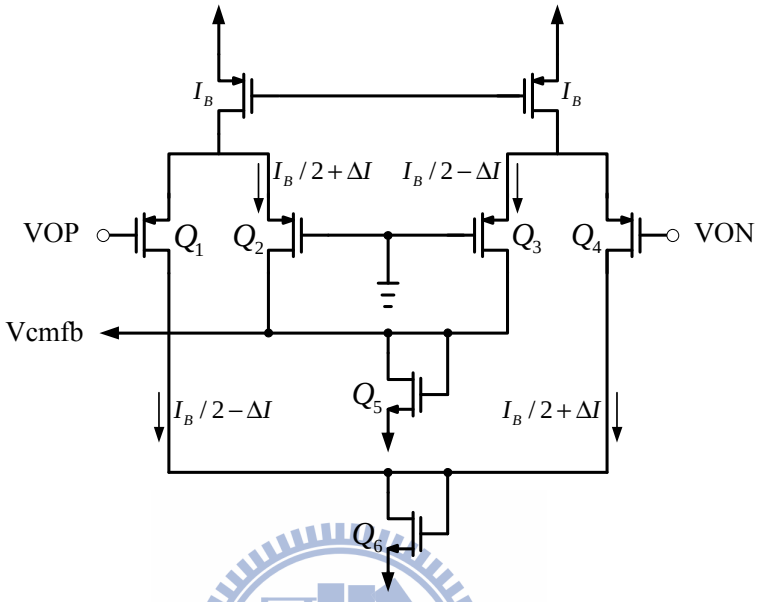


Fig. 4.11 Schematic of CMFB circuit

4.4.3 Comparator

Fig. 4.12 shows the circuit of the comparator including a preamplifier and a low-offset regenerative latch [15]. In Fig. 4.12 (a), using a cross-coupled load to increase Ro, the differential gain can be improved and it can be expressed as

$$A_{dm} = g_{m1,2} \cdot \frac{1}{g_{m3,4} - g_{m5,6}} \tag{4.7}$$

In Fig. 4.12 (b), when V_{CK} goes to high, the M1 and M2 work in saturation region and due to the mismatched current in the M1 and M2, the outputs

are resulted from the cross-coupled inverters which form the positive feedback loop. In this phase, since the M1 and M2 are in saturation region so that the comparator has low offset voltage. When V_{CK} goes to low, the outputs are reset to VDD and the SR latch maintains previous outputs to form the NRZ shape. The truth table of the SR latch is shown in Table 4.3. Another advantage of the regenerative latch is that when V_{CK} goes to low, there is no power dissipation.

In order to reduce the influence of the excess loop delay, we add an additional preamplifier to improve the speed. Fig.4.13 shows the simulation result of the comparator. The sine wave is the input and the square is the output of the SR latch.

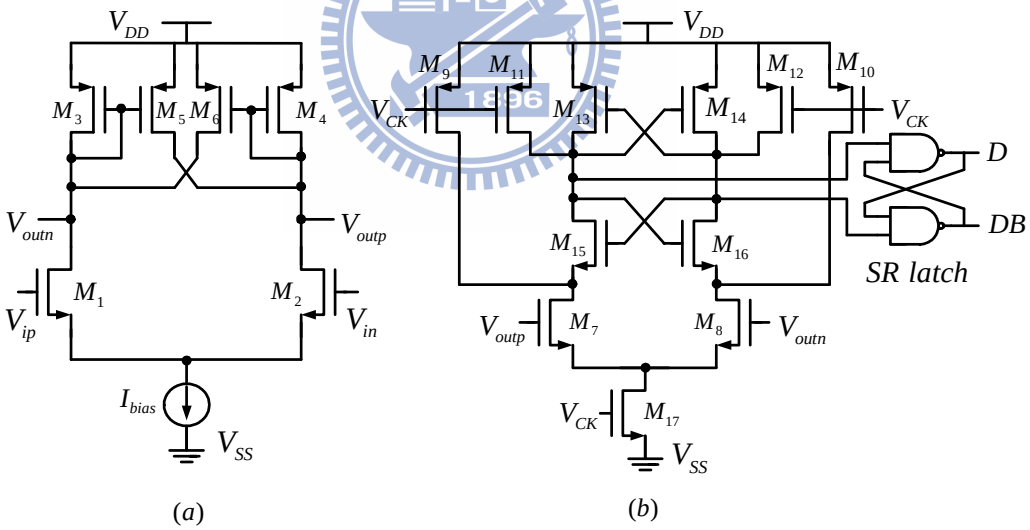


Fig. 4.12 (a) A cross-coupled preamplifier and (b) Low-offset regenerative latch

Table 4.3 Truth table of SR latch

S	R	D	DB
0	0	1	1
0	1	0	1
1	0	1	0
1	1	D	DB

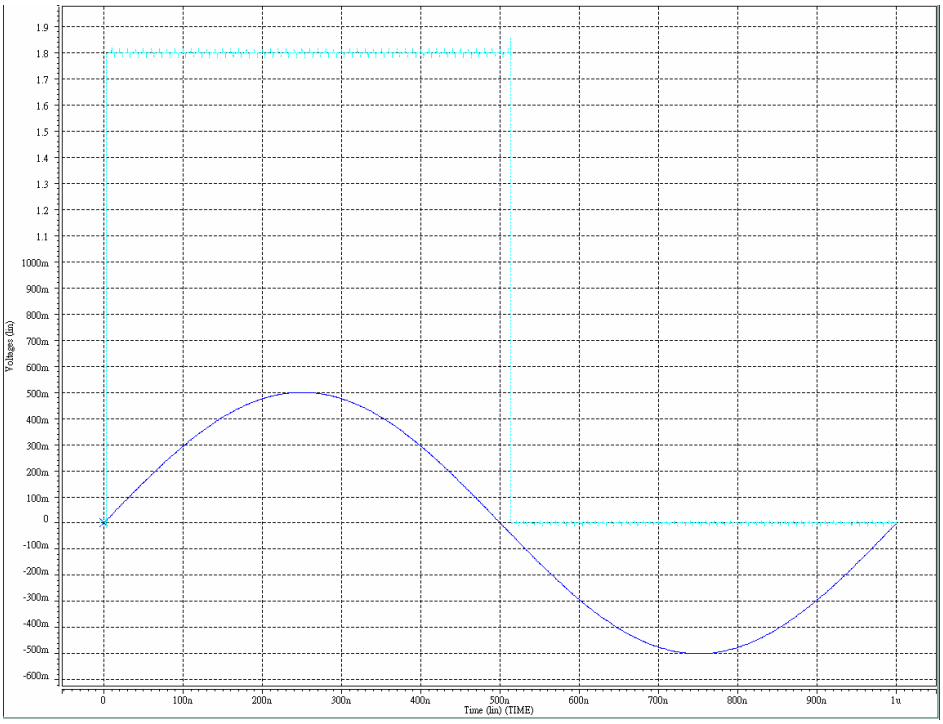


Fig. 4.13 Simulation result of the comparator

4.4.4 Current Steering DAC

Fig. 4.14 shows the active-RC integrator with the current steering DAC. The DAC signal (-1, +1) is controlled by the feedback digital codes (D, DB). The difference of the input signal and the DAC signal is stored into Ci and then transferred into the next stage integrator. The operation of the current steering DAC is described as follows:

When the feedback digital code D is high the $0.5I_{DAC}$ current source

passes through the switch so that $0.5I_{DAC}$ is pulled from the V_{ip} to I_{DAC} current source. Since the another switch turns off $0.5I_{DAC}$ current source above the switch injects current into the Vin to from the feedback loop

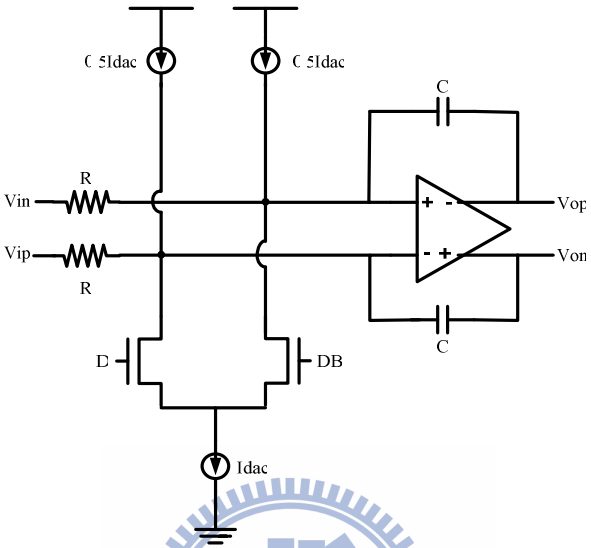


Fig. 4.14 Active-RC integrator with current steering DAC

4.4.5 Low Jitter Clock Generator

All the system blocks are synchronized by a clock to implement the function. As previous sessions discuss, CT $\Delta\Sigma$ modulators are sensitive to clock jitter. Therefore, this clock needs to have sufficiently low jitter in order not to increase the modulator output noise floor due to non-shaped jitter noise. In our design, system level simulations show that less than 0.1%Ts clock jitter is required. Some design strategies are adopted to minimize clock jitter due to device and supply noise. Fig. 4.15 shows the simplified circuit to generate the low jitter clock.

To reduce common mode noise probably coupled to the testing board and to obtain the least amount of clock jitter from the external clock source, sinusoidal differential clock inputs are generated on board and

fed to the modulator. It is critical to use as few clock driver stages as possible to generate the low jitter clock with sufficient driving capability because any extra stages generate extra device noise, hence larger clock jitter. To reduce the supply noise, a dedicated and clean supply is used solely for the low jitter clock generation circuit [16].

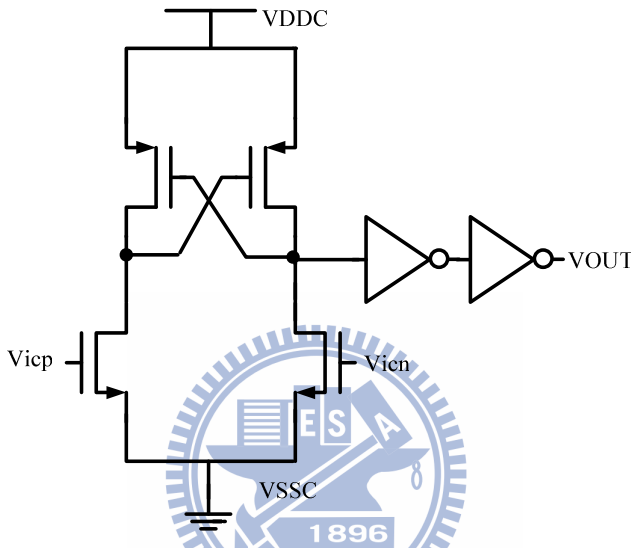


Fig. 4.15 Low-jitter clock generator

4.4.6 Tuning Circuit

We want to maintain SNDR performance. To ensure that the modulator is in stable operation, the tuning circuit shown in Fig. 4.16 must be used. In Fig. 10, there are an always-in-use capacitor which is 16C and five in-use capacitors which are 1C, 2C, 4C, 8C and 16C. The normal value of the capacitances is 32C. Through the use of the digital control signals, the minimum and maximum available capacitances are 16C and 47C, respectively. Thereby, the minimum tuning range is from -50% (16C/32C) to +46.875% (47C/32C) and the tuning resolution is 3.125% (C/32C), where C is the tuning step.

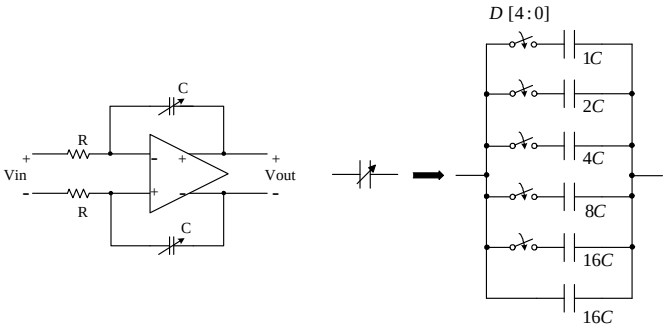
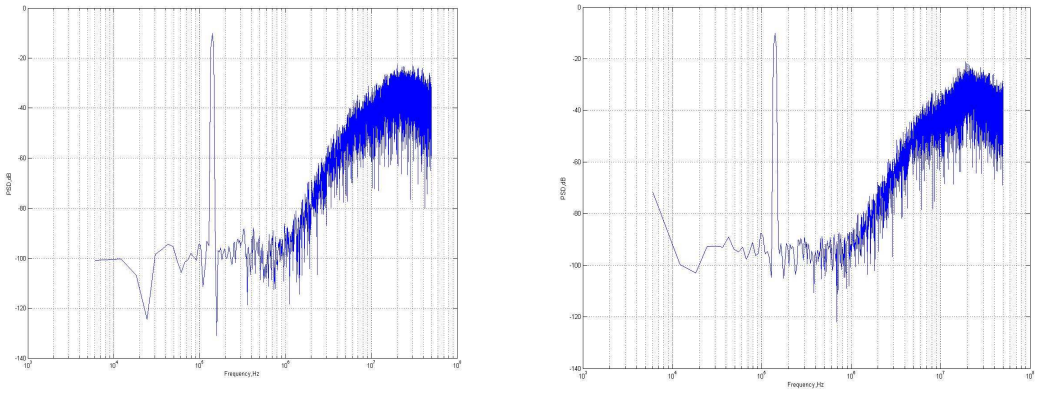


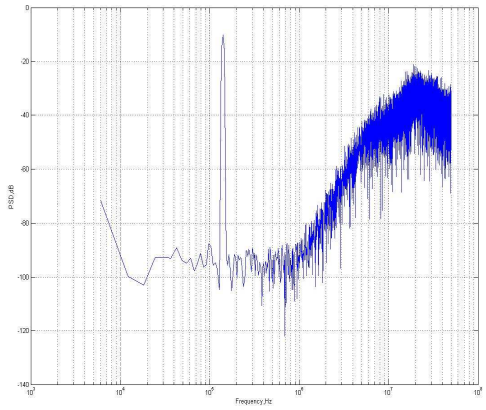
Fig. 4.16 Tuning circuit

4.5 Circuit Level Simulation Result

The simulated power spectral density of the continuous-time third-order single-bit active-RC sigma-delta modulator for Bluetooth is shown in Fig. 4.17. In Fig. 4.17, the sampling frequency is 100MHz and the signal bandwidth is 1MHz. The OSR is equal to 50 and the SNDR of the TT corner is about 61.5dB for -7 dBFS 140.43kHz input. The power consumption is 9.95mW at 1.8V supply voltage. The performance of this work is summarized in Table 4.5. The chip photo is shown in Fig.4.18. The total area, including pad is 1.074mm x 1.112mm.



(a) (b)



(c)

Fig. 4.17 Simulated power spectral density of this work (a) TT (b) FF (c) SS corner

Table 4.4 Performance summary of this work

	TT @ 50° C	FF @ 0° C	SS @ 100° C
Sampling Frequency	100MHz		
Signal Bandwidth	1MHz		
SNDR (Fin140.43kHz)	61.5dB	62.8dB	60.1dB
Power Consumption @1.8V	9.95mW		
Area	1.074mm x 1.112mm		
Technology	TSMC 0.18㎛ CMOS		

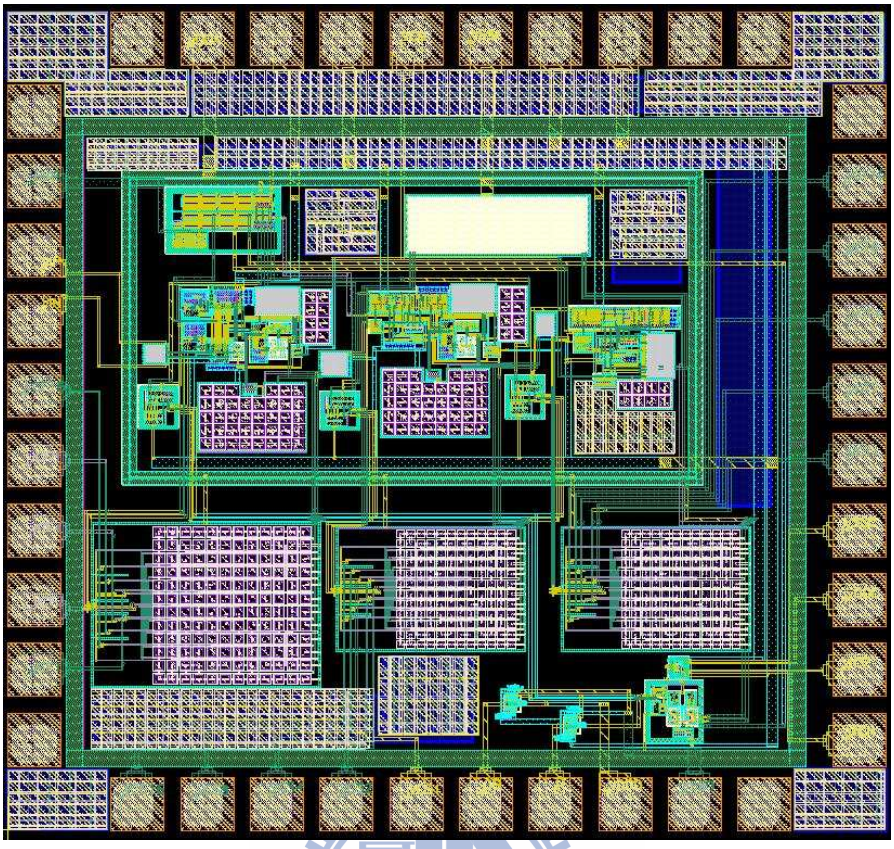


Fig. 4.18 Chip photo of this work using feedback resistors

4.6 Summary

A continuous-time third-order single-bit sigma-delta modulator for Bluetooth application is designed in TSMC 0.18μm digital CMOS process. The architecture of the modulator utilizes CRFB structure to improve the signal bandwidth. The integrators are implemented by active-RC type to have better linearity. Additionally, in order to reduce the effect of the clock jitter, the feedback DAC shape is realized by NRZ. The CT third-order single-bit modulator achieves 61.5dB SNDR and the power consumption is 9.95mW.

CHAPTER 5
BACKGROUND OF LIQUID CRYSTAL DISPLAY

In this chapter, first, the structure of liquid crystal display is explained. Then we describe the driving method of liquid crystal display. Finally, we introduce the periphery circuit block slightly.

5.1 Liquid Crystal Display Structure

5.1.1. Liquid Crystal

Liquid crystal is a phase of matter whose order is intermediate between that of a liquid and that of a crystal. The phase variation of liquid crystal in different temperature is shown in Fig. 5.1. And the molecules are typically rod-shaped organic moieties about 25 Angstroms in length and their ordering is a function of temperature [17][18][19].

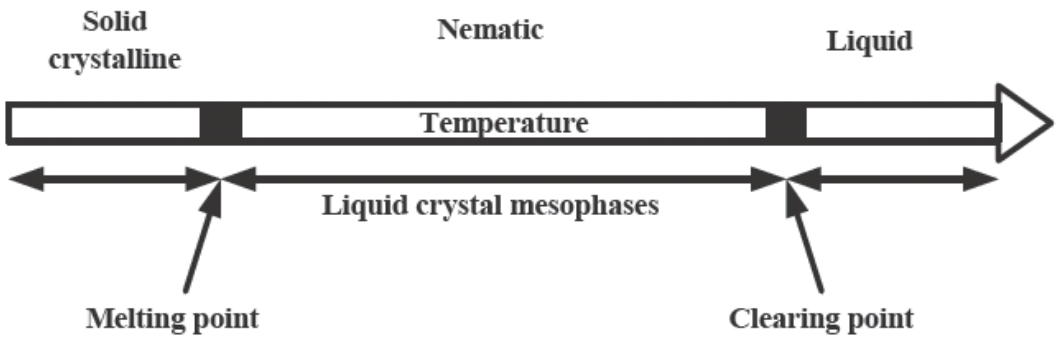


Fig. 5.1 Phase variation of liquid crystal in different temperature

In addition, the molecular orientation can be controlled with applying various electric fields. According to the way that liquid crystals are formed, it can be distinguished into thermotropic and lyotropic liquid crystals. For lyotropic liquid crystals, the phases formed depend upon the nature of the molecules involved, the temperature, and the type of solvent. In themotropic liquid crystals, the phase formed is characteristic of the temperature. But, if base on the arrangement of liquid crystal molecules, liquid crystals can be divided into three types — smetcic, nematic and cholesteric. Because the twist of liquid crystals can be controlled by the electric field that is applied across it, liquid crystals are used as a switch that passes or blocks the light. TN (twisted nematic) and STN (super twisted nematic) are the terms used to describe two types of liquid crystal displays. TN displays have a twist of 90 degrees or less. And almost all active matrixes have a 90 degree twist. As the name implies, STN displays have a twist that is greater than 90 but less than 360 degrees. Currently most STN displays are made with a twist between 180 and 240 degrees. The higher twist angle causes steeper threshold curve which puts the on and off voltages closer together. As a result, it is usually applied in passive matrixes. And the transparency of TN and STN in different voltage is illustrated in Fig. 5.2.

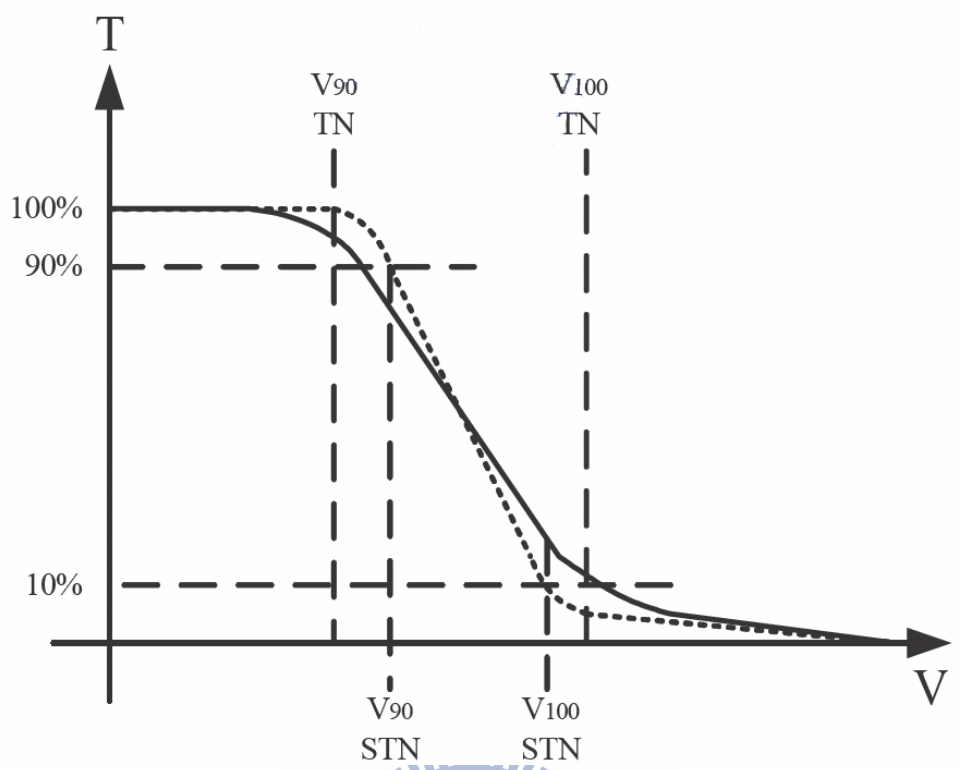


Fig. 5.2 Transparency of TN and STN in different voltage

5.1.2. Liquid Crystal

The cross section of LCD with polarizer, glass, LC (liquid crystal) material, and color filter is shown in Fig. 5.3. Polarizer can be divided into top polarizer and bottom polarizer. The top polarizer can polarize the incident light from random polarization into unique one. Before electric field is applied on the electrodes, the liquid crystals are aligned in a twist pattern. The path of light is then changed with the twist pattern of the liquid crystals. The bottom polarizer is aligned opposite of the top polarizer.

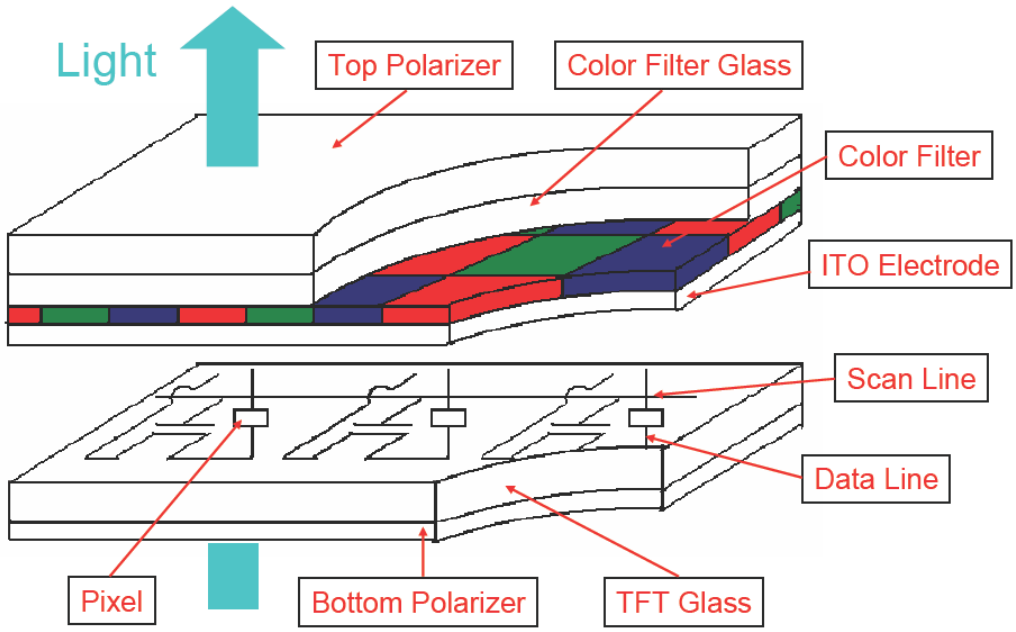


Fig. 5.3 Cross section of LCD model

Consequently, when the light reaches the bottom polarizer, they will align with each other and the light can pass through, which is illustrated in Fig. 5.4(a). On the contrary, if the electric is applied on the electrode, the liquid crystals will turn to the same direction. Then, the light can not pass the bottom polarizer, which is shown in Fig 5.4(b). In this case, it is usually called normally white.

The multiple step-and-repeat images of the LCD electrode on glass substrate are created by precise photolithography technique. TFT glass has so many TFT as the number of pixels while color filter glass has color filter that generates color. Three primary colors, red, green, and blue, can generate more than million kinds of color in different degrees of light.

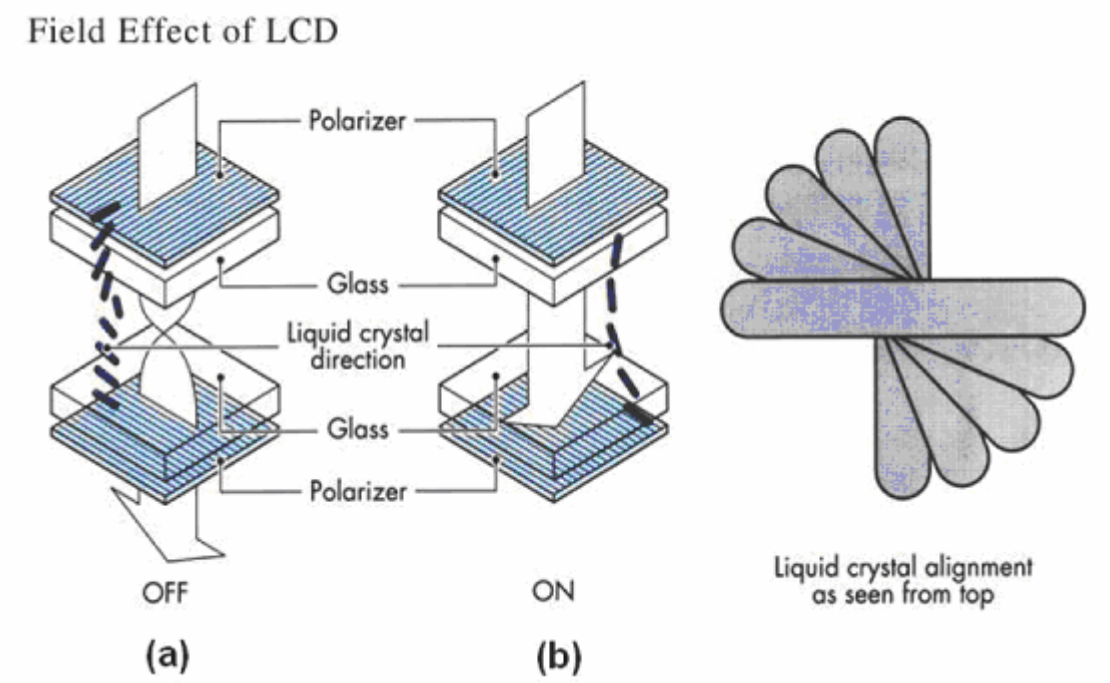


Fig. 5.4 The liquid crystal operates in normally white case: (a) light can pass and (b) light is blocked

5.2 Driving Method in LCD

5.2.1 Gamma Correction

Gamma correction of liquid crystal displays involves the pixel nonlinear voltage and the light modulation characteristics, so that equal changes in digital input must correspond to equal changes in light transmission. Base on this description, the relationship between digital input codes and input voltage across liquid crystals can be shown in Fig. 5.5(a). In this way, the smooth curve between digital input code and light transmission rate can be achieved in Fig 5.5(b). Moreover, there are something should be emphasized. In Fig 5.5(a), the curve is symmetrical to the input voltage axis. This is because that the permanent deflections

of liquid crystal molecules will occur if the DC (direct current) stress given on the LCD panel sustains a long period. As a result, the LCD panel should be driven by AC (alternating current) mode to eliminate the defect on LCD panel. Furthermore, LCD panel driven by AC mode can be classified into many kinds, and those will be discussed in the following sections.

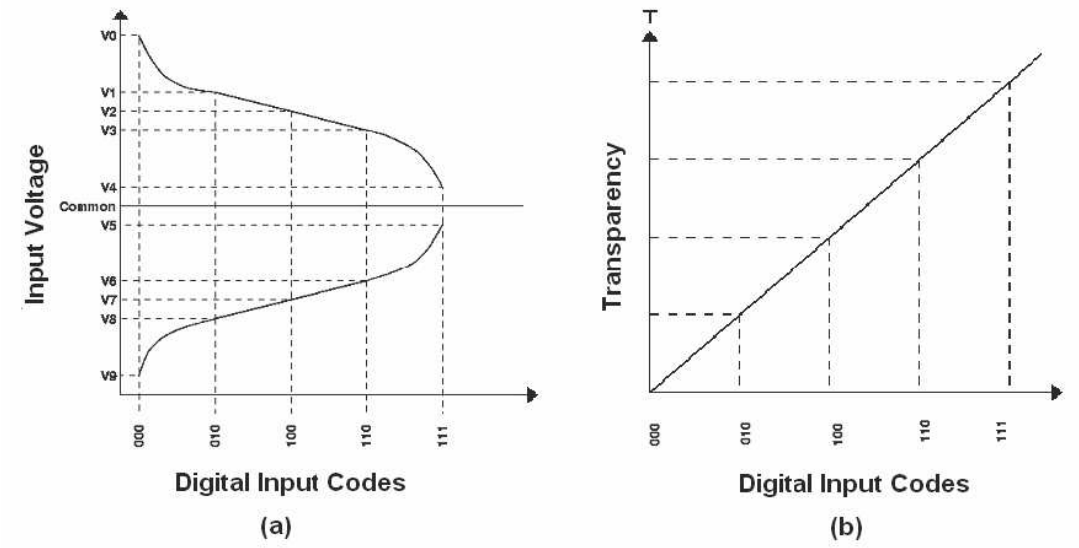


Fig. 5.5 (a) The relationship between digital input codes and input voltage across liquid crystals and (b) the smooth curve between digital input codes and light transmission rate

5.2.2 Driving Method

Liquid crystal molecules will be defected under a fixed voltage in a long period. Although the fixed voltage has vanished, the characteristic of the liquid crystals will be destroyed and the twist of liquid crystals can not change with electric field. Therefore, the electric field should be recovered every period to avoid the destruction of liquid crystals. When the frame picture is kept on the same gray level, the electric field

across liquid crystals is divided into two electrodes — positive electrode and negative electrode. As electric field is higher than common mode voltage the electrode is called positive electrode, otherwise it is called negative electrode. By this way, the liquid crystal molecules will avoid defection in the fixed electric field. In term of above description, LCD panel can be principally composed of four types — frame inversion, row inversion, column inversion, and dot inversion. They are listed in Fig. 5.6.

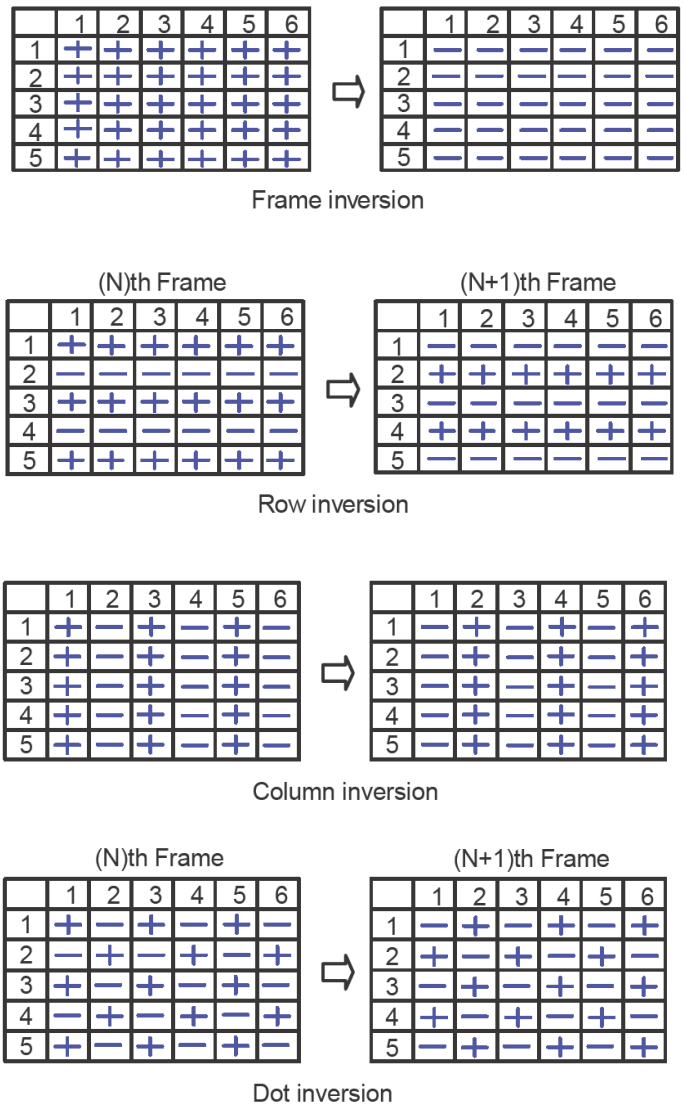


Fig. 5.6 Inversion of LCD panel

Frame inversion is that all the adjacent pixels of the LCD panel have the same electrode. Row inversion and column inversion is that each adjacent column pixel and adjacent row pixel have the same electrode respectively. Finally, all the adjacent pixels of LCD panel have different electrode is called dot inversion. Dot inversion is the major driving method of LCD panel. By the opposite polarity of the voltage vertically and horizontally side by side to each pixel, dot inversion can reduce clustered DC voltage in the screen which may result image sticking and to reduce the screen flickering. No matter what methods the LCD panel will be driven, all the pixels will change polarity on the frequency of 60 Hz (16ms). In other word, the polarity of each pixel is alternating changed.

Based on the operational type of common mode voltage, the driving method can also be classified into direct driving and AC modulation driving. They are shown in Fig. 5.7 and Fig. 5.8 respectively. Direct driving method would keep its common voltage on a constant level. But, the common mode voltage of AC modulation driving method would change its polarity in turns. The characteristics of two driving methods are listed below:

Direct driving method:

- Frame, row, column, and dot inversion are all available.
- Crosstalk and flicker can be eliminated.

AC modulation driving method:

- Frame and row inversion are available.
- Low power dissipation in data driver.

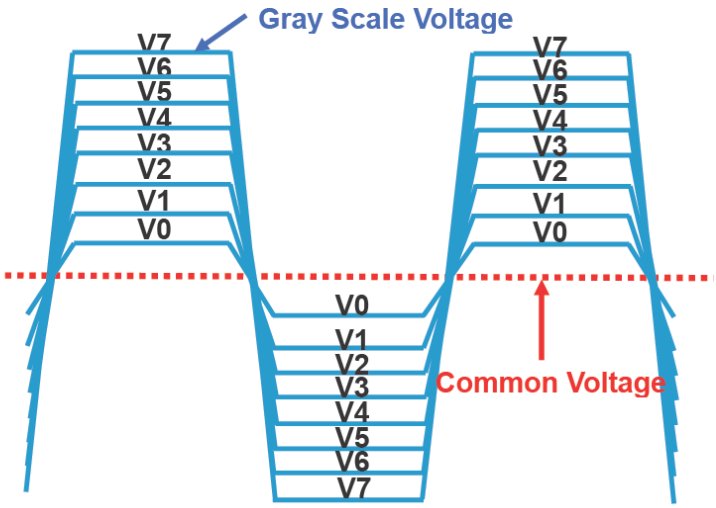


Fig. 5.7 The operational waveform of direct driving method

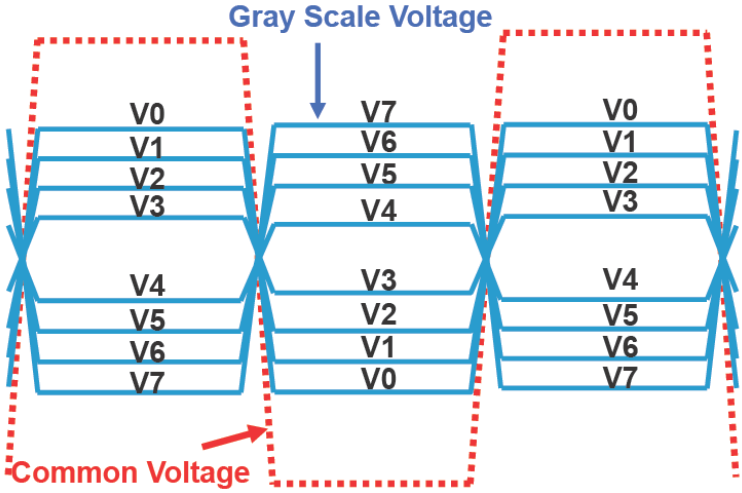


Fig. 5.8 The operational waveform of AC modulation driving method

5.2 Periphery Circuit Block

The periphery circuit blocks of LCD panel are composed of four parts — display panel, timing controller, scan driver and data driver. In Fig. 5.9 is the block diagram of the LCD panel driver circuits. Display panel is constructed of active matrixes and its structure layout is illustrated in the Fig. 5.10. The active matrixes are similar to DRAM

(dynamic random access memory) which is used to charge and discharge the capacitor on the pixels. Timing controller is responsible for transiting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver. As soon as one voltage level of the scan lines rises, the RGB signals will be transited through the data driver. After a period, the voltage level of this scan line will be disabled and next scan line will act. All voltage levels of those scan lines will change in turn. As for scan driver and data driver, they will be further discussed in the following sections.

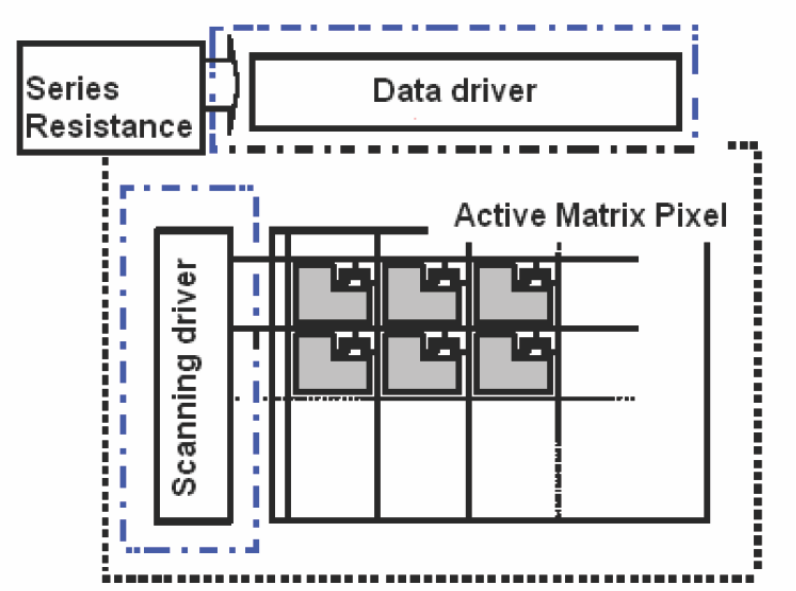


Fig. 5.9 Block diagram of the LCD panel driver circuits

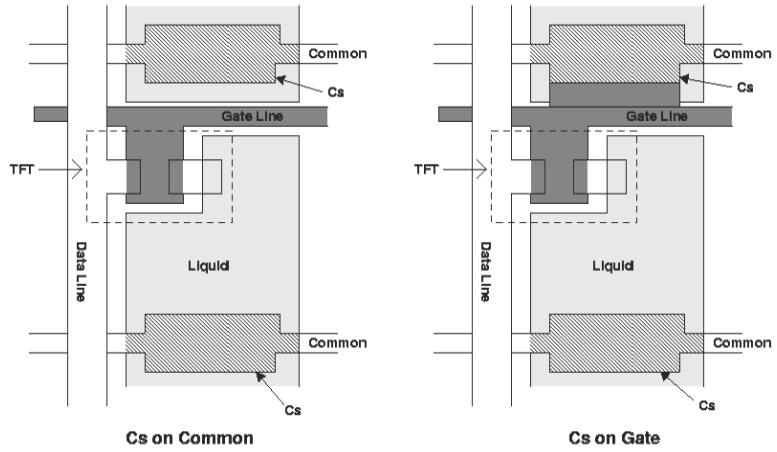


Fig. 5.10 The pixel layout structure of active matrix cell on LCD panel

5.2.1 Scan Driver Circuit

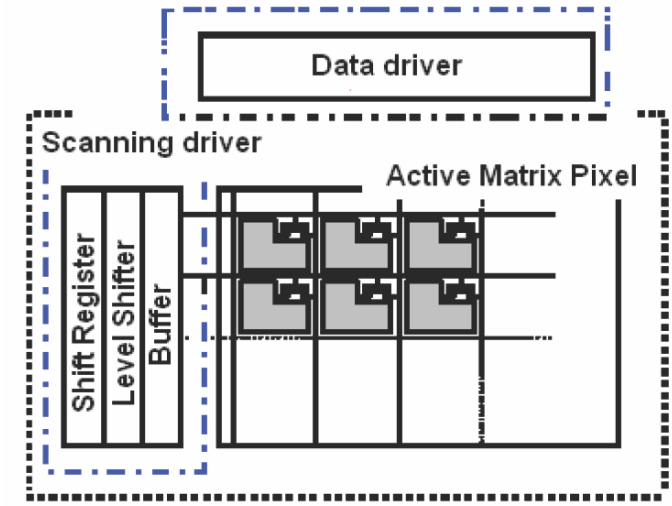


Fig. 5.11 The block diagram of scanning driver

Scan driver, shown in Fig. 5.11, consists of shifter register, level shifter, and output buffer. Shifter register is used to store digital input signals and transit them to the next stage according to timing clock. Because the turn-on voltage of active pixels is high, scan driver should drive the active pixels with a high voltage. The purpose of the level shifter is to convert the digital signals to a higher level voltage.

Finally, since the scan lines can be modeled as RC (resister and capacitor) ladder shown in Fig 5.12, the output buffer should be used in the last stage. The output buffer is composed of inverter chain. The number of stages employed in the inverter chain depends on the RC ladder.

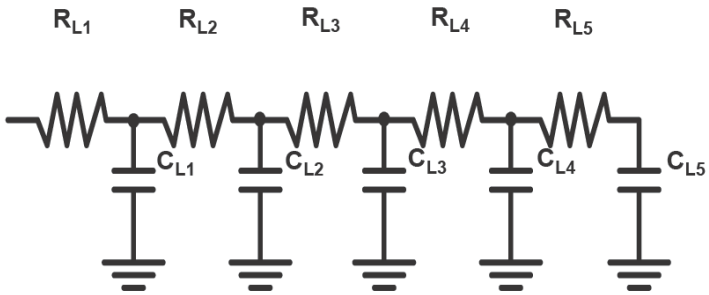


Fig. 5.12 RC (resister and capacitor) ladder of scanning line

5.2.2 Data Driver Circuit

Data driver, shown in Fig. 5.13, mainly contains shifter register, data latch, level shifter, digital to analog converter and output buffer. Furthermore, the first three parts classify as digital architectures. The other two parts belong to analog architectures. Shifter register and data latch manage to transit and store the RGB signals. Also, the purpose of level shifter is the same as the one in scan driver. It is applied to translate the RGB signal to a higher level voltage. As implied by the name, digital to analog converter is used convert the digital RGB signal to analog gray level. Its structures can be divided into many types often is R-string type, and we will describe a new architecture in after chapter.

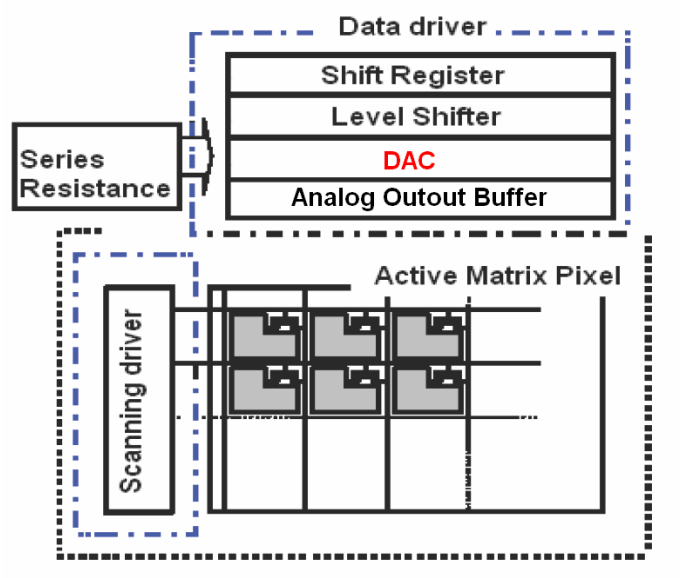


Fig. 5.13 The block diagram of data driver

CHAPTER 6
Basic Understanding of Digital-to-Analog Converter

Digital-to-analog converter converters (DACs) are essential in data processing systems. DACs interface the digital output of signal processors with the analog world and reconstruct the continuous-time analog signal. The digital-to-analog (D/A) converts a discrete amplitude, discrete time signal to a continuous amplitude, continuous time output.

A DAC is shown in Fig. 6.1. It converts a digital signal into an analog representation [20]. If the DAC generate large glitches during switching from one code to another, then a deglitching circuit is used to make the glitches. Finally a low-pass filter is required to suppress the sharp edges introduced by the DAC [21].

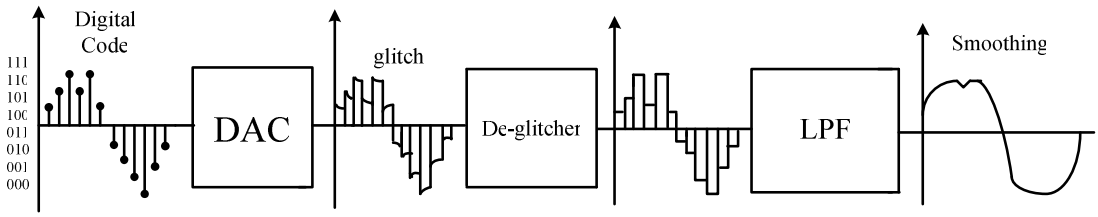


Fig. 6.1 Digital-to-analog conversion

In this chapter, first, the performance parameters of Digital-to-analog converter converters are explained. Then we introduce some DACs for LCD column driver.

6.1 Ideal D/A Converter

A digital-to-analog converter produces an analog output V_{out} that is proportional to digital input B_{in}. For a N-bit DAC shown in Fig. 6.2, the output V_{out} can be expressed as:

$$V_{out} = V_{ref}(D_0 2^0 + D_1 2^1 + ... + D_{n-2} 2^{n-2} + D_{n-1} 2^{n-1}) \quad (6.1)$$

where D_i equals 1 or 0. We also define b_0 as the least significant bit (LSB) and D_{n-1} as the most significant bit (MSB). In a DAC, a further classification is by the scaling methods. Three methods are called current, voltage and charge scaling.

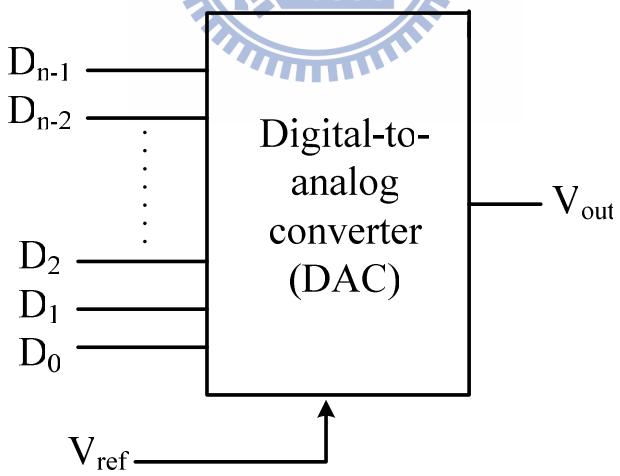


Fig. 6.2 Block diagram if a n-bit DAC

6.2 Performance Metrics

The characterization of DACs is very important in understanding its design. The characteristics of the digital-analog converter can be divided into static, dynamic and dynamic range properties [22].

6.2.1 Static Performance

Five basic static parameters are major content of this section of this section, which are offset error, gain error, INL, DNL and monotonicity. To distinguish all values of calculations in the DAC, $X_a(k)$ corresponds to the actual analog output for kth input code and $X_i(k)$ corresponds for the ideal tone.

6.2.1.1 Offset Error

The analog output should be 0V for digital input is equal to 0. However, an offset exists if the analog output voltage is not equal to 0. This can be seen as a shift in the transfer curve as illustrated in Fig. 6.3.

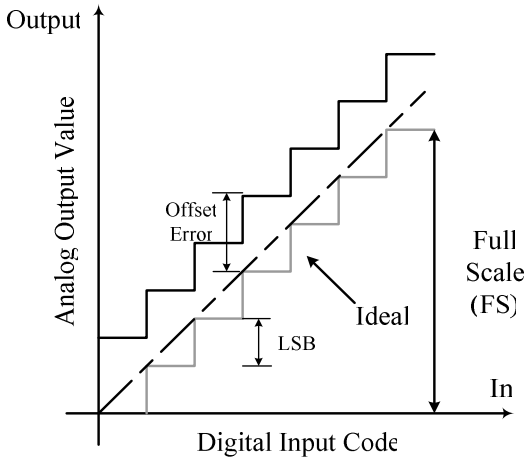


Fig. 6.3 Non-ideal transfer curve with offset error

6.2.1.2 Gain Error

Gain error is the difference at the full-scale value between the ideal and actual when the offset error has been reduced to zero. For a non-ideal transfer curve with gain error shown in Fig 6.4, the gain error can be expressed as:

$$GainError = \frac{X_a - X_i}{(2^N - 1) \bullet LSB} \tag{6.2}$$

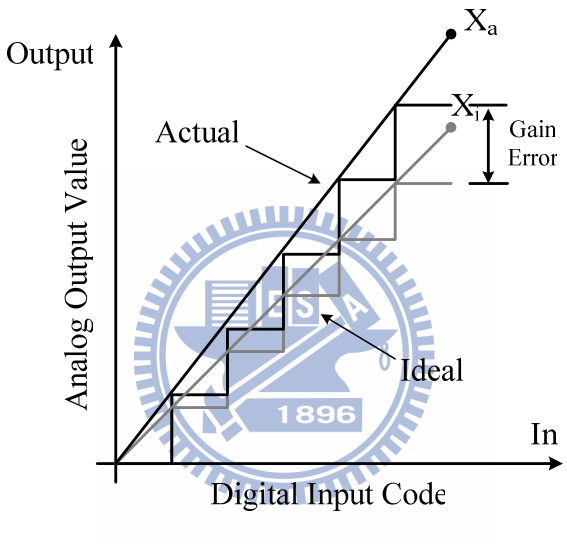


Fig. 6.4 Non-ideal transfer curve with gain error

6.2.1.3 Differential Non-Linearity (DNL)

The step size in the non-ideal data converter deviates from the ideal size Δ and this error is called the differential non-linearity (DNL) error. For a DAC the DNL can be defined as the difference between two adjacent analog outputs minus the ideal size, ie.

$$DNL_k = X_{a,k+1} - X_{a,k} - \Delta \tag{6.3}$$

The DNL is often normalized with respect to the step size to get the relative error, ie.

$$DNL_k = \frac{X_{a,k+1} - X_{a,k} - \Delta}{\Delta} \tag{6.4}$$

The above definitions are often most practical for DACs since the analog values can be directly measured at the output.

6.2.1.4 Integral Non-Linearity (INL)

The total deviation of an analog value from the ideal value is called integral non-linearity (INL). For non-ideal transfer function with INL and DNL errors show in Fig 6.5, the normalized INL can be expressed as

$$INL_k = \frac{X_{a,k} - X_{i,k}}{\Delta} \tag{6.5}$$

The relation between INL and DNL is given by

$$INL_k = \sum_{l=1}^{k} DNL_l \tag{6.6}$$

The non-linearity errors are usually measured using a low frequency input signal to exclude dynamic errors appearing at high signal frequencies. The DNL and INL are therefore usually used to characterize the static performance.

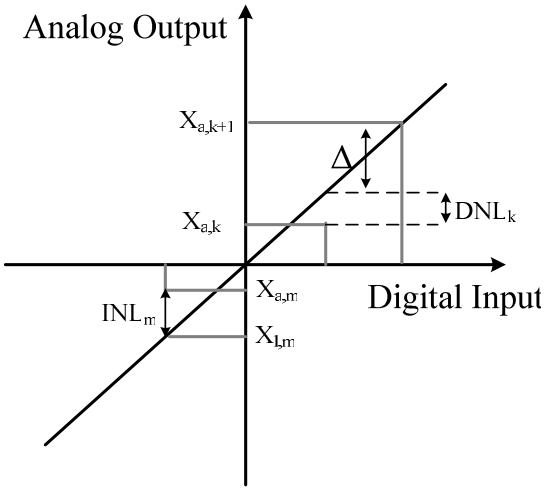


Fig. 6.5 Non-ideal transfer function with INL and DNL error of DAC

6.2.1.5 Monotonicity

If the analog amplitude level of the converter increases with increasing digital code, the converter is monotonic. An example of a non-monotonic DAC is shown in Fig. 6.6.

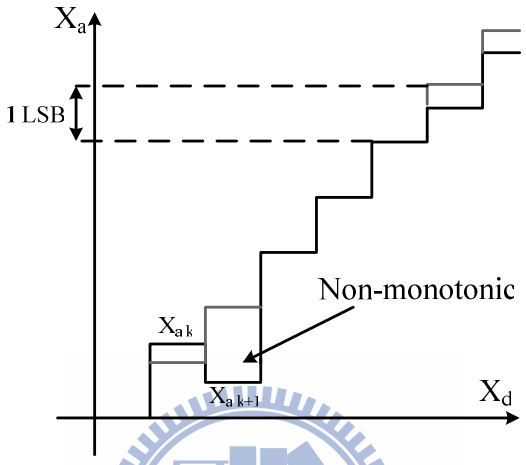


Fig. 6.6 A non-monotonic DAC

Monotonicity is guaranteed if the deviation from the best-fit straight line is less than half a LSB, ie.

$$|INL_k| \le \frac{1}{2} LSB \qquad \text{for all k} \tag{6.7}$$

This implies that the DNL errors are less than one LSB, ie.

$$|DNL_k| \le 1LSB \qquad \text{for all k} \tag{6.8}$$

It should be noted that the above relations are sufficient to guarantee monotonicity, but it is possible to have a monotonic converter that does not meet the relations in (6.7) and (6.8).

6.2.2 Dynamic Performance

In addition to the static errors that are cause by mismatch in the

components in the data converter several other error sources will appear when the input signal change rapidly. These dynamic errors are often dependent on signal frequency and increase with signal amplitude and frequency. They appear in data converter but are usually more critical in DACs since the shape of the analog wave form determines the performance.

6.2.2.1 Settling Time

The settling time is defined as the time it takes for the converter to settle within some specified amount of the final value. The primary dynamic characteristic of the DAC is the conversion speed. The settling time define the operation frequency of DAC. The factors that determine the setting time of the DAC are the gain bandwidth, slew rate of OPamp and parasitic capacitor. The output of transition can be illustrated as Fig. 6.7.

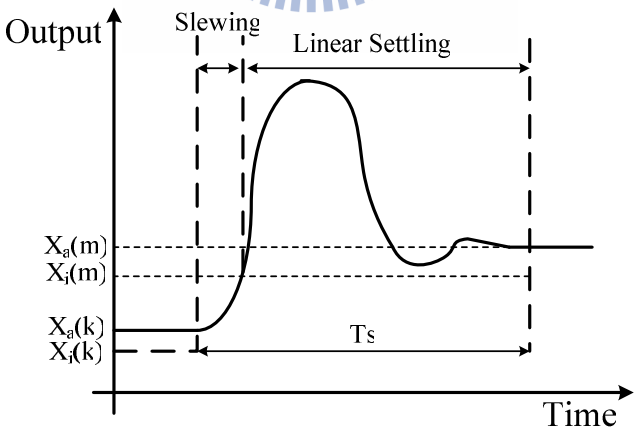


Fig. 6.7 Actual output signal and ideal output signal (dash) of a DAC

The settling can be divided in two phases, a non-linear slewing phase and a linear settling phase. The output signal of an actual DAC can not

change its value instantly. The time it takes for output to settle within a certain accuracy of the final value, for instance 0.1%, is called the settling time and introduce distortion in the analog waveform. The slewing is normally caused by a too small bias current in the circuit driving the output and is therefore increased for large steps when more current is needed.

6.2.2.2 Glitch

When the switching time of different bits in binary weighted DAC is unmatched, the glitch occurs. As Fig 6.8, if a DAC decodes 011 code to 100 code sequentially, the fast MSB changes previously than others. The output of a DAC will occur the error value. The plus effect of the output caused by different switching is called glitch.

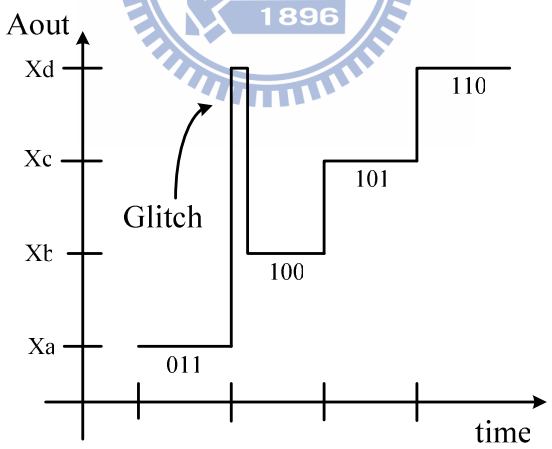


Fig. 6.8 Glitch output

6.3 DAC for LCD column driver

6.3.1 Resistor-String DAC

In addition, the accuracy of this DAC depends on the matching precision of resistors on the resistor string. However, the matching precision of resistor depends on the process of resistors used. Fig. 6.9 and Fig. 6.10 show two types of resistor-string DAC. The major differences between them are the architecture of decoder. First type employs the tree-like decoder as its decoder, and the decoder of second type used digital method. The properties of them are compared and listed bellow:

- DAC using tree-like decoder:
  - Speed is limited by the delay through switch network.
  - Using binary coder.
- DAC using digital decoder:
  - Simple and monotonic.
  - Good DNL (differential nonlinearity) error.
  - Higher speed than tree-like decoder.
  - Large chip size at higher bits.

In summary, it can say that, both of them are suitable for gamma correction DAC, because they are easy to produce different sections in resistor string. Furthermore, the operational speed of DAC using digital decoder is faster than DAC using tree-like decoder. But, DAC using digital decoder will consume more die area.

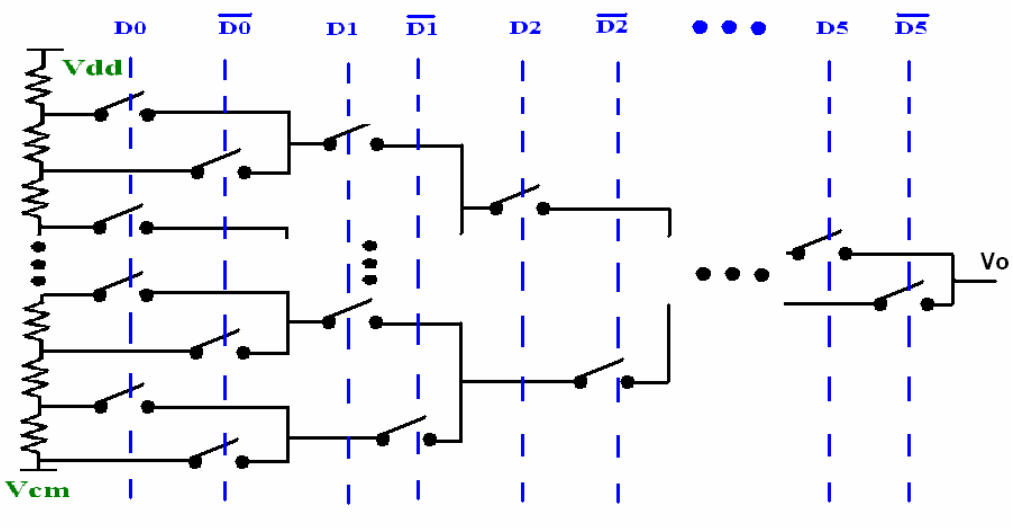


Fig. 6.9 DAC using tree-like decoder

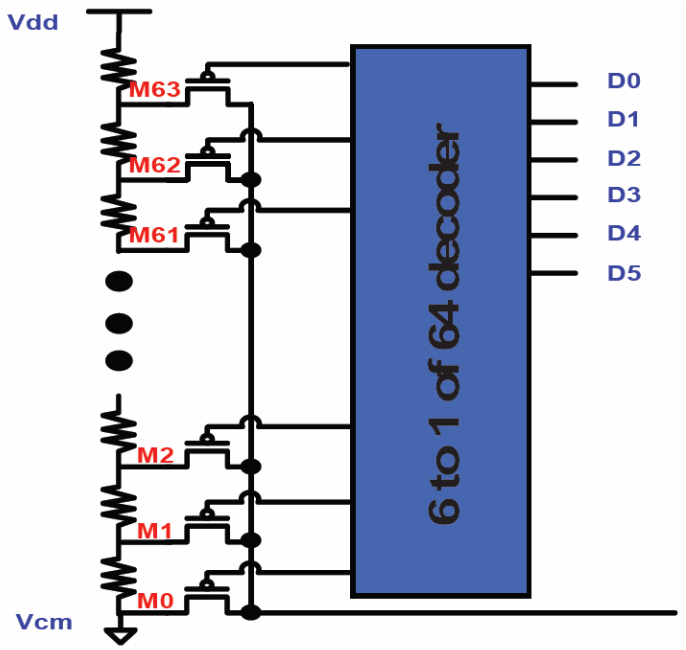


Fig. 6.10 DAC using digital decoder

6.3.2 Charge-Redistribution DAC

As shown in Fig. 6.11, it is the conventional charge-redistribution DAC. In this circuit, it has two phases. In first phase (φ1), all capacitor bottom plates are connected to a reference voltage and top plates are connected to ground. During second phase (φ2), capacitor

bottom plates are connected to a reference voltage or ground according to logic high or logic low in codes. And capacitor top plates are floating during this phase. By this operation, the voltage level in output terminal can be determined by a formula which is shown in follow:

$$V_o = V_{ref} \times \left(\frac{C}{2^N C + C_p}\right) \times \sum_{i=0}^{N-1} b_i 2^i \qquad (6.9)$$

Where bi is the bit number in input code and N is the total bit number. This circuit structure has some advantages better than the resistor-string DAC. First, the process matching for capacitor is better than resistor string. Second, charge-redistribution DAC can save more power. However, it has a big problem in LCD panel application. That is, this method is very difficult to achieve gamma correction. In other word it can not compensate the inherent characteristic of liquid crystal, so LCD column driver often use R-string DAC.

6.4 Summary

In this chapter, the fundamental of the digital-to-analog Converter (DACs) is presented first. The performance parameters used to characterize the specifications of DAC is also described. Also, some DACs for LCD column driver are introduced.

According to the discussions of advantages and disadvantages for two type DACs, LCD column driver often use R-string DAC, but R-string DAC have some problem for LCD column driver must overcome. So we develop a new system using a linear DAC for LCD column driver.

CHAPTER 7
A LCD Column Driver Using a Switch Capacitor DAC

LCD column drivers have traditionally used non-linear R-string style digital-to-analog converters (DAC). This chapter describes an architecture that uses linear charge redistribution DAC to implement LCD column driver. DAC performs its conversion in less than 15μs and draws less than 5μA.[5]

7.1 Introduction

The resistor string DAC has the following problems [5]:

- The inverse transfer curve is hardwired on each part, requiring accustom die for each type of LCD panel.
- The resistor string is not accurate enough. To obtain consistent voltages from die to die, 16 taps are brought out, wired together, and driven externally.
- The current in the resistor string is too high for mounting the die directly on the LCD glass.
- The die size becomes excessive for 10 bits per color.
- Supporting independent inverse transfer curves for each color increases the die size.

Because problems above-mentioned, we have developed a complete system using a linear DAC in the column driver. The linear DAC keeps the

die size small as well as supporting additional features.

7.2 Column Driver Architecture

The new column driver block diagram is shown in Fig. 7.1 [5]. The deserializer deskews the data and formats it into 4-bit parallel data at half the clock rate. The digital block sends the pixel data to the DACs, sequences the DAC's conversion, and controls their output enables. In our research, we only discuss two DACs per output.

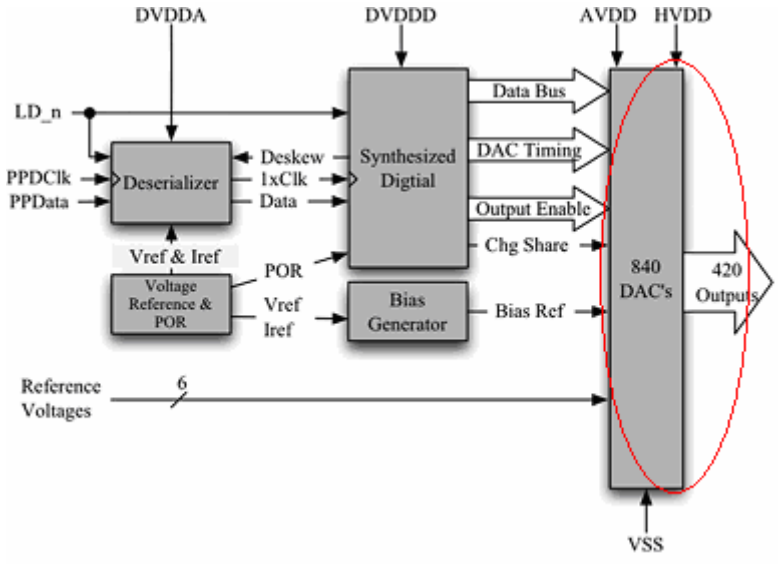


Fig. 7.1 New column driver block diagram [5]

There are two DACs per output. This configuration allows a full line time for one set of DACs to convert the digital data to an analog voltage, while the other set provides the output to the panel for the current line. Due to the symmetry of the LCD response and the use of pixel inversion in LCD panels, adjacent columns are always in opposite ranges above and below half the power supply. To take advantage of this, half of the DACs

cover the upper range and half cover the lower range. This symmetry improves the accuracy since each DAC must only span half the power supply voltage. Another advantage is that the current for the DACs can be shared. This arrangement is shown in Fig. 7.2 In this stacked design, current from the upperDACs flows through the lower ones, halving the total current. This design requires a third power supply pin, HV_{DD}, to maintain the center at $AV_{DD}/2$. If the currents for the upper and lower DACs are equal, the DC current supplied by HV_{DD} power pin is minimal.

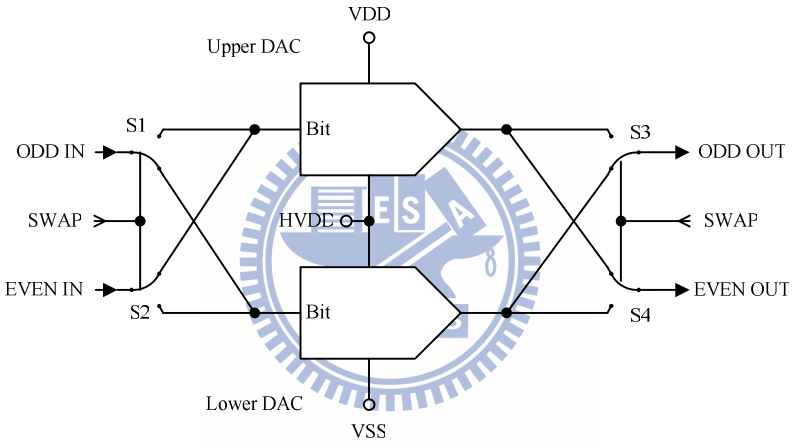


Fig. 7.2 Stacked amplifier configuration

7.3 Cyclic Switched Capacitor DAC

The DAC is the heart of the column driver. Charge redistribution (or cyclic) architecture was chosen for its small size and superior accuracy.

7.3.1 DAC Operation

Fig. 7.3 is a simplified schematic of the DAC. The SIGN and BIT signals are local; all other external signals are global. The circuitry in the

left box is shared between two copies of the circuitry in the right box. The switches not shown as NMOS transistors are CMOS switches and will require both the signal and its complement.

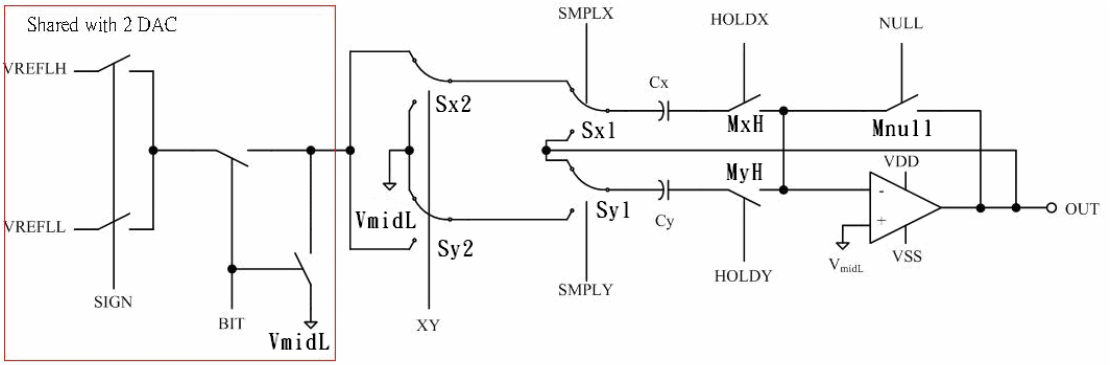


Fig. 7.3 Simplified schematic of lower DAC

The circuit produces an output according to the expression

$$V_{OUT} = V_{MIDL} + \left(S \cdot V_{REFLL} + \bar{S} \cdot V_{REFLH} - V_{MIDL}\right) \times \sum_{n=0}^{N-2} \frac{b_n}{2^{N-n-1}} \qquad (7.1)$$

where is sign bit, N is total number of bits converted, and is the bit to be converted. The three voltages, V_{MID}, V_{REFLL}, and V_{REFLH} are provided externally on pins. An identical circuit and three more reference voltages are needed for the upper range. Note that to obtain N-bit accuracy only N-1 conversions are required. The sign bit provides the additional bit. The sign bit is not converted; it is only used to select the reference.

The converter will be most accurate at V_{MIDL} since no charge is added for the MSBs. There will be no large error when the most significant bit (the sign bit) is changed because it only selects the reference. Fig. 7.4 is a plot of the DAC's output and the inverse transfer curve of the LCD. The center of the DAC can be positioned at the most sensitive portion of the LCD's response by careful choice of the reference voltages.

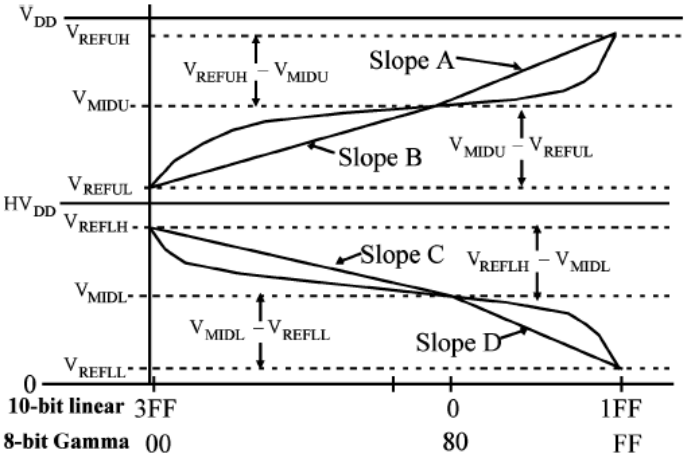


Fig. 7.4 DAC output versus linear and LCD respone [5]

During the first $\phi 1$, the switches are set to that of Fig. 7.5(a). Cx is the integration capacitor, Cy is the sampling capacitor, and MyH is always on. The first phase resets Cx and samples either the V_{REFLH}, V_{REFLL}, or V_{MIDL} (depending on the sign and bit values) onto Cy. The two capacitors are then placed in parallel during $\phi 2$ and the charge summed as shown in Fig. 7.5(b). The next cycles are identical except that Cx is left floating during $\phi 1$. Fig. 7.6 shows a timing diagram. Each conversion can be done in 1 μs. Most panels will require over 2 μs per conversion.

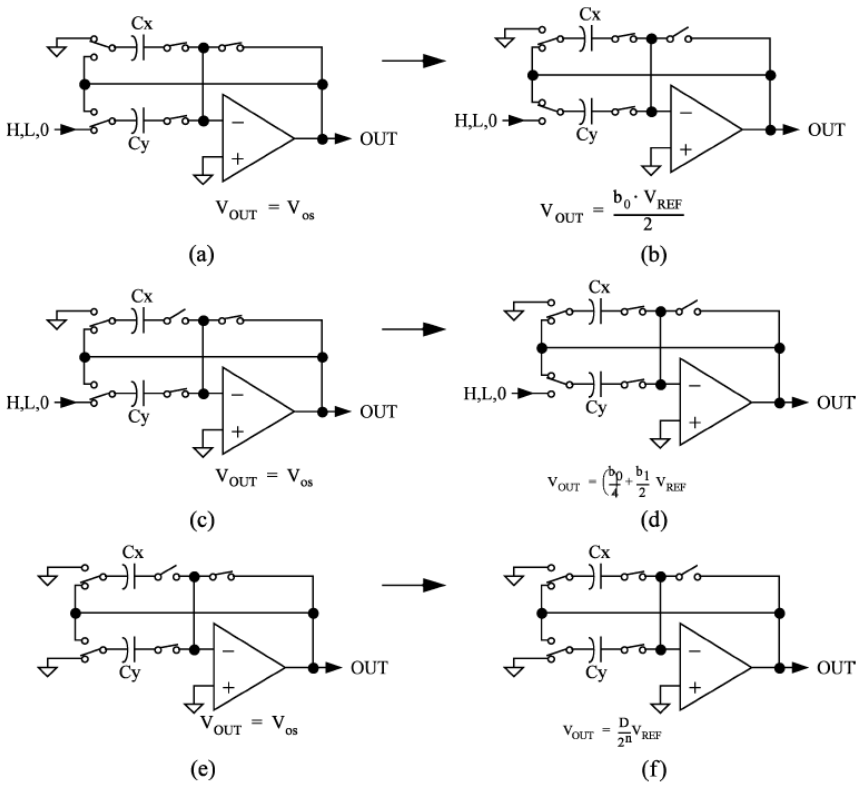


Fig. 7.5 DAC conversion sequence (a)ϕ10 and rest; (b)ϕ20; (c)ϕ11; (d)ϕ21; (e)ϕ1N; (f)ϕ2N [5]

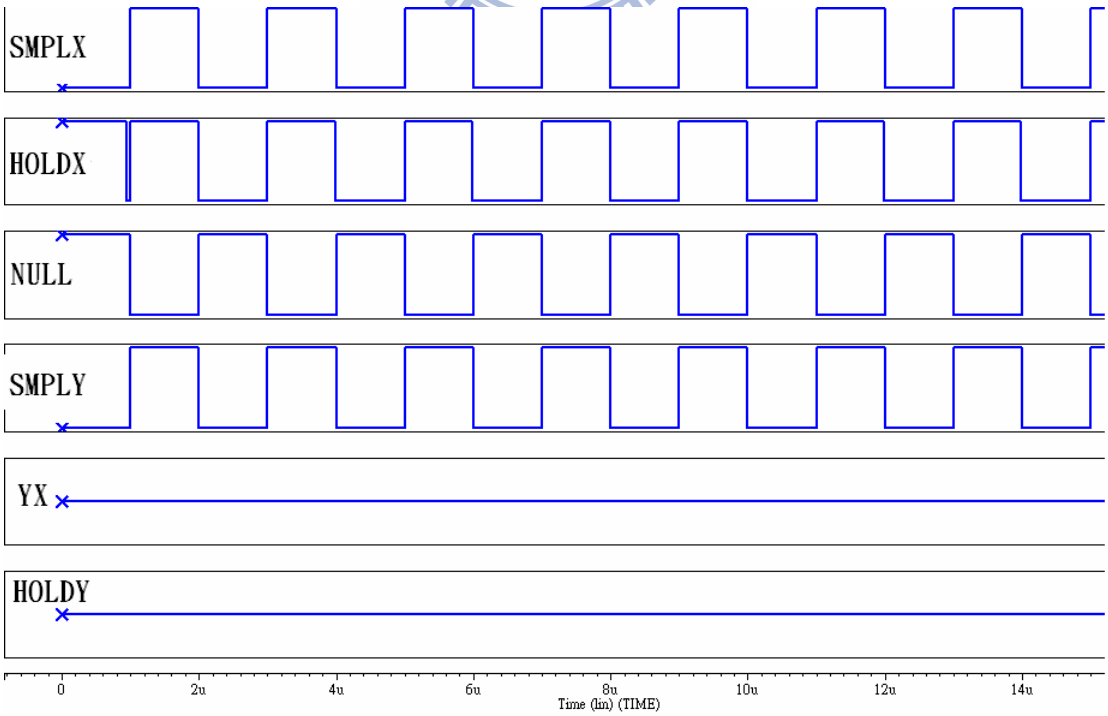


Fig. 7.6 Control signal timing

The last cycle is different. In this cycle Cy is always connected to and is not paralleled with Cx, but instead is left connected to V_{MIDL}, placing Cy between the inverting input of the amplifier and V_{MIDL}. Cy now forms the Wishakaboogle capacitor, which attenuates excursions of the negative input when output switched to the output pad.

The final voltage is held on Cx and its bottom plate is switched to the output pin separately through the main output switch inside the feedback loop.

There is no dependence on AV_{DD} or V_{SS}. The LSB is converted first and its contribution to the final value is divided by 2^{N-1}. If the noise V_{DD} on V_{SS} and cannot be entirely rejected by the amplifier at the beginning of the line (when the other amplifiers begin driving the panel) the error will be reduced by a factor of 2^{N-1}.

Conversion of the first bit requires the amplifier to reach $V_{MIDL} \pm V_{REF}/2$ or $AV_{DD}/2$ approximately from the power supply rails. The second conversion will put the amplifier's output at $V_{MIDL} \pm 3V_{REF}/4$ or $AV_{DD}/4$ approximately from the power supply rails. Only the last few conversions require the output of the amplifier to be within 200 mV of either power supply rail. AV_{DD} and V_{SS} will have recovered from driving the LCD array by this time.

7.3.2 DAC system's noise

The greatest source of error is from capacitor mismatch. Writing (7.1) incorporating the capacitor mismatch (and ignoring the sign bit) gives

$$V_{OUT} = V_{MIDL} + V_{REFL} \times \sum_{n=0}^{N-2} \frac{b_n}{\left(1+\frac{C_X}{C_Y}\right)^{N-n-1}} \tag{7.2}$$

In the actual implementation of the column driver, four DACs (two in the upper range and two in the lower range) are shared between two outputs. If it is assumed that the mismatch will be randomly distributed, uncorrelated, and that each output over four frames is the average of the four DACs.

Time averaging of the output can be used to reduce the capacitor mismatch error. Note that in Fig. 7.3 the circuits for C_X and C_Y are identical. In the circuit description, M_{YH} was always on. Changing the timing reverses the roles of C_X and C_Y. This role swapping allows the capacitor mismatch to be averaged.

Another DAC system's noise is charge injection. Device charge injection has three sources:

- M_{XH} turning off
- M_{NULL}turning off
- M_{XH}turning on

Ignoring the reset phase for the moment, coming out of $\phi 2_0$, M_{XH} is turned off, which $\Delta_H Q_{XH}$ injects onto C_X and $(1-\Delta_H)\ Q_{XH}$ onto C_Y where the Δ's represent the charge split from M_{XH}. Now in $\phi 1_1$ the amplifier is placed in unity gain and the bit voltage is stored on C_Y; eliminating any previous charge injection on C_Y. To get to $\phi 2_1$, M_{NULL} is turned off first,

which $\Delta_N Q_{NULL}$ injects onto C_Y. Next, M_{XH} turns on injecting $-Q_{XH}$ onto both C_X and C_Y. So the final charge injection is

$$Q_T = \Delta_H Q_{xH} + \Delta_N Q_{null} - Q_{xH}$$
$$Q_T = Q(\Delta_H + \Delta_N - 1) \quad (7.3)$$

The charge injection does not increase with each conversion because each conversion will divide the previous error by two. The total charge injection at the final output is

$$Q_{FINAL} = \frac{Q_{RESET}}{2^{N-1}} + Q(\Delta_H + \Delta_N - 1)\sum_{n=2}^{N}\frac{1}{2^{N-n}} \quad (7.4)$$
$$\approx Q(\Delta_H + \Delta_N - 1)$$

The reason for the in the N summation instead of N-1 is due to the last nulling phase for the Wishakaboogle capacitor. The charge injected during the reset phase is different than the others, but since it is reduced by 2^{N-1}, it can be ignored.

7.3.3 DAC 'S Amplifier

The most important characteristics of the amplifier are [1] [2]:

- High slew rate : > 15 V/μs(which implies that 90% of the maximum output voltage is reached within 20% of T_{CK}/2);
- Low power : < 10μA/amplifier;
- Unity-gain bandwidth : > 1MHz(The clock period, T_{CK} chosen equal to 2μs, requires that the amplifier GBW should be at least 2/T_{CK});
- Capable of driving the LCD column load(500fF);
- Gain : > 66dB(for a maximum conversion error due to the finite gain lower than 1mV, i.e, 1/5LSB for 5V 10-bit)

The amplifier is shown in Fig. 14. It is a modified folded cascade

design with a class AB output stage. M1 and M2 form the input differential pair. This ampifier's characteristic will discuss one by one.

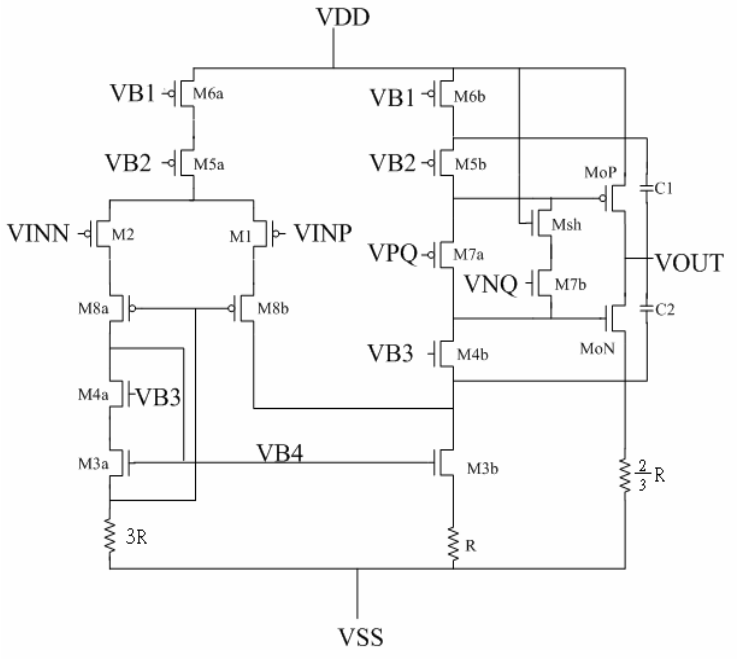


Fig. 7.7 DAC amplifier schematic

7.3.3.1 Increasing the Slew Rate

In the conventional folded cascode design the slew rate is I/C, where I is the current source of the differential pair and C is the total compensation capacitance.

In this amplifier, consider the case when the INP input goes high. All the tail current, I, flows through M_2, M_{8a}, M_{3a} and M_{4a}. The mirror is 3:1 so M_{3b}'s sinks 3I. M_{5b} sources I so the total current into C_1 and C_2 is I - 3I = -2I.

When the INP goes low. I flows through M_1 and M_{8b}. M_{3b}'s drain current is zero, so the total current into C_1 and C_2 is again: I + I = 2I. In both cases, the current is double that of the conventional folded cascade.

7.3.3.2 Class AB Control

In order to drive the high capacitive load of the LCD column, a class AB output stage is used as the second stage of the amplifier. The output devices, M_{oP} & M_{oN}, provide this drive. Their gates cannot be connected together like an inverter because they would draw too much current. Ideally, it would be best to put a voltage source between their gates. M_{7a} & M_{7b} do just that.

To see how this circuit works, consider the small-signal impedance between the gates of the output devices.

$$z_{PDRIVE,NDRIVE} = \frac{v_{PDRIVE} - v_{NDRIVE}}{v_{PDRIVE} \cdot gm_{7a} - v_{NDRIVE} gm_{7b}} = \frac{\Delta v}{\Delta v \cdot gm_7} = \frac{1}{gm_7} \tag{7.5}$$

Thus, there is low impedance connecting the gates of the output devices. During large signal transients either M_{7a} or M_{7b} is cut off, causing one output transistor to handle the large current while the other one's drain current remains constant.

The quiescent current with no load is fairly easy to see. P_{biasQ} is generated by two diode-connected devices identical to M_{oP} and M_{7a} and a current, I_{REF}. N_{biasQ} is generated in a similar fashion using the same I_{REF}. If everything is matched, the result is two current mirrors and the quiescent current in the output leg is I_{REF}.

For small loads all the devices are in the subthreshold region and their currents are given by

$$\frac{I_{MoP} \cdot I_{MoN}}{I_{MoP} + I_{MoN}} = I^2_{REF} \tag{7.6}$$

It is difficult to calculate the output currents as the amplifier delivers current to the load and the devices transition from weak to strong inversion. The maximum current is that with M_{oP} or M_{oN} ' s gate pulled to the opposite rail, so the maximum current is set by the size of M_{oP} and M_{oN}.

There is some concern about mismatching between the bias circuit devices and the amplifiers. Simulations have show that with a ± 50 mV mismatch the bias will vary 2.5:1. This offset affects the settling time of the amplifier, which is one of the reasons that $M_{7a,b}$, M_{oN}, and M_{op} are longer than minimum. The matching improves with longer devices. Unfortunately, the NMOS devices, M_{7b} and M_{oN} will have a large body bias ($AV_{DD}/2$) when used in the upper range and making them too long causes their gate voltages to rise. This high V_{GS} reduces the available headroom when operating below 10 V and a compromise had to be reached.

Another reason for making the output devices, M_{oN} and M_{oP} longer than minimum, is that their V_{DS} is different than their counter parts in the bias block. The bias devices have $V_{DS} = V_{GS}$, but the output device' s V_{DS} can be as much as $AV_{DD}/2$. Making them as long as possible increases their drain impedance and reduces this variation. It also reduces their drive capability, so again there is a compromise.

7.3.3.3 Cascoded Miller Compensation

Stability is achieved with cascoded Miller compensation formed by C1 and C2.

Fig. 7.8 is a simplified small signal equivalent of the output stage. The transconductance, gm_c, is the cascode device of the folded cascade (M_{4b} or M_{5b}), and gm_o is the output device (M_{oP} or M_{oN}). I_s is the current source (M_{3b} or M_{6b}). C_C is the total compensation capacitance (C1 + C2), C_L is the load capacitance, and C_g is the gate capacitance of the output device. r_C is the output resistance of the cascode device.

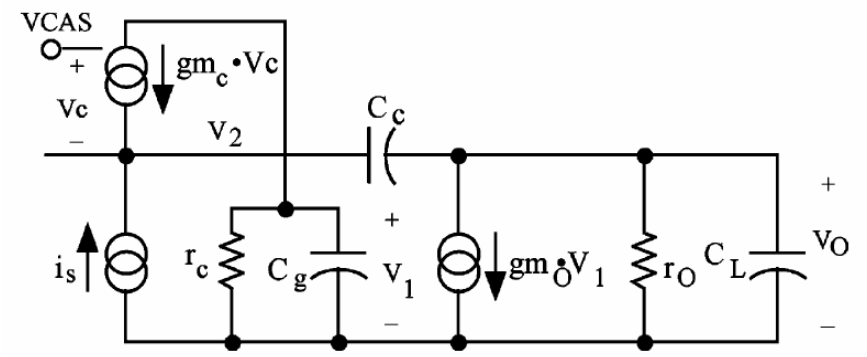


Fig. 7.8 Small signal representation of output stage with cascade Miller compersation [5]

To make the analysis easier, assume that is large enough that gm_1 the impedance at V_2 is zero. The expression for V_0 is then

$$V_O = \frac{-g_m r_O}{(Cg + CL) r_O s + 1} \tag{7.6}$$

V_1 is

$$V_1 = (i_s + C_C \cdot s \cdot V_O) \cdot \frac{r_C}{r_C \cdot Cg \cdot s + 1} \tag{7.7}$$

Solving for V_O/i_S, we get (7.6), shown at the bottom of the page. If the poles are far apart, the approximate expression for them is written as

$$P_1 \approx \frac{-1}{(C_G + C_L)\cdot r_O + r_C \cdot C_g + gm_O \cdot r_O \cdot r_C \cdot C_C}$$

$$\approx \frac{-1}{gm_O \cdot r_O \cdot r_C \cdot C_C} \tag{7.8}$$

$$P_2 \approx \frac{(CG + CL)\cdot rO + rC \cdot Cg + gm_O \cdot r_O \cdot r_C \cdot C_C}{(C_G + C_L)\cdot r_O \cdot r_C}$$

$$\approx \frac{gm_O \cdot C_C}{(C_G + C_L)\cdot C_G} \approx \frac{gm_O \cdot C_C}{C_L \cdot C_G} \tag{7.9}$$

The expressions have some significant differences from those of the conventional Miller compensation. First, note that there is no right half-plane zero. This zero causes much grief in low current circuits due to the low gm of the output transistor. P_1 is the same as that of the conventional Miller compensation, but P_2 is different. For conventional Miller compensation

$$P_{2M} \approx -\frac{gm_O \cdot C_C}{(C_G + C_C)\cdot C_L} \approx -\frac{gm_O}{C_L} \tag{7.10}$$

P_2 for the cascoded Miller compensation is increased by the term C_C/Cg which is the ratio of the compensation capacitor to the output device's gate capacitance. In this amplifier this ratio is about 2:1 for the PMOS output and 5:1 for the NMOS. The gain bandwidth using cascoded Miller compensation is three times higher than if a conventional Miller compensation was used.

There is another consequence of using Miller compensation that is not obvious. The output impedance at high frequencies is not r_0, but $1/gm_0$, which is why P_2 is gm_0/C_L, allowing the amplifier to reject high frequency signals coupled to its output.

The value for C_C can be calculated for a 45 phase margin by making the gain times the low-frequency pole equal to the second pole:

$$P_1 \cdot A_V = P_2 \Rightarrow \frac{A_V}{gm_O \cdot r_O \cdot r_C \cdot C_C} = \frac{gm_O \cdot C_C}{C_L \cdot C_G} \tag{7.11}$$

Solving for C_C

$$C_C = \sqrt{\frac{A_V \cdot C_L \cdot C_G}{gm_O^2 \cdot rO \cdot rC}} \tag{7.12}$$

Note that the gm_0r_0 term is just the gain of the output stage. So this reduce to

$$C_C = \sqrt{\frac{A_1 \cdot C_L \cdot C_G}{gm_O \cdot rC}} \tag{7.13}$$

where A1 is the gain of the first stage. But the gain of the first stage is $Gm_{1,2}r_C$, so now

$$C_C = \sqrt{\frac{Gm_{1,2} \cdot C_L \cdot C_G}{gm_O}} \tag{7.14}$$

The devices are all in weak inversion, so putting in the expressions for gm_0 and $Gm_{1,2}$ taking into account the source degeneration resistors

$$C_C = \sqrt{\frac{2C_L \cdot C_G}{\frac{2nV_T}{I} + R} \cdot \frac{2nV_T}{4I}} = \frac{1}{2}\sqrt{\frac{C_L \cdot C_G}{\frac{IR}{2nVT} + 1}} \tag{7.15}$$

where V_T is the thermal voltage, KT/q, and I is the bias current.

This expression demonstrates that reducing $Gm_{1,2}$ by source degeneration, reduces the size of the compensation capacitor C_C.

$$Gm_{1,2}=\frac{V_O}{i_S}=\frac{-gm_D\cdot r_O\cdot r_C}{(C_G+C_L)\cdot r_O\cdot r_C\cdot s^2+[(C_g+C_L)\cdot r_O+r_C\cdot C_g+gm_D\cdot r_O\cdot r_C\cdot C_C]s+1} \tag{7.16}$$

Increasing I or R will reduce the size of C_C. Alternately, keeping C_C constant and increasing R or I will improve the phase margin. Note that setting R to zero makes the value of C_C independent of the bias current.

When the amplifier is performing conversions, C_L=0.5 pF. For the output devices C_g=50fF. I=1μA and R=100 KΩ. So C_C will be

$$C_C=\frac{1}{2}\sqrt{\frac{0.5pF\cdot 50fF}{\frac{1\mu A\cdot 100\mathrm{K}\Omega}{2\cdot 2\cdot 0.026V}+1}}=0.113pF \tag{7.17}$$

This provides a starting value for C_C. The equation is only approximate, and a phase margin closer to 60° was required. After simulations over process, temperature, and bias currents, Cc was set to 1 pF (0.5 pF + 0.5 pF).

When driving the LCD load, the amplifier does not see a pure capacitive load and does not require as fast a settling time.

7.4 Simulation Result

First, we simulation our modified folded cascade design with a class AB output stage use TSMC 0.35 μm process in different corner, as a result in table 7.1.

Table 7.1 Performance of the Amplifier

Simulation Results	TT @ 50° C	FF @ 0° C	SS @ 100° C
Differential Gain	70.8 dB	68 dB	72 dB
Phase Margin	62°	60°	58°
Unity-Gain Frequency (5p)	2.2 MHz	2.4 MHz	2 MHz
Output Swing	4V		
Power Dissipation	about 57 μW		

Because TSMC 0.35 μm process is not high voltage process and does not have deep-subtrate technique, we simulation higher DAC and lower DAC one by one. We only simulation one set of DACs to make sure they function correct, as a result in Fig.7.9 and Fig. 7.10.

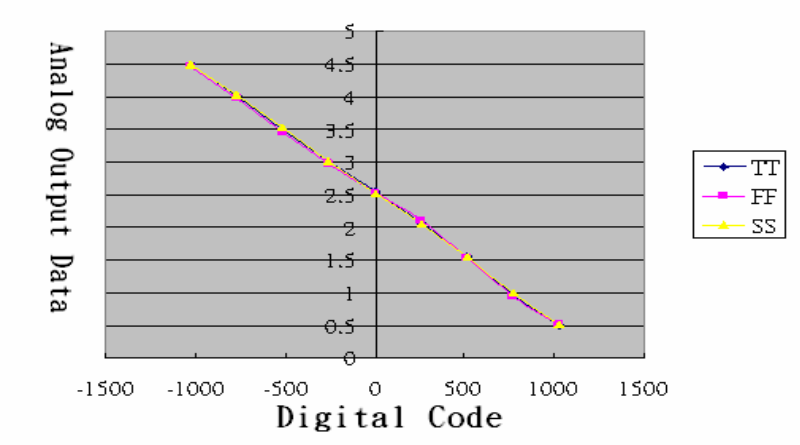


Fig. 7.9 Lower DAC simulation result

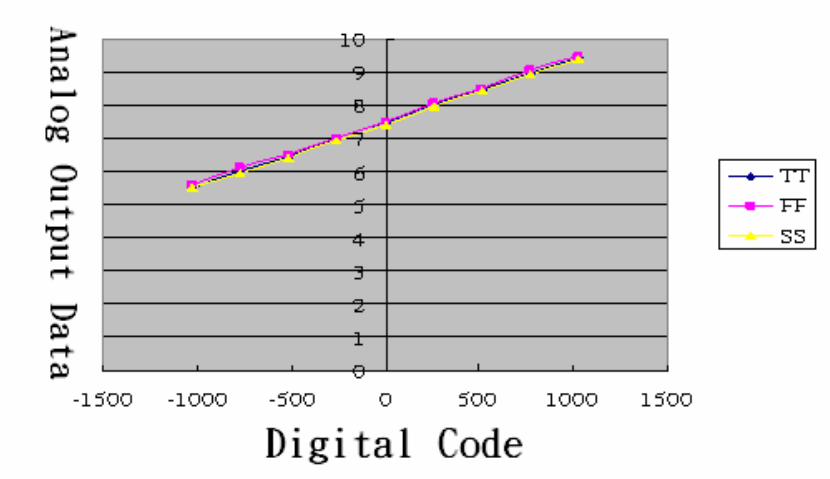


Fig. 7.10 Higher DAC simulation result

7.5 Summary

A LCD column driver using a switch capacitor DAC in TSMC 0.35μm process. This new architecture will solve the resistor string DAC's problems for LCD column driver. Although we don't finish whole LCD column driver or tapout chip, we use Hspice to simulation and verify the set of DACs can work correct and linearity.

CHAPTER 8
Test Setup and Measurement Results

8.1 Introduction

The continuous-time single-bit active-RC sigma-delta modulator for 1 MHz bandwidth by TSMC 0.18μm CMOS mixed-signal process, respectively. In this chapter, we present the testing environment, including the components on the printed circuit board (PCB) and instruments. Finally, the measurement results are shown and summarized.

8.2 Measuring Environment

Fig. 8.1 shows the measurement process. We use three power supplies, two function generators, an oscilloscope and a PC for Matlab processing to measure the device under test (DUT). The PCB contains single-to-differential transformers, bias, reference voltage generator and regulators which are analog, digital and clock parts. The separated regulators are supplied by power supplies respectively to isolate noise interference. The input signal and clock are provided by function generator hp 8656B and ROHDE & SCHWARZ SML03 shown in Fig. 8.2 and 8.3. The output waveform can be observed through the use of the oscilloscope and the digital output signals are fed into logic analyzer Agilent 16902A, as shown in Fig. 8.4. The output data are loaded into a PC and then by

using Matlab, the power spectral density performance can be obtained.

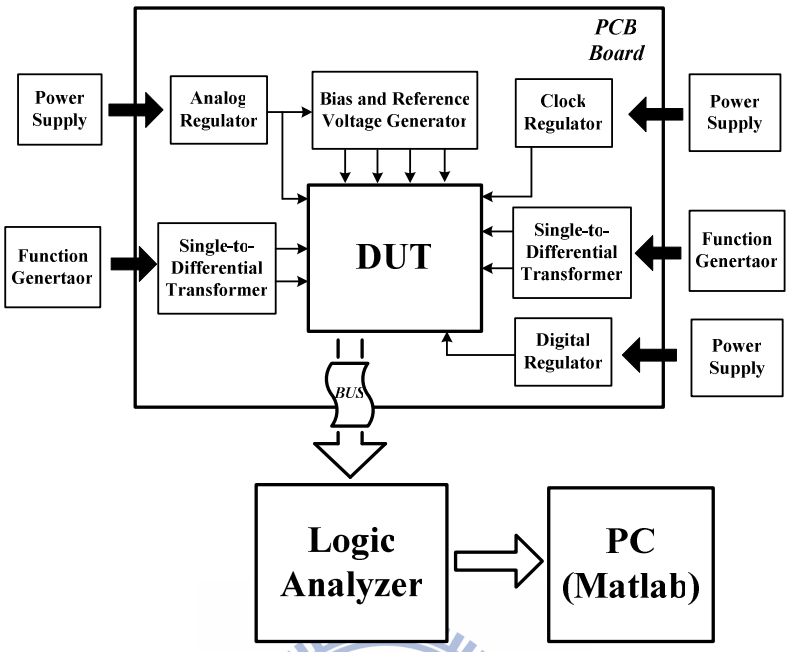


Fig. 8.1 Test setup

Fig. 8.2 Function generator hp 8656B for input signal

Fig. 8.3 Function generator ROHDE & SCHWARZ SML03 for clock

Fig. 8.4 Logic analyzer Agilent 16902A

8.2.1 Power Supply Regulator

The supply voltages are generated by LM317 adjustable regulators as shown in Fig. 8.5. The C_{in} is the bypass capacitor and the C_{out} is added to improve the transient response. The C_{ADJ} is used to increase the supply voltage rejection. The regulator provides an internal reference voltage of 1.25V between the output and adjustments. This is used to set a constant current. The output voltage of the regulator can be expressed as [23]

$$V_{out} = 1.25 \cdot (1 + \frac{R_2}{R_1}) + I_{ADJ} \cdot R_2 \qquad (8.1)$$

where I_{ADJ} is the DC current that passes through the variable resistor R_2. The device is designed to minimize the term I_{ADJ} and to maintain it very constant with line and load changes.

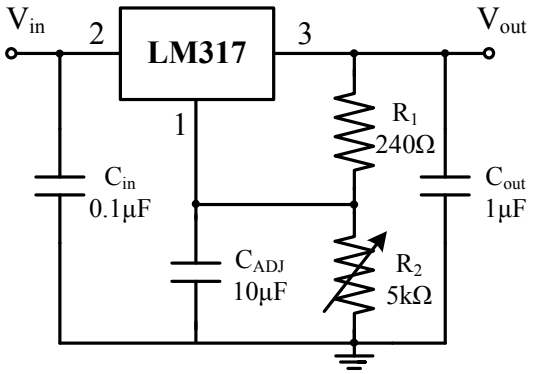


Fig. 8.5 Power supply regulator

8.2.2 Single-to-Differential Transformer

In Fig. 8.2 and 8.3, the output signal of the function generators is single-ended and only provides the ac component. Therefore, for our fully differential design, the single-to-differential transformer is needed as shown in Fig 8.6. Through the transformer, the differential output signal can be obtained and by using reference voltage generator, the common-mode voltage can be added to ensure the DC bias. Since the output impendence of the RF terminal is 50Ω, we use two 25Ω-resistors to match the resistance. The capacitor is used to steady the voltage, as the decoupling capacitor.

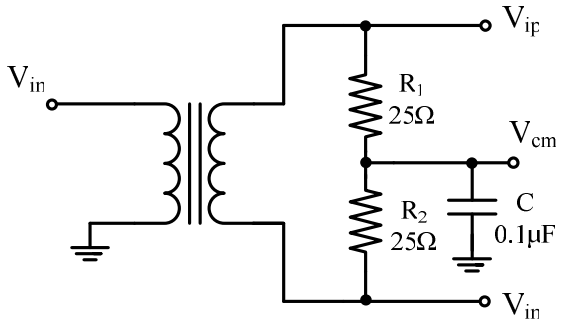


Fig. 8.6 Single-to-differential transformer

8.2.3 Reference Voltage Generator

In hybrid sigma-delta modulator with digital error truncation, due to the influence of the loading effect, the reference voltage can be varied to result in errors. Hence, we need to add a buffer to avoid the effect. Fig. 8.7 shows the use of the OP27 operated as the unity-gain buffer. The OP27 is supplied by ±9V voltage.

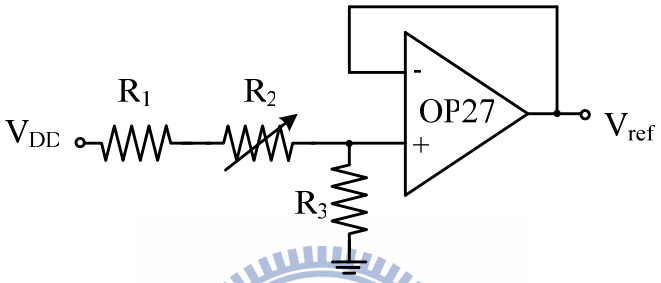


Fig. 8.7 Reference voltage generator

8.3 PCB and Pin Configurations

Fig. 8.8 shows the PCB of the continuous-time single-bit active-RC sigma-delta modulator for 1 MHz bandwidth. Fig. 8.9 presents the pin configurations and lists the pin assignments of the CT modulator. Fig. 8.10 shows the die photo of the CT SDM.

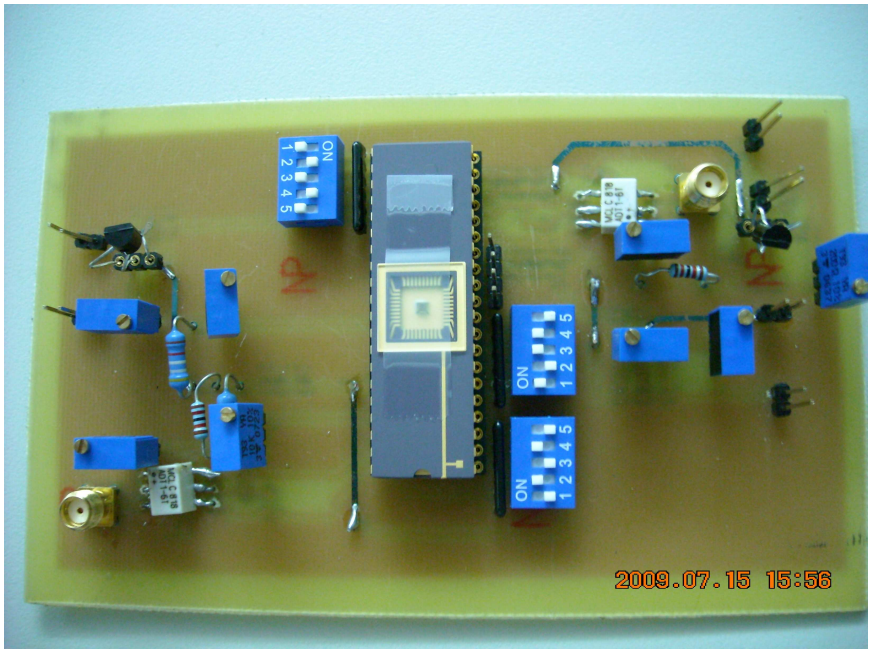
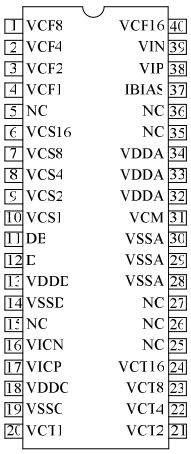


Fig. 8.8 PCB of the CT modulator



Pin	Name	I/O	Description	Pin	Name	I/O	Description
1	VCF8	In	8C control signal in 1st stage	21	VCT2	In	2C control signal in 3rd stage
2	VCF4	In	4C control signal in 1st stage	22	VCT4	In	4C control signal in 3rd stage
3	VCF2	In	2C control signal in 1st stage	23	VCT8	In	8C control signal in 3rd stage
4	VCF1	In	1C control signal in 1st stage	24	VCT16	In	16C control signal in 3rd stage
5	NC	-	No connection	25	NC	-	No connection
6	VCS16	In	16C control signal in 2nd stage	26	NC	-	No connection
7	VCS8	In	8C control signal in 2nd stage	27	NC	-	No connection
8	VCS4	In	4C control signal in 2nd stage	28	VSSA	In	Analog ground
9	VCS2	In	2C control signal in 2nd stage	29	VSSA	In	Analog ground
10	VCS1	In	1C control signal in 2nd stage	30	VSSA	In	Analog ground
11	DB	Out	Digital output signal (180°)	31	VCM	In	Common-mode voltage
12	D	Out	Digital output signal (0°)	32	VDDA	In	Analog power supply
13	VDDD	In	Digital power supply	33	VDDA	In	Analog power supply
14	VSSD	In	Digital ground	34	VDDA	In	Analog power supply
15	NC	-	No connection	35	NC	-	No connection
16	VICN	In	Clock input signal (180°)	36	NC	-	No connection
17	VICP	In	Clock input signal (0°)	37	IBIAS	In	Bias current control
18	VDDC	In	Clock power supply	38	VIP	In	Input signal (0°)
19	VSSC	In	Clock ground	39	VIN	In	Input signal (180°)
20	VCT1	In	1C control signal in 3rd stage	40	VCF16	In	16C control signal in 1st stage

(a) (b)

Fig. 8.9 (a) Pin configurations (b) Pin assignments of the CT modulator

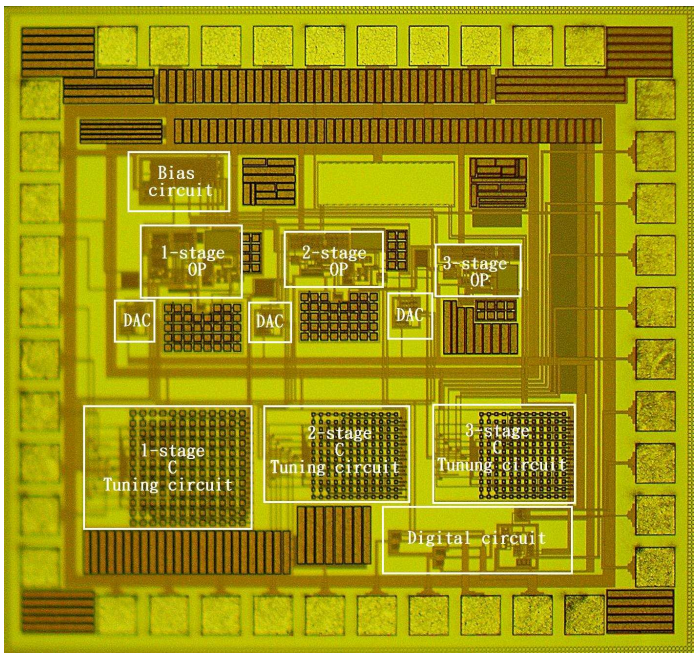


Fig. 8.10 The die photo of the CT SDM

8.4 Measurement Results

The continuous-time single-bit active-RC sigma-delta modulator for 1 MHz bandwidth has been fabricated by TSMC 0.18μm CMOS mixed-signal process. It is supplied by the 1.8V output of the regulator. The input sine wave is 0.798MHz and the sampling frequency is 100MHz. The signal bandwidth is 1MHz and the oversampling ratio is equal to 50. The output data of the modulator are saved through the logic analyzer. By using Matlab in a PC to do fast Fourier transformation with 65536 points, the power spectral density can be obtained as shown in Fig. 8.11. The SNDR is about 53.8dB for -7 dBFS input and the ENOB is 8.64bits. Fig. 8.12 is the post-simulation power spectral density and the SNDR is 65.5dB. Fig. 8.13 shows the dynamic range plot which is the SNDR versus the normalized input level. The measured power consumption is 10.2mW at 1.8V supply voltage.

The performance of this CT modulator is summarized in Table 6.1.

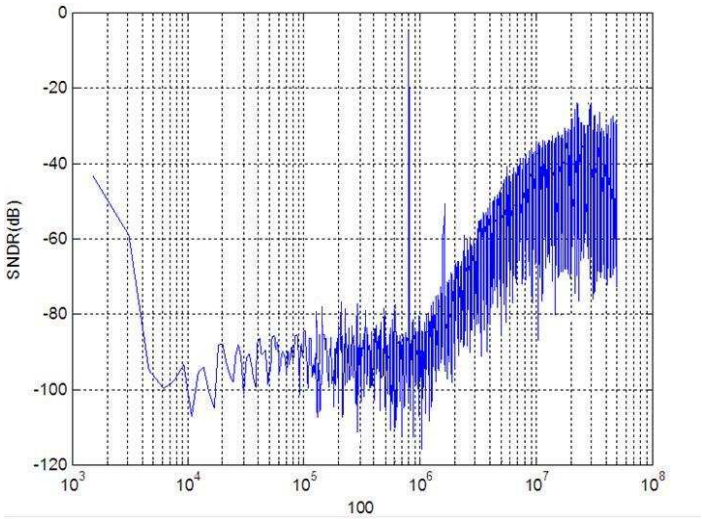


Fig. 8.11 Measured power spectral density of the CT modulator

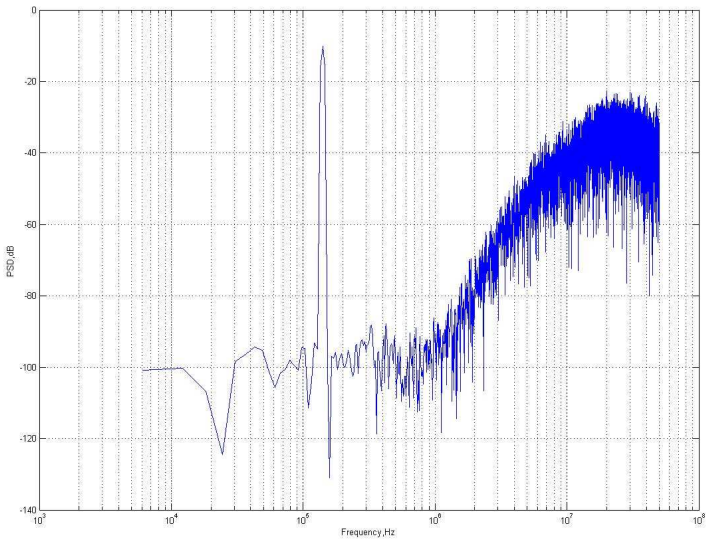


Fig. 8.12 Post-simulation power spectral density of the CT modulator

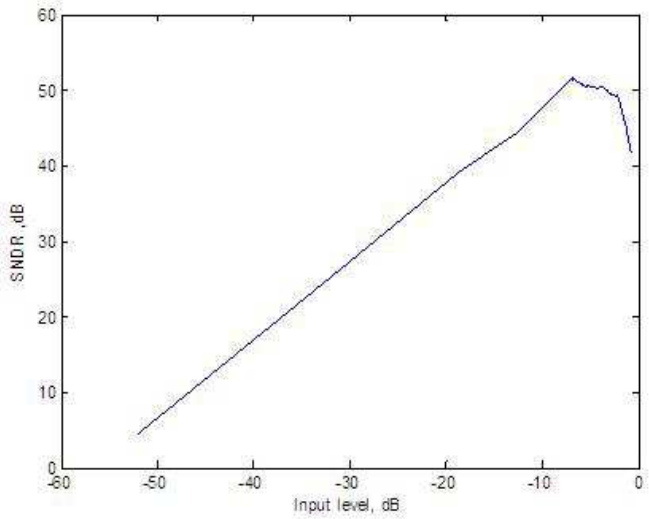


Fig. 8.13 Dynamic range plot of the CT modualtor

Table 8.1 Measurement results of the CT modulator

Parameters	Measurement Results
Technology	TSMC 0.18μm process
Power Supply	1.8V
Sampling Frequency	100MHz
Signal Bandwidth	1MHz
SNDR	53.8dB
ENOB	8.64bits
Dynamic Range	56dB
Area	1.074mm x 1.122mm
Power Consumption	10.2mW

8.5 Summary

In the CT modulator, the SNDR performance between the measurement result and post-simulation has about 10dB decay. The possible reason is that the signal isolation is not good enough. When the high frequency clock function generator is attached to the PCB, the power supply and reference voltage of the analog and digital parts suffers the influence to vibrate slightly. For the solution, it perhaps decreases the path from the BNC to chip and increases the distance from BNC to others in order to reduce the effect. Table 8.2 lists the comparison between previously reported DT SDM and the CT modulator. The FOM is described as follows

$$FOM = \frac{Power}{2 \cdot BW \cdot 2^{(SNDR-1.76)/6.02)}} \qquad (8.2)$$

Table 8.2 Comparison between DT SDM and the CT modulator

Reference	Architecture	SNDR (dB)	BW (MHz)	F_s (MHz)	Process	Power (mW)	FOM (pJ/conv.)
[25]	2-2 MASH	72	1.1	52.5	0.35μm	187	26.26
[25]	2-2-2 MASH	79	1.1	52.5	0.35μm	248	15.48
[26]	3rd-order	56.8	1	100	0.18μm	22.2	19.7
This work Post-simulation	3rd-order	53.8	1	100	0.18μm	10.2	12.7

CHAPTER 9
Conclusions and Future Works

9.1 Conclusions

The continuous-time third-order single-bit sigma-delta modulator for 1 MHz bandwidth has been implemented. The CT modulator utilizes CRFB architecture to improve signal bandwidth and we use active-RC integrators in order to have better linearity. However, the active-RC integrators need an additional output buffer to avoid loading effect which increases the power consumption. For reducing the influence of the clock jitter, the feedback DAC shape is realized by NRZ.

The chip has been fabricated by TSMC 0.18μm CMOS mixed-signal process. The sampling frequency is 100MHz and the signal bandwidth is 1MHz. the CT modulator achieves 53.8dB SDNR performance and 56dB dynamic range for Bluetooth application. The measured power consumption is about 10.2mW at 1.8V supply.

A column driver using a switch capacitor DAC has been implemented. LCD column drivers have traditionally used non-linear R-string style digital-to-analog converters (DAC). But R-string DAC has some problem, so we describe an new architecture for LCD column drivers. It uses linear charge redistribution DAC to implement LCD column driver. DAC performs its conversion in less than 15μs and draws less than 5μA. Although we don't finish whole LCD column driver or tapout chip, we use Hspice to simulation and verify the set of DACs can work correct and linearity.

9.2 Future Works

For the design of the sigma-delta modulator, the dynamic range mainly depends on three factors: oversampling ratio, the order of the modulator and quantizer resolution. For wideband communication system applications, it is impossible to enhance the dynamic range by increasing the oversampling ratio. On the contrary, the others can be increased to achieve the objective.

For the design of the LCD column driver, the amplifier in the DAC is very sensitive about resistance's variation. Because the amplifier has a three resistance under everyone path, if one resistance has some change, the system will become unstable. Another disadvantage is complex miller compensation function. So we find one new amplifier to solve this problem [24]. It has no resistance and it has high gain. Most of all, its bias circuit is more simple.

Bibliography

[1] R. Feldman, B. Boser, and P. R. Gray, "A 13-bit, 1.4-MS/s sigma-delta modulator for RF baseband channel applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1462-1469, Oct. 1998.

[2] J. Grilo, I. Galton, K. Wang, and R. G., Montemayor, "A 12-mW ADC delta-sigma modulator with 80 dB of dynamic range integrated in a single-chip Bluetooth transceiver, " *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp.271-278, Mar. 2002.

[3] J. H. Nielsen and E. Bruun, "A Design Methodology for Power-Efficient Continuous-Time A/D Converters," *Proc. ISCAS. 2003*, vol. 1, pp. 1069-1072, May 2003.

[4] L. J. Breems, "A Cascaded Continuous-Time ΔΣ Modulator with 67dB Dynamic Range in 10MHz Bandwidth," *ISSCC Dig. Tech. Papers*, pp. 72-73, Feb. 2004.

[5] M.J. Bell. "An LCD Column Driver Using a Switch Capacitor DAC," IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2756-2765, Dec. 2005.

[6] E. Boser, and B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

[7] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion, Fundamentals, Performance Limits and Robust Implementations*, Springer Berlin Heidelberg 2006

[8] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, Piscataway NJ: IEEE Press, 2005.

[9] S. R. Norsworthy, R. Schreier and G. C. Temes, *Delta-Sigma Data Converters, Theory, Design, and Simulation*, New York: IEEE Press, 1997.

[10]A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc., 1997.

[11]A. M. Thurston, T. H. Pearce, and M. J. Hawksford, "Bandpass implementation of the sigma delta A-D conversion technique," *Int. Conf. on A-D and D-A Conversion*, pp. 81-86, 1991.

[12]J. A. Cherry and W. M. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulator," IEEE Trans. Circuits & System II, vol. 46, pp. 376-389, Apr. 1999.

[13]Z. Li, "Design of a 14-bit Continuous-Time Delta-Sigma A/D Modulator with 2.5MHz Signal Bandwidth," Ph.D. Thesis, Oregon State University, Corvallis, Oregon, Jan. 2006.

[14]S. Yan and E. Sanchez-Sinencio, "A Continuous-Time Sigma-Delta Modulator with 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," IEEE J. Solid-State Circuits, vol. 39, no. 1, pp. 75-86, Jan. 2004

[15]B. Razavi, 1999, *ISSCC Short Course*.

[16]K. Falakshahi, C.-K. K. Yang, and B. A. Wooley, "A 14-bit, 10-Msamples/sec digital-to-analog converter using multi-bit sigma-delta modulation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 607-615, May. 1999.

[17]T. Tsukada, Liquid-Crystal Displays Addressed by Thin-Film Transistors, Gordon and Breach Publishers, 1996.

[18]E. Lueder, Liquid Crystal Displays Addressing Schemes and Electro-Optical Effects, John Wiley and Sons, Inc., 1996.

[19]L. W. MacDonald and A. C. Lowe, Display Systems Design and Applications, John Wiley and Sons, Inc., 1997.

[20]R. JACOB BAKER, “CMOS (CIRCUIT DESIGN,LAYOUT,AND SIMULATION),” NJ:IEEE Press,2005.

[21]Behzad Razavi, “Principles of Data Conversion System Design.” NJ:IEEE Press,1995.

[22]Mikael Gustavsson,J Jacob Wikner and Nianziong Nick Tan, “CMOS Data Converters for communications,” Kluwer Academic Publishers, Boston,2000.

[23]STMicroelectronics, LM217, LM317, Low Current, 1.2V to 37V Adjustable Voltage Regulator, STMicroelectronics, 2005.

[24]Di Fazio, S.; Pulvirenti, F.; Signorelli, T.; Lao, C.; Pennisi, S. “Low quiescent current high speed amplifier for LCD column driver,” Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on 27-30 Aug. 2007 Page(s):523 - 526.

[25]J. Morizio, et al., “14-bit 2.2-MS/s Sigma-Delta ADC’s,” *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 968-76, Jul. 2000.

[26]Wen-Lin Yang, Chung-Chih Hung, "A Third-Order Continuous-Time Single-Bit Active-RC," VLSI-DAT, 2009