國 立 交 通 大 學

電信工程學系

碩 士 論 文

並聯 *RC* 回授與變壓器雜訊抵消之

超寬頻低雜訊放大器設計

Parallel-*RC* Feedback and Transformer Noise-Canceling Low Noise Amplifiers for UWB Application

研 究 生：何廣琪

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中 華 民 國 九 十 八 年 七 月

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A Thesis

Submitted to Department of Communication Engineering
College of Electrical Engineering and Computer Science
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master
in

Communication Engineering

July 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年七月

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摘要

本論文提出了一個利用並聯RC回授與一個利用變壓器達成雜訊抵消的超寬頻低雜訊放大器設計。我們所提出的電路使用TSMC 0.18-μm CMOS 製程技術製作完成。

第一個電路我們使用RC並聯回授和一個源極電感來達成寬頻阻抗匹配並有效的降低雜訊。再利用並聯LC網路更進一步的壓制高頻雜訊達成很低的雜訊水平。量測結果為最低的雜訊指數為2.5 dB。在3.1-10.6 GHz的功率增益為10.9-13.9 dB。在3.1-15 GHz的輸入返回損耗為-9.4至-32.4 dB。在1.4V偏壓下的消耗功率為14.4 mW，整體面積為0.46 mm^2。

第二個電路我們使用一個變壓器輸入級達成寬頻的雜訊抵消與輸入阻抗匹配，並只需要小的晶片面積與低的消耗功率。量測結果為最低的雜訊指數為3.8 dB。在3.1-10.6 GHz內的功率增益大於10.2 dB。在3.1-13 GHz內的輸入返回損耗低於-10.1 dB。在1.2V偏壓下的消耗功率為9.7 mW，整體面積為0.47 mm^2。

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Abstract

In this thesis, a parallel-*RC* feedback and a transformer noise-canceling low noise amplifier for ultra-wide-band applications are presented. These propose circuits are implemented by the TSMC 0.18-μm CMOS process.

In our first design, the parallel-*RC* shunt feedback with a source inductance is proposed to obtain the broadband input matching and to reduce noise level effectively. The parallel-*LC* network at drain is drawn to further suppress the high-frequency noise and a low noise level is achieved. Measured results show that minimum noise figure is 2.5 dB. The power gain is 10.9-13.9 dB from 3.1 to 10.6 GHz. The input return loss is below －9.4 dB from 3.1 to 15 GHz. It consumes 14.4 mW from 1.4 V supply voltage and occupies an area of only 0.46 mm^2.

In our second design, a transformer input stage is proposed to achieve broadband noise cancellation and input matching with small chip area and low power consumption. Measured results show that minimum noise figure is 3.8 dB. The power

gain is more than 10.2 dB from 0.7 to 11.5 GHz. The input return loss is below −10.1 dB from 3.1 to 13 GHz. It consumes 9.7 mW from 1.2 V supply voltage and occupies an area of only 0.47 mm^2.

誌　　謝

在新竹交通大學碩士班的這二年歲月裡，誠心的感謝我的指導教授 唐震寰老師提供我一流的實驗室學習環境與專業上的指導。讓我對於射頻電路能夠有著非常多的進步與了解。雖然新竹的食物有些並不怎美味，但是交通大學還是一個非常好的地方，在學習鑽研知識上是一個很讓人讚賞的地方。

在這滿滿回憶的兩年生活裡，感謝梁小姐每天幫我們處理那麼多事情，真的很辛苦。感謝 810 實驗室的博班學長標哥與佩宗平時幫我們解決那麼多問題與教導我們。感謝學長雅仲、焯基哥與俊彥哥一起度過了愉快的一年。感謝學弟冠豪、國政、鉦淀與耿賢的陪伴。感謝共同在一起兩年同樂同患難的夥伴明宗、政銘與兆凱。

在這兩年的求學生涯裡，感謝我的家人一直陪伴著我與鼓勵著我，讓我有著一個避風港，很累時可以回家休息充電。在交大讀書的這兩年裡，充滿著許多的回憶，遇見了很多人，祝大家都能很快樂幸福，完成自己的夢想。

何廣琪　誌予

九十八年七月

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Chapter 1 *Introduction*

1.1 Related Works and Motivation

In recent years, Ultra-wide-band (UWB) systems have attracted more interest due to their capability of transmitting data with high data rate and low power consumption. For IEEE 802.15.3a standard, the allocated band of UWB is between 3.1-10.6 GHz. The wide-band low noise amplifier (LNA) for wireless front-end radio frequency receiver is a critical block. Since the LNA is the first gain stage in the receive path, its noise figure directly adds to that of the system. Thus the LNA needs to fulfill several requirements, such as broadband input matching, sufficient power gain, and low noise figure, etc.

Recently, CMOS technology has suddenly become the topic of active research because of its low cost, low power, and high integration. Several major types of UWB CMOS LNAs have been reported. However, LNA's performances almost always involve trade-offs. For example, although the distributed amplifier (DA) provides good wideband input matching and flat gain, it consumes more power and chip area. The resistive shunt feedback is a well-known wide band technique, which provides wide band input matching but increases NF due to the local feedback [1]. The inductive degeneration can only provide a narrowband input matching but it can achieve better noise performance [2]. Another technology is to use a multistage input filter for broadband input matching [3]. However, the input filter insertion loss degrades the LNA's NF, and a large chip area is unavoidable.

To solve these problems, a parallel-*RC* feedback and a transformer noise-canceling LNAs are presented for UWB applications. In our first design, the parallel-*RC* shunt feedback with a source inductance is proposed to obtain the broadband input matching and to reduce noise by the local feedback effectively. The parallel-*LC* network at drain is drawn to further suppress the high-frequency noise and a low noise level is achieved. It needs only a small inductor for broadband matching, so chip area can be realized in a small area. In our second design, a transformer input stage is proposed to achieve broadband noise cancellation and input matching. The proposed noise-canceling technique can achieve noise cancellation and signal addition without high-Q inductors, so it can be realized in a small chip area with low power consumption.

1.2 Thesis Organization

The thesis consists of five chapters. Chapter 1 gives a introduction. Chapter 2 describes basic concepts in LNA design, emphasizing the effects of noise and nonlinearity. Chapter 3 discusses a parallel-*RC* feedback UWB LNA with simulation and measured results. In the Chapter 4, a broadband noise-canceling LNA using transformer is introduced. Eventually, all the work is summarized and concluded in Chapter 5.

Chapter 2 *Basics of LNA Design*

2.1 Effects of Nonlinearity

While many RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena. For a nonlinear system, the input-output relationship can be approximated as

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.1}$$

Equation (2.1) can help us to understand some effects of nonlinearity.

2.1.1 Harmonics

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. In (2.1), if x(t)＝Acosωt, then

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \tag{2.2}$$

$$= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \tag{2.3}$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \tag{2.4}$$

In Eq. (2.4), the term with the input frequency is called the “fundamental” and higher-order terms the “harmonics”.

2.1.2 Gain Compression

The small-signal gain of a circuit is usually obtained with the assumption that harmonics are negligible. In fact, nonlinearity can be viewed as variation of the small-signal gain with the input level. As the signal amplitude increases, the gain begins to vary. In most circuits of interest, the output is a "compressive" or "saturating" function of the input; that is, the gain approaches zero for sufficiently high input levels. In (2.14) this occurs if $\alpha_3 < 0$. Written as $\alpha_1+3\alpha_3A^2/4$, the gain is therefore a decreasing function of A. In RF circuits, this effect is quantified by the "1-dB compression point", defined as the input signal level that caused the small-signal gain to drop by 1 dB (Fig. 2.1).

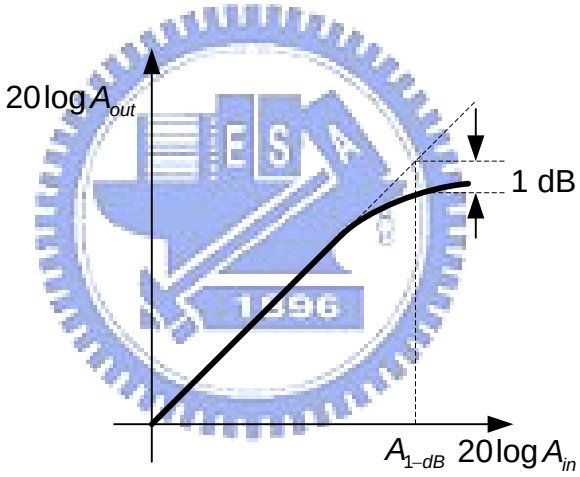


Figure 2.1 Definition of the 1-dB compression point.

2.1.3 Inter-modulation

When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. Called inter-modulation (IM), this phenomenon arises from "mixing" (multiplication) of the two signals when their sum is raised to a power greater than unity. We assume $x(t)=A_1\cos\omega_1 t+A_2\cos\omega_2 t$. Thus,

$$y(t)=\alpha_1(A_1\cos\omega_1 t+A_2\cos\omega_2 t)+\alpha_2(A_1\cos\omega_1 t+A_2\cos\omega_2 t)^2$$

$$+\alpha_3(A_1\cos\omega_1 t+A_2\cos\omega_2 t)^3 \tag{2.5}$$

Expanding the left side and discarding DC terms and harmonics, we obtain the following inter-modulation products:

$$\omega=\omega_1\pm\omega_2:\alpha_2A_1A_2\cos(\omega_1+\omega_2)t+\alpha_2A_1A_2\cos(\omega_1-\omega_2)t \tag{2.6}$$

$$=2\omega_1\pm\omega_2:\frac{3\alpha_3A_1^2A_2}{4}\cos(2\omega_1+\omega_2)t+\frac{3\alpha_3A_1^2A^2}{4}\cos(2\omega_1-\omega_2)t \tag{2.7}$$

$$=2\omega_2\pm\omega_1:\frac{3\alpha_3A_2^2A_1}{4}\cos(2\omega_2+\omega_1)t+\frac{3\alpha_3A_2^2A_1}{4}\cos(2\omega_2-\omega_1)t \tag{2.8}$$

and these fundamental components

$$\omega=\omega_1,\omega_2:\left(\alpha_1A_1+\frac{3}{4}\alpha_3A_1^3+\frac{3}{2}\alpha_3A_1A_2^2\right)\cos\omega_1 t+\left(\alpha_1A_2+\frac{3}{4}\alpha_3A_2^3+\frac{3}{2}\alpha_3A_2A_1^2\right)\cos\omega_2 t \tag{2.9}$$

As shown in Fig. 2.2, if a weak signal accompanied by two strong interferers experiences third-order nonlinearity, then one of the IM products falls in the band of interest, corrupting the desired component.

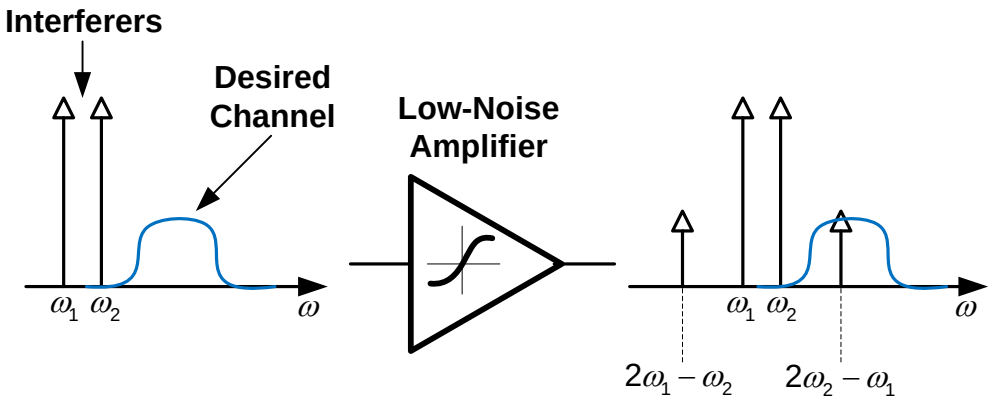


Figure 2.2 Corruption of a signal due to inter-modulation between two interferers.

This phenomenon can be measured by a two-tone test in which A is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant and equal to α_1. From (2.7), (2.8), and (2.9), we note that as A increases, the fundamentals increase in proportion to A, whereas the third-order IM products increase in proportion to A^3. Plotted on a logarithmic scale, the magnitude of the IM products grows at three times the rate at which the main components increase. As shown in Fig. 2.3, the third-order intercept point is defined to be at the intersection of the two lines. The horizontal coordinate of this point is called the input IP_3 (IIP_3), and the vertical coordinate is called the output IP_3 (OIP_3).

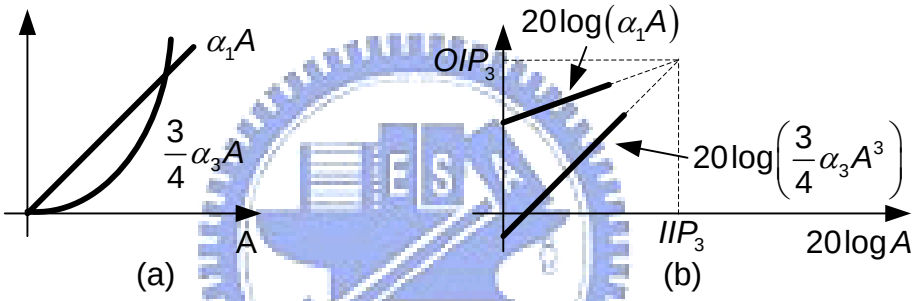


Figure 2.3 The third-order intercept point in a two-tone inter-modulation test.

In Fig. 2.4(a), $\Delta L \times \tan\theta_2 - \Delta L \times \tan\theta_1 = \Delta P$, $\tan\theta_2 = 3\tan\theta_1$, and $\tan\theta_1 = 1$, we can obtain $\Delta L = \Delta P/2$, and

$$20\log A_{IP_3} = \frac{1}{2}\left(20\log A_{\omega_1,\omega_2} - 20\log A_{IM_3}\right) + 20\log A_{in} \tag{2.10}$$

That is, if all the signal levels are expressed in dBm, the IIP3 is equal to half the difference between the magnitudes of the fundamentals and the IM3 products at output plus the corresponding input level.

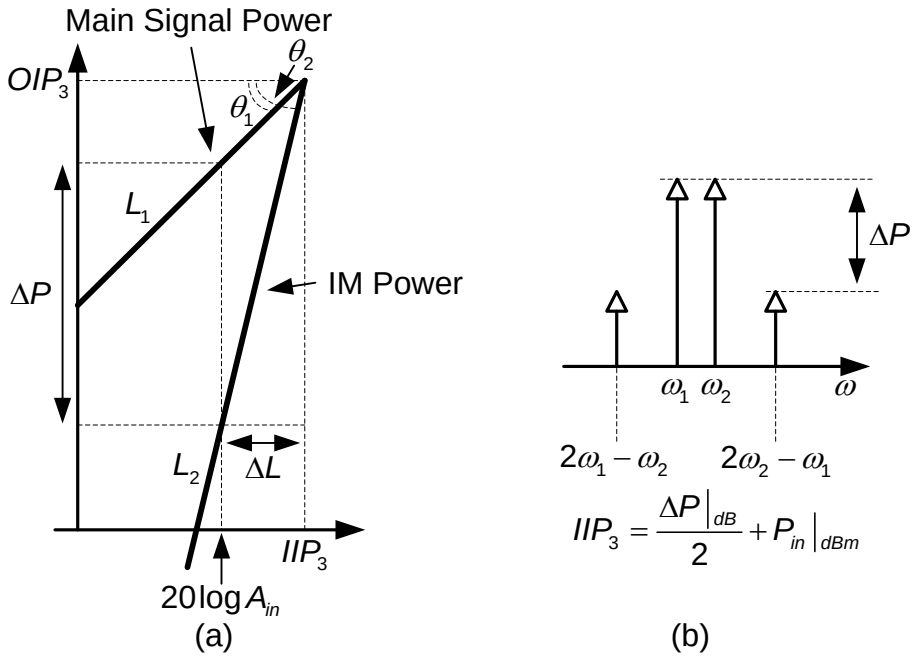


Figure 2.4 (a) Graphical interpretation of IIP_3, (b) calculation of IIP_3 without extrapolation.

2.2 Noise

Noise can be loosely defined as any random interference unrelated to the signal of interest. In this subsection, we will introduce two major noise sources in RF circuit, some definition, and noise analysis technique.

2.2.1 Thermal Noise

Present in all circuits is thermal noise, generated by resistors, base and emitter resistance of bipolar devices, and channel resistance of MOSFETs.

Resistor Thermal Noise The random motion of electrons in a conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. Thus, the spectrum of thermal noise is proportional to the absolute temperature.

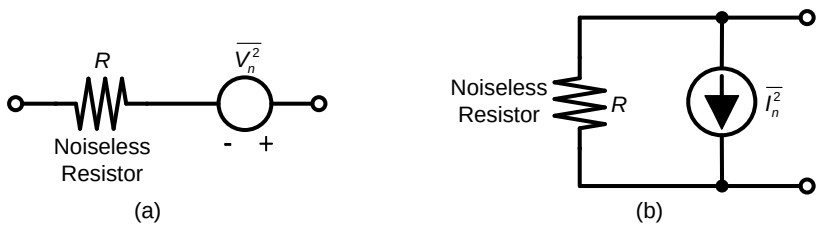


Figure 2.5 Thermal noise of a resistor: (a) equivalent series voltage source, (b) equivalent parallel current source.

As shown in Fig. 2.5, the thermal noise of a resistor R can be modeled by a series voltage source or a parallel current source.

$$\overline{V_n^2} = 4kTR\Delta f \tag{2.11}$$

$$\overline{I_n^2} = 4kT/R\,\Delta f \tag{2.12}$$

Where k＝1.38×10^{-23}J/K is the Boltzmann constant.

MOSFETs MOS transistors also exhibit thermal noise. The most significant source is the noise generated in the channel. The channel noise can be modeled by a current source connected between the drain and source terminals.

$$\overline{I_n^2} = 4kT\gamma g_{d0} \tag{2.13}$$

Where g_{d0} is the drain-source conductance with V_{DS}=0.

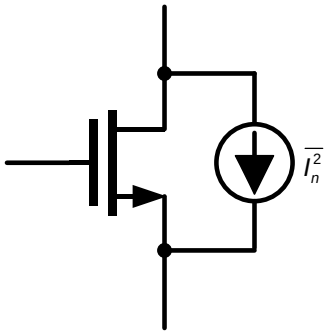


Figure 2.6 Thermal noise of a MOSFET.

2.2.2 Flicker Noise

The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since the silicon crystal reaches an end at this interface, many "dangling" bonds appear, giving rise to extra energy states (Fig. 2.7). As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current. Unlike thermal noise, the average power of flicker noise cannot be predicted easily. However, it can be easily modeled as a voltage source in series with the gate and roughly given by

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.14}$$

where K is a process-dependent constant on the order of $10^{-25}V^2F$. Note that our notation assumes a bandwidth of 1Hz.

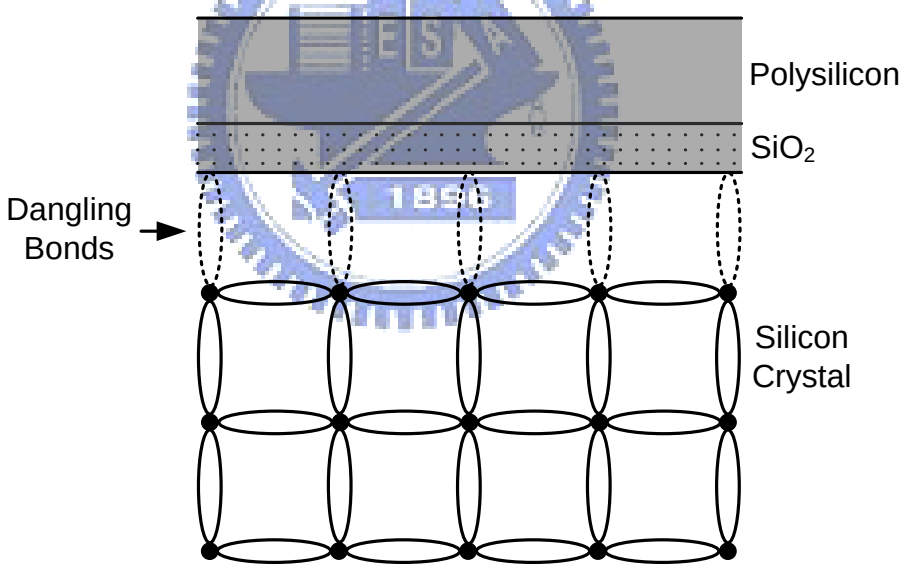


Figure 2.7 Dangling bonds at the oxide-silicon interface.

2.2.3 Input-Referred Noise

As shown in Fig. 2.8, the noise of a two-port system can be modeled by two input noise generators: a series voltage source and a parallel current source. Sometimes, this representation of noise can help us to analyze noise clear.

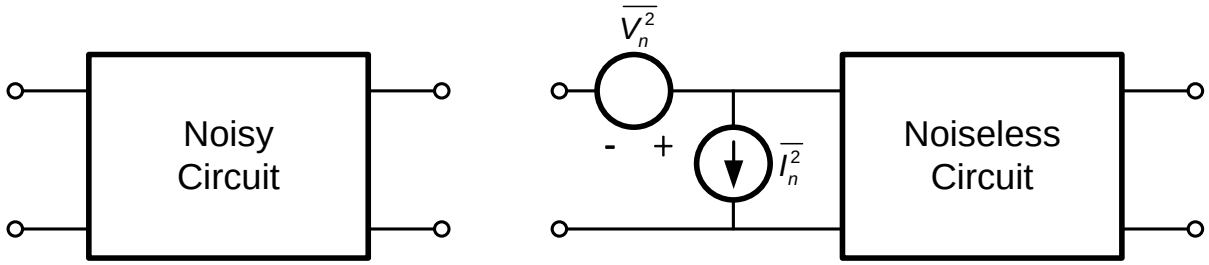


Figure 2.8 Representation of noise by input noise generators.

2.2.4 Noise Figure

In many analog circuits, the signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. In RF design, most of the front-end receiver blocks are characterized in terms of their "noise figure" rather than the input-referred noise. This is partly for computational convenience and partly from tradition.

Noise figure has been defined in a number of different ways. The most commonly accepted definition is

$$noise\ \ figure = \frac{SNR_{in}}{SNR_{out}} \tag{2.15}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output, respectively. Changing the expression slightly, we have

$$NF = \frac{\dfrac{V_{in}^2}{\overline{V_{RS}^2}}}{\dfrac{A_V^2 V_{in}^2}{V_{n,out}^2}}$$

$$= \frac{V_{n,out}^2}{A_V^2 \overline{V_{RS}^2}}$$

$$= \frac{V_{n,out}^2}{A_V^2} \frac{1}{4kTR_S} \tag{2.16}$$

where $V_{n,out}^2$ represents the total noise at the output. Thus, to calculate *NF*, we divide the total

output noise power by the square of the voltage gain from V_{in} to V_{out} and normalize the result to the noise of R_s.

2.2.5 Noise Figure of Cascaded Stages

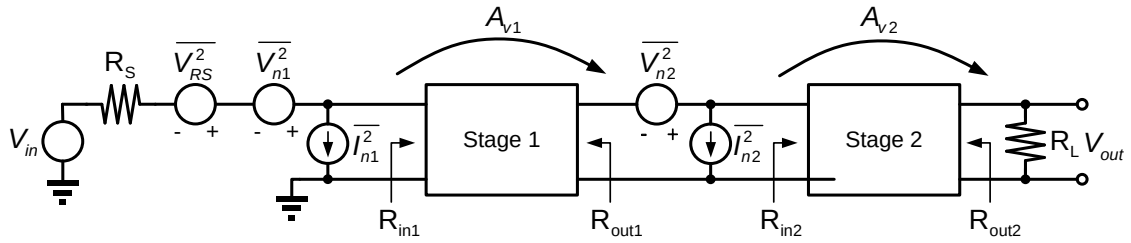


Figure 2.9 Cascaded noisy stages.

For a cascade of stages, the overall noise figure can be obtained in terms of the NF and gain of each stage. Consider the system shown in Fig. 2.9, where NF_1 and NF_2 is the noise figure of the first stage and the second stage, respectively. Note that reactive components of the impedances are nulled and A_{v1} and A_{v2} denote the unloaded voltage gain of two stages. The total noise power at the input of the first stage can be written as

$$V_{n,in1}^2 = \overline{\left[I_{n1}\left(R_S \parallel R_{in1}\right) + V_{n1}\frac{R_{in1}}{R_{in1}+R_S}\right]^2} + \overline{V_{RS}^2}\frac{R_{in1}^2}{\left(R_{in1}+R_S\right)^2} \tag{2.17}$$

The total noise power at the input of the second stage is

$$V_{n,in2}^2 = V_{n,in1}^2 A_{v1}^2\left(\frac{R_{in2}}{R_{out1}+R_{in2}}\right)^2 + \overline{\left[I_{n2}\left(R_{out1} \parallel R_{in2}\right) + V_{n2}\frac{R_{in2}}{R_{in2}+R_{out1}}\right]^2} \tag{2.18}$$

Thus, the total output noise power of the cascade equals

$$V_{n,tot}^2 = V_{n,in2}^2 A_{v2}^2 \frac{R_L^2}{\left(R_L+R_{out2}\right)^2} \tag{2.19}$$

Since the total voltage gain from V_{in} to V_{out} equals

$$A_{v,tot} = \frac{R_{in1}}{R_S + R_{in1}} A_{v1} \frac{R_{in2}}{R_{out1} + R_{in2}} A_{v2} \frac{R_L}{R_{out2} + R_L} \tag{2.20}$$

the overall noise figure is

$$NF_{tot} = \frac{1}{A_{v,tot}^2} A_{v2}^2 \left(\frac{R_L}{R_L + R_{out2}} \right)^2 V_{n,in2}^2 \cdot \frac{1}{4kTR_S} \tag{2.21}$$

Using (2.17) and (2.18) and simplifying the result, we have

$$NF_{tot} = \frac{4kTR_S + \overline{\left(I_{n1}R_S + V_{n1}\right)^2}}{4kTR_S} + \frac{\overline{\left(I_{n2}R_{out1} + V_{n2}\right)^2}}{A_{v1}^2} \frac{1}{\alpha^2} \frac{1}{4kTR_S} \tag{2.22}$$

where α is equal to $\left(\frac{R_{in1}}{R_S + R_{in1}} \right)^2$.

The first term on the right-hand side can be identified as the NF of the first stage with respect to a source impedance R_S. The second term, on the other hand, is not as straightforward. In the special case where $R_S=R_{in1}=R_{out1}=R_{in2}$, we have

$$\begin{aligned} NF_{tot} &= NF_1 + \frac{\overline{\left(I_{n2}R_S + V_{n2}\right)^2}}{\alpha^2 A_{v1}^2} \frac{1}{4kTR_S} \\ &= NF_1 + \frac{NF_2 - 1}{\alpha^2 A_{v1}^2} \end{aligned} \tag{2.23}$$

where NF_2 is the noise figure of the second stage with respect to a source impedance R_S.

In the general case, we simplify (2.23) using the concept of "available power gain," A_p. This type of gain is defined as the available power at the output (the power that the circuit would deliver to a conjugate-matched load) divided by the available source power (the power that the source would deliver to a conjugate-matched circuit.) The available output power of stage 1 in Fig. 2.9 is

$$P_{out,av} = V_{in}^2 \alpha^2 A_{v1}^2 \cdot \frac{1}{4R_{out1}} \tag{2.24}$$

and the available source power is

$$P_{source,av} = \frac{V_{in}^2}{4R_S} \tag{2.25}$$

Thus,

$$A_p = \alpha^2 A_{v1}^2 \frac{R_S}{R_{out1}} \tag{2.26}$$

We can write (2.23) as

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_p} \tag{2.27}$$

Similarly, for m stages,

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}} \tag{2.28}$$

where the NF of each stage is calculated with respect to the source impedance driving that stage. This is called the Friis equation [4]. The Friis equation indicates that the noise contributed by each stage decreases as the gain preceding the stage increases, implying that the first few stages in a cascade are the most critical.

2.3 Sensitivity and Dynamic Range

2.3.1 Sensitivity

The sensitivity of an RF receiver is defined as the minimum signal level that the system can detect with acceptable signal-to-noise ratio. To calculate the sensitivity, we write

$$NF = \frac{SNR_{in}}{SNR_{out}}$$

$$= \frac{P_{sig} / P_{RS}}{SNR_{out}} \tag{2.29}$$

where P_{sig} denotes the input signal power and P_{RS} the source resistance noise power, both per unit bandwidth. Since the overall signal power is distributed across the channel bandwidth, B, the (2.29) must be integrated over the bandwidth to obtain the total mean square power. Thus,

for a flat channel,

$$P_{sig,tot} = P_{RS} \cdot NF \cdot SNR_{out} \cdot B \tag{2.30}$$

Assuming conjugate matching at the input, we obtain P_{RS} as the noise power that R_S delivers to the receiver:

$$\begin{aligned} P_{RS} &= \frac{4kTR_S}{4}\frac{1}{R_{in}} \\ &= kT \\ &= -174 dBm/Hz \end{aligned} \tag{2.31}$$

at room temperature. Expressing the quantities in dB or dBm, we thus simplify (2.30) as

$$P_{in.\min} = -174 dBm/Hz + NF\big|_{dB} + 10\log B + SNR_{\min}\big|_{dB} \tag{2.32}$$

Note that the sum of the first three terms is the total integrated noise of the system and is sometimes called the "noise floor".

2.3.2 Spurious-Free Dynamic range (SFDR)

Dynamic range (DR) is generally defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit provides a reasonable signal quality. This definition is quantified in different applications differently. In RF design, on the other hand, the situation is more complicated. We base the definition of the upper end of the dynamic range on the inter-modulation behavior and the lower end on the sensitivity. Such a definition is called the "spurious-free dynamic range" (SFDR).

The upper end of the dynamic range is defined as the maximum input level in a two-tone test for which the third-order IM products do not exceed the noise floor. Expressing all of the quantities in dBm, we can rewrite (2.10) as

$$P_{IIP3} = P_{in} + \frac{P_{out} - P_{IM,out}}{2} \tag{2.33}$$

where $P_{IM,out}$ denotes the power of IM_3 components at the output. Since $P_{out}=P_{in}+G$ and $P_{IM,out}=P_{IM,in}+G$, where G is the circuit's power gain in dB and $P_{IM,in}$ is the input-referred level

of the IM_3 products, we have

$$P_{IIP_3} = P_{in} + \frac{P_{in} - P_{IM,in}}{2}$$
$$= \frac{3P_{in} - P_{IM,in}}{2} \tag{2.34}$$

and hence

$$P_{in} = \frac{2P_{IIP_3} + P_{IM,in}}{3} \tag{2.35}$$

The input level for which IM products become equal to the noise floor is thus given by

$$P_{in,\max} = \frac{2P_{IP_3} + F}{3} \tag{2.36}$$

where F = -174dBm+NF+10log B.

The SFDR is the difference (in dB) between $P_{in,max}$ and $P_{in,min}$:

$$SFDR = \frac{2P_{IIP_3} + F}{3} - \left(F + SNR_{\min}\right)$$
$$= \frac{2\left(P_{IIP_3} - F\right)}{3} - SNR_{\min} \tag{2.37}$$

The SFDR represents the maximum relative level of interferers that a receiver can tolerate while producing an acceptable signal quality from a small input level.

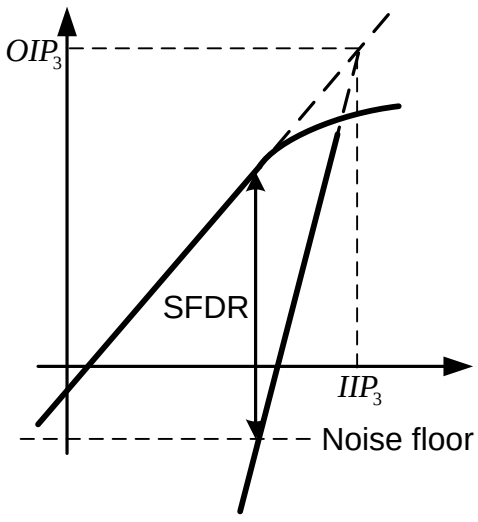


Figure 2.10 Spurious-free dynamic range.

2.4 Topologies Low Noise Amplifiers

In RF circuit design, the input and output matching is an important parameters, which indicate that how many power is reflected. When the amplifier of our design is the first gain stage in the receive path, not only impedance matching but also noise figure is significant consideration, since its noise figure directly adds to that of the system. In this subsection, we will introduce six input matching architectures.

2.4.1 Input Matching

A. Resistive termination

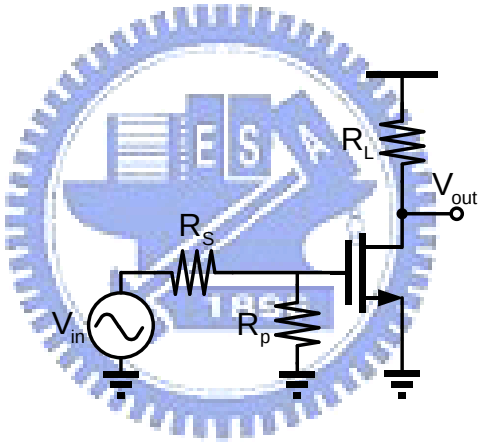


Figure 2.11 Common-source amplifier with shunt input resistor.

One straightforward approach to providing a reasonably broadband 50 Ohm termination is simply to put a 50 Ohm resistor across the input terminals of a common-source amplifier. In Fig. 2.11, a 50 Ohm resistor is placed in parallel with the input, and the capacitive part of input impedance is canceled by an external inductor.

The termination resistor, however, generates noise as well. In fact, the noise figure of a stage consisting of a parallel resistor R_p with respect to a source resistance R_S is

$$NF = 1 + \frac{R_S}{R_p} + \frac{\gamma}{\alpha}\frac{4}{g_m R_S} \tag{2.38}$$

where $\alpha=g_m/g_{d0}$.

Unfortunately, the resistor R_p adds thermal noise of its own, and attenuates the signal ahead of the transistor. The combination of these two effects generally produces unacceptably high noise figure. For $R_p=R_S$, the noise figure of the LNA exceeds 3dB. The key point here is that the circuit must exhibit a 50 Ohm input resistance without the thermal noise of a 50 Ohm resistor.

B. Resistive shunt feedback

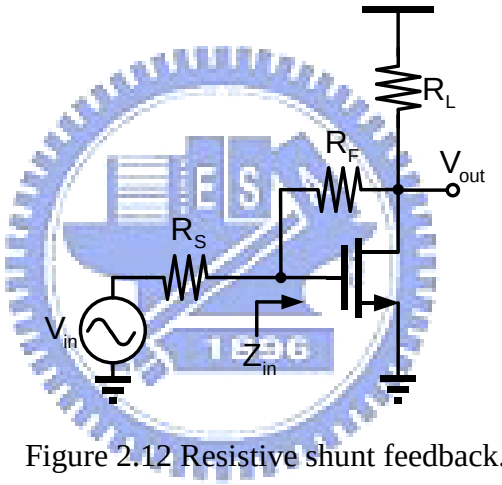


Figure 2.12 Resistive shunt feedback.

The circuit topology of a resistive shunt feedback LNA is shown in Fig. 2.12, which can provide a broadband input matching. The input impedance can be derived as

$$Z_{in}=\frac{R_F+R_{L1}}{1+g_{m1}R_{L1}} \tag{2.39}$$

The resistive feedback network continues to generate thermal noise of its own. The noise figure can be derived as

$$NF=1+\frac{1}{R_S}\left(\frac{1+g_{m1}R_S}{\frac{1}{\sqrt{R_F}}-g_{m1}\sqrt{R_F}}\right)^2+\frac{1}{R_SR_{L1}}\left(\frac{1+\frac{R_S}{R_F}}{\frac{1}{R_F}-g_{m1}}\right)^2+\frac{\gamma g_{m1}}{\alpha R_S}\left(\frac{1+\frac{R_S}{R_F}}{\frac{1}{R_F}-g_{m1}}\right)^2 \tag{2.40}$$

As a consequence, this topology typically requires larger power consumption or more advanced technologies to achieve an acceptable NF. This is primarily due to the inherently low transconductance of CMOS, which not only degrades the noise performance but also prohibits the use of a large feedback resistor.

C. Common Gate

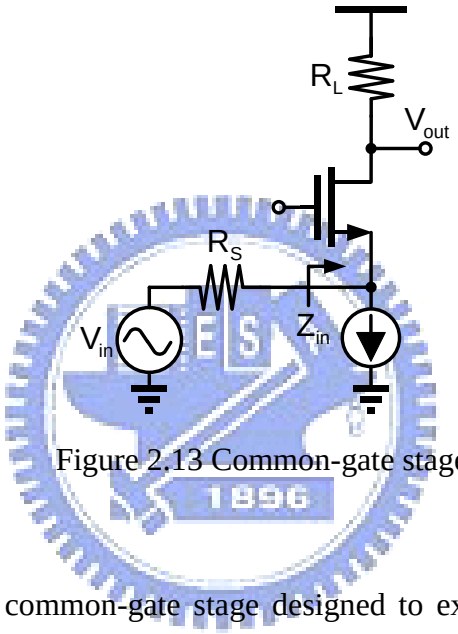


Figure 2.13 Common-gate stage.

Figure 2.13 depicts a common-gate stage designed to exhibit an input resistance of 50 Ohm; that is, $1/(g_m+g_{mb})$=50 Ohm. The input capacitance may be nulled by means of an external inductor. With the input impedance matched to 50 Ohm, its noise figure NF is derived as

$$NF = 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_{L1}} \tag{2.41}$$

The principal drawback of this topology is that the transconductance of the input transistor cannot be arbitrarily high, thus imposing a lower bound on the noise figure. The noise figure will be significantly worse at high frequencies and when gate current noise is taken into account.

D. Inductive degeneration

Another topology of creating an input resistance of 50 Ohm is illustrated in Fig. 2.14. Neglecting the gate-drain and source-bulk capacitance, we can write

$$Z_{in} = \frac{g_m L_S}{C_{gs}} + s\left(L_S + L_g\right) + \frac{1}{sC_{gs}} \tag{2.42}$$

The inductance L_S is chosen to provide the desired input resistance (equal to R_S, the source resistance). Since the input impedance is purely resistive only at resonance, an additional degree of freedom, provided by inductance L_g, is needed to guarantee this condition. An important advantage of this method is that one then has control over the value of the real part of impedance through choice of inductance. Whatever the value of this resistive term, it is important to emphasize that it does not bring with it the thermal noise of an ordinary resistor because a pure reactance is noiseless. We may therefore exploit this property to provide a specified input impedance without degrading the noise performance of the amplifier.

The principal drawback of this topology is that the input impedance is purely resistive at only one frequency (at resonance), however, so this method can only provide a narrowband impedance match.

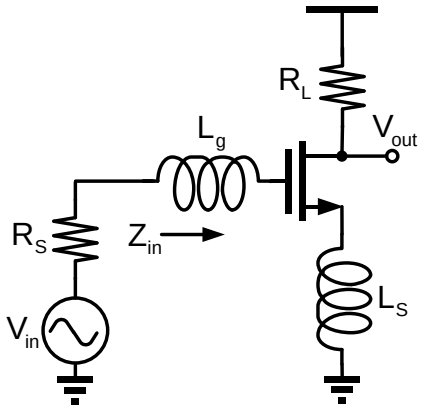


Figure 2.14 Resistive termination by Inductive degeneration.

E. Multistage input filter

As shown in Fig. 2.15, this topology is to use a multistage input filter for broadband input matching. Although this filter-type topology achieves broadband matching and low power consumption, the input filter insertion loss degrades the amplifier's noise performance, and this loss must be compensated for by increasing the gain, thereby lowering bandwidth. In addition, this topology requires a large number of high-Q inductors at the input, making it difficult to realize them in a small chip area.

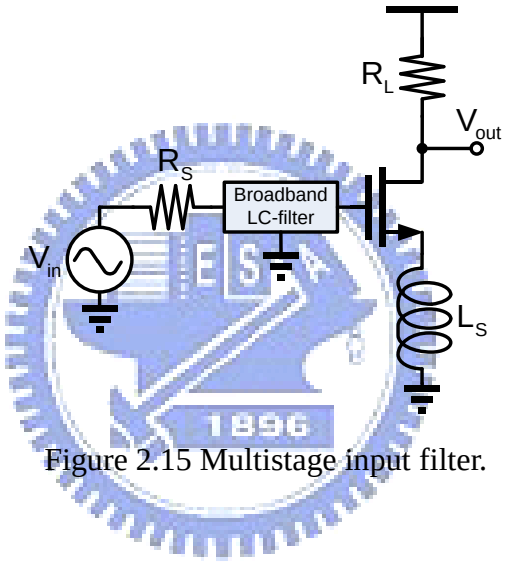


Figure 2.15 Multistage input filter.

F. Distributed amplifier

The basic distributed amplifier is shown in Fig. 2.16. The input impedance matching is achieved by designing the characteristic impedance of transmission line, $Z_o = \sqrt{L_g / C_g}$, equal to the source impedance, R_S, usually 50 Ohm. To avoid unwanted reflection from the transmission line, the gate-termination resistor, R_g is also set equal to the characteristic impedance, Z_o.

The distributed amplifier provides good impedance matching and flat gain over a wide range of frequencies. However, the demand for high-quality transmission lines makes them

less attractive to low-cost applications because of the larger chip area and higher power consumption.

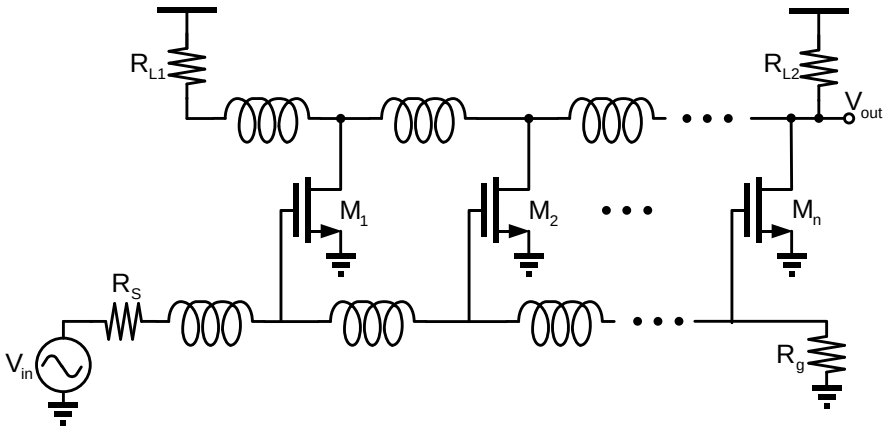


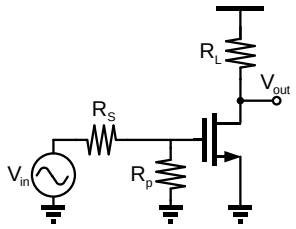
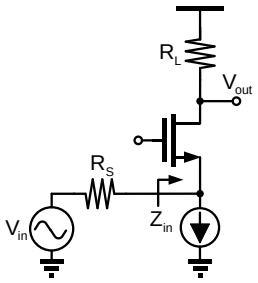
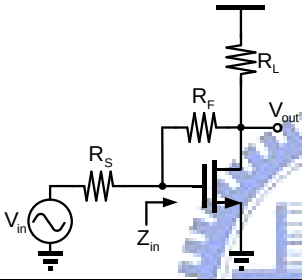
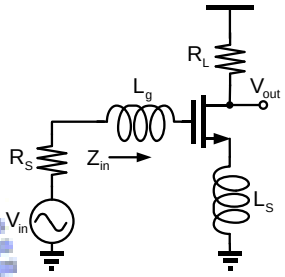
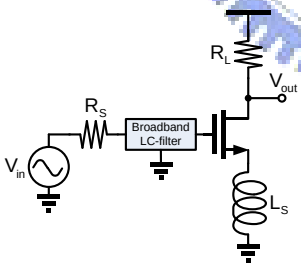
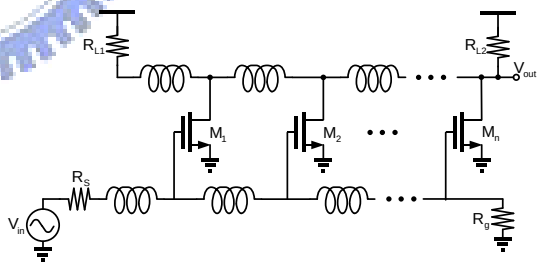
Figure 2.16 Basic distributed amplifier.

2.4.2 Summary

The summary of six input matching architectures is listed in Table I. The resistive termination provides good input matching but the resistor increases noise figure. The resistive shunt feedback provides wide band input matching but increases noise figure due to the local feedback resistor. The common-gate stage also provides wide band input matching. However, lower bound on the noise figure is restricted by lower transconductance. The inductive degeneration can only provide a narrowband input matching but it can achieve better noise performance. The multistage input filter topology provides broadband matching and low power consumption but insertion loss degrades the noise performance. Finally, the distributed amplifier provides good wideband input matching and flat gain. However, it consumes more power and chip area.

Table I

Six input matching architectures summary

	
(a) Resistive termination. Resistor degrade the noise figure.	(b) Common-gate stage. Lower bound on noise figure.
	
(c) Resistive shunt feedback Broadband but higher power consumption.	(d) Inductive degeneration Narrow band but can achieve better noise performance.
	
(e) Multistage input filter Broadband but insertion loss degrade noise performance with large chip area.	(f) Distributed amplifier Broadband and flat gain but large chip area with high power consumption.

2.5 Bandwidth Techniques

The bandwidth enhancement is achieved by shunt peaking, a method first used in the 1940's to extend the bandwidth of television tubes. We first describe the fundamentals of this approach. Then we will introduce a triple-resonance architecture.

2.5.1 Shunt Peaking

Although inductors are commonly associated with narrow-band circuits, they are useful in broadband circuits as well. In this section, we study how an inductor can enhance the bandwidth of a broadband amplifier [5].

We consider the simple common source amplifier illustrated in Fig. 2.17. For simplicity, we assume that the small signal frequency response of this amplifier is determined by a single dominant pole, which is determined solely by the output load resistance R and the load capacitance C [see Fig. 2.17(b)].

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R}{1 + j\omega RC} \tag{2.43}$$

The introduction of an inductance L in series with the load resistance alters the frequency response of the amplifier [Fig. 2.17(c)]. This technique, called shunt peaking, enhances the bandwidth of the amplifier by transforming the frequency response from that of a single pole to one with two poles and a zero [Fig. 2.17(d)].

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m (R + j\omega L)}{1 + j\omega RC - \omega^2 LC} \tag{2.44}$$

The zero is determined solely by the L/R time constant and is primarily responsible for the bandwidth enhancement. The frequency response of this shunt peaked amplifier is characterized by the ratio of the L/R and RC time constants. This ratio is denoted by m so that $L=mR^2C$.

Fig. 2.18 illustrates the frequency response of the shunt-peaked amplifier for three cases.

The case with no shunt peaking is used as the reference so that its low-frequency gain and its 3-dB bandwidth are equal to one.

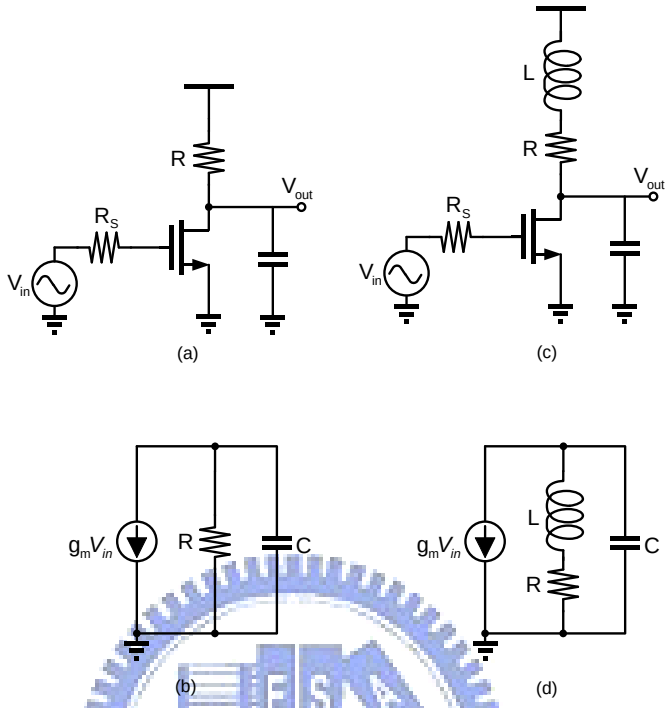


Figure 2.17 Shunt peaking a common source amplifier. (a) Simple common source amplifier and (b) its equivalent small signal model. (c) Common source amplifier with shunt peaking and (d) its equivalent small signal model.

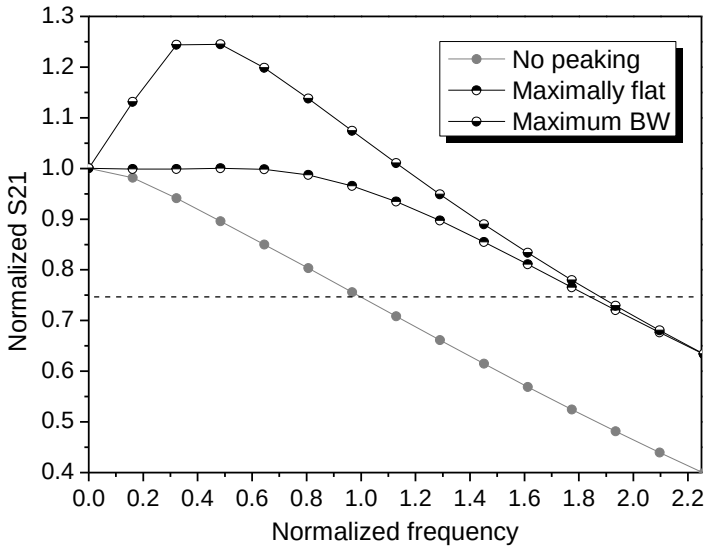


Figure 2.18 Frequency response of shunt-peaking amplifier for three cases.

2.5.2 Triple-Resonance Architecture

To arrive at the concept of the triple-resonance amplifier (TRA) [6], first consider the inductively peaked cascade of two stages shown in Fig. 2.19(a), where it is assumed that M_1 and M_2 contribute approximately equal capacitance (C/2) to node X. As the frequency approaches

$$\omega_1 = \frac{1}{\sqrt{L_1 C}} \tag{2.45}$$

the impedance of L_1 rises, allowing a greater fraction of I_{D1} to flow through C_1+C_2 and hence extend the bandwidth.

To increase the bandwidth, we insert an inductor L_2 in series with C_2 [Fig. 2.19(b)] such that L_2 and C_2 resonate at ω_1, thereby acting as a short and absorbing all of I_{D1}. Now, I_{D1} flows through C_2 rather than C_1+C_2, leading to a more gradual roll-off of gain. For L_2 and C_2 to resonate at ω_1, we have L_2=2L_1. Since, in practice, C_1 and C_2 are not exactly equal, the ratio of L_1 and L_2 can be adjusted to compensate for this difference. To minimize peaking, the output voltage at this frequency $I_{in}/(C_2\omega_1)$ must be equal to that at low frequencies $I_{in}R_1$, yielding

$$R_1 = 2\sqrt{\frac{L_1}{C}} \tag{2.46}$$

The series resonance of L_2 and C_2 depicted in Fig. 2.20(a) not only forces all of I_{in} to flow through C_2, but reverses the sign of the impedance Z_x, thus making V_x negative for $\omega>\omega_1$. As illustrated in Fig. 2.20(b), I_1 and I_2 must therefore flow into node X and, together with I_{in}, pass through C_2. Consequently, $|V_{out}/I_{in}|$ continues to rise until the π network consisting of C_1, L_2, and C_2 begins to resonate [Fig. 2.20(c)], presenting an infinitely impedance at node X and allowing all of I_{in} to flow through R_1 and L_1. For $\omega>\omega_2$, the π network becomes capacitive and $|V_{out}/I_{in}|$ begins to fall, returning to the mid-band value R_1 when the impedance of the π network resonates with L_1 [Fig 2.20(d)]. The amplifier exhibits the frequency response shown in Fig 2.21.

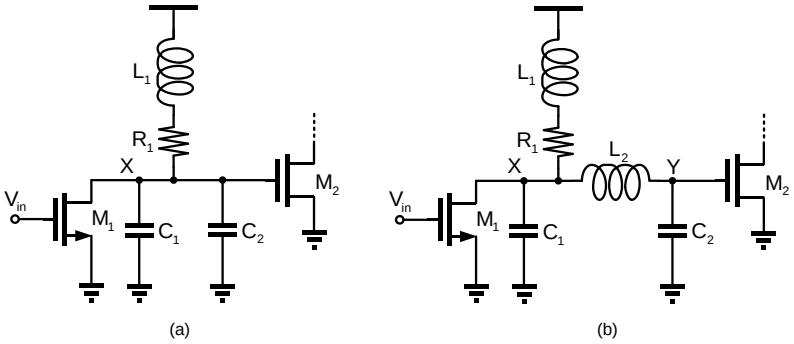


Figure 2.19 (a) Inductively peaked stage, (b) TRA.

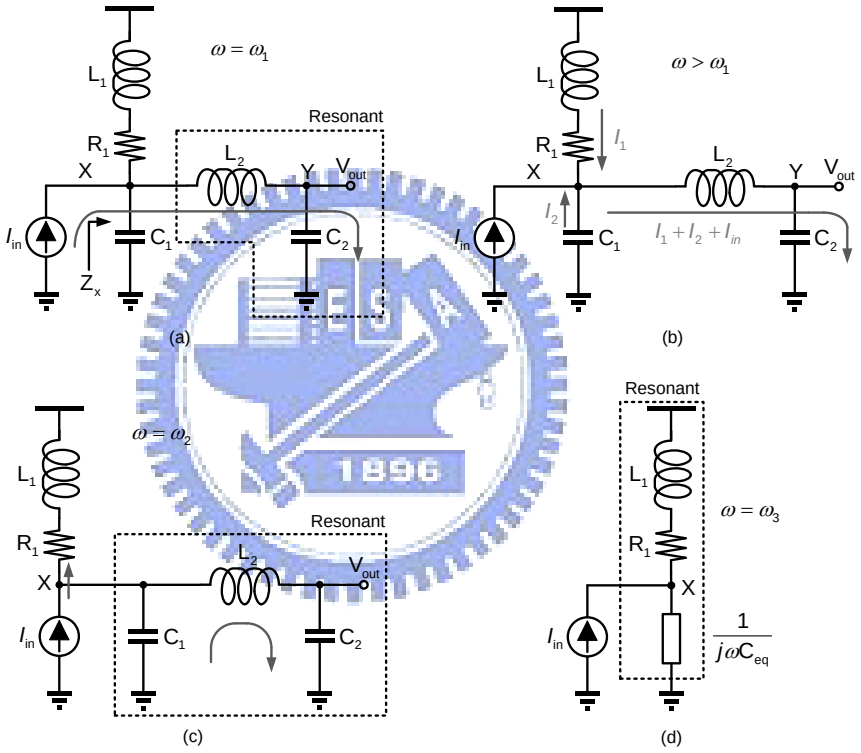


Figure 2.20 Behavior of a triple-resonance circuit at different frequencies.

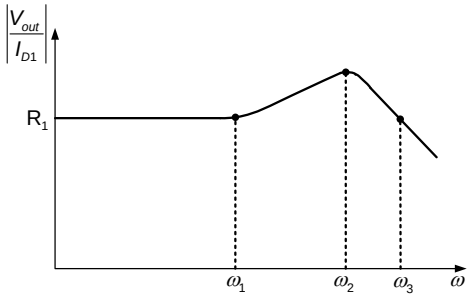


Figure 2.21 frequency response of the TRA.

Chapter 3 *Design of Parallel-RC feedback UWB LNA*

The challenge of building a single radio frequency front-end capable of receiving and processing a multiplicity of bands has stimulated interest in broadband RFIC design. As discussion in section 2.4, the resistive shunt feedback suffers high noise figure and the inductive degeneration can only provides narrow band. To solve these problems and combine the advantages of them, a CMOS UWB LNA with low noise figure, small chip area, and higher figure of merit (FoM) is presented.

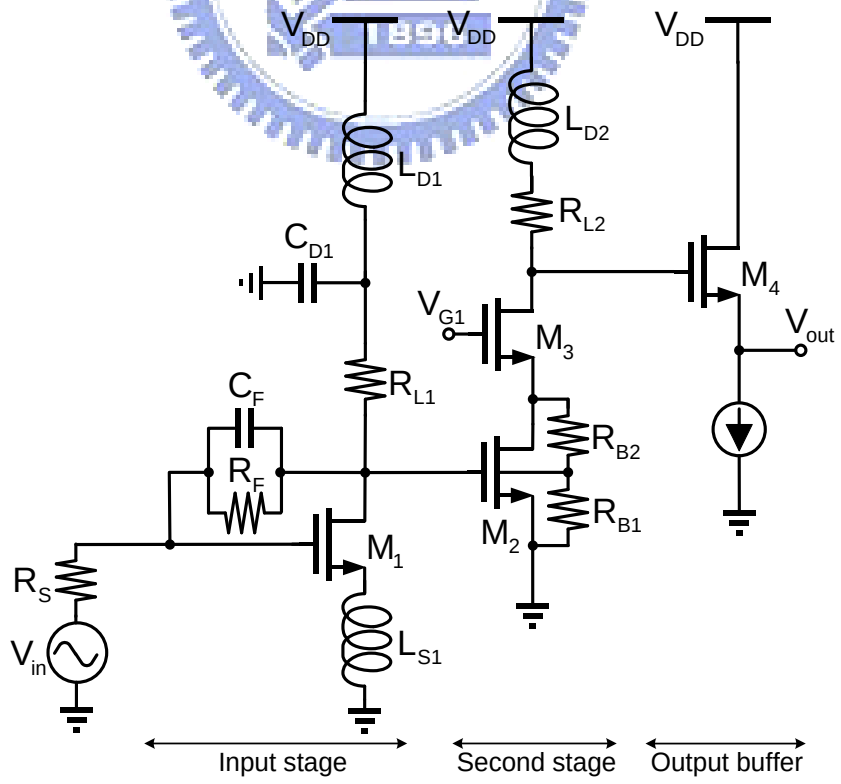


Figure 3.1 Proposed UWB LNA.

3.1 Circuit Design and Analysis

The proposed UWB LNA is depicted in Fig. 3.1. It consists of an input stage, a casecode second stage, and an output buffer. We will discuss their function in order.

3.1.1 Input Stage

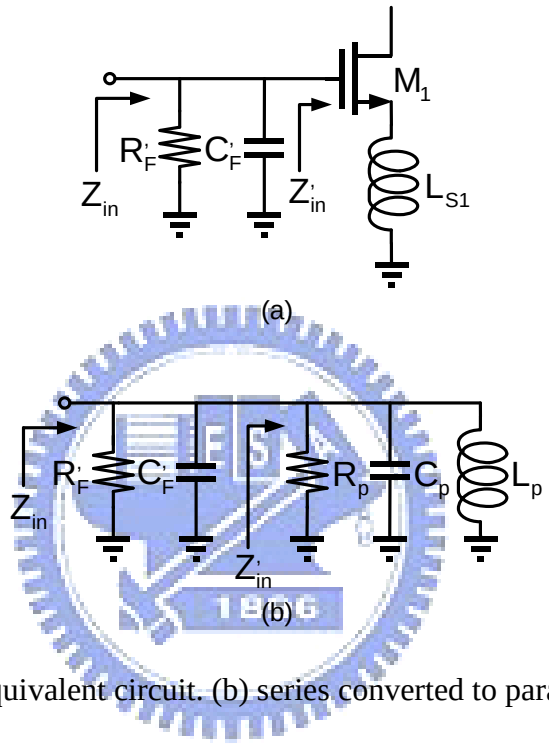


Figure 3.2 (a) Miller equivalent circuit. (b) series converted to parallel of equivalent circuit.

The input stage provides the broadband power and noise matching. The input impedance Z'_{in} seen looking into the gate of transistor M_1 is [2]

$$Z'_{in} = g_{m1}\frac{L_{S1}}{C_{gs1}} + sL_{S1} + \frac{1}{sC_{gs1}} \tag{3.1}$$

where g_{m1} and C_{gs1} is the transconductance and the gate-to-source capacitance of the transistor M_1, respectively. From Fig. 3.1, using Miller's theorem to convert the input stage to that shown in Fig. 3.2(a), we have $R_F' = R_F/(1+A_v)$ and $C_F' = C_F(1+A_v)$, where A_v is the voltage gain from gate to drain, and is equal to

$$A_v = \frac{\left(sC_{gs1}Z_{in}' - g_m Z_F\right)Z_L}{sC_{gs1}Z_{in}'\left(Z_F + Z_L\right)} \tag{3.2}$$

Equation (3.1) presents a series-*RLC* network. For simplicity, the series combination of *R*, *L*, and *C* can be converted to the equivalent parallel circuit shown in Fig. 3.2(b), where R_p, L_p, and C_p can be derived as

$$R_p = \frac{R^2 + \left(\omega L - 1/\omega C\right)^2}{R} \tag{3.3}$$

$$L_p = \frac{R^2 + \left(\omega L - 1/\omega C\right)^2}{\omega^2 L} \tag{3.4}$$

$$C_p = \frac{1}{\omega^2 C\left(R^2 + \left(\omega L - 1/\omega C\right)^2\right)} \tag{3.5}$$

Thus, the input impedance Z_{in} can be derived as

$$Z_{in} = \left(R_F' \parallel R_p\right) \parallel \left(sL_p \parallel \frac{1}{s\left(C_F' + C_p\right)}\right) \tag{3.6}$$

Referring to (3.6), we can make the following observations. First, the form of (3.6) clearly shows that the input impedance is purely resistive at resonance. Thus, a proper choice of g_{m1}, L_{S1}, R_F, and C_F yields a 50 Ω real part. In (3.6), C_F makes the capacitive reactance of Z_{in} closer to the inductive reactance. In other words, C_F makes the imaginary part of Z_{in} closer to zero (see Fig 3.3). Thus, Z_{in} is dominated by $R_F' \,//\, R_p$ during several gigahertz. As a result, the optimal choice of g_{m1}, L_{S1}, R_F, and C_F ensures broadband input matching condition. Second, the resistive component at the input is the parallel combination of R_F' and R_p, and the local feedback noise is inversely proportional to R_F; hence we can select larger feedback resistor R_F in order to suppress noise. The effect of R_F on NF is shown in Fig. 3.4. Third, different from the conventional inductive degeneration [7], the design in this study only uses a small inductor L_{S1} for input matching, so the core area can be reduced.

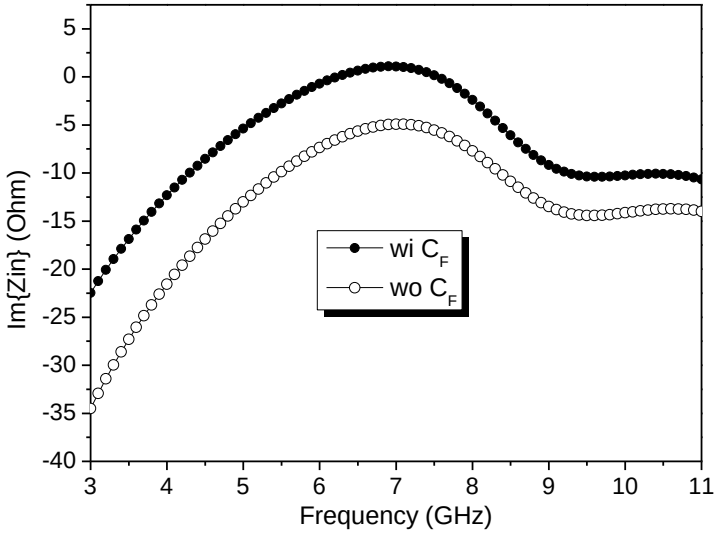


Figure 3.3 Effect of C_F on input impedance.

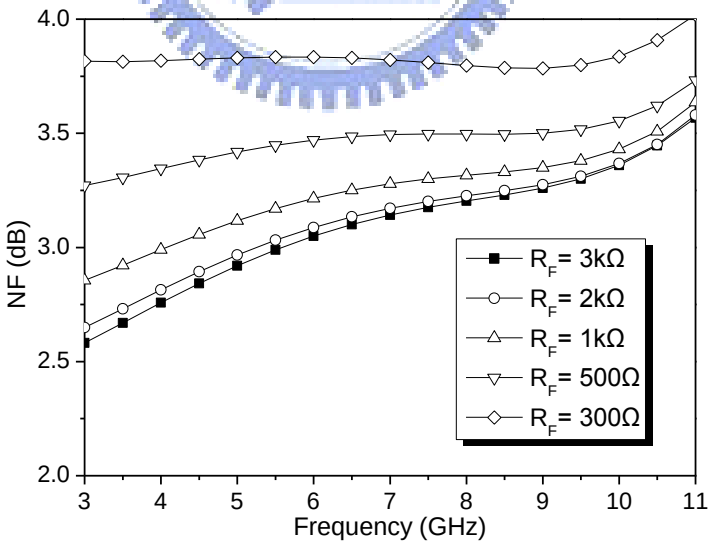


Figure 3.4 Effect of RF on NF.

From the above observations, the proposed input stage has combined the advantages of the resistive feedback and the inductive degeneration and can provide wide-band input matching and better noise performance with a relatively small area. Moreover, a general noise figure of common-source amplifier is linearly proportional to the frequency in 3-10 GHz. The noise factor of input stage F_{in} is equal to

$$F_{in} = \frac{V_{n,o1}^2}{A_v^2} \frac{1}{4kTR_S} \tag{3.7}$$

where $V_{n,o1}$ represents the total noise at output of input stage, which includes the thermal noise of R_S, R_F, R_{L1}, and M_1. From Fig. 3.2(a) the noise contributed by R_S, R_F, and M_1 is proportional to A_v, so R_{L1} plays a critical role in increasing F_{in} due to low A_v at high frequency. Thus we suppress the high-frequency noise of R_{L1} to maintain low NF. As depicted in Fig. 3.5, we assume that the impedance seen looking into the drain of M_1 is equal to Z_o, the impedance of parallel-LC circuit is Z_{LC}, and the output noise voltage contributed by R_{L1} can be derived as

$$V_{n,o1}^2 = 4kTR_{L1} \times \frac{Z_o^2}{\left(Z_o + R_{L1} + Z_{LC}\right)^2} \tag{3.8}$$

From (3.8) the $V_{n,o1}$ is inversely proportional to Z_{LC}, so the output noise voltage can be effectively reduced at resonance. As shown in Fig. 3.6, the L_{D1}, C_{D1}, and L_{S1} can reduce high-frequency noise (7- 15GHz) effectively.

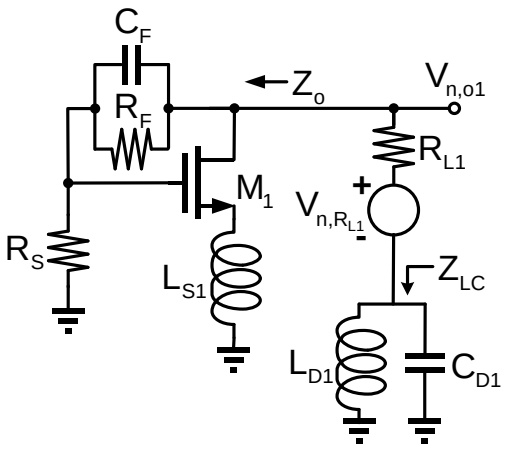


Figure 3.5 Equivalent circuit for suppressing thermal noise of R_{L1}.

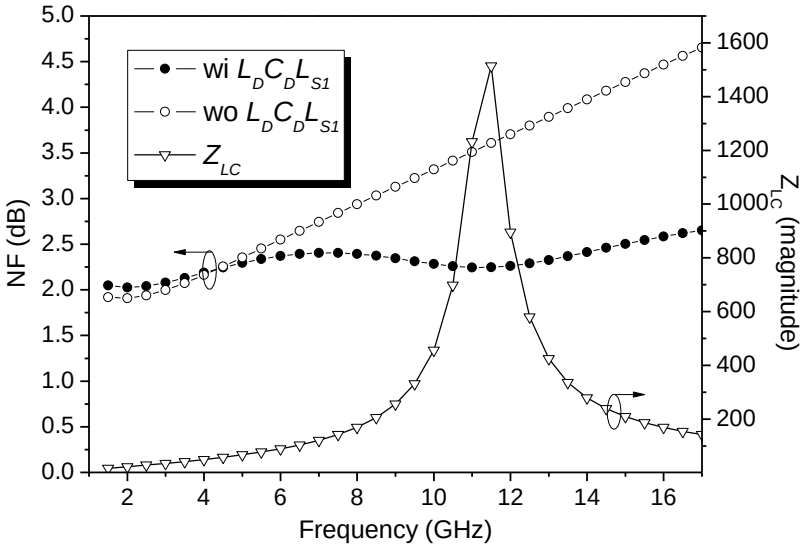


Figure 3.6 Effect of L_D, C_D, and L_{S1} on NF of input stage.

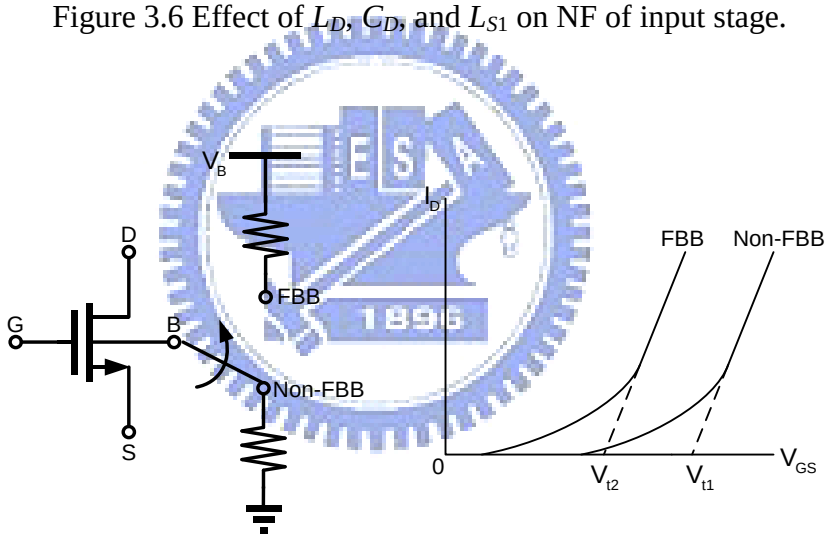


Figure 3.7 I-V characteristics of MOSFET with and without FBB.

3.1.2 Second Stage

The second stage is a cascode common-source stage, which provides high-frequency gain and better isolation. The transistor M_3 is used for improvement of M_1's Miller effect, better isolation, and higher gain. The series peaking inductor L_{D2} can resonate with the total parasitic capacitances C_{D3} at the drain of M_3, and a resistor R_{D2} is added to reduce Q factor of L_{D2} for flat gain.

For deep-submicrometer MOSFETs, the threshold voltage V_t is no longer constant, but influenced by circuit parameters such as gate length, channel width, and drain-to-source voltage due to the short-channel and narrow-channel effects [8]. Typically, transistors with a large channel width and a minimum gate length exhibit a reduced V_t, which is preferable for low-voltage operations. For a MOSFET device, the threshold voltage is governed by the body effect as

$$V_t = V_{t0} + \left(\sqrt{2qN_A\varepsilon_S}/C_{ox}\right)\cdot\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{3.9}$$

where V_{t0} is the threshold voltage for V_{SB}=0, ϕ_F is a physical parameter with a typical value of 0.3 V, N_A is the substrate doping, and ε_S is the permittivity of silicon. From (3.9) we can know that by applying a forward body bias (FBB) technology (see Fig. 3.7), the effective threshold voltage is thus reduced while maintaining a minimum forward junction current between the body and the source terminals.

As shown in Fig. 3.1, we use a voltage divider which consists of resistors R_{B1} and R_{B2} to achieve the Forward Body Bias technique [8]. A general FBB needs an extra DC bias. In other words, we can save an extra DC pad by using a voltage divider, therefore the complexity of layout is lessened; and the FBB can further obtain same g_{m2} with a low supply voltage so that the power consumption can be reduced. Finally, Fig. 3.8 shows simulation frequency response of input stage, second stage, and overall stage. The input stage and the second stage provides low-frequency power gain and high-frequency power gain, respectively. The combination both frequency response results a broadband power gain.

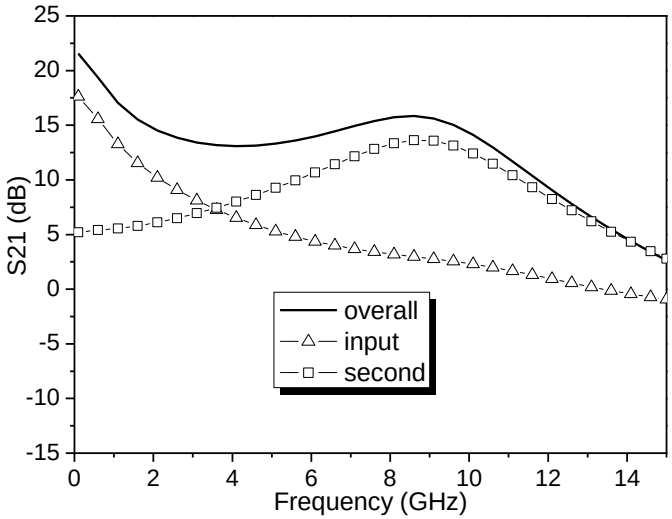


Figure 3.8 Simulation frequency response of input stage, second stage, and overall stage.

3.1.3 Output Buffer

The output buffer is a simple source follower. The output impedance can be approximated as $1/g_m$, which is selected as 50 Ohm for output matching. In order to reduce the parasitic capacitance arisen from a large device, the input device of this buffer must be reduced despite the larger loss occurs. The fixed bias current for M_4 is 4.4 mA from 1.4-V supply.

3.1.4 Noise Analysis

The noise figure of the proposed LNA is dominated by M_1, R_F, and R_{L1} and can be derived as

$$F_{M1} = \frac{\gamma g_m Z_L^2 \left[\left(Z_F + R_S \,||\, Z_{in}^{'} + Z_L \right) Z_{in}^{'} s C_{gs1} \right]^2}{\alpha \left[g_m Z_L \left(R_S \,||\, Z_{in}^{'} \right) + \left(Z_F + R_S \,||\, Z_{in}^{'} + Z_L \right) Z_{in}^{'} s C_{gs1} \right]^2} \frac{1}{A_V^2 R_S} \tag{3.10}$$

$$F_{RF} = \frac{R_F Z_L^2 \left[g_m \left(R_S \,||\, Z_{in}^{'} \right) + Z_{in}^{'} s C_{gs1} \right]^2}{\left(1 + s C_F R_F \right)^2 \left[\left(R_S \,||\, Z_{in}^{'} \right) g_m Z_L + \left(Z_L + Z_F + R_S \,||\, Z_{in}^{'} \right) Z_{in}^{'} s C_{gs1} \right]^2} \frac{1}{A_V^2 R_S} \tag{3.11}$$

$$F_{RL1} = \frac{Z_o^2}{\left(Z_{LC} + R_{L1} + Z_o \right)^2} \frac{R_{L1}}{A_V^2 R_S} \tag{3.12}$$

where Z_o is defined by

$$Z_o = \frac{\left(Z_F + R_S \parallel Z_{in}'\right) Z_{in}' s C_{gs1}}{1 + g_m \left(R_S \parallel Z_{in}'\right)} \tag{3.13}$$

Thus, the total noise factor F is approximated as

$$F = 1 + F_{M1} + F_{RF} + F_{RL1} \tag{3.14}$$

In Equation (3.11) and (3.12), the F_{RF} and the F_{RL1} is inversely proportional to R_F and Z_{LC}, respectively. As a result, a larger feedback resistor R_F and a parallel-LC network can suppress noise effectively.

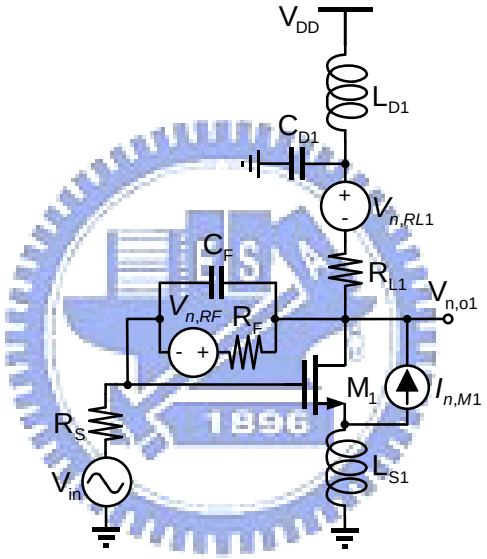


Figure 3.9 Noise equivalent circuit of input stage.

3.2 Experimental Results

The proposed UWB LNA has been fabricated by the TSMC 0.18-μm CMOS process. The chip microphotograph is shown in Fig. 3.10. The chip area is 0.697 mm × 0.657 mm including testing pads. The measurement is carried out on wafer for RF characterization.

Fig. 3.11 shows measured and simulated power gain and input return loss of the UWB LNA. The measured power gain is 12.4 dB (±1.5 dB variation) over 3.1 to 10.6 GHz. The measured high-frequency gain is less than simulated one about 1.4 dB. It may be due to

process variation and inaccuracy of inductor and transistor models. The measured input return loss is −9.4 to −32.5 dB from 3.1 to 15GHz. Fig. 3.12 shows measured and simulated output return loss and reverse isolation of the UWB LNA. The measured output return loss is below −8.5 dB and the measured reverse isolation is below −45 dB across the entire band.

The measured and simulated NFs are illustrated in Fig. 3.13. The measured NF is 2.5-4.7 dB from 3.1 to 10.6 GHz. The measured NF is larger than the simulated one due to degraded power gain. Fig. 3.14 shows IIP3 measured by applying two-tone test with 1-MHz spacing. The measured IIP3 is −8.5 dBm at 8 GHz.

In general, the figure of merit (FoM) is applied to evaluate performance of LNAs, and is defined as [9]

$$FoM\left[mW^{-1}\right]=\frac{S_{21}[1]\times BW[GHz]}{(NF-1)[1]\times P_{DC}[mW]\times f_t[GHz]}$$

This FoM includes the most relevant parameters in order to evaluate a UWB LNA for low-cost and low-power applications.

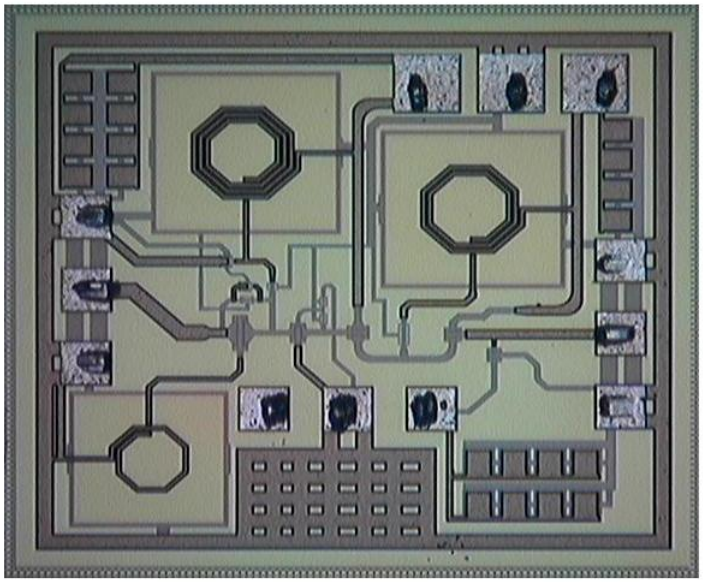


Figure 3.10 Chip microphotograph of the UWB LNA.

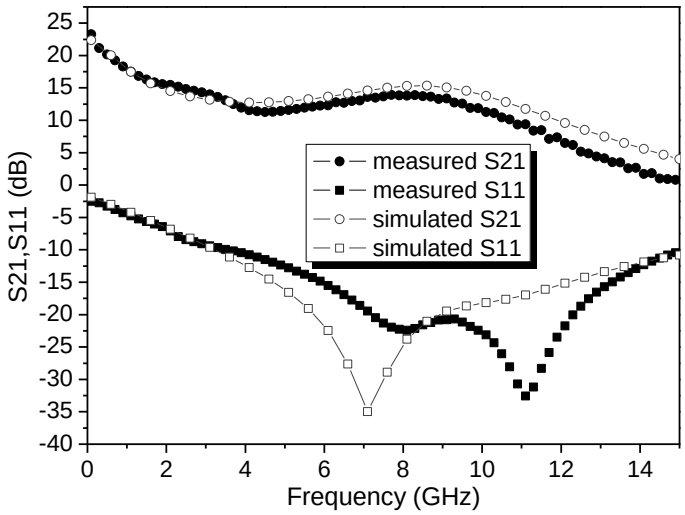


Figure 3.11 Measured and simulated power gain (S21) and input return loss (S11) of the UWB LNA.

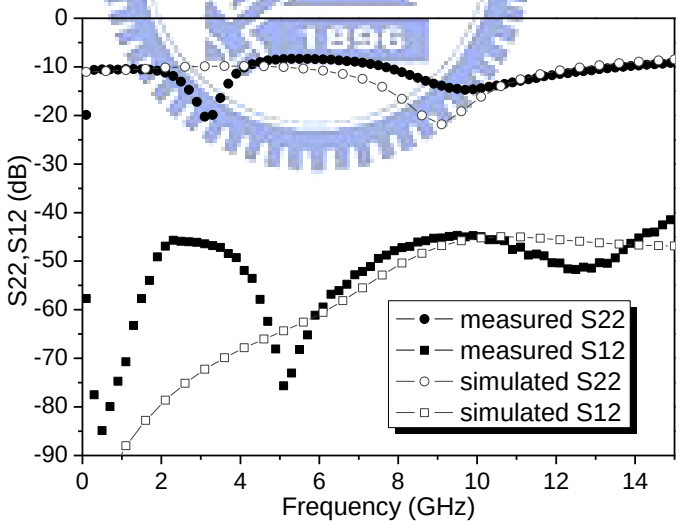


Figure 3.12 Measured and simulated output return loss (S22) and reverse isolation (S12) of the UWB LNA.

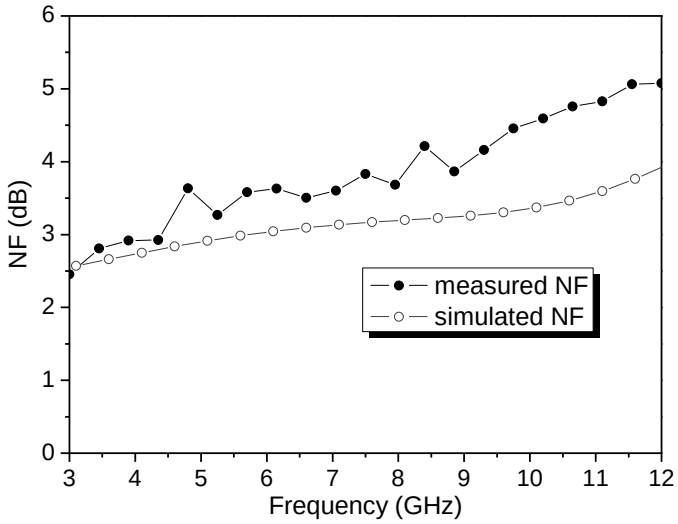


Figure 3.13 Measured and simulated noise figure of the UWB LNA.

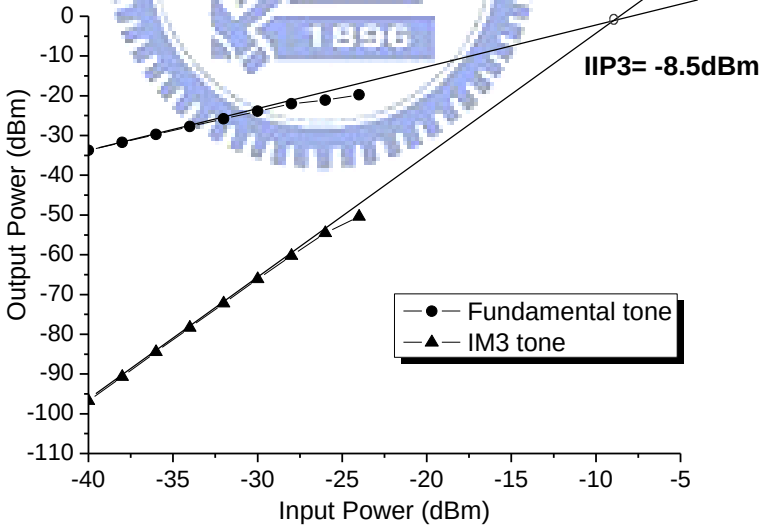


Figure 3.14 Measured IIP3 at 8 GHz.

TABLE II

Measured Performance Summary and Comparison

Ref.	CMOS Technology	$BW_{3\text{-}dB}$ (GHz)	G_{max} (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mm^2)	FoM (W^{-1})
This Work	**0.18μm**	**3.1－10.6**	**13.9**	**2.5－4.7**	**－8.5**	**14.4**	**0.46**	**57.1**
[1]	0.18μm	1.2－11.9	9.7	4.5－5.1	－6.2	20	0.59	15.5
[3]STD	0.18μm	2.3－9.2	9.3	4－8	－6.7	9	1.1	25.5
[10]	0.18μm	0.4－10	12.4	4.4－6.5	－6	12	0.42	32.8
[11]$^{+}$	0.18μm	3.1－10.6	17.5	3.1－5.7	－	33.2*	0.5	28.2
[12]	0.18μm	2.8－7.2	19.1	3－3.8	－1	32*	1.63	21.5
[13]	0.18μm	0.04－7	8.6	4.2－6.2	＋3	9	1.16	22.1

$^{+}$：Simulation only.

*：The power consumption including buffer, ours is 21mW.

3.3 Summary

A UWB LNA is proposed and implemented by the TSMC 0.18-μm 1P6M process. The measured performance of the proposed LNA is compared with others, which is summarized in Table II. It is found that our circuit achieves the lowest noise figure and the best FoM. The proposed UWB LNA compared with other UWB techniques has excellent noise performance, small size, and higher FoM.

Chapter 4 *Design of Noise-Canceling UWB LNA*

Since the LNA is the first gain stage in the receive path, its noise figure directly adds to that of the system. As discussed in section 2.4, we suppress noise of LNA as much as possible in order to obtain better SFDR. In this chapter, we use a transformer to achieve noise cancellation with low power consumption and realize in UWB frequency.

4.1 Noise-Canceling Principle

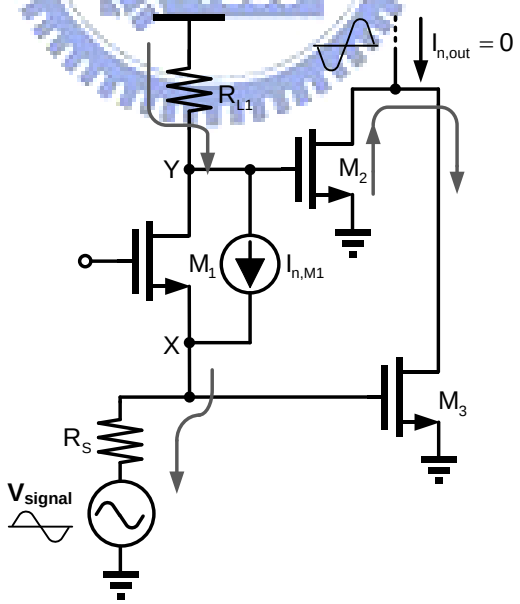


Figure 4.1 Principle of the noise-canceling technique.

The purpose of noise cancellation is to decouple the input matching with NF by canceling the output noise from the matching device. Fig. 4.1 illustrates an example, which is based on a common-gate LNA. The input matching is accomplished by setting $1/g_{m1}$ to 50 Ω. The noise current of M_1 is modeled by the current source $I_{n,M1}$, which flows into node X but out of node Y. This creates two fully correlated noise voltages at nodes X and Y with opposite phases. These two voltages are converted to currents by M_3 and M_2, respectively. By properly designing g_{m2} and g_{m3}, the noise contributed by M_1 can be cancelled at the output. On the other hand, the signal voltages at nodes X and Y are in phase, resulting in constructive addition at the output. The condition for complete noise cancellation is derived as [1]

$$I_{n,out} = \frac{I_{n,M1}}{1+g_{m1}R_S} R_{L1} g_{m2} - \frac{I_{n,M1}}{1+g_{m1}R_S} R_S g_{m3} = 0$$

$$\Rightarrow g_{m2} R_{L1} = g_{m3} R_S \tag{4.1}$$

Although the noise contributed by M_1 can be cancelled at the output, another input device M_3 is still contributed noise to the output. Thus, the noise of the whole system is difficult to be reduced to a very low level.

According to the points discussed above, by using a transformer to achieve noise cancellation is proposed. An initially noise-canceling topology is depicted in Fig. 4.2. We will be divided into signal and noise two parts and analyzed the noise-canceling principle. As shown in Fig. 4.2(a), the input signal at gate of transistor M_1 can produce an opposite-phase signal at drain of transistor M_1. The transformer induces an opposite-phase signal at source of M_1. Consequently, the signals at source and drain of M_1 can be amplified and added to the output via M_2 and M_3, respectively. As shown in Fig. 4.2(b), the noise current of M_1 is modeled by the current source $I_{n,M1}$ which flows into node X but out of node Y. This produces two fully correlated noise voltages at nodes X and Y with opposite phases. These two voltages are converted to currents by M_2 and M_3, respectively. We assume that the impedance at drain of M_1 is Z_D and impedance at source of M_1 is Z_S, the output noise current can be derived as

$$I_{n,out} = I_{n,M1}\left(Z_D \times g_{m2} - Z_S \times g_{m3}\right) \tag{4.2}$$

Thus, the condition for complete noise cancellation is

$$Z_D \times g_{m2} - Z_S \times g_{m3} \tag{4.3}$$

The proposed noise-canceling technique does not have noise source contributed by another input device, so we can be in order to expect its noise is suppressed effectively.

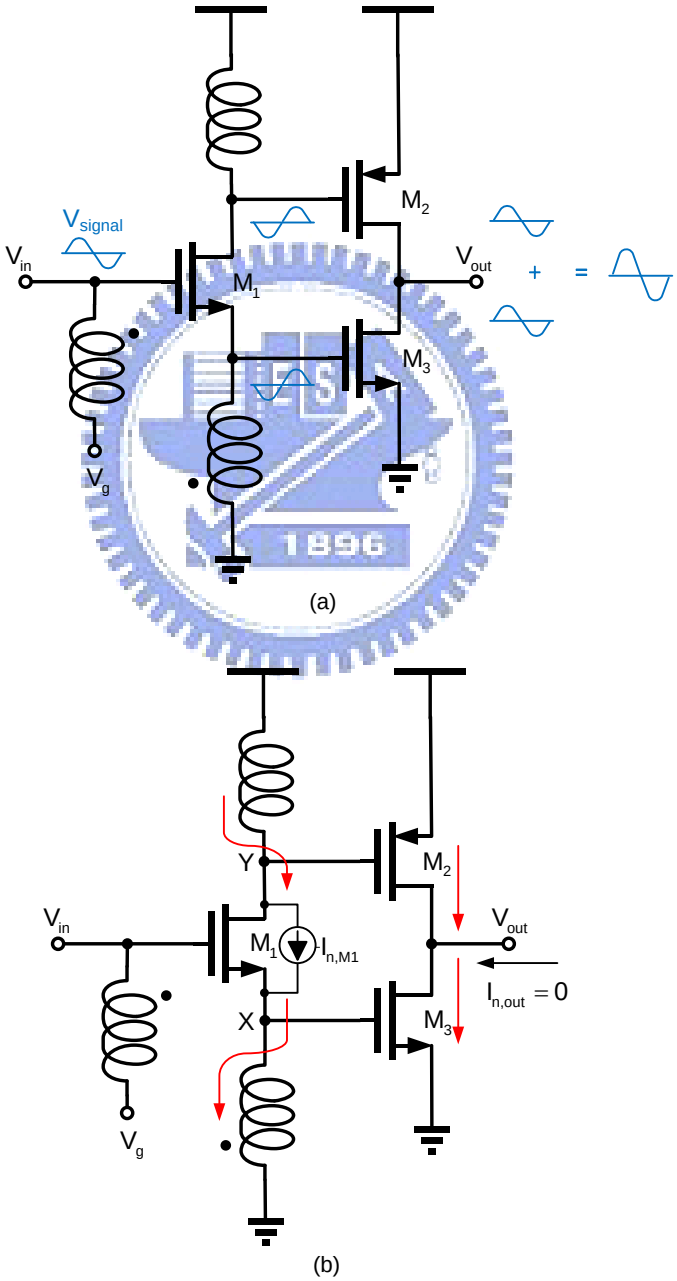


Figure 4.2 Proposed noise-canceling technique.

4.2 Circuit Design of The Noise-Canceling UWB LNA

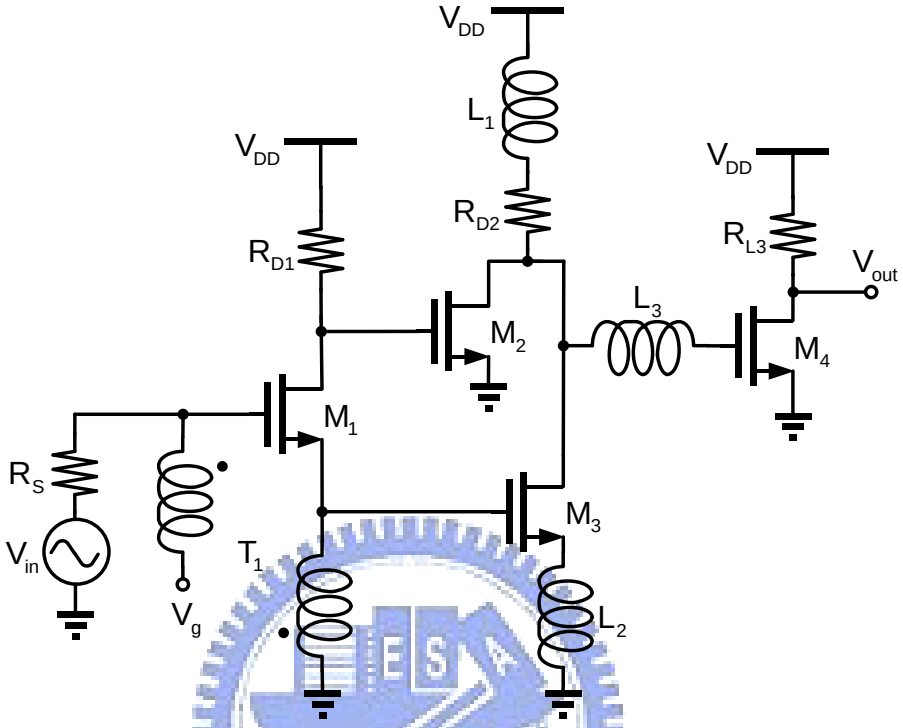


Figure 4.3 Proposed noise-canceling UWB LNA.

The proposed noise-canceling UWB LNA is depicted in Fig. 4.3. The inductor L_1 is used for shunt peaking, extending the bandwidth efficiently. The input capacitance of M_3 influences inductance of transformer to bring unnecessary resonance. In order to lighten this problem we use a series inductor L_2 at source of M_3. Thus, the equivalent input capacitance of M_3 is reduced. The series inductor L_3 further resonates with the input capacitance of M_4, resulting in a large bandwidth. An output matching stage which consists of transistor M_4 and resistor R_{L3} is added for measurement purpose only.

4.2.1 Input Match

Fig. 4.4 shows the small-signal equivalent circuit for the transformer input stage. Parasitic resistance in both the primary and secondary windings (r_{pri} and r_{sec}, respectively) are retained in order to relate the physical size of the transformer to input impedance. The A is the forward current gain from gate to source of M_1

$$A = \frac{i_s}{i_g} = 1 + g_m Z_{gs} \tag{4.4}$$

The feedback factor (β) is the inverse of the transformer's effective turn ratio k/n. The k is the magnetic coupling factor and n is the physical turn ratio. Here, β simplifies to ($1/n$) for the model of Fig. 4.4. In Fig. 4.4, we have $i_{fb}=\beta i_s=\beta A i_g$, the voltage of secondary winding V_{sec}

$$\begin{aligned} V_{\text{sec}} &= V_X - i_{fb} r_{\text{sec}} \\ &= V_X - \beta A i_g r_{\text{sec}} \end{aligned} \tag{4.5}$$

and the voltage of primary winding V_{pri}

$$V_{pri} = \beta V_{\text{sec}} = \beta\left(V_X - \beta A i_g r_{\text{sec}}\right) \tag{4.6}$$

Then, we use a testing voltage source to calculate the input impedance. The testing voltage V_x is derived as

$$\begin{aligned} V_x &= i_g\left(r_g + Z_{gs} + A r_{pri}\right) - V_{pri} \\ &= \frac{i_g}{1+\beta}\left[A\left(\beta^2 r_{\text{sec}} + r_{pri}\right) + r_g + Z_{gs}\right] \\ &= i_g \frac{A}{1+\beta}\left[\left(\beta^2 r_{\text{sec}} + r_{pri}\right) + \frac{A-1}{g_m A} + \frac{r_g}{A}\right] \end{aligned} \tag{4.7}$$

and the testing current i_x is derived as

$$\begin{aligned} i_x &= i_{fb} + i_g \\ &= i_g\left(1+\beta A\right) \end{aligned} \tag{4.8}$$

Thus, the input impedance Z_{in} equal to V_x/i_x can be derived as

$$Z_{in} = \frac{A}{(1+\beta)(1+\beta A)}\left[\left(\beta^2 r_{\sec} + r_{pri}\right) + \frac{A-1}{g_m A} + \frac{r_g}{A}\right]$$

$$\approx \frac{1}{(1+\beta)\beta g_m} \tag{4.9}$$

It depends chiefly on the feedback factor (β) and transconductance g_m. From (4.9), a proper designed transformer and select g_m ensures broadband input matching condition.

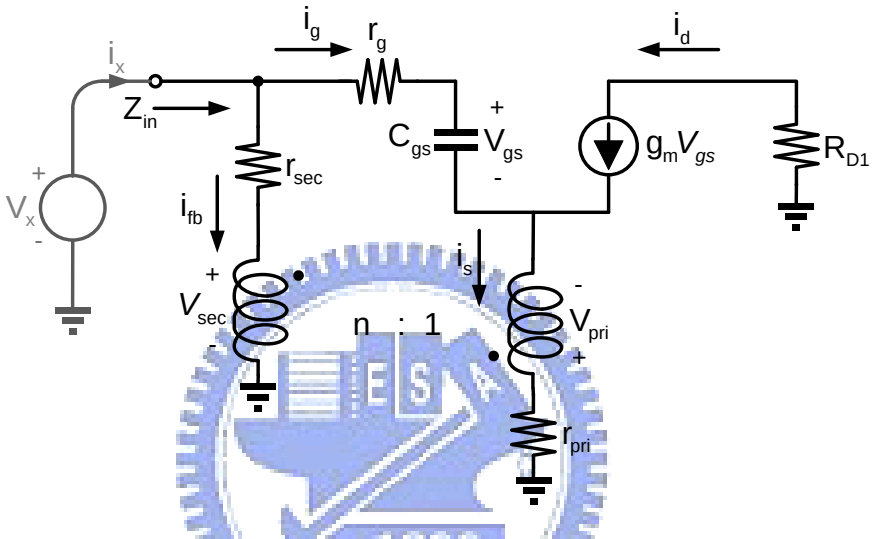


Figure 4.4 Small-signal equivalent circuit for the transformer input stage.

4.2.2 Noise Analysis

The transformer input stage shown in Fig. 4.4 has a transconductance (G_D) of

$$G_D = \frac{1}{Z_{in} + R_S}\frac{A-1}{1+A\beta} \tag{4.10}$$

where A is the forward current gain from gate to source of M_1

$$A = \frac{i_s}{i_g} = 1 + g_m Z_{gs} \tag{4.11}$$

By applying the proposed noise-canceling technique, the noise figure of the LNA is dominated by R_{L1}, M_2, and M_3. We ponder a mismatch between $g_{m2}Z_D$ and $g_{m3}Z_S$, the noise factor F can be derived as the following equations:

$$F = 1 + F_{M1} + F_{RL1} + F_{M2} + F_{M3} \tag{4.12}$$

where F_{M1}, F_{RL1}, F_{M2}, and F_{M3} are described by

$$F_{M1} = \frac{\tau^2 4kTg_{m1}\gamma/\alpha\left(g_{m2}R_{D1} - \sigma\beta^2 g_{m3}R_S\right)^2}{4kTR_S\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2}$$

$$= \frac{\tau^2 g_{m1}\gamma\left(g_{m2}R_{D1} - \sigma\beta^2 g_{m3}R_S\right)^2}{\alpha R_S\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2} \tag{4.13}$$

$$F_{RD1} = \frac{4kTR_{D1}g_{m2}^2}{4kTR_S\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2}$$

$$= \frac{R_{D1}g_{m2}^2}{R_S\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2} \tag{4.14}$$

$$F_{M2} = \frac{4kTg_{m2}\gamma/\alpha}{4kTR_S\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2}$$

$$= \frac{g_{m2}\gamma}{\alpha R_S\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2} \tag{4.15}$$

$$F_{M3} = \frac{4kTg_{m3}\gamma/\alpha}{4kTR_S\left(1+g_{m3}sL_2\right)\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2}$$

$$= \frac{g_{m3}\gamma}{\alpha R_S\left(1+g_{m3}sL_2\right)\left(G_D g_{m2}R_{D1} + \sigma\beta g_{m3}\right)^2} \tag{4.16}$$

where τ and σ are defined by

$$\tau = \frac{1}{1+(1+\beta)\beta g_{m1}R_S} \tag{4.17}$$

$$\sigma = \frac{1}{1+g_{m3}sL_2 + s^2L_2C_{gs3}} \tag{4.18}$$

As shown in Fig. 4.5, the computed noise figure is also compared to the case with M_3 turned OFF. The simulated *S* parameters of this LNA with M_3 turned ON and OFF, respectively, are shown in Fig. 4.6. The comparison is performed with the same power consumption and a similar bandwidth.

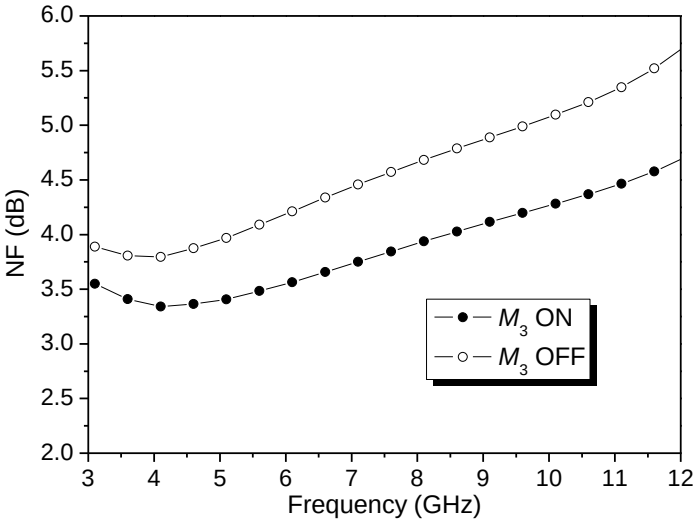


Figure 4.5 Computed NF of LNA with M_3 turned ON and OFF.

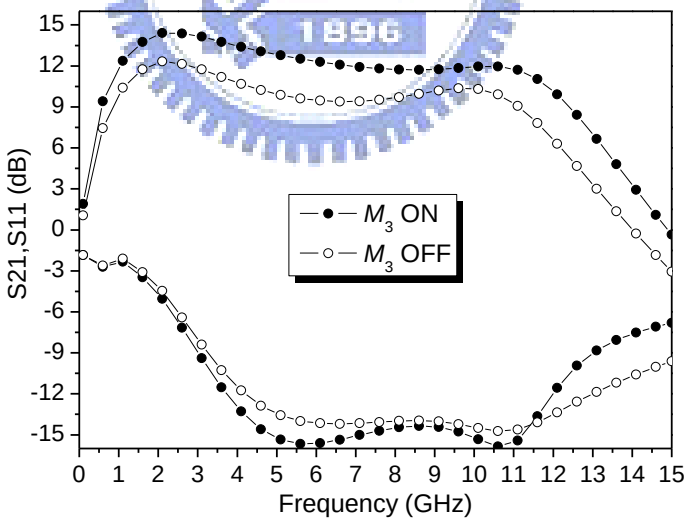


Figure 4.6 Simulated *S* parameters of LNA with M_3 turned ON and OFF.

4.3 Experimental Results

The proposed transformer noise-canceling LNA has been fabricated by the TSMC 0.18-μm CMOS process. The chip microphotograph is shown in Fig. 4.7. The chip area is 0.731 mm × 0.645 mm including testing pads. The measurement is carried out on wafer for RF characterization.

Fig. 4.8 shows the measured and the simulated power gain and input return loss of the noise-canceling LNA. The measured power gain is 13.05 dB (±2.85 dB variation) over 0.7 to 11.5 GHz. The measured high-frequency gain is less than simulated one about 1.4 dB and the measured low-frequency gain is more than simulated one about 1.6 dB. It may be due to process variation and inaccuracy of inductor and transistor models. Thus, the 3-dB bandwidth whole moved to high frequency (3.7 to 11.5 GHz). The measured input return loss is －10.1 to －17.8 dB from 3.1 to 13 GHz. Fig. 4.9 shows the measured and the simulated output return loss and reverse isolation of the noise-canceling LNA. The measured output return loss is below －9.3 dB and the measured reverse isolation is below －40.8 dB across the entire band.

The measured and simulated NFs are illustrated in Fig. 4.10. The measured NF is 3.8-5.6 dB across the entire band. The transformer has not protected with guard ring in order to save chip area. The substrate noise may be introduced in the transformer, so the measured NF is larger than the simulated one due to the substrate noise. Fig. 4.11 shows IIP3 measured by applying two-tone test with 1-MHz spacing. The measured IIP3 is －5 dBm at 6 GHz.

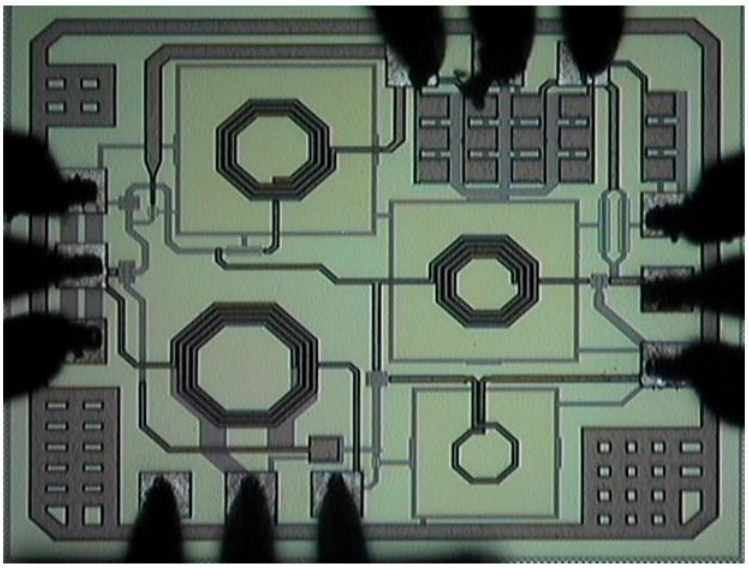


Figure 4.7 Chip microphotograph of the noise-canceling LNA.

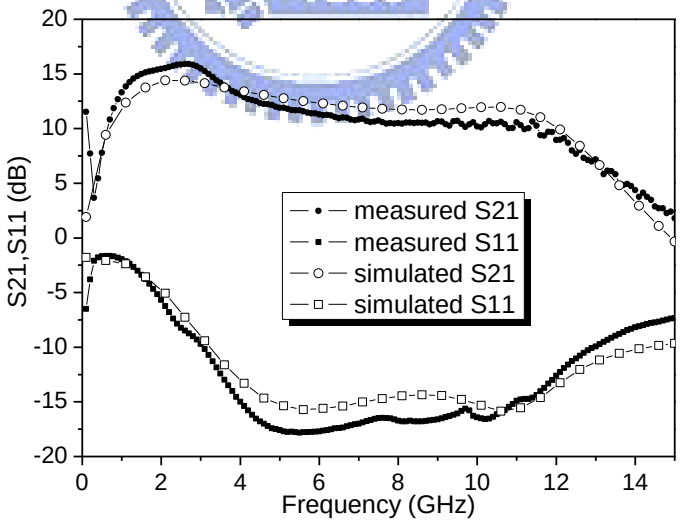


Figure 4.8 Measured and simulated power gain (S21) and input return loss (S11) of the noise-canceling LNA.

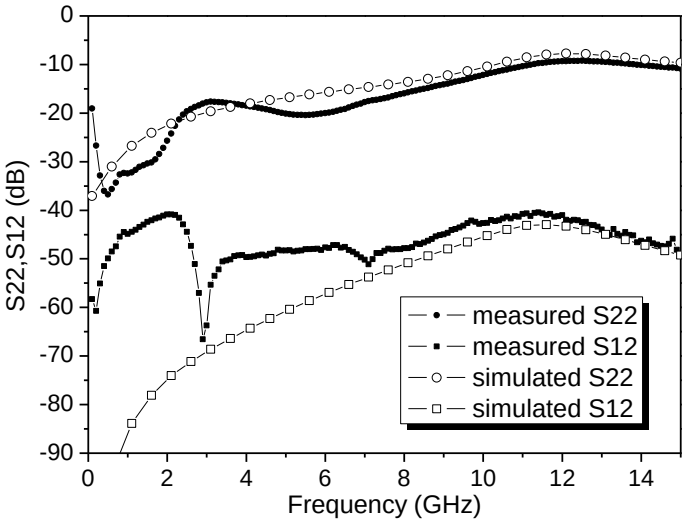


Figure 4.9 Measured and simulated output return loss (S22) and reverse isolation (S12) of the noise-canceling LNA.

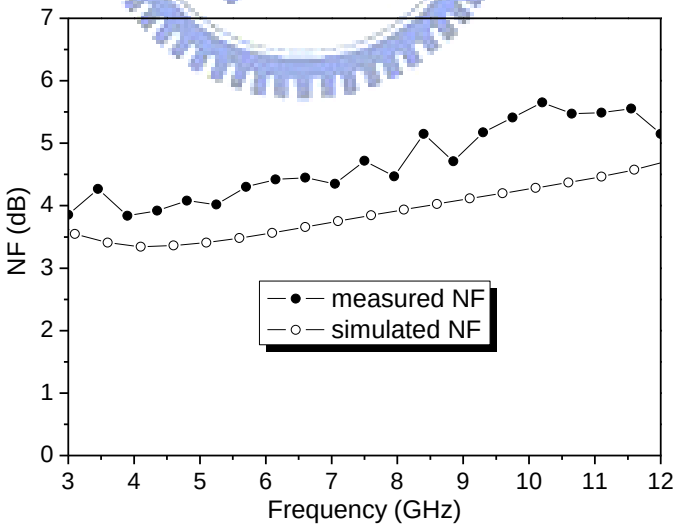


Figure 4.10 Measured and simulated noise figure of the noise-canceling LNA.

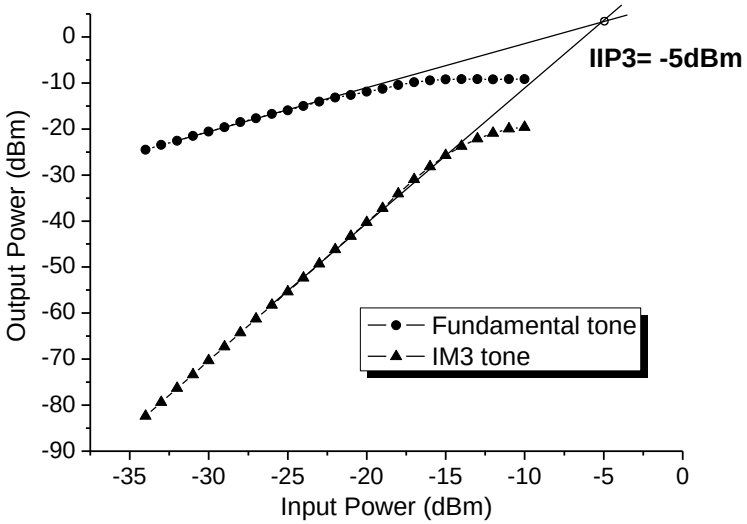


Figure 4.11 Measured IIP3 at 6 GHz.

TABLE III

Measured Performance Summary and Comparison

Ref.	CMOS Technology	$BW_{3\text{-}dB}$ (GHz)	G_{max} (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Area (mm^2)	FoM (W^{-1})
This Work	**0.18µm**	**3.7-11.5**	**13.9**	**3.8-5.6**	**−5**	**9.7**	**0.47**	**47.4**
[1]	0.18µm	1.2-11.9	9.7	4.5-5.1	−6.2	20	0.59	15.5
[3]STD	0.18µm	2.3-9.2	9.3	4-8	−6.7	9	1.1	25.5
[3]TW	0.18µm	2.4-9.5	10.4	4.2-8	−8.8	9	1.1	27.6
[13]	0.18µm	0.04-7	8.6	4.2-6.2	+3	9	1.16	22.1
[14]	0.18µm	1-12.6	10.8	4.6-5.5	+7	39.6	0.66	9.5
[15]	0.18µm	2.7-9.1	10	3.8-6.9	−	7	1.57	35.7

4.4 Summary

A noise-canceling UWB LNA is proposed and implemented by the TSMC 0.18-μm 1P6M process. The measured performance of the proposed LNA is compared with others, which is summarized in Table III. It is found that our circuit achieves the lowest chip area, higher power gain, and the best FoM.

Chapter 5 *Conclusion*

In this thesis, we present a parallel-*RC* feedback low noise amplifier and a transformer noise-canceling low noise amplifier for UWB applications. These proposed circuits are fabricated by the TSMC 0.18-μm 1P6M process.

In chapter 3, by using the proposed parallel-*RC* feedback with a source inductance technique, the local feedback noise can be reduced to achieve very low NF and broadband input matching. The measured NF is 2.5-4.7 dB and measured power gain is 10.9-13.9 dB from 3.1 to 10.6 GHz. The measured input return loss is below －9.4 dB from 3.1 to 15 GHz. The IIP3 is －8.5 dBm at 8 GHz. It consumes 14.4 mW from 1.4 V supply and occupies a chip area of only 0.46 mm^2.

In chapter 4, by using inductive peaking techniques and the proposed noise-canceling topology, the broadband noise cancellation can be brought to the desired UWB band. Moreover, the broadband input matching and power gain are also achieved. The measured NF is 3.8-5.6 dB across the entire band. The measured power gain is more than 10.2 dB from 0.7 to 11.5 GHz. The measured input return loss is below －10.1 dB from 3.1 to 13 GHz. The IIP3 is －5 dBm at 6 GHz. It consumes 9.7 mW from 1.2 V supply and occupies a chip area of only 0.47 mm^2 for a low cost design.

The area of millimeter-wave (MMW) system research and design has become increasingly popular in recent years. As the size scales down, the CMOS devices have achieved a much

higher operation frequency. Thus, we will be devoted to designing high-frequency IC (for example high than 60 GHz) in the future.

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