國立交通大學

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碩 士 論 文

尾電流塑形低相位雜訊暨

電流共用低功率四相位輸出壓控振盪器設計與研究

Design of Tail Current-Shaping Low Phase Noise QVCO and

Current-reused Low Power QVCO

研究生：黃子哲

指導教授：周復芳　博士

中　華　民　國　九　十　八　年　七　月

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尾電流塑形(Tail Current-Shaping)低相位雜訊暨電流共用低功率四相位輸出壓控振盪器設計與研究

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摘　要

本論文討論分為兩部份，第一部份為利用尾電流塑型技巧達成低相位雜訊目地之四相位輸出壓控振盪器，第二部份為利用電流共用架構達成低功率消耗之四相位輸出壓控振盪器。在第一部份，我們利用了兩個差動輸出一階諧波鎖相振盪器建構出一尾電流塑形四相位輸出壓控振盪器。利用此振盪器之輸出訊號作為尾端電流源之電晶體閘極端的交流輸入訊號我們可以達成降低相位雜訊之目地。本四相位壓控振盪器由 TSMC 0.18μm mixed-signal/RF CMOS 1P6M 製程實現，晶片面積為 0.7x1.1 mm^2。量測結果顯示出：本壓控振盪器之振盪頻率為 5.28GHz，在供應電壓為 1.4V 之條件下損耗功率為 11.2mW，相位雜訊為-119.3dBc/Hz@1MHz。

第二部份本論文提出一電流共用架構來降低壓控振盪器之功率消耗。藉由此共用電流之方法，我們可將振盪器之功率消耗降至為原先的二分之一。我們將兩差動輸出電流共用振盪器利用背閘極耦合(Back-Gate Coupling)方式建構出一四相位輸出振盪器來達成低功率損耗之目地。模擬結果顯示：本壓控振盪器之振盪頻率為 10GHz，在供應電壓為 1.2V 之條件下損耗功率僅為 1.64mW，相位雜訊為-111.7dBc/Hz@1MHz。

Design of Tail Current-Shaping Low Phase Noise QVCO and Current-reused Low Power QVCO

Student: Tze-Che Huang Advisor: Dr. Christina F. Jou

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ABSTRACT

This thesis discusses about designs of tail current-shaping low-phase noise QVCO and current-reused low power QVCO. In the first part, we present a new tail current-shaping quadrature voltage-controlled oscillator (QVCO) which consists of two first-harmonic injection-locked oscillators (ILOs). The outputs of the proposed QVCO are injected back to the gates of the QVCO's tail transistors in order to shape the tail current. With the implementation of tail current-shaping, the RMS value of the effective impulse sensitivity function (ISF) of the proposed QVCO is 40% smaller than the conventional QVCO topology. The proposed CMOS LC-tank QVCO has been implemented with the TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology and the die area is 0.7x1.1 mm^2. The total power consumption is 11.2 mW at the supply voltage of 1.4 V. The measured phase noise at 1MHz offset is -119.3dBc/Hz at the oscillation frequency of 5.28 GHz and the figure of merit (FOM) of the proposed QVCO is about -183dBc/Hz.

In the second part, we propose a current-reused QVCO topology to reduce the power consumption. In our design, the proposed QVCO consists of two NMOS current-reused differential VCO. The qudra-phase signals are coupled by back-gate coupling technique. Therefore, the power consumption of the proposed QVCO can be cut in half by reusing the dc

currents compared to the conventional QVCO topologies. The simulated results show that the total power consumption is about 1.64 mW since the QVCO core circuit draws 1.37 mA from a 1.2 V V_{dd} supply. The simulated phase noise at 1 MHz offset is-111.7dBc/Hz at the oscillation frequency of 10 GHz and the FOM is about -189.6dBc/Hz.

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時光飛逝，兩年碩士班生涯匆匆的就過去了，回首過程的點滴，才發現許多回憶和經歷都是值得回味的。從高中畢業決定專業志向至今一路走來，首要感謝的是我的父母對我全心的信任以及全方位的支持，感謝你們陪我走過求學歷程中的許多起伏，在我小有成就時給予我極大的鼓勵，在我面對挫折時對我不求回報的包容，對於這份親情的付出我此生都無以回報，只能在此表達我對你們由衷的感謝。此外要感謝的還有關心我的親人們，感謝我的弟弟子晏，即便遠在太平洋的另一端仍不時的給我關心支持，感謝我的奶奶及其它親人們，你們對我的期許是我前進的動力，感謝我的女友顗如，在我最需要妳的時候與我相逢，改變了我的態度及生活，因為擁有妳的笑容，才讓我有力量面對生活的一切。

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黃子哲 於 風城

2009, July

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1.1 Background and Motivation

In the last years, the requirements of low-cost and low-power for wireless system have dramatically increased due to the continuous growth of personal wireless communications. Wireless transceivers for many standards, including GSM, Bluetooth, WLAN require low-power design techniques to enhance their battery lifetime and to improve their portability. For radio frequency integrated circuit (RFIC) designers, a low-power and high-integration design is a great concern.

In the wireless transceiver blocks, phase-locked loops (PLL) are widely utilized such as frequency synthesizers and clock sources. Since the voltage-controlled oscillators (VCO) play a key role in the PLL circuits and the phase noise of the VCO directly affect the performance of the PLL circuits, the low-power and low-phase noise of VCOs are required. Due to the requirements of quadrature local oscillator (LO) generation for up- and down-conversions with image-reject mixing in the wireless transceiver blocks, a quadrature VCO (QVCO) with accurate quadra-phase outputs is a general design.

In 2002, the Federal Communications Commission (FCC) has allocated 7500-MHz of spectrum for ultra wideband (UWB) system in 3.1~10.6 GHz [1]. According to FCC's definition, UWB system occupied a bandwidth is equal to or greater than 500MHz when the center frequency is over than 2.5GHz, or has a fractional bandwidth is equal to or greater than 20 % of the center frequency when the center frequency is less than 2.5GHz. There are two proposals for UWB system: DS-CDMA (Direct-Sequence Code Division Multiplexing Access) and MB-OFDM (Multi-Band Orthogonal Frequency Division Multiplexing).

Table 1-1 Wireless communication system characteristic

System	WCDMA	WLAN		WPAN	
		802.11 b/g	802.11 a	Bluetooth	UWB
Frequency (GHz)	1.92~1.98 2.11~2.17	2.4~2.4835	5.15~5.35	2.4~2.48	3.1~10.6
Modulation	QPSK	QPSK/OFDM	OFDM	GFSK	DSSS/QPSK
Channel Bandwidth	5 MHz	20 MHz	20 MHz	1 MHz	528 MHz
Data Rate (bit/sec)	384 k/2 M	11/54 M	54 M	1 M	110/480 M

DS-CDMA uses a sequence of Gaussian monocycle pulses which their spectrum is spread as in Fig. 1-1.The lower band occupies the spectrum from 3.1 to 4.85 GHz and the upper band occupies the spectrum from 6.2 to 9.7 GHz [2]. The 5-6 GHz band is dedicated to WLAN 802.11a systems.

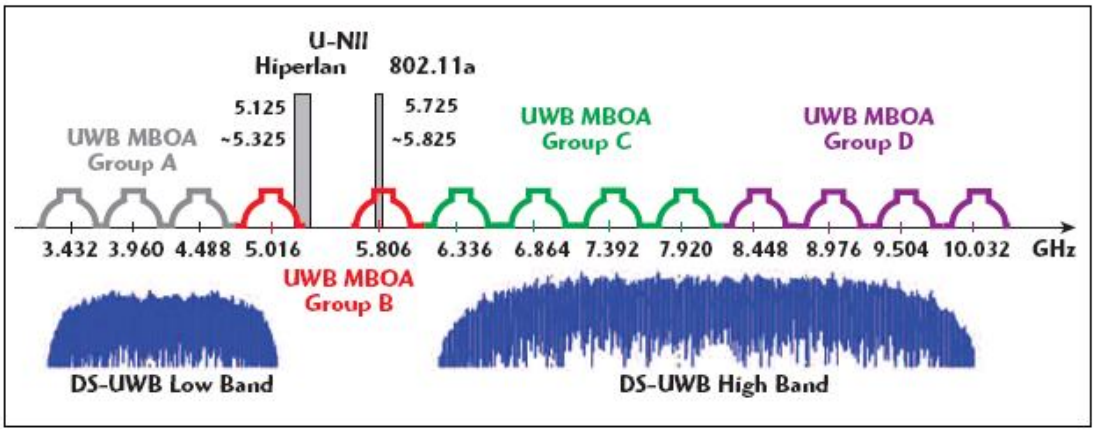


Fig. 1-1 DS-UWB spectrum allocation

See Fig. 1-2. In M-B-OFDM UWB, frequency span is grouped into five major band groups which are in turn sub-divided into 14 bands in total, each band is 528 MHz bandwidth [3].

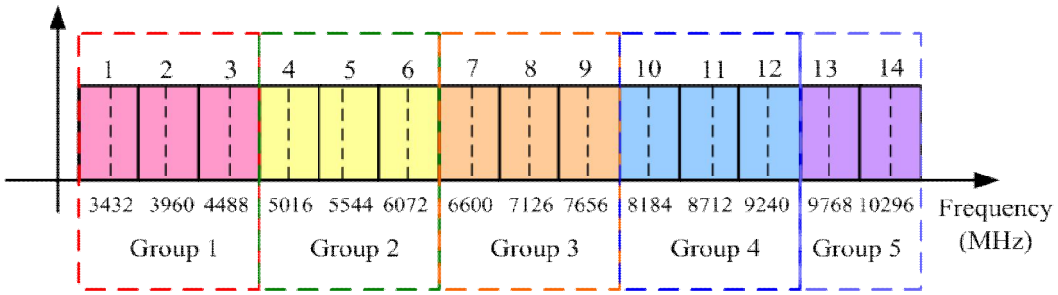


Fig. 1-2 Multi-band spectrum allocation

1.2 Thesis Organization

In this thesis, a quadrature voltage-controlled oscillator for WLAN 802.11a is implemented by using TSMC RF 1P6M 0.18 μm CMOS technology, and a very low-power QVCO operating at 10 GHz oscillation frequency has been proposed.

Chapter 2 will introduce a low-phase noise QVCO. In order to improve phase noise, we utilizing tail current-shaping technique and forward-body bias technique to decrease the phase noise.

Chapter 3 will propose a very low-power QVCO, which is a novel current-reused topology. We also utilized back-gate coupling technique not only to reduce the power dissipation but also to improve the phase noise.

Chapter 4 will give some discussions of these proposed QVCOs to compare the measured results with the simulation results and the references. A conclusion about this thesis is proposed in the end.

Chapter 2 Tail Current-Shaping Low-Phase Noise QVCO

2.1 Introduction

Phase-locked loop (PLL) circuits play a very important role in radio-frequency (RF) transceiver system. In order to generate a low phase noise local clock, the voltage-controlled oscillator (VCO) in the PLL circuit must be carefully designed. Therefore, the ways of improving the phase noise of VCO becomes a popular issue. In this paper, we proposed a novel tail current-shaping technique to reduce the VCO's phase noise.

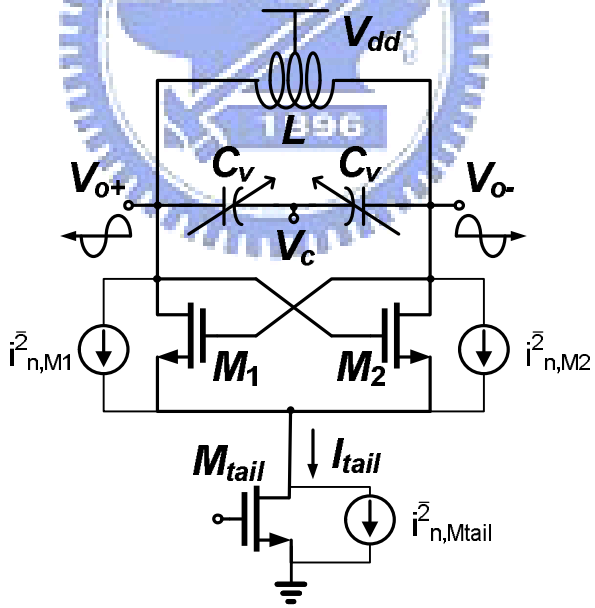


Fig. 2-1 Circuit schematic of a differential VCO

The main contributors to the phase noise of a conventional differential VCO, as shown in Fig. 2-1, are the cross-coupled devices(M_1 and M_2) and tail transistor(M_{tail}). $\overline{i^2_{n,M_1}}$ and $\overline{i^2_{n,M_2}}$ model the noise source of the cross-coupled devices, $\overline{i^2_{n,M_{tail}}}$ models the noise source

of the tail transistor. The low-frequency device noise can be up-converted to the high-frequency phase noise of the oscillator. Depending on the state of the oscillator, current noise present in these components is converted more efficiently into phase noise. Refer to the impulse sensitivity function (ISF) [4], the impact of any noise source on the oscillator phase noise varies across oscillation period. By shaping the tail current I_{tail}, we can decrease the active time of the noise source to reduce the oscillator phase noise. There are many tail current-shaping skills were proposed to reduce the device noise up-converting to VCO's phase noise, one method was brought up that is to couple the oscillating signal to the tail current source of VCO as an inductor, which will spend large chip area [5]. Another way of current-shaping is to input an additional pulse into the gate of tail transistor. However, it's not a convenient way to inject an additional pulse signal into our circuit, although the phase noise reduction of this manner had been mathematically proved [6].

Instead of generating an additional pulse as the injection signal or spending extra chip area, we build a quadrature VCO (QVCO) with two first-harmonic injection locked structure [7] and use the QVCO's own outputs signals as a self-injection signal to shape the tail current I_{tail}. This paper proposed a novel QVCO circuit implemented in the TSMC 0.18 μm CMOS 1P6M technology and operating at 5.3 GHz oscillation frequency. The quadra-phase outputs of the oscillator are coupled by 4 PMOS in series, and the tail current source injection signals come from the QVCO's outputs signals. We also use forward body bias (FBB) technique to reduce the supply voltage. Therefore, a tail current-shaping QVCO, which reaches low phase noise, can be obtained.

2.2 Circuit Design Consideration

2.2.1 Tail Current-Shaping Technique

A. the phase noise analysis of a conventional VCO

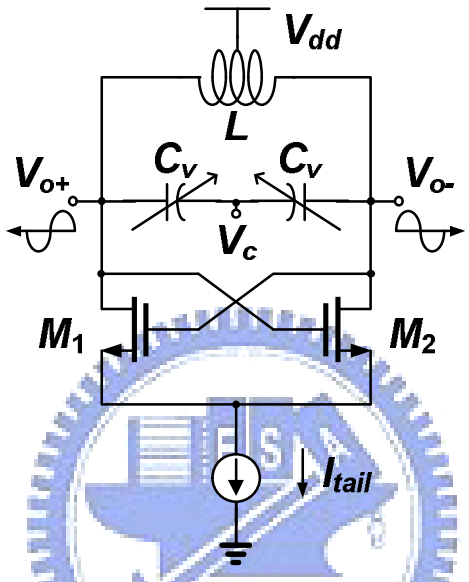


Fig. 2-2 Conventional cross-coupled VCO

Fig. 2-2 shows a conventional differential VCO. As mention in introduction before, the main contributors to the phase noise of this VCO are the cross-coupled devices (M_1 and M_2) and the tail current source (I_{tail}). It is because that the low-frequency device noise can be up-converted to the high-frequency phase noise of the oscillator. Because of the phase noise in the single-ended and the differential signals are identical, we therefore use a single-ended phase noise analysis to keep the equations simple. The thermal current noise power spectral density of transistor M_1 can be expressed as $\overline{i_{n0,M_1}^2}/\Delta f = 4kT\gamma g_{m0,M_1}$ when M_1 is conducting current, and it is close to zero when the transistor is OFF and highly resistive; g_{m0,M_1} is the transconductance of M_1, and γ is a coefficient related to device size.

The effective ISF of M_1 can be expressed as $\Gamma_{M_1,eff}(\boldsymbol{\varphi}) = \Gamma_{M_1}(\boldsymbol{\varphi})\boldsymbol{\alpha}(\boldsymbol{\varphi})$, where $\boldsymbol{\alpha}(\boldsymbol{\varphi})$ is the noise modulation waveform [4]. When $\Gamma_{M1} = \sin(\varphi)$ [8], the RMS value of the effective ISF becomes

$$\Gamma^2_{M1,eff,RMS} = \frac{1}{2\pi}\int_{-\pi}^{\pi}\Gamma^2_{M1}(\varphi)\alpha^2(\varphi)d\varphi = \frac{1}{2\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\sin^2\varphi d\varphi = \frac{1}{4} \qquad (1)$$

B. the phase noise analysis of a VCO with parallel capacitance to the tail transistor for current-shaping

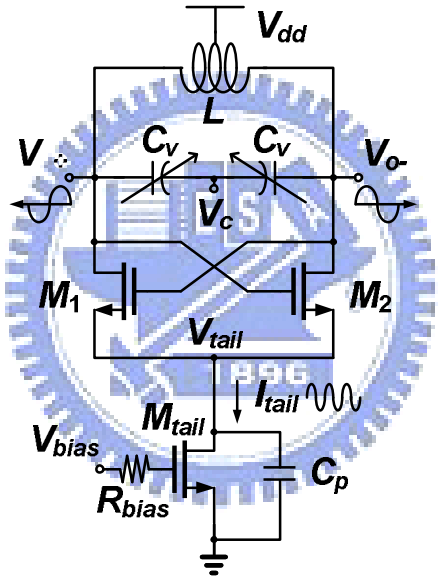


Fig. 2-3 Conventional cross-coupled VCO with a capacitance $\boldsymbol{C_p}$ which paralleled to the tail transistor $\mathbf{M_{tail}}$

Fig. 2-3 shows a conventional differential VCO with a NMOS tail current transistorM_{tail}. To improve the oscillator's phase noise, a capacitance C_p is connected with the tail transistor in parallel for the tail current-shaping. The voltage at the tail node will be a sinusoid of frequency$2\omega_o$, where ω_o is the oscillating frequency. Therefore, the tail current can be expressed as

$$I_{tail} = I_{bias} - 2\omega_o C_p A_s \sin(2\omega_o t - \theta) \quad (2)$$

I_{bias} is the DC value of the tail current, A_s is its amplitude, and $\boldsymbol{\theta}$ is its phase delay compared to the output voltage V_{o+} and V_{o-}. By designing the size of the devices, we can let $\theta = \pi/2$ and $2\omega_o C_p A_s = I_{bias}$ and the tail current will become

$$I_{tail} = I_{bias}(1 + \cos(2\omega_o t)) \quad (3)$$

With this sinusoidal signal, the power spectral density of the thermal current noise becomes $\overline{i_{n1}^2}/\Delta f = \left(\overline{i_{n0}^2}/\Delta f\right)\sqrt{2(1+\cos(2\varphi))} = \left(\overline{i_{n0}^2}/\Delta f\right)\alpha^2(\varphi)$, and the noise modulation function $\alpha^2(\varphi) = \sqrt{2(1+\cos(2\varphi))}$. Therefore, the RMS value of ISF of M_1 can be showed as

$$\Gamma_{M1,eff,RMS}^2 = \frac{1}{2\pi}\int_{-\pi}^{\pi} \Gamma_{M1}^2(\varphi)\alpha^2(\varphi)d\varphi$$

$$= \frac{1}{2\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \sin^2(\varphi)\sqrt{2(1+\cos(2\varphi))}d\varphi = \frac{2}{3\pi} \quad (4)$$

, which is about 15% smaller than (1). Therefore, up-conversion noise from cross-coupled device and tail current can be further reduced with the tail-current shaping technique [6, 9].

C. the proposed QVCO design

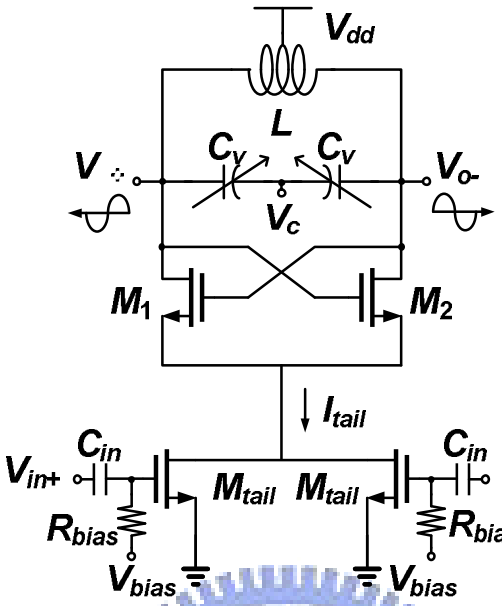


Fig. 2-4(a) First-harmonic injection-locked oscillator

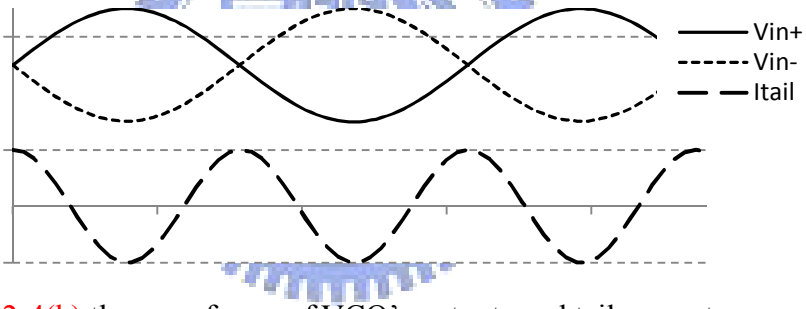


Fig. 2-4(b) the waveforms of VCO's outputs and tail current

Fig. 2-4

In this design, we propose a QVCO with a new tail current-shaping technique so as to improve the phase noise. The proposed QVCO is based on two first-harmonic injection-locked oscillators (ILOs) and utilize the QVCO's own output signals as a self-injection signal to shape the tail current.

Fig. 2-4(a) shows the ILO structure, the external injection signals V_{in+} and V_{in-} are injected into the gates of the tail current transistor pair M_{tail}. The ILO structure can be considered as a simple doubler, therefore, the tail current signal I_{tail} with frequency $2\omega_o$

can be obtained (ω_o is the oscillating frequency of the VCO). See Fig. 2-4(b), the sinusoidal tail current I_{tail} of $2\omega_o$ frequency is aligned with the zero-crossing point of the out-of-phase signals V_{in+} and V_{in-}.

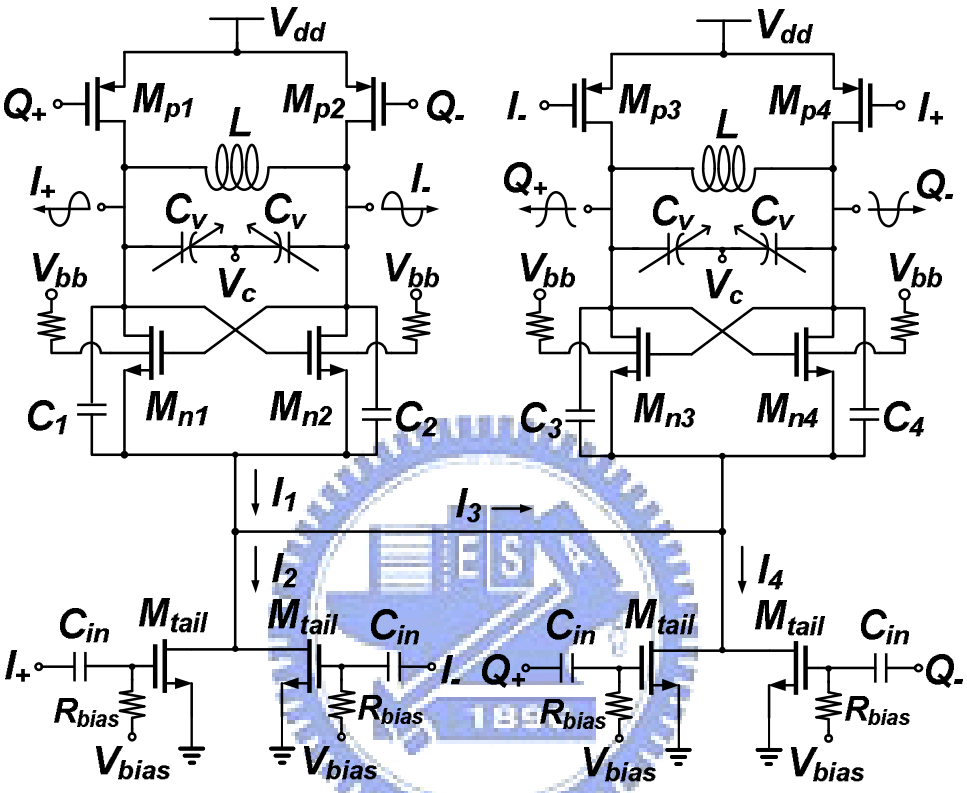


Fig. 2-5(a) the proposed QVCO with tail current-shaping

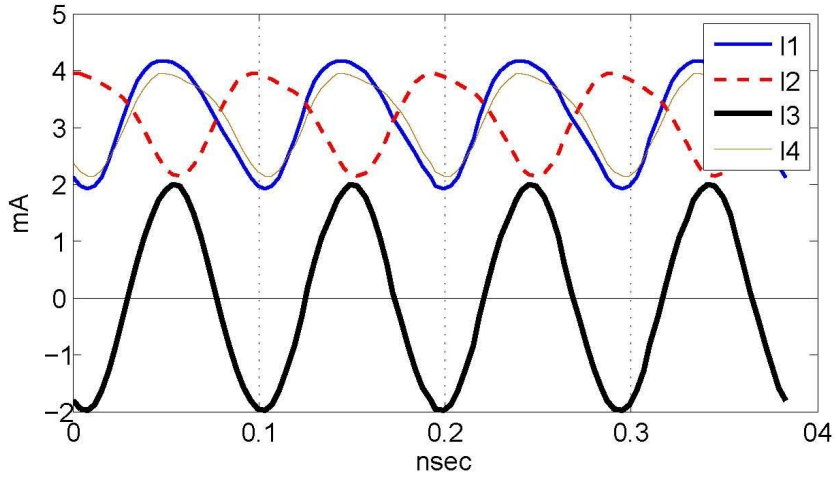


Fig. 2-5(b) the waveform of the tail currents

Fig. 2-5

Fig. 2-5(a) shows the proposed QVCO, the PMOS pairs (M_{p1} and M_{p2}, M_{p3} and M_{p4}) at the top of the circuit were used to couple the two ILOs in quadrature phase [10]. By injecting the quadra-phase outputs signals (I_+ and I_-, Q_+ and Q_-) back to the gates of the tail transistors M_{tail} as shown in Fig. 2-5(a), the tail currents of ILOs can be shaped at frequency $2\omega_o$ without external signals. However, the currents of tail transistor pairs I_2 and I_4 would have asymmetric waveforms, it is because of the parasitic capacitance at the drain of tail transistors. To eliminate the asymmetric phenomenon, the connection between two tail transistor pairs offers a path I_3 for tail currents switching. Fig. 2-5(b) shows the simulation result of the relationship between the tail currents I_1, I_2, I_3, and I_4. The waveforms of the currents I_2 and I_4, which pass through the tail transistor pairs, have out-of-phase relationship because of the quadrature phase injection signals I and Q. By the switching current I_3 between I_2 and I_4, the asymmetric phenomenon of I_2 and I_4 can be canceled by each other, therefore, a symmetric waveform can be obtained at the tail current I_1. The sinusoidal tail current I_1 of the ILO which is aligned with the zero-crossing point of I^+ and I^- can be expressed as

$$I_1 = I_{bias}(1 + \sin(2\omega_o t)) \tag{5}$$

In this proposed QVCO, the thermal current noise power spectral density of M_{n1} can be expressed as

$$\bar{i_{n1}^2}/\Delta f = (\bar{i_{n0}^2}/\Delta f)\sqrt{2(1+\sin(2\varphi))} = (\bar{i_{n0}^2}/\Delta f)\alpha^2(\varphi) \tag{6}$$

And the RMS value of effective ISF can be obtained as

$$\Gamma_{Mn1,eff,RMS}^2 = \frac{1}{2\pi}\int_{-\pi}^{\pi}\Gamma_{Mn1}^2(\varphi)\alpha^2(\varphi)d\varphi$$

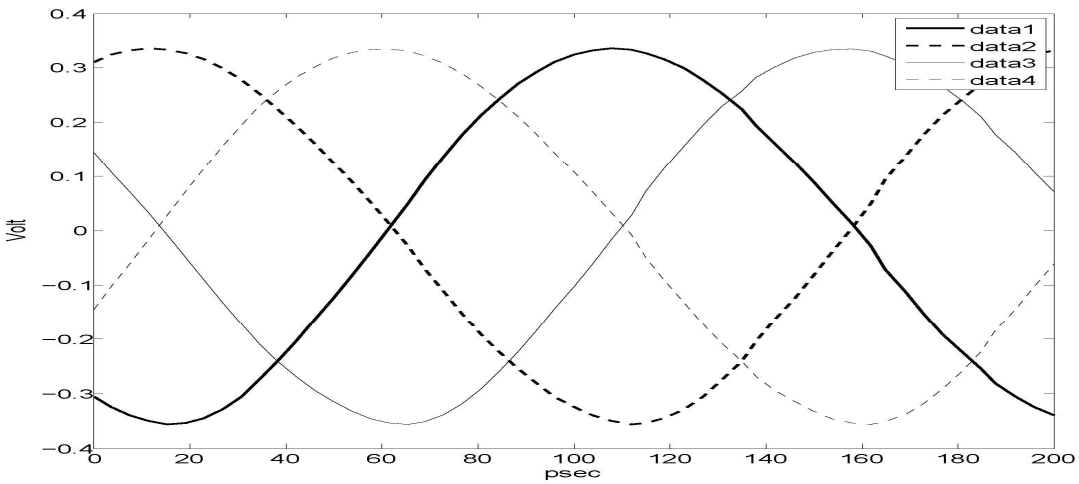
$$= \frac{1}{2\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\sin^2(\varphi)\sqrt{2(1+\sin(2\varphi))}d\varphi = \frac{\sqrt{2}}{3\pi} \tag{7}$$

, which is about 40% smaller than (1). By shaping the tail currents of ILOs, the phase noise contribution from the cross-coupled devices and tail transistors can be minimized. The ADS

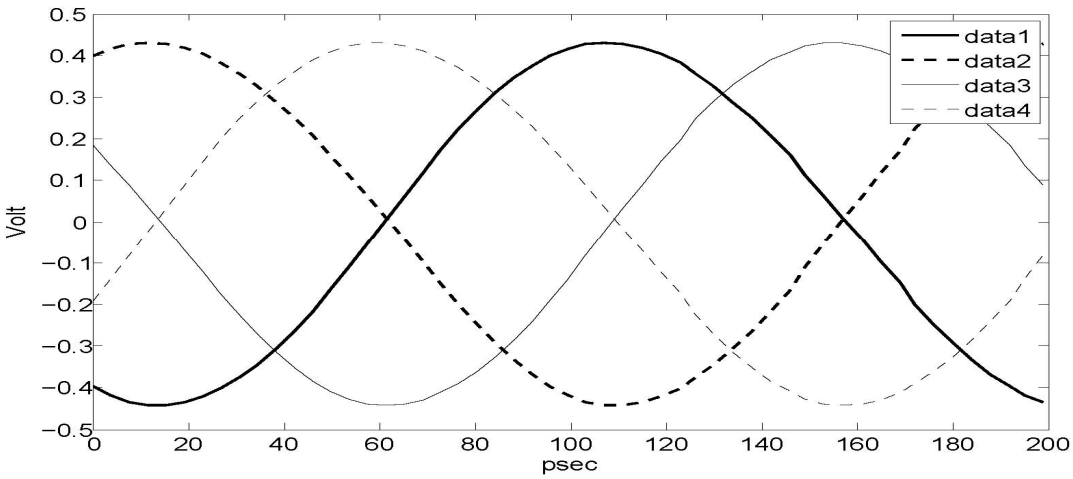
simulation results showed that the proposed QVCO's phase noise is -120 dBc/Hz @ 1 MHz offset frequency.

2.2.2 The LC Tank Design

In the design of the proposed QVCO's LC tank, we add 4 capacitances $C_1 \sim C_4$ as shown in Fig. 2-5(a) to increase the amplitude of the outputs waveform. The equivalent capacitance of the LC tank $C_{tank} = C_{var} + C_1$, and the oscillating frequency ω_o becomes $\frac{1}{\sqrt{LC_{tank}}}$.



(a) The outputs voltage waveform without $C_1 \sim C_4$



(b) The outputs voltage waveform with $C_1 \sim C_4$

Fig. 2-6

Fig. 2-6 shows the comparison of the outputs voltage waveform between the condition within and without the additional capacitances $C_1 \sim C_4$. The amplitude of the outputs waveform within $C_1 \sim C_4$ is 26% larger than the one without the additional capacitances. Fig. 2-7 shows the waveforms of the tail current I_1 in Fig. 2-5(a), and the amplitude of I_1 is a equation about $C_1 \sim C_4$ [11]. By adjusting the value of the additional capacitances $C_1 \sim C_4$, we made I_1 match to equation (5) to obtain better current-shaping effect, and the phase noise can also be improved as shown in Table 2-1.

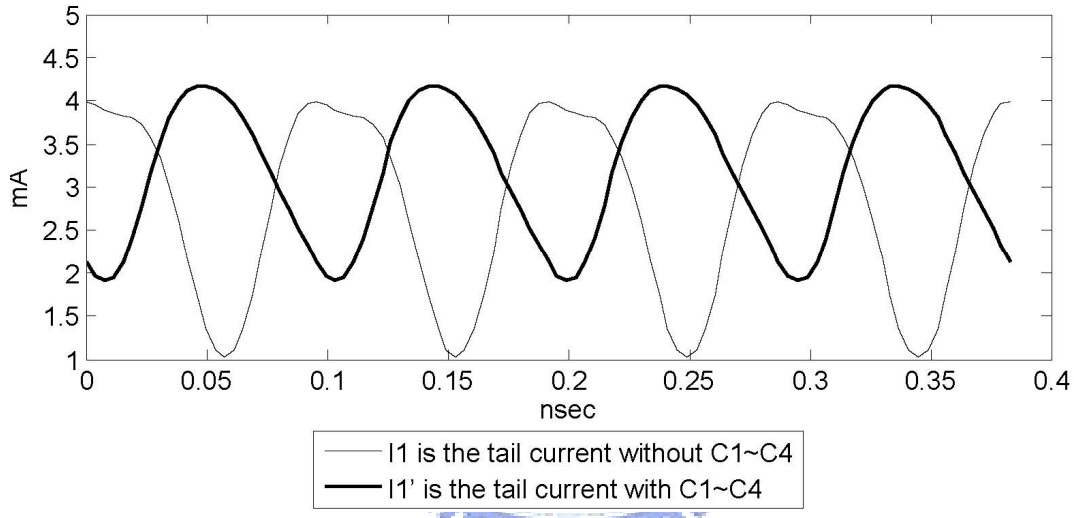


Fig. 2-7 the waveform of tail currents

Table 2-1 Comparison of additional capacitance

	Without $C_1 \sim C_4$	**Within $C_1 \sim C_4$**
Oscillating frequency	5.201GHz	5.218GHz
Outputs amplitude	0.691mV	0.871mV
Phase noise	-117dBc/Hz	-120dBc/Hz

2.2.3 Forward Body Bias

Considering the body effect, the threshold voltage V_t is no longer constant but influenced by the parameter of devices such as gate length, channel width, and body-to-source voltage V_{BS}. The threshold voltage V_t of the NMOS transistor is a function of V_{SB} as

$$V_t = V_{t0} + \left(\frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}}\right) * \left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}\right) \quad (8)$$

Where V_{t0} is the threshold voltage when $V_{SB} = 0$ V, N_A is the substrate doping, ε_s is a physical parameter with a typical value of 0.3 V, and C_{ox} is the parasitic capacitance at the gate oxide. By applying a forward body bias voltage to the body through a current-limiting resistor R_{bias}, a forward junction between body and source terminal appears. Therefore, we can adjust V_{SB} to change V_t and increase the current flow through the MOSFET [12]. Fig. 2-8 shows the simulated drain current of a NMOS, which has same size and operation condition with the NMOS M_{n1}~M_{n4} in the proposed QVCO as shown in Fig. 2-5(a).

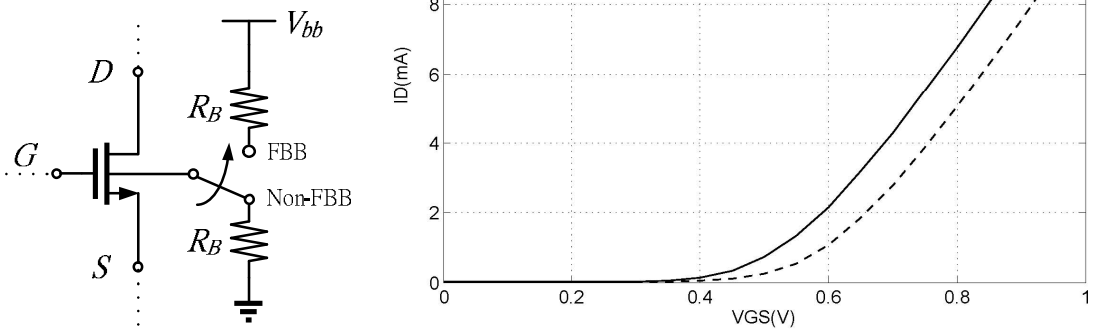


Fig.2-8 the IV curve of the MOSFET with and without FBB

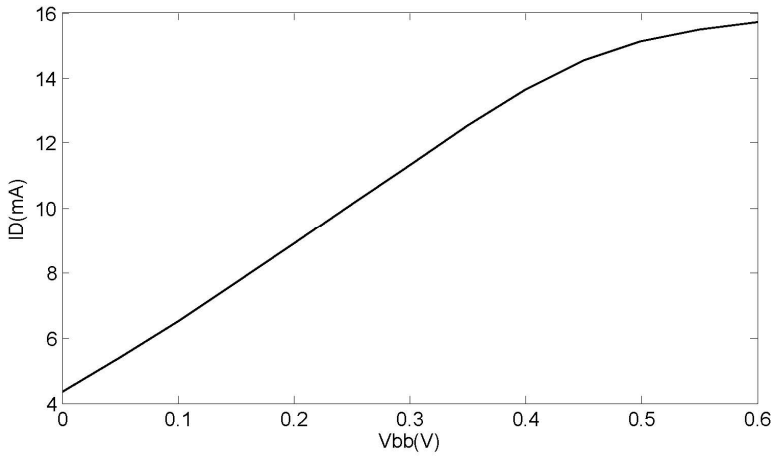


Fig. 2-9 Drain current of the MOSFET with FBB

In the proposed QVCO as shown in Fig. 2-5(a), bias voltages V_{bb} is used to the body of each cross-coupled NMOS FETs M_{n1}, M_{n2}, M_{n3}, and M_{n4} to increase the currents without higher V_{dd}. After all, we can achieve the operation current with lower V_{dd}.

2.3 Chip Layout and Simulation Results

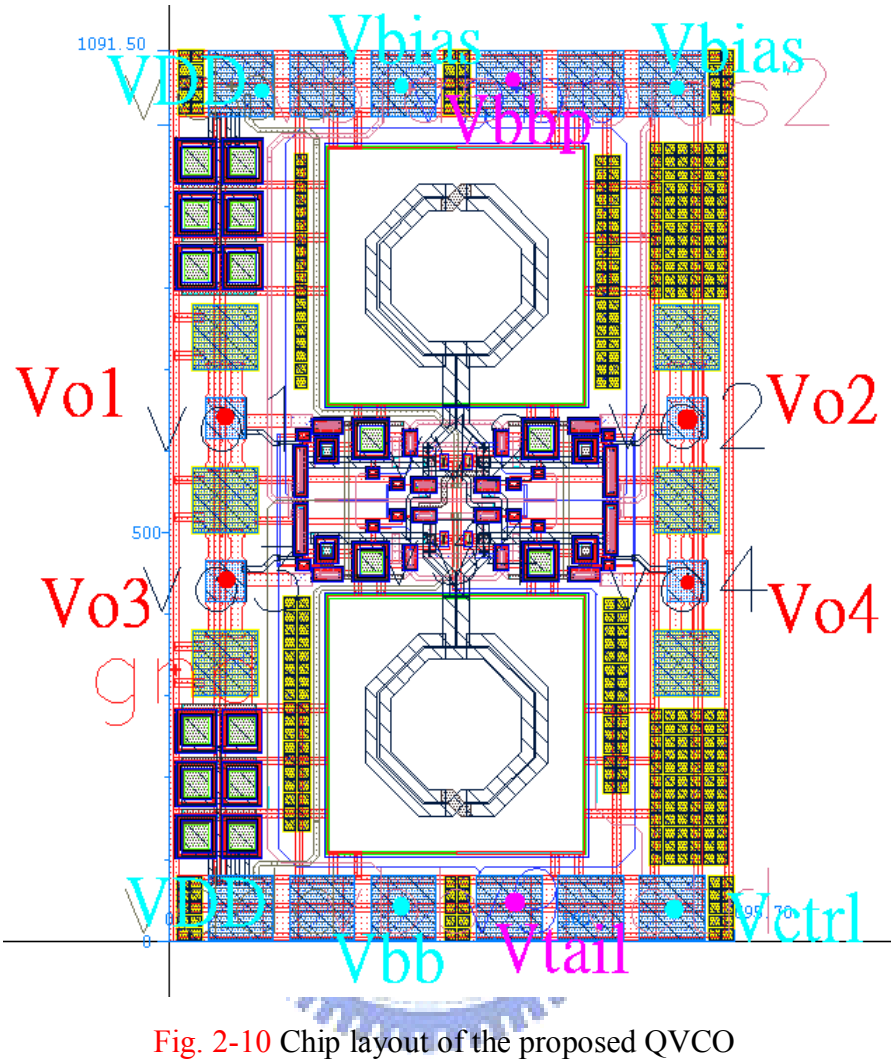


Fig. 2-10 Chip layout of the proposed QVCO

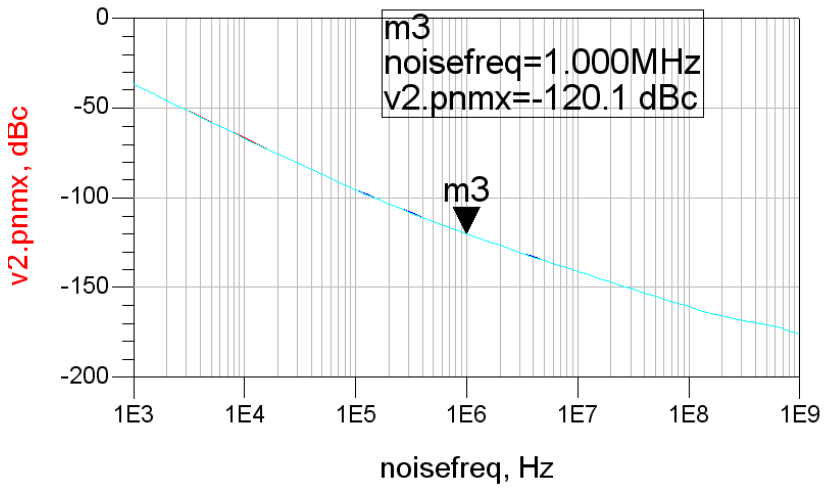


Fig. 2-11 the phase noise of the proposed QVCO

Fig. 2-10 shows the chip layout's photograph of the proposed QVCO, which designed and processed by TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The chip area is 0.7*1.1 mm^2 including all pads and bypass capacitances, and each buffer of the quadrature outputs were designed as a common-drain voltage follower. The ADS simulation results is shown in Fig. 2-11, Fig. 2-12, and Fig. 2-13. The oscillating frequency of the QVCO is 5.22 GHz, and the phase noise is-120.1 dBc/Hz @ 1 MHz offset frequency. As the tuning voltage V_{ctrl} raising from 0 V to 3 V, the tuning range of the QVCO is about 120 MHz from 5.22~5.34 GHz. In Fig. 2-13, the outputs voltage waveform with the peak-to-peak voltage is about 0.87 V, and the phase error $< 2^o$. The QVCO core circuit draws 4.56 mA from a 1.4 V supply.

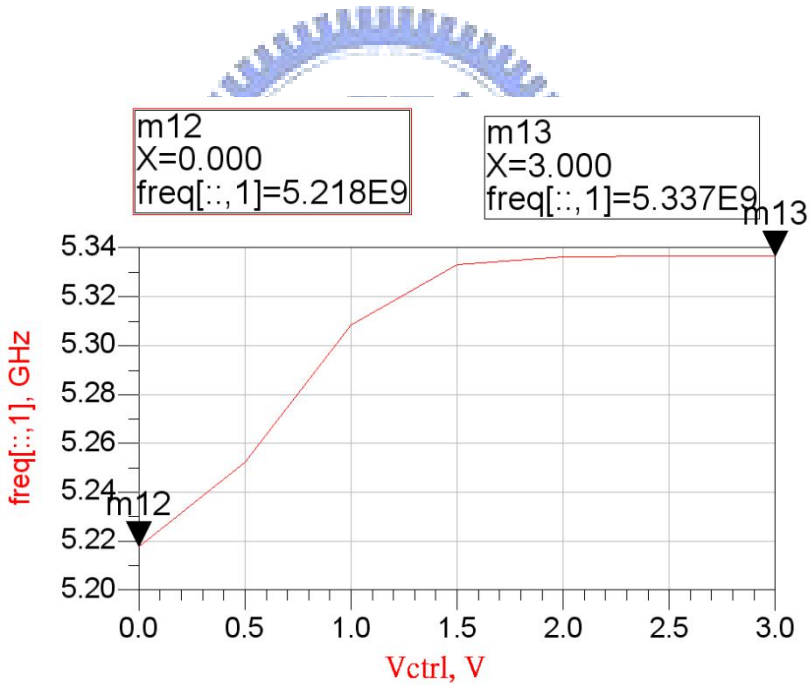


Fig. 2-12 Tuning range of the proposed QVCO

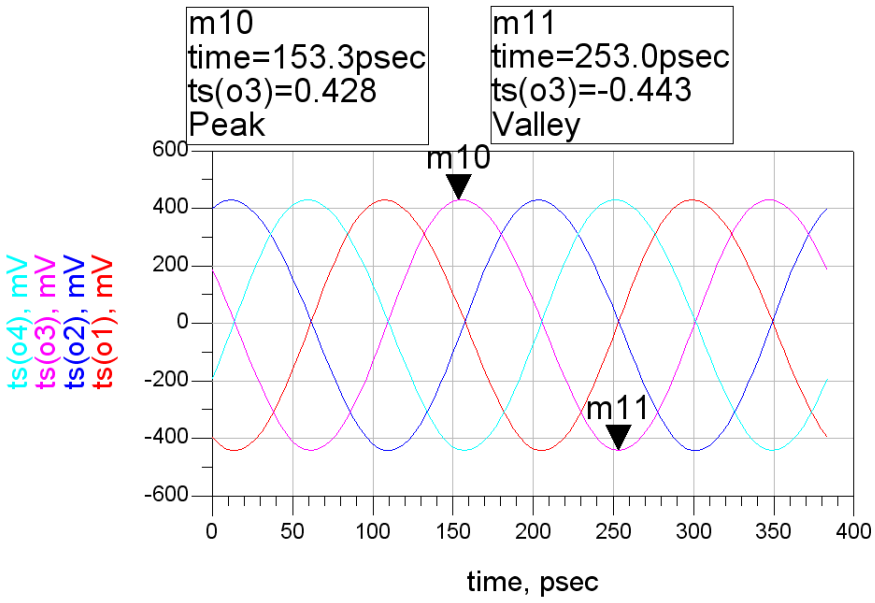


Fig. 2-13 the outputs waveform of the proposed QVCO

To take all performance into account, the figure-of-merit (FOM) is expressed as

$$\boldsymbol{FOM}(\Delta\boldsymbol{\omega}) = -\boldsymbol{\mathcal{L}}(\Delta\boldsymbol{\omega}) + 20\,\boldsymbol{log}\left(\frac{\boldsymbol{\omega_o}}{\Delta\boldsymbol{\omega}}\right) - 10\,\boldsymbol{log}(\boldsymbol{P}) \qquad (9)$$

where $\boldsymbol{\omega_o}$ is the oscillating frequency, $\Delta\boldsymbol{\omega}$ is the offset frequency, and $\boldsymbol{P}$ is the power consumption (in mW) of the QVCO. The FOM of the proposed QVCO is about 186 @ 1 MHz offset frequency.

Table 2-2 QVCO simulated performance in different corner condition

corner	TT	FF	SS
Tuning Range (GHz)	5.22~5.34GHz	5.13~5.2GHz	5.12~5.17GHz
Phase Noise (dBc/Hz)	-120@1MHz	-115@1MHz	-108@1MHz
Core Power	6.384mW	10.78mW	3.612mW

2.4 Measurement Results and Discussion

2.4.1 Measurement Consideration

The proposed QVCO are designed for on-wafer testing, and the DC voltage are supplied by two sets of six-pin probe, so that the distance between each DC pad must more than 50 μm to satisfy the probe testing rule. The outputs buffer of each quadrature outputs voltage is designed using common-drain voltage follower, and the source end of each buffer MOSFET is connected to a RF pad. For measurement, we connect four bias-tee terminals to the corresponding RF pads as shown in Fig. 2-14.

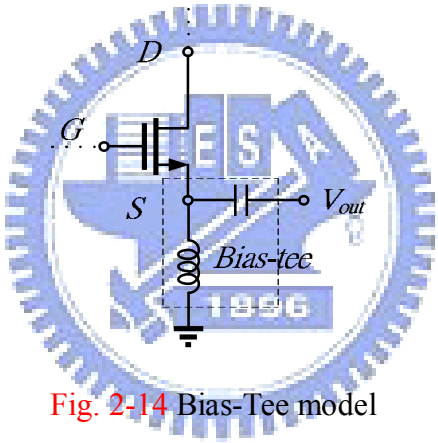


Fig. 2-14 Bias-Tee model

The phase noise, tuning range and outputs spectrum are measured using signal source analyzer (Agilent E5052A) and down-converter (Agilent E5053A) shown in Fig. 2-15.

(a)SSA(Agilent E5052A) (b)down-converter(Agilent E5053A)

Fig. 2-15

2.4.2 Measurement Result

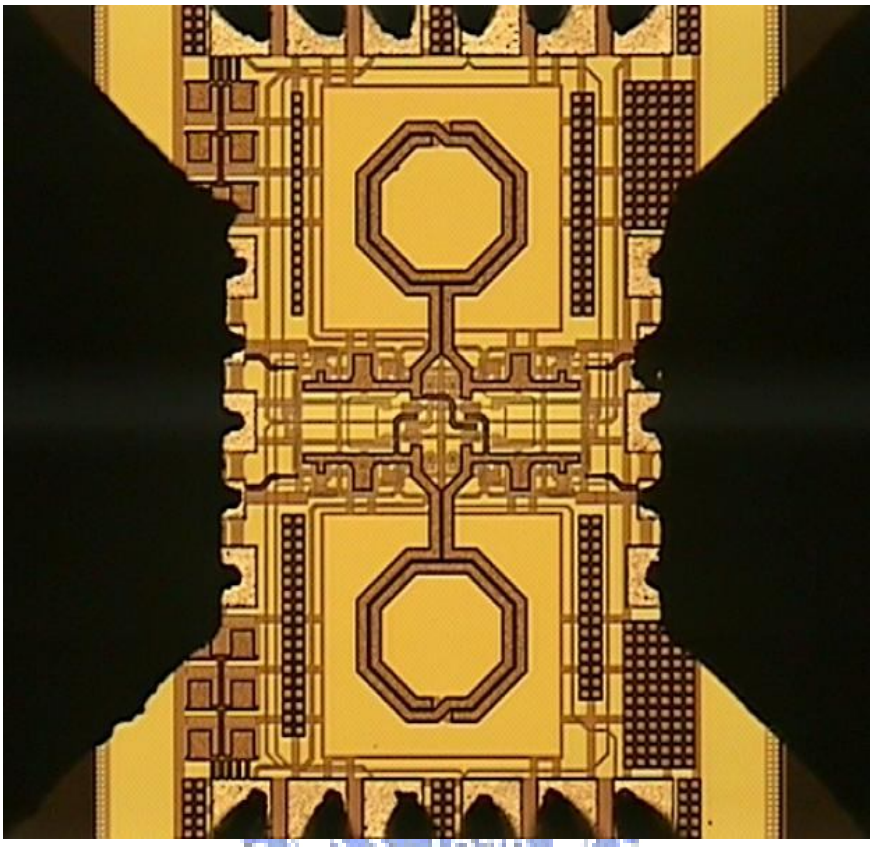


Fig. 2-16 Chip photo of the proposed QVCO

Fig. 2-16 is the chip photograph of the proposed current-shaping QVCO. According to the figures below, this QVCO oscillates at 5.28 GHz and the output power is -5 dBm. The measured phase noise is -119.3 dBc/Hz @ 1 MHz offset frequency, and the tuning range is about 140 MHz since 5.3 GHz ~ 5.44 GHz. Fig. 2-20 also shows the measured outputs voltage waveform, because of the phase delay and loss of the cable line and connector, the phase error is about 7^{o}~15^{o}. After all, the power consumption of the implemented QVCO is about 11.2 mW, and the FOM is around 183 @ 1 MHz offset frequency.

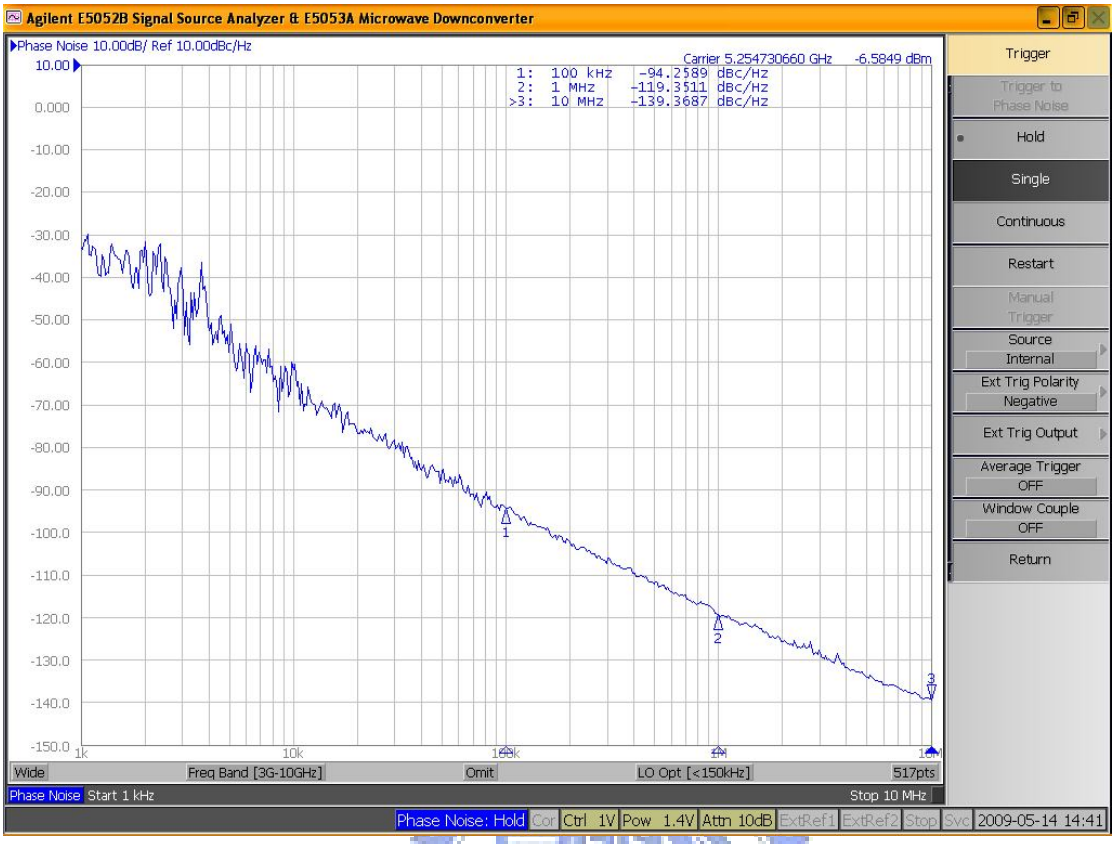


Fig. 2-17 the measured phase noise of the proposed QVCO

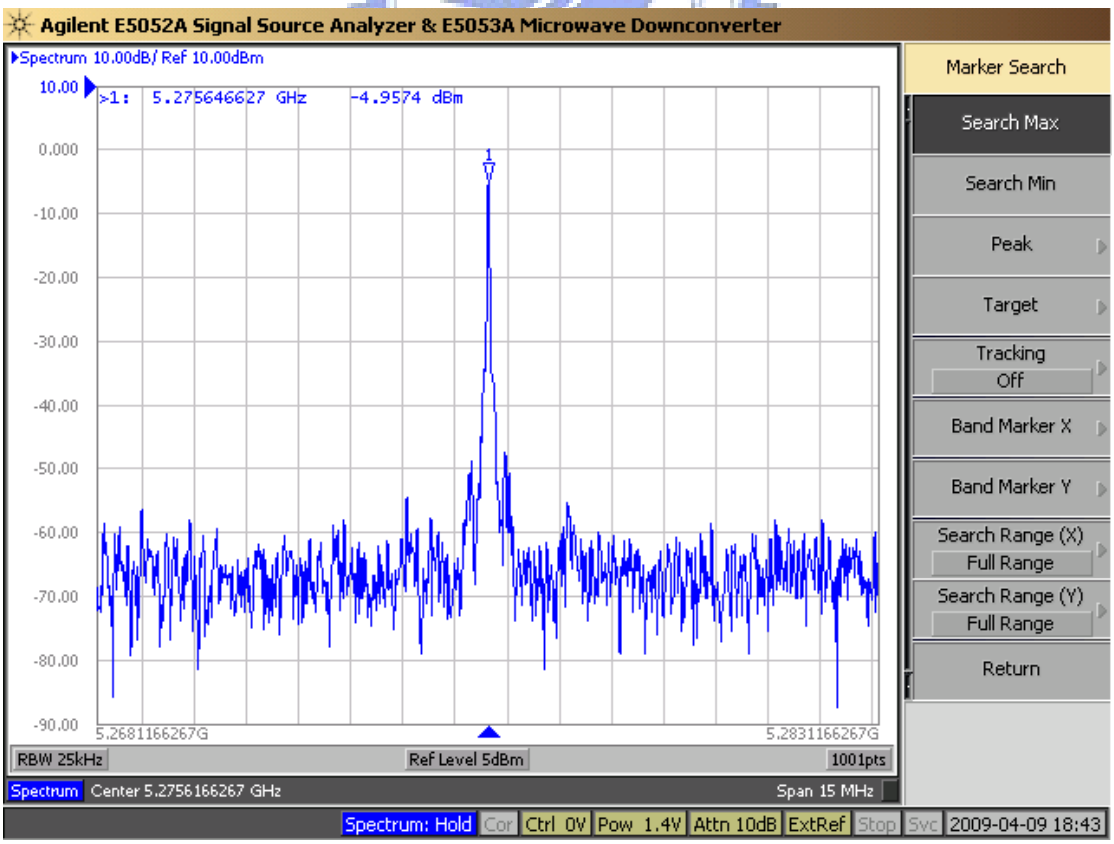


Fig. 2-18 the outputs spectrum of the proposed QVCO

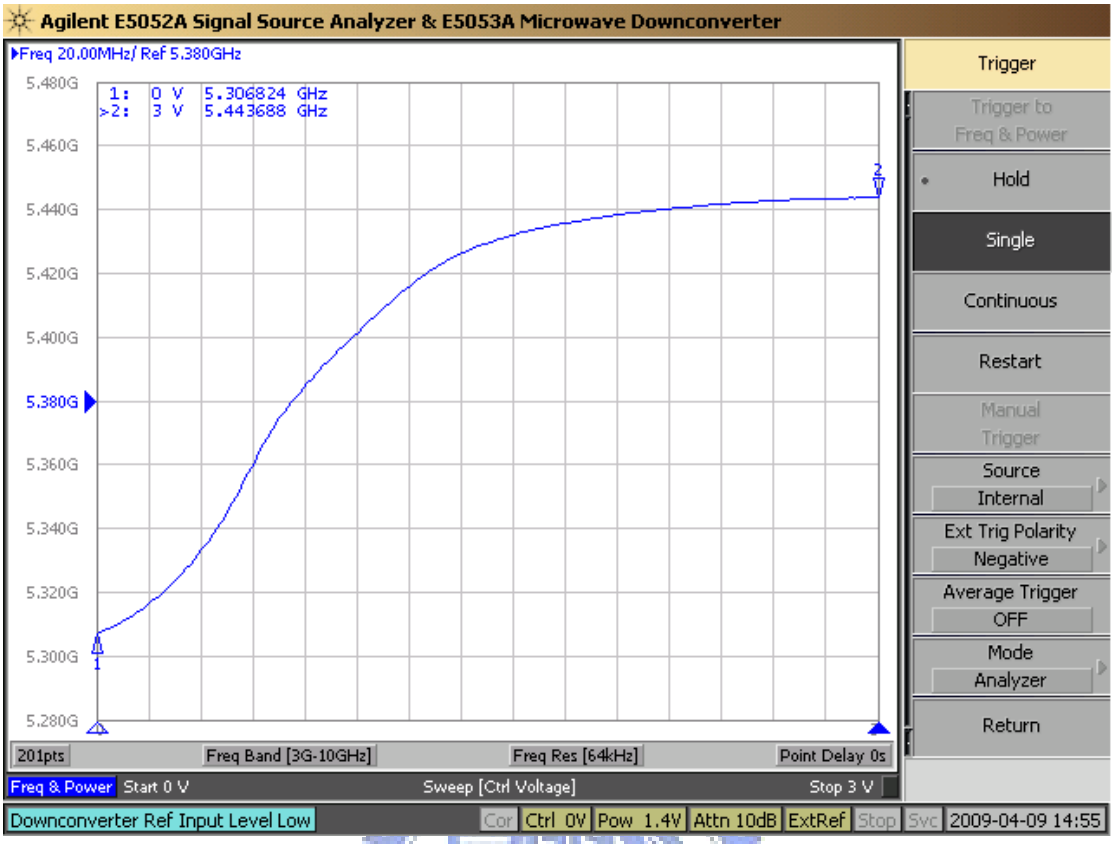


Fig. 2-19 the tuning range of the proposed QVCO

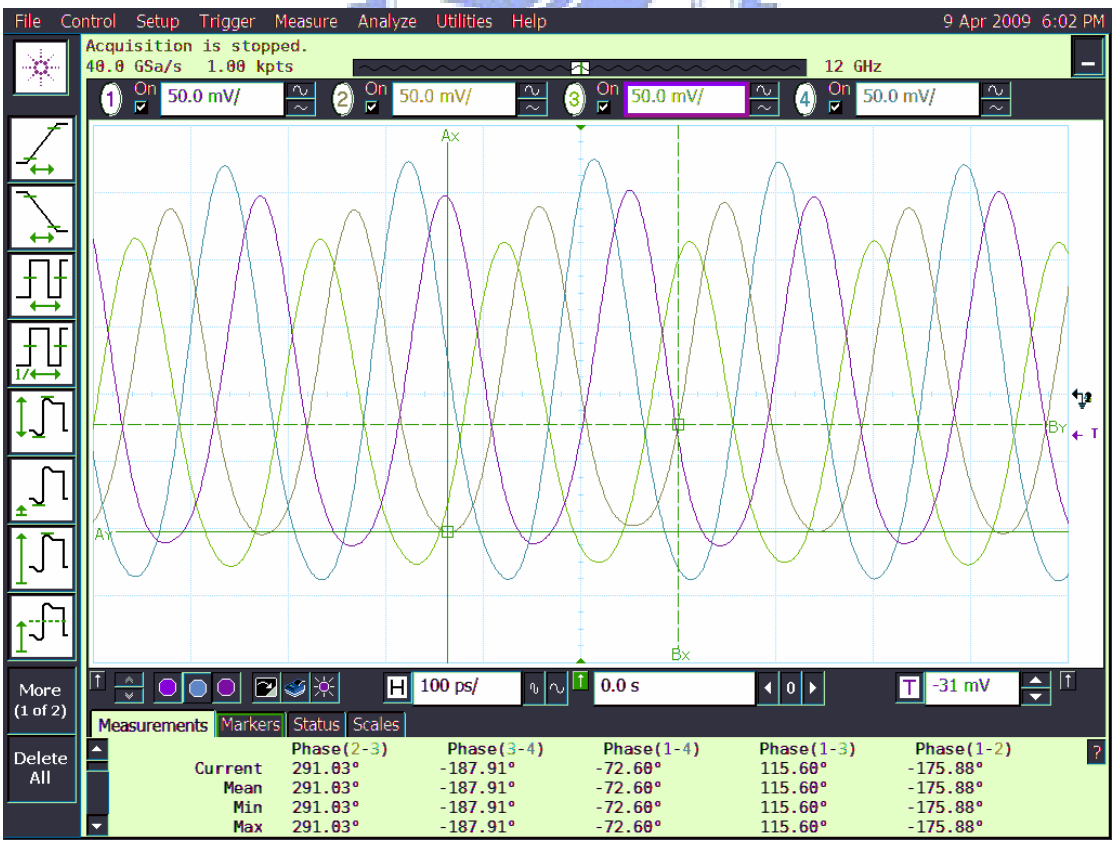


Fig. 2-20 the outputs voltage waveform of the proposed QVCO

Table 2-3 comparison between simulation and measurement

performance	Post-simulation	Measurement
Supply voltage	1.4 V	1.4 V
Tuning range	5.22 ~ 5.34 GHz	5.3 ~ 5.44 GHz
Phasenoise@1MHz	-120 dBc/Hz	-119 dBc/Hz
Power consumption	6.384 mW	11.2 mW
Output power	0 dBm	-5 dBm
FOM	-186	-183

Table 2-4 comparison between this work and references

performance	This work	[13]	[14]
Oscillation frequency	5.3 GHz	5 GHz	3.6 GHz
Phase noise@1MHz	-119 dBc/Hz	-118 dBc/Hz	-114 dBc/Hz
Power consumption	11.2 mW	16.5 mW	8 mW
FOM	-183	-180	-176

Chapter 3 Current-Reused QVCO

3.1 Introduction

Recently, due to the demand for the low-power, low-cost, and highly integrated transceiver, many research have focused on the low-power voltage-controlled oscillator (VCO) design. There are various ways to reduce the power consumption of the VCO, and the most common method is reusing the dc currents of the devices[15-17]. In our design, we proposed a current-reused topology to stack the switching transistors of the VCO vertically. Therefore, the dc current drew by the oscillator core can be cut in half of the conventional VCO as sown in Fig. 3-1.

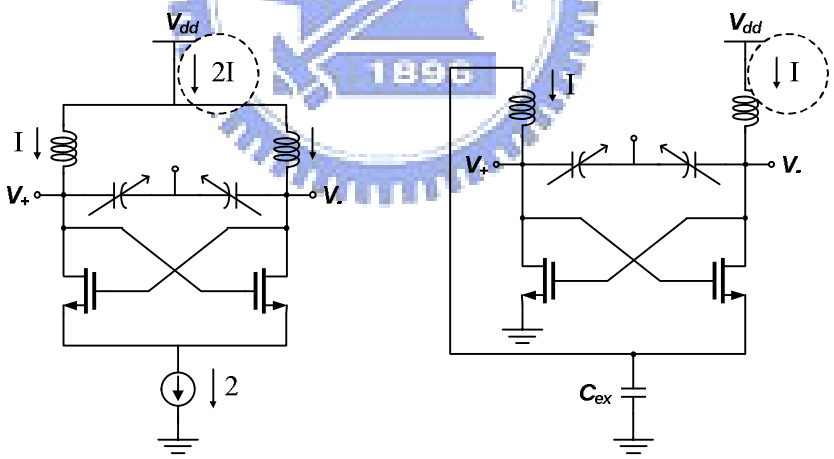


Fig. 3-1 (a) the conventional VCO (b) the current-reused VCO

According to most of the modern wireless communication standards require quadrature modulation, accurate quadrature generations in the VCOs is required. For quadrature signals, in-phase (I) and quadrature-phase (Q) match is an important requirement while meeting the requirements of low-phase noise and low-power for integrated VCOs. The quadrature

characteristics can be evaluated in terms of phase error and amplitude imbalance. There are several ways to couple two VCOs in quadrature phase[10, 18]. One common quadrature VCO (QVCO) topology is utilizing the parallel coupling transistors[19], which consumes large current to bias both the switching and coupling transistors. In order to reduce the power consumption, we couple two current-reused VCOs by back-gate coupling technique[20]. We first assume all switching transistors are in different wells, so that each transistor can be used as full four-terminal device. Therefore, the output signals of one VCO can be coupled to the back-gate of the switching transistors of the other VCO. A low-power QVCO without requiring additional coupling transistors can be obtained.

3.2 Circuit Design Consideration

A. Current reused differential VCO

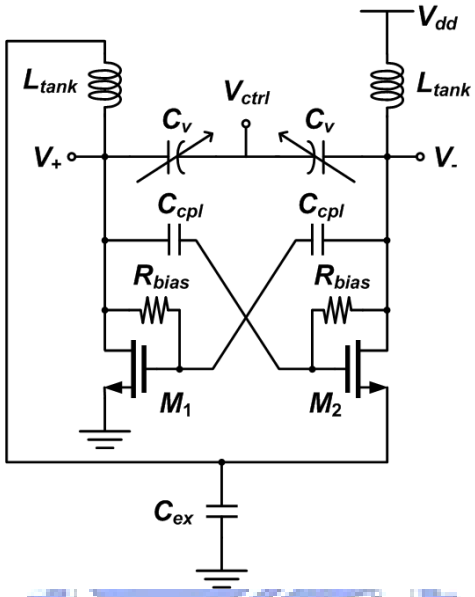


Fig. 3-2 the current reused differential VCO

Fig. 3-2 shows the topology of a current reused differential VCO for low-power consumption application[21]. For dc operation, the switching NMOS M_1 and M_2 are stacked vertically, therefore the dc current of M_1 and M_2 can be reused. The resistors R_{bias} are adopted for diode connection of M_1 and M_2 to ensure M_1 and M_2 are both operating in active region. For constituting a differential VCO in ac operation, the external capacitor C_{ex} is for ac ground and the capacitors C_{cpl} are adopted for ac coupling. The LC tank of the VCO is composed of L_{tank} and varactor C_v. Therefore, a low-power consumption differential VCO can be obtained.

B. the proposed current reused QVCO with back-gate coupling

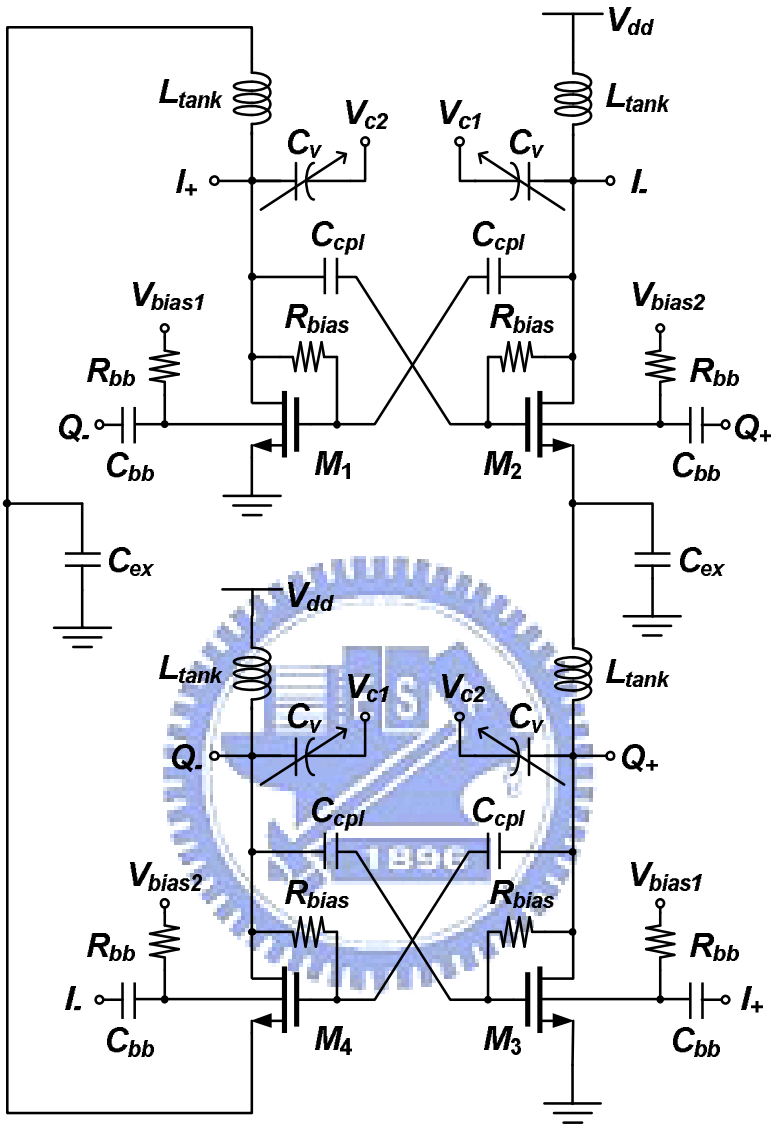


Fig. 3-3(a) the proposed current reused QVCO

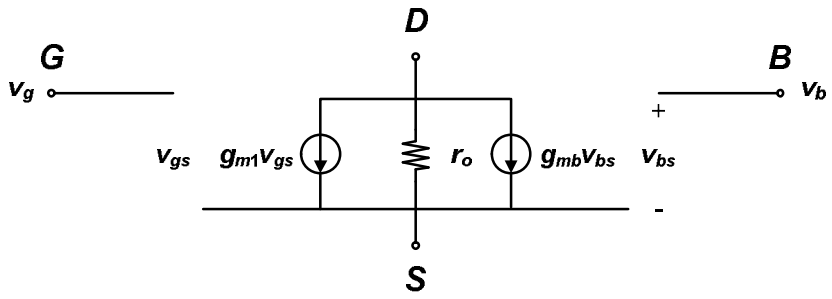


Fig. 3-3(b) the small signal equivalent circuit of switching transistor M_1

In Fig. 3-3(a), we proposed a quadrature VCO with the same idea of current reused topology as mentioned before. For reusing the dc current, the switching transistors M_2 and M_3 are stacked vertically, and M_1 and M_4 are stacked vertically, too. The coupling capacitors C_{cpl} are both for ac coupling and dc blocking, therefore, the differential outputs I_+ and I_-, Q_+ and Q_- can be generated. Because of the dc voltages at the drain of M_1, M_2, M_3, and M_4 are different, we utilize the resistors R_{bias} for diode connection to ensure all switching transistors are operating in active region. The LC tank are designed with L_{tank} and C_v. Since the dc voltages are different between two differential output nodes, the control voltages of the varactors were supplied as V_{c1} and V_{c2} separately. The I and Q signals of the proposed QVCO are generated by coupling two differential VCOs through C_{bb} to the back-gate of the switching transistors M_1-M_4. For back-gate coupling[20], V_{bias1} and V_{bias2} bias the body voltages of M_1-M_4 for different condition through resistors R_{bb}, and C_{bb} is the coupling capacitors to couple the output signals in quadrature phase. The external capacitors C_{ex} have large value to have tight ground effects for ac currents. Therefore, the power consumption of the proposed QVCO can be cut in half by reusing the dc currents compared to the conventional QVCO topologies.

C. back-gate coupling

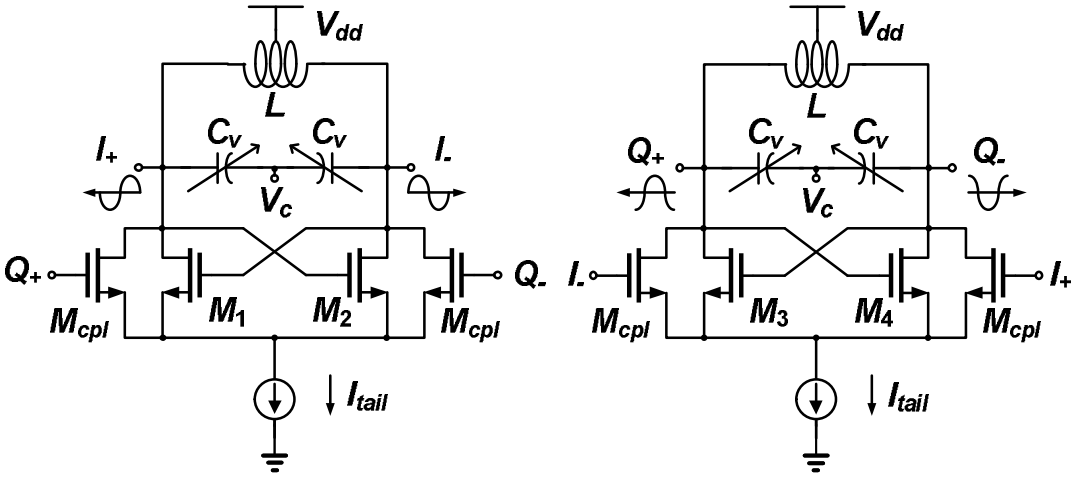


Fig. 3-4(a) a conventional parallel-coupled QVCO

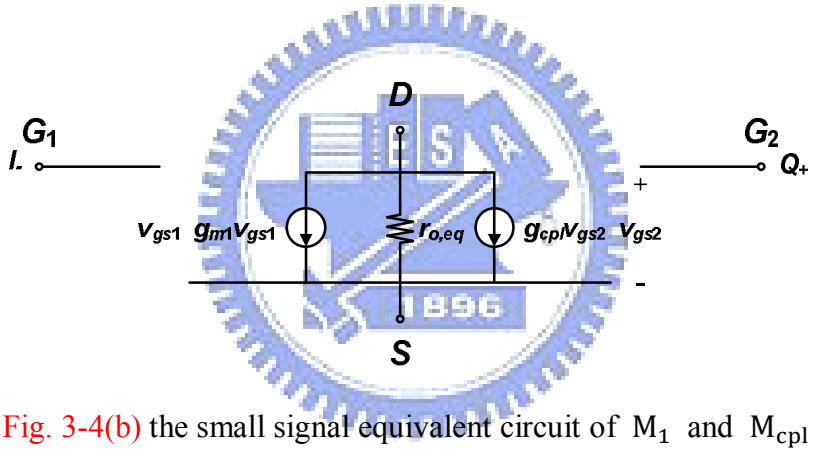


Fig. 3-4(b) the small signal equivalent circuit of M_1 and M_{cpl}

Fig. 3-4(a) shows a conventional parallel- coupled QVCO (P-QVCO) where the I and Q signals are generated by coupling two differential VCOs through coupling transistors M_{cpl} in parallel with the switching transistors M_1-M_4. Because of the differential pair circuits M_1-M_2 and M_3-M_4 are symmetric, we use a single-ended analysis to make the analysis simple. Fig. 3-4(b) shows the small signal equivalent circuit of the switching transistor M_1 and corresponding coupling transistor M_{cpl}. The coupling strength α of the P-QVCO can be defined as[22]

$$\alpha = \frac{g_{cpl}}{g_{m1}} = \frac{W_{cpl}}{W_{m1}} \qquad (3-1)$$

where g_{cpl} is the transconductance and W_{cpl} is the width of the coupling transistor $\mathrm{M_{cpl}}$, and g_{m1} and W_{cpl} are the transconductance and width of the switching transistor $\mathrm{M_1}$. The phase noise degradation of the P-QVCO is induced by the increase in transconductance of the coupling transistors. On the other hand, the phase error is reduced while α increasing as the increase in g_{cpl}. Therefore, a trade-off between phase noise and phase error occurs. In addition, the coupling transistors lead a higher power consumption of the QVCO.

Fig. 3-3(b) shows the small signal equivalent circuit of the switching transistor $\mathrm{M_1}$ in Fig 3-3(a). The coupling strength α_{B} through the back-gate can be given by[22]

$$\alpha_{\mathrm{B}} = \frac{g_{mb}}{g_{m1}} = \frac{\gamma}{2\sqrt{2\Phi_{\mathrm{F}} - \mathrm{V_{BS}}}} \qquad (3-2)$$

Where γ is the body effect coefficient, Φ_{F} is the work function, and $\mathrm{V_{BS}}$ is the back-gate (body) to source bias voltage. Therefore, we can increase α_{B} by minimizing the body-to-source reverse bias $\mathrm{V_{BS}}$ in order to reduce the phase error without additional power consumption.

In our design, by reusing the dc currents of switching transistors, the power consumption of the proposed QVCO shown in Fig. 3-3(a) can be half of the conventional QVCO. Low phase noise and phase error can also be obtained without higher power consumption by back-gate coupling to generate the I and Q signals.

3.3 Simulation Results

The ADS simulation results of the proposed current-reused QVCO are shown in Fig. 3-5 ~ Fig. 3-8. The proposed QVCO operates at 9.98GHz oscillating frequency, and the phase noise is -112 dBc/Hz @ 1 MHz offset frequency. The total power consumption is 1.64 mW since the QVCO core circuit draws 1.37 mA from a 1.2 V V_{dd} supply. As the tuning voltages V_{c1} and V_{c2} raising from 0 V to 3 V and 0.6 V to 3.6 V, the tuning range of the QVCO is about 4 GHz from 9.98~13.97 GHz. Fig. 3-7 shows the time domain voltage waveform at the output nodes. Fig. 3-8 shows the output voltages waveform through a dc blocking capacitor, and the phase error of the proposed QVCO $< 0.2^{o}$. The FOM of the proposed QVCO is about 189.6 @ 1 MHz offset frequency.

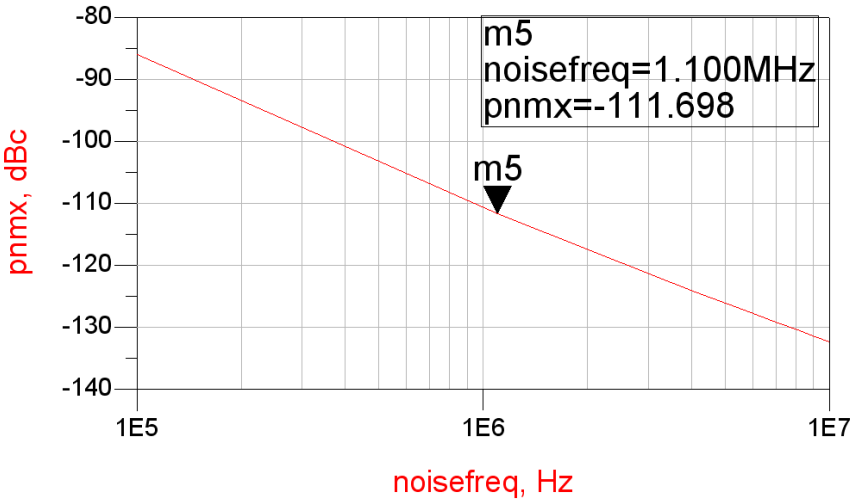


Fig. 3-5 the simulated phase noise of the proposed QVCO

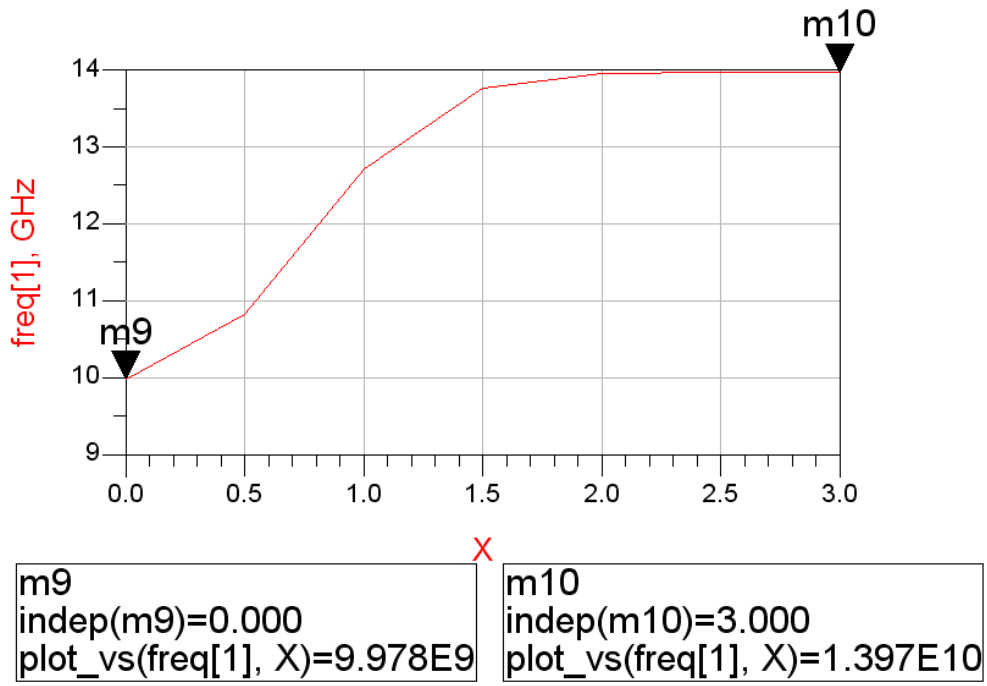


Fig. 3-6 the simulated tuning range of the proposed QVCO

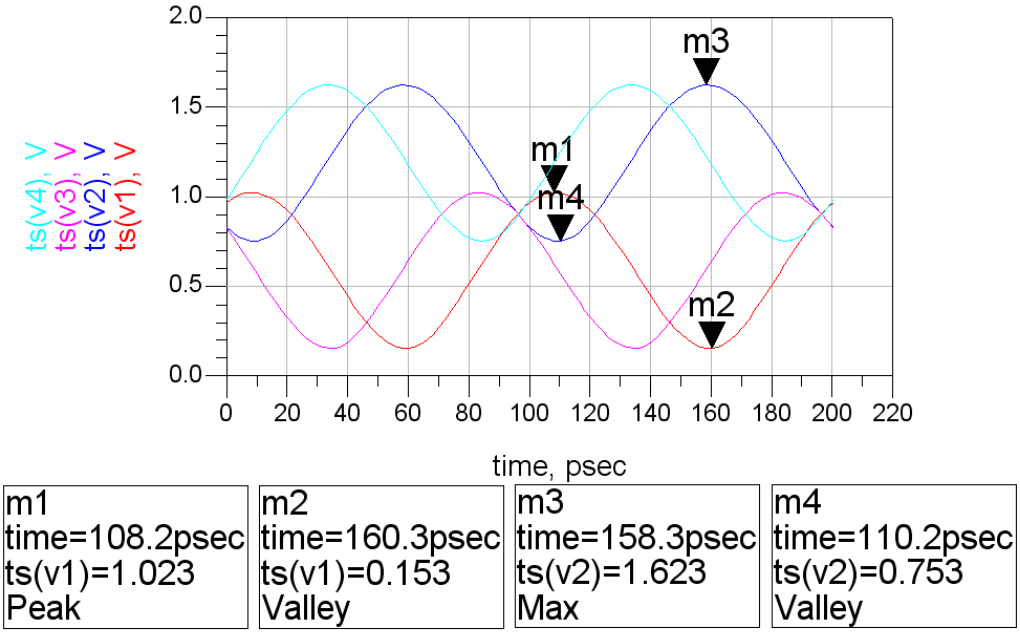


Fig. 3-7 the outputs voltage waveform

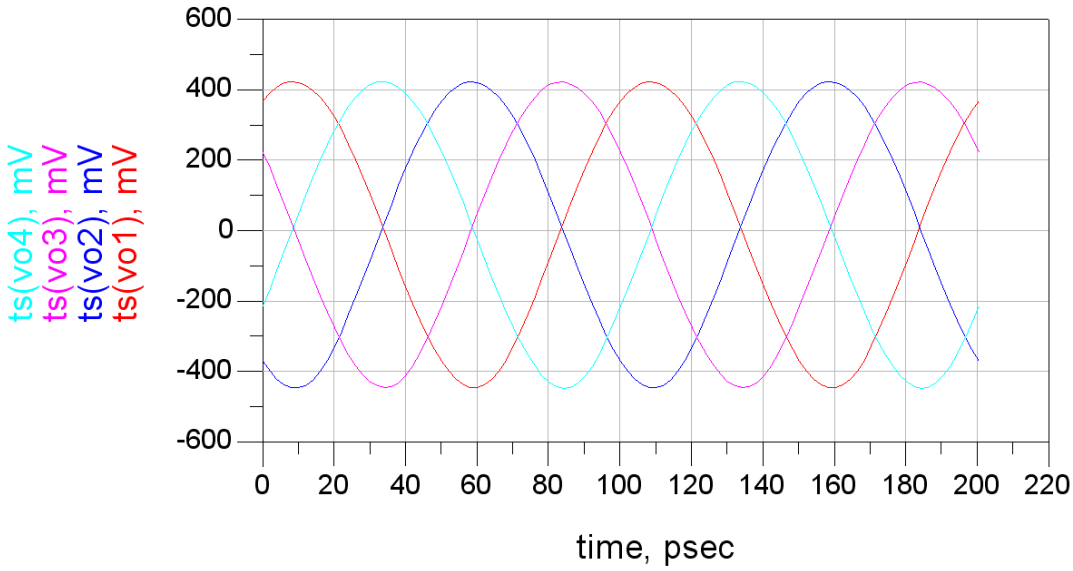


Fig. 3-8 the outputs voltage waveform through dc blocking capacitors

Table 3-1 the comparison between the proposed QVCO and references

	This work(sim)	**[20]**	**[21]**
Tuning Range (GHz)	9.98~13.97GHz	1.047~1.39GHz	3.0~3.2GHz
Phase Noise (dBc/Hz)	-111@1MHz	-120@1MHz	-102
Core Power	1.64mW	5.4mW	4.32mW
FOM(dBc)	-189.6	-173.5	-166

Chapter 4 Conclusion

4.1 Simulation Results

In chapter 2, a low-phase noise QVCO utilizing tail current-shaping technique has been proposed. The low-phase noise QVCO is base on two first-harmonic injection-locked oscillators. In order to reduce the phase noise, we inject the output signals of the proposed QVCO back to its tail transistors and shape the tail currents. With this tail current-shaping technique, the RMS value of the impulse sensitivity function (ISF) of the proposed QVCO can be reduce to only 60% of the conventional one. The LC tank of the proposed QVCO has also been designed so as to increase the output amplitude, and the forward-body-bias technique is used to maintain the dc current without higher voltage supply. The measured results are shown in chapter 2.4, the phase noise is -119 dBc/Hz @ 1 MHz offset and the oscillation frequency of the QVCO is 5.28 GHz. The power consumption is 11.2 mW of 1.4 V supply voltage.

In chapter 3, we proposed a low-power QVCO by utilizing a novel current-reused topology. In order to reduce the power consumption, we not only reuse the dc current of the switching transistors, but also couple the quadrature signals by using back-gate coupling technique to avoid using additional coupling transistors. The simulated results are shown in chapter 3.3, the power consumption is only 1.64 mW of 1.2 V voltage supply. The phase noise is -111.7 dBc/Hz @ 1 MHz offset and the oscillation frequency of the QVCO is 10 GHz. The tuning range is from 9.98 GHz to 13.97 GHz, and the figure of merit (FOM) is -189.6 dBc.

Reference

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