國 立 交 通 大 學

電信工程學系

碩 士 論 文

低功率和低電壓之電壓控制振盪器設計

Current-reused VCO with Low Power and Low Voltage

研 究 生：李明宗

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中 華 民 國 九 十 八 年 七 月

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低功率和低電壓之電壓控制振盪器設計

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摘要

本篇論文的研究焦點著重於降低電壓控制振盪器其功率消耗及相位雜訊的設計。利用電流再利用的架構，可以使電壓控制振盪器在運作時的工作電流只需傳統型電壓控制振盪器運作時的一半而達到低功率消耗的目的。同時，我們提出在共振腔上並聯一組負阻電路，此方法可以有效降低功率損耗、供應電壓和相位雜訊。根據上述架構及方法，我們完成低功率、低電壓和低相位雜訊2.5和3.5GHz之電壓控制振盪器。由量測結果(TSMC 0.18-μm 1P6M CMOS 製程)，實作之IC均與模擬結果相近並達到預期之特性。此設計的提供電壓和消耗功率分別為0.93V、0.54mW和1V、1.9mW，其工作頻率於3.5GHz和2.5GHz時，相位雜訊在距離中心頻率1 MHz分別為-116.9dBc/Hz和-125dBc/Hz。

Current-reused VCO with Low Power and Low Voltage in 0.18 μm CMOS

Student：Ming-Tsung Li　　Advisor：Dr. Jenn-Hwan Tarng

Department of Communication Engineering
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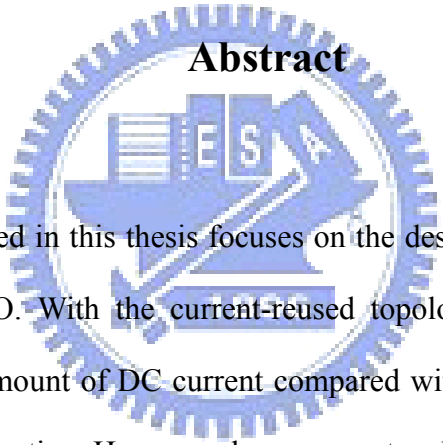

Abstract

The research described in this thesis focuses on the design of a low power consumption and phase noise LC-VCO. With the current-reused topology, the proposed LC-VCO can operate using only half amount of DC current compared with the conventional topologies to achieve low power consumption. Here, we also propose to add a negative-resistance cell shunt to the *L*-*C* tank, can effectively reduce of both the power consumption、supply voltage and phase noise. Based on proposed topology and novel method, we implement a low power、low voltage and low phase noise LC-VCO, which operates at 3.5/2.5 GHz. The proposed dual-band LC-VCO is implemented by TSMC 0.18-μm 1P6M CMOS process and the measured results are similar to simulation ones. Therefore, the performances of the proposed LC-VCO achieve anticipation. The measurement result of the VCO demonstrates a the power consumption and the supply voltage of its core is only 0.54 mW with 0.93 V and 1.9 mW with 1 V, the proposed LC-VCO operates 3.5 GHz and 2.5 GHz with phase noise of -116.9 dBc/Hz and -125 dBc/Hz, respectively, at 1 MHz offset frequency.

誌　　謝

在碩士班研究的這二年歲月，首先要感謝的是我的指導教授　唐震寰教授並致上我最誠摯的謝意。感謝老師在專業的通訊領域中，給予我不斷的指導與鼓勵，並賦予了實驗室豐富的研究資源與環境，使得這篇碩士論文能夠順利完成。同時，亦感謝口試委員國立臺灣大學　李學智教授及國立臺灣科技大學　楊成發教授對於論文內容所提出的寶貴建議及指導，在此致上最誠懇的謝意。

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李明宗　誌予

九十八年七月

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Chapter 1 Introduction

1.1 Background and Problems

In recent years, the development of several kinds of new communication technique is expected to provide high data rate, wide range and high speed communications in wireless area networks [1]. As the advancement of wireless communication system, transmission distance and data rate growing rapidly, the design of high performance radio frequency (RF) transceivers is an aspiration target.

At present, RF transceivers have been widely implemented by SiGe, GaAs or HBT processes due to the high performance at high frequency. However, the system cost will remain high because that those processes are not compatible with the silicon process and let along of a system on a chip (SOC) solution for the present time. Thus, the CMOS technology is an attractive process to meet the low cost requirement in RF transceivers.

Among function blocks of a RF transceiver as shown in Fig 1.1, the voltage controlled oscillator (VCO) is used to provide clean, stable, and precise carrier signals for frequency

translation in wireless transceivers. Because the purity (phase noise) of local signal which generated by the VCO will dominate the performance of the system, the design of high performance VCO is an urgent and momentous subject. In the design of VCOs, there are several common goals, such as low phase noise, low power consumption, low cost, satisfactory output power, and sufficient tuning range. Mostly, the low phase noise is a critical specification of VCOs for actual practice. As the shrinking of chip size and the growing demand of portable applications and power-efficient issues, the low voltage and low power design is another important target of VCOs. However, according to the well-known Leeson's model of phase noise [2], the phase noise and power consumption usually formed a key tradeoff in the circuit design of VCOs. Hence, how to design a VCO that satisfies the requirements described above is a challenging issue.

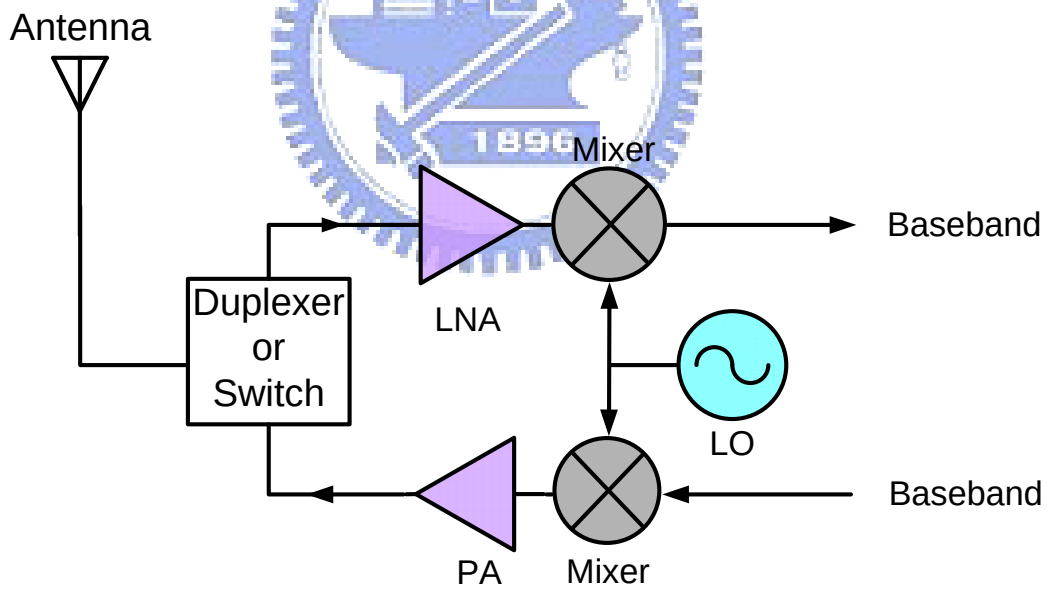


Figure 1.1 Block diagram of a typical RF front-end transceiver

1.2 Related Works and Motivation

In designing a VCO, low power consumption and low phase noise are two important parameters. The low power consumption may be achieved by reducing the supply voltage and/or the current in the VCO core circuit. Forward body bias (FBB) has been proposed as an effective method for improving the device performance in MOSFETs. Forward bias the body to source voltage V_{BS} and source to body voltage V_{SB} of NMOS and PMOS reduce the threshold voltage (V_t). The increase in high frequency noise with V_{BS} was qualitatively explained by considering the contributions from nonequilibrium channel noise and substrate resistance noise in 0.18 μm CMOS transistors. Therefore, in RF circuit applications, an FBB scheme is not favorable if high frequency noise is an important concern [3]. However, the low voltage limits the signal amplitude, which in turn limits the signal-to-noise ratio (SNR) and leads to an increase of the phase noise of the VCO. There is a tradeoff between the VCO phase noise and power consumption due to the degradation of the phase noise with the increased VCO gain needed for a larger power consumption. Therefore, how to control a low phase noise effectively at the low power level becomes an important and challenging issue. [4] suggests adding an external circuit called a harmonic tuned (HD) LC tank to suppress the harmonic frequency of the circuit. This method can reduce the phase noise effectively, but it also increases both the die area and power consumption. In conclusion, how to obtain a comparable phase noise effectively at the low power level becomes a bottleneck to design.

In this thesis, low power 、 low voltage and low phase noise LC-VCO by the negative resistance enhancement method in a current-reused VCO. In the VCO design, achieving the goal of low power or low voltage may not be a difficulty. The real problem is the phase noise performance is considerably poor at low power level. On the other hand, the bottleneck is how to improve the phase noise of VCOs at low voltage or low power operation. The negative

resistance enhancement method employs a PMOS shunt to the LC-tank, can reduce both the power consumption and the phase noise effectively.

1.3 Thesis Organization

The thesis is organized into five chapters including the introduction. Chapter 2 deals with the basic concepts of VCO design, its metrics and some popular voltage-controlled oscillator (VCO) topologies. In chapter 3, some advanced popular VCO topologies are reviewed. In chapter 4, we design the low phase noise low power consumption dual-band VCO with the simulated and measured results. Chapter 5 conclusion is drawn.

Chapter 2 *Basics of CMOS VCO*

2.1 General Consideration

A simple oscillator produces a periodic output, usually in the form of voltage. As such, the circuit has no input while sustaining the output indefinitely. How can a circuit oscillate? Consider the unity gain negative feedback circuit shown in Fig. 2.1, where

$$\frac{V_{out}}{V_{in}}(s)=\frac{H(s)}{1+H(s)} \tag{1}$$

If the amplifier itself experiences so much phase shift at high frequencies that the overall feedback becomes positive, then oscillation may occur. More accurately, if for s=$j\omega_0$, H($j\omega$)=-1, then the closed loop gain approach infinity at ω_0 indefinitely. In fact, as conceptually illustrated in Fig. 2.2, a noise component at ω_0 experiences a total gain of unity and a phase shift of 180°, returning to the subtractor as a negative replica of the input. Upon subtraction, the input and the feedback signals give a lager difference. Thus, the circuit continues to "regenerate," allowing the component at ω_0 to grow.

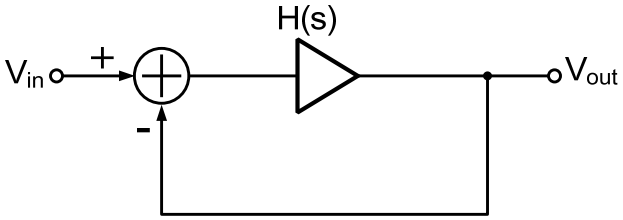


Figure 2.1 Feedback system

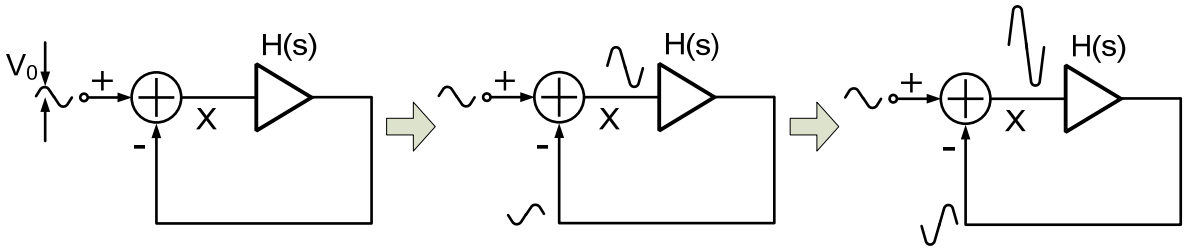


Figure 2.2 Evolution of oscillatory system with time

For the oscillation to begin, a loop gain of unity or greater is necessary. This can be seen by following the signal around the loop over many cycles and expressing the amplitude of the subtractor's output in Fig. 2.2 as geometric series (if $\angle$H($j\omega$)=180°):

$$V_X = V_0 + |H(j\omega_0)|V_0 + |H(j\omega_0)|^2 V_0 + |H(j\omega_0)|^3 V_0 + \cdots \tag{2}$$

If $|H(j\omega_0)| > 1$, the above summation diverges whereas if $|H(j\omega_0)| < 1$, then

$$V_X = \frac{V_0}{1-|H(j\omega_0)|} < \infty \tag{3}$$

In summary, if a negative feedback circuit has a loop gain that satisfies two conditions:

$$|H(j\omega_0)| \geq 1 \tag{4}$$

$$\angle H(j\omega_0) = 180° \tag{5}$$

then the circuit may oscillate at ω_0, which is Called "Barkhausen criteria." These conditions are necessary but not sufficient. In order to ensure oscillation in the presence of temperature and process variations, we typically choose the loop gain to be at least twice or three times the required value.

We may state the second Barkhausen critertion as $\angle H(j\omega_0) = 180°$ or a total phase shift of 360°. This should not be confusing: if the system is designed to have a low frequency negative feedback, it already produces 180° of phase shift in the signal traveling around the loop in Fig 2.1, and $\angle H(j\omega_0) = 180°$ denotes an additional frequency dependent phase shift that, as illustrated in Fig 2.2, ensures the feedback signal enhances the original signal. Thus, three illustrated in Fig 2.3 are equivalent in terms of the second criterion. We say the system of Fig 2.3 exhibits a frequency dependent phase shift of 180°. The difference between Figs.

2.3(b) and (c) is that the open loop amplifier in the former contains enough stages with proper polarities a total phase shift of 360° at ω_0 whereas that in the latter produces no phase shift at ω_0.

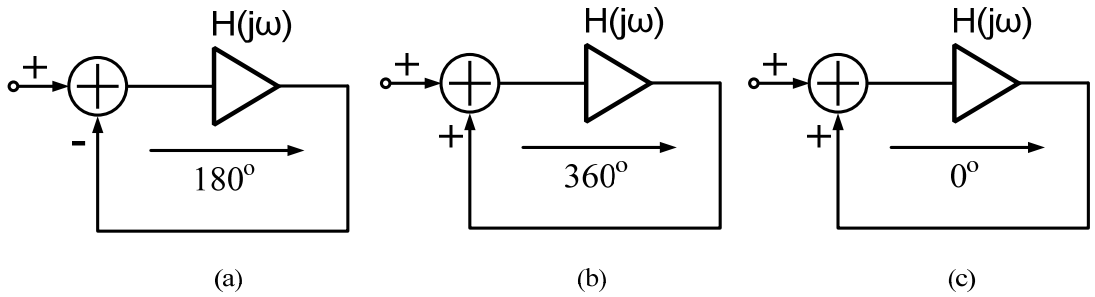


Figure 2.3 Various views of oscillatory feedback system

2.2 One port oscillator

An alternative view that provides more insight into the oscillation phenomenon employs the concept of "negative resistance." To arrive at this view, let us first consider a simple tank that is stimulated by a circuit impulse Fig. 2.4(a). The tank responds with a decaying oscillatory behavior because, in every cycle, some of the energy that reciprocates between the capacitor and the inductor is lost in the form of heat in the resistor. Now suppose a resistor equal to $-R_p$ is placed in parallel with R_p and experiment is repeated Fig. 2.4(b). Since $R_p \parallel (-R_p)=\infty$, the tank oscillates indefinitely. Thus, if a one port circuit exhibiting a negative resistance is placed in parallel with a tank Fig. 2.4(c), the combination may oscillate. Such a topology is called a one port oscillator.

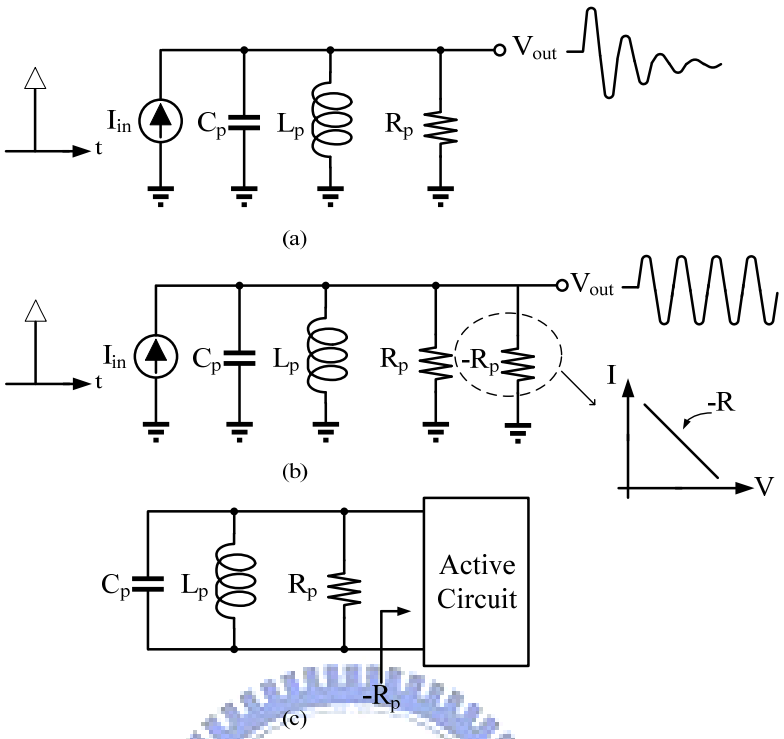


Figure 2.4 (a) Decaying impulse response of a tank, (b) addition of negative resistance to cancel loss in R_p, (c) use of an active circuit to provide negative resistance.

How can a circuit provide a negative resistance? Recall that feedback multiplies or divides the input and output impedances of circuits by a factor equal to one plus the loop gain. Thus, if the loop gain is sufficiently negative, (i.e., the feedback is sufficiently positive), a negative resistance is achieved.

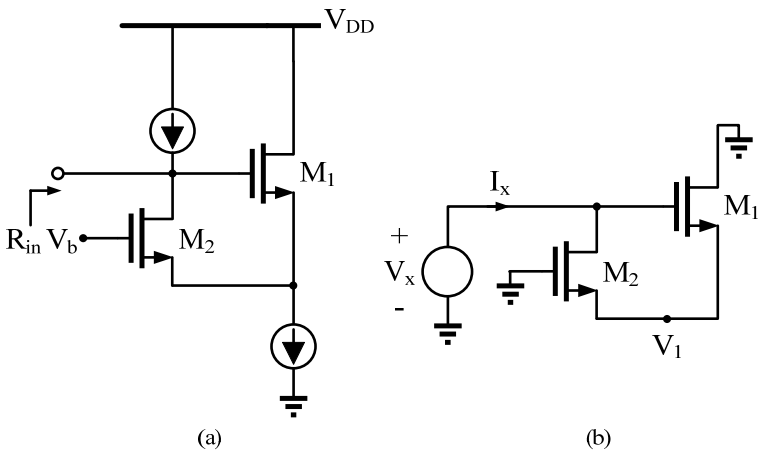


Figure 2.5 (a) Source follower with positive feedback to create negative input impedance, (b) equivalent circuit if (a) to calculate the input impedance

For feedback system $R_{in} = \frac{R}{1+T(s)}$, R_{in} becomes negative as T(s) < -1

$$I_X = -g_{m2}V_1 \tag{6}$$

$$I_X = g_{m1}(V_g - V_X) \tag{7}$$

$$\frac{V_X}{I_X} = -(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}) = -\frac{2}{g_m} \text{ (if } g_{m1}=g_{m2}=g_m) \tag{8}$$

2.3 Negative-R LC Oscillator

With a negative resistance available, we can now construct an oscillator as illustrated in Fig. 2.6. Here, R_p denotes the equivalent parallel resistance of the tank and, for oscillation build-up, R_p-2/g_m ≧ 0.

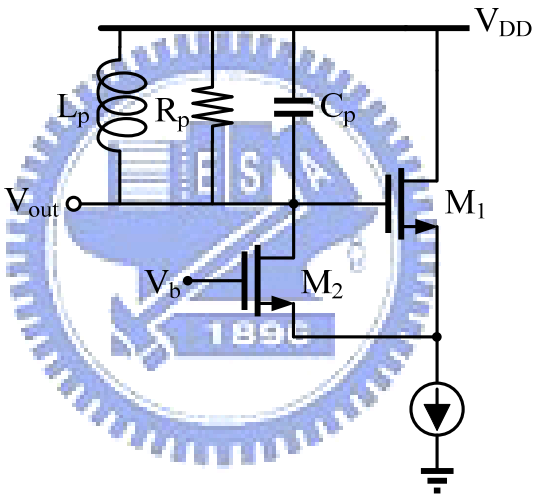


Figure 2.6 Oscillator using negative input resistance of a source follower with positive feedback

More interestingly, the circuit can be redrawn as in Fig. 2.7(a), bearing a resemblance to Fig. A.6(b). in fact, if the drain current of M_1 flows through a tank and resulting voltage is applied to the gate of M_2, the topology of Fig. 2.7(b) is obtained.

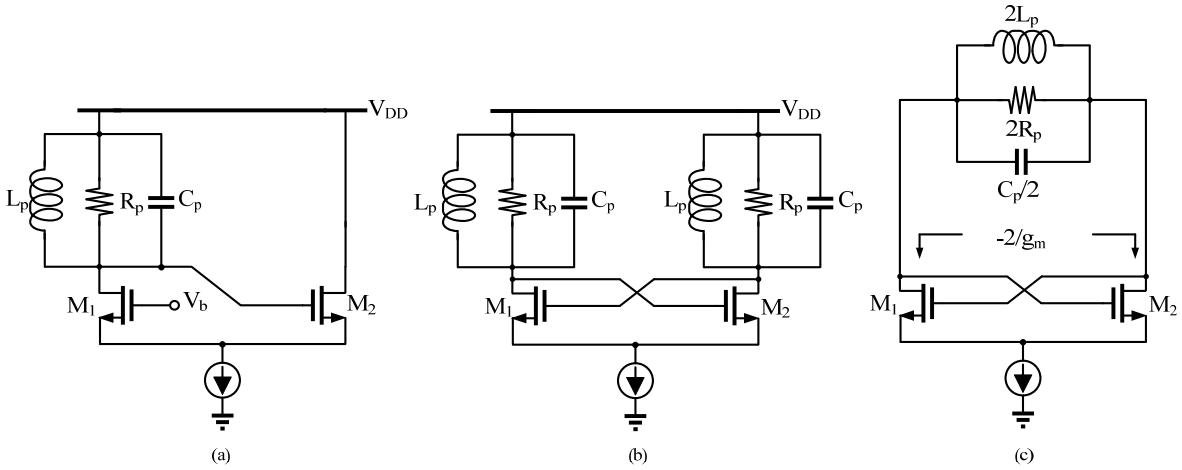


Figure 2.7 (a) Redrawing of the topology shown in Fig. 2.6, (b) differential version of (a), (c) Equivalent circuit of Fig. 2.7(b)

For oscillation build-up $2R_p\text{-}2/g_m \geqq 0$, $R_p \geqq 1/g_m$.

2.4 Voltage-Controlled Oscillators

Most applications require that oscillators be "tunable," i.e., their output frequency be a function of a control input, usually a voltage. An ideal voltage-controlled oscillator is a circuit whose output frequency is a linear function of its control voltage (Fig. 2.8):

$$\omega_{out} = \omega_0 + k_{VCO}V_{cont} \tag{9}$$

Here, ω_0 represents the intercept corresponding to $V_{cont}=0$ and K_{VCO} denotes the "gain" or "sensitivity" of the circuit (expressed in rad/s/V). The achievable range, $\omega_2\text{-}\omega_1$, is called the "tuning range."

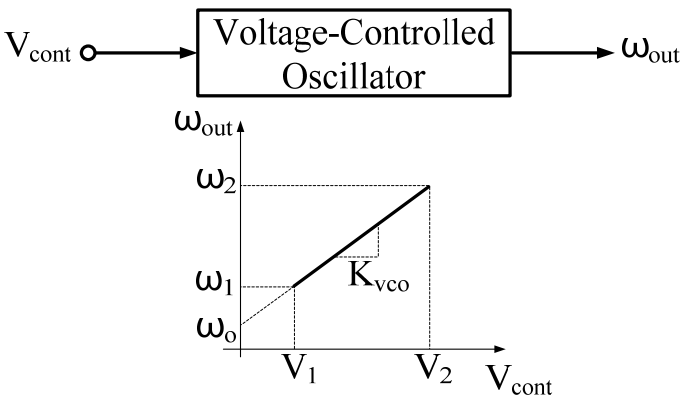


Figure 2.8 Definition of a VCO

2.5 Center Frequency

The center frequency (i.e., the midrange value in Fig. 2.8) is determined by the environment in which the VCO used.

2.6 Tuning Range

The required tuning range is dictated by two parameters: (1) the variation of the VCO center frequency with process and temperature and (2) the frequency range necessary for the application. The center frequency of some CMOS oscillator may vary by a factor of two at the extreme of process and temperature, thus mandating a sufficiently wide ($\geqq 2$) tuning range to guarantee that the VCO output frequency can be driven to the desired value.

An important concern in the design of VCOs is the variation of the output phase and frequency as a result of noise on the control line. For a given noise amplitude, the noise in the output frequency is proportional to K_{VCO} because $\omega_{out}=\omega_0+K_{VCO}V_{cont}$. Thus, to minimize the effect of noise in V_{cont}, the VCO gain must be minimized, a constraint in direct conflict with the required tuning range. In fact, if, as shown in Fig. 2.8, the allowable range of V_{cont} is from V_1 to V_2 (e.g., from 0 to V_{DD}) and the tuning range must span at least ω_1 to ω_2, then K_{VCO} must satisfy the following requirement:

$$K_{VCO} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1} \tag{10}$$

Note that, for a given tuning range, K_{VCO} increase as the supply voltage decreases, making the oscillator more sensitive to noise on the control line.

Tuning Linearity

As exemplified by Eq. (A.16), the tuning characteristics of VCOs exhibit nonlinearity, i.e., their gain, K_{VCO}, is not constant. Nonlinearity degrades the settling behavior of phase-locked loops. For this reason, it is desirable to minimize the variation of K_{VCO} across the tuning range. Actual oscillator characteristics typically exhibit a high gain region in the middle of the range and a low gain at the two extremes (Fig. 2.9). Compared to a linear characteristic (the gray

line), the actual behavior displays a maximum gain greater than that predicted by (10), implying that, for a given tuning range, nonlinearity inevitably leads to higher sensitivity for some region of the characteristic.

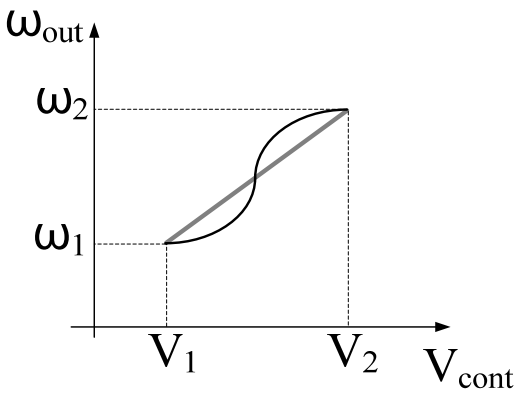


Figure 2.9 Nonlinear VCO characteristic

2.7 Output Power

In general, it is not easy to predict the output power of the realistic VCO, but we can know that the maximum output power of VCO is not larger than the output power of the transistor in the VCO through large-signal analysis. The output power must be maximized in order to make the waveform less sensitive to noise or to lower phase noise. It trades with power consumption, supply voltage, and tuning range. The designer can choose the active devices whose parameter is known. Therefore, when the VCO is designed, we also can predict the output power of the VCO.

2.8 Harmonic Rejection

The VCO has a good harmonic rejection performance that means it is closed to a sinusoidal output waveform. In wireless communication systems, harmonic rejection is specified how much smaller the harmonics of the output signal are compared with the fundamental output power.

2.9 Power Consumption

With fast growth in the radio-frequency (RF) wireless communications market, the demand for low-power and high-performance but low-cost RF solutions is rising. Low–power operation can extend the lifetime of the battery and save money for consumers.

2.10 Phase Noise

Noise injected into an oscillator by its constituent devices or by external means may influence both the frequency and the amplitude of the output signal. In most cases, the disturbance in the amplitude is negligible or unimportant, and only the random deviation of the frequency is considered.

For a nominally periodic sinusoidal signal, we can write $x(t)=A\cos[f_c t+\phi_n(t)]$, where $\phi_n(t)$ is a small random excess phase representing variations in the period. The function $\phi_n(t)$ is called "phase noise". Note that for $|\phi_n(t)| \ll 1$ rad, we have $x(t) \fallingdotseq A\cos f_c t - A\phi_n(t)\sin f_c t$; that is, the spectrum of $\phi_n(t)$ is translated to $\pm f_c$.

In RF applications, phase noise is usually characterized in the frequency domain. For an ideal sinusoidal oscillator operating at f_c, the spectrum assumes the shape of an impulse, whereas for an actual oscillator, the spectrum exhibits "skits" around the carrier frequency (Fig. 2.10). The frequency fluctuations correspond to jitter in the time domain, which is a random perturbation of zero crossings of a periodic signal (Fig. 2.11).

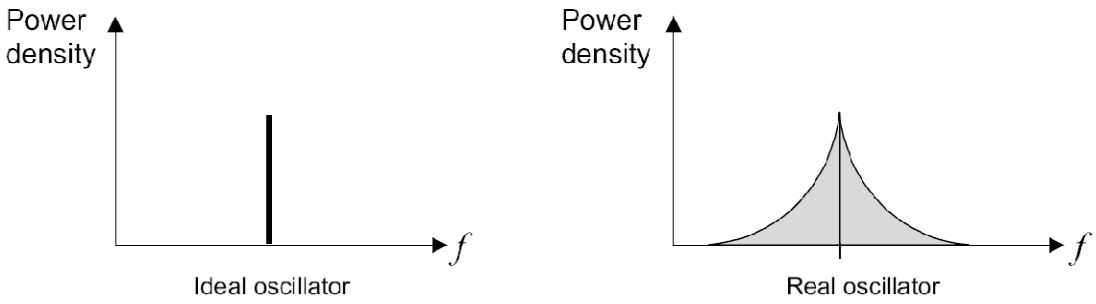


Figure 2.10 Frequency spectrum of ideal and real oscillators

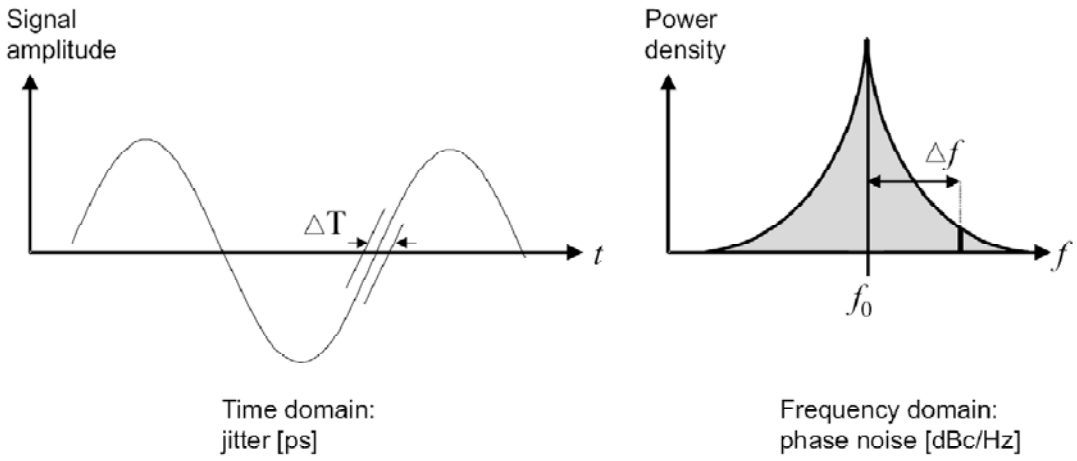


Figure 2.11 Jitter in the time domain relates to phase noise in the frequency domain

Frequency fluctuations are usually characterized by the single sideband noise spectral density normalized to the carrier signal power (Fig. 2.10). It is defined as

$$L(f_c, \Delta f) = 10\log\left[\frac{P_{sideband}(f_c + \Delta f, 1Hz)}{P_{carrier}}\right] \tag{11}$$

and has units of decibels below the carrier per hertz (dBc/Hz). $P_{carrier}$ is the carrier signal power at the carrier frequency f_C and $P_{sideband}(f_c+\Delta f, 1\ Hz)$ denotes the single sideband power at the offset Δf from the carrier f_C at a measurement bandwidth of 1 Hz.

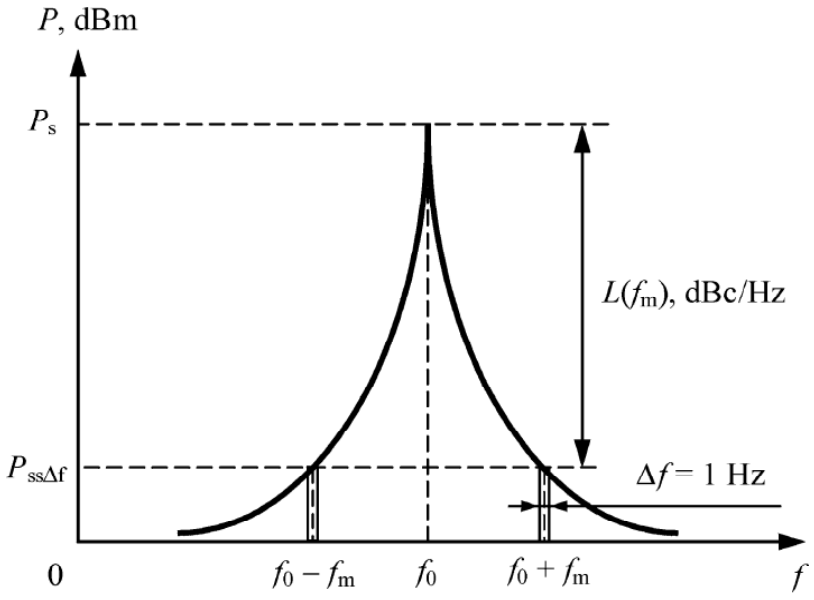


Figure 2.12 Oscillator output power spectrum

The typical oscillator output power spectrum is shown in Fig. 2.12. The noise distribution on each side of the oscillator signal is subdivided into a larger number of strips of width Δf located at the distance f_m away from the single. It should be noted that, generally, the spectrum of the output single consists of the phase noise components. Hence, to measure the phase noise close to the carrier frequency, one needs to make sure that any contributions of parasitic amplitude modulation to the oscillator output noise spectrum are negligible compared with those from frequency modulation. The single sideband phase noise $L(f_m)$ usually given logarithmically is defined as the ratio of signal power $P_{ss\Delta f}$ in one phase modulation sideband per bandwidth Δf=1 Hz, at an offset f_m away from the carrier, to the total signal power P_s.

Time invariant model

In this section, phase noise analysis is described by using time invariant model. Time invariant means whenever noise sources injection, the phase noise in VCO is the same. In the other words, phase shift of VCO caused by noise is the same in any time. Therefore, it's no need to consider when the noise is coming. Suppose oscillator is consists of amplifier and resonator. The transfer function of a band-pass resonator is written as

$$H(j\omega)=\frac{j\omega\frac{1}{RC}}{\frac{1}{LC}+j\omega\frac{1}{RC}-\omega^2} \tag{12}$$

The transfer function of a common band-pass is written as

$$H(j\omega)=\frac{j\omega\frac{\omega_0}{Q}}{\omega_0^2+j\omega\frac{\omega_0}{Q}-\omega^2} \tag{13}$$

Compare equation (12) with (13). Thus,

$$\omega_0=\frac{1}{LC} \quad \text{and} \quad Q=\omega_0 RC \tag{14}$$

The frequency $\omega = \omega_0 + \Delta\omega$ which is near oscillator output frequency. If $\omega_0 \gg \Delta\omega$, we can use Taylor expansion for only first and second terms. Hence

$$H(j\omega) \approx 1 + \frac{2}{j\frac{\omega_0}{Q}} \cdot \Delta\omega \tag{15}$$

The close-loop response of oscillator is expressed by

$$G(j\omega) = \frac{1}{1 - H(j\omega)} \approx \frac{-j\frac{\omega_0}{Q}}{2 \cdot \Delta\omega} \tag{16}$$

When input noise density is $S_i(\omega)$, the output noise density is

$$S_0(\omega) = S_i(\omega)\left|G(\omega)\right|^2 = FkT\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{17}$$

The above equation is double sideband noise. The phase noise faraway center frequency $\Delta\omega$ can be expressed by

$$L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_S} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{18}$$

Where F is empirical parameter ("often called the device excess noise number"), k is Boltzman' s constant, T is the absolute temperature, P_S is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, and Q is the effective quality factor of the tank with all the loading in place(also known as loaded Q). From equation (18), increasing power consumption and higher Q factor can get better phase noise. Increasing power consumption means increasing the power of amplifier. This method will decrease noise figure (NF) and improve phase noise.

From, equation (18), we can briefly understand phase noise. But the equation and actual measured results are different. The VCO spectrum is shown as Fig. 2.12. The phase noise equation can be modified as the same as equation (31) that is called Lesson's model [5].

$$L(\Delta\omega) = 10\log\left\{\frac{2FKT}{P_S}\cdot\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\cdot\left[1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right]\right\}$$

These modifications, due to Leeson, consist of a factor to account for the increased noise in the $1/(\Delta\omega)^2$ region, an additive factor of unity (inside the braces) to account for the noise floor, and a multiplicative factor (the term in the second set of parentheses) to provide a $1/|\Delta\omega|^3$ behavior at sufficiently small offset frequencies. With these modifications, the phase-noise spectrum appears as in Fig. 2.13.

It is important to note that the factor F is an empirical fitting parameter and therefore must be determined from measurements, diminishing the predictive power of the phase-noise equation. Furthermore, the model asserts that $\Delta\omega_{1/f^3}$, the boundary between the $1/(\Delta\omega)^2$ and $1/|\Delta\omega|^3$ regions, is precisely equal to the $1/f$ corner of device noise. However, measurements frequently show no such equality, and thus one must generally treat $\Delta\omega_{1/f^3}$ as an empirical fitting parameter as well. Also, it is not clear what the corner frequency will be in the presence of more than one noise source with $1/f$ noise contribution. Last, the frequency at which the noise flattens out is not always equal to half the resonator bandwidth, $\omega_0/2Q$. Both the ideal oscillator model and the Leeson model suggest that increasing resonator Q and signal amplitude are ways to reduce phase noise. The Leeson model additionally introduces the factor F, but without knowing precisely what it depends on, it is difficult to identify specific ways to reduce it. The same problem exists with $\Delta\omega_{1/f^3}$ as well. Last, blind application of these models has periodically led to earnest but misguided attempts to use active circuits to boost Q. Sadly, increases in Q through such means are necessarily accompanied by increases in F as well, preventing the anticipated improvements in phase noise. Again, the lack of analytical expressions for F can obscure this conclusion, and one

continues to encounter various doomed oscillator designs based on the notion of active Q boosting.

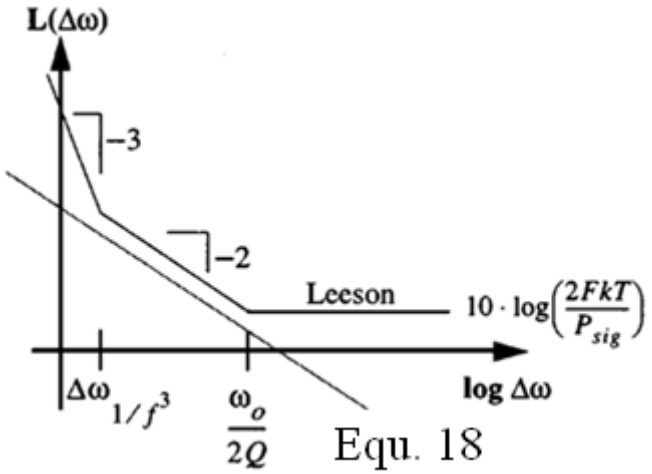


Figure 2.13 Phase noise: Leeson versus (18).

Time Variant

In the general case, multiple noise sources affect the phase and amplitude of an oscillator. This chapter begins by investigating the effect of a single noise source on the amplitude and phase of the oscillator.

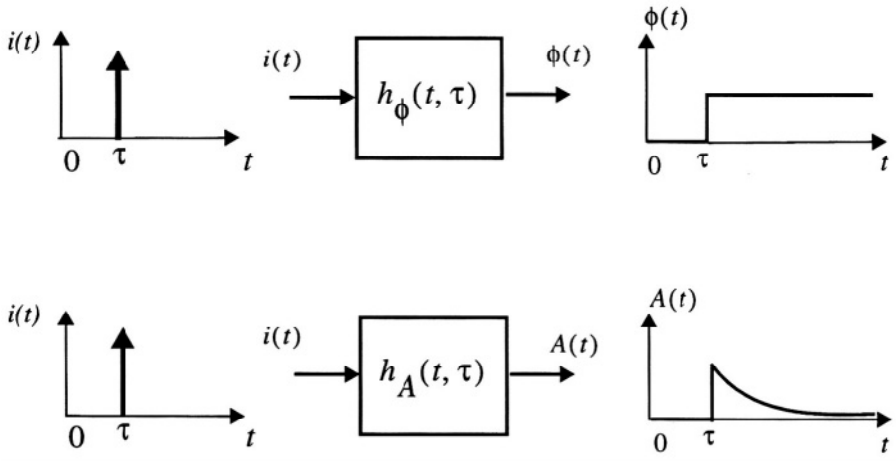


Figure 2.14 Equivalent systems for phase and amplitude

Since each input source generally affects both amplitude and phase, a pair of equivalent systems, one each for amplitude and phase, can be defined. Each system can be viewed as a single-input, single-output system as shown in Fig. 2.14. The input of each system in Fig.

2.14 is a perturbation current (or voltage) and the outputs are the excess phase, ϕ(t), and amplitude, *A(t)*. Both systems shown in Fig. 2.14 are time-variant as shown by the following examples.

The first example is an ideal parallel *LC* tank oscillating with voltage amplitude, as shown in Fig. 2.15. If one injects an impulse of current at the voltage maximum, only the voltage across the capacitor changes; there is no effect on the current through the inductor. Therefore, the tank voltage changes instantaneously, as shown in Fig. 2.15. Assuming a voltage- and time-invariant capacitor, the instantaneous voltage change ΔV is given by

$$\Delta V = \frac{\Delta q}{C_{total}} \tag{19}$$

where Δq is the total charge injected by the current impulse and C_{total} is the total capacitance in parallel with the current source. It can be seen from Fig. 2.15 that the resultant change in *A*(*t*) and ϕ(t) is time dependent. In particular, if the impulse is applied at the peak of the voltage across the capacitor, there will be no phase shift and only an amplitude change will result, as shown in Fig. 2.15(a). On the other hand, if this impulse is applied at the zero crossing, it has the maximum effect on the excess phase, ϕ(t), and the minimum effect on the amplitude, as depicted in Fig. 2.15(b).

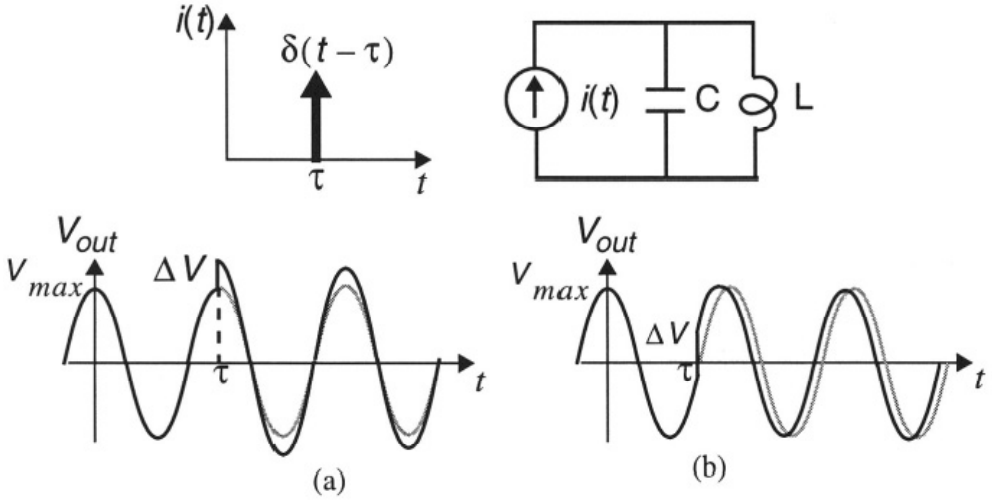


Figure 2.15 Impulse response of an ideal LC oscillator

To emphasize the generality of this time-variance, consider two more examples. The

relaxation oscillator known as the Bose oscillator is shown in Fig. 2.16. It consists of a Schmitt-trigger inverter and an RC circuit. The hysteresis in the transfer function of the inverter and the RC time constant determine the frequency of oscillation. The resulting capacitor voltage waveform is shown with a solid line in Fig. 2.17.

As before, imagine an impulsive current source in parallel with the capacitor, injecting charge at t=τ, as shown in Fig. 2.16. All of the injected charge goes into the capacitor and changes the voltage across it instantaneously. This voltage change, ΔV, results in a phase shift, Δϕ, as shown in Fig. 2.17. As can be seen from Fig. 2.17, for a small area of the current impulse (injected charge), the resultant phase shift is proportional to the voltage change, ΔV, and hence to the injected charge, Δq. Therefore, Δϕ can be written as

$$\Delta\phi = \Gamma(\omega_0\tau)\frac{\Delta V}{V_{\max}} = \Gamma(\omega_0\tau)\frac{\Delta q}{q_{\max}} \qquad \Delta q \ll q_{\max} \tag{20}$$

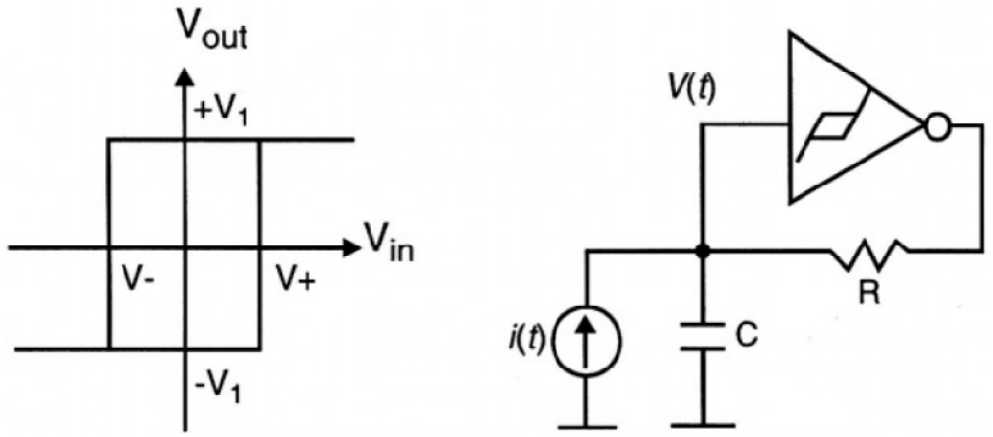


Figure 2.16 Bose oscillator with parallel perturbation current source

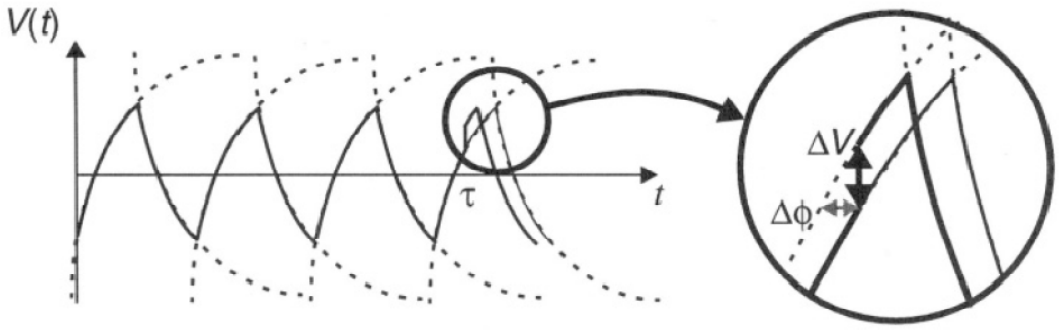


Figure 2.17 The waveform of the Bose oscillator shown in Figure 3

where V_{max} is the voltage swing across the capacitor and $q_{max}=C_{node}V_{max}$ is the maximum charge swing. The function, $\Gamma(x)$ is the time-varying "proportionality factor". It is called the *impulse sensitivity function* (ISF), since it determines the sensitivity of the oscillator to an impulsive input. It is a dimensionless, frequency- and amplitude-independent function periodic in 2π that describes how much phase shift results from applying a unit impulse at any point in time.

In any event, to develop a feel for typical shapes of ISF's, consider two representative examples, first for an *LC* and a ring oscillator in Fig. 2.18(a) and (b).

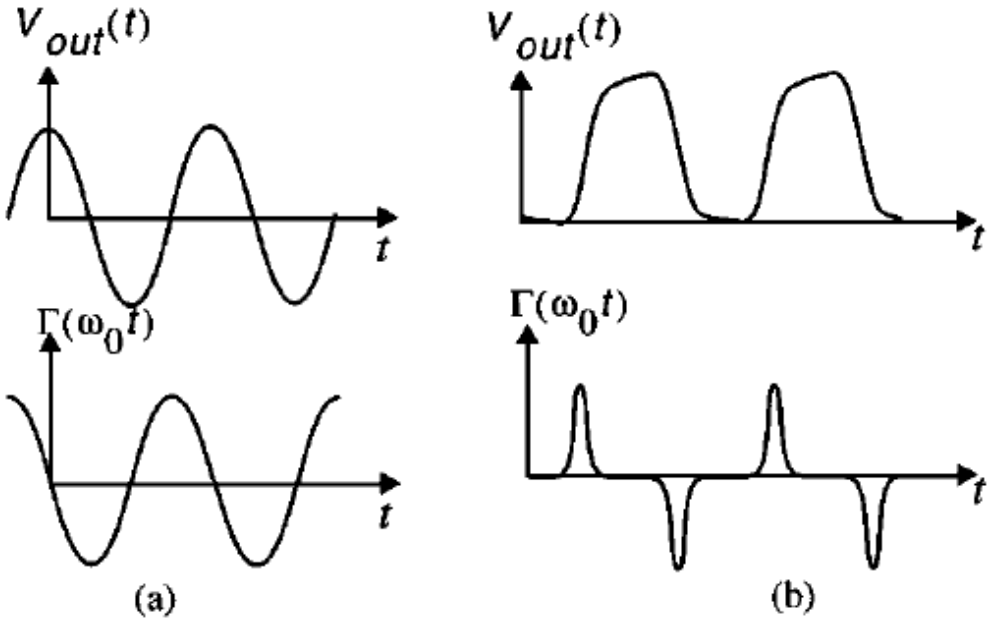


Figure 2.18 Example ISF for (a) *LC* oscillator and (b) ring oscillator.

It is critical to note that the current-to-phase transfer function is linear for small injected charge, even though the active elements may have strongly nonlinear voltage current behavior. It should also be noted that the linearity and time-variance of a system depends on both the characteristics of the system and its input and output variables. The linearization of the current-to-phase system of Fig. 2.14 does not imply linearization of the nonlinearity of the voltage-current characteristics of the active devices. In fact, this nonlinearity affects the shape of the ISF and therefore has an important influence on phase noise, as will be seen shortly.

Noting that the introduced phase shift persists indefinitely, the unity phase impulse response can be easily calculated from (20) to be

$$h_{\Phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t-\tau) \tag{21}$$

where $u(t)$ is the unit step.

Thanks to linearity, the output excess phase, $\phi(t)$, can be calculated for small charge injections using the superposition integral

$$\phi(t) = \int_{-\infty}^{+\infty} h_{\phi}(t,\tau) i(\tau) d\tau = \int_{-\infty}^{t} \frac{\Gamma(\omega_0\tau)}{q_{\max}} i(\tau) d\tau \tag{22}$$

where $i(t)$ represents the input noise current injected into the node of interest. Equation (22) is one of the most important results of this section and will be referred to frequently.

The output voltage, $V(t)$, is related to the phase, $\phi(t)$, through a phase modulation process. Thus the complete process by which a noise input becomes an output perturbation in $V(t)$ can be summarized in the block diagram of Fig. 2.19. The essential features of the block diagram of Fig. 2.19 are a modulation by a periodic function, an ideal integration and a nonlinear phase modulation. The complete process thus can be viewed as a cascade of an LTV system that converts current (or voltage) to phase, with a nonlinear system that converts phase to voltage.

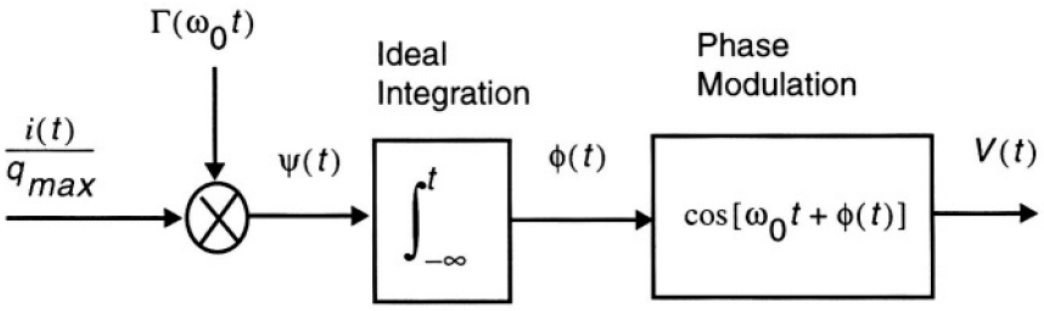


Figure 2.19 The equivalent block diagram of the process.

Since the ISF is periodic, it can be expanded in a Fourier series

$$\Gamma(\omega_0\tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n) \tag{23}$$

where the coefficients c_n are real-valued, and θ_n is the phase of the *n*th harmonic. As will be seen later, θ_n is not important for random input noise and is thus neglected here. Using the expansion in (23) for $\Gamma(\omega_0\tau)$ in the superposition integral and exchanging the order of summation and integration, the following is obtained:

$$\phi(t) = \frac{1}{q_{\max}}\left[c_0 \int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\hbar}^{t} i(\tau)\cos(n\omega_0\tau)d\tau\right] \tag{24}$$

Equation (24) identifies individual contributions to the total $\phi(t)$ for an arbitrary input current $i(t)$ injected into any circuit node, in terms of the various Fourier coefficients of the ISF. The decomposition implicit in (24) can be better understood with the equivalent block diagram shown in Fig. 2.20.

Each branch of the equivalent system in Fig. 2.20 acts as a bandpass filter and a downconverter in the vicinity of an integer multiple of the oscillation frequency. For example, the second branch weights the input by c_1, multiplies it with a tone at ω_0 and integrates the product. Hence, it passes the frequency components around ω_0 and downconverts the output to the baseband. As can be seen, components of perturbations in the vicinity of integer multiples of the oscillation frequency play the most important role in determining $\phi(t)$.

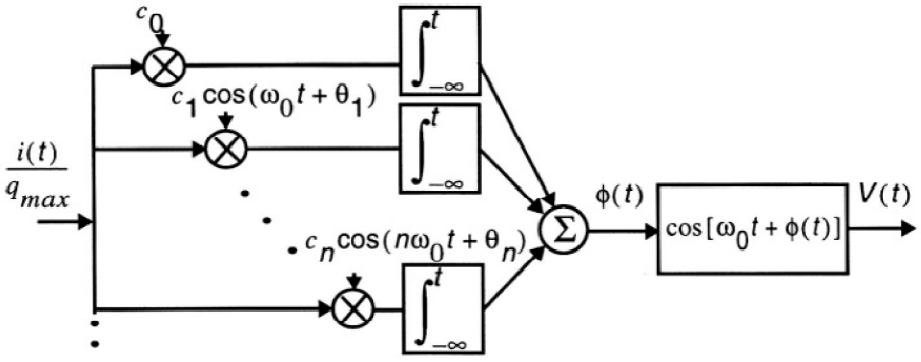


Figure 2.20 The equivalent system for ISF decomposition

To investigate the effect of low frequency perturbations on the oscillator phase, a low frequency sinusoidal perturbation current, $i(t)$, is injected into the oscillator at a frequency of $\Delta\omega \ll \omega_0$:

$$i(t) = I_0 \cos(\Delta\omega t) \tag{25}$$

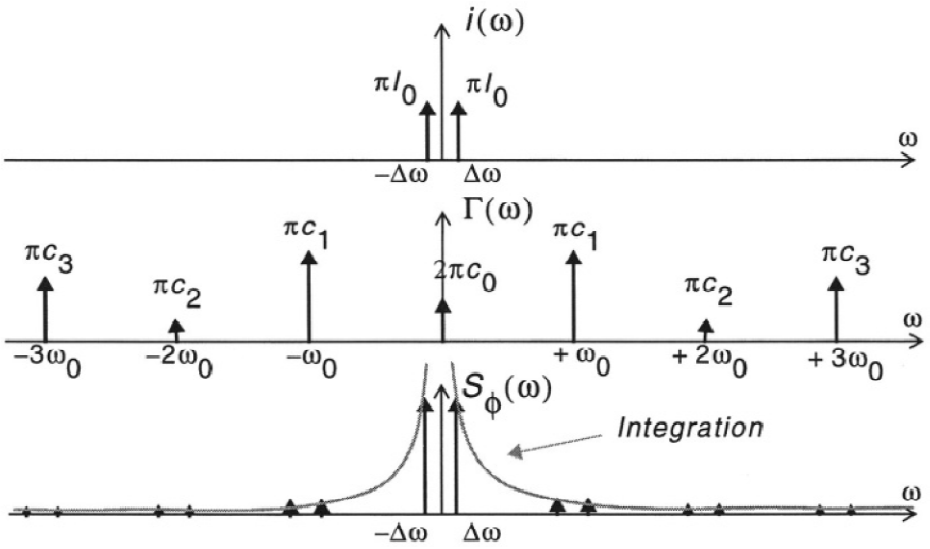


Figure 2.21 Conversion of a low frequency sinusoidal current to phase

where I_0 is the amplitude of $i(t)$. The arguments of all the integrals in (24) are at frequencies higher than $\Delta\omega$ and are significantly attenuated by the averaging nature of the integration, except the term arising from the first integral, which involves c_0. Therefore, the only significant term in $\phi(t)$ will be

$$\phi(t) \approx \frac{I_0 c_0}{q_{\max}} \int_{-\infty}^{t} \cos(\Delta\omega\tau) d\tau = \frac{I_0 c_0 \sin(\Delta\omega t)}{q_{\max} \Delta\omega} \tag{26}$$

As a result, there will be two impulses at $\pm\Delta\omega$ in the power spectral density of $\phi(t)$, denoted as $S_\phi(\omega)$ as shown in Fig. 2.21.

As another important special case, consider a current at a frequency close to the oscillation frequency given by

$$i(t) = I_1 \cos\left[(\omega_0 + \Delta\omega)t\right] \tag{27}$$

A process similar to that of the previous case occurs except that the spectrum of $i(t)$ consists of two impulses at $\pm(\omega_0+\Delta\omega)$ as shown in Fig. 2.22. This time the dominant term in (24) will be the second integral corresponding to n=l. Therefore, $\phi(t)$ is given

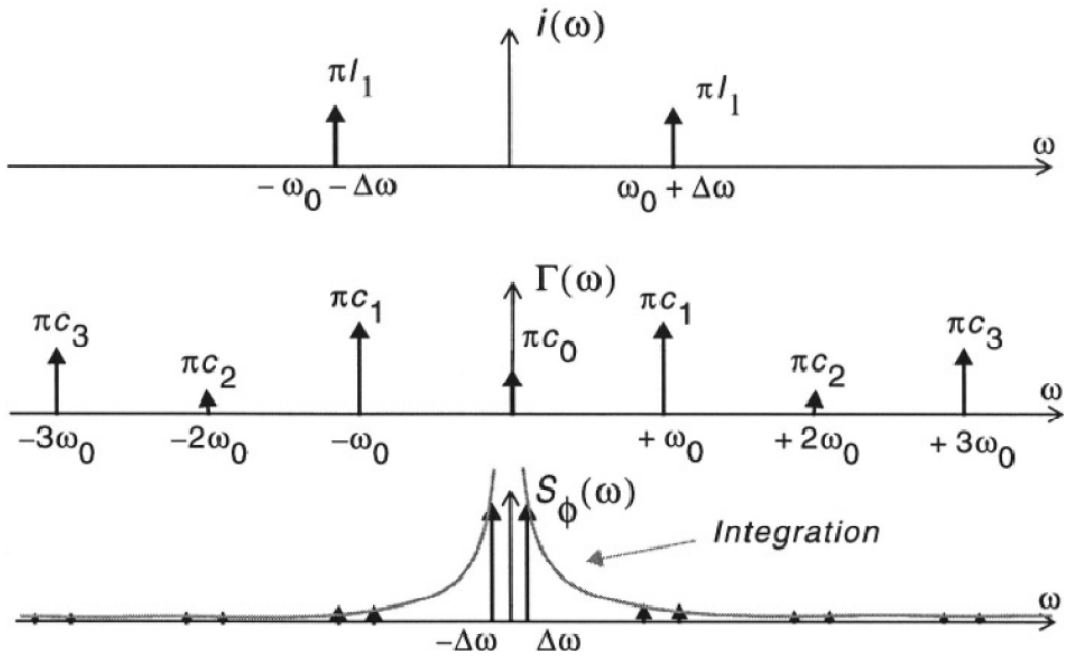


Figure 2.22 Conversion of a tone in the vicinity of ω_0

by

$$\phi(t) \approx \frac{I_1 c_1 \sin(\Delta\omega t)}{2q_{\max}\Delta\omega} \tag{28}$$

which again results in two equal sidebands at $\pm\Delta\omega$ in $S_\phi(\omega)$.

More generally, (24) suggests that applying a current, $i(t) = I_n \cos\left[(n\omega_0 + \Delta\omega)t\right]$, close to any integer multiple of the oscillation frequency will result in two equal sidebands at $\pm\Delta\omega$ in $S_\phi(\omega)$. Hence, in the general case $\phi(t)$ is given by

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{\max}\Delta\omega} \tag{29}$$

for $n\neq 0$. For $n=0$, phase is given by (26).

Unfortunately, we are not quite done: (29) allows us to figure out the spectrum of $\phi(t)$, but we ultimately want to find the spectrum of the output voltage of the oscillator, which is not quite the same thing. The two quantities are linked through the actual output waveform, however. To illustrate what we mean by this linkage, consider a specific case where the output may be approximated as a sinusoid, so that $v_{out}(t) = \cos[\omega_0 t + \phi(t)]$. This equation may be considered a phase-to-voltage converter; it takes phase as an input, and produces from it the output voltage. This conversion is fundamentally nonlinear because it involves the phase

modulation of a sinusoid.

Performing this phase-to-voltage conversion, and assuming "small" amplitude disturbances, we find that the single-tone injection leading to (29) results in two equal-power sidebands symmetrically disposed about the carrier

$$P_{SBC}(\Delta\omega) \approx 10 \cdot \log\left(\frac{I_n c_n}{4q_{\max}\Delta\omega}\right)^2. \tag{30}$$

The foregoing result may be extended to the general case of a white noise source

$$P_{SBC}(\Delta\omega) \approx 10 \cdot \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\sum_{n=0}^{\infty} c_n^2}{4q_{\max}^2\Delta\omega^2}\right). \tag{31}$$

Equation (30) implies both upward and downward frequency translations of noise into the noise near the carrier, as illustrated in Fig. 2.23. This figure summarizes what the foregoing equations tell us: components of noise near *integer multiples* of the carrier frequency all fold into noise near the carrier itself.

Noise near dc gets *upconverted*, weighted by coefficient , so $1/f$ device noise ultimately becomes $1/f^3$ noise near the carrier; noise near the carrier stays there, weighted by ; and white noise near higher integer multiples of the carrier undergoes *downconversion*, turning into noise in the $1/f^2$ region. Note that the $1/f^2$ shape results from the integration implied by the step change in phase caused by an impulsive noise input. Since an integration (even a time-varying one) gives a white voltage or current spectrum a $1/f$ character, the power spectral density will have a $1/f^2$ shape.

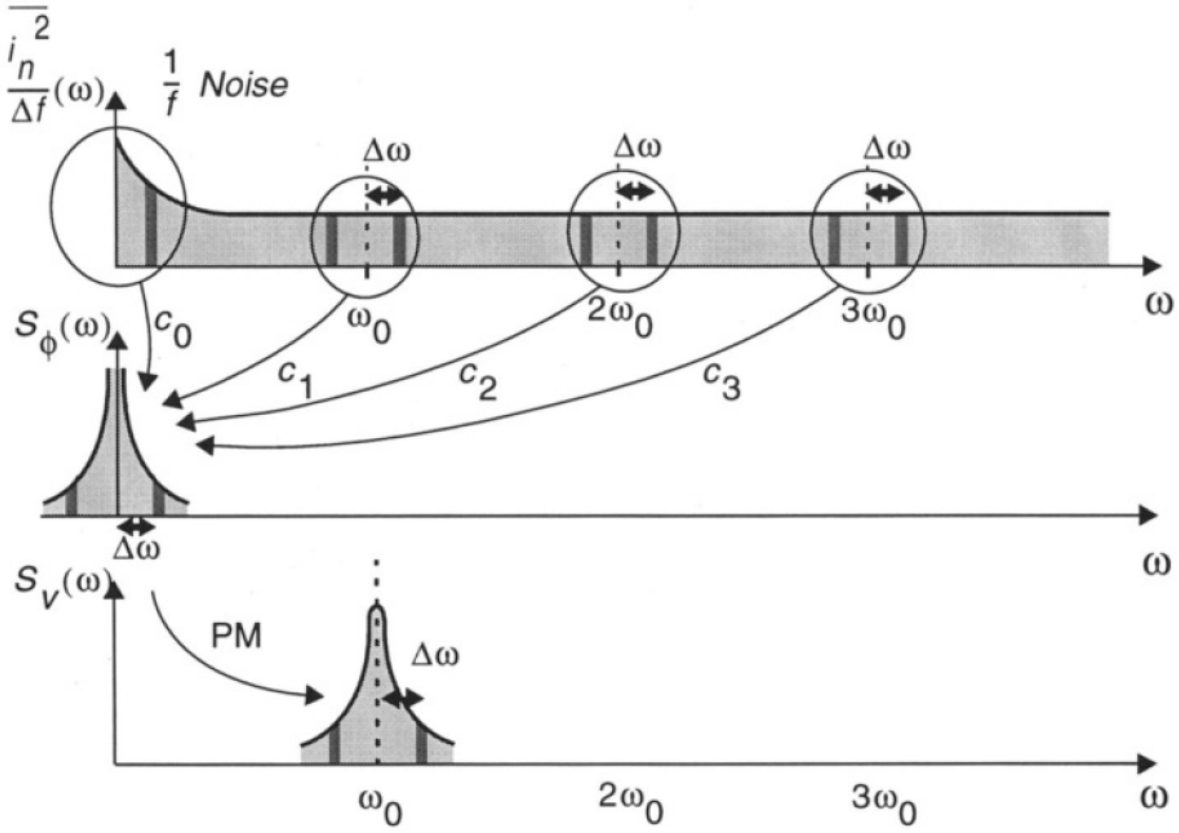


Figure 2.23 Evolution of circuit noise into phase noise.

It is clear from Fig. 2.23 that minimizing the various coefficients c_n (by minimizing the ISF) will minimize the phase noise. To underscore this point quantitatively, we may use Parseval's theorem to write

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \tag{32}$$

so that the spectrum in the $1/f^2$ region may be expressed as

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{\max}^2 \Delta\omega^2}\right) \tag{33}$$

where Γ_{rms} is the rms value of the ISF. All other factors held equal, reducing Γ_{rms} will reduce the phase noise at all frequencies. Equation (33) is the rigorous equation for the $1/f^2$ region and is one key result of the LTV model. Note that no empirical curve-fitting parameters are present in (33).

Calculation of the 1/f^3 Noise Corner

Many active and passive devices exhibit low frequency noise with a power spectrum that is approximately inversely proportional to the frequency. It is for this reason that noise sources with this behavior are referred to as 1/*f* noise.

Noting that device noise in the 1/*f* region can be described by

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \qquad (\Delta\omega < \omega_{1/f}) \tag{34}$$

where $\omega_{1/f}$ is the corner frequency of device 1/*f* noise, (30) and (34) result in the following expression for phase noise in the 1/f^3 portion of the phase noise spectrum:

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f} c_0^2}{8q_{\max}^2 \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right) \tag{35}$$

which describes the phase noise in the 1/f^3 region. The 1/f^3 corner frequency is then

$$\Delta\omega_{1/f^3} = \omega_{1/f} \cdot \frac{c_0^2}{4\Gamma_{rms}^2} = \omega_{1/f} \cdot \left(\frac{\Gamma_{dc}}{\Gamma_{rms}} \right)^2 \tag{36}$$

from which we see that the 1/f^3 phase noise corner is not necessarily the same as the 1/*f* device/circuit noise corner, but is *smaller* by a factor equal to c_0^2 / Γ_{rms}^2 where c_0 is the dc value of ISF,

$$c_0 = \frac{1}{2\pi} \int_0^{2\pi} \Gamma(x) dx \tag{37}$$

it will generally be lower. In fact, since Γ_{dc} is the dc value of the ISF, there is a possibility of reducing *by large factors* the 1/f^3 phase-noise corner.

The ISF is a function of the waveform, and hence potentially under the control of the designer, usually through adjustment of the rise- and fall-time symmetry. This result is not anticipated by LTI approaches, and is one of the most powerful insights conferred by this LTV model. This result has particular significance for technologies with notoriously poor 1/*f* noise performance, such as CMOS and GaAs MESFET's.

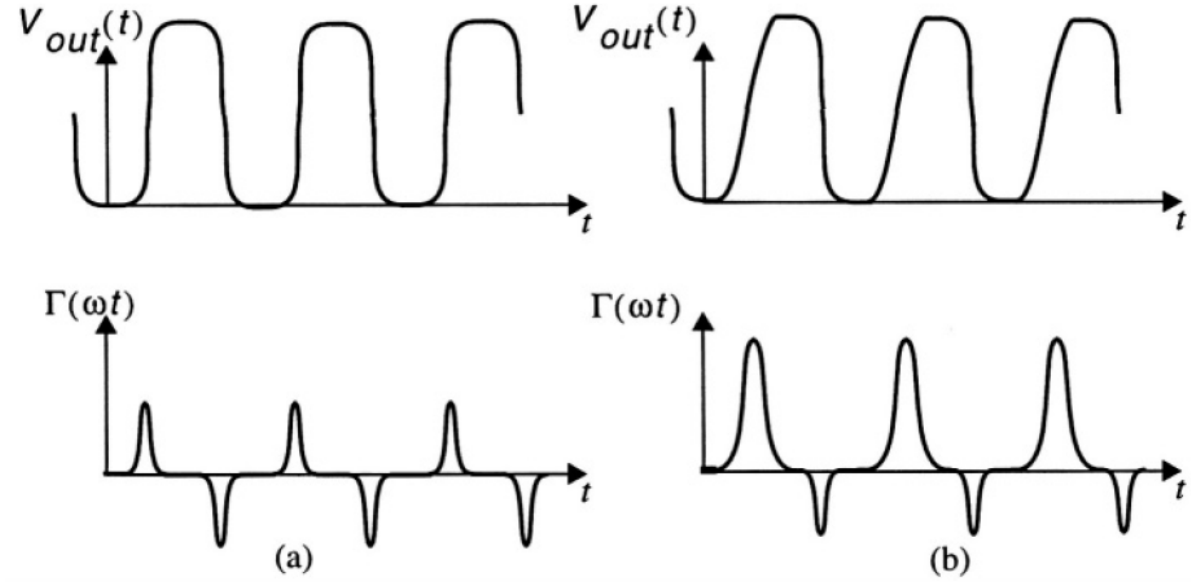


Figure 2.24 (a) Waveform and ISF for the symmetric waveform (b) the asymmetric waveform

To understand what affects c_0, consider two ring oscillators, with waveforms shown in Fig 2.24. The first waveform has symmetric rising and falling edges, *i.e.,* its rise time is the same as its fall-time. Assuming a time-invariant node capacitor1, the sensitivity of this oscillator to a perturbation during the rising edge is the same as its sensitivity during the falling edge, except for a sign. Therefore, the ISF has a small dc value. The second case corresponds to an asymmetric waveform with slow rising edge and a fast falling edge. In this case, the phase is more sensitive during the rising edge, and is also is sensitive for a longer time; therefore, the positive lobe of the ISF will be taller and wider as opposed to its negative lobe which is short and thinner, as shown in Fig. 2.24.

The dc value of the ISF for the asymmetric rising and falling edge is much larger than that in the symmetric case, and hence a low frequency noise source injecting into it shows a stronger upconversion of low frequency noise. A limited case of the effect of odd-symmetric waveforms on phase noise. However minimizing (37) is more a general criterion because although odd-symmetric waveforms may have small c_0 coefficients, the class of waveforms with small c_0 is not limited to those with odd symmetry.

Chapter 3 *Review of Low Power and Low Phase Noise Designs*

3.1 Low Power VCO Design in CMOS

A. Forward Body Bias (FBB) [6]

For deep-submicrometer MOSFETs, the threshold voltage V_t is no longer constant, but influenced by circuit parameters such as gate length, channel width, and drain-to-source voltage due to the short-channel and narrow-channel effects. Typically, transistors with a large channel width and a minimum gate length exhibit a reduced V_t, which is preferable for low-voltage operations. In this VCO topology, the fundamental limitation on the supply voltage is imposed by the threshold voltage of the cross-coupled transistors. To further reduce the supply voltage, the FBB technique is adopted as shown in Fig. 3.1. For a MOSFET device, the threshold voltage is governed by the body effect as

$$V_t = V_{t0} + (\sqrt{2qN_A\varepsilon_s}/Cox)\cdot(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \quad (1)$$

where V_{t0} is the threshold voltage for V_{SB} = 0 V, ϕ_F is a physical parameter with a typical value of 0.4 V, N_A is the substrate doping, and ε_s is the permittivity of silicon. By applying a forward bias voltage to the body through a current-limiting resistor R_B, the effective threshold

voltage is thus reduced while maintaining a minimum forward junction current between the body and the source terminals. The simulated effective threshold voltage and the drain current of a MOSFET with $W = 64 \ \mu$m and $L = 0.18 \ \mu$m are demonstrated in Fig. 3.2, indicating a threshold voltage reduction more than 100 mV due to the FBB technique.

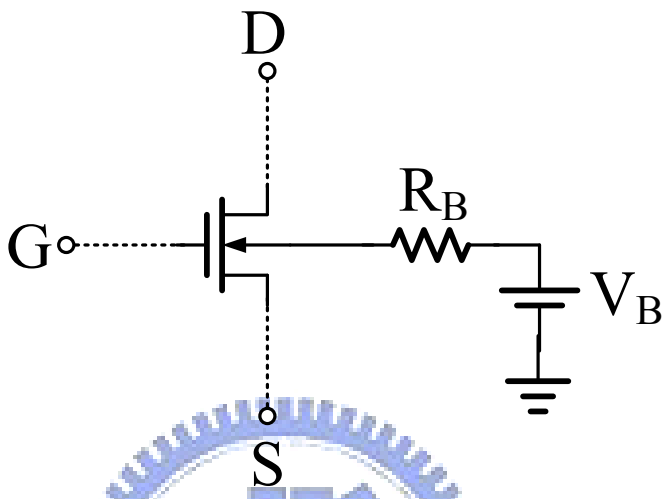


Figure 3.1 Schematic of the FBB

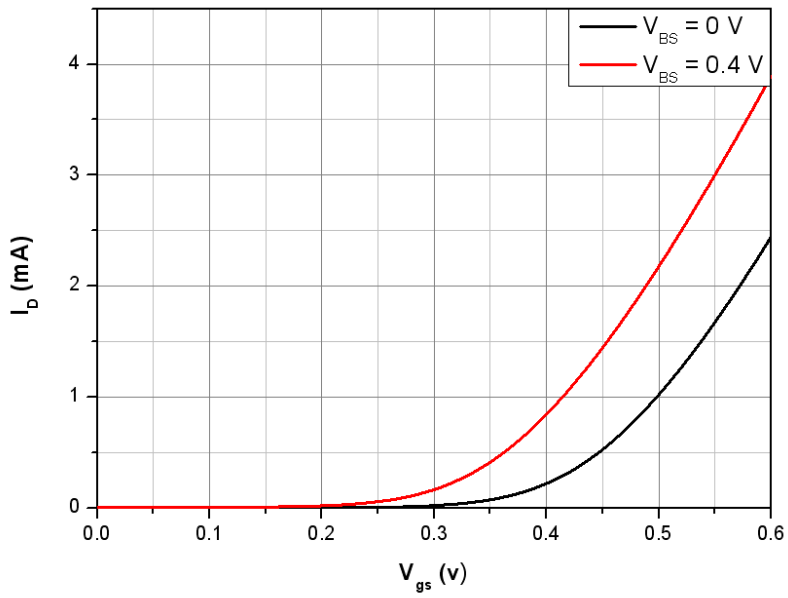


Figure 3.2 I-V characteristics of the MOSFET with and without FBB

B. Dynamic Threshold Voltage MOSFET (DTMOS) [7]

For low power operation at very low voltages, a MOSFET should ideally have a high V_t at $V_{GS} = 0$ to achieve low leakage and low V_t at $V_{GS} = V_{dd}$ to achieve high speed. By tying body and gate of an SO1 MOSFET together, a dynamic threshold voltage MOSFET (DTMOS) is obtained. This device has ideal 60 mV/dec subthreshold swing. DTMOS threshold voltage drops as gate voltage is raised, resulting in much higher current drive than regular MOSFET. DTMOS is ideal for very low voltage (< 0.6 V) operation, as demonstrated by ring oscillator data. DTMOS also solves the floating body problems of SO1 MOSFET such as kinks and V_t stability. Furthermore, carrier mobility is enhanced.

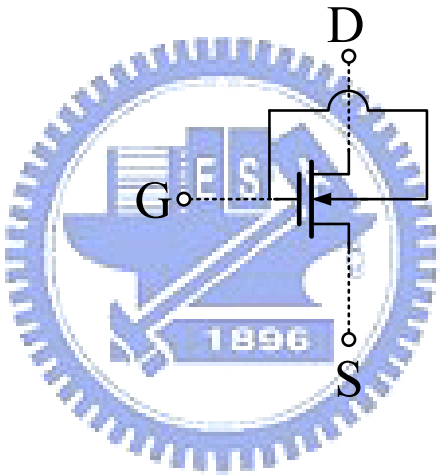


Figure 3.3 Schematic of the DTMOS

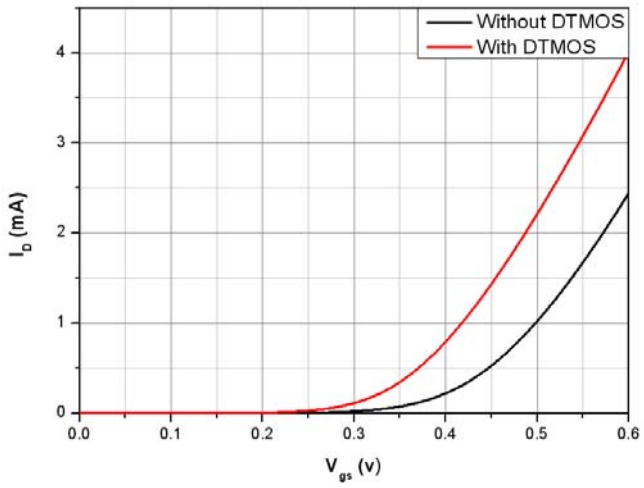


Figure 3.4 I-V characteristics of the MOSFET with and without DTMOS

C. Current-Reuse CMOS Differential LC-VCO [8]

Figure 3.5 shows schematics the current-reuse differential LC-VCO. The series stacking of N- and P-MOSFETs allows the supply current to be reduced by half compared to that of the conventional LC VCO while providing the same negative conductance.

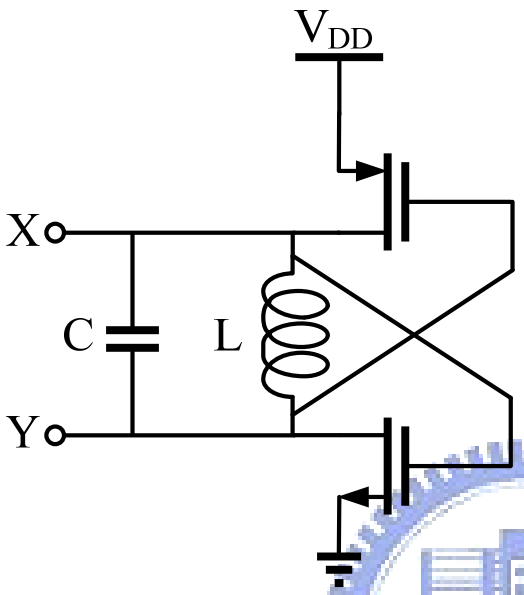


Figure 3.5 Schematic of the Current-Reuse VCO

3.2 Low Phase Noise VCO Design in CMOS

A. A Low Phase-Noise CMOS VCO With Harmonic Tuned *LC* Tank [4]

The filtering, by parallel resonation at $2f_0$ frequency using an inductor with the parasitic capacitor at the common source, stops the differential-pair FETs in the triode region from loading the resonator, preventing the degradation of the resonator Q. As shown in Fig. 3.6, an L_s is used to make a parallel resonation with the parasitic capacitance C_p at $2f_0$ frequency. This technique has an independent phase-noise reduction effect and the combination of the harmonic tuning and filtering techniques can reduce the phase noise significantly for $1/f^3$ and $1/f^2$ regions. Using these techniques, a complementary VCO is designed to achieve the minimum phase noise. The phase-noise simulation results in Fig. 3.7 show the phase-noise reduction effect of each technique independently and also that of the combined case.

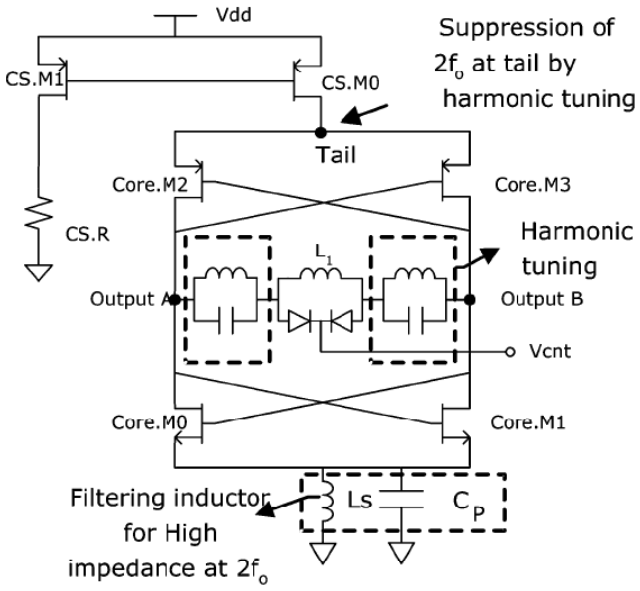


Figure 3.6 Simplified schematic diagrams of optimized HT VCO.

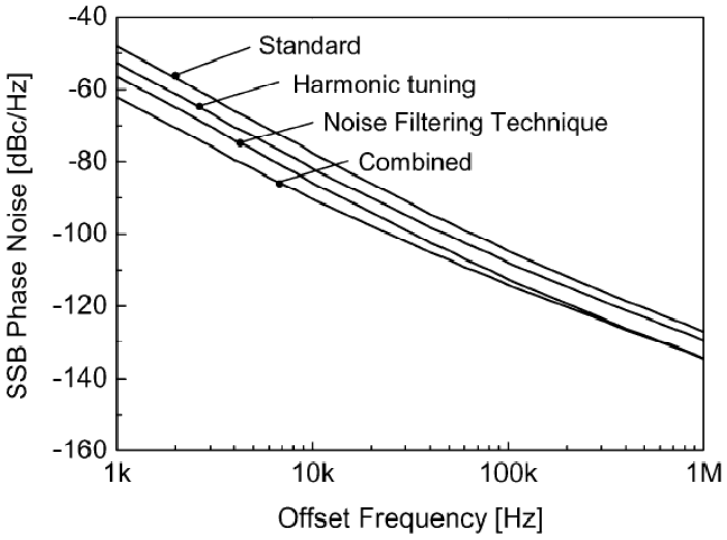


Figure 3.7 Simulated phase-noise results for each technique.

B. Effects of Forward Body Bias on High-Frequency Noise in 0.18-μm CMOS Transistors [3]

The effects of FBB on the high-frequency noise in 0.18-μm, MOS transistors have been investigated. Although MOSFET dc performance could be improved when the substrate is forward biased, significant degradation of RF noise was observed in both N and PMOS devices. The increase in high-frequency noise with was qualitatively explained by considering the contributions from nonequilibrium channel noise and substrate resistance noise. The increase in RF noise in PMOS noise was found to be strongly correlated to the substrate resistance noise, while the increase in RF noise in NMOS was attributed to a combinational effect of substrate resistance noise and channel noise. Our experimental results in this study suggest that, for RF circuit applications, a forward body biasing scheme is not favorable if high-frequency noise is an important concern.

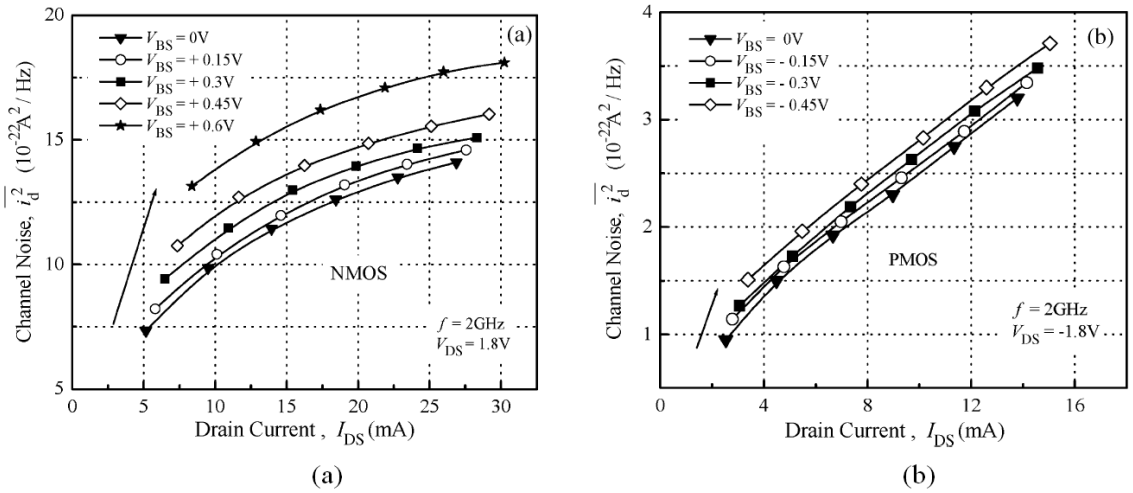


Figure 3.8 Channel noise $\overline{i_d^2}$ against drain current I_{DS} as a function of body bias V_{BS}. (a) NMOS. (b) PMOS.

Chapter 4 *Proposed Low Power, Low Voltage and Low Phase Noise VCO*

4.1 INTRODUCTION

Among the building blocks of a radio frequency (RF) transceiver, the voltage-controlled oscillator (VCO) is an important block since it affects the system performance of the transceiver to a large extent. In designing a VCO, low power consumption and low phase noise are two important parameters. The low power consumption may be achieved by reducing the supply voltage and/or the current in the VCO core circuit. Forward body bias (FBB) has been proposed as an effective method for improving the device performance in MOSFETs. Forward bias the body to source voltage V_{BS} and source to body voltage V_{SB} of NMOS and PMOS reduce the threshold voltage (V_t). The increase in high frequency noise with $|V_{BS}|$ was qualitatively explained by considering the contributions from nonequilibrium channel noise and substrate resistance noise in 0.18 μm CMOS transistors. Therefore, in RF circuit applications, an FBB scheme is not favorable if high frequency noise is an important concern [3].

However, the low voltage limits the signal amplitude, which in turn limits the signal-to-noise ratio (SNR) and leads to an increase of the phase noise of the VCO. There is a tradeoff between the VCO phase noise and power consumption due to the degradation of the phase noise with the increased VCO gain needed for a larger power consumption. Therefore,

how to control a low phase noise effectively at the low power level becomes an important and challenging issue. [4] suggests adding an external circuit called a harmonic tuned (HD) LC tank to suppress the harmonic frequency of the circuit. This method can reduce the phase noise effectively, but it also increases both the die area and power consumption.

In this chapter, a low power, low voltage and low phase noise LC-VCO circuit is proposed. An external negative-resistance cell is also added between the different outputs, which can effectively reduce both the power consumption, supply voltage and the phase noise. The proposed LC-VCO is validated by an implementation using the TSMC 0.18 μm 1P6M process.

4.2.1 Current-reused VCO with Low Power and Low voltage

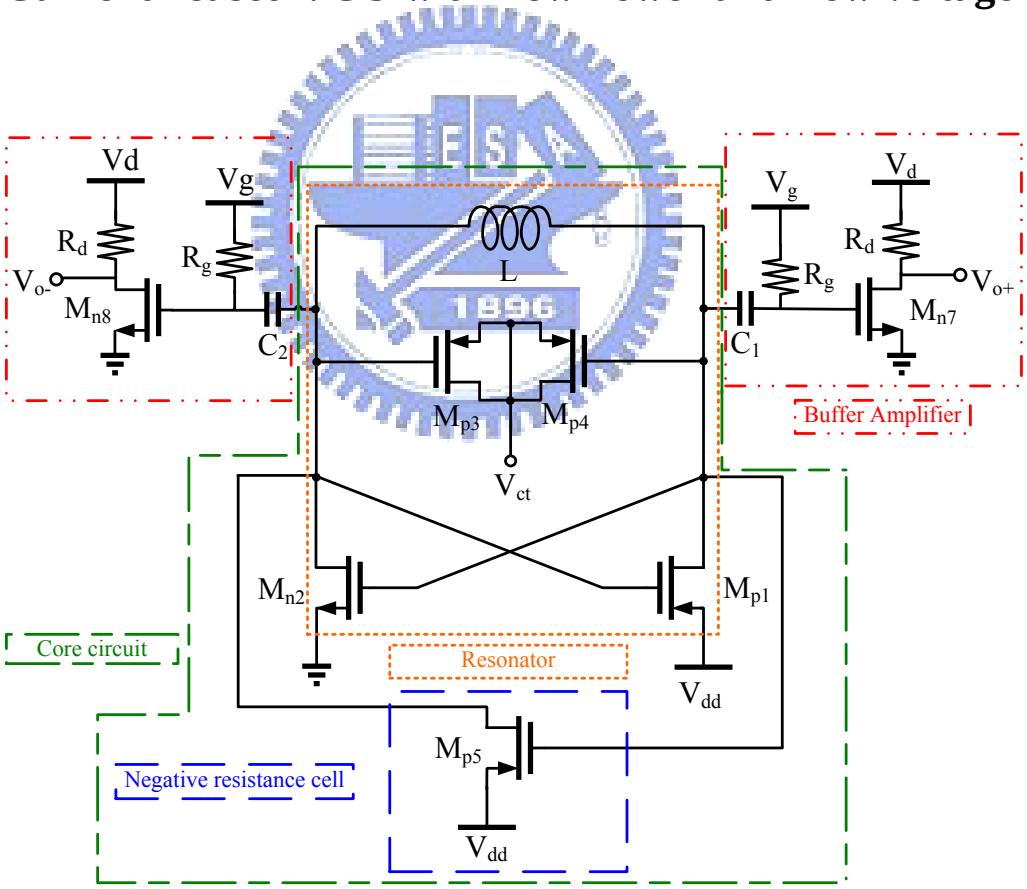


Figure 4.1 Proposed VCO1 circuit.

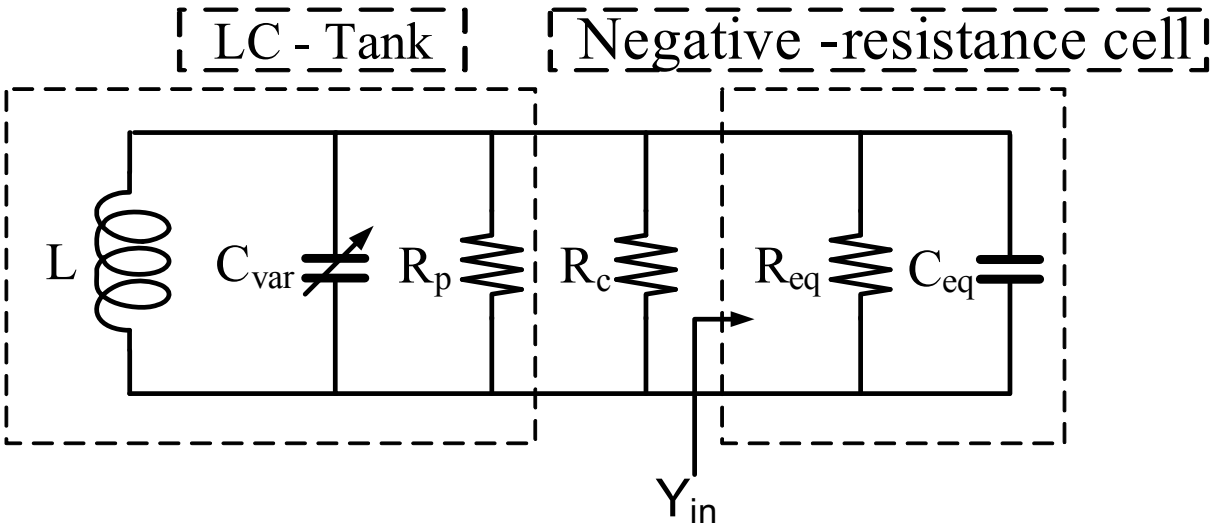


Figure 4.2 Parallel LC oscillator model of the proposed VCO1.

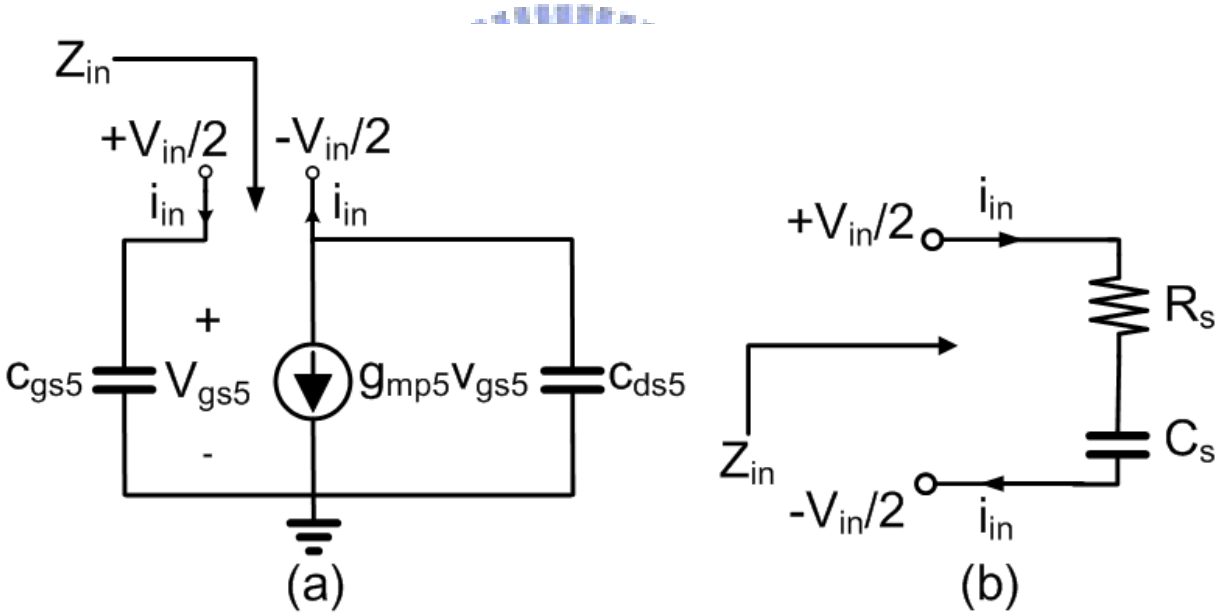


Figure 4.3 (a) Negative-resistance cell circuit; (b) Series circuit model of the negative-resistance cell.

Our design, as shown in Fig. 4.1, adds a negative-resistance cell (M_{p5} and C_{gs5}-C_{ds5}) shunt to the L-C tank to a current-reuse topology (M_{p1}-M_{n2}) [8], which effectively enlarges the negative resistance and leads to the reduction of both the core power consumption, supply voltage and phase noise of the VCO. Fig. 4.2 shows a simplified equivalent circuit of the proposed VCO shown in Fig.1 in the steady state, where the resistance R_p represents the tank loss. R_c is the negative resistance created by the current-reused topology, which is

approximately equal to $-(1/g_{mN1} + 1/g_{mP2})$. R_{eq} and C_{eq}, which represent the equivalent resistance and capacitance of the negative-resistance cell, are given by

$$R_{eq} = -\frac{\omega^2 (C_{gs5} + C_{ds5})^2 + g_{m5}}{\omega^2 C_{gs5} C_{ds5}} \tag{1}$$

$$C_{eq} = C_{gd5} + \frac{C_{gs5} C_{ds5}}{C_{gs5} + C_{ds5} + \frac{g_{m5}^2}{\omega^2 (C_{gs5} + C_{ds5})}} \tag{2}$$

where g_{m5} is the transconductance of M_{p5}, the symbols (C_{gs5} , C_{ds5}) represent the (gate-source, drain-source) capacitor of pMOS M_{p5} and ω is the operating frequency. They are derived by using a small-signal model as shown in Fig. 4.3(a). The series circuit mode of the cell circuit is given in Fig. 4.3(b) and then the input impedance of the differential negative-resistance cell, $Z_{in} = v_{in}/i_{in}$, is given by

$$Z_{in} = -\frac{g_{m5}}{\omega^2 C_{gs5} C_{ds5}} + \frac{1}{j\omega}\left(\frac{1}{C_{gs5}} + \frac{1}{C_{ds5}}\right) = R_s + \frac{1}{j\omega C_s} \tag{3}$$

Therefore,

$$R_s = -\frac{g_{m5}}{\omega^2 C_{gs5} C_{ds5}}, \quad C_s = \frac{C_{gs5} C_{ds5}}{C_{gs5} + C_{ds5}}$$

In order to simplify the analysis, conductance Y_{in} is given as $1/Z_{in}$, and Y_{in} is defined as $1/R_{eq} + j\omega C_{eq}$. With Eq. (3), R_{eq} and C_{eq} are given by

$$R_{eq} = R_s + \frac{1}{\omega^2 R_s C_s^2}, \quad C_{eq} = \frac{C_s}{\omega^2 R_s C_s R_{eq} + 1} \tag{4}$$

Thus, equations (1) and (2) are derived. By tuning W/L for MOSFET (M_{p5}) in the typical design, we can easily achieve $g_{m5} \gg \omega^2 (C_{gs5} + C_{ds5})^2$ and $(C_{gs5} + C_{ds5}) \gg \frac{g_{m5}^2}{\omega^2 (C_{gs5} + C_{ds5})}$.

Then, (1) is simplified and given by

$$R_{eq} \approx -\frac{g_{m5}}{\omega^2 C_{gs5} C_{ds5}} \tag{5}$$

$$C_{eq} \approx C_{gd5} + \frac{C_{gs5}C_{ds5}}{C_{gs5} + C_{ds5}} \tag{6}$$

In (5), the magnitude of the negative resistance R_{eq} is inversely proportional to the square of ω and is linearly proportional to the transconductance of M_{p5} which is proportional to the transistor current. This means that the larger the frequency or the smaller current is, the larger the negative resistance is, which shows that our proposed circuit can achieve a much larger negative resistance than conventional designs in RF circuit applications. The small current flow has the advantage of a low power consumption. To analyze the effect of the negative resistance on the phase noise level, the pioneering work by Hajimiri and Lee is applied to evaluate the phase noise L of the circuit at an offset frequency Δω from the carrier [5]. L is given by

$$L(\Delta\omega) = 10\log\left(\frac{\overline{i_n^2}\Gamma_{rms}^2}{2\Delta\omega^2 C_{eq}^2 A_{tank}^2}\right) \tag{7}$$

with A_{tank} being the oscillation amplitude across the resonator. C_{eq} is the tank capacitance, and Γ_{rms} is the root mean square value of the impulse sensitivity function (ISF). Equation (7) demonstrates that a larger C_{eq} of the resonant tank results in a lower phase noise. In (6), C_{gs5} and C_{ds5} are equivalent to C_{eq} by using a negative-resistance cell. Thus can lower the phase noise.

4.3 EXPERIMENTAL RESULTS

The die microphotograph of the proposed VCO is shown in Fig. 4.4, where the proposed VCO is fabricated by using the TSMC 0.18 μm CMOS process. Its die area is 0.67× 0.81 mm^2 including the pads. An on-wafer measurement is carried out for RF characterization. The measured oscillation frequencies cover 3.6 GHz to 3.4 GHz while the control voltage Vct is changed from 0 V to 1.3 V, as shown in Fig. 4.5. Fig. 4.6 shows the VCO output spectrum

with values of -5 dBm. As shown in Fig. 7, the measured phase noise of the proposed VCO is about -116.89 dBc/Hz at 1MHz offset frequency. The power consumption of the proposed VCO core is 0.54 mW at the supply voltage of 0.93 V. The figure of merit (FOM) of the proposed VCO is -190.4 dBc/Hz with the FOM defined by

$$FOM = L\{\Delta f\} + 10 \times \log\left(\frac{P_{DC}}{1mW}\right) - 20 \times \log\left(\frac{f_0}{\Delta f}\right) \quad (8)$$

where f_0 is the oscillating frequency, Δf is the offset frequency, $L\{\Delta f\}$ is the measured phase noise at Δf, and P_{DC} is the DC power consumption of VCOs in mW. Table I summarizes the measured phase noise (PN), f_0, power consumption and FOM of the proposed VCO and other published results. The comparison shows that our proposed work yields very low power consumption and achieve a high FOM performance.

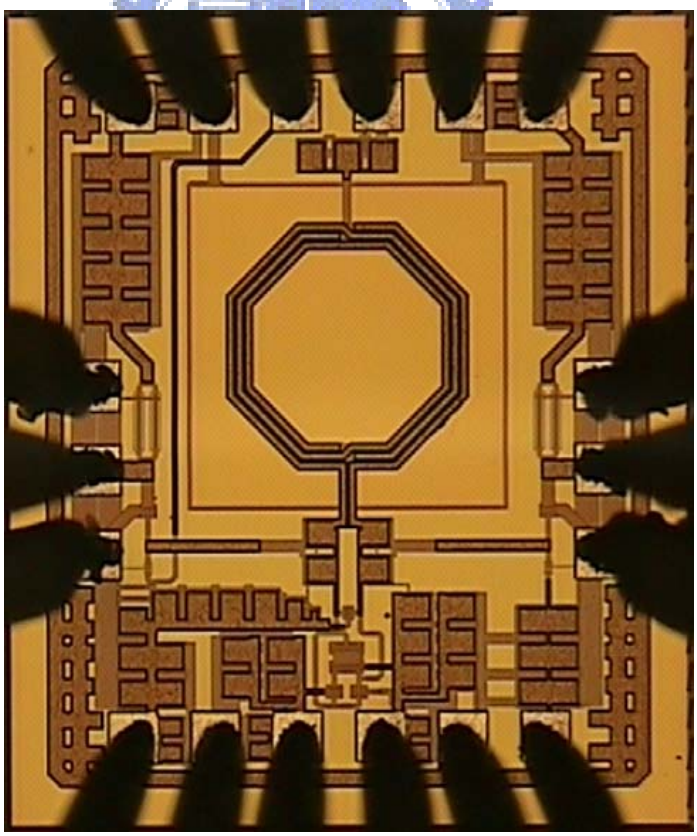


Figure 4.4 Microphotograph of the VCO1.

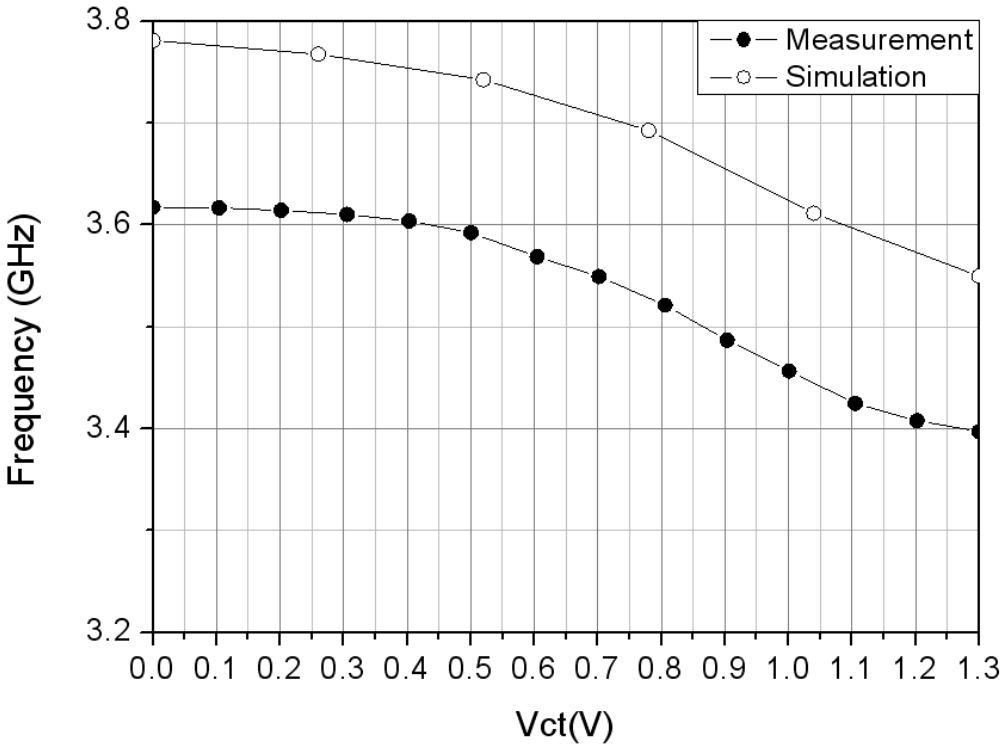


Figure 4.5 Measure tuning range of the VCO1.

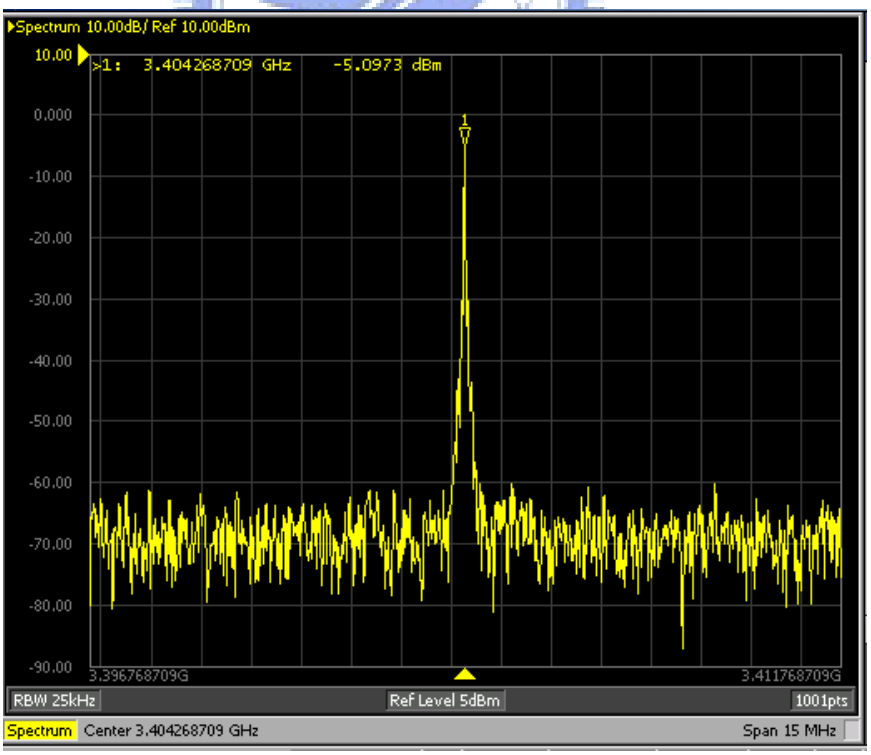


Figure 4.6 Measured the VCO1 output spectrum at 3.5 GHz.

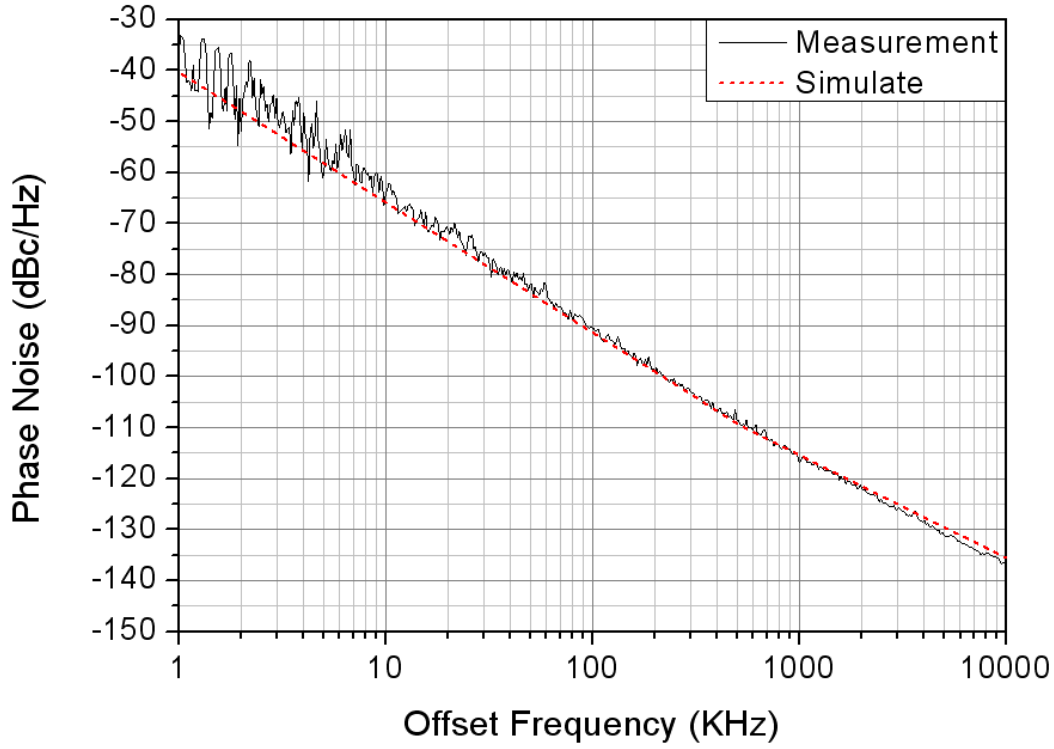


Figure 4.7 Measured phase noise versus offset frequency of the VCO1 at 3.5 GHz.

TABLE I

Current-reused VCO with Low Power and Low voltage MEASURED PERFORMANCE SUMMARY AND COMPARISON

Ref.	CMOS Technology (μm)	Freq. (GHz)	Phase Noise @ 1-MHz offset (dBc/Hz)	P_{DC} (mW)	FOM (dBc/Hz)
[9] MWCL 2005	0.18	4.96-5.32 4.98-5.45	-116.71 -110.02	3.9 2.59	-185 -180
[6] MTT2007	0.18	5.6	-118	3	-189
[10] MWCL 2007	0.18	2.01	-124	2.2	-186.7
[11] CASII 2008	0.18	2.17-2.73	-122.3	2.7	-186.3
[12] MWCL 2009	0.18	5.6	-119.13	2.4	-190
[13]MWCL 2009	0.18	5.46	-120.2	6.4	-187
[14]MWCL 2009	0.18	2.93-3.62	-122	1.7	-190
VCO1	0.18	3.5	-116.89	**0.54**	**-190.4**

4.4 Current reused VCO with Low Power and Low Phase Noise

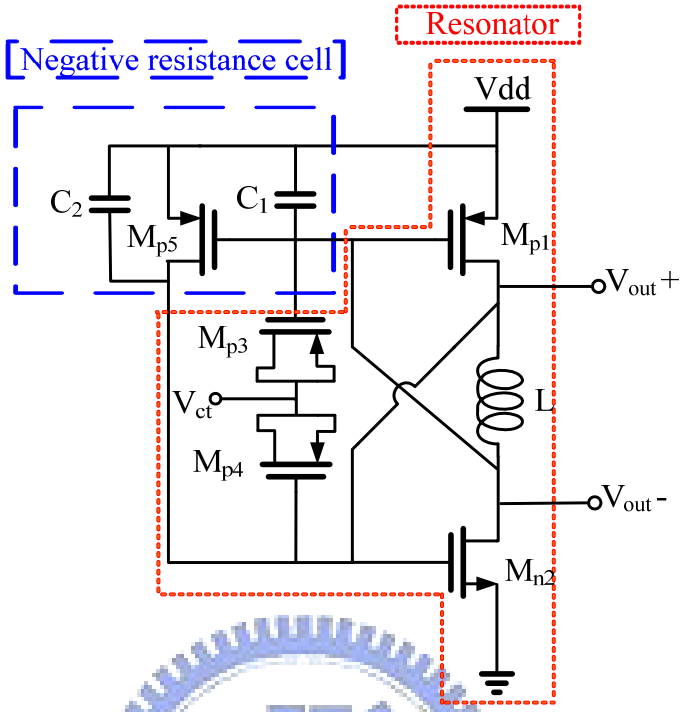


Figure 4.8 Proposed VCO2 circuit.

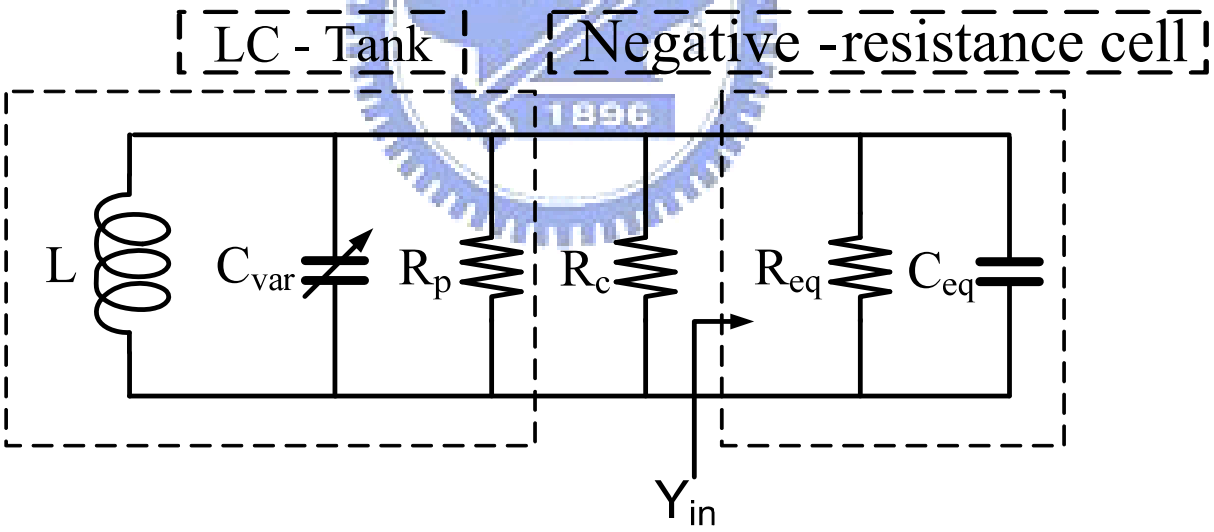


Figure 4.9 Parallel LC oscillator model of the proposed VCO2.

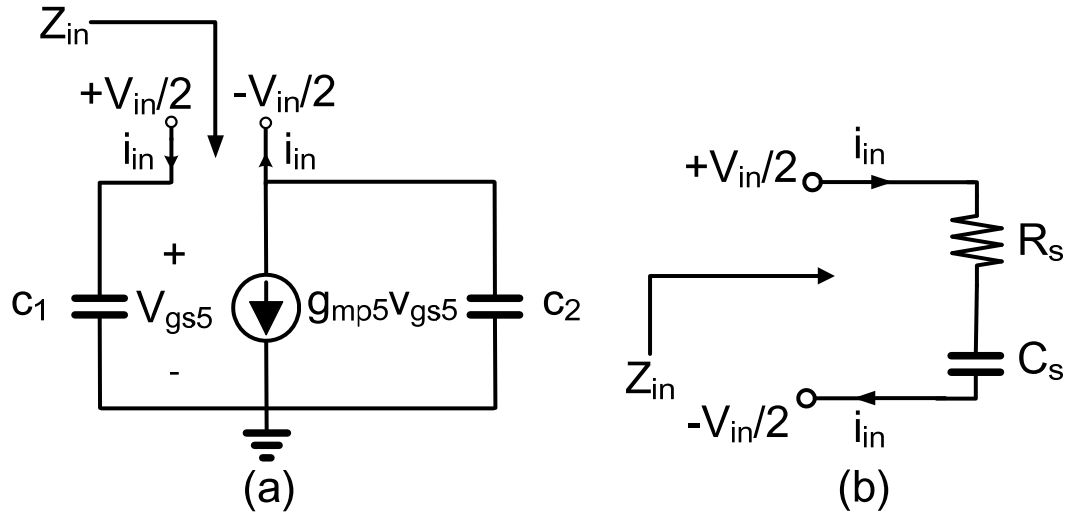


Figure 4.10 (a) Negative-resistance cell circuit; (b) Series circuit model of the negative-resistance cell.

$$R_{eq} \approx -\frac{g_{m5}}{\omega^2 C_1 C_2} \tag{8}$$

$$C_{eq} \approx \frac{\omega^2}{g_{m5}} \frac{C_1 C_2}{C_1 + C_2} \tag{9}$$

Form (9), C_1−C_2 can be enlarged to C_{eq} by using a negative-resistance cell, and C_{eq} is positively correlated with $(\omega/g_{m5})^2$ without any additional capacitance and thus can lower the phase-noise.

4.5 EXPERIMENTAL RESULTS

The die microphotograph of the proposed VCO is shown in Fig. 4.11, where the proposed VCO is fabricated by using the TSMC 0.18 μm CMOS process. Its die area is 0.56× 0.71 mm^2 including the pads. An on-wafer measurement is carried out for RF characterization. The measured oscillation frequencies cover 2.52 GHz to 2.41 GHz while the control voltage Vct is changed from 0 V to 1.3 V, as shown in Fig. 4.12. Fig. 4.13 shows the VCO output spectrum with values of -3.5 dBm. As shown in Fig. 4.14, the measured phase noise of the proposed VCO is about -125 dBc/Hz at 1MHz offset frequency. The power consumption of the proposed VCO core is 1.9 mW at the supply voltage of 1 V.

The figure of merit (FOM) of the proposed VCO is -190 dBc/Hz with the FOM defined by

$$FOM = L\{\Delta f\} + 10 \times \log\left(\frac{P_{DC}}{1mW}\right) - 20 \times \log\left(\frac{f_0}{\Delta f}\right) \quad (10)$$

where f_0 is the oscillating frequency, Δf is the offset frequency, $L\{\Delta f\}$ is the measured phase noise at Δf, and P_{DC} is the DC power consumption of VCOs in mW. Table II summarizes the measured phase noise (PN), f_0, power consumption and FOM of the proposed VCO and other published results. The comparison result shows that our proposed work yields very low phase noise even with a relatively low power consumption, and shows the best FOM performance.

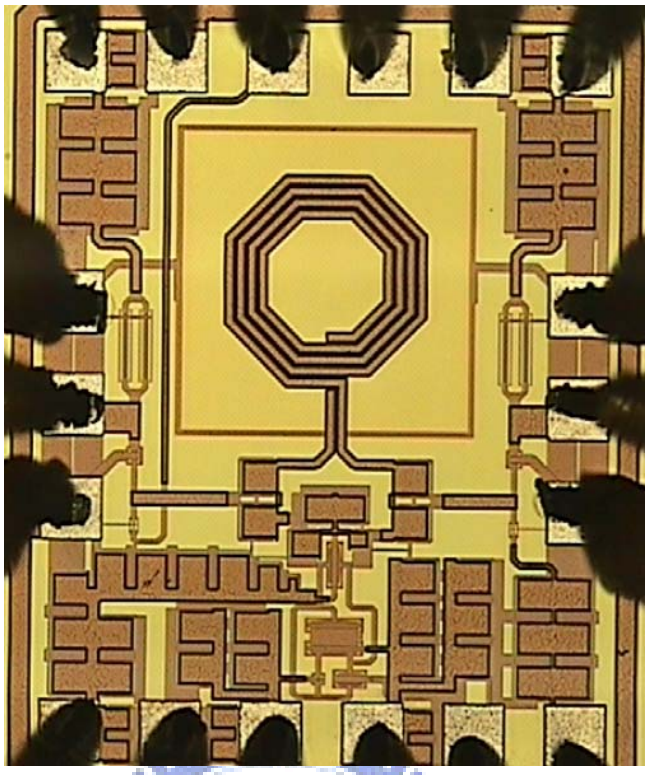


Figure 4.11 Microphotograph of the VCO2.

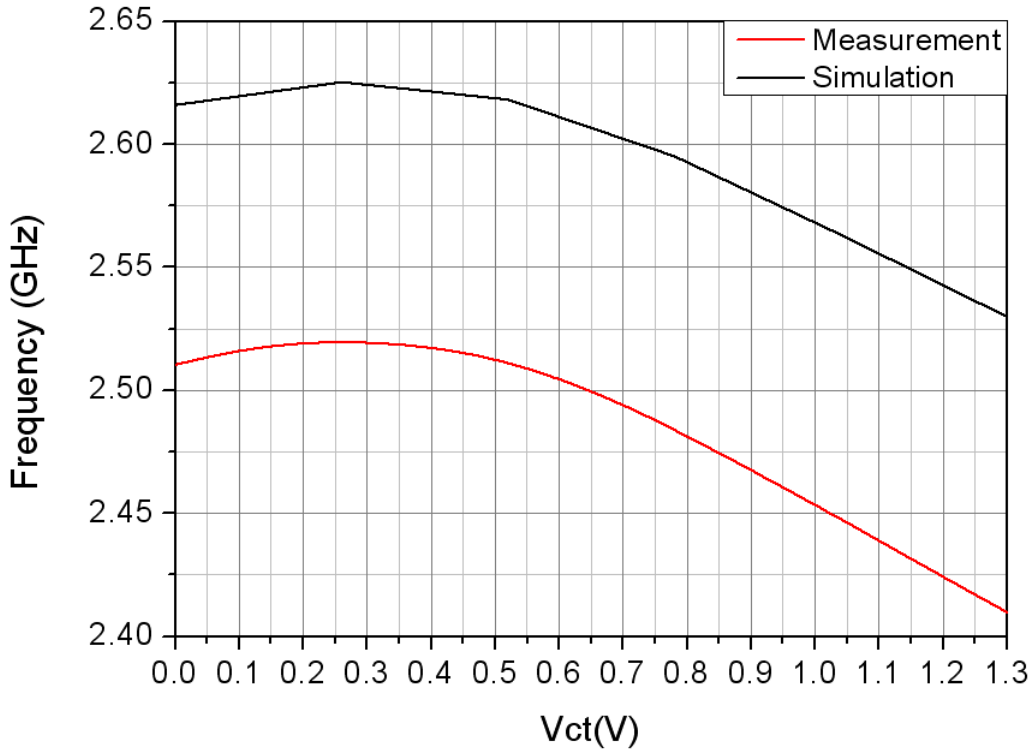


Figure 4.12 Measure tuning range of the VCO2.

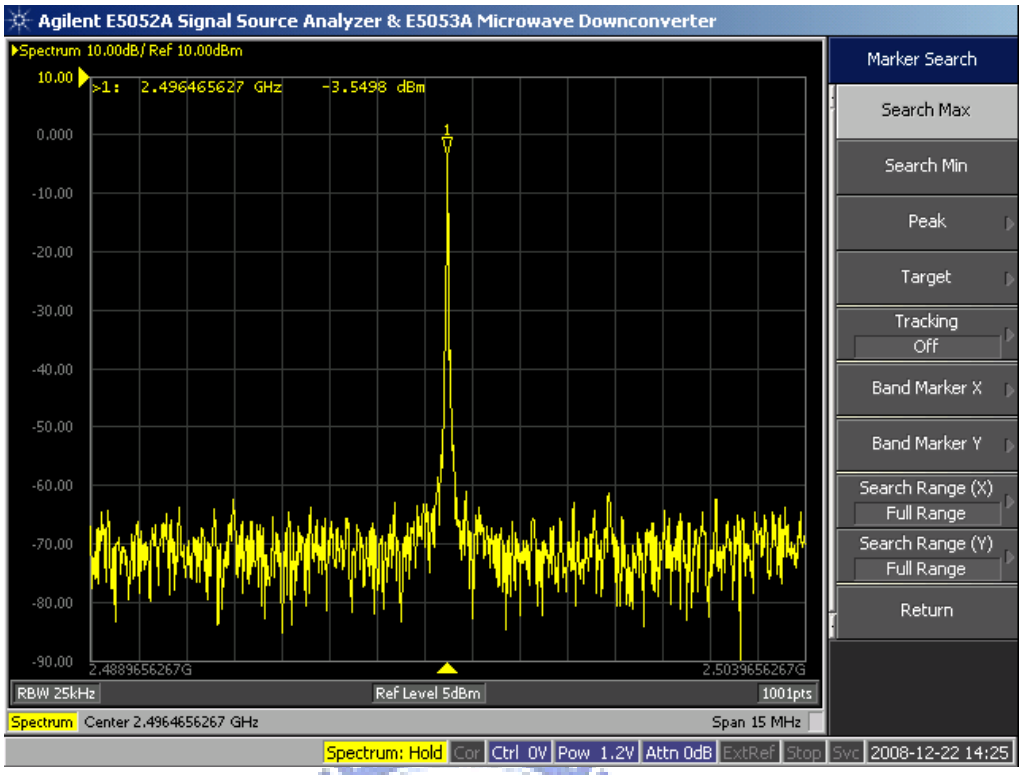


Figure 4.13 Measured the VCO2 output spectrum at 2.4 GHz.

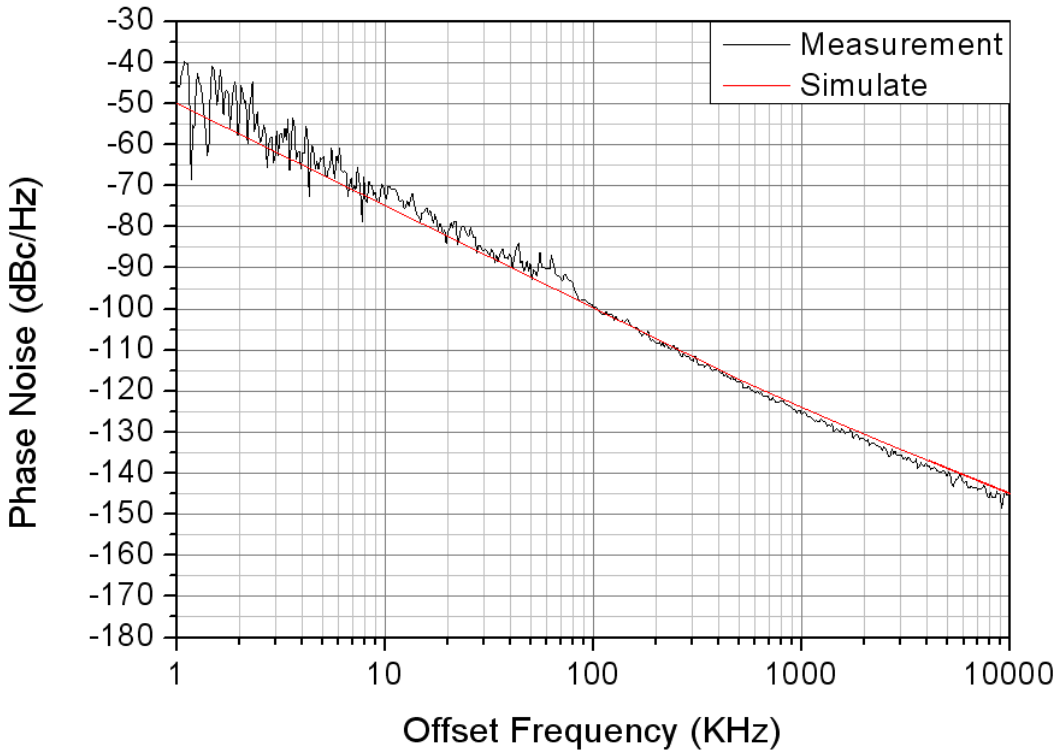
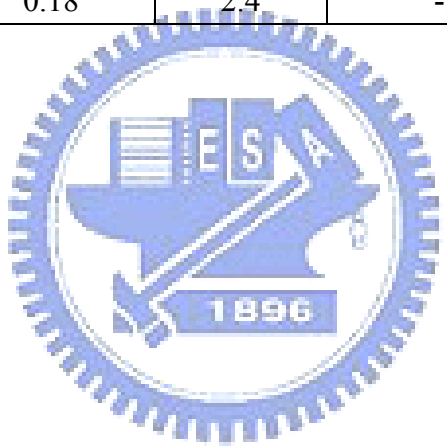


Figure 4.14 Measured phase noise versus offset frequency of the VCO2 at 2.4 GHz.

TABLE II

Current reused VCO with Low Power and Low Phase Noise MEASURED PERFORMANCE SUMMARY AND COMPARISON

Ref.	CMOS Technology (μm)	Freq. (GHz)	Phase Noise @ 1-MHz offset (dBc/Hz)	P_{DC} (mW)	FOM (dBc/Hz)
[9] MWCL 2005	0.18	4.96-5.32 4.98-5.45	-116.71 -110.02	3.9 2.59	-185 -180
[6] MTT2007	0.18	5.6	-118	3	-189
[10] MWCL 2007	0.18	2.01	-124	2.2	-186.7
[11] CASII 2008	0.18	2.17-2.73	-122.3	2.7	-186.3
[12] MWCL 2009	0.18	5.6	-119.13	2.4	-190
[13]MWCL 2009	0.18	5.46	-120.2	6.4	-187
[14]MWCL 2009	0.18	2.93-3.62	-122	1.7	-190
VCO2	0.18	2.4	**-125**	1.9	**-190**



Chapter 5 *Conclusion*

A low power、low voltage and low phase noise LC-VCO operating at 2.5 GHz and 3.5 GHz is proposed and implemented by TSMC 0.18-μm 1P6M CMOS process. Our design, based on a current-reused topology and adding a negative-resistance cell shunt to the L-C tank, can effectively reduce of both the power consumption and supply voltage. With the current-reused topology, the proposed LC-VCO can operate using only half amount of DC current compared with the conventional topologies. An external negative-resistance cell is also added between the different outputs, which can effectively reduce both the power consumption and supply voltage. The proposed LC-VCO consumes 1.9 mW and 0.54 mW at 2.5 GHz and 3.5 GHz, respectively. The measured phase noise at 1 MHz offset frequency is -125 dBc/Hz and -116.89 dBc/Hz in the 2.5 GHz and 3.5 GHz. The FoM of proposed LC-VCO is -190 dBc/Hz and -190.4 dBc/Hz at operating frequency 2.5 GHz and 3.5 GHz, respectively. Although the power consumption is obviously improved, there is still a lot of space for noise reduction. Several extensive studies have been underway to further reduce phase noise of LC-VCOs. In this field, it may be worth our effort in the future works, such as low phase noise LC-VCOs.

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Appendix A *Basic Oscillator Theory*

Ring Oscillators

Ring oscillators employing more than three stages are also feasible. The total number of inversions in the loop must be odd so that the circuit does not latch up. For example, as shown in Fig A.1(a), a ring can incorporate N inverters, providing a frequency of $1/(2NT_D)$. On the other hand, the differential implementation can utilize an even number of stages by simply configuring one stage such that it does not invert. Illustrated in Fig A.1(b), this flexibility demonstrates another advantage of differential circuits over their single ended counterparts.

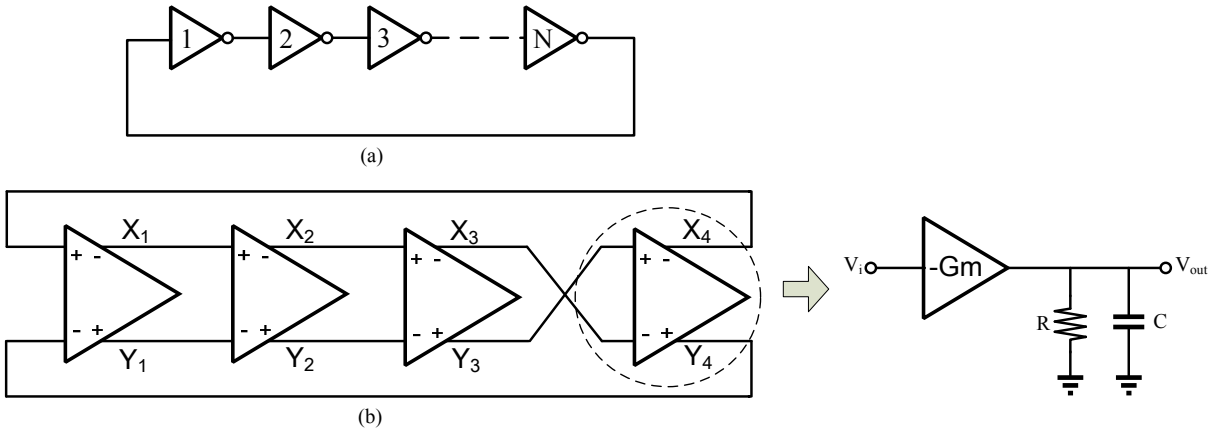

Figure A.1 (a) N-stage single ended ting oscillator, (b) four-stage differential ring oscillator

Let $A = G_m R$ $\omega_p = \frac{1}{RC}$

$$H(s)=\frac{V_{out}}{V_i}=-\frac{-G_mR}{1+sRC}=\frac{-A}{1+s/\omega_p} \tag{1}$$

$$H(j\omega)=\frac{-A}{1+j\omega/\omega_p}=\frac{-A}{\sqrt{1+(\frac{\omega}{\omega_p})^2}e^{i\theta}} \quad \text{where} \quad \theta=\tan^{-1}\frac{\omega}{\omega_p}$$

N-Stage loop gain $$[H(j\omega)]^N=\frac{(-1)^N A^N}{\left[1+(\frac{\omega}{\omega_p})^2\right]^{N/2}}e^{iN\theta} \tag{2}$$

Assume N is an odd number, according to Barkhausen criterion

$$|H(j\omega)|^N \geq 1 \Rightarrow A \geq \sqrt{1+(\frac{\omega}{\omega_p})^2} \qquad \angle[H(j\omega)]^N = 2k\pi \tag{3}$$

To find minimum gain A, we have

$$N\theta=\pi \Rightarrow \theta=\frac{\pi}{N} \qquad A \geq \sqrt{1+\tan^2\frac{\pi}{N}} \Rightarrow A \geq \sec\frac{\pi}{N} \tag{4}$$

If N=3, A must $\geqq$ 2

If N=4, A must $\geqq \sqrt{2}$

LC Oscillators

As shown in Fig A.2(a), an inductor L_1 placed in parallel with a capacitor C_1 resonates at a frequency $\omega_{res}=1/\sqrt{L_1C_1}$. At this frequency, the impedances of the inductor, $jL_1\omega_{res}$, and the capacitor, $jC_1\omega_{res}$, are equal and opposite, thereby yielding an infinite impedance. We say the circuit has an infinite quality factor, Q. In practice, inductors and capacitors suffer from resistive components. For example, the series resistance of the metal wire used in the inductor can be modeled as shown in Fig A.2(b). We define the Q of the inductor as $L_1\omega/R_s$. For this circuit, the reader can show that the equivalent impedance is given by

$$Z_{eq}(s)=\frac{R_s+L_1s}{1+L_1C_1s^2+R_sC_1s} \tag{5}$$

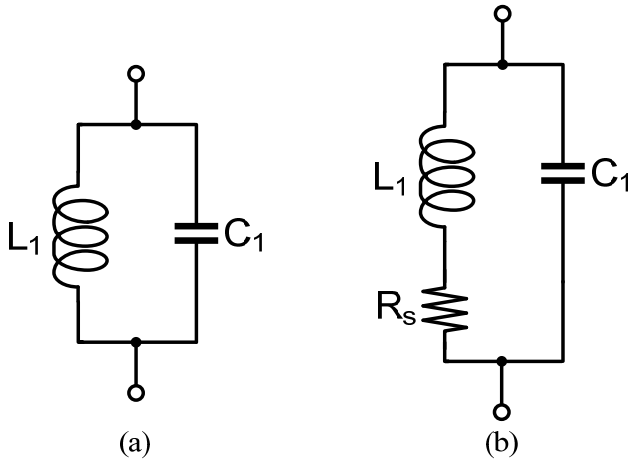

Figure A.2 (a) Ideal and (b) realistic LC tanks

and hence,

$$\left|Z_{eq}(s=j\omega)\right|^2 = \frac{R_s^2 + L_1^2\omega^2}{(1+L_1C_1\omega^2)^2 + R_s^2C_1^2\omega^2} \tag{6}$$

That is, the impedance does not go to infinity at any s=jω. We say the circuit has a finite Q. The magnitude of Z_{eq} in (6) reaches a peak in the vicinity of $\omega = 1/\sqrt{L_1C_1}$, but the actual resonance frequency has some dependency on R_s.

The circuit of Fig A.2(b) can be transformed to an equivalent topology that more easily lends itself to analysis and design. To this end, we first consider the series combination shown in Fig A.3(a). For a narrow frequency range, it is possible to convert the circuit to the parallel configuration of Fig A.3(b). For the two impedances to be equivalent:

$$L_1 s + R_s = \frac{R_p L_p s}{R_p + L_p s} \tag{7}$$

Considering only the steady state response, we assume s=jω and rewrite (7) as

$$(L_1R_p + L_pR_s)j\omega + R_sR_p - L_1L_p\omega^2 = R_pL_pj\omega \tag{8}$$

This relationship must hold for all values of ω, mandating that

$$L_1R_p + L_pR_s = R_pL_p \tag{9}$$

$$R_sR_p + L_1L_p\omega^2 = 0 \tag{10}$$

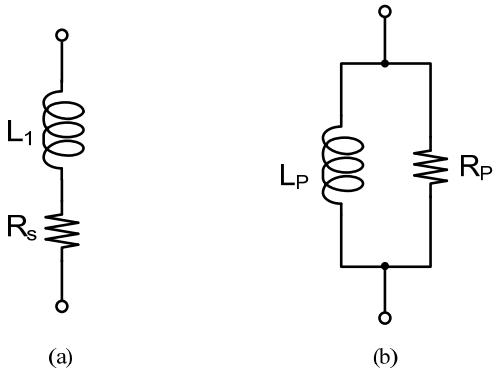

Figure A.3 Conversion of a series combination to a parallel combination

Calculating R_p from the latter and substituting in the former, we have

$$L_p = L_1(1+\frac{R_s^2}{L_1^2\omega^2}) \tag{11}$$

Recall that $L_1\omega/R_s=Q$, a value typically greater than 3 for monolithic inductors. Thus,

$$L_p \approx L_1 \tag{12}$$

and

$$R_p \approx \frac{L_1^2\omega^2}{R_s} \approx Q^2 R_s \tag{13}$$

In other words, the parallel network has the same reactance but a resistance Q^2 times the series resistance.

Let us now consider the tuned stage of Fig A.4(a), where an LC tank operates as the load. At resonance, $jL_p\omega=1/(jC_p\omega)$ and the voltage gain equals $-g_{m1}R_p$. The phase shift approach +90° at very low frequency and -90° at very high frequency. At resonance, the total phase shift around the loop is equal to 180°. Thus, the circuit does not oscillate.

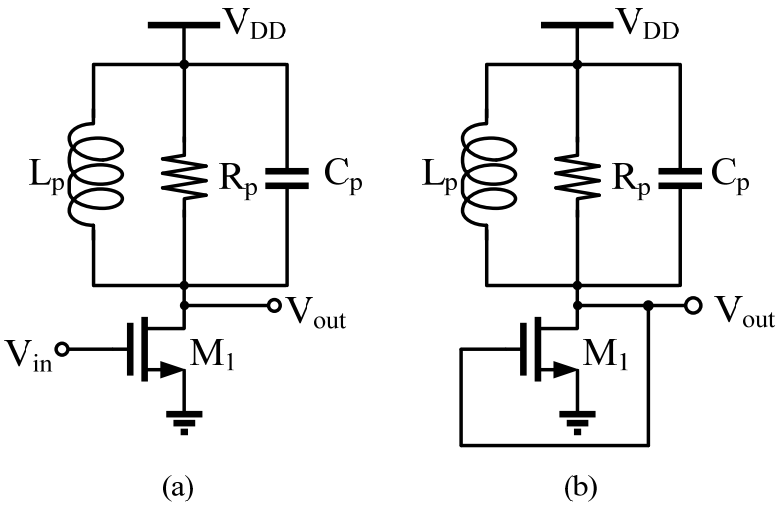

Figure A.4 (a)Tuned gain stage, (b) stage of (a) in feedback

Crossed-Coupled Oscillator

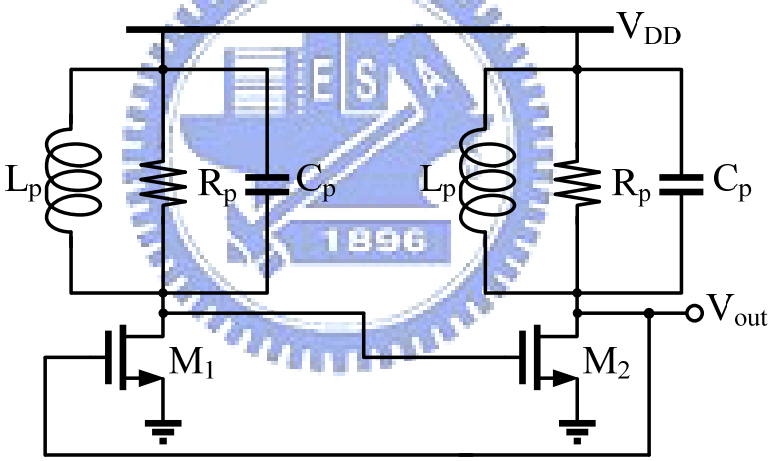

Figure A.5 Two tuned stages in a feedback loop

Suppose we place two stages of Fig. A.4(a) in a cascade, as depicted in Fig. A.5. Furthermore, at resonance, the total phase shift around the loop is zero because each stage contributes zero frequency dependent phase shift. That is, if $g_{m1}R_pg_{m2}R_p \geqq 1$, then the loop oscillates.

The circuit of Fig. A.5 serves as the core of many LC oscillators and is sometimes drawn as in Fig. A.6(a). However, the drain currents of M_1 and M_2 and hence the output swings heavily depended on the supply voltage. Since the waveforms at X and Y are differential, the

drawing in Fig. A.6(a) suggests that M_1 and M_2 can be converted to a differential pair as depicted in Fig. A.6(b), where the total bias current is defined by I_{ss}.

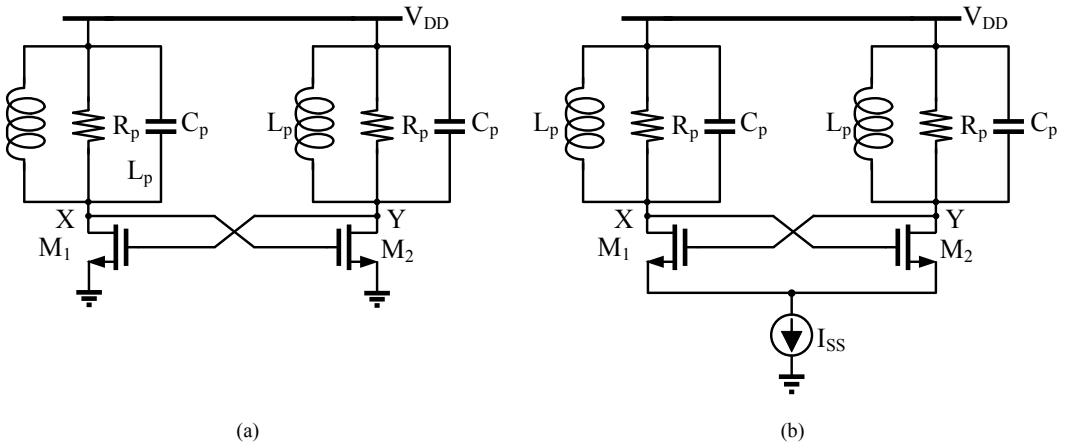

Figure A.6 (a) Redrawing of the oscillator shown in Fig. 8 (b) adding of tail current source to lower supply sensitivity

The oscillator of Fig. A.6(c) is constructed in fully differential form. The supply sensitivity of the circuit is nonzero even with perfect symmetry. This because the drain junction capacitance of M_1 and M_2 vary with the supply voltage.

Assume C_p=0, consider only the drain junction capacitance, C_{DB}, of M_1 and M_2. Since C_{DB} varies with the drain-bulk voltage, if V_{DD} changes, so does the resonance frequency of the tank. Noting that the average voltage across C_{DB} is approximately equal to V_{DD}, we write

$$C_{DB} = \frac{C_{DB0}}{(1+\frac{V_{DD}}{\phi_B})^m} \tag{14}$$

and

$$K_{VCO} = \frac{\partial \omega_{out}}{\partial V_{DD}} = \frac{\partial \omega_{out}}{\partial C_{DB}} \frac{\partial C_{DB}}{\partial V_{DD}} \tag{15}$$

with $\omega_{out} = 1/\sqrt{L_p C_{DB}}$, we have

$$K_{VCO} = \frac{-1}{2\sqrt{L_P C_{DB}} C_{DB}} \cdot \frac{-mC_{DB}}{\phi_B(1+\frac{V_{DD}}{\phi_B})} = \frac{m}{2\phi_B(1+\frac{V_{DD}}{\phi_B})} \cdot \omega_{out} \tag{16}$$

Note that the relationship between ω_{out} and V_{cont} is nonlinear because K_{VCO} varies with V_{DD} and ω_{out}.

Colpitts Oscillator

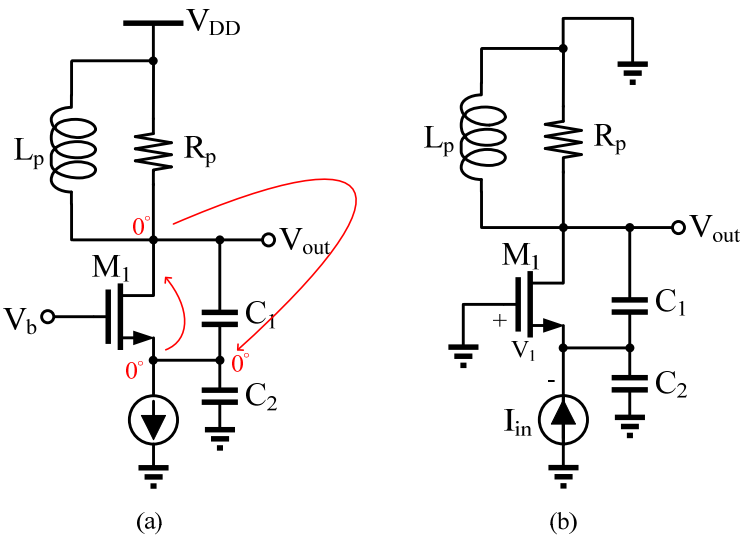

Figure A.7 (a) Colpitts oscillator (b) equivalent circuit of (a) with input stimulus

Approximating M_1 by a single voltage dependent current source, we construct the equivalent circuit of Fig. A.7(b). Since the current through the parallel combination of L_p and R_p is given by $V_{out}/(L_ps)+V_{out}/R_p$, the total current through C_1 is equal to $I_{in}-V_{out}/(L_ps)-V_{out}/R_p$, yielding

$$V_1 = -(I_{in} - \frac{V_{out}}{L_p s} - \frac{V_{out}}{R_p})\frac{1}{C_1 s} \tag{17}$$

Writing the current through C_2 as $(V_{out}+V_1)C_2s$, we sum all of the currents at the output node:

$$-g_m(I_{in} - \frac{V_{out}}{L_p s} - \frac{V_{out}}{R_p})\frac{1}{C_1 s} + [V_{out} - (I_{in} - \frac{V_{out}}{L_p s} - \frac{V_{out}}{R_p})\frac{1}{C_1 s}]C_2 s + \frac{V_{out}}{L_p s} + \frac{V_{out}}{R_p} = 0 \tag{18}$$

It follows that

$$\frac{V_{out}}{I_{in}} = \frac{R_p L_p s(g_m + C_2 s)}{R_p C_1 C_2 L_p s^3 + (C_1 + C_2)L_p s^2 + [g_m L_p + R_p(C_1 + C_2)]s + g_m R_p} \tag{19}$$

The circuit oscillates if the closed-loop transfer function goes to infinity at an imaginary value of s.

$$-R_p C_1 C_2 L_p \omega_R^3 + [g_m L_p + R_p(C_1 + C_2)]\omega_R = 0 \tag{20}$$

$$-(C_1 + C_2)L_p \omega_R^2 + g_m R_p = 0 \tag{21}$$

Since with typical values, $g_m L_p \ll R_p(C_1 + C_2)$, Eq. (20) yields:

$$\omega_R^2 = \frac{1}{L_p \dfrac{C_1 C_2}{C_1 + C_2}} \tag{22}$$

and Eq. (21) results in

$$g_m R_p = \frac{(C_1 + C_2)^2}{C_1 C_2} = \frac{C_1}{C_2}(1 + \frac{C_1}{C_2})^2 \tag{23}$$

We determine the ratio C_1/C_2 for minimum required gain. The reader can prove that the minimum occurs for $C_1/C_2=1$, requiring

$$g_m R_p \geq 4 \tag{24}$$

For cross-coupled LC-tank oscillator the minimum gain requirement (=1), (better than Colpitts oscillator). Consider the parasitic capacitance (C_p) in parallel with the inductor

$$\omega_R^2 = \frac{1}{L_p(C_p + \dfrac{C_1 C_2}{C_1 + C_2})} \tag{25}$$

Mathematical model of VCOs

Consider two waveforms $V_1(t) = V_m \sin[\phi_1(t)]$ and $V_2(t) = V_m \sin[\phi_2(t)]$, where $\phi_1(t)=\omega_1 t$, $\phi_2(t)=\omega_2 t$, and $\omega_1<\omega_2$. As illustrated in Fig. A.8, $\phi_2(t)$ crosses integer multiples of π faster than $\phi_1(t)$ does, yielding faster variations in $V_2(t)$. We say $V_2(t)$ accumulates phase faster.

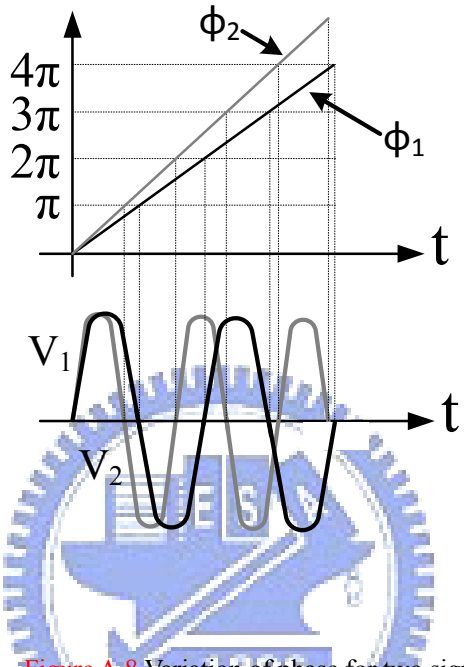

Figure A.8 Variation of phase for two signals

The faster the phase of a waveform varies, the higher the frequency of the waveform, suggesting that the frequency can be defined as the derivative of the phase with respect to time:

$$\omega = \frac{d\phi}{dt} \tag{26}$$

$$\phi = \int \omega t + \phi_0 \tag{27}$$

$\omega_{out} = \omega_0 + K_{VCO} V_{cont}$, we have

$$V_{out}(t) = V_m \cos(\int \omega_{out} dt + \phi_0) = V_m \cos(\omega_0 t + K_{VCO} \int V_{cont} dt + \phi_0) \tag{28}$$

This term, $K_{VCO} \int V_{cont} dt$, is called the "excess phase," ϕ_{ex}.

$$\phi_{ex} = K_{VCO} \int V_{cont} dt \tag{29}$$

$$\frac{\phi_{ex}}{V_{cont}}(s) = \frac{K_{VCO}}{s} \tag{30}$$

A VCO senses a small sinusoidal control voltage $V_{cont}=V_m\cos\omega_m t$.

$$V_{out}(t) = V_0\cos(\omega_0 t + K_{VCO}\int V_{cont}dt) = V_0\cos(\omega_0 t + K_{VCO}\frac{V_m}{\omega_m}\sin\omega_m t) \tag{31}$$

$$= V_0\cos\omega_0 t\cos(K_{VCO}\frac{V_m}{\omega_m}\sin\omega_m t) - V_0\sin\omega_0 t\sin(K_{VCO}\frac{V_m}{\omega_m}\sin\omega_m t)$$

If V_m is small enough that $K_{VCO}V_m/\omega_m \ll 1$ rad, then

$$V_{out}(t) \approx V_0\cos\omega_0 t - V_0(\sin\omega_0 t)(K_{VCO}\frac{V_m}{\omega_m}\sin\omega_m t) \tag{32}$$

$$= V_0\cos\omega_0 t - \boxed{\frac{K_{VCO}V_mV_0}{2\omega_m}}\left[\cos(\omega_0-\omega_m)t - \cos(\omega_0+\omega_m)t\right] \tag{33}$$

The output therefore consists of three sinusoids having frequency of ω_0, ω_0-ω_m, and ω_0+ω_m. The spectrum is shown in Fig. A.9. The components at $\omega_0\pm\omega_m$ are called "sidebands"

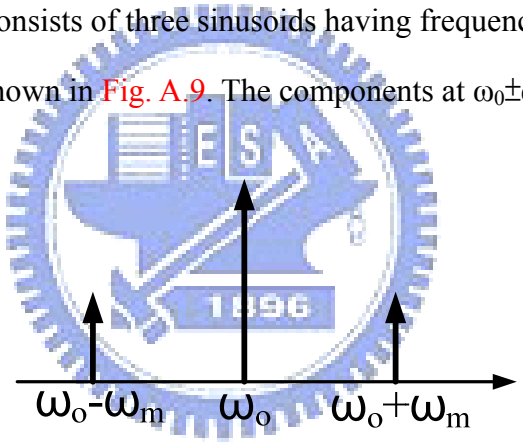

Figure A.9

Variation of the control voltage with time may create unwanted components at the output. In practice, depending on the type and speed of the oscillator, the output may contain significant harmonics.

$$v_{out}(t) = V_1\cos(\omega_0 t + \phi_1) + V_2\cos(2\omega_0 t + \phi_2) \tag{34}$$

If V_{cont} varies by ΔV, then the frequency of the first harmonic varies by $K_{VCO}\Delta V$, the frequency of the second harmonic varies by $2K_{VCO}\Delta V$.

$$v_{out}(t) = V_1\cos(\omega_0 t + K_{VCO}\int V_{cont}dt + \theta_1) + V_2\cos(2\omega_0 t + 2K_{VCO}\int V_{cont}dt + \theta_2) \tag{35}$$

TABLE III Comparison of oscillator topologies

Parameter	Ring oscillator	Colpitts	LC resonator	Cross-couples
Max. oscillation frequency up to which parasitic can be compensated	Low / moderate, parasitic of at least three gates determine speed in CMOS technology	Moderate, high voltage gain of approximately 4 required	high	Very high since minimum voltage gain as low as 1 is required
Output power	Depends on output buffer	Depends on output buffer	Moderate to high. Output buffer is not necessarily required	Depends on output buffer, advantage of differential operation with double voltage swing but disadvantage since additional voltage headroom required for current source
Efficiency	Low, several gates have to be fed, capacitive load of following stage has to be driven, multistage buffer required for impedance matching	Moderate to low since output buffer required	High since no output power or impedance transformer necessarily required	Moderate to low depends on buffer
Noise	High since no high Q frequency stabilisation	Moderate to low	Moderate, noise generated in gate resonator is amplified	Low given weak loading of core by means of high impedance buffer, high voltage swing, differential inductor has higher Q
Immunity against external noise /common mode rejection	High using differential gates, low with single-ended CMOS gates	Low if single-ended	Low since single-ended	Low since differential
Circuit size	Very compact since no inductors required	Moderate, at least one inductor required	Moderate, at least one inductor required	Moderate, at least one differential inductor required
Suitability for integrated systems	High, suited to generate multiphase outputs	Up to low / moderate frequencies, high in III/V tech.	Up to moderate frequencies, high in III/V technologies	Very high

Effect of Phase Noise in RF Communications

To understand the important of phase noise in RF systems, consider a generic transceiver as depicted in Fig. A.10, where a local oscillator provides the carrier signal for both the receive and transmit paths. If the LO output phase noise, both downconverted and upconcerted signals are corrupted. This is illustrated in Fig. A.11.

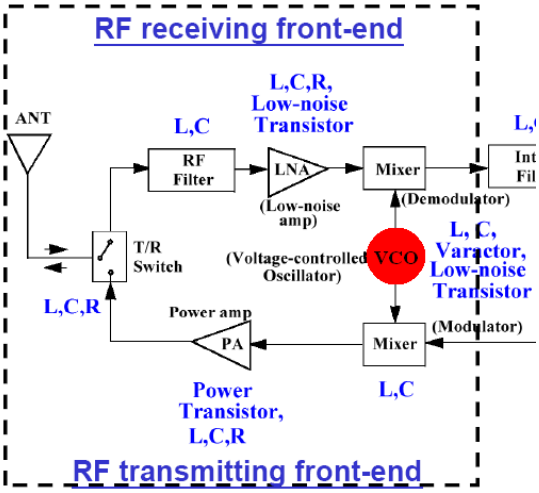

Figure A.10 Generic wireless transceiver

If the LO output contains phase noise, both the downconverted and upconverted signals are corrupt. This is illustrated in Fig. A.11(a) and (b) for the receive and transmit paths, respectively.

Referring to Fig. A.11(a), we note that in the ideal case, the signal band of interest is convolved with an impulse and thus translated to a lower frequency with no change in its shape. In reality, however, the wanted signal may be accompanied by a large interferer in an adjacent channel, and the local oscillator exhibits finite phase noise. When the two signals are mixed with the LO output, the downconverted band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to tail of the interferer. The effect is called “reciprocal mixing”.

Show in Fig. A.11(b), the effect of the phase noise on the transmit path is slightly different. Suppose a noiseless receiver is to detect a weak signal at ω_2 while a powerful, nearby transmitter generates a signal at ω_1 with substantial phase noise. Then, the wanted signal is corrupted by the phase noise tail of the transmitter.

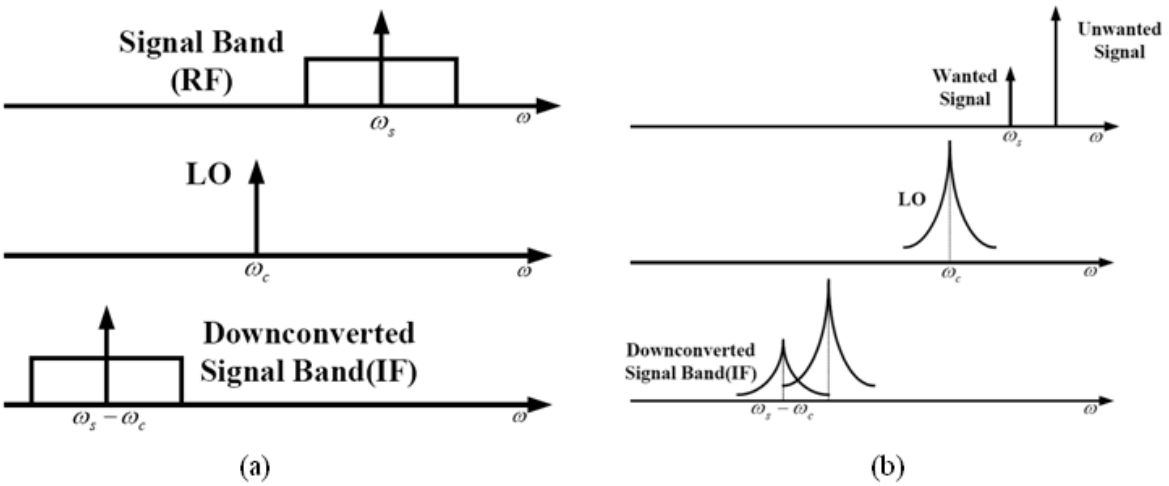

Figure A.11 (a) Downconversion by an ideal oscillator, (b) reciprocal mixing

General considerations

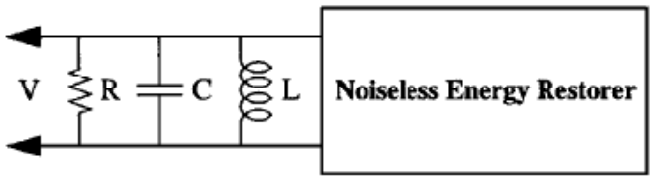

Figure A.12 Perfectly efficient RLC oscillator

To highlight some import issues in a very approximate and general way, consider a single RLC bandpass resonator use in an oscillator. The resonator is connected to an active element that has the unrealizable property that is contributes no noise of its own; see Fig. A.12. The noiseless magic box supplies just enough energy to the tank to compensate for the dissipation by tank's resistance, thereby leading to a constant amplitude oscillator. Although the magic box is noiseless, the tank resistance is not.

The signal energy stored in the tank is simply

$$E_{stored} = \frac{CV_{pk}^2}{2} \tag{36}$$

so that the mean-square signal voltage is

$$\overline{V_{sig}^2} = \frac{E_{stored}}{C} \tag{37}$$

where we have assumed a sinusoid waveform.

By postulate, the only source of noise is the tank resistance. The total mean-square noise voltage is found in the usual way, by integrating the resistor's thermal noise over the noise bandwidth of the RLC filter:

$$\overline{V_n^2} = 4kTR\int_0^\infty \left|\frac{Z(f)}{R}\right|^2 df = \frac{4kTR}{4RC} = \frac{kT}{C} \tag{38}$$

Taking the ratio of mean-square voltages, we find that the noise to signal ratio is equal to the ratio of thermal energy to the stored signal energy:

$$\frac{N}{S} = \frac{\overline{V_n^2}}{\overline{V_{sig}^2}} = \frac{kT}{E_{stored}} \tag{39}$$

Thus, we want to maximize the energy of the desired signal relative to the thermal energy. All other factors held constant, one therefore needs to use the maximum possible signal levels if the noise to carrier ratio is to be minimized.

To bring power consumption and resonator Q explicitly into the discussion, recall from the chapter on passive RLC networks that Q is most generally defined as proportional to the energy stored, divided by the energy dissipated:

$$Q = \frac{\omega E_{stored}}{P_{diss}} \tag{40}$$

Hence, we may write

$$\frac{N}{S} = \frac{\omega kT}{QP_{diss}} \tag{41}$$

The power consumed by this model oscillator is simply equal to P_{diss}, the amount dissipated by the tank loss. The noise to carrier ratio is here inversely proportional to the product of resonator Q and the power consumed, and directly proportional to the oscillation frequency. This set of relationships still holds approximately for real oscillators, and explains

the near obsession of engineers with maximizing resonator, for example.

Minimization of phase noise

A. Maximization of LO Power

Proper choice of the bias and the landline is important to maximize the LO power. Corresponding design issues are very similar to those of power amplifiers. To increase the single swing, complementary P and NMOS structures are efficient in topologies capable of adding the individual voltage swings of the devices.

B. Optimum Gain

To ensure start-up, the negative resistance and consequently the gain provided by the active device must be high to compensate the losses in the system within a wide frequency band, temperature range and process variations. In steady-state, the LO signal is subject to power compression, whereas the phase noise is not compressed. That means that at a certain gain level the noise is amplified but not the LO signal leading to a degradation of L. thus, depending on the system requirements a reasonable tradeoff has to be found for the gain.

C. Maximization of Resonator Q

The Q of the resonator has a significant impact on the noise and must be kept as high as possible. At low to moderate frequencies, the Q fact of the resonator is clearly determined by the inductor in the resonator requiring lots of turns and large area. Thus, the inductor exhibits significant resistive losses associated with the large series resistance of the lines and the coupling to the lossy substrate. Towards very high frequencies, the varactor becomes more and more the limiting element since the varactor Q is more or less inversely proportional to frequency.

D. Choice of transistor

The noise floor is impacted by the noise properties of the device. A low average noise figure along the whole signal swing is important but more or less determined by the

technology used. What about the transistor type? On one hand, FET devices are less nonlinear than bipolar transistors. On the other hand, the $\omega_{1/fn}$ of bipolar devices is much lower than for FETs. Values for $\omega_{1/fn}$ range from 1 to 10 KHz for bipolar transistors and 0.1 to 1 MHz for FETs. Thus, typically, bipolar devices provide lower 1/f noise, which can dominate the total VCO noise performance.