國立交通大學

電信工程學系

碩 士 論 文

應用於超寬頻系統之電流再利用低雜訊放大器、

9-26GHz 寬頻互補式電晶體低雜訊放大器

之設計與研究

Design of Current-Reused LNA for UWB,

9-26GHZ Wideband CMOS LNA

研 究 生：林宗廷

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中 華 民 國 九十八 年 六 月

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碩 士 論 文

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摘　　要

本論文的第一部份提出一超寬頻低雜訊放大器。此電路輸入阻抗之匹配是利用電流再利用應用於 LC Ladder 使得此架構適合低電壓使用，然而在利用電流再利用之技術來放大射頻訊號。因此超寬頻低雜訊放大器能夠同時達到輸入端寬頻匹配與高增益。模擬結果:-10dB 之輸入與輸出端反射損耗、3.3dB 之最小雜訊指數、14.3dB 之最高增益並消耗 17.75mW 之功率。

第二部份針對不同於 3.1-10.6GHz 的低雜訊放大器設計提出一利用 0.18 製程所達到 9-26GHz 之低雜訊放大器。此電路設計是期望能利用 L 和 R-C 匹配方式，來達到寬頻及相對低的雜訊指數。模擬結果: -10dB 之輸入與輸出端反射損耗、低雜訊、高增益於不同偏壓情況下。

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ABSTRACT

In the first part of this thesis, an ultra-wideband (UWB) LNA is proposed. The input matching of this circuit used a LC Ladder with current-reused so that this topology is suitable for low voltage. Using current-reused to amplify RF signal. Therefore, the proposed LNA can simultaneously achieve input impedance matching and high gain. The simulated results:-10dB input and output return loss, minimum noise figure of 3.3dB, and maximum gain of 14.3dB from 17.75mW.

In the second part, a 9-26GHz LNA using 0.18um technology different from 3.1-10.6 GHz (In general, the 0.18um CMOS LNA usually be designed for 3−10GHz operating range.) is proposed. The design of this circuit used L and R-C matching to achieve wideband and low noise figure. The simulated results:-10dB input and output return loss, low noise figure, and high gain at different bias voltage.

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能夠完成碩士這兩年的學業，首先我要先感謝我的指導老師周復芳博士，再這兩年的期間總是能適時的給我關心以及指導，不僅讓我在射頻積體電路設計的領域上有很好的基礎也讓我的心態與態度都有所成長。也感謝電子工程學系胡樹一教授給我一個機會能開始接觸如何設計低雜訊放大器以及論文口試委員郭建男授的不吝指導。

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Nino @ 2009 年 新竹 夏

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Chapter 1

Introduction

1.1 Background and motivation

The Federal Communications Commission (FCC) authorize the unlicensed use of ultra-wideband(UWB) in 3.1-10.6 GHz in February 14 2002[1]. UWB is a technology that can be used at very low energy levels for transmitting information spread over a large bandwidth (＞500 MHz). Beside, UWB communications transmit in a way that doesn't interfere largely with other more traditional narrow band and continuous carrier wave uses in the same frequency band. Direct sequence code division multiple access (DS-CDMA) and multi-band orthogonal frequency division multiple access (MB-OFDM) are two mainly modulation technologies for UWB communications. The DS-CDMA UWB supports two independent operated bands. The lower band occupies the spectrum from 3.1-5.15 GHz and the upper band occupies the spectrum from 5.825-9.7 GHz as shown in Fig.1.1

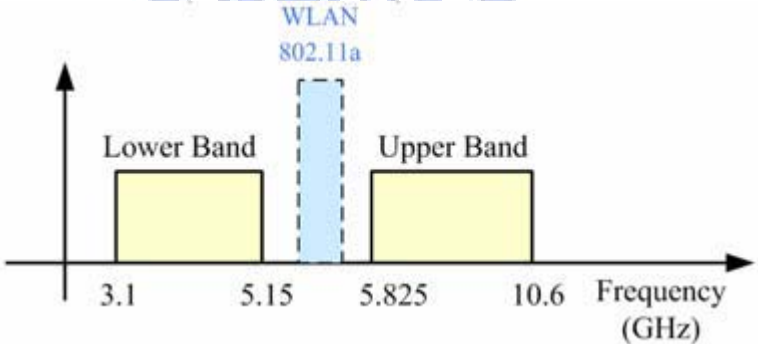


Fig.1.1 DS-UWB spectrum allocation

The MB-OFDM UWB, the 7500-MHz bandwidth is divided into 5 major Band Groups which are in turn sub-divided into 14 bands in total and each band is 528MHz bandwidth and each band includes 128 sub-channels, sub-channel is 4.125 MHz as shown in Fig.1.2.

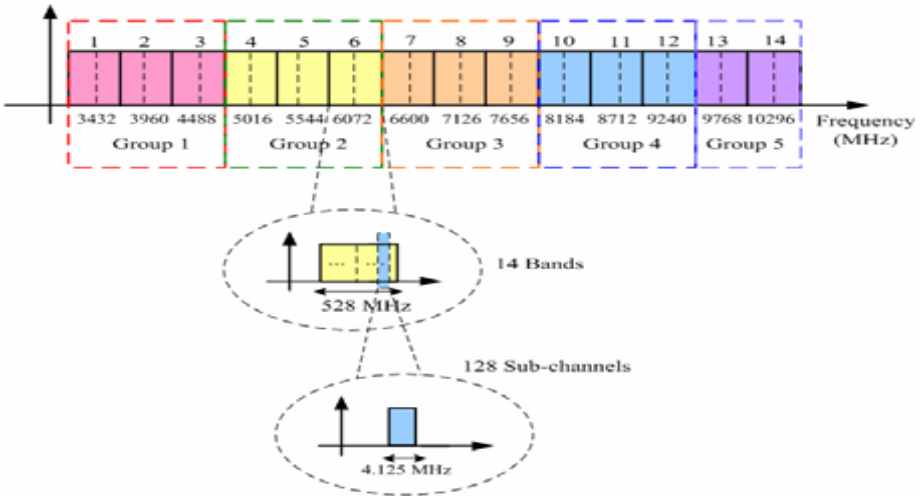


Fig.1.2 MB-OFDM UWB spectrum allocation

The low-noise amplifier (LNA) is a key component in the front-end of a radio receiver circuit. It is located after the antenna, so that losses in the feedline become less critical. The overall noise figure of the receiver front-end is dominated by the first few stages. Using an LNA, the noise of all the subsequent stages is reduced by the gain of the LNA, while the noise of the LNA itself is injected directly into the received signal. Thus, it is necessary for an LNA to be low noise and high gain.

1.2 Thesis organization

This thesis will discuss about the two kinds of circuit and implementation for ultra-wideband applications. The contents consist of two major topics:" Design of current-reused LNA for UWB " and " 9−26GHz Wideband CMOS LNA Design " , respectively in chapter 2 and chapter 3. In these chapters, we will propose the architecture and explain the circuit. The circuit principles, design consideration and Layout consideration will be analyzed. In chapter 2, we discuss several researches recently. By improving their drawback, we proposed current-reused amplifier which stacking NMOS and PMOS. The input impedance can be achieved 50Ω over the frequency band of interest and the gain will not reduce due to the enhancement of transconductance. The details will be explained in chapter2.

In chapter 3. Base on the technology of the narrowband LNA, we use the LC matching and five-stage common source cascade architecture to achieve a wideband 9 – 26 GHz and low noise circuit. The details will be explained in chapter 3.

Chapter 2

Design of Current-Reused LNA for UWB

2.1 Introduction

The ultra-wideband (UWB) system is a high data rate , low power consumption and for a short range wireless personal area network technology [2][3]. Because it can handle the requirement of high transmission speed for the multimedia material (for example phantom and sound) , it becomes more and more popular for wireless system. The FCC has defined 7500 MHz bandwidth in 3.1 - 10.6 GHz frequency range (lower band : 3.1 – 5 GHz ; upper band : 6 – 10.6 GHz) for the UWB standard IEEE 802.15.3a.

One of the challenges is to design the front-end LNA. Because it is the first block in the radio receiver, its performance will affect the sensitivity of the overall system. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible so that the retrieval of this signal is possible in the later stages in the system.

2.2 Numerous topology of wideband LNA

Because of the input matching can directly affect the noise performance of an LNA. Thus, there are some researches that can provide 50Ω input impedance over a wide bandwidth will be discussed as follow.

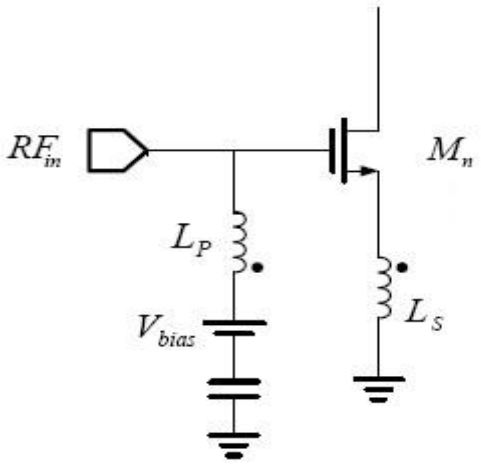


Fig.2.1 (a) The transformer feedback amplifier

(a) The transformer feedback amplifier[4][5]

The transformer feedback topology has good input matching entire frequency band of interest. There is no input matching devices in the input gate of the purpose circuit, so that the LNA can achieve lower NF. However, the transformer silicon set up is very sensitive to the technology dispersions thus strengthening the design hardness.

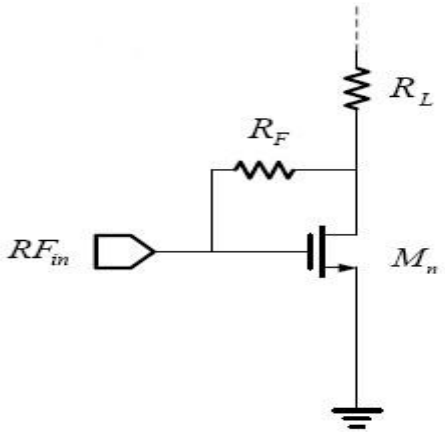


Fig.2.1 (b) Resistive shunt-feedback amplifier

(b) Resistive shunt-feedback amplifier[6]

The resistive shunt-feedback topology could have better bandwidth than conventional low noise amplifier, but it has limited input matching or NF and vice versa. In other words, the resistive shunt-feedback amplifier exhibits trades off in terms of bandwidth, input matching and NF. Indeed, its lower voltage gain will cause the noise of next stage won't be suppressed.

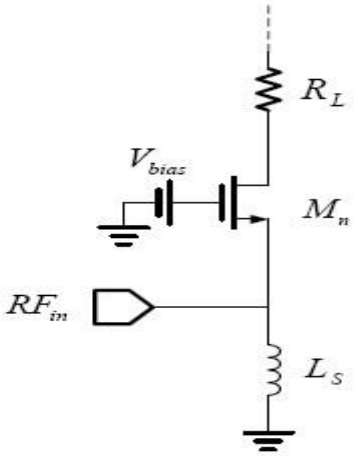


Fig.2.1 (c) The common-gate amplifier

(c) Common-Gate amplifier[7]

The input impedance is approximately as $Z_{in} = \frac{1}{g_m + jwC_{gs}}$. In the low frequency, the input impedance is approximately as $Z_{in} \approx \frac{1}{g_m}$. It is easy to be matched to the 50Ω. However, with the increasing of the operating frequency, the parasitic transistor capacitance (C_{gs}) degrades the amplifier performance in the high frequency. In addition, its noise is also larger than that of the other topologies.

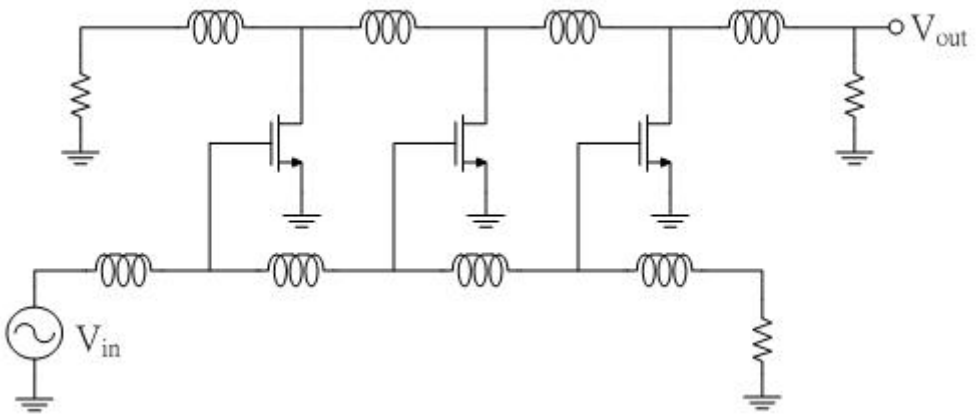


Fig.2.1 (d) The distributed amplifier

(d) Distributed amplifier[8]

The distributed amplifier that can provide wide bandwidth and relatively flat gain over entire frequency band of interest. However, due to multiple transistor stages and much inductors are used so that the drawback is large power consumption and occupies large die size, respectively. In one word, it will make them unsuitable for integration.

Here, we proposed a LC ladder with current-reused topology for input matching as shown in Fig.2.2. To combine a NMOS and a PMOS transistor using the same supply voltage allows LC ladder technology to be low voltage compatible[9].

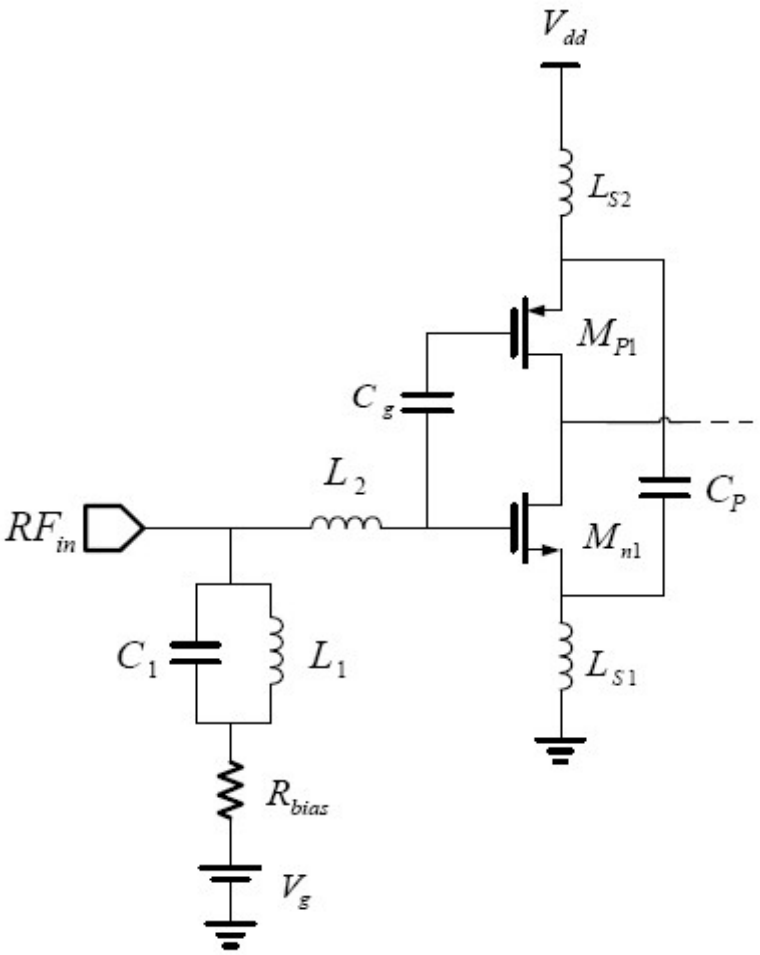


Fig.2.2 The LC ladder with current-reused topology

2.3 Conventional current-reused amplifier

Fig.2.3 shows the topology of current-reused amplifier. The current reused configuration can be considered as two-stage casade amplifier [10] [11], where the first stage M_1 and the second stage M_2 are two common-source amplifiers. The function of L_1 and C_1 is to perform a series-resonant with C_{gs} of M_3 for a low impedance path, and the impedance of L_2 is quite large to provide a high impedance path to block RF signal. Consequently, the RF signal can be amplified twice by this co-current structure. Because the resonate circuit

composed of L_1 and C_1 presents a narrowband characteristic, the current reused topology is designed to boost the gain at upper end of the required band. R_1 and L_3 is used to compensate the high gain roll-off of the circuit. Due to the increased impedance of the L_1 and C_1 path, the function of current reused amplification is degraded at lower end of the designed band. However, by using LC ladder at input with current reused topology, an overall wideband flat-gain performance can be achieve.

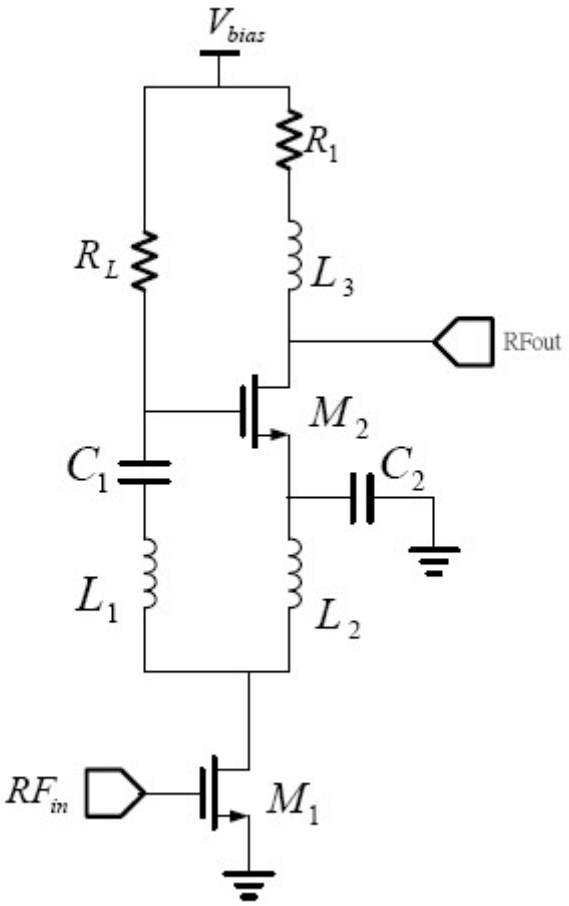


Fig.2.3 The current-reused amplifier topology

2.4 Architecture

The proposed UWB LNA as shown in Fig.2.4 employs three stages. This circuit is designed to require three bias voltage sources of 1.0V (V_{dd}), 0.7V (V_g) and 1.2V (V_{bias}). The first input stage including LC ladder and M1p, M1n is current-reused configuration. It can provide wideband matching. The second stage M2 and the third stage M3 are current-reused configuration, too. A large resistor R_L (5KΩ) is employed in bias circuit to isolate noise of voltage source from internal circuit. The function of C_g in input stage is to make the gate wideband flat-gain performance can be achieve.

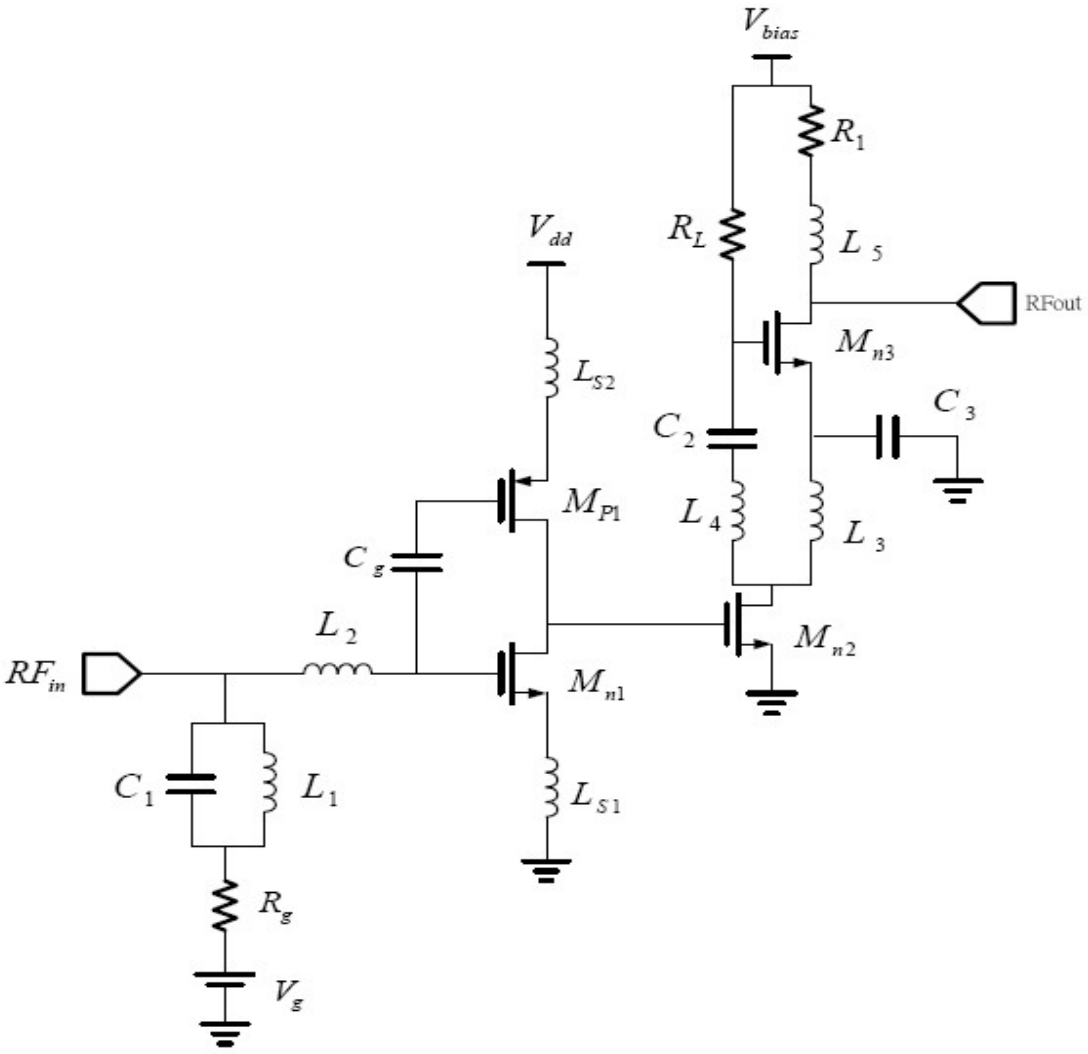


Fig.2.4 Schematic of the proposed UWB LNA

2.5 Design Considerations

2.5.1 Input matching analysis

The proposed LNA use a fourth-order bandpass ladder filter to match 50Ω. The fourth-order bandpass ladder filter is shown in Fig.2.5[12].

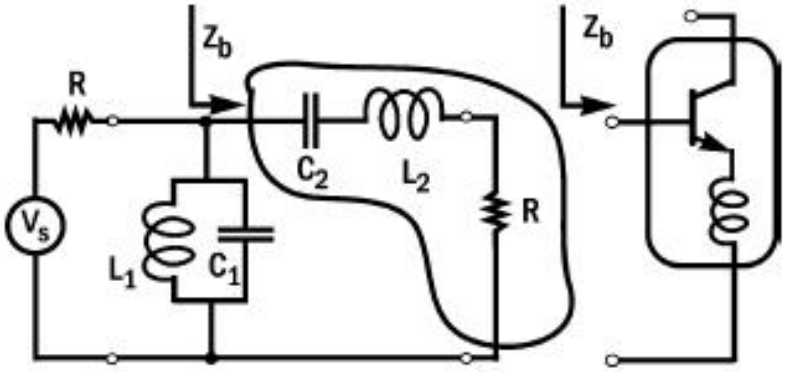


Fig.2.5 Fourth-order bandpass filter used for impedance matching

From the results of recent research, we can find that the input impedance of the fourth-order bandpass ladder filter across the overall passband from W_L to W_U is equal to a constant resistance R as shown in Fig.2.6.

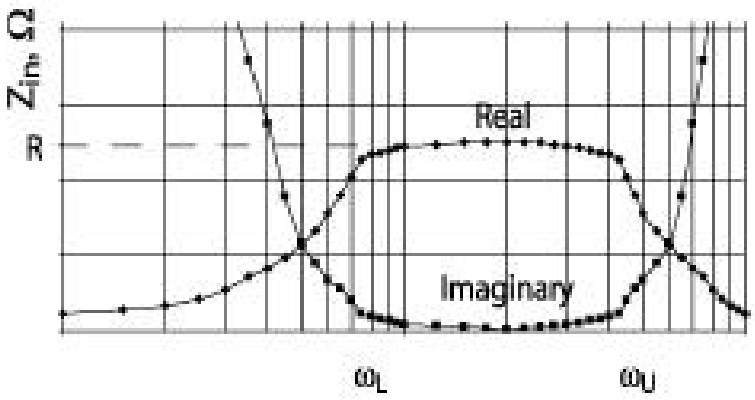


Fig.2.6 Input impedance of the bandpass filter versus frequency

By means of a first approximation of the upper frequency (W_U) and the lower frequency (W_L) of this LC ladder filter is given by: $W_U \approx \frac{1}{RC_1}$ and $W_L \approx \frac{1}{RC_2} \approx \frac{R}{L_1}$. Obviously, the LC ladder filter can provide a real impedance over a frequency band of interest. Because of the Fig.2.5 shows, the equivalent circuit of the inductively degenerated transistor in Fig.2.5 looks like the right part of the bandpass filter. Therefore the overall input matching small signal equivalent circuit is shown in Fig.2.7.

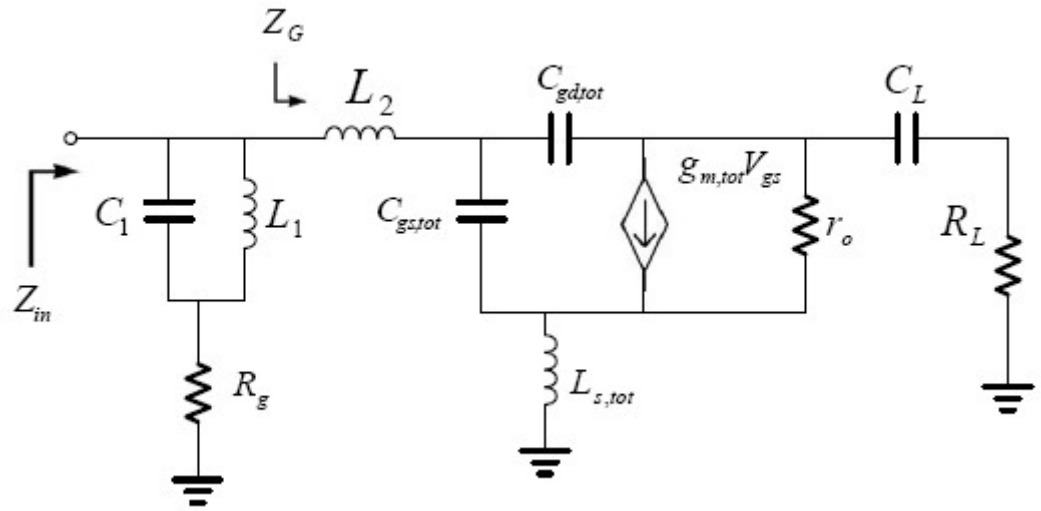


Fig.2.7. The overall input matching small signal equivalent circuit

According to the novel wideband feedback mechanism proposed by [13]. C_L and R_L are the parasitic capacitance and resistance which is contributed from the next stage. The capacitor C_L dominates at low frequency and the resistor R_L dominates at high frequency. The LNA input equivalent circuit at high frequency is shown in Fig.2.8.

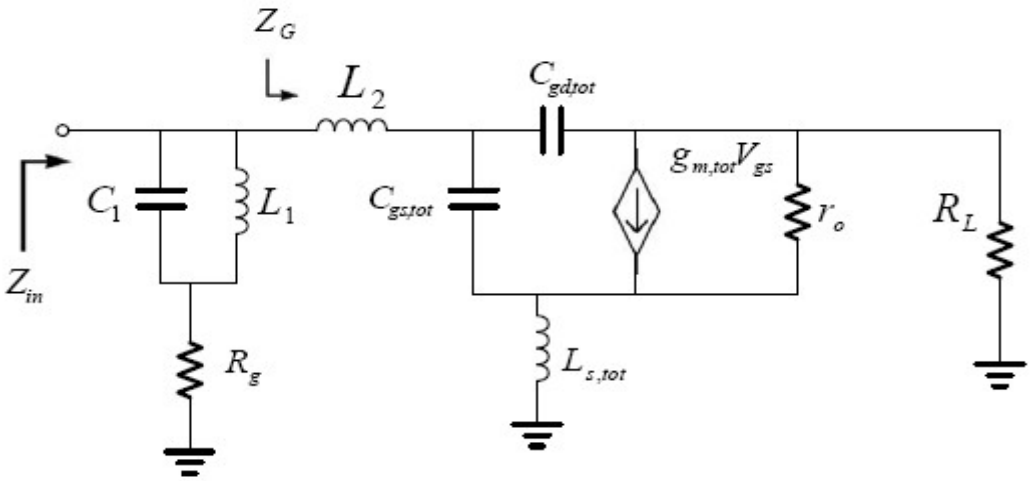


Fig.2.8 Input small signal equivalent circuit at high frequency

While we assume that $WL_{S,tot} << \frac{1}{WC_{gs,tot}}$, $WL_{S,tot} << R_L$ and we can find the input impedance can be expression as following equation :

$$Z_{in} \approx (jwL_1 // \frac{1}{jwC_1}) + R_g // Z_G \tag{2-1}$$

where $Z_G = jwL_2 + (\frac{1}{jwC_{gs,tot}} + \frac{L_{S,tot}\gamma g_{m,tot}}{C_{gs,tot}}) \cdot [1 + \frac{C_{gd,tot}}{C_{gs,tot}}(1 + \gamma g_{m,tot} R_L)^{-1}]$ (2-2)

$$\gamma = \frac{r_O}{r_O + R_L + jwL_{S,tot}}.$$

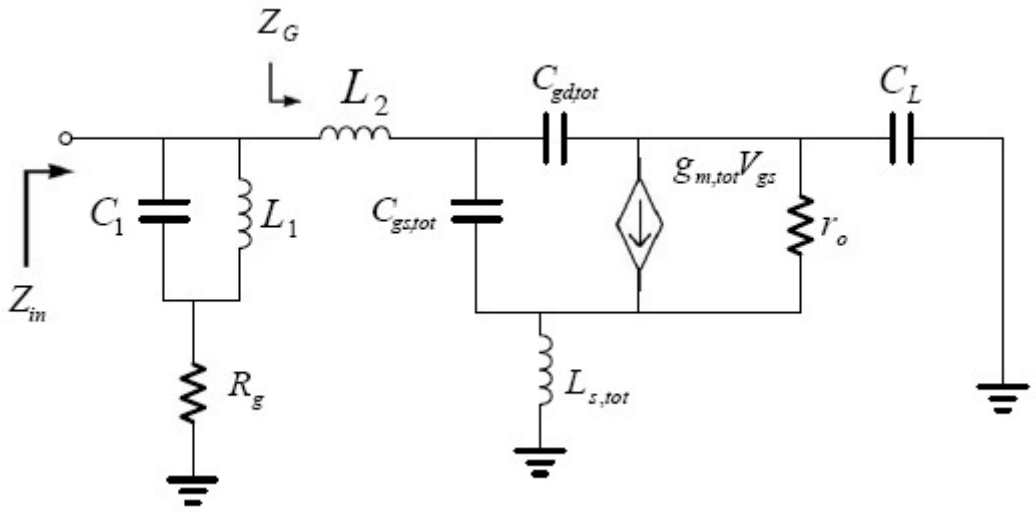


Fig.2.9 Input small signal equivalent circuit at low frequency

The LNA input equivalent circuit at low frequency is shown in Fig.2.9. In order to analysis the input impedance, we apart this circuit into two branches. Therefore, we can find the input impedance is $Z_{in} \approx (jwL_1 + \frac{1}{jwC_1}) \ // Z_G$. (2-3)

$$\text{where } Z_G = jwL_2 + \left(Y_\alpha + \frac{1}{Z_\beta} \right)^{-1}. \quad (2\text{-}4)$$

Y_α is the impedance looking into the $C_{gd,tot}$ and Z_β is the impedance looking into the $C_{gs,tot}$. While we assume that the current flow through the capacitor $C_{gd,tot}$ and $C_{gs,tot}$ is smaller than the current source $g_{m,tot} v_{gs}$. Thus

$$Y_\alpha = jwC_{gd,tot} + (R_\alpha + \frac{1}{jwC_\alpha} + jwL_\alpha)^{-1} \quad (2\text{-}5)$$

$$\text{and } Z_\beta = \frac{1}{jwC_{gs,tot}} + (\frac{1}{R_\beta} + jwC_\beta + \frac{1}{jwL_\beta})^{-1}. \quad (2\text{-}6)$$

$$\text{with } R_\alpha = \frac{C_L}{g_{m,tot} C_{gd,tot}} \quad C_\alpha = g_{m,tot} r_o C_{gd,tot} \quad L_\alpha = \frac{L_{S,tot} C_L}{g_{m,tot} r_o C_{gd,tot}} (1 + g_{m,tot} r_o) \quad (2\text{-}7)$$

$$R_\beta = \frac{g_{m,tot} L_{S,tot}}{C_{gs,tot}} \quad C_\beta = \frac{C_{gs,tot}}{g_{m,tot} r_o} \quad L_\beta = \frac{L_{S,tot} g_{m,tot} r_o C_L}{C_{gs,tot}} \quad (2\text{-}8)$$

Therefore, when the values of the inductors are designed properly, the input impedance will approach the $50\,\Omega$.

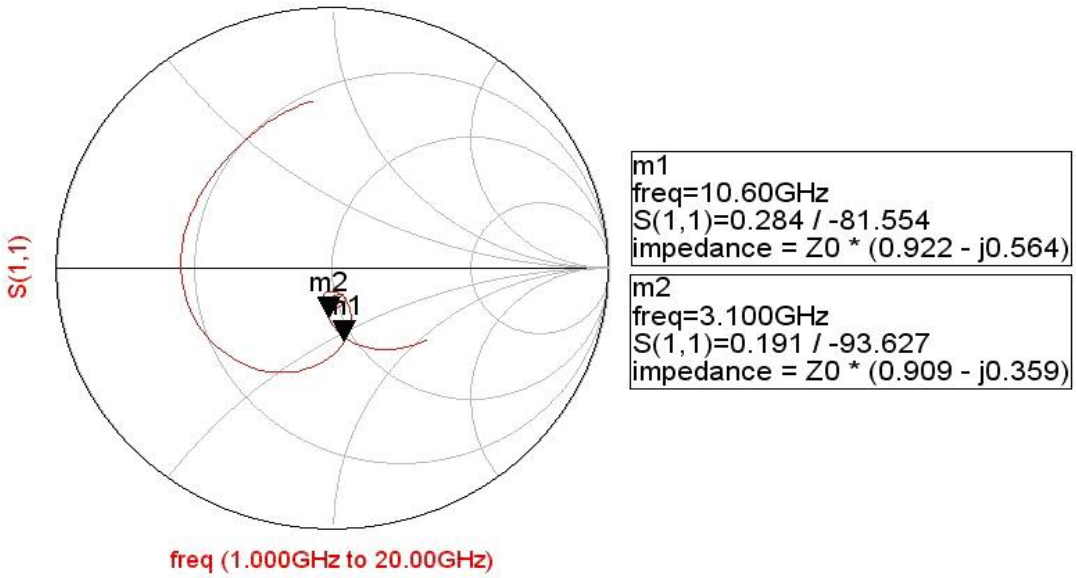


Fig.2.10 Simulated input reflection coefficients

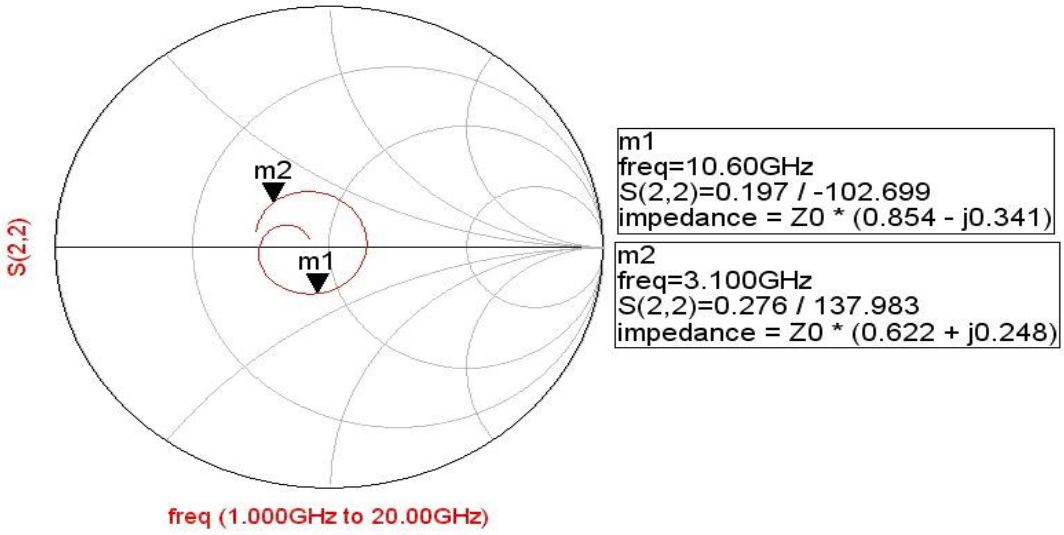


Fig.2.11 Simulated input reflection coefficients

Fig.2.10 and Fig2.11 shows the simulated input reflection coefficients (S11) and the simulated output reflection coefficients (S22), respectively. As can be seen, the curve is near by the center of the Smith chart when frequency increases from 3.1GHz to 10.6GHz. In other words, this design can achieve wideband input matching successfully.

2.5.2 Gain analysis

Because of the current-reused configuration, the stacking NMOS and PMOS increase transconductance from g_m to approximately $2g_m$.In addition, by using L_4 and C_2 is to perform a series-resonant with C_{gs} of M_4 for a low impedance path, and the impedance of L_3 is quite large to provide a high impedance path to block RF signal. Consequently, the RF signal can be amplified twice by two current-reused configuration, respectively.

2.6 Chip implementation and simulated result

2.6.1 Layout considerations

The chip layout of the proposed LNA is shown in Fig.2.12, The skill of layout is very important for radio frequency circuit design, because high frequency will make more coupling and parasitic effects occur to influence performances. To get the high speed that the 0.18 μm gate length was chosen. All elements with guard-rings can prevent noise and interference from substrate. Because the RF pad has parasitic capacitance that will degraded the RF signal, the RF pad with its size is 50×50 μm^2 will be used. The smaller pad size can lead to a smaller parasitic capacitance. The bypass capacitors are used between each voltage source node and ground node to ensure voltage working like ground in AC and filter out noise. All connection wires are simulated by ADS momentum to extract parasitical effect.

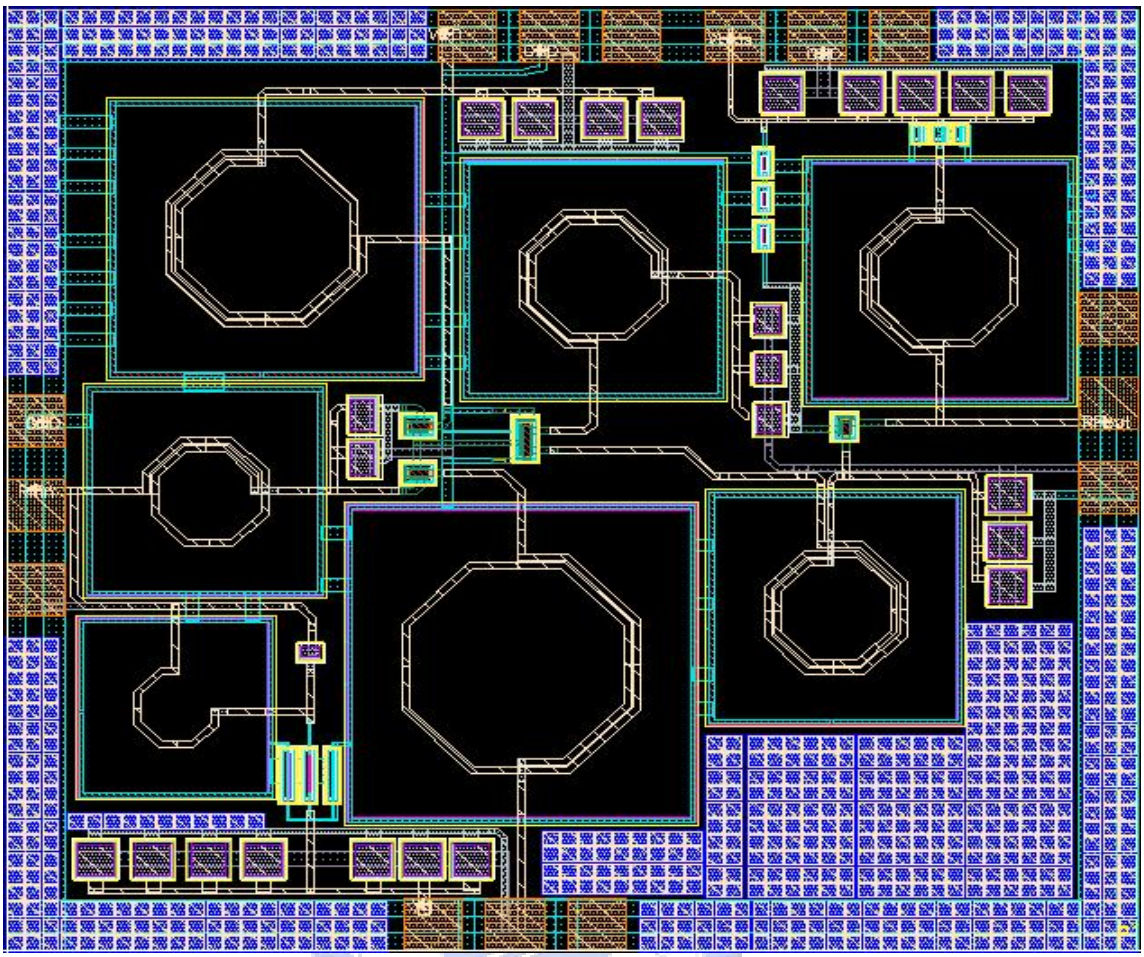


Fig.2.12 Chip layout of the UWB LNA.

2.6.2 Simulated result

The chip size of the proposed LNA is $0.969 \times 0.895\, mm^2$ and it is fabricated using TSMC $0.18\,\mu m$ mixed-signal/RF CMOS 1P6M technology. The total consumption is 17.758mW with bias voltage source of 1.0V and 1.2V. The simulated result of the input return loss (S11) and the output return loss (S22) in Fig2.13 and Fig2.14 is lower than -10 dB, respectively. The gain (S21) in Fig2.15 is 13dB~14.3dB over 3.1 ~10.6 GHz. The noise figure (NF) performance is shown in Fig.2.17. The simulated NF has maximum 4.65dB and minimum 3.34dB. The simulated input-referred third-order intercept point (IIP3) at three frequency points are shown in Fig.2.18 (a) ~ (c). The simulated IIP3 shows -9dB at 3.1GHz, -7dB at 6.8GHz, -6.2dB at 10.6GHz. The simulated input-referred 1dB compression point (P1dB) are

shown in Fig.2.19 (a) ~ (c). The simulated P1dB shows -23.4dB at 3.1GHz, -21.2dB at 6.8GHz, -20.3dB at 10.6GHz. The performance summary is listed in table 2.1. The performances of the proposed UWB LNA are compared with other works for UWB band listed in Table2.2.

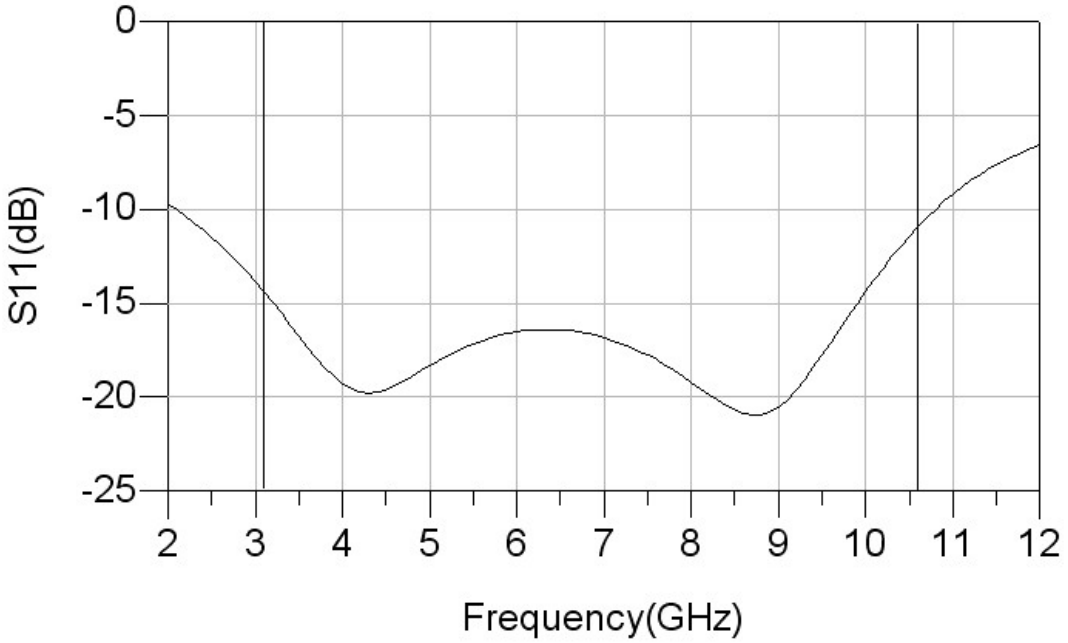


Fig.2.13 Simulated result of S11

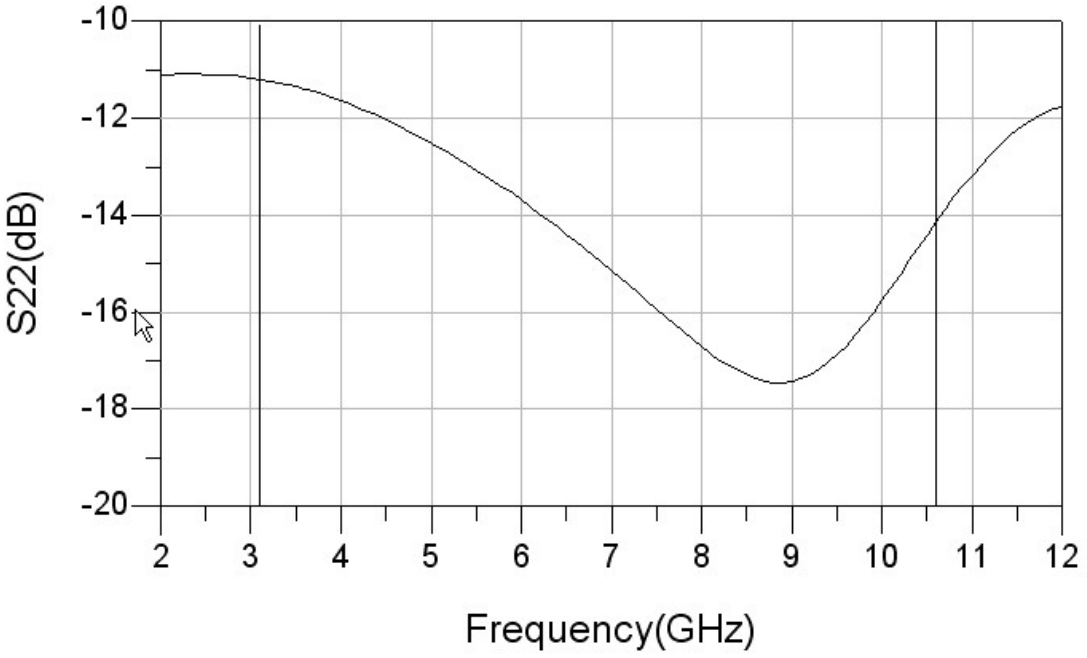


Fig.2.14 Simulated result of S22

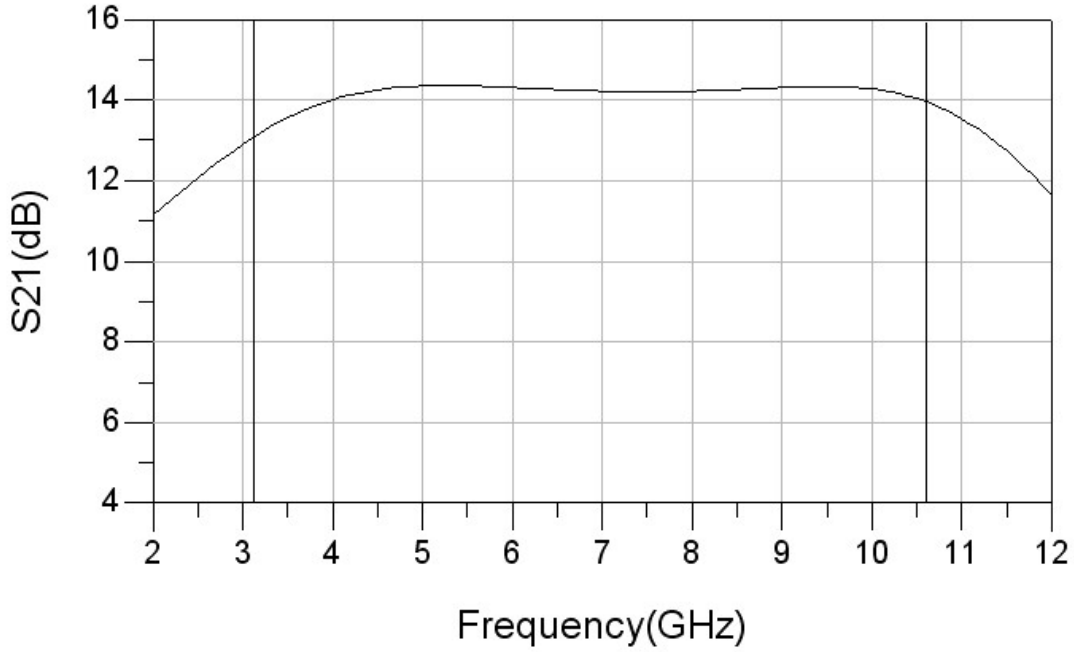


Fig.2.15 Simulated result of S21

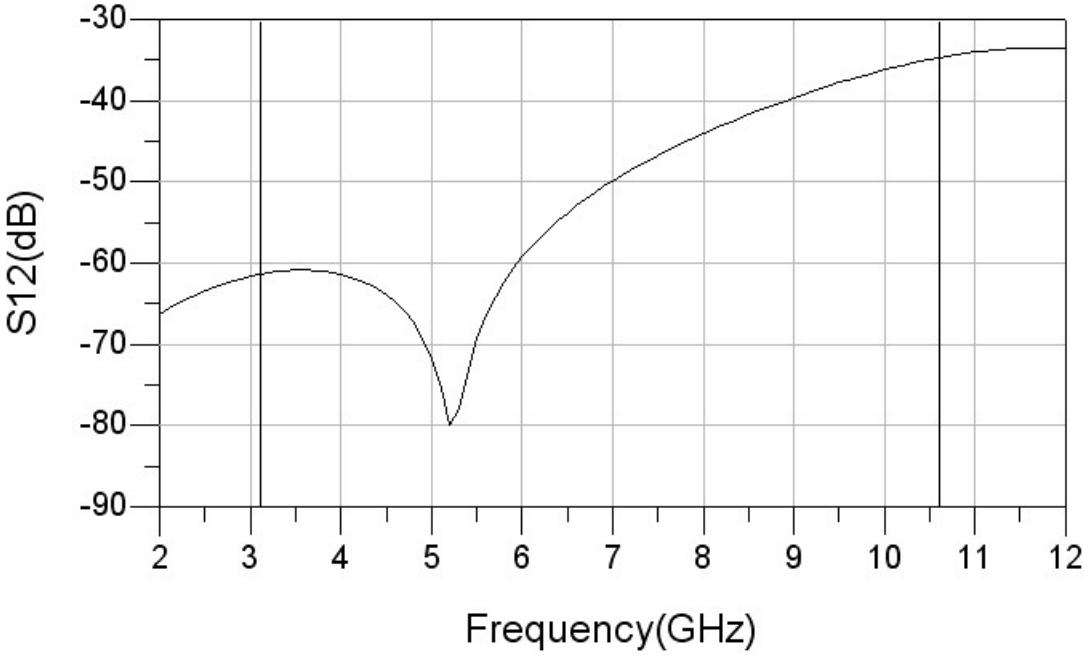


Fig.2.16 Simulated result of S12

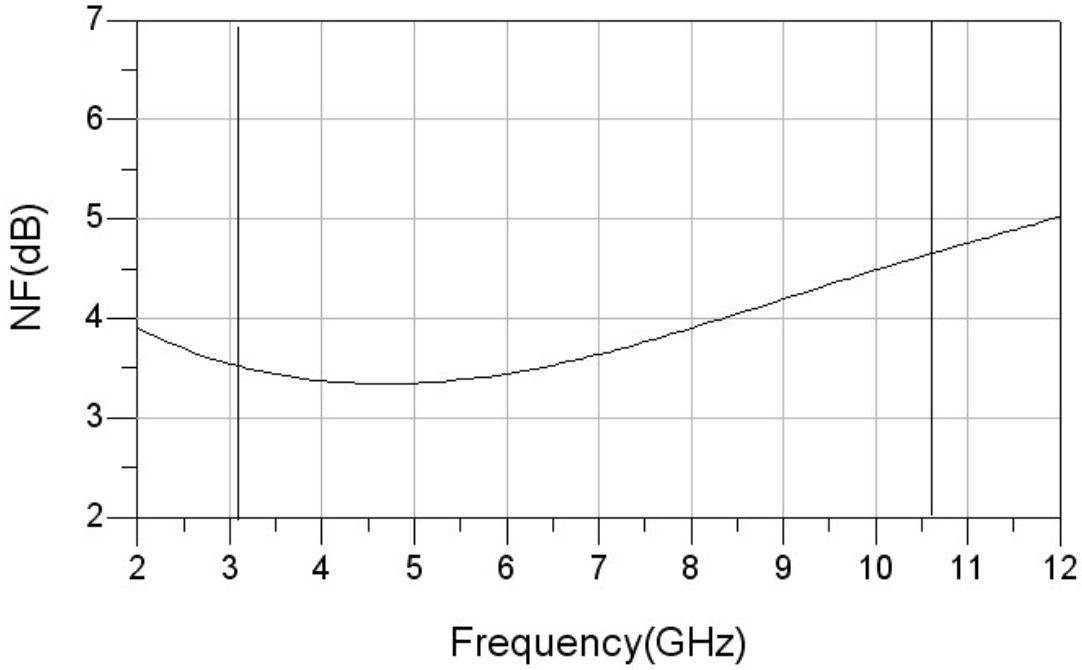
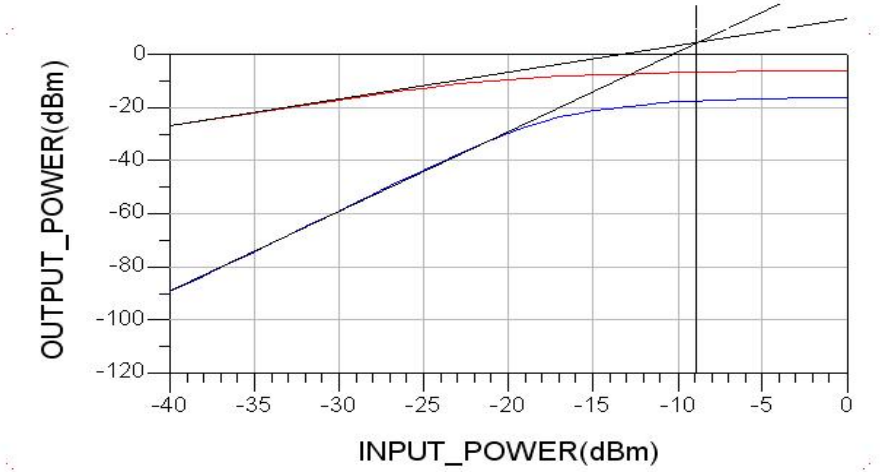
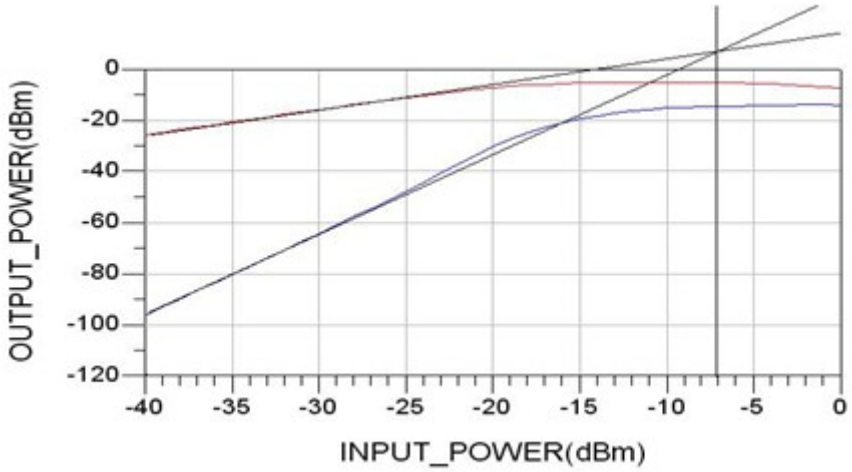


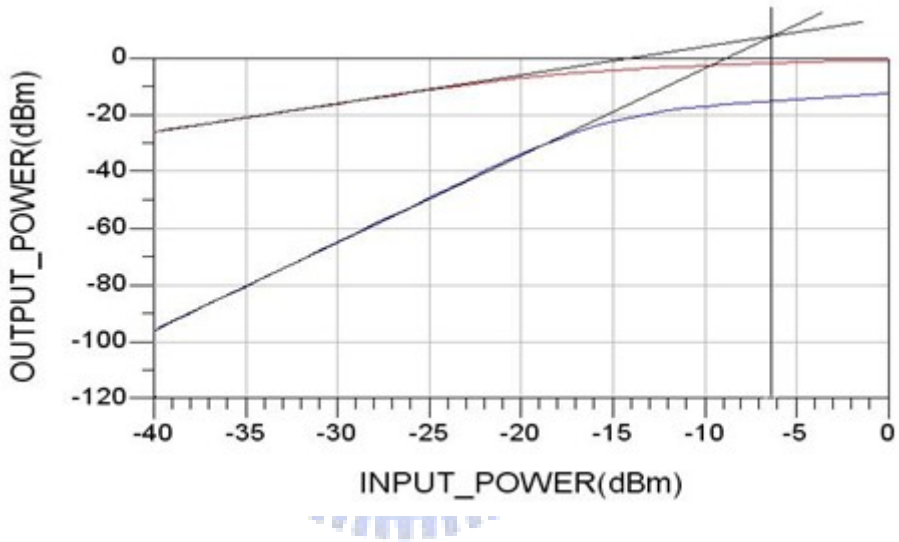
Fig.2.17 Simulated result of NF



(a)

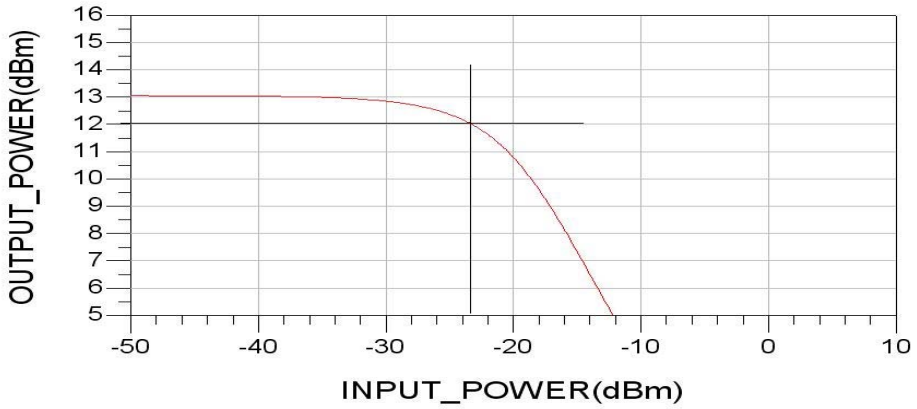


(b)

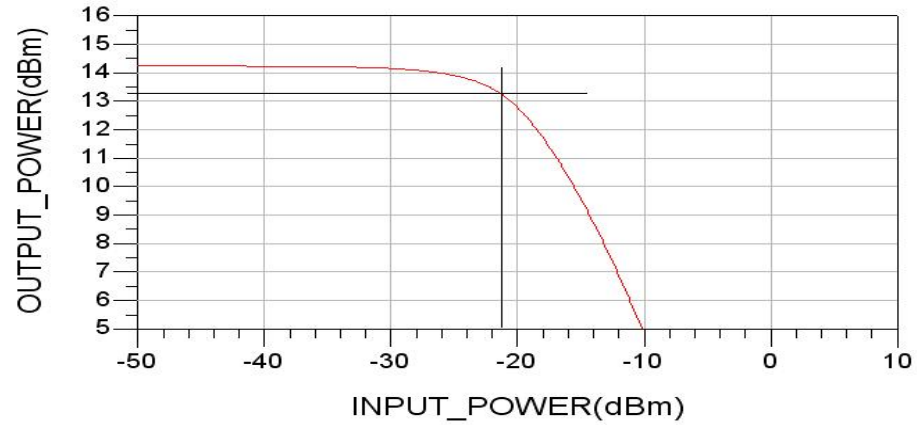


(c)

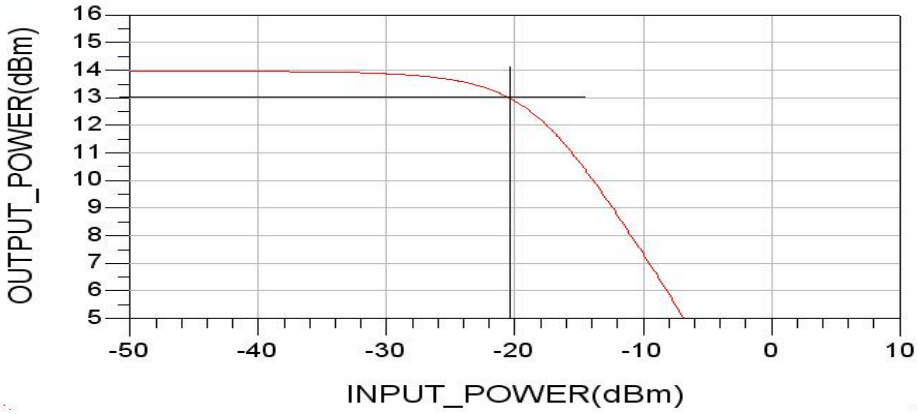
Fig.2.18 Simulated results of IIP3 at (a) 3.1GHz. (b) 6.8GHz. (c) 10.6GHz.



(a)



(b)

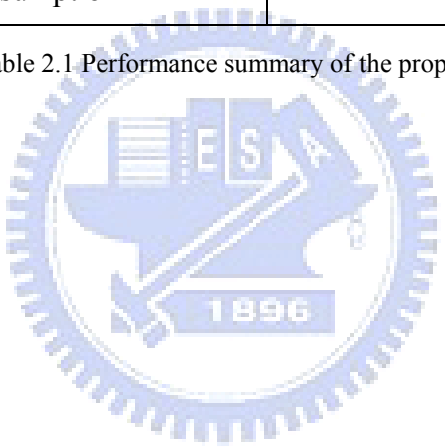


(c)

Fig2.19 Simulated results of P1dB at (a) 3.1GHz. (b) 6.8GHz. (c) 10.6GHz

Specification	Post Simulated
Input Return Loss (dB)	-20.9 ~ -10.9
Output Return Loss (dB)	-17.4 ~ -11.1
Gain (dB)	13 ~ 14.3
Isolation (dB)	-34.7 ~ -80.0
IIP3 (dB)	-9 ~ -6.2
P1dB (dB)	-23.4 ~ -20.3
NF (dB)	3.34 ~ 4.65
V_{dd} (V)	1.0V
Power Consumption	17.75mW

Table 2.1 Performance summary of the proposed LNA



Ref.	Process	BW (GHz)	S11 (dB)	S22 (dB)	Gain ave.(dB)	NF (dB)	IIP3	Power (mW)
This work (Sim.)	0.18um CMOS	3.1~10.6	<-10.9	<-11.1	13.5	3.3~4.7	-9.0	17.5
[8] 2004 (Sim.)	0.18um CMOS	3.1~10.6	<-10	<-9	18	5~7	N/A	54
[16] 2005 (Meas.)	0.18um CMOS	3.1~10.6	<-11	<-14	8.85	4.5~5.1	-6.2*	20
[17] 2007 (Meas.)	0.18um CMOS	3.1~10.6	<-9.7	<-8.4	11.4	4.12~5.16	0.72#	22.7
[18] 2008 (Meas.)	0.13um CMOS	3.1~10.6	<-17.5	<-14.4	7.92	2.5~4.56	-4*	10.68
[19] 2006 (Meas.)	0.13um CMOS	3.1~10.6	<-9.5	N/A	9.4	3.6~4.95	-7.2*	19

Table 2.2 Comparison of UWB LNA

Chapter 3

9−26GHz Wideband CMOS LNA Design

3.1 Introduction

Square Kilometer Array (SKA) is one the most advanced radio telescope technology. Its observation and operation frequencies are 100MHz - 25GHz. The Square Kilometre Array (SKA) is a radio telescope in development which will have a total collecting area of approximately one square kilometre. It will operate over a wide range of frequencies and its size will make it 50 times more sensitive than any other radio instrument. By utilizing advanced processing technology it will be able to survey the sky more than ten thousand times faster than ever before.In the outer space communication aspect, in NASA Space Communication and Navigation Architecture Recommendations for in 2005-2030 of Space Communication Architecture Working Group (SCAWG) has the very clear introduction to the future outer space communication construction[14]. It divides SCA into approximately four regions : earth, moon, mars vicinity and deep space. And it uses the frequency of UHF, S, L, K, Ku and Ka frequency bands. For example, Ground-based Earth Element to Near-Earth Relay Element is use 13 ~ 15 GHz and Launch Vehicles、Earth Orbital User、Lunar Surface and Orbital User is use 22 ~ 27 GHz. Therefore, that is the reason we chose 9 – 25 GHz frequency band to design LNA. The table.3.1 shows the used frequency band of the applications.

Application		Frequency Band
Astronomy	SKA	100MHz – 25GHz
Military	EW / ECM	9 – 26 GHz
Satellite Communication	Lower Ka-band	17.7 – 21.2 GHz
Space Communication	Ground to Space	13 – 15 GHz
Space Communication	Space to space	22 – 27 GHz

Table.3.1 The used frequency band of the applications

3.2 The principles of narrowband LNA

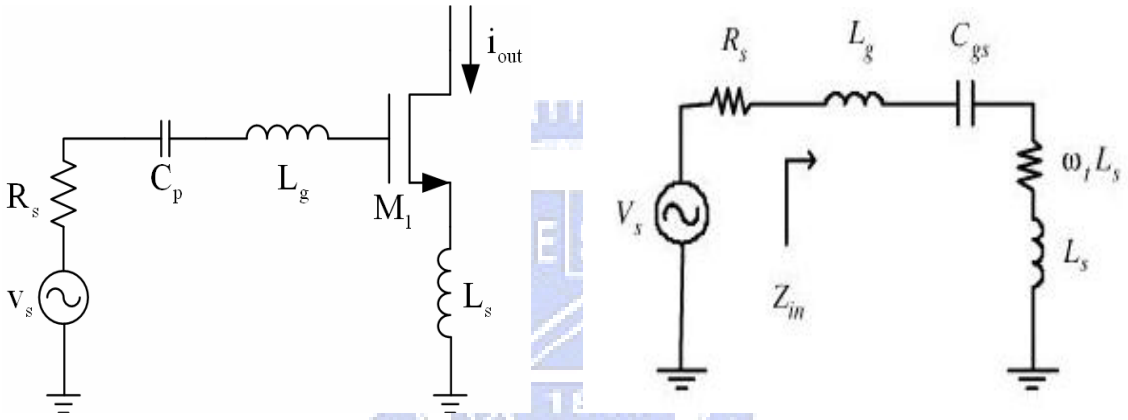


Fig.3.1 (a) The input part of a typical narrowband LNA Fig.3.1 (b) The small signal equivalent circuit

The input part of a typical narrowband LNA is shown as Fig.3.1 (a). The inductor L_g is added for the simultaneous input matching and low NF [15]. Fig.3.1 (b) shows the small signal equivalent circuit for the input part of the narrowband LNA, where C_{gs} is the gate-source capacitance of the transistor M_1. The input impedance of the narrowband LNA can be represented as $Z_{in} = jw(L_g + L_S) + \frac{1}{jwC_{gs}} + w_T L_S$ (3-1), where w_T is the cutoff frequency of M_1. The reactive element can be designed to resonate at the interest frequency such that Z_{in} becomes a real value with $w_T L_S$ being to R_S. Therefore, we can match the input impedance to 50Ω.

3.3 Architecture

The schematic of the proposed LNA is shown in Fug.2.2. This circuit uses two bias voltage sources of V_{dd} and V_g. It employs five-stage common source cascade architecture to enhance the gain. The inductors which are inserted between each stage are to boost the gain and to match the circuit. The capacitances which are inserted between each stage are to block DC signal and to match the circuit, too.

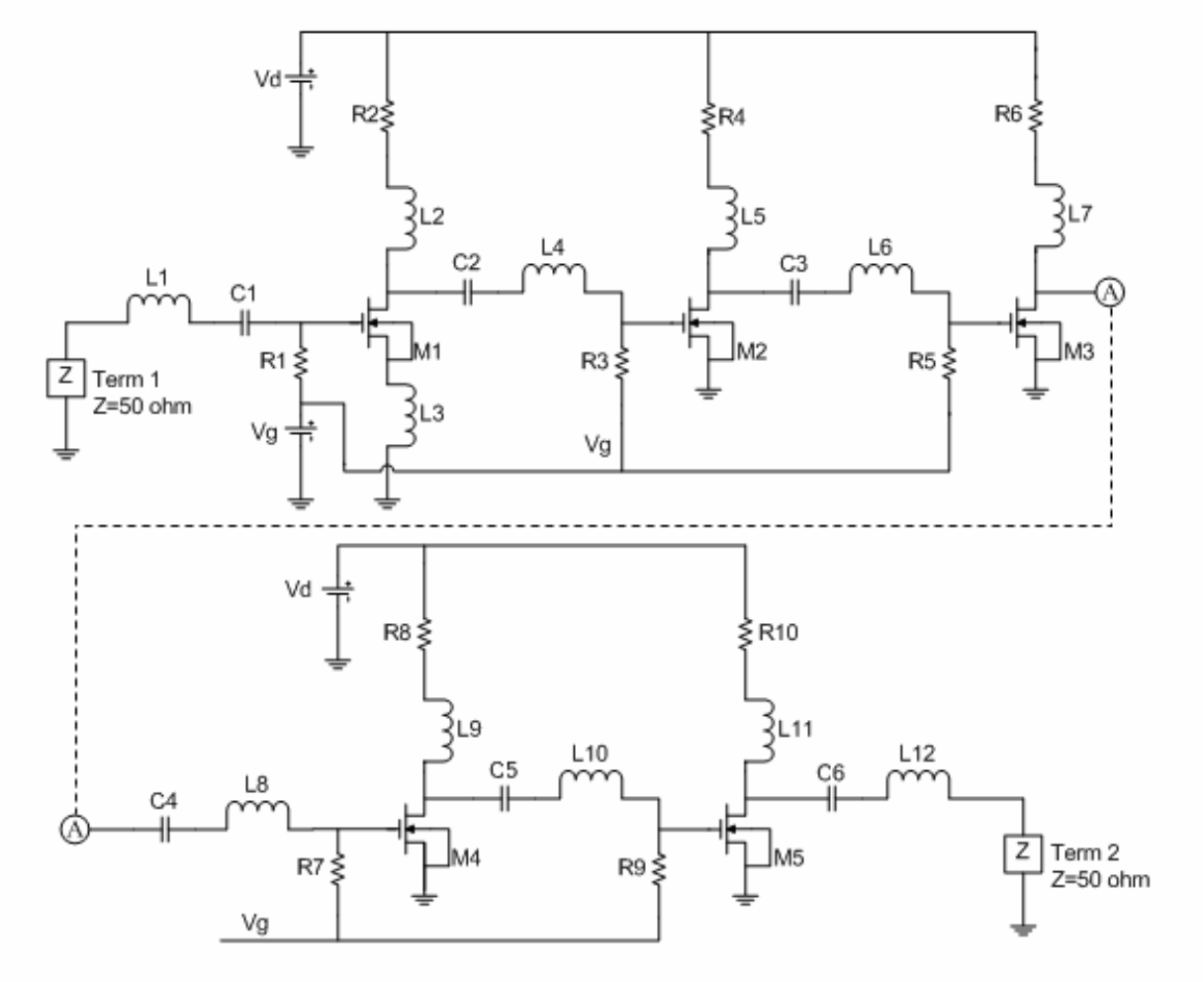


Fig.3.2 The schematic of the proposed LNA

3.4 Design Considerations

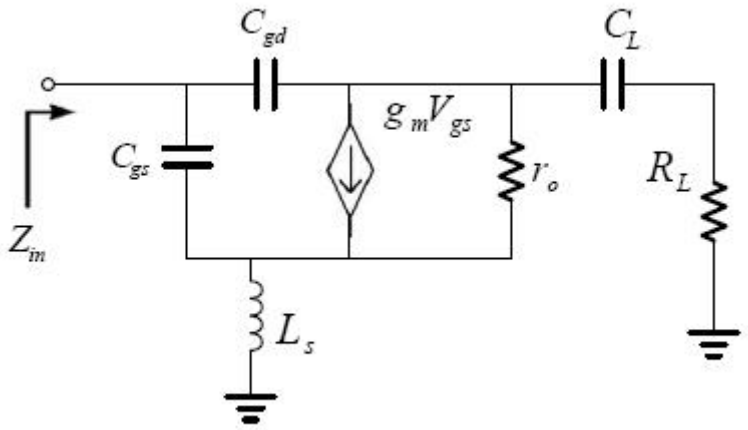


Fig.3.3 The overall input matching small signal equivalent circuit

The overall input matching small signal equivalent circuit is shown in Fig.2.2. According to the novel wideband feedback mechanism proposed by [13]. C_L and R_L are the parasitic capacitance and resistance which is contributed from the next stage. The capacitor C_L dominates at low frequency and the resistor R_L dominates at high frequency. Therefore, the wideband circuit can be divided into two parts. The LNA input equivalent circuit at high frequency is shown in Fig.2.6

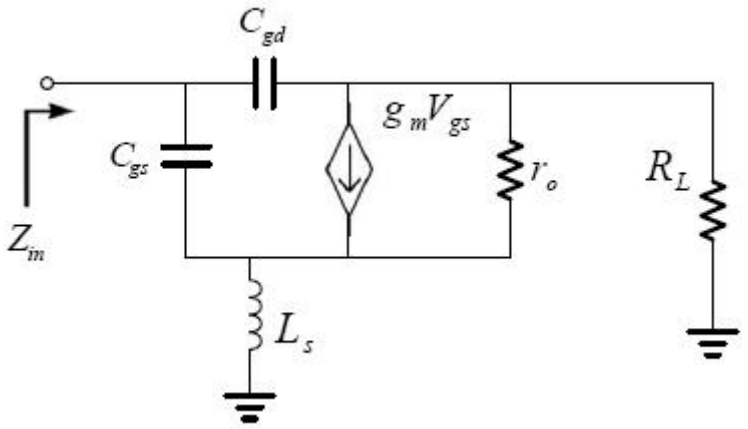


Fig.3.4. Input small signal equivalent circuit at high frequency

While we assume that $WL_S << \frac{1}{WC_{gs}}$, $WL_S << R_L$ and we can find the input impedance can be expression as following equation where

$$Z_{in} = (\frac{1}{jwC_{gs}} + \frac{L_S \gamma g_m}{C_{gs}}) \cdot [1 + \frac{C_{gd}}{C_{gs}}(1 + \gamma g_m R_L)^{-1}] \ , \tag{3-2}$$

$$\gamma = \frac{r_O}{r_O + R_L + jwL_S} . \tag{3-3}$$

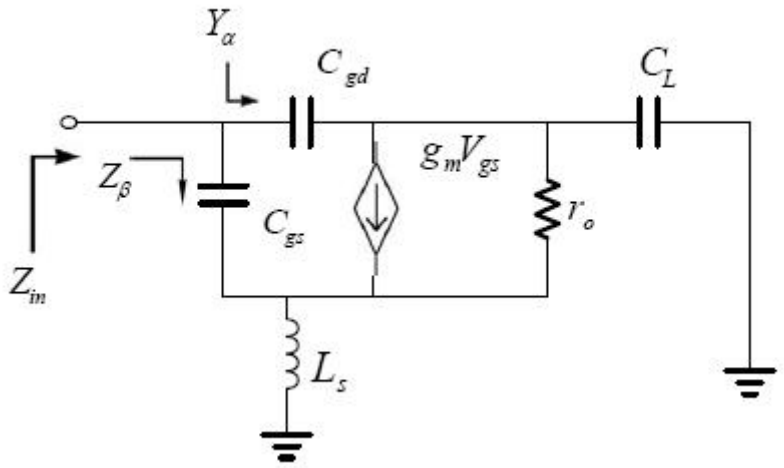


Fig.3.5. Input small signal equivalent circuit at low frequency

The LNA input equivalent circuit at low frequency is shown in Fig.2.3. In order to analysis the input impedance, we apart this circuit into two branches. Therefore, we can find the input impedance is $Z_{in} = (Y_\alpha + Z_\beta)^{-1}$. (3-4)

Y_α is the impedance looking into the $C_{gd,tot}$ and Z_β is the impedance looking into the $C_{gs,tot}$. While we assume that the current flow through the capacitor $C_{gd,tot}$ and $C_{gs,tot}$ is smaller than the current source $g_{m,tot} v_{gs}$. Thus

$$Y_\alpha = jwC_{gd} + (R_\alpha + \frac{1}{jwC_\alpha} + jwL_\alpha)^{-1} \quad (3\text{-}5)$$

$$\text{and} \quad Z_\beta = \frac{1}{jwC_{gs}} + (\frac{1}{R_\beta} + jwC_\beta + \frac{1}{jwL_\beta})^{-1}. \quad (3\text{-}6)$$

$$\text{with} \quad R_\alpha = \frac{C_L}{g_m C_{gd}} \quad C_\alpha = g_m r_o C_{gd} \quad L_\alpha = \frac{L_S C_L}{g_m r_o C_{gd}}(1 + g_m r_o) \quad (3\text{-}7)$$

$$R_\beta = \frac{g_{m,} L_S}{C_{gs}} \quad C_\beta = \frac{C_{gs}}{g_m r_o} \quad L_\beta = \frac{L_S g_m r_o C_L}{C_{gs}} \quad (3\text{-}8)$$

Fig.3.6 and Fig3.7 shows the simulated input reflection coefficients (S11) and the simulated output reflection coefficients (S22), respectively. As can be seen, the curve is near by the center of the Smith chart when frequency increases from 9GHz to 26GHz. In other words, this design can achieve wideband input matching successfully.

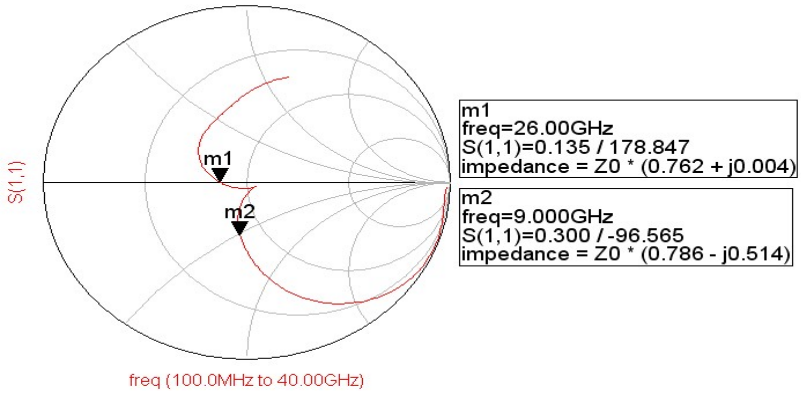


Fig 3.6 Simulated input reflection coefficients

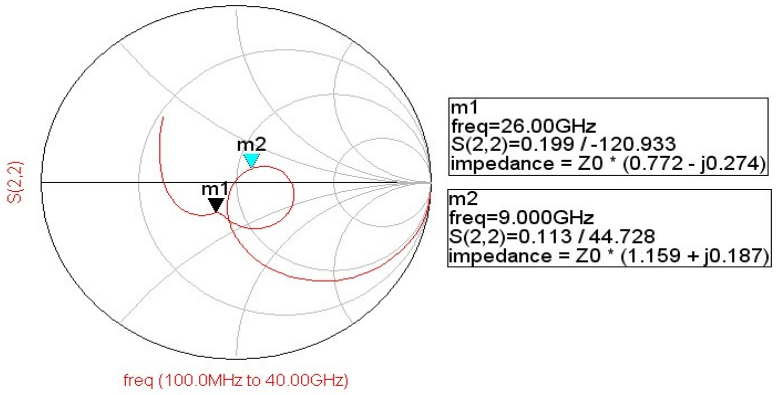


Fig 3.7 Simulated output reflection coefficients

Insert the power trace into layer2 and layer 4 ground rings. It will be equal an inductance to avoid signals feedback as Fig3.8 shows.

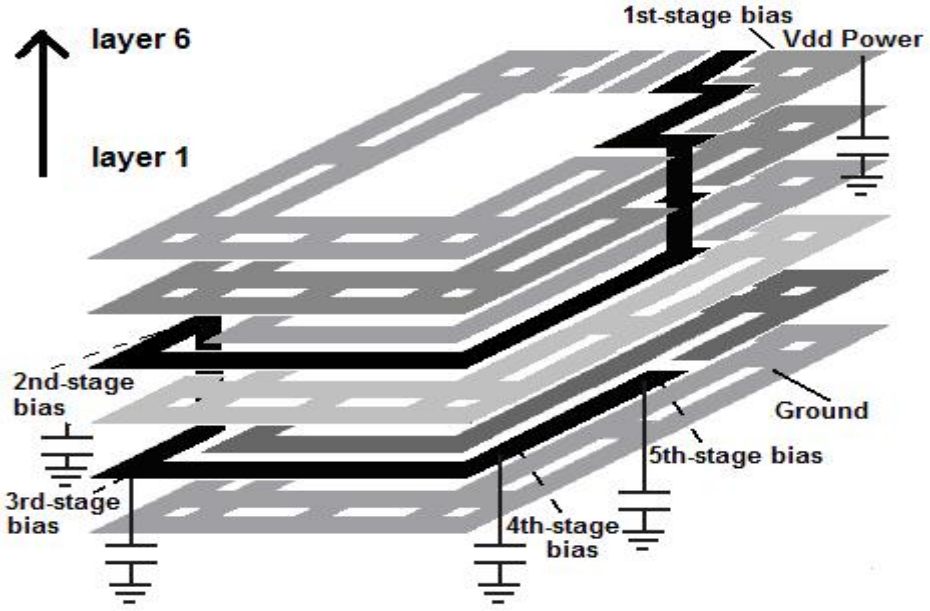


Fig.3.8 The power line of the proposed LNA

In order to achieve high gain, we use five-stage common source cascade architecture. Therefore, the RF signal can be amplified by five common source amplifiers. Unlike other complex LC matching network, this proposed LNA uses only one inductor in the input stage. Therefore, the proposed LNA will achieve low noise figure over the frequency band of interest.

3.5 Chip implementation and simulated result

The chip size is 0.974 X 1.294 (mm^2) and is fabricated on TSMC 0.18 μm mixed-signal/RF CMOS 1P6M technology as shown in Fig.3.9. Complete simulated results were simulated by ADS momentum. We will present two different biases voltages condition. The total power consumption is 100 mW at $V_g = 0.8V$, $V_d = 2.0V$ and the other one is 64.8 mW at $V_g = 0.8V$, $V_d = 1.4V$. The total performance summary will show in table3.2 and table3.3, respectively.

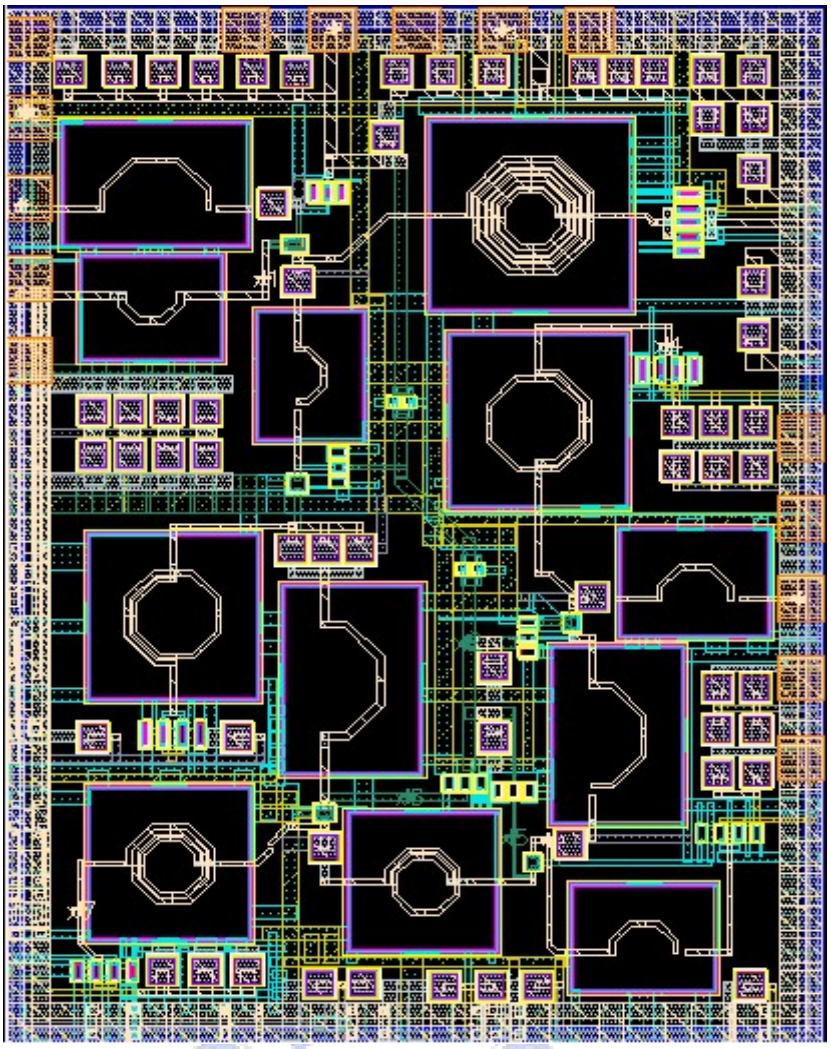


Fig.3.9 Chip layout of the UWB LNA

3.5.1 When $V_g = 0.8V$ and $V_d = 2.0V$:

The simulated result of the input return loss (S11) and the output return loss (S22) in Fig.3.10 and Fig.3.11 is lower than -10 dB, respectively. The gain (S21) in Fig.3.12 is 20dB~21.2dB over 9 ~ 26GHz. The maximum variation of power gain is about 1dB. The noise figure is between 2.4dB ~ 5.4dB as shown in Fig.3.14. The simulated input-referred third-order intercept point (IIP3) at three frequency points are shown in Fig.3.15 (a) ~ (c). The simulated IIP3 shows -17dB at 9 GHz, -11dB at 18 GHz, -8dB at 26 GHz. Fig.3.16 presents stable factor K, Mu, and B. When Mu > 1, K >1, and B >0, the proposed circuit will be unconditional stable. The performance summary is listed in table 3.2.

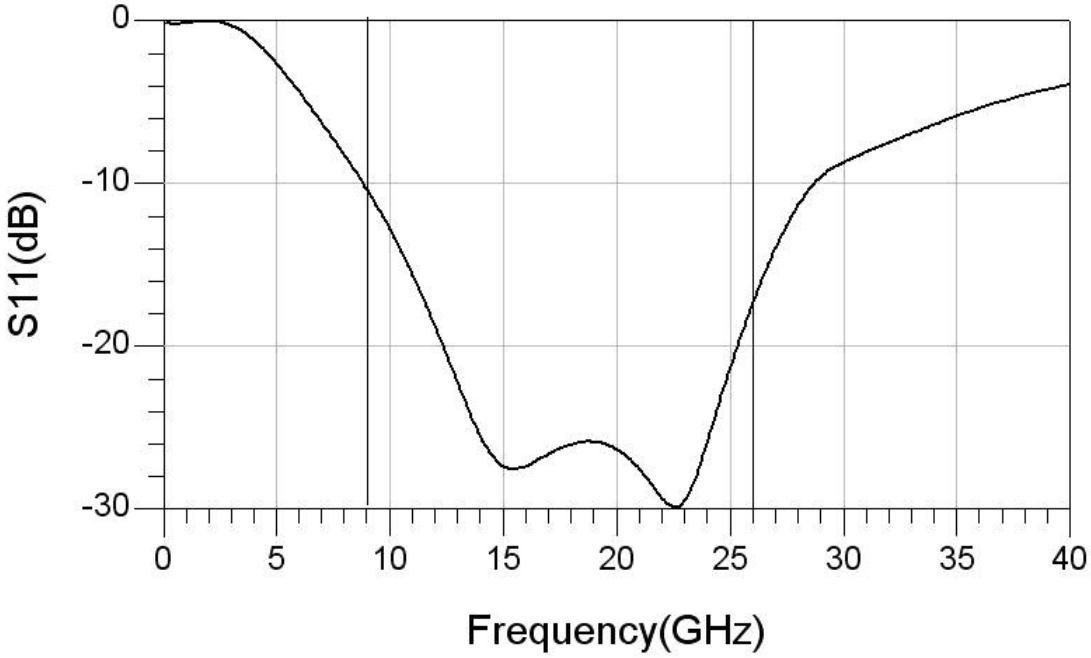


Fig.3.10 Simulated result of S11

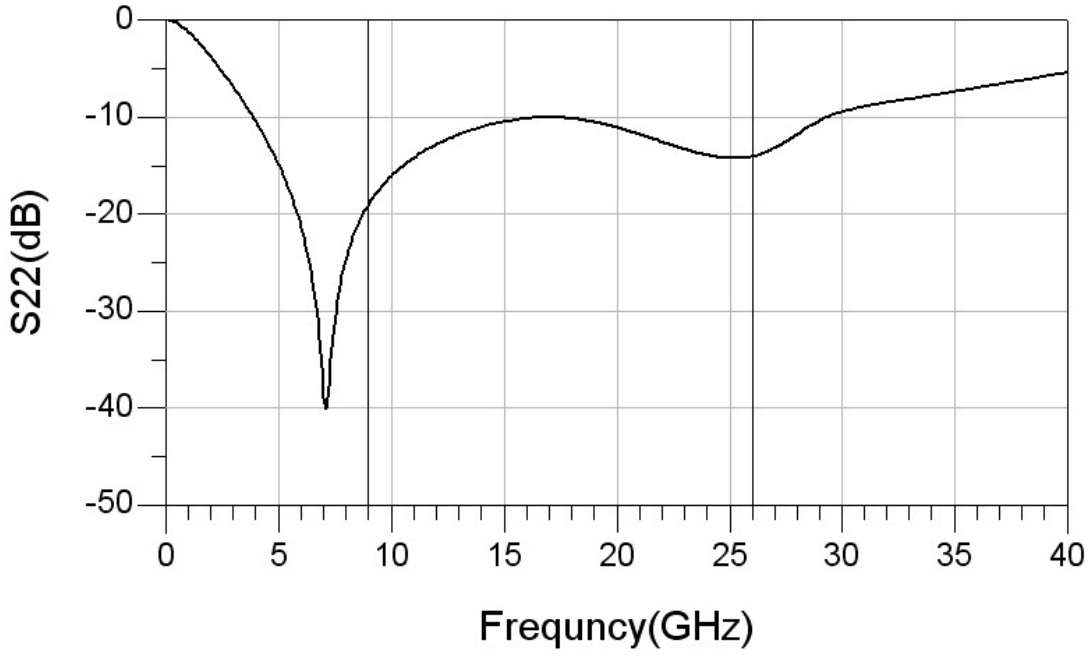


Fig.3.11 Simulated result of S22

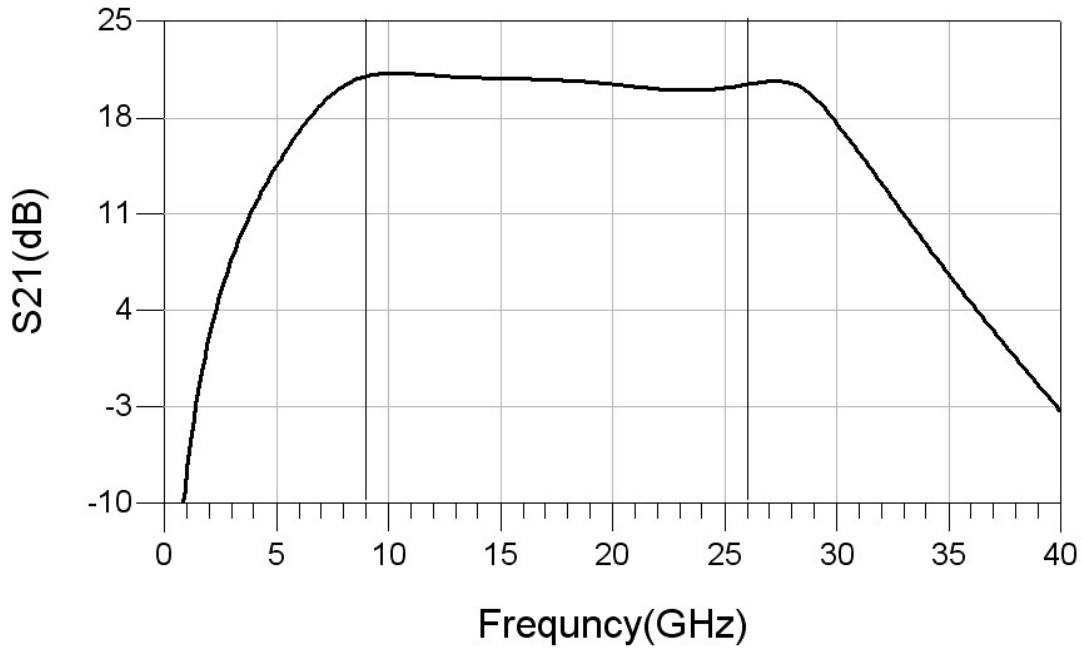


Fig.3.12 Simulated result of S21

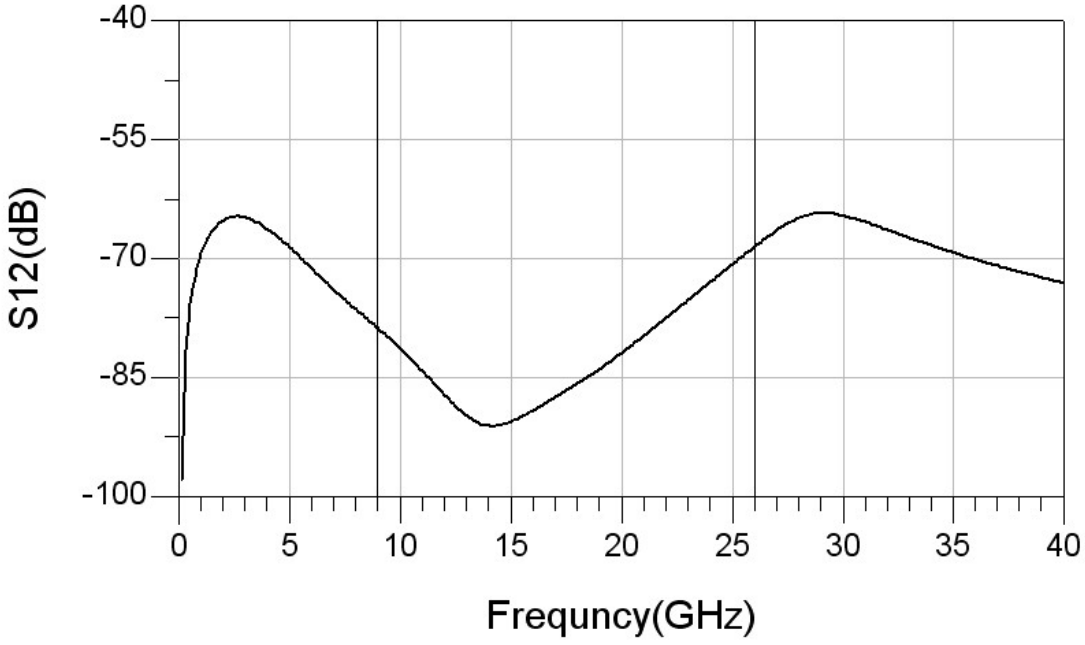


Fig.3.13 Simulated result of S12

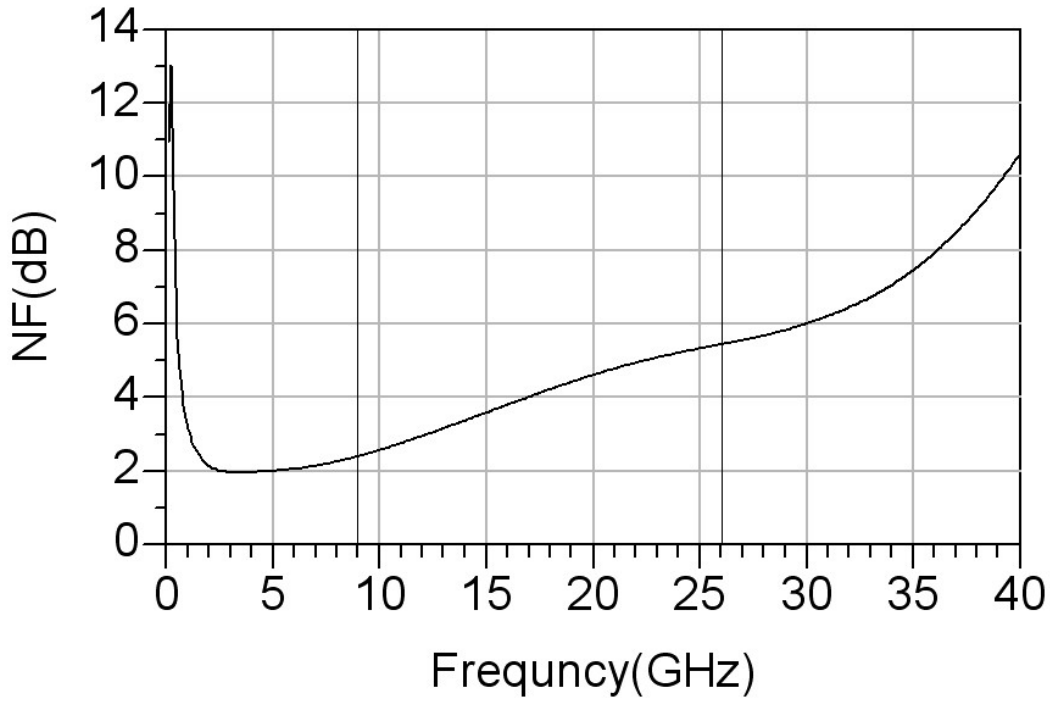


Fig.3.14 Simulated result of NF

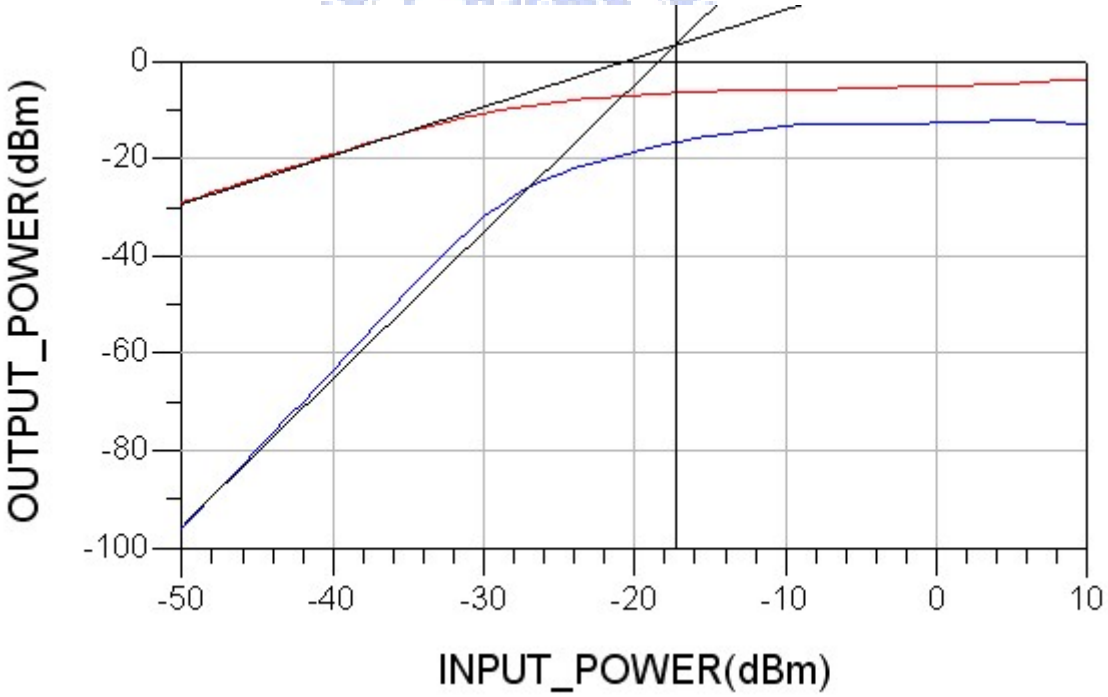


Fig.3.15 Simulated results of IIP3 at (a) 9 GHz.

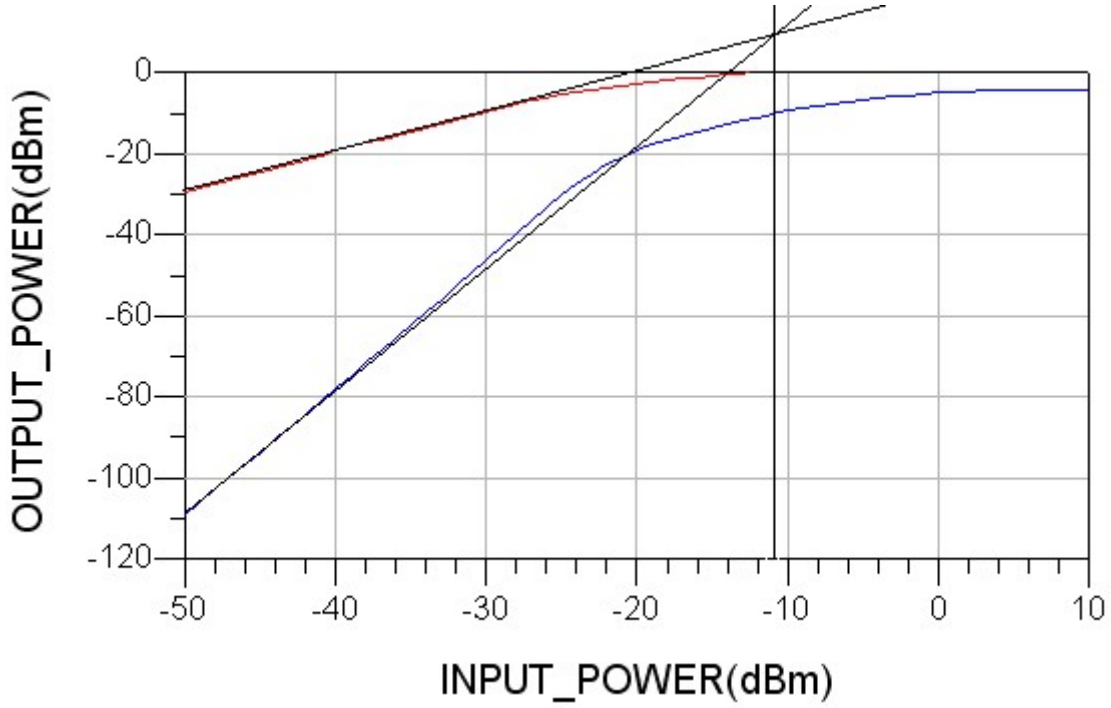


Fig.3.15 Simulated results of IIP3 at (b) 18 GHz.

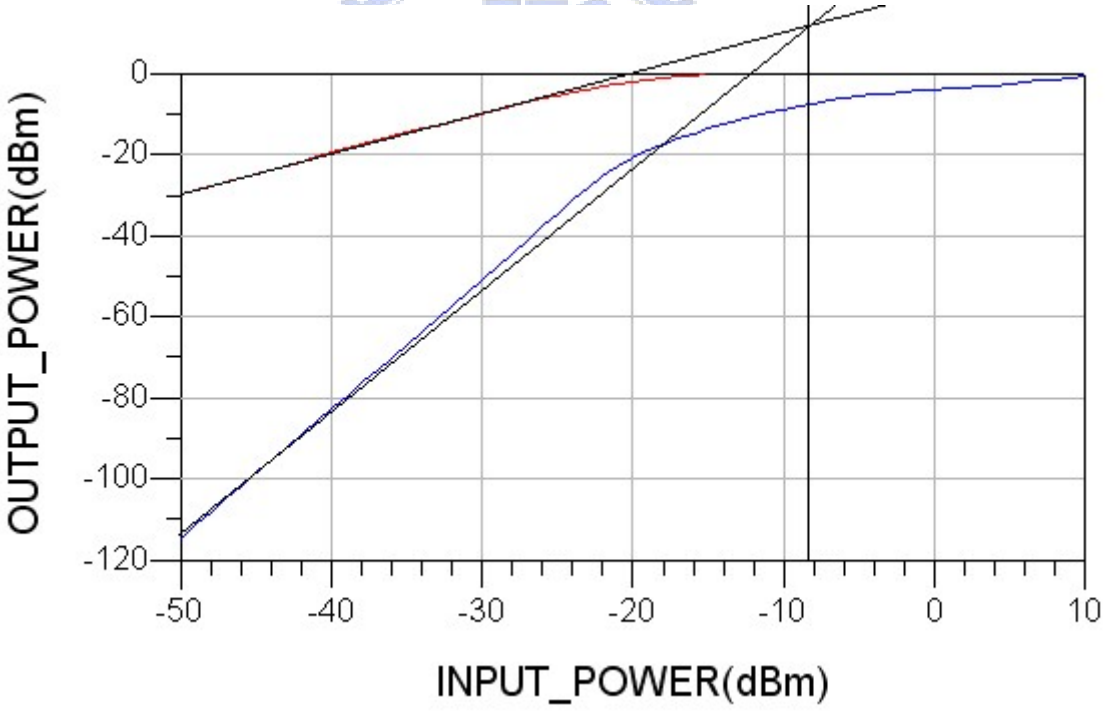


Fig.3.15 Simulated results of IIP3 at (c) 26 GHz.

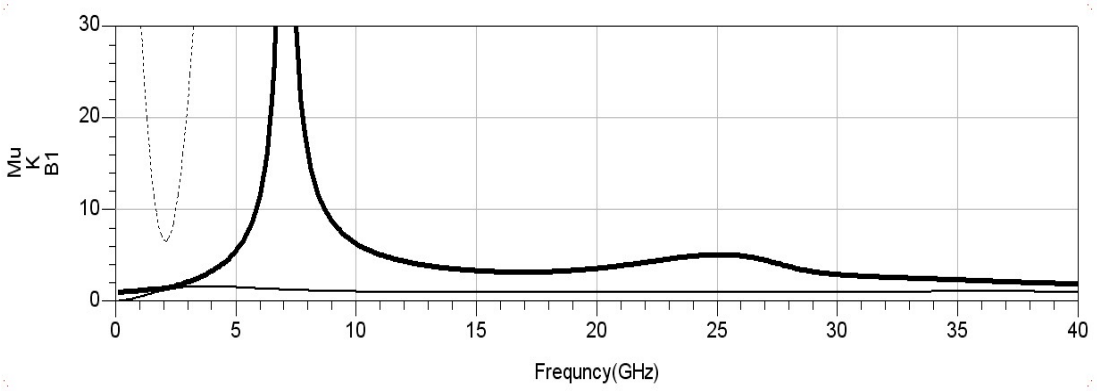


Fig.3.16 Simulated result of Stability (K: Dot line; Mu: Solid line; Thin line)

Specification	Post Simulated
Input Return Loss (dB)	-10.4 ~ -29.9
Output Return Loss (dB)	-10.0 ~ -18.9
Gain (dB)	20 ~ 21.2
Isolation (dB)	-68.5 ~ -91.1
IIP3 (dB)	-17 ~ -8
Max. NF (dB)	5.4
Min. NF (dB)	2.4
V_{dd}	2.0V
Power Consumption	100 mW

Table3.2 Performance summary of the proposed LNA

3.5.2 When $V_g = 0.8V$ and $V_d = 1.4V$:

The simulated result of the input return loss (S11) and the output return loss (S22) in Fig.3.16 and Fig.3.17 is lower than -10 dB, respectively. The gain (S21) in Fig.3.18 is 17.8dB~18.3dB over 9 ~ 26GHz. The maximum variation of power gain is less than 1dB. The noise figure is between 2.7dB ~ 5.8dB as shown in Fig.3.20. The simulated input-referred third-order intercept point (IIP3) at three frequency points are shown in Fig.3.21 (a) ~ (c). The simulated IIP3 shows -16dB at 9 GHz, -10dB at 18 GHz, -9dB at 26 GHz. Fig.3.22 presents stable factor K, Mu, and B. When Mu > 1, K >1, and B >0, the proposed circuit will be unconditional stable. The performance summary is listed in table 3.3.

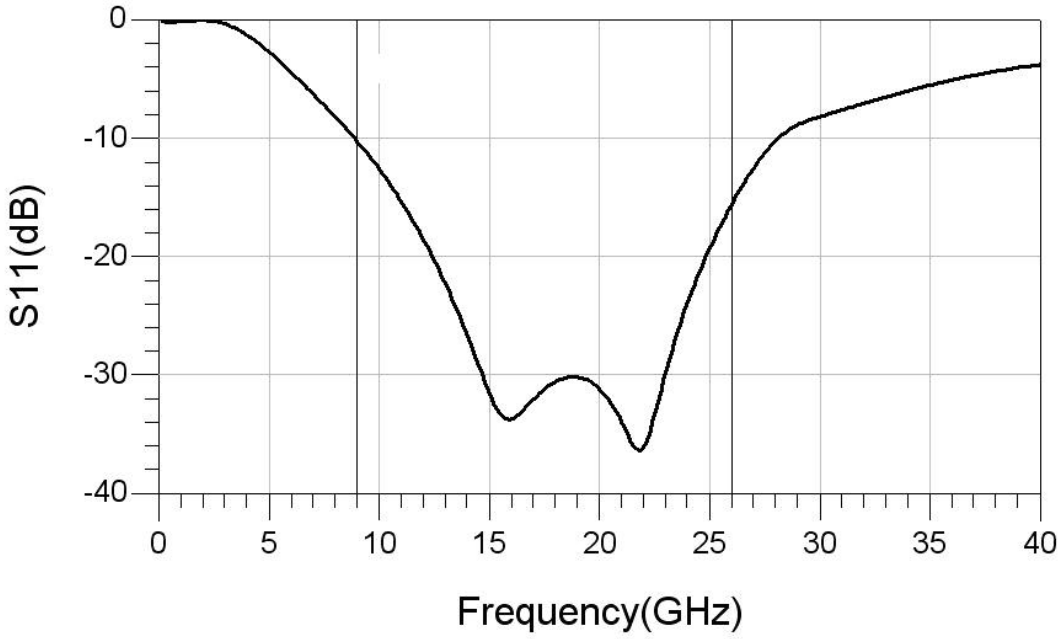


Fig.3.17Simulated result of S11

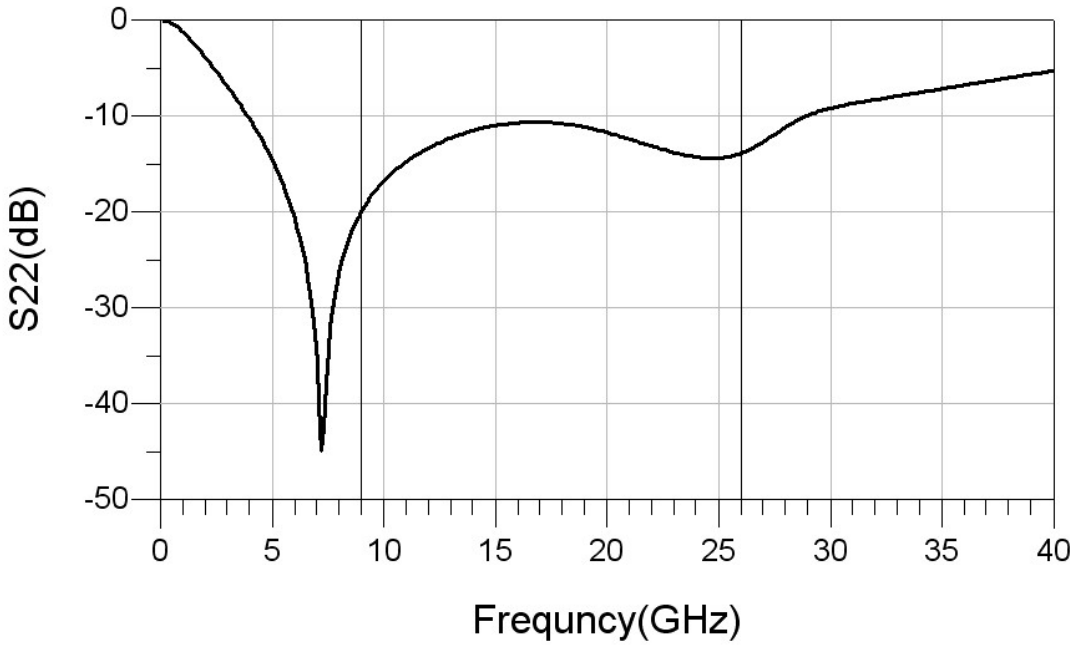


Fig.3.18Simulated result of S22

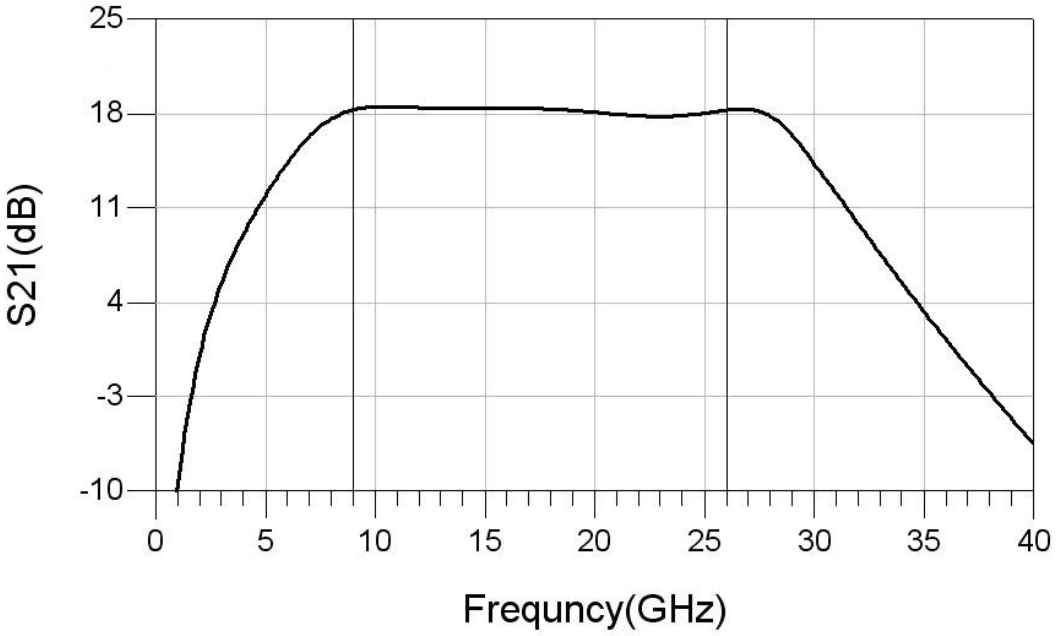


Fig.3.19Simulated result of S21

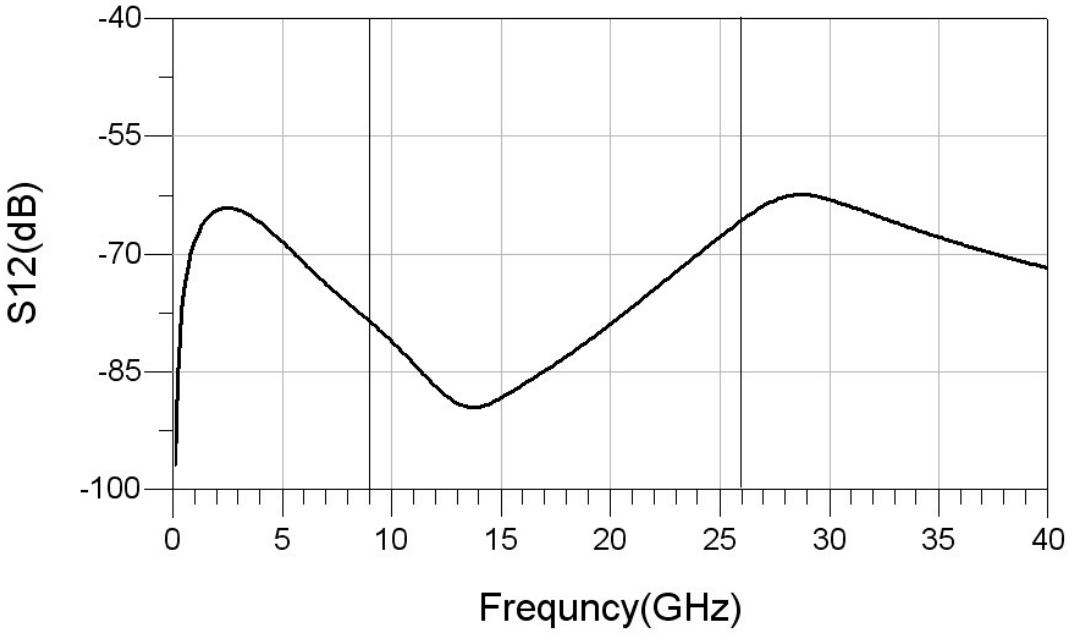


Fig.3.20imulated result of S12

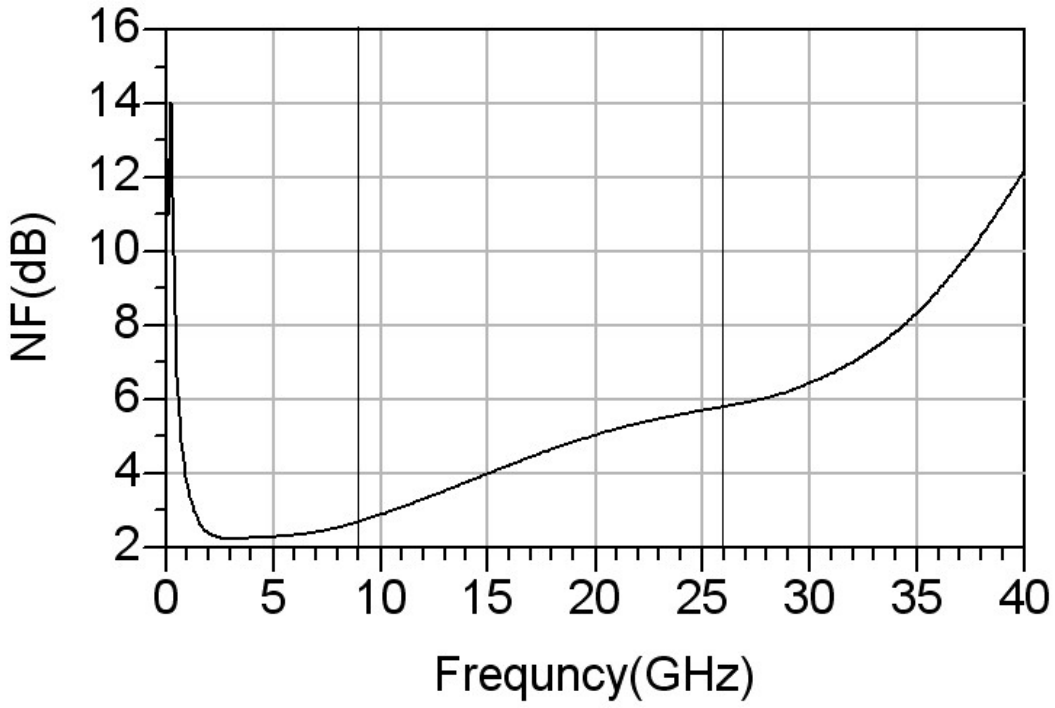


Fig.3.21Simulated result of NF

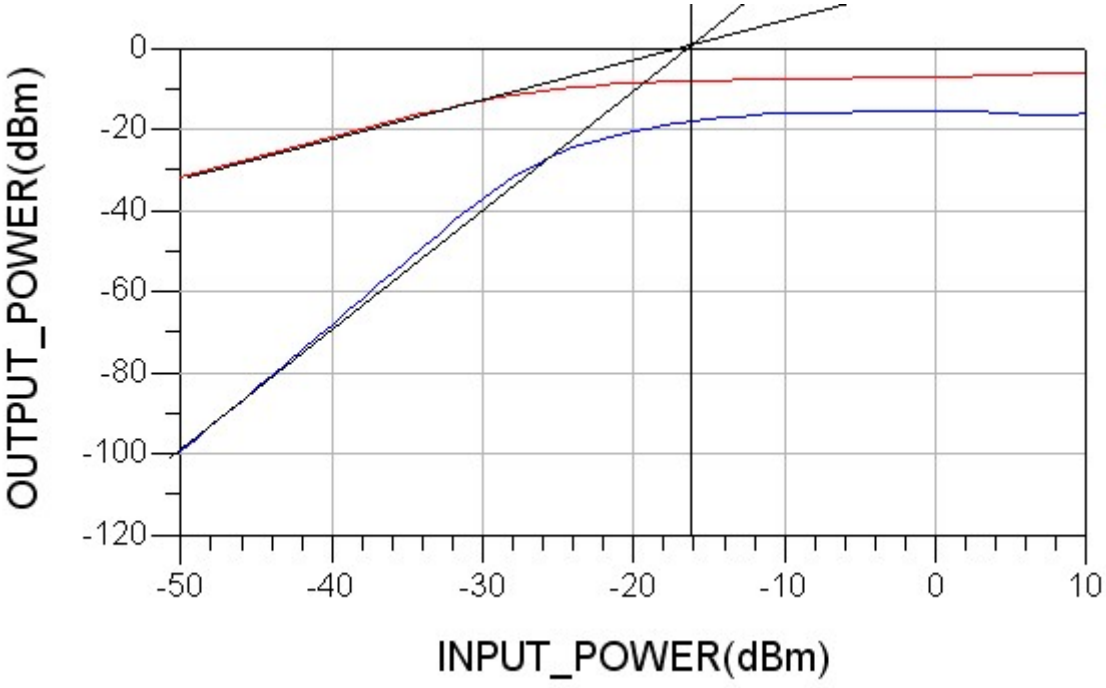


Fig.3.22Simulated results of IIP3 at (a) 9 GHz.

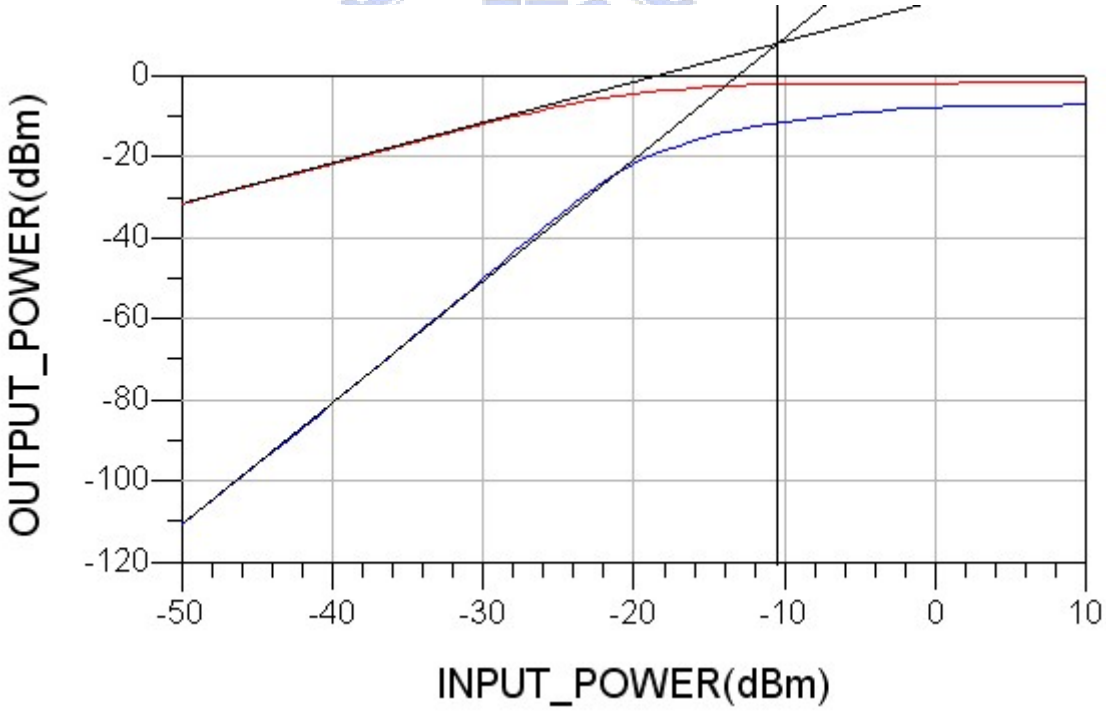


Fig.3.22Simulated results of IIP3 at (b) 18 GHz.

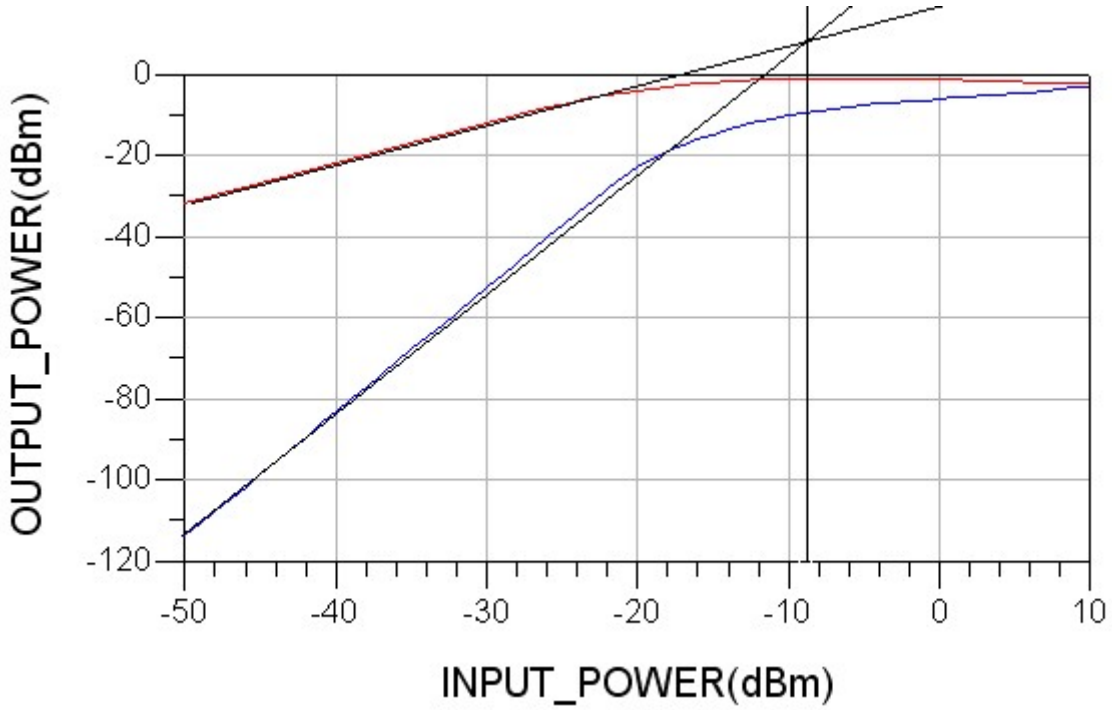


Fig.3.22Simulated results of IIP3 at (c) 26 GHz.

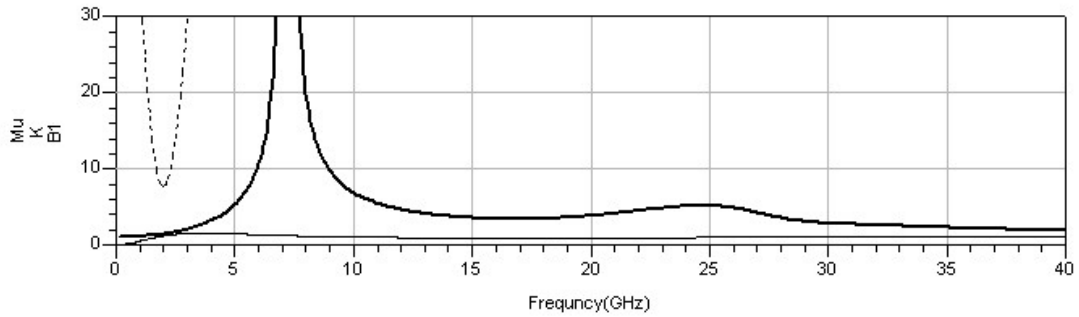


Fig.3.23Simulated result of Stability (K: Dot line; Mu: Solid line; Thin line)

Specification	Post Simulated
Input Return Loss (dB)	-10.3 ~ -36.4
Output Return Loss (dB)	-10.6 ~ -19.9
Gain (dB)	17.8 ~ 18.3
Isolation (dB)	-65.7 ~ -89.6
IIP3 (dB)	-16 ~ -9
Max. NF (dB)	5.8
Min. NF (dB)	2.7
V_{dd}	1.4V
Power Consumption	64.8 mW

Table3.3 Performance summary of the proposed LNA

Chapter 4

Conclusion and Future Work

4.1 Conclusion and Future Work

This thesis contains two studies: the low noise amplifier with current reused topology, and the 9 – 26GHz CMOS ultra-wideband low noise amplifier. For the first circuit, the LC ladder current reused configuration is used as input matching with low voltage. The current reused configuration can be considered as two-stage casade amplifier. Therefore, the RF signal can be amplified twice by this co-current structure to achieve high gain. The simulated result shows the good input and output matching will be achieved and maximum 14.3dB power gain is attained. The simulated noise figure is between 3.134 ~ 4.65dB within the wideband. For the second circuit, we propose a 9 - 26 GHz wide band 0.18μm MOS low noise amplifier. It is five-stage cascade circuit topology and match input impedance by output RC loading and source inductance. This amplifier achieves a 20.6 ± 0.5 dB power gain, 2.4 ~ 5.4dB noise figure, and good input、output matching at $V_g = 0.8V$ and $V_d = 2.0V$. Indeed, the other bias voltage condition $V_g = 0.8V$ and $V_d = 1.4V$, this amplifier achieves a 18 ± 0.2 dB power gain, 2.7 ~ 5.8dB noise figure, and good input、output matching .Obviously, the design of this circuit can tolerate the large variation of bias voltage. The result indicates that the amplifier has lower noise figure by using output RC loading and source inductance to match impedance, and standard 0.18μm MOS process can work for millimeter-wave wideband applications.

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