國 立 交 通 大 學

電 子 工 程 學 系 電 子 研 究 所

博 士 論 文

超大型積體電路連線的解析模型與最佳化設計

The Analytical Models and Optimization Designs for VLSI Interconnection

研 究 生: 李 國 暘

指導教授: 曾 俊 元 教授

鄭 晃 忠 教授

中華民國 96 年 7 月

超大型積體電路連線的解析模型與最佳化設計

The Analytical Models and Optimization Designs for VLSI Interconnection

研 究 生 : 李國暘　　Student : Gwo-Yann Lee

指導教授 : 曾俊元 博士　　Advisor : Dr. Tseung-Yuen Tseng

鄭晃忠 博士　　Advisor : Dr. Huang-Chung Cheng

國立交通大學

電子工程學系　電子研究所

博士論文

A Dissertation
Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao-Tung University
In Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in Electronics Engineering
2007
Hsinchu, Taiwan, Republic of China

中華民國 九十六 年 七 月

超大型積體電路連線的解析模型與最佳化設計

研究生：李國暖　　指導教授：曾俊元 博士

鄭晃忠 博士

國立交通大學電子工程學系　電子研究所博士班

摘要

隨著的積體電路複雜程度不斷增加，其金屬連線對電路特性的影響越來越重要. 在本論文中，我們發展了一系列完整的超大型積體電路金屬連線電容模型。這些電容模型包含三種結構 1）平行的金屬線在一平板之上，2）平行的金屬線在上下兩平板之間， 3）不同金屬層之間的連線交錯所組成的三維電容結構。利用這些電容模型計算所得到的解和 Poisson 方程式的數值解及量測資料一致。

有了這些電容模型，我們接著推導一系列的延遲及串音雜訊模型。其包含了1）單一金屬連線，2）雙線交聯的金屬連線，以及 3)多線交聯的金屬連線系統。我們也提出了考慮電感效應的延遲模型。我們發現在較慢的操作頻率及長度較長的金屬線其電感效應並不明顯。本論文提出一種新的準則可以判別電感的重要與否。這個準則可以讓晶片設計工程師減少需要考慮模擬電感的時機進而減少晶片設計的時間。這裡所提出的模型皆用 SPICE 模擬驗證並得到良好的準確性。

根據以上的模型，這裡提出針對延遲及串音雜訊的表現進行金屬連線最佳化設計的方法。我們發現 1）對於沒有上層金屬板的連線而言，最佳化的製程結構為薄的介電質層厚度，2）對於上層有金屬板的連線，較厚的介電質層及較厚的

金屬線可以提供比較好的設計容許範圍，以及 3)在較小的線寬及線距之下將，設計容許範圍會大幅度縮小。

在進入奈米級的製程時，不管是元件（前段製程）或金屬連線（後段製程），製程變動對其特性以及產品良率的影響將是關鍵性因素。因製程變動越來越明顯，設計的不確定因素越來越大，如動態/靜態功率消耗、延遲及串音雜訊的不確定。本文採取機率統計的方式來計算金屬連線寄生參數(如電容及電阻)，延遲及串音雜訊來取代傳統的 corner-based 的方法。使用這種方法可以幫助設計工程師及製程工程師找到高良率的晶片設計及製造方法。使用機率統計的分析，我們發現 1）較厚的介電質層厚度(*H*)及較厚的金屬線厚度(*T*)可以提供對製程變異比較好的抵抗力。2）對於信號延遲分析， 水平間距 (pitch) (*P*) 和介電質層厚度有一最佳的關係(*P/H=2.5*)，此一最佳結構讓延遲對製程變異不敏感。 3）對於串音雜訊而言，*P/(T+H)=0.77* 的結構對製程變異敏感度最大。設計或製程工程師應該避免此一結構。所以針對串音雜訊，我們建議佈局的範圍為 $P < 0.77*(T+H)$ 或 $P > 0.77*(T+H)$。本文的內容相信對超大型積體電路的設計以及最佳化有很大的助益。

The Analytical Models and Optimization Designs for VLSI Interconnection

Student: Gwo-Yann Lee *Advisors: Dr. Tseung-Yuen Tseng*

Dr. Huang-Chung Cheng

Department of Electronics Engineering &

Institute of Electronics

National Chiao Tung University

Abstract

Increasing complexity in very large scale integration (VLSI) circuits makes metal interconnection a significant factor affecting circuit performance. The dramatically increased amount of interconnection line in chip makes the interconnect delay and crosstalk noise more dominant factors in the overall circuit speed. In this thesis, we first develop new closed-form capacitance formulas for three major structures commonly happened in VLSI, namely, 1) parallel lines in a plane, 2) parallel lines between two planes and 3) inter-layer wire crossings which are three-dimensional (3-D) nature. The capacitance models agree well with numerical solutions of three-dimensional (3-D) Poisson`s equation as well as measurement data.

We then further derive closed-form solutions for the delay and crosstalk noise for several interconnect structures. The structures include, 1) interconnect system which

has only one line, 2) interconnect system which has two parallel coupled wires and 3) interconnect system which has multiple wires coupled with each other. We also propose analytical models considering the effects of interconnect inductance. We found the effect of inductance is not significant for lower frequency operation conditions and longer line. Hence, another contribution of this thesis is that we propose criteria to help the designer to answer the question, “when does the interconnect inductance become important?”. It is helpful to reduce the efforts of performing full chip simulation with inductance. The delay and crosstalk models proposed in this thesis all agree well with SPICE simulations.

Based on the models, interconnect delay and crosstalk performance is optimized over the range of process and design dimension of interest. In specified, we find 1) for wire without top wiring, the optimal dielectric thickness is relatively small, this agree with process concept nowadays 2) for lines with top wiring, larger dielectric thickness and wire thickness give better performance, and 3) the range of allowable wire thickness and dielectric thickness reduces seriously as the design pitch reduces.

The variations in the process, whether device (front-end) or interconnect variations (backend), is becoming critical issue for nano-era chip designs. Along with increased process variations, the design uncertainty is increasing such as dynamic power consumption, delay and crosstalk noise. Traditional corner-based analysis provides pessimism or optimism design; hence, we propose the statistical parasitic (ex. capacitance and resistance), delay and crosstalk analysis methodology which help design or process engineer to deliver the robust chip design and enhance the product yield. In this study, we find 1) the thicker dielectric thickness (H) and metal thickness (T) provide better process variation immunity. 2) For delay analysis, horizontal pitch (P) and dielectric thickness has one optimum relationship ($P/H=2.5$) to achieve designs that could reduce performance impact due to variability. 3) For crosstalk analysis, $P/(T+H)=0.77$ is

the structure most sensitive to process variation and both process and design engineer should prevent to use the structure. Hence, we recommend to use small horizontal pitch (P) so that $P < 0.77*(T+H)$ or large pitch so that $P > 0.77*(T+H)$ to minimize the impact due to process variation. These results are believed to be helpful in VLSI design and optimization.

誌　謝

僅以此論文獻給我敬愛的父母-李興男先生與朱秀琴女士，感謝你們多年來辛苦的培育我，教育我，有了你們持續的支持與付出，才能讓我得以全心投入學業，完成博士學位。

感謝我的論文指導教授鄭晃忠博士及曾俊元博士，老師在研究上的熱心指導以及謙恭溫和的待人處事，都讓我獲益良多，也使我能順利完成博士學位。

感謝實驗室的學長、同學及學弟們，謝謝你們在學術研究或是生活上都能夠給予我支持與關心，使得我的研究能夠順利完成，其中包含了黃全洲學長、史德智同學、王志良學弟。有了你們在我的研究生生涯一路不斷的相互扶持，才能順利完成論文。

感謝宋美雅女士在我研究生生涯中默默的在背後支持我，在我低落的時候，可以陪伴著我，使我能再次打起精神面對下一個挑戰，由衷的感謝妳。

最後感謝所有曾經幫助過我的朋友們，謝謝你們一路上給我的支持與關心，我今天才可以完成博士學位。

Contents

Table Lists

Chapter 1

Chapter 3

Chapter 6

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

layer) has no metal plates at (n+1, n+2 & n-1 and n-2-th layer) interlayer.

Chapter 1 Introduction and Motivation for Research

This chapter presents the introduction and motivation for the modeling of Very-Large-Scale-Integrated circuit (VLSI) interconnection. It is well known that the interconnect is becoming an important bottleneck in Ultra-Large-Scale-Integrated circuit (ULSI) performance. Accurate interconnect modeling methods are required to evaluate interconnect parasitic and it's impact on the interconnect performance and the optimization interconnect design.

In Section 1.1, we first present an overview and background for multilevel copper metallization. Section 1.2 reviews the basic interconnect process for CMP, and Section 1.3 reviews the basic interconnect design method. In Section 1.4, we discuss the motivation for this thesis, including previous related work and a brief summary of the contributions of this thesis. Finally, Section 1.5 presents the organization of the rest of the thesis.

1.1 Overview Of VLSI Interconnects

The standard aluminum-copper alloy has been the choice for interconnects in integrated circuits for over three decades. However, with severe dimension shrinkage and transistor performance improvements in integrated circuits, the interconnect delay, crosstalk and the geometry variation during fabrication are becoming an important bottleneck in Ultra-Large-Scale-Integrated circuit (ULSI) performance and fabrication, especially at the gate lengths of 0.25 μm and below as shown in Fig. 1.2 [1.1]. The substitution of copper for the standard aluminum-copper alloy for interconnects is an big step in this transition. IBM and Motorola each announced their revolutionary

transition to copper interconnect technology at the 1997 IEEE International Electron Devices Meeting Fig. 1.1 [1.2, 1.3].

The migration to new alternatives material for metal and dielectric, interconnects design has bring-up many process integration issues as well as design challenge. The new technology gave more promising on smaller wire spacing and thinner wire thickness; hence, the signal integrity issue now draws more and more attention due to advanced wire technology.

1.2 Interconnect Integration and Processes Variation Issues

It is well known that multilevel topography, or surface height variation, resulting from pattern dependencies in various processes, especially Chemical-Mechanical Planarization (CMP) in Fig.1.3, is a major problem in interconnects. CMP induced copper dishing and erosion that would cause the deviations of interconnect resistance and capacitance as shown in Fig. 1.4.

With scaling of the trench thickness, erosion and dishing have to be minimized correspondingly to meet performance requirements. It is a major challenge to reach the requirements set by the International Technology Roadmap for Semiconductors (ITRS), 2005 edition, which is increasingly stringent at 65 nm and below, Table 1.1.

Process approach to improve the CMP erosion and dishing.

In order to improve polishing performance and compatibility with low-κ dielectrics, cost-efficient low down force CMP polishing techniques have to be further developed. Several potential technologies, such as ACM's electropolishing technology and Applied Materials' electrochemical-mechanical polishing (ECMP).

ACM Research proposes that electropolishing can be the solution for the next generation copper planarization [1.4]. Electropolishing can be looked at as the reverse

process of electroplating. The surface copper on the wafer, acting as an anode under external applied voltage, is converted to copper ions by losing electrons, which then dissolve into the electrolyte. The voltage will determine the current density, and the copper removal rate is proportional to the current density. This stress-free, non-contact process is friendly to low-K dielectrics. However, the price is low planarization capability due to nearly equal removal rates at field, protruding, and recessed locations [1.5]. There is no dielectric loss or erosion problem, however, since electropolishing is inert to nonconductive materials. Thus an initially flat topography is necessary to limit dishing due to low planarization ability. The use of conventional CMP to remove steps in the bulk copper prior to electropolishing is a potential solution, although this appears to require two equipment sets and steps. Another approach is to place dummy fill in wide structuresto flatten the post-plating topography [1.4]. However, the problem of low planarization ability still limits the application of electropolishing in manufacturing.

Applied Materials' electrochemical-mechanical planarization, or ECMP, is seeking to solve the problems of CMP and electropolishing, while keeping the advantages of these two processes by combining electrochemical copper removal with conventional CMP [1.6]. The wafer with an applied voltage is submerged in an electrolyte, as in electropolishing. A specially designed chemical is added into the electrolyte that passivates the surface of copper to block copper dissolution. A rotating polishing pad then softly removes the contacted copper-complex passivation layer only on raised copper areas to open the path for copper dissolution under the applied voltage. The recessed areas are protected by the passivation layer and remain untouched. Figure 1.5 compares the differences in polishing mechanism between electropolishing and ECMP.

However, ECMP still has some limitations in its application to current

semiconductor technology. Conventional CMP steps are stilled required, following the bulk copper removal by ECMP, in order to achieve copper clearance and then barrier removal. However, the over-polishing using conventional CMP required to clear the copper from field regions to account for both chip-scale topography and wafer-scale, nonuniformity can still introduce significant dishing and erosion.

Design approach to improve the CMP erosion and dishing.

In order to further improve the polishing productivity and planarity to compete with ECMP, dummy filling, slotting will likely be required in conjunction with CMP process improvements. Design method to modeling these geometry variation and corresponding performance impact is also important to prevent under-design or over design which both cases will decrease the yield of the chip.

1.3 Theory Background and Motivation Of This Thesis

Many works have been devoted to calculating line capacitance, e.g., [3.2]-[3.4]. Sakurai and Tamaru [3.2] derived formulas, both for parallel lines on a large plane. Choudhury et al. [3.3] gave models for several layout primitives but only for one set of technology parameters. Chern et al. [3.4] gave a general capacitance formula for three-dimensional crossing lines assuming the same dielectric and wire thickness for all layers.

For delay and crosstalk modeling, Sakurai [4.15] derived a good simple solution of the partial differential equation of a single isolated line under the assumption of step input waveform. This model is good for its intended applications such as two coupled lines and high input impedance gates. However, it overestimates or underestimates the amount of crosstalk signal for more general structures. Moreover, no general closed-form solution of the delay time and crosstalk noise voltage was

shown in Sakurai's paper in the case of two coupled lines. Cases and Quinn [4.16] discussed the transient response of single RLC transmission lines but the closed-form solution was omitted from their work. The coupled interconnect structure, which is very important in VLSI circuits, was not discussed. Davis and Meindl [4.17], [4.18] gave the closed-form solution for coupled RLC transmission lines but the step input, infinite length line and open load were assumed in their work.

The yield loss will worsen in future technologies due to increasing process variations. This is because as the feature sizes decrease, the ability to control the manufacturing spread or accuracy of a given feature size or doping concentration is also decreasing. Along with increased process variations, the uncertainty caused by design is also increasing such as interconnect coupling noise and delay. The impact of these process variations on performance has been increasing with each process technology generation. These is no any method so far for the optimization design of interconnect by considering the process variation.

Thus, the main goals and objectives of this thesis are as follows:

1. Develop comprehensive and accurate interconnect capacitance formulas for delay, crosstalk and optimization design
2. Develop an generalized accurate delay and crosstalk modeling for optimization design
3. Provide the interconnection optimization method considering both the delay and crosstalk noise; and
4. Provide the statistical modeling and interconnection optimization method considering the process variation

1.4 Thesis Organization

This thesis is organized into eight chapters. Chapter 2 gives a brief summary of the plan and procedure for this thesis.

In Chapter 3, the comprehensive capacitance, resistance and inductance modeling methods are discussed. Chapter 4 introduces the comprehensive interconnect delay and crosstalk analytical modeling for various interconnect structures. Chapter 5 presents the interconnect optimization method based on the analytical formulas derive from chapter 3 and chapter 4. Chapter 6 presents the statistic capacitance, delay and crosstalk models and optimization design based on the model is discussed. Chapter 7 summarizes the major results and contributions of this thesis. Finally, Chapter 8 discusses potential topics for future research in this area.

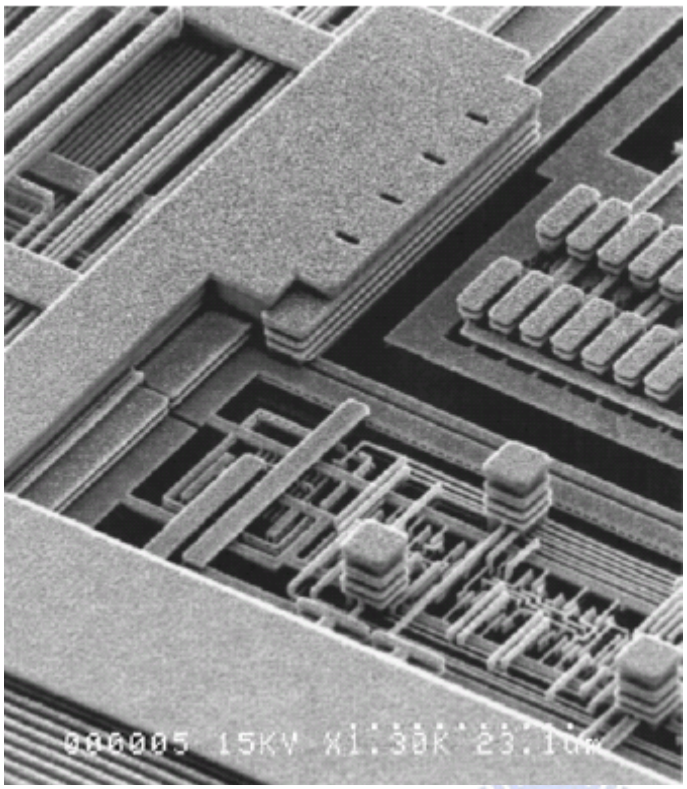


Figure 1.1 Copper metallization morphology of a six-level structure.

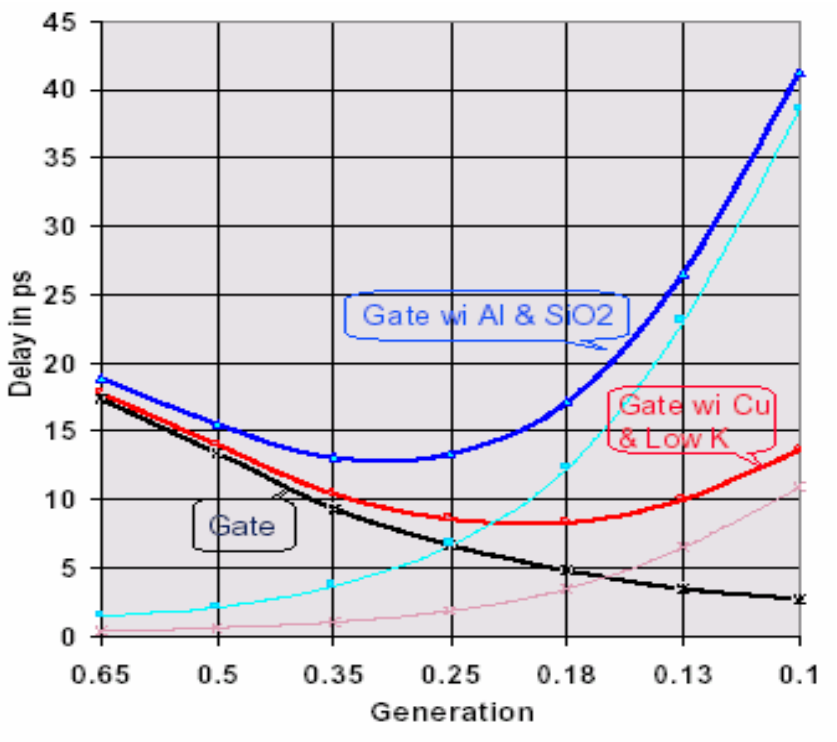


Figure 1.2 Circuit delay as a function of the feature size (low K=2).

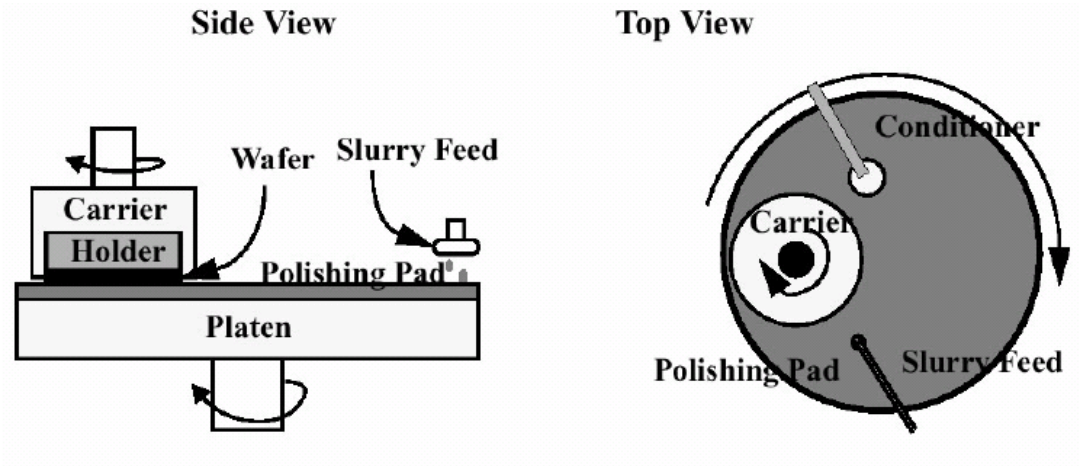


Figure 1.3 CMP tool.

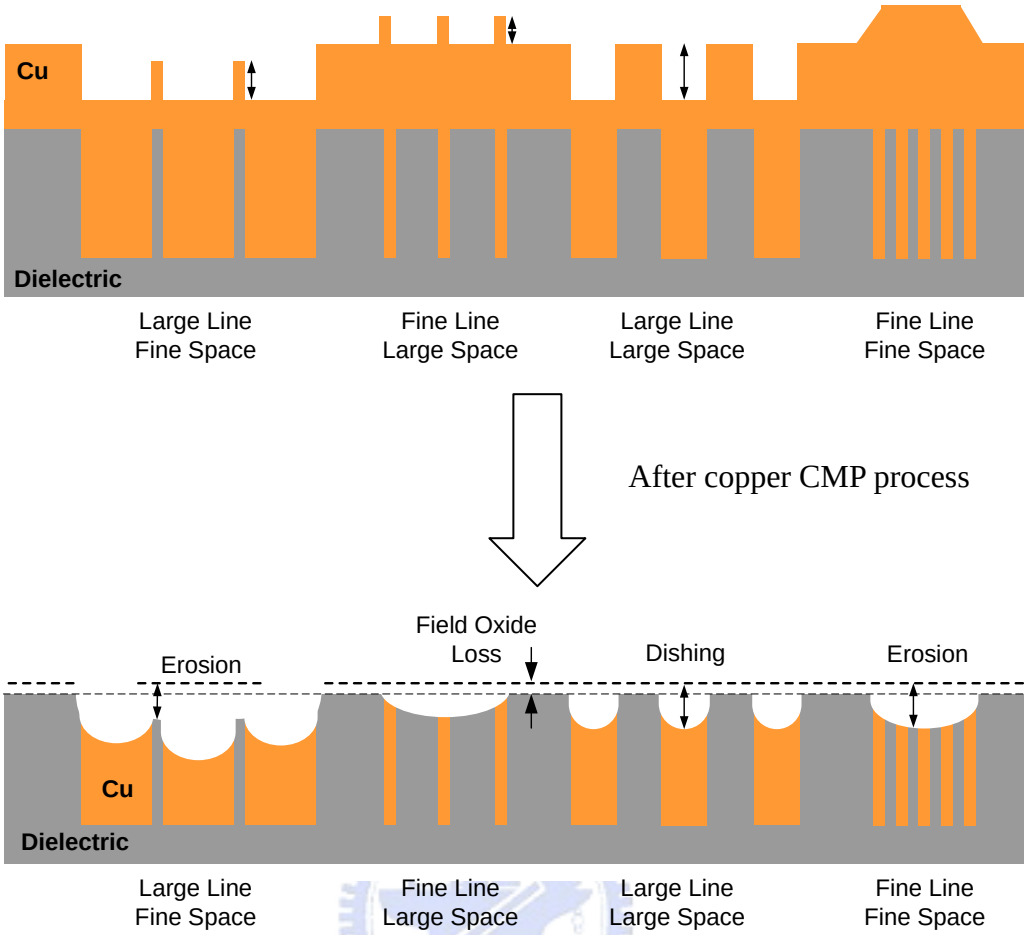


Figure 1.4 Copper CMP pattern dependencies.

Table 1.1 MPU interconnect technology requirements of SIA roadmap—near-term years.

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	15	13	12	11	9	8	7	6	6
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	17	14	13	11	9	8	7	7	6
Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	250	260	260	260	280	280	280	250	250
Cu thinning global wiring due to dishing (nm), 100 µm wide feature	24	21	19	17	15	14	13	13	10

White: Manufacturable solution exists, and are being optimized

Yellow: Manufacturable solution are known

Red: Manufacturable solution are NOT known

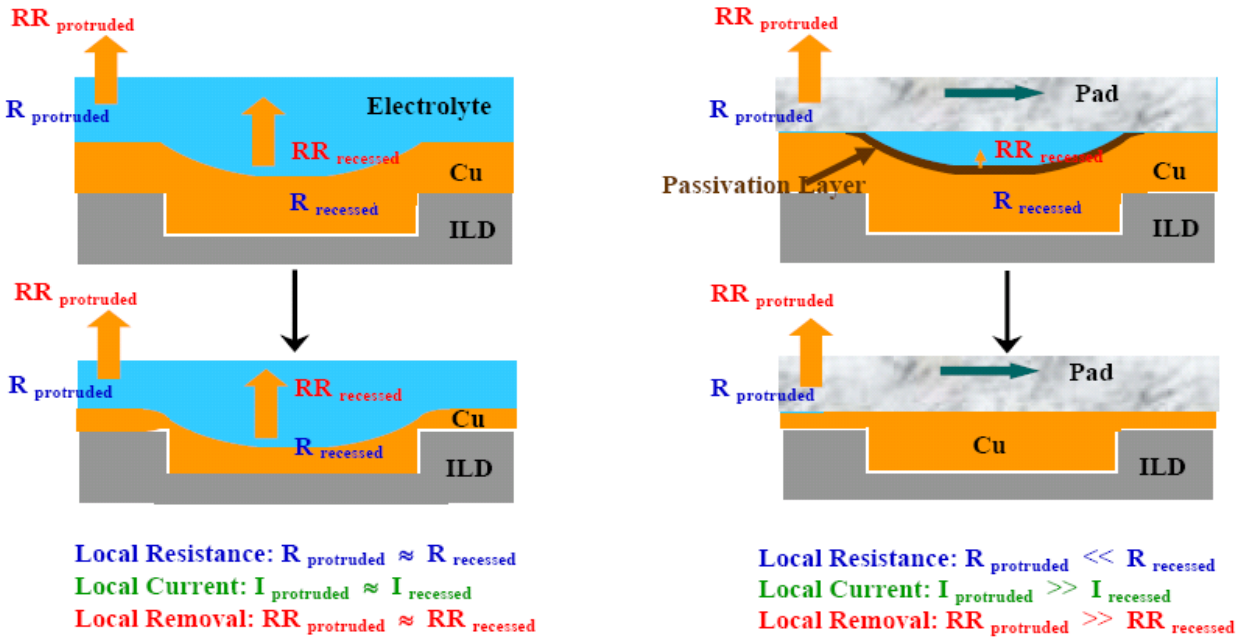


Figure 1.5 Mechanisms of electropolishing and ECMP [1.6].

Chapter 2 Methodologies and Modeling Developments

Before discussing the details of interconnect analytical models and optimization design, it is necessary to introduce the overall methodology and formulas development plan.

Figure 2.1 is the general interconnect structure which is driven by the drivers and terminated with receiver. The parasitic R, L and C are distributed across the interconnect. Two important performance parameters for interconnect are the delay and crosstalk noise which are correlated to the value of R/L/C parasitics.

First, an accurate interconnect parasitic models are must-have information to discuss the overall performance of interconnect. Based on the capacitance models, a set of new generalized delay and crosstalk model are derived and verified. And then, we have the required formulas on hand, the optimization design is then discussed.

In the presence of process variation, the study of the statistic analysis on delay and crosstalk are introduced.

2-1 Methodologies and Modeling Developments

The general interconnect layout is shown in Fig. 2.2. Interconnect could be categorized into three structures (Region A, B and C) based on the correlation between wire under discussion and near by interconnect layout. Region A represents interconnect surrounded by metal line at the same layers (intra-layer) and with many dense coupled wires of different layer (inter-layer) run across it. Region B represents interconnect surrounded by intra-layer wires and without inter-layer wire run over it. Region C represents interconnect surrounded by intra-layer metal lines and with single inter-wire (or a set of loosely coupled wires) run across it. In Region A, we could emulate the structure as lines with top plate. For any metal density equal 33% or greater (metal_spacing < 2*metal_width) can be approximated as a plate with negligible loss of accuracy due to the electric field shielding effect. Hence, we could model the dense-coupled wire as big plate [2.1]. Otherwise, 3-Dimensional effects need to be considered like interconnect crossover area as Region C. In Region B, the structure emulates lines without top wiring. In Region C, the capacitance is of a 3-D nature due to

fringe field in crossover section. The total crossover-area capacitance (Region C) can then be easily obtained by combining the crossover capacitance with the 2-D intralayer coupling capacitance. Then, we provide a systematic approach to decompose any structure into a series of 3-D plus 2-D segments. Therefore, the total capacitance (C_{total}) of dash wire in figure is calculated as $C_{total}=C_{Region\_B}+C_{Region\_C}+C_{RegionB}+C_{RegionA}$. The dash wire represents the wire need to calculate the capacitance in Fig. 2.2. Our assumptions are that any interconnect structures are the combination of the three basic structures and any interconnect capacitance could be extracted by dividing interconnect into the three capacitance elements. Hence, one of our goals of this thesis is to develop the capacitance models for all the three structures.

The methodology to develop the capacitance formula is highlighted in Fig. 2.3. A set of accurate empirical capacitances for the three structures mentioned above will be provided in Chapter 3 along with the methodology.

With capacitance models derived in Chapter 3, we develop analytical formulas of interconnect delay and crosstalk noise in Chapter 4. From Fig. 2.2, we could see that interconnect could be layout as single isolated wire or dense coupled wire. Hence, different delay and crosstalk noise model are developed for various interconnect structures.

To this point in the thesis, we have the detailed analysis techniques and formulas for interconnect parasitic, delay and crosstalk model. In Chapter 5, we will use the formulas derived from Chapter 3 and Chapter 4 to drive the optimization studies. Two optimization methodologies, process and design optimization, are proposed in Chapter 5. The goal of the optimization is to find the maximum design or process window that meet the delay and crosstalk noise criterion simultaneously.

The statistical analysis techniques are discussed in Chapter 6. We will propose the method for statistical capacitance, delay, crosstalk analysis. The proposed methodology is shown in Fig.2.4. Our plans, based on the methodology, are to develop (A) *layout design techniques* that can deal with variability, and (B) *process parameters* that reduce the

performance due to variability.

2-2 Summary

This research adopts an empirical modeling methodology for interconnect capacitance. Delay and crosstalk noise analytical models are proposed, too. By incorporating the capacitance, delay and crosstalk models presented in this thesis, the optimization design is presented. Finally, the statistical analysis method is given to consider the issue of process variations.

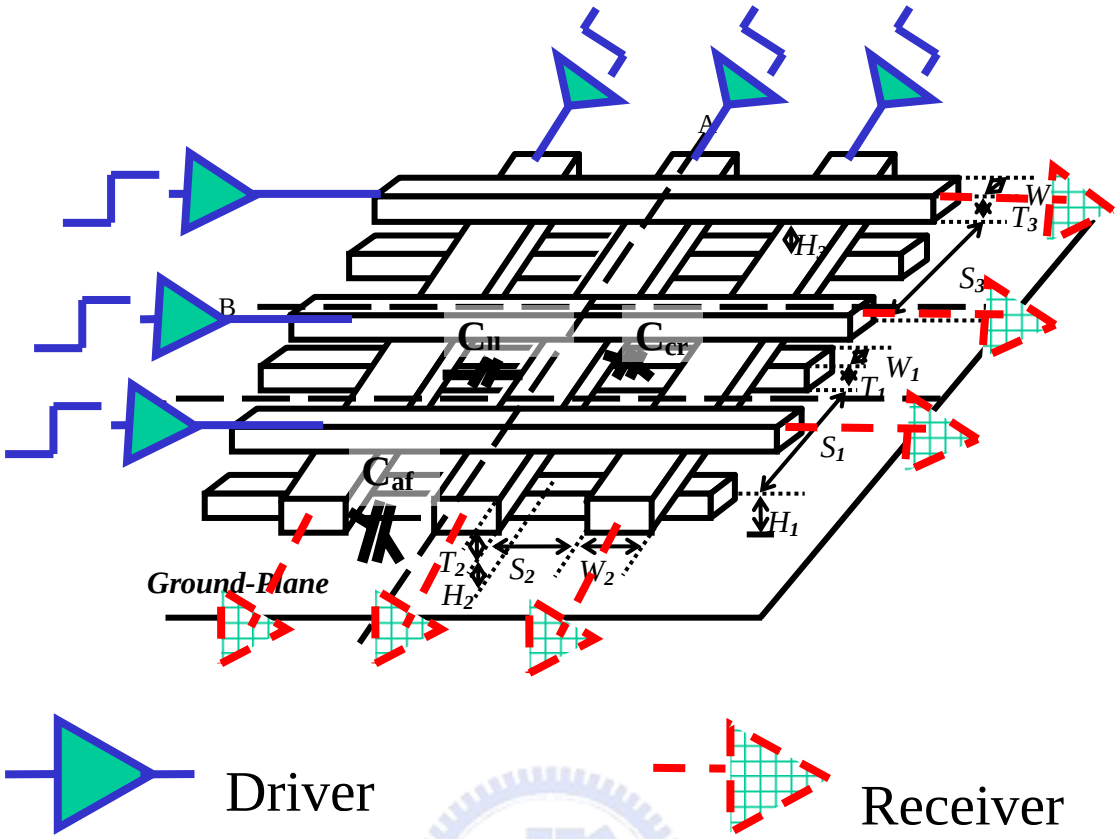


Figure 2. 1 General interconnect structure plot with driver and receiver.

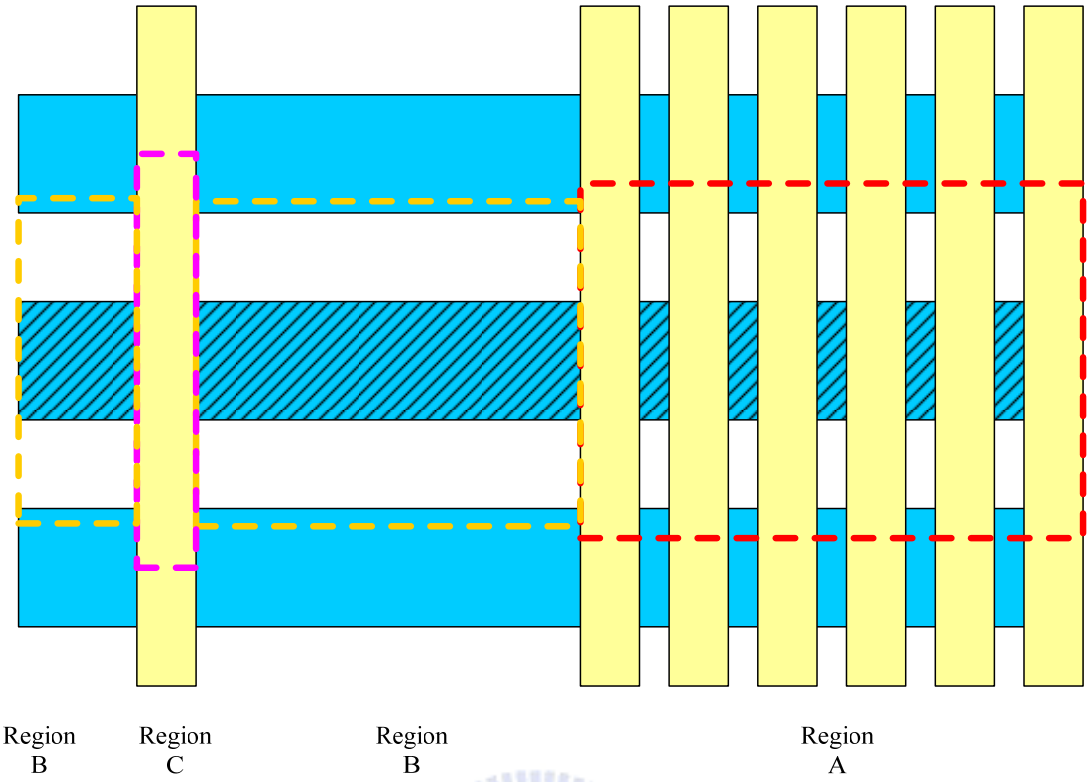


Figure 2. 2 Interconnect could be categorized into three structures (Region A, B and C). Region A represents interconnect surrounded by metal line at the same layers (intra-layer) and with many dense coupled wire of different layer (inter-layer) inter-wires run across it. Region B represents interconnect surrounded by intra-layer wires and *without* inter-layer wire run over it. Region C represents interconnect surrounded by intra-layer metal line and with single wire (or a set of loosely coupled wires) run across it. The dash wire represents the wire need to calculate the capacitance. Decomposition of interconnect structure into a series of 3-D and 2-D segments. The total capacitance (C_{total}) of dash line $C_{total}=C_{Region\_B}+C_{Region\_C}+C_{Region\_B}+C_{Region\_A}$.

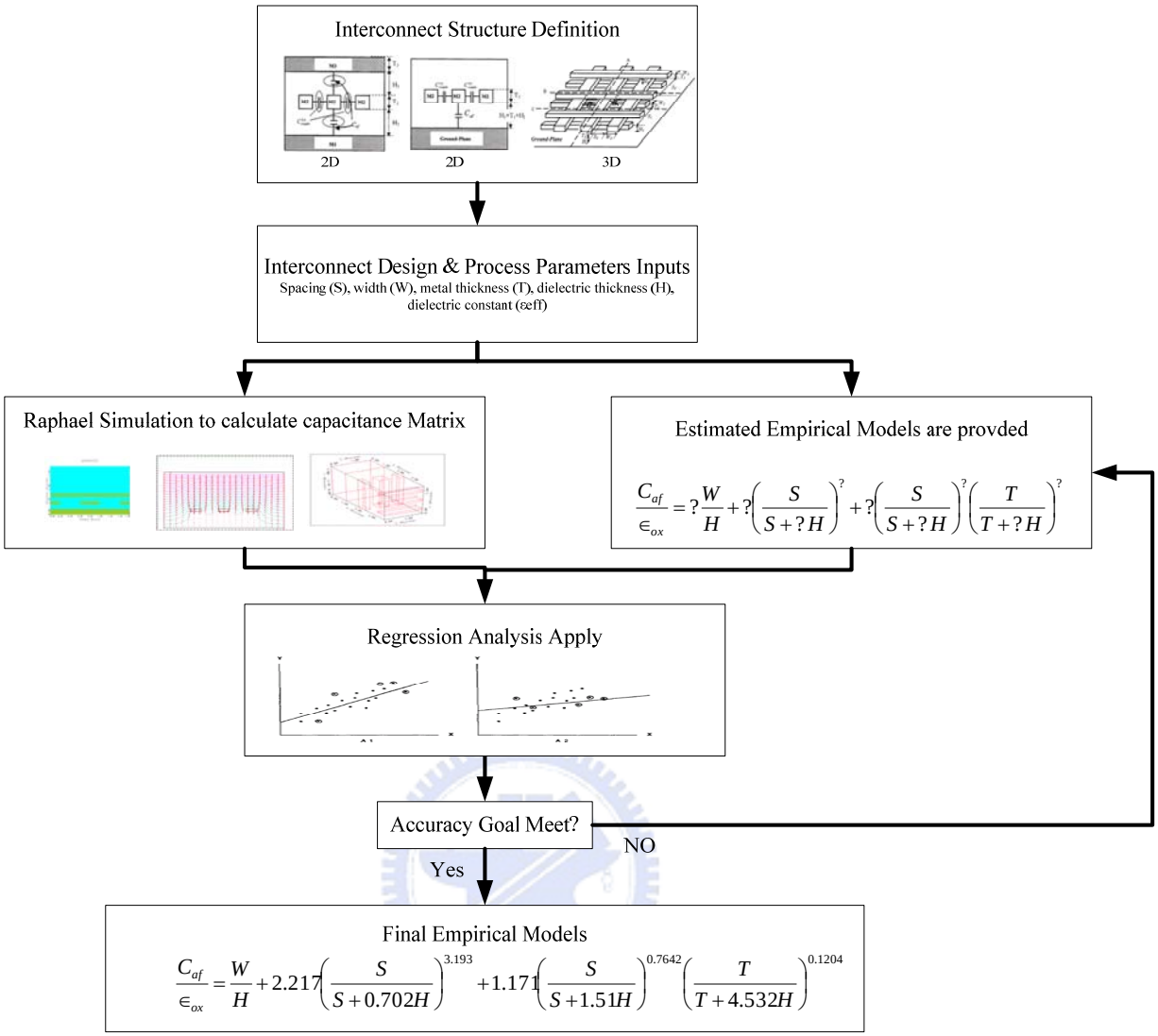


Figure 2. 3 Methodology for interconnect capacitance model development

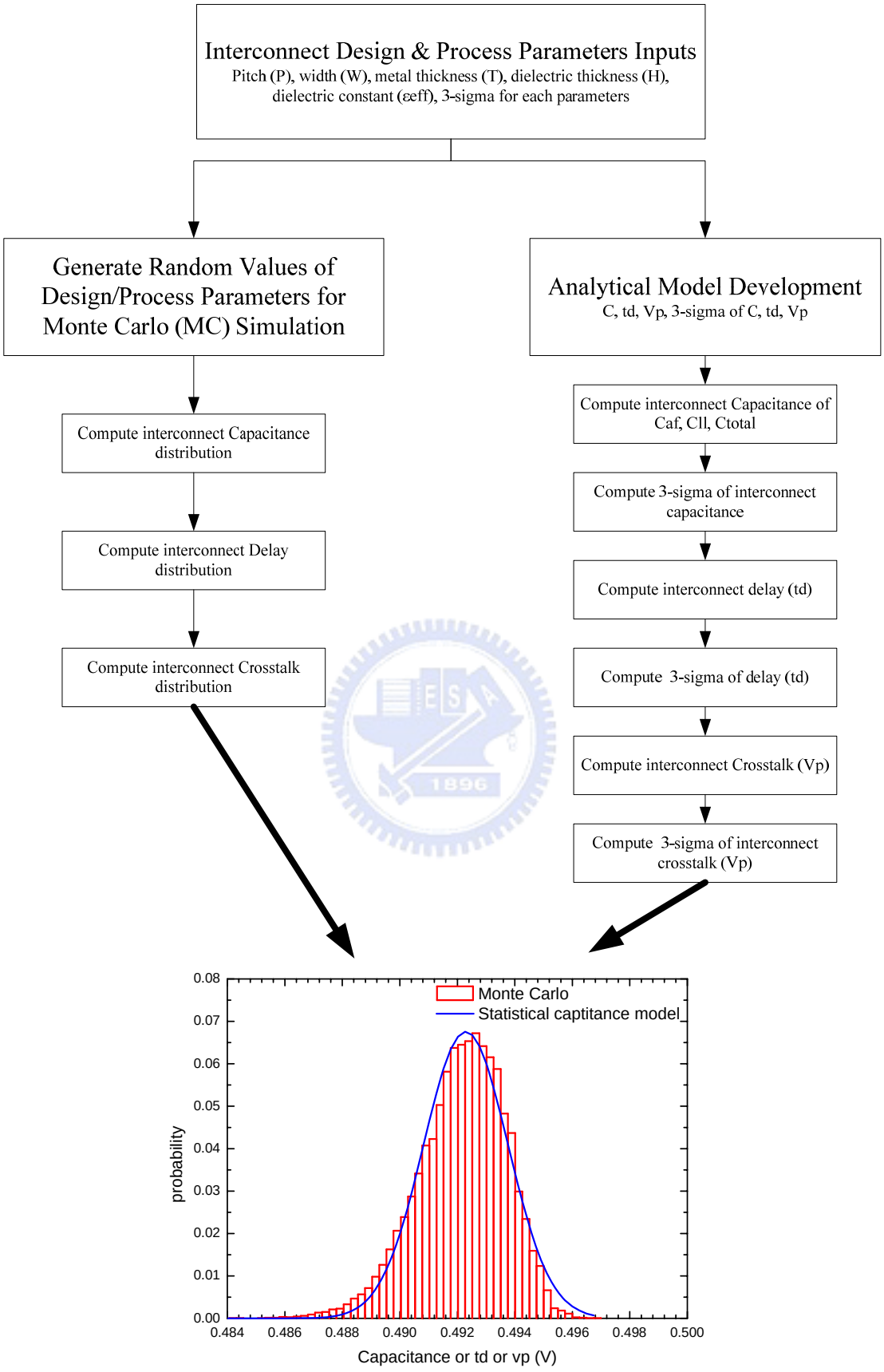


Figure 2. 4 Methodology for interconnect statistical analysis

Chapter 3 Interconnect Parasitic Component Modeling

3-1 Two-dimensional Interconnect Capacitance Model and Extraction

With the increasing complexity in VLSI circuits makes metal interconnection a significant factor affecting circuit performance. In this thesis, we first develop new closed-form capacitance formulas for two major structures in very large scale integration (VLSI), namely , 1) parallel lines in a plane and 2) wires between two planes, by considering the electrical flux to adjacent wires and to ground separately . We then further derive closed-form solutions for the delay and crosstalk noise. The capacitance models agree well with numerical solutions of three-dimensional (3-D) Poisson's equation as well as measurement data. The delay and crosstalk models agree well with SPICE simulations.

In modern very large scale integration (VLSI) technology, efforts have been devoted to reduce metal wiring pitch to increase chip density and to save silicon budget [3.3]-[3.5]. This makes metal wiring line resistance and line-to-line capacitance, thus the resistance-capacitance delay (RC delay) and interline crosstalk noise, increase. The huge amount of interconnection line in VLSI makes the interconnect delay and crosstalk noise more dominant factors in the overall circuit speed [3.6]-[3.8].

Many works have been devoted to calculating line capacitance, e.g., [3.2]-[3.4]. Sakurai and Tamaru [3.2] derived formulas, both for parallel lines on a large plane. Choudhury et al. [3.3] gave models for several layout primitives but only for one set of technology parameters. Chern et al. [3.4] gave a general capacitance formula for three-dimensional crossing lines assuming same dielectric and wire thickness for all layers. In delay and crosstalk modeling, Sakurai [3.5] gave equations of distributed RC line, but solutions were not obtained in closed-form.

In this thesis, we give a new model of metal interconnection, where closed-form formulas are derived for the wiring capacitance, delay and crosstalk noise, all as explicit functions of the wire thickness, dielectric thickness, inter-wire spacing and wire width. New capacitance formulas are

first developed for two major structures in VLSI: 1) parallel lines on a plane and 2) wires between two planes; combinations of them can cover any given layout. The developed capacitance formulas then in turn lead to closed-form formulas for the delay, crosstalk noise, optimization design and statistic analysis: Chapter 3 derive the capacitance model, Chapter 4 gives the delay and crosstalk models, Chapter 5 gives the optimization of interconnect and Chapter 6 provide the statistic analysis of interconnect.

We define two capacitance structures: 1) parallel lines on one plate as shown in Fig. 3.1(a), and 2) parallel lines between two plates as shown in Fig. 3.1(b). The first structure emulates lines without top wiring, and the second structure emulates lines with top wiring. In VLSI, that a line in a given layer is not (is) underneath a line can be covered by the first (second) structure. Developing formulas for the two fundamental structures is useful for simulating arbitrary integrated circuit layouts.

The interconnect capacitance is decomposed into two capacitance components; 1) C_{ll} is the flux to adjacent wire which affects both wiring delay and crosstalk noise and 2) C_{af} is the area and fringe flux to the underlying plane which determines wiring delay only.

Physical approach requires analytical solution of Poission`s equation, which often results in lengthy and complicated equations, often nonsolvable. Thus, we adopt a semi-empirical approach here [3.2]-[3.5]. We use rations functions to give simple and explicit observations of field line variations with geometry parameters. The derived formulas model the field flux from different portions of an electrode separately, so that unique dimensional dependence of each electrical flux can be taken care of independently.

A. Parallel Line on a Ground Plane

As shown in Fig. 3.1(a), wire thickness is denoted by T, dielectric thickness by H, inter-wire spacing by S and wire width by W. The range of dimension is chosen as $0.15 < T < 1.2$, $0.16 < H < 2.71$, $0.16 < S < 10$, and $0.16 < W < 2$, all in unit of micrometers. The ranges of these parameters are selected based in applications in deep submicron VLSI. Although our models [(1)-(4) below] are tested and verified only over these selected ranges, they should prove to hold for parameters outside the above ranges. It is simply because the

solutions to Poisson's equation are majorly affected by the relative values of the dimensional parameters, not their individual ones. This is exactly the rationale behind the derivation of our models in what follows.

First, C_{ll} is modeled as the summation of three rational functions which simulate three flux components, and is obtained explicitly via the least-square fitting as

$$\frac{C_{ll}}{\in_{ox}} = 1.144\frac{T}{S}\left(\frac{H}{H+2.059S}\right)^{0.0944} + 0.7428\left(\frac{W}{W+1.592S}\right)^{1.144} + 1.158\left(\frac{W}{W+1.874S}\right)^{0.1612}\left(\frac{H}{H+0.9801S}\right)^{1.179}, \tag{3. 1}$$

where $\in_{ox} = 3.9\times 8.85\times 10^{-14}$ F/cm and it could change to $\in_{eff}$ easily by considering multi-layer effective dielectric in modern VLSI technology. The first term on the right-hand side of (3.1) models side-wall flux, which linearly proportional to *T* and decrease as *H*/*S* decrease (i.e., as ground flux increases), because more flux originated form side wall now gets attracted to ground. The second term gives the upper-surface flux contribution, which increases as W increases or as S decrease, and which is independent of the ground flux. The third term models the lower surface flux, which is heavily inversely proportional to the ground flux. The power-law dependence in these functions has been a good approximation to the field strength between adjacent non-overlapping perpendicular surfaces [3.2] and [3.5].

C_{af} is similarly modeled as the summation of three rational functions to simulate three flux components, and is obtained explicitly via the least-square fitting as

$$\frac{C_{af}}{\in_{ox}} = \frac{W}{H} + 2.217\left(\frac{S}{S+0.702H}\right)^{3.193} + 1.171\left(\frac{S}{S+1.51H}\right)^{0.7642}\left(\frac{T}{T+4.532H}\right)^{0.1204}. \tag{3. 2}$$

The total capacitance of the wire M_b is $C_{total} = C_{af} + 2C_{ll}$. The first term

in the right-hand side of (3.2) models bottom plate-to-ground flux, which is simply the plate-to-plate capacitance. The second term and the third term model the upper surface and side-wall flux contributions, respectively; in the both terms, that the flux reduces with reduced S is because more coupling flux is attracted to the adjacent electrode M_a and M_b.

B. Parallel Lines Between Two Planes

As shown in Fig. 3.1(b), the thickness of top dielectric layer and bottom dielectric layer are denoted by H_1 and H_2, respectively. The range of dimension is as in the previous case, expect that 0.16 < H_1 < 2.71 and 0.16 < H_2 < 2.71 . By similar rational function approach and similar reasoning as before, C_{ll} is modeled to simulate the side-wall flux and upper lower planes flux. C_{af} is modeled to simulate the upper and lower surface flux and the side-wall flux. Again, using least-square fitting, we have

$$\frac{C_{ll}}{\in_{os}} = 1.4116\frac{T}{S}\exp\left(-\frac{2S}{S+8.014H_1}-\frac{2S}{S+8.014H_2}\right)+1.1852\left(\frac{W}{W+0.3078S}\right)^{0.25724}$$

$$\times\left\{\left(\frac{H_1}{H_1+8.961S}\right)^{0.7571}+\left(\frac{H_2}{H_2+8.961S}\right)^{0.7571}\right\}\exp\left(-\frac{2S}{S+3(H_1+H_2)}\right) \tag{3.3}$$

and

$$\frac{C_{af}}{\in_{os}} = \left(\frac{W}{H_1}+\frac{W}{H_2}\right)+2.04\left(\frac{T}{T+4.5311H_1}\right)^{0.071}\left(\frac{S}{S+0.5355H_1}\right)^{1.773}$$

$$+2.04\left(\frac{T}{T+4.5311H_2}\right)^{0.071}\left(\frac{S}{S+0.5355H_2}\right)^{1.773}. \tag{3.4}$$

Again, $C_{total} = C_{af} + 2C_{ll}$.

C. Model Validation

The accuracy of our capacitance model is verified by numerical solutions from Raphael [3.1] and measured data. We also include results from Sakurai`s

analytic model [3.2], [3.5] for comparison, Fig 3.2(a) gives the comparison results for wires on one plane. The accuracy of C_{ll}, C_{af} and the interaction between them are observed, and improvement of our model over Sakurai's model [3.2], [3.5] is demonstrated. The comparison of our model for wires between two planes with Raphael is shown in Fig. 3.2(b). The detail error table for Fig, 3.2(a) and (b) are given as Table 3.2 and Table 3.3 respectively, which only displays a partial set of our data used for parameter fitting. Note that in Fig, 3.2(b). C_{ll}^{1p} denotes the coupling capacitance obtained from Sakurai's model [3.2], and C_{total}^{1p} is the value by adding up the capacitances to top plate and to bottom-plate calculated using Sakurai's model [3.2]. The root-mean-square error (rmse) for C_{af} (C_{ll}) is 3.68% (4.45%) and 1.05% (16.13%) for one- and two-plane cases, respectively. The number of data points used in calculating the root mean square error is 627.

Our model is further compared with measured data, and the results are shown in Table 3.1. Five dies have been measured per wafer for six wafers, and the typical die around the distribution mean was used for comparison. Test structures were fabricated in two technologies: 1) a 0.5-μm twin-well CMOS with SOG plannarized three-level metals and 2) a 0.35-μm twin-well CMOS with chemical mechanical polished (CMP) three-level metals. All dielectric thicknesses used in model calculation are measured from large-plane capacitors on the same die as measured structures for accurate reflection of dielectric constant and dielectric thickness *H*. This thickness *H* is used for calculating all capacitance structures. The large-plane capacitors have been placed close to other capacitance structures in test key to eliminate intra-die dielectric thickness variations. Wire width W, inter-wire spacing S, and wire thickness T are determined from SEM bars of small inter-wire spacing on the same wager. The small spacing between SEM bars guarantees that horizontal dimension in dense array is adopted for capacitance calculation. All measurements are executed using a HP4284 impedance meter at 100 kHz, with all parasitic effects canceled using an open-pad calibration structure. Good agreement is observed, and this further demonstrates the accuracy of our capacitance model.

Accurate closed-form models have been developed for wire capacitance.

The capacitance model gives line-to-line and line-to-ground capacitances separately, and lead to precise delay and crosstalk estimations provided in next chapter. These formulas allow for simple analytic prediction of capacitance for arbitrary interconnect dimensions. Our model is useful for VLSI design and process optimization.

3-2 Three-Dimensional Interconnect Capacitance Models and Extraction

We develop an empirical model for the crossover capacitance induced by the wire crossings in VLSI with multilevel metal interconnects. The crossover capacitance, which is formed in any three adjacent layers and of a three-dimensional (3-D) nature, is derived in closed form as a function of the wire geometry parameters. The total capacitance on a wire passing many crossings can then be easily determined by combining the crossover capacitance with the two-dimensional (2-D) intralayer coupling capacitance de-fined on a same layer. The model agrees well with the numerical field solver (with a 6.7% root-mean-square error) and measurement data (with a maximum error of 4.17%) for wire width and spacing down to 0.16m and wire thickness down to 0.15m. The model is useful for VLSI design and process optimization.

Deep submicrometer integrated circuit performance is influenced by interconnect RC delay [3.9]–[3.11]. Although the device delay decreases as the technology scales down, the inter-connect-induced delay, however, increases, because both line resistance and intralayer capacitance increase [3.9], [3.10], [3.12]. In VLSI circuits with multilevel interconnects, lines in adjacent metal layers are placed orthogonally to each other to minimize over-lapped capacitances and enhance routing flexibility. This procedure forms many wire crossings, inducing crossover capacitance, which becomes the major factor in affecting the circuit speed [3.10], [3.13]. An accurate model for the crossover capacitance is essential for estimating the interconnect circuit performance. Many previous works on interconnects exist in the literature. The works of [3.11], and [3.13]–[3.15] either considered two-dimensional (2-D) structures or approximated the three–dimensional (3-D) wirings by 2-D cross sections; both approaches cannot model 3-D fringe field. The models of [3.13]–[3.15] were based on numerical solutions, thus not allowing for closed-form estimation. The work of Chern [3.10] gave a crossover model for triple-level metal layers but with same thickness in all layers. The work of Pan et al. [3.16] derived an

analytical expression for crossover capacitance specifically for packaging geometries. The work of Kuhn et al. [3.17] gave an optimization study for delay time and power dissipation using combined device and interconnect capacitances; it, however, ignored both intralayer coupling and crossover capacitances that are important in deep submicron VLSI. The work of Vladimir and Mittra [3.18] gave improved boundary conditions for numerical solution of interconnect and packaging capacitances. Some other works focused on novel measurement methods for extracting interconnect capacitance on various layout structures. For instance, the work of Wee et al. [3.19] developed a complete set of structures for characterizing multilevel metal capacitances for both stack and crossing configurations; the impact of metal-edge slope and void was also extracted. The work of Nouet and Toulouse [3.20] characterized interlayer and intralayer capacitance novel test patterns, and compared on-chip and off-chip measurement. In [3.20], it was identified that the 3-D crossings (crossover) is a critical component in the total wiring capacitance, and a linear model with different components was then proposed with linear dependence on area, periphery length, and spacing. The work of Aoyama et al. [3.21] characterized coupling and ground capacitance using test patterns and numerical solutions, and it provided an optimization study by wire pitch to dielectric thickness ratio. The work of Chao et al. [3.22] presented a novel extraction method-ology and test pattern, with verifications on SOG and CMP processes. The work of Chen et al. [3.23] gave a novel on-chip measurement method for small wire capacitance. In [3.24], we developed models for 2-D wiring capacitance, wire delay, and inter-wire cross-talk noise. The capacitance model of in previous section gives accurate intralayer and line-to-ground capacitance estimation for both parallel lines on a plane and lines between two planes, with agreement with measurement data.

In this thesis, we continue our work in previous section by focusing on the modeling of crossover capacitance for VLSI's with multilevel metal interconnect of arbitrary dielectric and wire thickness, width, and spacing in all layers. The crossover capacitance is formed in any three adjacent layers of the multilevel metal interconnects and is of a 3-D nature. We derive closed-form formula for the crossover capacitance as a function of the wire geometry parameters of three adjacent layers, including the wire width, spacing, thickness,

and dielectric thickness of a line and of lines in the upper and lower layers. The total net capacitance on a wire passing many crossings can then be easily obtained by combining the crossover capacitance with the 2-D intralayer coupling capacitance defined on a same layer obtained in previous section. The result of our model shows agreement with the numerical field solver [3.25] and measurement data. This work extends the work of 2-D modeling provide in previous section to provide a complete solution for the modeling of interconnect capacitance for arbitrary multilevel interconnects. The complete model can be used in the delay and capacitance estimation in circuit design and process optimization.

The crossover capacitance is formed in any three adjacent layers of the multilevel metal interconnect. Consider any triple-level wire crossings, as shown in Fig. 1, where the second-level metal lines (M_2) cross the first-level (M_1, the lower level) and third-level (M_3, the upper level) metal lines. The line width, pacing, and thickness are denoted by, W_i, S_i and T_i for the *i*th-level metal layer, $i = 1,2,3$. The dielectric layer thickness is denoted by H_1, H_2, and H_3 for the dielectric between M_1 and the substrate (or the next lower layer, say, M_0), and M_2, M_1 and M_3 and M_2, respectively. For each M_2 line crossing M_1 line, a crossover capacitance C_{cr} exists. Note that M_1 and M_3 lines are not necessarily aligned to each other. This capacitance C_{cr} is restricted within a neighborhood of the lines intersection. Outside the intersection neighborhood, M_2 line capacitance can be estimated by existing 2-D intralayer coupling capacitance models discussed in previous section.

To derive the crossover model for C_{cr} we adopt an empirical approach here, because the usual power series or numerical solutions for Poisson's equation are not appropriate for VLSI simulation [3.25], [3.26]. In deriving these expressions, a rational function is first constructed to model each type of electrical flux variations with geometry variation. The rational functions are then multiplied to each other to form one flux component. Finally, all flux components are added, giving the lumped crossover capacitance C_{cr}. Here, three flux components, C_1, C_2, and, are involved. That is

$$C_{cr} = C_1 + C_2 + C_3 . \tag{3.5}$$

Capacitance C_1 represents the area component from M_1 top surface to M_2 bottom surface. Capacitance C_2 represents the component from M_1 side wall to M_2 bottom surface. Capacitance C_3 represents the component from the M_2 side wall to M_1 top surface. To derive C_1, note that C_1 is simply the plate-to-plate capacitance, and hence

$$\frac{C_1}{\in_{OX}} = \frac{W_1 W_2}{H_2} \quad , \tag{3.6}$$

where $\in_{ox} = 3.9 \times 8.85 \times 10^{-14}$ F/cm and it could change to $\in_{eff}$ easily by considering multi-layer effective dielectric in modern VLSI technology.

The flux component C_2 is modeled as the product of rational functions in the following general form:

$$\frac{C_2}{\in_{OX}} = c_1 W_2^{\alpha 1} (S_1 \times S_2)^{\alpha 2} \left(\frac{T_1}{T_1 + c_2 H_2} \right)^{\alpha 3} \left(\frac{T_1}{T_1 + c_3 S_1} \right)^{\alpha 4} \times \left(\frac{H_1}{H_1 + c_4 S_1} \right)^{\alpha 5} \exp \left(\frac{- H_2}{c_3 (S_1 + c_6 H_2)} \right) , \tag{3.7}$$

where the c_i's are constants and the α_i's are the power coefficient, both to be determined later.

We now explain the physical rationale behind each term adopted on the right-hand side of (3) for C_2 : 1) the W_2 term follows from a power-law dependence of the capacitance on the line width [3.10], [3.11], [3.26]; 2) the S_1 and S_2 terms are to catch the intrawire spacing dependence: Because the M_1 side wall to M_2 wire flux is reduced by intra-M_1 flux as shown in the cross-section A of Fig. 3.3, C_2 decreases with reduced intra-M_1 spacing S_1; similar impact can be induced by intra-M_2 spacing S_2. Here, the same power

coefficient α_2 is used to reflect their same influence; 3) the term $(T_1/(T_1+c_2H_2))^{\alpha 3}$ is adopted to model the fact that the flux originated from side wall heavily relies on the wire side wall thickness with a power-law dependence [3.11]. The power-law dependence has been proved in [3.26] as a good approximation to the field strength between adjacent non-overlapping perpendicular surfaces. Note that this dependence will be weakened for large thickness (because such flux only exists at the side wall corner adjacent to the dielectric layer); the constant reflects this dependence weakening; 4) the terms $(T_1/(T_1+c_3S_1))^{\alpha 4}$ and $(H_1/(H_1+c_4S_1))^{\alpha 3}$ are used to model the fact that C_2 decreases with reduced T_1/S_1 as well as with reduced H_1/S_1 because of enhanced flux from M_1 to ground plane, as shown in the cross-section A of Fig. 3.3; and 5) the exponential term modifies the $1/H_2$ dependence constructed in (2), giving weakened H_2 impact with increased H_2/S_1, because intra-M_1 flux prevents field lines from being pulled up to M_2, electrode, as shown in the cross-section A of Fig. 3.1.

To derive C_3, we observe that C_3 is approximately a 180^0 turnover of C_2. Therefore, similar mathematical patterns will be adopted to emulate the similar electrical flux distributions. Differences in C_2 and C_3 exist, however: C_2 has a larger plate next to (or under) the side wall flux, whereas C_3 has many narrower wirings (M_3 wires) next to (or above) the side wall component. The consequence is that the side wall flux reduction induced by larger adjacent plane in C_2 and by adjacent wirings in C_3 will be different. C_3 is modeled in the following general form:

$$\frac{C_3}{\in_{OX}} = d_1 W_1^{\beta_1} S_1^{\beta_2} S_2^{\beta_3} \left(\frac{T_2}{T_2 + d_2 H_2}\right)^{\beta_4} \exp\left(\frac{-H_2}{d_3(S_2 + d_4 H_4)}\right) \times \left(\frac{H_3}{H_3 + d_5 S_2}\right), \tag{3.8}$$

where the d_i's are constants and the β_i's are the power coefficients, both again to be determined later.

Now, similar physical explanation, as is the case with C_2 ,can be made for each term on the right-hand side of (4) for C_3: 1) the W_1 term shows the power-law dependence as be-fore; 2) the power terms of S_1 and S_2 again catch the intra-wire spacing dependence, but here we use different power coefficients for them because their influence will be different. In fact, the influence of S_2 term in C_3 is weaker than in C_2, for the impact in C_3 is weakened by the M_3-to-M_2 flux; 3) the term $\left(T_2/\left(T_2+d_2H_2\right)\right)^{\beta_4}$ models the fact that C_3 increases with increased T_2/H_2; 4) the exponential term further modifies the $1/H_2$ dependence constructed in (2), giving weakened H_2 impact with increased H_2/S_2, because intralayer flux prevents field lines from being pulled down to M_1 electrode; and 5) the last term $\left(H_3/\left(H_3+d_5S_2\right)\right)^{\beta_5}$ models the impact of M_3 layer on C_3, which gives reduced C_3 with reduced H_3/S_2, because the intralayer coupling flux between M_2 lines forms a shield that isolates the C_3 flux from the influence of the M_3-to-M_2 flux. This shielding effect is very strong when S_2 is small, as shown.in the cross-section B of Fig. 3.3. This shielding effect is reduced with large S_2, and hence, C_3 can be significantly reduced with reduced H_3. Note that this effect is opposed to the phenomenon that C_3 increases with increased S_2, as predicted by the power terms of $\left(S_1\right)^{\beta_2}$ and $\left(S_2\right)^{\beta_3}$. This term and the power-law term provide contradictory influences by S_2 spacing, and our model can well describe these two opposing phenomena, which will later be demonstrated in Fig. 3.5.

To determine all constants and power coefficients in (3) and (4) for C_2 and C_3, we use the approach of least-mean-squares-errors fitting, and we obtain

$$\frac{C_2}{c_{ox}} = 3.73 W_2^{0.6} \left(S_1 \times S_2\right)^{0.2} \times \left(\frac{T_1}{T_1 + 0.035 H_2}\right)^{0.64}$$
$$\times \left(\frac{T_1}{T_1 + 0.851 S_1}\right) 0.12 \times \left(\frac{H_1}{H_1 + 0.051 S_1}\right)^{1.0}$$
$$\times \exp\left(\frac{-H_2}{0.7\left(S_1 + 0.4 H_2\right)}\right)$$

(3. 9)

and

$$\frac{C_3}{c_{ox}} = 3.73 W_1^{0.6} S_1^{0.2} S_2^{0.1} \left(\frac{T_2}{T_2 + 0.035 H_2}\right) 0.64$$
$$\times \exp\left(\frac{-H}{0.7\left(S_2 + 0.4 H_2\right)}\right) \times \left(\frac{H_3}{H_3 + 0.015 S_2}\right)^3 .$$

(3. 10)

The root-mean-square error between the model and the numerical solutions is 6.71%, based on a total of 272 data points using the least-squares-error fitting approach. The 272 total data points were basically selected randomly, but with more dense data points chosen toward smaller dimension range (as the capacitance effect is more pronounced at smaller dimension range). A list of error distribution is shown is Table 3.4, which only displays a partial set of our data used for parameter fitting.

The segments of M_2 outside the intersection neighborhood can be modeled by the 2-D capacitance formulas derived in previously section. The capacitance components here include 1) intralayer coupling capacitance C_{couple}^{1p}, which is the intra-M_2 flux in the wire region without M_3 wirings crossing above, as shown in the cut-line C and cross section C of Fig. 3.3, 2) C_{couple}^{2p}, which is the intra-M_2 flux in the M_2 region with M_3 wirings crossing above, as shown in the cut-line B and cross-sec-tion B of Fig. 3.3, and 3) line-to-ground capacitance C_{af} in the region without M_3 wirings crossing above, as shown in the cross section C of Fig. 3.3. These capacitances were obtained in previous section as

$$\frac{C_{af}}{c_{ox}} = \frac{W_2}{H} + 2.217\left(\frac{S_2}{S_2 + 0.702H}\right)^{3..913} + 1.171\left(\frac{S_2}{S_2 + 1.51H}\right)^{0.764} \times \left(\frac{T_2}{T_2 + 4.532H}\right)^{0.12},$$

(3. 11)

$$\frac{C_{ll}^{1p}}{\in_{ox}} = 1.144\frac{T_2}{S_2}\left(\frac{H}{H + 2.059S_2}\right)^{0.0944} + 0.7428\left(\frac{W_2}{W_2 + 1.592S_2}\right)^{1.144} + 1.158\left(\frac{W_2}{W_2 + 1.874S_2}\right)^{0.1612}\left(\frac{H}{H + 0.9801S_2}\right)^{1.179}$$

(3. 12)

and

$$\frac{C_{ll}^{2p}}{c_{ox}} = 1.412\frac{T_2}{S_2}\exp\left(-\frac{2S_2}{S_2 + 8.014H_2} - \frac{2S_2}{S_2 + 8.014H_3}\right) + 1.1852\left(\frac{W_2}{W_2 + 0.3078S_2}\right)^{0.25724} \times \left\{\left(\frac{H_2}{H_2 + 8.961S_2}\right)^{0.7371} + \left(\frac{H_3}{H_3 + 8.961S_2}\right)^{0.7371}\right\} \times \exp\left(-\frac{2S_2}{S_2 + 3(H_2 + H_3)}\right).$$

(3. 13)

where $H = H_1 + H_2 + T_1$. In previous section, the above 2-D capacitance model provides accurate capacitance prediction, with a root-mean-quare error of 3.68, 4.45, and 16.13% for C_{af}, C_{ll}^{1p}, and C_{ll}^{2p}., respectively, compared with the numerical solutions.

The total capacitance on a M_2 line of length L with $nM_1 - M_2$ crossings and another $nM_2 - M_3$ crossings can be calculated by combining the total intralayer coupling capacitance and the total crossover capacitance. The total intralayer coupling capacitance is easily determined as

$$(L - nW_1)C_{ll}^{1p} + nW_1C_{ll}^{2p} + (L - nW_1)C_{af}.$$

The total crossover capacitance is calculated according to the following: 1)

each crossing of M_1 and M_2 gives a crossover capacitance $C_{cr(M_2-M_3)}$. To compute $C_{cr(M_2-M_3)}$, we need to view the triple-layer upside down before applying the above-developed formulas. That is, M_3 is now treated as the lower layer and M_1 the upper layer, which means that H_3 should be used as H_2 and H_2 should be used as H_3 in the formulas. H_1 to be used in the formulas should be the spacing between M_3 and the next adjacent higher layer (say, M_4 if exists). If M_3 is the actual top layer, we have $H_1 = \infty$. Here, in such a case, we use the value $H_1 = 5\mu m$ as infinity.

Combining the crossover and intralayer coupling capacitances, we have

$$C_{total} = n[C_{cr(M_1-M_2)} + C_{cr(M_2-M_3)}] + (L - nW_1)C_{ll}^{1p} + nW_1C_{ll}^{2p} + (L - nW_1)C_{af} \quad . \tag{3. 14}$$

Our model, which is derived based on three-metal layers, can be applied to a process with any number of metal layers. The crossover capacitance of a metal wire with the layer underneath it can be accurately predicted by our model, with or without above-passing wires. In the general multilayer case, any layer above the first layer or under the third layer is shielded from the second layer and, hence, does not affect the crossover capacitance.

The agreement between our model and the numerical field solver [3.25] is shown in Table 3.4. In Table 3.4, the error is defined as Error = (model-Raphael/Raphael)$\times 100\%$. The final model has been tested based on 272 data points with a root-mean-square error of 6.71%. The valid ranges of the model are the following: $0.16\mu m \le S_1, S_2, S_3 \le 5\mu m$, $0.16\mu m \le W_1, W_2, W_3 \le 2\mu m$, $0.15\mu m \le T_1, T_2, T_3 \le 1.2\mu m$, $0.16\mu m \le H_1, H_2, H_3 \le 3\mu m$. The valid ranges for our model were determined based on practical applications in integrated circuit (IC) technology. The upper bound for parameter S set at $5\mu m$ is to take care of both dense and sparse lines. The upper bounds for and were set to match the practical dieletric and metallization thicknesses.

The comparison between the model and the numerical simulations [3.25] for various H_1 and H_2 is shown in Fig. 3.4. The strong H_2 dependence can be accurately predicted by our model. On the other hand, only influences C_{cr} minorly, simply because the flux of C_{cr} is shielded from the line-to-ground flux by the intra-M_1 flux, as shown in the cross-section A in Fig. 3.3. The intra-M_1 flux plays the role of electrical buffer between C_{cr} and line-to-ground flux, and this buffer is weakened for small (here, $H_1 \le 0.5\mu m$), as shown in Fig. 3.4. Our model is useful here for predicting strong H_2 dependence, weak H_1 dependence induced by intra-M_1 flux shielding effect, and the onset of weakened shielding effect when C_{cr} reduces with reduced H_1.

The comparisons of the crossover capacitance C_{cr} and total M_2 wiring capacitance C_{total} between our model and the numerical solutions for various intralayer spacing are shown in Fig. 3.5. Note that C_{cr} decreases with reduced S_1 and S_2 because of enhanced intra-M_1 and intra-M_2 coupling effects, respectively. At small S_1 (or S_2), the C_{cr} variation versus S_1 is symmetrical to that of versus. At large S_1 or S_2, it should be noted that C_{cr} variations with S_1 and S_2 are different, and this difference depends on the magnitude of H_3. To investigate this in more detail, note that for the curves with $H_3 = 3\mu m$, C_{cr} increases strongly with increased S_2 than with increased S_1, which can be explained as follows: because large H_3 (at $3\mu m$) is adopted in these data, increased S_2 eliminates the intra-M_2 flux and enhances the C_{cr} flux. On the other hand, with increased S_1, considerable line-to-ground flux (as shown in the cross-section A of Fig. 3.3), becomes influential because H_1 is only $0.6\mu m$ and will retard the C_{cr} flux. As a result, C_{cr} increases with increased S_2 much stronger than with increased S_1.

Another point worth studying is the following question. When can the impact of top-level metal in any three-level metal combination be ignored for C_{cr} between the first and second level metals? Being able to identify a no-influence region here would allow for an easy C_{cr} estimation without

considering parameters of the top-level wire, which will greatly simplify RC extraction [3.13] and process design [3.9], [3.12]. To investigate this process, first it can be observed that the impact of H_3 is negligible for small, because $H_3 = 0.3\mu m$, and $H_3 = 3\mu m$ gives the same C_{cr} for $S_2 \le 0.5\mu m$, because the strong intra-flux completely shields the M_3 -to- M_2 flux from influencing C_{cr} . The impact of H_3 is much more pronounced when is larger than $0.8\mu m$, because C_{cr} can be significantly retarded by the M_3 -to- M_2 flux, as shown in the cross-section B of Fig. 3.3, especially when the intra- M_2 coupling disappears. Hence, C_{cr} at $H_3 = 3\mu m$ is much larger than at $H_3 = 0.3\mu m$ Furthermore, as mentioned before, for $H_3 = 0.3\mu m$, C_{cr} saturates with reduced H_3 / S_2 (or increased S_2) for $S_2 \ge 4\mu m$, as predicted by the term $(H_3 /(H_3 + d_5 S_2))^{\beta_5}$ in (3.8). These observations on C_{cr} give us a region where C_{cr} is influenced by the third-level metal, and this region is defined by $S_2 \ge 0.3\mu m$ and $H_3 \le 0.3\mu m$. Outside this region, C_{cr} immunizes from the impact of M_3 , and thus C_{cr} estimation can be performed with the top-level wiring effect ignored.

The calculated C_{total} is the total M_2 capacitance in a cell with ten lines for M_1, M_2 , and M_3 each. It is shown that C_{total} slightly increases with increased S_1 , because of increased C_{cr} .On the other hand, C_{total} significantly decreases with increased S_2 , because of decreased C_{ll}^{2p} between M_2 lines. The larger error of C_{total} for $S_1 \ge 0.5\mu m$ is induced by the approximation of the last term in (10), i.e., $(L - nW_1)C_{af}$. The calculation of the 2-D capacitance using this term in the region outside the crossing neighborhood may overestimate the line-to-ground capacitance, because many metal-2 field lines near the crossing neighborhood will be attracted to the crossing metal-1 instead of being terminated to ground, as shown in cross-section A of Fig. 3.3. This process implies that the approximated length for C_{af} of $L - nW_1$ may cause slight overestimation. Note that because our model mainly tends to be used in deep submicron VLSI, the error for S_1 larger than $0.5\mu m$ may not affect the

calculation accuracy for densely packed VLSI.

The impact of the top layer wiring is shown in Fig. 3.6, where C_{cr} varies with S_3 and H_3. C_{cr} is noticeably reduced with reduced H_3 when intrawire spacing is $1\mu m$, agreeing with our observation from Fig. 3.5 made in the previous paragraph, as some M_2 flux is attracted to the M_3 electrode. The disagreement between the model and numerical solution at small H_3 is caused by the large variation generated by the last term in (3.10) as a result of its rational function form. The form is chosen for tradeoff at large H_3.

The comparison between our model and measurement data is performed based on test structures fabricated in a $0.35-\mu m$ twin-well logic CMOS process. The interconnection in this process is composed of AlCuSi metal lines, an oxide dielectric layer, and chemical–mechanical polished dielectric layers. Three test structures are included in this study, with each test structure composed of three layers of intracoupled wires. Each test structure has 726 crossovers. The C_{cr} between M_2 -to- M_3 or between M_2 -to- M_1 is then measured by grounding all additional wires to eliminate all intralayer and line-to-ground flux. Measurement has been performed on ten dies a wafer for four wafers, with the mean and standard deviation shown in Table 3.5. Agreement is shown between our model and measurement with a maximum error of 4.17%.

It should be noted that our model has been derived based on normalized dielectric constant, and is, hence, independent of the oxide dielectric constant. In comparing our model with measurement data, however, dielectric constant must be determined. The dielectric constant is determined by measuring large-plate capacitors using HP4284 impedance meter at 100 kHz, with an exciting signal of 100 mV. Based on the measured unit-area capacitance C_{ox}, $\in_{ox}$ is obtained by $\in_{ox}=t_{ox}C_{ox}$ In this work, we have obtained nearly the same $\in_{ox}=3.79$ for all dielectric layers. For cases with various dielectric layers having different values of dielectric constant, it is also possible to apply our model by taking their dielectric constant average as a common $\in_{ox}$ and used in the model equations, but this has not been tested yet.

From our analysis, it is easily seen that the crossover capaci-tance, because of its 3-D feature, can be influenced by numerous parameters, and the impacts of these parameters are strongly coupled with each other. Our model here can be very helpful in predicting the capacitance variation versus various electrical flux fluctuations, and in optimizing the total capacitance via appropriately adjusting physical dimensions.

A complete closed-form model for the 3-D crossover capacitance in multilevel, densely packed interconnections has been developed for arbitrary wiring dimensions. The combined use of the developed crossover capacitance model and existing intralayer coupling and lines-to-ground capacitance model can determine the total capacitance on a wire passing many crossings.

3-3 Interconnect Resistance Model

To calculate RC or RLC equivalent interconnect electrical performance, we need to calculate the value of resistance (R) also. For a uniform metal line of width W and thickness T, its dc resistance per unit length, R, can be calculated as

$$R = \frac{\rho}{WT} \quad , \tag{3. 15}$$

where ρ is the metal resistivity (ρ = 2.2 μΩ·cm for copper and 3.3 μΩ·cm for aluminum).

The shape of metal line may not exact the rectangular shape. For example, the shape of line formed by Cu damascene process is generally trapezoidal. This resistance could be easily calculated based from the information of trapezoidal area size.

3-4 Interconnect Inductance Model

Inductance (L) effects become significant in the nanometer regime, particularly for global interconnects in high-speed applications. In contrast to capacitance, in which only a line itself and its nearest neighbors should be included, inductance is a long range effect and, since magnetic fields decays very slowly with increasing distance. Hence the inductance should be

considered globally. The fundamental definition of inductance is

$$L = \frac{\Phi}{I} = \frac{\oint_A Bds}{I} \quad , \tag{3. 16}$$

where Φ is the magnetic flux in webers, I is the current in amperes, B the magnetic field induced from I, and s represent the current flow loop area. This definition indicates that the determination of inductive behavior must consider the entire current loop. However, in modern interconnect structures [driver-line-loading capacitance, there are no dc paths to form a well-defined loop. As a result, return current usually spreads over a long range, which complicates the analysis. Consequently, the extraction analysis should include all neighboring lines that are possibly involved in the current loop.

Because of the uncertainty of the return current path, it is difficult to calculate loop inductance in realistic designs. To overcome this difficulty, the concept of partial inductance is introduced, in which the induced current is assumed to return at infinity, avoiding the need to define the return loop. This inductance calculation technique, known as the partial element equivalent circuit (PEEC) method [3.27], is very suitable for design automation since it depends only on the geometry of the lines.

General speaking, inductance can be calculated using field solvers, such as FastHenry and Raphael, or closed-form solutions. Field solver extraction of inductance has high accuracy but it is time and memory expensive. For rectangular cross-sectional wires, the closed-form solutions are first derived by Rosa and Grover [3.28] and then simplified to the following relationships when $l >> W, T,$ and d [C]:

$$L_s = \frac{\mu_0}{2\pi}\left[l \ln\left(\frac{2l}{W+T}\right) + \frac{l}{2} + 0.2235(W+T)\right] , \tag{3. 17}$$

$$L_m = \frac{\mu_0}{2\pi}\left[l \ln\left(\frac{2l}{S}\right) - 1 + d \right] \quad . \tag{3. 18}$$

Here μ_0 is the magnetic permittivity of the dielectrics; W, T, and l are the width,

thickness, and length of the segment, respectively; S is the center-to-center distance between two lines; and L_m is the mutual inductance of two equal-length lines (a more general solution for Lm of non-equal-length lines is also provided in [3.29]). These expressions indicate that inductance has a nonlinear dependence on segment length. Therefore, in contrast to RC extraction, which is scalable with length, L must be calculated over the entire length of the wire. Furthermore, the logarithmic function in equation (3.17) and (3.18) implies that L has a weaker dependence on line geometry than do R and C. Note that only lines on the same layer, which are parallel to each other, contribute to inductive coupling; lines on neighboring layers do not influence the coupling, due to their orthogonal layout.

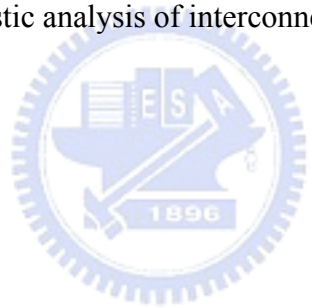
Although PEEC can deal with general inductance extractions without a priori knowledge of the current return loop, the nonsparsity of the inductance matrix (caused by the long-range inductive coupling) leads to expensive computations in further analyses [3.40]. Unlike the C matrix, in which it is sufficient to keep only the short-range coupling values, the L matrix cannot be truncated for simplicity.

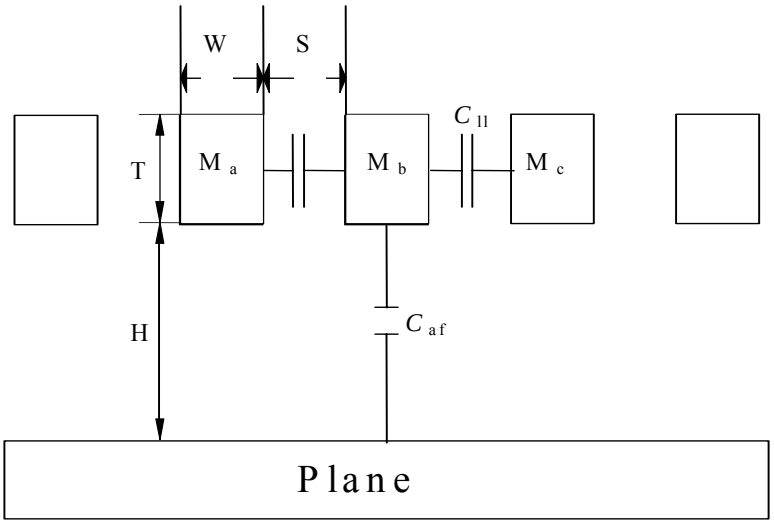
Inductance has been a concern for the design of off-chip interconnects such as those on system board design, package designs. However, inductance effects are more complicate for on-chip interconnect and could not use the knowledge of off-chip directly. 1) from inductance extraction point of view, ground planes are usually placed beside the signal (beside or upper/lower-layers, e.g., the stripe-line/micro-stripe-line structure) in the layout to reduce the inductance. Since the current paths are well defined, the inductance could be calculated easily use formulas derived in pre-defined structure. On the on other hand, current return paths of interconnects on-chip usually do not have well-defined because of the limited routing resources and smaller geometry (hence, magnetic flux has longer range affection). 2) Resistance effect are different between on-chip and off-chip interconnect. Off-chip interconnects have bigger cross sections compared to on-chip interconnects. Therefore, on-chip interconnects are much lossy than off-chip interconnects. The on-chip interconnect resistance shield the effects of inductance because the series connection natural ($R+jwL$). So, low-loss transmission-line theory can be applied in off-chip interconnect analysis where transmission-line behavior, such

as wave reflections are important and inductance effect to take into consideration. On the other hand, on-chip transmission lines usually suffer from high loss and therefore RC equivalent circuit is sufficiently to accurate to model the majority of on-chip interconnects performance.

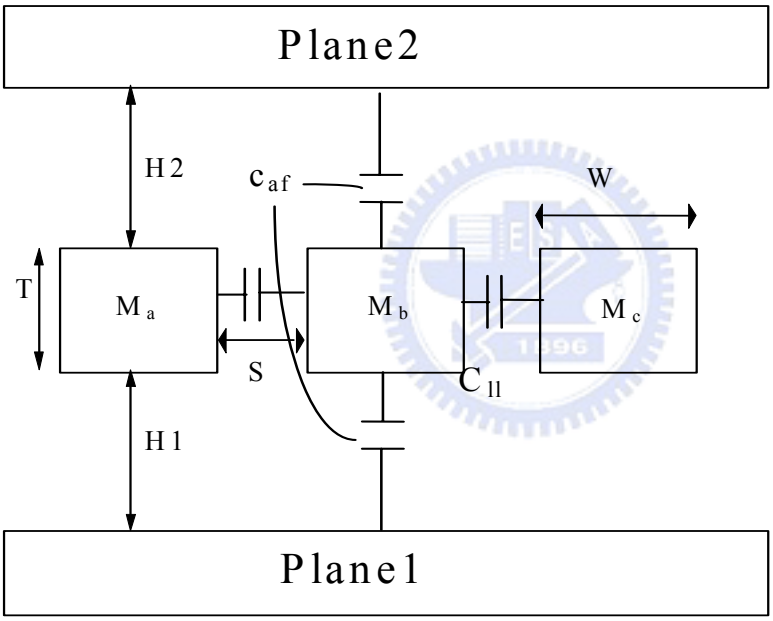
3-5 *Summary*

Accurate closed-form models for the 2-D capacitance and 3-D crossover capacitance in multilevel interconnections has been developed for arbitrary wiring dimensions. The model has been validated by the numerical solutions and measurement data, and it can be used for VLSI design and process optimization. The developed formulas then will be used many times in the following chapters for the delay, crosstalk noise, optimization design and statistic analysis in the following chapters: Chapter 4 will give the delay and crosstalk models, Chapter 5 will introduce the optimization of interconnect and Chapter 6 provide the statistic analysis of interconnect.



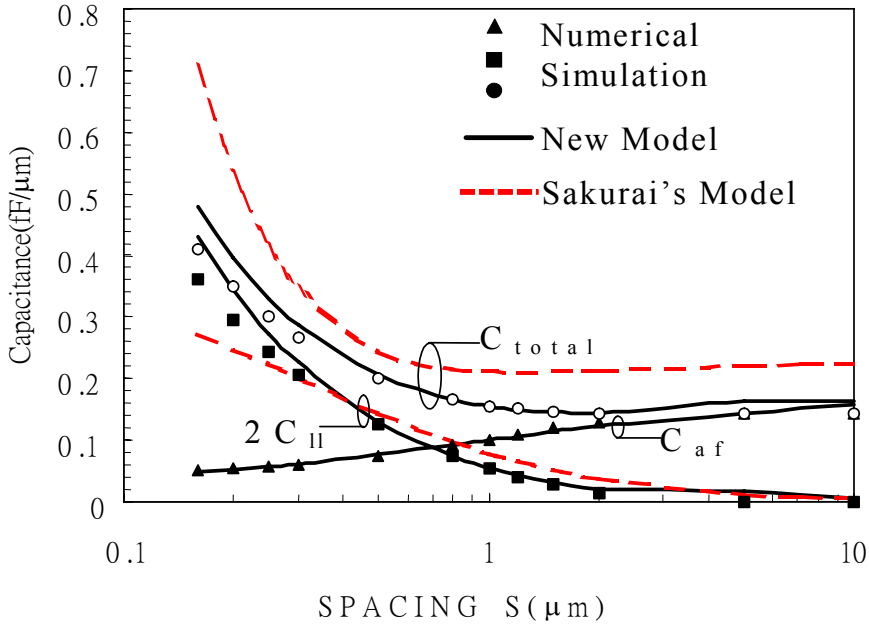


(a)

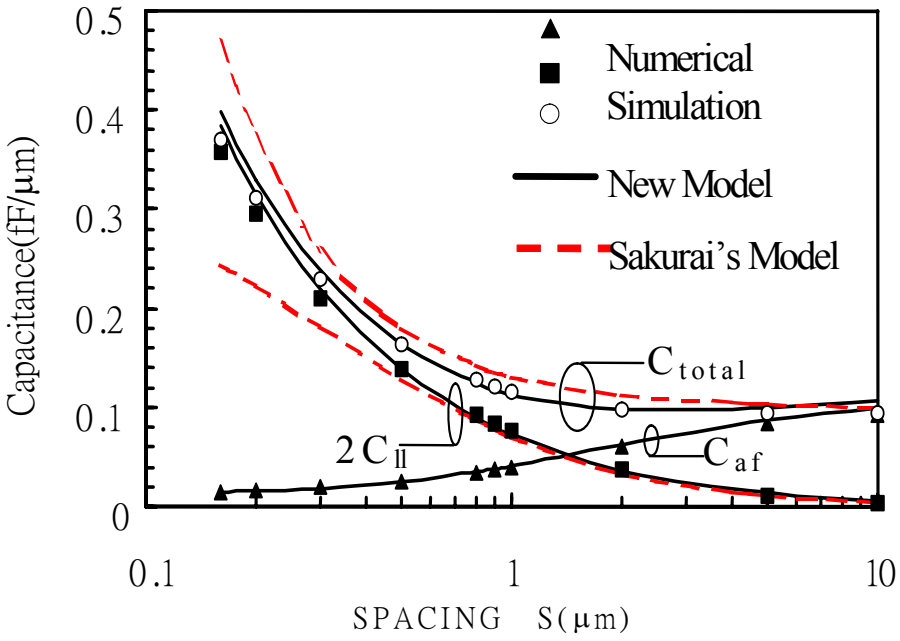


(b)

Figure 3. 1 (a) Cross-section diagram of parallel lines on one plane. (b) Cross-section diagram of parallel lines between two planes



(a)



(b)

Figure 3. 2 (a) Verification of model accuracy of various capacitance components [(1)-(2)]; symbols: Raphael, solid line: our model, dashed line: model in [2]. W=0.2μm and T=0.64μm, H=0.89μm. (b) Verification of model accuracy of various capacitance components [(3)-(4)]; symbols: Raphael, solid line: our model, dashed line: calculated by adding up the one-plane model based on formula in [2]. W=0.5μm and T=0.64μm, H_1=H_2=0.89μm.

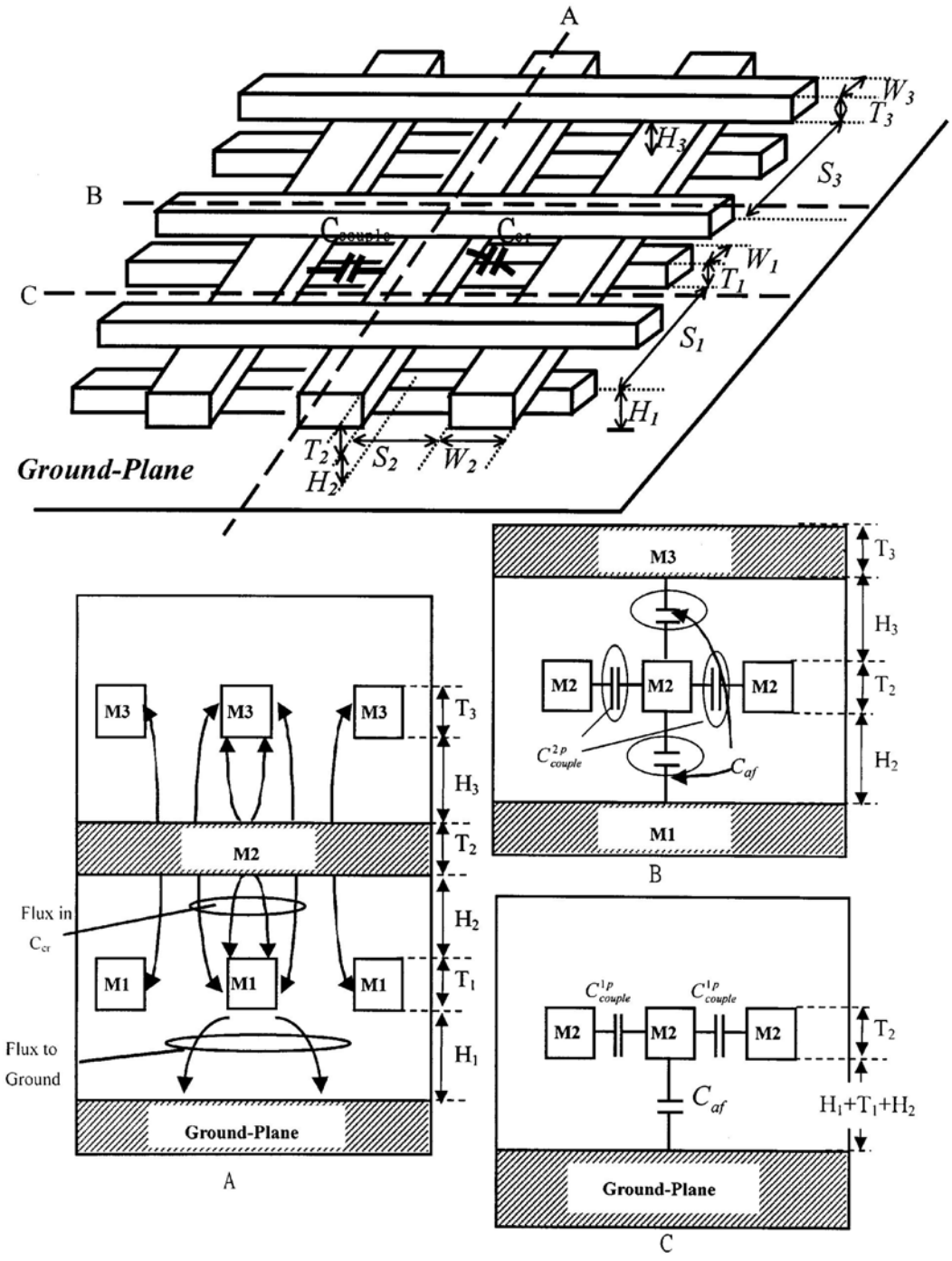


Figure 3. 3 Metal wiring crossover structure and cross sections along cut lines A, B, and C. H_1, H_2, and $H_3$are dielectric thickness, T_1, T_2, and $T_3$are metal wire thicknes, W_1, W_2 , and W_3 are wire width, and S_1, S_2, and S_3 are interwire spacing.

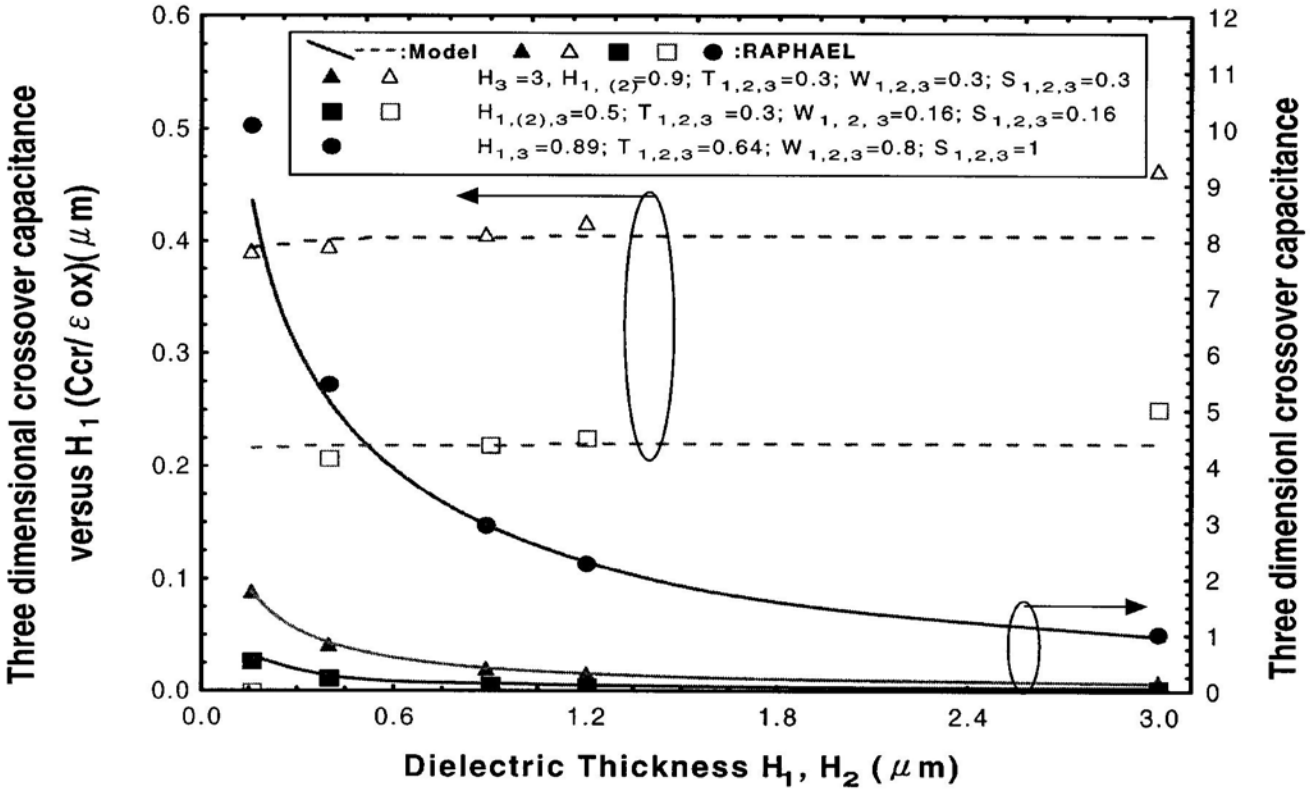


Figure 3. 4 Crossover capacitance variation versus dielectric thickness. Symbols denote Raphael simulation, and dashed and solid lines denote our model calculation.

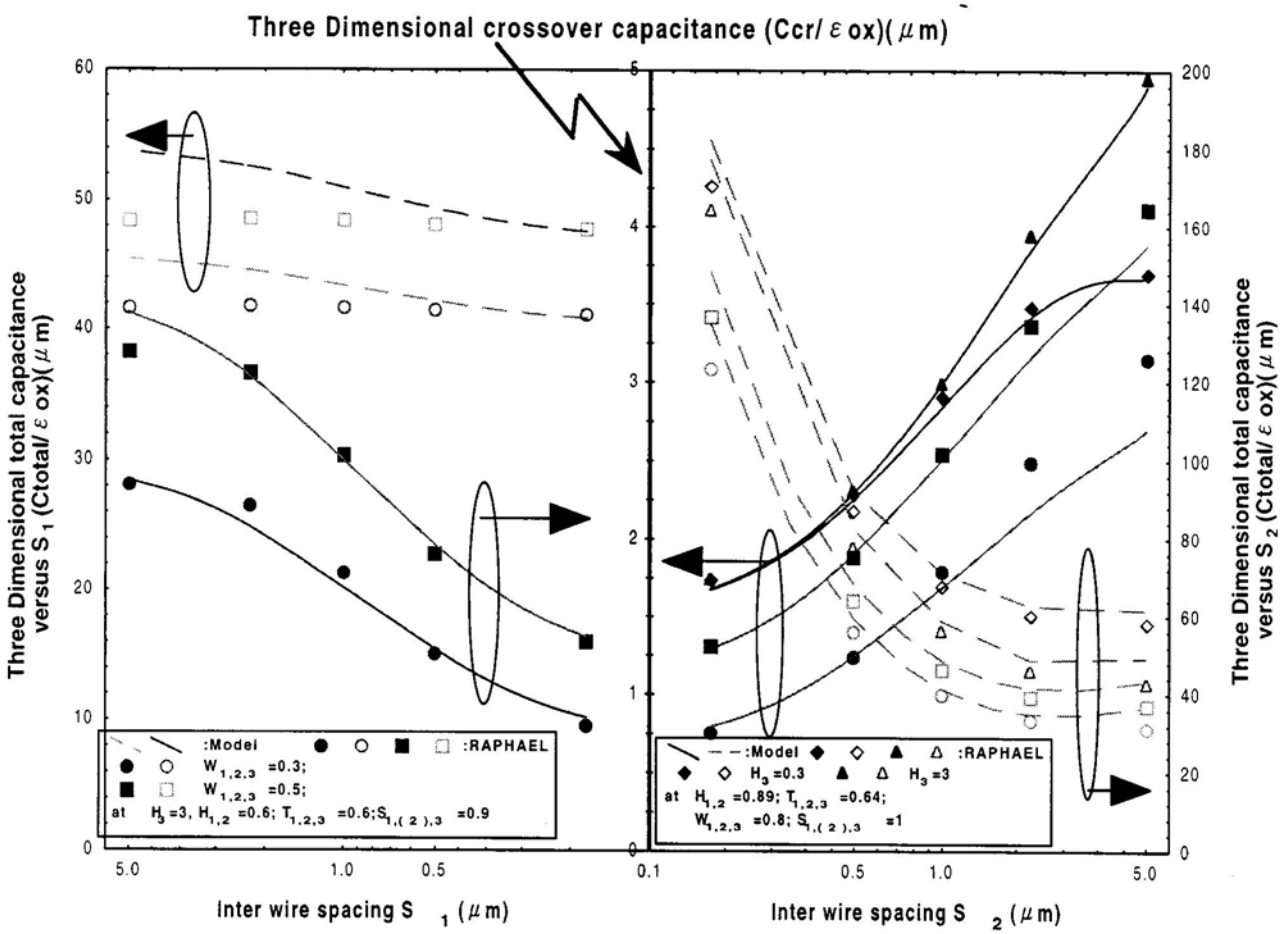


Figure 3. 5 Crossover capacitance and total capacitance variation versus intralayer wire spacing. Symbols denote Raphael simulation, and lines denote our model calculation. The left graph and right graph are correlated to each other by sharing the common axis of C_{cr} for comparing the different C_{cr} variation versus S_1 and. S_2 .

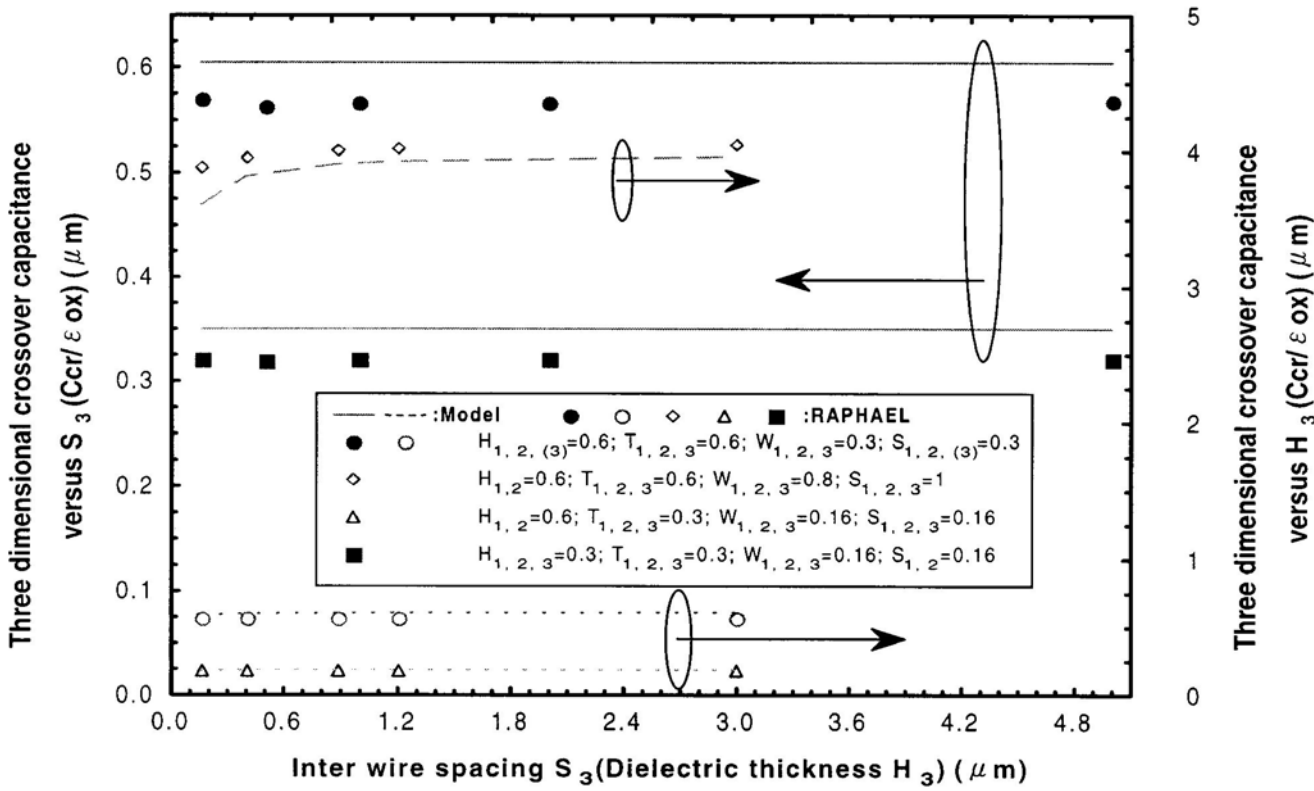


Figure 3. 6 Crossover capacitance variation versus top-level wire dielectric thickness and intralayer wire spacing. Symbols are Raphael simulation, and lines denote model calculation.

Table 3.1 Comparison of capacitance model with measurement data

Structure/Process	Model(10^{-12} Farad)	Measured(10^{-12} Farad)	Dimension parameters(μm)
M2-M1-poly, structure-2/0.5 μm	16.14	18.31	{W,S,T, H_1, H_2}={0.79,0.71,0.63,0.717}
M1-poly-field, structure-2/0.5 μm	17.45	17.52	{W,S,T, H_1, H_2}={0.805,0.695,0.63,0.378,0.717}
M1-field, structure-1/0.35 μm	7.741	8.176	{W,S,T,H }={1.032,0.685,0.969,1.023}
M3-M2-M1, structure-2/0.35 μm	19.77	19.55	{W,S,T, H_1, H_2}={0.501,0.776,0.49,0.737,0.793}
M2-M1-Field, structure-2/0.35 μm	10.72	11.27	{W,S,T, H_1, H_2}={0.50,0.99,0.776,1.02,0.737}

Table 3.2 Error table of the capacitance model of parallel lines on one plane compared with numerical solutions

	T	0.15	0.15	0.15	0.15	0.15	0.64	0.64	0.64	0.64	0.64	0.92	0.92	0.92	0.92	0.92	1.20	1.20	1.20	1.20	1.20
	H	0.16	0.20	0.50	0.89	2.71	0.16	0.20	0.50	0.89	2.71	0.16	0.20	0.50	0.89	2.71	0.16	0.20	0.50	0.89	2.71
S	**W**																				
0.16	**0.16**	-1.1	-1.2	-1.5	-2.7	-5.6	-2.4	-3.1	-5.9	-7.6	-9.9	-2.4	-3.3	-6.6	-8.4	-10.5	-2.6	-3.6	-7.1	-8.9	-11.0
0.16	**0.20**	-1.2	-1.3	-1.4	-2.1	-4.7	-2.4	-3.1	-5.8	-7.4	-9.5	-2.5	-3.4	-6.6	-8.2	-10.3	-2.6	-3.6	-7.1	-8.8	-10.8
0.16	**0.50**	-0.6	-0.9	-0.4	0.1	0.8	-2.1	-2.8	-5.1	-5.8	-6.6	-2.3	-3.1	-6.0	-7.0	-8.1	-2.4	-3.4	-6.6	-7.7	-9.0
0.16	**0.80**	0.0	0.2	0.7	2.0	4.7	-1.4	-2.0	-4.2	-4.7	-4.5	-1.7	-2.5	-5.3	-6.1	-6.4	-1.9	-2.8	-6.0	-7.0	-7.7
0.16	**2.00**	1.7	2.0	3.4	5.2	10.9	0.3	-0.1	-1.7	-2.0	-0.3	-0.2	-0.7	-3.1	-3.8	-3.0	-0.5	-1.2	-4.0	-5.0	-4.8
0.20	**0.16**	-1.0	-0.7	-0.1	-1.5	-5.3	-1.3	-2.0	-4.8	-6.5	-9.4	-1.4	-2.3	-5.5	-7.4	-10.1	-1.4	-2.4	-6.1	-8.0	-10.7
0.20	**0.20**	-0.87	0.1	0.7	-0.4	-3.2	-1.5	-1.7	-4.3	-5.9	-8.2	-1.6	-2.1	-5.2	-7.0	-9.3	-1.5	-2.3	-5.8	-7.7	-10.1
0.20	**0.50**	-0.72	-0.4	0.4	1.0	1.3	-1.5	-1.9	-4.1	-4.9	-5.9	-1.5	-2.2	-5.0	-6.1	-7.5	-1.5	-2.3	-5.6	-6.9	-8.5
0.20	**0.80**	-0.13	0.2	0.8	2.0	4.3	-0.9	-1.4	-3.5	-4.1	-4.1	-1.1	-1.7	-4.5	-5.4	-6.0	-1.2	-2.0	-5.1	-6.3	-7.2
0.20	**2.00**	1.41	1.7	3.0	4.5	10.0	0.5	0.2	-1.2	-1.6	0.0	0.2	-0.2	-2.4	-3.2	-2.5	0.0	-0.6	-3.3	-4.4	-4.2
0.50	**0.16**	-0.20	-0.4	2.4	3.3	-2.2	2.0	1.2	0.0	-0.7	-5.1	2.5	1.4	-0.6	-1.7	-6.2	2.8	1.7	-1.1	-2.6	-7.0
0.50	**0.20**	-0.12	0.6	3.5	5.0	1.1	1.7	1.6	0.6	0.1	-3.8	2.2	1.7	-0.3	-1.4	-5.3	2.7	1.9	-0.8	-2.3	-6.3
0.50	**0.50**	-0.13	0.0	1.4	3.0	1.8	1.0	0.5	-0.8	-0.9	-3.2	1.4	0.7	-1.3	-2.1	-4.6	1.7	0.9	-1.7	-2.8	-5.7
0.50	**0.80**	-0.07	-0.1	0.6	1.9	2.7	0.7	0.2	-1.2	-1.4	-2.3	1.1	0.4	-1.6	-2.3	-3.9	1.4	0.6	-1.9	-3.0	-4.9
0.50	**2.00**	0.56	0.5	0.9	1.8	5.1	0.8	0.5	-0.5	-0.8	0.1	1.0	0.6	-0.9	-1.6	-1.6	1.2	0.7	-1.2	-2.2	-2.8
1.00	**0.16**	-0.25	-1.7	-1.7	2.6	3.7	6.1	4.3	1.0	2.2	1.9	6.7	4.9	1.1	1.6	0.3	7.0	5.3	1.0	1.1	-0.8
1.00	**0.20**	0.12	-0.4	0.0	4.1	5.8	5.9	4.6	1.6	2.7	2.3	6.4	5.1	1.4	1.8	0.6	6.8	5.3	1.2	1.1	-0.7
1.00	**0.50**	1.25	0.6	0.1	3.0	5.1	4.3	3.4	0.7	1.4	1.6	4.7	3.8	0.6	0.8	0.0	5.1	4.1	0.6	0.3	-1.1
1.00	**0.80**	1.22	0.6	-0.2	1.8	4.6	3.3	2.6	0.1	0.6	1.2	3.7	2.9	0.1	0.0	-0.2	4.1	3.2	0.1	-0.4	-1.3
1.00	**2.00**	0.94	0.6	-0.3	0.5	3.4	1.9	1.4	-0.3	-0.4	0.7	2.1	1.7	-0.3	-0.8	-0.5	2.3	1.9	-0.3	-1.1	-1.3
2.00	**0.16**	-1.18	-3.6	-9.1	-6.4	4.6	10.8	8.5	0.7	0.0	6.2	12.4	10.1	2.1	0.8	5.4	13.1	10.9	2.8	1.2	4.5
2.00	**0.20**	-0.38	-2.4	-7.5	-5.0	6.5	10.6	8.5	1.2	0.6	6.5	12.0	10.0	2.4	1.1	5.4	12.7	10.8	3.0	1.3	4.4
2.00	**0.50**	1.98	0.7	-3.4	-2.0	6.3	8.2	7.0	1.6	0.9	5.3	9.3	8.1	2.5	1.2	4.4	9.9	8.7	2.9	1.3	3.5
2.00	**0.80**	2.34	1.4	-2.1	-1.3	5.7	6.7	5.9	1.5	0.6	4.5	7.5	6.7	2.1	0.9	3.6	8.0	7.1	2.5	0.9	2.8
2.00	**2.00**	1.85	1.4	-0.7	-0.9	3.4	3.8	3.4	0.8	-0.2	2.2	4.2	3.9	1.1	-0.1	1.6	4.5	4.1	1.3	0.0	1.0

Table 3.3 Error table of the capacitance model of parallel lines between two planes compared with numerical solutions

	T	0.15	0.15	0.15	0.15	0.15	0.64	0.64	0.64	0.64	0.64	0.92	0.92	0.92	0.92	0.92	1.20	1.20	1.20	1.20	1.20
	H1 &H2	0.16	0.20	0.50	0.89	2.71	0.16	0.20	0.50	0.89	2.71	0.16	0.20	0.50	0.89	2.71	0.16	0.20	0.50	0.89	2.71
S	**W**																				
0.16	**0.16**	-0.6	0.3	4.1	11.5	33.4	-4.1	0.1	14.1	21.9	35.4	-5.2	-0.2	15.9	23.8	35.8	-5.9	-0.5	16.9	24.9	36.1
0.16	**0.20**	-0.5	0.3	3.1	9.4	29.9	-4.0	0.1	13.4	20.8	34.0	-5.0	-0.2	15.3	22.9	34.7	-5.7	-0.4	16.5	24.2	35.1
0.16	**0.50**	-0.2	0.3	0.6	2.5	15.0	-3.0	0.1	11.1	16.5	26.7	-4.0	-0.1	13.3	19.4	29.1	-4.8	-0.3	14.8	21.2	30.6
0.16	**0.80**	-0.1	0.3	0.4	0.9	8.5	-2.4	0.1	10.0	14.8	23.0	-3.3	-0.1	12.3	18.0	26.1	-4.1	-0.3	13.8	20.0	28.1
0.16	**2.00**	0.0	0.2	0.3	0.2	0.9	-1.3	0.1	7.4	11.9	17.3	-2.0	0.0	9.6	15.1	21.3	-2.6	-0.2	11.2	17.4	24.0
0.20	**0.16**	-1.4	-0.3	2.1	8.2	31.7	-7.8	-3.6	10.6	18.6	34.0	-9.7	-4.7	12.1	20.5	34.6	-11.0	-5.5	13.0	21.7	34.9
0.20	**0.20**	-1.2	-0.3	1.2	6.4	37.4	-7.5	-3.5	10.0	17.5	32.5	-9.3	4.5	11.6	19.7	33.4	-10.7	-5.3	12.7	21.0	33.9
0.20	**0.50**	-0.6	0.0	-0.5	0.3	13.6	-5.5	-2.6	8.0	13.3	24.9	-7.3	-3.4	9.9	16.3	27.4	-8.6	-4.4	11.1	18.1	29.0
0.20	**0.80**	-0.4	0.0	-0.5	-0.9	7.0	-4.3	-2.1	7.1	11.8	20.9	-6.0	-3.0	9.0	14.8	24.1	-7.3	-3.8	10.3	16.8	26.2
0.20	**2.00**	-0.2	0.0	-0.2	-0.9	-0.5	-2.4	-1.2	5.1	9.2	14.9	-3.5	-1.9	6.8	12.2	19.0	-4.5	-2.4	8.1	14.3	21.8
0.50	**0.16**	-2.9	-1.1	2.0	0.7	15.8	-18.2	-15.0	-1.2	4.9	21.1	-22.6	-18.8	-2.2	5.9	22.8	-26.0	-21.8	-3.0	6.6	23.9
0.50	**0.20**	-2.6	-1.0	1.5	0.0	14.0	-17.2	-14.1	-1.3	4.4	20.1	-21.4	-24.7	-2.2	5.5	21.9	-24.7	-20.9	-3.0	6.2	23.1
0.50	**0.50**	-1.5	-0.5	0.7	-2.3	4.1	-11.7	-9.9	-1.2	2.5	13.5	-15.1	-13.1	-2.0	3.8	16.3	-18.1	-15.8	-2.7	4.7	18.3
0.50	**0.80**	-1.0	-0.3	0.6	-2.5	-1.0	-8.9	-7.7	-0.9	1.9	9.6	-11.7	-10.4	-1.6	3.2	12.9	-14.3	-12.8	-2.3	4.1	15.2
0.50	**2.00**	-0.5	-0.1	0.5	-1.5	-6.0	-4.5	-4.0	-0.5	1.4	4.2	-6.2	-5.7	-1.0	2.4	7.8	-7.7	-7.2	-1.5	3.1	10.5
1.00	**0.16**	-1.1	1.0	7.2	6.2	4.1	-18.4	-14.4	-6.1	0.2	7.6	26.7	-24.2	-9.5	-1.2	9.4	-30.1	-27.6	-12.0	-2.3	10.8
1.00	**0.20**	-1.0	0.9	6.5	5.4	3.3	-17.2	-18.3	-6.0	0.1	7.3	-25.1	-22.9	-9.2	-1.3	9.1	-28.4	-26.3	-11.7	-2.3	10.4
1.00	**0.50**	-0.5	0.6	56.5	2.8	-1.7	-13.8	-12.7	-4.8	-0.5	3.9	-17.4	-16.4	-7.5	-1.5	6.0	-20.1	-19.2	-9.6	-2.4	7.7
1.00	**0.80**	-0.4	0.0	3.4	2.0	-4.5	-10.4	-9.7	-3.9	-0.5	1.6	-13.3	-12.8	-6.2	-1.4	3.9	-15.6	-15.1	-8.1	-2.1	5.7
1.00	**2.00**	-0.2	0.2	1.9	1.4	-6.7	-5.2	-5.0	-2.2	-0.2	-1.2	-6.9	-6.8	-3.7	-0.8	0.9	-8.2	-8.2	-5.0	-1.4	2.7
2.00	**0.16**	1.3	4.2	14.1	16.1	6.7	-22.1	-19.9	-7.8	0.0	3.3	-27.7	-25.7	-13.5	-4.4	2.9	-31.5	-29.7	-17.4	-7.5	2.8
2.00	**0.20**	1.2	3.8	12.9	14.8	6.1	-20.7	18.8	-7.6	-0.2	3.1	-26.1	-24.4	-13.2	-4.5	2.8	-29.7	-28.2	-17.0	-7.4	2.8
2.00	**0.50**	0.7	2.3	8.4	9.7	2.1	-14.0	-13.1	-6.3	-0.8	1.7	-18.1	-17.5	-10.7	-4.2	1.8	-21.0	-20.6	-14.0	-6.7	1.9
2.00	**0.80**	0.5	1.7	6.6	7.7	0.1	-10.6	-10.1	-5.1	-0.1	0.6	-13.8	-13.6	-8.9	-3.7	-0.9	-16.2	-16.2	-11.7	-5.9	1.1
2.00	**2.00**	0.2	0.8	3.7	4.7	-1.9	-5.3	-5.2	-2.9	-0.4	-0.7	-7.1	-7.2	-5.3	-2.3	-0.3	-8.5	-8.7	-7.2	-3.8	0.0

Table 3.4 Error table of the capacitance model for crossover structure compared with numerical solutions

Technology dimension (μm)						Wire dimension (μm)						Error(%)
H3	H2	H1	T3	T2	T1	W3	W2	W1	S3	S2	S1	
2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	-2.700
0.16	0.16	0.16	0.16	0.16	0.16	2.0	2.0	2.0	2.0	2.0	2.0	-3.900
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	1.0	0.16	-2.285
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	1.0	0.5	1.166
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	0.16	1.0	-3.982
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	0.16	1.0	1.0	-0.152
0.89	0.89	0.89	0.64	0.64	0.64	0.8	0.8	0.8	1.0	1.0	1.0	-0.223
3.0	0.9	0.16	0.6	0.6	0.6	0.3	0.3	0.3	0.3	0.3	0.3	2.953
3.0	0.9	3.0	0.6	0.6	0.6	0.3	0.3	0.3	0.3	0.3	0.3	-7.232
0.9	0.16	0.9	0.6	0.6	0.6	0.3	0.3	0.3	0.3	0.3	0.3	0.596
0.16	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	2.682
0.89	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	4.693
3.0	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	5.145
0.16	0.16	0.16	0.16	0.16	0.16	2.0	2.0	2.0	0.16	0.16	0.16	-5.500
0.3	0.3	0.3	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	8.905
0.5	0.5	0.4	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	5.470
0.5	0.5	0.9	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	-0.241
0.5	0.16	0.5	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	8.028
0.16	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	0.414
0.4	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	1.341
0.89	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	1.759
3.0	0.6	0.6	0.3	0.3	0.3	0.16	0.16	0.16	0.16	0.16	0.16	2.035
0.16	0.16	0.16	2.0	2.0	0.16	0.16	0.16	0.16	0.16	0.16	0.16	4.800
2.0	2.0	2.0	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	8.300
2.0	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	6.300
0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	6.400

Table 3.5 Comparison between measurement data and the model for crossover structure

Capacitance/ Parameters(μm)	Model (aF/crossover)	Measurement (aF/crossover) Mean, standard deviation
M_2-M_3 C_{cr} W_1=W_2=S_1=S_2=0.4, T_1=T_2=0.6, H_1=2.602, H_2=0.848, H_3=0.979	26.06	24.85, 1.64%
M_2-M_3 C_{cr} W_1=W_2=0.8, S_1=S_2=0.4, T_1=T_2=0.6, H_1=2.602, H_2=0.848, H_3=0.979	55.69	56.49, 1.67%
M_1-M_2 C_{cr} W_1=W_2=0.4, S_1=S_2=0.4, T_1=T_2=0.6, H_1=0.966, H_2=0.848, H_3=0.979	25.95	24.91, 2.42%

Chapter 4 Interconnect Delay and Crosstalk Modeling

In modern VLSI, to increase circuit density, the width and spacing of wire should be reduced in accordance with the scaling rule. This, however, increases the resistance and line-to-line coupling capacitance dramatically. The increased resistance and coupling capacitance affects the performance of circuits by delaying signal transfer and crosstalk noise on the adjacent wire[4.1]-[4.3]. Many methods were proposed to solve the problem, such as the use of the new low-dielectric-constant ILD (Inter-Layer-Dielectric) and a copper metal wire [4.4]-[4.5]. To determine the optimized designs of interconnect, many related parameters, such as wire geometry, driver size, loading conditions and dielectric property have to be considered simultaneously. On the other hand, analytical models for calculating the interconnection delay and crosstalk noise are needed for the optimization design of the interconnect system. To our knowledge, previous works [4.15], [4.17], [4.18] on the time-domain closed-form solution all focused on the step input approximation and the simple loading condition, and none of them modeled the general compact model of interconnect delay time and crosstalk voltage for various loadings and input waveforms for distributed coupled interconnects. The purposes of this study are to develop signal delay and crosstalk voltage models for fast and accurate calculation of interconnect performance and to implement these models to the optimization design.

Conventionally, much time-consuming work needs to be executed before a circuit designer can actually estimate interconnect performance. Initially, the capacitances of some specified wire dimensions are simulated by a 2D (two-dimensional) or 3D (three-dimensional) field solver for various layout structures,

thereby generating many huge look-up tables from the simulation data. The capacitances are then calculated by the method of interpolation from complex look-up tables. Thereafter, SPICE simulation is executed to calculate the delay and crosstalk noise of a system based on the previously calculated interconnection capacitances. According to this flow, the process for interconnection optimization design is very time-consuming. To evaluate rapidly the circuit performance for the optimization design, accurate closed-form equations for wire capacitance, signal delay time, and crosstalk noise voltage are necessary.

The complete evaluation of interconnect performance includes line capacitance, delay and crosstalk calculation. Much work has been devoted to the calculation of line capacitance [4.6]-[4.13]. Chang [4.6] used the conformal mapping method to solve a two-dimensional Poisson's equation. Sakurai and Tamaru [4.7] developed empirical formulas for parallel lines on a large plane. However, the overestimation of total capacitance (C_{total}) and area-fringe capacitance (C_{af}) and the underestimation of line-to-line capacitance (C_{ll}) for small interconnection geometry were observed [4.8]. Choudhury and Sangiovanni-Vincentelli [4.9] formulated models for several layout primitives but only for one set of technology parameters. Chern et al.[4.10] formulated a general capacitance formula for three-dimensional crossing lines assuming the same dielectric and wire thickness for all layers. Wong et al [4.11] developed several lumped empirical capacitances for various interconnection structures for delay calculation only. Although lumped total capacitance may be a convenient approach for the approximation of delay time, it may cause serious errors in crosstalk noise analysis even though the total capacitance models are accurate. Arora et al.[4.12] presented a look-up table method for computer-aided design. In this thesis (Chapter 3) [4.13] presented a new 3D crossover capacitance model for various interconnect dimensions and verified that the total capacitance is the combination of

those of the 2D structure (Chapter 2) [4.14] and the 3D crossover structure.

For delay and crosstalk modeling, Sakurai [4.15] derived a good simple solution of the partial differential equation of a single isolated line under the assumption of step input waveform. This model is good for its intended applications such as two coupled lines and high input impedance gates. However, it overestimates or underestimates the amount of crosstalk signal for more general structures. Moreover, no general closed-form solution of the delay time and crosstalk noise voltage was shown in Sakurai's paper in the case of two coupled lines. Cases and Quinn [4.16] discussed the transient response of single RLC transmission lines but the closed-form solution was omitted from their work. The coupled interconnect structure, which is very important in VLSI circuits, was not discussed. Davis and Meindl [4.17], [4.18] gave the closed-form solution for coupled RLC transmission lines but the step input, infinite length line and open load were assumed in their work.

Instead of presenting a new set of capacitance models, we use herein the physical-based empirical interconnection capacitance models discussed in Chapter 3. The most important contributions of the previous discussed capacitance models are that they are decoupled capacitance models. The decoupled capacitance models separate the lumped total capacitance into area-fringe capacitance per unit length (c_{af}) and line-to-line capacitance per unit length (c_{ll}). c_{af} contributes to the delay of signal and c_{ll} is related to the amount of coupled noise and the signal delay. Then, the new and complete signal delay and crosstalk noise equations proposed in this paper are based on these decoupled interconnection capacitance models. The delay and crosstalk solutions are verified for various ramp input waveforms, loading resistances, and capacitances by SPICE simulation.

In next chapter (Chapter 5), a new interconnect design concept, the guaranteed-performance design method, is proposed which is based on the

capacitance, delay and crosstalk models discussed in Chapter 3 and Chapter 4.

4-1 One-Line Interconnect System Delay Modeling

A long global interconnect wiring is mostly used as the top layer in a multilayered interconnect system. To relax RC delay and crosstalk noise due to the long interconnect wiring, i.e., large resistance and coupling capacitance, and to diminish technological problems induced by surface nonuniformity at the top layer after a multilayered process, the spacing of the interconnect in this layer is deliberately designed to be large. Therefore, the analysis of interconnect performance in this case can be viewed as an isolated single line problem. The interconnect in this layer will not be affected by nearby noise; therefore, crosstalk noise is not a problem of this isolated line. On the other hand, signal delay is the most important concern when high-speed signal transfers on the long isolated single line. The use of wider copper lines and low-k material can reduce the resistance and capacitance of wire and solve the problem of time delay.

The nonlinear characteristic of CMOS (Complementary Metal Oxide Semiconductor) device is approximately simplified as a linear one. Then, the gate is modeled as a resistance (R_s) at the driving port and a capacitance (C_L) at the driven port. The single interconnect with driving and driven ports can be modeled as the RC network shown in Fig. 4.1.

The derivation of the output voltage with ramp input in the s-domain is given in the Appendix (Part A). Accordingly, the output voltage at the end of the line in the time domain, $V(t,l)$, is derived from the inverse Laplace transformation of eq. (A-2) in the Appendix, and is given by

$$V(l,t) = \frac{m\left(RC_{af}\,k\left(1 - e^{-\sigma t / RC_{af}}\right) + t\sigma + \left(RC_{af}\,k\left(-1 + e^{-(t-a)\sigma / RC_{af}}\right) + (a-t)\sigma\right)U(t-a)\right)}{\sigma} \quad .$$

(4. 1)

The definitions of k and σ are found in Part A of the Appendix.

To derive the closed-form solution of the delay time, a reasonable assumption is made that 90 % threshold delay time, t_d, is longer than the input ramping rate, a. Therefore, $U(t-a)$ equals 1 in the following discussions. Then eq. (4.1) is rewritten as

$$V_x = V(l, t_d) = am + \frac{RC_{af}\,km}{\sigma}\left(e^{a\sigma / RC_{af}} - 1\right)\chi \ , \qquad (4.2)$$

where V_x is the output voltage rise to 90% V_{dd}, t_d is the output signal delay time, and χ represents $e^{-\sigma t_d / RC}$.

Then, the 90% threshold delay time t_d is calculated from the solution of χ in eq. (4.2) and given by

$$t_d = -\frac{RC_{af}}{\sigma}\ln(\chi) = -\frac{RC_{af}}{\sigma}\ln\left(\frac{\sigma(V_{dd} - V_x)}{RC_{af}\,km(1 - e^{a\sigma / RC_{af}})}\right) \quad . \qquad (4.3)$$

To examine the accuracy of the models developed as described above, SPICE simulation was carried out. In SPICE simulation, to make sure that the distribution properties of the line are well simulated, the wire is divided into 20 lumped sections. The wire delay time for various input rise times is plotted in Fig. 4.2. The figure shows that the delay time is dependent on the input ramping rate and well formulated in the new model. Dashed lines in Fig. 4.2 represent the solutions of Sakurai's model [15], which did not take the input rise time into consideration in the interconnect

delay time calculation. The delay time symmetry of R_T and C_T in the one-line system is observed in both SPICE simulation and the new model. Taking the design of repeater, a series of connected CMOS and each CMOS is separated by interconnect, as an example, the reduction of driver resistance (R_s) by increasing driver size will increase the loading capacitance (C_L) next stage [20]. These two phenomena compensate for each other and keep the delay time at an approximately constant value if the relations R_T*C_T and R_T+C_T are kept constant.

4-2 Dual Parallel Coupled Interconnect Delay and Crosstalk Modeling

For two coupled interconnect, let us discuss the special case for step input first. And then we will continue on the discuss the general case for ramp inputs which is important for accurate capture the delay time and crosstalk induced noise effects.

4.2.1 Step Input Case

Our delay model is based on the circuit schematic diagram shown in Fig, 4.1(b) with step inputs, where two lines of length L in the same layer run in parallel, with each line being modeled by a distributed RC-line. These two lines couple via the coupling capacitance c_{ll} per unit length. c_{af} is the unit-length line-to-ground capacitance of each line.

Let V_1 and V_2 denote the signals propagating on first and second line, and let r_1 and r_2 be the unit-length resistance of the first and second line. Applying step function input E_1 to the first line and with input of the second line being grounded, we analyze the signal at the end of the first line as the signal delay and at end of the second line as the crosstalk noise.

Let $C_{af} = c_{af} L$, $C_{ll} = c_{ll} L$ and $R = r_1 L = r_2 L$. From the Maxwell equations of [5], we have at $x = L$

$$\frac{V_1(L,t)}{E_1} = 1 + \frac{K_{11}}{2}\exp(-\frac{\sigma_{11}t}{RC_{af}}) + \frac{K_{12}}{2}\exp(-\frac{\sigma_{12}t}{RC_{af} + 2RC_{ll}}) \quad (4.4)$$

and

$$\frac{V_2(L,t)}{E_1} = 1 + \frac{K_{11}}{2}\exp(-\frac{\sigma_{11}t}{RC_{af}}) - \frac{K_{12}}{2}\exp(-\frac{\sigma_{12}t}{RC_{af} + 2RC_{ll}}) \quad , \quad (4.5)$$

where

$\sigma_{11} = 1.04/(R_T + C_{T11} + R_T C_{T11} + (2/\pi)^2)$, $\sigma_{12} = 1.04/(R_T + C_{T12} + R_T C_{T12} + (2/\pi)^2)$,

$K_{11} = (-1.01(R_T + C_{T11} + 1))/(R_T + C_{T11} + (\pi/4))$,

$K_{12} = (-1.01(R_T + C_{T12} + 1))/(R_T + C_{T12} + (\pi/4))$, $R_T = R_S/R$,

$C_{T11} = C_L/C_{af}$ and $C_{T12} = C_L/(C_{af} + 2C_{ll})$.

Note that in theory, one should have $V_1(L,0) = V_2(L,0) = 0$ at t=0. The forms in (4.4)-(4.5) actually give a small deviation from zero, which is induced by the approximations in obtaining σ_{11}, σ_{12}, K_{11} and K_{12}. This initial deviation does not affect the final results.

Here, the equations of (4.4)-(4.5) are based on a simplified two-line structure. This is intended to provide sufficient physical modeling in its simplest form. To consider three (or more) lines, one will end up with a set of three (or more) partial differential equations with three (or more) unknowns. To simplify such a set of differential equations to make it to solvable as in (4.4)-(4.5) , one in general needs to make the assumption that the signals on two successive even (or odd) numbered lines are the same, which can essentially reduce to our two-line model . Our two-line approximation is effective, as it will give simple closed-form solutions, and is directly

applicable in at least two applications. 1) Assuming that the M_b is the active line and M_c is the victim line, our result is directly applicable when M_a has the same signal with M_b , hence the signal flow to M_a can be eliminated . 2) When both M_a and M_c are quiet victim lines, our model can be applied by simply modifying C_{ll} to $2C_{ll}$, which approximates the signal on the forth line next to M_a being similar to that on M_b .

To solve (4.4) , set x = exp(-(σ_{11}/RC_a)) , α = $C_{af}/(C_{af}+2C_{ll})(\sigma_{12}/\sigma_{11})$ and $a = 2((V_1/E_1)-1)$, and we rewrite (4.4) as $K_{12}x^{\alpha}+K_{11}x$ = a, whence $x \approx ((a-K_{11}x)/K_{12})^{1/a} = (a/K_{12})^{1/a}(1-(K_{11}x/a))^{1/a}$. Since 0 < x < 1 and 0 < a < 1 , it follows that $0.5^{1/a} < x/a < 0.5$, and (1-$(K_{11}x/a))^{1/a}$) can be well approximated by a first order polynomial using . Taylor's expansion , i.e. x = $(a/K_{12})^{1/a}(1-(K_{11}x/a))^{1/a} \approx (a/K_{12})^{1/a}(1-(K_{11}/a)(x/a))$, whence x is solved as x $\approx (a/k_{12})^{1/\alpha}(1+((a/k_{12})^{1/\alpha}K_{11})/\alpha a)^{-1}$. The delay time for $V_1(t)$, denoted by t_d , which is to rise to 0.9 E_1 , is simply

$$t_d = -\frac{RC_{af}L}{\sigma_{11}}\ln\left(\frac{(a/k_{12})^{1/\alpha}}{1+((a/k_{12})^{1/\alpha}K_{11})/\alpha a}\right) . \qquad (4.6)$$

The time for peak crosstalk noise on the adjacent wire, denoted by t_p , can be obtained by solving the equation $(dV_2(L,t))/dt = 0$ in (6) , with

$$t_p = -\frac{RC_{af}L}{\sigma_{11}}\ln\left(\frac{\alpha K_{12}^{\frac{1}{a-1}}}{K_{11}}\right) \quad . \tag{4.7}$$

The peak crosstalk noise V_p on the adjacent wire is given by (6) with t $\approx t_p$, i.e.

$$V_p = \frac{E_1}{2}\left\{K_{11}\exp\left(-\frac{\sigma_{11}t_p}{RC_{af}^a}\right) - K_{12}\exp\left(-\frac{\sigma_{12}t_p}{R(C_{af}^a + 2C_{ll}^a)}\right)\right\} . \tag{4.8}$$

To examine the accuracy of the models developed above , we calculate interconnect lines as a distributed RC delay line . We divide the delay line into 20 sections. Coupling and area-fringe capacitances of the lines , C_{comple} and C_{nf} , are obtained from our capacitance model of Chapter 3 , and resistance of each line section is proportional to the in verse of cross-section area and to the length of each section , with resistivity of 0.025 $\Omega\mu m$. The accuracy of our delay and cross talk model is demonstrated in Fig . 4.3(a) , (b) , with comparison with SPICE simulations . Good agreement is shown.

Note that R_x in Fig . 4.1(c) in the active-line transistor and victim-jine transistor should in general be different . This may cause some tedious calculations in the derivations above. However, during the initial period of charging process , both transistors are dominated by the PMOS resistance in the saturation region . Thus , for that period , the use of the same resistance R_s in active and victim lines is a reason able approximation .

Here , we use a step input model in deriving the delay and crosstalk . In next section of this chapter. a different interconnect model with a ramp input will be given.

Fig. 4.3. (a) model accuracy of RC line delay model. (b) Model accuracy of RC

line crosstalk model.

Accurate closed-form models have been developed for wire delay and crosstalk noise with step inputs. The model developed here can be extending to cover the case with a ramp input in next section. The capacitance model in Chapter 3 gives line-to-line and line-to-ground capacitances separately, and lead to precise delay and crosstalk estimations. The delay and crosstalk formulas allow for simple analytic prediction of interconnection performance for arbitrary interconnect dimensions. Our model is useful for VLSI design and process optimization.

4.2.2 Ramp Input Case

For signal transfer on two parallel lines or on the outermost line of a set of parallel interconnections, the two-line system can be adopted in the analysis of interconnect performance. In the two-line system shown in Fig. 4.1(b), area capacitance (c_{af}) and line-to-line coupling capacitance (c_{ll}) can both contribute to signal delay. Moreover, the signal can be coupled to the adjacent quiet line, victim, by means of the coupling capacitance between two wires. The coupling noise can lead to erroneous level judgment and extra leakage power consumption of the gate next stage connected by victim.

The s-domain solutions of the coupled partial differential equations (PDEs) of the two-line system are given in the Appendix (Part B). In the derivation of s-domain solutions, we use the coupled equations $V_+(x,t)$ and $V_-(x,t)$ to decouple the PDEs, where $V_+(x,t) = V_1(x,t) + V_2(x,t)$ and $V_-(x,t) = V_1(x,t) - V_2(x,t)$ and $V_1(x,t)$ and $V_2(x,t)$ denote the signals on the aggressor and victim lines, respectively. Consequently, the time domain solutions of $V_+(x,t)$ and $V_-(x,t)$ are solved from the inverse Laplace transformation of eqs. (B-5) and (B-6) in the Appendix. Then, waveforms at the end of the interconnect, $V_1(l,t)$ and $V_2(l,t)$, in the time domain are

obtained by calculating $V_1(l,t) = (V_+(l,t) + V_-(l,t))/2$ and $V_2(l,t) = (V_+(l,t) - V_-(l,t))/2$. The waveform at the end of the aggressor line, $V_1(l,t)$, is

$$V_1(l,t) = am - \frac{C_{af}k_1mR(1-\alpha)}{2\sigma_1}\chi - \frac{C_{af}k_2mR(1-\lambda)}{\sigma_2}\left(\frac{1}{2}+\frac{C_{ll}}{C_{af}}\right)\chi^{\eta}, \quad (4.9)$$

where $\chi = e^{-t\sigma_1/RC_{af}}$, (4. 10)

$$\eta = \frac{C_{af}}{C_{af}+2C_{ll}}\frac{\sigma_2}{\sigma_1}, \quad (4.11)$$

$$\alpha = e^{a\sigma_1/RC_{af}}, \quad (4.12)$$

$$\lambda = e^{a\sigma_2/R(C_{af}+2C_{ll})}, \quad (4.13)$$

and the total line resistance (R), the total area-fringe capacitance (C_{af}), and the total line-to-line capacitance (C_{ll}) are calculated as $R=r\times l$, $C_{af}=c_{af}\times l$, and $C_{ll}=c_{ll}\times l$, respectively, and l is the length of the wire. Definitions of k_1, k_2, σ_1, and σ_2 are found in the Appendix (Part B).

For simplicity of expression, we set

$$A = \frac{C_{af}k_2mR(1-\lambda)}{\sigma_2}\left(\frac{1}{2}+\frac{C_{ll}}{C_{af}}\right), \quad (4.14)$$

$$B = -\frac{C_{af}k_1mR(1-\alpha)}{2\sigma_1} \text{ and} \quad (4.15)$$

$$P = am - V_1(l,t). \quad (4.16)$$

Then, eq. (4.9) can be rewritten as

$$A\chi^{\eta} - B\chi - P = 0. \quad (4.17)$$

Then, the solution of χ in eq. (4.17) is

$$\chi = \left(\frac{P}{A}\right)^{1/\eta}\left(1+\frac{B}{P}\chi\right)^{1/\eta} . \qquad (4.\ 18)$$

Equation (4.18) can be well approximated by a first-order polynomial using Taylor's expansion in the range of our applications, i.e.,

$$\chi = \left(\frac{P}{A}\right)^{1/\eta}\left(1+\frac{1}{\eta}\frac{B}{P}\chi\right) . \qquad (4.\ 19)$$

It is also possible to approximate the right-hand side of eq.(4.18) by a polynomial of order 2 using Taylor's expansion. Then, χ can be solved by solving a standard second-order polynomial equation that, in general, has better accuracy than first-order polynomial. However, our approximation already gives sufficient accuracy.

Then, the 90 % threshold delay time t_d is given by

$$t_d = RC_{af}\ \ln(\zeta_1)/\sigma_1 \ , \qquad (4.\ 20)$$

where

$$\zeta_1 = \frac{RC_{af}k_1 m(1-\alpha)}{2\eta\sigma_1(am-V_x)} + \left[\frac{R(C_{af}+2C_{ll})k_2 m(1-\lambda)}{2\sigma_2(am-V_x)}\right]^{1/\eta}$$

and $V_x = 0.9V_{dd}$.

The time for peak crosstalk voltage on the adjacent wire is calculated from the solution of $dV_2(l,t)/dt = 0$ and is given by

$$\frac{dV_2(l,t)}{dt} = \frac{1}{2}k_1 m(1-\alpha)\chi - \frac{C_{af}k_2 m(1-\lambda)}{C_{af}+2C_{ll}}\left(\frac{1}{2}+\frac{C_{ll}}{C_{af}}\right)\chi^{\eta} = 0\,. \tag{4. 21}$$

Following the methods similar to those described in the delay time calculation in this section, the time of the peak crosstalk voltage t_p is calculated as

$$t_p = -RC_{af}\ln(\zeta_2)/\sigma_1\,, \tag{4. 22}$$

where $\zeta_2 = \left((1-\alpha)k_1/(1-\lambda)/k_2\right)^{1/(\eta-1)}$.

The peak crosstalk voltage V_p on the adjacent wire is given by $V_p=V_2(l,t)=(V_+(l,t) - V_-(l,t))/2$ with $t=t_p$. Then,

$$V_p = \frac{1}{2}\frac{V_{dd}}{a}R\left[-\frac{(1-\alpha)C_{af}k_1\zeta_2}{\sigma_1} + \frac{(1-\lambda)(C_{af}+2C_{ll})k_2\zeta_2{}^{\eta}}{\sigma_2}\right], \tag{4. 23}$$

where α and λ are defined as eqs. (4.12) and (4.13).

SPICE simulation is based on the coupled interconnection circuit shown in Fig 4.1(b). The coupled wires are divided into 20 sections to describe the distribution properties of the interconnect. The interconnect in each section is modeled as a lumped serial connecting RC , and is a practical assumption within a reasonable length of the interconnect. Extra interconnection sections are easy to implement in SPICE if needed. The ramp input waveform is fed into the beginning of the interconnection. Signal delay is measured at the end of the line where the signal transferred (aggressor line). Crosstalk noise is measured at the end of the quiet line (victim line) adjacent to the signal line. Figures 3 and 4 show respectively the

accuracy of the delay time and the normalized crosstalk noise for various driver resistances and loading capacitances. The rise-time dependent delay time and crosstalk voltage are shown in both model and SPICE simulation. The new model coincides with the SPICE simulation.

4-3 Multiple Parallel Coupled Interconnect Delay and Crosstalk Modeling

The time-domain response of delay and crosstalk for the coupled line system is derived based on the equivalent circuit in Fig. 4.1(c). Capacitances c_{ll} and c_{af} can be obtained from the empirical equations in a previous chapter (Chapter 3).

The time-domain solutions of coupled equations, $V_+(x,t)$ and $V_-(x,t)$, are obtained from the inverse Laplace transformation of (C-5) and (C-6). The coupled equations in this system are $V_+(x,t) = V_1(x,t) + 2V_2(x,t)$ and $V_-(x,t) = V_1(x,t) - V_2(x,t)$. Then, waveforms at the end of the interconnect, $V_1(l,t)$ and $V_2(l,t)$, in the time domain are obtained by $V_1(l,t) = (V_+(l,t) + 2V_-(l,t))/3$ and $V_2(l,t) = (V_+(l,t) - V_-(l,t))/3$. From methods similar to those mentioned in section 4-2, the 90% threshold delay time (t_d) for $V_1(l,t)$ is simply

$$t_d = RC_{af} \ln(\zeta_3)/\sigma_1 \quad . \tag{4. 24}$$

ζ_3 in eq. (4.24) stands for

$$\zeta_3 = \frac{RC_{af}k_1 m(1-\alpha')}{3\eta'\sigma_1(am-V_x)} + \left(\frac{2R(C_{af}+3C_{ll})k_2 m(1-\lambda')}{3\sigma_2(am-V_x)}\right)^{1/\eta'},$$

where $V_x = 0.9V_{dd}$, $\eta' = C_{af}\sigma_2/(C_{af}+3C_{ll})/\sigma_1$, $\alpha' = \exp(a\sigma_1/R/C_{af})$, and $\lambda' = \exp(a\sigma_2/R/(C_{af}+3C_{ll}))$. Definitions of k_1, k_2, σ_1, and σ_2 can be found in the Appendix (Part C).

The time of peak crosstalk voltage (t_p) at the end of the victim lines is obtained by the solution of $dV_2(l,t)/dt = 0$ and is calculated as

$$t_p = -RC_{af} \ln(\zeta_4)/\sigma_1 \quad , \tag{4. 25}$$

where $\zeta_4 = [(1-\alpha')k_1/(1-\lambda')/k_2]^{1/(\eta'-1)}$.

Then, crosstalk voltage (V_p) at the end of the victim lines is given by $V_2\ (l,t)$ with $t=t_p$. The solution of the crosstalk voltage (V_p) is

$$V_p = \frac{1}{3}\frac{V_{dd}}{a} R\left[-\frac{(1-\alpha')C_{af}k_1\zeta_4}{\sigma_1} + \frac{(1-\lambda')(C_{af}+3C_{ll})k_2\zeta_4{}^{\eta'}}{\sigma_2}\right] \quad . \tag{4. 26}$$

SPICE simulation of the signal delay time and crosstalk noise voltage is based on three-coupled interconnect equivalent circuit shown in Fig. 4.1(c). The ramping input is applied at the beginning of the middle line (aggressor line). Signal delay is measured at the end of the middle line where a signal been transferred, and crosstalk noise is measured at the end of two quiet interconnects (victim lines) adjacent to the aggressor line. Figures 4.6 and 4.7 show the accuracy of the delay time and the normalized crosstalk noise for various driver resistances and loading capacitances. The rise time dependent delay time and crosstalk voltage are shown in both the model and SPICE simulation. The new model exhibits good agreement with the SPICE simulation, as shown in Fig. 4.6 and 4.7. For a large loading capacitance, the effect of crosstalk noise can be reduced because of the slow waveforms at the signal and the quiet lines, and is well modeled by the closed-form equations described above.

4-4 Crosstalk-Induced Delay Time Model

With the development of system-on-chip (SoC) design, more functions can now be integrated into a single chip, even if the die size remains relatively constant. Consequently, the average wire length has remained relatively constant despite the decrease in pitch. Total wire capacitance decreases with the reduction of wire width, but the fraction of lateral coupling capacitance increases dramatically, i.e., coupled noises that affect the signal that travels on the victim line have increased dramatically.

Crosstalk-induced delay deterioration cannot be eliminated by any practical technique except shielding all nets, which doubles the routing resources. However, increasing the timing margins to account for the extra delay in the stage of circuit simulation can solve the problem. This approach has been used over the years in the guise of multiplying the coupling capacitances by a constant, named the switching factor, to account for the Miller effect. Miller's theorem states that when there are two nodes connected by an admittance Y, the network can be equivalently realized by isolating the two nodes from each other by placing new admittances between each node and the ground node. The values of the new admittances are given by Y(1-*K*) and Y(1-1/*K*), where *K* is the voltage gain from node 1 to node 2. The voltage gain is 1 for a pair of lines switching in the same direction and the switching factor is zero. In the case of nets switching simultaneously in opposite directions, the voltage gain is –1. Thus, the new values for admittances are both 2Y. In this example, doubling the coupling capacitance accounts for the out-of-phase signal on the victim and aggressor lines. However, voltage gain on distributed interconnect is not exactly –1 at any instant. Hence, this method gives a pessimistic estimation of wire delay, which should be regarded as the upper-bounded solutions. Thus, a better timing analysis that accurately depicts the timing shift due to noise is required.

The problem of crosstalk-induced delay time deterioration is shown in Fig. 4.8(a).

The middle line is the victim line that switches in the direction opposite to that of the two neighboring aggressor lines. The signal-dependent delay is complex because the timing of inputs that drive the interconnect depends on the delay across the first gate, the interconnect, and the behavior of the other adjacent nets. The mismatches of driver, repeater, buffer size and wire parameters between parallel wires in the same interconnect system can drag and stretch the timing of inputs. The dragging and stretching inputs give a non-monotonic response to the victim line during switching and these non-simultaneously switching signals contribute to the additional delay time.

a_1 and a_2 in Fig. 4.8(a) are input ramping rates and b_1 and b_2 are arrival times of inputs in victim and aggressor lines, respectively. c_{ll} and c_{af} represent the intralayer and the interlayer capacitance per unit length, respectively. Capacitances can be calculated from the empirical capacitance equations discussed in Chapter 3 or a numerical field solver [4.21]. The CMOS (Complementary Metal Oxide Semiconductor) gate is modeled as a resistance (R_s) at the driving port and a capacitance (C_L) at the driven port.

For the worst-case delay time modeling, the input waveforms on the victim and aggressor lines are respectively denoted $V_{r1}(0,t)$ and $V_{r2}(0,t)$ and written as

$$V_{r1}(0,t) = U(t-b_1)m_1(t-b_1) - U(t-b_1-a_1)m_1(t-b_1-a_1) \quad (4.27)$$

and

$$V_{r2}(0,t) = -\left[U(t-b_2)m_2(t-b_2) - U(t-b_2-a_2)m_2(t-b_2-a_2)\right], \quad (4.28)$$

where m_1 and m_2 are the slopes of the input signals and are written as V_{dd} / a_1 and V_{dd} / a_2, respectively.

These generalized expressions for two ramp inputs account for the input arrival times (b_1 and b_2) and the signal rise and fall times (a_1 and a_2) on victim and aggressor lines. For simplicity of expression of the closed-form solutions, both lines are assumed to have zero arrival time (b_1=b_2=0) in the following calculation. The solutions can be easily extended to the case of non-zero arrival time (b_1≠0 and b_2≠0) using similar procedures to those used in this study.

The boundary conditions at the driving port of the interconnect are written as

$$V_{r1}(0,t) - I_1(0,t) * R_s = V_1(0,t) \tag{4. 29}$$

$$V_{r2}(0,t) - I_2(0,t) * R_s = V_2(0,t), \tag{4. 30}$$

where $V_1(x,t)$ and $V_2(x,t)$ are, respectively, the voltages on victim and aggressor lines at a distance x from the input. After the addition and elimination calculation of eqs. (3) and (4) above, the new boundary conditions for the coupled system are

$$\left(V_{r1}(0,t) + 2V_{r2}(0,t)\right) - I_+(0,t)R_s = V_+(0,t) \tag{4. 31}$$

$$\left(V_{r1}(0,t) - V_{r2}(0,t)\right) - I_-(0,t)R_s = V_-(0,t), \tag{4. 32}$$

where $V_+(0,t)=V_1(0,t)+2V_2(0,t)$, $V_-(0,t)=V_1(0,t)-V_2(0,t)$, $I_+(0,t)=I_1(0,t)+2I_2(0,t)$ and $I_-(0,t)=I_1(0,t)-I_2(0,t)$.

From the boundary conditions, eqs. (4.31) and (4.32), the coupled wires are decouple into two single isolated interconnects in which the effective total capacitances are C_{af} and C_{af}+3C_{ll} and driven by the input signals of $V_{r1}(0,t)+2V_{r2}(0,t)$ and $V_{r1}(0,t)-V_{r2}(0,t)$. Procedures similar to those in a previous study[1)] were used to calculate the s-domain solutions at the end of nets, $V_+(l,s)$ and $V_-(l,s)$,

$$V_+(l,s) = L\{1 - k_1 \exp(-\sigma_1 t / RC_{af})\} \times s \times L\{V_{r1}(0,t) + 2V_{r2}(0,t)\} \quad (4.33)$$

$$V_-(l,s) = L\{1 - k_2 \exp(-\sigma_2 t / R(C_{af} + 3C_{ll}))\} \times s \times L\{V_{r1}(0,t) - V_{r2}(0,t)\}, \quad (4.34)$$

where R, C_{ll}, and C_{af} are total resistance, line-to-line capacitance and area-fringing capacitance of the line calculated by rl , $c_{ll}l$ and $c_{af}l$, respectively, l is the length of the interconnection, and $L\{-\}$ in eqs. (4.33) and (4.34) represents the Laplace transformation. Then $k_1 = -1.01(R_{T1} + C_{T1} + 1)/(R_{T1} + C_{T1} + \pi/4)$, $k_2 = -1.01(R_{T2} + C_{T2} + 1)/(R_{T2} + C_{T2} + \pi/4)$, $\sigma_1 = 1.04/(R_{T1}C_{T1} + R_{T1} + C_{T1} + (2/\pi)^2)$, $\sigma_2 = 1.04/(R_{T2}C_{T2} + R_{T2} + C_{T2} + (2/\pi)^2)$, $R_{T1} = R_{T2} = R_t / R$, $C_{T1} = C_L / C_{af}$, and $C_{T2} = C_L / (C_{af} + 3C_{ll})$.

The time-domain solutions, $V_+(l,t)$ and $V_-(l,t)$, can be obtained by the inverse Laplace transform of the two s-domain equations above [eqs.(4.33) and (4.34)], hence the time-domain solution at the end of the victim line ($V_1(l,t)$) in Fig. 1(a) is calculated from the addition and elimination of $V_+(l,t)$ and $V_-(l,t)$ and shown as

$$\begin{aligned} V_1(l,t) &= L^{-1}\{V_+(l,s) + 2V_-(l,s)\}/3 = [V_+(l,t) + 2V_-(l,t)]/3 \\ &= [V_1(l,t) + 2V_2(l,t) + 2(V_1(l,t) - V_2(l,t))]/3 \quad . \end{aligned} \quad (4.35)$$

The time domain solutions of victim line for ramp input are (dependent on the input)：

Region I: $t_d > a_1$ and a_2

$$V_1(l,t) = a_1 m_1 + \frac{RC_{af} k_1 m_1}{3\sigma_1} e^{-t\sigma_1 / RC_{af}} \left[\left(\frac{2m_2}{m_1} - 1 \right) + \left(\alpha - \frac{2m_2}{m_1} \beta \right) \right]$$
$$+ \frac{2R(C_{af} + 3C_{ll}) k_2 m_1}{3\sigma_2} e^{-t\sigma_2 / R(C_{af} + 3C_{ll})} \left[-\left(\frac{m_2}{m_1} + 1 \right) + \gamma + \lambda \frac{m_2}{m_1} \right] .$$

(4. 36)

Region II: $a_1 < t_d < a_2$

$$V_1(l,t) = a_1 m_1 - \frac{2RC_{af} k_1 m_2}{3\sigma_1} + \frac{2R(C_{af} + 3C_{ll}) k_2 m_2}{3\sigma_2}$$
$$+ \frac{RC_{af} k_1 m_1}{3\sigma_1} e^{-t\sigma_1 / RC_{af}} \left[\left(\frac{2m_2}{m_1} - 1 \right) + \alpha \right]$$
$$+ \frac{2R(C_{af} + 3C_{ll}) k_2 m_1}{3\sigma_2} e^{-t\sigma_2 / R(C_{af} + 3C_{ll})} \left[\gamma - \frac{m_2}{m_1} - 1 \right] .$$

(4. 37)

Region III: $a_2 < t_d < a_1$

$$V_1(l,t) = m_1 t + \frac{RC_{af} k_1 m_1}{3\sigma_1} + \frac{2R(C_{af} + 3C_{ll}) k_2 m_1}{3\sigma_2}$$
$$+ \frac{RC_{af} k_1 m_1}{3\sigma_1} e^{-t\sigma_1 / RC_{af}} \left[\frac{2m_2}{m_1} - 1 - \frac{2m_2}{m_1} \beta \right]$$
$$+ \frac{2R(C_{af} + 3C_{ll}) k_2 m_1}{3\sigma_2} e^{-t\sigma_2 / R(C_{af} + 3C_{ll})} \left[-\left(\frac{m_2}{m_1} + 1 \right) + \lambda \frac{m_2}{m_1} \right] .$$

(4. 38)

Region IV: $t_d < a_1$ and a_2

$$V_1(l,t) = m_1 t - \frac{2RC_{af}k_1m_2}{3\sigma_1} + \frac{RC_{af}k_1m_1}{3\sigma_1} + \frac{2R(C_{af}+3C_{ll})(m_1+m_2)k_2m_2}{3\sigma_2}$$
$$+ \frac{RC_{af}k_1m_1}{3\sigma_1} e^{-t\sigma_1/RC_{af}} \left[\frac{2m_2}{m_1} - 1\right]$$
$$+ \frac{2R(C_{af}+3C_{ll})k_2m_1}{3\sigma_2} e^{-t\sigma_2/R(C_{af}+3C_{ll})} \left[-\frac{m_2}{m_1} - 1\right],$$

(4. 39)

where $\alpha = e^{a_1\sigma_1/RC_{af}}$, $\beta = e^{a_2\sigma_1/RC_{af}}$, $\gamma = e^{a_1\sigma_2/R(C_{af}+3C_{ll})}$ and $\lambda = e^{a_2\sigma_2/R(C_{af}+3C_{ll})}$. t_d is the delay time of the wire.

To solve eq. (4.36) explicitly, we set

$$\chi = \exp\left(-t\sigma_1/RC_{af}\right) \tag{4. 40}$$

and

$$\eta = C_{af}/\left(C_{af}+3C_{ll}\right)\left(\sigma_2/\sigma_1\right). \tag{4. 41}$$

Then, eq. (4.36) can be rewritten as

$$\frac{2R\left(C_{af}+3C_{ll}\right)k_2m_1}{3\sigma_2}\left[-\left(\frac{m_2}{m_1}+1\right)+\gamma+\lambda\frac{m_2}{m_1}\right]\chi^{\eta}$$
$$+\frac{RC_{af}k_1m_1}{3\sigma_1}\left[\left(\frac{2m_2}{m_1}-1\right)+\left(\alpha-\frac{2m_2}{m_1}\beta\right)\right]\chi+\left(a_1m_1-V_1(l,t)\right)=0.$$

(4. 42)

For simplicity of derivation, we set

$$A = \frac{2R\left(C_{af} + 3C_{ll}\right)k_2 m_1}{3\sigma_2}\left[-\left(\frac{m_2}{m_1}+1\right)+\gamma+\lambda\frac{m_2}{m_1}\right], \tag{4. 43}$$

$$B = \frac{RC_{af}k_1 m_1}{3\sigma_1}\left[\left(\frac{2m_2}{m_1}-1\right)+\left(\alpha-\frac{2m_2}{m_1}\beta\right)\right], \tag{4. 44}$$

$$P = a_1 m_1 - V_x\,. \tag{4. 45}$$

V_x in eq. (4.45) is the delay time threshold voltage.

Then, replacing symbols A, B and P in eq. (4.42) gives

$$\chi = \left(-\frac{P}{A}\right)^{1/\eta}\left(1+\frac{B}{P}\chi\right)^{1/\eta}. \tag{4. 46}$$

From the theory of Elmore [4.22], the 50% threshold delay time in the case of normal operation (middle line is active while outer lines are grounded), $t_{d,50\%}$, can be approximated as $t_{d,50\%}=R(C_{af}+2C_{ll})$. On the other hand, the 90% threshold crosstalk-induced delay time, $t_{d,90\%}$, is always greater than $t_{d,50\%}$, whence $t_{d,90\%} > R(C_{af}+2C_{ll}) > RC_{af}$. Then, from eqs. (4.40) and (4.41), $0<\chi<1$ and $0<\eta<1$ for 90% threshold delay calculation. In the range of interest, it follows easily from eqs.(4.44) and (4.45) that $0<\frac{B}{P}\chi<1$.

We find that the first-order approximation of eq. (4.46) is sufficient to obtain the accurate solution of interest. Then, the term $(1+\chi B/P)^{1/\eta}$ on the right-hand side of eq. (4.46) can be approximated with sufficient accuracy by a first-order polynomial using

Taylor's expansion, i.e.,

$$\chi = \left(-\frac{P}{A}\right)^{1/\eta}\left(1+\frac{1}{\eta}\frac{B}{P}\chi\right). \tag{4. 47}$$

Solving x in eq.(4.47) and combining with eq.(4.44), we obtain the crosstalk-enhanced delay time for victim line, denoted by $t_{d,x}$:

$$t_{d,x} = \frac{1}{\sigma_1}\left[RC_{af} * \ln(\zeta)\right], \tag{4. 48}$$

where $\zeta = (-A/P)^{1/\eta} - B/P/\eta$.

Approximation of the right-hand side of eq.(4.46) by a polynomial of order two using Taylor's expansion generally provides better accuracy. However, the first-order polynomial approximation in the parameter values of our interest already provides sufficient accuracy.

Solutions of region II, eq.(4.47), can be obtained from similar procedures to those of eq.(4.48) by replacement of $A = 2R(C_{af}+3C_{ll})k_2 m_1[\gamma - m_2/m_1 - 1]/3\sigma_2$, $B = RC_{af}k_1 m_1[(2m_2/m_1 - 1)+\alpha]/3\sigma_1$, and $P = a_1 m_1 - 2RC_{af}k_1 m_2/3\sigma_1 + 2R(C_{af}+3C_{ll})k_2 m_2/3\sigma_2 - V_x$. The solution of regions III and IV, eqs. (4.48) and (4.49), can be obtained numerically.

To verify the validity of the above solutions, SPICE simulation for various input signals and driving and driven conditions is given. We divide the distributed interconnect into 20 lumped sections in SPICE simulation. The accuracy of the crosstalk-induced delay time deterioration model is demonstrated in Figs. 2-4. First,

we investigate the waveforms at the end terminal of the victim line. Analytical and numerical solutions of the equations in regions I to IV are shown in Figs. 2(a) and 2(b). The output waveforms of SPICE simulation for the given inputs are plotted on these figures. The curves of the models overlapped with the curves of SPICE simulation. The undershoot signal on victim line in region IV of Fig. 2(a) is due to the negative coupled noise from the aggressor line's fast falling voltages. The extra negative coupled noise that clamps the rising voltage of the victim line is shown in region II of Fig. 2(b). The non-monotonic responses are well formulated using our models. The new models show excellent accuracy in all regions.

Figure 3 shows the 90% threshold delay time for victim and aggressor lines that switch out of phase simultaneously. Here we assume that the 90% threshold delay time is always longer than the rise and fall times of the input signal. Then, the delay time of the victim can be calculated from the time domain solution of region I. Equation (4.48) gives the closed-form solution of the delay time. The analytical model gives an accurate prediction to the SPICE simulation for various driver and loading sizes. The input-rise-time-dependent delay time is simulated well especially for small R_T and C_T where interconnects dominate the overall delay time, and is well modeled in this study.

The aggressor input waveform can be stretched ($a_1 \neq a_2$) and staggered ($b_1 \neq b_2$) because of signal transmission on the interconnect. Figure 4 demonstrates the delay time deterioration due to the stretched signal on the aggressor net. Signal delay uncertainties due to nearby switching signals are observed. The delay time increases significantly because extra noise on the victim line is coupled from aggressors and it takes more time for the victim line to reach the 90% threshold. The extra delay time is due to the non-monotonic coupling noise of the aggressor signal such that it causes a non-monotonic response on the victim net during non-simultaneous switching. These

phenomena can be verified in Figs. 2(a) and 2(b). The results above reveal that it may not be accurate to take the worst-case delay time as the case that victim and aggressor lines switch simultaneously. On the other hand, it is observed that the delay time becomes even shorter than in the simultaneously switching case (shown in Fig. 4 by a dotted line) for long aggressor rise time. Because the rise time on the aggressor line is longer than the delay time on the victim line, the coupling signal has little effect on the monotonic response on the victim line. Moreover, because of the slow transition of the aggressor, the effective coupling capacitance of the non-simultaneously switching case becomes smaller ($|K|<1$ for the first-order approximation of the Miller effect) than that of the simultaneously switching case ($|K|=1$) and the delay time become shorter. These delay uncertainties due to noise in Fig. 4 are calculated using the closed-form solutions of regions I and II, which show very high accuracy compared to SPICE simulations.

4-5 Worst Crosstalk Modelings

The demand for higher performance is translated to the requirement for higher clock frequency with much faster switching signals. The faster a signal switches, the more noise is coupled onto the neighboring lines. The worst-case crosstalk occurs when all aggressors switch as a step waveform at the same time and in the same direction so their noise peaks align. However, the step input situation may never actually occur due to signal transition. Thus, the input-waveform-dependent worst crosstalk model is important to consider in order to avoid the overestimation of crosstalk effects.

Here we denote the ramp input signal on the aggressor lines as V_{r2}':

$$V_{r2}'(0,t) = U(t-b_2)m_2(t-b_2) - U(t-b_2-a_2)m_2(t-b_2-a_2), \quad (4.49)$$

where a_2 and b_2 represent the rise time and the arrival time of input signal, respectively, as shown in Fig. 1(b). The slope of the input signal is written as m_2 and is the fraction of VDD and a_2. *U(t)* represents the unit step function of t.

Figure 1(b) depicts the worst case of crosstalk noise. In the derivation of the crosstalk noise model, boundary conditions can be written as

$$-I_1(0,t)R_t = V_1(0,t) \quad (4.50)$$

$$V_{r2}'(0,t) - I_2(0,t)R = V_2(0,t). \quad (4.51)$$

Careful observations, it is found that these new boundary conditions are those of the special case discussed in the previous section with $V_{r1}(0,t)$=0 in eqs.(5) and (6).

The new boundary conditions for the coupled interconnect are calculated from eqs. (4.50) and (4.51) and are

$$2V_{r2}'(0,t) - I_+(0,t) = V_+(0,t) \quad (4.52)$$

$$-V_{r2}'(0,t) - I_-(0,t) = V_-(0,t), \quad (4.53)$$

where $V_+(0,t) = V_1'(0,t) + 2V_2'(0,t)$, $V_-(0,t) = V_1'(0,t) - V_2'(0,t)$, $I_+(0,t) = I_1'(0,t) + 2I_2'(0,t)$, and $I_-(0,t) = I_1'(0,t) - I_2'(0,t)$. From these boundary conditions, eqs. (4.52) and (4.53), the coupled system can be solved from the solution of a single isolated line by the replacement of total capacitance with C_{af} and $C_{af}+3C_{ll}$ for the input as $2V_{r2}'(0,t)$ and

$-V_{r2}'(0,t)$. The crosstalk-induced voltage on the end of the victim line, which is calculated from the time-domain solutions of $V_+(t,l)$ and $V_-(t,l)$, is given by

$$V_1(t,l) = (V_+(t,l) + 2V_-(t,l))/3. \tag{4.54}$$

The time to reach the worst (max) peak crosstalk voltage on the adjacent net, denoted by $t_{p,max}$, for a specified input can be obtained by solving $dV_1(t,l)/dt=0$ in eq. (4.54). Calculations give

$$t_{p,\max} = -\frac{RC_{af}}{\sigma_1}\ln(\zeta_2), \tag{4.55}$$

where $\zeta_2 = ((1-\beta)k_1/(1-\lambda)/k_2)^{1/(\eta-1)}$. The definitions of β, λ, η, k_1, k_2, and σ_1 can be found in the previous section.

Then, the worst (max) crosstalk voltage, $V_{p,max}$, is obtained from eq.(4.54) with the replacement of $t=t_{p,max}$, i.e.,

$$\frac{V_{p,\max}}{V_{dd}} = \frac{2}{3}\frac{R}{a_2}\left\{\frac{(\beta-1)C_{af}k_1\zeta_2}{\sigma_1} - \frac{(\lambda-1)(C_{af}+3C_{ll})k_2\zeta_2{}^{\eta}}{\sigma_2}\right\}. \tag{4.56}$$

Verification of these models is carried out by SPICE simulation and the results are shown in Fig. 5. First, this figure shows that the faster a signal switches, the more noise is coupled onto neighboring lines.However, the coupling noise becomes insignificant under large loading conditions because of the slow signal transition. Second, crosstalk can be reduced by adjusting the magnitude of the driver resistance and the loading capacitance. For slow ramp input, however, crosstalk noise can be

reduced under small loading conditions; this should be carefully considered for the signal integrity problem in circuit design. All phenomena are well modeled and formulated in this paper.

4-6 Interconnect Models Considering Inductance Effects

A new set of delay time and overshoot voltage models, considering the distributed resistance, capacitance and inductance of the interconnect are presented for step and ramp input signals. These models are consistent with SPICE simulations over a wide range of input parameters; they are therefore helpful in predicting the integrity of an interconnect signal at a high confidence level. This work also proposes new guidelines for evaluating the influence of inductance on the simulated performance of an interconnect, considering both the driving and the loading conditions. These new rules are regarded as helpful to chip designers who employ advanced technology in realizing an optimized design methodology and flow which incorporates the effect of on-chip inductance in real silicon.

The increasing operating frequency and die sizes of advanced chips are such that the signal voltage transition from low-to-high or high-to-low can no longer be treated as purely digital. Electrical parameters such as output delay time and overshoot voltage are now crucial to characterize the high-frequency signal. Accordingly, signal-integrity concerns must be raised in the verification stage in high-end chip design flow. Increasing the operating frequency increases the impedance associated with the inductance. Additionally, reducing the resistance of the wire using a cooper interconnect magnifies the effect of inductance on wire performance at high frequency because of the series connection characteristics of resistance and inductance. Models that incorporate the effects of inductance are important in accurately calculating the interconnect performance in an analysis of the integrity of the signal.

In delay and crosstalk modeling, Sakurai [4.7] derived solutions to the partial differential equation of a single isolated line and a coupled line, assuming a step input waveform. In previous section, we investigated the modeling of delay time and crosstalk by considering the ramp input under various driving and loading conditions. However, these aforementioned studies did not discuss the effects inductance on the calculated delay time, which are shown later in this work to be very important. Cases [4.16] addressed the transient response of single RLC transmission lines but did not derive a closed-form solution. Davis [4.17], [4.18] provided the closed-form solution for coupled RLC transmission lines but he assumed a step input, infinitely long line and open loading. Cao et al. [4.23] found the closed-form solution based on empirical assumptions.

Obtaining a convergent solution for netlists that include inductance is computationally intensive, especially for advanced SOCs, which have very many nets. A designer must neither overlook nor be over-conservative in considering the effect of inductance on real silicon. The best method is to screen out the critical nets on which inductance has a real impact on the electrical performance, from the interconnect sea. The figure of merit and methods of characterizing the effect of the on-chip inductance of wires have been discussed [4.24], [4.25]. However, comprehensive criteria must be applied to achieve a reliable screening flow. The final section of this work will introduce the newly developed criteria, which incorporate the driving and loading strength of the wire, as well as the wire length effect.

4.6.1 ANALYTICAL MODELING OF RLC TRANSMISSION LINE

Figure 4.14 schematically depicts a single interconnect driven by a resistance, R_S, and terminated at a load capacitance, C_L. The interconnect itself is modeled as distributed capacitances (c), inductances (l) and resistances (r). According to the

theory of transmission lines [4.19], the electrical behavior of a single line system in Fig. 1 may be described by the PDE,

$$\frac{\partial^2 V(x,t)}{\partial x^2} = rc\frac{\partial V(x,t)}{\partial t} + lc\frac{\partial^2 V(x,t)}{\partial t^2}, \tag{4. 57}$$

where r, l and c represent the line resistance, the line inductance and line-to-ground capacitance per unit length, respectively. *V(x,t)* represents the signal at any position *x* on the line at time *t*.

The transfer function of the wire in s-domain can be derived from PDE (4.57) as follows. (See Appendix A for details.)

$$H(s) = \frac{V(l,s)}{V(0,s)} = \frac{1}{(1+sC_L R_S)\cos\sqrt{-(R+sL)sC} + (R_S\sqrt{\frac{-sC}{R+sL}} + sC_L\sqrt{-\frac{R+sL}{sC}})\sin\sqrt{-(R+sL)sC}} \tag{4. 58}$$

R, L and C represent the lumped line resistance, the inductance and the line-to-ground capacitance, respectively, and are given by $R = r*z$, $L = l*z$ and $C = c*z$, where z is the length of the line. The nonlinear characteristics of the CMOS device are simplified as if the device were linear. Then, the CMOS gate is modeled as a resistance (R_S) at the driving port and a capacitance (C_L) at a driven port.

In this work, a two-step procedure is used to solve the single line PDE. Initially, Eq. (4.58) is approximated by the Heaviside expansion. Then, this approximation is further simplified as a rational polynomial using the two-pole approximation method. These procedures are proven to yield an accurate analytical solution that is proven in the SPICE simulation in a later section.

To calculate the poles of the transfer function, Eq. (4.58) is rewritten as a

function of s',

$$H(s') = \frac{1}{(1 - s'C_T R_T)\cos\sqrt{s'} + (R_T + C_T)\sqrt{s'}\sin\sqrt{s'}} \quad , \tag{4. 59}$$

where $s' = -(R + sL)sC$, $R_T = R_S/(R + sL)$ and $C_T = C_L / C$.

Then, the transfer function of the RLC wire in terms of s is calculated using the Heaviside expansion and simplified as

$$H'(s) = 1 + \frac{sk}{s + \sigma/\left[(R + sL)sC\right]} \quad . \tag{4. 60}$$

where

$$k = -1.01\frac{R_T + C_T + 1}{R_T + C_T + \pi/4}, \tag{4. 61}$$

$$\sigma = \frac{1.04}{R_T C_T + R_T + C_T + (2/\pi)^2} \quad . \tag{4. 62}$$

Appendix E explains the details of the derivation of the transfer function, (4.60). The transfer function $H'(s)$, (4.60), can be expanded and expressed in general as

$$H''(s) = \frac{p_0 + p_1 s + p_2 s^2 + \ldots + p_n s^n}{q_0 + q_1 s + q_2 s^2 + \ldots + q_n s^n} \quad . \tag{4. 63}$$

The two poles approximation is applied here to simplify (4.63) further. Hence, $H''(s)$ is approximated as $H(s)$ and written as

$$H(s) = \frac{a_0}{b_0 + b_1 s + b_2 s^2} \quad . \tag{4. 64}$$

The coefficients of the transfer function, b_1 and b_2, in (4.64) are determined from the moments of $H(s)$ as

$$M_0 = H(s)\big|_{s=0} = \frac{a_0}{b_0}, \tag{4. 65}$$

$$M_1 = -\frac{\partial H(s)}{\partial s}\bigg|_{s=0} = b_1, \tag{4. 66}$$

$$M_2 = \frac{1}{2!}\frac{\partial^2 H(s)}{\partial s^2}\bigg|_{s=0} = b_1^2 - b_2. \tag{4. 67}$$

M_0, M_1 and M_2 are the moments of the transfer function $H(s)$.

Similar procedures are performed for (4.60) to yield the moments of $H'(s)$. Hence, the moments of the transfer function $H'(s)$ - M'_0, M'_1 and M'_2 - are calculated as

$$M'_0 = H'(s)\big|_{s=0} = 1, \tag{4. 68}$$

$$M'_1 = -\frac{\partial H'(s)}{\partial s}\bigg|_{s=0} = \gamma RC, \tag{4. 69}$$

$$M'_2 = \frac{1}{2!}\frac{\partial^2 H'(s)}{\partial s^2}\bigg|_{s=0} = \frac{C\left[\alpha L + \beta R^2 C\right]}{\pi^4 (4m + 4n + \pi)^2} \quad , \tag{4. 70}$$

where $m = C_T / C$, $n = R_T / R$,

$\gamma = 1.24\left[\left(\frac{2}{\pi}\right)^2 + m^2(1+n) + n(1.41+n) + m(1.41 + n(3+n))\right] / \left(1 + \frac{4}{\pi}(m+n)\right)$,

$\alpha = -1513.6\left[m^3 + 2m^2(1.1+n) + m(1.51 + 2.8n + 1.21n^2) + 0.8n + 0.62n^2 + 0.32\right]$

and

$$\beta = 189 + 1353.5\begin{pmatrix}(m+n)+0.4\left(m^2+n^2\right)+2.6(m+n)^3+\left(m^4+n^4\right)+5.43mn+10.8\left(m^2n+mn^2\right)\\+8.4\left(m^3n+mn^3\right)+2\left(m^2n+n^2\right)\left(mn^2+m^2\right)+15.55m^2n^2+\left(m^2n^4+m^4n^2\right)\end{pmatrix}.$$

For the case of $R_S = C_L = 0$, that is $m = n = 0$, the parameters in (4.69) and (4.70) is calculated as $\gamma = 0.5$, $\alpha = -481.8$, $\beta = 187.8$. Accordingly, $M_1' = 0.5RC$ and $M_2' = C\left(-481.8L + 187.8R^2C\right)/\pi^6$.

It is a means to an end of this work to approximate the transfer function, (4.60) as a rational polynomial , (4.64), by equalizing the moments of the two transfer functions, $H(s)$ and $H'(s)$.

Hence, the coefficients b_0, b_1 and b_2 in (8) are calculated by equalizing the corresponding pairs of moments; that is, $M_0 = M_0'$, $M_1 = M_1'$ and $M_2 = M_2'$. A comparison of (4.65) and (4.68) yield the simplest result $a_0 = b_0 = 1$ by intuition. b_1 and b_2 are given by

$$b_1 = M_1', \tag{4. 71}$$

and

$$b_2 = (M_1'^2 - M_2'). \tag{4. 72}$$

After b_1 and b_2 are known, the two poles (σ_1 and σ_2) of the transfer function are derived as

$$H(s) = \frac{1}{1 + b_1 s + b_2 s^2} = \frac{1}{b_2}\frac{1}{(s-\sigma_1)(s-\sigma_2)}\ , \tag{4. 73}$$

and the poles are given by

$$\sigma_{1,2} = \frac{-b_1 \pm \sqrt{b_1^2 - 4b_2}}{2b_2}\ . \tag{4. 74}$$

A comprehensive study for two different input signals, step and ramp, are discussed separately below.

A. Step Input

Then, given a step input ($V(0,s)=V_{dd}/s$) fed into the start-end of the wire, the response at the end of the line is $V(z,s)=V(0,s)H(s)$. Hence, the output response to the step input is

$$\frac{V(z,s)}{V_{dd}}=\frac{1}{s}H(s)=\frac{1}{s}+\frac{\sigma_2}{\sigma_1-\sigma_2}\frac{1}{s-\sigma_1}-\frac{\sigma_1}{\sigma_1-\sigma_2}\frac{1}{s-\sigma_2} \quad . \tag{4. 75}$$

Then, the time domain solution is obtained by taking the inverse Laplace transform of (4.75)

$$\frac{V_0(l,t)}{V_{dd}}=1+\frac{\sigma_2}{\sigma_1-\sigma_2}e^{\sigma_1 t}-\frac{\sigma_1}{\sigma_1-\sigma_2}e^{\sigma_2 t} \quad . \tag{4. 76}$$

Set $x=e^{\sigma_1 t}$, (4.76) is then transferred into

$$(\sigma_1-\sigma_2)(\frac{V_0(l,t)}{V_{dd}}-1)=\sigma_2 x-\sigma_1 x^{\sigma_2/\sigma_1} . \tag{4. 77}$$

Since $\sigma_2<\sigma_1$, so (4.77) can be rewritten as

$$\left(\sigma_2-\frac{\sigma_2}{\sigma_1}\right)x-\sigma_1-(\sigma_1-\sigma_2)\left(\frac{V_0(l,t)}{V_{dd}}-1\right)=0 \quad . \tag{4. 78}$$

The delay time (t_d) for the output voltage to increase to χ % of V_{dd} is determined by setting $V_0(l,t_d)=\chi V_{dd}$.

Hence, the delay time (t_d) is calculated as

$$t_d=\sigma_1 \ln\left[\frac{\sigma_1+(\sigma_1-\sigma_2)(\chi-1)}{\sigma_2-\sigma_2/\sigma_1}\right]. \qquad (4.79)$$

B. Ramp Input

For a ramp input signal fed into the beginning of the line, it can be expressed in the s-domain as

$$V(0,s)=\frac{m}{s^2}+\frac{ame^{-as}}{s}-\frac{m(1+as)e^{-as}}{s^2}, \qquad (4.80)$$

where *m* represents the slope of the ramp waveform and *a* is the input ramp rate. The relationship between *m* and *a* is $m=V_{dd}/a$. Hence, the output waveform at the end of the wire can be derived by combining (4.80) with the RLC transfer function to yield,

$$V_0(l,s)=V_{in}(0,s)H(s). \qquad (4.81)$$

Then, the output waveform at the end of the line is given by

$$V_0(l,t)=m\left[\frac{\sigma_1^2\left(1-e^{\sigma_2 t}\right)-\sigma_2^2\left(1-e^{\sigma_1 t}\right)}{b_2\sigma_1^2\sigma_2^2(\sigma_1-\sigma_2)}+t\right] \qquad \text{for t < a,}$$

(4.82)

$$V_0(l,t) = m\left[\frac{\sigma_1^2\left(e^{\sigma_2(t-a)} - e^{\sigma_2 t}\right) - \sigma_2^2\left(e^{\sigma_1(t-a)} - e^{\sigma_1 t}\right)}{b_2\sigma_1^2\sigma_2^2(\sigma_1 - \sigma_2)} + a\right] \qquad \text{for t > a.}$$

(4. 83)

When $t >> a$, the solution to (4.83) approaches V_{dd}, meaning that the output signal becomes stable at V_{dd} for a particular period. For $t=a$, the solutions to (4.82) and (4.83) are the same. Hence, a smoothing function is applied to smooth the two functions. It is given by

$$t_{eff} = a - 0.5\left((a-t-\Delta) + \sqrt{(a-t-\Delta)^2 + 4\Delta a}\right). \qquad (4.\ 84)$$

Here, t_{eff} approaches t when t is small and approaches a when t exceeds a. Hence, (4.82) and (4.83) can be combined as

$$V_0(l,t) = m\left[\frac{\sigma_1^2\left(e^{\sigma_2(t-t_{eff})} - e^{\sigma_2 t}\right) - \sigma_2^2\left(e^{\sigma_1(t-t_{eff})} - e^{\sigma_1 t}\right)}{b_2\sigma_1^2\sigma_2^2(\sigma_1 - \sigma_2)} + t_{eff}\right]. \qquad (4.\ 85)$$

The delay time can be calculated following similar procedures as in the step input case, described in the preceding section. Hence, the 90% delay time is derived as

$$t_d = \frac{1}{\sigma_1}\ln(\xi), \qquad (4.\ 86)$$

where $\xi = (\chi - 1)a\dfrac{(\sigma_1/\sigma_2)\left(1 - e^{-a\sigma_2}\right) + (\sigma_1 - \sigma_2)}{(\sigma_2/\sigma_1)\left(1 - e^{-a\sigma_1}\right) - \left(1 - e^{-a\sigma_2}\right)}$ and $\chi = 0.9$.

4.6.2 Model verification

Figure 4.15 plots the waveforms obtained by the SPICE simulation and the analytical model at the end of the wire, driven by a ramp input. The delay time and the overshoot voltage, which indicate the interconnect performance, of these curves are compared. Careful observation of these curves reveals the following important information. Initially, the RLC analytical model discussed herein accurately predicts both the output delay and the maximum overshoot voltage, which are the most important parameters in evaluating the performance of the wire. Secondly, RC distributed networks cannot be used to predict accurately the 50% delay to which parasitic inductance contributes markedly. Intuitively, the delay predicted by RC is less than that predicted by RLC because inductance retards the driving current. The RC structure also cannot predict the overshoot, which is important in evaluating the time taken for the signal to become stable. The analytical models herein accurately predict the results of the simulation. That is, the RLC models presented in this study accurately predict important performance parameters such as the 50% and 90% delay times and the overshoot voltage of the interconnect ; however, the RC model cannot yield consistently accurate solutions for a wire that is significantly affected by inductance.

Parasitic inductance clearly influences the accuracy of the analysis of the interconnect performance, and hence the results of the chip simulation. However, designers must use extra computing resources to extract and simulate the effects of inductance. Fortunately, designers need not always include inductance effects in their simulations if they have idea when the inductance could be neglected. Therefore, a new developed rule of thumb that helps designers to develop method for determining whether to consider the effects of inductance will be introduced below.

Figure 4.16 compares the delay times in the RC and RLC and the corresponding percentage error at various input rising times. The RC wire model deviated markedly from the SPICE simulation without inductance, especially at small rise times.

The symbol t_{r_c} in this figure refers to the rule to be followed by the designer in determining whether inductance effects can be neglected. Studying the figure carefully, it is found that neglecting inductance may cause a significant error in the evaluation of performance if the input rise time is less than t_{r_c}. A later section of this study will discuss the calculation of t_{r_c} and apply it to this figure. Figure 4.17 compares RC and RLC at 90% delay and plots error percentage vs. input rise time. This figure implies that the RC and RLC models predict quite well the delay except in the case of the small rise time, for which RLC yields predictions that is more consistent with the SPICE simulations. Figures 4.16 and 4.17 also provide evidence that the prediction of the delay could be quite inaccurate if the rise time of the ramp input is not considered.

Figures 4.18 and 4.19 detail the loading conditions and further evidence that the RLC models herein yields results that are consistent with those of the SPICE simulations at 50% and 90% delays, given various input waveforms. Driving and loading significantly influence the delay time.

Figure 4.20 presents evidence that the RLC models herein yield results that are consistent with those of the SPICE simulation at 50% delay for various lengths of wire.

Figure 4.21 compares the results of the RC models at 50% delay with RLC SPICE simulation data, along with corresponding plots of error percentages against the length of the wire. Significant errors arise for short wires because the RC models ignore the effects of inductance. This figure again implies that the error in the RC model may be significant in certain cases in which inductance effects are crucial.

Another important parameter of the integrity of the signal in a single RLC wire is overshoot voltage, which cannot be modeled using an RC equivalent network. Figure 4.22 plots the RLC overshoot modeling accuracy versus length of wire. The overshoot voltage increases with the length of the wire for short wires; however, the voltage declines as the length increases over a particular value. This phenomenon will be further elucidated in the next section by defining the critical length, z_c, of the wire, by applying the criteria to determine the effect of inductance on the interconnects.

4.6.3 Criteria for Determining the Effects of Inductance on Interconnects

Inductance has been proven to affect performance, and so must not be overlooked by a designer. However, the overshoot/undershoot electrical behaviors of the RLC transmission line indicate that obtaining a convergent solution for a circuit model that includes inductance is computationally intensive. Hence, a designer should not be over-conservative about the effects of inductance in the deep-submicron circuit simulation. The best method is to develop a filtering methodology using the accurate criteria to screen-out the nets that are really affected by the inductance in the interconnect performance analysis.

If the poles of *H(s)* in (4.75) are complex, then the response of the circuit is under-damped. That is, the interconnect is R-L-C-like and the effect of inductance on the performance evaluation is critical. Otherwise, if the poles of *H(s)* are real, then the response of the circuit is over-damped, such that the wire is R-C like. The effect of inductance can then be neglected in the analysis of the performance of the interconnect.

However , the inductance is connected in series with the resistance, so the effect of the inductance must be compared to that of the resistance, to determine which dominates.

Therefore, this section proposes two criteria, which are applied as guidelines in elucidating the effect of inductance, derived from the analytical models and from concepts described above.

A. Criterion 1: Poles of the Interconnect Transfer Function Must Be Complex

The first step of this work is to analyze whether the poles like that in (4.73) are complex or real to identify whether the effects of inductance are important in the interconnect analysis. Hence, if the interconnect behavior is like that of the R-L-C network, then the poles in (4.73) are complex. Hence, using $b_1^2 - 4b_2 < 0$, the first criterion is

$$z < z_c , \tag{4. 87}$$

where $z_c = \frac{\kappa}{r^{2/3}} \left(\frac{l}{c} \right)^{1/3} z^{1/3}$ and $\kappa = \frac{4.4 + 1.06m + 0.53n}{1.08 + 1.93m + 2.91n + 0.83m * n}$.

Here, the range of wire lengths over which the interconnect exhibits significant inductance is defined in terms of a critical length, z_c. The effect of inductance is a function of the length of the wire because the RLC transmission line has some lossy effects. If the length (z) satisfies the criterion, then the effects of inductance are significant. When the length of the wire exceeds z_c , *RC* dominates the delay.

The RLC effect is greatest at small driving resistance and loading capacitance ($R_S = C_L = 0$).

If $R_S = C_L = 0$, accordingly m=n=0, then the critical length, z_c, can be reduced to

$$z_c = \frac{4.1}{r^{2/3}}\left(\frac{l}{c}\right)^{1/3} z^{1/3}. \quad (4.88)$$

However, if the operating frequency is not sufficiently high, then the inductance of the wire only slightly affects the performance of the interconnect. Hence, criterion 1 must incorporate the effect of the operating frequency, as defined in criterion 2, which will be considered below to complete the guidelines to be followed in understanding the effect of inductance.

B. Criterion 2: The Impedance Of On-Chip Inductance Is Greater Than Serial Connected Resistance

The impedance of inductance increases with frequency, so, the operating frequency must be sufficiently high that inductance has an effect when resistance and inductance are connected in series. Therefore, inductance is considered to dominate the serial connected impedance if the impedance of the inductance exceeds the resistance. That is,

$$2\pi f_c L > R. \quad (4.89)$$

where f_c is the significant frequency[10] , defined as $f_c = 0.34/t_r$, and is the highest frequency of interest that affects the interconnect performance analysis. Hence, (4.89) is re-arranged into

$$t_{r\_c} < 0.68\pi \frac{L}{R}. \quad (4.90)$$

t_{r_c} represents the rise time when the impedance of the inductance exceeds the resistance. That is to say, if the rise time of the simulated signal is less than t_{r_c}, then the inductance must be considered in the analysis of the interconnect performance.

Combining the critical wire length, z_c in (4.87), and rise time, t_{r_c} in Eq. (4.90) enables the designer to determine whether the inductance may be neglected in the performance simulation. Figure 4.23 summarizes the criteria for determining the effect of inductance; the shaded area is the inductance effect window, in which the effect of inductance is significant. The size of the inductance effect window is inversely proportional to the interconnect driving resistance and the loading capacitance.

Figures 4.16 and 4.17 apply the criteria discussed in this section. The length of the wire in the figure is less than z_c, so any input signal which has an input rise time of under t_{r_c} will have an inductance effect that is important in performance analysis. The dashed vertical line in these two figures represents the calculated t_{r_c}. These plots clearly imply that, when the rise time is less than t_{r_c}, failing to consider the effects of inductance in analyzing the delay will cause a large error.

Figure 4.21(c) shows another application of the criteria presented herein. The values of z_c that corresponds to various wire lengths and loads are indicated. The input rise time, which is 50ps in this plot, is less than the critical input rising time, t_{r_c}, and so satisfies the second criterion. Hence, according to criteria 1 and 2, the length of the wire (z), being less than z_c (ie. $z<z_c$), will cause significant inductance effects. The dashed line in Fig. 4.21(c) represents the condition $z=z_c$. Here, the area in which $z>z_c$ is denoted as Region I and the area in which $z<z_c$ is denoted as Region II. Therefore,

the effects of inductance must be considered for lines in Region II. However, the effects of inductance on lines in Region I can be ignored without generating an excessively large error when the RC model is used to evaluate the performance. Consider for example a wire that is 1000 μm long; three loading conditions yield a calculate z_c in Region II (R_t (C_t)=0, 0.5, 1), corresponding to significant errors in the RC model error plot in Fig. 4.21(b). Under the loading condition R_t (C_t)=1 , (diamond symbols in the plot), the corresponding error shown in Fig. 4.21(b) decreased as the interval (Fig. 4.21(c)) between z_c and the dashed line, where z=z_c, declined indicating the interconnect RC is like. This finding is strong evidence that the criteria presented herein are useful in determining whether the effect of inductance is significant. Figure 4.21(c) also provides evidence that the overshoot voltage is significant for wires with lengths that exceed the critical length in Region II. The overshoot voltages decline as the length of the wire decreases because the wire corresponds to z_c in Region 1 and so behaves more like an RC line.

Ismail [7] proposed two bounds, z'_{c1} and z'_{c2}, for defining the range of critical lengths z'_{c1} < critical length < z'_{c2}. Deustech [8] presented an upper critical length that was similar to that, z'_{c1}, in [7] , but developed further criteria that involved some empirical parameters, to elucidate driving and loading conditions. Figure 4.21 plots z'_{c1} and z'_{c2} for comparison with the new value, z_c, given herein. The values z'_{c1} and z'_{c2}, are independent of the length of the wire and driving and loading conditions. However, the new criterion reveals that the effect of parasitic inductance becomes weaker as the wire length increases for the same wire parameters r, l and c. This finding is evidenced by the RLC SPICE simulation and the error (%) plot in Figs. 4.21(a) and (b), respectively.

The critical net is defined as the interconnect in which inductance significantly influences the performance analysis. It should be analyzed using RLC transmission line. A complex SOC design project involves very many interconnects. However, verifying a full-chip design by including and simulating all inductances of all wires is impractical. Hence, a novel design and simulation method, based on the newly developed criteria, is recommended. The methodology is based on the idea of filtering out non-critical nets and focusing on nets whose inductance effects are important. This method increases the accuracy of verification without excessively increasing the computational burden of the simulation because only critical nets are treated as RLC wires.

Hence, the recommended first step of the new method is to perform full-chip geometry extraction to establish a basic database of interconnects on chips for parasitic calculation. Then, the critical path can be identified using the filter mechanism presented herein. This filtering mechanism is used to screen out and categorize critical/non-critical nets from the whole interconnect geometry database. The factors that influence the filtering mechanism are the driver and the loading size, the signal frequency, the wire geometry and the wire length. A chip designer can add parasitic inductances in series into the predetermined critical path and perform the RLC transmission line simulation. Using this recommended design flow, a designer can speed-up chip simulation without ignoring inductance that affects the performance of the circuit or being over-conservative.

General interconnect delay time models, considering RLC transmission line effects, are presented herein. These models are derived from the telegraph equation using two-step approximation functions. Models are validated over a wide range of wire lengths, signal ramp times, driving conditions and loading conditions. The new criteria and method for screening-out critical interconnects that the inductance

significantly affect the interconnect performance are developed and discussed comprehensively. These new criteria take into account all interconnect factors, such as wire length, signal ramp time, driving conditions and loading conditions. The screening rules are believed to be very helpful to advanced chip designers who want to design chips without overlooking effects of inductance on the interconnect, and without being too conservative.

4-7 Summary

Accurate closed-form models have been developed for various interconnect systems. The delay considering inductance effects are also discussed and the guideline to estimate the effect of the inductance is presented. The delay and crosstalk formulas allow for simple analytic prediction of interconnection performance for arbitrary interconnect dimensions. Our model is useful for VLSI design and process optimization.

Appendix A : One-Line System

From the transmission line theory, the PDE of the one-line system in Fig. 1(a) can be expressed as

$$\frac{1}{r}\frac{\partial^2 V(x,t)}{\partial x^2} = c_{eff}\frac{\partial V(x,t)}{\partial t}, \tag{A-1}$$

where r denotes the line resistance per unit length. c_{eff} represents the effective capacitance of the one-line system and is equal to c_{af}, which denotes line-to-ground capacitance. $V(x,t)$ denotes the signal on line.

Let $R=r*l$ and $C_{eff}=c_{eff}*l= c_{af}*l$, where l is the length of the line. Then, the output waveform at the end of the interconnect ($x=l$) in the frequency domain for ramp input is

$$V(l,s) = L\left\{1 - k\exp\left(-\sigma t / RC_{eff}\right)\right\} \times s \times L\left\{U(t)mt - U(t-a)m(t-a)\right\}, \tag{A-2}$$

where $\sigma = 1.04/\left(R_T + C_T + R_T * C_T + (2/\pi)^2\right)$, $k = -1.01(R_T + C_T + 1)/(R_T + C_T + \pi/4)$, $R_T = R_s / R$, and $C_T = C_L / C_{eff}$. R_s and C_L are the driver resistance and the loading capacitance, respectively. $U(t)mt - U(t-a)m(t-a)$ represents the ramping input signal, $U(t)$ denotes the step input, m denotes the slope of the ramp waveform, and a is the input ramping rate. The relationship between m and a is $m=V_{dd}/a$. $L\{-\}$ in eq. (A-2) represents the Laplace transform. The first term in eq. (A-2) is the solution of the step input in the case of the single line and the second and third terms represent the contributions of the step and ramp input, respectively.

Appendix B : Two-Line System

From the coupled interconnection circuit in Fig. 1(b), the differential equation can be constructed as:

$$\frac{1}{r}\frac{\partial^2 V_1(x,t)}{\partial x^2} = (c_{af} + c_{ll})\frac{\partial V_1(x,t)}{\partial t} - c_{ll}\frac{\partial V_2(x,t)}{\partial t} \quad \text{(B-1)}$$

$$\frac{1}{r}\frac{\partial^2 V_2(x,t)}{\partial x^2} = (c_{af} + c_{ll})\frac{\partial V_2(x,t)}{\partial t} - c_{ll}\frac{\partial V_1(x,t)}{\partial t} \quad \text{(B-2)}$$

,

where c_{af} , c_{ll} and r denote the line-to-ground capacitance, the line-to-line capacitance and the line resistance per unit wire length, respectively. $V_1(x,t)$ and $V_2(x,t)$ denote the signals on aggressor and victim lines, respectively.

Combining the differential equations (B-1) and (B-2), new PDEs are obtained as

$$\frac{1}{r}\frac{\partial^2 V_+(x,t)}{\partial x^2} = c_{eff}^{2a}\frac{\partial V_+(x,t)}{\partial t} \quad \text{(B-3)}$$

$$\frac{1}{r}\frac{\partial^2 V_-(x,t)}{\partial x^2} = c_{eff}^{2b}\frac{\partial V_-(x,t)}{\partial t} \quad \text{(B-4)}$$

,

where $V_+(x,t) = V_1(x,t) + V_2(x,t)$ and $V_-(x,t) = V_1(x,t) - V_2(x,t)$. $c_{eff}^{2a} = c_{af}$ and $c_{eff}^{2b} = (c_{af} + 2c_{ll})$ represent the effective capacitances of two combined differential equations. Clearly, the differential equations have a similar form to that of the one-line case (compare with eq. (A-1)). The solution of eqs. (B-3) and (B-4) at the end of the lines, $V_+(l,t)$ and $V_-(l,t)$, can be obtained by the same approach as the previous case. Then, from the observation of eqs. (A-1) and (A-2), the solutions of eqs. (B-3) and (B-4) at the end of the lines for the ramping input in the frequency domain are

$$V_+(l,s) = V_1(l,s) + V_2(l,s) = Laplace\{1 + \mathrm{k}_1 \exp(-\sigma_1 t / rc_{eff}^{2a} l^2)\} \times s \times Laplace\{U(t)mt - U(t-a)m(t-a)\} \quad \text{(B-5)}$$

$$V_-(l,s) = V_1(l,s) - V_2(l,s) = Laplace\{1 + \mathrm{k}_2 \exp(-\sigma_2 t / rc_{eff}^{2b} l^2)\} \times s \times Laplace\{U(t)mt - U(t-a)m(t-a)\} \quad \text{(B-6)}$$

where k_1, σ_1, R_{T1} and C_{T1} have the same forms as k, σ, R_T and C_T in the one-line case with the replacement of c_{eff} with c_{eff}^{2a}. k_2, σ_2, R_{T2} and C_{T2} have the same forms as k, σ, R_T and C_T in the one-line case with the replacement of c_{eff} with c_{eff}^{2b} in the two-line system.

Appendix C : Multiple Coupled Line System

Because of the symmetry of the induced crosstalk noise voltage on the two victim lines adjacent to the signal line [Fig. 1(c)], the derivation of delay time and crosstalk noise voltage can be realized by taking the three parallel coupled transmission lines as two non-symmetrical coupled transmission lines, as shown in Fig. 1(d). The coupled partial differential equations for interconnection in Fig. 1(d) are

$$\frac{1}{r}\frac{\partial^2 V_1(x,t)}{\partial x^2} = (c_{af} + 2c_{ll})\frac{\partial V_1(x,t)}{\partial t} - 2c_{ll}\frac{\partial V_2(x,t)}{\partial t} \quad \text{(C-1)}$$

$$\frac{1}{\frac{1}{2}r}\frac{\partial^2 V_2(x,t)}{\partial x^2} = (2c_{af} + 2c_{ll})\frac{\partial V_2(x,t)}{\partial t} - 2c_{ll}\frac{\partial V_1(x,t)}{\partial t} \quad \text{(C-2)}$$

.

For the calculation of the PDEs above, two new differential equations are obtained by the calculation of (C-1)+(C-2) and (C-1)−(C-2)/2. Then, the two new differential equations are shown as

$$\frac{1}{r}\frac{\partial^2 V_+(x,t)}{\partial x^2} = c_{eff}^{3a}\frac{\partial V_+(x,t)}{\partial t} \quad \text{(C-3)}$$

$$\frac{1}{r}\frac{\partial^2 V_-(x,t)}{\partial x^2} = C_{eff}^{3b}\frac{\partial V_-(x,t)}{\partial t} \quad \text{(C-4)}$$

,

where $V_+(x,t) = V_1(x,t) + 2V_2(x,t)$ and $V_-(x,t) = V_1(x,t) - V_2(x,t)$. $c_{eff}^{3a} = c_{af}$ and $c_{eff}^{3b} = (c_{af} + 3c_{ll})$ represent the effective capacitances of two combined differential equations in the multiple coupled line system.

By comparing the PDEs of the coupled-line case, eqs. (C-3) and (C-4), with the PDE of the single-line case, eq. (A-1), it is found that the forms of these equations are

similar. Then, following procedures similar to those for the two-line system, the output waveforms at the end of the lines for the ramping input in the s-domain are

$$V_+(l,s) = V_1(l,s) + 2V_2(l,s) = Laplace\{1 + \mathrm{k}_1 \exp(-\sigma_1 t / rc_{eff}^{3a} l^2)\} \times s \times Laplace\{U(t)mt - U(t-a)m(t-a)\} \quad \text{(C-5)}$$

$$V_-(l,s) = V_1(l,s) - V_2(l,s) = Laplace\{1 + \mathrm{k}_2 \exp(-\sigma_2 t / rc_{eff}^{3b} l^2)\} \times s \times Laplace\{U(t)mt - U(t-a)m(t-a)\} \quad \text{(C-6)}$$

where k_1, σ_1, R_{T1} and C_{T1} have the same forms as k, σ, R_T and C_T in the one-line case with the replacement of c_{eff} with c_{eff}^{3a}. k_2, σ_2, R_{T2} and C_{T2} have the same forms as k, σ, R_T and C_T in the one-line case with the replacement of c_{eff} with c_{eff}^{3b} in the three-line system.

Appendix D : The Transfer Function of RLC Wire

For a distributed R-L-C wire, the relationship between current and voltage on the two ends of wire could be described as

$$\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix} = \begin{bmatrix} 1 & R_S \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cosh(ng) & Z_0 \sinh(ng) \\ Z_0^{-1} \sinh(ng) & \cosh(ng) \end{bmatrix} \begin{bmatrix} V(z,s) \\ I(z,s) \end{bmatrix} , \quad \text{(D-1)}$$

$$I(z,s) = sC_L V(z,s), \quad \text{(D-2)}$$

where $Z_0 = \sqrt{\frac{R+sL}{sC}}$. For distributed R-L-C wire, $n \to \infty$; hence, $ng = sC(R+sL)$. $V(0,s)$ and $I(0,s)$ are the voltage and current at driving port and $V(z,s)$ and $I(z,s)$ are the voltage and current at the end-point of wire.

Hence, the transfer function $H(s)$ of the wire with driver resistance and loading capacitance are derived from (A-1) & (A-2) as

$$H(s) = \frac{V(z,s)}{V(0,s)} = \frac{1}{(1+sC_L R_S)\cos\sqrt{-(R+sL)sC} + (R_S\sqrt{\frac{-sC}{R+sL}} + sC_L\sqrt{-\frac{R+sL}{sC}})\sin\sqrt{-(R+sL)sC}} . \quad \text{(D-3)}$$

Appendix E : Transfer Function Approximation

The initial step to perform the inversion of the Laplace transformation for a complex function as (3) is to split the function into the summation of smaller polynomials from the poles of the complex function. Heaviside's method is the method that could systematically perform the partial fraction expansion. Even though the poles of (3) are infinite, the first pole is usually dominant. Hence, only the first pole will be used for the transfer function approximation. Hence, the voltage at the end of line, $V(z,s')$, could be calculated from the Heaviside's method using first pole approximation for step input signal, $V(0,s')=1/s'$, and written as

$$V(z,s')=V(0,s')H(s')=\frac{1}{s'}+\frac{k}{s'-\sigma}, \tag{E-1}$$

where σ is the first pole of (3) and is calculated from the solution of $\tan\sqrt{s'}=\frac{1-R_TC_Ts'}{(R_T+C_T)\sqrt{s'}}$ where $R_T=R_S/(R+sL)$ and $C_T=C_L/C$.

k in (B-1) is correlated to σ and calculated from the Heaviside's expansion formula.

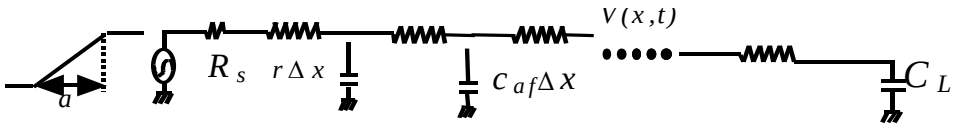
The method to calculate the closed-form solutions of k and σ is analogy to the method as R-C element constructed interconnect [1] and derived to be

$$k=-1.01\frac{R_T+C_T+1}{R_T+C_T+\pi/4}, \tag{E-2}$$

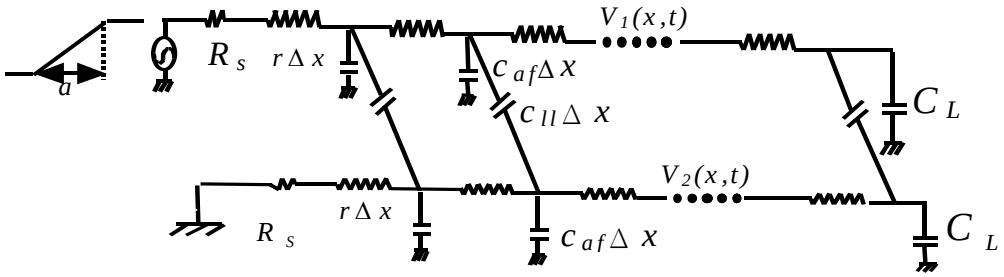
$$\sigma=\frac{1.04}{R_TC_T+R_T+C_T+(2/\pi)^2}. \tag{E-3}$$

After the simple arithmetic, the transfer function in s-domain, $H'(s)$, is calculated as

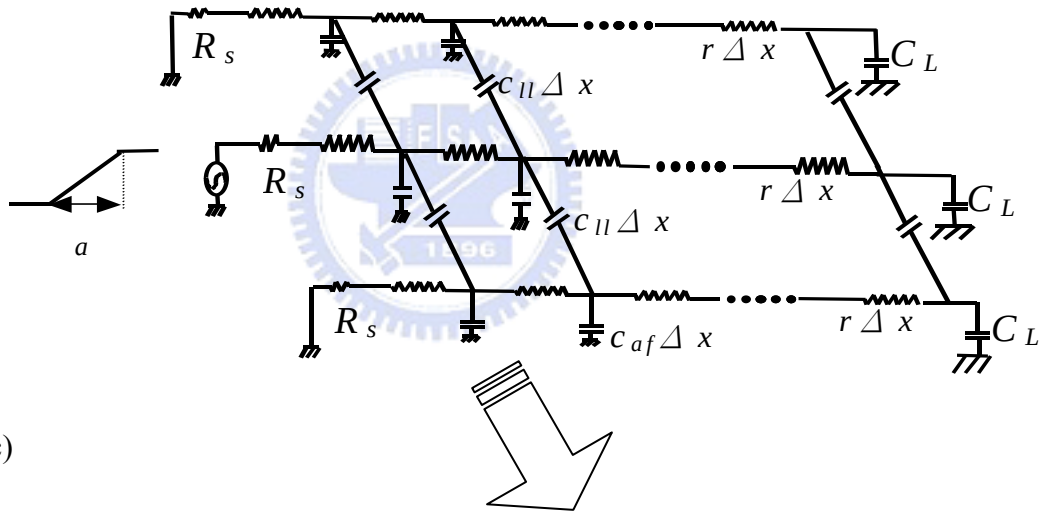
$$H'(s) = s'(\frac{1}{s'} + \frac{k}{s' - \sigma}) = 1 + \frac{sk}{s + \sigma/[(R + sL)sC]} \quad . \tag{E-4}$$



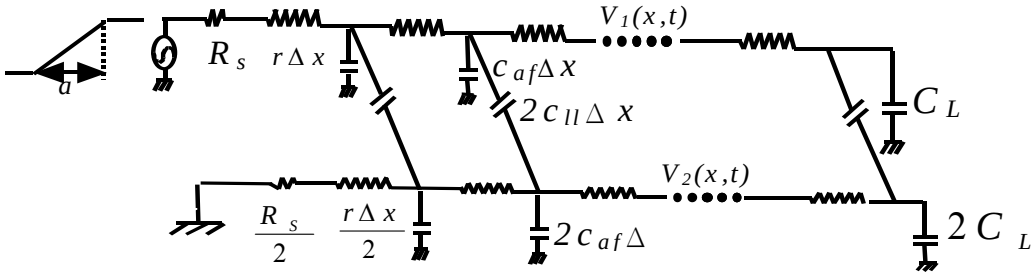
(a)



(b)



(c)



(d)

Figure 4. 1 (a) Schematic diagram of isolated one-line system. (b) Schematic diagram of two coupled lines. (c) Schematic diagram of three coupled lines. (d) The symmetry of the interconnection structure in (c) can be represented by the asymmetric interconnection.

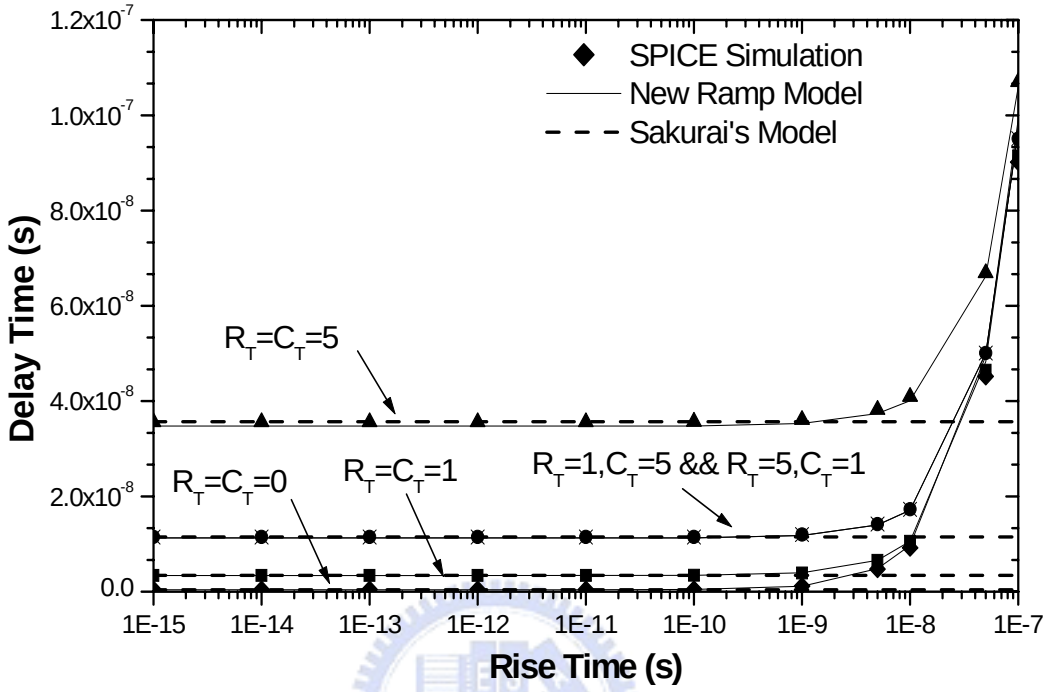


Figure 4. 2 Comparison of SPICE simulation, new ramp model and Sakurai's model for an isolated one-line system of various driver resistances and loading capacitances. Input ramping rate independent delay time is observed in Sakurai's model.

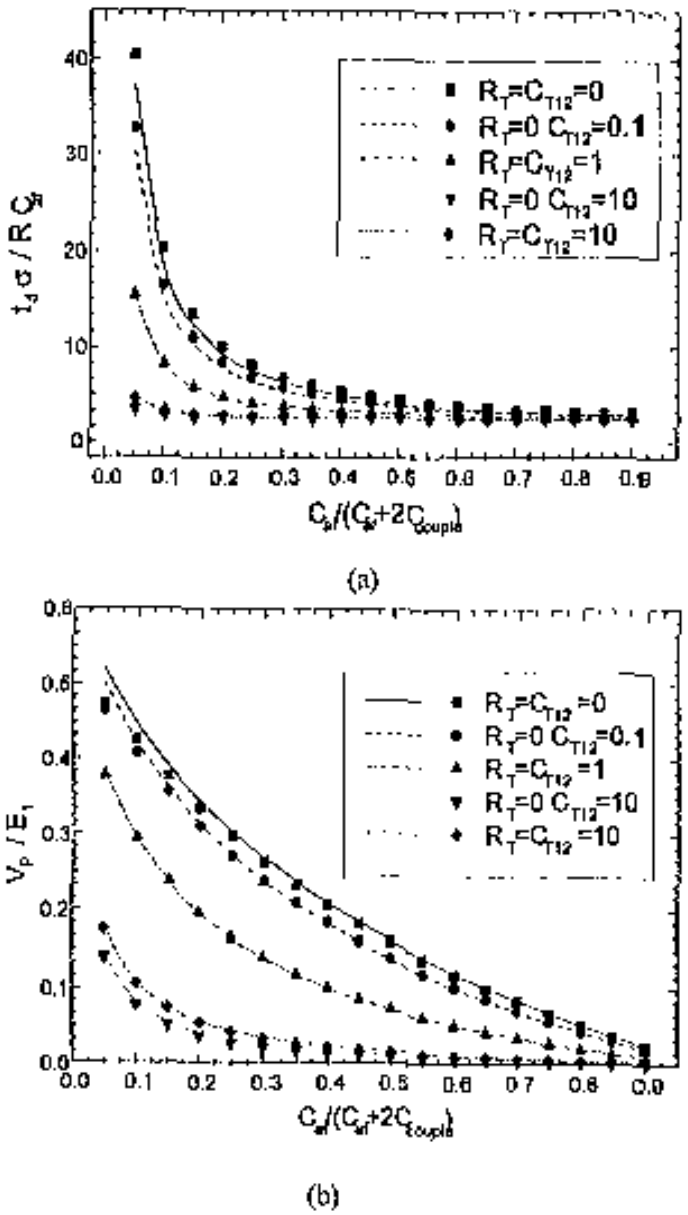


Figure 4. 3 (a) Model accuracy of RC line delay model. (b) model accuracy of RC line crosstalk model.

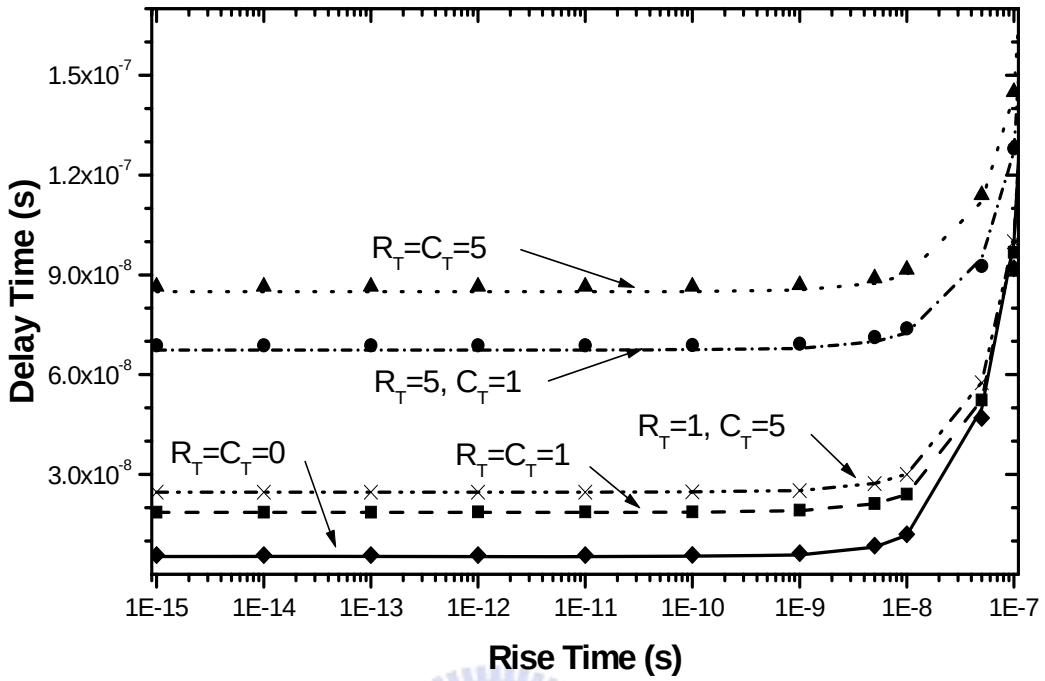


Figure 4. 4 Delay times in SPICE simulation (symbols) and the new ramp model (lines) for the two-line system [Fig. 4.1(b)] are compared.

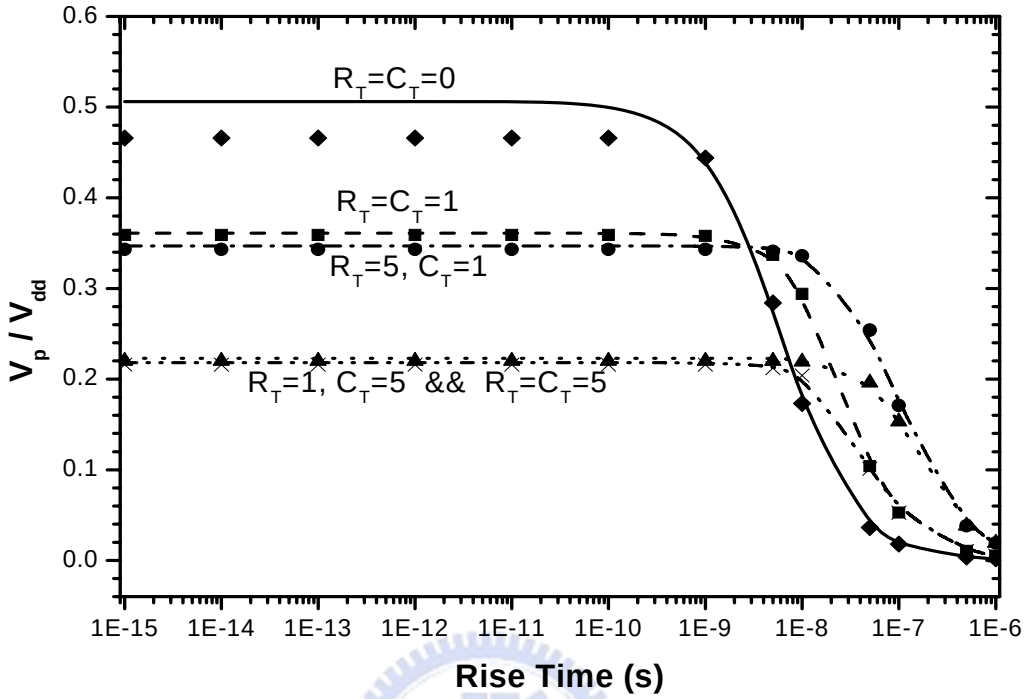


Figure 4. 5. Normalized crosstalk noises in SPICE simulation (symbols) and the new ramp model (lines) for the two-line system [Fig. 4.1(b)] are compared. The crosstalk noise shows input rise time dependence.

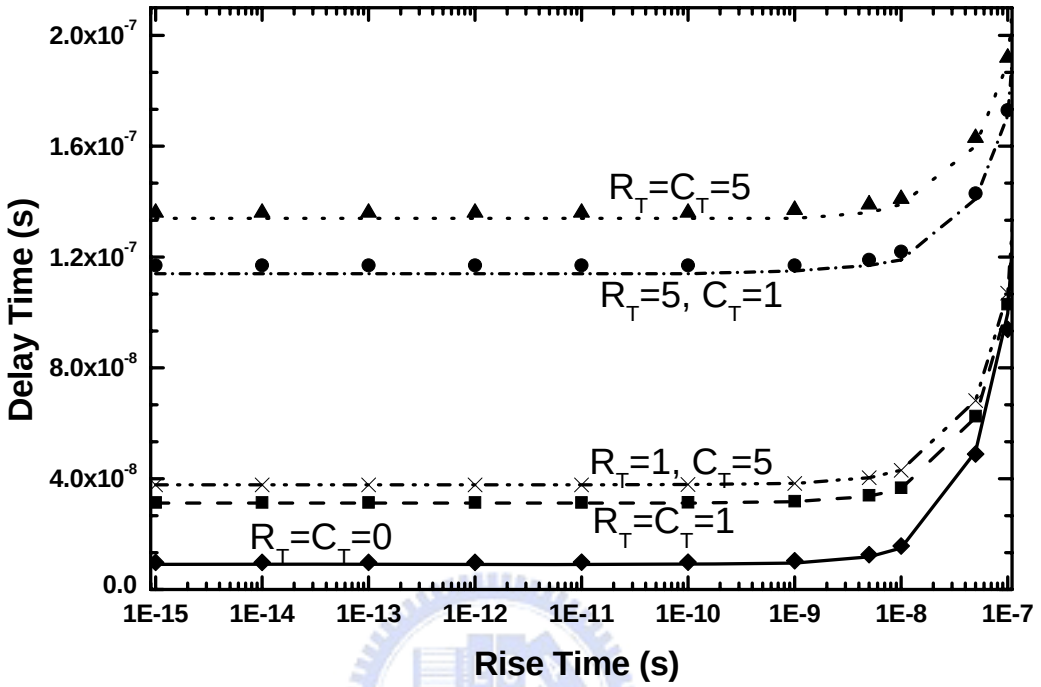


Figure 4. 6 Delay times in SPICE simulation (symbols) and new ramp model (lines) for the multiple coupled line system [Fig. 4.1(c)] are compared.

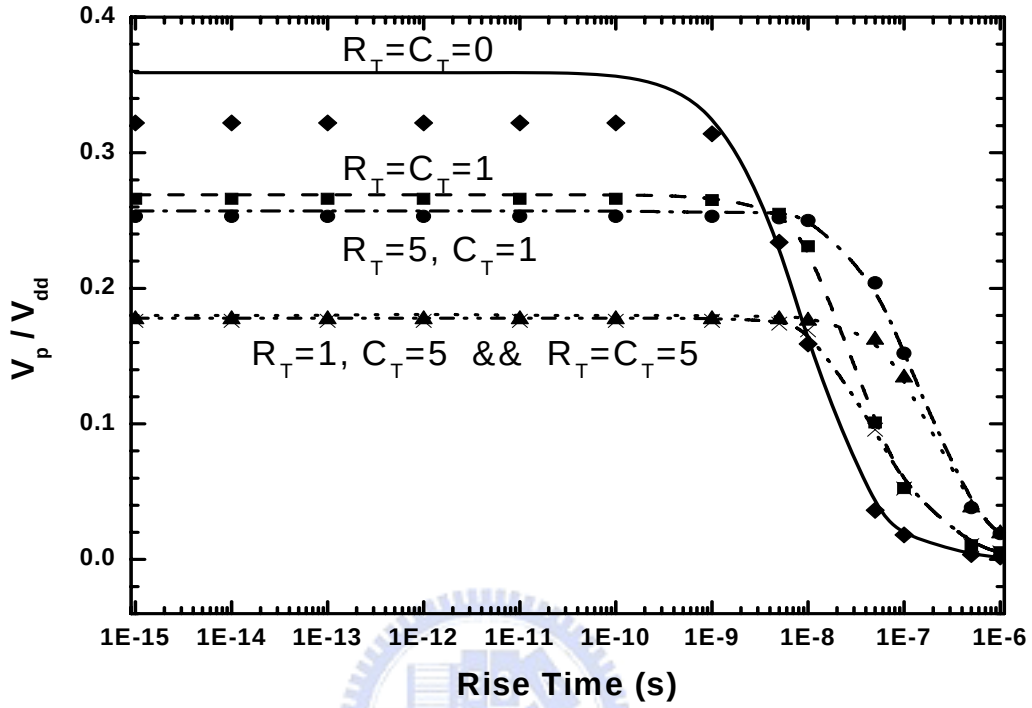
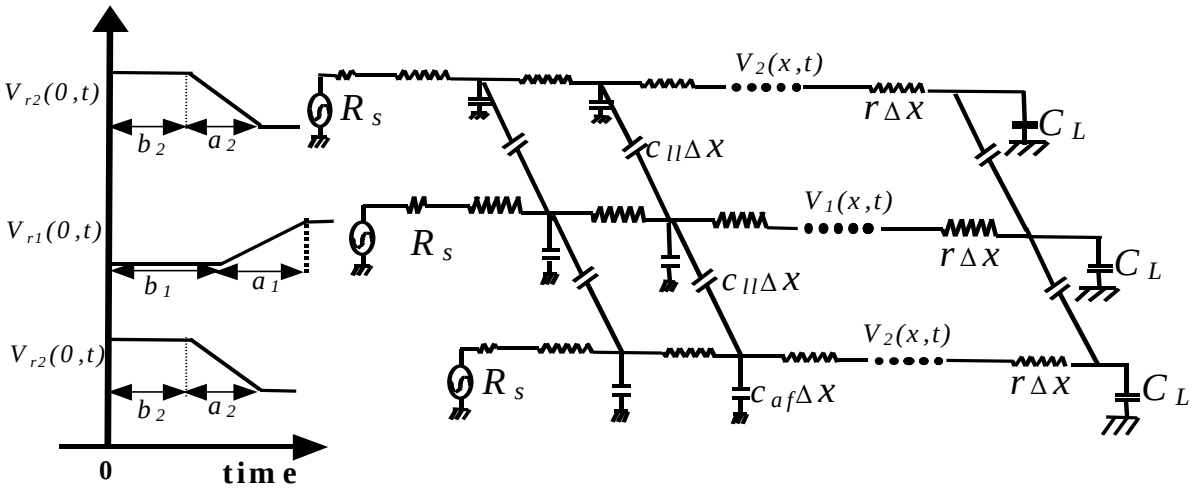
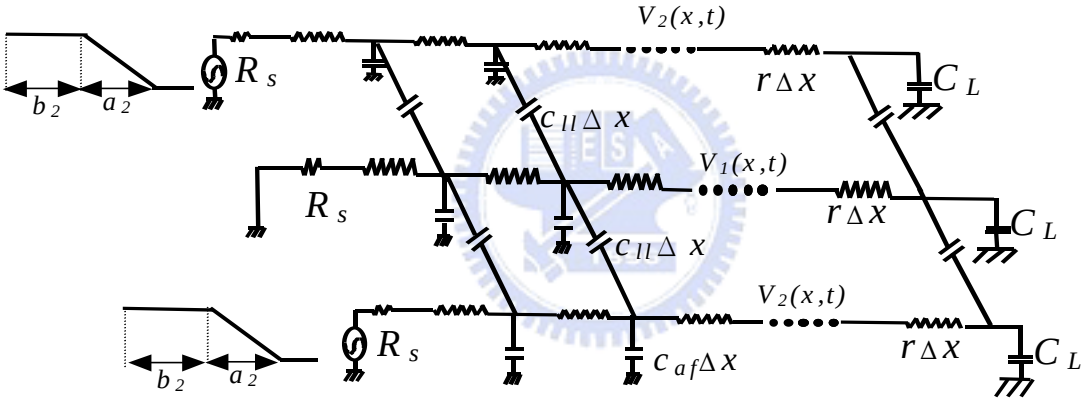


Figure 4. 7. Normalized crosstalk noises in SPICE simulation (point) and the new ramp model (line) in the multiple coupled line system [Fig. 4.1(c)] are compared. The crosstalk noise shows input rise time dependence.

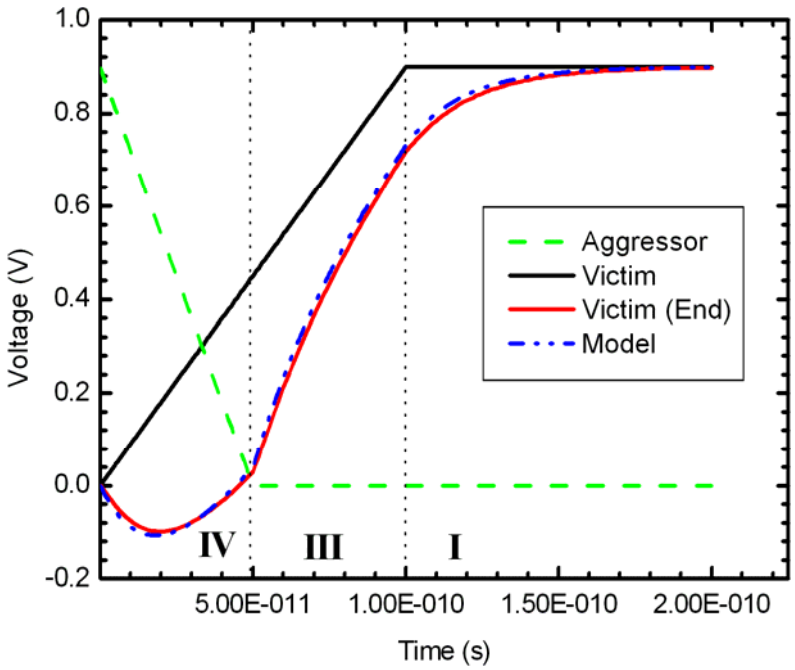


(a)

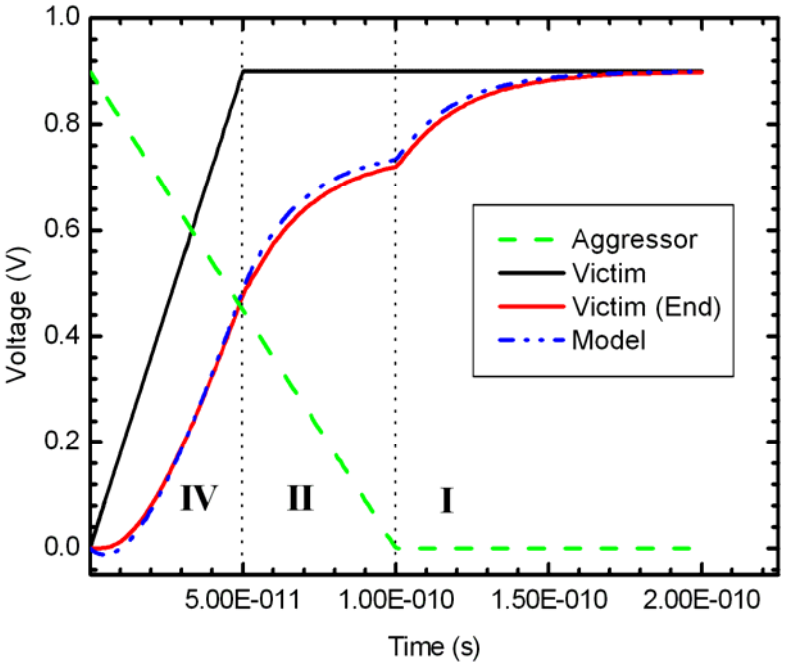


(b)

Figure 4. 8 (a) Schematic diagram of crosstalk-enhanced delay time case and (b) worst crosstalk case for coupled interconnect.



(a)



(b)

Figure 4. 9 Comparison of the output waveforms calculated from SPICE simulation and new models. (a) $a_1 > a_2$. (b) $a_1 < a_2$.

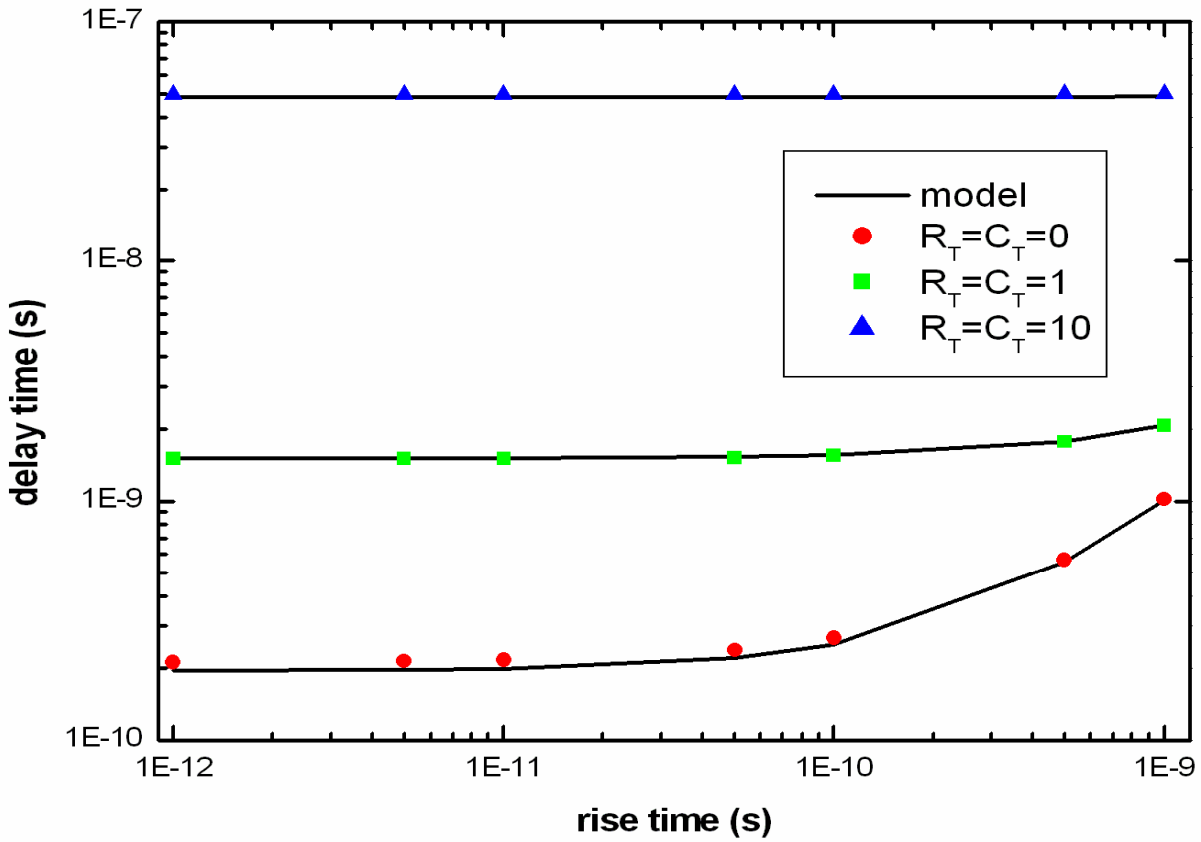


Figure 4. 10 Comparison of SPICE simulation (symbols) and new model (lines) for crosstalk-induced delay times in the system of Fig. 1(a), where $R_T = R_s/R$ and $C_T = C_l/(C_{af}+3C_{ll})$.

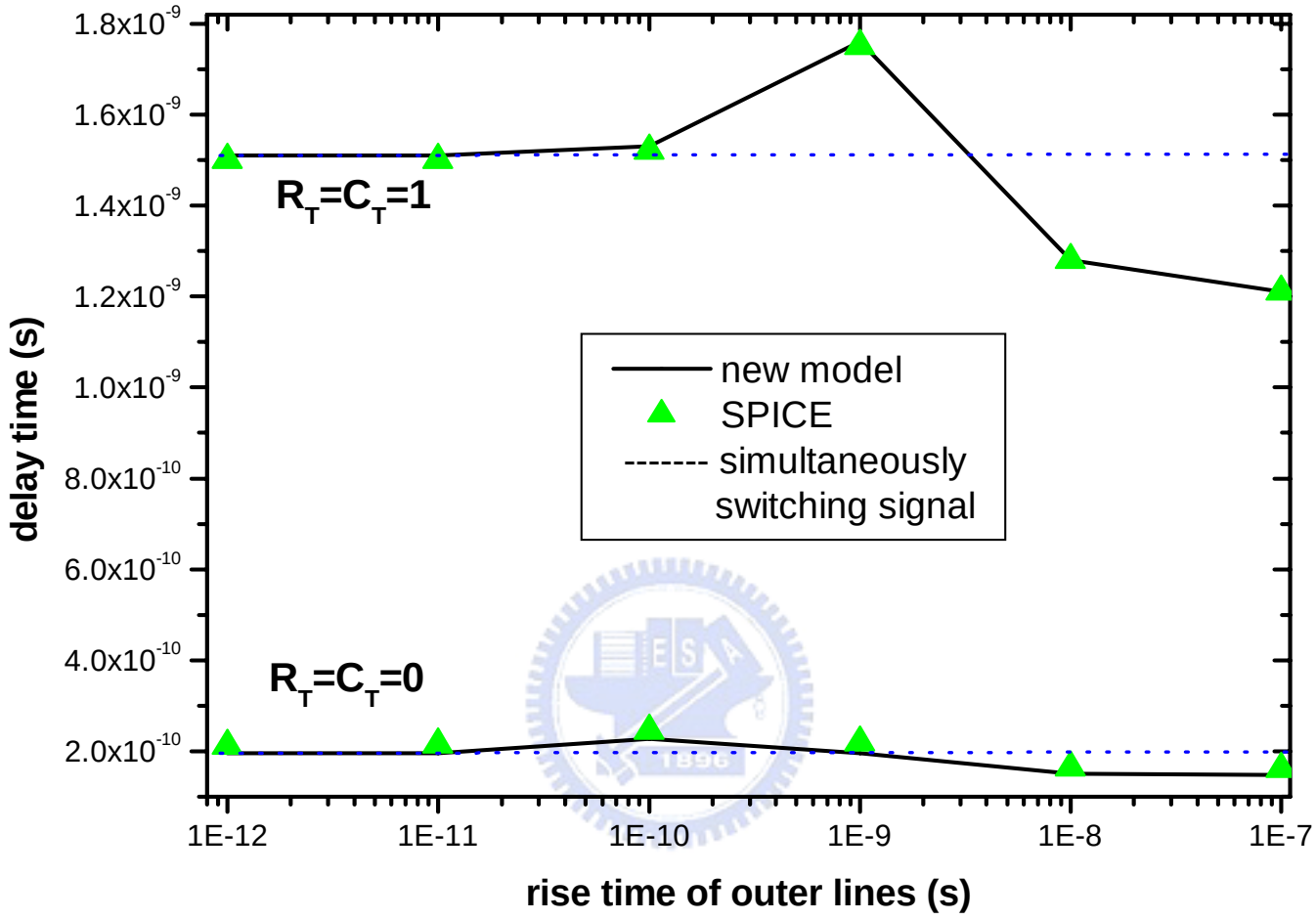


Figure 4. 11. Comparison of SPICE simulation and new model for crosstalk-enhanced delay time case in the system of Fig. 1(a). The rise time in the simultaneously switching case is 1ps, where $R_T = R_s/R$ and $C_T = C_L/(C_{af}+3C_{ll})$.

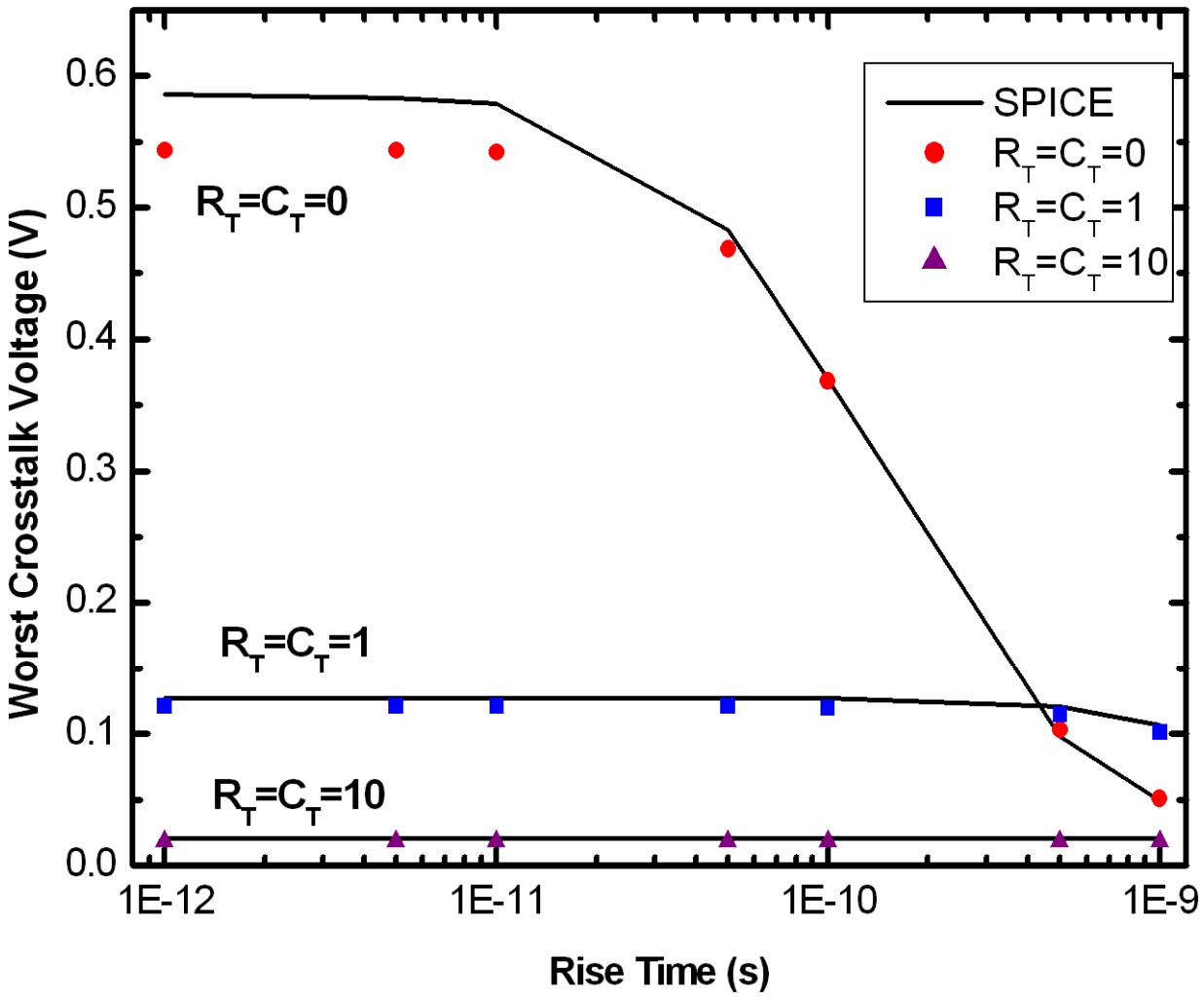


Figure 4. 12 Comparison of SPICE simulation (symbols) and new model (lines) for worst crosstalk noise in the system of Fig. 1(b), where $R_T = R_s/R$ and $C_T = C_l/(C_{af}+3C_{ll})$.

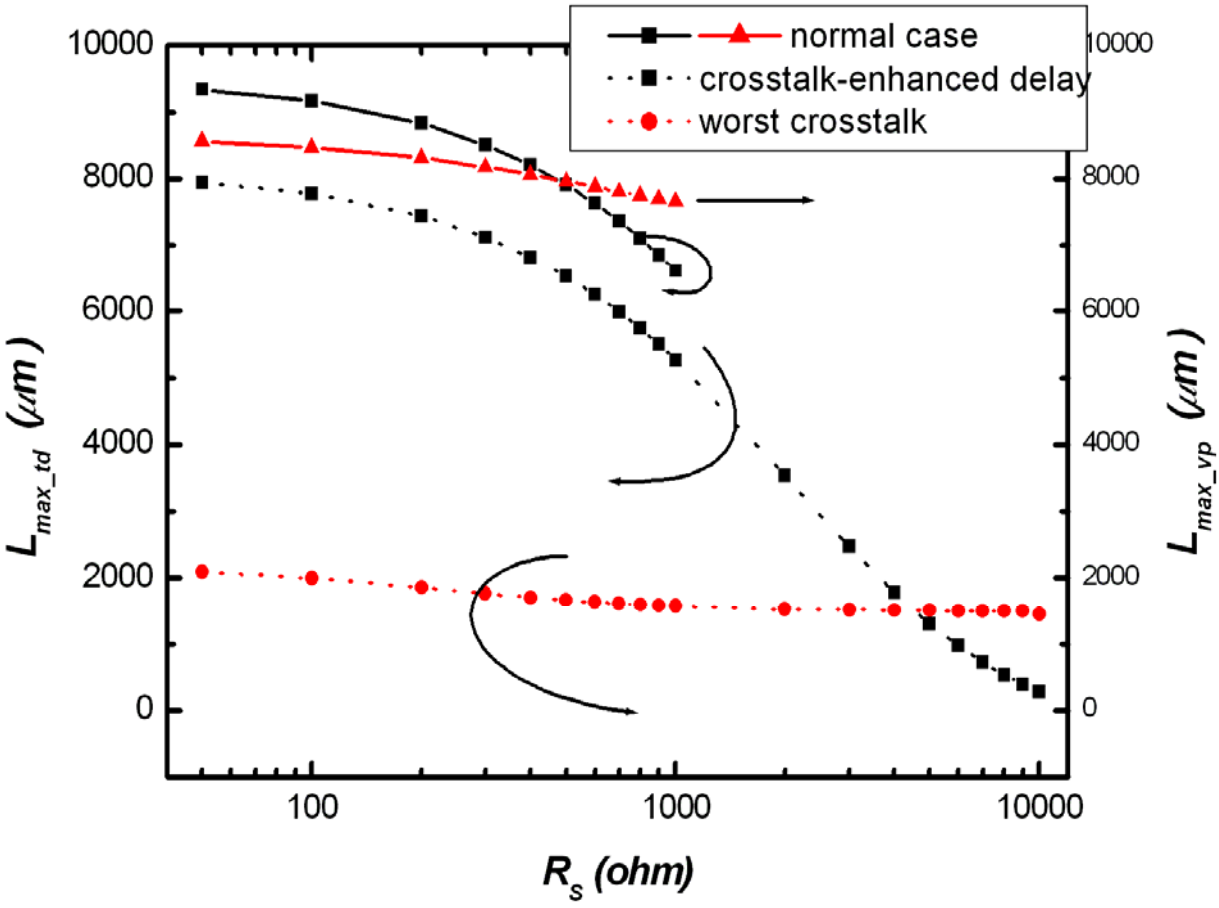


Figure 4. 13 Maximum routing length is limited by the crosstalk for small driver resistance and by the delay time for large driver resistance.

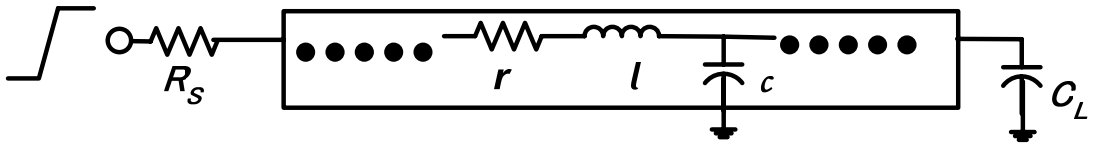


Figure 4. 14. Interconnect modeled as distributed *r*-*l*-*c*.

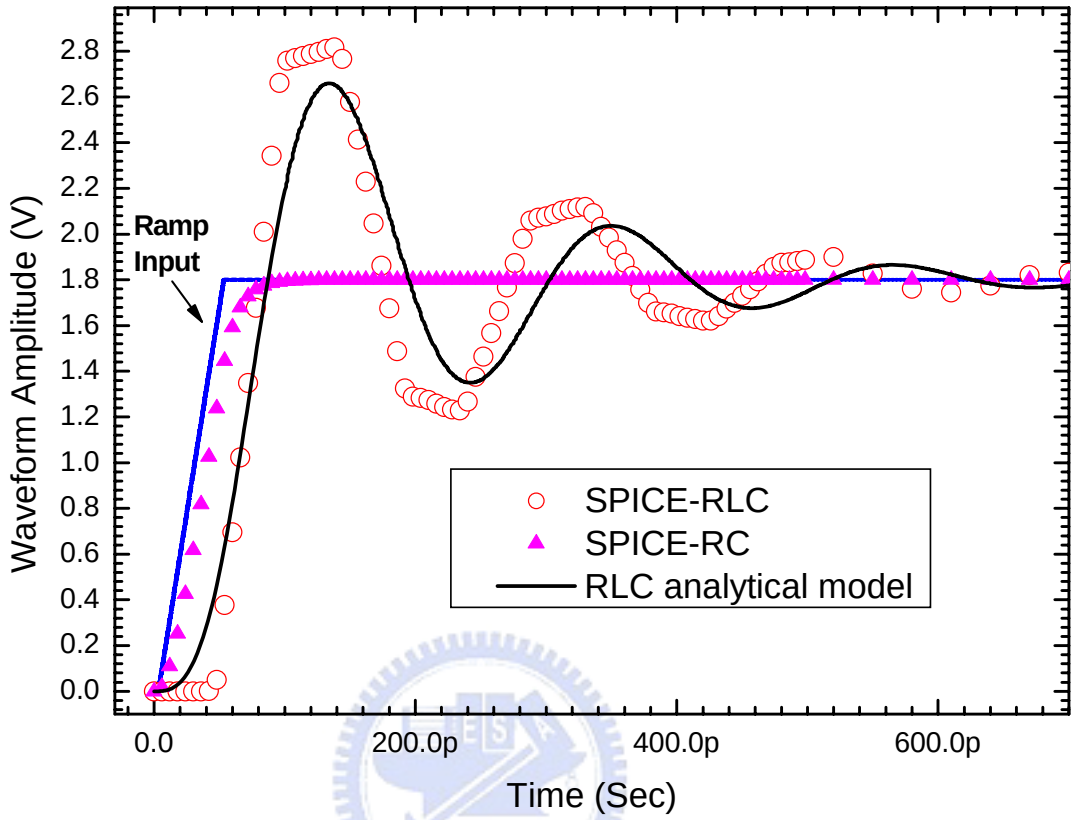


Figure 4. 15. Waveform, at the end-terminal of the wire in Fig. 4.14, calculated from SPICE simulation and herein analytical model.

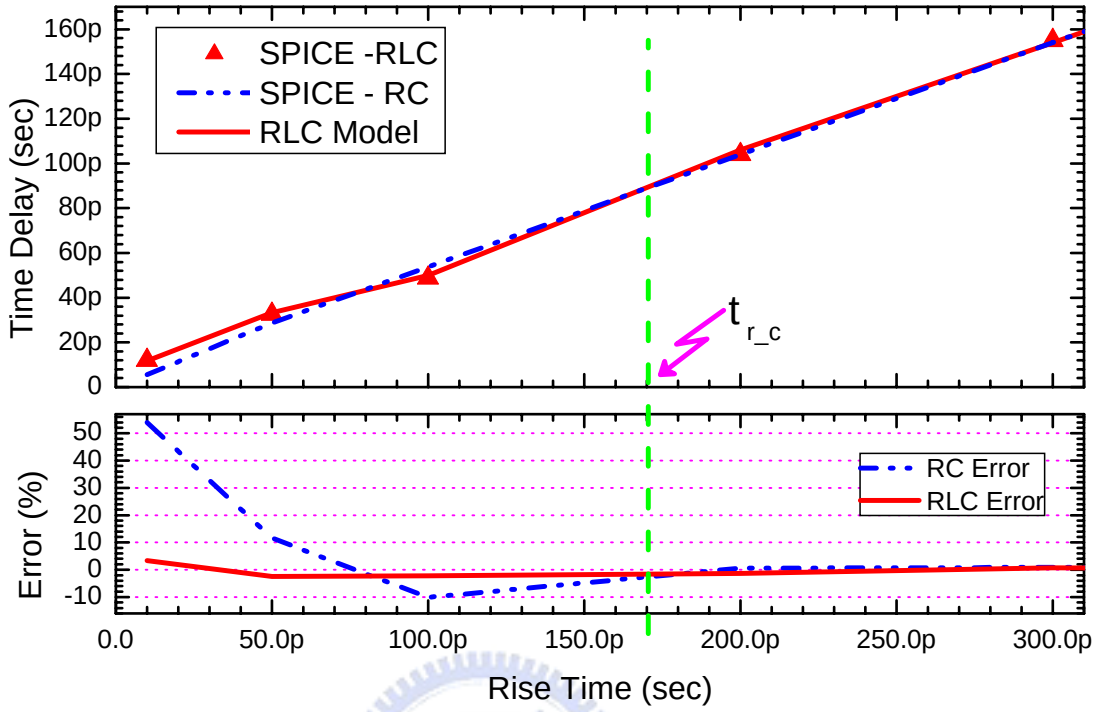


Figure 4. 16. RLC models and RC and RLC SPICE simulation and corresponding percentage error for 50% delay time at R_T=C_T=1, z=1000um.

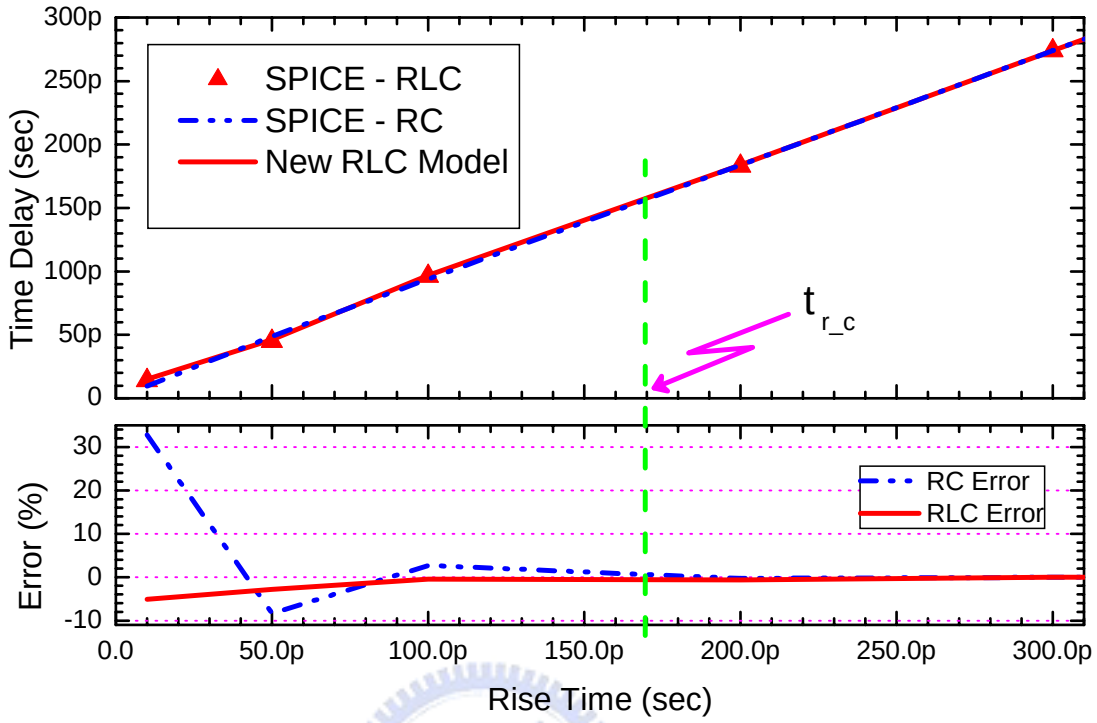


Figure 4. 17. RLC models and RC and RLC SPICE simulation and corresponding percentage error for 90% delay time at R_T=C_T=1, z=1000um.

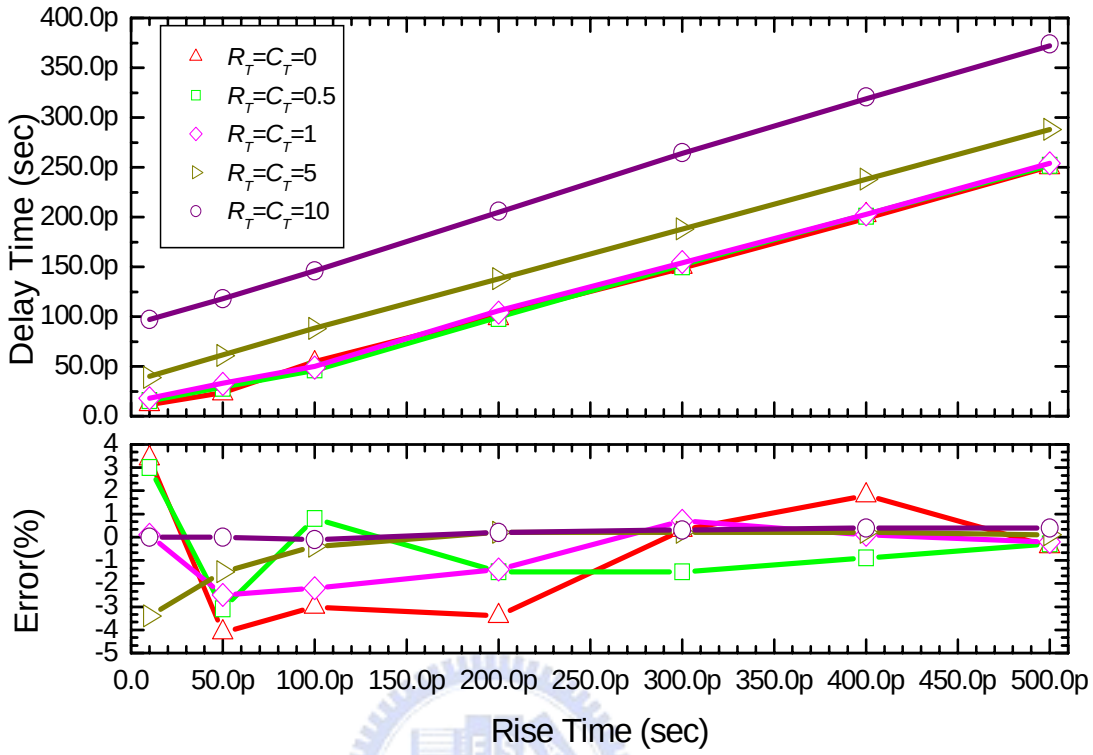


Figure 4. 18 SPICE simulation data (point) versus new model (line) and percentage error plot. The plot gives 50% delay time vs. input rising time for various combinations of driving and loading conditions. Wire length is 1000um.

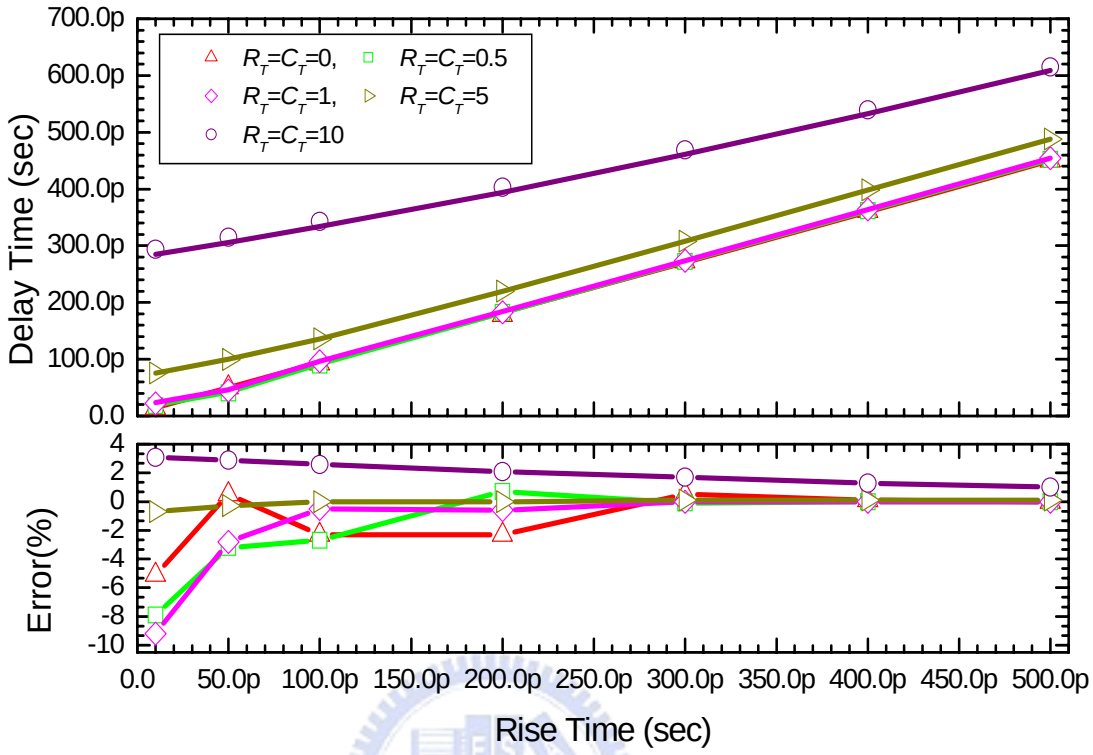


Figure 4. 19 SPICE simulation data (point) versus new model (line) and percentage error plot. The plot gives 90% delay time vs. various input rising time for various combination of driving and loading conditions. Wire length is 1000um.

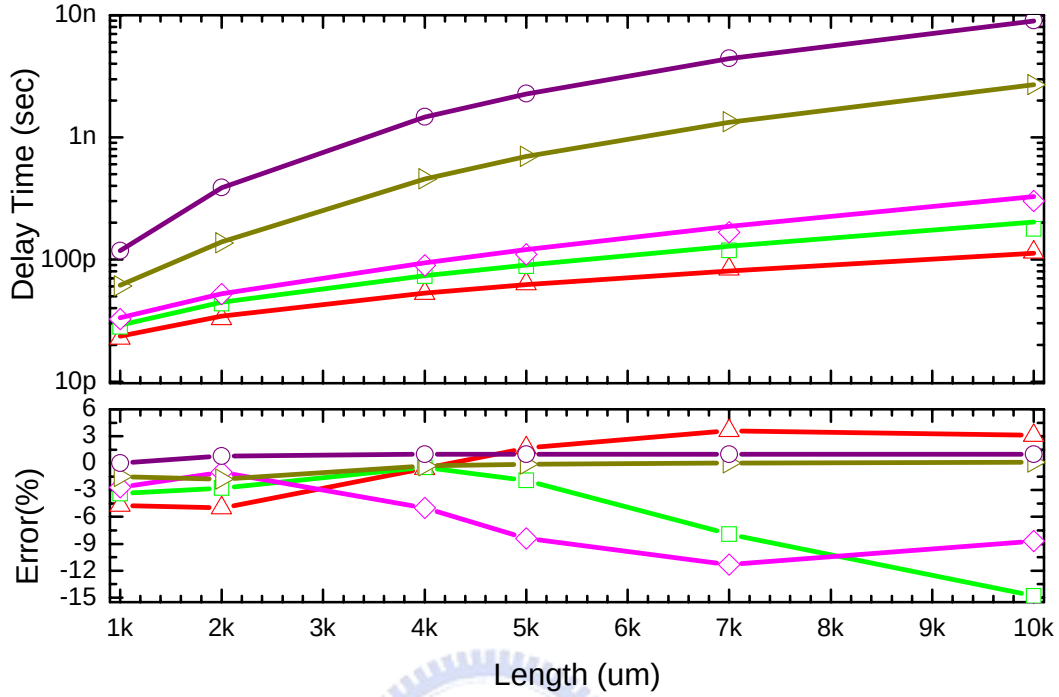


Figure 4.20 50% Delay time vs. wire length for various driving and loading conditions. The input rising time in this plot is 50pS. The legend of this plot is the same as Figure 4.19.

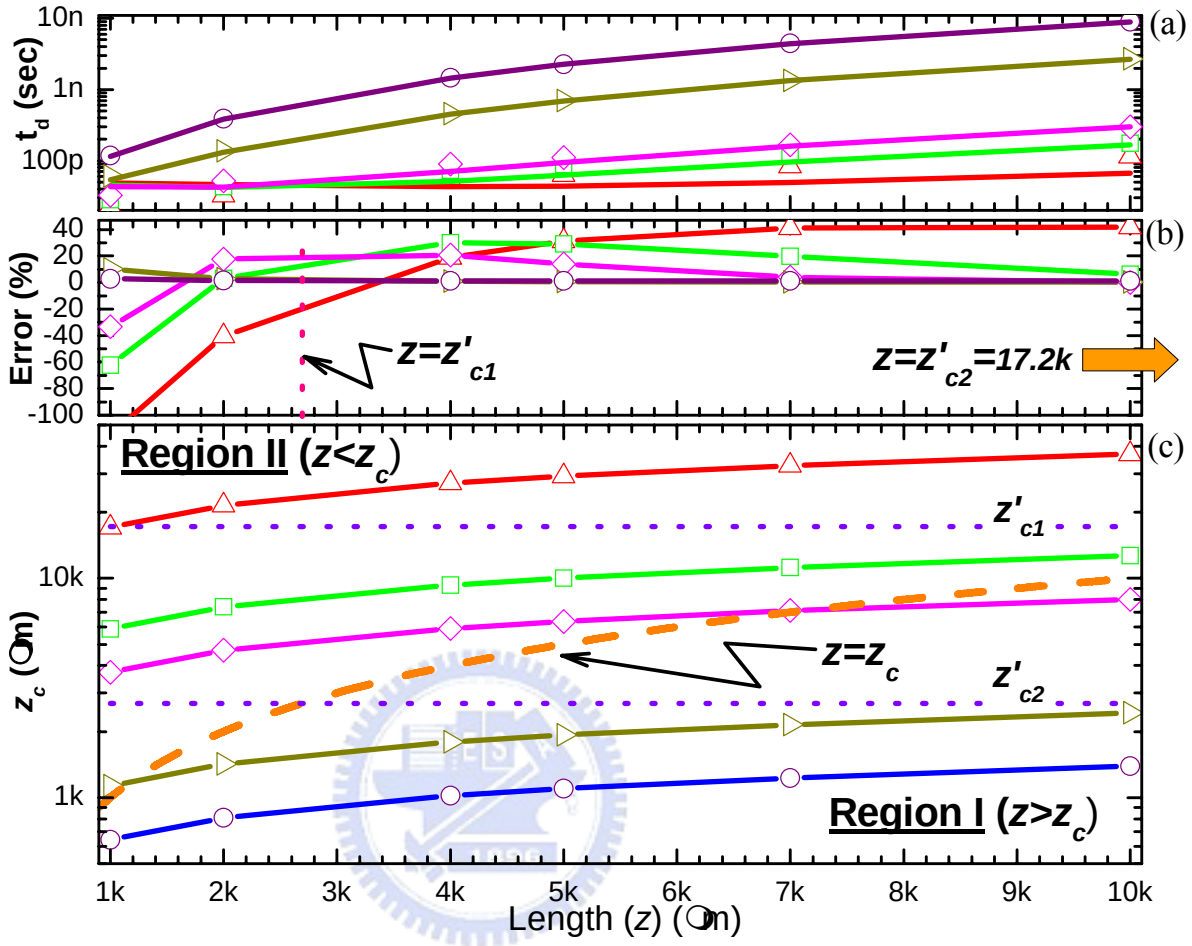


Figure 4. 21 (a) 50% Delay time (point: RC, solid line: RLC and data are from SPICE simulation) vs. wire length for various driving and loading conditions for a=50pS. (b) Percentage error plot for RC model with respect to RLC SPICE simulation. (c) calculated inductance critical length (z_c) vs wire length for various driving/loading conditions. The dash line (▬ ▬) represents the condition that wire length is equal to the critical length ($z=z_c$). The dot line (▪▪▪▪▪) represents the critical length calculated from the two criterions in [4.24] and [4.25]. The legend of point symbols for this figure is the same as Figure 4.19.

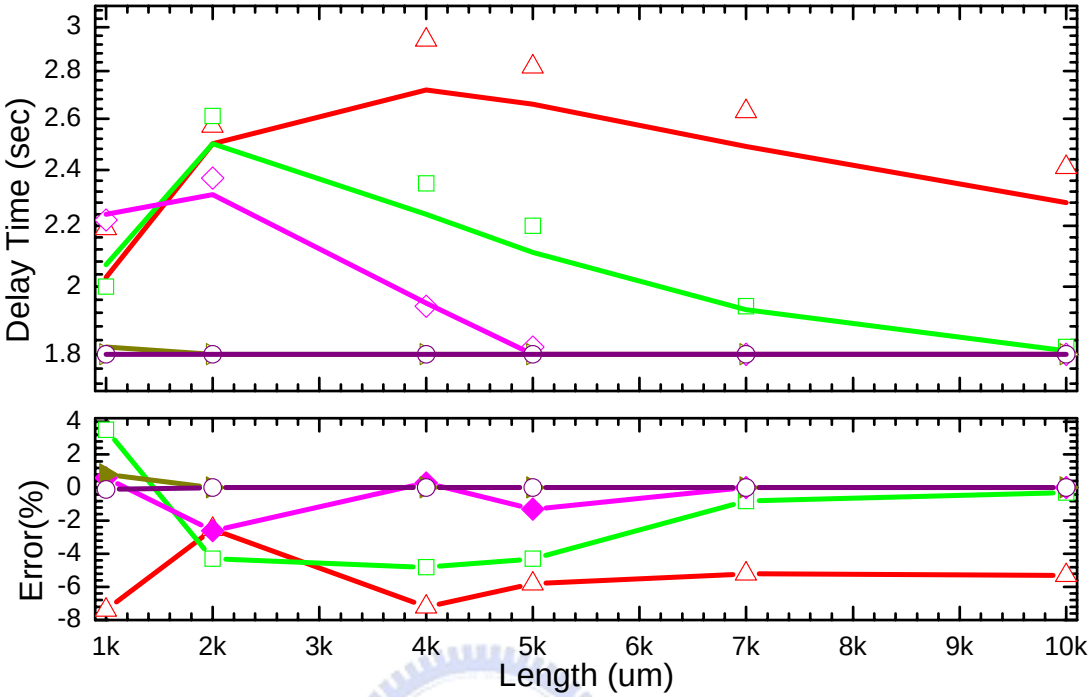


Figure 4. 22. Overshoot voltage vs. wire length for various driving and loading conditions. The legend of point symbols for this figure is the same as Figure 4.19.

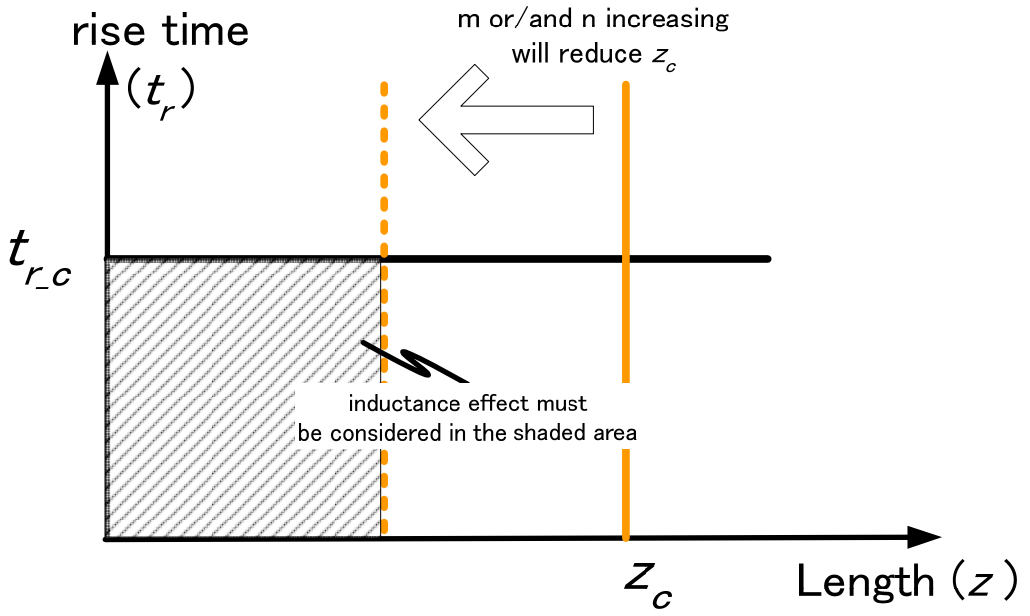


Figure 4. 23. Critical length (z_c) and inductance effect window changing with loading conditions.

Chapter 5 Interconnect Optimization Design

5-1 Interconnect Optimization Design Method

With the developed analytic formulas at hand, we now give a thorough optimization study for the interconnect performance for the delay-line circuit of Fig. 5.1. We give constraints on the delay and crosstalk, and our goal is to find the best process (resp. design) dimension which gives the largest range of design (resp. process) dimension parameters for which both delay and crosstalk are below their individual constraints. In other words, we are interested in finding the largest guaranteed performance region. More precisely, we define two optimization problems:

(1) Find the **optimal process** dimension parameters which give the largest set of design dimension parameters with guaranteed performance (i.e. constraints satisfied); this is referred as process optimization.

(2) Find the **optimal design** dimension parameters which give the largest set of process dimension parameters with guaranteed performance; this is referred as design optimization.

The performance constraints of interest are the maximum delay and maximum peak crosstalk noise; here in this study, the following values are assumed: T_{dmaxl} = *30ps,* T_{dmax2} = *50pS,* T_{dmax3} = *70ps,* T_{dmax4} = *l00ps, and* V_{pmax} = $0.2E_1$. Further, in the circuit of Fig. 5.1, we assume that $C_L = R_s = 0$ to emulate the situations with dominating interconnect delay ($C_{af} >> C_L$) and with large input buffer ($R_s << R$). These values are selected to explore the impact of design and process dimensions on the line delay and crosstalk in the deep sub-micrometer range. The closed-form

models of line capacitance, signal delay and crosstalk noise developed in Chapter 4 allow for analytical performance evaluation for arbitrary interconnection dimensions, without resorting to the cumbersome SPICE simulation, or the over-simplified delay formulas.

5-2 Process Optimization

Since we are interested in finding the best process dimension which yields the largest set of design dimension parameters (*W* and *S*) for which constraints on both delay and crosstalk are satisfied, we first investigate the joint impact of *W* and *S* on interconnect line performance. Contour plots of wire width Wand wire spacing S are generated for three sets of wire thickness *T* and dielectric thickness *H*. as shown by contour C-l, C-2, C-3 and C-4 in Fig. 5.2 for delay time of 30ps, 50ps, 70ps and l00ps, respectively. For small *W* and *S*, wire width increases as wire spacing reduces, because higher C_{couple} needs to be compensated by smaller line resistance. Note that for *S* above 0.6 μm, *W* to achieve a certain delay time does not vary with *S*, since the coupling capacitance at such spacing is small and does not dominate line delay anymore, and constant wire width gives constant C_{af} as well as constant line delay. Contour C-5, the crosstalk contour, points out that larger spacing is required for small wire width to sustain crosstalk noise at a specified level. This need of increasing S is due to the fact that C_{couple}/C_{af} ratio increases as wire width reduces, and enhances signal propagation to the adjacent wire and thus induces higher crosstalk noise. Relaxing wire spacing to relax coupling capacitance is hence needed.

We then investigate the influence of process dimension, i.e. wire thickness *T* and dielectric thickness *H*, on the contour analysis as mentioned above. The impact of T and H can be observed by comparing Fig. 5.2 and 5.3. In Fig. 5.3, as T increases to 0.7 μm, it is obvious that the crosstalk contour C-5 goes through higher S, indicating

that increasing T induces higher coupling capacitance, resulting in more severe constraint on S. On the contrary, for delay contour, both smaller W and S are allowed, when comparing to the case of T = 0.5 μm in Fig. 5.2; this is due to the fact that increasing T gives lower line resistance and thus lower delay time. The comparison of Fig. 5.2 and Fig. 5.3 indicates that the well-known existing approach to reduce delay, which is to increase aspect ratio with technology scaling [5.1], may induce serious crosstalk noise which can only be reduced by relaxing the inter-wire spacing in chip design. Our optimization study is now formalized: For a given process dimension (T and H), we define guaranteed performance region as the region of design dimension points (Wand S) over which the constraints on both delay and crosstalk are satisfied, as marked by dashed-lines in Fig. 5.2. That is, the guaranteed performance region is simply the dashed region enclosed by C-l and C-5 for the delay constraint of 30ps (or C-3 and C-5 for the delay constraint of 70ps), in Fig. 5.2. The point (W, S) which intersects C-l and C-5 (or C-3 and C-5) is the point where both delay and crosstalk constraints are met exactly; call such point (W, S) as the target point. As the process dimensions T and H vary, the target point (W, S) moves and the guaranteed performance region changes accordingly. Denote by Ad as the area of the guaranteed performance region. We seek to find the process dimension parameters T and H that can yield the largest Ad, since such a region can cover most design dimension points (W, S) having satisfactory performance, thus impact of (uncertain) dimension variations mentioned earlier can be mostly reduced. Our process optimization problem is

Maximize Ad over all feasible (T,H).

The calculated target-point trajectory and Ad for lines on one plane structure are shown in Fig. 5.4 and Fig. 5.5 for signal delay constraints of 30ps and 70ps, respectively. The target-point trajectory and Ad for lines between two planes are

shown in Fig. 5.6 for delay constraint 70ps. It is observed that the target-point trajectory moves toward larger W and smaller S, as H decreases with constant T. This is due to the fact that increasing line to ground capacitance causes severe signal delay. Reducing line resistance or increasing line width to reduce signal delay is thus essential. Furthermore, increasing line to ground flux simultaneously decreases line to line coupling capacitance, allowing for smaller S while keeping the same crosstalk noise level. Another observation with varying T shows that smaller S is allowed for smaller T and same H, as the crosstalk noise is significantly reduced by decreasing T and coupling capacitance. However, larger W is required to sustain same signal delay, as line resistance increases as T decreases. For optimal solutions, we find that the target point (W, S) = (0.23 μm, 0.36 μm) corresponds to (T,H) = (0.5 μm,0.2 μm), which the technology dimension allowing for best guaranteed interconnection performance region for arbitrarily distributed (W, S) above (0.16 μm, 0.16 μm). These observations can be extracted from the variation of Ad versus H and T. As shown in Fig. 5.5, the process with T = 0.5 μm offers a maximum Ad at H = 0.2 μm and it is indeed the point where both W and S can be minimized to (0.23 μm, 0.36 μm), while sustaining a delay of 70ps and a crosstalk noise of 0.2E1. Similar analysis can be applied to the data in Fig. 5.4, where the best process dimension is identified to be (T, H) = (0.7 μm, 0.3 μm), this process dimension gives largest Ad and corresponds to (W, S) = (0.5 μm, 0.5 μm). It is worth noting that the optimal values of H for both 30ps and 70ps delay constraints are relatively small, an observation which disagrees with traditional concept of technology design in which H is often kept large to relax signal delay. The small value of the optimum H is induced by the crosstalk noise constraint. On the other hand, if the wire width is small, then the wire to ground dielectric thickness often needs to be small for the crosstalk noise performance. The dielectric thickness limit can be relaxed by decreasing T. As T

decreases, the optimal value of H increases, as shown by Ad in Fig. 5.4 and Fig. 5.5. In Fig. 5.4, for T = 0.3 μm, optimal value of H rises to 0.7 μm, this demonstrating such crosstalk-delay tradeoff. It is worth mentioning that the optimization point of (T, H) = (0.3 μm,0.7 μm) corresponds to (W, S) = (0.56 μm, 0.68 μm), giving much larger design pitch than the point (W,S) = (0.4 μm,0.5 μm) given by (T,H) = (0.7 μm,0.3 μm). The process dimension (T, H) = (0.7 μm, 0.3 μm), or the high-T with low-H design approach, hence improves over the traditional large-H approach. In deep submicron technology, it is needed to maintain reasonable wire width and thickness ratio by reducing T with design-pitch scaling. Based on our study, in order to use small (W, S) the wire thickness, it is useful to sustain T as high as possible, and using reduced dielectric thickness H to limit crosstalk noise. Similar optimization contours are shown in Fig. 5.6 for parallel lines between two plates, with delay time constraint of 70ps. Here, comparing to the one-plane case in Fig. 5.4 and Fig. 5.5, much larger W is required to sustain the same signal delay constraint, and much smaller S can be used to sustain the same crosstalk noise level. This is because the top plane attracts much flux, greatly reducing the C_{couple}. The Ad variation shows that optimal process dimension is around (T, H) = (0.7 μm,0.3 μm), leading to target points (W, S) = (0.20 μm,0.32 μm). To investigate impact of T, it is shown that the capacitances to both top plane and bottom plane put a severe constraint on wire thickness T or the wire resistance. That is, decreasing T will seriously decrease Ad due to increased wire resistance. Comparing to the one-plane case where the wire thickness only weakly influences Ad, we suggest that performance of interconnection with dense top overlapping wires (emulating the case in local interconnect) is very sensitive to wiring resistance, and this performance can be greatly improved with low resistance material or high wire thickness. A direct comparison of target point (W, S) with one plane and with two planes is shown in Fig. 5.7 for line delay constraints of

30ps. It can be clearly observed that for reduced T, i.e., T under 0.5 μm, decreasing H only weakly increases the required W for lines on one plane (from 0.31 μm to 0.39 μm, for H from 0.7 μm to 0.5 μm with T = 0.5 μm), but significantly increases the required W for lines between two planes (from 0.55 μm to 1.02 μm for H from 0.7 μm to 0.5 μm with T = 0.5 μm) due to its significant wiring delay. In summary, the optimal process dimension for lines with dense top wiring should choose both large H and large T, if T is under 0.5 μm. If T larger than 0.5 μm can be fabricated, wiring delay can be .greatly reduced even with small (W, S), and with crosstalk noise regulated by an optimal H as in the one-plane case. The adopted T should also meet the requirement of aspect ratio as mentioned in [5.1]. The optimization presented here takes care of the movement of the design target with process dimensions, and also gives a quantified figure of merit (the area of guaranteed performance region) for identifying the technology with the best inter- connect performance. The optimization framework and procedure is believed to be useful for process dimension design.

5-3 Design Optimization

Similar optimization study as above is formalized: For a given design dimension (W and S), we define guaranteed performance region as the region of process dimension points (T and H) over which the constraints on both delay and crosstalk are satisfied, as shown by the dashed region in Fig. 6(b). The target point (T, H) is similarly defined, i.e. the intersection point of the delay and crosstalk contours at which both delay and crosstalk constraints are met exactly. As the design dimensions Wand S vary, the target point (T, H) moves and the guaranteed performance region changes accordingly. Denote by Ap as the area of the guaranteed performance region. The design optimization problem is

Maximize Ap over all feasible (W, S).

A solution to the design optimization problem identifies the design dimension

parameters Wand S, which yield the widest range of process dimension parameters T and H for guaranteed performance. Note that the best guaranteed performance region Ap (given by the best design (W, S)) can also be identified by the associated optimal target point (T, H). Analysis is similarly done here to investigate the target point of (T, H), and its movement with design dimension (W, S). The process to determine the optimal target point (T, H) (which corresponds to the optimal *Ap*) among a certain set of design pitches (dimensions) is often executed in the initial stage of new process development, when a preliminary set of design pitches has been suggested, based on which process engineers need to determine their process dimension. The process dimension should provide best performance when being incorporated with the design pitch. As so formulated, the optimization problem again boils down to the study of the trajectories of the target point (T, H) and the objective function *Ap*, as the design pitches vary the T -H contours for parallel lines on one ground plane are shown in Fig. 5.8 and Fig. 5.9, for (W, S) = (0.4 μ m, 0.4 μ m) and (0.4 μ m, 0.6 μ m), respectively. It is shown in Fig. 5.8 that delay contours C-1, C-2 and C-3 are almost independent of T for H above 0.76 μ m. This is because if H is sufficiently large, Ccouple dominates line capacitance, and constant T gives constant Ccouple, resistance and hence constant delay. On the contrary, for very small H, Caf dominates line capacitance, and reducing H will attract sidewall flux to ground, thus increasing Caf. This increased Caf can be compensated by increasing wire thickness T and thus decreasing the wire resistance. The crosstalk contour C-4 shows that the C_{couple} from increasing T can be eliminated by reducing H , i.e. attracting the coupling flux to ground to reduce line to line flux. The T -H contour in Fig. 5.9 shows that smaller T (higher resistance) than the one-plane case (Fig. 5.8) is allowed for delay contours C-1, C-2 and C-3, due to the decreased Ccouple (and thus decreased total capacitance). Crosstalk contour C-4 in Fig. 5.8 is almost not realized in our parameter range due to small S, but is clearly

shown in Fig. 5.9 as the relaxed S gives much lower crosstalk noise level, allowing for higher H . Target point (T, H) defined by the intersection of C-1 and C-4, and Ap are shown in Fig. 5.10 and Fig. 5.11. Note that here Ap is the area of the region sandwiched between C-1 and C-4 as shown by the dashed region in Fig. 5.9, with crosstalk noise being reduced at smaller H. The target point trajectory in Fig. 5.10 and 5.11, for the delay constraints of 30ps and 70ps, shows that to maintain low level of wire delay and crosstalk noise, higher 11 ratio is required with decreasing W. This is because increasing T compensates wire resistance induced by small W, and reducing H degrades the coupling capacitance and hence crosstalk noise. Note that in Fig. 5.10, the optimal point with (W,S) = (0.4 μ m,0.5 μ m) now needs (T,H) = (0.7 μ m,0.29 μ m), indicating extremely thin dielectric thickness. The objective parameter Ap now monotonically decreases with reduced S and also reduced W, indicating that technology scaling gives increasingly severe constraints in vertical technology dimension design. Here, the upper bound on H is limited by crosstalk (from C-4) noise and the lower bound is limited by signal delay (from C-1). The upper bound on T is limited by crosstalk noise (from C-4) and the lower bound is limited by signal delay (from C-1). With reduced design pitch, C-1 moves right and C-4 moves down, and both severely reduce the process window Ap. The target points for lines between two planes are shown in Fig. 7(c) for td = 70ps, higher T and also higher H than in the one-plane case are observed for the same delay and crosstalk specification. This is because the top plane significantly prevents the coupling capacitance from increasing, and hence T are allowed to increase without causing crosstalk noise problem. However, wire delay is more serious here, and hence large T which reduces wire resistance and large H which reduces total capacitance are useful in relaxing wiring delay. Results of the one plane study can be applied to optimize global interconnection lines (among cells), and results of the two-plane study can be applied

to local interconnections (intra cells).

5-4 Summary

Optimization of interconnect performance based on wire delay and crosstalk noise has been formulated and studied. Accurate analytic closed-form models have first been developed for wire capacitance, wire delay and crosstalk noise. In the capacitance model, line to line capacitance and line to ground capacitance are modeled separately, to giye precise delay and crosstalk estimation. Based on the developed analytic models, our interconnection optimization study has been done in two approaches: process optimization and design optimization. Our results indicate that larger T and H (or equivalently, p = T + H) is useful to reduce wire delay for lines between two planes, and an optimal H exists for lines on one plane which is different from traditional large-H approach. The design window Ad is severely degraded in the two-plane case with reduced T, as compared to the one-plane case, due to wire resistance and delay. However, lines between two planes allow for much larger Ap than lines on one plane, due to the relaxed constraint of H or crosstalk noise in the two-plane case. This work is believed to be useful in future technology design and layout optimization. The capacitance, delay and crosstalk models can themselves be used in cell modeling and gate-level simulations.

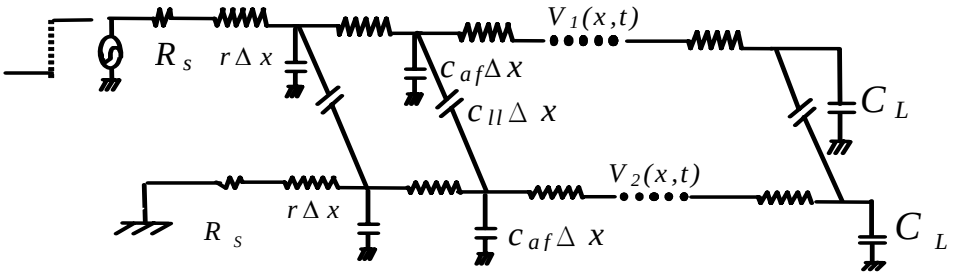


Figure 5. 1 Interconnect schematic for optimization design.

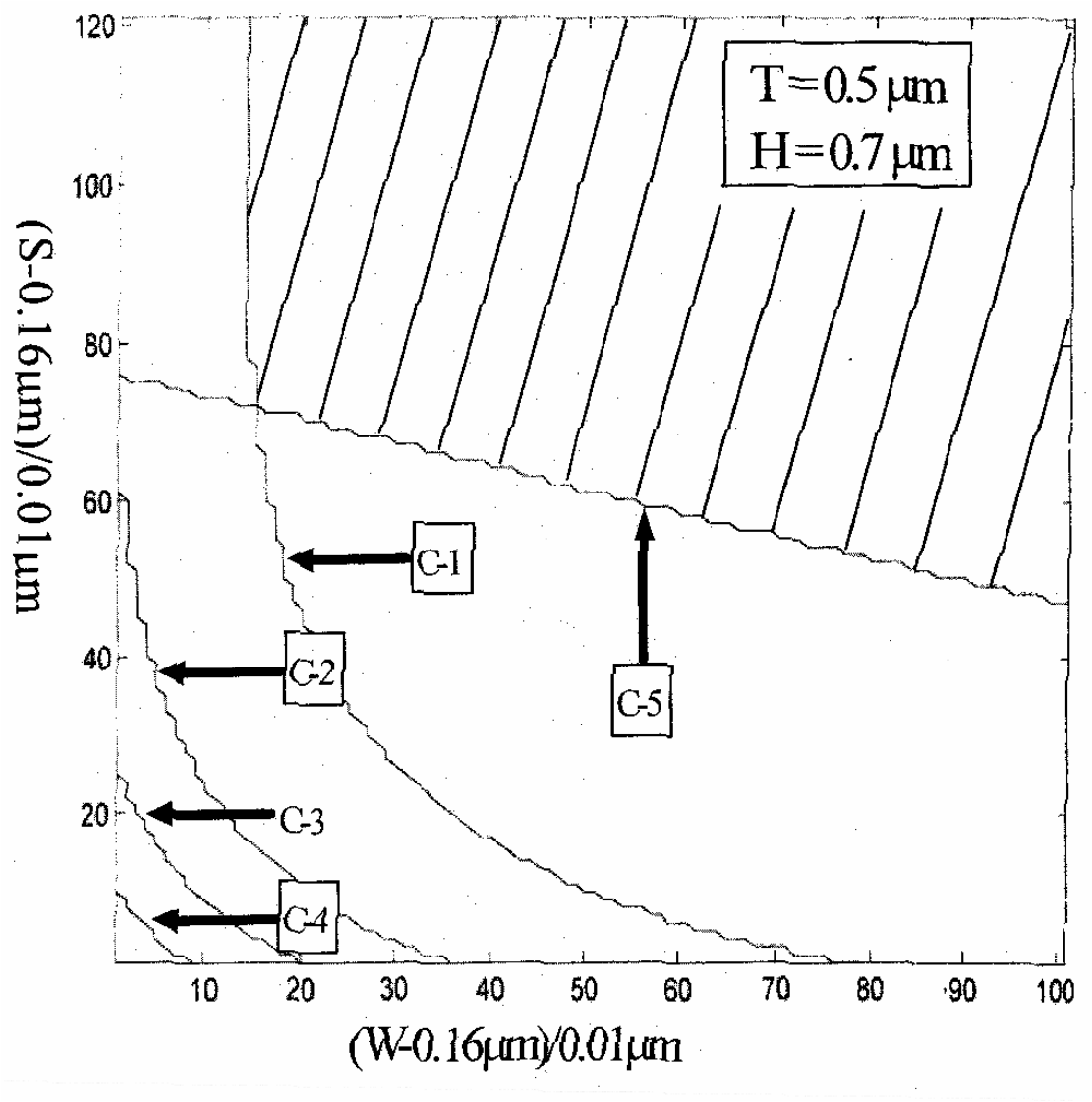


Figure 5. 2 Design contour analysis of delay and crosstalk

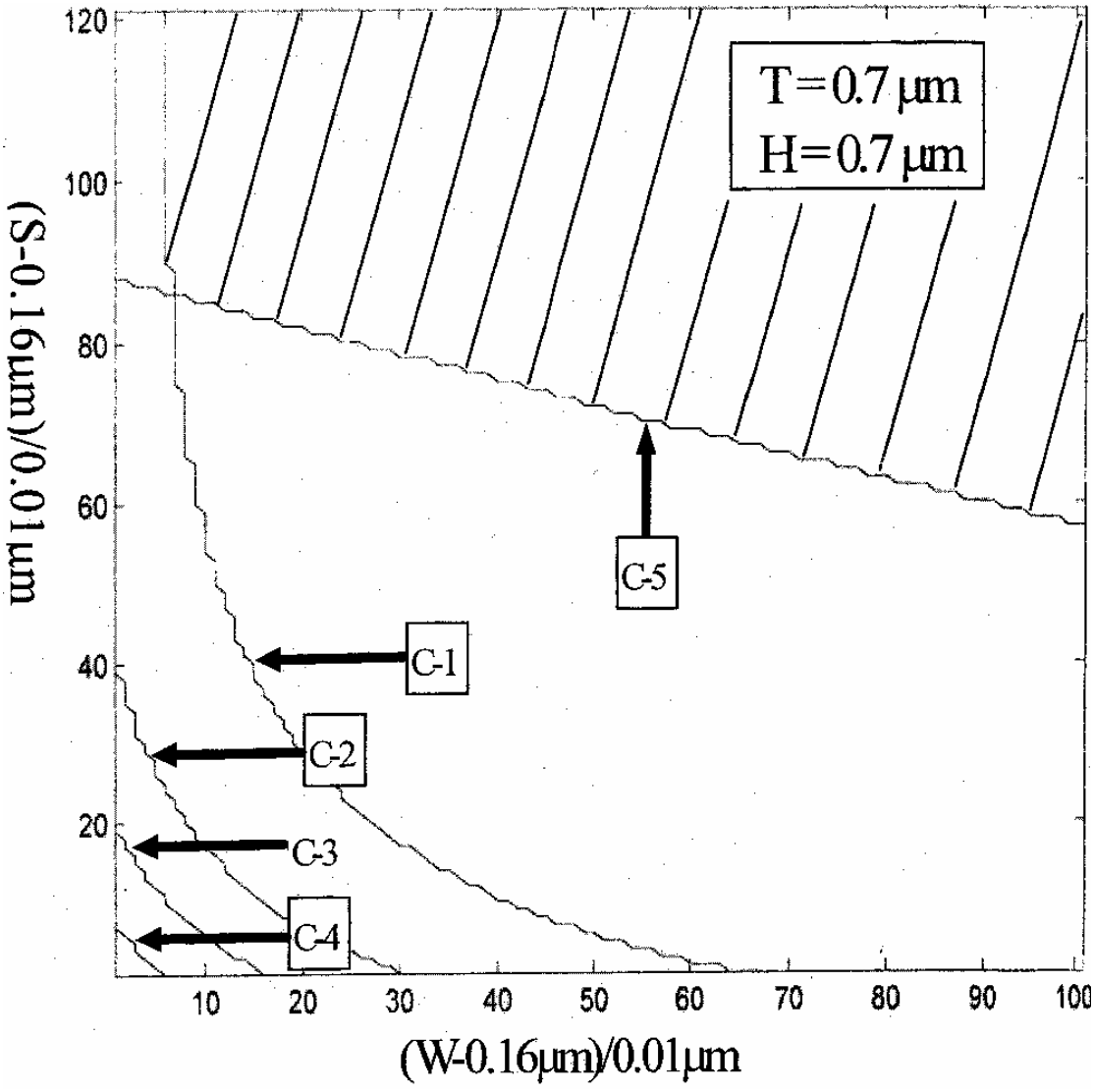


Figure 5. 3 Design contour analysis of delay and crosstalk for structure T=H=0.7 μm.

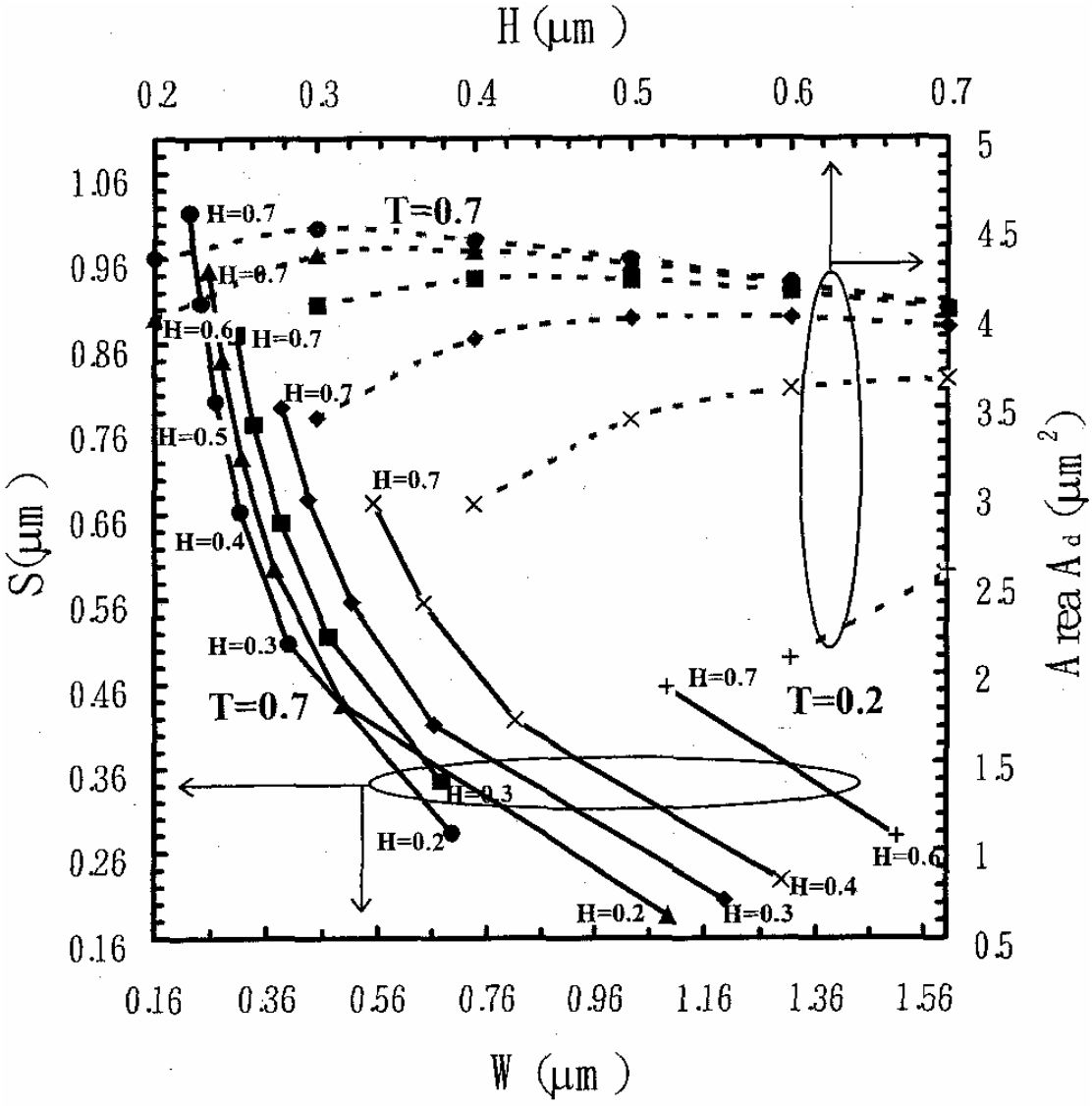


Figure 5. 4 Design target and A_d analysis for lines on one plane, t_d=30ps. circle:T=0.7, triangle: T=0.6, square: T=0.5, diamond: T=0.4, cross: T=0.3, plus: T=0.2, star: T=0.16.

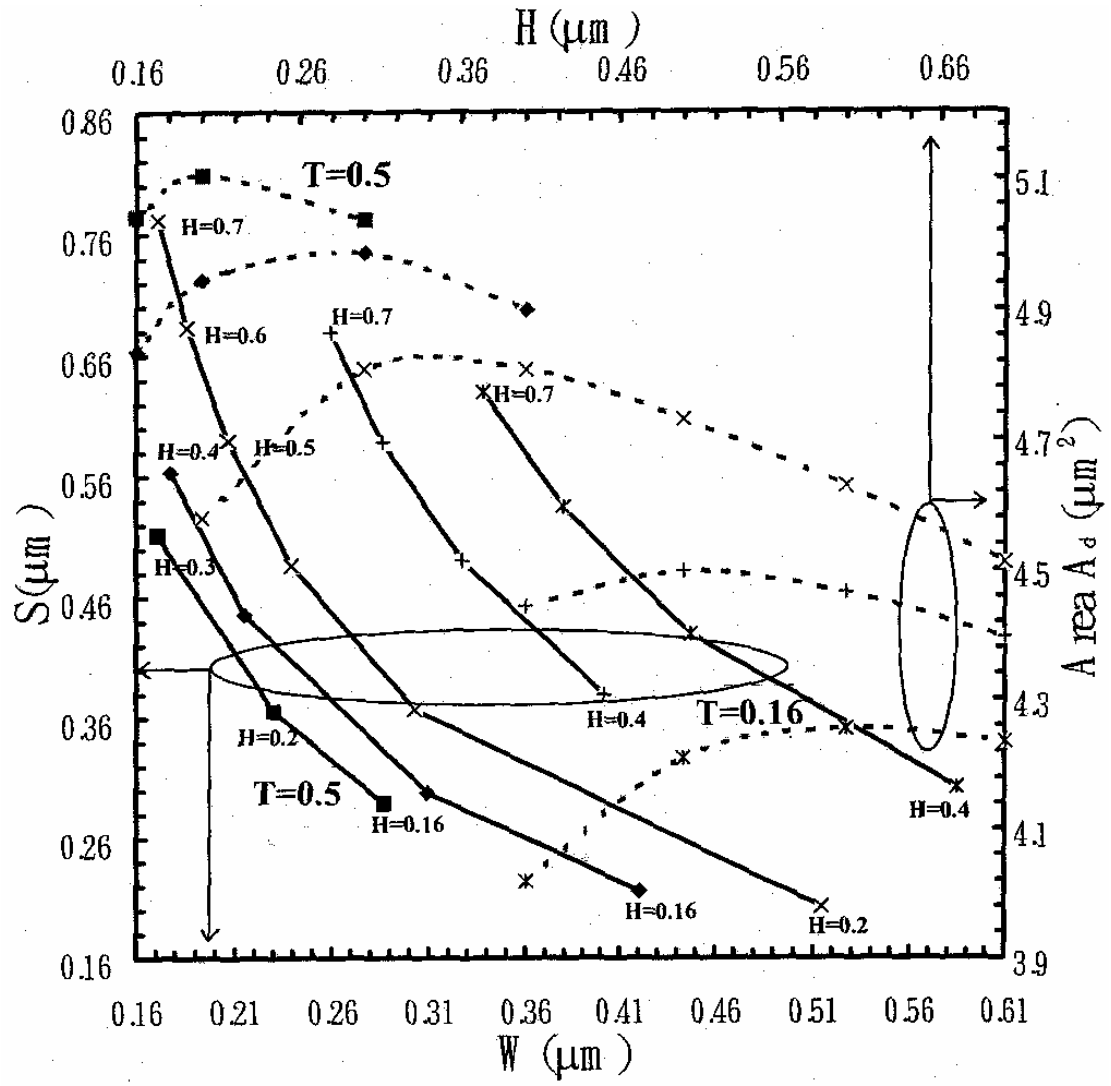


Figure 5. 5 Design target and A_d analysis for lines on one plane, t_d=70ps. circle: T=0.7, triangle: T=0.6, square: T=0.5, diamond: T=0.4, cross: T=0.3, plus: T=0.2, star: T=0.16.

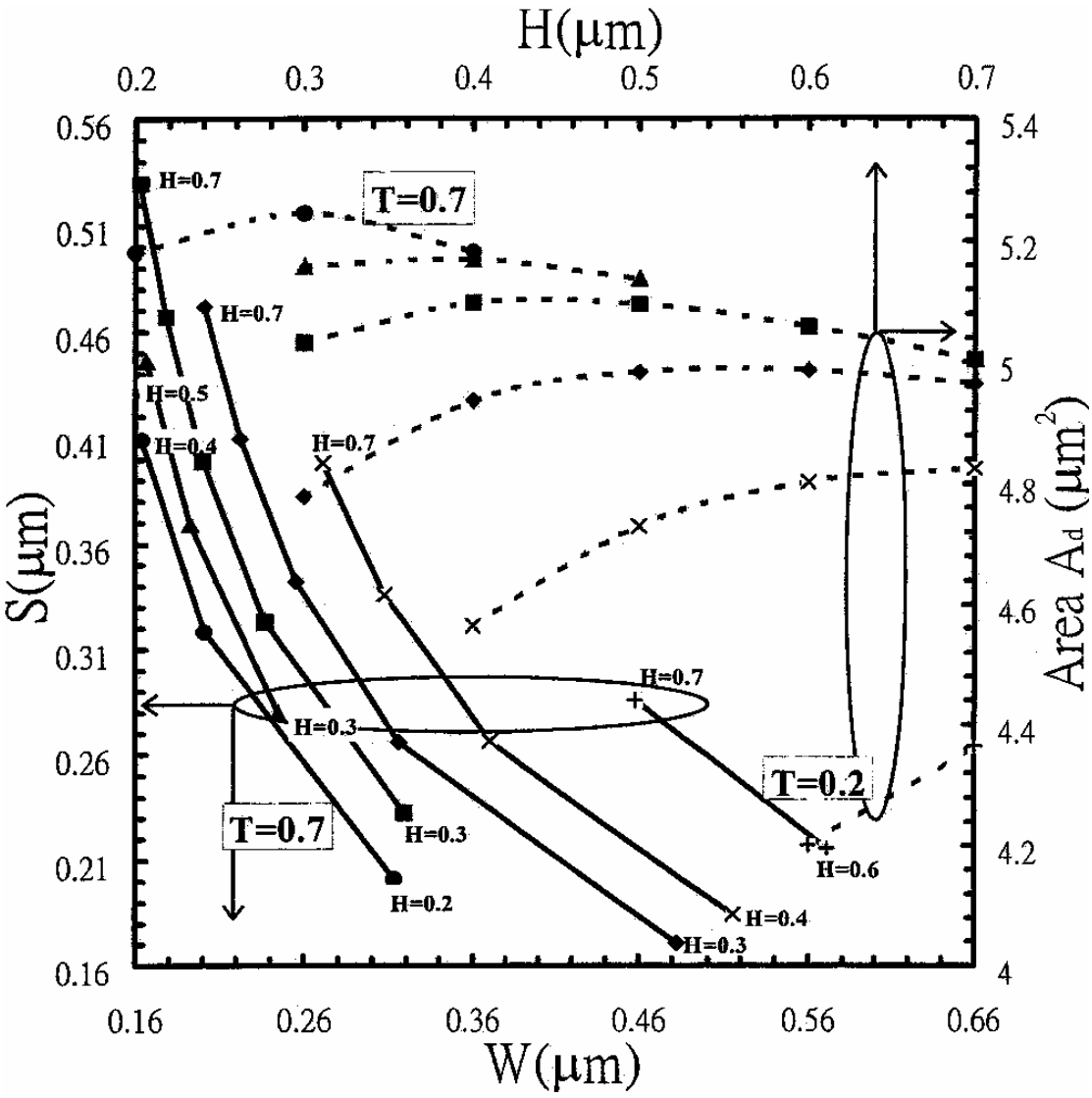


Figure 5. 6 Design target and A_d analysis for lines between two planes, t_d=70ps. circle: T=0.7, triangle: T=0.6, square: T=0.5, diamond: T=0.4, cross: T=0.3, plus: T=0.2, star: T=0.16.

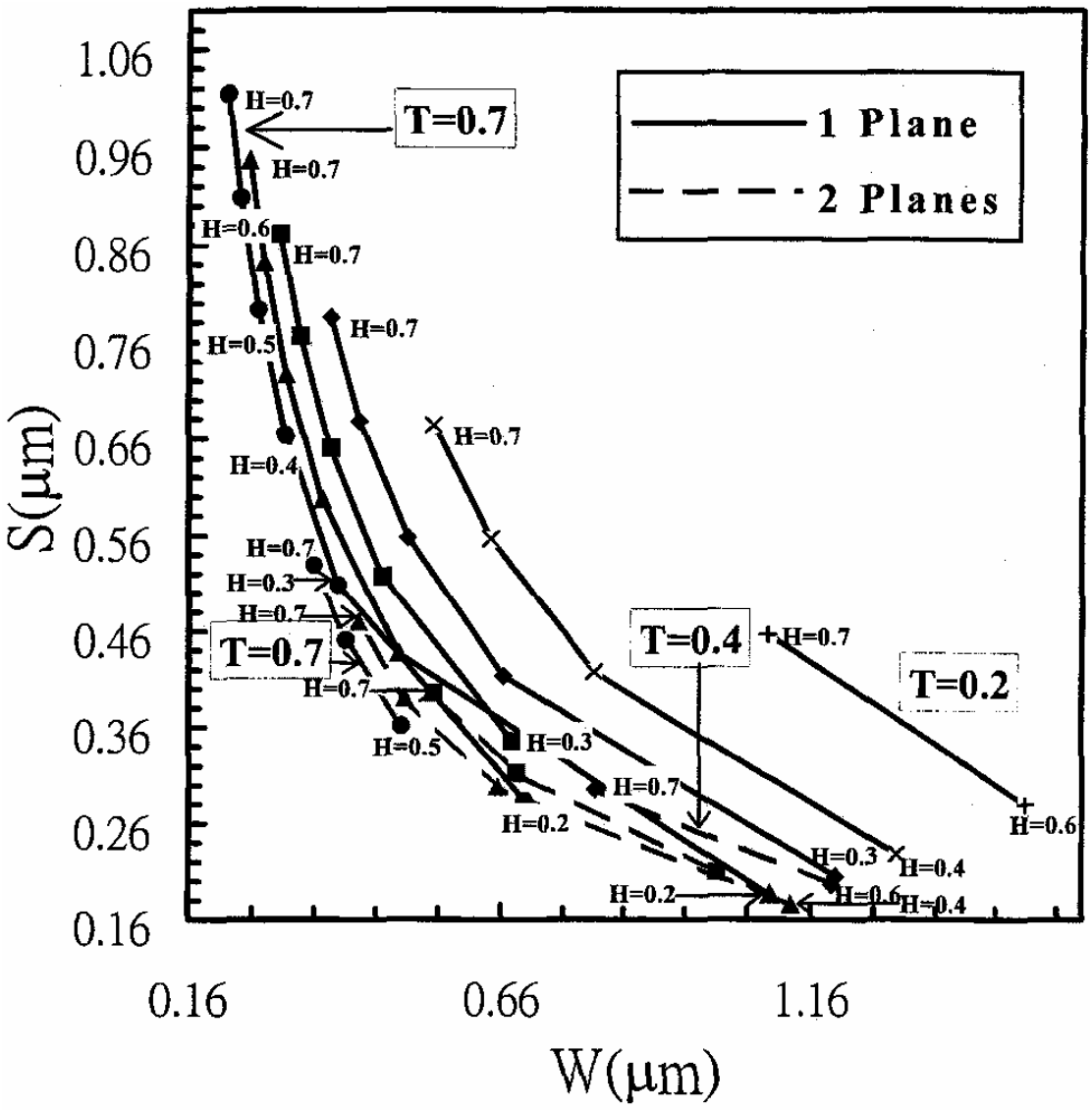


Figure 5. 7 Comparison of design target for lines on one plane and between two planes, t_d=30ps. circle:T=0.7, triangle: T=0.6, square: T=0.5, diamond: T=0.4, cross: T=0.3, plus: T=0.2, star: T=0.16.

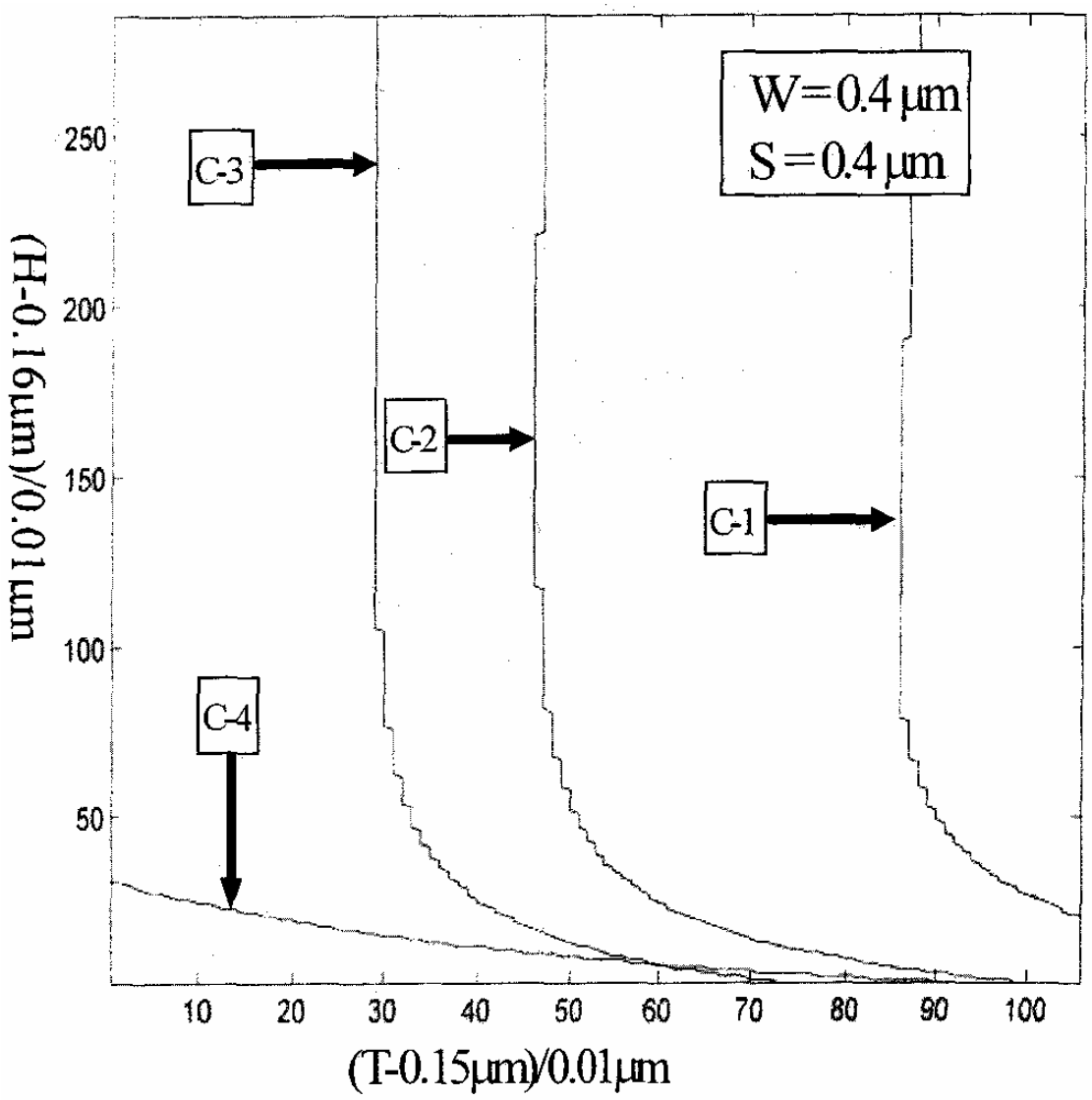


Figure 5. 8 Process contour analysis of delay and crosstalk for structure W=0.4 μ m and S=0.4 μ m.

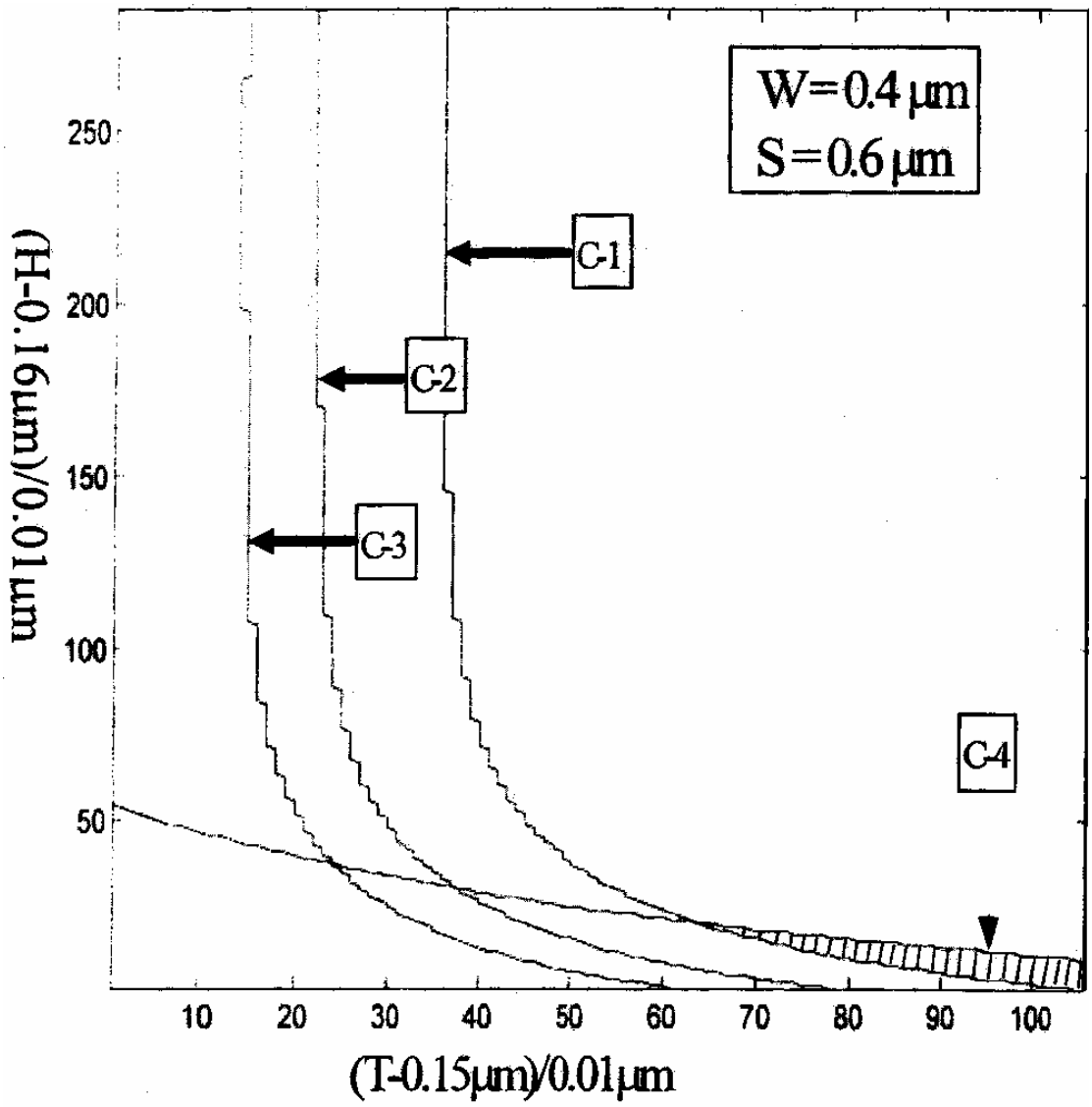


Figure 5. 9 Process contour analysis of delay and crosstalk for structure W=0.4 μ m and S=0.6 μ m.

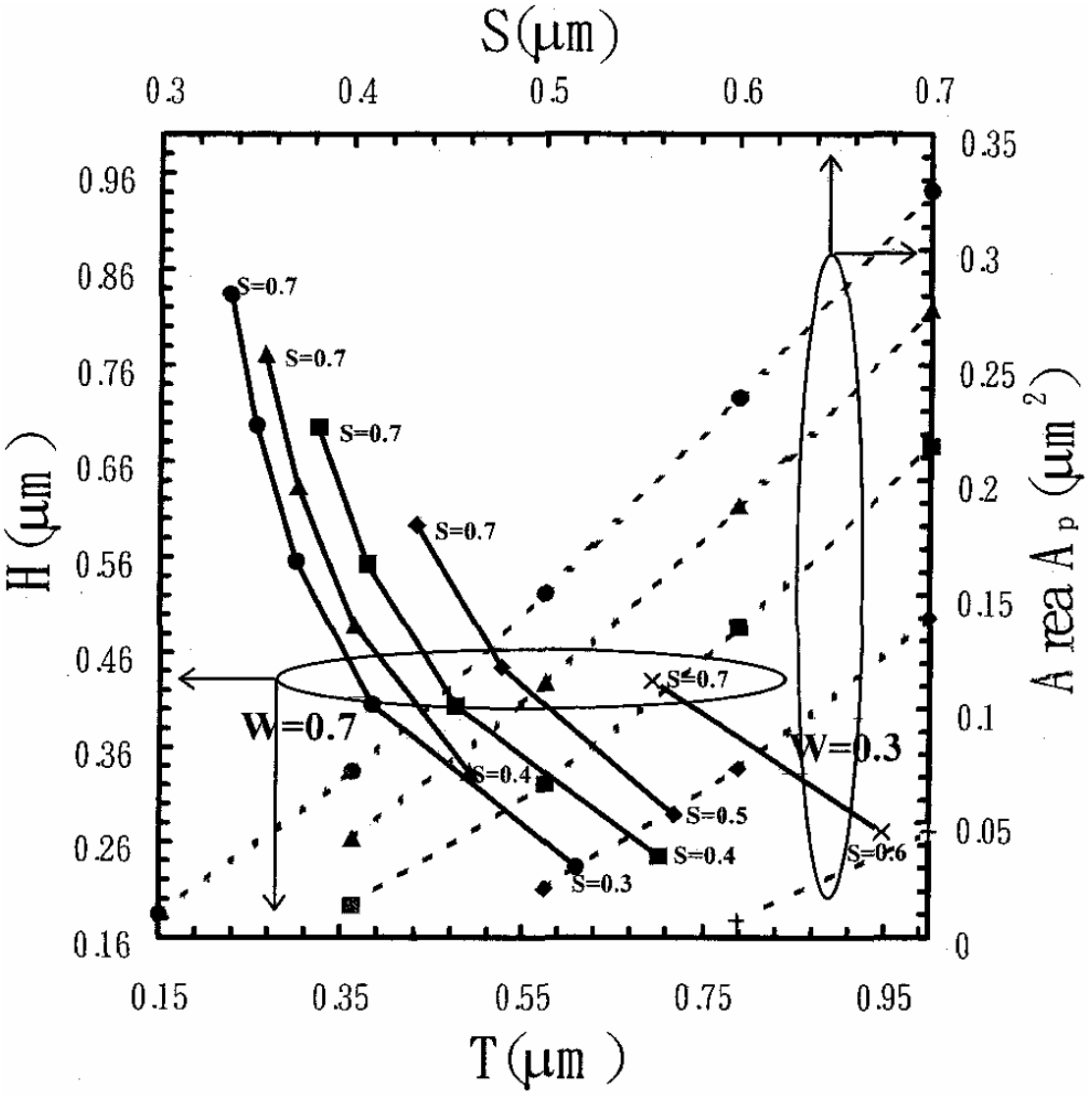


Figure 5. 10 Process target and *Ap* distribution for lines on one plane, t_d=30ps. circle: *W*=0.7, triangle: *W*=0.6, square: *W*=0.5, diamond: *W*=0.4, cross: *W*=0.3.

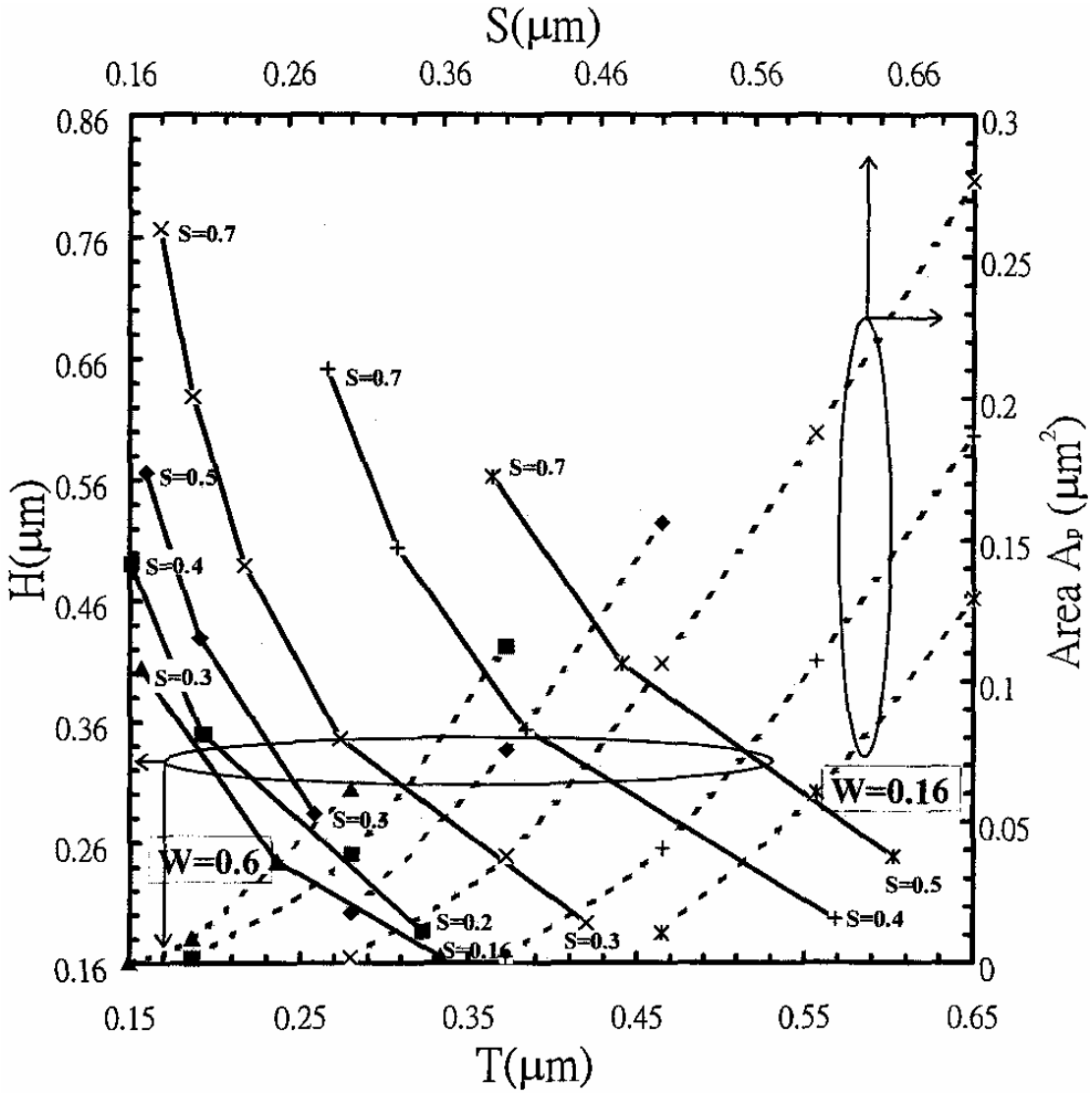


Figure 5. 11 Process target and *Ap* distribution for lines on one plane, t_d=70ps. triangle: *W*=0.6, square: *W*=0.5, diamond: *W*=0.4, plus: *W*=0.3, cross: *W*=0.16.

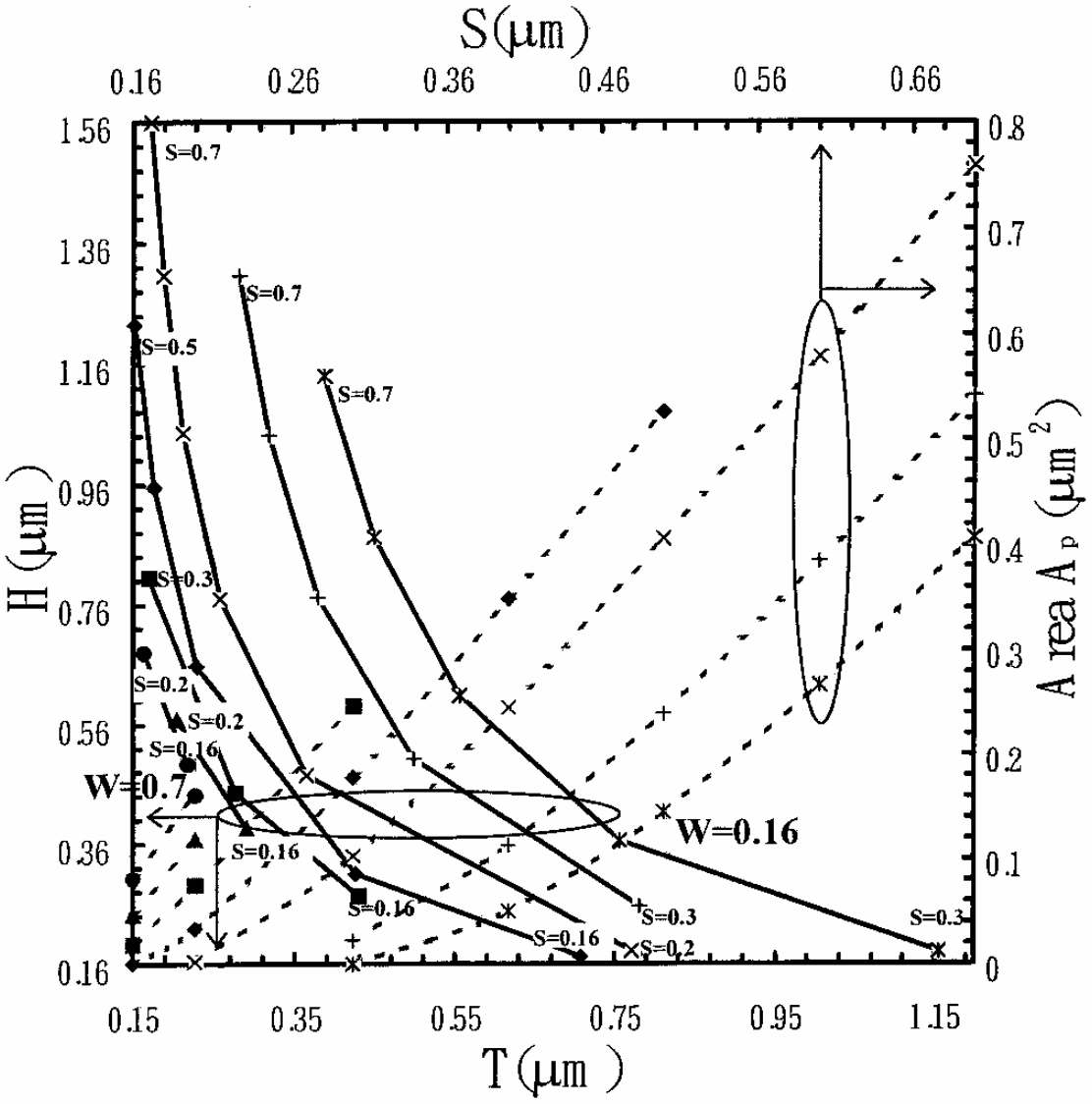


Figure 5. 12 Process target and *Ap* distribution for lines between two planes, t_d=70ps. circle: *W*=0.7, triangle: *W*=0.6, square: *W*=0.5, diamond: *W*=0.4, plus: *W*=0.3, cross: *W*=0.16.

Chapter 6 Statistical Analysis and Optimization for VLSI Interconnection

The yield loss will worsen in future technologies due to increasing process variations. This is because as the feature sizes decrease, the ability to control the manufacturing spread or accuracy of a given feature size or doping concentration is also decreasing. Along with increased process variations, the uncertainty caused by design is also increasing such as interconnect coupling noise and delay. The impact of these process variations on performance has been increasing with each process technology generation. For example, with increasing clock and data frequency, the variation become a larger fraction of the total clock period. However, the traditional corner based analysis provides pessimism or optimism design. The pessimism design would lead to the long design cycle to meet the spec and impact time to market. And the process corner analysis method not guarantee the worst case of chip design. Hence, the method to accounts the performance impact of all portion of the parameter variation in a single analysis is important. Therefore, variations in the process, whether device or interconnect variations, will be a major issue for nano-CMOS designs. For the design to survive the much larger variations, the methodology must have provisions to deal with variations. The traditional worst corner methodology becomes increasingly meaningless and will lead to costly overdesign at the expense of chip area and power in some cases and in other cases missing an important worse-case condition entirely.

For a specified process node, different design may have different parametric yield. That is, same process variation has significant different impacts on performance

due to various sensitivity of each design parameters.

The critical variables in timing analysis is no longer just transistor critical dimension as interconnect become critical. Moreover, the interconnect dimension on real silicon is a statistic distribution function instead of exact value drawn on layout especially in deep submicron era, which small variation could be significant on performance fluctuation [6.1][6.2].

The growth of process variability in scaled CMOS technology requires special addressed in the design of high performance SOC. To achieve good yield in production, worst case design method is usually used to design the SOC considering process variation. However, by putting too much guardband at everywhere on the design would probably results in un-acceptable performance, die size, power consumption and project schedule. Hence, the traditional corner based analysis provides pessimism or optimism design. And what makes thing worse is that the corner analysis methods not guarantee the real worst case of chip design. Hence, the method to accounts the performance impact of all portion of the parameter variation in a single analysis is important. If designer could have insight in which nets are critical to the process variation in advanced, the chip could be designed without scarifying too much performance and schedule. Therefore, the chip analysis considering statistical dimension and spacing of nearby wire are the key for high-end SOC design.

The first contribution of this thesis is to presents the simple and yet accuracy methods to calculate the statistical models of interconnect capacitance, delay and crosstalk. Second, we propose method to help both design and process engineer to have insight of the structure that the process and design window which is process variation insensitivity or, on the contrary, which process and design window are very sensitivity to process variation. The ability to screen-out the process sensitivity layout

is very helpful to increase the yield and optimize design. And the techniques help EDA vendor to have the method of pre-running techniques that identify interconnect that have a larger or smaller sensitivity without running a full statistical timing analysis is very valuable. Furthermore, the design guidelines to adjust the layout to the process insensitivity region are also proposed. Therefore after the discuss of this section, we could achieve

(A) *layout design techniques that can deal with variability*, and

(B) *process window that reduce performance impact due to variability*

(C) the method to quickly identify layout design that are sensitivity to process variation

6-1 Variation Source and Impact on Performance

The variation sources, for examples, includes variation of optical exposure duration during chip fabrication, the len aberration and other lithography effects[6.3, 6.4] which cause the variation of interconnect width control. Metal thickness variation within same layer or different layers due to erosion and dishing effect of copper CMP process is serious. The effective dielectric constant variation due to etch, strip, clean and re-work are serious especially for porous dielectric materials and need to be considered in performance impact. The variation of metal resistively is significant due to copper metallization [6.5].

Before we start the detail discussion of the statistical modeling, let's first look at the categories of variation sources.

6-1.1 Process Variations

Process variations are fluctuations in the value of process parameters observed after fabrication. These variations result from a wide range of factors during the fabrication process which determine the range of variations. It is obvious that the process variations

would cause the variations of performance. The performance distribution causes the fraction of manufactured devices fail to meet the defined performance specification in design phase. The performance yield loss is defined as parametric yield loss. These fail devices are not defect type fail (which cause wire open or short), which defined as manufacturing yield loss, and they could function normal at different frequencies. For a microprocessor product, companies perform speed-binning and sell higher frequency parts at higher cost and sell lower frequency parts at lower cost. However, in ASIC business, chips can only be sold only if it meets frequency specification. Furthermore, all samples (just meet specification and better than specification) of ASIC products are sold at the same price. Hence, again, for ASIC business, over-designed product to consider the variation of process will not gain more profits from fraction of the devices with better performance and, on the other hand, the defect yield may increase due to increased area. On the other hand, design without consider the process variation will suffer parametric yield loss and defect related yield loss also.

6-1.2 Environmental Variations

These variations indicate the variations in the surrounding environment. This includes temperature variations, power supply variations and power droop or ground bounce due to SSN. The static and/or dynamic IR- drop would introduced “noise” that transistors “see” different supply voltage at different locations and at different times (depends on switching activity). A reduced power supply lowers the drive strengths of devices and hence degrades performance. The increased temperature results in performance degradation for devices and interconnects. Power supply and temperature variation are generally not treated statistically, since every shipped chip is required to operate without failures caused by this variation. Hence, design team focus on minimizing temperature and power supply variations as much as possible.

6-1.3 Modeling Variations

The variation result from the fact that the power and delay models used to perform design analysis and optimization are inaccuracy and do not perfectly capture device characteristics. The modeling errors happens at different design stage (Fig. 6.1). This is especially critical for SOC design because the timing models provided by IP vendor or cell lib vendor may have different model accuracy due to different modeling methods [6.4]. These models, if conservative, will make it harder to meet design specifications and larger die size and lower yield due the die size, whereas aggressive models (under design) will result in yield loss. In Traditional design method, the conservative approach is typically used to account for the modeling variation and over design is used. Modeling variation are generally not treated statistically. How to design the chip with high accuracy model is an important topic to reduce the design and production impact due to modeling variations.

6-1.4 Dynamic Variations

There are physical effects that results in a change in process parameter with time. Supply voltage and temperature fluctuations may vary from circuit operation. It depends on circuit activity and hard to be compensated. These effects includes phenomenon such as hot electrons, electron migration. Any of these dynamic effects should be considered during chip design phase since they may result in timing issues and hard defects during operation or burn-in and become chip reliability and quality issue. The analysis of these variations is difficult since they become issue after reasonable operation time and the circuit simulation tool may not support on this. Therefore, it may need some accelerated testing method such as burn-in for voltage and temperature stress on some weak point of the chip.

As the feature sizes decrease, the ability to control the manufacturing spread of variations mentioned above is also more difficult. Hence, we will discuss the impact of performance due to variation and solution to reduce the impact due to the variation in next few sections.

6-2 *Modeling Of Variation Source*

Although all variation sources are important for a manufacturability design, we will focus on the variation of process variation which includes all the parameters of interconnection. Assuming a fixed wire pitch, line width (*W*) and spacing (*S*) are anti-correlated by one. There are not universal agreements that the variations (in the process) can always be modeled as random variables and their corresponding distribution may be. Nevertheless, there are many literatures based on the assumption that the variations are random and that they can be modeled by normally distributed (Gaussian) random variables (RVs). This thesis will also be based on this assumption. That is, wire spacing variation is the negative of wire width variation. Metal thickness (*T*) and interlevel dielectric (ILD) thickness (*H*) are independent variation parameter. The dielectric constant and resistivity of metal lines are models as independent random variable. All parameters variations are modeled as normal distribution with σ_i and μ_i where σ_i and μ_i are standard deviation and mean of *i*th parameters.

6-3 *Model Approximation Method and Characterization*

This section we propose the method to estimate the variation transmitted by the inputs to the output based on the relationship between the inputs (interconnect nominal values and variation of the individual inputs) and the outputs (capacitance, dynamic power, delay and crosstalk) as shown in Fig. 6.3. We will propose the method to reduce the formula for the optimization design.

To discuss how the design and process parameter response on delay and crosstalk noise due to process variations, we could run parametric analysis by providing many trial runs to get enough data to see how the output response and calculate variation accordingly. However, by using this method have some drawbacks. First, this would be time consuming to run so many simulations. Second, the variation observed during the study may not

representative of the full range of variation. Third, this approach only suitable for parametric analysis and could be difficult in applying to the optimization design. Hence, in this thesis, we present an approach that estimates the standard deviations of the output response for design and process parameters. Therefore, designer could save a lot of computation time and optimization design could be done by exploring different scenarios by using these methods. We could then easily tell how the standard deviation of the response corresponding to the variations of specified target inputs and provide the solution to handle these variations.

Therefore, the standard deviation equation for resistance, capacitance, delay and crosstalk respective to all design and process parameters will be presented in this paper.

To derive the closed form of standard deviation for interconnect capacitance, delay time and crosstalk, we introduce the variation transmission method (or statistical tolerance analysis, propagation of errors). Here Y is the response of inputs $(x_1, x_2, \ldots, x_n)$ and assume the polynomial highest order is quadratic

$$Y = c_0 + c_1 f_1(x_1, \ldots, x_n) + c_2 f_2(x_1, \ldots, x_n) + \ldots + c_m f_m(x_1, \ldots, x_n). \quad (6.1)$$

where c_i are the constants, and the $f_i()$ are the functions of x_i. x_i is not correlated is assumed in the following derivation. For parameters which are correlated, the PCA (Principle Component Analysis) could be used to derive the non-correlated parameters. In the quadratic polynomial the $f_i()$ are restricted to the following forms:

$$f(x_1, x_2, \ldots, x_n) = x_i,$$

$$f(x_1, x_2, \ldots, x_n) = x_i^2,$$

$$f(x_1, x_2, \ldots, x_n) = x_i x_j \qquad i \neq j.$$

The variance of the sum (correlated or not correlated) is calculated as

$$\mathrm{VAR}\left[\sum_{i=1}^{n} f_i\right] = \sum_{i=1}^{n}\sum_{j=1}^{n}\mathrm{COV}\left(f_i, f_j\right). \tag{6. 2}$$

It indicates that the variance of a polynomial (f_i) equals to the sum of all elements in the covariance matrix of the components.

Covariance has properties of

$$\mathrm{COV}\left[f_i, f_i\right] = \mathrm{VAR}\left[f_i\right], \tag{6. 3}$$

$$\mathrm{COV}\left[c_i f_i, c_j f_j\right] = c_i c_j \,\mathrm{COV}\left[f_i, f_j\right]. \tag{6. 4}$$

In the covariance expression, the order of two terms not restricted; hence,

$$\mathrm{COV}[f_i, f_j]=\mathrm{COV}[f_j, f_i]. \tag{6. 5}$$

And if $f_i()$ and $f_j()$ have no x_i in common (no correlation), then

$$\mathrm{COV}[f_i, f_j] = 0. \tag{6. 6}$$

Hence, the square of standard deviation of Y is calculated from (6.2)–(6.6)as

$$\sigma_Y^2 = c_1^2\,\mathrm{VAR}\left[f_1(x_1, x_2, \ldots, x_n)\right] + c_2^2\,\mathrm{VAR}\left[f_2(x_1, x_2, \ldots, x_n)\right] + \ldots$$

$$c_m^2\,\mathrm{VAR}\left[f_m(x_1, x_2, \ldots, x_n)\right] + 2c_1c_2\mathrm{COV}\left[f_1(x_1, x_2, \ldots, x_n), f_2(x_1, x_2, \ldots, x_n)\right]$$

$$+ 2c_1c_3\mathrm{COV}\left[f_1(x_1, x_2, \ldots, x_n), f_3(x_1, x_2, \ldots, x_n)\right] + \ldots +$$

$$2c_{m-1}c_m \mathrm{COV}\left[f_{m-1}(x_1, x_2, \ldots, x_n), f_m(x_1, x_2, \ldots, x_n) \right],$$

(6. 7)

where VAR[] represents the variance and COV[] represents the covariance. There are total m variance terms and m(m-1)/2 covariance terms. To expansion (6-2), the required expressions are listed

$$\mathrm{VAR}[x_i] = \sigma_i^2,$$

$$\mathrm{VAR}[x_i^2] = 4t_i^2 \sigma_i^2 + 2\sigma_i^4,$$

$$\mathrm{VAR}[x_i x_j] = t_i^2 \sigma_j^2 + t_j^2 \sigma_i^2 + \sigma_i^2 \sigma_j^2,$$

$$\mathrm{COV}[x_i, x_i^2] = 2t_i \sigma_i^2,$$

$$\mathrm{COV}[x_i, x_i x_j] = t_j \sigma_i^2,$$

$$\mathrm{COV}[x_i^2, x_i x_j] = 2\, t_i t_j \sigma_i^2,$$

$$\mathrm{COV}[x_i x_j, x_i x_k] = t_j t_k \sigma_i^2,$$

where t_i represent the nominal value of x_i.

For non-polynominal equation as capacitance, delay time and crosstalk formula, we could taking first order Taylor series expansion of ($x_1, x_2, \ldots, x_n$) and apply the procedures as variation of polynomial discussed above.

Said that $f(x_1, x_2, \ldots, x_n)$ is the response function and it is an non-polynomial equation and we will derive the standard deviation for it. The 2nd order Taylor series expansion for $f(x_1, x_2, \ldots, x_n)$ at ($t_1, \ldots t_n$) is calculated as

$$f(x_1,...,x_n) = f(t_1,...,t_n) + (x_1 - t_1)\frac{\partial f}{\partial x_1} + ... + (x_n - t_n)\frac{\partial f}{\partial x_1}$$
$$+ \frac{1}{2}(x_1 - t_1)^2 \frac{\partial^2 f}{\partial x_1^2} + ... + \frac{1}{2}(x_n - t_n)^2 \frac{\partial^2 f}{\partial x_n^2}$$
$$+ (x_1 - t_1)(x_2 - t_2)\frac{\partial f}{\partial x_1}\frac{\partial f}{\partial x_2} + ... + (x_{n-1} - t_{n-1})(x_n - t_n)\frac{\partial f}{\partial x_{n-1}}\frac{\partial f}{\partial x_n} \quad .$$

(6. 8)

By set $x_i' = x_i - t_i$, we re-write (6.5) as

$$f(x_1',...,x_n') = f(0,...,0) + x_1'\frac{\partial f}{\partial x_1'} + ... + x_n'\frac{\partial f}{\partial x_n'}$$
$$+ \frac{1}{2}(x_1')^2 \frac{\partial^2 f}{\partial x_1'^2} + ... + \frac{1}{2}(x_n')^2 \frac{\partial^2 f}{\partial x_n'^2}$$
$$+ x_1'x_2'\frac{\partial f}{\partial x_1'}\frac{\partial f}{\partial x_2'} + ... + x_{n-1}'x_n'\frac{\partial f}{\partial x_{n-1}'}\frac{\partial f}{\partial x_n'} \quad .$$

(6. 9)

Based on the analogy between eq. (6.1) and (6.5), we could use similar procedures above to derive the standard deviation as

$$\sigma_f^2 = g_1(t_1,t_2,...,t_n)^2\sigma_1^2 + g_2(t_1,t_2,...,t_n)^2\sigma_2^2 + ... + g_n(t_1,t_2,...,t_n)^2\sigma_n^2$$
$$+ \frac{1}{2}g_{1,1}(t_1,t_2,...,t_n)^2\sigma_1^4 + ... + \frac{1}{2}g_{n,n}(t_1,t_2,...,t_n)^2\sigma_n^4$$
$$+ g_{1,2}(t_1,t_2,...,t_n)^2\sigma_1^2\sigma_2^2 + g_{1,3}(t_1,t_2,...,t_n)^2\sigma_1^2\sigma_3^2$$
$$+ ... + g_{n-1,n}(t_1,t_2,...,t_n)^2\sigma_{n-1}^2\sigma_n^2 \quad ,$$

(6. 10)

where $g_i(x_1,\cdots,x_n) = \partial f(x_1,\cdots,x_n)/\partial x_i$ and $g_{i,j}(x_1,\cdots,x_n) = \partial f(x_1,\cdots,x_n)/\partial x_i \partial x_j$

To simplify the standard deviation formula, we have two assumptions. First, we assume that that the variables $x_1,...,x_n$. are all independent. Second, we assume that the

higher order terms of (6.6) could be ignored without too much error introduced. Therefore, only the first order terms are retained. So, for $f(x_1,\ldots,x_k,\ \ldots\ ,x_n)$ be a function of n variables $x_1,\ldots,x_n$. The variance of each variable is given by σ_k. Then, the variance of f, defined as σ_f, is calculated as:

$$\sigma_f = \left(\sum_{k=1}^{n} \left(\sigma_k \frac{\partial f(x_1,\cdots,x_n)}{\partial x_k} \right)^2 \right)^{0.5}, \qquad (6.11)$$

where $\frac{\partial f(x_1,\cdots,x_n)}{\partial x_k}$ is the partial derivative of f for the k-th variable.

To verify the accuracy of the approximation model, we use Monte Carlo simulation to verify the approximation formulas. We will prove in later section that the assumption of neglecting higher order terms in (6.4) does not have significant impact on the accuracy.

6-4 *Statistical Capacitance, delay and crosstalk Model*

The methods for modeling interconnect capacitance, delay and crosstalk while considering variability in the interconnect process and design parameters are discussed in this section. All of the models presented in this paper include design parameters (line width and spacing) and process parameters (metal thickness, dielectric thickness and dielectric constant); hence, this method preserves all correlations and it is very useful in sensitivities evaluation. In these methodologies, capacitance, delay and crosstalk are modeled as a function of the design and process parameters and the impact due to the variation are modeled accordingly.

Monte Carlo simulations are another method to provide the analysis of the effects of process variations. However, Monte Carlo techniques are time consuming and cannot be used to efficiently to provide guides to the optimization design. Hence, the analytical methods are very useful to achieve performance variation analysis and optimization design.

Monte Carlo simulation methods are used to evaluate the accuracy obtained by the analytical models newly developed in this thesis. By doing this, we could study (1) the real impact of process variation on interconnect performance, and (2) provide interconnect design guideline to design engineers and process engineers for them to reduce the impact on performance.

Capacitance Model Considering Variations

Two generic interconnection structures are discussed in this thesis shown in Fig. 6-4. In Fig.6-4, W is the wire width, T is the wire thickness, H is the inter-layer dielectric (ILD) thickness and S is the spacing between two wires in the same metal layer. To accurate estimate the delay and crosstalk, the capacitance models that could separate the lumped total capacitance (c_{wire}) into area-fringe capacitance (c_{af}) and line-to-line capacitance (c_{ll}) is necessary. The area-fringe capacitance (c_{af}) and line-to-line capacitance (c_{ll}) are developed in chapter 2. We use herein the physical-based empirical interconnection capacitance models presented in previous chapter. c_{af} contributes to the dynamic power, delay of signal and c_{ll} is related to the amount of coupled noise, the dynamic power and the signal delay. Hence, the variation of interconnect dimension and material indicate the variations on dynamic power, delay of signal and crosstalk noise. Without considering the variations in the design phase, will cause issue for nano-CMOS designs.

The change in capacitances and resistances due to variations in interconnect dimensions can be modeled by the simple linear approximation

$$C_{ll} = C_{ll,nom} + k_W^{cll}\Delta W + k_T^{cll}\Delta T + k_H^{cll}\Delta H \quad , \qquad (6.12)$$

$$C_{af} = C_{af,nom} + k_W^{caf}\Delta W + k_T^{caf}\Delta T + k_H^{caf}\Delta H\ , \tag{6. 13}$$

$$C_{total} = 2C_{ll} + C_{af} = C_{total,nom} + k_W^{total}\Delta W + k_T^{total}\Delta T + k_H^{total}\Delta H\ , \tag{6. 14}$$

$$\mathrm{R} = \mathrm{R}_{nom} + k_W^{\mathrm{R}}\Delta W + k_T^{\mathrm{R}}\Delta T + k_\rho^{\mathrm{R}}\Delta\rho\ .$$

Here, $C_{ll,nom}$, $C_{af,nom}$, $C_{total,nom}$, R_{nom} represent nominal capacitance values of line-to-line, area-fringe and total capacitance, computed when the wire dimensions are at their nominal values. ΔW, ΔT, and ΔH represent the change in metal width, metal thickness, and inter layer dielectric thickness respectively due to process variation. The line width (W) and spacing (S) are anti-correlated by one. That is, wire spacing variation is the negative of wire width variation. The coefficients k_W^{cll}, k_T^{cll}, k_H^{cll}, k_W^{caf}, k_T^{caf}, k_H^{caf}, k_W^{ctotal}, k_T^{ctotal}, k_H^{ctotal}, k_W^{R}, k_T^{R} and k_ρ^{R} are the modeling coefficients in the linearized model and calculated as

$$k_W^{caf} = \partial C_{af}/\partial W\ ,\ k_T^{caf} = \partial C_{af}/\partial T\ ,\ k_H^{caf} = \partial C_{af}/\partial H\ ,$$

$$k_W^{cll} = \partial C_{ll}/\partial W\ ,\ k_T^{cll} = \partial C_{ll}/\partial T\ ,\ k_H^{cll} = \partial C_{ll}/\partial H\ ,$$

$$k_W^{ctotal} = 2k_W^{cll} + k_W^{caf}\ ,\ k_T^{ctotal} = 2k_T^{cll} + k_T^{caf}\ ,\ k_H^{ctotal} = 2k_H^{cll} + k_H^{caf}\ ,$$

$$k_W^{\mathrm{R}} = \partial \mathrm{R}/\partial W\ ,\ k_T^{\mathrm{R}} = \partial \mathrm{R}/\partial T \text{ and } k_\rho^{\mathrm{R}} = \partial R/\partial\rho\ .$$

Reference [6.7] proposes a methodology that requires a one-time nominal capacitance extraction after which look-up tables are used to calculate delta capacitances due to geometric parameter variations. In this paper, we use empirical capacitance modeling equations in Chapter 3 to compute linear coefficients. From equation (6.5), we could calculate the standard deviation of C_{wire} in terms of the standard deviations of wire width-σ_W, wire spacing-σ_S, wire thickness-σ_T, inter-layer dielectric thickness-σ_H, metal resistivity-σ_ρ and dielectric constant-$\sigma_{\varepsilon_{eff}}$.The mean function are written as

$$E(C_{wire}) = C_{wire}(W_{nom}, S_{nom}, T_{nom}, H_{nom}, \varepsilon eff_{nom}) . \quad (6.15)$$

The standard deviation is written as

$$\sigma_{C_{wire}} = \left(\left(\sigma_W \frac{\partial C_{wire}}{\partial x_W} \right)^2 + \left(\sigma_T \frac{\partial C_{wire}}{\partial x_T} \right)^2 + \left(\sigma_H \frac{\partial C_{wire}}{\partial x_H} \right)^2 + \left(\sigma_{Eeff} \frac{\partial C_{wire}}{\partial x_{\varepsilon eff}} \right)^2 \right)^{0.5} , \quad (6.16)$$

where W_{nom}, S_{nom}, T_{nom}, H_{nom}, εeff_{nom} represent the wire dimensions at nominal values. The linearity assumption model is compared to Monte Carlo simulation. In this study, Monte Carlo simulation with 10000 runs where the variation sources all vary simultaneously and independently. That is, each model of process variability provides 10000 sets of random parameter values. As showed in Fig. 6-5, the capacitance distribution of structure-A with nominal $\{W, S, T, H, \rho, \varepsilon_{eff}\}$=$\{0.15\ \mu m, 0.15\ \mu m, 1.2\ \mu m, 1\ \mu m, 2.65\ \mu \Omega$-cm, 3.9$\}$ for a 30% 3σ variation in all parameters. The accuracy of mean and standard deviation between the model and Monte Carlo simulation is good. The accuracy is further investigated by change the amount of parameter variation as showed in Fig. 6-6. Comparing the standard deviations in capacitance obtained using models mentioned above and those obtained using Mote Carlo simulation for a set of random generated test points, the error in standard deviation is found to be within 2.5% respectively for 30% 3σ variation in all parameters. The results show the validation of the linear model proposed.

Since the interconnect capacitance is correlated to the dynamic power, which is important parameter for high performance and low power application. Power variation also draws many attentions recently and may suffer yield loss due

to process variation [6.7]. So, the variation of dynamic power due the process variation is discussed here.

The dynamic power dissipation include both interconnects and gates is given as

$$P_d = \sum SfV_{dd}^2 (C_{wire} + C_{gate}), \quad (6.17)$$

where the summation is over all interconnect and gates of chip. C_{wire} and C_{gate} are the capacitance of interconnect and a gate, V_{dd} is the power supply voltage, f is the operation frequency and S is the switching probability. From eq. (6-11), the dynamic power is proportional to the value of C_{wire}. and hence the variation of dynamic power is proportional to the variation of C_{wire}.

Delay time and crosstalk model Considering Variations

We consider the delay (t_d) and crosstalk (V_p) as

$$t_d = 2.3RC, \quad (6.18)$$

$$V_p = C_{ll} / C_{total}. \quad (6.19)$$

The method mentioned in this paper could be extended to consider the delay distribution by using other higher order delay model mentioned in Chapter 4. Hence, the standard deviation of t_d in terms of the standard deviations in physical dimensions σ_W, σ_S, σ_T, σ_H, and σ_{Eeff} is calculated as

$$E(t_d) = t_d(W_{nom}, S_{nom}, T_{nom}, H_{nom}, Eeff_{nom}), \quad (6.20)$$

$$E(V_p) = V_p(W_{nom}, S_{nom}, T_{nom}, H_{nom}, Eeff_{nom}). \quad (6.21)$$

The standard deviation of delay and crosstalk are written as σ_{t_d} and σ_{V_p}

$$\sigma_{t_d} = \left(\left(\sigma_W \frac{\partial t_d}{\partial W}\right)^2 + \left(\sigma_S \frac{\partial t_d}{\partial S}\right)^2 + \left(\sigma_T \frac{\partial t_d}{\partial T}\right)^2 + \left(\sigma_H \frac{\partial t_d}{\partial H}\right)^2 + \left(\sigma_{Eeff} \frac{\partial t_d}{\partial Eeff}\right)^2 \right)^{0.5}, \quad (6.22)$$

$$\sigma_{V_p} = \left(\left(\sigma_W \frac{\partial V_p}{\partial W}\right)^2 + \left(\sigma_S \frac{\partial V_p}{\partial S}\right)^2 + \left(\sigma_T \frac{\partial V_p}{\partial T}\right)^2 + \left(\sigma_H \frac{\partial V_p}{\partial H}\right)^2 + \left(\sigma_{Eeff} \frac{\partial V_p}{\partial Eeff}\right)^2 \right)^{0.5}. \quad (6.23)$$

Instead of calculating (6.22) and (6.33) to get the standard deviation for delay and crosstalk, we propose another better method below

$$\begin{aligned} t_d &= 2.3RC = 2.3\left(R_{nom} + k_W^R \Delta W + k_T^R \Delta T + k_\rho^R \Delta\rho\right)\times \\ &\quad \left(C_{total,nom} + k_W^{ctotal} \Delta W + k_T^{ctotal} \Delta T + k_H^{ctotal} \Delta H + k_{\varepsilon eff}^{ctotal} \Delta \varepsilon eff\right) \\ &= 2.3 \begin{pmatrix} R_{nom} C_{total,nom} + R_{nom}\left(k_W^{ctotal} \Delta W + k_T^{ctotal} \Delta T + k_H^{ctotal} \Delta H + k_{\varepsilon eff}^{ctotal} \Delta \varepsilon eff\right) + \\ C_{total,nom}\left(k_W^R \Delta W + k_T^R \Delta T + k_\rho^R \Delta\rho\right) + \\ k_W^R\left(k_W^{ctotal} \Delta W^2 + k_T^{ctotal} \Delta W \Delta T + k_H^{ctotal} \Delta W \Delta H + k_{\varepsilon eff}^{ctotal} \Delta W \Delta \varepsilon eff\right) + \\ k_T^R\left(k_W^{ctotal} \Delta T \Delta W + k_T^{ctotal} \Delta T^2 + k_H^{ctotal} \Delta T \Delta H + k_{\varepsilon eff}^{ctotal} \Delta T \Delta \varepsilon eff\right) + \\ k_\rho^R\left(k_W^{ctotal} \Delta\rho \Delta W + k_T^{ctotal} \Delta\rho \Delta T + k_H^{ctotal} \Delta\rho \Delta H + k_{\varepsilon eff}^{ctotal} \Delta\rho \Delta \varepsilon eff\right) \end{pmatrix}. \end{aligned} \quad (6.24)$$

The 2nd order terms are ignored and we could re-write (6.24) formulas as

$$td = 2.3\left(R_{nom} C_{total,nom} + k_W^{td} \Delta W + k_T^{td} \Delta T + k_H^{td} \Delta H + k_\rho^{td} \Delta\rho + k_{\varepsilon eff}^{td} \Delta \varepsilon eff\right), \quad (6.25)$$

where $k_W^{td} = C_{total,nom} k_W^R + R_{nom} k_W^{ctotal}$, $k_T^{td} = C_{total,nom} k_T^R + R_{nom} k_T^{ctotal}$, $k_H^{td} = R_{nom} k_H^{ctotal}$, $k_\rho^{td} = C_{total,nom} k_\rho^R$ and $k_{\varepsilon eff}^{td} = R_{nom} k_{\varepsilon eff}^{ctotal}$. The coefficients ($k_x^R, k_x^{ctotal}$) are derived in the linearized models of capacitance and resistance already. The benefits of the

linearized models proposed in the thesis is we don't need additional derivatives to calculate delay and crosstalk models as (6.22) and (6.23).

Hence, the standard deviation of delay could be calculated as

$$\sigma_{t_d} = \left(\left(\sigma_W k_W^{td} \right)^2 + \left(\sigma_T k_T^{td} \right)^2 + \left(\sigma_H k_H^{td} \right)^2 + \left(\sigma_\rho k_\rho^{td} \right)^2 + \left(\sigma_{\varepsilon eff} k_{\varepsilon eff}^{td} \right)^2 \right)^{0.5}. \tag{6.26}$$

For crosstalk noise, we could write in the form as

$$\begin{aligned} V_p &= C_{ll} / C_{total} \\ &= \frac{\left(C_{ll,nom} + k_W^{cll} \Delta W + k_T^{cll} \Delta T + k_H^{cll} \Delta H + k_{\varepsilon eff}^{cll} \Delta \varepsilon eff \right)}{\left(C_{total,nom} + k_W^{ctotal} \Delta W + k_T^{ctotal} \Delta T + k_H^{ctotal} \Delta H + k_{\varepsilon eff}^{ctotal} \Delta \varepsilon eff \right)} \quad . \end{aligned} \tag{6.27}$$

After linearized

$$V_p = \frac{C_{ll,nom}}{C_{total,nom}} \left(1 + k_W^{\mathrm{Vp}} \Delta W + k_T^{\mathrm{Vp}} \Delta T + k_H^{\mathrm{Vp}} \Delta H + k_{\varepsilon eff}^{\mathrm{Vp}} \Delta \varepsilon eff \right), \tag{6.28}$$

where $k_W^{\mathrm{Vp}} = \frac{k_W^{\mathrm{cll}}}{C_{ll,nom}} - \frac{k_W^{\mathrm{ctotal}}}{C_{\mathrm{total},nom}}$, $k_{\mathrm{T}}^{\mathrm{Vp}} = \frac{k_{\mathrm{T}}^{\mathrm{cll}}}{C_{ll,nom}} - \frac{k_{\mathrm{T}}^{\mathrm{ctotal}}}{C_{\mathrm{total},nom}}$, $k_{\mathrm{H}}^{\mathrm{Vp}} = \frac{k_{\mathrm{H}}^{\mathrm{cll}}}{C_{ll,nom}} - \frac{k_{\mathrm{H}}^{\mathrm{ctotal}}}{C_{\mathrm{total},nom}}$ and

$k_{æff}^{\mathrm{Vp}} = \frac{k_{æff}^{\mathrm{cll}}}{C_{ll,nom}} - \frac{k_{æff}^{\mathrm{ctotal}}}{C_{\mathrm{total},nom}}$.

Hence, the standard deviation of crosstalk could be calculated as

$$\sigma_{V_p} = \left(\left(\sigma_W k_W^{Vp} \right)^2 + \left(\sigma_T k_T^{Vp} \right)^2 + \left(\sigma_H k_H^{Vp} \right)^2 + \left(\sigma_{Eeff} k_{Eeff}^{Vp} \right)^2 \right)^{0.5} . \qquad (6.29)$$

The linearity assumption model is compared to Monte Carlo simulation. As showed in Fig. 6.7 for delay and crosstalk, the capacitance statistical distribution of structure-A with nominal $\{W, S, T, H, \rho, \varepsilon_{eff}\}$=$\{0.15\,\mu$m, $0.15\,\mu$m, $1.2\,\mu$m, $1\,\mu$m, $2.65\,\mu\,\Omega$-cm, $3.9\}$ for a 30% 3σ variation in all parameters. The accuracy of mean and standard deviation between the model and Monte Carlo simulation is good. The accuracy of standard deviation of for delay and crosstalk are further investigated by change the amount of parameter variation as showed in Fig. 6.8 and Fig. 6.9 respectively. The figure shows that the errors are less than 4% for process variation as much as 30%.

The experiments results above give evidence that the approximation method to calculate the variation of capacitance, delay and crosstalk for maximum 30% 3σ variation has insignificant error.

6-5 Optimization Design of Interconnect Considering Process Variations

In previous section, we derive the formula to analyze the amount of output variation due to the variation of inputs. We will continue to use those formulas on the optimization of interconnection design. Fig. 6.10 (1-plane (1P)) and Fig. 6.11 (2-plane (2P)) are plots of capacitances and corresponding standard deviation. Fig. 6.12 is the summary of variation percentage for 1-plane and two-planes structure.

From these figures, we could summarize as

1. C_{ll} dominate the total capacitance variation compared to C_{af} for small pitch. C_{ll} varies significant over the range of interest. This indicates crosstalk variation may be significant due to C_{ll} variation.

2. The standard deviation in 2-plane structure is larger than 1-plane structure for coupling capacitance. Therefore, metal lines which have metal runs over both top and bottom layer tend to more sensitivity to the process variation.

3. From process point of view, the thicker and taller metal line is less sensitivity to process variation. Hence, local metal layers tend to have issue of process variation impact compared to intermediate or global metal line.

4. The capacitance variation in small pitch interconnect is larger than large pitch capacitance

5. Under same pitch, the interconnect with narrow metal width has smaller process variation impact on coupling capacitance (c_{II}).

From capacitance (dynamic power) point of view, the narrow width (for specified pitch) and larger pitch will help to release the impact of process variation. For backend process which has thicker dielectric and metal thickness will contribute more process variation immunity. Therefore, the higher metal wire and via aspect ratio with large spacing between intra-wire is better design if chip has dynamic power variation concerns.

However, the narrow wire width could increase the resistance of wire and hence RC delay. The next step is to estimate the impact of variation on the delay and crosstalk performance.

The variation percentage is important for delay analysis. For example, 100ps delay variation is 10% setup (or hold time) variation for 1GHz frequency signal vs. 1% difference for 100MHz. On the other hand, shorter delay caused process variation may be good for setup time but it may cause hold time violation. Hence, we will focus more on the variation percentage in the following delay analysis. The Figure 6.13 gives the delay and corresponding standard deviation due to process variation. There are few interesting phenomenon are observed.

1. The delay decreases with the increasing of pitch; however, the standard deviation and variation percentage increased with pitch. It is opposite to that observed in the study of statistical capacitance previously. This is because for large pitch interconnects, the delay is dominated by resistance of wire not capacitance.
2. For *W=S,* we found the layout design is immunity to the process variation. At the same time, the delay is minimum at *W=S* also. This is the balance between resistance increase (decrease) and capacitance decrease (increase) for smaller (larger) *W*. The optimized width and spacing under specified pitch is observed to be *W=S=Pitch/2*. The variation percentage contours are drawing in Fig. 6.14. And again, it shows the half pitch wire width and spacing is the optimum design considering both process variation and performance.
3. From process point of view, the thicker and taller metal line is less sensitivity to process variation.

Instead of percentage variation, the amount of change on crosstalk is more important than percentage variation. For example, 0.01V will not be the issue for crosstalk. However, 0.01V crosstalk variation is 10% variation for 0.1V crosstalk noise at nominal and 100% variation for 0.01V crosstalk noise at nominal. Hence, we will use the amount of change (standard deviation) of crosstalk noise as the criterion for the following crosstalk noise analysis.

Figure 6.15 is the crosstalk and corresponding standard deviation.

1. For thin dielectric and metal thickness of metal line, the crosstalk noise is small compare to thicker one. At the same time, the standard deviation is larger for thin metal line than thicker one. Hence, if we take the process variation into consideration, we found the thinner metal line may have more

crosstalk noise compare to thick metal line structure which the standard deviation is smaller.

2. The pitch which has highest crosstalk sensitivity could be found at specified pitch. We will explain the relationship between this special pitch and other interconnect dimension laser in this section.

We turn our attention to compare the design of different technology node. Three different advanced technologies are chosen for study and they are 65nm, 90nm and 130nm. The detail simulation parameter and 3 σ is provided in Table 6.1. These values are taken from ITRS roadmap and industry data.

Figure 6.16 and 6.17 are the plots of delay and corresponding variation for different technology nodes.

From these data, we could found

1. for smaller pitch, the couple capacitance dominate, hence delay time is large for older technology (thicker metal)
2. large pitch section, delay increase with pitch and decrease with dielectric thickness due to Caf component.
3. variation on old technology is bigger (rsp. to metal thickness) ; hence, the standard variation is larger also
4. smaller pitch section, the smaller metal thickness has smaller RC and smaller variation. Performance and variation are both better.
5. *P/H=2.5* has optimum (minimum) variation percentage

Figure 6.18 and 6.19 are the plots of crosstalk and corresponding variation for different technology nodes. The following information is observed.

1. The trade-off between Vp performance and the standard deviation of Vp is observed. Again, we use the standard deviation instead the variation

percentage to evaluate the impact of crosstalk noise caused by process variation.

2. At a larger pitch, 65nm the variation as a percentage is still higher than 90nm/130nm even though the absolute variation may be more for the 65/90nm at large pitch.

3. *P/(T+H)=0.77* has worst (maximum) standard deviation for crosstalk. That is, such structure which we should try to prevent, the layout/process is most sensitivity to process variation. So, to minimum the layout area (small horizontal pitch), the vertical dimension has to be scale-down (*P/(T+H)>0.77)* or scale-up (*P/(T+H)<0.77)* to prevent the worst corsstalk noise sensitivity happen. On the contrary, for specified process parameters T and H, we should design to prevent the layout that happen this criterion.

6.6 Summary

The interconnection parasitic capacitances, delay and crosstalk variation due to process variations for 1-plane (1P) and 2-plane (2P) structure are shown in this chapter. Based on the analysis above, 1) the thicker dielectric and metal thickness provide better process variation immunity which is conflict to the results of the optimization results in Chapter 5 which not take process variation into consideration. 2) *P/H=2.5* has optimum (minimum) variation percentage for delay analysis. 3) *P/(T+H)=0.77* has worst (maximum) standard deviation for crosstalk

Using the optimization methodology presented here that design and process engineer could achieve robust and insensitive designs with high yield and minimum variation. Hence, statistical design methodology presented in this chapter will be very useful for the yield optimization of deep submicron design.

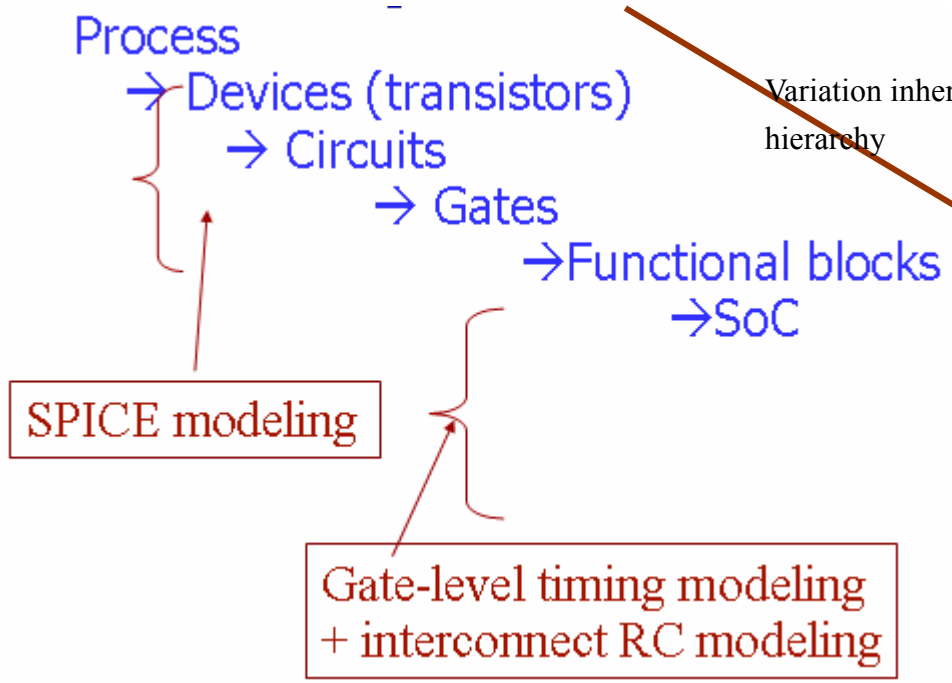


Figure 6.1 General design flow hierarchy from process to SOC.

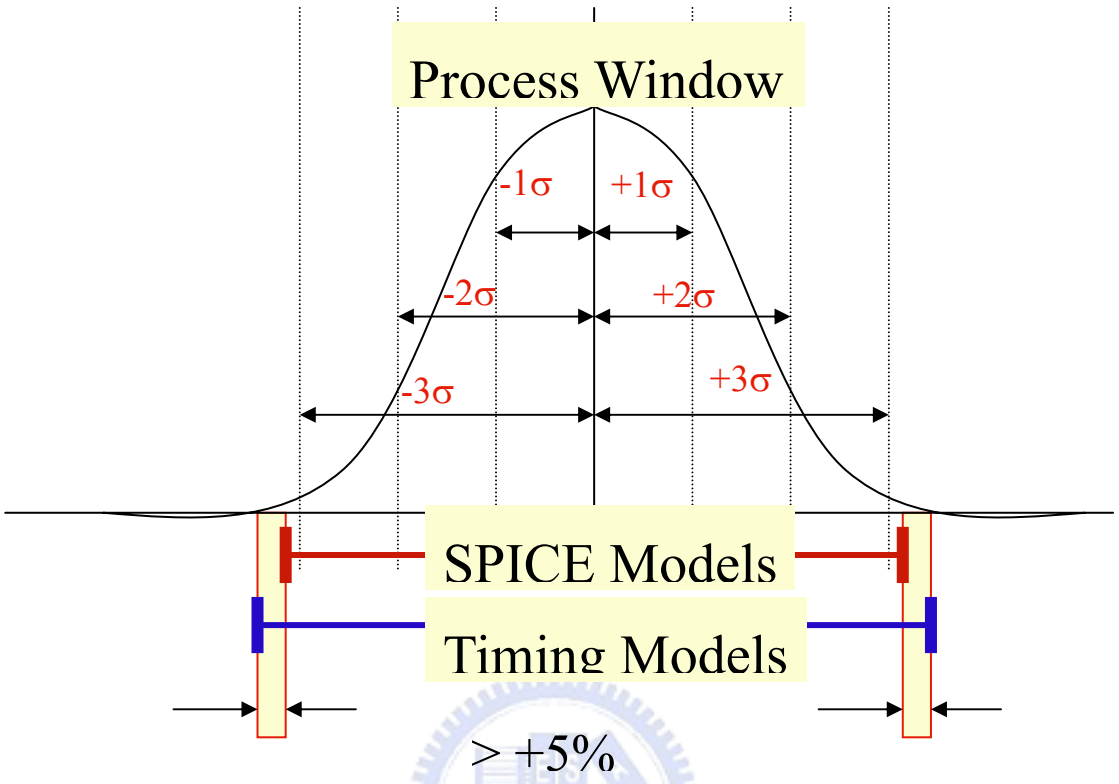


Figure 6.2 Process variation plus model error caused variation.

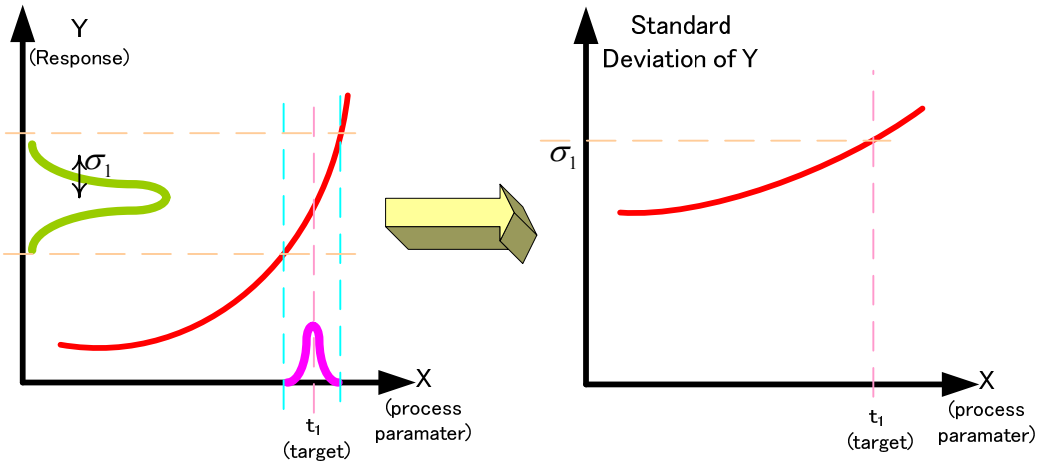
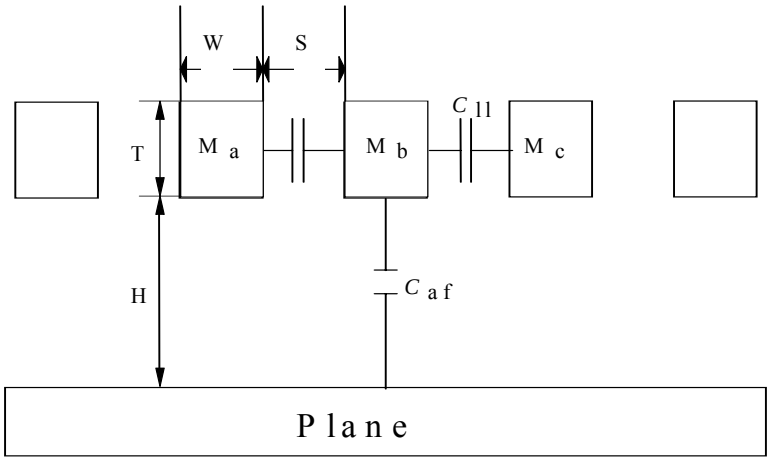
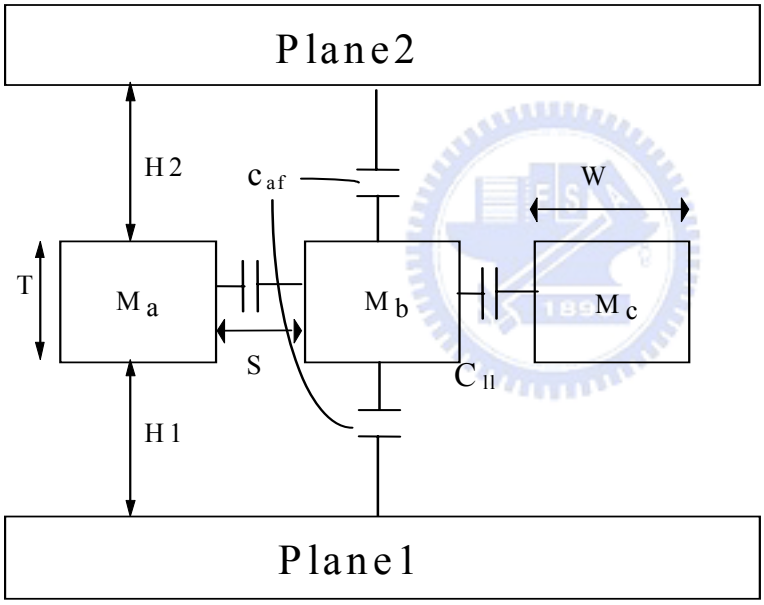


Figure 6.3 The effect of X on Y. The variation of Y (σ_1) depend on the nominal value (t_1) of X. The relationship between standard deviation and X is derived by the variation transmission method.



(a)



(b)

Figure 6.4 (a) cross-section of interconnect over one plane and (b) cross-section of interconnect between two planes.

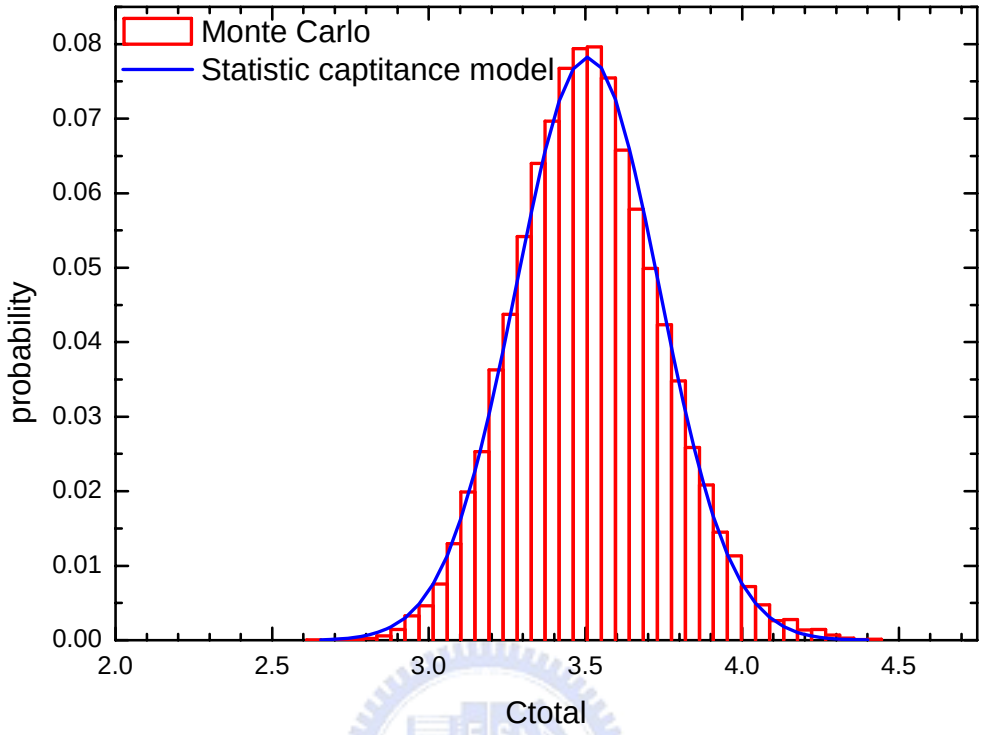


Figure 6.5 The capacitance distribution calculated from Monte Carlo simulations and statistical capacitance model.

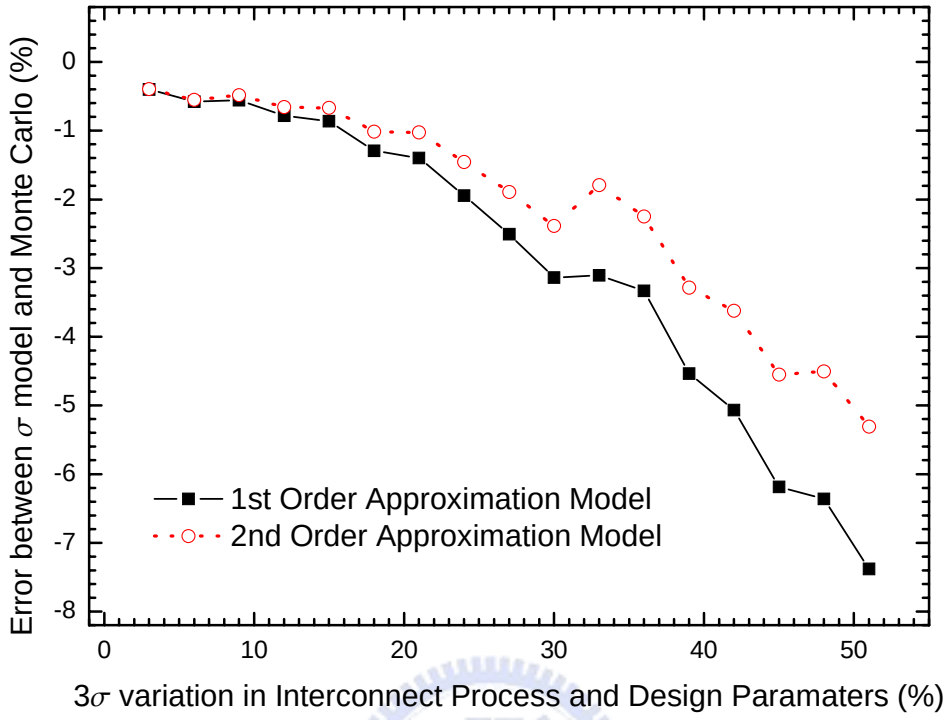
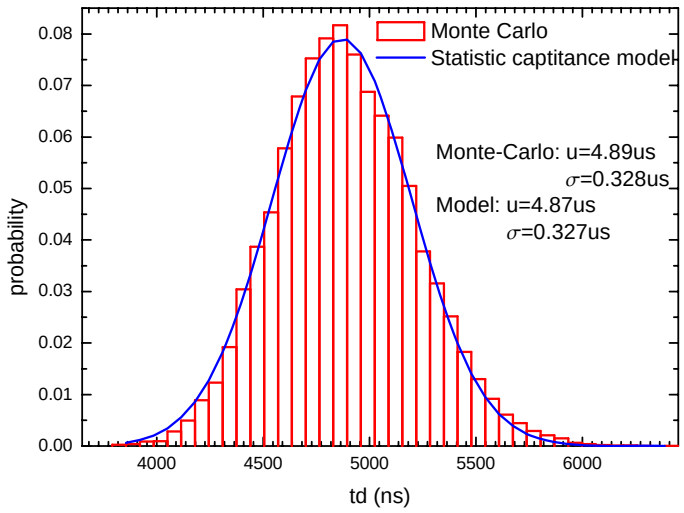
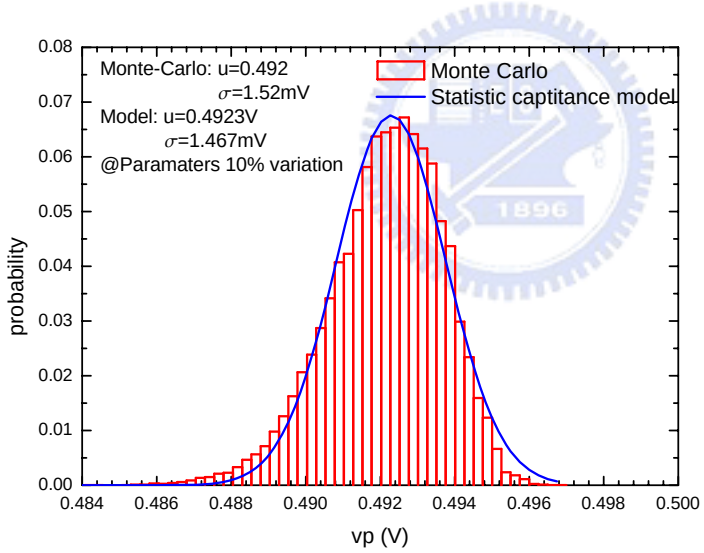


Figure 6.6 Error in statistical model of total capacitance (C_{total}) as a function of interconnect process (T, H, ρ and ε_{eff}) and design parameters (W and S). 0.7% (-3.1% vs. -2.4%) difference exists between 1st and 2nd order model at 30 % 3-sigma.



(a)



(b)

Figure 6.7 (a) Delay statistical distribution and (b) crosstalk statistical distribution calculated from Monte Carlo simulations and statistical capacitance model.

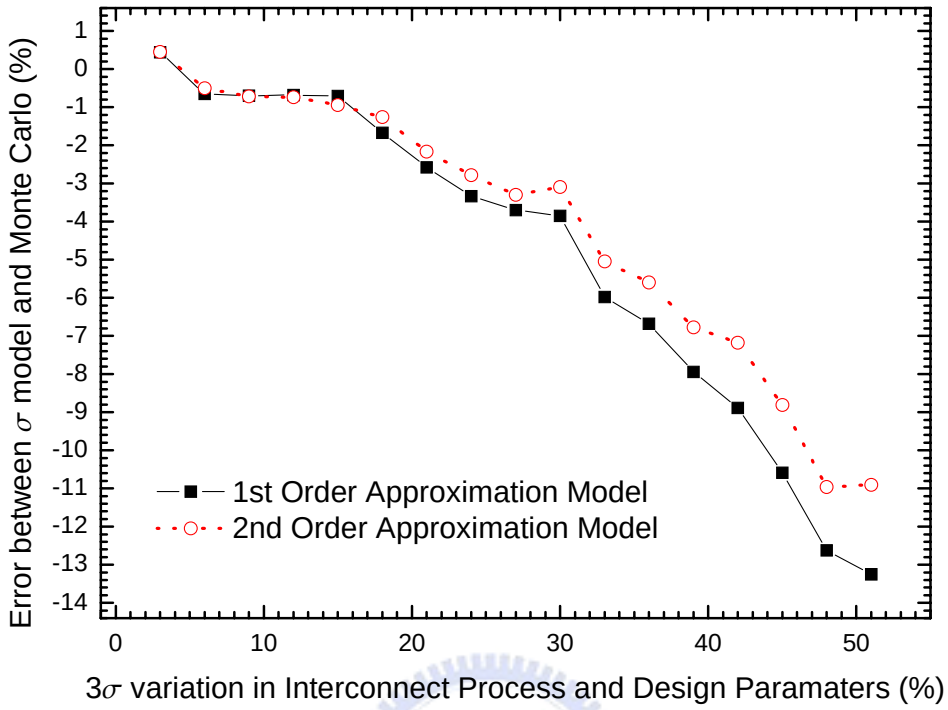


Figure 6.8 Error in statistical model of delay (t_d) as a function of interconnect process (T, H, ρ and ε_{eff}) and design parameters (W and S). 0.7% difference exists (-3.8% vs. -3.1%) between 1st and 2nd order model at 30 % 3-sigma.

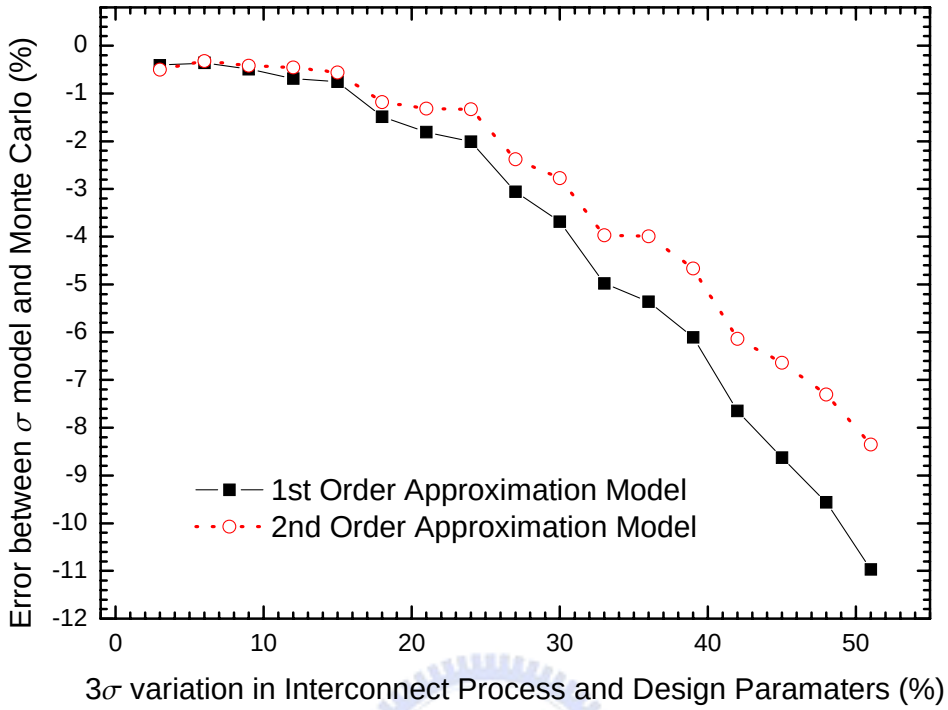


Figure 6.9 Error in statistical model of crosstalk voltage (Vp) as a function of interconnect process (T, H, ρ and ε_{eff}) and design parameters (W and S). 0.9% (-3.7% vs. -2.8%) difference exists between 1st and 2nd order model at 30 % 3-sigma.

Table 6.1 Simulation parameter table

	130nm			90nm			65nm		
	Short	IMD	Global	Short	IMD	Global	Short	IMD	Global
W (A)	1600 ± 10%	2000 ± 10%	4200 ± 10%	1200 ± 10%	1400 ± 10%	4200 ± 10%	900 ± 10%	1000 ± 10%	4000 ± 10%
S (A)	1800 ± 10%	2100 ± 10%	4200 ± 10%	1200 ± 10%	1400 ± 10%	4200 ± 10%	900 ± 10%	1000 ± 10%	4000 ± 10%
T (A)	2600 ± 25%	3700 ± 25%	8300 ± 25%	2400 ± 18%	3100 ± 19%	8500+20%	1800 ± 16.4%	2200 ± 15%	9000 ± 10%
H (A)	5500 ± 20%	5400 ± 10%	7700 ± 10%	4400 ± 15%	3200 ± 9.22%	7750±6.87%	3100 ± 15%	1750 ± 13.14%	6700 ± 6.85%
ε	3.7±10%	3.7±10%	4.2±10%	2.9 ± 10%	2.9 ± 10%	4.2±10%	2.9 ± 10%	2.9 ± 10%	4.2 ± 10%
ρ (μ ohm-cm)	2.2 ± 30%	2.2 ± 30%	2.2 ± 30%	2.2 ± 30%	2.2 ± 30%	2.2 ± 30%	2.2 ± 30%	2.2 ± 30%	2.2 ± 30%

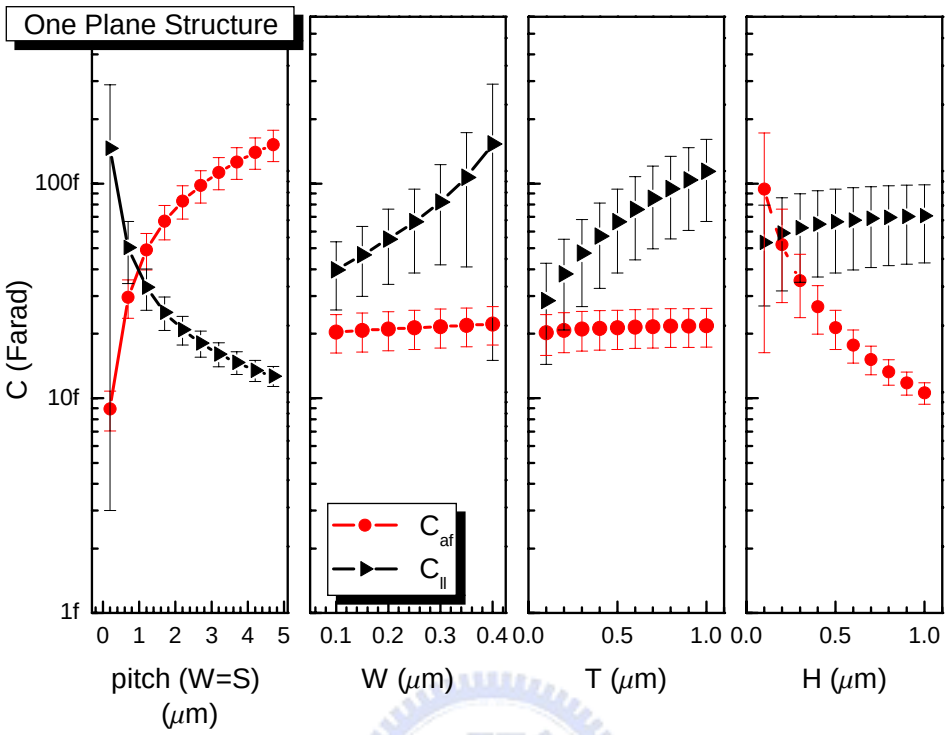


Figure 6.10 Capacitance values and corresponding standard deviation for line-to-line capacitance (C_{ll}) and area-fringe capacitance (C_{af}) for one-plane (structure-A) in Fig.6.4.

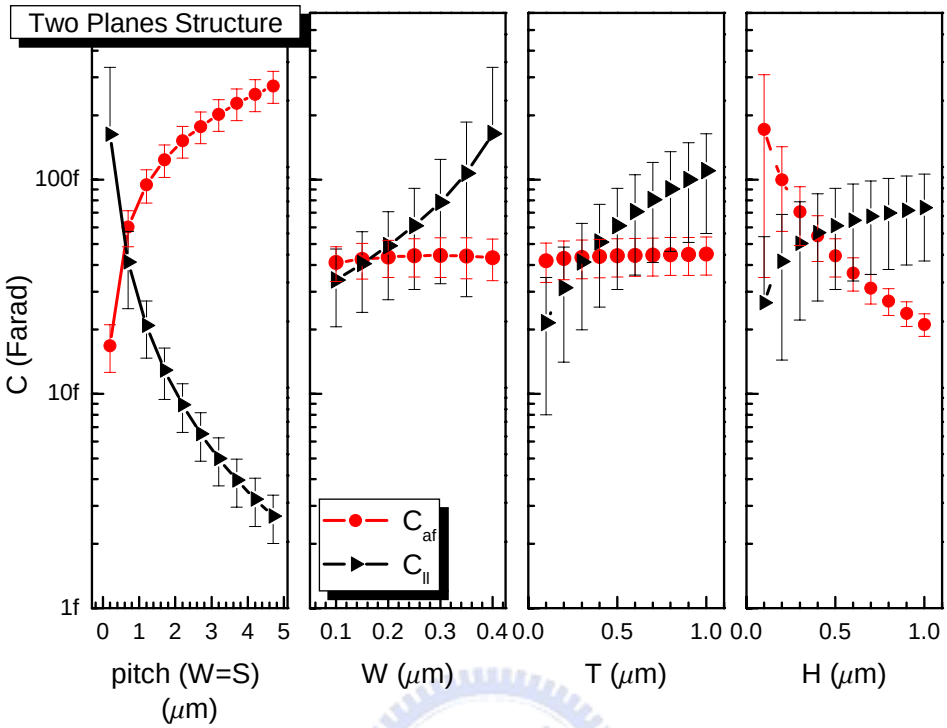


Figure 6.11 Capacitance components breakdown comparison for two planes structure (structure-B) in Fig.6.4.

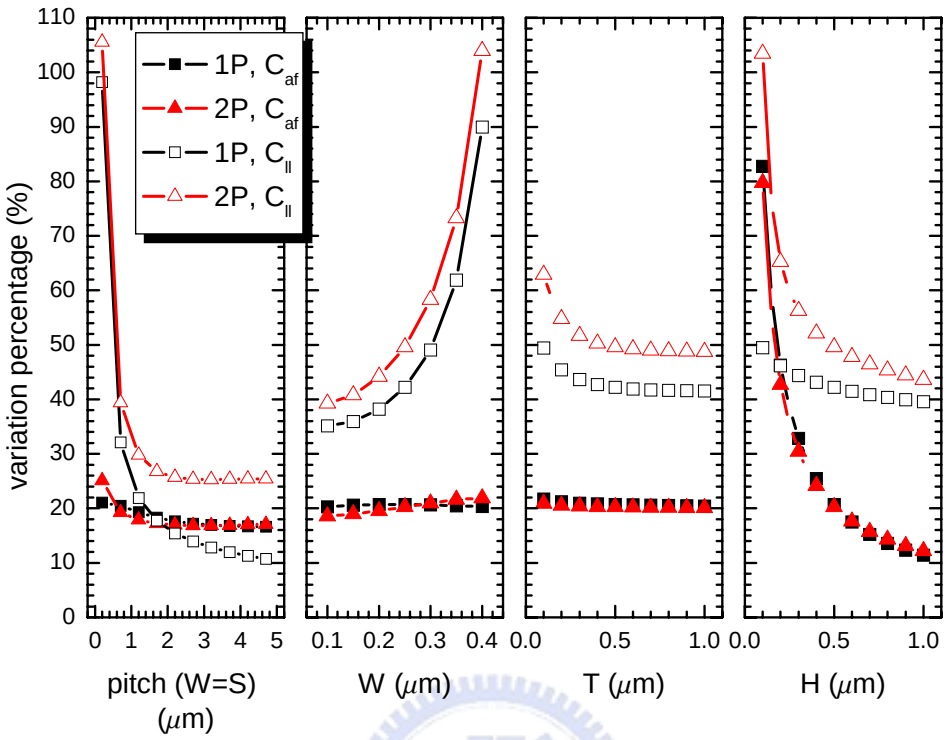


Figure 6.12 Capacitance variation breakdown plot.

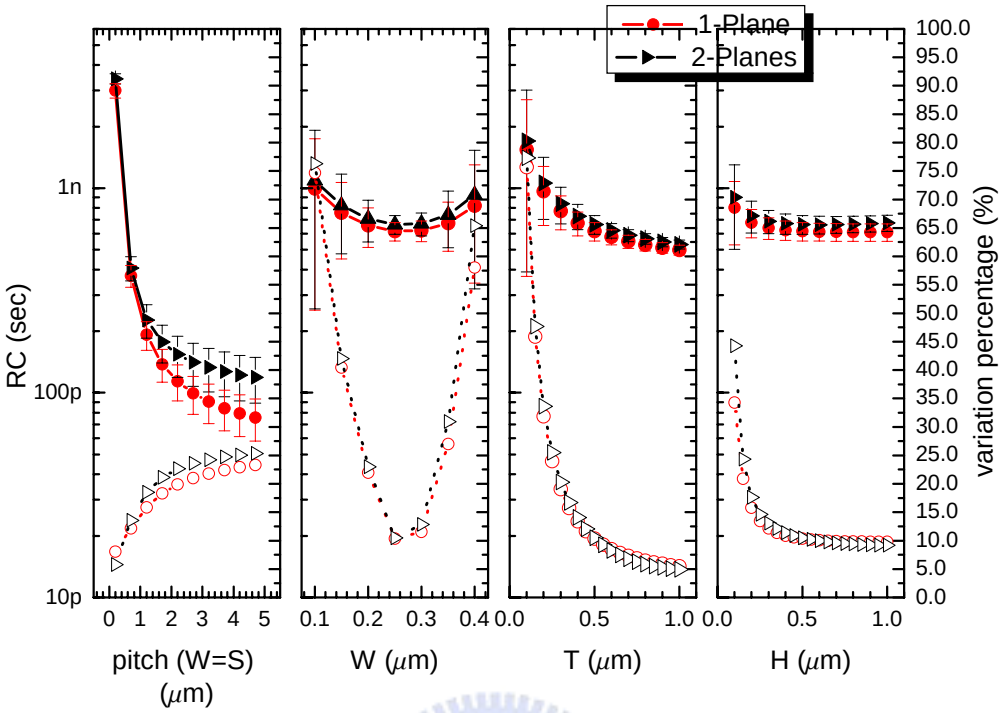


Figure 6.13 RC components breakdown corresponding std. variation comparison.

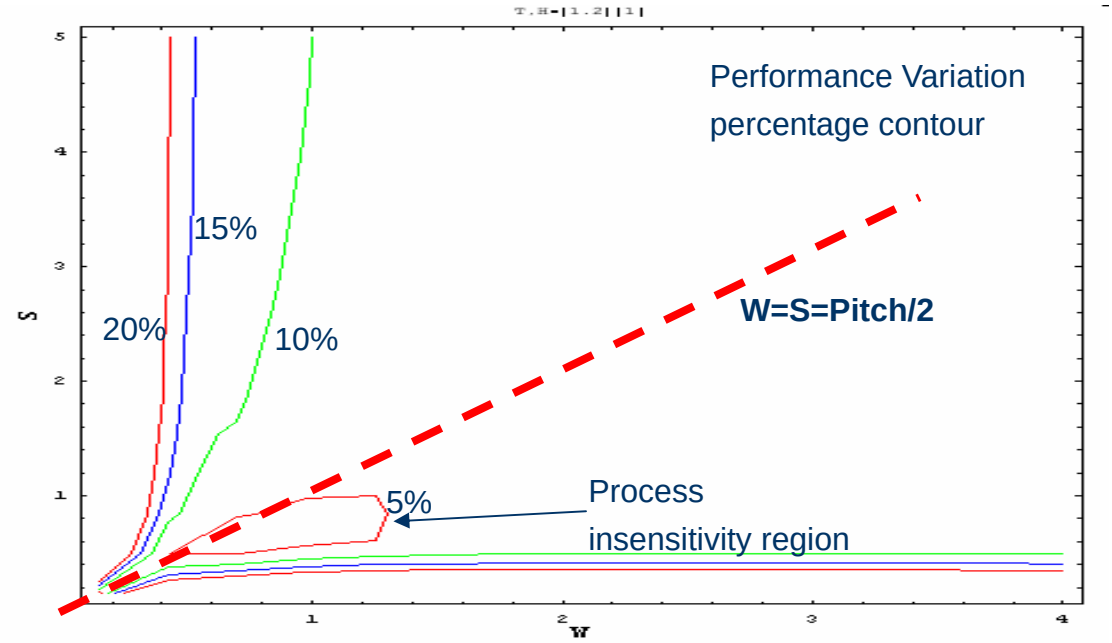


Figure 6.14 Standard deviation of delay contour plot at T=1.2/H=1 μ m.

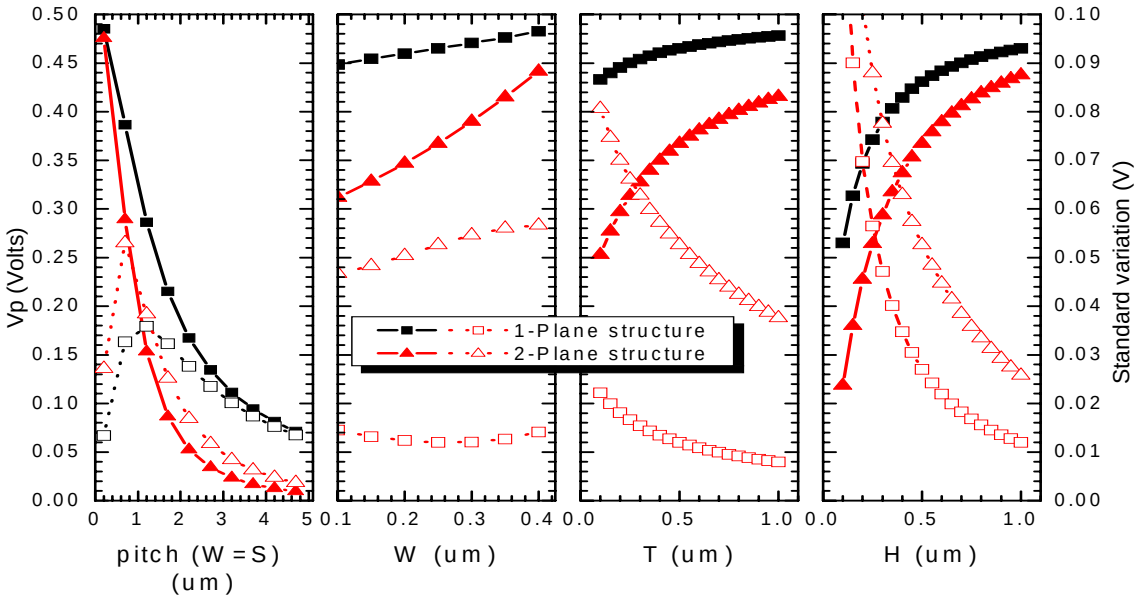
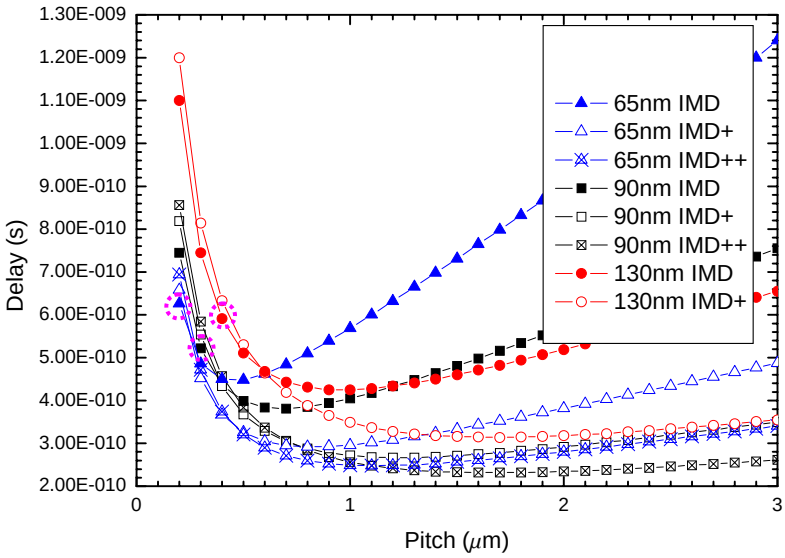
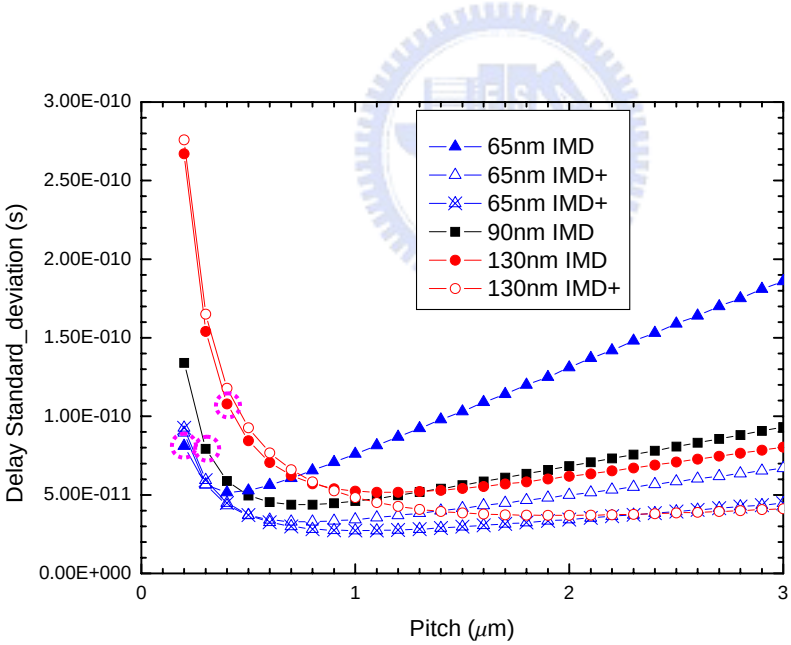


Figure 6.15 Interconnect crosstalk noise variation.



(a)



(b)

Figure 6.16 (a) delay for different technology node (b) the standard deviation of delay of 2-Planes structure for different technology node. The interconnect structure is calculated based on table 6.1. The symbol marked by dash-cycle is the minimum pitch dimension for different technology node mentioned in Table 6.1. IMD+ represents interconnect (n-th layer) has no metal plates at (n+1 & n-1-th layer) interlayer. IMD++ represents interconnect (n-th layer) has no metal plates at (n+1, n+2 & n-1 and n-2-th layer) interlayer.

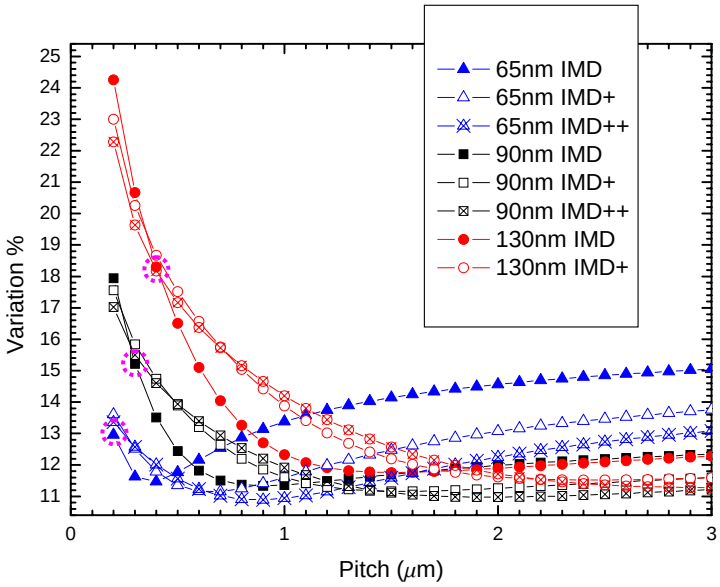
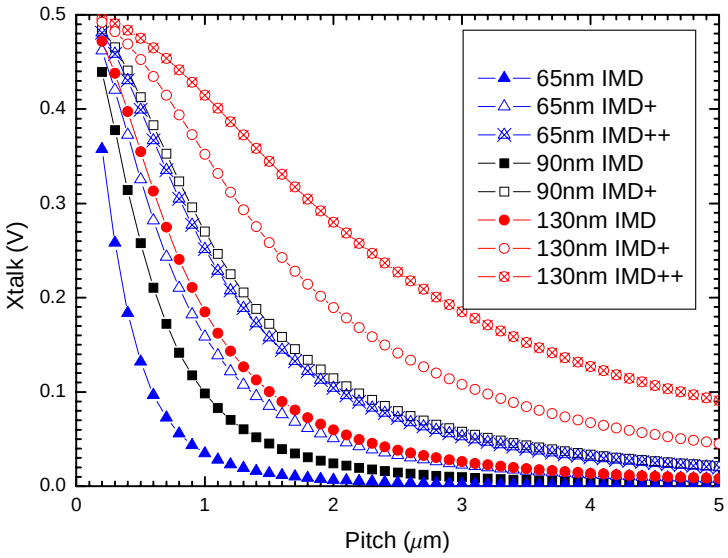
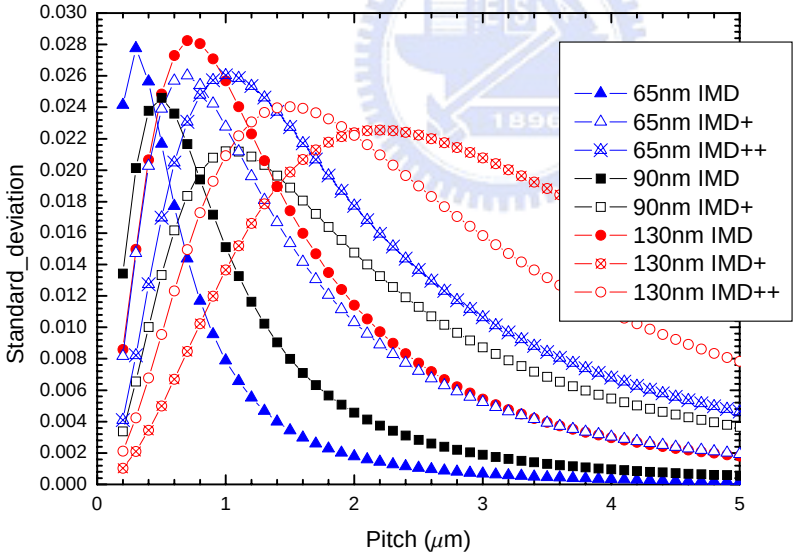


Figure 6.17 Percentage variation for the delay of 2-Planes structure for different technology node. The symbol marked by dash-cycle is the minimum pitch dimension for different technology node mentioned in Table 6.1. IMD+ represents interconnect (n-th layer) has no metal plates at (n+1 & n-1-th layer) interlayer. IMD++ represents interconnect (n-th layer) has no metal plates at (n+1, n+2 & n-1 and n-2-th layer) interlayer.



(a)



(b)

Figure 6.18 (a) crosstalk for different technology node (b) the standard deviation of crosstalk of 2-Planes structure for different technology node. The interconnect structure is calculated based on table 6.1. IMD+ represents interconnect (n-th layer) has no metal plates at (n+1 & n-1-th layer) interlayer. IMD++ represents interconnect (n-th layer) has no metal plates at (n+1, n+2 & n-1 and n-2-th layer) interlayer.

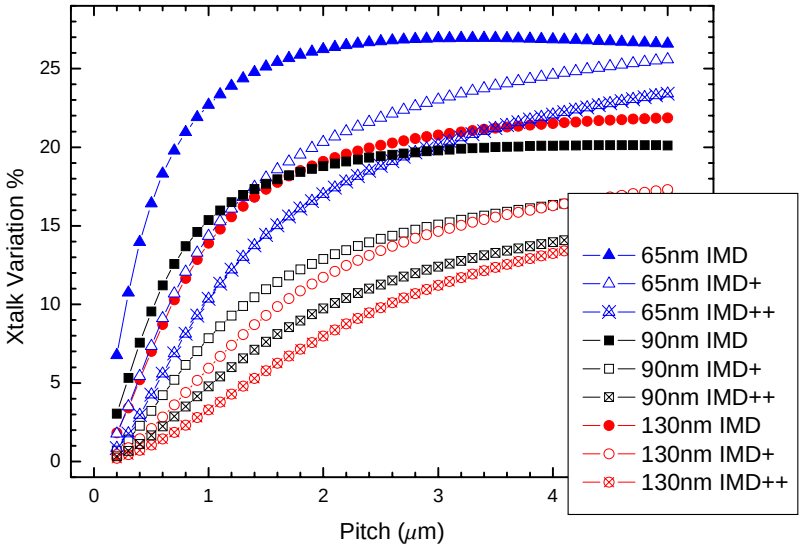


Figure 6.19 Percentage variation for the crosstalk of 2-Planes structure for different technology node. IMD+ represents interconnect (n-th layer) has no metal plates at (n+1 & n-1-th layer) interlayer. IMD++ represents interconnect (n-th layer) has no metal plates at (n+1, n+2 & n-1 and n-2-th layer) interlayer.

Chapter 7 Summary and Conclusions

In this chapter, the key results of this research and the major contributions of the thesis are summarized.

In this thesis, a complete closed-form capacitance models for three major structures in very large scale integration (VLSI) are developed. The developed models include 1) parallel lines in a plane, 2)wire between two planes and 3) inter-layer wire crossings which consider three-dimensional (3-D) nature. All the capacitance models agree well with numerical solutions of Poisson`s equation as well as measurement data.

We then further derive closed-form solutions for the delay and crosstalk noise for several interconnect structures. The delay and crosstalk formulas allow for simple analytic prediction of interconnection performance for arvitrary interconnect dimensions. The delay and crosstalk models agree well with SPICE simulations. Our model is useful for VLSI design and process optimization.

Based on the models, interconnect delay and crosstalk performance is optimized over the range of process and design dimension of interest. In specific, we find 1) for wire without top wiring, the optimal dielectric thickness is relatively small, this well agreeing with the roadmap of foundry and the aspect ratio limitation of via, 2) for lines with top wiring, larger dielectric thickness and wire thickness give better performance, and 3) the range of allowable wire thickness and dielectric thickness reduces seriously as the design pitch reduces.

We propose statistical capacitance, delay and crosstalk analysis methodology to help design or process engineer to deliver the robust chip design and enhance the

product yield. The proposed statistical models shows that errors are less than 2.5% and 4% for capacitance and delay (and crosstalk) for process variation as much as 30% compared with Monte Carlo simulation. Furthermore, we use these models to find 1) the thicker dielectric thickness (*H*) and metal thickness (*T*) provide better process variation immunity. 2) For delay analysis, horizontal pitch (*P*) and dielectric thickness has one optimum relationship (*P/H=2.5*) to achieve designs that could reduce performance impact due to variability. 3) For crosstalk analysis, *P/(T+H)=0.77* is the structure most sensitivity to process variation and both process and design engineer should prevent to use the structure. Hence, we recommend to use small horizontal pitch (*P*) so that $P < 0.77*(T+H)$ or large pitch so that $P > 0.77*(T+H)$ to minimum the impact due to process variation. These results are believed to be helpful in VLSI design and optimization.

These results are believed to be helpful in VLSI design and optimization.

Chapter 8 Future Prospects

In this chapter, the possible directions for future work are suggested.

Two possible directions of future work are suggested in this section, including the optimization design include device performance and the statistical analysis of static power. The real world of interconnect is driven by driver and terminated with receiver. To provide the analysis with device could give us the overall information about the optimization in real silicon.

The variation of static power is more and more important in advanced technology [8.1]. In [8.1], the 20X variation in static is found for 1.3X frequency variation in microprocessor design. The chip may fail at static power spec even the speed of this chip meet the spec. Hence, to prevent the over design or under-design of static power, the statistical design for static power of chip is important in the near future.

The effects of thermal are becoming more and more important due to increased of operating frequency and hence dynamic power. Higher temperature increases interconnect delay because the electrical resistivity of metal increases linearly with temperature. Therefore, the impacts of temperature on the delay and crosstalk are worth to further investigate.

References

Chapter 1

[1.1] R. Rosenberg, D. C. Edelstein, C.-K. Hu, and K. P. Rodbell, "Copper Metallization for High Performance Silicon Technology," *Annu. Rev. Mater. Res.*, vol. 30, pp. 229-262, 2000.

[1.2] D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T.McDevitt, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz, L.Su, S. Luce, and J. Slattery, "Full Copper Wiring in a Sub-0.25 μm CMOS ULSI Technology," Proc. IEEE IEDM, pp. 773-776, 1997.

[1.3] S. Venkatesan, A. V. Gelatos, V. Misra, B. Smith, R. Islam, J. Cope, B. Wilson, D.Tuttle, R. Cardwell, S. Anderson, M. Angyal, R. Bajaj, C. Capasso, P. Crabtree, S.Das, J. Farkas, S. Filipiak, B. Fiordalice, M. Freeman, P. V. Gilvert, M. Herrick, A.Jain, H. Kawasaki, C. King, J. Klein, T. Lii, K. Reid, T. Saaranen, C. Simpson, T.Sparks, P. Tsui, R. Venkatraman, D. Watts, E. J. Weitzman, R. Woodruff, I. Yang, N.Bhat, G. Hamilton, and Y. Yu, "A High Performance 1.8V, 0.29 μm CMOSTechnology with Copper Metallization," Proc. IEEE IEDM, pp. 769-772, 1997.

[1.4] J. Pallinti, S. Lakshminaryanan, W. Barth, L. Kwak, P. Burke, S. Gu, C. Falk, M.Lu, S. Sun, P. Wright, J. Elmer, L. Duong, S. Reder, R. Donis, W. Catabay, D. Wang, B. Hannan, F. Ho, D. Zhang, and J. Wang, "Stress Free Polishing – A Technique forCopper removal in Advanced Technology Nodes," CMPMIC, pp. 43-50, Marina Del Rey, CA, February 2004.

[1.5] A. West, "Practical and Theoretical Considerations for e-CMP," NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, ERC TeleSeminar Presentation, July 13, 2006.

[1.6] A. Brown, “Flat, Cheap, and Under Control: Applied Materials’ New Polishing Technology Could be the Key to the Coming Generation of Microchips,” *IEEE Spectrum*, pp.40-45, January 2005.

Chapter 2

[2.1] D. Sylvester, C. Hu, "Analytical modeling and characterization of deep-submicrometer interconnect," *Proceedings of the IEEE*, Vol. 89, No. 5 , pp. 634-664, May 2001.

Chapter 3

[3.1] RAPHAEL Users’Manual , Technology Modeling Associte , 1995.

[3.2] T. Sakurai and K. Tamaru , “Simple formulas for two-and three- di - mensional capacitances , ” *IEEE Trans. Electron Devices* , vol . 30 . pp . 183-185 , 1983 .

[3.3] K. Choudbury and A . Sangiovanni’Vincentelli , “ Automatic gencration of analytical models for inter conncetion capacitances , ”*IEEE Trans . Computer-Aided Design,* vol . 14 , pp . 470-480 , 1995 .

[3.4] J.–H. Chern , J. Huang, L. Arledge . P . – C. Li. And P. Yang . “Multjlcvel metal capacitance models for CAD design synthesis systems , ”*IEEE Electron Device Letter* , vol . 13 , pp . 32-34 , 1992 .

[3.5] T. Sakurai, “Closed-form formulas for interconnection delay, coupling and corosstalk in VLSTs ,” *IEEE Trans. Electron Dev.*vol.40,pp.118-124,1993.

[3.6] N. D. Arora, K. V. Roal, r. schwnann, and L. M. Rjchardson , “Modeling and extraction of interconnect for multilayer VI.SI circuits. ”*IEEE Computer-Aided Design*, vol. 15, pp. 58-67, 1996.

[3.7] M. Shoji, High Speed Digital Circuits. Reading, MA: Addison Weslcy,1996.

[3.8] S. Nakagawa, D. M. Sylvester, J.G. McBride, S.Y. Oh, “On-chip cross talk noise

model for deep submicron ULSI interconnect, ”Hewlett Packard J. pp. 39, Aug.1998.

[3.9] M. T. Bohr, “Interconnect scaling—The real limiter to high performance ULSI,” in Proc. IEDM, 1995, pp. 241–244.

[3.10] J.-H. Chern, J. Huang, L. Arledge, P.-C. Li, and P. Yang, “Multilevel metal capacitance models for CAD design synthesis systems,” *Electron Device Lett.*, vol. 13, pp. 32–34, 1992.

[3.11] T. Sakurai, “Closed-form formulas for interconnection delay, coupling and crosstalk in VLSI’s,” *IEEE Trans. Electron Device*, vol. 40, pp.118–124, 1993.

[3.12] K. Rahmat, O. S. Nakagawa, S.-Y. Oh, J. Moll, and W. T. Lynch, “Ascaling scheme for interconnect in deep-submicron process,” in Proc.IEDM, 1995, pp. 245–248.

[3.13] N. D. Arora, K. V. Roal, R. Schumann, and L. M. Richardson, “Modeling and extraction of interconnect capacitances for multilayer VLSI circuits,” *IEEE Trans. Circuits Syst.*, vol. 15, pp. 58–67, 1996.

[3.14] K. J. Chang, Soo-Young Oh, Norman Chang, and Ken Lee, “Parameterized SPICE subcircuits for multilevel interconnect modeling and simulation,” *IEEE Trans. Circuits Syst.II,* vol.39, pp. 779–789, 1992.

[3.15] D. H. Cho, Y. S. Eo, M. H. Seung, N. H. Kim, J. K. Wee, O. K. Kwon,and H. S. Park, “Interconnect capacitance, crosstalk and signal delay for0.35um CMOS technology,” in Proc. IEDM, 1996.

[3.16] G.-W. Pan, M. Toupikov, and B. K. Gilbert, “A combined finite difference and analytic expression approach to crossover capacitance in a multilayer dielectric environment,” *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 19, pp. 615–620, 1996.

[3.17] S. A. Kuhn, M. B. Kleiner, P. Ramm, and W. Weber, “Performance modeling of

the interconnect structure of a three-dimensional integrated RISC processor/cache system," *IEEE Trans. Comp., Package., Manufact. Technol. B*, vol. 19, pp. 719–727, 1996.

[3.18]V. Vladimir and R. Mittra, "A technique for fast calculation of capacitance matrices of interconnect structures," *IEEE Trans. Comp.,Package and Manufact. Technol. B*, vol. 21, 1998, pp. 241–249.

[3.19]J.-K. Wee, Y.-J. Park, H.-S. Min, D.-H. Cho, M.-H. Seung, and H.-S.Park, "Measurement and characterization of multilayered interconnectcapacitance for deep-submicron VLSI technology," *IEEE Trans. Semiconduct. Manufact.*, vol. 11, pp. 636–644, 1998.

[3.20]P. Nouet and A. Toulouse, "Use of test structures for characterization and modeling of inter-layer capacitances in a CMOS process," *IEEE Trans. Semiconduct. Manufact.*, vol. 10, pp. 233–241, 1997.

[3.21]K. Aoyama, K. Ise, H. Sato, K. Tsuneno, and H. Mauda, "A new characterization of sub- m parallel multilevel interconnect and experimental verification," *IEEE Trans. Semiconduct. Manufact.*, vol. 9, pp. 20–26,1996.

[3.22] C.-J. Chao, S.-C. Wong, M.-J. Chen, and B. K. Liew, "An extraction method to determine interconnect parasitic parameters," *IEEE Trans.Semiconduct. Manufact.*, vol. 11, pp. 615–623, 1998.

[3.23] J. C. Chen, D. Sylvster, and C. Hu, "An on-chip interconnect capacitance characterization method with sub-femto-farad resolution," *IEEE Trans.Semiconduct. Manufact.*, vol. 11, pp. 204–210, 1998.

[3.24] S.-C. Wong, G.-Y. Lee, and D.-J. Ma, "Modeling of interconnect capacitance, delay and cross-talk in VLSI," *IEEE Trans. Semiconduct. Manufact.*, Vol.13, NO.1 , pp.108-111, 2000

[3.25] RAPHAEL Users' Manual, Technology Modeling Associate, 1995.

[3.26] J. D. Kraus and K. R. Carver, Electromagnetics, 2nd ed. New York:McGraw-Hill, 1973, pp. 290–304.

[3.27]A. E. Ruehli, “Inductance calculations in a complex integrated circuit environment”, *IBM J. Res. Dev.*, pp. 470–481, Sept. 1972.

[3.28]E. B. Rosa and F. W. Grover, Formulas and Tables for the Calculation of Mutual and Self-Inductance, U.S. Government Printing Office, Washington, DC, 1916.

[3.29]X. Qi, Gaofeng Wang, Zhiping Yu and. Robert. W. Dutton, Tak Young, “On-chip inductance modeling and *RLC* extraction of VLSI interconnects for circuit simulation”, Proceedings of Custom Integrated Circuits Design Conference, pp. 487–490, 2000.

[3.30]K. Gala, Vladimir Zolotov, Rajendran Panda, Brian Young, Junfeng Wang, David Blaauw, “On-chip inductance modeling and analysis”, Proceedings of Design Automation Conference, pp. 63–68, 2000.

Chapter 4

[4.1] M.T.Bohr, ”Interconnection scaling-The real limiter to high performance ULSI.”, in Porc. IEDM , pp. 241-244, 1995.

[4.2] K. Rahmat, O.S. Nakagawa, S.Y. Oh, J. Moll, “A Scaling Scheme for interconnect in deep submicron process” Porc. IEDM, pp. 245-248, 1995.

[4.3] N. Delorme, M. Belleville, “Interconnection parasitics evaluation and optimization,” *Microelectronic Engineering*, vol. 33, pp. 407-414, 1997.

[4.4] Michel. Brillouet, “Multilevel interconnection technologies and future requirements for logic applications,” *Microelectronic Engineering*, vol. 33, pp. 5-13, 1997.

[4.5] R. Liu, C. S. Pai, E. Martinez, “Interconnect technology trend for

microelectronics," *Solid-State Electronics*, vol. 43, pp. 1003-1009, 1999.

[4.6] W. H.Chang, "Analytical IC metal-line capacitance formulas," *IEEE Trans. Microwave Theory and Techniques*, vol. 9, pp. 608-611, 1976.

[4.7] T. Sakurai and K. Tamaru, "Simple formulas for two- and three-dimensional capacitances," *IEEE Trans. ED*, vol. 30, pp. 183-185, 1983.

[4.8] G. Y. Lee, S. C. Wong, S. T. Lin, T. C. Su, and Patrick S. Liu, "A wiring capacitance model for deep submicron VLSI circuits," Proceedings of IEDMS , pp. 289-292, 1996.

[4.9] Umakanta Choudhury and Alberto Sangiovanni-Vincentelli, "Automatic Generation of analytical models for interconnection capacitances," *IEEE Trans. Computer-Aided Design of Integrated Circuits and System*, vol. 14, pp. 470-480, 1995.

[4.10] J. H. Chern, J. Jurang, L. Arledge, P. C. Li and P. Yang, "Multilevel metal capacitance models for CAD design synthesis system," *IEEE Electron Device Letter*, vol. 13, pp. 32-34, 1992.

[4.11] S.C. Wong, Patrick S. Liu, Jien-Wen Ru and S. T. Lin, "Interconnection capacitance models for VLSI circuits," *Solid-State Electronics*, vol. 42, pp. 969-977, 1998.

[4.12] N.D. Arora , K.V. Raol, R. Schumann, L.M. Richardson, "Modeling and extraction of interconnect capacitances for multilayer VLSI circuits," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 15, pp. 58-67, 1996.

[4.13] S. C. Wong, G. Y. Lee, D. J. Ma and C. J. Chao, "An Empirical Three-Dimensional Crossover Capacitance Model for Multi-Level Interconnect VLSI Circuits," *IEEE Trans. Semiconductor Manufacturing*, vol.13, pp. 219-227, 2000.

[4.14] S. C. Wong, G. Y. Lee and D. J. Ma, “Modeling of Interconnect Capacitance, Delay, and Crosstalk in VLSI,” *IEEE Trans. Semiconductor Manufacturing*, vol. 13, pp.108-111, 2000.

[4.15] T. Sakurai, “Closed-Form Expressions for Interconnect Delay, Coupling and Crosstalk in VLSIs,” *IEEE Trans. ED*, vol. 40, pp.118-124, 1993.

[4.16] M. Cases, D. M. Quinn, “Transient Response of Uniformly Distributed RLC Transmission Lines,” *IEEE Trans. Circuits and Systems*, vol 37, pp. 200-207, 1980.

[4.17] J. A. Davis, J. D. Meindl, “Compact Distributed RLC Interconnect Models-Part I: Single Line Transient, Time Delay, and Overshoot Expressions,” *IEEE Trans. ED* , vol. 47, pp. 2068-2077, 2000.

[4.18] J. A. Davis, J. D. Meindl, “Compact Distributed RLC Interconnect Models-Part II: Coupled Line Transient Expressions and Peak Crosstalk in Multilevel Networks,” *IEEE Trans. ED*, vol. 47, pp. 2078-2087, 2000.

[4.19] David K. Cheng, “Field and wave electromagnetics,” Addison-Wesley Publishing Company, pp.379-385.

[4.20]H. B. Bakoglu: Circuits, Interconnections, and Packaging for VLSI Addison-Wesley, Massachusetts, 1990, pp. 212.

[4.21] RAPHAEL Ver. 4.0, Avant! corporation.

[4.22]W. C. Elmore,”The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifier,” *J. Applied Physics*, Vol. 19, Jan. 1948, pp.55-63.

[4.23]Yu Cao, Xuejue Huang, Sylvester D., Chang, N., Chenming Hu, “A new Analytical Delay and Noise Model for On-Chip RLC interconnect,” Tech. Digest of IEDM, pp. 823-826, Dec. 2000..

[4.24]Yeha I. Ismail, Eby G. Friedman, and Jose L. Neves, “Figure Of Merit To

Characterize The Importance Of On-Chip Inductance", Proc. 35th Design Automation Conference, San Francisco, pp. 560-565, June 1998.

[4.25]Alina Deutsch, Paul W. Coteus, Gerard V. Kopcsay, Howard H. Smith, Christopher W. Surovic, Byron L. Krauter Daniel C. Edelstein, and Phillip J. Restle, "When are Transmission-Line Effects Important for On-Chip Interconnections?", *IEEE Trans. Microwave Theory And Techniques*, vol. 45, pp.1836-1846, 1997.

Chapter 5

[5.1] M.T.Bohr, "Interconnection scaling-The real limiter to high performance ULSI.", in Porc. IEDM , pp. 241-244, 1995.

Chapter 6

[6.1] S.R. Nassif, "Delay Variability: Sources, Impacts and Trends", ISSCC, 2000, pp.368-369

[6.2] S.R. Nassif, "Design for Variability in DSM technologies", ISQED, 2000, pp.451-454

[6.3] Paul S. Zuchowski, P. A. Habitz, J. D. Hayes, J. H. Oppold," Process and environmental variation impacts on ASIC timing", ICCAD 2004, pp336-342

[6.4] S. B. Samaan, "The impact of device parameter variations on the frequency and performance of VLSI chips", ICCAD 2004, pp.343-346.

[6.5] Mustafa Celik,Lawrence Pileggi,Altan Odabasioglu, "IC Interconnect Analysis", Kluwer Academic Publishers, 2002.

[6.6] Shekhar Borkar , Tanay Karnik , Siva Narendra , Jim Tschanz , Ali Keshavarzi , Vivek De, Parameter variations and impact on circuits and microarchitecture, Proceedings of the 40th conference on Design automation, pp.338-342, 2003,

Anaheim, CA, USA.

[6.7] V. Mehrotra, S. Nassif, D. Boning, and J. Chung, “Modeling the Effects of Manufacturing Variation on High-Speed Microprocessor Interconnect Performance,” IEEE Electron Devices Meetings, pp. 767-770, 1998.

Chapter 8

[8.1] Shekhar Borkar , Tanay Karnik , Siva Narendra , Jim Tschanz , Ali Keshavarzi , Vivek De, “Parameter variations and impact on circuits and microarchitecture, Proceedings of the 40th conference on Design automation”, pp.338-342, 2003, Anaheim, CA, USA

簡歷

姓　　名: 李國曖

性　　別: 男

出生年月日: 民國六十三年六月三十日

地　　址:台中市西屯區西安街 172 巷 7-2 號

學　　歷: 私立逢甲大學電機工程學系

(民國八十一年九月~民國八十五年六月)

私立逢甲大學　電機工程研究所碩士班

(民國八十五年九月~民國八十七年六月)

國立交通大學 電子工程研究所博士班

(民國八十七年九月~民國九十六年六月)

論文題目:超大型積體電路連線的解析模型與最佳化設計

The Analytical Models and Optimization Designs for VLSI Interconnection

Publication List

International Journal:

[1] **Trent Gwo-Yann Lee**, Tseung-Yuen Tseng, Shyh-Chyi Wong, Cheng-Jer Yang , Mong Song Liang and Huang-Chung Cheng," Generalized Interconnect Delay Time and Crosstalk Models： I. Applications of Interconnect Optimization Design," Jpn. J. Appl. Phys., vol. 40, pp.6686-6693, 2001.

[2] **Trent Gwo-Yann Lee**, Tseung-Yuen Tseng, Shyh-Chyi Wong, Cheng-Jer Yang , Mong Song Liang and Huang-Chung Cheng," Generalized Interconnect Delay Time and Crosstalk Models： II. Crosstalk-Induced Delay Time Deterioration and Worst Crosstalk Models," Jpn. J. Appl. Phys., vol. 40, pp.6694-6699, 2001.

[3] Fang-Long Chang, Ming-Jang Lin, **Gwo-Yann Lee**, Young-Shying Chen, C. W. Liaw and Huang-Chung Cheng,"Modeling and Design of the High Performance Step SOI-LIGBT Power Devices by Partition Mid-Point Method", Solid-State Electronics, Volume 47, Issue 10, October 2003, Pages 1693-1698

[4]. Jyh-Liang Wang, Yi-Sheng Lai, **Trent Gwo-Yann Lee**, Bi-Shiou Chiou, Chun-Chien Tsai, Huai-Yuan Tseng, Chueh-Kuei Jan, and Huang-Chung Cheng, "Characteristics of Low-temperature Pulse-Laser-Deposited (Pb,Sr)TiO3 Films in Metal/Ferroelectric/Silicon Structure", J. Phys. D: Appl. Phys., vol. 40, pp. 254-259, 2006.

International Conferences:

[7] **Trent Gwo-Yann Lee**, Tseung-Yuen Tseng, Shyh-Chyi Wong, Cheng-Jer Yang , Mong Song Liang, Huang-Chung Cheng, "Interconnect Optimization Design with Guaranteed Performance Methods", Proc. International Symposium on Integrated Circuits, Devices & Systems (ISIC) 2001

[8] **Trent Gwo-Yann Lee**, Tseung-Yuen Tseng, Shyh-Chyi Wong, Cheng-Jer Yang , Mong Song Liang, Huang-Chung Cheng, "The Generalized Delay Time and Crosstalk Models for the Interconnect Optimization Design", Proc. International Symposium on Integrated Circuits, Devices & Systems (ISIC) 2001

Patents:

[9] 鄭晃忠, **李國曄**, 楊正杰: "金屬連線寄生電容的量測結構及其量測方法", 中華民國專利, No.

472335。

[10] 鄭晃忠, **李國暖**, 史德智, 黃全洲, 許獻文:"鐵電非揮發性記憶單元之結構", 中華民國專利, No. 448568。