國 立 交 通 大 學

機械工程學系

碩 士 論 文

負回授多級放大電路之設計與實作

A Feedback Structure for Muti-Cell Linear Power Amplifier Circuit

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碩 士 論 文

A thesis

Submitted to Department of Mechanical Engineering

College of Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

In

Mechanical Engineering

August 2009

Hsinchu, Taiwan, Republic of China

中華民國九十八年八月

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摘要

本文內容提出一負回授多級放大電路的架構，此電路架構延續著多級放大電路可平均將高總功率消耗分散至各級的特點，並加以改良為一負回授架構，以提高其抗雜訊能力。且針對此架構所需的交換式供電系統作研究及實作。文中首先回顧開迴路多級放大電路的分析及數學模型。隨後接續著提出一負回授的多級放大電路架構，對此電路架構提出了數學模型分析及模擬，並對此架構作六級架構的設計與模擬。之後介紹交換式電源供應器的理論、返馳式電源供應器控制電路的分析。最後實際製作一 100W 的返馳式電源供應器，並量測其參數。

A Feedback Structure for Multi-Cell Linear Power Amplifier Circuit

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Abstract

This article proposes a feedback structure for the multi-cell linear power amplifier circuit, which maintains the merit to divide total power dissipation to the each module. And the feedback structure can promote the ability to resist noise. The switching power supply needed by the circuit is also discussed in this article. In the beginning, we reviewed the multi-cell linear power amplifier circuit then propose a feedback structure of this circuit. The mathematical model is later build up and a six cells design of this structure is then made and analyzed. The theory of switch mode power converters is introduced. The control circuit of flyback converter is later illustrated. A 100W flyback converter is made and measured to compare with simulations.

誌　謝

首先真誠的感謝成維華教授和鄭時龍博士，感謝兩位老師在學生兩年的碩士生涯中的指導，不論在求學問的態度與做人處事的道理，讓學生在這兩年收穫良多。

感謝實驗室向斌學長、葛雷學長和黑人學長，給予的指導及照顧，學磊、星雲、富源、強哥、文彬、洋豪和小賴學長在經驗上的傳承。感謝同屆身高一般但籃球身手不凡的文祥(小妞豬)、身高差不多但手比我長10公分的冠今(砍怕啦)、熱愛宅物的宅宅安鎮(槍鎮)和愛看書的志隆，還有一票熱愛電力電子的學弟們。

系足的同胞們在我研究所兩年共同奮戰，拿到了大機盃冠軍、系際盃冠軍、交大足球聯賽冠軍等等，還把我踢的世界波拍成影片，實在是揪甘心。

最後也是最重要的是要感謝我的父母及家人，做為我強力的後盾讓我能無後顧之憂全力衝刺學業，三不五時還帶一些好料的來讓我有一兩餐能不用吃交大的.....。

丁之浩　謹於　2009.08

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Chapter 1 Introduction

1.1. General Introduction

The Multi-Cell Linear Power Amplifier is proposed for applications involving high capacitive load and large voltage output swing, such as piezoelectric (PZT) actuator drivers. Voltage amplifiers are often used to drive piezoelectric actuators because they can precisely generate any waveform. The Multi-Cell Linear Power Amplifier is one of the topology of voltage amplifiers. It has the advantages including approximately constant corner frequency and high common mode rejection ratio (CMRR), which offer the accuracy and linearity for piezoelectric applications. Strong electrical isolation keeps high voltages away from equipment and reduces the risk if electrical shock. The drawback of the multi-cell circuit topology is that many isolated switching power supply units are required to feed the individual cell of power.[1][2]

1.2.Literature Review

An innovative amplifier called Multi-Cell Linear Power Amplifier is proposed for application involving high capacitive load and large voltage output swing. It's bandwidth can up to 100kHz with ±200V output swing.[1][2]

Nomenclature

α , α_N , α_P : Resistance ratio of closed-loop amplifier

A_D , $\mathbf{A_D}$: Open loop dc gain and frequency response of operational

amplifier

A_C : Closed loop dc gain of operational amplifier

A_I , $\mathbf{A_I}$: Differential gain and frequency response of isolation amplifier

V_{i+} , V_{i-} : Input signal of difference amplifier

V_b : Bias voltage of the power supply

V_{bs} : Bias voltage of isolation amplifier

V_{in} : Input voltage of isolation amplifier

V_o : Output voltage of difference amplifier

V_{o+} , V_{o-} : Output voltage of floating signal module

V_{out} : Differential output voltage of floating signal module

V_{ps} : Power supplies of operational amplifier

V_G : Ground potential

ω : Frequency operator

ω_c : Cutoff frequency of operational amplifier

ω_{ci}, ω_{cs} : Bandwidth of isolation and difference amplifier

1.2.1. Differential Amplifier

The differential gain $\mathbf{A_D}$ of the operational amplifier (op-amp) is given by

$$\mathbf{A}_{\mathbf{D}}(j\omega) = \frac{A_D}{1 + \frac{j\omega}{\omega_c}} \tag{1.1}$$

Where ω_c denotes the 3dB cut off frequency. Providing a bias voltage on the power supply V_b, the output voltage of the difference amplifier, as illustrated in Fig 2.1, is expressed as

$$V_o = \left(\frac{\alpha_N}{\alpha_P}(\alpha_P - 1)V_{i+} - (\alpha_N - 1)V_{i-} \right) \frac{\mathbf{A}_{\mathbf{D}}}{\mathbf{A}_{\mathbf{D}} + \alpha_N} + V_b \tag{1.2}$$

The bandwidth of the difference amplifier ω_{cs} is derived from (1.2) for $A_D >> \alpha_N$

$$\omega_{cs} = \left(1 + \left(\frac{A_D}{\alpha_N} \right) \right) \omega_c \approx \frac{A_D \omega_c}{\alpha_N} \tag{1.3}$$

If $V_b = 0$, then the output voltage swing is bounded by the power supply, i.e., $\pm V_{ps}$. As illustrated in Figure 1.2(a), the dotted line indicating the output signal is bounded by solid lines indicating power supply voltages. Conversely, the supply voltages may be varied, i.e., $V_b = V_b(t)$, to yield different output signals as indicated in Figure 1.2(b). Such a power supply providing output voltage $V_{ps} + V_b(t)$ is called the floating power supply. An op-amp feedback application should always be restricted by a constant-gain-bandwidth product [3]. According to (1.3), the difference amplifier has a large close-loop bandwidth (ω_{cs}) corresponding to a small close-loop voltage gain (α_n).

1.2.2. The Isolated Floating Difference Amplifier

A difference amplifier using floating power supplies can generate sufficiently large output signal with respect to the ground as shown in Figure 1.2(b). Such an amplifier structure may comprise an isolation amplifier, and a difference amplifier with floating power supplies called the isolated floating difference amplifier, as illustrated in Figure 1.3. Providing the differential gain of the isolation amplifier $\mathbf{A_I}$ and the bias voltage of the isolation amplifier V_{bs}, the differential outputs of the isolation amplifier may be obtained where

$$V_{i+} = -\frac{\mathbf{A_I}}{2} V_{in} + V_b + V_{bs} \tag{1.4a}$$

$$V_{i-} = \frac{\mathbf{A_I}}{2} V_{in} + V_b + V_{bs} \tag{1.4b}$$

The isolation amplifier imposes a bias voltage V_b on the input signal of difference amplifier. The biased input signal is then fed into the difference amplifier to modify the common-mode voltage. For simplicity, α_P-1 =α_N-1 = α may be selected, where $A_D >> \alpha >> 1$. By substituting (1.4a) and (1.4b) into (1.2), the output of an isolated floating difference amplifier is obtained as

$$V_o = -\frac{\mathbf{A_D A_I} \alpha V_{in}}{\mathbf{A_D} + \alpha_N} + V_b \tag{1.5}$$

1.2.3. Multi-Cell Amplifier

A. Floating Signal Module

Figure 1.4 illustrates a floating signal module based on the isolated floating difference amplifier. Each floating signal module comprises one non-inverting

amplifier and one inverting amplifier. The output swing is therefore double the swing that would be produced by a single difference amplifier. The output voltage of the non-inverting amplifier is

$$V_{o+} = \frac{\mathbf{A}_{\mathbf{D}}\mathbf{A}_{\mathbf{I}}\alpha V_{in}}{\mathbf{A}_{\mathbf{D}} + \alpha_N} + V_G \tag{1.6}$$

The output voltage of the inverting amplifier is

$$V_{o-} = -\frac{\mathbf{A}_{\mathbf{D}}\mathbf{A}_{\mathbf{I}}\alpha V_{in}}{\mathbf{A}_{\mathbf{D}} + \alpha_N} + V_G \tag{1.7}$$

The overall output of the floating signal module is

$$V_{out} = V_{o+} - V_{o-} = \frac{2\mathbf{A}_{\mathbf{D}}\mathbf{A}_{\mathbf{I}}\alpha}{\mathbf{A}_{\mathbf{D}} + \alpha_N} V_{in} \tag{1.8}$$

The output signal is independent on the ground pin, which is the key to the flexibility of the floating signal module.

B. Cascaded Multi-Cell Amplifier

The cascaded multi-cell amplifier shown in Figure 1.5 consists of familiar floating signal modules in cascaded connection. Each floating signal module is made from low voltage devices and provides both positive and negative analogous voltage levels. In the following, the superscript i refers to the i^{th} cell of floating signal module. The isolated bipolar power sources are required to

provide sufficient power to the floating signal module and to deliver a specified power to a load. Previous results indicate that each floating signal module yields two output voltages $V_{O+}^{(i)}$ and $V_{O-}^{(i)}$, which are equal in magnitude but anti-phase. The non-inverting output terminal of the $(i-1)^{th}$ cell of the floating signal module is directly connected to the inverting output terminal of the i^{th} cell of the floating signal module

$$V_{o+}^{(i-1)} = V_{o-}^{(i)} \tag{1.9}$$

Substituting (2.6), (2.7) into (2.9) and rearrange the terms yields

$$V_G^{(i)} = V_G^{(i-1)} + \frac{2\mathbf{A}_\mathbf{D}\mathbf{A}_\mathbf{I}\alpha}{\mathbf{A}_\mathbf{D} + \alpha_N} V_{in} \tag{1.10}$$

The maximum output voltage between the non-inverting output terminal of the i^{th} cell of the floating signal module and the inverting output terminal of the first cell of the floating signal module is

$$V_{O+}^{(i)} - V_{O-}^{(1)} = \frac{\mathbf{A}_\mathbf{D}\mathbf{A}_\mathbf{I}\alpha}{\mathbf{A}_\mathbf{D} + \alpha_N} V_{in} + V_G^{(i)} + \frac{\mathbf{A}_\mathbf{D}\mathbf{A}_\mathbf{I}\alpha}{\mathbf{A}_\mathbf{D} + \alpha_N} V_{in} - V_G^{(1)} \tag{1.11}$$

Solving the ground potential among each cell circuit by recursively commutating from (1.10) enables (1.11) to be rewritten as

$$V_{O+}^{(i)} - V_{O-}^{(1)} = i\frac{2\mathbf{A}_\mathbf{D}\mathbf{A}_\mathbf{I}\alpha}{\mathbf{A}_\mathbf{D} + \alpha_N} V_{in} \tag{1.12}$$

The synthesized voltage waveform may be specified as a sum of output voltages of floating signal module cells. Any number of floating signal modules may

have in general any number of cells.

1.3.Thesis Structure

In the next chapter we will propose a feedback structure for the Multi-Cell Linear Power Amplifier which we suggest to have better performance than the open-loop structure. And we will introduce the flyback converter which is one topology of the isolated switching power supply. The converter is for the purpose to feed the Multi-Cell Linear Power Amplifier circuit.

Chapter 2 Feedback Structure for Multi-Cell Linear Power Amplifier

2.1. Topology of the Feedback Structure

A feedback structure is proposed here to improve the multi-cell circuit. The advantage of the closed-loop system is that the use of feedback make the system response relatively insensitive to external disturbances and internal variations in system parameters and still keeps the advantages of the multi-cell amplifier. The topology of a feedback structure is shown in Figure 2.1.In this topology we use several resistors to take out a part of output voltage for feedback use. The feedback circuit is consisted of two op-amps and one isolation amplifier. The first op-amp is use to adjust the take out voltage to meet the input limitation of the isolation amplifier. The second op-amp is use to adjust the feedback parameter to meet our design. The isolation amplifier is used for the purpose of electrical isolation between the input device and the output load.

2.2. Mathematical Modeling of the Feedback Structure

To analyze the characteristic of the closed loop circuit, we develop a mathematical model. First we introduce the electronic components we selected for this circuit. For the isolation amplifiers we choose HCPL 7820, for the difference amplifiers we choose LM3875 and for the op-amps we choose LM6361. The abbreviated specifications of these electronic components are shown in Table 2.1. By the discussion we made in chapter 1 we can write the

mathematical model of isolation amplifier as

$$\mathbf{A}_{\mathbf{I}}(j\omega) = \frac{A_I}{1 + \frac{j\omega}{\omega_{ci}}} \tag{2.1}$$

And repeat (1.1) we write the mathematical model of the difference amplifier as

$$\mathbf{A}_{\mathbf{D}}(j\omega) = \frac{A_D}{1 + \frac{j\omega}{\omega_{cs}}} \tag{2.2}$$

The other op-amps we used in the circuit we can write their models separately as

$$\mathbf{A}_{\mathbf{op1}}(j\omega) = \frac{A_{op1}}{1 + \frac{j\omega}{\omega_{cop1}}} \tag{2.3}$$

$$\mathbf{A}_{\mathbf{op2}}(j\omega) = \frac{A_{op2}}{1 + \frac{j\omega}{\omega_{cop2}}} \tag{2.4}$$

Therefore we can draw our system block diagram as in Fig 2.2 according to the topology and the models we made. Where $\mathbf{A_{op1}}(j\omega)$, and $\mathbf{A_I}(j\omega)$ has already shown in (2.1) and (2.3). Forward transfer function $\mathbf{G}(j\omega)$ and feedback transfer function **H(jω)** can be express as (2.5) and (2.6).

$$\mathbf{G}(j\omega) = 2i\mathbf{A}_{\mathbf{op1}}(j\omega)\mathbf{A}_{\mathbf{I}}(j\omega)\mathbf{A}_{\mathbf{D}}(j\omega) \tag{2.5}$$

$$\mathbf{H}(j\omega) = \mathbf{K}(j\omega)\mathbf{A}_{\mathbf{I}}(j\omega)\mathbf{A}_{\mathbf{op2}}(j\omega) \tag{2.6}$$

Where i is the number of cells and $\mathbf{K}(j\omega)$ is the transfer function of the

output voltage sampling circuit which we will discuss in the next section.

The closed-loop system transfer function $\mathbf{T}(j\omega)$ becomes

$$\mathbf{T}(j\omega) = \frac{2i\mathbf{G}(j\omega)}{1+2i\mathbf{G}(j\omega)\mathbf{H}(j\omega)} = \frac{2i\mathbf{A}_{op1}(j\omega)\mathbf{A}_{I}(j\omega)\mathbf{A}_{D}(j\omega)}{1+2i\mathbf{K}(j\omega)\mathbf{A}_{I}(j\omega)\mathbf{A}_{op2}(j\omega)\mathbf{A}_{op1}(j\omega)\mathbf{A}_{I}(j\omega)\mathbf{A}_{D}(j\omega)} \quad (2.7)$$

2.3. System Compensation

First, we give the values of the parameters of the model refer to the specifications [9][10][11] of the components we choose and the DC gain of $\mathbf{T}(j\omega)$ to be 40. The values of the parameters are shown in table2.2. Initially, we let $K(0)$ to be a constant, which implement to the circuit is a voltage divider using the resistors. The Bode plot of the mathematical model is shown in Figure2.3. We can see from the simulation result that the system phase margin and the system gain margin are both negative, so the system is unstable and need to be compensated.

We set our target to compensate the phase margin to have at least 30 degrees. The phase lead-lag compensator is the method we utilize. Considering the gain cross frequency at w_g and the slope is -60db/Decade, we plan to use three passive filters to compensate. The circuit of the passive filter is shown in Figure2.4. We can write the transfer function of the passive filter as

$$\frac{V_{p,\,out}}{V_{p,\,in}} = \frac{R_2}{2R_1 + R_2} \frac{1 + R_1 C_1 s}{1 + \frac{R_2}{2R_1 + R_2} R_1 C_1 s} \tag{2.8}$$

Where $V_{p,in}$ is the input voltage of the passive filter and $V_{p,out}$ is the output voltage of the passive filter. Then we can write the pole introduce by the passive filter as (2.9).

$$\frac{2R_1 + R_2}{R_2} \frac{1}{2\pi R_1 C_1} \tag{2.9}$$

And the zero introduce by the passive filter as (2.10).

$$\frac{1}{2\pi R_1 C_1} \tag{2.10}$$

We set the zeros of the three passive filters around w_g and the poles according to the following equation

If we use three identical passive filters, the value of the resistors can be decided by (2.11) and the poles should be (2.12)

$$\mathbf{K}(0) = \left(\frac{R_2}{2R_1 + R_2} \right)^3 \tag{2.11}$$

$$\sqrt[3]{\mathbf{K}(0)} \frac{1}{2\pi R_1 C_1} \tag{2.12}$$

Thus, the transfer function of the sampling circuit **K***(jw)* can be write as

$$\mathbf{K}(j\omega) = \left(\frac{2R_1 + R_2}{R_2} \frac{1}{2\pi R_1 C_1} \right)^3 \tag{2.13}$$

2.4. Simulation Result

In this section, we will simulate both mathematical model and the circuit by software. In Figure2.5 we show the compensated system Bode plot, which we set the zeros at 1.7MHz and poles at 20.6MHz. We can see from Figure2.5 that the compensated system has a gain margin 11.1dB and a phase margin 44.4degrees. Figure2.6 and Figure2.7 show the IsSpice simulation Bode plot of the circuit implementation of the system. We can see from Figure2.6 and Figure2.7 that the compensated system has a gain margin 4.7dB and a phase margin 33degrees. The difference between the two simulations occurs at frequency over 1MHz, which we believe is cause by the high frequency poles that we didn't consider in the mathematical models.

Chapter 3 Switch-Mode Power Converter

3.1 . Introduction of Switch-Mode Power Converter

Switch-mode power converter is one of the circuit structures of DC to DC converter. Switch-mode power converter has three basic topologies: step-down, step-up, step-down/up. Those three are the fundamental and non-isolated ones, each of the three can correspond to their isolated topologies which are: buck, forward (step-down), boost (step-up), flyback (step-down/up). Depending on their operating conditions, switch-mode power converters may operate either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Under transient conditions, the operation of power converters may slide in and out both modes. For closed-loop control of converters, two fundamental mechanisms, voltage-mode control or current-mode control, are generally employed. Current-mode control has been often used for its superior performance. Current-mode control can further subdivided into average-current control and peak-current control. The switch-mode power converter we tend to design and use is the flyback converter. The chip IC we used, UC3844, is a fixed frequency current-mode control IC.

3.2 The Flyback Converter

In this section we will introduce the basic theory of the flyback converter. First, as shown in Figure3.1 we can see the basic topology of the flyback converter. When we turn on the switch, the primary winding will store energy from the primary current. In the same time, the second winding has been cut off

because the diode is reversed biased. Therefore, there is no energy transformed from primary side to the second side at this period. As we turn off the switch, the primary current comes to zero, and the transformer polarity reversed. The energy we stored in the first period then transformed to the second side. Repeating this mechanism by controlling the voltage across the gate and source of the MOSFET, we can get a continuous power output.

According to three different operating mode: continuous conduction mode (CCM), discontinuous conduction mode (DCM) and boundary conduction mode (BCM), we will have three discussions respectively.

Several assumptions we have to make before the discussions:

1. Assuming the output capacitor is ultra large and let the output voltage to be constant.
2. The circuit is operating under steady-state.
3. The switch and the diode are ideal.
4. The duty ratio is D, which means the switch turned on DT_s and turned off $(1-D)T_s$, where T_s is the period of one switching cycle.

A.. Continuous conduction mode (CCM)

Figure3.2 show the current and voltage when the converter is operating under continuous conduction mode. Figure3.3 and Figure3.4 show the equivalent circuit of the converter at $0 \sim DT_s$ and $DT_s \sim T_s$.

When the switch is on the equivalent circuit as shown in Figure3.3 we can write the primary voltage as

$$v_L = v_{in} = L_p \frac{di_p}{dt} \quad ,0 \le t \le DT_s \tag{3.1}$$

Where V_L is the voltage across the primary side of the transformer, V_{in} is the input voltage and L is the primary inductance of the transformer. We can write the change of primary winding current Δi_p as

$$\Delta i_p = \frac{V_{in} D T_s}{L_p} \tag{3.2}$$

The secondary winding current due to the reverse bias of the diode is zero

$$i_s = 0 \tag{3.3}$$

Thus, we can see from (3.3) that primary winding current gains linearly and no current flow through secondary winding when the switch is on.

As we turn off the switch at the time $DT_s \sim T_s$, the primary winding voltage is shown as follow

$$V_p = -V_{out} \frac{N_1}{N_2} = L_p \frac{di_p}{dt} \quad DT_s \le t \le T_s \tag{3.4}$$

Where V_{out} is the output voltage, N_1 is the turns of primary winding and N_2 is the turns of secondary winding. From (3.4) we can get the change of primary winding current

$$\Delta i_p = \frac{-V_{out}(1-D)T_s}{L_p} \frac{N_1}{N_2} \tag{3.5}$$

While we assume operating under steady-state, the change of the winding during a cycle should be zero. By this relation and using (3.4) (3.5) we can acquire the relation between output voltage and input voltage as

$$V_{out} = V_{in} \frac{D}{1-D} \frac{N_1}{N_2} \tag{3.6}$$

B. Boundary conduction mode (BCM)

When the flyback converter is working at boundary conduction mode, is the situation that the primary winding current decreases to zero at DT_s.

C. Discontinuous conduction mode (DCM)

The discontinuous conduction mode during the time 0~DT_s, the switch is on and just like operating under CCM, the primary winding current gains linearly and no current flow through secondary winding. But the difference with CCM is that the primary winding current of DCM will decrease to zero before the next cycle starts. Thus, each cycle the primary winding current will start from zero, we can calculate the peak current of the primary winding from (3.2)

$$i_{pp} = 0 + \Delta i_p = \frac{V_{in} D T_s}{L_p} \tag{3.7}$$

Assuming no energy loss during energy transfer, we can derive the relation between the output voltage and the input voltage by the following equations.

The average of input current I_{in} which we can calculate from the area under Figure3.5 (b) divided by a cycle time

$$I_{in} = \frac{V_{in} D^2 T_s}{2 L_p} \tag{3.8}$$

The input power is equal to the output power

$$\frac{V_{in}{}^2 D^2 T_s}{2 L_p} = \frac{V_o{}^2}{R} \tag{3.9}$$

From (3.9) we can get the relation between the output voltage and the input voltage

$$V_{out} = V_{in} D \sqrt{\frac{T_s R}{2 L_p}} \tag{3.10}$$

We can see as the comparison of CCM and DCM that the relation between the output voltage and the input voltage only depends on the turn ratio and duty ratio at CCM but depends on switching frequency, output load, primary inductance and duty ratio.

3.3 The Switching Component

In this section we will introduce the switching component used for dc to dc converters. In the early 1970s, switch-mode power converters employed bipolar junction transistors as the main power switch exclusively, since MOSFET were not yet mature for power application. Bipolar transistor switches at that time, in general, also operated at switching frequencies of lower tens of kilohertz. The latter is attributed to the slower response time as a result of distributed junction capacitances in the bipolar transistor's junctions. More important, the bipolar transistors are current-controlled devices. Effective control of the transistor requires timely injection, or removal, of charge carriers into, or out of, the base terminal.

In contrast to the bipolar transistors, the MOSFETs are voltage-controlled transistors, which is easier to drive than the bipolar transistors. In normal situation, no gate current is required. The region between the gate and the channel of the MOSFET form a parallel-plate capacitor. Only when MOSFETs are switched on/off will required current to build up the conducting channel.

To understand the switching behavior of MOSFETs, we have to consider the parasitic capacitances that exist between pairs of terminals: C_{GS}, C_{GD}, and C_{DS}. As a consequence of these capacitances, the transistor experiences a turn-on delay $t_{d(on)}$ corresponding to the time required to charge the equivalent input capacitance to the threshold voltage V_T. As shown in Figure3. , the rise time t_r is defined as the time it takes to charge the gate from the threshold voltage to the gate voltage required to have the MOSFET in the triode region V_{GSP}. The turnoff delay time $t_{d(off)}$ is the time required for the input capacitance to discharge, so that the gate voltage can drop and v_{DS} can begin to rise. As v_{GS} continues to decrease, we define the fall time t_f as the time required for v_{GS} to drop below the threshold voltage and turn the transistor off. Typical switching time is about 30ns to 50ns and is faster than the bipolar transistor.

3.4 Resistor-Capacitor-Diode(RCD) Snubber

In general, the load lines encountered in a switch-mode power converter are inductive. On the *i-v* coordinate plane, the power switch current and voltage traverse a nonlinear trajectory. This load behavior exerts significant stress on the switch in the form of local power dissipation that elevates the devices operating temperature and reduces reliability. The switching losses are associated with the transitory nature of rising and falling of switch voltage and current at the very moment of on/off state changes. The voltage rising due to an inductive *di/dt* kickback is more pronounced when the switch turns off. We, therefore, focus on the turnoff snubbers, which are intended to manage the rate of falling current.

Conventional snubbers are made of passive elements. To direct current flow in

a preferred, guided way, diodes are also used. Figure3.6 gives a turn-off RCD snubber.

The operating sequence of the circuit can be briefly described as follows. When the power switch terminates conduction, the inductive load voltage flips polarity (Figure3.7). The clamping diode conducts and keeps the magnetizing current flowing without interruption; though at a decreasing rate. The action moves the energy previously stored in the magnetic core to the capacitor. When the next on-cycle commences, the clamping diode disengages the RC network and the capacitor discharges its contents (Figure3.8).

3.5 Current Mode Control

By nature, signals in current forms have advantages over those in voltage form, since voltage is an accumulation of electron flux and, therefore, slow in time as far as control mechanism is concerned. In the early 1980s, this understanding spawned a new tide in switch-mode power supply design, namely, the current-mode control. In this control mode, the averaged or peak current of magnetic origin is employed in the feedback loop of switch-mode power converters. Figure3.9 demonstrates the general feature of a current-mode control scheme. We can see from the current-mode control scheme that two loops are involved. The external loop includes the output voltage feedback sensing error amplifier. The internal loop is the current sensing circuit.

Here, we will give an example to illustrate how peak-current current-mode control is working. In Figure 3.10 shows that the instantaneous switch current is sensed by a current sensing resistor R_{sen} that provides isolation and current

scaling. The switch is turned on at a clock edge. It is turned off when the sensed current in voltage form intercepts the error voltage, V_e (Figure3.11).

The current-mode control has some benefit compared with voltage-mode control [16]:

1. The peak current flow through the power MOSFET can be limited. Because of the peak current of the inductance is measured directly, we can limit the peak current by adjusting the current sensing resistor.
2. Can overcome the saturation of the transformer. If the transformer is saturate, extreme large current will shut down power MOSFET by the peak-current sensing mechanism.
3. Has better response time than the voltage-mode control process.
4. Has better performance to loading current modulation.

3.6 Current Mode Control Circuit

The PWM controller we used in our circuit is the UC3844, which is a peak-current current control mode IC. The UC3844 is a high performance fixed frequency current mode controllers. It is specifically designed for Off−Line and DC−DC converter applications offering the designer a cost−effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Also included are protective features consisting of input and reference undervoltage lockouts each

with hysteresis, cycle−by−cycle current limiting, programmable output deadtime, and a latch for single pulse metering. The simplified block diagram is shown in Figure3.12.

3.7 Isolated Feedback

Both voltage and current feedbacks are used effectively in modern power converters. Early on, voltage feedback had the upper hand, since it was easy to implement. Non-isolated voltage feedback is even easier. It takes just a node voltage and two resistors as a voltage divider. Of course, its simplicity hides its shortcoming—no isolation. To implement isolated voltage feedback, either magnetic or optical means must be employed. The magnetic approach requires that the voltage being fed back must first be converted into AC form. The optical approach requires that the feedback voltage be in current form to drie an optical element. Therefore, the requirement of isolation wipes out the advantage voltage feedback has over current feedback. The latter stands out as a better choice for that reason and others. In addition to the ability of offering isolation, current feedback is also less prone to noise. A voltage node with certain impedance can be easily influence by radiated emissions with no direct connection. In contrast, it is not so easy to inject unwanted current into a current-sensing branch without direct physical contact.

In Figure3.13 is a magnetic isolated feedback circuit and Figure3.14 is an optical isolated feedback circuit. The optical isolated feedback circuit involved an opto-coupler, a precision shunt regulator and several resistors. As shown in Figure3.14, the output to be regulated feeds a voltage divider that samples the

output. The sampled output is compared with a reference voltage, V_{ref}=2.5V, residing in TL431, a precision shunt regulator. The error voltage is converted into drive current for the opto-coupler, an LED and phototransistor combination. The current transfer ratio of the opto-coupler transfers the drive current. The opto-coupler output current is converted into a feedback voltage via a resistor.

Chapter 4 Experimental Results

4.1 Experimental Setup

Figure4.1 displays the photograph of the experimental setup of the flyback converter. The flyback converter is designed to supply 100W power and multiple output voltages: +40V, +15V, 0, +5V, -15V and -40V. It's maximum output voltage is 80V and output current is 1.2A.. Input voltage we give 110VAC. The load we use for testing is shown in Figure 4.3. The flyback implementation circuit schematic is in Figure 4.20.

4.2 Results of the Experiment

We measured the gate to source voltage, drain to source voltage, source voltage and 80V output of flyback converter with different loadings: no loading, 32W and 100W. The actual value due to different scale we take is not correctly shown in the oscilloscope capture picture, so we annotate the actual value below the photograph except for the source voltage, we exchange its actual voltage value to the current flow through by dividing sensing resistor R_s. Figure4.4, Figure4.5 and Figure4.6 show the output voltage and ripple for different loads. Figure4.7, Figure4.8 and Figure4.9 show the gate to source voltage which is the switching signal for the MOSFET and the source voltage which is the peak-current sensing signal. Figure4.10, Figure4.11 and Figure4.12 show the gate to source voltage and the drain to source voltage which is the voltage stress that the MOSFET has to bear.

4.3 Compare with the Spice Simulation

In Figure4.13, Figure4.14 and Figure4.15 we show the simulation result of gate to source voltage and the current on the peak-current sensing resistor. Figure4.16, Figure4.17 and Figure4.18 we show the simulation result of gate to source voltage and the drain to source voltage. The simulation spice model demonstrated in Figure 4.19.

Chapter 5 Conclusions

The feedback structure of multi-cell linear power amplifier offers a way to drive high output power loads while the total power dissipation divided into each of the modules. The switch mode flyback converter provides a way to feed the individual cell of power. Integration of the two can be a more compact and flexible solution for high power output usage.

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Figures

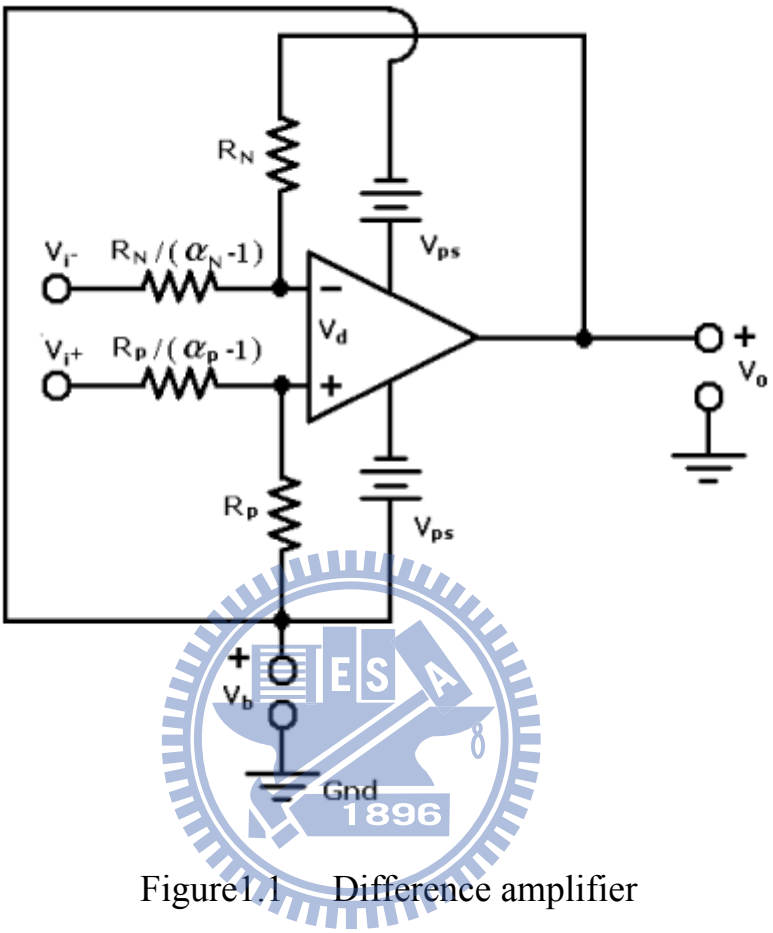


Figure1.1 Difference amplifier

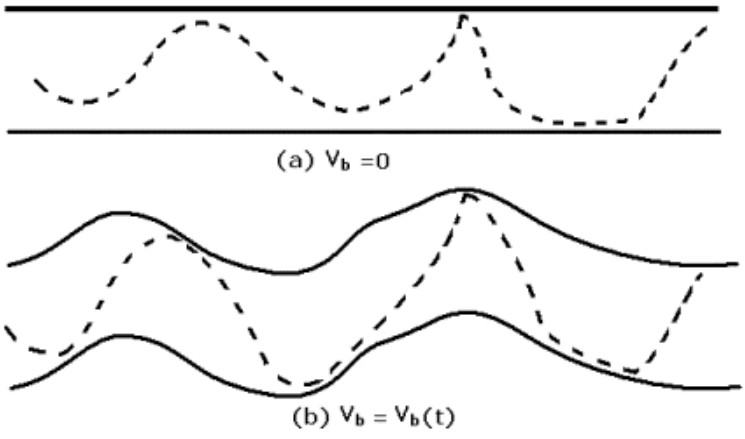


Figure1.2 Output signals from difference amplifier

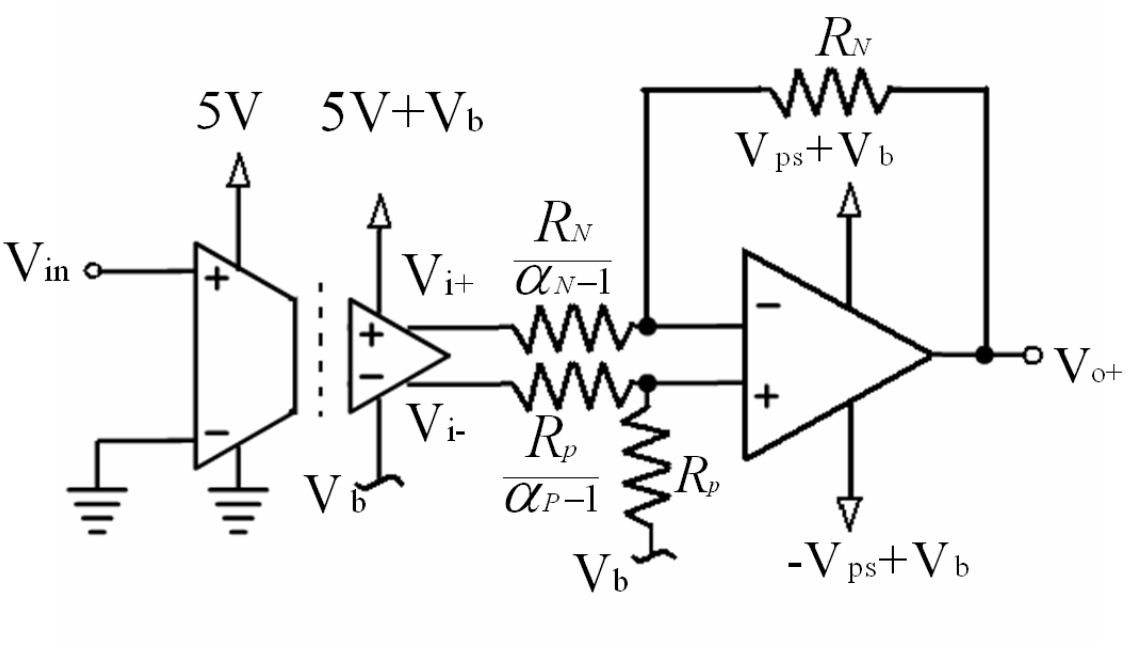


Figure1.3 Isolated floating difference amplifier

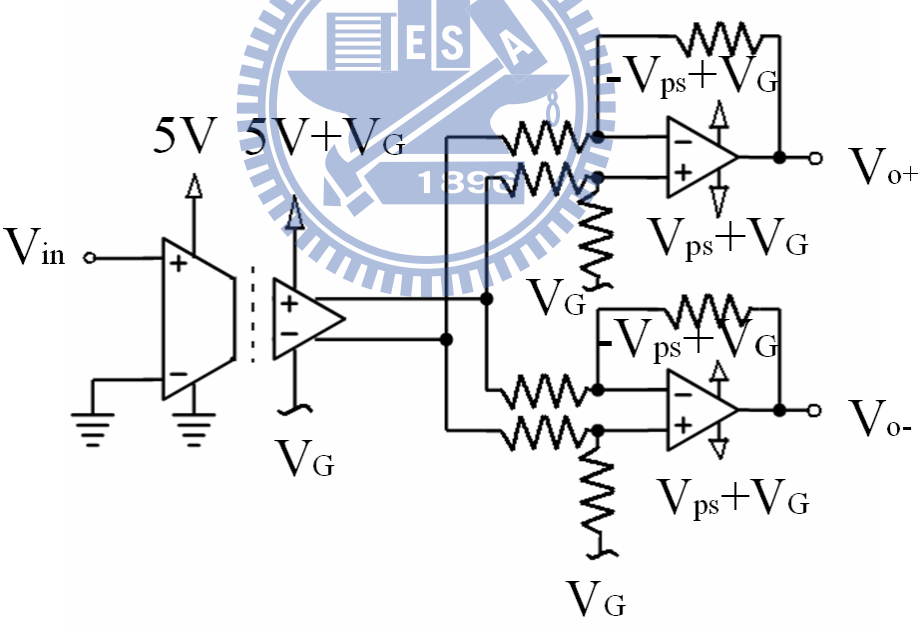


Figure1.4 A floating signal module

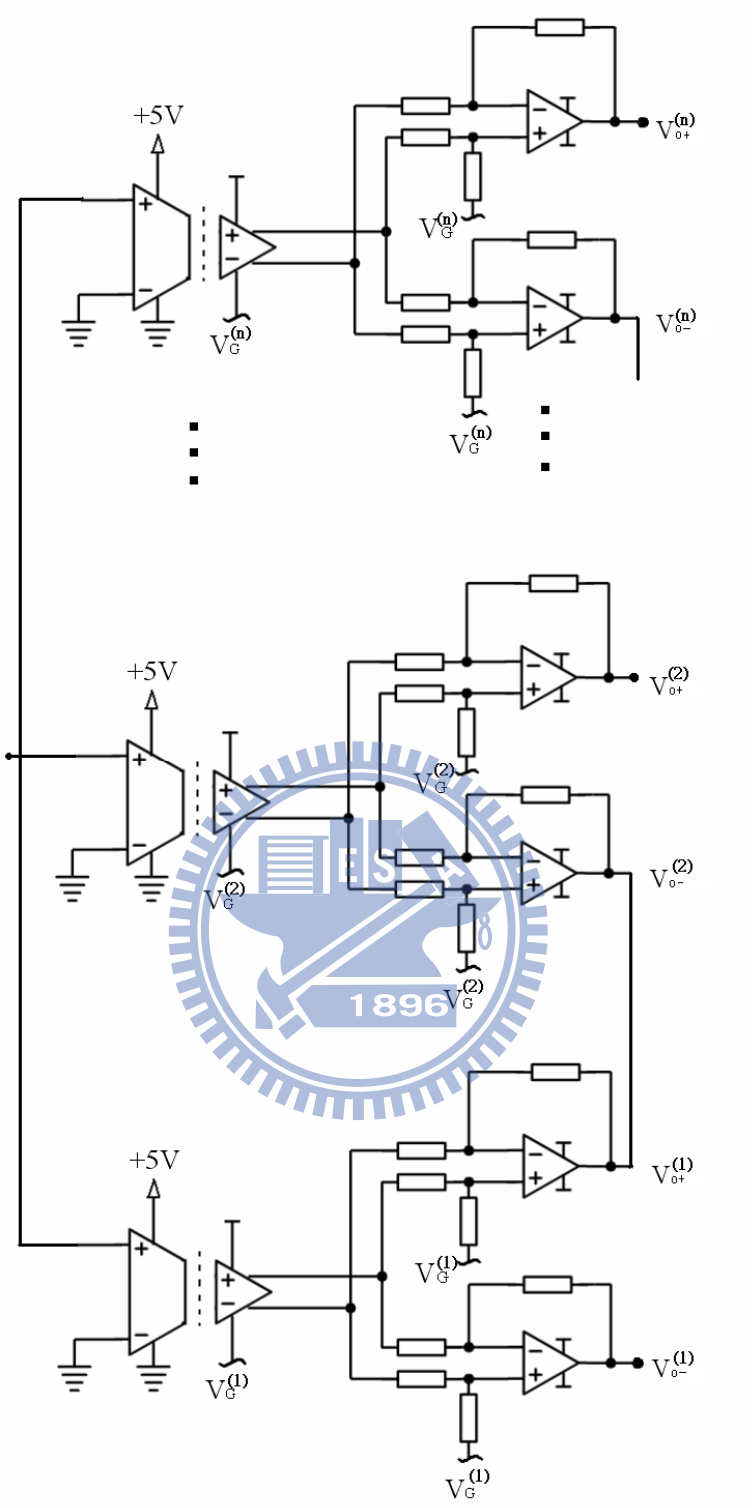


Figure1.5 The cascaded multi-cell amplifier

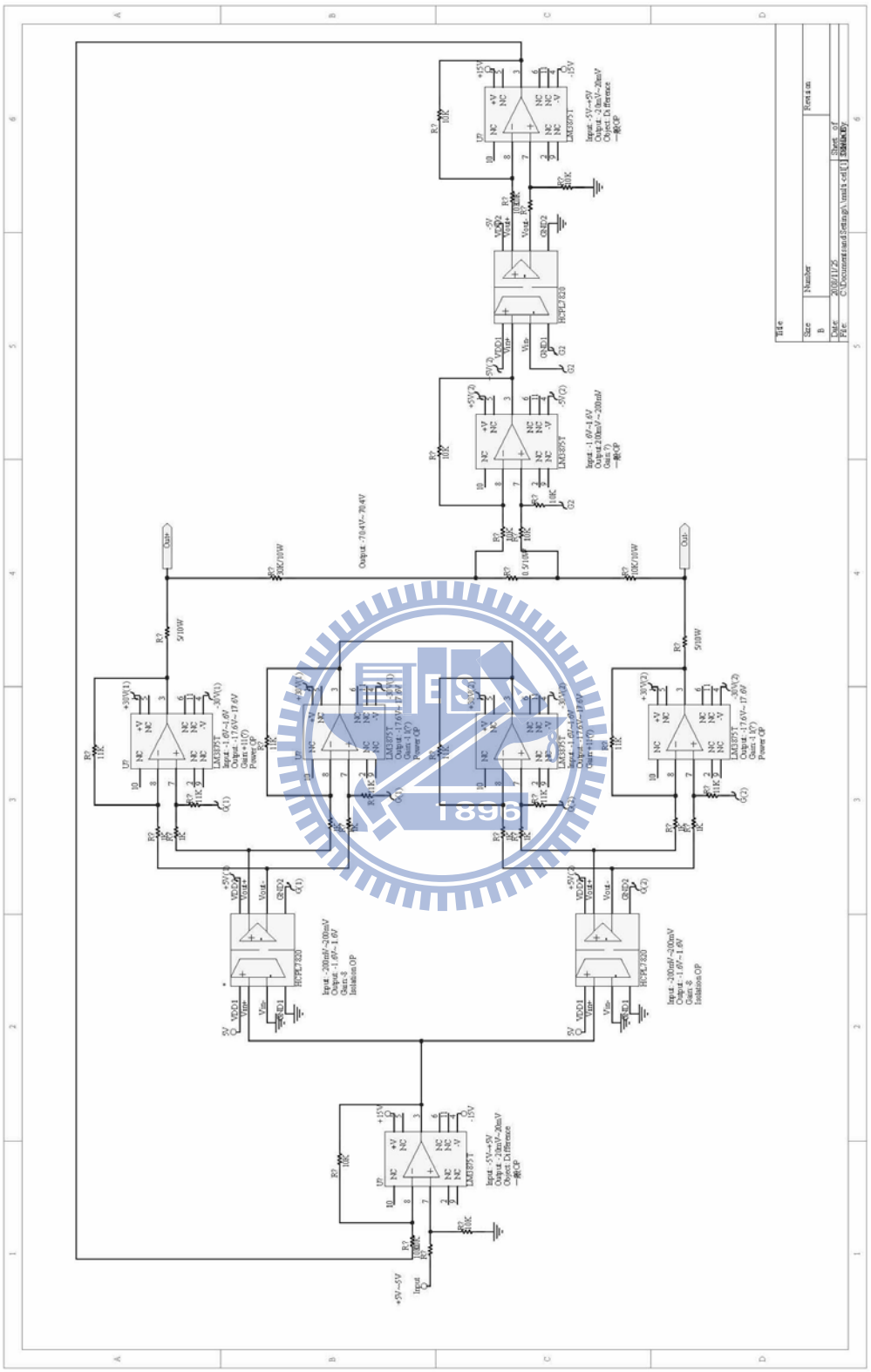


Figure2.1 The topology of the feedback structure

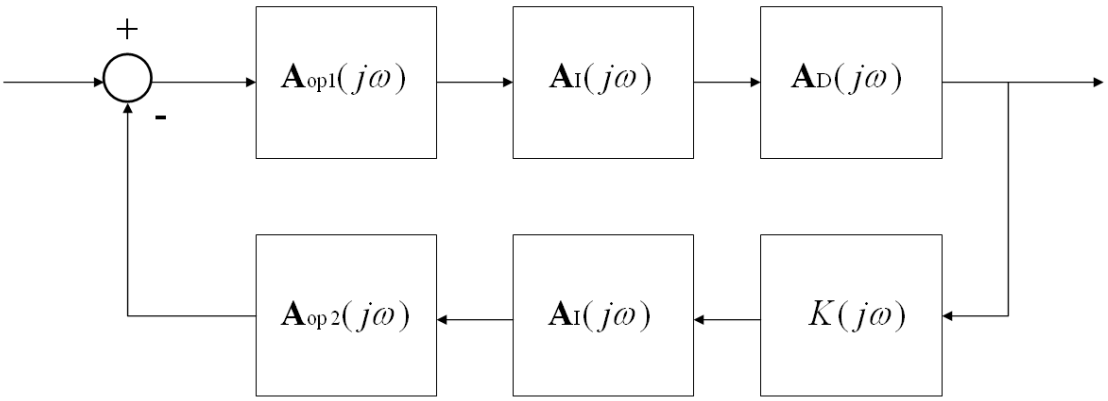


Figure2.2 The system block diagram of the feedback structure

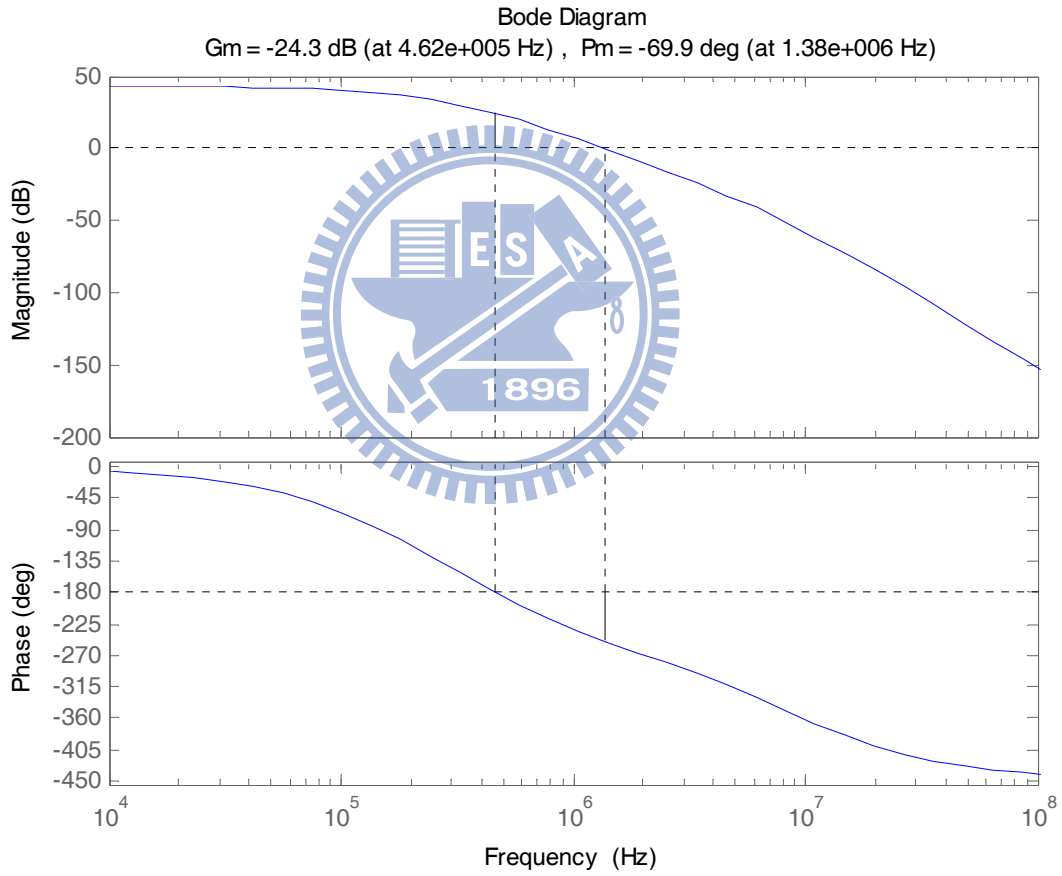


Figure2.3 The Bode plot of the uncompensated system

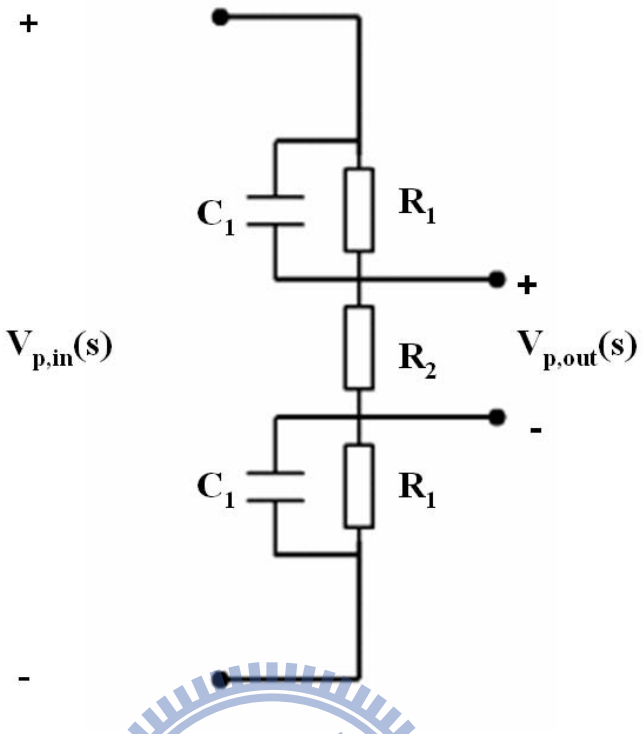


Figure2.4 The circuit of the passive filter

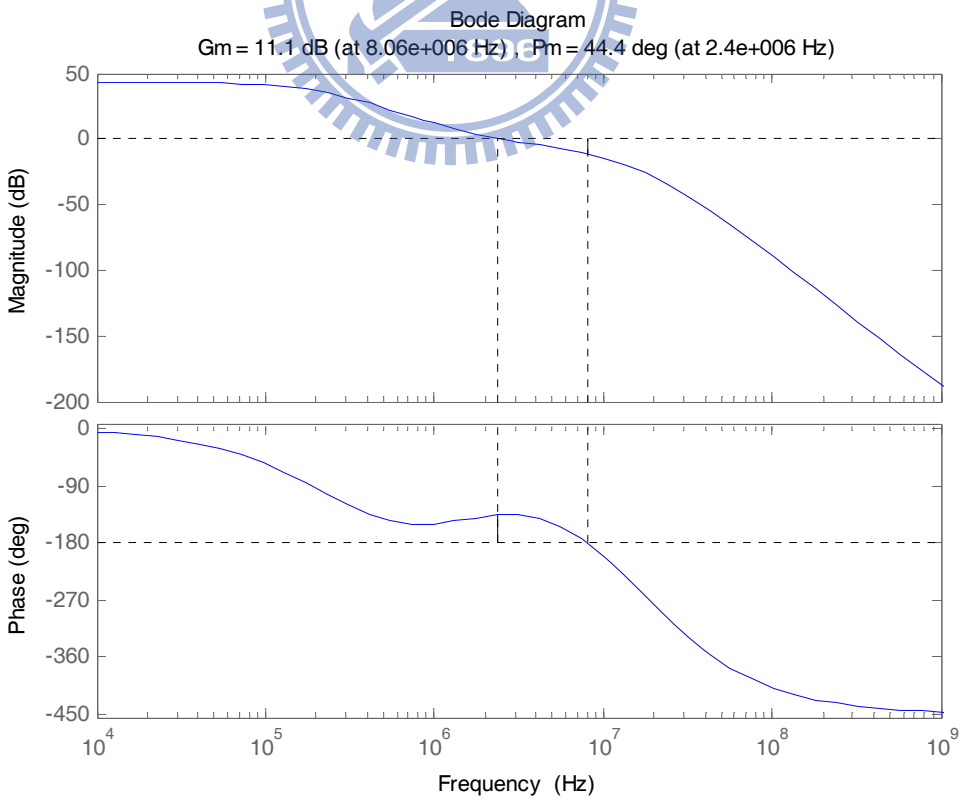


Figure2.5 The Bode plot of the compensated system

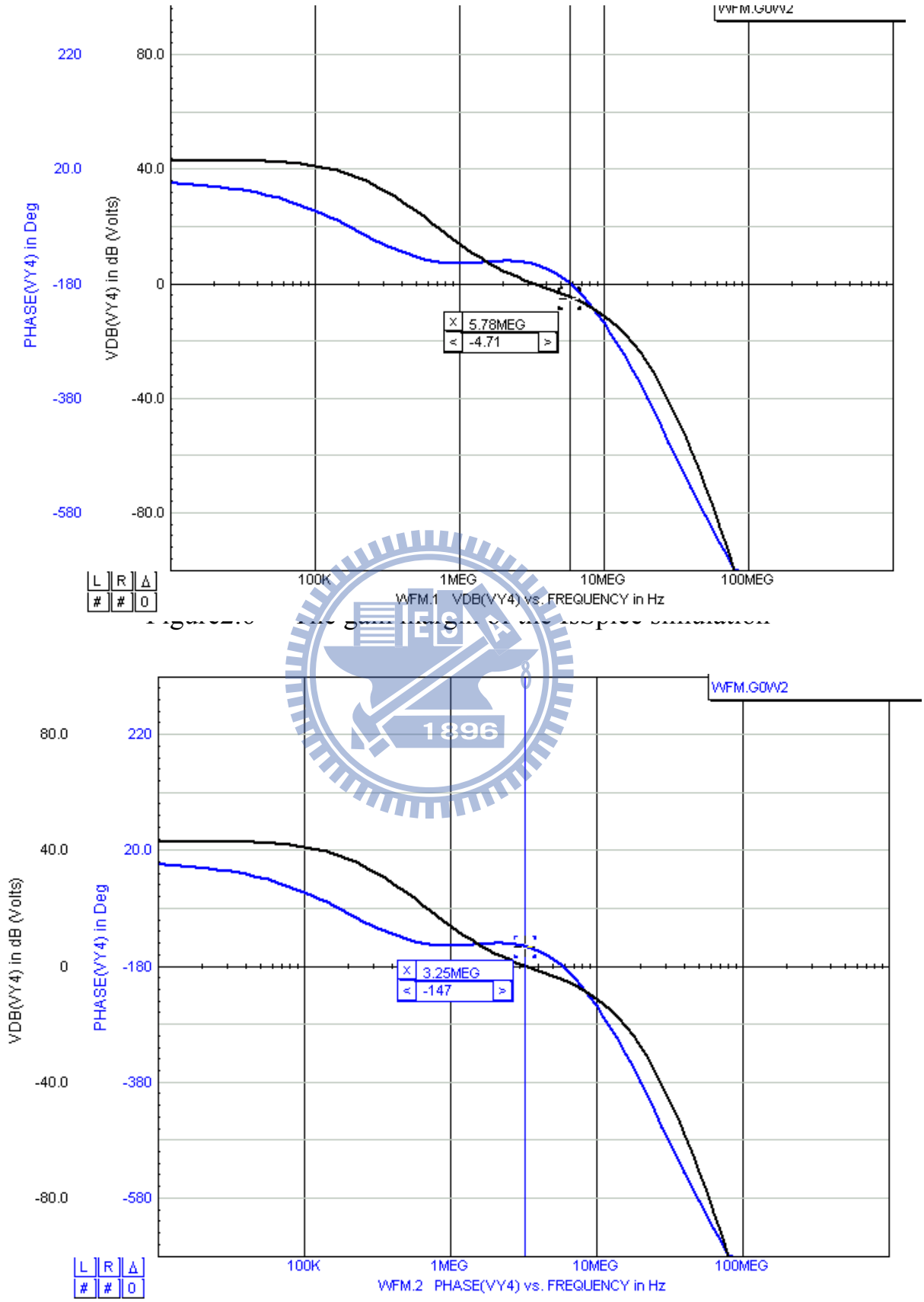


Figure2.7 The phase margin of the IsSpice simulation

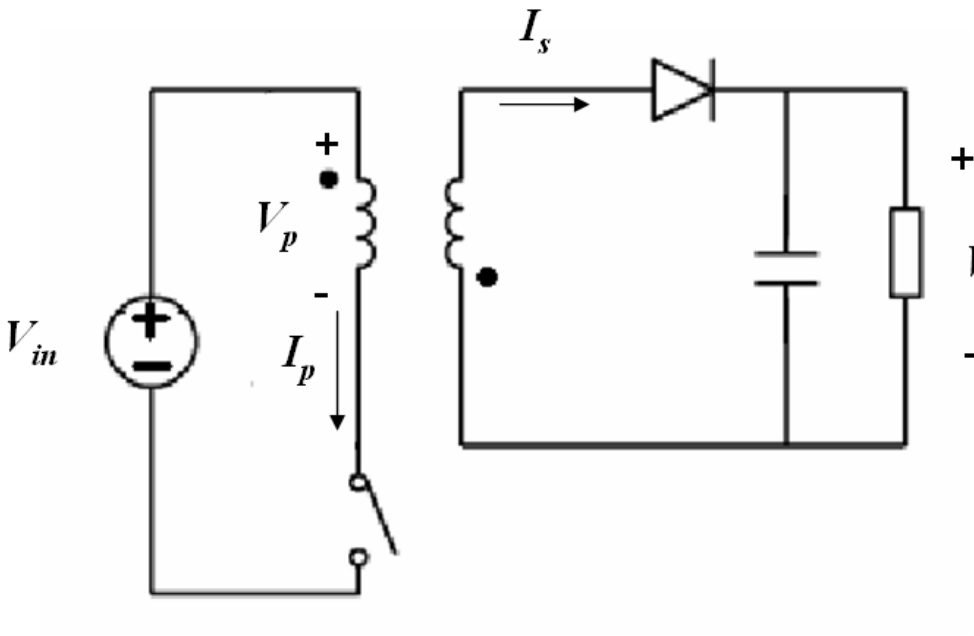


Figure3.1 The basic topology of the flyback converter

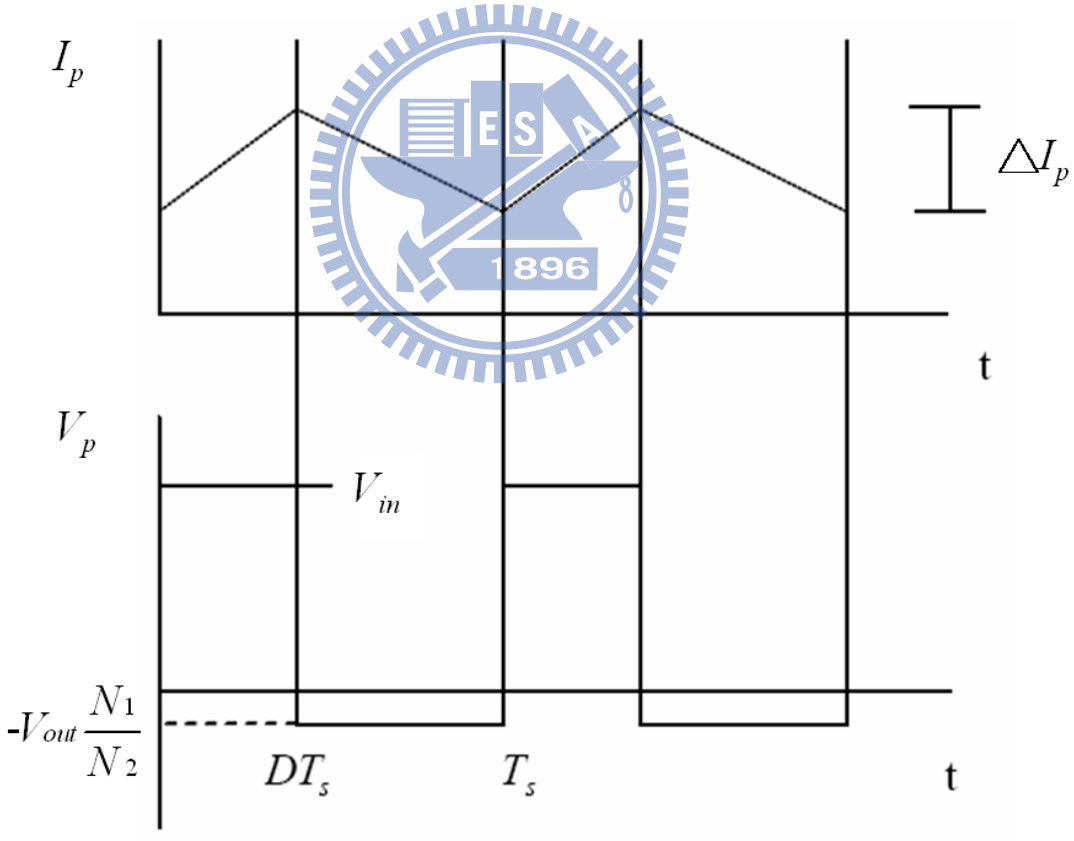


Figure3.2 Primary winding current and voltage at CCM.

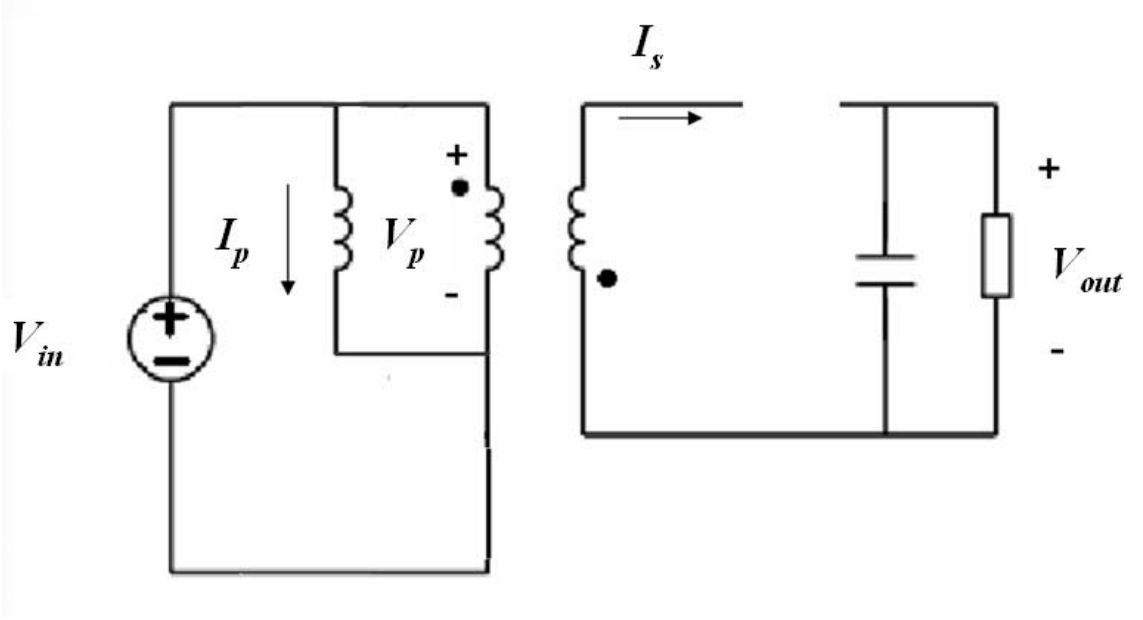


Figure3.3 The equivalent circuit of the converter at 0~ DT_s

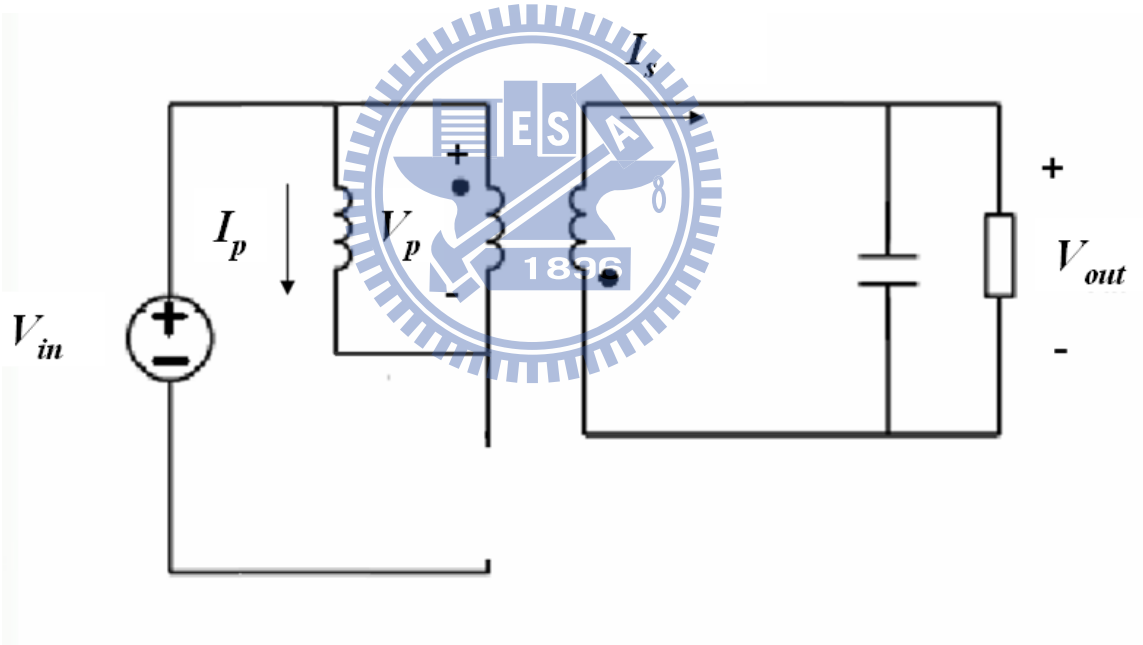


Figure3.4 The equivalent circuit of the converter at DT_s ~ T_s

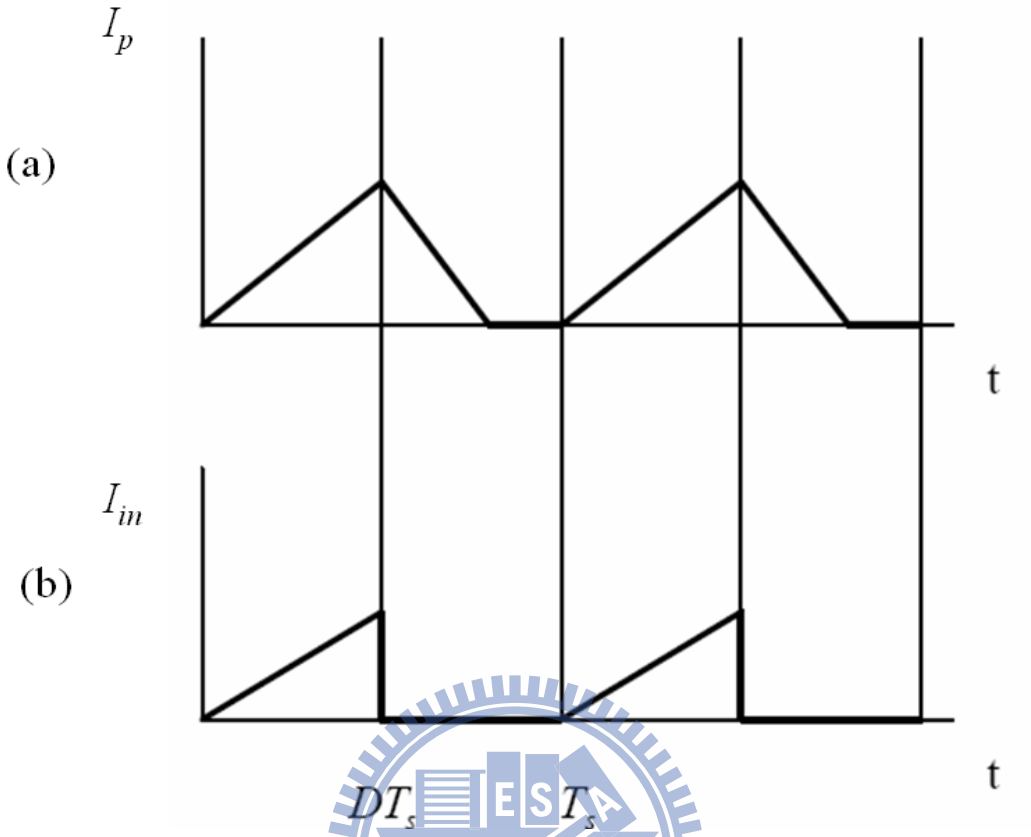


Figure3.5 Primary winding current and input current at DCM.

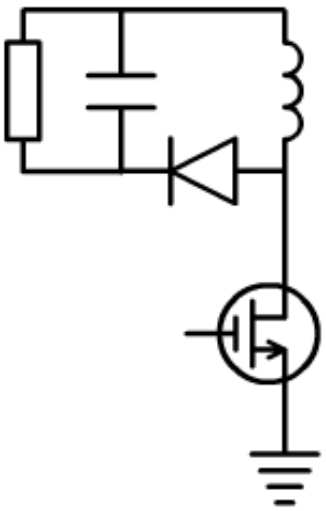


Figure3.6 RCD turn-off snubber

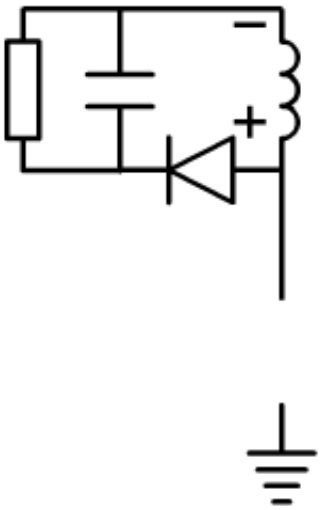


Figure3.7 RCD turn-off snubber state 1

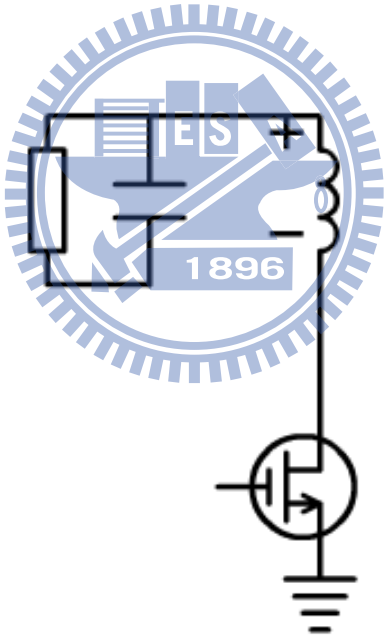


Figure3.8 RCD turn-off snubber state 2

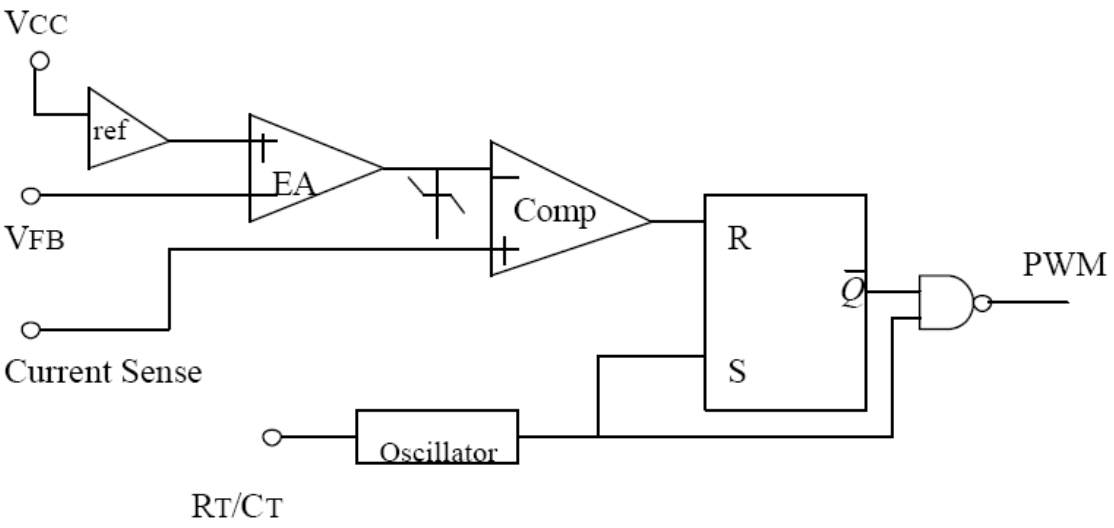


Figure3.9 Current-mode control scheme

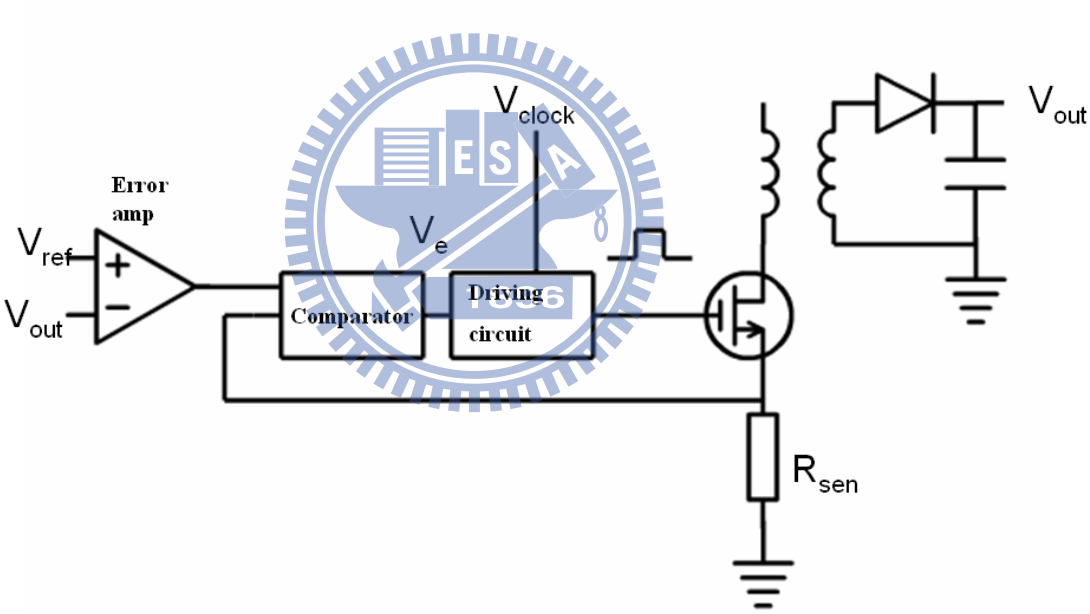


Figure3.10 Simplified current control circuit

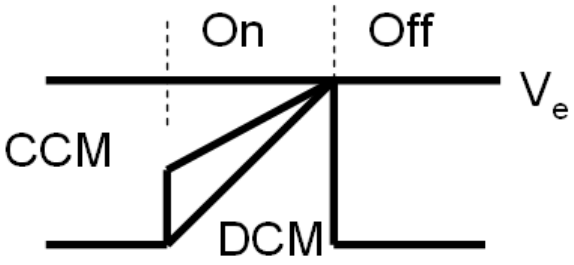


Figure3.11　Determination of the peak current-mode duty cycle

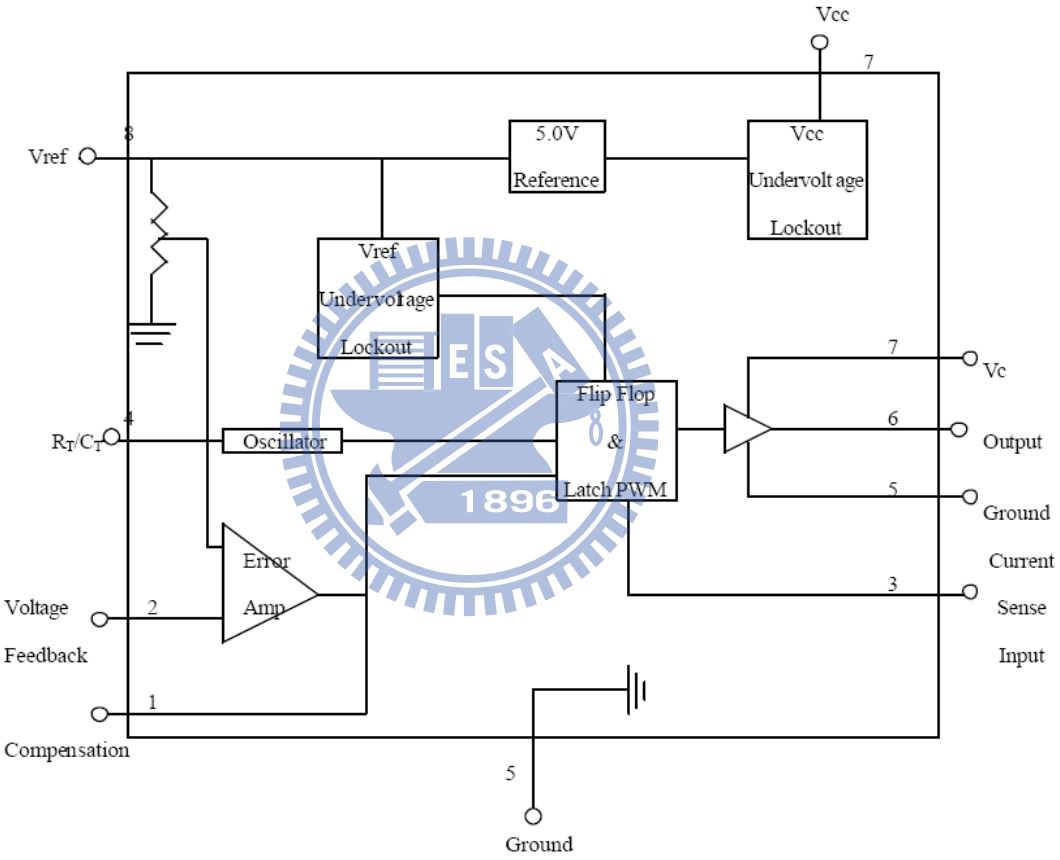


Figure3.12　Simplify block diagram of UC3844

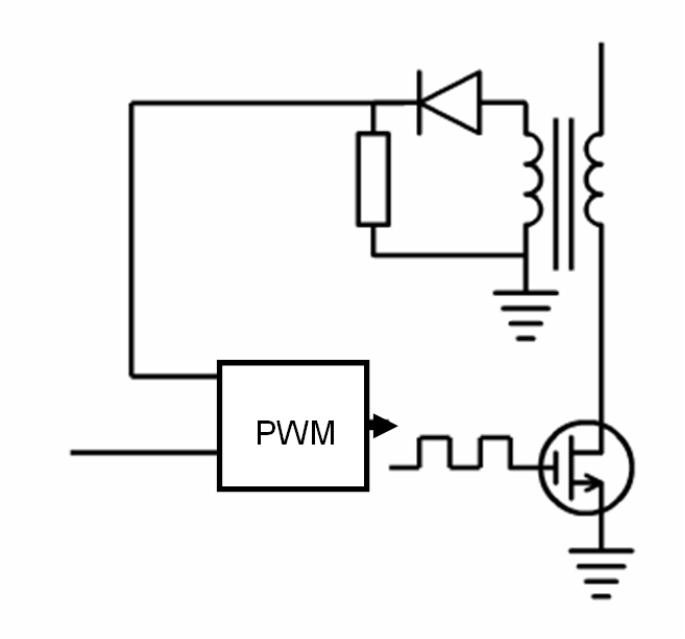


Figure3.13　Magnetic isolated feedback circuit

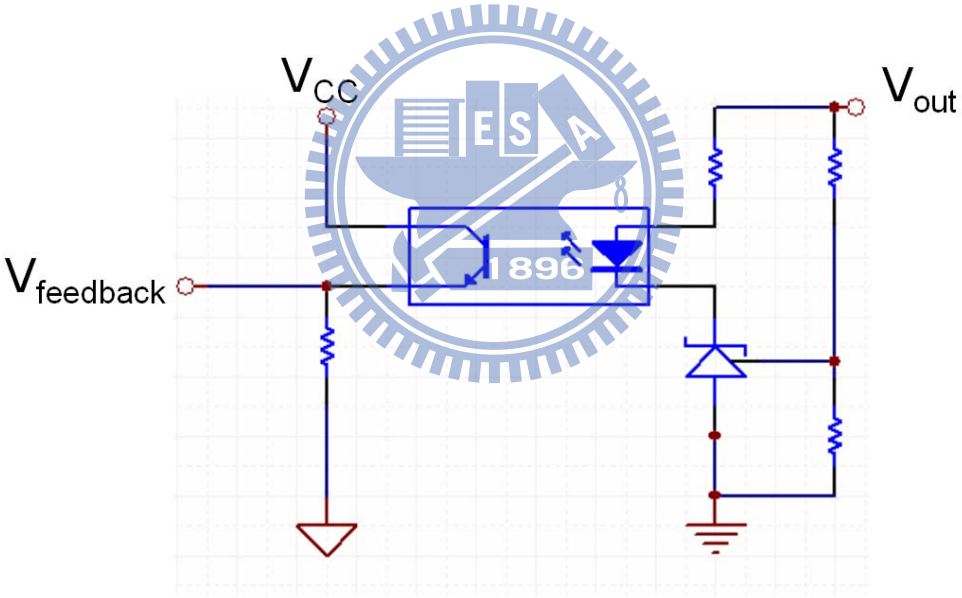


Figure3.14　Optical isolated feedback circuit

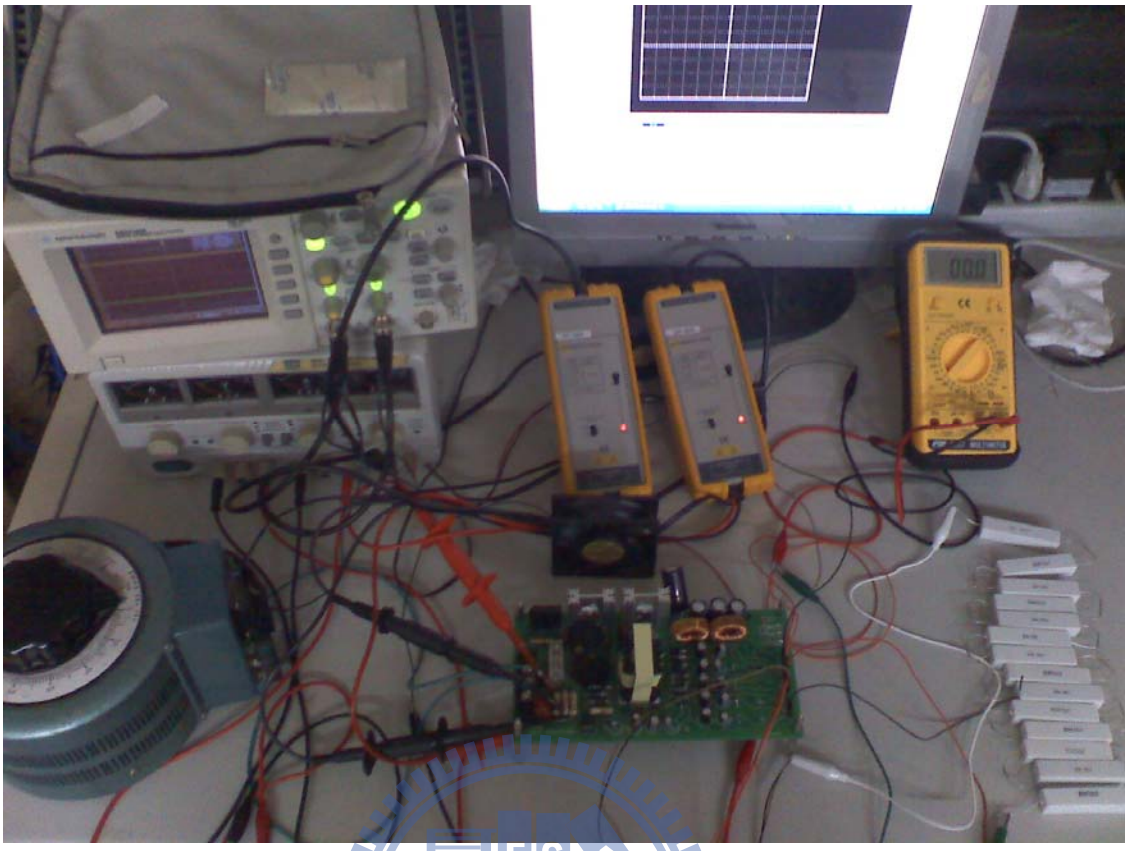


Figure4.1 Experimental setup

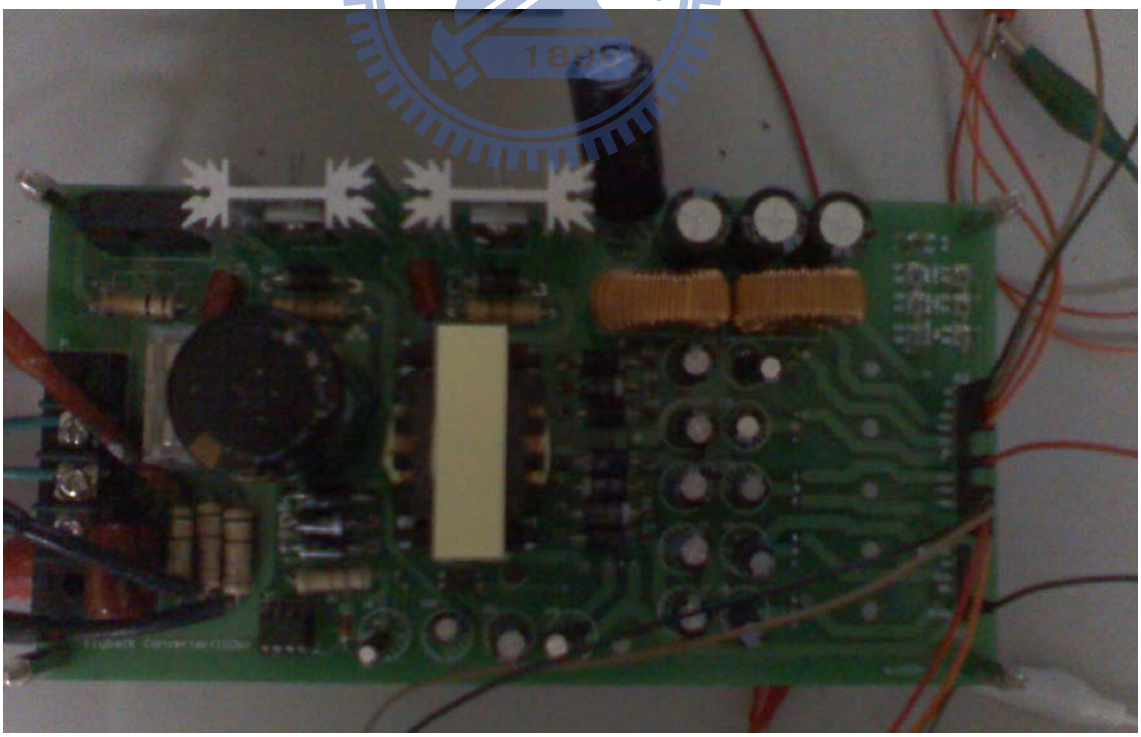
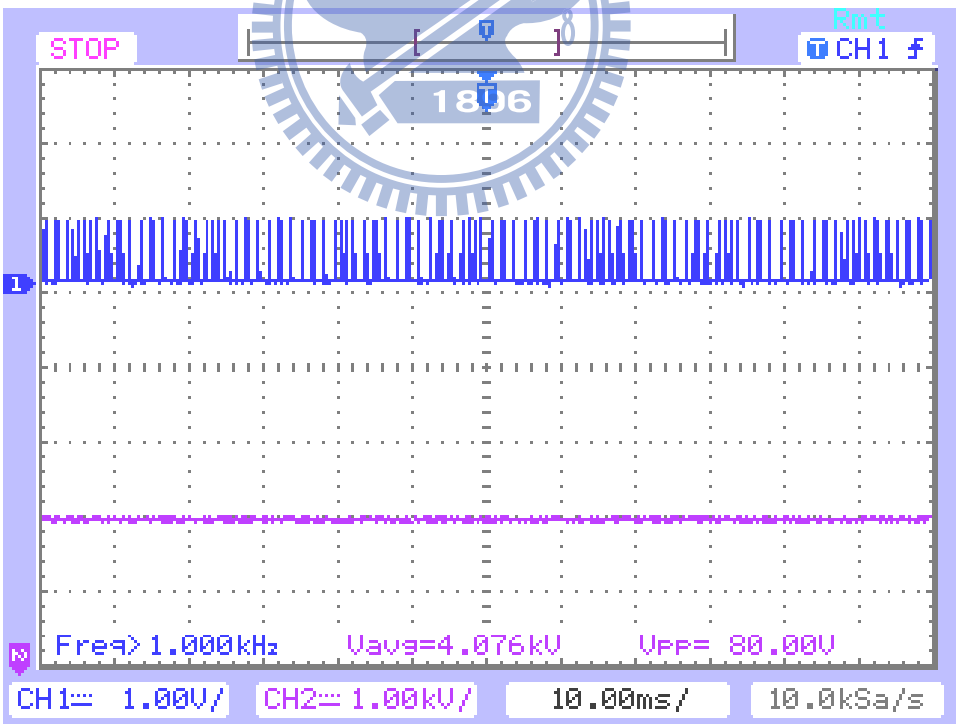


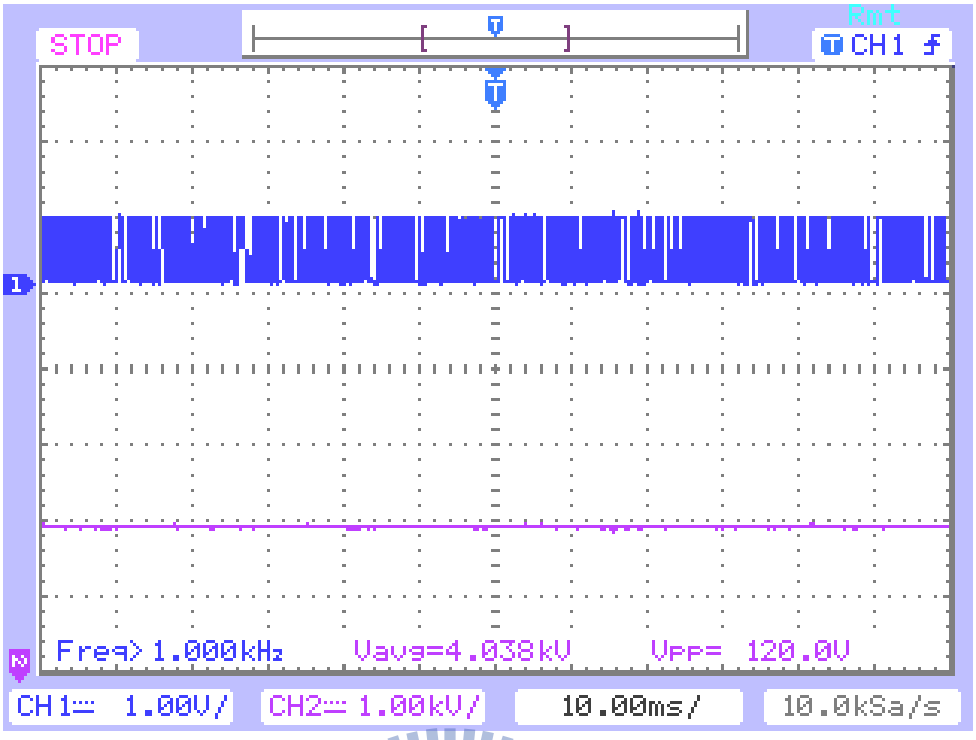
Figure4.2 The flyback converter

Figure4.3　Cement resistor loads



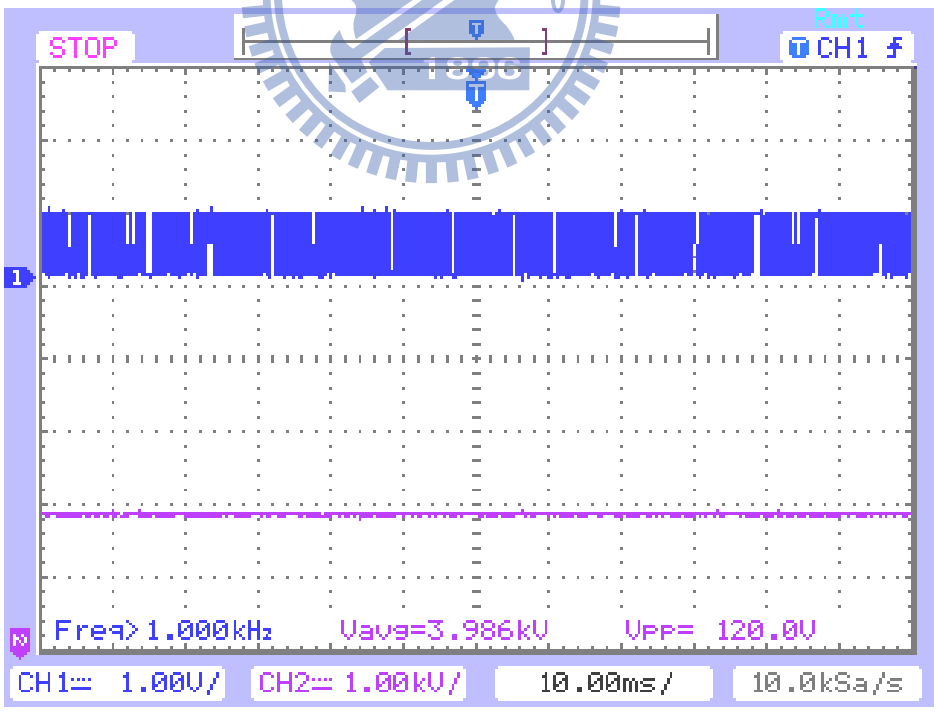
V_{GS}: signal1　　V_{output}: signal2　　V_{avg}=81.52V, V_{pp}=0.08V

Figure4.4　Output ripple 0.08V at no loading situation



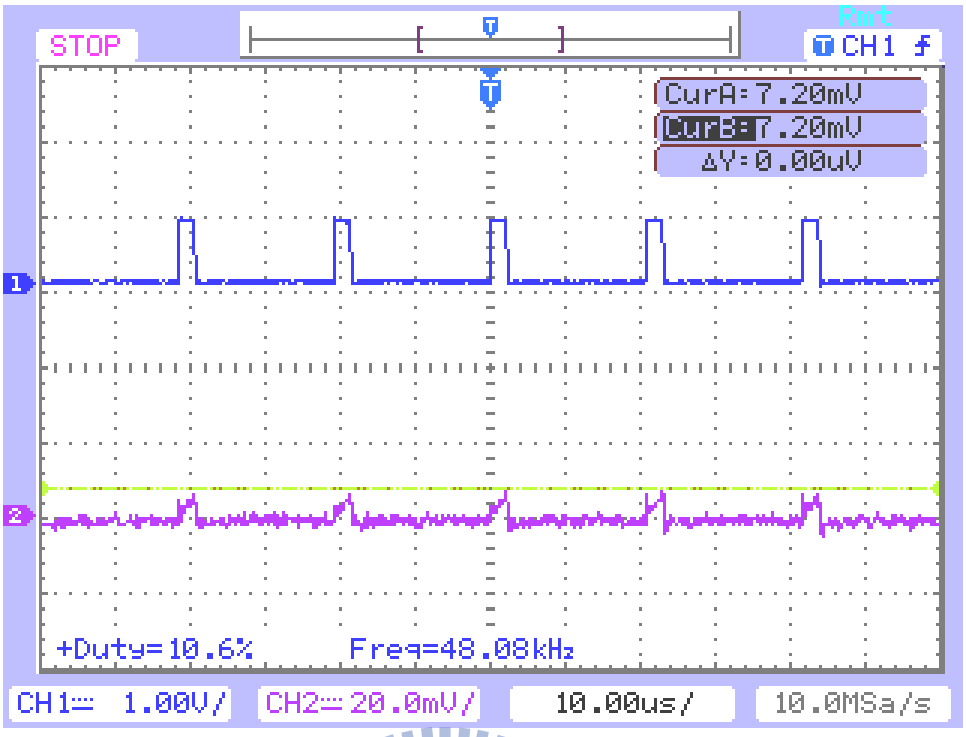
V_{GS}: signal1 V_{output}: signal2 V_{avg}=80.76V, V_{pp}=0.12V

Figure4.5 Output ripple 0.12V at 32W loading situation



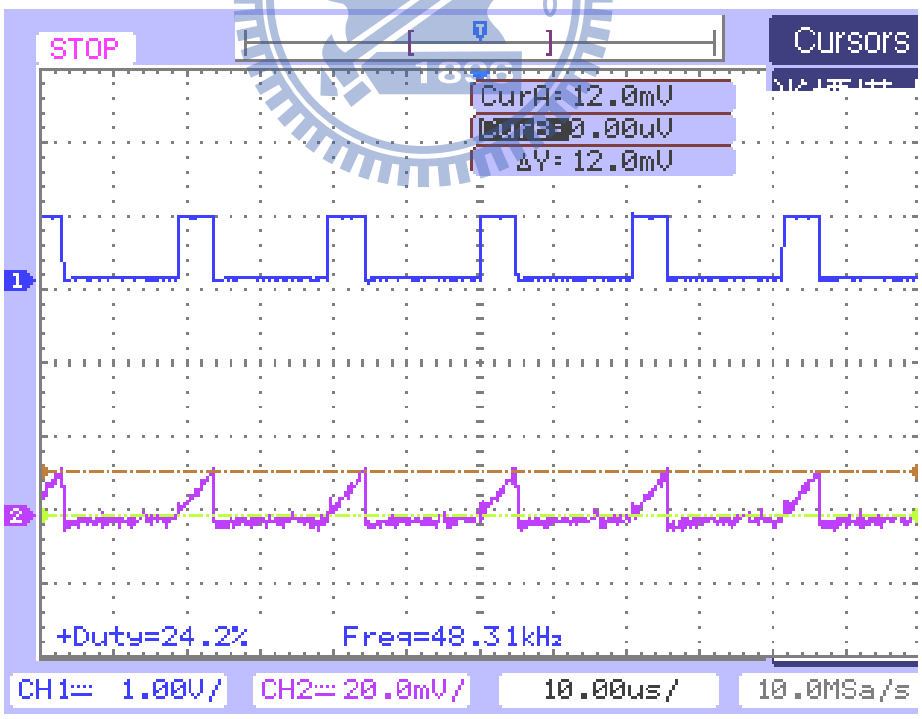
V_{GS}: signal1 V_{output}: signal2 V_{avg}=79.72V, V_{pp}=0.12V

Figure4.6 Output ripple 0.12V at 100W situation



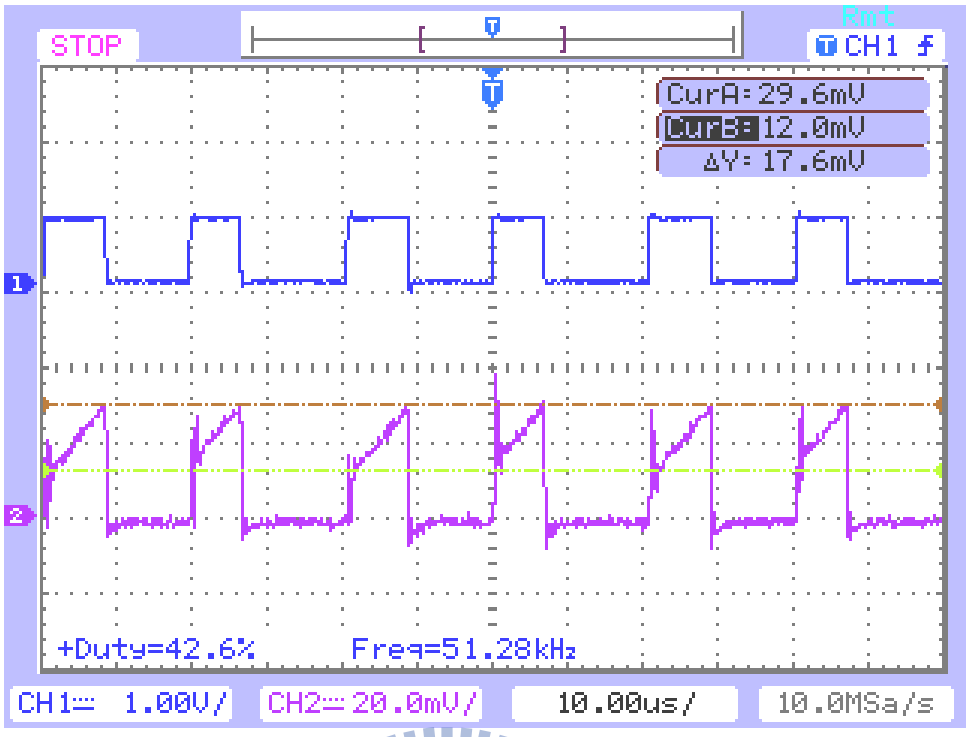
V_{GS}: signal1 V_S: signal2 $I_{sen,min}$=0A, $I_{sen,max}$=0.864A

Figure4.7 The V_{GS} and V_S signal at no loading situation



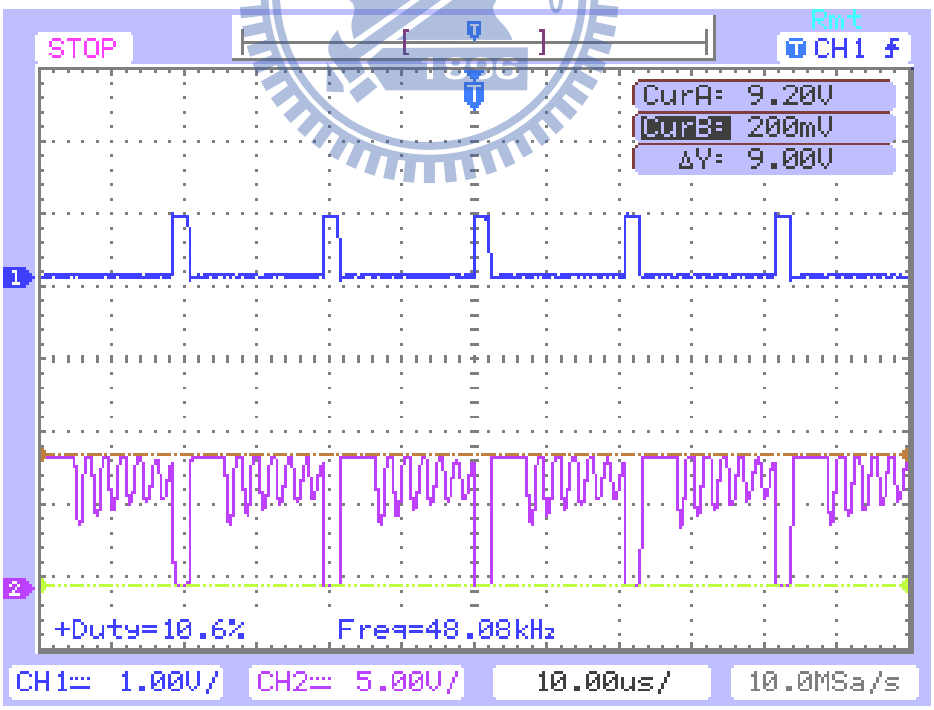
V_{GS}: signal1 V_S: signal2 $I_{sen,min}$=0A, $I_{sen,max}$=1.44A

Figure4.8 The V_{GS} and V_S signal at 32W loading situation



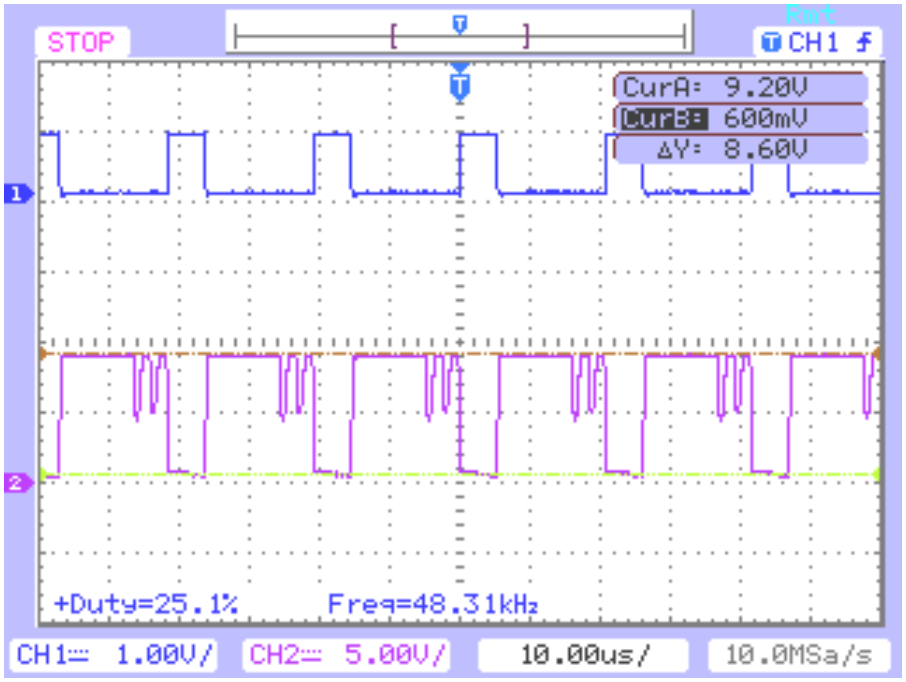
V_{GS}: signal1 V_S: signal2 $I_{sen,min}$=1.44A, $I_{sen,max}$=3.552A

Figure4.9 The V_{GS} and V_S signal at 100W loading situation



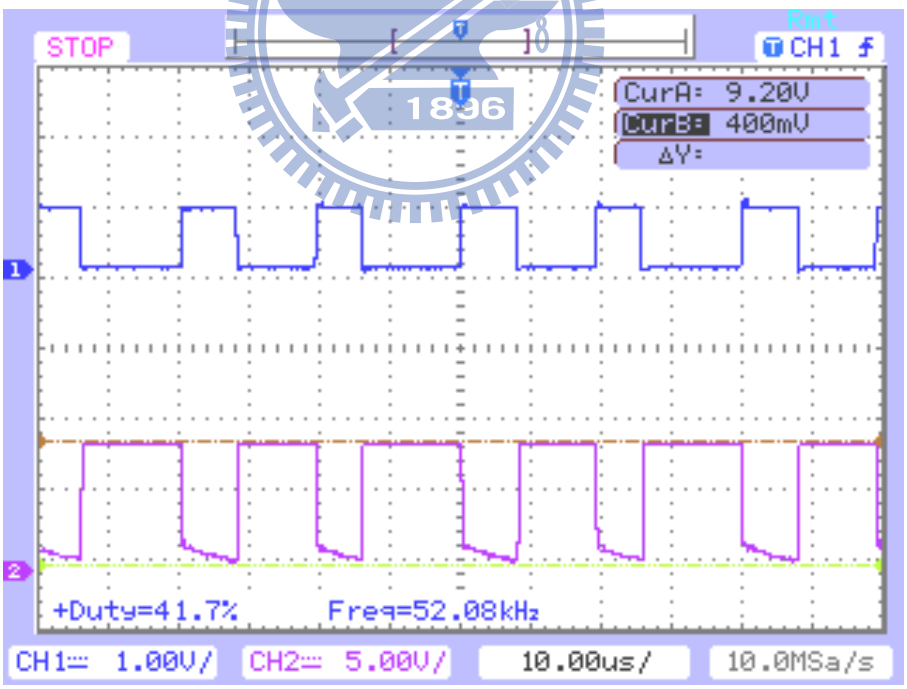
V_{GS}: signal1 V_{DS}: signal2 $V_{DS,min}$=4V, $V_{DS,max}$=184V

Figure4.10 The V_{GS} and V_{DS} signal at no loading situation



V_{GS}: signal1 V_{DS}: signal2 $V_{DS,min}$=12V, $V_{DS,max}$=184V

Figure4.11 The V_{GS} and V_{DS} signal at 32W loading situation



V_{GS}: signal1 V_{DS}: signal2 $V_{DS,min}$=8V, $V_{DS,max}$=184V

Figure4.12 The V_{GS} and V_{DS} signal at 100W loading situation

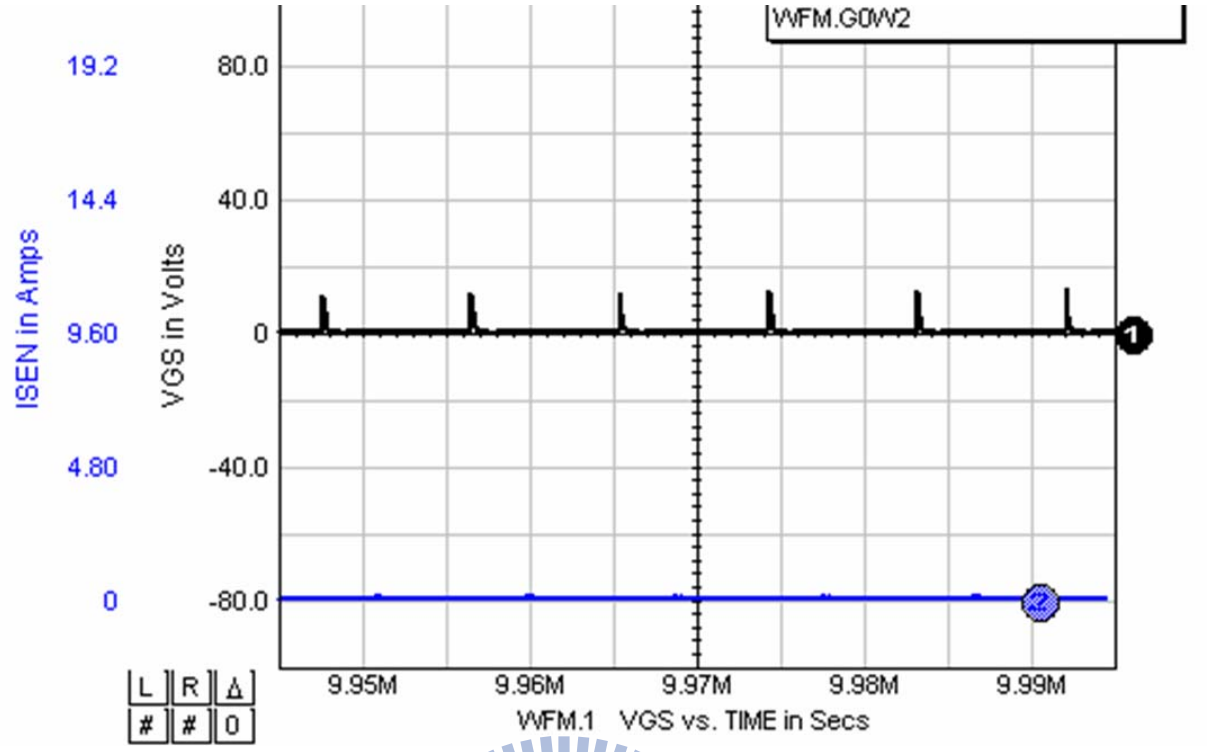


Figure4.13 V_{GS} and sensing current at no load

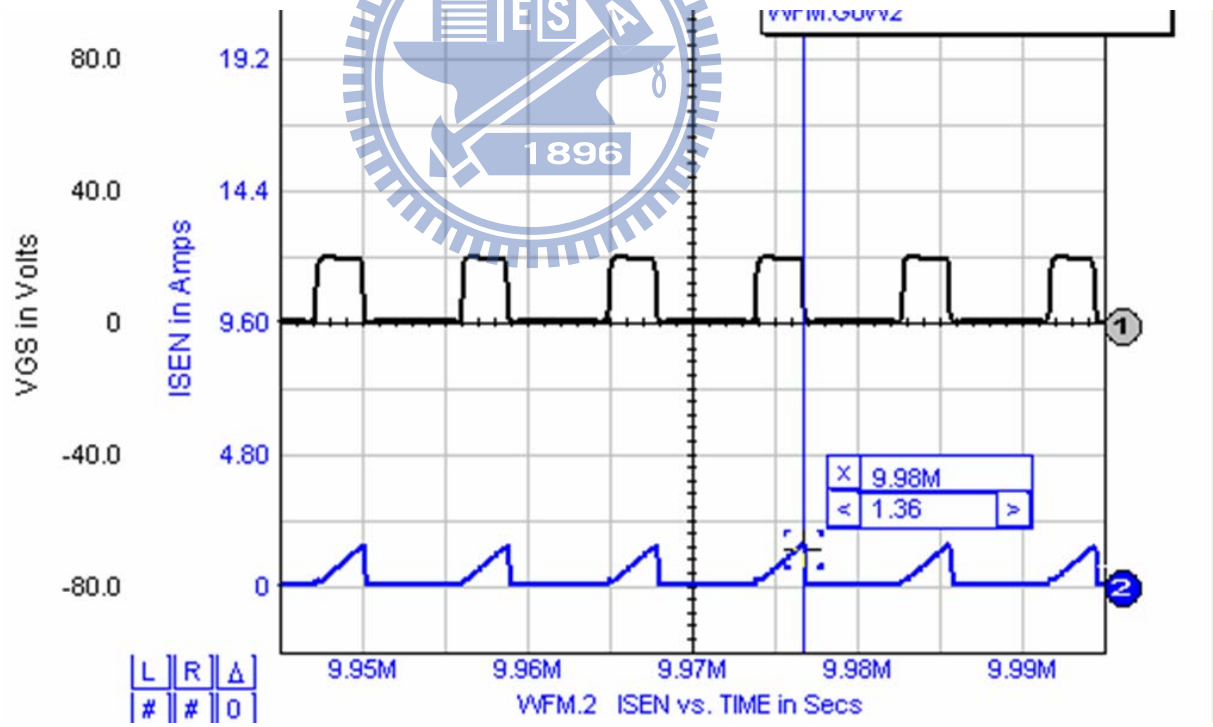


Figure4.14 V_{GS} and sensing current at 32W load

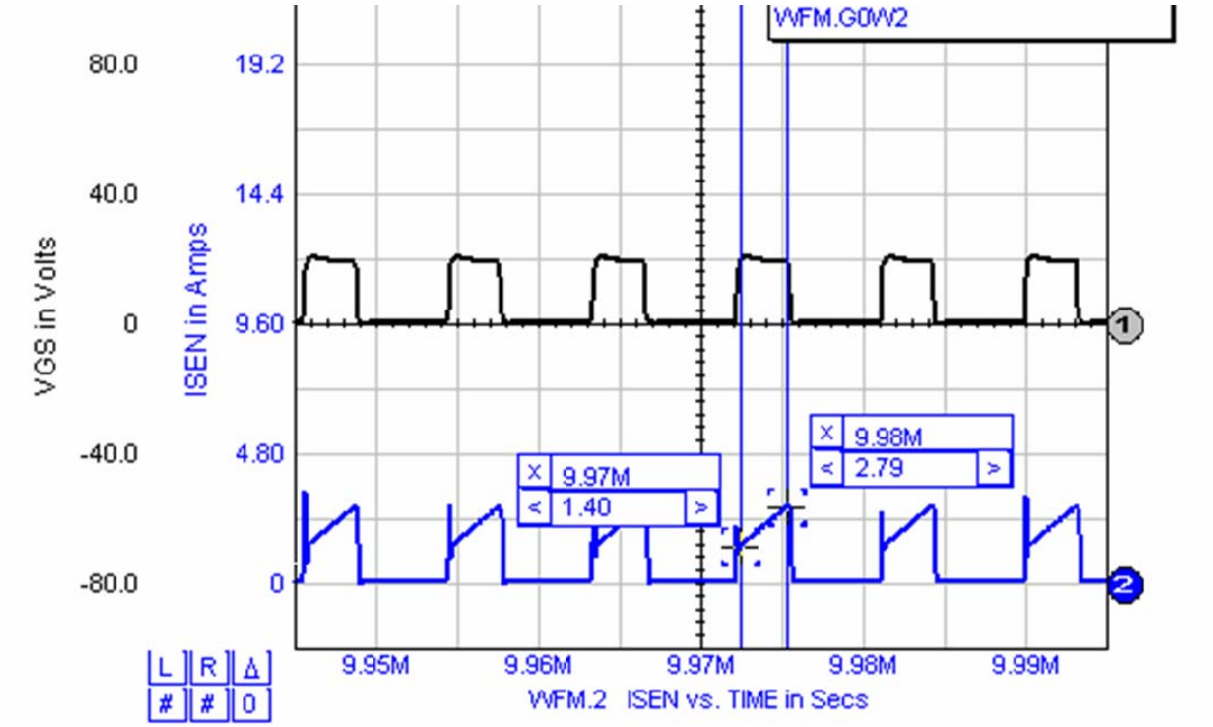


Figure4.15 V_{GS} and sensing current at 100W load

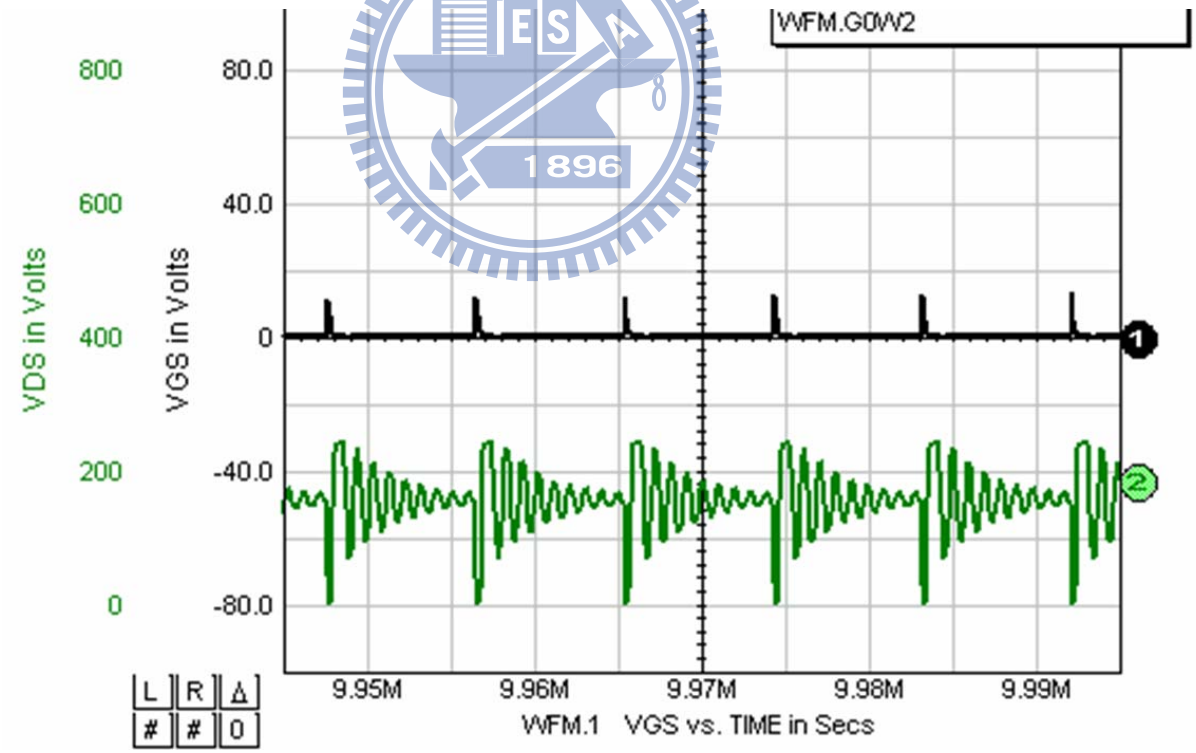


Figure4.16 V_{GS} and V_{DS} at no load

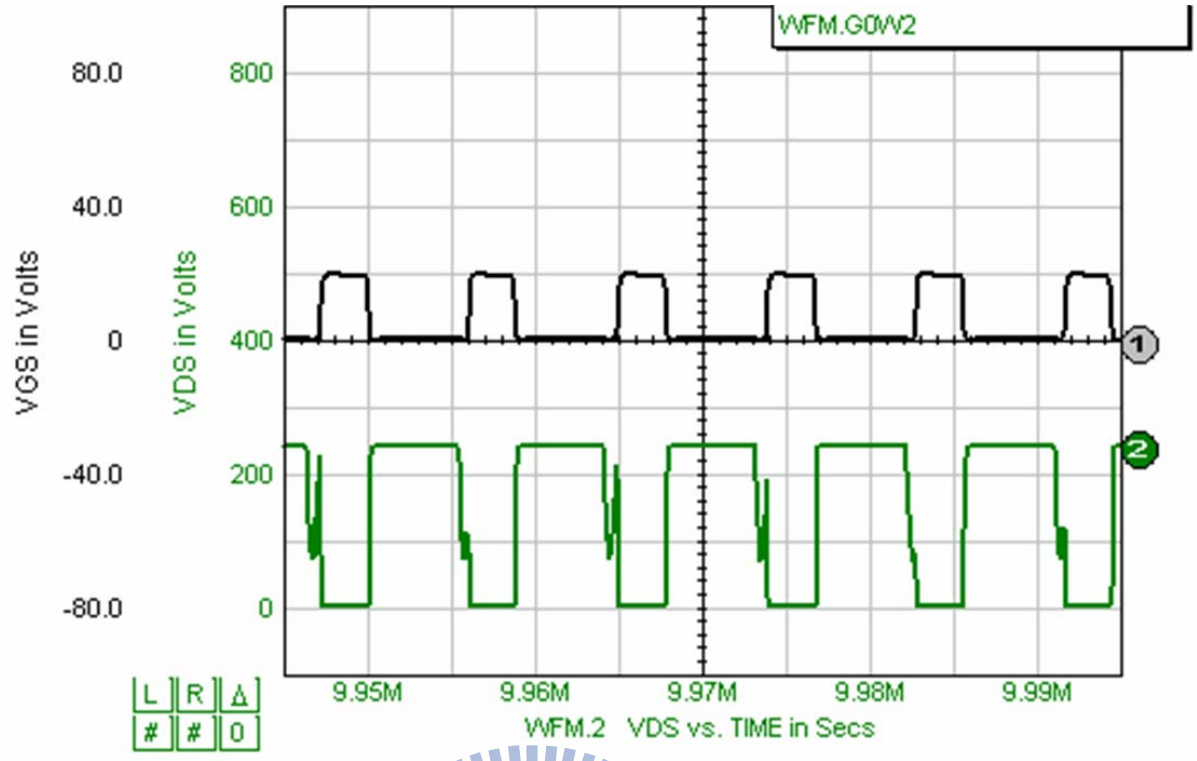


Figure4.17 V_{GS} and V_{DS} at 32W load

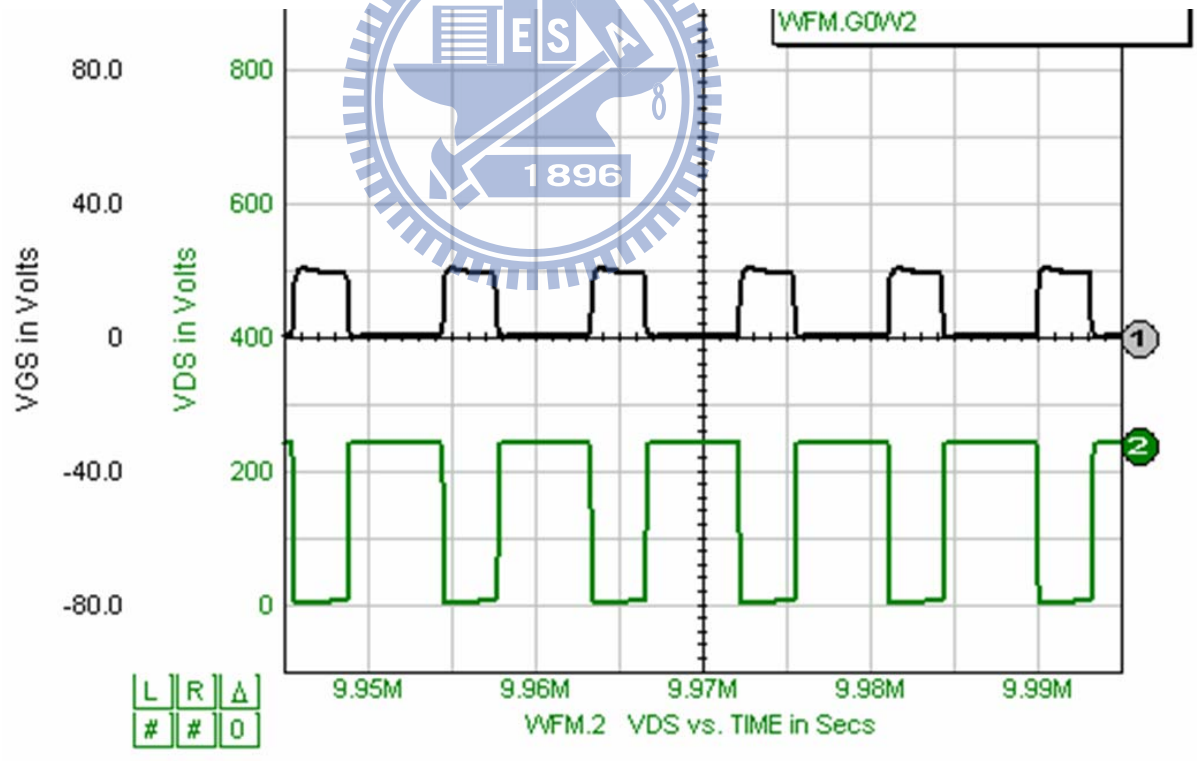


Figure4.18 V_{GS} and V_{DS} at 100W load

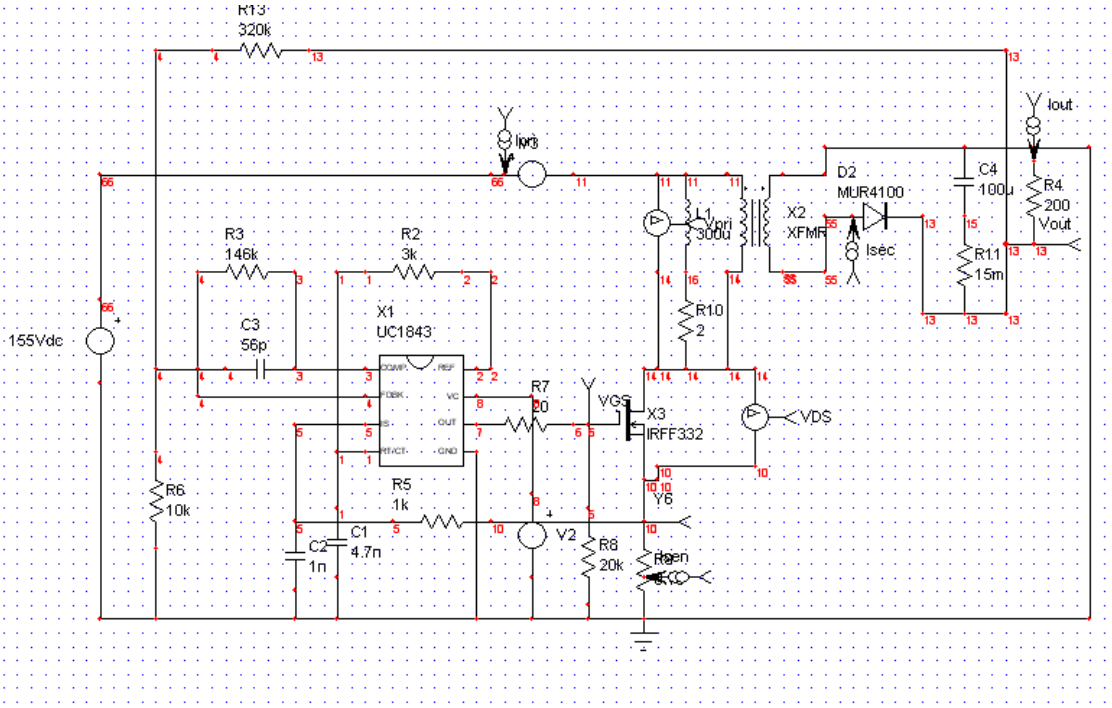


Figure4.19 Spice simulation model of the flyback converter

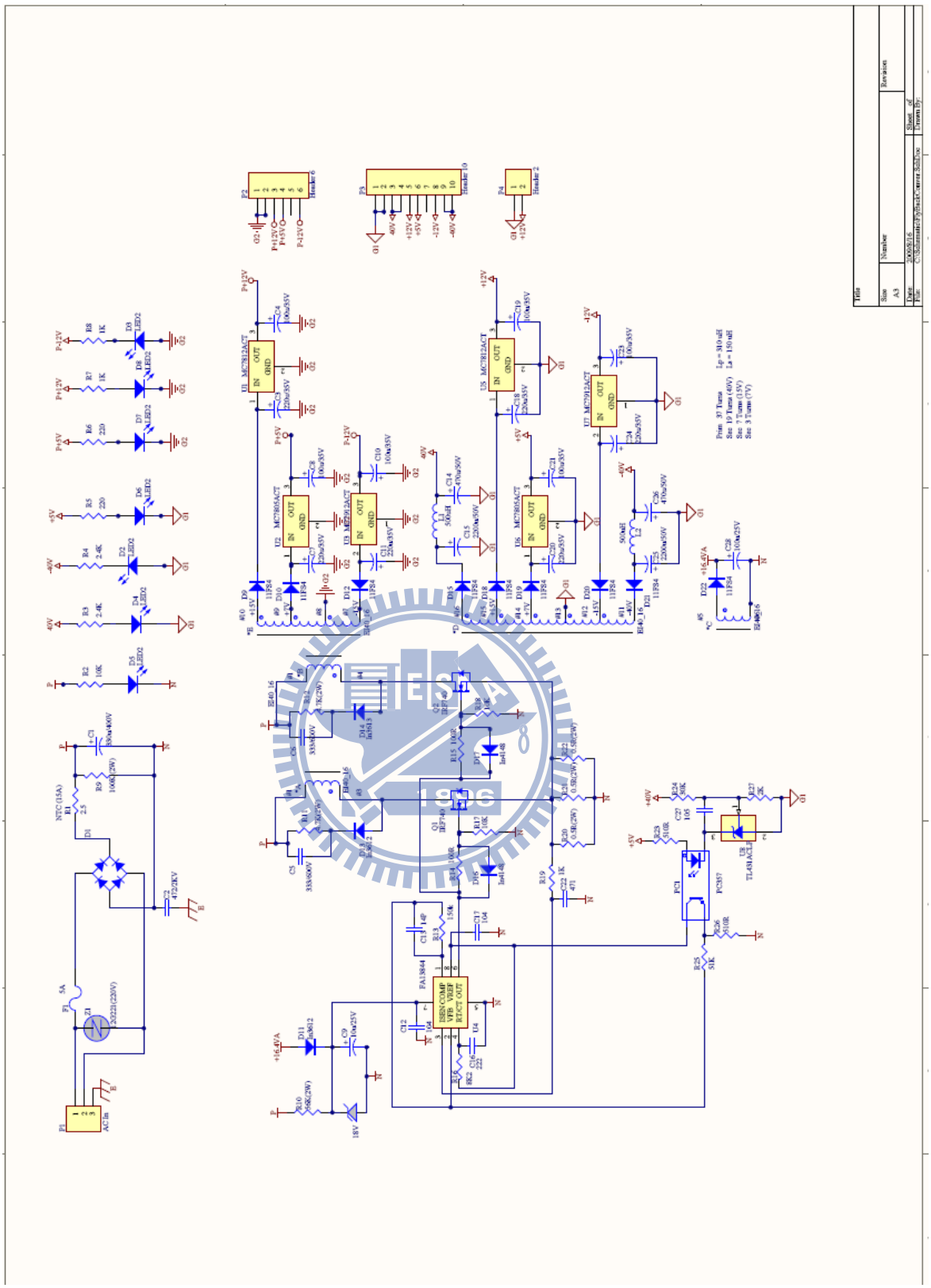


Figure4.20　The flyback implementation circuit schematic

Tables

Isolation Amplifier (IC:HCPL7820)	Input voltage Swing	±200mV
	Gain	8
	Bandwidth	200kHz
Difference Amplifier (IC:LM3875)	Maximum Supply Voltage	±84V
	Output Dissipation	50W
	Maximum Output Current	6A
	Gain-Bandwidth Product	8MHz
	Open-Loop Gain	120dB
	Slew rate	11V/μs
Op-Amp (IC:LM6361)	Maximum Supply Voltage	±15V
	Gain-Bandwidth Product	40MHz

Table2.1 The amplifiers' specifications

Description of parameter	Parameter	Value of parameter
DC gain of OpAmp1	A_{op1}	4
Cut-off frequency of OpAmp1	ω_{cop1}	20000000 π
DC gain of OpAmp2	A_{op2}	5.5
Cut-off frequency of OpAmp2	ω_{cop2}	14540000 π
DC gain of difference amplifier	A_D	15
Cut-off frequency of difference amplifier	ω_{cs}	1066000 π
DC gain of isolation amplifier	A_I	8
Cut-off frequency of isolation amplifier	ω_{ci}	400000 π
Output voltage sampling resistor ratio	$\mathbf{K}(0)$	0.000595

Table2.2 Values of the parameters of the mathematical model