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Active ESD protection circuit design against charged-device-model ESD event in CMOS integrated circuits

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Abstract

CDM ESD event has become the main ESD reliability concern for integrated-circuits products using nanoscale CMOS technology. A novel CDM ESD protection design, using self-biased current trigger (SBCT) and source pumping, has been proposed and successfully verified in 0.13-μm CMOS technology to achieve 1-kV CDM ESD robustness.

1. Introduction

On-chip electrostatic discharge (ESD) protection has become a challenge for CMOS ultra-large-scale integrated (ULSI) circuits implemented in nanoscale CMOS technology [1,2]. The very thin gate oxide is the main issue for ESD protection, especially for charged-device-model (CDM) ESD event [3–5]. CDM ESD event is caused by a charged device discharging to a grounded surface through a device pin. The CDM ESD event generates a peak current in the order of 5–10 A (the peak value of a CDM ESD current strongly depends on the parasitic capacitance of the charged device), a rise time of about 200–400 ps, and a duration of about 1 ns [6]. Due to the very high speed and huge amplitude of the CDM ESD current, the human-body model (HBM) and machine model (MM) ESD protection designs can not offer CDM ESD protection for the thin gate oxide of input stage in nanoscale CMOS technology. Generally, an additional ESD clamp device, such as a gate-grounded NMOS (GGNMOS), is added nearby the internal input stage to locally limit the overvoltage across the gate oxide of the input stage during CDM ESD stresses, as shown in Fig. 1. However, such CDM ESD protection design with GGNMOS can not provide efficient protection in nanoscale CMOS IC products, because the CDM ESD clamp realized with GGNMOS is triggered by drain-to-bulk junction breakdown during negative CDM ESD stress. The high trigger voltage and low turn-on efficiency of GGNMOS can not effectively protect the input stage with a thin gate oxide in nanoscale CMOS technologies.

In this work, a new CDM ESD protection design is proposed and verified in a 0.13-μm 1.2-V CMOS technology with a gate oxide thickness of 2.8 nm. The proposed CDM ESD protection design has an active trigger mechanism, self-biased current trigger (SBCT) mechanism, to reduce the trigger voltage to efficiently clamp the ESD voltage across the gate oxide of input stages. In addition, the source pumping design further reduces the ESD voltage across the gate oxide to enhance CDM ESD robustness of the input stage in nanoscale CMOS technology. The CDM ESD robustness of input stages with the new proposed CDM ESD protection design can be over 1000 V under positive/negative CDM ESD stresses.

2. Realization of the novel CDM ESD protection design

The new proposed CDM ESD protection design, consists of a NMOS transistor (Mn3) with self-biased current

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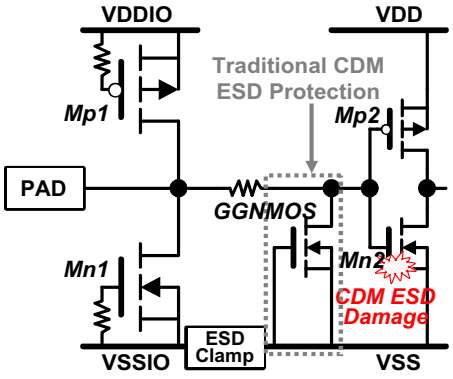

Fig. 1. Traditional CDM ESD protection with gate-grounded NMOS (GGNMOS) added to the gate of input stages.

trigger mechanism and a diffusion resistor of source pumping design, (Fig. 2). The gate terminal of the NMOS transistor (Mn3), which is neighbored with the input stage, is connected to the VSSIO line, not VSS line. To turn on NMOS transistor (Mn3), its gate terminal can be biased by the CDM ESD current discharging through the ESD clamp between VSSIO and VSS lines under CDM ESD stresses. The similar scheme had been proposed to solve ESD damages in mixed-power domains applications under HBM and MM ESD stresses [7]. Its drain terminal is connected to the input signal line and through an input series resistance to the input pad. Its source terminal is connected to the VSS line through an N+ diffusion resistance ($R1$). In addition, the source terminal of the NMOS transistor (Mn2) in the input stage is also connected to the VSS line through the same N+ diffusion resistance ($R1$). The gate oxide of NMOS transistor (Mn2) in the input stage can be clamped by NMOS transistor (Mn3) with self-biased current trigger mechanism and the pumping resistance ($R1$) under CDM ESD stresses.

2.1. Design with self-biased current trigger (SBCT) mechanism

The NMOS transistor (Mn3), to implement self-biased current trigger mechanism, is different from the traditional CDM ESD protection (with GGNMOS) in the gate connection to VSSIO line, instead of VSS line. During normal circuit operation, the NMOS transistor (Mn3) is kept off state by the gate terminal biased at 0 V. Under positive CDM ESD stresses, the device is initially charged at positive voltage through the VSS and VSSIO pins. The CDM ESD currents are mainly discharged by the drain-to-bulk diode of the GGNMOS transistor (Mn1) and the NMOS transistor (Mn3) which are forward-biased when the input pad is grounded by the probe pin of the CDM ESD test head. In addition, the overvoltage can also be clamped by the forward-biased drain-to-bulk diode of the NMOS transistor (Mn3). Because forward-biased diodes have a low turned-on voltage and high conduction efficiency, the CDM ESD currents can be rapidly and efficiently discharged in positive CDM ESD stresses (even, in the traditional CDM ESD protection design with GGNMOS). Generally, the positive CDM ESD robustness of the input stage is much higher than its negative CDM ESD robustness. Therefore, the CDM ESD robustness of the input stage is defined by negative CDM ESD stresses.

During negative CDM ESD test, the device is initially charged at a negative voltage through the VSS and VSSIO pins. The substrate of the device stores a large quantity of negative charges. When the input pad is suddenly grounded, charges are discharged from the substrate to the grounded input pad through several paths, such as path 1 and path 2 shown in Fig. 3. The high voltage between the grounded input pad and the substrate (negatively biased) causes the drain-to-bulk junction breakdown of GGNMOS transistor (Mn1) and consequently the discharge of the ESD current through the turned-on parasitic npn bipolar transistor (Q1) of the GGNMOS transistor (Mn1), (path 1 shown in Fig. 3). The current is discharged through the GGNMOS transistor (Mn1) between the grounded input pad and the VSSIO line, ESD clamp between VSSIO line and VSS line, the VSS line, and the internal P+ pickup of the p-substrate, (path 2 shown in Fig. 3). The voltage drops between VSSIO line and VSS line can be generated

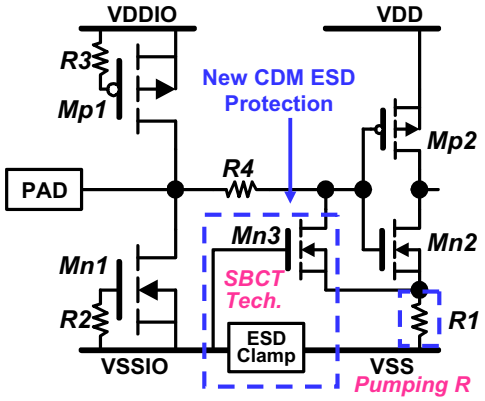

Fig. 2. CDM ESD protection with the proposed self-biased current trigger mechanism and source pumping design.

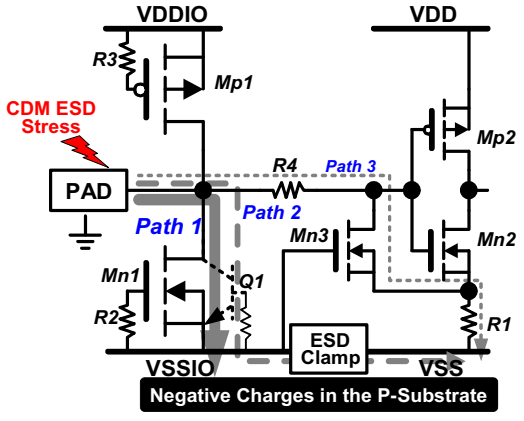

Fig. 3. CDM ESD current discharging paths in the CDM ESD protection with self-biased current trigger mechanism and source pumping design under negative CDM ESD stresses.

by discharging CDM ESD current in path 2. The NMOS transistor (Mn3) can be turned on by ESD current discharging through the ESD clamp between VSSIO and VSS lines to generate a gate-to-source voltage (Vgs) of NMOS transistor (Mn3). The overvoltage across the gate oxide of NMOS transistor (Mn2) of the input stage is then efficiently clamped by the turned-on NMOS transistor (Mn3). Without requiring to reach junction breakdown, NMOS transistor (Mn3) with this self-biasing current trigger mechanism can be efficiently triggered on and it clamps the overvoltage across the gate oxide of the input stage to improve the negative CDM ESD robustness of input stages in nanoscale CMOS process.

2.2. Design with source pumping

According to previous studies [2], gate oxide breakdown voltages of gate-to-source terminals and gate-to-bulk terminals are quite different in NMOS transistor. The gate oxide breakdown voltage of gate-to-source terminal is remarkably lower than that of gate-to-bulk terminal. To improve the ESD robustness of the input stage with thin gate oxide in nanoscale CMOS process and extend the design window of ESD protection circuits, the source pumping design had been used to reduce the ESD voltage across the gate-to-source terminal in the NMOS transistor of input stage under HBM ESD stresses [2]. In this work, a similar source pumping design is used to reduce the ESD voltage across the gate-to-source terminals in the NMOS transistor of input stage under CDM ESD stresses. The source terminal of NMOS transistor (Mn2) in the input stage and the internal P+ pickup are connected by the additional N+ diffusion, as a pumping resistor. Under negative and positive CDM ESD stresses, part of the CDM ESD currents is discharged through the pumping resistor between NMOS transistor (Mn2) source terminal and VSS line by the turned-on NMOS transistor (Mn3) or parasitic drain-to-bulk diode of NMOS transistor (Mn3), respectively, (path 3 shown in Fig. 3). Part of the CDM ESD current is discharged by path 3 to raise the potential of the source terminal of NMOS transistor (Mn2), and also reduce the ESD voltage across the gate-to-source terminal of NMOS transistor (Mn2) in the input stage.

To investigate the new CDM ESD protection designed with self-biased current trigger mechanism and source pumping, a testchip has been implemented with NMOS transistors (Mn3) of 0.18-μm channel length and two different channel widths, 20 μm and 60 μm, a 15 Ω pumping resistance and 200 Ω input series resistance in a 0.13-μm 1.2-V CMOS process. In addition, the CDM ESD protection design with forward-biased 3-stacked diode strings is also implemented to compare with the new proposed CDM ESD protection design, as shown in Fig. 4. The occupied silicon area of the CDM ESD protection designs with forward-biased 3-stacked diode strings has been designed similar to the new proposed CDM ESD protection design. The diode perimeters of the CDM ESD protection design with forward-biased 3-stacked diode strings are varied in 18 μm and 38 μm to compare with the new proposed CDM ESD protection design of NMOS transistor (Mn3) with channel widths of 20 μm and 60 μm, respectively.

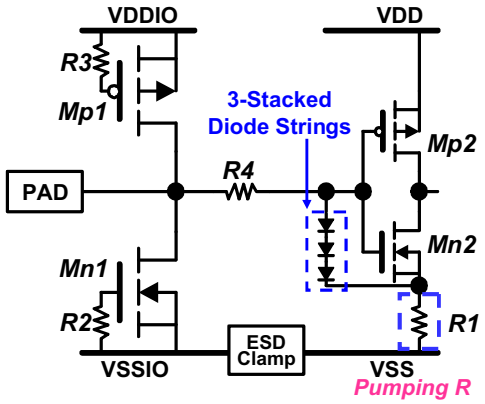

Fig. 4. CDM ESD protection with 3-stacked diode strings.

3. Experimental results and discussions

The testchips have been assembled in a DIP-40-pin package. The CDM ESD stresses are applied with socketed-mode tester (*ZapMaster* ESD simulator). The CDM ESD robustness of the traditional ESD protection design with GGNMOS, such as shown in Fig. 1, is listed in Table 1. The ESD levels of input stages with traditional ESD protection design are obviously below 500 V under negative stresses. Table 2 shows the robustness of the new proposed protection designed with different channel widths for the NMOS transistor (Mn3). The robustness of NMOS transistor (Mn3) with 60-μm channel width is significantly higher than that with 20-μm channel width. All input stages with the new protection design can achieve over 1000-V CDM ESD robustness under positive and negative stresses. Table 3 shows the ESD robustness of protection design with forward-biased 3-stacked diode strings.

According to the whole measured results, the robustness of input stage with the forward-biased 3-stacked diode strings is much lower than that with the new proposed protection design. In the protection design with self-biased current trigger mechanism, the currents are initially and mainly discharged by paths 1 and 2 under negative stresses. With selfbiased current trigger mechanism, the negative CDM ESD current is discharged through path 1, path 2, and path 3 in sequence. However, the turned-on voltage

Table 1
CDM ESD robustness of the traditional protection design with GGNMOS

W/*L* of GGNMOS (μm)	CDM (+) (V)	CDM (−) (V)
20/0.18	450	300
60/0.18	950	350

Table 2
CDM ESD robustness of the protection design with selfbised current trigger mechanism and source pumping

W/L of Mn3 (μm)	CDM (+) (V)	CDM (−) (V)
20/0.18	1350	1150
60/0.18	1600	1450

Table 3
CDM ESD robustness of the protection design with forward-biased 3-stacked diode strings

Perimeters of the diodes (μm)	CDM (+) (V)	CDM (−) (V)
18	1100	600
38	1250	900

of the forward-biased 3-stacked diode strings is lower than the junction breakdown voltage of the drain-to-bulk junction in GGNMOS (Mn1). The CDM ESD currents can be initially discharged by the forward-biased 3-stacked diode strings between the VSS lines and input pad through the input series resistance and pumping resistance ($R1$) under negative stresses. The smaller silicon areas of the diodes in the design with forward-biased 3-stacked diode strings can not sustain the huge CDM ESD current to cause the significant leakage current after negative CDM ESD stresses.

Besides, the input series resistance is added between input pad and input stage to efficiently limit the CDM ESD current through the discharging path 3. Fewer ESD current is discharged through path 3 in the proposed protection design under the negative stresses. The voltage drops along path 3 are shown in following equation:

$$V_{\text{pad}} = I_{\text{CDM,path3}} \times (R4 + R_{\text{on,Mn3}} + R1) \quad (1)$$

The input series resistances between input pad and input stage will remarkably affect the discharging distributions of CDM currents and the voltage drops along path 3. The robustness of the proposed protection design is significantly dropped to about 650 V if no input series resistance is used (they are below 200 V in diode-string designs). Without the input series resistance, path 3 will also provide a low impendence discharging path under the positive and negative stresses. The smaller silicon area of NMOS transistor (Mn3) can not sustain huge CDM current. The CDM currents mainly discharged through path 1 and path 2 if the input stage with a 200-Ω input series resistance. The V_{pad} would be dominated by the CDM currents discharging through path 1 and path 2 in parallel. The 200-Ω input series resistance is much higher than the turned-on resistance of Mn3 ($R_{\text{on,Mn3}}$) and the pumping resistance ($R1$). The voltage drops almost occur across the input series resistance ($R4$) in path 3. Therefore, the ESD voltage across the gate-to-source terminal of NMOS transistor (Mn2) in the input stage with a 200-Ω input series resistance is much lower than that without input series resistance.

4. Conclusion

A new CDM protection design with self-biased current trigger mechanism and source pumping design has been successfully verified in a 0.13-μm 1.2-V CMOS process. The CDM robustness of the input stages with the proposed CDM protection design can achieve over 1000 V under positive/negative stresses. Such self-biased current trigger mechanism can provide efficient CDM protection for input stages in general nanoscale CMOS process.

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