Chapter1

Introduction

1.1 Overview of Low temperature poly-silicon thin-film transistors (LTPS TFTs)

In recent years, low-temperature polycrystalline silicon(LTPS) thin film transistors(TFTs) have attracted much attention because they have very successfully applied in active matrix displays, such as active matrix liquid crystal displays(AMLCDs)[1~7] and active matrix organic light emitting displays(AMOLEDs)[8~14]. Besides large are display panels, poly-Si TFTs have been applied into some memory device such dynamics random access memories (DRAMs) [15], static random access memories(SRAMs) [16], and have great potential for 3-dimension IC applications [17~18].

Compared with conventional a-Si TFTs, the field effect mobility of poly-Si TFTs is much higher. Higher field effect mobility means transistors can provide higher driving current. The higher driving currents can allow pixel-switching element TFT's dimension shrinkage, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. Besides, the superior mobility performance allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry on the same glass substrate, which brings the era of system-on-glass (SOG) that will include a memory, central processing unit(CPU), and display on the same glass. In this way, the process complexity can be greatly simplified and manufacturing cost can be substantially reduced.

The ability of fabricating high-performance LTPS TFTs enables their use in a wide

range of new applications. Therefore, there is a great interest in improving the performance of LTPS TFTs.

In comparison with signal-crystalline silicon, poly-Si film contains many grain boundary defects and intra-grain defects. The order of poly-Si grain size is about 0.3um. At present, when poly-Si TFTs are used in LCD applications, the minimum channel length is typically much larger than 3μm, and therefore a large number of grain boundaries are present in the channel. Electrons are scattered at the grain boundaries or trapped by the interface states, leading to lower mobility than in single crystal silicon. Much effort has been made to increase the performance of LTPS TFTs [19~21]. Crystallization of a-Si thin films has been considered the most critical process for fabricating high-performance LTPS TFTs. Among various crystallization technologies, excimer laser crystallization has become the mainstream technology for mass production of flat panel displays (FPDs) because of high throughput, low temperature process compatible with glass substrate, and formation of high-quality poly-Si. In this way, the process complexity can be greatly simplified and manufacturing cost can be substantially reduced.

In summary, it is expected that the poly-Si TFTs will become increasingly important in future technology, especially when the 3-D circuit integration and SOG era is coming. There are lots of interesting and important topics that are worthy to be researched.

1.2 Motivation

Conventional driving method would result in a big kick-back voltage issue, which comes from the coupled capacitance between gate and drain electrodes. In storage-on-gate structure (Fig1-1) of active matrix, three-level-gate-driving method is often used to compensate coupling effect of pixel circuit. Fig1-2 shows the gate pulse of the n_{TH} scan line Vgate(n), the voltage on the pixel Vtotal(n), and its previous scan line pulse Vgate(n-1).

At T1, the $(n-1)_{TH}$ TFT starts to write in, resulting in the voltage Vtotal(n) up and down through Cs. The voltage on the pixel Vtotal(n) would then suffer the coupling effect and have the coupled voltage drop △V1. At T2 when TFT(n) opens and Vtotal(n) is charged to data signal. After charging, TFT(n) closes and Vtotal(n) drops △V2 because of the coupling effect. At T3 Vgate(n-1) rises, which pulls the voltage at the one side of the capacitor Cs and therefore the voltage Vtotal(n) is also lifted up. Finally, △Vtotal(n) would be set zero by Vgate(n) raise up which causes a voltage shift △V3 after T3. With deliberately designing the value Cs, Cgd and driving pattern Vgate(n), the coupling effect can be compensated.

In such driving method, switch TFT has actually went through three different gate voltage levels in different period (T1, T2, T3), in which only one voltage will turn on LTPS-TFT and the other two will just be set to eliminate the coupling effect. In the other words, the LTPS TFT in this pixel circuit is under dynamic gate pulse when three-level-gate-drive method works.

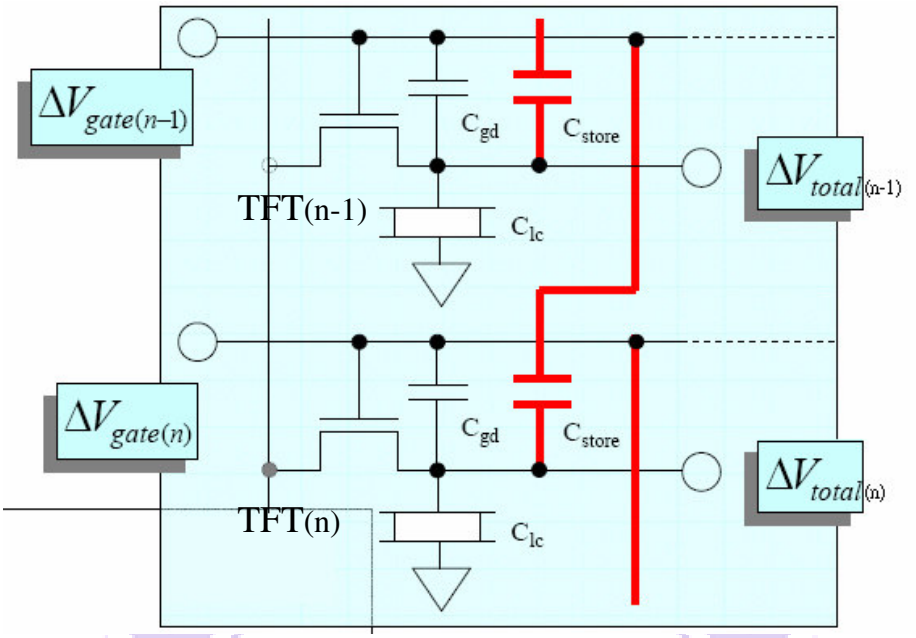

Fig1-1 Storage on gate pixel circuit

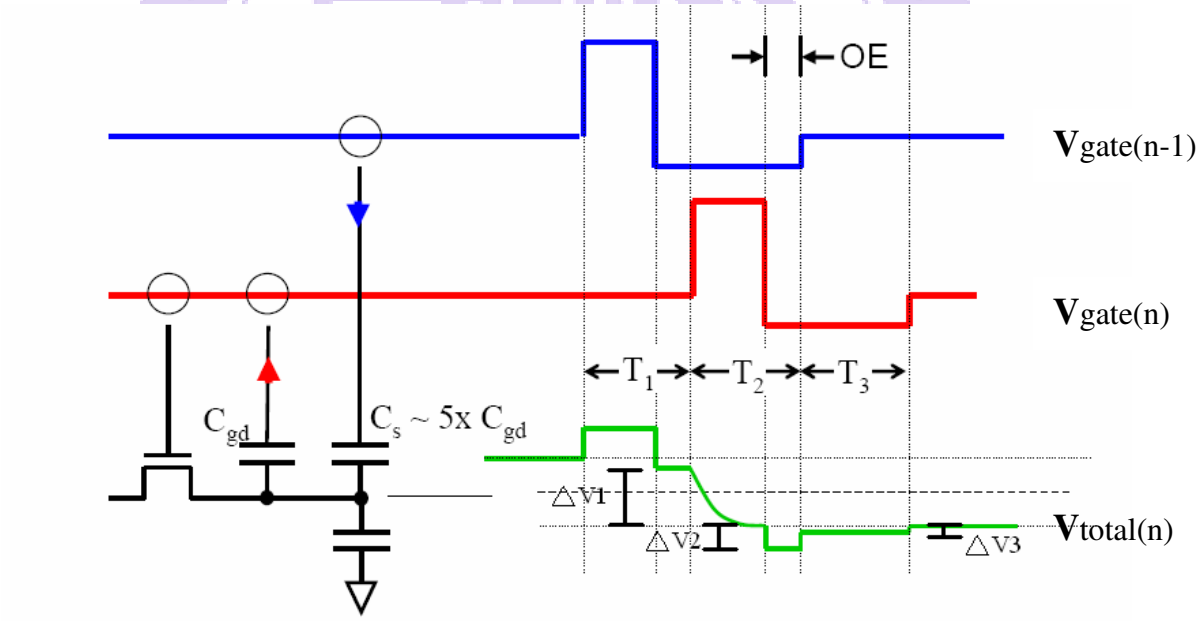

Fig1-2 Three Level Gate Drive Pulse

In active matrix display panels, LTPS TFTs are mainly used as switching elements. Fig.1-3. shows a conventional active matrix circuit. Each LTPS TFT connects to single data-line at the source electrode and single scan-line at the gate electrode for controlling the pixel. By scanning the gate bus-lines sequentially, and by

applying signal voltages to all source bus-lines in a specified sequence, we can address all pixels accordingly. In fact, for each TFT in the pixels, most of time it is not addressed, in the other words it is under off-state dynamic source pulse from data line while signals continue writing in.

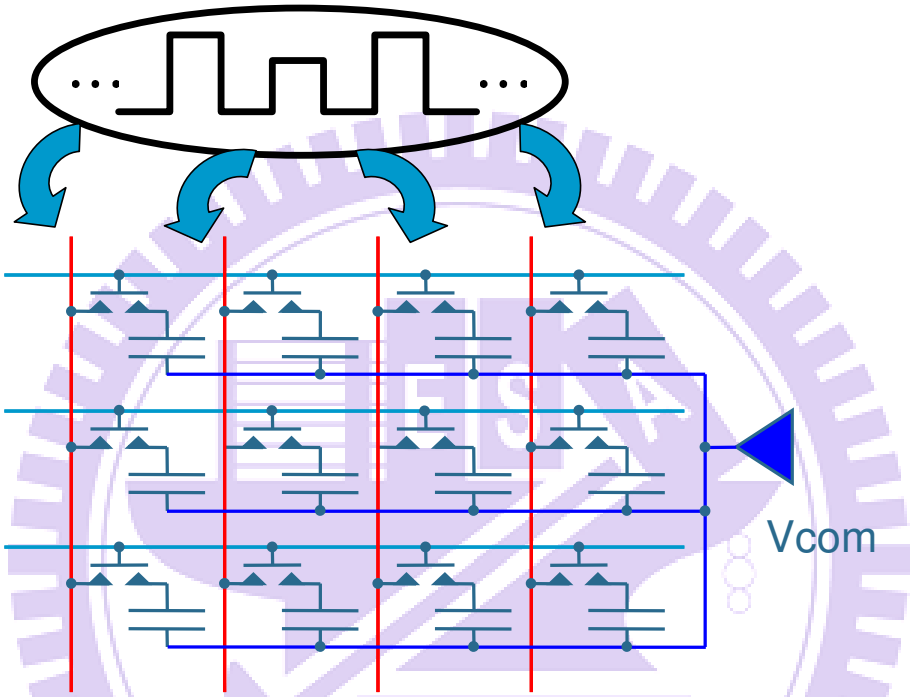

Fig.1-3 Active addressing of a 3x3 matrix

Therefore, it is important to know what happens in LTPS TFTs under dynamic operation, especially in off region under which the above two applications of LTPS TFTs are operated. The degradation mechanism for dynamic operation in the off region should be understood in detail.

In this work, we want to find out the degradation mechanism for dynamic operation in the off region in detail. We would mainly focus on the difference of mobility ratio and CV measurements of LTPS TFTs between initial value and after AC stress. Moreover, the equivalent circuit model for the device is proposed and the voltage drop on the elements in the circuit during stress would be discussed.

1.3 Review of Degradation Model for TFT under AC Stress

In previous reports, Uraoka *et al*. attributed the dominant AC degradation mechanism to hot electrons generated by trapped electrons exposed to the high electric field and gain energy from the electric field during AC stress. The mechanism was analyzed by using a pico-second emission microscope and device simulation to examine the transient current experimentally and theoretically.

The degradation model under AC stress observed by Uraoka is described as follow. When the gate voltage is high (ON state and Vg=15V), the electrons gather to form a channel, as shown in Fig. 1-4 (a). When the gate voltage drops (ON→OFF and Vg=15V→-15V), the electrons in the channel move rapidly to the source and drain shown in Fig. 1-4 (b). Some of the trapped electrons are exposed to the high electric field and gain energy from the field. Hot electrons are generated at this moment and form electron traps shown in Fig. 1-4 (c), result in the increase of density of state (DOS) in tail edge of poly-Si.

As for the P-type TFTs, when the gate voltage is low (ON state and Vg=-15V), the holes gather to form a channel shown in Fig. 1-5 (c). When the voltage transition from low to high (ON→OFF and Vg=-15V→15V), the holes in the channel move rapidly to the source and drain shown in Fig. 1-5 (b). Carriers gain energy from this electric field and become hot carriers. Therefore, more hot electrons are generated which causes trap formation at the grain boundaries around the drain edge shown in Fig. 1-5 (a).

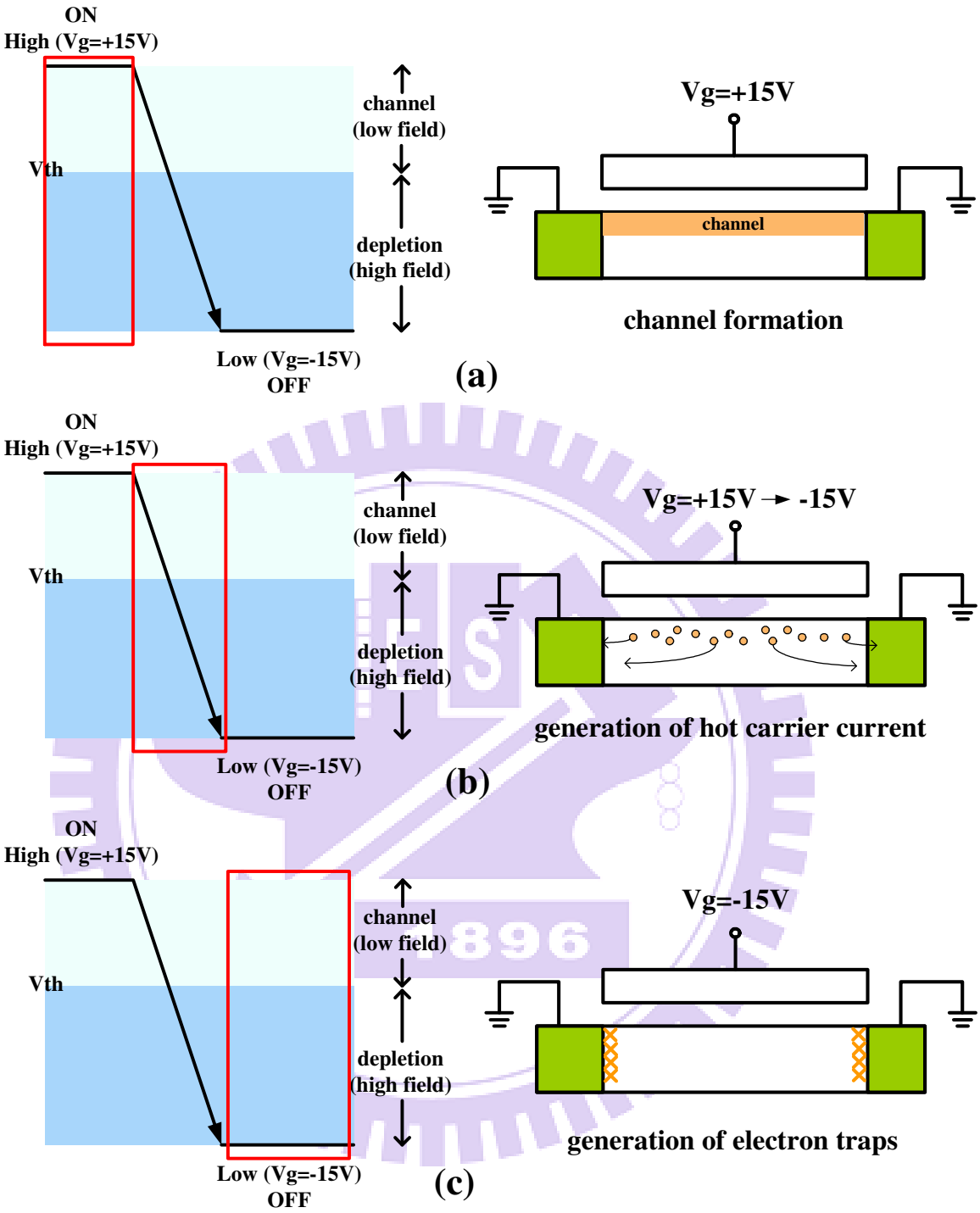

Fig. 1-4 A schematic diagram for degradation model of the N-type TFT

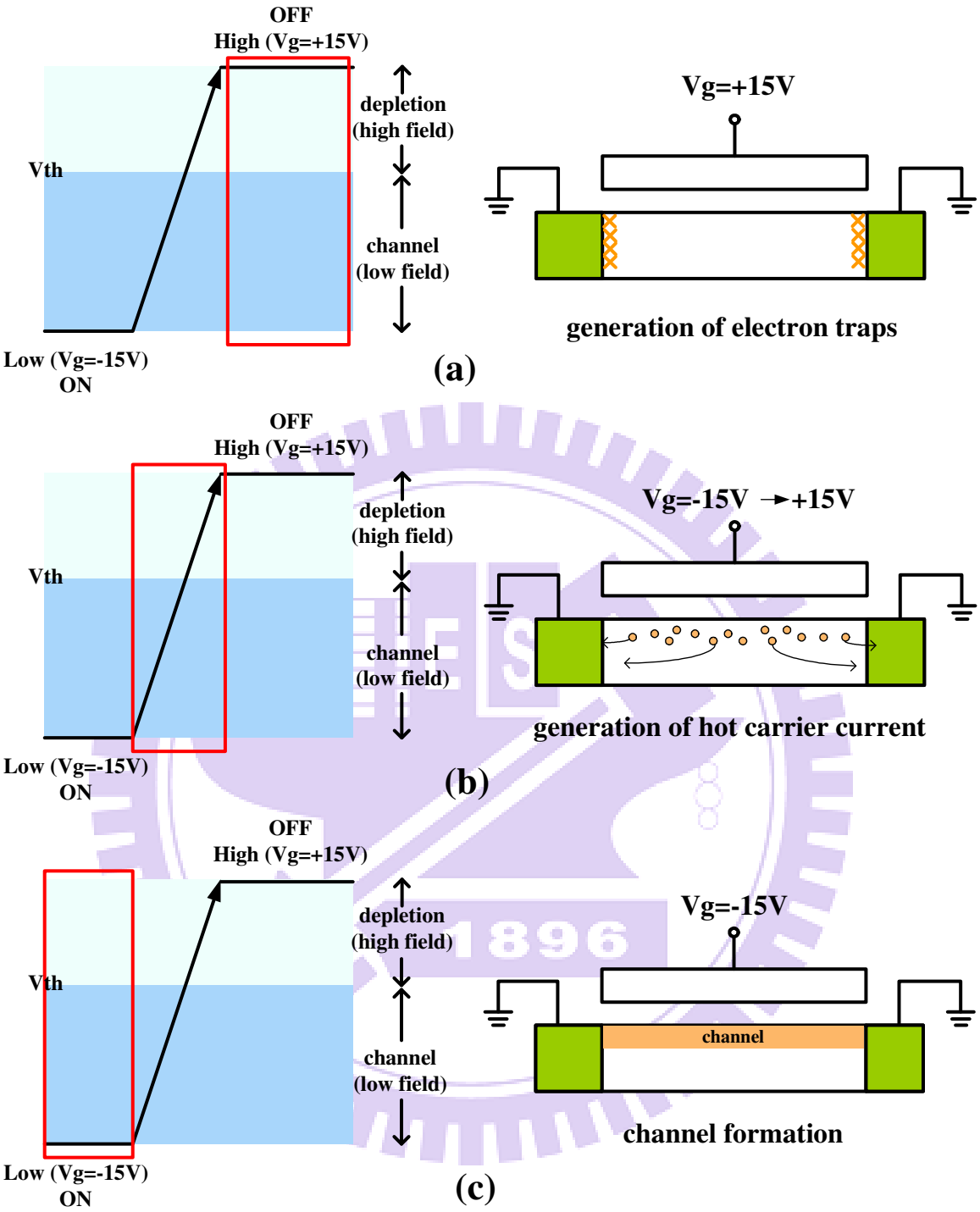

Fig. 1-5 A schematic diagram for degradation model of the P-type TFT

1.4 Thesis Organization

Chapter1 Introduction

1.1 Overview of LTPS

1.2 Motivation

1.3 Review of degradation model for TFT under AC Stress

1.4 Thesis structure

Chapter2 Experimental procedures

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2.2.2 AC stress conditions

2.2.3 CV measurement

2.3 Parameter extraction method

Chapter3 Poly-Si TFT under pulse stress in OFF Region

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3.1.1 Drain and Gate toggling effect in the OFF region

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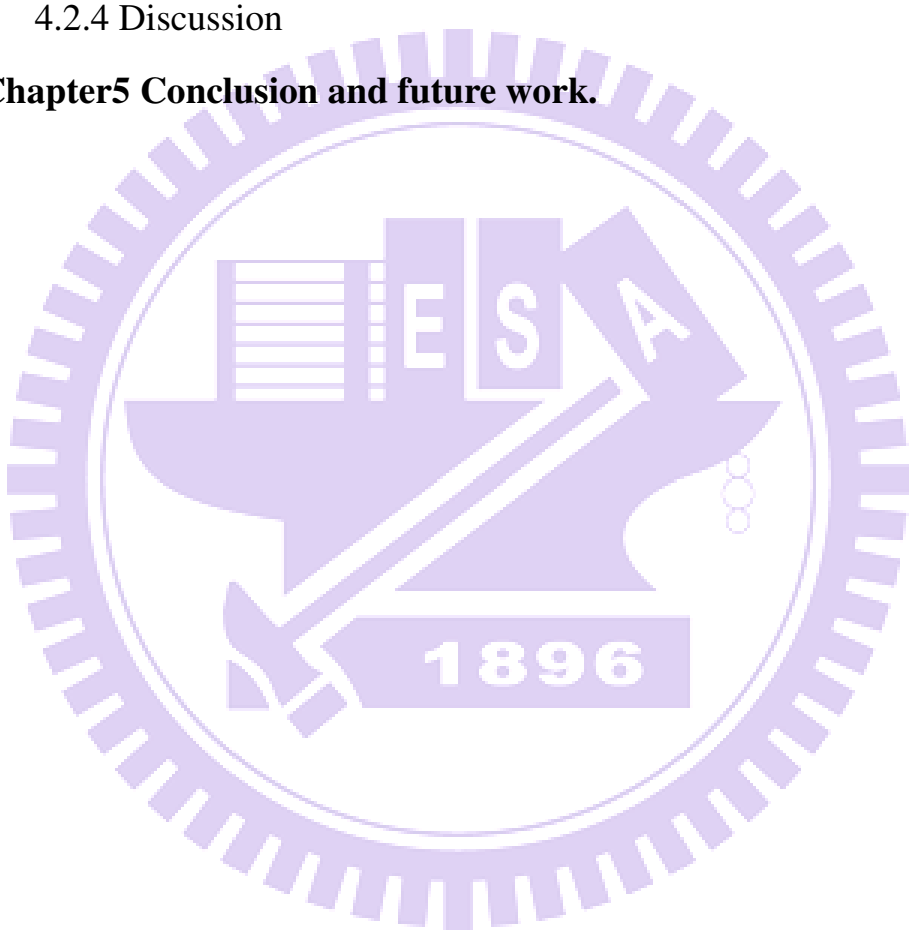


Chapter2

Experimental Procedures

2.1 Procedures of Fabrication of LTPS TFTs

LTPS TFTs used in the experiment were the conventional top-gate structure and fabricated on glass substrates. The cross-section views of N-channel and P-channel LTPS TFT are shown in Fig 2-1 and Fig. 2-2 respectively. The basic process flow is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates by the PECVD system. Then, XeCl excimer laser was used to crystallize a-Si:H film followed with poly-Si active area definition. Subsequently, gate insulator was deposited by PECVD. The thickness of gate oxide is 650Å. Next, the metal gate formation and source/drain doping were performed. Dopant activation and hydrogenation was carried out after interlayer dielectric deposition. Finally, contact holes formation and metallization were performed to complete fabrication work. The lightly doped drain (LDD) structure was used in the N-channel TFTs to enhance hot carrier endurance while not used in P-type devices. The width/length of the TFT was 20 μ m/5 μ m. The length of LDD is 1.5 μ m.

In order to ensure the identical performance under reliability test in following chapters, all the TFTs are fabricated from above process.

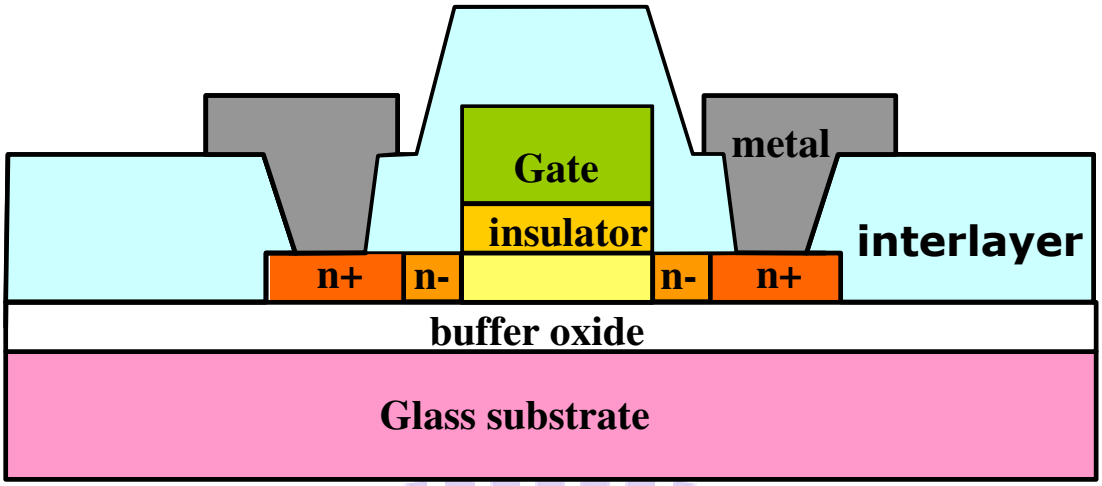


Fig. 2-1 The cross-section view of N-channel LTPS TFT with LDD structure

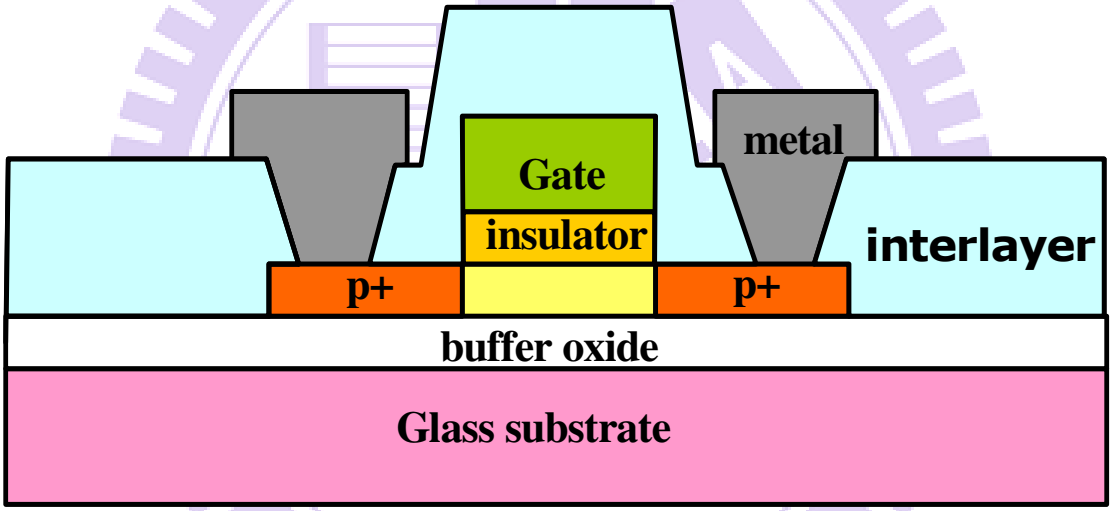


Fig. 2-2 The cross-section view of P-channel LTPS TFT

2.2 Experimental IV and CV

2.2.1 IV measurement

For knowing the electric characteristics, Keithley Model 4200-SCS Semiconductor Characterization System which embodies a dual channel pulse generator was used to measure I-V transfer curves and stress devices under various

AC/DC conditions. We used a fresh TFT sample for each stress condition to ensure the uniformity of initial characteristics and measured the transfer curves at drain-to-source voltage (Vds) of 0.1V and 5V to get the characteristics in linear region and saturation region. We can also notice that the larger Vds, 5V, is not as much as previous reports (10V). It is because we want to avoid Hot-carrier effect (especially in P-type TFT, the difference between each stress condition is not obvious compared with N-type TFT) when Vds is large enough to accelerate carriers in channel under On region.

2.2.2 AC Stress conditions

The basic parameters of AC signal consists of frequency (F), signal peak level (V_{PEAK}), signal base level (V_{BASE}), pulse width (W_P), pulse period (T), rising time (T_R), and falling time (T_F). Fig 2-4 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is given as follows:

$$F = 1/T \tag{2.2}$$

$$\text{Duty ratio} = W_P/T \tag{2.3}$$

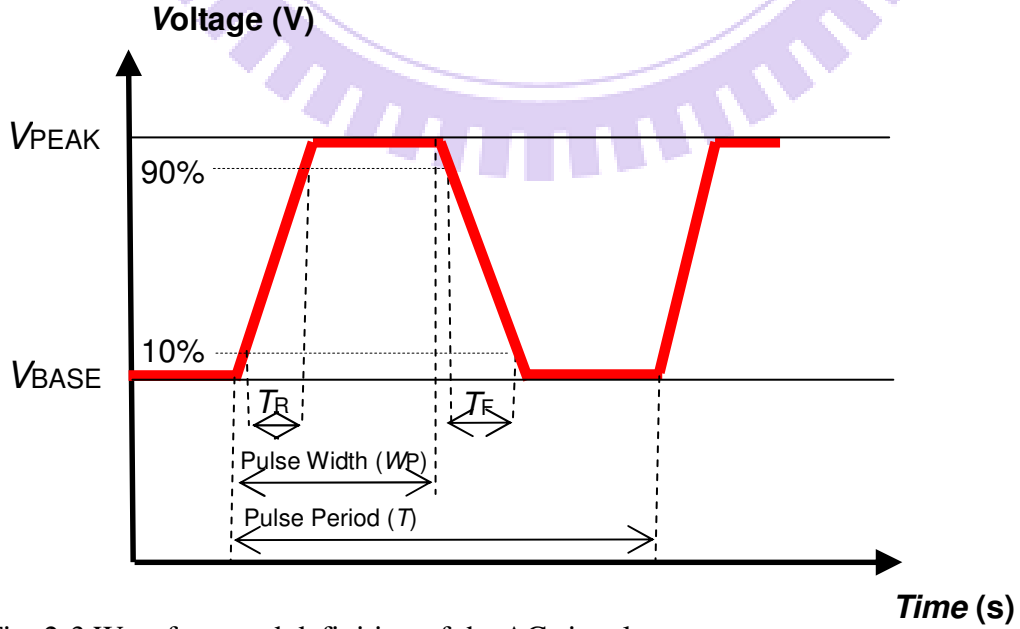


Fig. 2-3 Waveform and definition of the AC signal.

In the AC stress experiments, pulse voltage was applied to the drain electrode or gate electrode while the other two electrodes were grounded, as shown in Fig 2-5 and 2-6. Various experiments for discussing peak level, frequency, duty ratio, rising time and falling time dependence were performed to verify the mechanism of degradation under AC off region stress. The stress time for AC stress was 1000s.

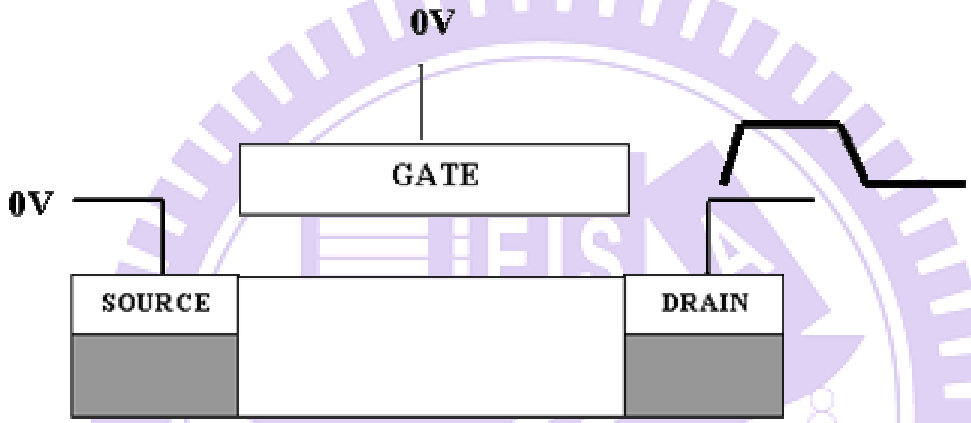


Fig2-4 TFT under drain AC stress with gate and source grounded

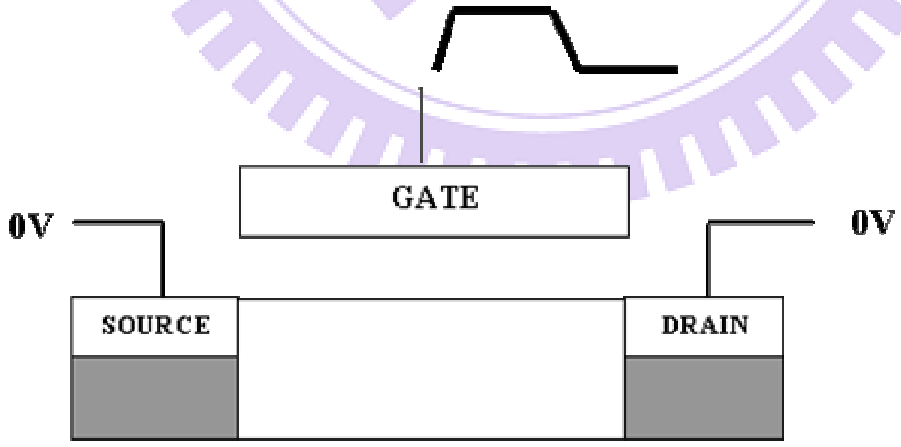


Fig2-5 TFT under gate AC stress with drain and source grounded

The pulse generator of Keithley Model 4200-SCS Semiconductor

Characterization System can stress the device with different conditions listing below:

N-Type OFF Region

Experiments	Gate Voltage(V)	Drain Voltage(V) Source Voltage(V)	Frequency(Hz)	Rising Time(ns)	Falling Time(ns)	Duty(%)
Vd Level	0V	VD0~15V,Vs0V VD0~17.5V,Vs0V VD0~20V,Vs0V VD0~22.5V,Vs0V	500KHz	100	100	50
Frequency	0V	VD0~20V,Vs0V	250KHz 500KHz 1MHz	100	100	50
Duty	0V	VD0~20V,Vs0V	500KHz	100	100	10,50,90
Vg Level	0~-10V 0~-15V 0~-20V	0V	500KHz	100	100	50
Frequency	0~20V	0V	50KHz 500KHz 1MHz	100	100	50
Duty	0~20V	0V	500KHz 50KHz	100	100	10,50,90

Table2-1 Experiment conditions of N-type TFT OFF Region AC Stress.

P-Type OFF Region

Experiments	Gate Voltage (V)	Drain Voltage(V) Source Voltage(V)	Frequency(Hz)	Rising Time(ns)	Falling Time(ns)	Duty(%)
Vd Level	0V	VD0~-15V,Vs0V VD0~-17.5V,Vs0V VD0~-20V,Vs0V VD0~-22.5V,Vs0V	500KHz	100	100	50
Frequency	0V	VD0~-20V,Vs0V	250KHz 500KHz 1MHz	100	100	50
Duty	0V	VD0~-20V,Vs0V	500KHz	100	100	10,50,90
Vg Level	0~10V	0V	500KHz	100	100	50

	0~15V, 0~20V					
Frequency	0~15V	0V	250KHz 500KHz 1MHz	100	100	50
Duty	0~20V	0V	500KHz	100	100	10,50,90

Table2-2 Experiment conditions of P-type TFT OFF Region AC Stress.

2.2.4 CV Measurements

The C-V curves of the gate-to-drain capacitance (C_{GD}) before and after stress at different frequencies were measured with the Agilent E4980A precision LCR meter. We usually measured CV in fresh devices and devices which are stressed for 200 seconds.

Since it is difficult to observe the defect position in TFTs with the I-V characteristic, the C-V measurement is used to examine the information about position and type of degradation in the device after stress [23///改]. For instance, if carriers are trapped by defects, C-V curve stretch out slightly, or if states are generated additionally, C-V curve increase somewhat in the depletion region. Besides, the C−V curves are helpful to identify whether the dominant mechanism of degradation is the increase of fixed charges or trap states. In this work, since the degradation should be symmetric for the gate-to-source and gate-to-drain case, the C-V curves are obtained only for the Cgd curves measured between the drain and the gate.

2.3 Parameter Extraction Method

For most of the researches on TFT, the constant current method is widely-used to determine the threshold voltage (V_{th}). The threshold voltage in the thesis is determined from this method, which extracts V_{th} from the gate voltage at the normalized drain current $I_N=I_D/(W_{eff}-L_{eff})=10nA$ for V_D=0.1V.

The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs. The MOSFETs can be applied to the poly-Si TFTs, so the first order I-V relation in the bulk Si. The field effect mobility (Mu, μ_{FE}) is derived from the maximum value of the transconductance g_m, which can be expressed as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D^2] \quad (2\text{-}1)$$

Where

C_{ox} is the gate capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If the drain voltage V_D is much smaller as compared with$(V_G - V_{th})$ (i.e. $V_D << V_G$ - Vth), then the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \quad (2\text{-}2)$$

And the transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D$$

Therefore, the field effect mobility can be expressed as:

$$\mu_{FE} = \frac{L}{C_{ox}WV_D} g_m \quad (2\text{-}3)$$

In other words, the field-effect mobility can be extracted by taking the maximum value of the g_m into (2-3) when $V_D = 0.1V$

Chapter3

Poly-Si TFT under Pulse Stress in OFF Region

3.1 Degradation Behavior

As we mentioned in chapter1, it is important to know degradation mechanism of TFT under OFF region. There are two stress conditions of AC OFF Region. The first one is Drain AC stress which we mentioned in active matrix. The second one is Gate AC stress which usually happens in three level driving operation.

3.1.1 Drain and Gate toggling effect in the OFF region

N-type TFT

Let us first look at N-type TFT under drain pulse stress. Here we simulate the operation of TFT in active matrix. For stress conditions of N-type TFT, drain electrode is given a 500KHz ,duty 50% ,rising time and falling time 100ns pulse from 0V to 20V, source and gate electrode was grounded in shown in Fig3-1. We can notice that Vgs will be from zero to -20V, there is no voltage difference between gate and source electrode.

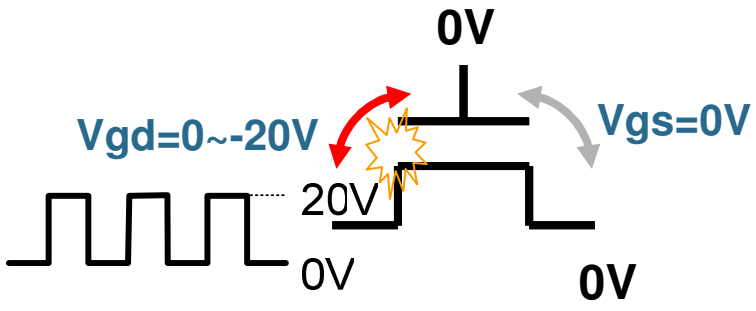


Fig 3-1 N-type TFT under Drain AC OFF region stress

Gate AC stress is very similar to the previous one, but the pulse signal is connected to gate electrode and from zero to 20V to ensure the device operated in OFF region. Drain and source electrodes were grounded which is shown in Fig3-2.

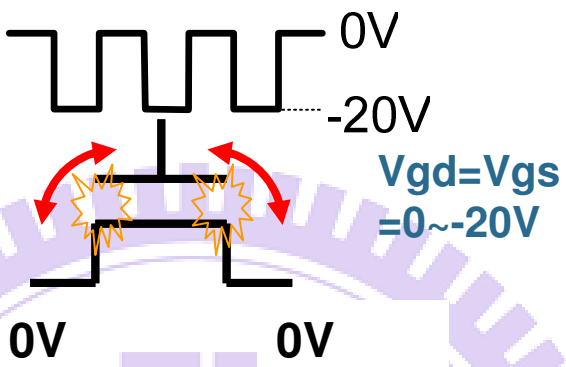


Fig 3-2 N-type TFT under Gate AC OFF region stress

What is the difference between these two stress conditions? We examined IV and CV behavior after stress. Fig 3-3 and Fig 3-4 show IV and CV characteristics after Drain AC stress for N-type TFT. We can find on current lower, mobility decreased and off current increased after stress in IV curves. There is the distortion behavior [22] in CV behavior when we measured the capacitance between gate and drain electrode.

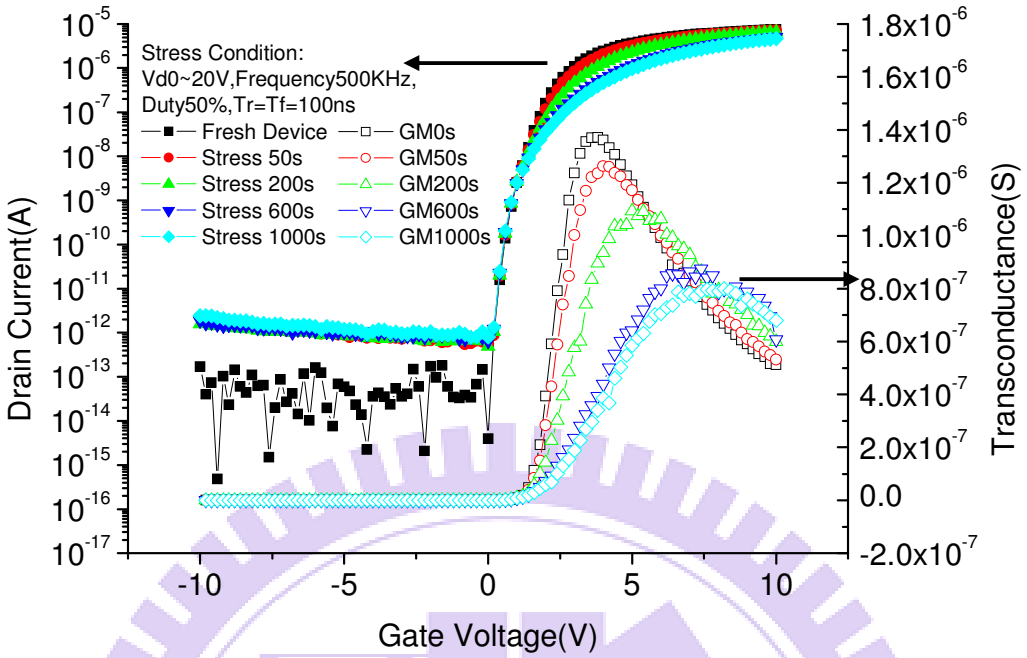


Fig3-3 Id-Vg and transconductance curves before and after AC stress condition of Vd=0~20V Vs=Vg=0V

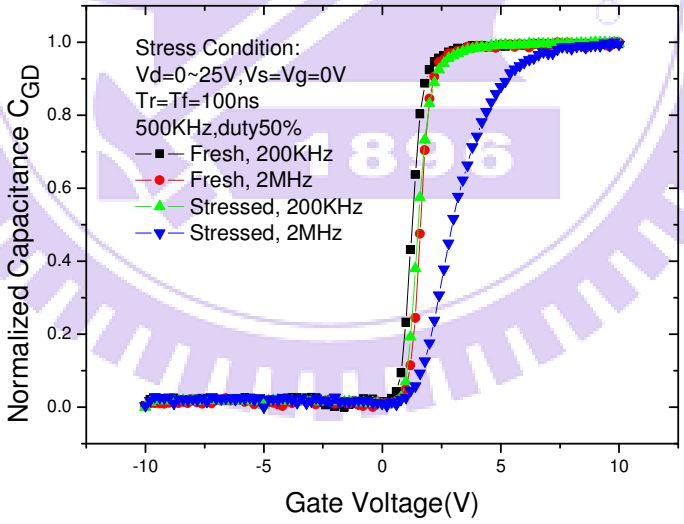


Fig3-4(a)Normalized capacitance Cgd curves for N-type TFT before and after stress in drain AC OFF Region Stress

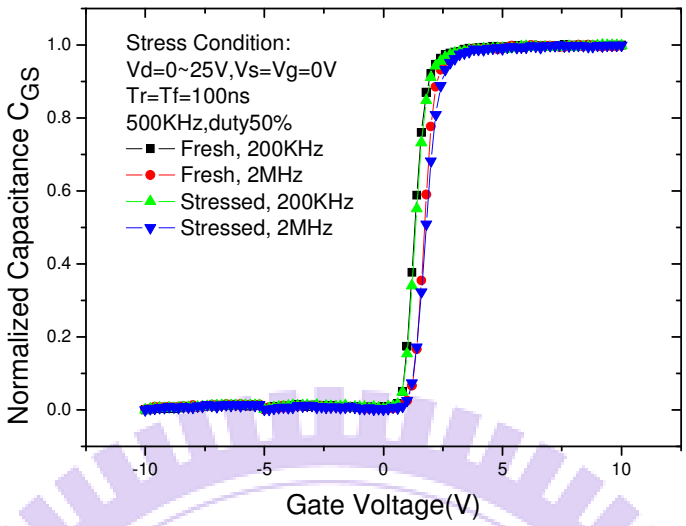


Fig3-4(b) Normalized capacitance Cgs curves for N-type TFT before and after stress in drain AC OFF Region Stress

The phenomenon we see here is similar to Gate AC OFF region stress for N-type TFT which is shown in Fig 3-5 and Fig 3-6. On current , mobility decreased and off current increased after stress. There is also distortion CV behavior in Gate AC OFF region stress. Because of symmetry, the behavior between CGS and CGD is the same.

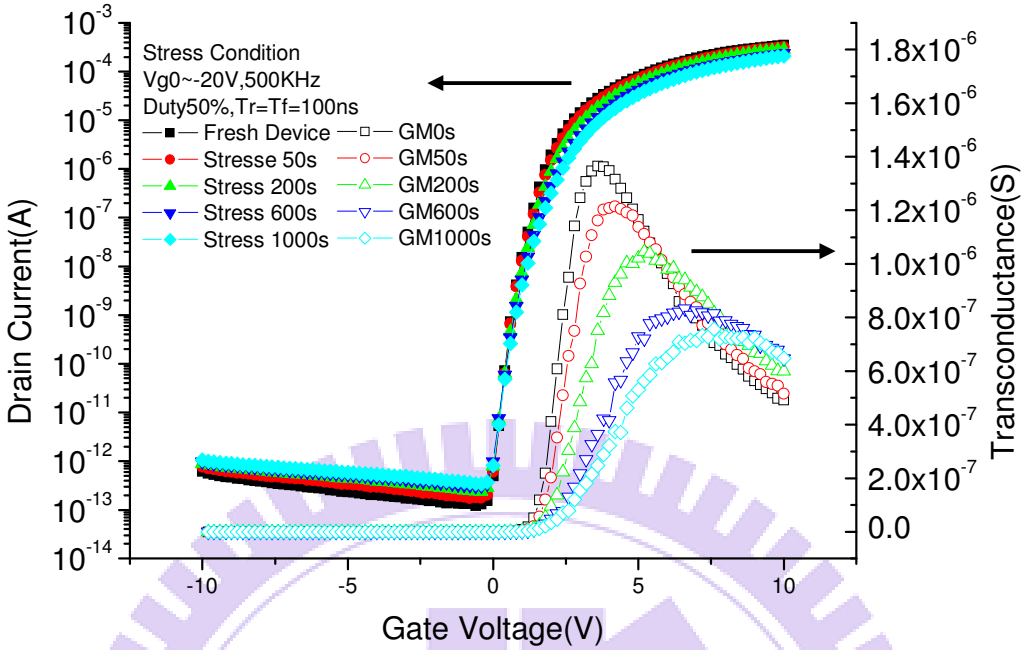


Fig3-5 IV transfer curve of N-type TFT under off region gate pulse

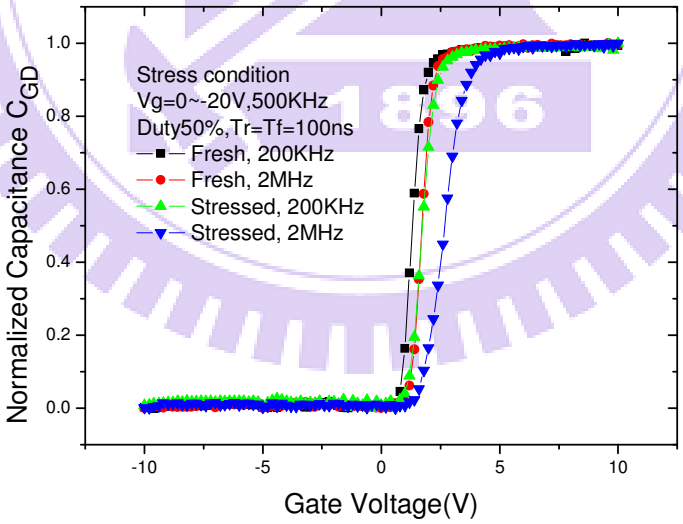


Fig3-6(a) The capacitance behavior CGD of N-type TFT under Gate AC Off region stress

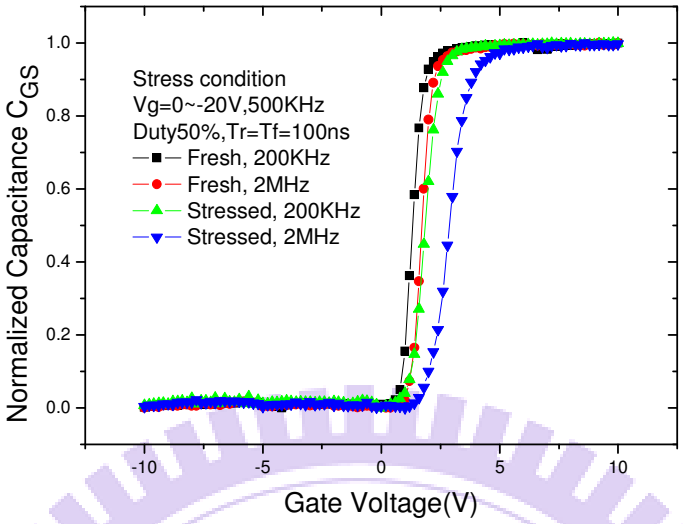


Fig3-6(b) The capacitance behavior CGS of N-type TFT under Gate AC Off region stress

P-type TFT

The difference between Drain AC Off and Gate AC off is shown in Fig3-7 and Fig 3-8. Like N-type TFT, Drain AC Off stress makes Vgd from zero to 20V and Vgs zero. And Gate AC Off stress would let Vgd and Vgs from zero to -20V.

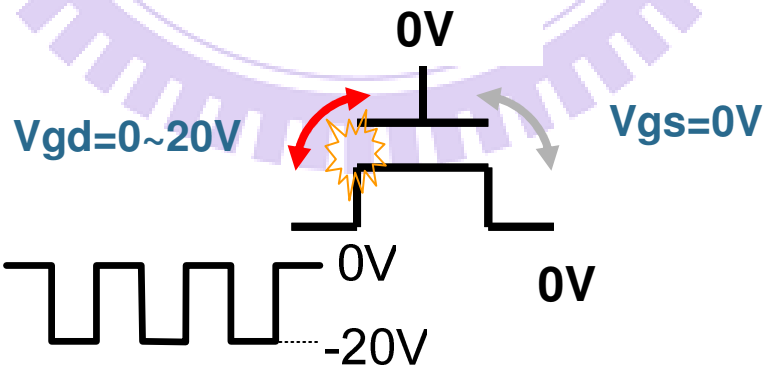


Fig3-7 P-type TFT under Drain AC OFF region stress

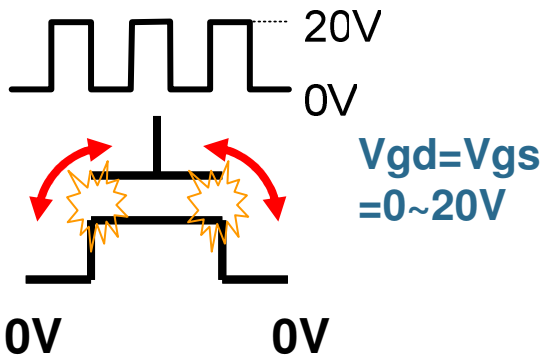


Fig3-8 P-type TFT under GateAC OFF region stress

We also compare IV and CV characteristics under two different stress conditions. For P-type TFT, degradation behavior under Drain AC off region stress is shown in Fig 3-9 and Fig3-10. We may find mobility increased and off current decreased after stress in Fig3-9. CV curves show apparent increase for the gate voltage which is less than the flat band voltage in Fig3-10(a)

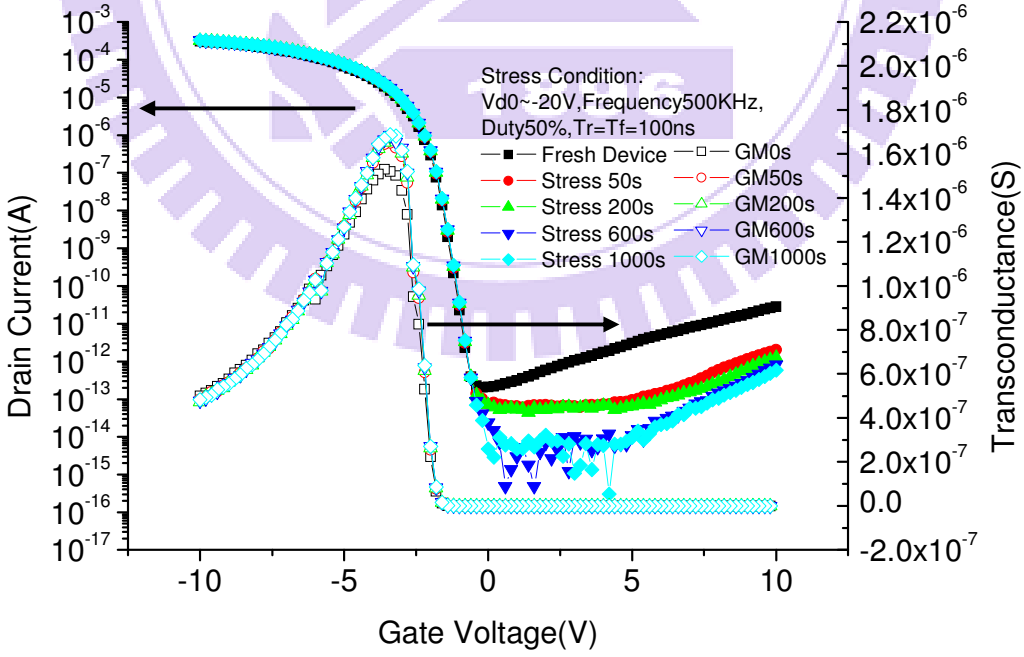


Fig3-9 Id-Vg and transconductance curves before and after AC stress condition of Vd=0~-20V Vs=Vg=0V

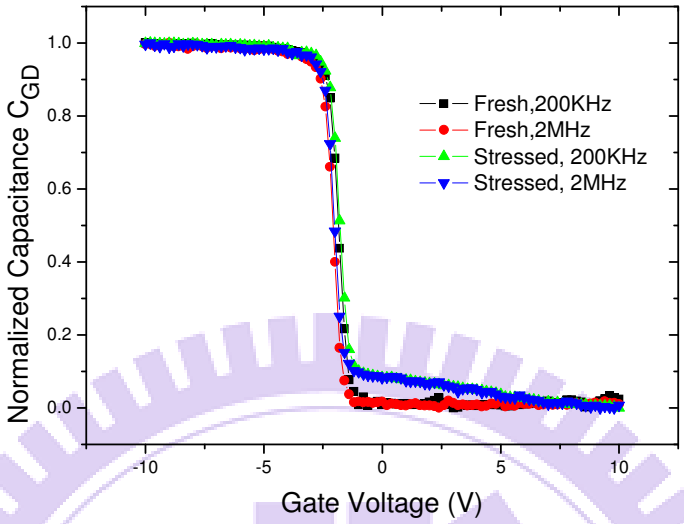


Fig3-10(a)Degradation of normalized Cgd curve in P-type TFT under 200 seconds off region drain stress

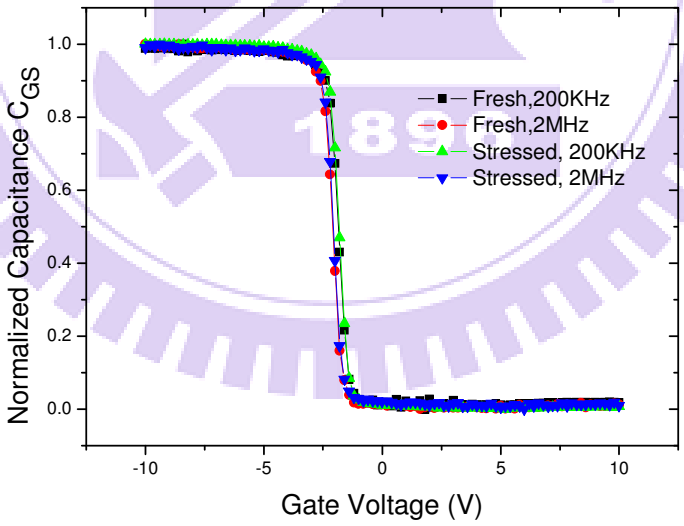


Fig3-10(b)Degradation of normalized Cgs curve in P-type TFT under 200 seconds off region drain stress

We got similar behavior in Gate AC stress in P-type TFT which is shown in

Fig3-11 and Fig3-12.

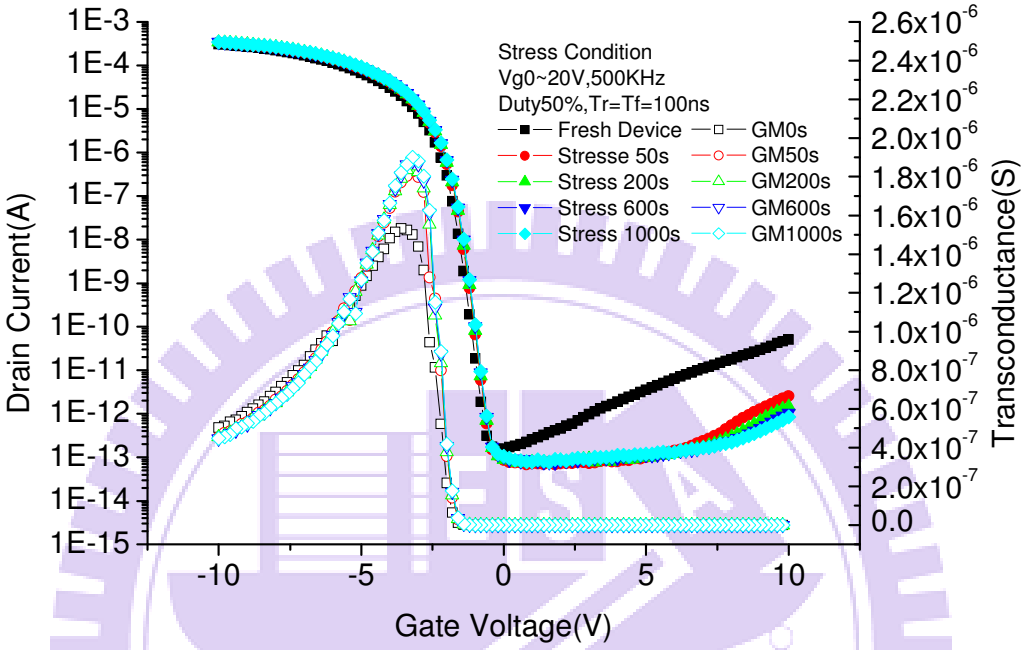


Fig3-11 IV transfer curve of P-type TFT under off region gate pulse

Fig3-12 is the capacitance behavior under gate pulse stress. For the stressed device, the Cgd curves show apparent increase for the gate voltage lower than the flat band voltage. For symmetry we mentioned before, the capacitance behaviors of Cgd and Cgs are also the same.

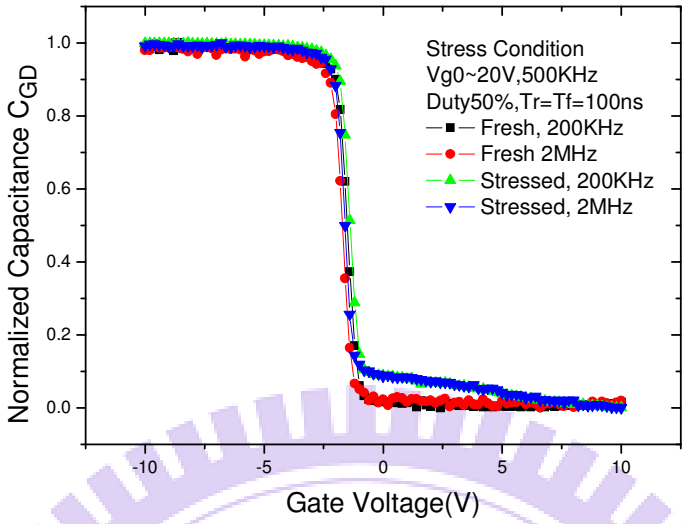


Fig3-12(a) Capacitance behavior between gate and drain electrode of P-type TFT

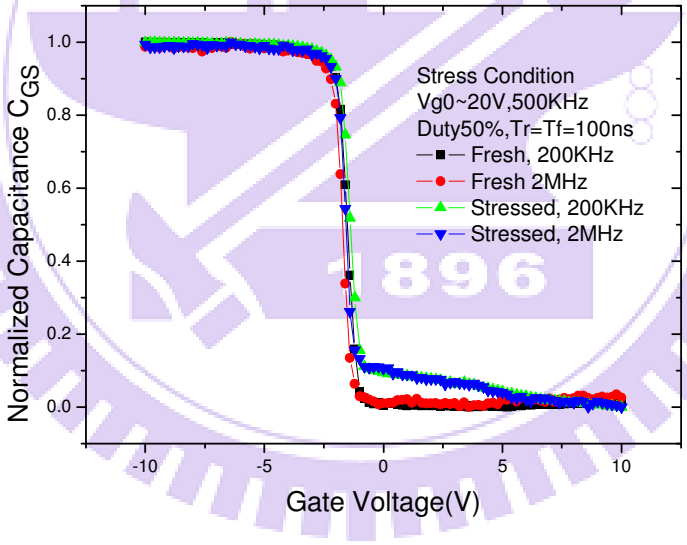


Fig3-12(b) Capacitance behavior between gate and source electrode of P-type TFT

From above experiments, we find the similarity between drain and gate AC stress. Device behavior is alike after stress. So we would like to focus on the behavior of Gate AC stress. And we can link to previous study in which the device is operated under Gate AC On/Off pulse signal [23].

3.1.2 Frequency response circuit model

In order to have precise understanding of AC stress, we consider the device operated in different frequency. Fig 3-13 shows the equivalent circuit of TFT, distributed Cin is insulator capacitance, Cj junction capacitance, Rch is channel resistance and Rc is junction resistance.

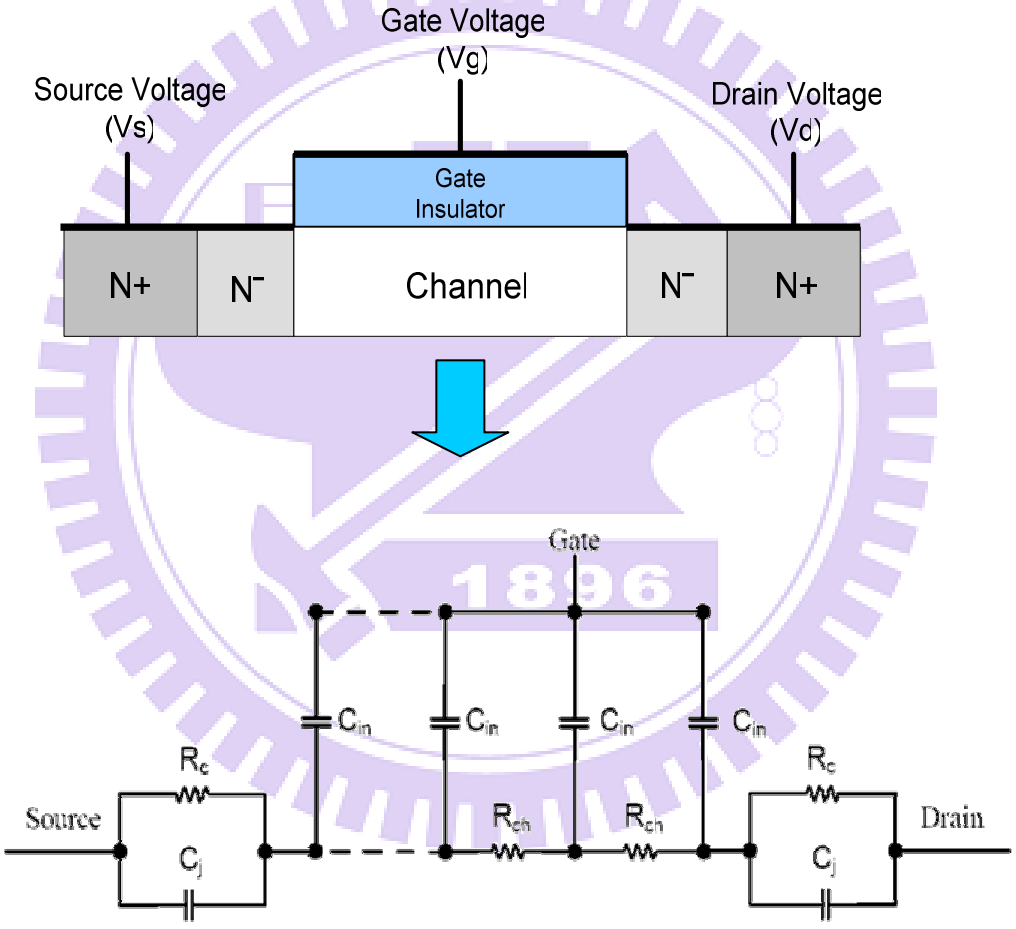


Fig3-13 Equivalent circuit of N-type TFT

The impedance of oxide will be "|Zox|" , the value would be |1/j2 π fCin| . The capacitance of oxide in our device is 50fF, so the impedance of oxide , |Zox|, is 1/(2 π f50fF). The impedance will change under different signal frequency. And the

impedance of resistance Z_R under off region operation will be the channel resistance which can be expressed as VD/ID. Averagely, the off current is around 10^{-12}A when drain voltage is applied at 10V. As the result, the impedance of resistance is around $10^{13}\Omega$.

If the device is under low frequency operation, the impedance of oxide will be very large. |Zox| would be dominate term in the equivalent circuit, the voltage of signal would be mainly cross on oxide.Fig3-14 shows the low frequency operation in DC stress condition, gate voltage was -20V and source and drain electrode were grounded. The IV behavior shows that mobility increased a little(less than 5%) after 1000 second operation.

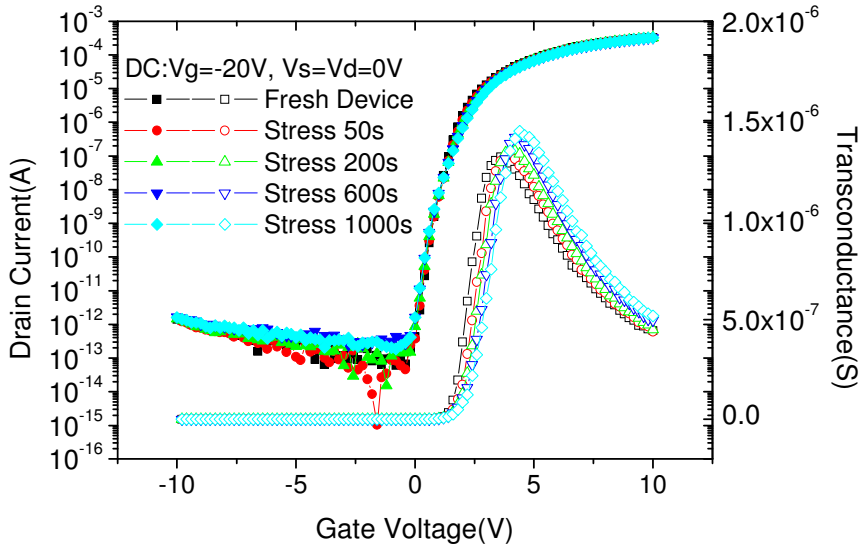


Fig3-14 The device operated in low frequency impulse signal.

If the device is under high frequency operation, the impedance of oxide would be smaller than Z_R. The impedance of oxide--|Zox| --is 6MΩ, it is very small compared

to Z_R which value is $10^{13}\Omega$. So Z_R would be the dominate term in high frequency operation. The signal voltage would be mainly across on resistance. Fig 3-15 shows the device operated in 500KHz off region signal. After 1000 seconds stress, mobility of the device decreased a lot (40%).

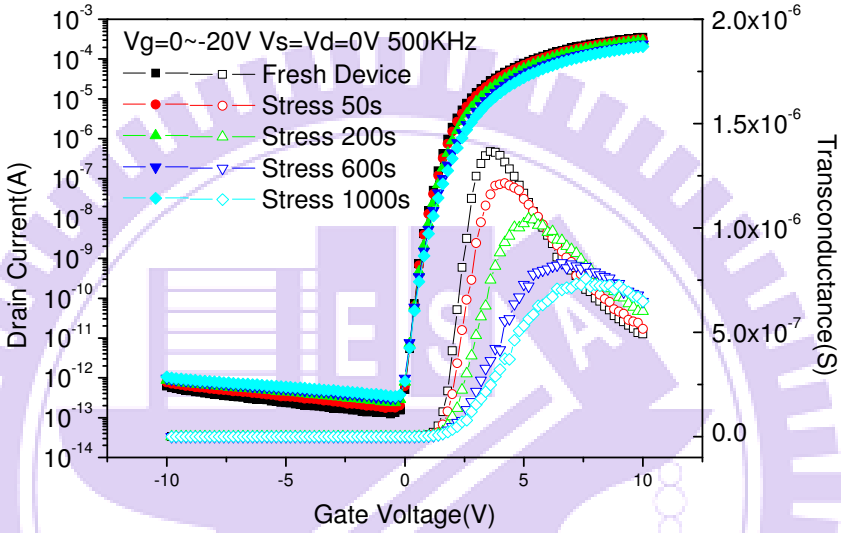


Fig3-15 The device operated in high frequency impulse signal.

After discussing the device operating under different frequency, we know the degradation behavior after long time operation is ambiguous in low frequency impulse signal. So the study of Gate AC stress will be mainly on high frequency operation. And it can also link to previous study which is operated in 500KHz AC On/Off pulse signal [24].

3.2 Similarity to other stress conditions

3.2.1 DC On region

N-type TFT

The degradation behavior of gate toggling was shown in section 3.1.1 and Fig3-16. From previous research [25], we find the similarity between DC hot carrier effect and gate AC toggling under off region. Fig 3-17 shows the IV and CV behavior of N-type TFT after DC hot carrier stress. After stress, mobility and on current became lower in IV curves, CV distorted under high frequency measurement in both stress conditions. The similarity of degradation behavior really exists.

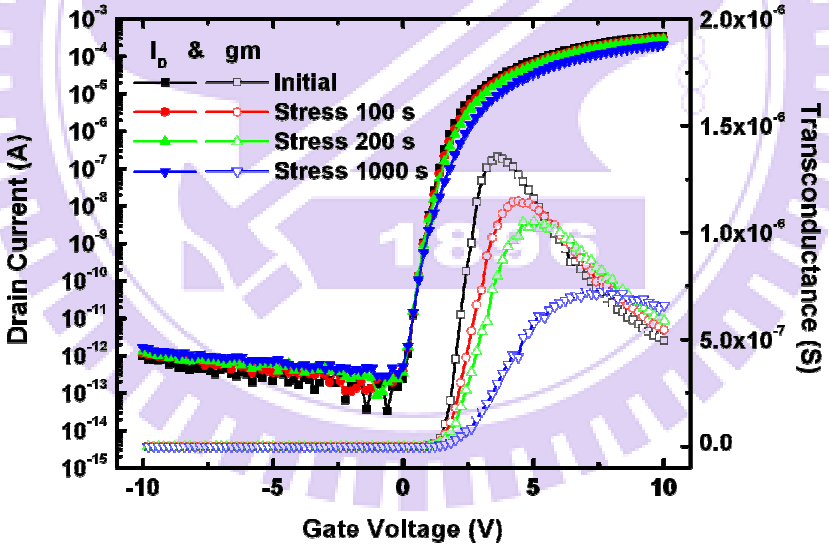


Fig3-16(a) IV characteristics under gate AC toggling in N-type TFT

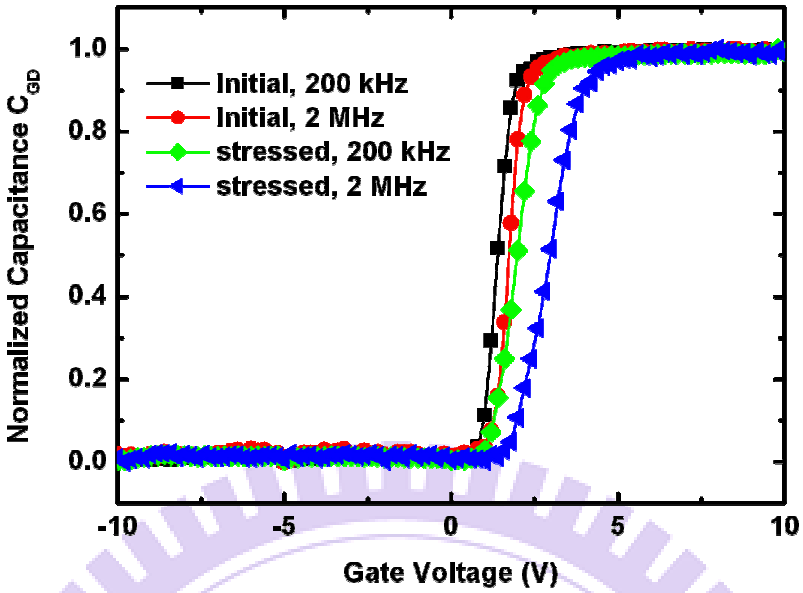


Fig3-16(b) CV behavior under gate AC toggling in N-type TFT

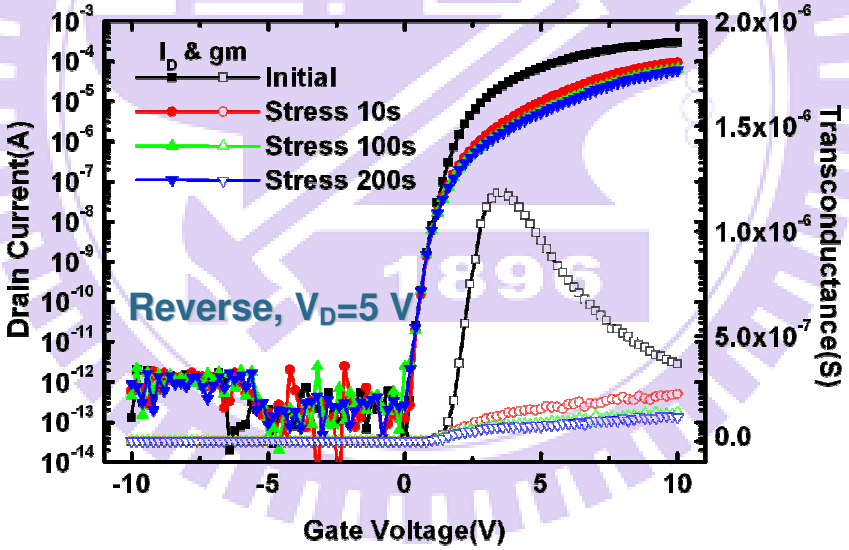


Fig3-17(a) IV characteristics under DC hot carrier stress (Vg=3V, Vd=15V, Vs=0V) in N-type TFT.

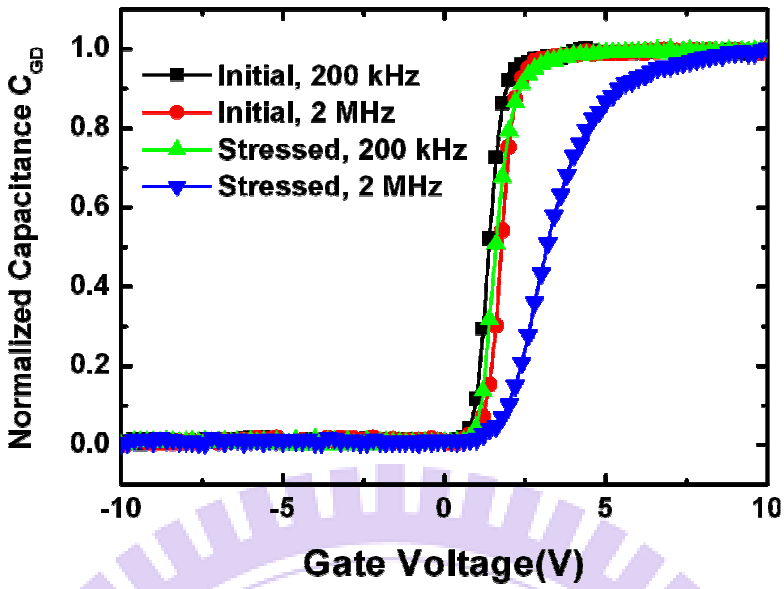


Fig3-17(b) CV behavior under DC hot carrier stress (Vg=3V, Vd=15V, Vs=0V) in N-type TFT.

P-Type TFT

There is also similarity between DC hot carrier stress and gate AC toggling effect in P-type TFT which is shown in Fig3-18 and Fig3-19.

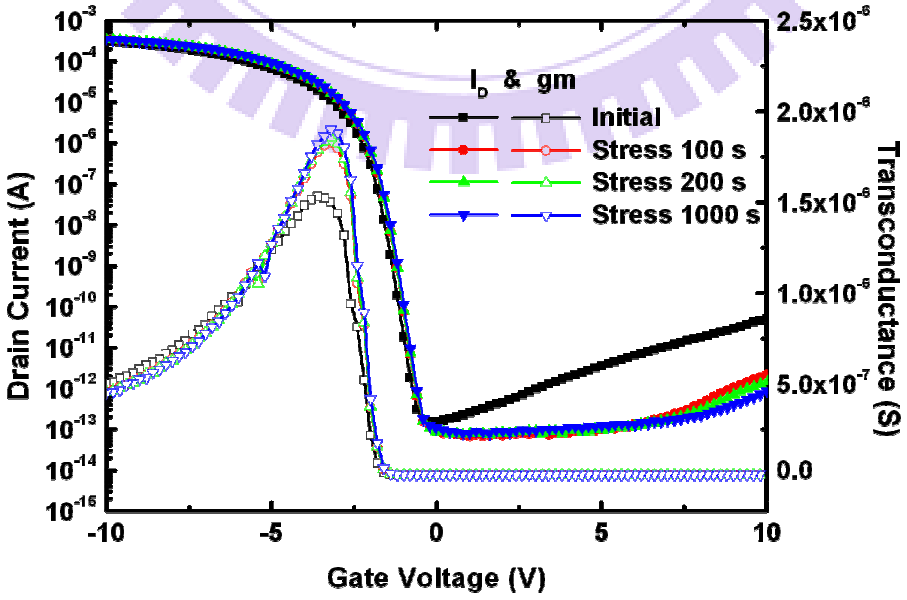


Fig3-18(a) IV characteristics under gate AC toggling in P-type TFT

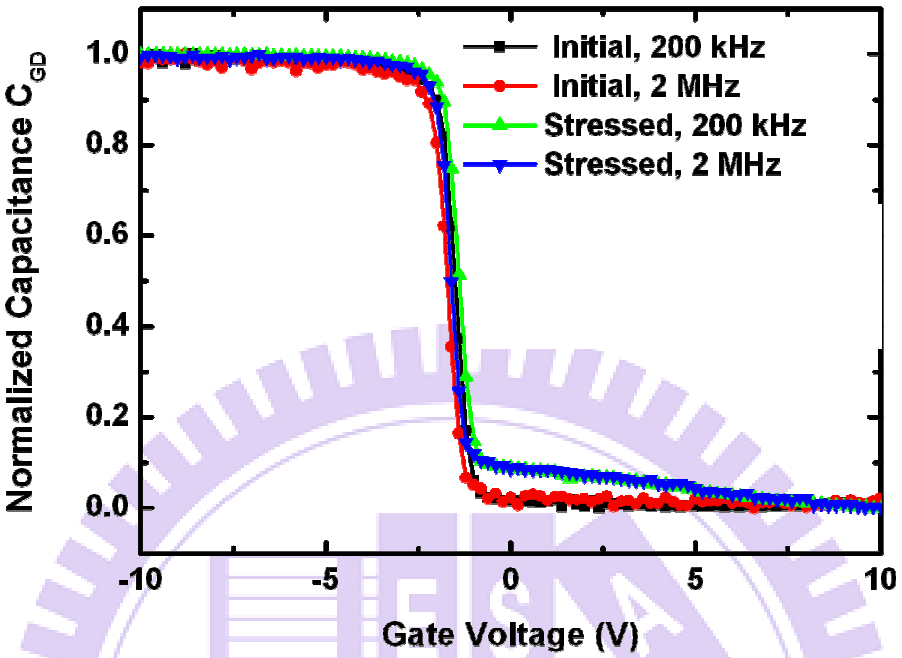


Fig3-18(b) CV behavior under gate AC toggling in P-type TFT

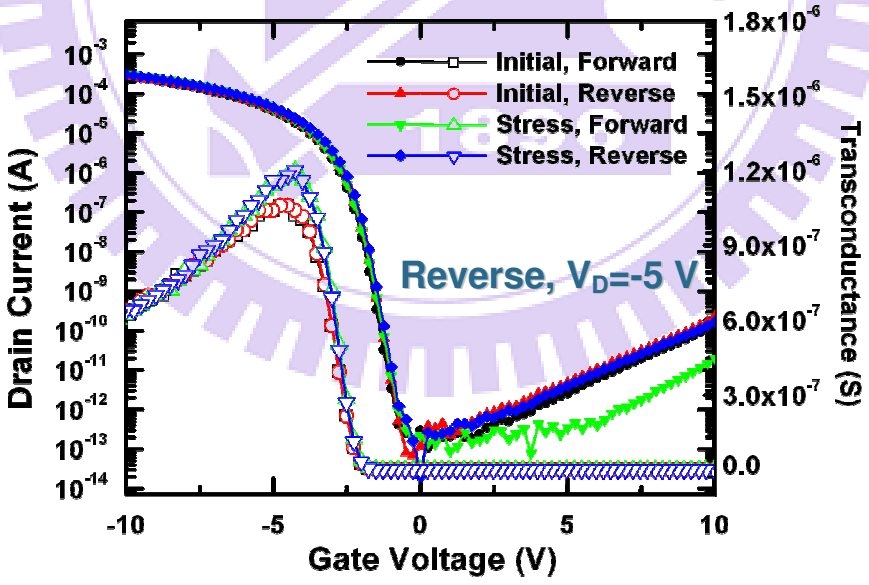


Fig3-19(a) IV characteristics under DC hot carrier stress (Vg=-3V, Vd=-20V, Vs=0V) in P-type TFT.

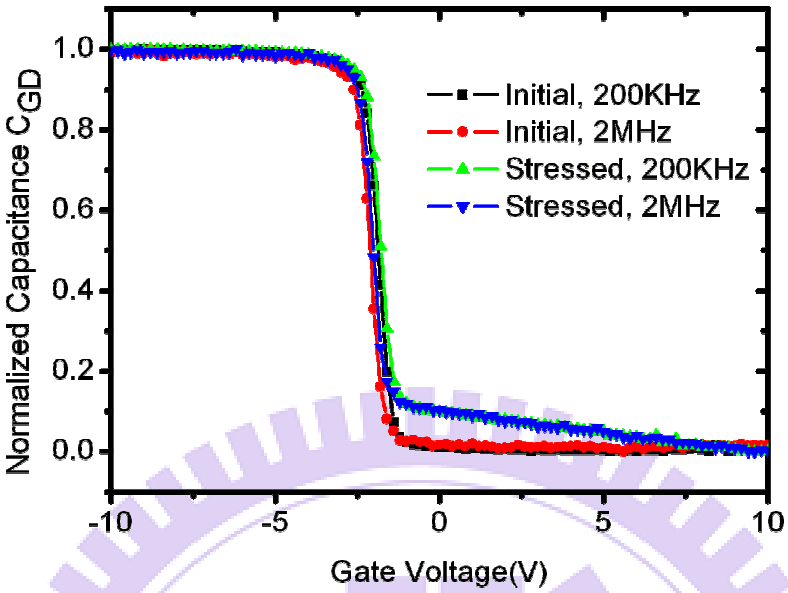


Fig3-19(b) CV behavior under DC hot carrier stress (Vg=-3V, Vd=-20V, Vs=0V) in P-type TFT.

Here comes the question: what makes the device behavior in gate AC toggling similar to DC hot carrier stress? We know that the device under DC hot carrier stress condition would have large current and large electric field near the drain side (because of large drain voltage). However, in gate AC toggling stress, impedance of resistance would be dominate term in high frequency operation based on our model, the signal voltage would be across resistance or junction. So there could be large electric field near the drain if voltage across junction. But the stress current would be small because device is operated in off region. It is not the case compared to large stress current in DC hot carrier stress.

3.2.2 DC Off region

Therefore, we consider another condition: DC Off Region stress. Unlike DC On region stress (hot carrier), the device is operated under off region (shown in Fig3-20)

to ensure a small stress current.

Fig3-20 DC Off region stress for N-Type TFT

The large drain positive voltage is applied to make a large electric field in the drain junction. It is shown in Fig3-21, the right figure is the band diagram under DC off region stress. We can see the drain junction is largely reversed.

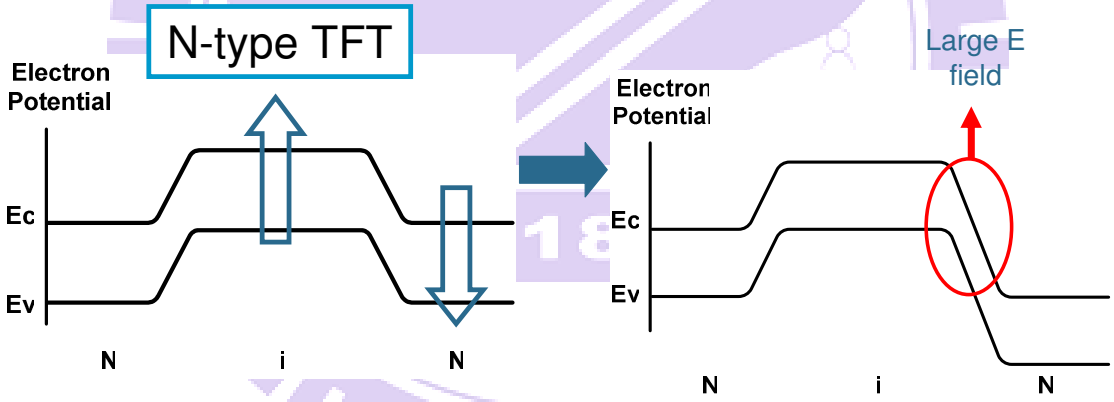


Fig 3-21 Band diagram of drain DC off region stress (the right one)

The degradation behavior of IV and CV characteristic is shown in Fig3-22.

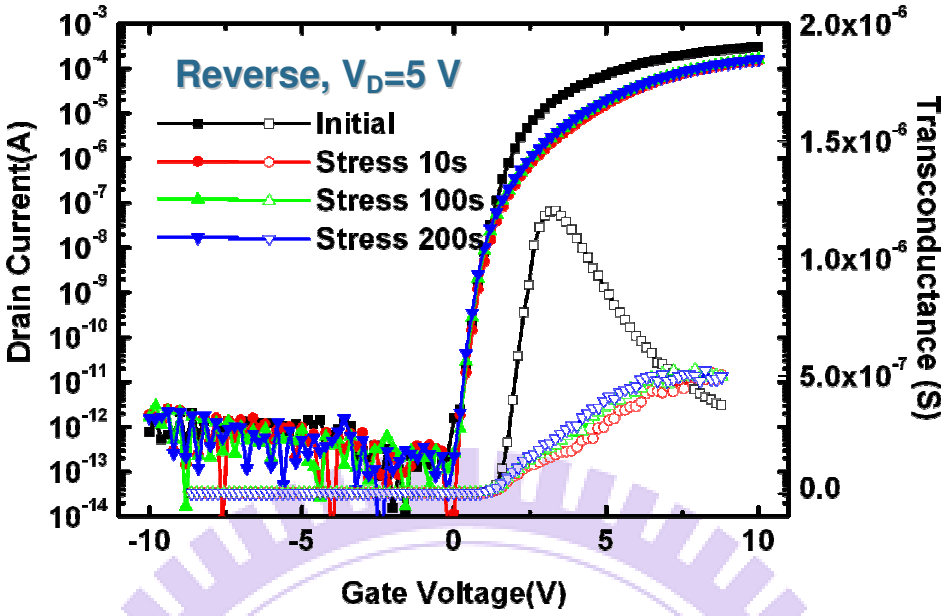


Fig 3-22(a) IV characteristics under Drain DC off region stress

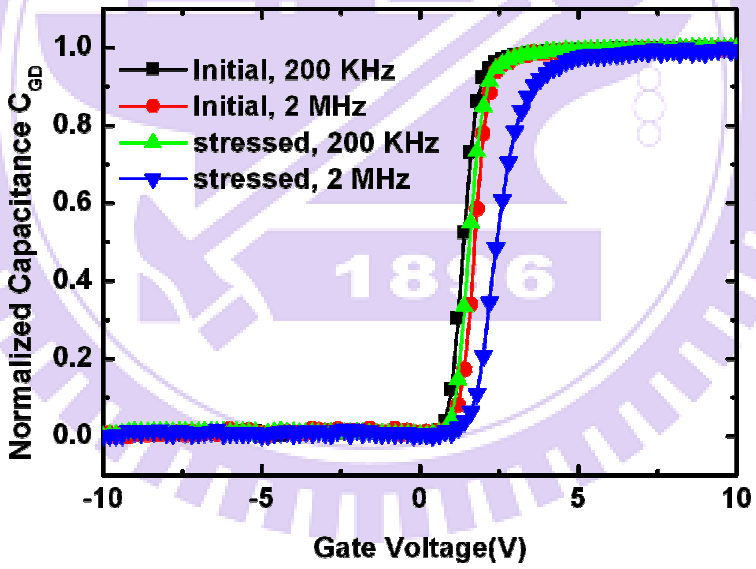


Fig3-22(b) CV behavior under Drain DC off region stress

As smarter as you, you had knew the similarity between Drain DC off region stress and gate AC toggling stress. And it is also true for P-type TFT we can see in Fig3-25. In this time, the device is still operated in off region (Fig3-23), but the drain is applied to a large negative drain voltage to make drain junction largely reversed shown in Fig3-24.

Fig3-23 DC Off region stress for P-Type TFT

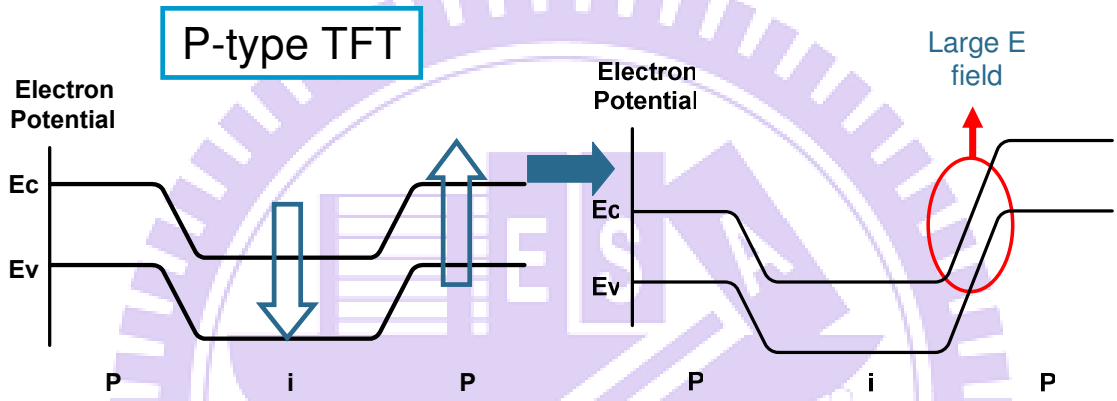


Fig 3-24 Band diagram of drain DC off region stress (the right one)

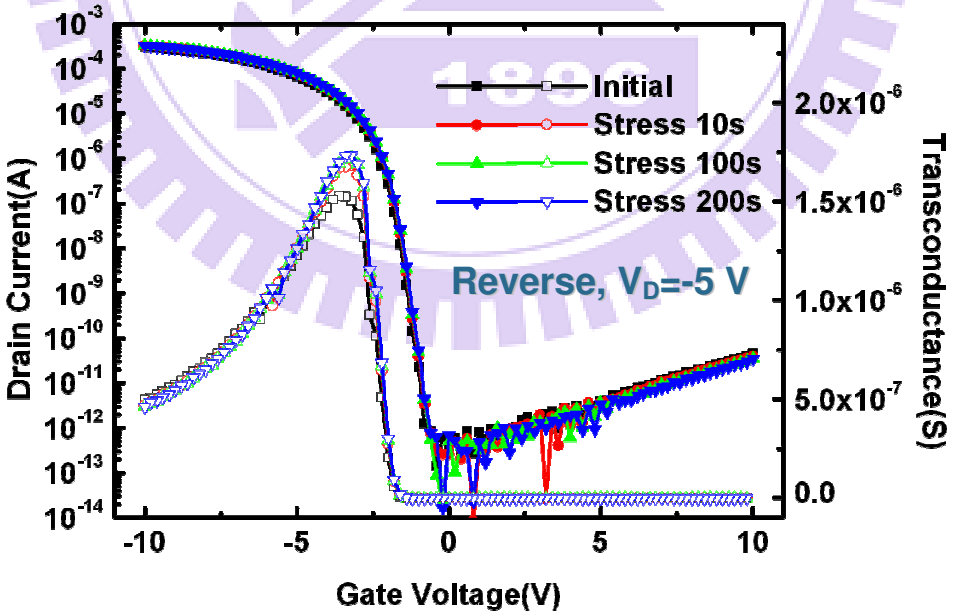


Fig 3-25(a) IV characteristics under Drain DC off region stress

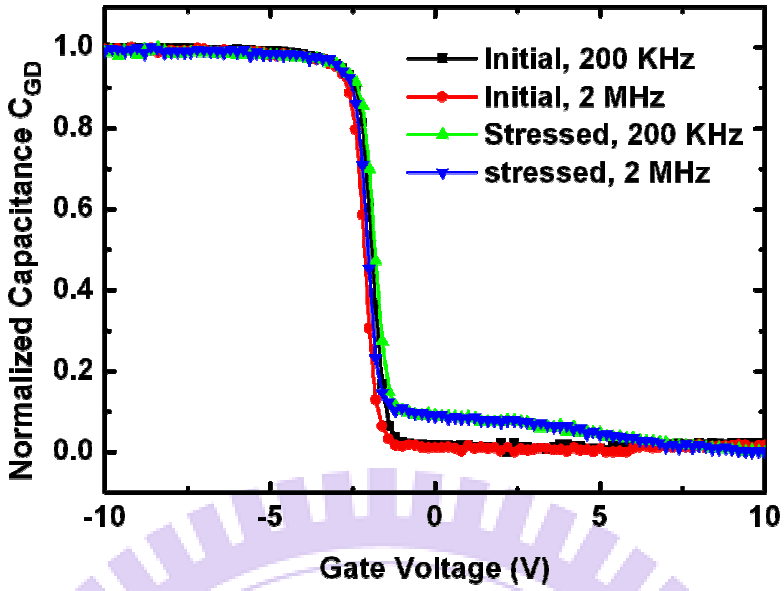


Fig3-25(b) CV behavior under Drain DC off region stress

Consider DC Off region and AC gate toggling stress, there is similar degradation behavior. And we know the device of DC off region stress is under large drain electric field and has small stress current for sure. The device of gate AC toggling effect also has small stress current but we are not sure whether if there is large electric field to make the degradation. By the similar degradation behavior, we could know there would be a large electric field in drain junction analogically.

3.2.3 AC On/Off region

From previous section, we know the degradation is due to large electric field in drain junction. How about AC On/Off region stress? According to previous study [26], there are many carriers which induced in the accumulation period. And the device would have large electric field near source/drain electrode during transient time of AC pulse signal shown in Fig3-26 generating defects. Could there be the similar degradation behavior in AC On/Off region stress?

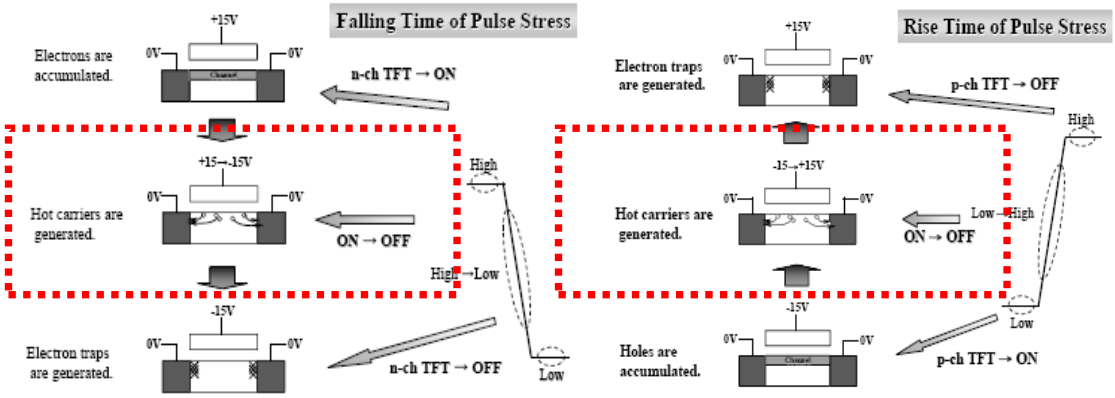


Fig3-26 AC On/Off region stress in N and P type TFT.

The answer is "yes" according to Fig3-27 and Fig3-28 which show gate AC On/Off region stress for N and P type TFT. Both devices have similar degradation behavior compared to devices in gate AC toggling condition.

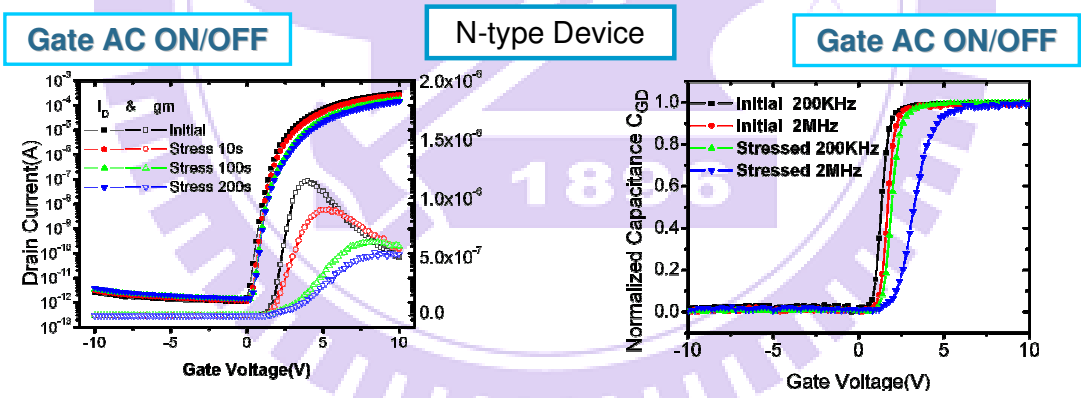


Fig 3-27 Gate AC On/Off region stress for N-type TFT

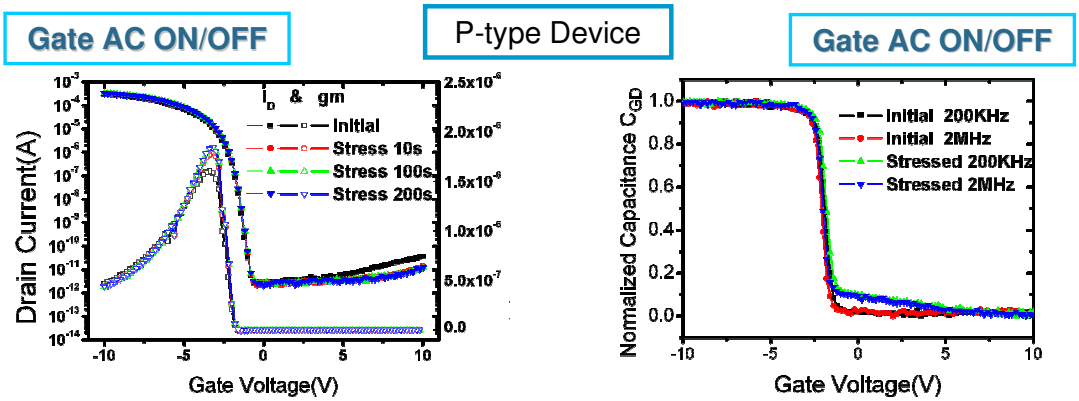


Fig 3-28 Gate AC On/Off region stress for P-type TFT

3.2.4 Comparison and Discussions

The Figure below (Fig3-29) is the degradation behavior among these four stress conditions discussed in previous sections. For N-type TFT, mobility would decrease as time goes by. The degradation rate of AC On/Off region is larger than AC Off region when device is under dynamic operation. The degradation rate of DC hot carrier stress (DC On region) is larger than DC Off region when DC voltage is applied.

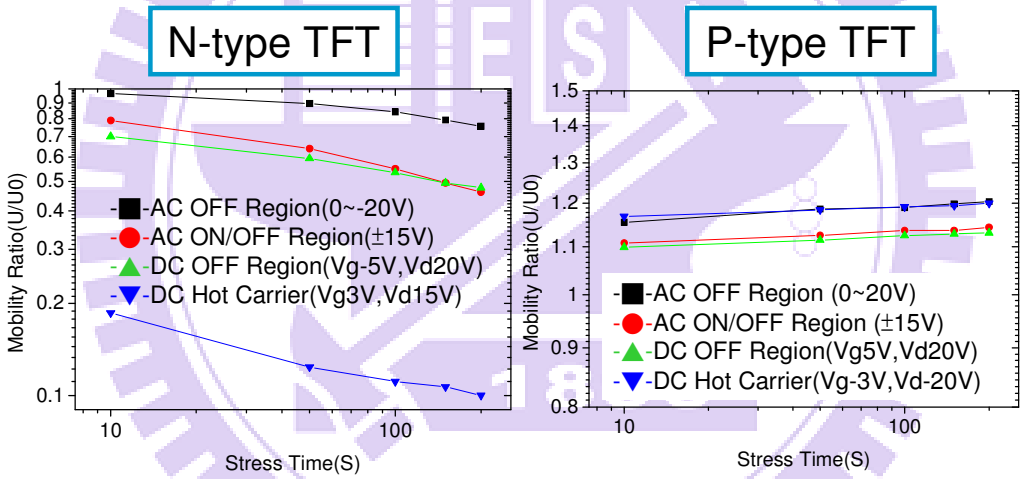


Fig 3-29 Degradation behavior in these four different stress conditions

For P-type TFT, mobility increases as time goes by. There is not big difference of degradation rate among these four stress conditions.

What is the difference? We try to figure it out through Fig3-30. Under degradation, there is a large electric field on junction. For N-type TFT, conduction carriers which are activated by thermal energy would collide, break the silicon bonds and generate many defects. Actually, these defects are extra states, which would make

on-current, mobility decreased and off-current increased in IV characteristics, CV curves would have distortion behavior under high frequency measurement [27]. For P-type TFT, electrons which are leakage current under large electric field would flow through junction and get trapped in oxide because of positive gate voltage. This is called Channel shortening effect [28], so the mobility would increase and off current would decrease after stress. And the coulomb blockade effect from channel shortening would make the difference small among different stress condition. The degradation rate among different stress condition would be ambiguous.

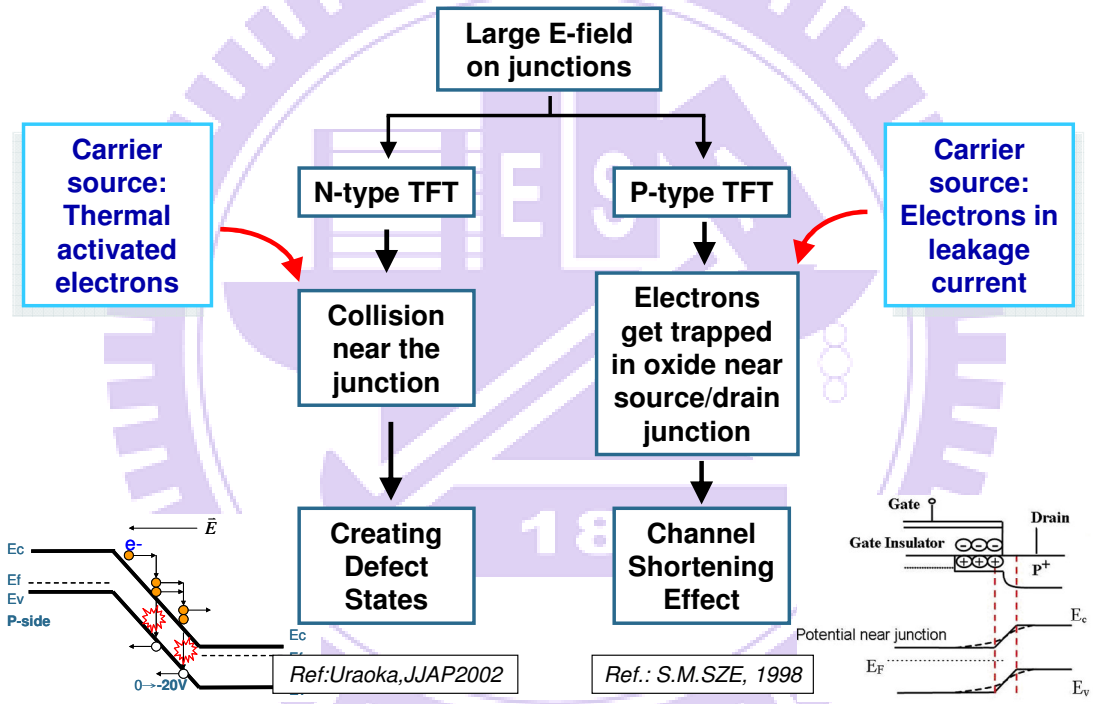


Fig3-30 Degradation Mechanism of N and P type TFT under large electric field in junction

Here we put all stress conditions together and they all have similar degradation behavior. According to the description of hot carrier effect, there should be carrier source and large electric field for carriers gaining high kinetic energy. For AC and DC Off region stress, carriers would mainly come from thermal activation. For AC On/Off and DC On region stress, carriers are almost conduction carriers. And there all

have large electric field at junctions under stress. So we can say that they all are “hot carrier effects” shown in Fig 3-31.

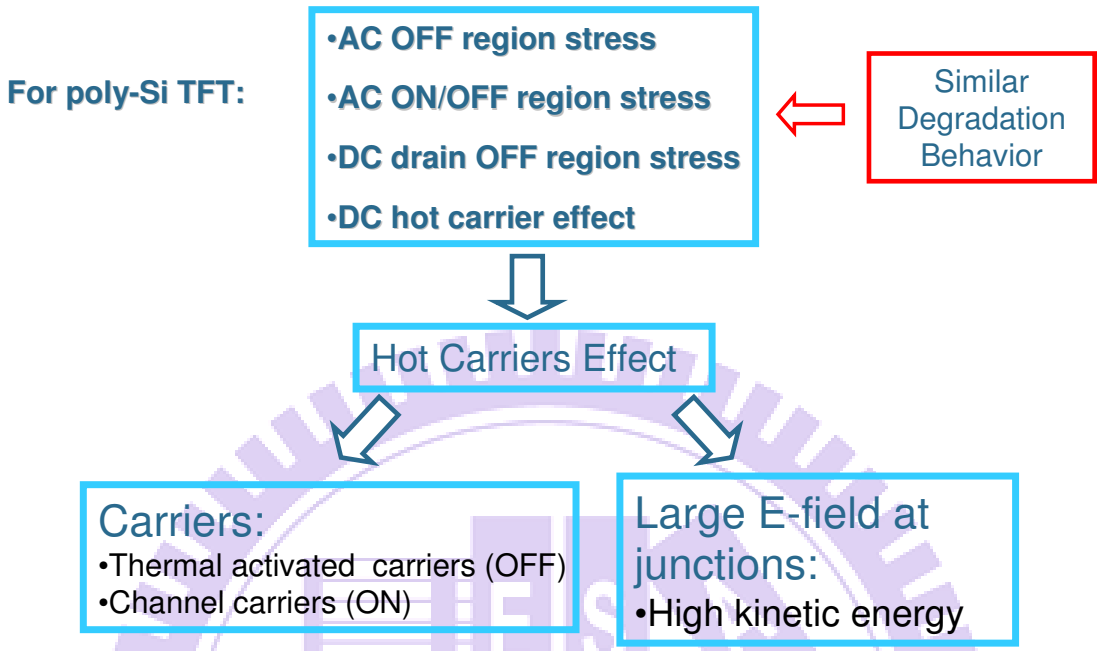


Fig. 3-31. Hot carrier effects

Chapter4

Details of dynamic operation

4.1 Waveform parameters

From previous chapter, we discussed gate toggling and other stress conditions in which the degradation behavior comes from hot carrier effect. But for AC toggling effect, we know the device is dynamically operated, there may be transient behavior, electric field would change rapidly under different pulse period. In order to know the details, we consider the relation between different waveform parameters and degradation rate of device (Table 4-1).

Experiments	Gate Voltage(V)		Frequency(Hz)	Duty(%)	TR(ns)	TF(ns)
Vg, OFF Amplitude	N-Type: 0~-15V 0~-17.5V 0~-20V 0~-22.5V	P-Type: 0~15V 0~17.5V 0~20V 0~22.5V	500KHz	50	100ns	100ns
Frequency	0~-20V	0~20V	250KHz 500KHz 1MHz	50	100ns	100ns
Duty	0~-20V	0~20V	500KHz	10% 50% 90%	100ns	100ns
TR	0~-20V	0~20V	500KHz	50	100ns 300ns 700ns	100ns
TF	0~-20V	0~20V	500KHz	50	100ns	100ns 300ns 700ns

Table 4-1 Waveform parameters for N-type and P-type TFT

4.1.1 N-type TFT

From Fig4-1 to Fig4-5, we can see the degradation behavior under different parameters. Larger signal range, larger frequency, larger duty ratio, we can have worse degradation. In addition, larger duty ratio would have larger pulse width shown in Fig 4-3(b).Larger rising time and falling time, we can have smaller degradation rate.

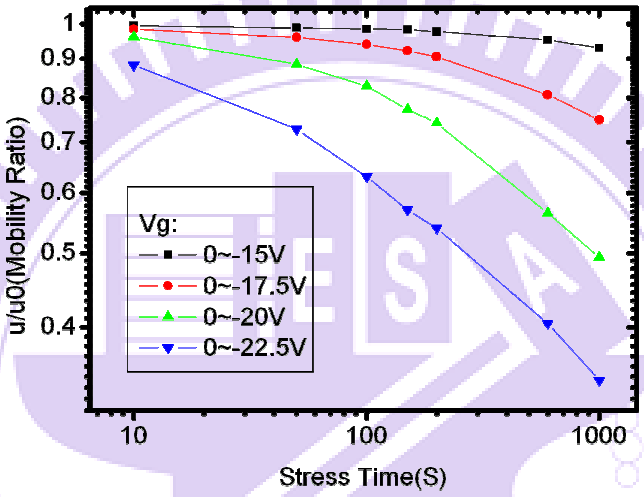


Fig4-1 Degradation behavior under different vg range

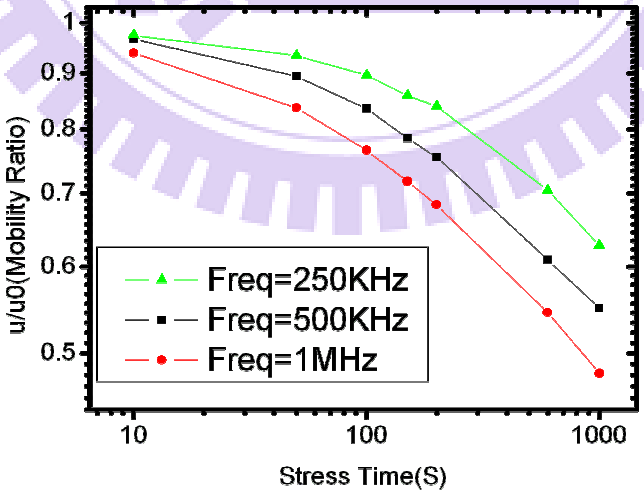


Fig4-2 Degradation behavior under different frequency

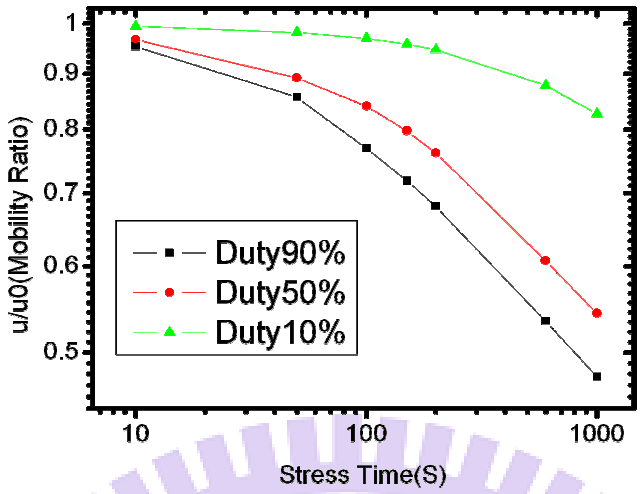


Fig4-3(a) Degradation behavior under different duty ratio

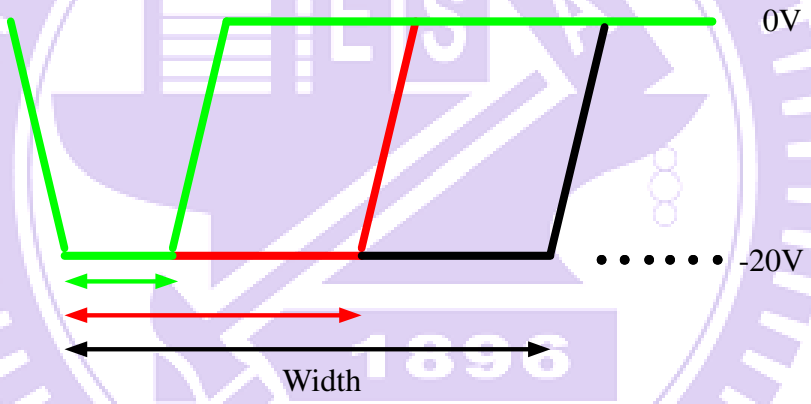


Fig4-3(b) Larger duty ratio has larger width

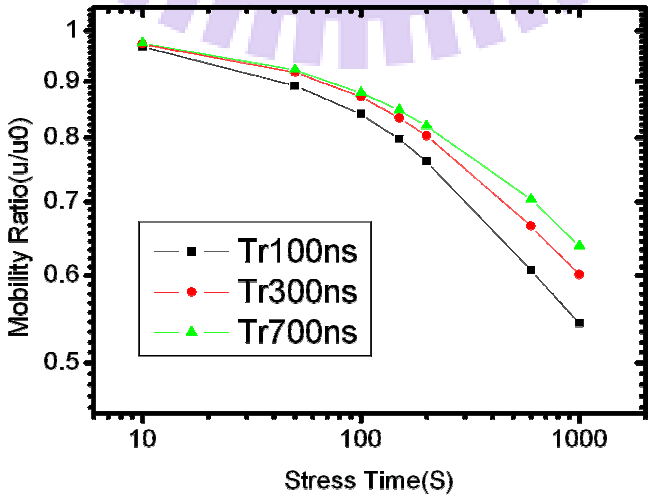


Fig4-4 Degradation behavior under different rising time

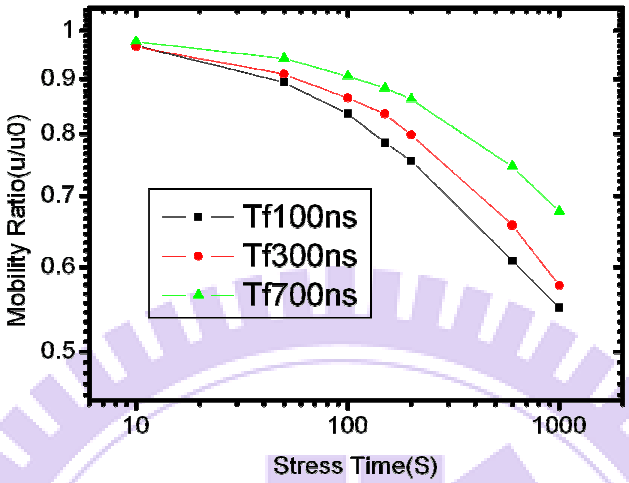


Fig4-5 Degradation behavior under different falling time

4.1.2 P-type TFT

In Fig4-6, degradation rate is larger when vg range is larger. But the degradation behavior is not obvious in difference frequency shown in Fig4-7. Three lines in different frequency cross each other. Same thing happens in different rising time and falling time shown in Fig 4-9 and Fig4-10 and happens partly in Fig 4-8. In Fig4-8, the degradation rate in duty 10% is lower than duty 50% and 90%. But the other two lines cross each other , it is hard to tell the overall trend of degradation behavior.

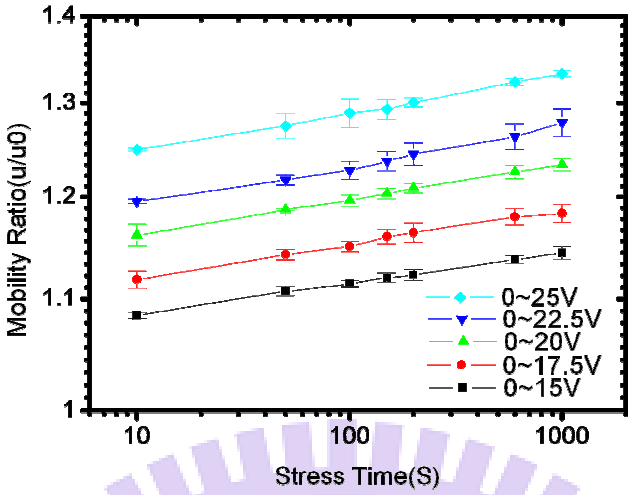


Fig4-6 Degradation behavior under different vg range

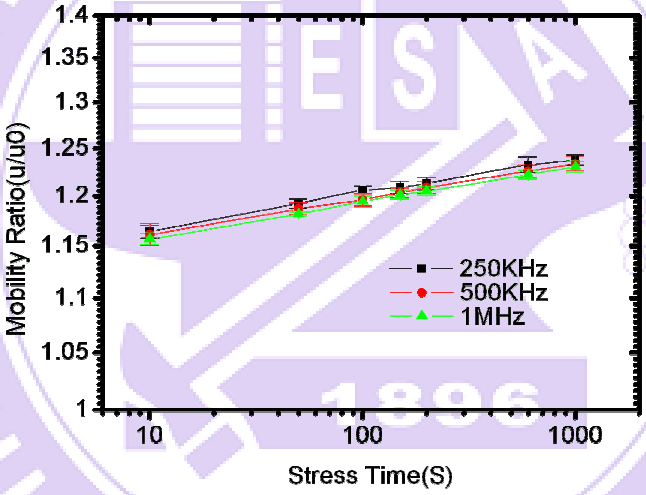


Fig4-7 Degradation behavior under different frequency

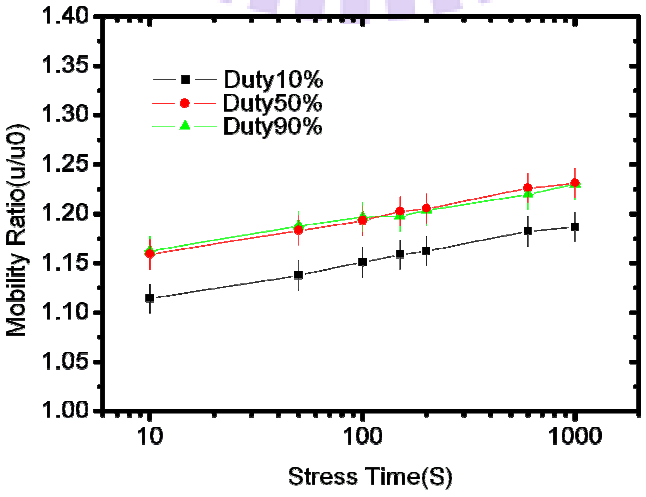


Fig4-8(a) Degradation behavior under different duty ratio

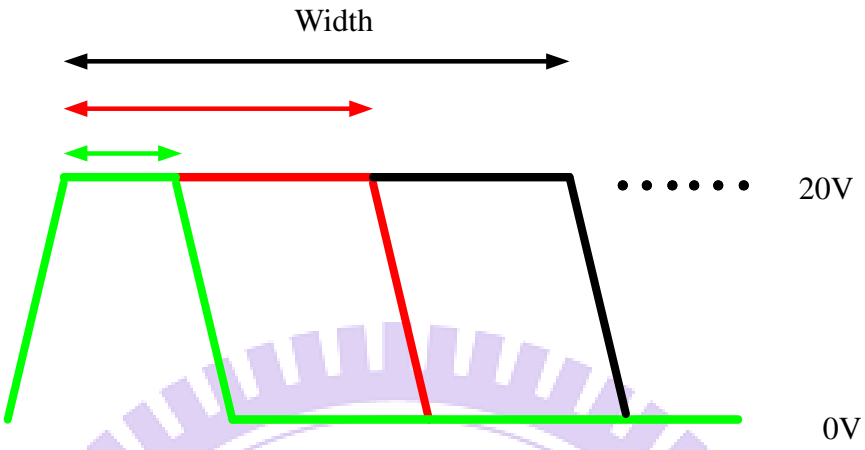


Fig4-8(b) Larger duty ratio has larger pulse width

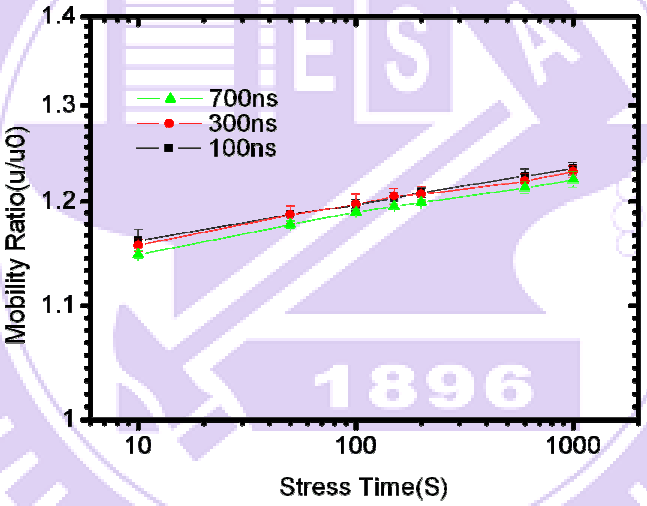


Fig4-9 Degradation behavior under different rising time

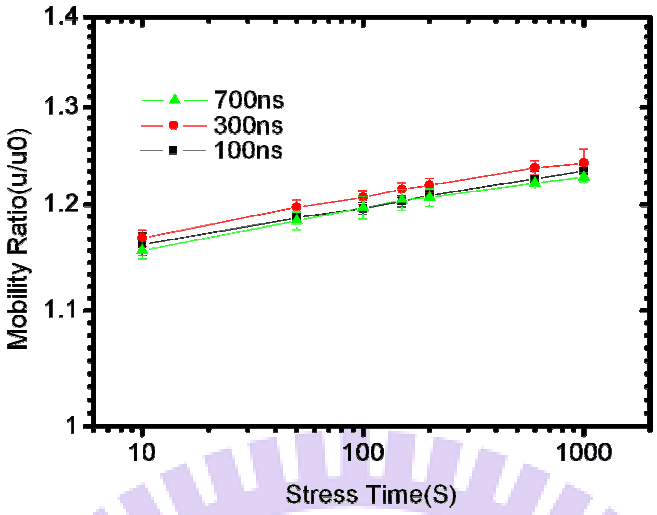


Fig 4-10 Degradation behavior under different falling time

4.1.3 Discussion

Table 4-2 is the summary of waveform parameters for N and P-type TFT. For P-type TFT, degradation rate has dependence on signal range. Mobility behavior is ambiguous in other waveform parameters. We guess it is because the coulomb blockade in channel shortening effect makes the behavior ambiguous. So we want to focus on the obvious degradation behavior in N-type TFT.

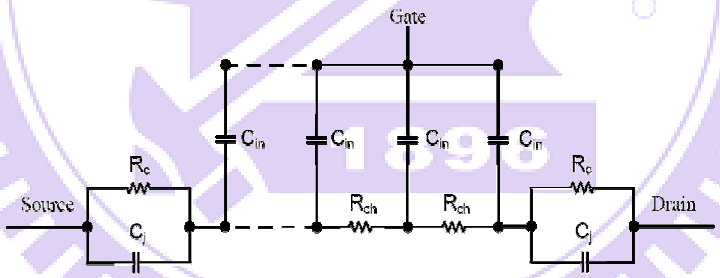
Items	Range	Frequency	Duty	TR	TF
N-type TFT	μ ↘ as Range ↗	μ ↘ as Frequency ↗	μ ↘ as Duty ↗	μ ↘ as TR ↘	μ ↘ as TF ↘
P-type TFT	μ ↗ as Range ↗	μ behavior ambiguous			

Table 4-2 Summary of waveform parameters for N and P type TFT

4.2 RC charge and discharge model

4.2.1 Behavior of charge and discharge

In order to explain the parameter dependence of degradation behavior, we use RC charge and discharge concept in TFT. Fig4-11 shows the voltage cross junction under dynamic operation. First period is rising time period when signal is from zero to -20V. The signal voltage would across on junction so we can see the peak in the end of rising time. As signal stays at -20V, capacitor is starting charging, junction voltage would gradually decrease till falling time. During falling time, junction voltage would change rapidly to a positive peak (capacitor voltage) because of the signal jumps from -20V to zero. After falling time, capacitor starts to discharge, so the junction voltage drops. Because the junction is forward biased now, discharge current would be large and junction voltage would drop rapidly. We try to use this concept to explain the relation between degradation behavior and waveform parameters.



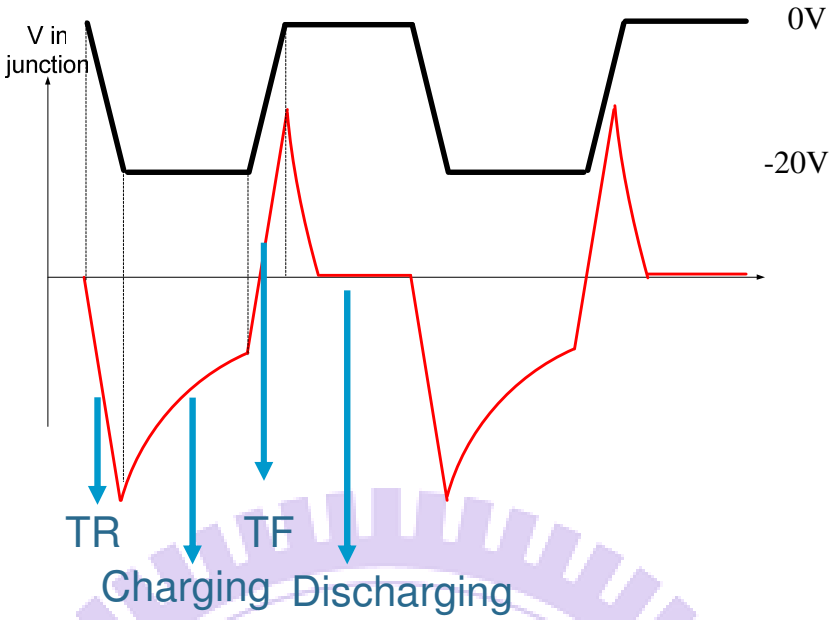


Fig4-11 Voltage in junction under dynamic operation

4.2.2 Parameters dependence

According to this concept, we know when voltage of signal is larger, the amplitude of junction voltage would be larger too. As the result, the degradation of device would be worse.(Fig4-12)

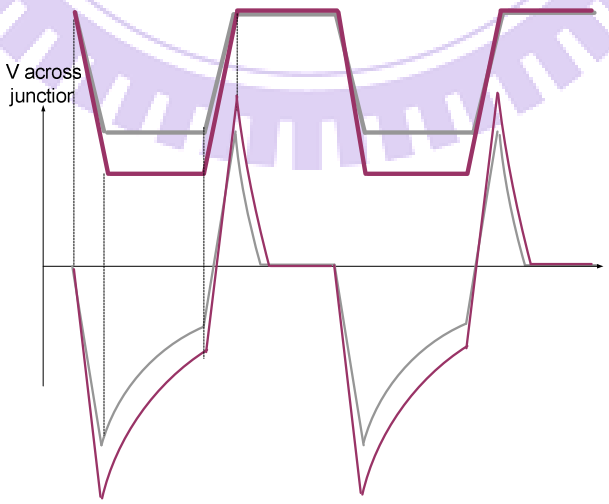


Fig4-12 Larger Vg range, larger junction voltage amplitude

Larger signal frequency means more repetitions of impulse in Fig4-13. Therefore, the degradation rate of device will be larger when frequency increases.

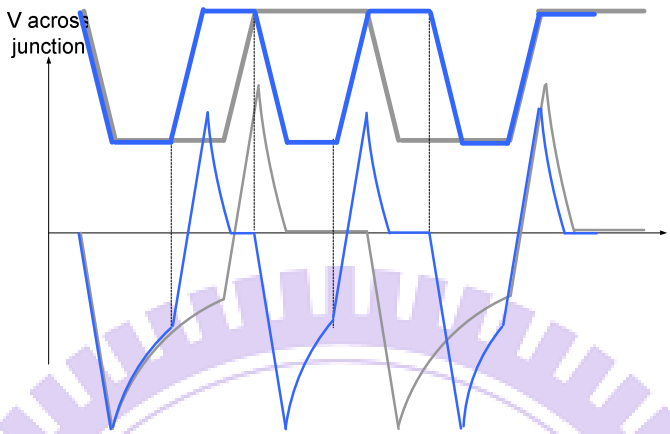


Fig4-13 Larger frequency, more repetitions of impulse

We can see the effect when signal has larger duty ratio in Fig4-14, it means capacitor would charge longer and junction voltage would remain longer while signal level is -20V. Carriers in the junction could have larger kinetic energy. In addition, longer charging time means junction voltage would be closer to zero compared to smaller duty ratio, the peak junction voltage would be larger in the period of falling time. This would also result worse degradation.

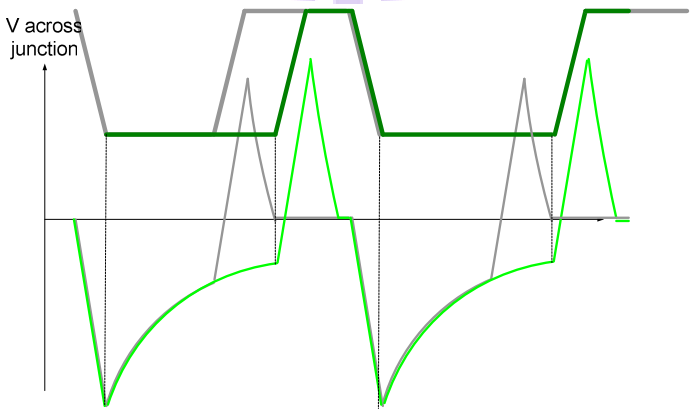


Fig4-14 Larger duty ratio of stress sigal

Longer rising time in RC charge and discharge model will have lower peak of junction voltage during rising time shown in Fig4-15. We would get smaller degradation rate when the rising time is longer.

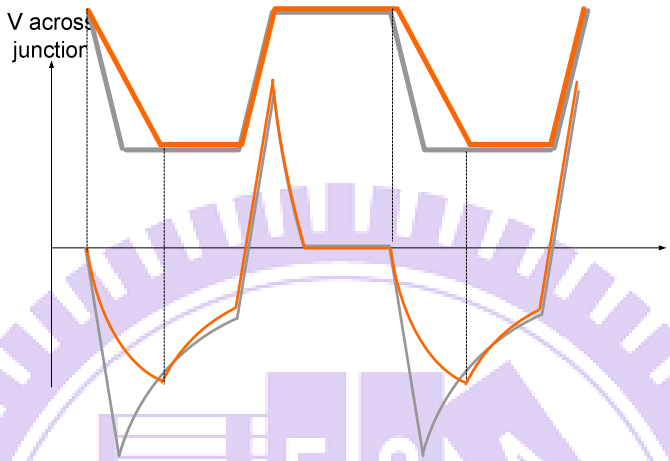


Fig4-15 Larger rising time

It is also true for longer falling time shown in Fig4-14. Longer falling time means lower peak of junction voltage during AC signal's falling time. The degradation rate also becomes lower.

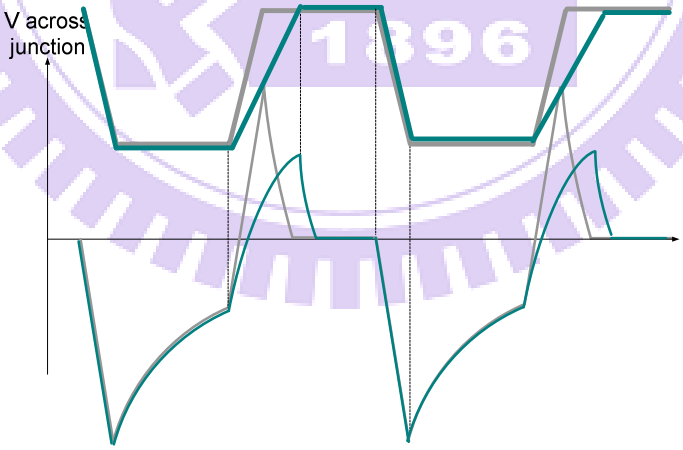


Fig 4-16 Lower falling time

4.2.3 Other parameters

The parameter dependence could be well explained by using our RC charge and discharge circuit concept. We try other experiments to verify our concept. We change the pulse width first shown in Fig4-17. Longer pulse width means larger duty ratio as we discussed in previous section. Based on our idea, junction voltage would gradually drop to zero during the charging time, so at specific pulse width, the junction voltage would be zero. And if you change larger pulse width, the junction voltage would still be zero. It means the degradation rate of device would not be worse when pulse width is larger than this specific one. As we expected, in experiment we find that the degradation rate no longer change when pulse width larger than 3900ns(see the right figure).

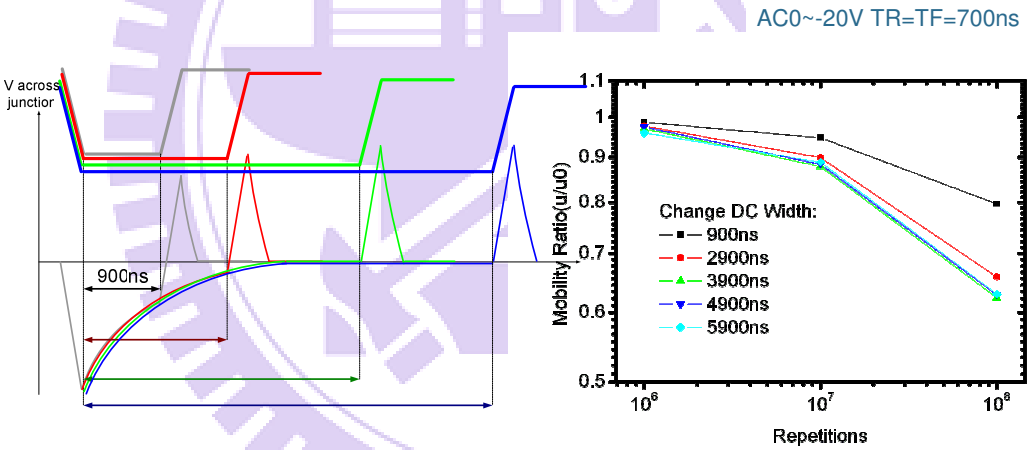


Fig4-17 Degradation rate with different pulse width

We mentioned that junction voltage would drop rapidly to zero after falling time because the junction is forward biased. So if we change longer W2 (Fig4-18), the junction voltage would still remain zero. The degradation rate of device would not change while we use longer W2. The experimental result shows what we expect; the degradation rate is the same among three different W2 at the same pulse repetitions.

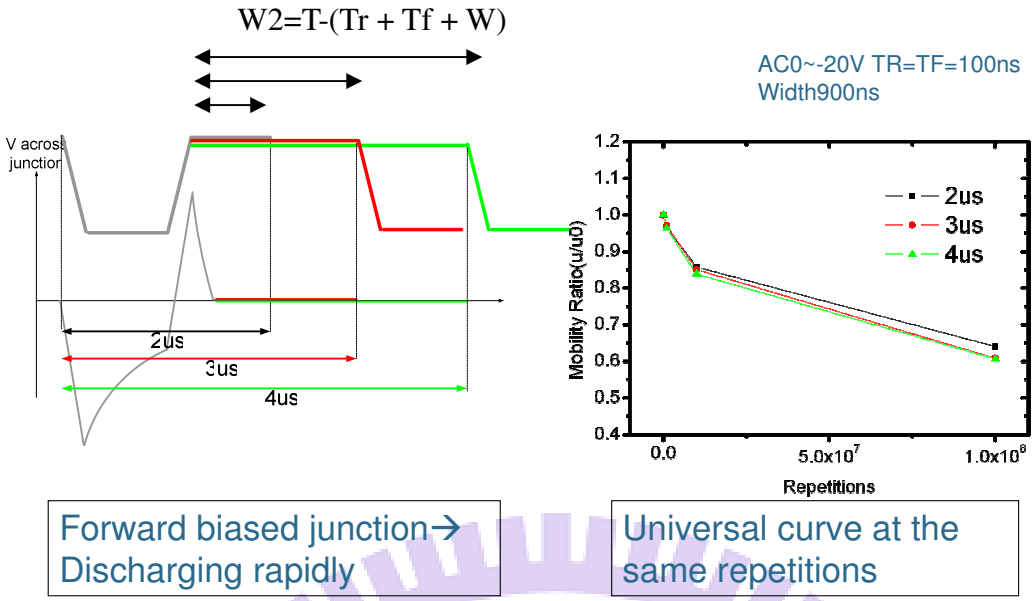


Fig4-18 Degradation rate with different W2

In capacitor discharging period, because the junction is forward biased, there is a large stress current. More precisely, there are a large current and a large electric field at junction. If we offset the pulse signal, make it shift 10V downward, and the peak of junction voltage during falling time period would be negative. At this time, the junction would have smaller stress current and would have smaller degradation rate. In experimental results, the degradation rate of vg range -10V~-30V is smaller than vg range 0~-20V. The results fits our idea.

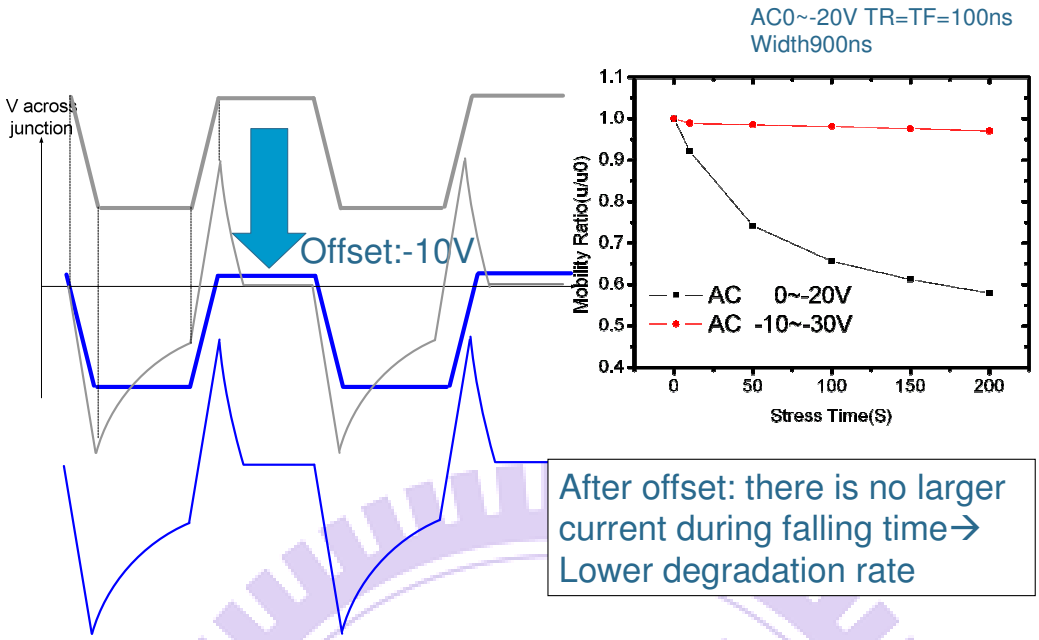


Fig4-19 Degradation rate with different impulse signal

4.2.4 Discussion

Although we can not know precise value of resistance and capacitor in the TFT, and it is also difficult to probe the electric field under dynamic operation because the oscilloscope has no large impedance. In this section, we try to explain the parameter dependence of degradation behavior by using the concept of RC charge and discharge model. And we also consider other parameters (different pulse width, W2 and DC offset) to examine our idea. The experiment results are consistent with our ideas. We think it is a good step in the study of dynamic operation.

Chapter5

Conclusion and Future work

In this thesis, we discussed Poly silicon TFTs under off region dynamic operation. By comparing to similarity of the other stress conditions, we find the degradation behavior is from large electric field at junction. We can call these degradation “hot carrier effect”. In order to know the details of device under dynamic operation, we consider many waveform parameters and compare its dependence of degradation behavior. And we propose a concept of charge and discharge behavior in RC circuit and try to explain the dependence in these experiments. It is important to know the degradation behavior under off region dynamic operation, because most of time, device is under off region stress. We recommend engineer should take drain engineering to enhance reliability.

In the future, we would like to establish a “degradation index” in which there are specific values of electric field and stress current. We want to discussion the relation between degradation rate and these values. By using degradation index, we may evaluate the life device time under dynamic operation and clarify the whole map of degradation mechanism of TFT. These would be the issues which we can work on in the future days.

Reference

[1] J. G. Blake, J. D. III Stevens, and R. Young, “ Impact of low temperature polysilicon on the AMLCD market,” Solid State Tech., vol.41, pp.56-62,1998

[2] Y. Matsueda, T. Ozawa, M. Kimura, T. Itoh, K. Kitwada, T. Nakazawa, H.Ohsima, “A 6-bit-color VGA low-temperature poly-Si TFT-LCD with integrated digital data drivers,” in SID Tech. Dig., pp.879-882, 1998 films,” Phys. Rev. Lett., vol. 25, no.8, pp.509-511, Aug. 1970.

[3] Y. Aoki,T. Lizuka, S. Sagi, M. Karube, T.Tsunashima, S. Ishizawa, K. Ando, H. Sakurai, T. Ejiri, T. Nakazono, M.Kobayashi, H. Sato, N. Ibaraki, M. Sasaki, and N. Harada, ”A 10.4-in. XGA low-temperature poly-Si TFT-LCD for mobile PC application,” in SID Tech. Dig., pp.176-179, 1999

[4] H. J. kim, D. kim, J.H. Lee, I.G. Kim, G. S. Moon, J. H. Huh, J. W. Huang, S. Y. Joo, K.W. Kim, and J.H. Souk, “A 7-in. full-color low-temperature poly-Si TFT-LCD,” in SID Tech. Dig., pp.184-187, 1999

[5] Kiyoshi Yoneda, Hidenori Ogata, Shinji Yuda, Kohji Suzuki, Toshifumi Yamaji, Shiro Nakanishi, Tsutomu Yamada, and Yoshiro Morimoto, “Optimization of low-temperature poly-Si TFT-LCDs and a large-scale production line for large glass substrates,” Journal of the SID, vol.9, pp.173-179, 2001

[6] Yasuhisa Oana, “Current and future technology of low-temperature poly-Si TFT-LCDs,” Journal of the SID, vol.9, pp.169-172, 2001

[7] Jun Hanari, “Development of a 10.4-in. UXGA display using low-temperature poly-Si technology,” Journal of the SID, vol.10, pp.53-56, 2002

[8] Mutsumi Kimura, Ichio Yudasaka, Sadao Kanbe, Hidekazu Kobayashi, Hiroshi Kiguchi, Shun-ichi Seki, Satoru Miyashita, Tatsuya Shimoda, Tokuro Ozawa,

Kiyofumi Kitawada, Takashi Nakazawa, Wakao Miyazawa, and Hiroyuki Ohshima, “Low-temperature polysilicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display,” IEEE Trans. Electron Devices, vol. 46, pp2282-2288,1999.

[9] Mark Stewart , Robert S. Howell, Leo Pires, Mitiadis K. Hatakis, Webster Howard, and Olivier Prache, “Polysilicon VGA active matrix OLED display-technology and performance,” in IEDM Tech. Dig.,1998,pp.871-874

[10]Mark Stewart , Robert S. Howell, Leo Pires, Mitiadis K. Hatakis, Webster Howard, and Olivier Prache, “Polysilicon VGA active matrix OLED display-technology and performance,” IEEE Trans. Electron Devices, vol. 48, pp845-851,2001

[11] Tatsuya Sasaoka, Mitsunobu Sekiya, Akira Yumoto, Jiro Yamada, Takashi Hirano, Yuichi Iwase, Takao Yamada, Tadashi Ishibashi, Takao Mori, Mitsuru Asano, Shinichiro Tamura, and Tetsu Urabe, “A 13.0-inch AM-OLED display with top emitting structure and adaptive current mode programmed pixel circuit (TAC),” in SID Tech. Dig., pp.384-387, 2001

[12] Zhiguo Meng, Haiying Chen, Chengfeng Qiu, Hoi S. Kwok, and Man Wong,” Active-matrix organic light-emitting diode display implemented using metal-induced unilateral crystallized polycrystalline silicon thin-film transistors,” in SID Tech. Dig., pp.380-383, 2001

[13] Zhiguo Meng and Man Wong,” Active-matrix organic light-emitting diode displays realized using metal-induced unilateral crystallized polycrystalline silicon thin-film transistors,” IEEE Trans. Electron Devices, vol. 49, pp991-996,2002

[14] G. Rajeswaran, M. Itoh, M. Boroson, S. Barry, T. K. Hatwar, K. B. Kahen, K. Yoneda, R. Yokoyama, T. Yamada, N. Komiya, H. Kanno, and H. Takahashi, “Active matrix low temperature poly-Si TFT/OLED full color

displays:development status," in SID Tech. Dig., pp.974-977, 2000

[15] H. Kuriyama, T. Okada, M. Ashida, O. Sakamoto, K. Yuzuriha, K. Tsulsumi, T. Nishimura, K. Anami, Y. Kohno, and H. Miyoshi, "An asymmetric memory cell using a C-TFT for ULSI SRAM," Symp. On VLSI Tech., pp.38, 1992

[16] T. Yamanaka, T. Hashimoto, N. Hasegawa, T. Tanala, N. Hashimoto, A. Shimizu, N. Ohki, K. Ishibashi, K Sasaki, T. Nishida, T. Mine, E. Takeda and T. Nagano, " Advanced TFT SRAM cell technology using a phase-shift lithography," IEEE Trans. Electron Devices, vol. 42, pp1305-1313,1995

[17] S. D. S. Malhi, H. Shichijo, S. K. Banerjee, R. Sundareson, M. Elahy, G. P. Pollack, W. Richarson, A. H. Sha, L. R. Hite, R. H. Womark, P. Chatterjee, and H. William, " Characteristics and three-dimension integration of MOSFETs in a small-grain LPCVD polycrystalline silicon," IEEE Trans. Electron Devices, vol. ED-32, no.2, pp258-281, 1985.

[18] Kaustav Banerjee, Shukri J. Souri, Pawan Kapur, and Krishna C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and system-on-chip integration," Proceedings of the IEEE, vol. 89, pp.602-633,2001

[19] H. J. Kim and J. S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin film transistors," Appl. Phys. Lett., vol.68, pp.1513-1515,1996

[20] M. Cao, S. Talwar, K. Josef Kramer, T. W. Sigmon, and K. C. Saraswat, "A high-performance polysilicon thin-film transistor using XeCl excimer laser crystallization of pre-patterned amorphous Si films," IEEE Trans. Electron Devices, vol. 43, pp561-567,1996.

[21] J. H. Jeon, M. C. Lee, K. C. Park, and M. K. Han, "A new polycrystallines silicon TFT with a single grain boundary in the channel," IEEE Electron Device

Lett., vol. 22,pp.429-431,2001.

[22] Y.-H. Tai, S.-C. Huang, C. W. Lin, and H. L. Chiu, "Degradation of the Capacitance-Voltage Behaviors of the Low-Temperature Polysilicon TFTs under DC Stress," Journal of The Electrochemical Society, Vol. 154, No. 7, pp. 611-618, 2007

[23] Y. Uraoka IEEE02,03,04,07

[24] Ibid 23

[25] Degradation of the Capacitance-Voltage Behaviors of the Low-Temperature Polysilicon TFTs under DC Stress, ECS 2007,YHTai

[26] Y. Uraoka 2002 JJAP

[27] Y. Uraoka, JJAP2002; Y.H. Tai ECS 2007.

[28] S.M.SZE, 1998.