國 立 交 通 大 學

電子工程學系　電子研究所

博 士 論 文

低溫製程技術應用於動態隨機存取記憶體之鈦酸鍶鋇
薄膜電容器之研究

Low-Temperature Processing Techniques Applied on Barium Strontium Titanate Films for the Applications of DRAM Storage Capacitors

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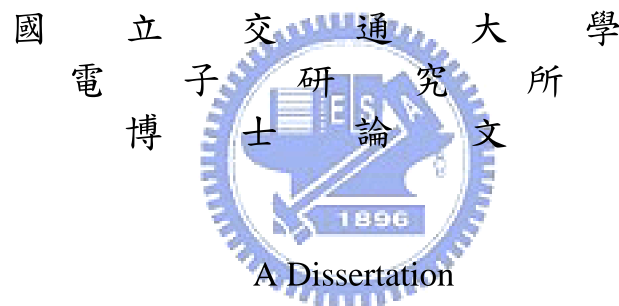

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事由：　推薦電子研究所博士班研究生史德智提出論文並參加國立交通大學博士論文口試。

說明：　電子研究所博士班研究生史德智先生，業已修畢部訂所需學分，通過博士資格考之學科考試，並完成博士論文初稿之撰寫，論文名稱為：「低溫製程技術應用於動態隨機存取記憶體之鈦酸鍶鋇薄膜電容器之研究」。博士論文內容中已有數篇期刊論文、會議論文及專利發表，同時尚有數篇論文投稿中，準備發表於學術期刊。茲列舉如下：

Journal Papers

1. **Der-Chi Shye,** Bi-Shiou Chiou, Ming-Jiunn Lai, Chuan-Chou Hwang, Cheng-Chung Jaing, Jyh-Shin Chen, Ming-Hwu Cheng, and Huang-Chung Cheng, " Low-Temperature Radio-Frequency-Sputtered (Ba, Sr)TiO_3 Films on Pt/TiN/Ti/Si Substrates with Various Oxygen/Argon Mixing Ratios", Journal of The Electrochemical Society, vol. 150(2) p. F20-F27, 2003.
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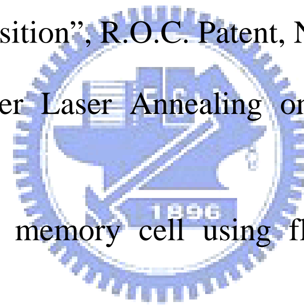
2. "Methodologies of Excimer Laser Annealing on DRAMs' Capacitors", R.O.C. Patent, No. 137418.



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史德智先生已具備交通大學電子研究所應有之教育及訓練水準，特以推薦參加博士論文畢業口試。

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邱 碧 秀 博士

低溫製程技術應用於動態隨機存取記憶體之鈦酸鍶鋇薄膜電容器之研究

研究生：史德智　　　　　　　　　　　　指導教授：邱碧秀 教授

國立交通大學

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摘 要

本論文將研究以先進低溫製程技術製備之鈦酸鍶鋇((Ba, Sr)TiO_3, BST) 薄膜電容器之特性。本研究中，Pt/TiN/Ti/Si 基板被應用於所有的樣本上，用以模擬動態隨機存取記憶體 (DRAM) 之 capacitor over bit-line (COB) 結構。

本實驗使用雙靶射頻磁控濺鍍系統在低基板溫度下 (<450°C)來成長鈦酸鍶鋇(BST)薄膜電容器。環境氣體壓力、濺鍍鎗功率和氧氣/氬氣混合比 (O_2/(Ar+O_2) mixing ratio, OMR)為此鈦酸鍶鋇薄膜製備過程之主要參數。電氣特性與材料特性分析顯示濺鍍環境氣氛之氧氣/氬氣混合比 (O_2/(Ar+O_2) mixing ratio, OMR)扮演最重要的角色。電漿光譜顯示 BST 薄膜之成長速度和品質將被 OMR 之值所嚴重影響，而在 5% OMR 之下可以得到薄膜之最高介電常數值。較高之 OMR 可提升時間相對之介電崩潰限度(TDDB)，換言之、即 BST 薄膜之可靠度因為薄膜中氧空缺補償之故而大幅提升。此外導電電流分析顯示在高電場下 Pt/BST/Pt 薄膜之導電機制將被 Poole-Frenkel emission (PF) 所主導，而低電場下則為蕭特基發射(Schottky

emission, SE) 所主導，當 OMR 增加時蕭特基發射之機制影響亦增加。在本文中將以能帶圖來分析探討此導電電流機制。

BST 薄膜於極低溫沉積完成後，低溫後處理將被應用於改善薄膜之品質。應用 248nm 波長之 KrF 準分子雷射(ELA) 於低基板溫度 300°C 下對此薄膜進行熱處理，以強化此膜之結晶性與電介質特性。實驗結果顯示結晶特性及電介特性將被顯著地強化。光學及熱傳分析顯示 BST 薄膜對 248nm 波長之準分子雷射之光吸收深度只有 20nm，因此下層電極和元件將不會被此製程所損傷。雖然準分子雷射能於 BST 陶瓷薄膜之上表面進行快速有效的”淺層加熱”，但卻也容易破壞薄膜表面、形成大量之氧空缺，因之漏電流也隨之上升。此外、薄膜之優選晶向也會被雷射熱處理所影響，卽處理完後由 (mm0) 轉變成 (m00) 與 (mmm)，此將影響薄膜之光學與高頻電性。製程參數中，入射能量、薄膜厚度，基板組成結構和溫度都會明顯地影響此雷射熱處理之效能。

在氬離子環境中濺鍍與 ELA 處理所造成之 BST 表面氧空缺損傷會引起高的漏電流。本實驗使用氧氧離子電漿 (oxygen plasma) 後處理來改善此現象。氧離子電漿後處理可有效地鈍化與補償薄膜表面之氧空缺以降低漏電流，並提高薄膜之可靠度。但電漿處理時間過長將會引起電漿損傷，所以時間與入射能量等參數必須被謹慎地控制。

此外、超薄奈米尺度之鉻金屬夾層被應用於鈦酸鍶鋇薄膜電容器上，形成 BST/nano-scaled Cr/BST 之三明治夾層事之結構。此三明治夾層結構可以大幅降低漏電流與增強電容與色散特性之熱穩定性，這些有趣的特性將十分有助於實際 DRAM 電容器之元件整合與應用規範需求。實驗結果顯示漏電流與熱穩定性與鉻金屬夾層之厚度呈相依函數之關係，且 2nm 厚度之鉻金屬夾層可得最低漏電流。此外，在不同操作溫度下(室溫到 150°C)的溫度電容係數(Temperature coefficient of

capacitance, TCC) 由單層 BST 電容 400nm 之 35% 降至 BST(200nm)/Cr(2nm)/BST(200nm) 三明治複合多層電容之 5%以下。微觀分析指出非理想介面之散射行為、異常空間電荷場形成與金屬氧化物串接電容為此低電流與熱穩定性之形成機制。

透過低溫製程技術之整合，鈦酸鍶鋇(BST)薄膜電容元件將可成為 Giga-bit 世代 DRAM 電容器之最佳候選元件。本文中將綜合結論鈦酸鍶鋇薄膜電容器之最佳特性可由製程參數控制、後處理方法應用與特殊多層膜結構之整合而得到完全低溫低熱預算之製程技術。

Low-Temperature Processing Techniques Applied on Barium Strontium Titanate Films for the Applications of DRAM Storage Capacitors

Student: Der-Chi Shye Advisors: Dr. Bi-Shiou Chiou

Abstract

The characteristics of (Ba, Sr)TiO_3 thin films, prepared by novel techniques of low temperature treatments, were systematically studied in this thesis. Pt/TiN/Ti/Si substrates were applied on each sample to simulate the real capacitor over bit-line (COB) structure of dynamic random access memory (DRAM).

(Ba, Sr)TiO_3 (BST) films were sputtered by radio frequency (RF) magnetron system with dual targets at low substrate temperature, lower than 450°C (340°C at sample surface), and the effects of the process parameters were also investigated. The work pressure, the sputtering gun power and the gas-mixing ratio are the important parameters in the BST film deposition. Material analyses and electrical testing show that the low temperature BST films are significantly affected by those process parameters. The O_2/(Ar+O_2) mixing ratio (OMR) is a most critical parameter during BST film sputtering. Plasma emission spectra indicate that the deposition rate declines at a higher OMR due to oxide formation on the target surface. The dielectric constant of

the BST films can reach a maximum of 364 at 5% OMR. The ten-year lifetime of the time-dependent dielectric breakdown (TDDB) implies that the reliability of the capacitor can be enhanced at a higher OMR due to the compensation of oxygen vacancies and smaller grain sizes. Current-voltage analysis indicates that the leakage current of the Pt/BST/Pt capacitor is limited by Schottky emission (SE)/Poole-Frenkel emission (PF) at a lower/higher applied field, accordingly. The applied field boundary between SE and PF shifts toward higher field as OMR increases. Moreover, an energy-band model was proposed and this leakage mechanism was also discussed.

Post low-temperature treatments were applied on the BST films to further improve their crystallinities and electrical properties. A novel process, KrF excimer laser annealing (ELA) at the wavelength of 248 nm, had been undertaken to implement BST films at a process temperature of 300° C to avoid the steep thermal gradient in thin films. The dielectric constant of the amorphous (α) BST film was remarkably enhanced from 80 to over 250 after ELA treatment. The optical testing and the heat conduction analyses indicate that the underlayer films and devices cannot be damaged during ELA treatment due to a very shallow light absorption depth (20 nm) of the BST film at the wavelength of 248-nm. Besides, the laser energy fluence and film thickness greatly influence the thermal conduction and the temperature distribution within the BST films. In the meanwhile, the as-deposited films revealed (mm0) preferred orientation, and, intriguingly, the preferred orientations changed into (m00) and (mmm) after ELA treatments. The optical and the high frequency properties may be affected by this preferred-orientation change. However, although the ELA can perform "shallow-depth annealing" for BST thin film, the degradation of upper surface is strongly influenced by

the laser energy fluence. Hence, the leakage current will be significantly affected by the energy fluence of the laser.

The leakage current of the ferroelectric film increases after sputtering process and post ELA treatment, but post oxygen plasma treatment can effectively improve the BST film surface to suppress the leakage at low processing temperature of 250°C. According to the analysis results in this thesis, the oxygen plasma treatment can effectively passivate the oxygen vacancies of BST films, decreasing the leakage currents. The leakage current can be reduced as many as two orders of magnitude under proper control of plasma conditions. The characteristics of the dielectric reliability, TDDB, can be also improved by this treatment due to the compensation of the surface oxygen vacancies.

In addition, a nano-scaled chromium (Cr) layer is applied onto (Ba, Sr)TiO_3 (BST) thin film capacitor as an inter-layer to enhance thermal stability of capacitance and suppress leakage current. Temperature coefficient of capacitance (TCC) using this BST/Cr/BST (200nm/2nm/200nm) multifilm can achieve 30% lower than that using BST mono-layer (400nm) film. Besides, the leakage current can be also greatly suppressed by applying this nano-scaled Cr layer onto BST thin film capacitor. TCC and leakage current behave as functions of Cr thickness, so the optimal properties can be obtained with the Cr thickness of 2nm. Microstructure analysis suggests that the interfacial continuity strongly influences the TCC and leakage property due to scattering centers and series capacitance formed at imperfect interface. The correlated mechanisms between electric and material properties are systematically investigated in this work.

BST thin film can be the most promising candidate for Giga-bit generation cell

capacitor, because the low temperature processes can be compatible to the IC's integration. In this thesis, the optimal properties of the BST films can be obtained by adjusting process parameter, applying post treatments and using thermal stabilization structures to achieve thorough low-temperature processes.

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Chapter 1

Introduction

1-1 *Challenges of Advanced BST Cell Capacitors*

1-1.1 BST capacitors applied on advanced DRAM cells

Since the dynamic random access memory (DRAM) with one-transistor and one-capacitor (1T1C) cell was invented in the late 1960s [1], the DRAM technology has progressed at a rapid pace in the past decades. In the past 20 years, the chip density has been quadrupled every three years, and the chip size is 1.5X bigger than that of previous generation. Therefore, three-dimensional (3-D) cell structure has been widely introduced into high-density DRAM cells, and Figure 1-1 shows a typical 3-D cell with capacitor-over-bit line (COB) structure [2].

The stacked cell with COB structure can easily integrate with non-silicon-dioxide

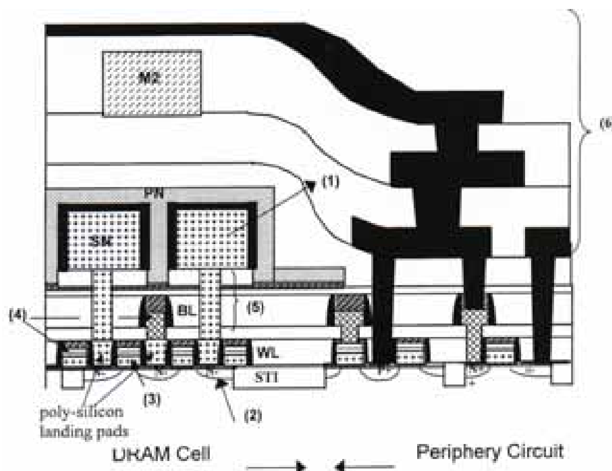


Figure 1-1 The schematic representation of typical COB stacked cell. (1) storage node, (2) storage node junction, (3) cell transistor, (4) world line interconnection, (5) metal or silicide plug and (6) metallized interconnection and dielectric isolation layers [2].

DRAM Generation	Lithography (μm)	Cell Area (μm^2)	Device Voltage (V)	Cell Capacitance (fF)	Equivalent Oxide Thickness, t_{ox} (nm)	Maximum Capacitor Voltage, V_{BLH}, V_{WLL}=0 (V)
1Mbit	1.00	30.00	**5.0**	**35-40**	8.8	2.7
4Mbit	0.80	10.00	5.0	35	8.8	2.7
16Mbit	0.50	3.50	3.3	**30-35**	6.6	1.8
64Mbit	0.35	1.30	3.3	30	6.6	1.8
128Mbit	0.25	0.75	2.5	**25-30**	5.0	1.2
256Mbit	0.18	0.25	2.5	25	5.0	1.2
512M~1G bit	0.13	0.11	1.8	25	3.6	0.7
4Gbit	0.10	0.07	1.5	**>25**	3.0	0.4
16Gbit	0.07	0.03	1.2	**>25**	2.4	0.3
32Gbit	0.045	0.012	1.0	**>25**	2.0	0.25

Table 1-1 DRAM device requirements and overall technology trend.

materials and provide large capacitor area, but there are still many critical requirements for the capacitor scaling down, as listed below [3].

(1) *Sufficient capacitance for cell operation:* Both of increasing cell area and using high-dielectric materials can enhance the cell capacitance. However, the planar dimensions of capacitors and stacked height must be severely constricted due to cell size shrunk of new generation requirements [4, 5]. Therefore, the high dielectric materials must be necessary for advanced capacitor applications.

(2) *Low leakage-current/dielectric ratio for data retention:* The data retention time is one of the most important parameters for DRAMs' applications. The data retention time is the period of the stored data lost owing to the leakage current before data refreshing, and that has to be doubled as the memory density increases 4X in every new generation [6]. Therefore, the node leakage must be improved to obtain a better data retention property.

(3) *Plenty of manufacturing resources and mature technologies for CMOS-IC processes:*

Medium dielectric constant materials			
Dielectric	ε_r	**Ccrit (fF μm^{-2})**	**Note**
SiO_2	3.9	25	
Si_3N_4	7	7 ~ 10	
Ta_2O_5	25 ~ 50	12 ~ 20	
TiO_2	30 ~ 40	10	
ZrO_2	14 ~ 30	10	
Nb_2O_3	30 ~ 100	-	
Y_2O_3	15 ~ 20	5	
(Ba, Sr)TiO_3 (BST)	300 ~ 800	40 ~ 120	Paraelectric Phase
(Pb, La)(ZrTi)O_3 (PLZT)	~1400	80 ~ 90	Ferroelectric Phase

Table 1-2 Comparisons of the relevant properties for various dielectrics

In practical applications, cost and production feasibilities are the key concerns for the developments of new generation technologies. The mature techniques, such as CVD and PVD, used for thin film fabrications can easily satisfy those targets of the cost reduction and the feasibility concerns. Especially, the fabrication cost will be incredibly huge for the generation scaled down to nano-order, so plenty of manufacturing resources will become very high priority for the new technology developments.

(4) *Performing excellent reliability to satisfy the qualification criteria in practical applications:* The qualification criteria become more and more severe for new generation IC chip due to the crucial requirements in high-speed, low power and embedded memory integrated into a system-on-chip (SOC). For instance, according to the industrial standards, the operation junction-temperatures for DRAMs' applications and qualification spec range from –0 °C to 120°C (ambient temperature ranging from –40~85 °C for consumer IC), so the thermal stabilities of the electrical properties become the very critical concerns for the device developments and

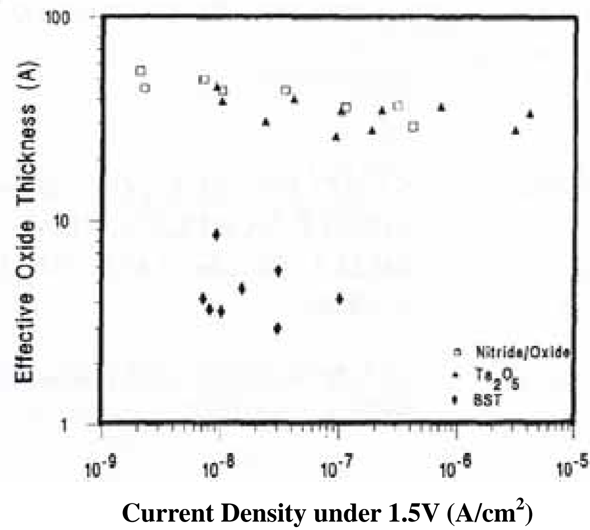


Figure 1-2 Comparisons of N/O, $Ta2O_5$ and BST performance [22].

applications.

The requirements of the DRAMs' cells from 1Mbit to 64Gbit are summarized in Table 1-1, which was further modified by the information of ITRS 2003 and IBM Res. [7, 8]. This technology roadmap reveals the high dielectric materials applied on cell capacitor is indeed necessary for giga-bit generation DRAM.

(Ba, Sr)TiO_3 (BST) film has been investigated as capacitor's material for giga-bit DRAM applications because of the following reasons.

(1) *Extremely large dielectric constant:* BST has a very large dielectric constant at the high frequency zone for memory operation. Comparing with many high-k dielectrics, BST exhibits unbelievably high dielectric constant in paraelectric phase, as depicted in Table 1-2 [9~11]

(2) *Lower leakage-current/dielectric ratio for data retention:* BST capacitor behaves semi-insulation properties, but the leakage current is still acceptable during refreshing cycle. Figure 1-2 shows the effective oxide thickness versus leakage

current using different high dielectric materials, such as N/O, Ta_2O_5 and BST [22]. Obviously, the effective oxide thickness of the BST is smallest at the same leakage current, that is, BST has best capability for charge storage among such high-k materials. Hence, the BST capacitor possesses excellent property of data retention.

(3) *Compatible materials for CMOS processing:* The film does not contain the harmful elements, such as Na, K and Li, which can greatly degrade the performance of Si transistor.

(4) *Paraelectric phase in operation temperature:* The composition of BST film can be adjusted into paraelectric phase, without spontaneous polarization, at operation temperature, so the film can get rid of fatigue phenomenon.

(5) *Plenty of fabrication resources:* Abundant technologies can be easily applied on this film fabrication, such as sputtering, sol-gel, PLD, CVD etc., so it's easy to find a suitable resource to reduce the cost.

Consequently, according to the above excellent characteristics, BST thin film capacitors are almost able to satisfy the requirements of the new generation cell capacitors, but some of the integration obstacles must be concerned below.

1-1.2 Challenges of BST capacitors integrated with CMOS IC processing

BST is the best candidate of Giga-bit DRAM material, but there are still some challenges for the integrations of CMOS processing.

(1) *CMOS devices deformed by high temperature process:* In general, high temperature (>450°C) deposition of BST films is frequently applied to obtain good crystallinity of a perovskite structure [12, 13], as denoted in Table 1-3 [23 - 34], but the high temperature process may deform the junction profile and alter the gate length of the metal-oxide-semiconductor field-emission-transistor (MOS-FET), especially on the deep submicron scale. In stacked-capacitor (STC) structure, the MOS-FET dopant is always implemented prior to the capacitor fabricated, which needs to be fabricated at low temperature to avoid the damage of the MOS-FET.

(2) *Difficult electrode formation of BST capacitor:* Usually, there is serious inter-diffusion between dielectrics and silicon during the deposition of dielectrics. A thermally and electrically stable diffusion barrier is needed to prevent inter-diffusion,

BST samples prepared by various techniques

Deposition Technologies	Post Treatments	Low Temperature Process Anounced?	Compositions	Substrates	Film Thickness (nm)	Dielectric Constant	Reference
RF-sputtering (660°C)	n/p	no	$(Ba_{0.75}, Sr_{0.25})TiO_3$	$Pt/SiO_2/Si$	30	250	[23]
RF-sputtering (640~660°C)	n/p	no	$(Ba_{0.5}, Sr_{0.5})TiO_3$	$Pt/SiO_2/Si$	20	320	[24]
RF-sputtering (500~550°C)	n/p	yes	$(Ba_{0.4}, Sr_{0.6})TiO_3$	$LNO/Pt/Ti/SiO_2/Si$	80	250	[25]
ECR-sputtering (200°C)	Microwave (300°C) *1	yes	$SrTiO_3$	$Pt/Ti/SiO_2/Si$	200	260	[26]
CVD (400°C)	Furnace Annealing (700°C)	yes	$(Ba_{0.6}, Sr_{0.4})TiO_3$	$Pt/TaOx/SiO_2/Si$	30	170	[27]
CVD (400°C)	Furnace Annealing (600°C)	yes	$(Ba_{0.6}, Sr_{0.4})TiO_3$	SRO	10	< 260	[28]
LSCVD (500°C)	n/p	no	$(Ba_{0.5}, Sr_{0.5})TiO_3$	$Pt/Poly\text{-}Si/SiO_2$	35~200	300	[29]
ECR-CVD (450°C)	RTA (700°C)	yes	$(Ba_{0.5}, Sr_{0.5})TiO_3$	$Pt/TaO_x/Si$	61	220	[30]
Sol-gel (RT)	Furnace Annealing (700°C)	no	$(Ba_{0.5}, Sr_{0.5})TiO_3$	Si	250	435	[31]
MOD (RT)	Furnace Annealing (750°C)	no	$(Ba_{0.7}, Sr_{0.3})TiO_3$	Pt/Ti/Si	140	480	[32]
PLD (700°C) *2	n/p	no	$(Ba_{0.6}, Sr_{0.4})TiO_3$	$Pt/Ti/SiO_2/Si$	200~400	450~600	[33]
PLD (400°C) *2	ELA(400°C)	yes	$BaTiO_3$	Pt/Ti/Si	250	150~1200	[34]

*1: Microwave treatment behaves low substrate temperature, but high thermal budget. Besides, this technique may damage the underlayer due to bump heating.

*2: PLD technology behaves bad uniformity for practical applications.

n/p: not performed

Table 1-3 Comparisons of various technologies for BST films deposited at different conditions.

and it also cannot be oxidized during high temperature processes with O_2 ambient.

(3) *Leakage current increasing after thermal cycles or Ar/N_2 plasma processing:* The leakage current of the BST film would be greatly increased after post annealing or ion sputtering process [1.14~1.17]. Although the dielectric properties can be greatly enhanced, the increased leakage current will result in the degradation of the data retention.

(4) *Dramatic variations of the dielectric properties for the device operating in various temperatures:* The dielectric constant and the conduction current can decrease about 20% and increase 3-order, respectively, while the BST capacitor operates from room temperature to 110°C [18,19]. In industrial criteria, the operation junction-temperatures for DRAMs' applications and qualification spec range from –0 ^{o}C to 120°C (ambient temperature ranging from –40~85 ^{o}C for consumer IC), so the dramatic variations of the electric-temperature properties may cause the deviation of the normal device operation.

Therefore, the thin film technologies of the BST capacitors must overcome the above tough barriers, or it should be impossible to perform the practical DRAM applications.

1-2 Motivation of this Thesis

This thesis dedicated in obtaining excellent characteristics of BST capacitor fabricated by low-temperature novel technologies. The motivation and the major concepts of this study are listed below.

(1) *Optimizing the process controls for BST thin film fabricated at low temperature:* In general, Dual-Gun RF-sputtering-system can reduce the reaction energy than Single-Gun RF-sputtering-system theoretically, so this sputtering technique was applied on BST film fabrication in this thesis, using two individual targets, $BaTiO_3$ and $SrTiO_3$, simultaneously. Although a low temperature technique is required for the deposition of BST in the IC process, controlling the crystallinity and dielectric constant is normally more difficult with a low temperature technique than with a high temperature technique. The process parameters and the electrical mechanisms were systematically studied to obtain the optimal process conditions.

(2) *Enhancing the crystallinity of BST films using the novel post-treatment of ELA technique:* Low temperature prepared BST films always exhibit poor crystallinity, so the films have to be post treated by the annealing process to enhance the crystallinity and dielectric properties. A novel low-temperature technique, using excimer laser annealing (ELA), was introduced in this work due to its very low thermal budget and high crystallization efficiency. In addition, the shallow depth of energy absorption using ELA won't damage the under layer devices. Hence, ELA is an extremely powerful technology to achieve a successful integration process at low temperature. The comparisons of several post treatment technologies are listed in Table 1-4, which shows ELA possesses excellent characteristics for thin film applications. Although ELA technology is widely used for preparing poly-Si thin film in current semiconductor industry, but up to now, very few reports investigate the ELA mechanism for ferroelectric films. Hence, this thesis investigated the effects, the mechanisms and the process window of ELA technique applied on BST

films.

(3) *Suppressing the leakage current using oxygen plasma technique after post annealing:* The leakage current increases after sputtering and post annealing process due to surface damage. Oxygen plasma treatment can effectively improve the surface states, and therefore the leakage current can be greatly reduced because of oxygen vacancies compensation.

(4) *Enhancing thermal stability using the novel sandwich structure of BST/Nano-scaled Cr/BST Multifilm:* The stable properties of the dielectric constant and conducting current are indeed necessary during device operating. The nano-scaled Cr layer was applied onto the BST capacitor to enhance the thermal stability. The electric characteristics and corresponding mechanisms will be systematically discussed in this investigation.

Besides, according to previous studies, the excellent bottom electrodes can be obtained by the formation controls of the Pt/TiN/Ti/Si multilayer films, and the barrier capability of the TiN layer can be largely enhanced by rapid thermal annealing (RTA)

Comparisons of Various Post Treatment Technologies				
	Thermal Budget	Mechanical Stress Releasing	Uniformity	Throughput for Mass Production
RTA	low	bad	good	good
Microwave	high	good	excellent	good
Furnace Annealing	high	excellent	good	excellent
ELA with Optical Scanning System	low	excellent	good	worse *
* The throughput of ELA technique can be improved by equipment modifications				

Table 1-4 Comparisons of various post treatment technologies.

[14, 20, 21]. Therefore, this thesis won't discuss the electrode formation anymore.

1-3 Thesis Organization

This thesis reports how the novel low temperature techniques applied on the BST capacitor fabrications. The structure of Pt/TiN/Ti/Si was proposed as the bottom electrode substrate for BST deposition, simulating the COB capacitor structure of DRAM capacitor in this study. Electrical and material properties are systematically analyzed in this work.

Chapter 2 reports the general background and the literature review of BST thin film capacitors. Lots of works reported the DRAM's new generation trends and developments, low-temperature techniques, mechanisms/applications of BST thin films, obstacles and potential solutions for BST applications.

Chapter 3 presents the details of the experimental concepts and the equipments of this study. The experimental procedures, thin film fabrication processes, electric and material analysis techniques will be introduced in this chapter.

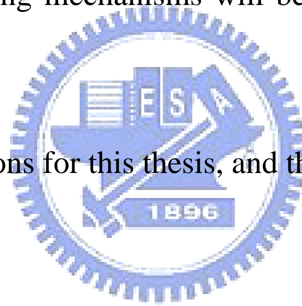
Chapter 4 investigated the characteristics of the low-temperature prepared BST Films. Processing parameters were carefully controlled and studied, and then the experimental results show oxygen/argon-mixing-ration (OMR) plays a most important role in the RF co-sputtering process. The corresponding analysis of the electric and the material properties were performed in this chapter.

Chapter 5 demonstrates the effects of ELA treatment applied on the BST capacitors. The mechanisms of recrystallization were thoroughly analyzed by thermal conduction analysis. Furthermore, the material and the electric analysis show the process window

of the ELA BST film is very hard to control. This chapter thoroughly investigated the ELA processing issues.

Chapter 6 presents the post treatment using oxygen plasma applied on the BST/Pt/TiN/Ti/Si multilayer films. The great enhancement of leakage suppressing can be achieved, and the corresponding mechanisms were studied.

Chapter 7 demonstrates a novel sandwich structure of BST/nano-scaled-Cr/BST multifilm was introduced into the cell capacitor. The thermal stability of BST capacitance can be greatly enhanced by applying this nono-scaled Cr layer. The electric characteristics and corresponding mechanisms will be systematically discussed in this investigation.



Chapter 8 makes conclusions for this thesis, and the future prospects are suggested.

Chapter 2

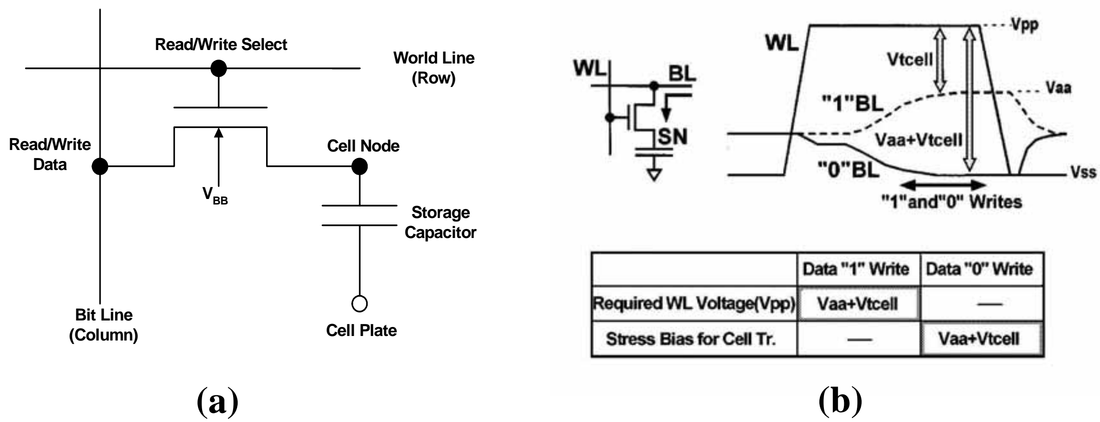
General Backgrounds and Literature Review

2-1 *General Backgrounds of DRAM Cell*

2-1.1 Overview on DRAM Cell

Figure 2-1(a) shows a DRAM cell with one-transistor and one-capacitor (1T1C) structure, and Fig. 2-1(b) depicts one of the typical cell operations [35]. The cell data is read out to bit line (BL) while the selected world line (WL) is boosted to V_{pp}. After sensing, the BL voltage is fully amplified to internal array operation voltage V_{aa} for data "1" and V_{ss} for data "0" simultaneously. For data "1" write, the WL voltage must be higher than V_{pp} (=V_{aa}+V_{tcell}) to write data "1" to the memory cell, where V_{tcell} is the threshold voltage of the cell transistor. Besides, for data "0" write, the bit line must be biased to ground.

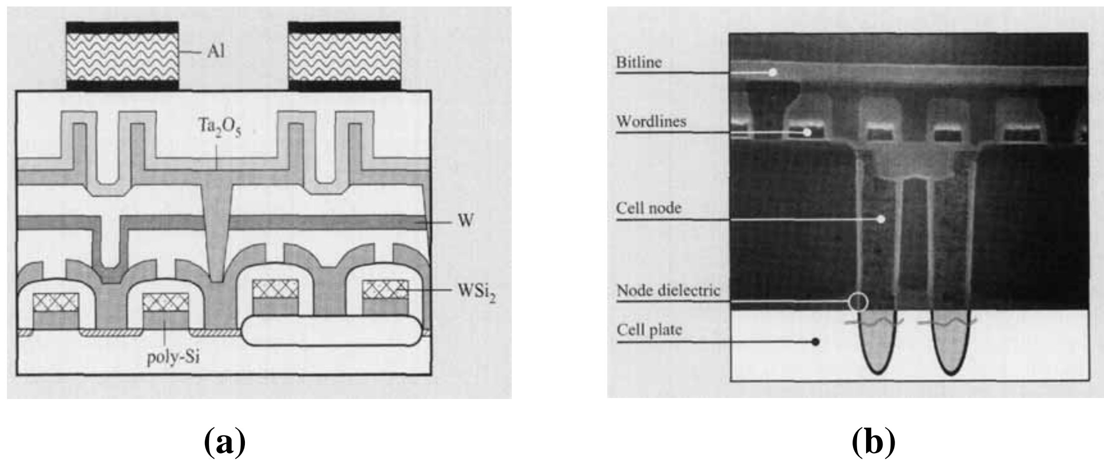
In the early age of DRAM development, two-dimensional cell structure, formed by double polysilicon transistor, was widely applied on the standard DRAM cell, known as the "planar type" DRAM. Three-dimensional cell structure was introduced to 4Mb-above generation, and these innovations included the trench capacitor cell and stacked capacitor cell (STC). Both of the trench and the stacked cell techniques are used



	Data "1" Write	Data "0" Write
Required WL Voltage(Vpp)	Vaa+Vtcell	—
Stress Bias for Cell Tr.	—	Vaa+Vtcell

Figure 2-1 (a) Schematic diagram of 1T1C-transistor cell in DRAMs. (b) Operation scheme and stress bias conditions [35].

in commercial DRAM products till now, but they have been greatly improved in the past generations, as depicted in Figs. 2-2 (a) and (b) [36, 37]. The most important benefits of the trench cell are high transistor performance and effective topology. Excellent transistor performance results from the trench capacitor formed at the early processing stage, so the thermal budget can be reduced during chip fabrication. Hence, it makes trench technology more favorable as the embedded memories integrated with the high performance CMOS logic [7]. The topology of trench can effectively raises the capacitance up, but without increasing the planar cell area. The disadvantages of trench cell come from the obstacles of the manufacture and the new material applications. The extremely deep trench etching and the cell isolation are very difficult to be manufactured by semiconductor processing technologies. In addition, the leakage current density of the trench capacitor rapidly increases as the cell size decreases due to lots of profile defects. Trench cell also lacks of fabrication technologies for high dielectric material applications, such as penta-oxide (Ta_2O_5) and barium strontium



(a) **(b)**

Figure 2-2 Schematic cross section of (a) stacked and (b) trench capacitor cell [7].

titanate (BST).

On the other hands, the benefits of using the stacked cell (STC) are that the standard techniques of the planar silicon processing are still available for this capacitor fabrication, which is contained in the multiple interconnect layers above the silicon. Therefore, lots of techniques can be applied on the stacked capacitor using the high dielectric materials. Stacked cell has been changed from the capacitor-under-bit line (CUB) to capacitor over bit line (COB) structure to increase the cell capacitance, as shown in Figs. 2-3 and 1-1 respectively. Compared with CUB, the COB stacked cell can

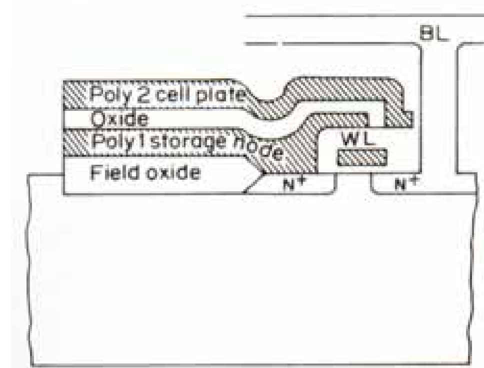
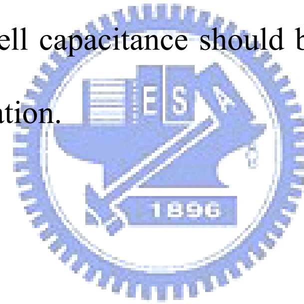


Figure 2-3 The schematic representation of the stacked cell using the typical structure of capacitor under bit-line (CUB) [3].

provide larger cell area, so that will be a promised candidate for the giga-bit scaled DRAM. Although COB could be able to applied on giga-bit generation, there are still many challenges for scaling down, such as large leakage current at the storage junction, variation of cell transistors' threshold voltage, parasitic resistance and capacitance between the bit-line/the cell-capacitor, and insufficient cell area. However, insufficient cell area is one of the most disadvantages for STC, so the high dielectric material is indeed necessary as the capacitor material for the new generation stacked-cell [3].

Memory cell capacitance plays a key role, which can determine the sensing signal margin, speed, data retention time and endurance against the soft error. In the multimega bit generation, the minimum cell capacitance should be 25 fF/cell. Capacitance can be described as the following equation.



$$C_S = A \times \frac{\varepsilon}{d} \qquad (2\text{-}1)$$

where C_S is the memory cell capacitance, ε is the capacitor dielectric, *A* denotes the capacitor area and *d* is the capacitor thickness. The leakage current at the cell node, consisted by sub-threshold leakage, irradiation charge loss, noise coupling, junction leakage and cell dielectric leakage, will strongly affect the sensing signal margin, as shown in the following equation.

$$V_s = \frac{1}{2(C_S + C_B)} C_S V_{cc} - \frac{1}{(C_S + C_B)}((I_j + I_{sub} + I_d)t_{ref} + C_B V_N + Q_C) \qquad (2\text{-}2)$$

where V_S presents the sensing signal voltage, C_B is the parasitic bit line capacitance, I_j, I_{sub} and I_d indicate the current of junction leakage, sub-threshold leakage and dielectric leakage. T_{ref} is the refresh time, V_N is the nose voltage owing to nose coupling and

transistor-threshold/sensing amplifier mismatch, and Q_C is the charge loss induced by irradiation [2]. To obtain the excellent properties of crystallinity and leakage reduction, the choice of electrode structure is another important concern. The trend of electrode-capacitor material structure is shown in Fig 2-4. The capacitor of COB cell adopted the silicon-insulator-silicon (SIS) structure before, but the novel Ta_2O_5 or Al_2O_3 dielectric in metal-insulator-silicon (MIS) is replacing the long-lived NO dielectric in SIS, ranging from 0.18 μm to 100 nm node. As the feature size shrinking under 100 nm, the advanced high-K dielectric, Ex. BST, with metal-insulator-metal (MIM) will be inevitably applied on the giga-bit generation DRAM cell.

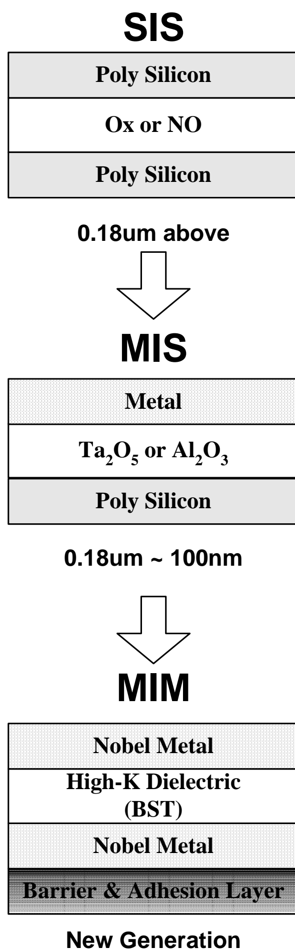


Figure 2-4 The evolvement trend of the multilayer structure used for DRAM cell capacitors.

2-1.2 Trend and Challenges of DRAM

In the past 20 years, the desktop PC was the primary driver for DRAM's industry. Although the PC market still keeps on growing, the DRAMs' market structure must be modulated due to the high-end demand rising [38]. Fig. 2-5(a) indicates the memory sizes for the computer segment. In general, the communication servers require the highest density DRAM in each generation. Fig. 2-5(b) presents the market trends of 128-megabit-equivalent DRAM. Obviously, the market share of PCs' DRAM are decreasing, but that of communications' is greatly growing. The evolution of CMOS technologies was described as Moor's law, which predicted the number of components would be double on the integrated circuit (IC) chip each year. The common rule of Moor's law is still useful even though that has been modified several times [39]. The trend of lithographic capability was predicted by Semiconductor

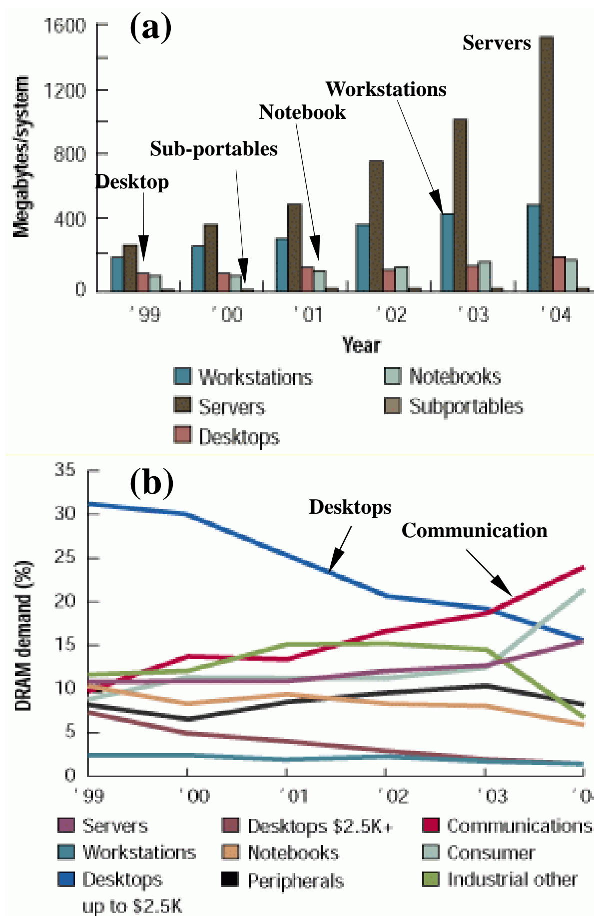


Figure 2-5 DRAM capacity requirement for (a) average Mbytes/system by computer segment, and (b)major application demands [38].

Industry Association (SIA), as shown in Fig. 2-6(a), where half pitch is the minimum size of lithographic features on a chip. According to the experiential rule in the past 20 years, the chip density has been quadrupled every three years, and the chip size is 1.5X bigger than that of previous generation. In addition, the chip speed keeps on improving in spite of the chip size increasing. Table 1-1 shows the DRAM device requirements and overall technology trend. Fig. 2-6(b) shows the forecast of the chip-size/cell-size versus generation, based on the architecture of $8F^2$ folded line cell, where F is the feature size [4]. The vertical stack height is another important factor of COB technologies. To meet the requirement of minimum cell capacitance, dielectric thickness decreasing or stack height increasing are carried out as the solutions of the new generation cell, but both of them will induce large leakage current. The upper limitation trend of the stack height is shown in Fig. 2-6(c), which shows the stack height must be lower than 1 μm to satisfy the 0.11 μm technology and under [5].

The DRAM manufacturing was developed from 4Mb to 256Mb through the decade of the 1990s. During those generations, density-enhancing technologies dedicated in the shallow trench isolation (STI), bit-line contact borderless to world-line, capacitance enhancing, junction leakage suppressing and self-aligned buried strap [7]. A high substrate doping density, $> 5\times10^{17}$ /cm^3, was required in order to keep the threshold voltage at 1 volt to suppress the short channel effect, but the junction leakage current would be the crucial issues due to this high doping density. Hence, the self-aligned channel implantation was introduced as the solution of substrate doping suppressed [2, 4]. The trend of cell transistor's channel length is a function of substrate doping density, as shown in Fig. 2-7(a). In general, the minimum accepted cell capacitance is

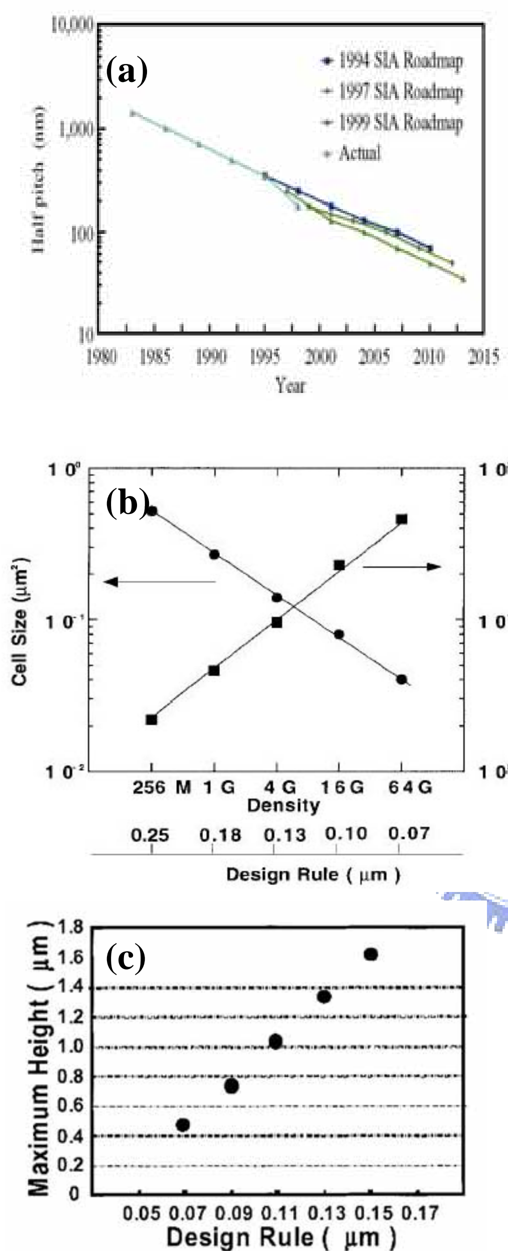


Figure 2-6 Historical and future trends of (a) lithographic resolution capability, (b) cell sizes and chip sizes estimations based on the 8F2 folded bit line. (c) the maximum stack height of cylinder-type COB stack cell [4, 5, 39].

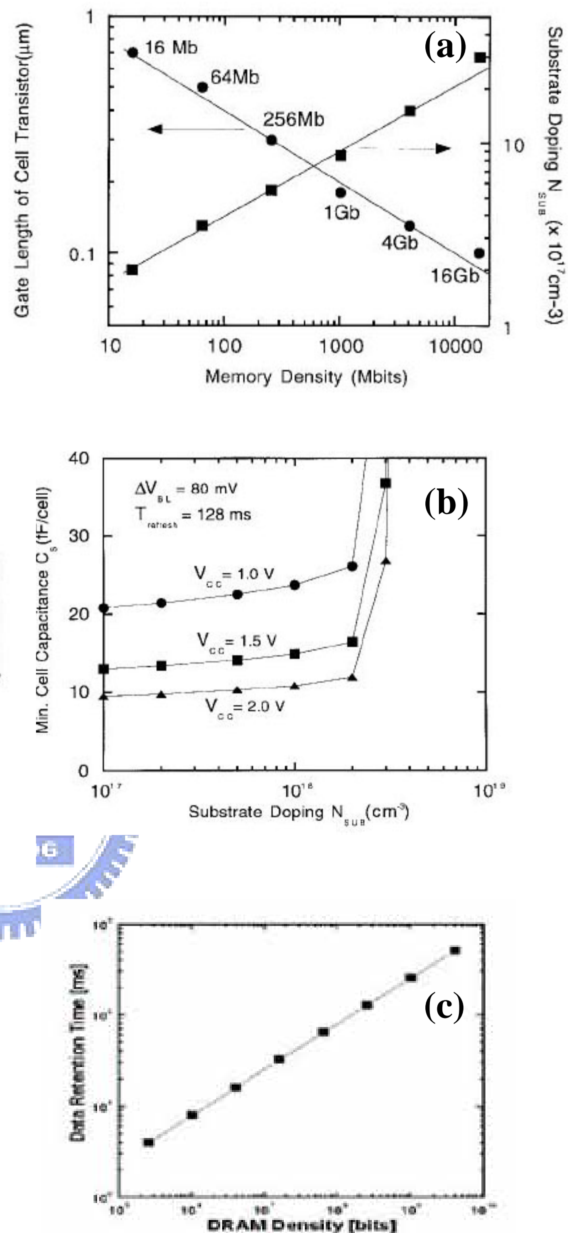


Figure 2-7 (a) Trend of channel length and substrate doping density of cell transistors. (b) Min cell capacitance as a function of substrate doping density. (c) Data retention time as a function of DRAM density [4, 6].

Year of the First Product Shipment, Technology Node	2001 130 nm	2002	2003	2004 90 nm	2005	2006	2007 65 nm	2010 45 nm	2013 32nm	1016 22nm
Upper Electrode	Metal									
High-k Dielectric	ONO or NO	Ta_2O_5, Al_2O_3				BST, STO		Epi BST		
Bottom Electrode	Poly Silicon		Metal					Perovskite		

Table 2-1 The solution roadmap of DRAM capacitor.

reduced as the new generation progressing, but that must be higher than 25 fF /cell for the giga-bit DRAM cell. High doping density results in the junction leakage current increasing, so the cell capacitance must be higher than 25 fF /cell, as shown in Fig. 2-7(b). However, the requirements of the DRAMs' cells from 1Mbit to 64Gbit are summarized in Table 1-1, which was further modified by the information of ITRS 2003 and IBM Res. [7, 8]. Besides, the data retention time is the one of the most important parameters for DRAMs' applications. The data retention time is the period of the stored data lost owing to the leakage current before data refreshing. The data retention time has to be doubled as the memory density increases 4X in every new generation to satisfy the requirements of high speed and low power consumption, as shown in Fig. 2-7(c) [6]. The leakage current at a cell node, which was consisted by the cell transistor sub-threshold current, cell dielectric leakage and source/drain junction current, greatly influences the data retention time. Therefore, to obtain a better data retention property, the node leakage should be improved in many ways, such as interface improvement of shallow trench isolation, electric field suppressed at the cell node junction and material improvement in cell dielectric layer.

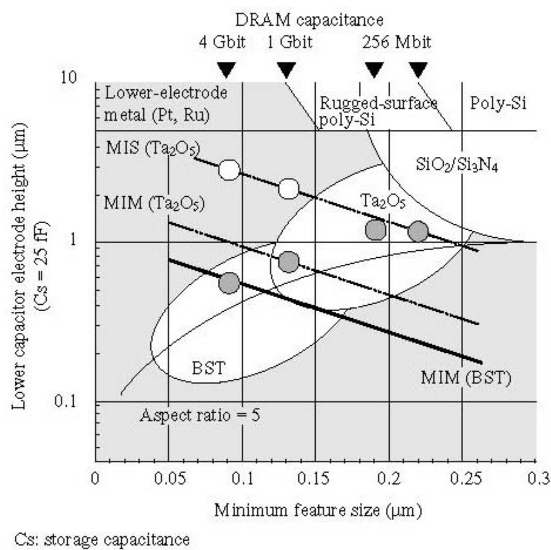


Figure 2-8 Trend of dielectric materials applied on various DRAM generations [40].

The selections of dielectric material and the electrode structure are very important for the electric properties of cell capacitor. Fig. 2-8 depicts the roadmap of capacitors' material applied on various DRAMs' generations [40]. The cell capacitor of the high density DRAM adopted Si_3N_4/SiO_2 (nitride/oxide, NO) as its insulator's material under 256M-bit generation. Because the ultimate of NO dielectric is limited to around 4-nm in oxide equivalent thickness, the only possible solution is to increase surface area using hemi-spherical grain (HSG) technique. However, there is not much room for the cell size scaling down owing to the limitations of the stack height and the HSG grain size. Therefore, a tantalum pentoxide (Ta_2O_5) is being applied on the generations of 256M-bit~4G-bit generation now instead of nitride material. The capacitor using Ta_2O_5 dielectric is based on metal-insulator-silicon (MIS) structure, but the capacitor structure will switch to metal-insulator-metal (MIM) structure for the generation scaling down to 0.13 μm. The metal storage node instead of the poly silicon node is in order to eliminating the native oxide formed at the poly silicon node, but the technique of the metal electrode integrated with Ta_2O_5 dielectric is a big challenge due to large leakage current. So far, the Ta_2O_5 can be further scaled down to 0.13 μm technology, but its limitation will be 2-3 nm in oxide equivalent

thickness. One of the prevalent candidate for multi-giga bit generation is probably (Ba, Sr)TiO_3 (BST) dielectric, because BST can achieve extremely high dielectric constant around 150-400 and be crystallized on the noble metal electrode. MIM BST capacitor is the most promised cell capacitor in the near future. Table 2-1 indicates the roadmap of the cell capacitor development using different electrode structures and insulator material.

At current technology timeline, DRAM progressing is limited by further scaling-down of MOSFET channel length, leakage current and insufficient cell capacitance. As DRAM enters the 21st century, the advanced technologies ranging from 0.18 μ m to below 100nm give bright future for the new generation applications.

2-2 Basic Concepts of the High-k Perovskite Material

2-2.1 The material and the electrical characteristics of perovskite Ceramic

Capacitor material is one of the most important factors for the characteristic of DRAM cell. Cell capacitance, leakage current and fabrication process can be significantly influenced by this factor. Some of the fundamental parameters of capacitor material are introduced below. The electric displacement D related to polarization P can be expressed as:

$$
\begin{aligned}
D &= \varepsilon_0 E + P \\
&= \varepsilon_0 E + \chi_e \varepsilon_0 E \\
&= \varepsilon_0 (1 + \chi_e) E
\end{aligned}
$$

$= \varepsilon_0 \varepsilon_r E = \varepsilon E$ *(2-3)*

where D: electric displacement

E: external electric field

P: polarization

ε_0: the vacuum permittivity

ε_r: the relative dielectric constant of dielectric material

χ_e: electric susceptibility

$$\chi_e \propto \partial P / \partial E \qquad (2\text{-}3\text{-}1)$$

$$\varepsilon_r = 1 + \chi_e \qquad (2\text{-}3\text{-}2)$$

The definition of electric polarization is shown below.

$$P = \sum_N \alpha E = \sum_N \varepsilon_0 (\varepsilon_r - 1) E \qquad (2\text{-}4)$$

where α is polarizability.

The total polarizability can be divided into four possible compositions, as denoted below.

$$\alpha = \alpha_e + \alpha_i + \alpha_d + \alpha_s \qquad (2\text{-}5)$$

These four compositions are illustrated as following.

(1) The electronic polarizability, α_e, is caused by a slight displacement of the negatively charged electron cloud in an atom relative to the positively charged nucleus. Electronic polarizability occurs in all solids and in some, such as diamond, it is the only contributor to the dielectric constant since ionic, dipolar and space charge

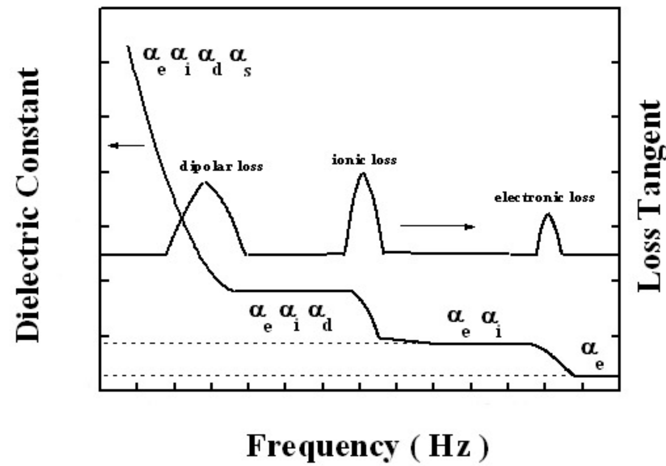


Figure 2-9 The dispersion relation of dielectric constant and tangent loss of the dielectric materials [41].

polarizabilities are absent.

(2) The ionic polarizability, α_i, arises from a slight relative displacement or separation of anions and cations in a solid. It is the principal source of polarization.

(3) Dipolar polarizability, α_d, arises in materials such as HCL or H_2O that contain permanent electric dipoles, these dipoles may change their orientation and they tend to align themselves with an applied electric field. The effect is usually very temperature dependent since the dipoles may be " frozen in " at low temperature.

(4) Space charge polarizability, α_s, occurs in materials that are not perfect dielectric but in which some long range charge migration may occurs.

Usually, the polarizability decreases in the order $\alpha_e < \alpha_i < \alpha_d < \alpha_s$. Fig. 2-9 shows the dispersion relation of dielectric and tangent loss [41]. In general, the tangent is loss due to the leakage current, and that can be express as:

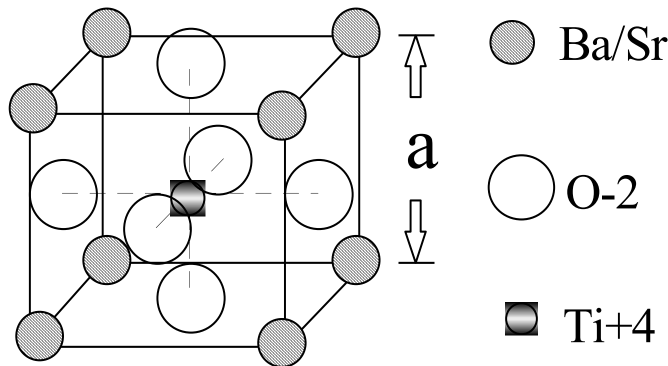


Figure 2-10 Typical crystal structure of perovskite $(Ba.Sr)TiO_3$.

$$\tan \delta = G/\omega C = \varepsilon''/\varepsilon' \qquad (2\text{-}6)$$

where G is the conductance of the capacitor, ω is the operation frequency, ε" and ε' are the imaginary and real parts of the dielectric constant.

(Ba, Sr)TiO_3 (BST) behaves excellent dielectric and material properties for semiconductor applications. First, comparing with many high-k dielectrics, BST exhibits unbelievably high dielectric constant in paraelectric phase, as depicted in Table 1-2 [9 - 11]. Second, the BST capacitor possesses excellent property of data retention. Figure 1-22 shows the effective oxide thickness versus leakage current using different high dielectric materials, such as N/O, Ta_2O_5 and BST [22]. Obviously, the effective oxide thickness of the BST is smallest at the same leakage current, that is, BST has best capability for charge storage among such high-k materials. In addition, there are plenty of technologies applied on BST fabrications [23 – 34], including vacuum evaporations, sputtering, CVD, MOD, MBE and sol-gel processes. Consequently, according to the above discussions, BST can greatly satisfy the requirements of the new generation cell capacitors.

Fig. 2-10 sketches a typical perovskite structure of BST crystal, which is a

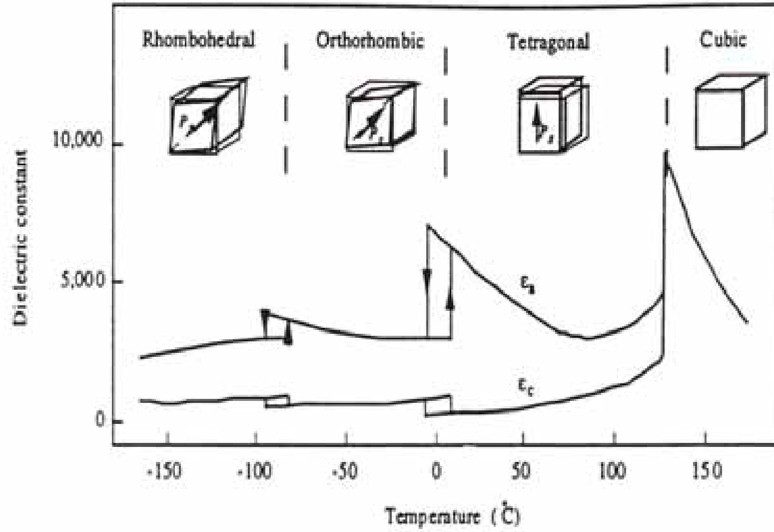


Figure 2-11 Various phase transitions in barium titanate.

substitutional solid solution consisted of $BaTiO_3$ (BTO) and $SrTiO_3$ (STO). Fig. 2-11 sketches the phase transition diagram of barium titanate [42]. In high temperature paraelectric phase, there is no spontaneous polarization, but, below the transition temperature T_C, the spontaneous polarization occurs. This transition temperature T_C is called Curie temperature. T_C of BTO is about 130°C, and that of STO is about 105°K. Therefore, the Currie temperature can be adjusted by the Ba/Sr ratio.

In principle, the phenomenon of spontaneous polarization can be analyzed by the energy equation [42].

$$W_{tot} = W_{dip} + W_{elas} = [(k/2Nq^2)-(N\alpha\gamma^2/9\varepsilon_0^2)]P^2 + [k'/4N^3q^4]P^4 \quad (2\text{-}7)$$

where W_{tot} is the total energy of unit volume, W_{dip} and W_{elas} are the energies of dipole moment and elasticity, respectively. Here, γ is called Lorentz Factor, ε_0 is the permittivity of vacuum (8.85×10^{-12} F/m), ionic polarizability is α, N is the dipole density, and k' is the force constant. Spontaneous polarization can occur more easily in

perovskite structure due to a high value of Lorenz factor ($\gamma = 10^2$). Besides, the polarizability of the perovskite ferroelectric material is usually sensitive to temperature, inducing the phase transition. According to the Eq. 2-7, suppose the polarizability increases as temperature decreases, so a high α will result in ferroelectric phase, i.e. $(k/2Nq^2)-(N\alpha\gamma^2/9\varepsilon_0^2) < 0$. Oppositely, the temperature increasing will lead to paraelectric phase while $(k/2Nq^2)-(N\alpha\gamma^2/9\varepsilon_0^2) > 0$. Considering a first approximation of Eq. 2-7, the well-know Currie-Weiss law is derived in paraelectric phase.

$$\varepsilon = C/(T-T_0) \qquad (2\text{-}8)$$

where C is the Currie-Weiss constant and T_0 is the Currie-Weiss temperature. T_0 is slightly lower than the exact transition temperature T_C. The phase transition occurs at T_C, and the spontaneous polarization is continuously tending to zero. This phenomenon is called second-order transition.

Figure 2-12 shows schematically the temperature dependence of the spontaneous polarization P_S and permittivity ε. P_S deceases as temperature increases and vanishes

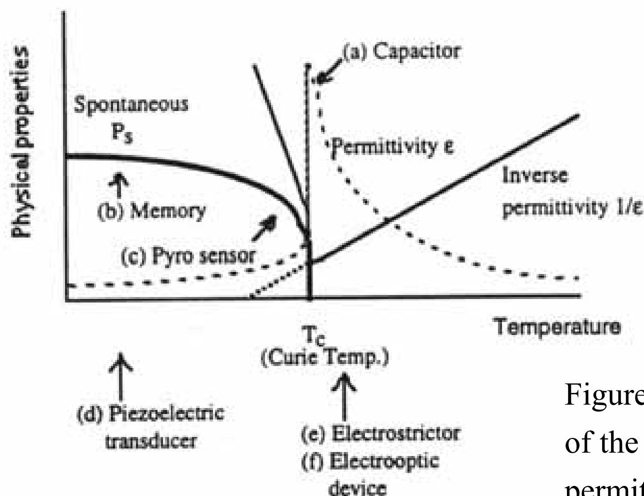


Figure 2-12 Temperature dependence of the spontaneous polarization and the permittivity in ferroelectric material.

at Currie Temperature. The permittivity follows the Currie-Weiss law in paraelectric phase. The applications of perovskite ferroelectric material are also denoted in the Fig. 2-12. The material in paraelectric phase, above T_C, is very promising for DRAM capacitor, and that in ferroelectric phase can be applied on nonvolatile memory. A large temperature dependence of the spontaneous polarization occurs below and near the Currie temperature, so the ferroelectric ceramic in this region is suitable for the pyroelectric sensors. These perovskite ferroelectric also possesses piezoelectric property, which can be used as pressure sensors and actuators. Besides, the barium titanate has positive temperature coefficient (PTC) of resistivity due to a junction effect, and the PTC effect can be applied on thermistors. Hence, perovskite ferroelectric can be widely applied on various electronic devices.

Leakage current and power consumption are the critical concerns of the electrical properties applied on the memory capacitor. The conduction mechanisms of high dielectric constant or ferroelectric materials are complicated, which may be associated with dielectric itself, grain boundaries, interfacial layers, electrodes, etc. Besides, many high dielectric constant or ferroelectric materials are found to polarize in a manner that displays substantial time dependence. In addition to an essentially instantaneous or very high-frequency polarization, polarization charging current flow into such materials with a power-law time dependence of approximately t^{-n}, where $n \leq 1$ usually, as in Fig. 2-13 [43]. The charging current is the sum of the polarizing current, which dominates at short times because of its t^{-n} behavior, and the true leakage current is referred to the current flow from electrons or holes, which dominates at long time. Therefore it should be very careful to identify the real and steady leakage current from the polarizing

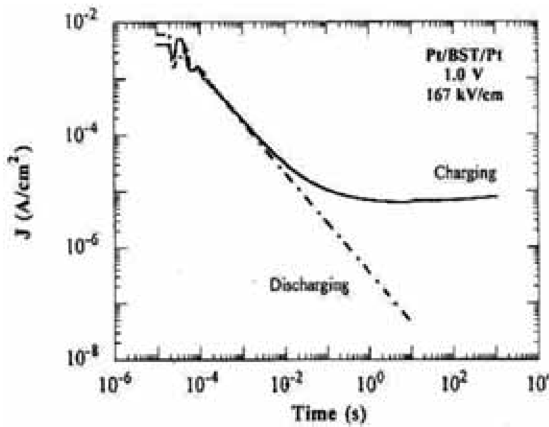


Figure 2-13 Short-time charging and discharging current in Pt/BST/Pt, exhibiting power-law behavior for the relaxation current. [43]

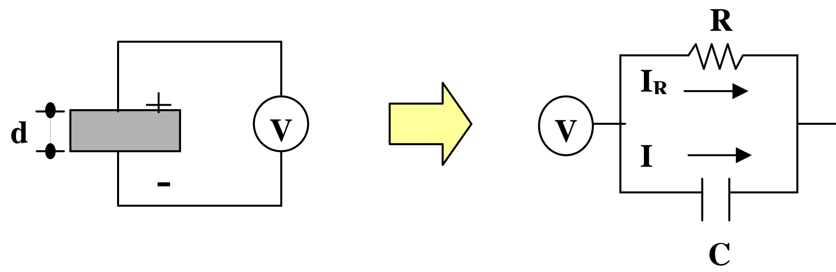
current with including a proper delay time during the I-V measurements.

The leakage behaviors of the ferroelectric material can be expressed by several conductive models due to many complicated mechanisms coexisted. Usually the Ohmic contact is not easily formed between the high dielectric constant or ferroelectric materials and electrodes, unless the carrier concentration of dielectrics is high enough in the interface and results in tunneling effect. Besides, the ultra thin dielectric insulator, usually thinner than 30nm, behaves tunneling current. Because there is strong temperature dependence of leakage current in the dielectrics, both Schottky emission (or thermionic emission) and Poole-Frenkel transport are the possible conduction mechanisms. The equations of these two conduction mechanisms are shown as the following:

SE model: $J_{SE}=A^{*}T^{2}exp\{-q[\varphi_B-(qE/4\pi\varepsilon_d\varepsilon_0)^{1/2}]/kT\}$ (2-9)

PF model: $J_{PF}=BEexp\{-q[\varphi_t-(qE/\pi\varepsilon_d\varepsilon_0)^{1/2}]/kT\}$ (2-10)

where φ_B, φ_t, d, ε_0, ε_d are the barrier height between dielectrics and electrodes, energy gap between the trapping levels and conduction band , insulator thickness, dielectric permittivity, dielectric constant of BST and A* and B are constants..



$$Q = CV ; V = V_0 e^{jwt}$$
$$I = \partial Q / \partial t$$
$$= j\omega C_0 \varepsilon' V + \omega C_0 \varepsilon'' V$$
$$= I_C + I_R$$
$$\tan\delta = |I_R / I_C| = \varepsilon'' / \varepsilon'$$

$$Z = R + jX$$
$$= 1/\omega C_0(\varepsilon'' + \varepsilon')$$
$$= \varepsilon'' - j\varepsilon' / \omega C_0(\varepsilon''^2 + \varepsilon'^2)$$
$$\therefore \tan\delta = \varepsilon''/\varepsilon' = |R/X|$$

Figure 2-14 The circuit model of tangent loss due to the leakage current through the loss by a parallel resistance.

In addition, many researches reported lots of other theories about the leakage current, such as Space Charge Limited Current (SCLC) and the effect of grain boundaries [44]. Consequently, the conduction mechanisms should be determined by the practical conditions, which is associated with the form of energy band diagram constructed from dielectrics, electrodes, grain boundaries, etc. [44 – 50].

The tangent loss is due to the leakage current through the loss by a parallel resistance, shown in Fig. 2-14, and it is defined as the ratio of the leakage current through the resistance (I_R) to the leakage current through the ideal dielectric (I_c). Therefore the value of tangent loss can be extracted from the following equations:

$$\begin{aligned} &Q = CV; V = V_0 e^{j\omega t} \\ &I = \partial Q/\partial t = j\omega CV = j\omega C_0(\varepsilon' - \varepsilon'')V \\ &\quad = j\omega C_0 \varepsilon' V + \omega C_0 \varepsilon'' V = I_c + I_R \\ &\tan\delta = |I_R / I_c| = \varepsilon''/\varepsilon' \end{aligned} \tag{2-11}$$

where $\varepsilon = \varepsilon' - j\varepsilon''$

$$Z = R + jX = 1/\,j\omega C_0(\varepsilon' - j\varepsilon'') = (\varepsilon'' - j\varepsilon')/\,\omega C_0(\varepsilon''^2 + \varepsilon'^2)$$

$$\therefore\ \tan\delta = \varepsilon''/\varepsilon' = |R/X| \qquad (2\text{-}12)$$

Besides, the total capacitance can be regarded as a combination of two capacitors and the equivalent circuit is shown in Fig. 2-15. C_d, R_e, C_e and R_e stand for the capacitance and resistance of the dielectric and those of the electrode, respectively. The measured series capacitance (C_s) and dissipation factor can be expressed as follow [51].

$$C_s = \frac{(1+\omega^2 C_d^2 R_d^2)(1+\omega^2 C_e^2 R_e^2)}{\omega^2 \left\{C_d R_d^2 (1+\omega^2 C_e^2 R_e^2) + C_e R_e^2 (1+\omega^2 C_d^2 R_d^2)\right\}} \qquad (2\text{-}13)$$

$$D = \frac{R_d(1+\omega C_e^2 R_e^2) + R_e(1+\omega^2 C_d^2 R_d^2)}{\omega^2 \left\{C_d R_d^2 (1+\omega^2 C_e^2 R_e^2) + C_e R_e^2 (1+\omega^2 C_d^2 R_d^2)\right\}} \qquad (2\text{-}14)$$

Assuming that a dielectric layer is an ideal insulator, Cs & D can be simplified below.

$$C_s = \frac{C_d(1+\omega C_e^2 R_e^2)}{1+\omega^2 C_e R_e^2 (C_d + C_e)} \qquad (2\text{-}15)$$

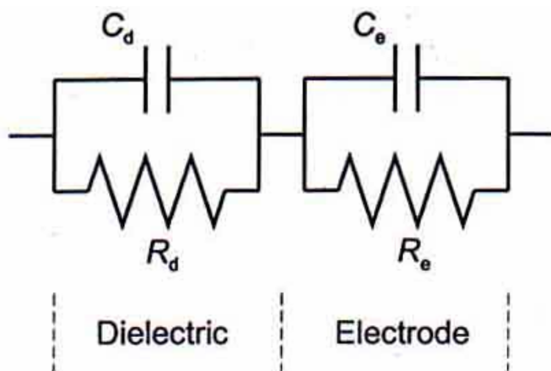


Figure 2-15 Equivalent circuit for a capacitor in series with a high resistance electrode [43].

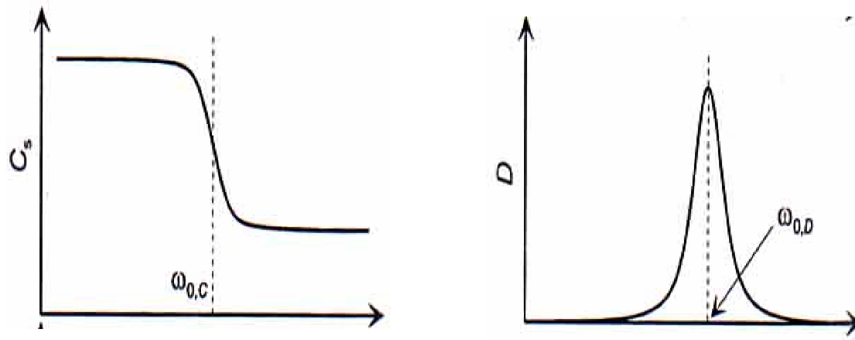


Figure 2-16 Schematic graphs of the frequency dependence of C_s and D. C_s and D show the Debye-type dispersion [51].

$$D = \frac{\omega C_d R_e}{1 + \omega^2 C_e R_e^2 (C_d + C_e)} \tag{2-16}$$

where Eqs. 2-15 and 2-16 show the Debye-type dispersion. The resonant frequency ω_0 in Cs is obtained the maximum slope of Cs versus frequency and the frequency w0 is obtained from the peak value of D, as shown in Fig. 2-16.

$$\omega_{0,C} = 1 \big/ R_e \sqrt{3C_e (C_e + C_d)} \tag{2-17}$$

$$\omega_{0.D} = 1 \big/ R_e \sqrt{C_e (C_e + C_d)} \tag{2-18}$$

Both $\omega_{0,C}$ and $\omega_{0,D}$ decrease with increasing R_e.

Usually the tangent loss comes from two mechanisms: resistive loss and relaxation loss. In the resistive loss mechanism, the energy is consumed by mobile charges in the film. In the case of the relaxation loss mechanism, it is the relaxation of the dipole that expends the energy. Both two mechanisms of tangent loss are associated with the leakage current in the dielectrics, also investigated in this thesis.

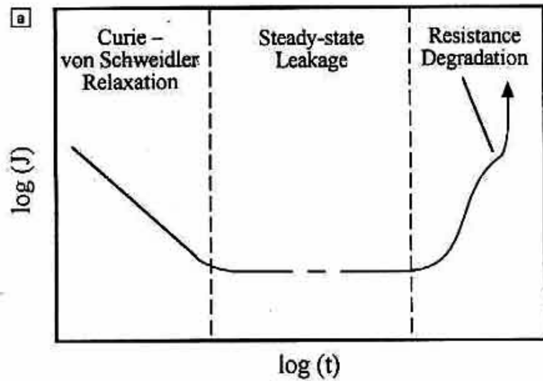


Figure 2-17 Schematic of different current regimes in metal-insulator-metal systems containing ferroelectric films. [52].

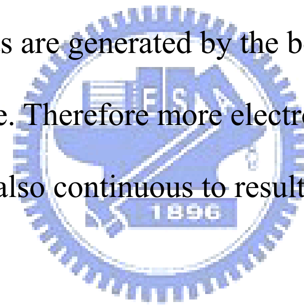
For the paraelectric or ferroelectric dielectrics, there are many electrical properties that will change with time, including the dielectric constant, remanent and maximum polarization, coercive electric field, tangent loss, leakage current, breakdown electric field, etc. Three time-dependent mechanisms will affect these electrical properties, which are aging, fatigue and resistive degradation.

Aging is generally defined as a spontaneous change in electrical properties with time, either under electric stress or not. However, fatigue is referred to the changes in the electrical properties with repeated polarization reversals. Both mechanisms are found in ferroelectric states and believed due to the pinning of domain walls from charge trapping, oxygen vacancies and associated defect dipoles.

The third mechanism is time-dependent dielectric breakdown (TDDB), which is also referred as resistance degradation, for both paraelectric and ferroelectric dielectrics. It is defined as an increase of the leakage current under a constant applied electric field after prolonged times, also shown in Fig. 1-18. The mechanisms of the resistance degradation have been studied widely for silicon dioxide. Two of the mechanisms are described below:

(1) *Hole-trapping model:* Impact ionization is resulted from the injected electrons due to F-N tunneling, and new electron-hole pairs are generated. Some holes will be more easily trapped by defects due to its lower mobility. Then the positively charged defects will move toward the cathode and pile up. This results in the increase of electric field at the cathode and induces more electrons to inject into the dielectric. Therefore more electron-hole pairs are generated and the feedback processes are continuous to dielectric breakdown.

(2) *Lattice deformation model:* The injected electrons due to F-N tunneling are accelerated by large electric field and bombard the interface between the dielectric and the anode. Many defects are generated by the bombardment and form positively charged defects at the anode. Therefore more electrons are induced to injection, and the feedback processes are also continuous to result in dielectric breakdown.



The suitability of these breakdown mechanisms to the paraelectric or ferroelectric dielectrics is investigated, too [42 – 56].

2-2.2 Applications of BST thin films for DRAM's cell capacitor

In the past decades, the high-k films had attracted great attentions for the applications of advanced DRAM capacitors. Comparing with many high-k dielectrics, BST exhibits excellent unbelievably high dielectric constant in paraelectric phase, as depicted in Table 1-2 [9 – 11]. Figure 1-2 shows the effective oxide thickness versus leakage current using different high dielectric materials, such as N/O, Ta_2O_5 and BST

List of the bottom electrode requirements
1. Must remain conductive after BST deposition
2. Must not react with BST
3. Must be a difussion barrier to O, Si and BST
4. Must maintain low contact resistance to underlying plug
5. Must adhere to silicon, silicon dioxide & plug material
6. Must be depositable using production tools
7. Must be etchable down to deep submicron features

Table 2-2 Bottom electrode requirements for stacked BST capacitor

[22]. Obviously, the effective oxide thickness of the BST is smallest at the same leakage current, that is, BST has best capability for charge storage among such high-k materials. Hence, the BST capacitor possesses excellent property of data retention.

The dielectric properties are greatly influenced by the process factors, such as substrate temperature, properties of electrode substrates and fabrication methods, because the dielectric properties is corresponding to the crystallinity of BST thin film. High temperature (>450°C) depositions or multi-thermal-cycle treatments are frequently applied to obtain good crystallinity of a perovskite structure, as listed in Table 1-3 [12, 13, 23 – 34].

The bottom electrodes of the BST films, applied on COB structure, must have specific requirements, as denoted in Table 2-2. The dielectric constant of BST is very large, so the oxidation layer of bottom electrode, forming the series low-k capacitor, will greatly degrade the capacitance. Hence, the materials of the bottom electrode must be stable in oxygen environment, so the only qualified materials should be noble metal or conductive oxides, such as Pt, Ir, Ru, RuO_2 or LSCO. There were plenty of studies on the properties of the bottom electrodes, as reported by M.S. Tsai, T.Y. Tseng and S.

Summerfelt etc. The surface stabilities of Ir and Ru are not as good as Pt. Although conductive oxides, ex. RuO_2 and LSCO, have excellent properties, they're still difficult to be applied on industrial devices due to their complicated compositions and expensive cost [11, 18, 57 – 59]. The oxygen stable bottom electrode must contact the substrate through a plug which is typically poly-Si. The key requirement for the barrier layer is preventing the interdiffusion of plug materials or Si. Several kinds of barrier materials have been investigated, such as TiN, TiAlN [60], TiSiN [61], TaN, TaAlN, TaSiN, etc. The metal/TiN/Ti/polysilicon-plug structure is widely applied as a bottom electrode of a standard COB-DRAM-Capacitor [62, 63].

2-2.3 Fabrication methods of perovskite thin films

Experientially, fabrication methods of perovskite thin films can be categorized into three fabrication types, i.e. wet chemical deposition (WCD), physical vapor deposition (PVD), and chemical vapor deposition (CVD).

(1) *Wet chemical deposition (WCD):* such as sol-gel [47 – 50], metal-organic deposition (MOD) [64]. The dielectric films can be deposited by spin coating in both of sol-gel and MOD methods. Easy process, low cost, high throughput and simple facility requirement are the advantages of WCD techniques. Although there are many advantages for WCD technologies, many problems still exist in this technology, such as the contamination control in the solvent and the porosity after baking. Besides, poor control of the perovskite phase stoichiometry can stem from varieties of the chemical source conditions. Poor step coverage and film crack after annealing

are another problems.

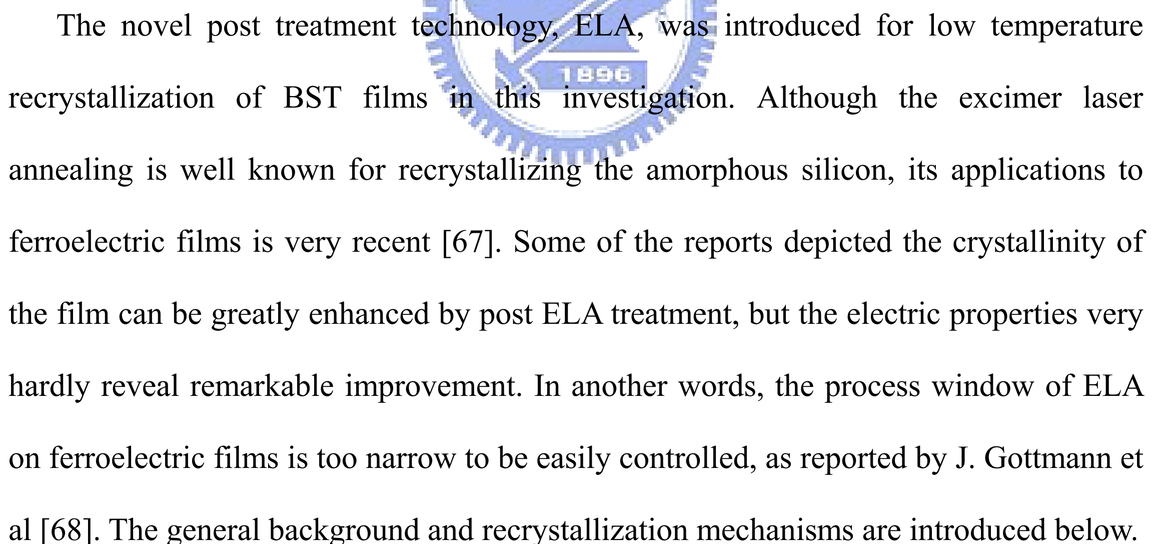
(2) *Chemical vapor deposition (CVD)* [51 – 54]*:* such as metal-organic chemical vapor deposition (MOCVD), liquid source misted chemical vapor deposition (LSMCVD) [65]… etc. CVD can promise as the technology of ferroelectric film fabrication for high-density devices due to excellent step coverage and uniformity. However, more complicated mechanisms of the process results in difficult process control, and the high temperature post-treatment is needed for removing the carbon species from precursor. Besides, the CVD process temperature is still very high for CMOS technology because of the chemical reaction requirement. Also utilizing metal-organic precursors, with which the technique is so called MOCVD, reduces the process temperature. However, more complicated mechanisms of the process are resulted and the remove of carbon species from precursors is needed with a post-treatment. Besides, LSMCD is one of CVD methods to deposit dielectrics. Only single precursor is misted by atomizer, carried to a chamber by Ar carrier gas and deposited on a substrate. The drying and crystallization processes are also needed. However, the uniformity for run to run is not stable.

(3) *Physical vapor deposition (PVD):* such as Sputtering, pulse laser ablation (PLA) [46]…etc. Sputtering is a term used to describe the technology in which atoms are removed from the target surface by collision with high energy particles. Sputtering can afford to perform a uniform thickness using large area target. This technology is good at producing layers of multicomponent materials and alloys. Besides, sputtering is a low cost, mature and easy-controlled technique. However, poor step coverage and different sputtering yield for different elements are disadvantages.

Pulse laser ablation can easily achieve the epitaxy growth and excellent crystallinity, but poor uniformity is formed.

In this thesis, the radio frequency (RF) magnetron sputtering technique was applied on the BST film fabrication. The RF alternating current (AC) generator is necessary for the fabrication of ferroelectric film, because the ferroelectric material, as a sputtering target, is a kind of insulation ceramic. The magnetron device can effectively enhance the ionization of sputtering gas Ar, increasing the sputte1ring yield [66].

2-3 Excimer Laser Annealing



The novel post treatment technology, ELA, was introduced for low temperature recrystallization of BST films in this investigation. Although the excimer laser annealing is well known for recrystallizing the amorphous silicon, its applications to ferroelectric films is very recent [67]. Some of the reports depicted the crystallinity of the film can be greatly enhanced by post ELA treatment, but the electric properties very hardly reveal remarkable improvement. In another words, the process window of ELA on ferroelectric films is too narrow to be easily controlled, as reported by J. Gottmann et al [68]. The general background and recrystallization mechanisms are introduced below.

2-3.1 General features of Excimer Laser Annealing

Laser Gas	XeF	XeCl	KrF	KrCl	ArF	F_2
λ(nm)	351	308	248	222	193	157

Table 2-3 Different excimer laser gases and corresponding wavelengths

Excimer laser is the most powerful UV light source, and that has been widely applied on the semiconductor industry, such as lithography, thin film fabrication and post annealing [69 – 71]. Table 2-3 shows that the various wavelengths, between 157~351 nm, can be obtained using different laser gas, and all excimer lasers are pulsed laser modes. In conventional technologies, amorphous ferroelectric films can be furnace annealed as high as 600°C above for a long period, reaching the solid phase crystallization. Besides, rapid thermal annealing (RTA) is also widely applied on thin film treatment, but it will induce large thermal stress in ferroelectric films. A novel technology, excimer laser annealing (ELA), was introduced to enhance the crystallinity of the BST films in this study, and a CMOS compatible process was also performed by ELA due to its low thermal budget and small thermally induced stress.

ELA behaves direct energy processing that the surface can be heated by laser beam. The first demonstrations of the utility of directed energy processing came from the annealing of implantation damage using lasers. For the roughly compared ELA with conventional furnace annealing (FA) and rapid thermal annealing (RTA), the large thermal budget and the entirely heating of FA result in the inter-diffusion and damages of under-layer structures, besides, too large thermal stress of RTA is not suitable in deep

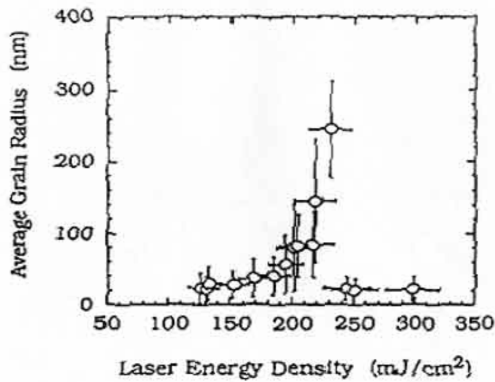


Figure 2-18 Average grain size of laser crystallized poly crystalline silicon films as a function of the laser energy fluence [72].

submicron even smaller design rules. ELA technology, strictly speaking, is not a real low temperature process, higher than 700°C in the top of laser absorption region, but this high-temperature absorption region is very shallow, 20-nm only, and the sustained time is as short as 10~100 nanosec. Hence, the under-layer substrate would not be damaged after ELA treatment.

ELA technology is widely used for preparing poly-Si thin film in current semiconductor industry. Although excimer laser may be an extremely powerful implement to achieve low temperature integrated process, but up to now, very few reports investigate the ELA mechanism for ferroelectric films. Therefore, the qualitative analyses below are all referred from the research about poly-Si.

(1) *The effect of laser energy density:* Fig. 2-18 shows that the average grain size is plotted as a function of the laser energy fluence, E_{laser} [72, 73]. Samples prepared at room temperature and with low laser energy fluence were composed of small grains. With increasing laser energy density the average grain size increases and eventually reaches a maximum value. But when the energy density above maximum value, the grain size decreases to a constant value. According to the above, the optimal energy

density is limited in a narrow region.

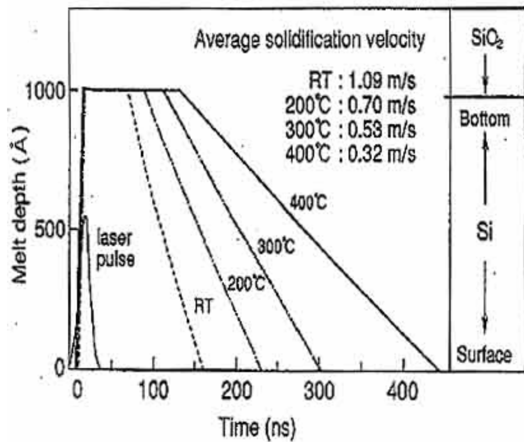


Figure 2-19 Time dependence of Si-layer melt front profiles under excimer laser irradiation [85].

(2) *The effect of substrate temperature:* Fig. 2-19 shows the time dependence of Si-layer melt front profiles under excimer laser irradiation [74]. It is assumed the whole Si layer was completely melted. As shown in this figure, the melting duration of the Si-layer is prolonged with increasing substrate temperature. The slope of the melt depth verses time graph decreases with increased substrate temperature during excimer laser annealing.

(3) *The effect of number of shots:* Fig. 2-20 shows the transition of grain size distribution with the above lateral grain growth as revealed in secco-etched SEM images [75 – 79]. As shown in this figure, poly-si films annealed using two shots exhibited almost lognormally distribution grains with an average grain size of about 200nm. The distribution of 64-shot-annealed poly-Si films, however, shifted to bimodal. This distribution seemed to occur during the process of lateral grain growth. Finally, 128-shots-annealed poly-Si films again exhibited almost monomodal grain size distribution with an average grain size of about 1.5 μm. This result clearly shows that, as the number of laser shots was increased, the average grain size is increased, and it was also found that dramatic lateral grain growth occurred.

In addition to the above, other variable process parameters, annealing ambient, laser duration, type of annealed films and substrate, should affect the re-crystallized process. Of course, the physical parameters, melting point, latent heat, thermal conductivity, density, specific heat, absorption coefficient, of annealed films must be serious considered first.

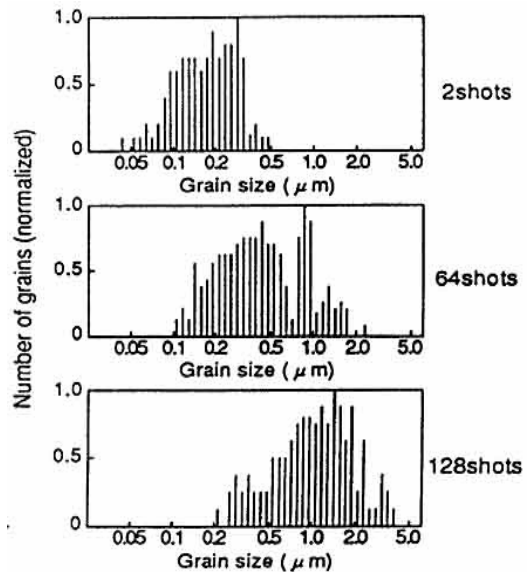


Figure 2-20 The transition of grain size distribution using various numbers of shots to perform excimer laser annealing [75].

ES

2-3.2 Mechanisms of Excimer Laser Annealing (ELA)

The directed energy processing has emerged for the processing and modification of the surface layers of semiconductors. And the directed energy sources such as lasers are used to heat the surface. The unique temporal and spatial control exercised over the heat flow by these beams allows formation of quite novel structures and alloys. For example, surface layers can be recrystallized in exceedingly short times. The dimensions of the layers that can be modified by the incident beams are just those required by Si integrated circuit technology [80 – 84]. The very short laser irradiating duration of ELA suppress the inter-diffusion and damages of the films bulk and under-layer structures.

The coupling of lasers to materials is very sensitive to the wavelengths and the states of the material. About the absorption mechanisms of laser radiation in semiconductor,

there are three regions must be contributed. One is the direct excitation of lattice vibrations in materials. This happens while the photon energy ($h\nu$) of light well below the band-gap energy (Eg). The other state is the excitation of free or nearly free carriers by absorption light. And this form occurs as $h\nu$<Eg; such carriers will always be present as a result of finite temperatures and/or doping. Finally, the third way of absorption energy of light is to create electron-hole pairs by light with $h\nu$>Eg. [82, 83]. The Eg of BST is about 3.6eV. for 248nm light, $h\nu$=5eV > Eg. We know it should be an efficient approach to BST films by 248nm light.

The thermal theory of ELA for poly-Si films is thoroughly developed in the past decade, but very few investigations reported the ELA thermal theory on ferroelectric films. As discussed below, the mechanisms of the thermal conduction will refer to the theory of Si-ELA. The facility of rapidly heating and cooling surface layers without heating the bulk depends on the pulse duration time τ and the coupling depths of the heat source. The cooling or quench rates of the surface layers using these pulsed sources will be in the range 10^9~10^{14}°C/sec. Longer irradiation times can be achieved by the use of continuous sources with scanned spots. The fastest irradiation times will be 10^{-7}~10^{-8}sec, with cooling rates less than 10^9°C/sec. In the case for 248nm applied on BST film for post annealing, the $\alpha^{-1}<(2D\tau)^{1/2}$ where α^{-1}, D and τ are absorption distance, heat diffusivity and pulse duration time. The absorbed energy is simply the laser power density multiplied by the pulse length $I\tau$ minus the reflected energy $IR\tau$. The average temperature rise in this $(2D\tau)^{1/2}$–thick layer is therefore given by the following equations [71, 85, 86]

$$\Delta T=(1-R)I\tau/\rho C(2D\tau)^{1/2} \quad (2\text{-}19)$$

ρ, C are density and specific heat. For more accuracy, temperature dependence of the material constants for each layer and latent heat during the phase change were taken into account. Three-dimensional nonlinear equation is used for solving the temperature distribution, solidification velocity during laser irradiation.

$$\rho c\frac{\partial T}{\partial t}=\frac{\partial}{\partial x}(k\frac{\partial T}{\partial x})+\frac{\partial}{\partial y}(k\frac{\partial T}{\partial y})+\frac{\partial}{\partial z}(k\frac{\partial T}{\partial z})+Q \qquad (2\text{-}20)$$

However, the thermal properties of ELA processing in ferroelectric films exhibit large differences from that in Si films due to the different absorption constant, heat capacitance, and thermal conduction mechanisms. Therefore, the processing model must be modified, as investigated in this thesis.

2-4 Process Integration of the BST Capacitor

BST is the best candidate of Giga-bit DRAM material, but there are still some challenges in the integrations of CMOS processing. High temperature (>450°C) deposition of BST films is frequently applied to obtain good crystallinity of a perovskite structure [12, 13], but the high temperature process may deform the junction profile and alter the gate length of the metal-oxide-semiconductor field-emission-transistor (MOS-FET), especially on the deep submicron scale. In STC structure, the MOS-FET is always implemented prior to the capacitor fabricated, which needs to be fabricated at low temperature to avoid the damage of the MOS-FET.

Another difficult issue is the electrode formation of BST capacitor. Usually, there is serious inter-diffusion between dielectrics and silicon during the deposition of

dielectrics. A thermally and electrically stable diffusion barrier is needed to prevent inter-diffusion, and it also cannot be oxidized during high temperature processes with O_2 ambient. Pt appears many excellent properties for using as electrodes of the BST capacitors, such as highly chemical stability, small leak current. The metal/TiN/Ti/polysilicon-plug structure has been successfully integrated into a standard COB-DRAM-Capacitor [62, 63]. The Ti layer forms $TiSi_x$ to improve the adhesion and the contact properties between TiN and polysilicon, and the TiN barrier layer prevents diffusion of Ti and Si into the BST films [87, 14]. According to our previous studies, the barrier capability of as-deposited TiN is not good enough, but the barrier capability of the TiN layer can be largely enhanced by rapid thermal annealing (RTA) [14, 20, 21]. Nevertheless, Ti was reported to diffuse through the Pt/TiN layer into the BST film to form TiO_x and oxygen vacancies, when the substrate temperature exceeds 450°C [15, 16, 21]. In addition, many studies reported that the leakage current of the BST film would be greatly increased after post annealing or ion sputtering process [14 – 17]. Although the dielectric properties can be greatly enhanced, the increased leakage current will result in the degradation of the data retention. Therefore, a low temperature process is indeed necessary for BST capacitor fabrications, but it still lacks systematically studies using low thermal budget technologies.

Otherwise, many reports indicated the dielectric constant and leakage current are greatly influenced under various operation temperatures [18, 19]. In general, the operation junction-temperatures for DRAMs' applications and qualification spec range from –0 ^{o}C to 120°C (ambient temperature ranging from –40~85 ^{o}C for consumer IC), so the dramatic variations of the electric-temperature properties may cause the deviation

of the normal device operation. The variations of dielectric constant and leakage current can reach as high as 20% above and 2~3 order, respectively, for the device operating between $0^{o}C$ and $100^{o}C$ [18, 19].

Consequently, the low temperature technologies are very important for the BST capacitor integrations, but very few papers reported the fully low temperature technique applied on BST capacitor fabrications, such as ELA treated BST films and oxygen plasma technology. Another most important challenge for BST capacitor integration is electrical variations during the device operating in different temperatures. Hence, the solutions of low temperature techniques and the thermal stability enhancement will be investigated in this thesis.

Chapter 3

Experimental Overview

3-1 Experimental Procedures

Multilayer specimen of Pt/BST/Pt/TiN/Ti/Si was employed to simulate the practical COB structure of DRAM's capacitor. The experiments in this thesis were focusing on low temperature fabrication technologies and the corresponding phenomenon analysis. The 6-inch silicon wafers, with (100) orientation, were treated by RCA cleaning, and the TiN/Ti layers were sputtered onto the Si substrates and post treated by RTA in N_2 ambient. The TiN/Ti/Si substrates were provides by Mosel Vitelic Inc. using standard industrial processes, and the process conditions were listed in the Table 3-1. The Pt films were sputtered onto the TiN/Ti/Si substrates as the bottom electrodes. The optimal conditions of the bottom electrode preparations have been reported in the previous investigations [88– 90].

Layer	Thickness	Function	Process Condiction
Si Substrate		Substrate (Si plug simulated)	Standard RCA Cleaning
Ti	50 nm	Adhesion Layer	Supttering Post RTA treated at 765°C (50 sec)
TiN	50 ~ 200 nm	Barrier Layer	Sputtering Post RTA Treated at 600°C (90 sec)
Pt	100 ~ 200 nm	Bottom Electrode	Sputtering

Table 3-1 The process parameters of Pt/TiN/Ti substrate preparation

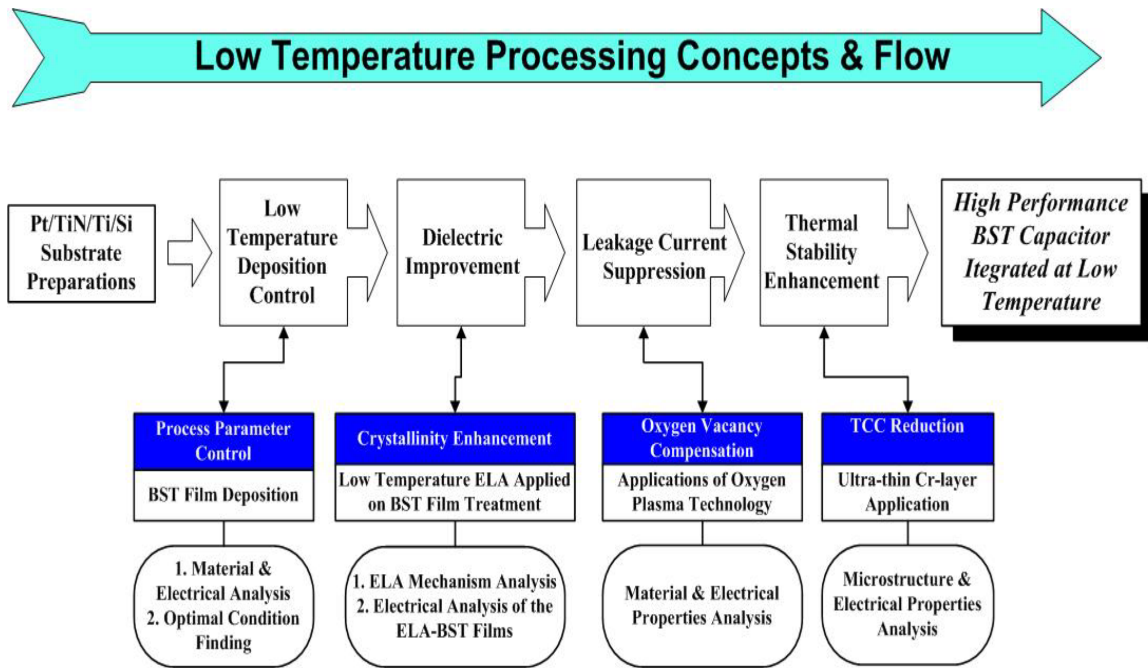


Figure 3-1 The experimental concepts of this thesis.

Figure 3-1 shows the experimental concept of this investigation. Low temperature process control, dielectric quality, leakage current suppression and thermal stability are the most critical concerns of BST capacitor integration. (Ba, Sr)TiO_3 (BST) films were fabricated on Pt/TiN/Ti/Si substrates by low-temperature radio frequency (RF) magnetron co-sputtering at 410°C, measured at wafer's backside. The material and electrical analysis were performed to study the mechanisms of dielectric properties, and the experimental flow is shown in Fig. 3-2.

The crystallinity of the BST film was enhanced by a novel technology using ELA treatment, which performed at low substrate temperature of 300°C. Fig. 3-3 shows the experimental flow of the ELA treatment and the post sample analysis. The residual gas analyzer was applied for surface species monitoring, which correlated to leakage

properties. Besides, the thermal conduction analysis concludes the electrical and material analysis results for ELA mechanisms of BST thin films. The process window and electrical behaviors were systematically studied by material, electrical and mathematical analysis. The succeeding treatment using oxygen plasma technique effectively suppressed the leakage current.

An intercrossing sandwich structure of Pt/BST/ultra-thin-Cr/BST/Pt was employed

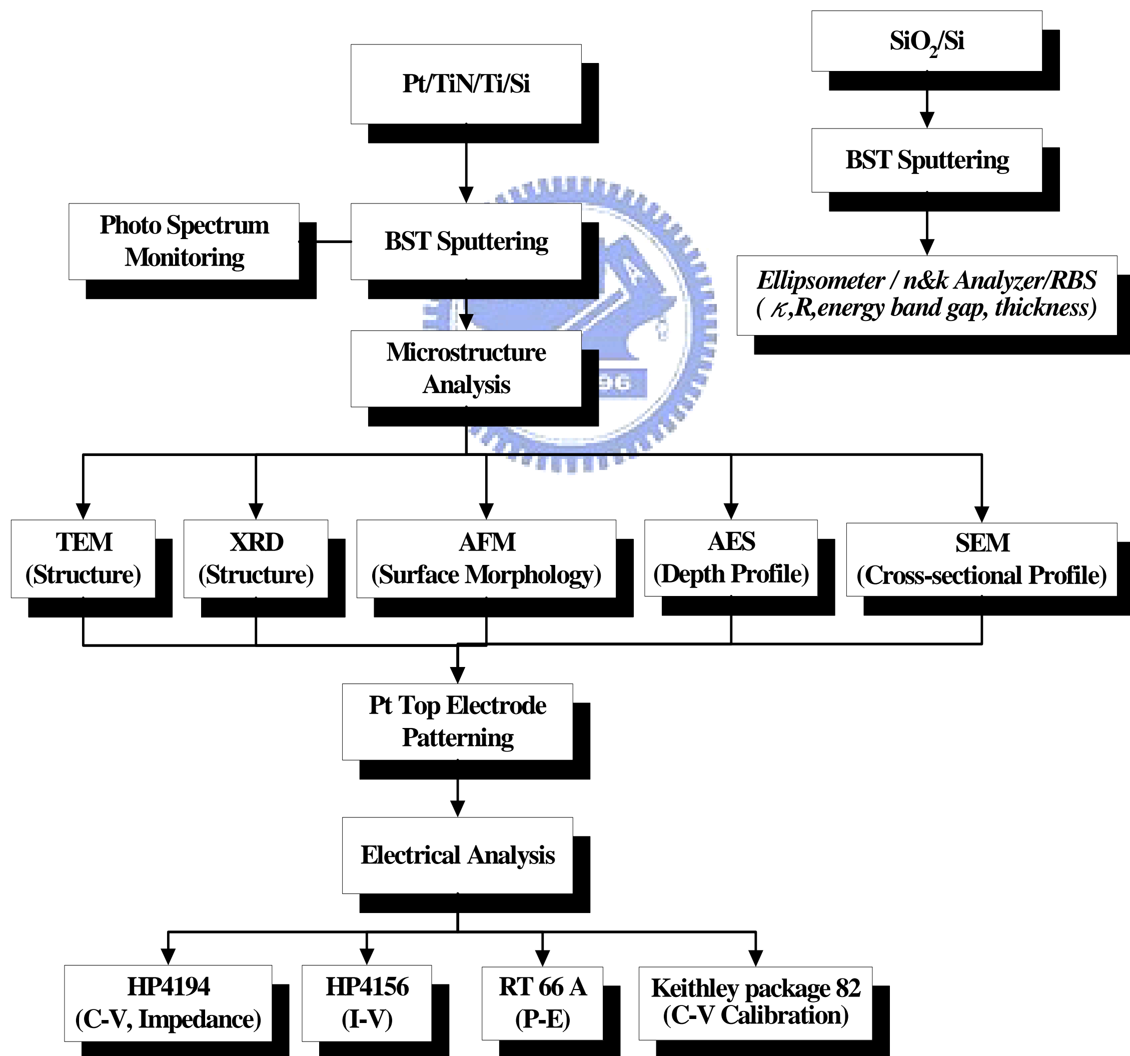


Figure 3-2 The experimental flow of the processes and the analysis for the BST capacitor formation.

as a thermal probing capacitor to avoid the thermal probing-stress. The manufacturing flow is indicated as Fig. 3-4, which indicates the Pt electrode was patterned by lift-off technology. The ultra-thin Cr layer (2nm) was fabricated as BST/ultra-thin Cr/BST multilayer film, which was integrated into BST capacitor as a thermal stable structure. The techniques of nano scale analysis were applied on this BST/Cr/BST multilayer to discover the mechanisms of those temperature-electric properties. The detailed experimental procedures will be discussed in the next several chapters.

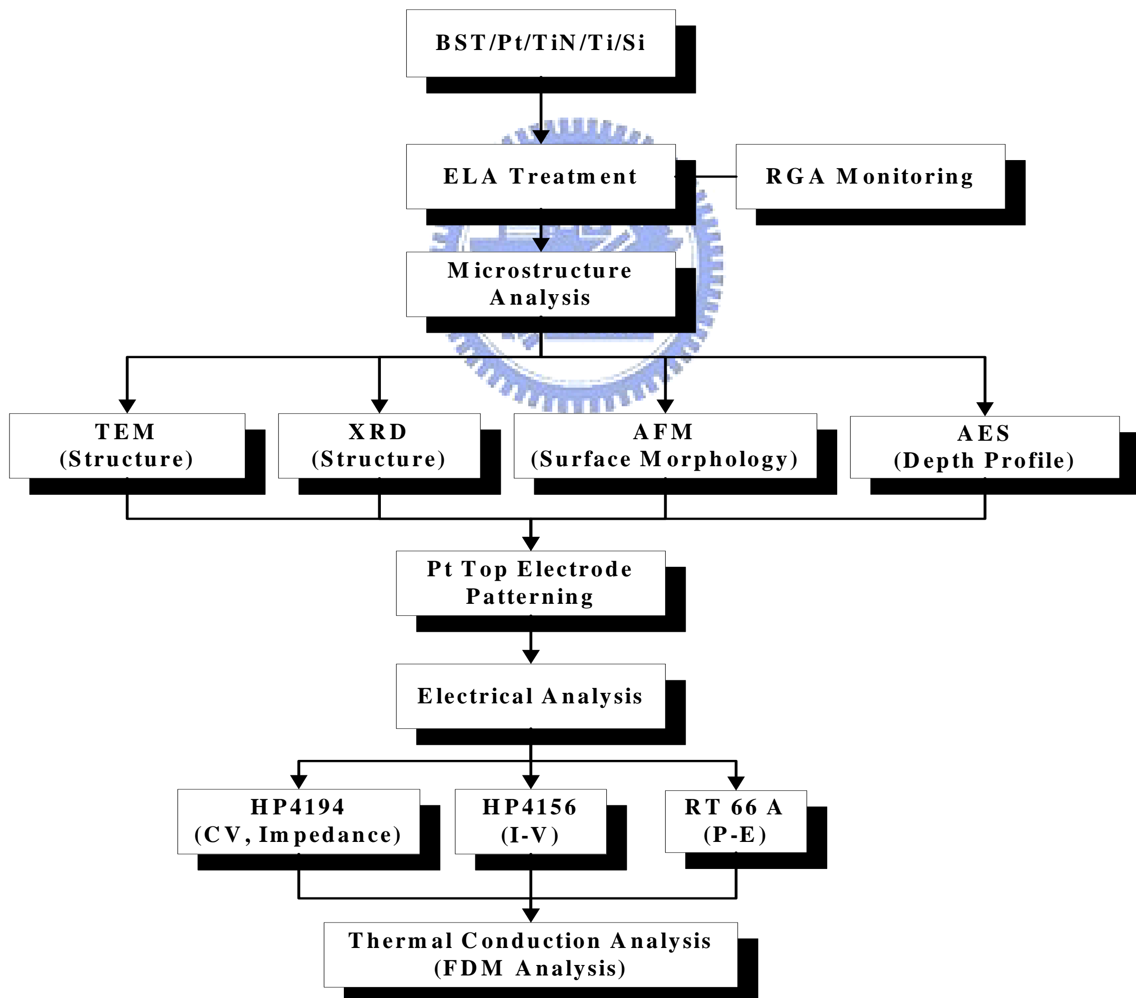


Figure 3-3 The experimental flow of the processes and the analysis for the ELA treatments.

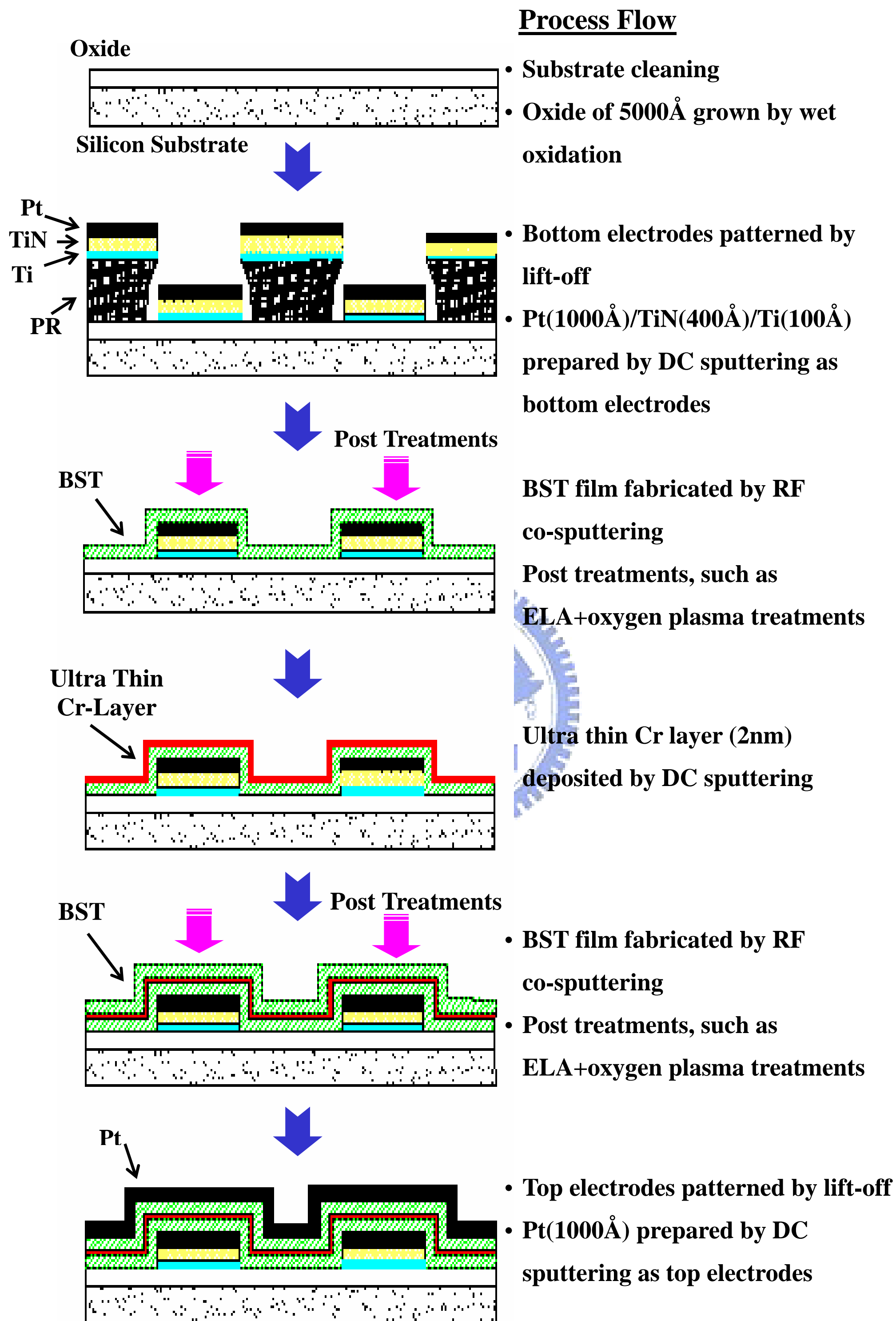


Figure 3-4 Fabrication process of the thermal testing capacitor with intercrossing electrodes

3-2 Sample Preparations

3-2.1 BST film fabrications

In this study, all of the BST films were fabricated by the RF magnetron co-sputtering. Figure 3-5 sketches the sputtering system is composed of the following portions.

(1) Sputtering chamber system consists of the chamber, vacuum components, vacuum pumps, and environmental sensing units. The base pressure of the sputtering system was maintained at 7×10^{-7} torr.

(2) Substrate holder and lamp heater. The distance is 17 cm between the substrate and

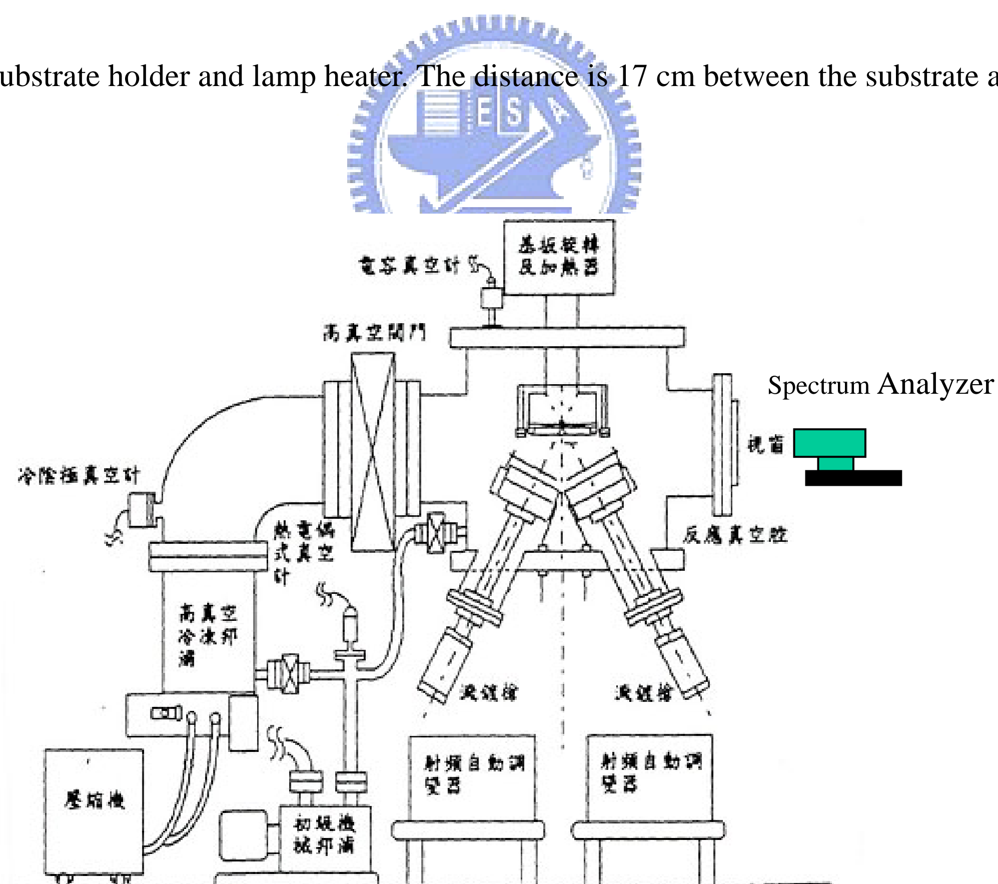


Figure 3-5 The schematic diagram of the RF magnetron co-sputter system.

Sputtering Condition	
RF Power	**BTO/STO 175/230(W/W)**
Target Size	**4-inch**
Substrate Temperature	**27~400 ^{o}C**
Ar Flow Rate	**40~80 sccm**
O2 Flow Rate	**0~40 sccm**
Gas Pressure	**6 ~ 40 mtorr**
Deposition Time	**40~80 mim**

Table 3-2 The process conditions of BST deposition.

target. The thermal couple wire directly contacts both of the front side and back side of the wafer to calibrate the measuring temperature.

(3) Gas supply, mass flow controller and pressure control system.

(4) Plasma spectrum analyzer.

(5) RF power supply and the RF sputtering gun. The angle is about 41° between the vertical and the normal of the target.

The BST film was fabricated onto the Pt/TiN/Ti/Si substrate using both of $BaTiO_3$ and $SrTiO_3$ targets simultaneously. The sputtering conditions are listed in the Table 3-2. Pt top electrodes were deposited on BST films by dc sputtering with 150 μm diameters of top electrode area defined by the shadow mask.

3-2.2 Post treatments

The low-temperature prepared BST films were post treated by excimer laser annealing (ELA) and oxygen plasma treatment. The main parts of the KrF excimer laser system are composed by a gas-discharge tube, optical system and bias power controller. KrF excimer laser is a four-level energy principle system, as shown in Fig 3-6 (a). Utilizing gaseous discharge to make high speed electron pumping and stimulate the gas ions the inversion of electrons and photons can be achieved and a 248-nm coherent laser

(a)

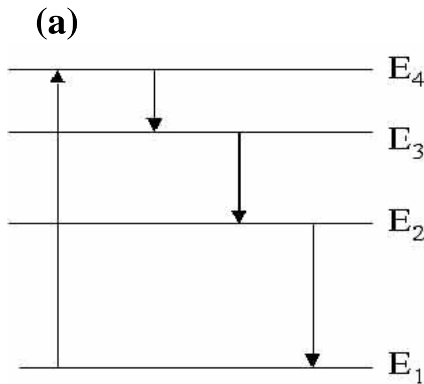
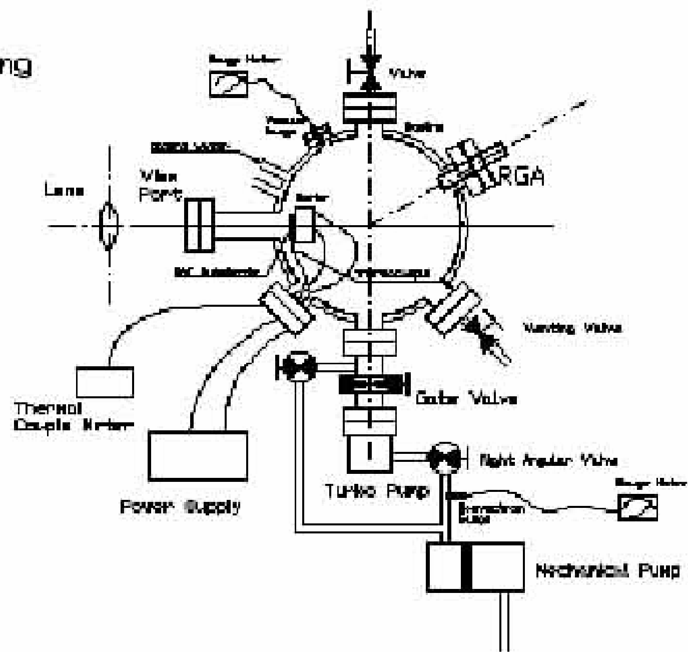


Figure 3-6 (a) The four-level energy system (KrF excimer laser) scheme and (b) ELA system.

(b)

Excimer Laser Annealing System

※1. Main chamber
※2. Lens
※3. Thermal couple and meter
※4. Heater and power supply
5. Turbo pump
※6. Mechanical Pump
7. Gate valve
※8. Angular valve
※9. Meter
※10. Target holder
※11. Cooling System
※12. Vacuum Gauge
※13. Vacuum Gauge Meter
※14. Heating Tape
※15. Residual Gas Analyzer



beam is radiated. Furthermore, Fig 3-6 (b) shows the annealing system, including laser optical system, chamber/vacuum system and substrate holder. The escaped oxygen from BST films was detected in-situ using a residual gas analyzer (RGA) during ELA processing. The oxygen plasma treatment was performed at a standard plasma treatment system under a low power of 300 Watt and short action time period. The detailed experimental conditions of the post treatments will be described in Chapters 4 and 5.

3-3 Characteristics Analysis

3-3.1 Physical characterization techniques

(1) Scanning Electron Microscope (SEM):

The thin film surface morphology, the cross sectional profile and the film thickness were examined by scanning electron microscopy (SEM) using Hitachi model S4000.

(2) X-Ray Diffraction (XRD) Analysis:

The microstructures of the thin films were characterized by a Siemens D5000 Diffractometer with Cu Ka-1 radiation. Two diffraction methods were generally

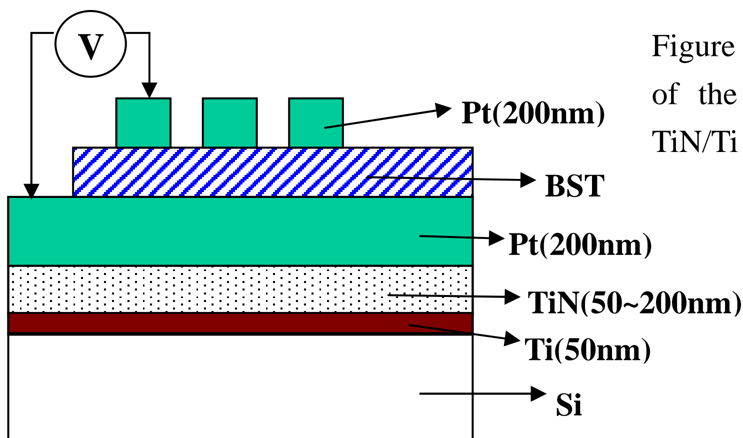
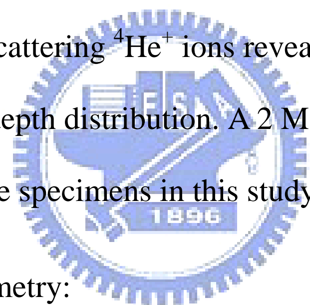


Figure 3-7 The schematic diagram of the MIM testing sample with TiN/Ti barrier layers.

used. For the theta-2 theta powder method, the detected X-ray beams are diffracted from the lattice-planes that are all parallel to the substrate. However, for glancing angle method, the normals of diffracted lattice planes are not parallel to each other and incline at various angle to the substrate. The powder method is suitable for comparison with standard X-ray powder diffraction data to find the preferred orientation in the films. The glancing method is good for phase identification and provides some "information" about orientation distribution.

(3) Rutherford Backscattering Spectroscopy (RBS):

RBS was used to analyze the composition of BST films. Quantity/energy measurements of the backscattering $^4He^+$ ions reveal the information of the elements, such as concentration and depth distribution. A 2 MeV $^4He^+$ ion beam, as an incident resource, was applied on the specimens in this study.



(4) N&k Analyzer and Ellipsometry:

The BST film thickness, reflectivity and extinction coefficients were measured by n&k Analyzer type 1200 (by n&k Technology Inc.). A well calibrated ellipsometer (Rudolph Auto EL-III), with a wavelength of 6328Å and the refractive index ranging between 1.8 and 2.4, was used to measure the film thickness and the refractive index.

(5) Transmission Electron Microscope (TEM)

The crystallinity and nano-scale structure were examined by the transmission electron microscope (TEM) (JEOL, 2000FXII). The maximum resolution of this instrument is about 0.31nm. The diffraction pattern, bright/dark field image were performed in this investigation.

(6) Auger Electron Spectrum (AES)

Depth profiling was accomplished with incorporated ion guns that enable the specimen surface to be continuously sputtered away while Auger electrons were being detected. Then the inter-diffusion of the elements was investigated.

(7) Atomic Force Microscope (AFM)

The surface roughness and surface morphology were examined by AFM (Digital Instruments Nano-Scope III). The root mean square value of the film roughness was calculated.

3-3.2 Electrical characterization techniques

(1) Current-Voltage Measurements

An automatic measurement system that combines IBM PC/AT, HP4156 and a probe station was used to measure I-V characteristics. Fig. 3-7 shows the metal-insulator-metal (MIM) structures, which was measured for leakage current, dielectric and breakdown characteristics. The capacitors with cap area of 1.766×10^{-4} cm^2 were stressed under various voltage to estimate the time depend dielectric breakdown (TDDB). Conduction mechanisms due to electrode-limited Schottky emission and bulk-limited Poole-Frenkel conduction in the dielectric film were investigated by analyzing current density vs. electric field (J-E) curves.

(2) Capacitance-Voltage Measurements

Computer-controlled Keithley package 82 system was used to obtain high frequency C-V and quasi static C-V simultaneous curves. Block diagram of the package 82 system is shown in Fig. 3-8. The package 82 system includes a model 590 CV analyzer for high frequency C-V measurement, a model 595 quasi static C-V meter

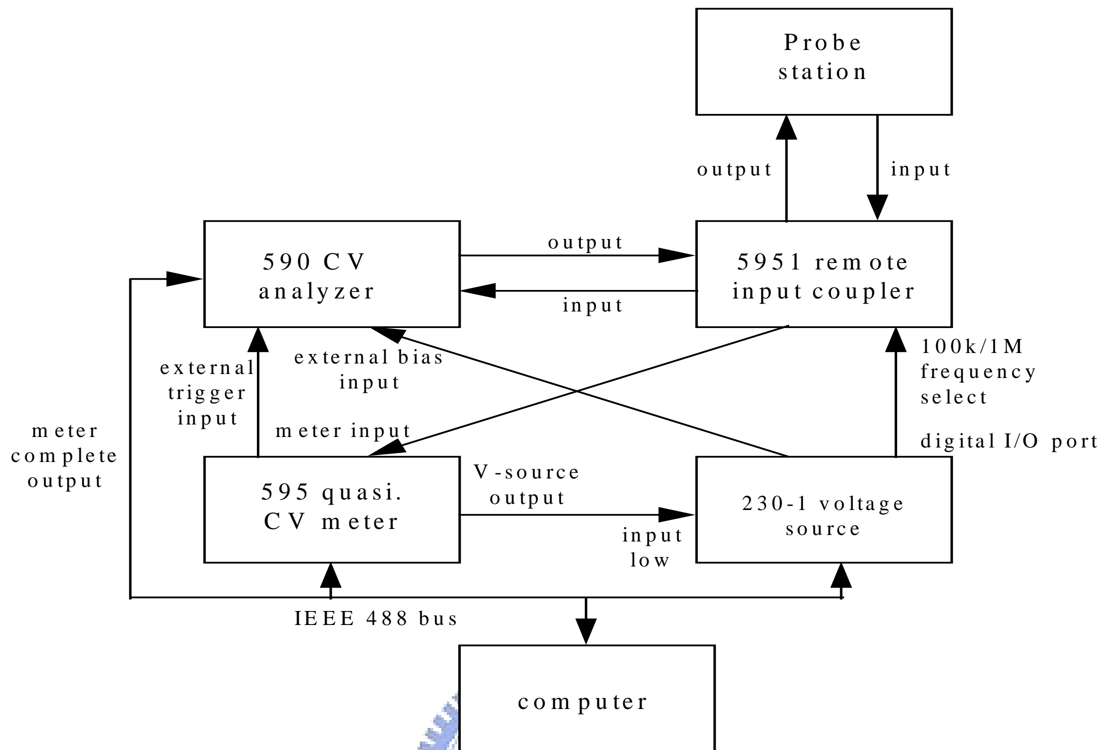


Figure 3-8 Block diagram of the Keithley C-V package 82 system.

along with the 595 remote coupler, lower noise BNC cables and IEEE 488 bus. An noticeable feature of package 82 system is the software analysis of semiconductor parameters such as band bending, doping profile, fixed oxide charge and interface state density. A model 230-1 voltage source and a model 5905 calibration source are included too. In this work, five high frequency C-V data at 100 kHz were taken on the capacitor with an area of 5.1x10^{-4} cm^{2} to determine the capacitance value in the accumulation mode on 3-inches wafers.

The dielectric constant was calculated from C-V and ellipsometry measurements using the following relation :

$$C = k * \varepsilon_O * A / d \qquad (3\text{-}1)$$

where

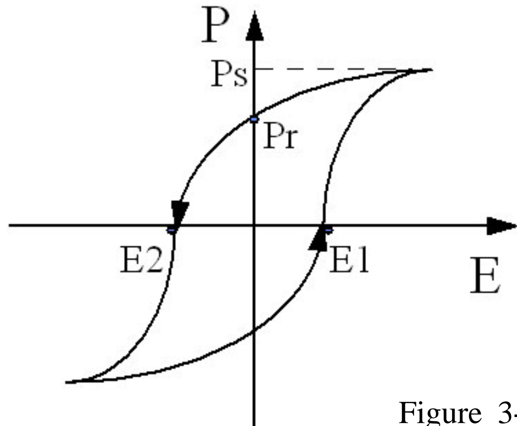


Figure 3-9 The typical hysteresis loop of the P-E curve in ferroelectric state.

A: capacitor area

d: thickness of the insulator

k: dielectric constant

C: the insulator capacitance

Capacitance value was re-checked by using HP4194 (impedance/gain-phase analyzer).

(3) Impedance-Voltage Measurements

Capacitance and tangent loss are functions of frequency, so the impedance/gain-phase analyzer (HP4194) was applied to extract the capacitance-frequency (C-f) and loss tangent-frequency (tanδ-f) data. The frequency of HP4194 ranges from 100 Hz to 15 MHz. The capacitance was doubly checked by Keithley C-V at 100 kHz, comparing the results with the data obtained from HP4194. Tangent loss is an indicator of resistive leakage. The leakage path is parallel to the capacitance in the equivalent circuit. If the loss tangent increases, the impedance will decrease, then the leakage current will increase. The admittance and impedance spectra were measured as a function of

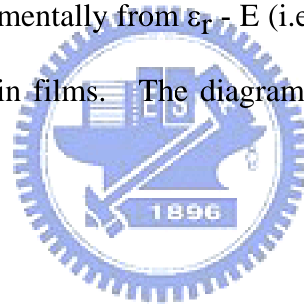
frequency with HP 4194A impedance gain phase analyzer and the temperature was varied from 300 to 423 K. The ac electrical data, in the form of parallel capacitance and conductance, were recorded in the frequency range of 100 Hz to 10 MHz at the AC signal amplitude of 0.1 V.

(4) Polarization Measurements

The P-E curve can be obtained analytically by calculating the polarization P from the ε_r - E using the following equation:

$$P = \varepsilon_o * \int (\varepsilon_r - 1) dE \qquad (3\text{-}2)$$

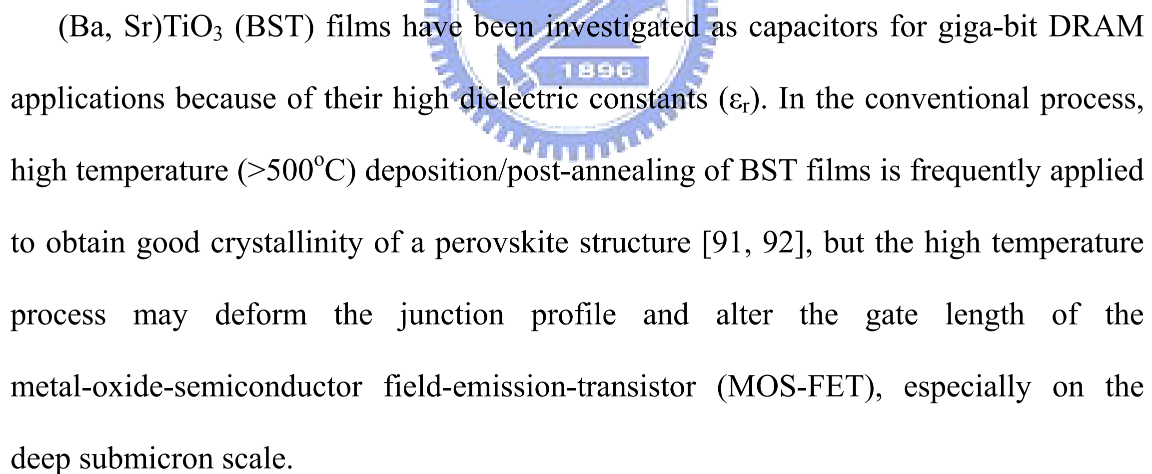
where ε_r is obtained experimentally from ε_r - E (i.e. C-V) data. Fig. 3-9 shows the P-E curves of dielectric thin films. The diagram of polarization vs. electric field can be obtained by Eq. 2-2.



Chapter 4

BST Thin Films Prepared by RF Co-Sputtering Technique at Low Substrate Temperature

4-1 BST/Pt/TiN/Ti/Si Multifilm Sputtered at Low Temperature



(Ba, Sr)TiO_3 (BST) films have been investigated as capacitors for giga-bit DRAM applications because of their high dielectric constants (ε_r). In the conventional process, high temperature (>500°C) deposition/post-annealing of BST films is frequently applied to obtain good crystallinity of a perovskite structure [91, 92], but the high temperature process may deform the junction profile and alter the gate length of the metal-oxide-semiconductor field-emission-transistor (MOS-FET), especially on the deep submicron scale.

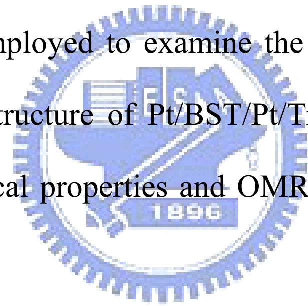
Besides, the metal/TiN/Ti/polysilicon-plug structure is generally proposed as a bottom electrode of a standard COB-DRAM-Capacitor [93, 94]. The Pt/TiN/Ti/Si substrates exhibit better adhesion and interfacial stress than Pt/SiO2/Si substrates, but the interdiffusion and chemical reaction of TiN/Ti layers should be carefully controlled. The Ti layer forms $TiSi_x$ to improve the adhesion and the contact properties between

TiN and polysilicon, and the TiN barrier layer prevents diffusion of Ti and Si into the BST films [95, 96]. Nevertheless, Ti was reported to diffuse through the Pt/TiN layer into the BST film to form TiO_x and oxygen vacancies, when the substrate temperature exceeds 450°C [96, 98, 116, 119]. Hence, a TiO_x series capacitor (C_s) with a smaller ε_r, formed at the interface between the BST and the bottom electrode, degrades the total capacitance of the storage node. However, the oxidation of diffused Ti or Si produces oxygen vacancies in the BST films, increasing the leakage current [96, 97]. Given the above important concerns, low temperature techniques for BST film growth are indeed necessary to suppress the degradation of total ε_r and the leakage current, during IC process.

In general, Dual-Gun RF-sputtering-system can reduce the reaction energy than Single-Gun RF-sputtering-system theoretically. The $BaTiO_3$ and $SrTiO_3$, mixed in the same sputtering target for the Single-Gun sputtering, have different activation energies, so sputtering the single target with two phases is more difficult to control the film qualities than sputtering the two individual targets with single phase. In this work, (Ba, Sr)TiO_3 films were deposited by Dual-Gun RF sputtering onto Pt/TiN/Ti/Si substrate using two individual targets, $BaTiO_3$ and $SrTiO_3$, simultaneously. Although a low temperature technique is required for the deposition of BST in the IC process, controlling the crystallinity and dielectric constant is normally more difficult with a low temperature technique than with a high temperature technique. The work pressure, the sputtering gun power and the gas-mixing ratio are the important parameters in the BST film deposition. Controlling the gas-mixing ratio during the sputtering of BST is a critical quality issue since the substrate temperature remains under 450°C. Oxygen

vacancies are generated in BST films sputtered in Ar ambient, because of oxygen degassing [98, 99]. The presence of oxygen vacancies degrades the electrical properties of BST films, so O_2 gas is introduced in the sputtering of BST to compensate these oxygen vacancies.

The effects of the $O_2/Ar+O_2$ ratio (OMR) for the BST/Pt/Oxide films have been reported by Dr. Tsai et. al., but very few works have reported the effects of OMR for the BST films deposited onto the Pt/TiN/Ti/Si substrate using Dual-Gun RF sputtering system [98, 99, 116, 119]. The effects of OMR on the structures and on the dielectric behaviors of BST films using low temperature depositions are investigated. Optical emission spectroscopy was employed to examine the deposition rate of BST films at various OMR. A multilayer structure of Pt/BST/Pt/TiN/Ti/Si was employed to study correlations among the electrical properties and OMR; the corresponding mechanisms are discussed.



4-2 Experiments

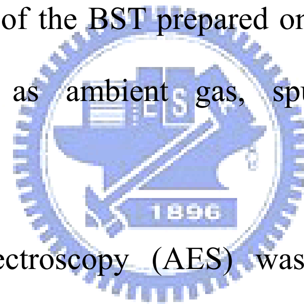
Multilayer specimen of Pt/BST/Pt/TiN/Ti/Si was employed to simulate the practical COB structure of DRAM's capacitor. The starting p-type Si (100) wafers were cleaned by the standard RCA cleaning process. The stacked TiN/Ti layers with 150/50 nm thickness were sputtered onto the Si substrates and RTA treated in N_2 ambient at 600°C for 90 sec. TiN/Ti layers, densified by rapid thermal annealing (RTA), can effectively prohibit the interdiffusion of Ti and Si during the BST thermal process, as reported in our previous works [96, 100, 101]. The bottom electrodes, 150-nm-thick Pt films, were

dc sputtered at room temperature.

There are many controversial arguments about the definition of “substrate temperature”. In general, the thermal couple sensor (TCS) is embedded between the stainless steel holder and wafer backside to prevent the TCS from the plasma damage and disturbance, particularly for the commercial RF-sputtering system. Thus, the substrate temperature of RF sputter system in many reports is measured at the interface between the stainless-steel-holder/wafer-backside [98, 116, 119], and this temperature is much lower than that measured at wafer’s upper surface. Hence, the substrate temperature (300°C), denoted in this paper, was calibrated at the upper surface of the wafer, and the temperature at the wafer-back side is about 410°C. BST films (100 nm) were deposited onto Pt/TiN/Ti/Si at 300°C. The chamber pressure was kept at 7 mtorr, and the O_2/(Ar+ O_2) mixing ratio (OMR) was regulated by gas flow rate. In general, the chamber gas ambient has a lowest fluctuation of the gas mixing uniformity and the flow rate control during RF sputtering. Thus, the larger scales of OMR conditions are chosen as 0%, 5%, 12.5, 25% and 50% in this study to prevent the disturbance of ambient fluctuations during BST film sputtering. $BaTiO_3$ (BTO) and $SrTiO_3$ (STO) targets were used simultaneously. Besides, BaTiO3 and SrTiO3 targets are applied individually to check the deposition rate of BTO and STO thin films. The Ba/Sr ratio can be controlled by tuning the RF powers applied to the targets, and, in the OMR study, the sputtering powers were fixed at 175W and 230W for $BaTiO_3$ and $SrTiO_3$ targets, respectively. Pt top electrodes were deposited on BST films by dc sputtering with 150 μm diameters of top electrode area defined by the shadow mask.

The thickness of BST film was checked by both n & k analyzer (n & k analyzer

1200, n & k Technology Inc.) and field emission scanning electron microscopy (FESEM) (S-4000, Hitachi Co.). Optical emission spectra of plasma near $BaTiO_3$ and $SrTiO_3$ targets were obtained using a 500mm monochromator (SpectroPro-500, ARC Co.) equipped with 1200 g/mm grating. These spectra could verify that the chemical and physical adsorption happened on target surface. X-ray diffractometer (D5000, Siemens Co.) was employed to analyze the film structure and grain size, and the compositions of BST films were inspected by both Rutherford backscattering spectrometer (RBS) and peak shift of X-ray diffraction (XRD) patterns. In addition, the BST films are sputtered onto the SiO_2/Si substrates for the RBS measurements in this study, and the Sr/Ba ratio is reasonable the same as that of the BST prepared on the Pt substrate under the same deposition conditions, such as ambient gas, sputtering powers and substrate temperature.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The Auger electron spectroscopy (AES) was also conducted to study the penetration of oxygen atoms at the Pt/TiN/Ti layers during BST sputtering. Besides, the grain size was doubly checked by FESEM and transmission electron microscopy (TEM). Atomic force microscope (AFM) (DI Nano-Scope III, Digital Instruments Co.) was used to inspect the surface morphology. The capacitance and tangent loss were measured by an impedance/gain-phase analyzer (HP 4194A, Hewlett Packard Co.) and double checked with a C-V analyzer (Package 82 system C-V 590, Keithley Co.). An automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (HP4156, Hewlett Packard Co.) and a probe station was used to measure the leakage current and lifetime.

4-3 *Properties of BST Films Sputtered at Low temperature*

4-3.1 Effects of process parameters during BST sputtering

Figure 4-1 shows a cross-sectional FESEM micrograph of the BST/Pt/TiN/Ti/Si capacitor, with the BST film deposited at 300° C. Fig. 4-2 indicates the deposition rate increases as work pressure decreases, and the deposition rate also dramatically decreases while the deposition Ar gas incorporates with oxygen gas. The mechanism of the BST deposition rate will be discussed in the next section. XRD analysis

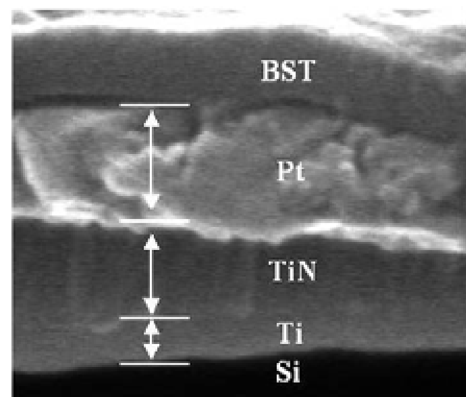


Figure 4-1 Cross-sectional micrograph of BST/Pt/TiN/Ti/Si capacitor.

shows the BST films sputtered at various work pressures behave similar crystallinity, as shown in Fig 4-3. Fig. 4-4 shows the dielectric constant and leakage current density versus work pressure at OMR 12.5%. The dielectric constant behaves a little higher value at 17 mtorr than that at 7 mtorr and 17 mtorr, and the leakage current slightly rises as the work pressure increases. However, the crystallinity, the dielectric properties and leakage current do not exhibit obvious variations for the film deposited

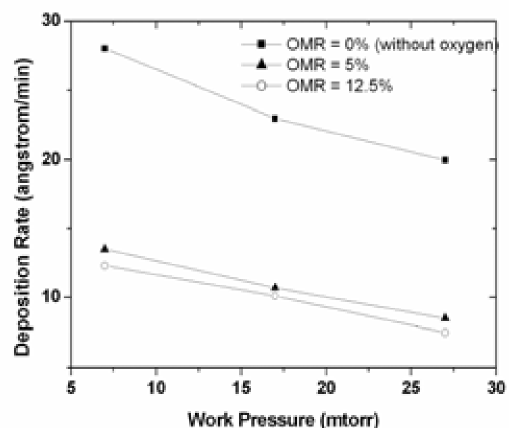


Figure 4-2 Deposition rate versus work pressure for the BST films sputtered at BTO/STO target powers of 175W/230W .

at various work pressures.

The chemical compositions of the (Ba, Sr)TiO_3 (BST) films can be controlled by adjusting the sputtering powers of BTO & STO targets. According to the previous work, the BTO/STO ratio of the BST films behaves as a function of the sputtering powers of BTO and STO targets, and the BTO/STO ratio of 0.4/0.6 can be obtained by the target powers of BTO/STO controlled at 175W/230W in pure Ar ambient gas, as reported by Dr Jiang and Hsu and sketched in Fig. 4-5 [127]. Besides, $Ba_{0.5}S_{r0.5}TiO_3$ films can be also obtained by the same power of 175W/230W in oxygen-Ar mixing ambient gas, and this phenomenon will be discussed in the following section. In the operation temperature, ranging from RT to 120°C, both of the $Ba_{0.4}Sr_{0.6}TiO_3$ and $Ba_{0.5}S_{r0.5}TiO_3$ film behave paraelectric properties, which is indeed necessary for DRAM applications. The crystallinity and grain are also affected by the sputtering powers. The dielectric constant of the films can be influenced by many factors, such as the chemical composition, grain sizes, thickness and crystallinity

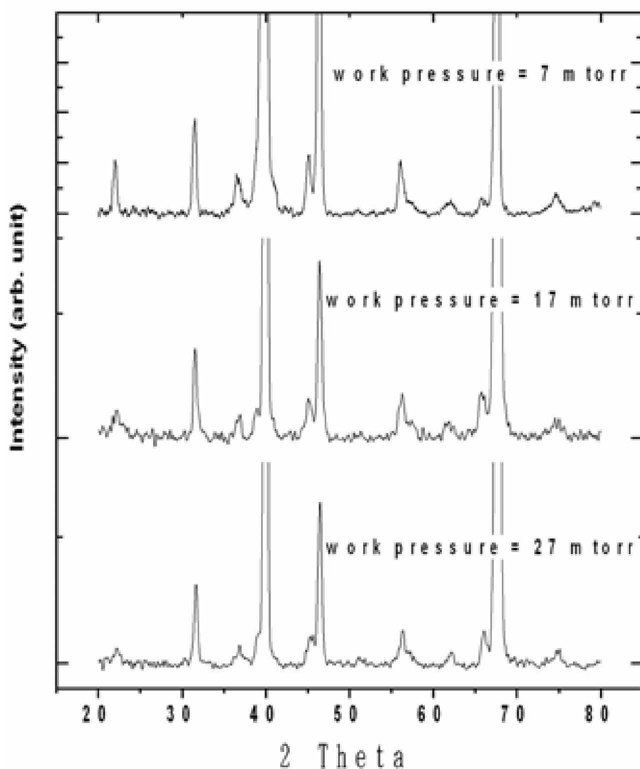


Figure 4-3 XRD patterns of BST films deposited on Pt/TiN/Ti/Si substrates with various work pressure.

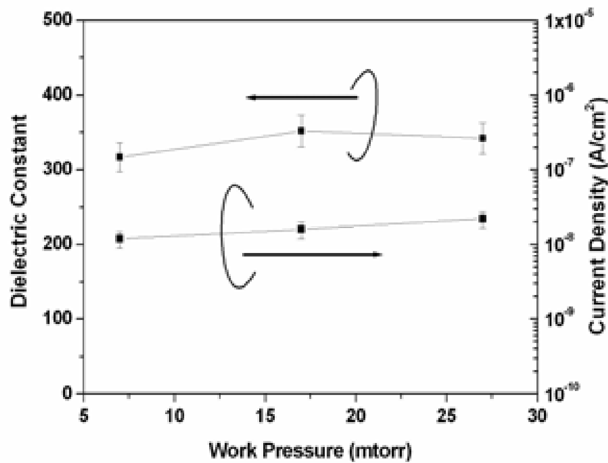


Figure 4-4 Plot of dielectric constant and current density versus work pressure for the films prepared at OMR 12.5%.

[98]. The dielectric constants of the $Ba_{0.4}Sr_{0.6}TiO_3$ and the $Ba_{0.5}S_{r0.5}TiO_3$ films can reach as high as 300 above, and therefore this sputtering power condition of 175W/230W (BTO/STO) will be applied on the succeeding studies.

Figure 4-6(a) reveals that the deposition rate of BST films drops dramatically when oxygen is introduced into the sputtering ambient. Figure 4-6(b) indicates the individual deposition rates of $SrTiO_3$ (STO) and $BaTiO_3$ (BTO), showing the same tendency as Fig. 4-6(a). The optical emission spectra of both Ar and Sr plasma near the STO target were therefore analyzed during sputtering in pure Ar (0% OMR) and 2.5% OMR ambient, as shown in Fig. 4-7. The intensity decay of Sr plasma (λ= 460.7nm, from 0% to 2.5% OMR ambient) is much more prominent (as shown in Fig. 4-7(a), (b)) than that of Ar plasma (λ= 763.5nm, from 0% to 2.5% OMR ambient)(as shown in Figs 4-7 (c), (d)). That is, the generation of Sr plasma is suppressed

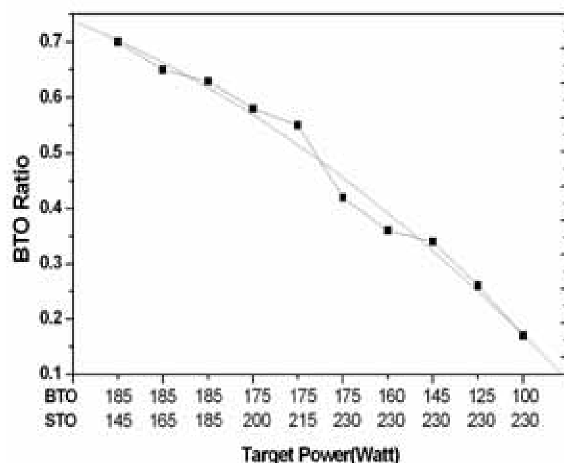


Figure 4-5 BTO ratio of BST films sputtered at various target powers [127].

in the presence of oxygen. The spectra of STO target sputtered in even higher OMR show similar results. These spectra imply that sputtering $SrTiO_3$ molecules with Ar^+ ions in O_2/Ar mixed ambient is difficult. The oxygen ions are reported to induce reactive sputtering and form oxide on the target surface, and the presence of oxide decreases the sputtering rate due to the increase in binding energy of the target surface [102 – 104]. Ba/Sr ratios of BST films prepared on SiO_2/Si substrates were obtained by RBS, as shown in Fig. 4-8. The chemical composition of BST films sputtered in pure Ar ambient shows Sr rich, and the Ba/Sr ratio is around 0.38/0.62. As indicated in Fig. 4-6(b), the deposition rate of STO drops faster than that of BTO when oxygen is applied during sputtering. The Ba/Sr ratio thus increases in the O_2/Ar mixed ambient and remains almost constant at 0.5/0.5 at a higher OMR (≧ 5%) for fixed sputtering powers, as shown in Fig. 4-8. The dielectric constant of powder BST generally increases with Ba/Sr ratio, but that of thin BST films must be considered with several other factors, as discussed later.

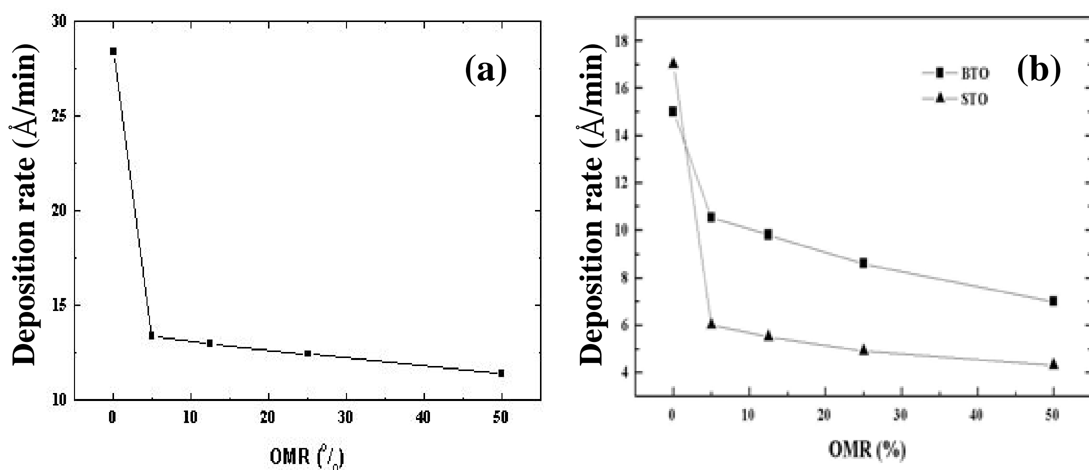


Figure 4-6 Deposition rate of (a) BST films, (b) individual STO and BTO films versus OMR with sputtering power 230W/175W applied on STO/BTO targets respectively.

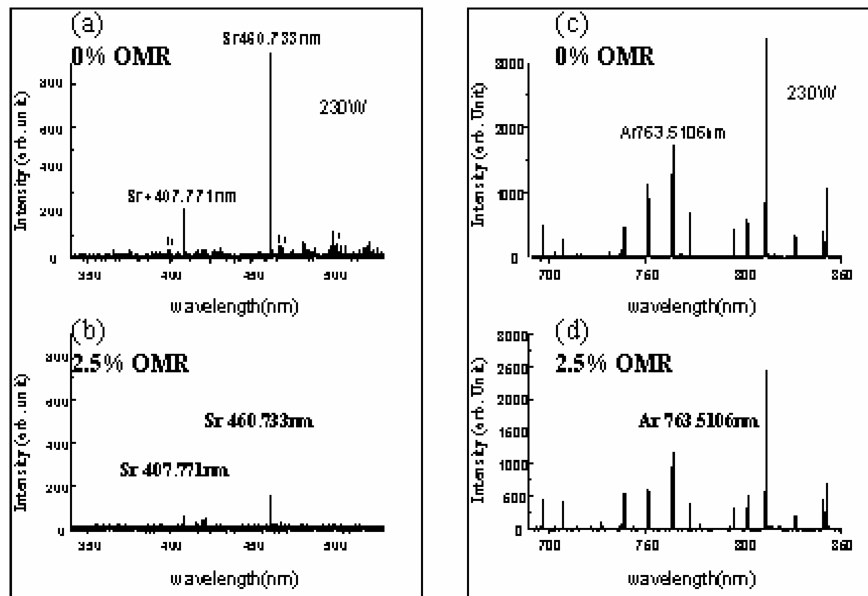


Figure 4-7 The plasma spectra of (a) Sr plasma in pure Ar ambient, (b) Sr plasma in 2.5% OMR, (c) Ar plasma in pure Ar ambient and (d) Ar plasma in 2.5 % OMR, all detected near $SrTiO_3$ target.

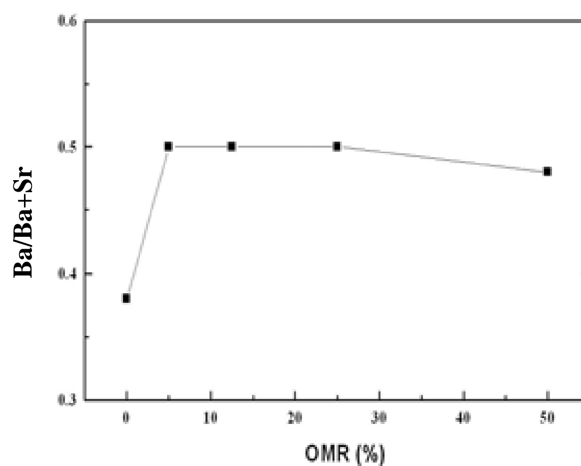


Figure 4-8 The Ba/Ba+Sr ratio of BST films prepared in various OMR.

4-3.2 Material and electrical analysis of sputtered BST thin films

Figure 4-9 gives XRD patterns of BST films deposited at various OMR. Among the conditions studied, BST film deposited in 12.5% OMR exhibits a best crystallinity.

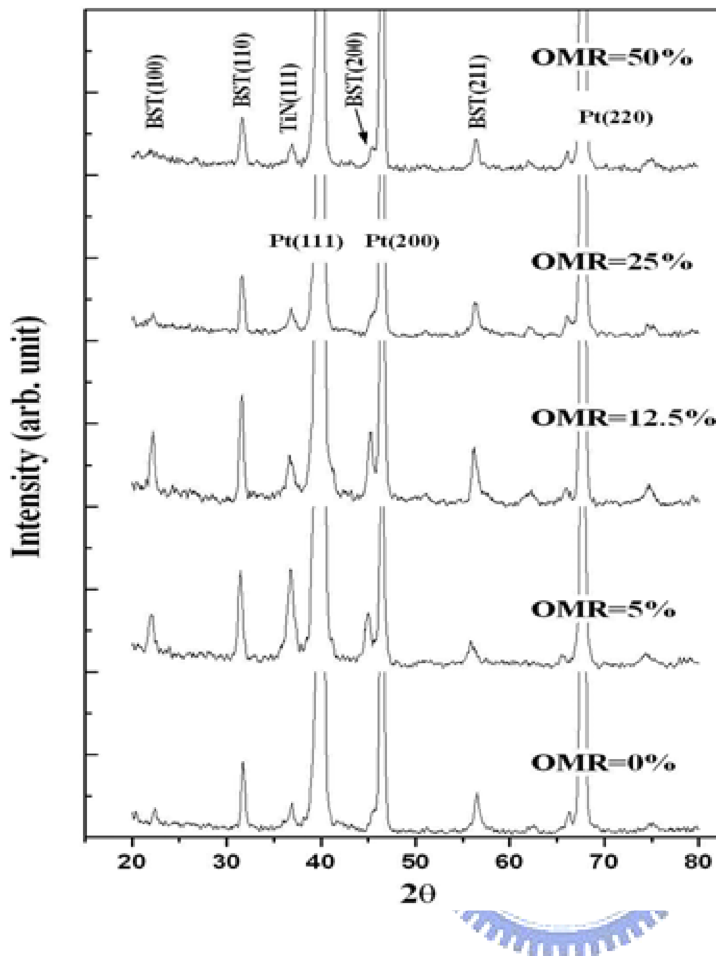
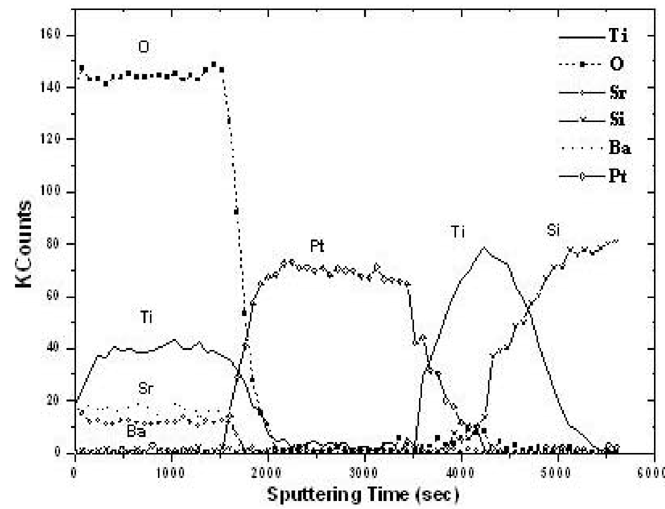
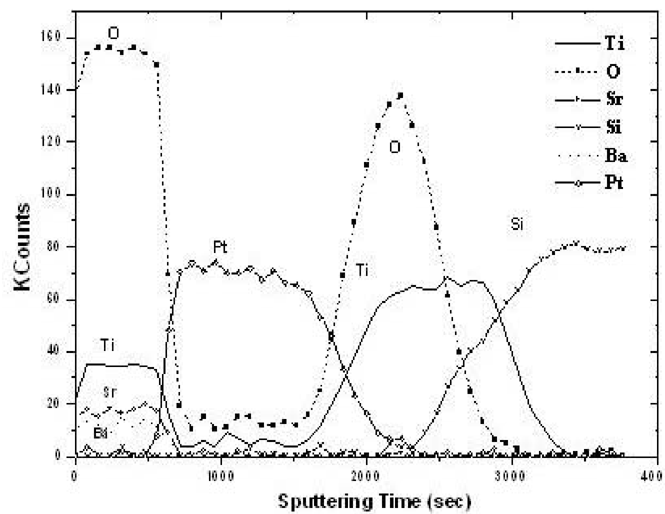


Figure 4-9 XRD patterns of BST films deposited on Pt/TiN/Ti/Si substrates with various OMR.

Figure 4-10 (a) and (b) indicates the Auger electron spectroscopy (AES) spectra of the BST films sputtered in 5% and 25% OMR, respectively. No oxygen atoms penetrate into the TiN/Ti layers under 5% OMR, as shown in Fig. 4-10(a), but, intriguingly, the oxygen atoms penetrate into the TiN/Ti layers at 25% OMR, as shown in Fig. 4-10(b). According to Fig. 4-9, the XRD intensity of TiN(111) is strongly enhanced at 5% OMR, but that degrades above 12.5% OMR. The deposition rate of the BST films sputtered in 5%OMR is much lower than that in 0% OMR, so the longer thermal cycling time will enhance the crystallinity of TiN/Ti layers. On the other hand, Fig. 4-10 (b) indicates the oxygen atoms penetrate the Pt film into TiN/Ti layers above 12.5% OMR, and thus the TiN/Ti layers react with the oxygen atoms, degrading this substrate. The crystallinity of



(a)



(b)

Figure 4-10 AES spectra of BST films sputtered in (a) 5% and (b) 25% OMR.

the BST film is strongly affected by the qualities of Pt/TiN/Ti substrate, as reported in previous works [96, 100, 101]. Hence, the crystallinity of the BST films degrades above 12.5% OMR due to the TiN/Ti substrate damaged by the penetrating oxygen atoms.

The grain size of BST films is estimated from the Full Width at Half-Maximum (FWHM) of the XRD patterns, using the Scherrer formula (grain size <100nm):

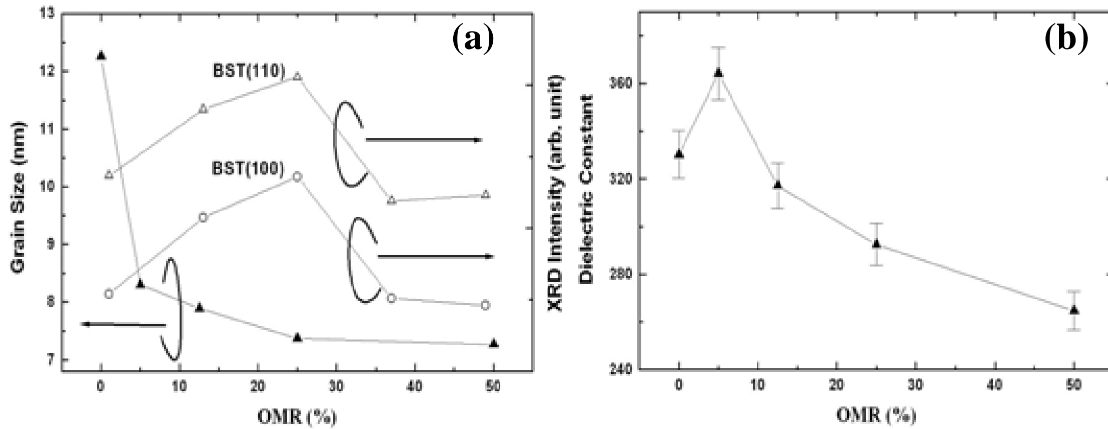
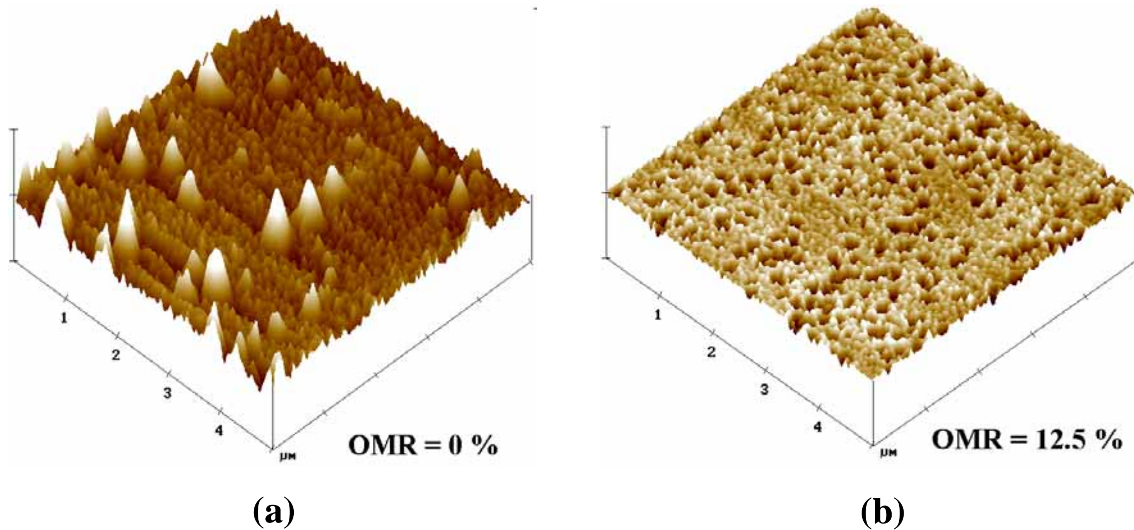


Figure 4-11 (a) Grain sizes and relative XRD intensities of (100) and (110) textures for the BST films sputtered at various OMR; (b) Dielectric constant of BST films prepared at various OMR.

$$Dcal=0.89\,\lambda\,/\,(\,B\times\cos\theta\,) \qquad (4\text{-}1)$$

where Dcal is the mean calculated grain size; λ is the X-ray wavelength (~0.154nm); B is the FWHM of the XRD peak, and θ is the diffraction angle [105]. The FWHM of the (110) peak increases with OMR, and the calculated grain sizes are deduced by Eq. 4-1. Besides, an estimation of grain size from the FWHM is distorted by interfacial stress, so the calculated grain size should be modified by a factor obtained from a reference sample using FESEM imaging. The real grain size is around 8.3 nm at 5% OMR, as reported in previous work [106]. Thus, the calculated grain size should be multiplied by a factor of 1.22 to estimate the real grain sizes under the same substrate conditions.



(a) **(b)**

Figure 4-12 AFM images of BST films deposited in (a) 0% OMR (R_{RMS} = 5.06 nm) and (b) 12.5% OMR (R_{RMS} = 2.46 nm).

In this study, relative grain sizes are much more important than absolute grain sizes. The small grain sizes of BST films decrease from 15 nm to 7 nm as OMR increases from 0 to 50%, as depicted in Fig. 4-11(a), suggesting that films prepared at a higher OMR have a smaller grain size; other work has revealed a similar trend [98, 99, 107]. Besides, Fig. 4-11(a) indicates that the strongest peaks of BST (100) and (110) textures are obtained for the samples sputtered at 12.5% OMR. Moreover, Fig. 4-11(b) shows that the dielectric constant increases with OMR, reaching a maximum of 364 at 5% OMR, and then decreasing as OMR increases further. Figure 4-11(a) shows that best crystallinity occurs at 12.5 % OMR and the grain size of the film shrinks as OMR increases. Many factors influence the dielectric constant of BST films such as composition, crystallinity, grain size and interface quality. A high Ba/Sr ratio and good crystallinity enhances the polarization of electric dipoles in a single grain [91, 98, 108], but a small grain size tends to depress the dielectric constant, as reported in previous

work [98, 99, 109]. Hence, the dielectric constant is inferred to increase as the crystallinity improves and as Ba/Sr ratio increases; but over 5% OMR the grain size effect dominates and the dielectric constant decreases as OMR further increases.

Figures 4-12 (a) and (b) present the AFM micrographs of BST surface morphology: the films deposited at a higher OMR have smoother surface. According to Fig. 4-12(a) and (b), the root mean square roughness (R_{RMS}) for films deposited in pure Ar ambient is 5.06 nm, while that for films prepared at 12.5% OMR is 2.46 nm. Smaller grain and a lower film deposition rate at higher OMR may result in a smoother surface.

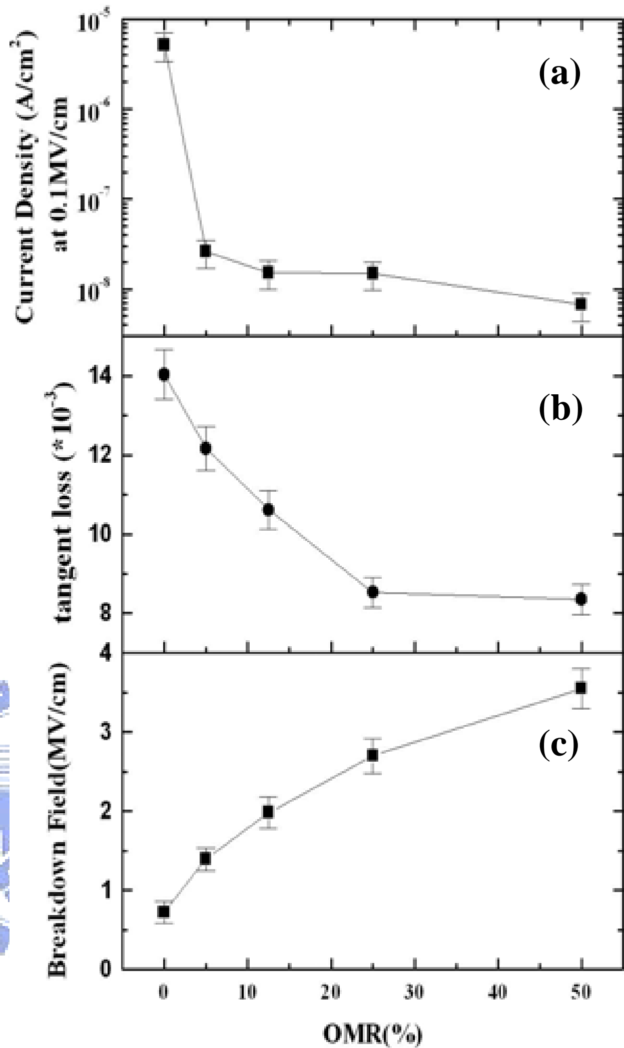


Figure 4-13 (a) Leakage current density, (b) tangent loss, and (c) the time-zero dielectric breakdown (TZDB) field of Pt/BST/Pt capacitors prepared in various OMR.

Figure 4-13(a) indicates the leakage current density decreases as OMR increase. The leakage current of Pt/BST/Pt capacitors may be affected by three factors, namely, the oxygen stochiometry in the BST films, surface morphology and the grain boundary.

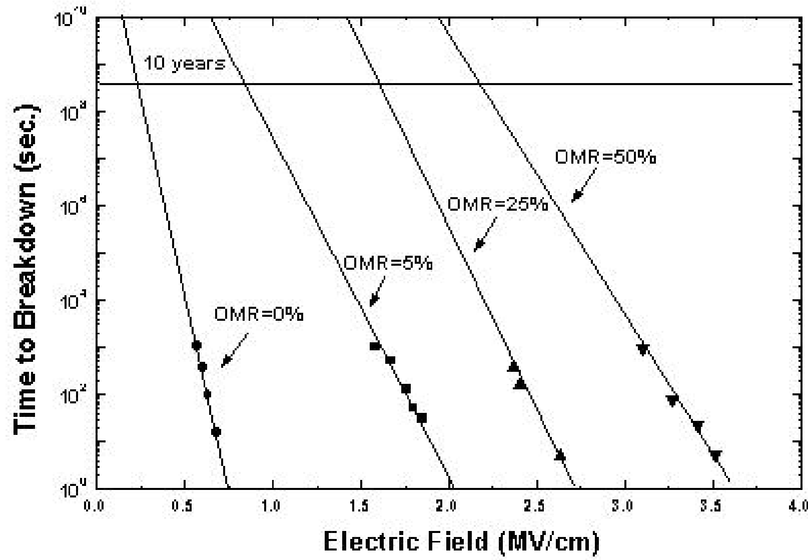


Figure 4-14 TDDB as a function of electric field of BST films deposited in various $O_2/Ar+O_2$ ratio (OMR).

Firstly, the oxygen stochiometries are different for the BST films prepared in various OMR ambient, according to the following reaction:

$$O_o \leftrightarrow V_o^{\bullet\bullet} + 2e' + \tfrac{1}{2} O_2 \qquad (4\text{-}2)$$

where O_o , $V_o^{\bullet\bullet}$ and e' represent the oxygen ion on its normal site, the oxygen vacancy and the electron, respectively. More oxygen vacancies yield a larger leakage current, causing a BST film form to act as an n-type semiconductor [110, 111]. Secondly, smoother surface morphology can prevent the lowering of barrier height by interfacial defects and reduce the local concentrated field to suppress the emission current [112, 118, 121]. Thirdly, a BST film, with a narrow band gap of 3.2eV~4.0eV, can normally be considered as semi-insulator or semiconductor, so the grain boundary scattering suppresses the current [113 – 115]. The reduced grain size with higher OMR forms more grain boundaries to decrease the leakage current. Hence BST films deposited in

higher OMR ambient exhibit compensation of oxygen vacancies, smoother interfaces and smaller grains, all of which reflect the decrease of the leakage current. Figure 4-13(b) shows the tangent loss of BST films versus OMR. Tangent loss proceeds by two mechanisms- resistive loss and relaxation loss [116]. In resistive loss case, energy is dissipated by mobile charges, and the tangent loss depends on the magnitude of leakage current; in relaxation loss case, energy is dissipated by relaxation of dipoles, and the tangent loss is proportional to the dielectric constant. Comparing Fig. 4-13(a) and (b) reveals that the trend of the tangent loss against OMR is similar to that of leakage current. Hence, the resistive loss dominates the tangent loss. Figure 4-13(c) indicates that the time-zero dielectric breakdown (TZDB) of the Pt/BST/Pt capacitor is enhanced by increasing OMR. BST films sputtered in higher OMR exhibit a higher breakdown field because of their smaller grain size and fewer oxygen vacancies [98, 117].

The BST films deposited in higher OMR have a longer lifetime, as indicated in Figure 4-14. Time-dependent dielectric breakdown (TDDB) is referred to as the resistance degradation of the dielectric ceramic, which slowly increases the leakage current under constant temperature and dc field stress [96, 98, 125]. The mechanisms of resistance degradations in perovskite films may be generally categorized into the grain boundary model and the reduction model [123 – 125]. The grain boundary model suggests the presence of very large potential drops across the grain boundaries due to the boundaries' high resistivities. The films with smaller grain sizes form more grain boundaries which the drops in voltage are shared, so the resistance degradation is suppressed. On the other hand, the reduction model suggests that oxygen vacancies and injection electrons cause resistance degradation, which can thus be retarded by a

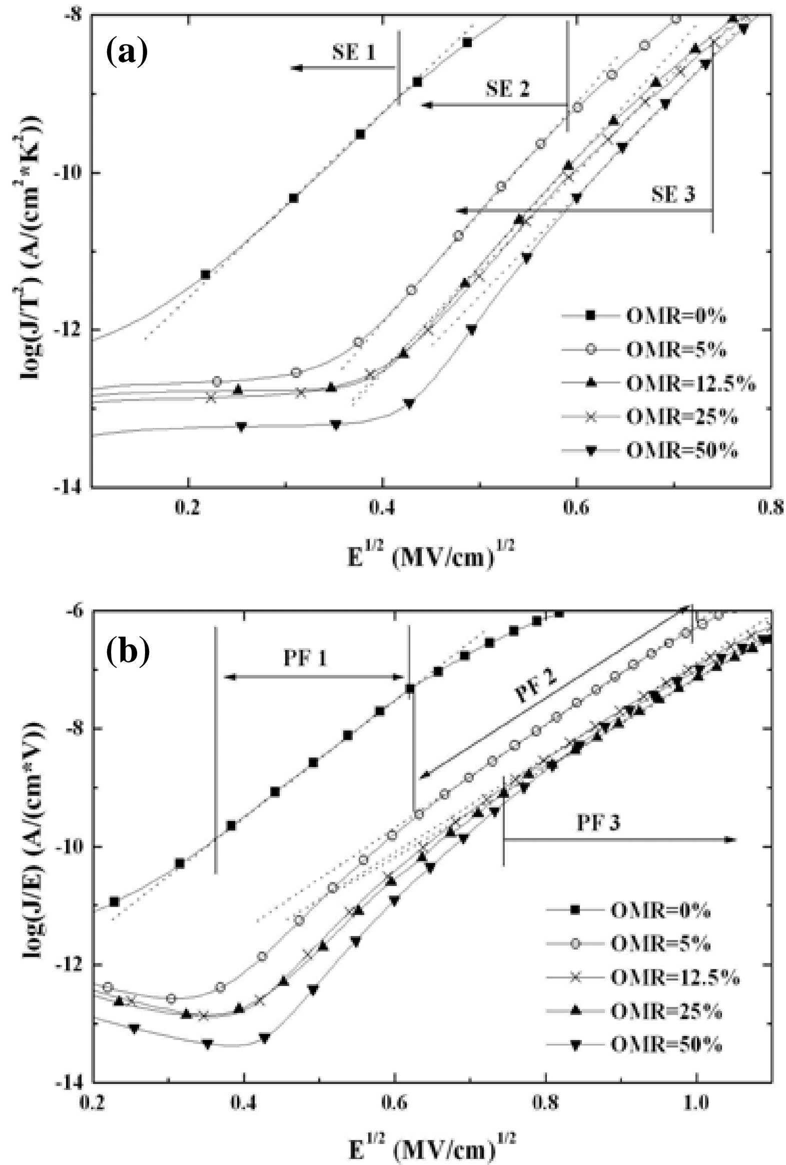


Figure 4-15 (a) The log (J/T^2) versus $E^{1/2}$ plot showing Schottky emission fitting, and (b) the log (J/E) versus $E^{1/2}$ plot showing Poole-Frenkel emission fitting for BST films prepared in various OMR.

smoother surface and lower oxygen vacancy concentration. Hence, BST films prepared with a higher OMR have a longer lifetime, which result can be attributed to the reduction of the grain sizes, compensation of oxygen vacancies and an improved interface.

4-3.3 Leakage current mechanisms

Figure 4-15 gives the current-voltage relationships of Pt/BST/Pt capacitors with various OMR. The conduction mechanisms of metal/BST/metal capacitors are usually interpreted as Schottky emission (interface-limited conduction) at lower electric fields, and Poole-Frenkel emission (bulk-limited conduction) at higher fields [118 – 122]. The leakage current governed by Schottky emission (SE) behavior is expressed as

$$log\,(J_{SE}/T^2) = -q[\varphi_{Bu} - (qE/4\pi\,\varepsilon_d\,\varepsilon_o)^{1/2}]\,/(\,kT.\ \ ln10)+log(A^*) \qquad (4\text{-}3)$$

where, A^* is the effective Richardson's constant; φ_B is the potential barrier height at the surface; ε_d is the dynamic dielectric constant of the ferroelectric material in the infrared region; q is the unit charge; k is Boltzmann's constant; T is temperature, and E is external electric field. The leakage current governed by Poole-Frenkel emission (PF) behavior is expressed as

$$log(J_{PF}/E) = -q[\varphi_t - (qE/\pi\,\varepsilon_d\,\varepsilon_o)^{1/2}]\,/(\,kT.\ \ ln10)+log\,(B) \qquad (4\text{-}4)$$

where B is a constant and φ_t is the trapped energy level. If the conduction current is governed by Poole-Frenkel emission (PF), then a log(J/E) against $E^{1/2}$ plot should be a straight line, the slope of which can be used to deduce the dynamic dielectric constant ε_d [118 – 122]. Similarly, a $log(J/T^2)$ against $E^{1/2}$ plot can be made for Schottky emission (SE). Figure 4-15(a) shows the Schottky emission plot and Fig. 4-15(b) shows the Poole-Frenkel emission plot using the same experimental I-V data in various OMR. The dashed lines are the fitted results. However, the dynamic dielectric constant can be inferred from the optical dielectric constant for an ideal insulating film, and the optical dielectric constant is directly obtained from the square of the refractive index n (ε_{opt} =

n^2) [119 – 122]. Table 4-1 lists the static, dynamic and optical dielectric constants of samples prepared at various OMR. In this work, the range of the dynamic dielectric constants (ε_d) calculated by PF fitting is between 2.3 and 4.3, and that calculated by SE fitting is between 1.75 and 2.1. The range of the optical dielectric constant for BST films sputtered with various OMR, measured using an n & k analyzer with λ = 700 nm, is between 3.5 and 5.5. The consistency between dynamic (ε_d) and the optical dielectric constant (ε_{opt}) is enough to trust the curve fitting, even though ε_d and ε_{opt} revealed some deviation, perhaps due to the fluctuations of material's density and deformation of its lattice.

Figure 4-15(a) and (b) indicate that Pt/BST/Pt capacitor sputtered at 0 % OMR exhibits Schottky / Poole-Frenkel emission under/above160 kV/cm, as denoted in the SE 1/PF 1 regions. Figure 4-15(b) reveals that $\log(J/T^2)$ curves for 5%, 12.5 %, 25% and 50% OMR are independent of the applied field (E) up to 160 kV/cm, possibly because of the dielectric relaxation of BST films; the curves then increase linearly with $E^{1/2}$ above 160 kV/cm. SE 2 and PF 2 regions show SE/PF behaviors under and above 360 kV/cm in 5% OMR, respectively. SE and PF regions in higher OMR (≧ 12.5%) are SE 3 and PF 3 regions, respectively.

Figure 4-16(a) rearranges the tendencies of the leakage mechanisms, and it reveals that the applied-field boundary of SE/PF linear fitting shifts to a higher field as OMR increases. In case 1, the fitting boundary shifts from 160 kV/cm (SE 1/PF 1) to360 kV/cm (SE 2/PF 2), as OMR increases from 0% to 5%, and, in case 2, it shifts to 560 kV/cm (SE 3/PF 3), when OMR is equal to or larger than 12.5%. The electron energy bands of the Pt/BST interface are applied to explain the mechanisms of leakage, as

OMR	Dynamic Dielectric Constant		Static Dielectric Constant	Optical Dielectric Constant
	PF	SE		
0 %	2.30	2.09	330	3.53
5 %	3.19	1.77	364	4.66
12.5 %	4.18	1.91	317	5.29
25 %	4.18	2.01	293	4.28
50 %	4.23	1.98	265	4.34

Table 4-1 The dynamic dielectric constant, static dielectric constants and optical dielectric constants of BST films prepared in various OMR.

presented in Fig. 4-16 (b) and (c). As mentioned above, the BST films can be treated as an n-type semiconductor, and the space charge density of the interfacial depletion region is assumed to be almost equal to the concentration of oxygen vacancies. The relationship between the barrier thickness, *d,* of the interfacial depletion region and the oxygen vacancy concentration can be derived as,

$$d_1/d_2 = [\, N_{VO2}/N_{VO1} \times (1 + kT/\Delta \times \ln(N_{VO1}/N_{VO2}))\,]^{0.5} \qquad (4\text{-}5)$$

where N_{VO} is the concentration of oxygen vacancies; *k* is Boltzmann's constant; *T* is temperature, and *Δ* is the work function difference between Pt and BST. Equation (4-5) reveals that decreasing the concentration of oxygen vacancies increases the barrier thickness, *d,* of the interfacial depletion region [126]. Figure 4-16(b) indicates that the BST films sputtered in pure Ar or in lower OMR ambient have more oxygen vacancies and a rougher surface than those sputter in higher OMR ambient, yielding a higher

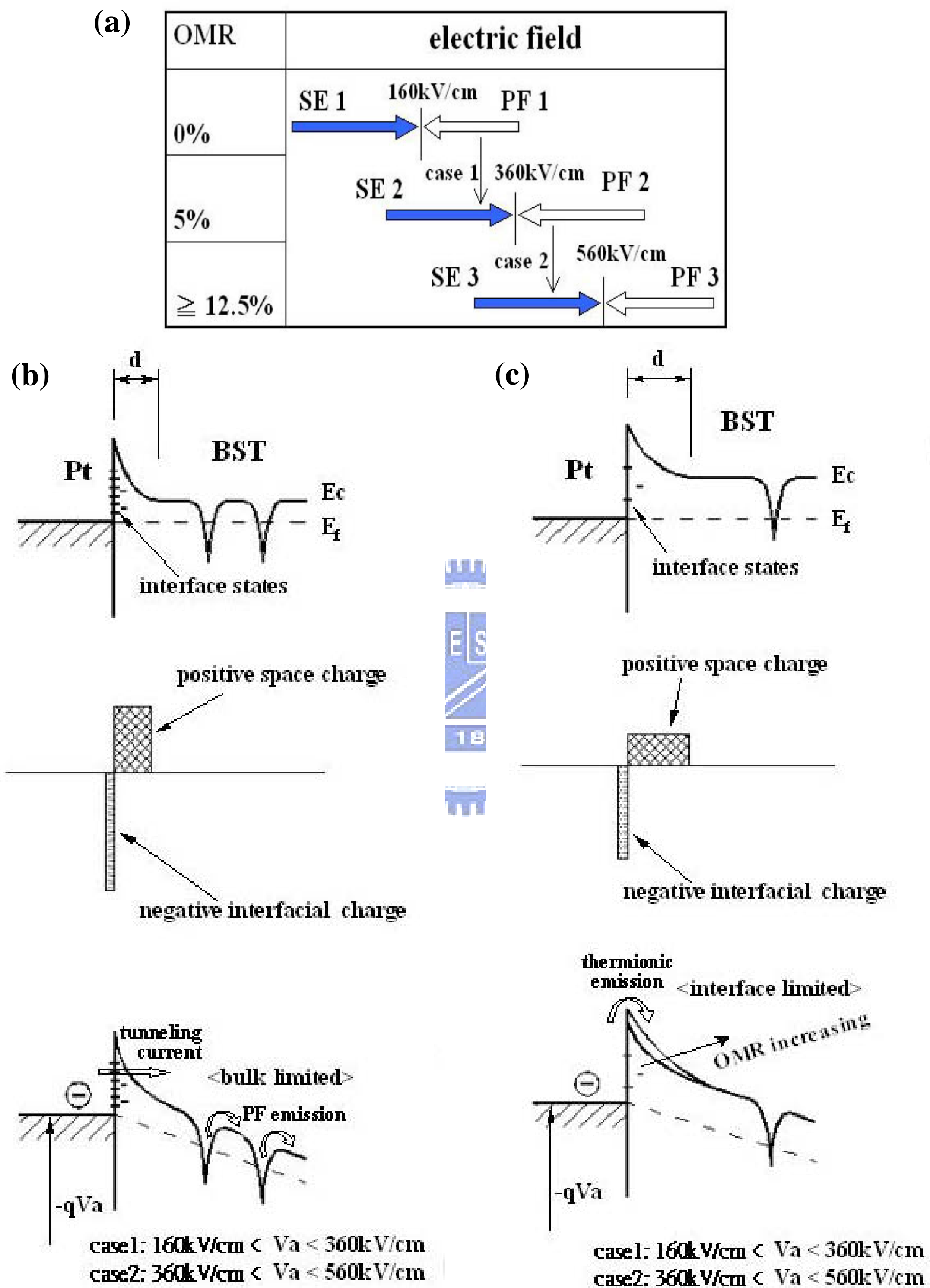


Figure 4-16 (a) the range of applied field for SE/PF mechanism in various OMR ambient, and the diagrams of the electron energy band in (b) pure Ar or lower OMR ambient and (c) higher OMR ambient.

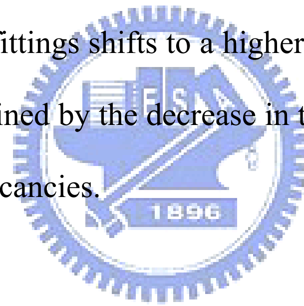
interfacial space charge concentration and many interface states to increase the opportunity of tunneling. Furthermore, the magnitude of the leakage current is governed by the balance among the tunneling current, trapping and detrapping rate. Thus, increasing the applied field induces the field-assisted emission of trapped charged carriers (Poole-Frenkel effect), such that the leakage current will be governed by PF emission rate. The bulk-limited mechanism therefore dominates the leakage current at lower OMR and higher applied field. Figure 4-16(c) shows that increasing OMR yield fewer interface states, a lower space charge density in the interfacial depletion region and fewer trapping states, by causing a smoother interface and compensating oxygen vacancies. Equation (4-5) states that a lower space charge density in the interfacial depletion region results in a thicker barrier, and the presence of fewer interface states greatly reduces the opportunity for tunneling. Hence, thermionic emission (SE behavior) is the dominate mechanism of injecting electrons in higher OMR. Consequently, considering cases 1 and 2 of Fig. 4-16 (a), the mechanism of the leakage current changes from bulk limited emission (PF) to interface limited emission (SE) as OMR increases.

4-4 Summary

The deposition rate of low-temperature sputtered BST decreases as OMR increases, due to the formation of oxide on the target surface by oxygen ions. Introducing proper oxygen gas during sputtering improves the crystallinity and surface roughness of BST films and changes the Ba/Sr ratio, but decreases the grain size. In addition, the excessive

OMR (>12.5%) degrades the crystallinity of BST film due to the TiN/Ti substrate damaged by the penetrations of the oxygen atoms. The dielectric constant is a trade-off determined by compositions, crystallinity and grain size, and the maximum dielectric constant is 364 at 5% OMR. Films prepared at higher OMR have a smaller leakage current density, a lower tangent loss and a longer lifetime, due to compensation of oxygen vacancies, a smoother surface morphology and voltage shared by smaller grains.

This chapter attributed the leakage mechanisms of the Pt/BST/Pt capacitor to Schottky emission(SE)/Poole-Frenkel emission(PF) at lower/higher applied field. Part of PF region changes to SE behavior if OMR increases. In other words, the applied field boundary between SE and PF fittings shifts to a higher field as OMR increases, and this observed I-V behavior is explained by the decrease in the number of interface states and the compensation of oxygen vacancies.



Chapter 5

The Effects and Analysis of Post Excimer Laser Annealing on BST Thin Films at Low Substrate Temperatures

5-1 Brief Concept of BST Films Post Treated by ELA

The low temperature sputtered BST films, lower than 300°C (backside temperature), have poor crystallinity and low dielectric constant, so those films must be post annealed to improve the dielectric properties. ELA can be carried out with low mechanical stress under low substrate temperature, but its process window is very hard to be controlled. This chapter describes how a novel excimer laser annealing (ELA) technique with a wavelength of 248-nm can achieve local-high-temperature heating and recrystallize the amorphous BST films. In addition, the process window of ELA treatment was analyzed by the optical absorption properties and the heat conduction analysis. Besides, material and electrical properties are examined to study the detailed effects of excimer laser annealing on BST films. Contrasting with the experimental results, the theoretical analysis can excellently elucidate that the material and electrical properties are consistent with the thermal distribution during ELA processing.

5-2 Experiments

The structure of Pt/BST/Pt/TiN/Ti/Si was used to simulate the practical capacitor over a bit-line (COB) DRAM capacitor structure. The p-type Si(100) silicon wafers were initially cleaned by the standard RCA cleaning process. Pt/TiN/Ti films of 200/100/50 nm were sputtered onto the p-type Si(100) substrates as the bottom-electrode/barrier/adhesion layers. $(Ba_{0.5} Sr_{0.5})TiO_3$ (BST) films of 20, 50, 100 and 300 nm thick were deposited by RF magnetron co-sputter system with $Ar+O_2$ mixed ambient at a substrate temperature of 150 ^oC (~260^oC at backside). The RF powers for the deposition of $BaTiO_3$ and $SrTiO_3$ were 175 Watt and 230 Watt, respectively.

The as-deposited thin BST samples were then transferred to an evacuated chamber (<10^{-6} Torr). The substrate temperature was elevated to 300^oC (backside temperature). The related investigations have indicated that substrate heating decreases the cooling rate, so the grain growth of BST film can be carried out [128, 129]. The KrF eximer laser with a wavelength of 248 nm and pulse width of 25-nsec was applied to the BST samples. Because the frequency was 20 Hz and shot number was 128, the samples were heated at backside temperature of 300 ^oC for a very short duration. The laser energy fluence (LEF), 45~70 mJ/(pulse × cm^2), is calibrated inside the annealing chamber by a photo-diode-meter, and that is much smaller than the nominal value (125~200 mJ/(pulse×cm^2)), which was directly read from the control panel, due to the laser intensity decayed by the reflecting mirrors and the focus lenses. The escaped oxygen from BST films was detected in-situ using a residual gas analyzer (RGA) during ELA processing. For the study of electric properties, the Pt top electrode with a diameter of 150 μm patterned by the shadow mask process was sputtered onto the BST film.

The reflectivity and extinction coefficients were measured by n&k Analyzer type 1200 (by n&k Technology Inc.). The film thickness of the BST film was examined by scanning electron microscopy (SEM). The crystallinity, texture and grain properties were then characterized by x-ray diffraction (XRD, Siemens D5000 diffractometer) and transmission electron microscopy (TEM). Next, the testing voltage biased on the top electrode, and the bottom electrode is grounded. The capacitance-voltage (C-V) characteristic was measured on the metal-insulator-metal (MIM) structure at a frequency of 100 kHz, and the dielectric constants of the films were calculated from the capacitance without a bias voltage. The dielectric properties and tangent loss were analyzed with an HP 4194A impedance-gain phase analyzer. An automatic measurement system that combines HP 4156A and a probe station was conducted to obtain the current-voltage (I-V) characteristics and constant voltage stress time dependent dielectric breakdown (TDDB) of the resulting BST capacitors.

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5-3 Properties and Analysis of ELA BST Films

5-3.1 Optical absorptions and thermal conduction analysis of ELA-BST films

Figure 5-1 shows reflectivity, *R*, and the extinction coefficient, k, of amorphous thin $Ba_{0.5}Sr_{0.5}TiO_3$ (α-BST) film for light of wavelength from 198 nm to 900 nm. The reflectivity of 248-nm laser light for amorphous BST film is 0.26. Thus, the incident energy transmitting into BST is as much as 74%. The law of absorption for the light intensity *I(x)* of a parallel beam propagating in x-direction is described as follows:

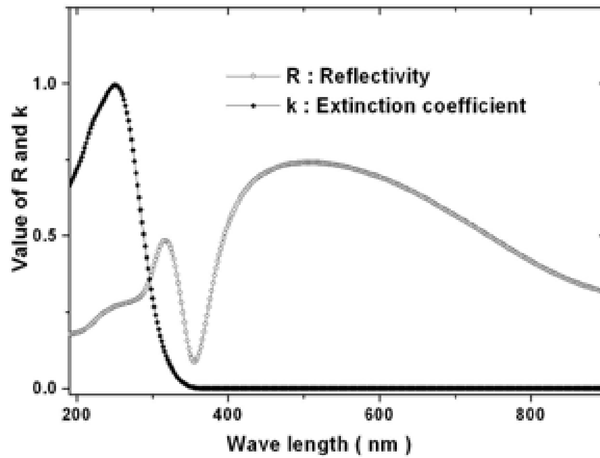


Figure 5-1 The reflectivity, R, and the extinction coefficient, k, of amorphous thin $Ba_{0.5}Sr_{0.5}TiO_3$ film for light of wavelength from 198 nm to 900 nm.

$$I(x) = I(x=0)e^{-\alpha(\omega)x} \quad (5\text{-}1)$$

where $\alpha(\omega)$ is the absorption coefficient and ω is the angular frequency.

$$\alpha(\omega)= 2\,\omega k(\omega)/c = 4\pi k_e(\omega)/\lambda \quad (5\text{-}2)$$

where $k_e(\omega)$ is the extinction coefficient. The distance d for the intensity of propagating light decay to $1/e$ (1/2.713) is:

$\alpha d=1$,

$d = 1/\alpha = \lambda / (4\pi \times k_e(\omega))$

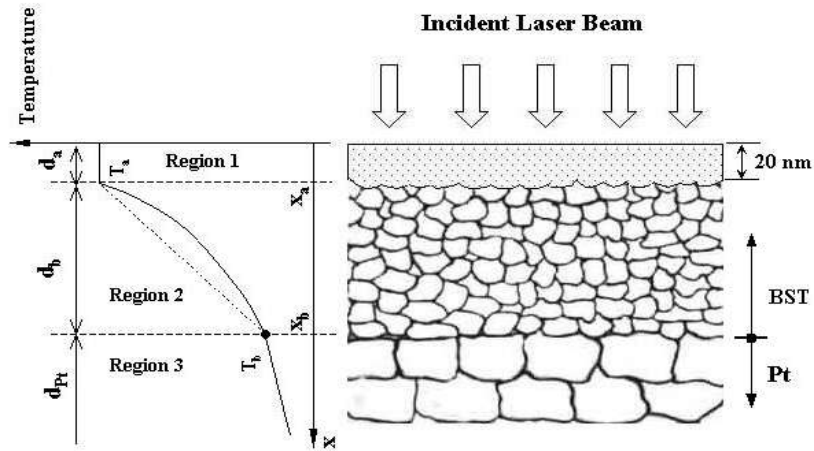
The $k_e(\omega)$ of BST for 248-nm light is as high as 0.993. Then,

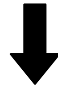
d = 248 nm/(4π×0.993) = 19.87 nm

Most of the propagating energy of the laser beam is absorbed to heat on the top 19.87 nm of BST film. The absorbed heat transfers from the BST surface to the interior region of the BST film and the underlayer films. The temperature distribution will be discussed later.

Figure 5-2 describes the process schemes of the ELA treatment for the BST film. Initially, the as deposited α-BST film has inhomogeneous grains and poorer crystallinity,

(a) During ELA Process





(b) After ELA Treatment

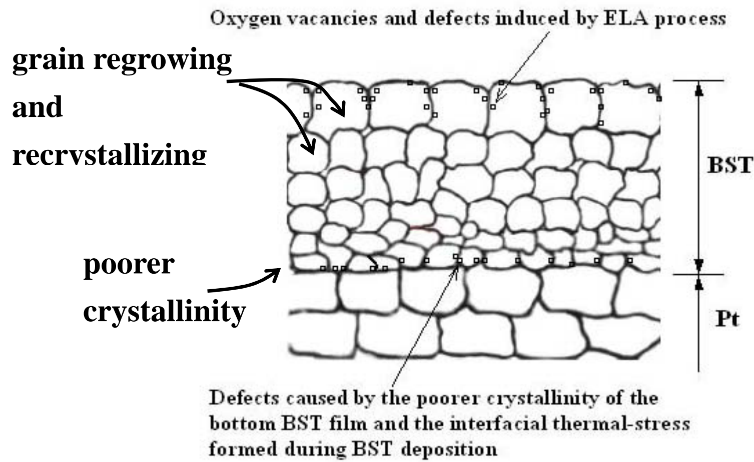


Figure 5-2 The process schemes of ELA treatment applied on the BST/metal-bottom-electrode multilayer: (a) during ELA process and (b) after ELA treatment.

which were investigated by TEM analysis in previous work [130]. Next, the excimer laser with a wavelength of 248-nm was applied on the BST film, and, as discussed above, the laser beam is absorbed at the surface region of 20-nm depth. The thermal analysis is carried out to realize the temperature distribution of the

BST/metal-bottom-electrode/Si-substrate multifilm during ELA process, as shown in Fig. 5-2 (a). In this analysis, this multifilm capacitor can be divided into three thermal regions: Region 1 is the photo absorption region; Region 2 is the heat conduction and absorption area of the ceramic BST film; and Region 3 is the metal films with very high heat conductance and lower thermal capacitance. In addition, the Si substrate, with high thermal capacitance and conductance, is reasonably considered as a semi-infinite heat sink in this case [131]. In the Region 1, as discussed above, the incident photons of the laser energy fluence (LEF) directly interact with the BST film at the surface region of 20-nm depth, so the governing equation of heat conduction in Region 1 can be considered as [132]

$$\frac{(1-R)\partial I(x)}{\partial x} = \frac{\partial^2 T(x,t)}{\partial x \partial t} - \sigma \frac{\partial^2 T(x,t)}{\partial x^2} \qquad (5\text{-}3)$$

where T(x,t) is the temperature distribution as a function of time and position; x-axis is perpendicular to the top surface of BST film; σ (=$\kappa/\rho C_p$) is the thermal diffusivity of BST which is 0.015 ($sec^{-1}cm^{-2}$); κ, ρ and C_p are heat conductance, mass density and thermal capacitivity of BST. In Region 1, the response time τ_a (= d_a^2/σ) of the temperature rising is about 0.3 nsec. Since the response time in Region 1 is much smaller than that of laser pulse width (25 nsec), the temperature distribution can be considered as a saturated stable value $T_{a(sat)}$. Next, the heat conduction equation of region 2 can be written as

$$\frac{\partial^2 T(x,t)}{\partial x^2} = \sigma \frac{\partial T}{\partial t} \qquad (5\text{-}4)$$

the boundary conditions are

$T(x_a,t)=T_{a\,(sat)}$

and

$$-\kappa_{BST}\frac{\partial T(x_b,t)}{\partial x}=-\kappa_{Pt}\frac{T(x_b,t)-T_{sub}}{d_{Pt}}$$

where $T_{a\ (sat)}$ is the saturation temperature at x_a, T_{sub} is the temperature between metal and Si substrate, κ_{BST} and κ_{Pt} are the heat conductance of BST and Pt. Besides, in Region 3, because the metal film has very high heat conductance and low thermal capacitance, the heat conduction is treated as a linear temperature-position relation:

$$J_{Pt} = (-\kappa_{Pt}\frac{T(x_b,t)-T_{sub}}{d_{Pt}}) \qquad (5\text{-}5)$$

where J_{Pt} is the heat conduction flow of Pt electrode. Consequently, the simplified approximate solutions of the $T(x,t)$ are deduced by Eqs. (3)~(5), and all the material parameters are substituted into these solutions to estimate the temperature distributions of the ELA-BST capacitor [131, 133]. The results of heat conduction analysis in different regions are deduced as [141]:

Region 1:

$$T(x,t) \quad \frac{2I(0)\sqrt{\sigma t}}{k_{BST}}\times\sum_{-\infty}^{\infty} ierfc\left[\frac{2nd_a - x}{2\sqrt{\sigma t}}\right](1-R) \qquad (5\text{-}6)$$

Region 2:

$$T(x,t) \quad (T_b+(1-(x-d_a)/d_b)(T_a-T_b)+\sum_{n=1}^{\infty}(T_a-T_b)Exp(-t/\tau_b)\bullet Sin(n\pi x/d_b) \qquad (5\text{-}7)$$

where T_b $(T_b^o-T_{sub})\times(1-Exp(-t/\tau_b))+T_{sub}$, d_a = 20 nm and the response time τ_b of region 2 is about 5 nsec.

Region 3:

$$T(x,t)= -(T_b-T_{sub})/d_{Pt}\,(x-x_b)+T_b, \qquad (5\text{-}8)$$

According to equations (6), (7) and (8), the saturation temperatures of heat transfer at x_a and x_b can be evaluated as follows:

$T_{a(saturation)}$ 700 °C for the laser energy fluence (LEF) of 60 mJ/(pulse×cm^2),

$T_{a(saturation)}$ 760 °C for LEF of 70 mJ/(pulse×cm^2),

$T_{b(saturation)}$ 410 °C for the LEF of 60 mJ/(pulse×cm^2),

$T_{b(saturation)}$ 420 °C for the LEF of 70 mJ/(pulse×cm^2),

where the density and thickness of BST film are 6 g/cm^3 and 100 nm. The heat transfer analysis, evaluated by finite differential method (FDM), depicts that the temperature of BST film exceeds 700°C at the top surface region, but it greatly decreases to 410°C at the interface of BST/Pt-bottom-electrode. Hence, the ELA, with a very shallow absorption depth of the BST thin film at wavelength of 248-nm, can carry out a local annealing from BST surface to interior region, and, furthermore, it would not damage the underlayer structures and devices. Fig. 5-2(b) shows the grains of the BST film

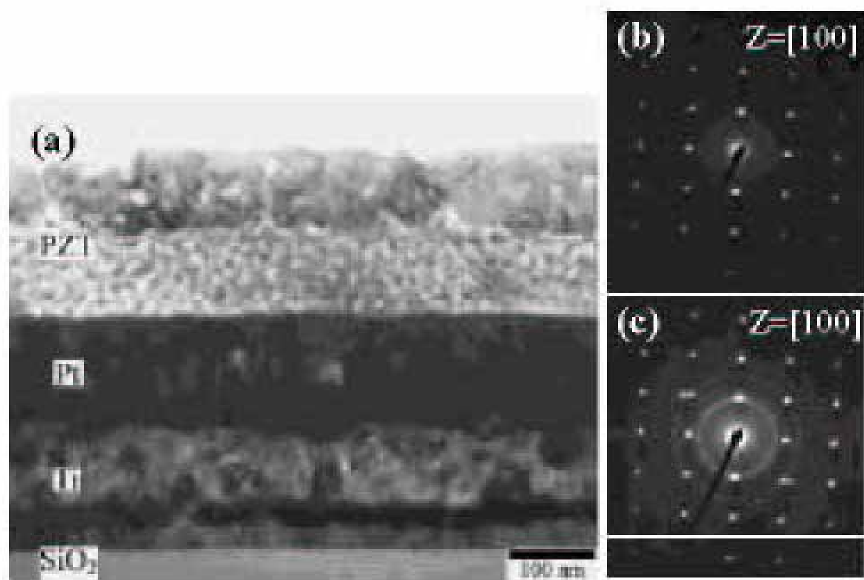


Figure 5-3 Cross-sectional TEM micrographs (a) bright-field images for the KrF-excimer-laser annealed PZT films, and (b) SADP of upper layer region and (c) lower layer region of PZT thin film [134].

gradually regrow up and recrystallize along the x-axis after ELA process, and thus the grains at top surface are larger than those at bottom interface. The cross-sectional TEM analysis reveals the grain sizes of the ELA-treated ferroelectric film gradually varied along the x-axis, which is consistent with Fig. 5-2(b), as reported in previous work and Fig. 5-3 [134]. On the other hand, it should be noticed that the region near the top surface of BST film exhibits a very high temperature (>700°C) during ELA process, so many oxygen vacancies and defects will be induced at the top surface, degrading the BST films._In addition, the thickness and density of the BST films significantly affect the thermal distribution in this work. The thermal property of an ultra thin BST film, smaller than laser absorption depth 20 nm, is greatly influenced by the underlayer metal, which results in increasing the photo reflectivity and the heat conductivity to reduce the ELA effect. In addition, there are many drawbacks in this ultra thin film, such as very high leakage current and high interface stress. The temperature between x_a and x_b raises as BST film thickness increases while the thickness is much larger than 20 nm, as deduced in Eq. (7) and (8). This phenomenon can be inferred that the heat transfer is enhanced due to increasing thermal gradient for reduced BST thickness and the very high thermal conductance metal-substrate. On the other hands, the heat response time τ rises as BST film thickness (d_a + d_b) and density ρ_{BST} increases. This response time reaches as high as 9 nsec (pulse width/2.72) while film thickness is 140 nm. Hence, if the BST film, ELA treated for 60 mJ/(pulse×cm^2), exceeds 140 nm, the thermal distribution in BST/metal films will be modified as follow:

$$J_{laser} \times \tau l = d_a \times C_{p(BST)} \times \rho_{BST} \times (T_a - 300) + \int_{xa}^{xb} (T(x,\tau) - 300) C_{p(BST)} \rho_{BST} dx + \int_{xa}^{x_{Si}} (T(x,\tau) - 300) C_{p(Pt)} \rho_{Pt} dx + \int_{0}^{\tau l} (-k) \frac{\partial T(X_b, t)}{\partial x} dt \qquad (5\text{-}9)$$

where τl, 25 nsec in this work, is laser pulse width. The temperature during ELA treatment decreases as BST film thickness increases under constant incident laser energy. Eq. (9) reveals that this temperature will be dropped by thermal absorption of the excessive thickness film. ELA temperature in BST film can be promoted by increasing LEF and pulse width. However, such experimental conditions were not performed due to the limitation of the equipments in this work.

5-3.2 Material and electrical characterizations of ELA BST films

Figure 5-4 shows the XRD patterns of the thin BST films post treated at various energy fluence. Fig. 5-4 (a) and (b) show the as-deposited and the 300°C post annealed (PA 300°C) in oxygen ambient BST films, respectively. No obvious crystalline peak of BST film appeared in the XRD spectrum of BST deposited at 150°C substrate temperature, which indicates that the structure of as-deposited BST films is primarily amorphous. Even though the 300°C post furnace annealing applied, the BST film remains predominantly amorphous. Fig. 5-4 (c), (d) and (e) indicate the BST films treated by ELA at 300°C substrates with LEF of 46.7, 57.8 and 66.7 mJ/(cm$^{2}\times$pulse), respectively. The ELA-treatment greatly enhances the crystallinity of BST films. Figure 5-4(b) indicates that 300°C PA alone cannot improve the crystallinity of BST films, and thus the crystallinity enhancements observed in Fig. 5-4(c), (d) and (e) are due to the ELA treatment. On the other hand, an excessive fluence of laser energy will degrade the BST films, because the defects and oxygen vacancies are formed by the elevated temperature at the top surface region, leading to a poorer crystallinity of BST film [130, 135]. In this study, the strongest peak of BST crystallinity is obtained for ELA 57.8

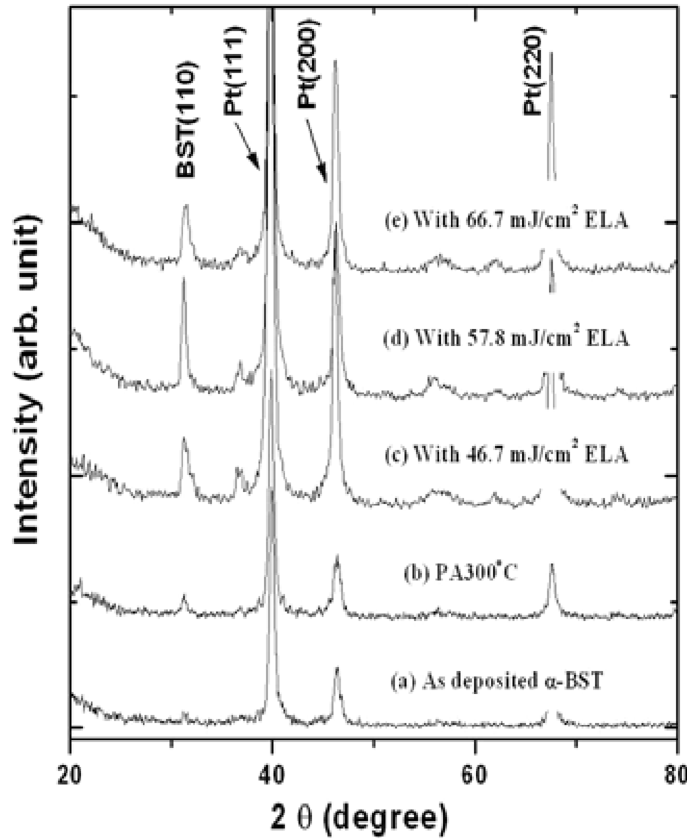


Figure 5-4 The XRD patterns of thin BST films (a) as-deposited, (b) with 300°C PA, (c) with 46.7 mJ/(cm^2×pulse) ELA, (d) with 57.8 mJ/(cm^2×pulse) ELA, and (e) with 66.7 mJ/(cm^2×pulse) ELA.

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mJ/(cm^2×pulse) treated samples, as shown in Fig. 5-4 (d). In general, the optical characteristics are strongly influenced by the textures of preferred orientations [136]. The variation in the texture of BST films treated under various conditions is deduced from the XRD patterns, as shown in Fig. 5-5. The percentage of a preferred-oriented texture in a film is calculated from the diffraction pattern of the film according to the following formulas [137]:

$$X_{hkl} = I^o_{hkl}/(I^o_{m00}+ I^o_{110}+ I^o_{111}+....) \qquad (5\text{-}10)$$

$$I^o_{hkl} = (I^o_{hkl})_{films}/(I^o_{hkl})_{ceramics} \qquad (5\text{-}11)$$

$$I^o_{m00b}= (I^o_{100}+ I^o_{200}+.... +I^o_{111})/n \qquad (5\text{-}12)$$

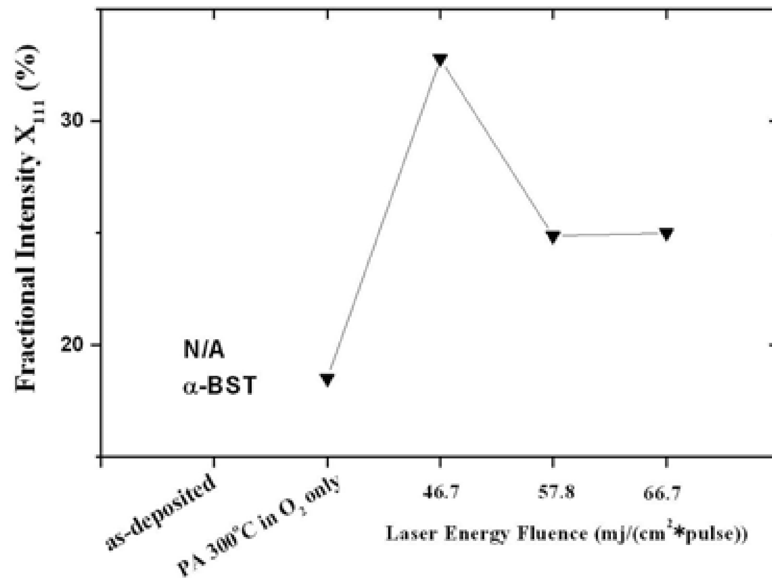


Figure 5-5 The fractional intensity of the (111) texture for the BST film post treated at various condition.

where X_{hkl} and I^{o}_{hkl} represent the fractional intensity of (hkl) orientation and the peak intensity in (hkl) orientation. X_{111} greatly increases for the sample treated by ELA, and reaches a maximum at 46.7 mj/(cm^2*pulse). Hence, the BST films treated by ELA reveal stronger (111) texture than those not so treated, as confirmed by TEM diffraction patterns. The ring patterns of the TEM diffraction show the polycrystalline nature of BST formed by post treatments, as shown in Fig. 5-6. Figure 5-6(a) indicates a strong (110) texture for a film treated only by PA 300°C. Furthermore, the broad width and weak intensity of the (110) ring reveal that the PA 300°C BST has poorer crystallinity, and the irregular reflection spots imply the presence of larger but inhomogeneous grains in this film [138]. On the other hand, an intensive (111) ring pattern shows that the (111) texture is greatly enhanced after post ELA treatment, consistent with the results of XRD

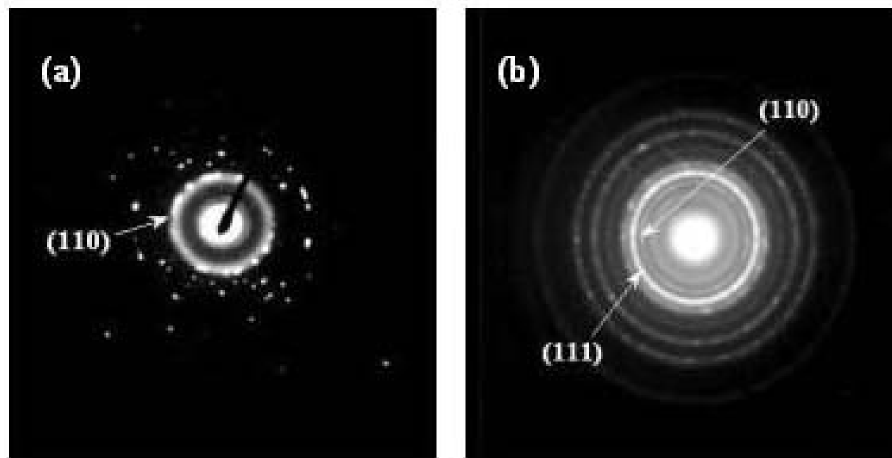
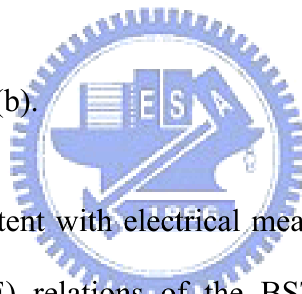


Figure 5-6 TEM diffraction patterns of (a) PA 300°C in O_2 ambient only, (b) 46.7 mJ/(cm^2*pulse) ELA treated BST films

analysis, as denoted in Fig. 5-6(b).



The crystallinity is consistent with electrical measurements. Figure 5-7 shows the polarization-electric field (P-E) relations of the BST films. ELA treatment greatly enhances polarization, and 57.8 mJ/(cm^2*pulse) ELA yield the maximum polarization. The rounded shape of the P-E shows that the BST film post treated at ELA 66.7 mJ/(cm^2*pulse) is very leaky under negative bias. Figure 5-8(a) demonstrates the dielectric

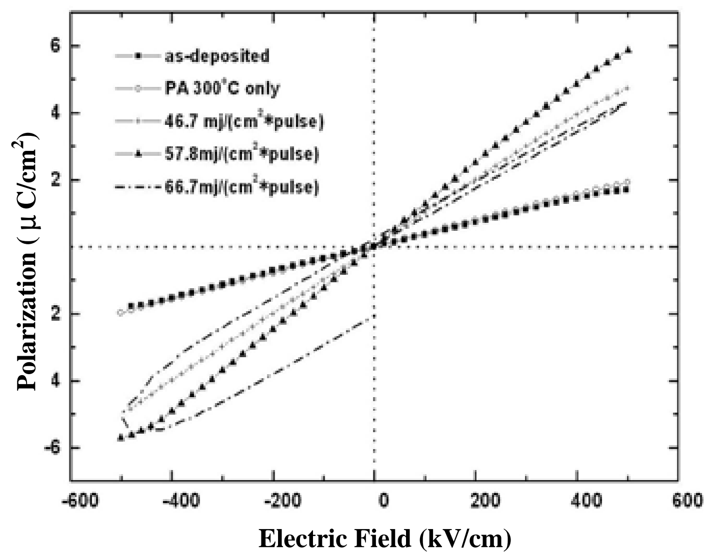
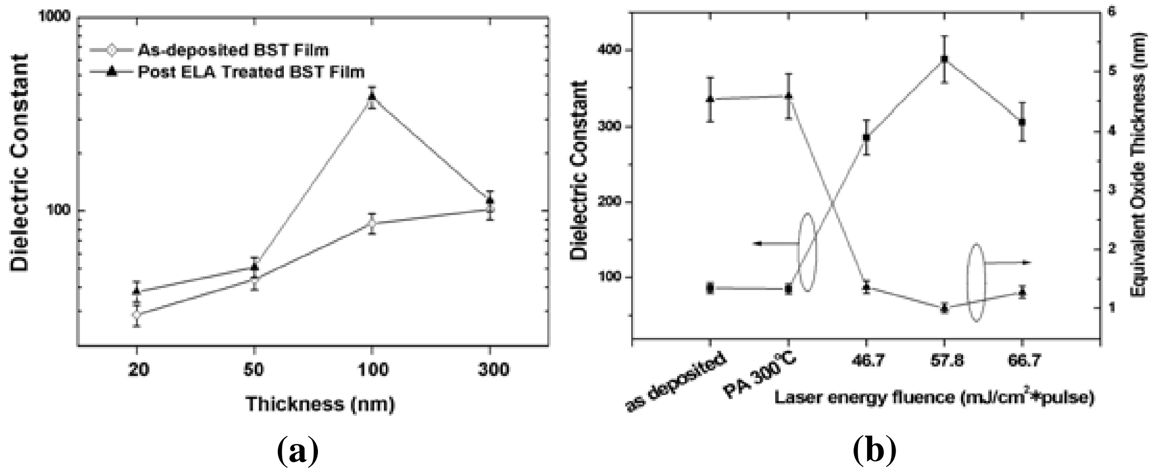


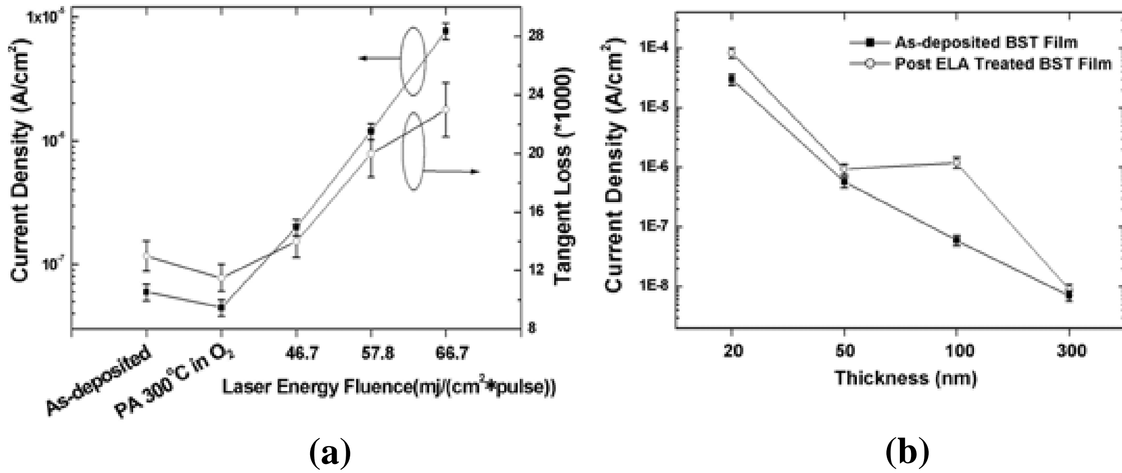
Figure 5-7 Polarization versus electric field of BST film treated at various ELA conditions.



(a) **(b)**

Figure 5-8 (a) The dielectric constants and equivalent SiO_2 thickness of the BST films versus LEF, and (b) the dielectric constant versus the thickness of the as-deposited/the 57.8 mJ and the ($cm^2\times$pulse)-ELA-treated BST film.

constants and equivalent SiO_2 thickness ($d_{ox} = d_{BST} \times \varepsilon_{ox} / \varepsilon_{BST}$) of the Pt/BST/Pt/TiN/Ti/Si samples wihout/with various energy ELA treatments. For the as-deposited BST films and the samples with PA 300°C, the dielectric constants are only 88 and 89, respectively. There is no apparent enhancement for the samples with PA 300°C only. However, a considerable raise of the dielectric constant appears in ELA treated samples, especially the 57.8 mJ/($cm^2\times$pulse) ELA one. The 57.8 mJ/($cm^2\times$pulse) ELA samples have a dielectric constant of 388, in contrast to the dielectric constant of 88 and 89 for the as-deposited and PA 300°C samples. The dielectric constant increases as LEF rises due to the crystallinity enhancement, but an excessive LEF, as shown in the case 66.7 mJ/($cm^2\times$pulse), will damage the film surface to degrade dielectric constant. An equivalent SiO_2 thickness of 1.01 nm was achieved for the 57.8 mJ/($cm^2\times$pulse) ELA one. The trend of dielectric constant is consistent with that of the crystallinity enhancement of the BST films, as shown in Fig.5-4 and 5-8 (a). Fig. 5-8 (b) indicates

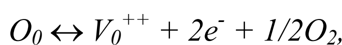


(a) **(b)**

Figure 5-9 (a) Leakage current density and tangent loss of the Pt/BST/Pt capacitors post treated at various ELA conditions, and (b) the leakage current density versus the thickness of as-deposited and the 57.8 mJ/(cm^2 X pulse)-ELA-treated BST film.

the dielectric constants of ELA treated (57.8 mJ/(cm^2×pulse)) and as-deposited BST films versus various film thicknesses. The 100nm BST film is dramatically enhanced after ELA treatment, but the 20, 50 and 300 nm films do not show obvious enhancement. As discussed above, a decreasing thickness results in laser_energy dissipation due to increasing heat conduction, but an excessive thickness increases heat capacity to reduce ELA temperature. Hence, a proper thickness of the ELA BST film, treated at constant LEF, can achieve an optimum dielectric property.

The leakage current and tangent loss characteristics of the Pt/BST/Pt/TiN/Ti/Si samples without/with various energy ELA treatments are shown in Fig.5-9 (a). In general, the oxygen escapes during thermal process, and the oxygen vacancies are subsequently generated according to



$O_0 \leftrightarrow V_0^{++} + 2e^- + 1/2O_2,$

where O_0, V_0^{++} and e^- denote the oxygen ion at its normal site, oxygen vacancy and electron, respectively. However, a higher concentration of oxygen vacancies leads to n-type conductivity of the BST materials due to the electrons generated, causing larger leakage currents [139]. The leakage current of the BST film with PA 300°C only in O_2 ambient is suppressed owing to oxygen vacancies compensated, but that of the film with ELA treatment increases as LEF rises due to the oxygen vacancies generated during ELA process. Although the leakage current of BST film increases after ELA treatment, it remains as low as 1 $\mu A/cm^2$ for ELA 57.8 $mJ/(cm^2 \times pulse)$ at 100 kV/cm. Besides, the tangent loss proceeds by two mechanisms- resistive loss and relaxation loss [140]. In resistive loss case, energy is dissipated by mobile charges, and the tangent loss depends on the magnitude of the leakage current; in relaxation loss, energy is dissipated by relaxation of dipoles, and the tangent loss is proportional to the dielectric constant. Comparing the dielectric and leakage characteristics shown in Figs. 5-8 and 5-9, one finds that the trend of the tangent loss is similar to that of the leakage current. Hence, the resistive loss dominates the tangent loss. Besides, the leakage current of the as deposited BST film increases as thickness decreases at a constant field 100 kV/cm, as indicated in Fig. 5-9 (b). The leakage current of 100 nm BST film remarkably rises after ELA treatment, and, as discussed above, the proper thickness results in high ELA temperature, but this high temperature also damages the film surface to enhance leakage current.

Lifetime extrapolation using constant voltage stress time dependent dielectric breakdown (TDDB) can predict a lifetime of ten years. Figure 5-10 shows the TDDB reliability of BST films treated at various conditions. The TDDB characteristic of ELA

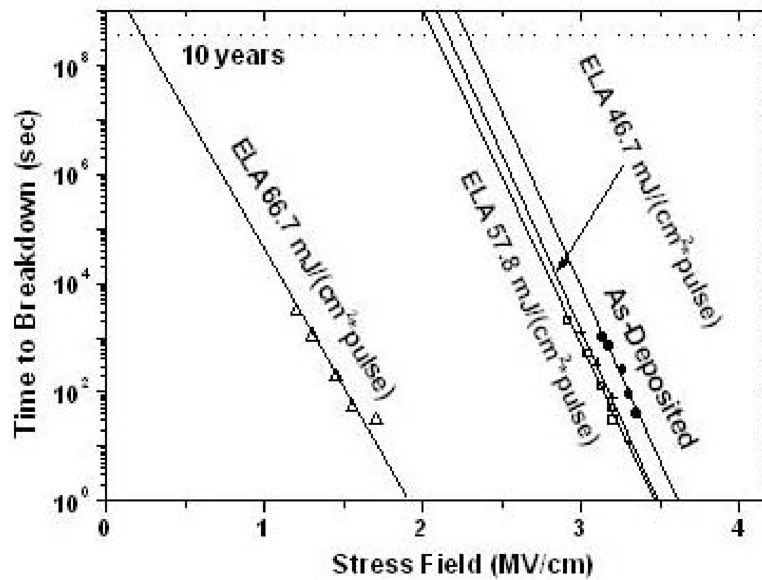


Figure 5-10 The TDDB reliability of BST films treated at various conditions.

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treated sample demonstrates a shorter lifetime than as-deposited sample. The leakage current of ELA treated sample is higher than that of as-deposited sample, and the lifetime decreases as ELA energy fluence increases. Thus, the increased leakage current accelerates the electrical degradation of the capacitors. However, samples with lifetime greater than 10 years at the stress field 2 MV/cm are obtained after ELA 57.8 mj/cm^2×pulse. The BST films with a high dielectric constant (388) and low leakage current (1 μA/cm^2) can be prepared under a low thermal budget process (ELA 57.8 mJ/(cm^2×pulse)).

5-3.3 Leakage current mechanisms

Furthermore, the leakage current of BST capacitors biased at positive/negative

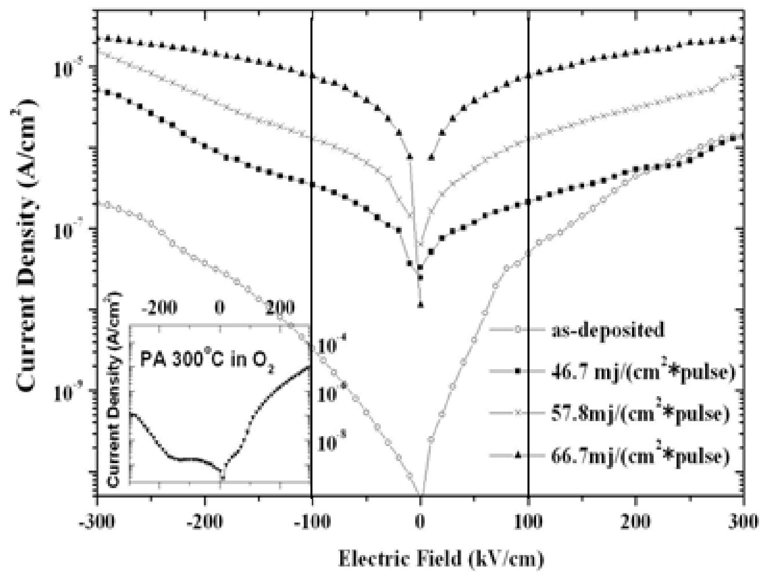


Figure 5-11 The leakage current densities of the Pt/BST/Pt/TiN/Ti capacitors biased at positive/negative voltage with various treatments.

voltage shows asymmetric before ELA and symmetric after ELA, as shown in Fig. 5-11. The leakage current of the as-deposited α-BST film biased at positive voltage is higher than that biased at negative voltage, and the inset shows the leakage current is more asymmetric after PA 300°C in oxygen ambient. In contrast, the current density of the BST film biased at positive/negative voltage shows the symmetric plot after ELA treatment. Further investigating on the degradation of the ELA-BST films, a residual gas analyzer (RGA) in-situ detected the species generated from the BST surface during ELA, as indicated in Fig. 5-12. In this study, the heating substrate (300°C) desorbed the adatoms of the BST surface and thus prevented experimental disturbance during RGA detection. The oxygen partial pressure during the ELA pulse to BST films is much higher than the background-oxygen-pressure before the ELA pulse applied. Consequently, oxygen atoms escape from BST films during ELA treatment, inducing many oxygen vacancies at the upper surface region. The leakage current increases as

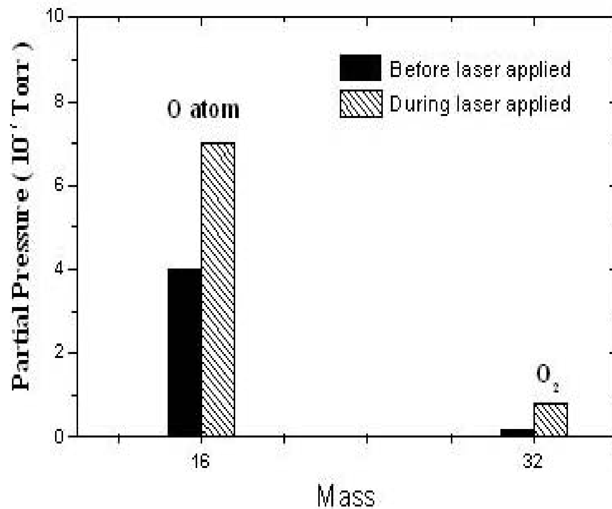


Figure 5-12 Oxygen species in-situ detected by RGA during ELA process.

laser energy fluence rises due to the injected electron current formed by the ELA-induced interface states. The degradation of the upper surface after ELA is obviously associated with the trend of the leakage current.

The electron energy band explains the mechanism of the leakage current, as shown in Fig. 5-13. Fig. 5-13(a) infers that many defects at the interface of BST/bottom-electrode are caused by the poorer crystallinity of the bottom BST film and the interfacial thermal-stress formed during BST deposition, so the injected electron current is formed under positive voltage. The inset of Fig. 5-11 depicts that the negative-biased leakage current of BST post-annealed in O_2 ambient is further suppressed due to the oxygen vacancies compensation and the formation of Schottky barrier at the top surface, as denoted in Fig. 5-8(b). Besides, as mentioned in Fig 5-2(a), a very high temperature (>700°C) exists at a very shallow depth (20-nm) of the photo absorption region during ELA. The oxygen atoms escape from the BST film due to this abnormally high temperature during ELA, and this phenomena was in-situ observed by residual gas analyzer (RGA), as shown in Fig. 5-12. Thus, many oxygen vacancies and defects at the BST top surface are induced by ELA treatment. Fig. 5-13(c) indicates an injected electron current of the ELA-BST film is formed by the ELA-induced interface-states at

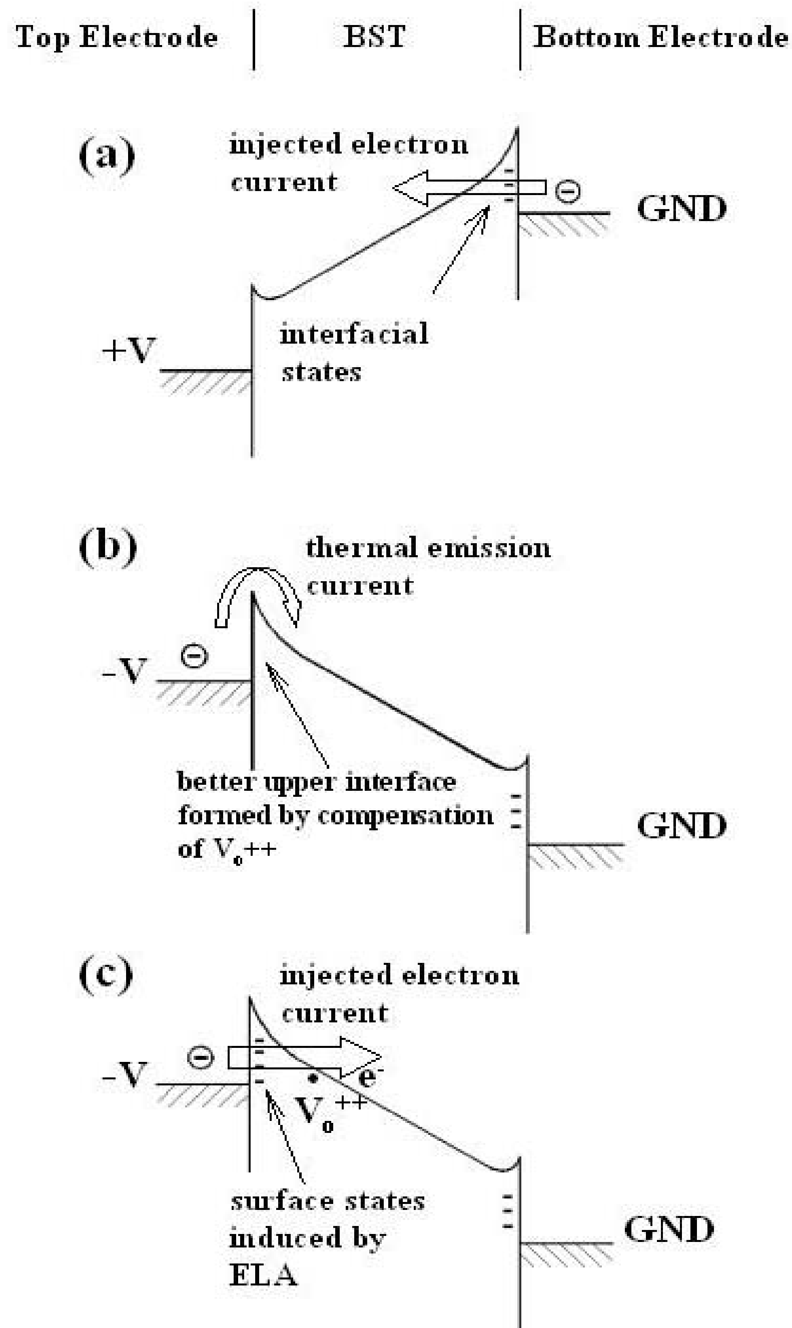


Figure 5-13 The electron energy band of (a) as-deposited BST film biased at positive voltage, (b) BST film post annealed in O_2 and biased at negative voltage, and (c) ELA-BST film biased at negative voltage.

upper surface under negative bias, and, this is, the negative-biased leakage current rapidly increases after ELA treatment. Hence, the leakage current profiles of the ELA-BST films biased at positive/negative voltage become symmetrical.

5-4 Summary

The ELA technique greatly enhances the crystallinity and dielectric constant of the BST films under low substrate temperature 300°C. The dielectric constant of the as-deposited BST films is remarkably improved from 80 to over 250 after ELA. In this study, the trend of the dielectric property versus laser energy fluence is similar to that of the crystallinity versus laser energy fluence, and a maximum dielectric constant (ε_r=388) is obtained at 57.8 mJ/(cm^2×pulse) ELA.

The energy propagation of the 248 nm light in BST film decays to only 1/e (1/2.713) during 20-nm depth. According to the heat transfer analysis, this very shallow absorption depth of 20-nm results in a very high temperature (>700°C) at the upper surface region of the BST film, and the temperature rapidly drops to 410°C at the bottom electrode. Hence, this local annealing carries out the recrystallization and grain regrowth from upper surface to interior region, and, particularly, it would not affect the underlayer structures at all. The temperature of the BST film during ELA treatment raises as thickness increases while the BST film is larger than 20 nm, but the excessive thickness will result in decreasing ELA temperature due to the thermal capacity and the thermal response time increased.

On the other hand, increasing laser energy fluence can enhance the crystallinity of

BST film, but excessive energy fluence creates too many oxygen vacancies and surface defects, degrading the BST films. This degradation was directly observed by RGA analysis, which indicated that the oxygen atoms escaped from the BST film during ELA process. The negative-biased leakage current indicates that there are many interface states induced by the post ELA treatment.

In summary, the 248-nm ELA technique applied on the BST film is very promising for the integration process of ICs, but the LEF and film thickness must be precisely controlled to reach the optimum electric properties.

Chapter 6

Leakage Current Improved by Post Treatment using Oxygen Plasma Technique

6-1 Brief Concept of Oxygen Plasma Treatment

One of the most crucial issues concerning electrical parameters is the leakage current of DRAM cells. The Schottky emission (SE) (electrode-limited) conduction mechanism dominates the leakage current measured at 1V for the above-mentioned BST thin films [142 – 144]. The SE leakage current can be affected by the metal work function of the electrodes, oxygen vacancy accumulation at the electrode interface, and surface morphology of the BST thin films [145 – 148]. Previous literature ascribed the mechanism of leakage current to the variation of the oxygen vacancies in the BST thin films [142 – 144, 149 – 152]. Recent studies indicated that the higher leakage current of BST films could be effectively reduced by activated oxygen annealing [149 – 152]. Unfortunately, these post-annealing processes require high processing temperatures (> 500°C) and long process duration (~ 1 h), so those processes will be harmful to the COMS structure. However, a low temperature technology, used for the compensation of oxygen vacancies, is necessary for the device integration.

In this study, oxygen plasma treatment was performed on the as-deposited BST films

at a low substrate temperature (250°C) to passivate the oxygen vacancies. Post oxygen plasma treatment can provide active oxygen atoms to decrease the oxygen vacancies and enhance the quality of BST films. Plasma treatments with different time intervals are also used to examine how they affect the leakage characteristics of BST thin films. In addition, the mechanism of improvement in the leakage characteristics of BST films is systematically investigated.

6-2 Experiments

$Ba_{0.5}Sr_{0.5}TiO_3$ films (100nm) were then deposited onto Pt/TiN/Ti/Si substrate using a RF magnetron co-sputtering system at a low temperature of 300 ^{o}C. The sputtering chamber was evacuated to a base pressure of $7x10^{-7}$ Torr. Next, all films were deposited at a constant pressure of 6.8 mTorr which was maintained by a mixture of argon and oxygen at 76 sccm and 4 sccm, respectively. To control the Ba/Sr ratio of BST thin films by tuning the RF power, $BaTiO_3$ and $SrTiO_3$ targets were used simultaneously. To achieve paraelectric characteristics, the Ba/Sr ratio of 1:1 was selected. The RF powers for the deposition of $BaTiO_3$ and $SrTiO_3$ were 175 and 230 W (power densities were 2.159 and 2.837 W/cm^2), respectively.

The oxygen plasma post-treatment was applied on the BST films to suppress the leakage current. The oxygen plasma post-treatment was performed in planar plasma in a 30 cm–diameter chamber for 3, 5, 10, and 15 min, to passivate the oxygen vacancies of the BST films. The planar plasma system was a parallel-plate, 2-electrode RF plasma. The upper electrode was powered and the sample sat on the lower grounded plate. These

two plates were 25 cm large in diameter. The samples were only 2.5 x 2.5 cm^2, and the electrode plate was much larger than the samples. The distance between the substrate and the target was 17 cm. The operating conditions for the oxygen-plasma treatment were as follows: flow rate of 900 sccm, gas pressure of 650 mTorr, substrate temperature of 250 ^oC, and RF power of 300 W.

Pt top electrodes, with a diameter of 150μm, were patterned on the BST films using shadow mask process. The physical properties of BST films were analyzed before Pt top electrode deposition. The composition of the resultant $(Ba,Sr)TiO_3$ films were analyzed by Rutherford backscattering spectroscopy (RBS). The crystallinity was then characterized by X-ray diffraction (XRD, Siemens D5000 diffractometer). Based on XRD data, the average grain size could be determined by Scherrer's formula [153]. The surface roughness was inspected using an atomic force microscope (AFM, Digital Instruments Nano-Scope III). The surface morphology, cross-sectional view, and film thickness of the BST films were examined by scanning electron microscopy (SEM). Next, the capacitance-voltage (C-V) characteristic was measured on the metal-insulator-metal (MIM) structure by measuring the capacitance at a frequency of 100 kHz. Dielectric constants of the films were calculated from the capacitance measured at 100kHz without a bias voltage. Analysis of depth profiles measured by AES confirmed the oxygen content comparison. The dielectric properties were analyzed with a HP 4194A impedance-gain phase analyzer. The current-voltage (I-V) characteristics were examined by an automatic measurement system of HP 4156A combined with a probe station.

6-3. Properties of BST Films Post Treated by Oxygen Plasma

6-3.1 Leakage current suppressed by oxygen plasma treatment

Figure 6-1 gives the leakage current-voltage relationship of the as-deposited BST films. The leakage current under a reverse bias is markedly higher than that under a positive one. In general, Schottky emission (SE) and Poole-Frenke (PF) conduction can be considered to interpret the leakage current of BST films. Many reports indicated the asymmetrical leakage current profiles of the BST capacitors biased at positive/negative voltage are caused by SE contact at Pt/BST interface of single side [154]. Chapter 4 also shows the similar results. The barrier height of SE (interface limited) is dependent on the work function of the electrode metal, electron affinity of the dielectric, and the surface states. The PF transport mechanism (bulk limited) is a result of the lowering of the barrier height of traps in the dielectrics. Hence, the PF transport mechanism does not exhibit polarity dependence [142 – 144, 150, 152]. Figure 6-1 shows the asymmetrical current-voltage profile of the capacitor biased at positive/negative voltage. Since both of the top and bottom electrodes are made from Pt materials, this asymmetrical current-voltage profile shows the Schottky barrier is formed at the interface of the BST/bottom-electrode. In addition, the interface states in the upper electrode

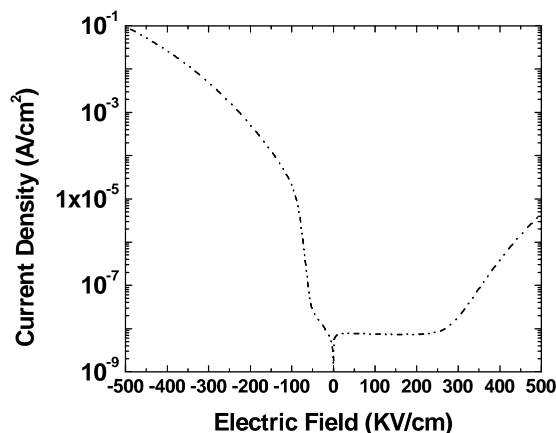
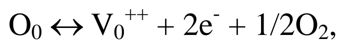


Figure 6-1 The typical curve of the leakage current versus the electric field for the as-deposited BST films.

result in high leakage current at a negative bias [149, 151, 155]. The interface defects are caused by high concentration of oxygen vacancies at top surface, which will be discussed later. Obviously, the BST film must be fabricated at a substrate surface temperature of 300°C above (410°C at wafer backside), and exposed to a plasma environment with high concentration Ar^+ during sputter process. Hence, the oxygen atoms escape from top surface, and then oxygen vacancies are subsequently generated according to the following equation:



$$O_0 \leftrightarrow V_0^{++} + 2e^- + 1/2O_2,$$

where O_0, V_0^{++} and e^- denote the oxygen ion at its normal site, an oxygen vacancy and an electron, respectively. A high concentration of oxygen vacancies led to n-type conductivity of the BST materials due to the electrons generated, causing large leakage currents. The oxygen vacancies can be greatly improved by an oxygen plasma treatment, which gives rise to active oxygen atoms, decreasing the oxygen vacancies. Figure 6-2 shows the leakage current, measured at various negative electric fields, is a function of the duration time of O_2 plasma treatment. The leakage current is significantly reduced for the samples post O_2 plasma treated with 3, 5 and 10 min, and,

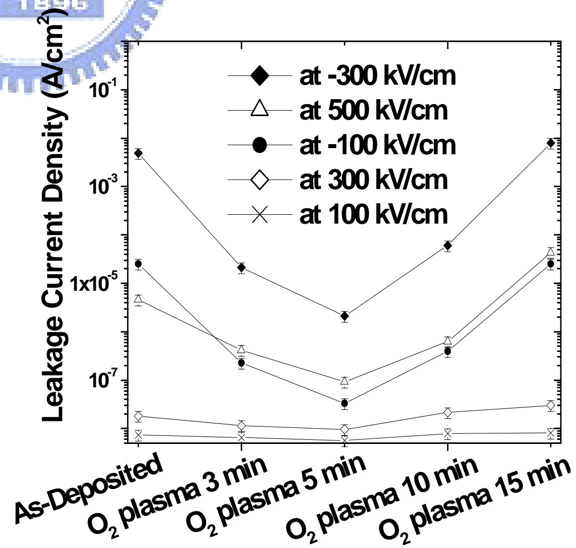
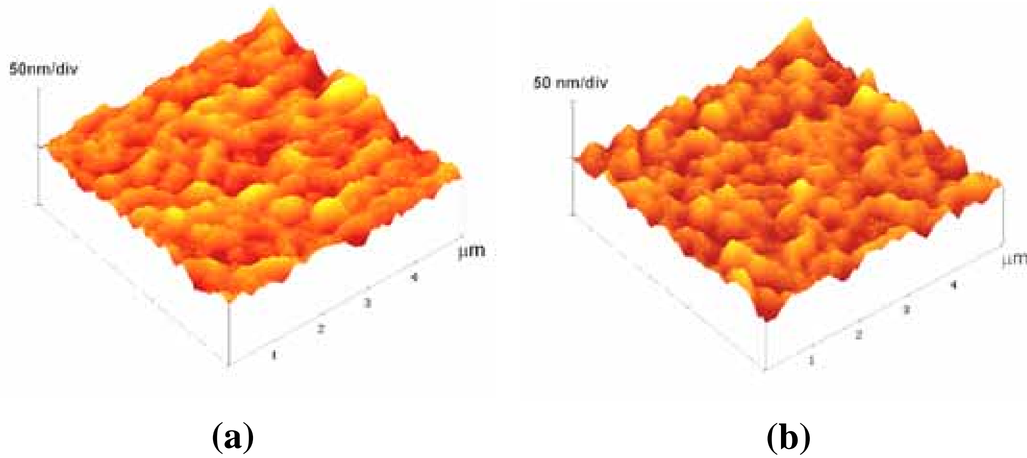


Figure 6-2 Dependence of the the leakage current measured at various electric fields with a delay time of 30 s on duration of O_2 plasma treatment after BST film deposition.

particularly, the 5 min treatment can reach a minimum value of leakage current. Besides, if the plasma treatment time is longer than 10 min, the leakage current will gradually increase. The substrate in oxygen plasma equipment is DC-biased. A DC-biased substrate will induce serious plasma bombardment damage. The oxygen plasma can effectively passivate the oxygen vacancies on the top surface of the BST film, but the treatment duration must be carefully controlled. If the oxygen plasma treatment with long duration is applied, the plasma bombardment damage will induce even more defects in the BST films.

6-3.2 Material and electrical characterizations of BST films post treated by oxygen plasma

The improvement of the leakage current may be attributed to several mechanisms, such as the improvement of surface roughness [155], variation of grain size [156, 157] or compensation of oxygen vacancies near the surface [142 – 144, 149, 152]. Detailed measurements were taken to clarify the reason why the leakage characteristics were enhanced. The surface morphologies of the as-deposited samples and samples O_2-plasma treated for 5 min samples were measured using the AFM, as shown in Fig. 6-3. The root-mean square (rms) roughness of the as-deposited and the 5-min O_2-plasma-treated samples were 7.581 nm and 7.584 nm, respectively. According to this figure, the surface roughness of the as-deposited BST films is not obviously different from that of samples treated by O_2 plasma for 5 min. Figure 6-4 shows the XRD patterns of the BST films post treated by oxygen plasma at various conditions. All of the samples, as-deposited and oxygen plasma treated, do not show obvious differences in XRD results, so the oxygen



(a) **(b)**

Figure 6-3 The surface roughness of (a) as-deposited BST thin films and (b) 5-min O_2-plasma-treated BST film.

plasma treatment does not change the BST crystalline structure. The preferential crystal orientation of each BST film, as confirmed by XRD, was (110). According to the Scherrer formula, the average grain size (<100nm) can be estimated by

$$D=0.9\lambda/(B*\cos\theta),$$

where D is the grain size, λ is the X-ray wavelength (~0.15428nm), B is the full-width at half-maximum (FWHM) of the XRD peak, and θ is the diffraction angle [153]. The FWHMs of all samples analyzed by XRD were identical, about 0.01725. Hence, the estimated grain size of each sample are almost the same, about 8.3 nm, as shown in Fig. 6-5. Those results of XRD analysis and grain size estimation are consistent with dielectric measurements. The dielectric constants of BST films do not shows greatly changes after post treatment using oxygen plasma, as indicated in Fig. 6-5.

On the other hand, the Auger electron spectroscopy (AES) profiles reveal the oxygen concentration distribution versus sputtering time, as depicted in Fig. 6-6. The

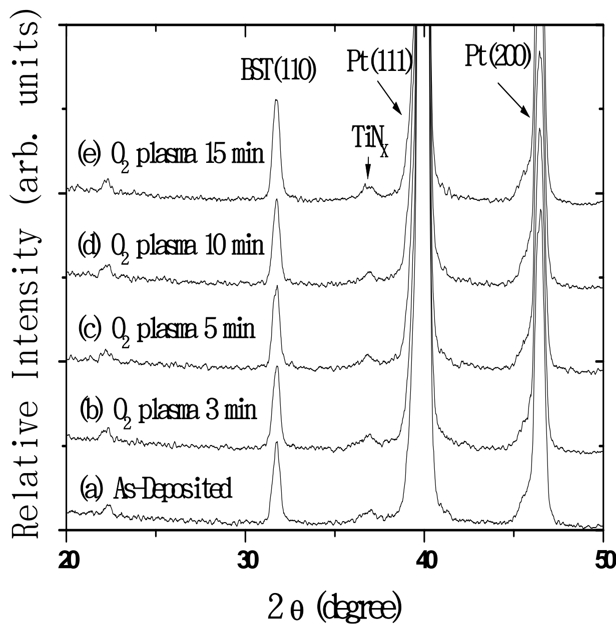


Figure 6-4 X-ray diffraction patterns of BST thin films with O_2 plasma treatment for different durations after BST film deposition.

sputtering time is proportional to the BST film depth, the direction of which is perpendicular to the top surface. The AES results show the samples post treated by oxygen plasma exhibit great oxygen passivation on BST surface. Obviously, the oxygen concentration at the top surface can be gradually improved by oxygen plasma treatment as the duration time increasing. Therefore, the improvement of leakage current at negative bias is primarily attributed to the compensation of surface oxygen vacancies. Moreover, the leakage currents in the high-electric-field region (0.3, -0.3 and 0.5 MV/cm) were also improved, and the PF transport mechanism dominated the leakage mechanism in such a region [142 – 144, 150, 151]. Therefore, the oxygen plasma treatment can compensate the oxygen vacancies not only on the surface but also in the bulk. The oxygen radicals in oxygen plasma are very active that they are able to oxidize BST films and compensate oxygen vacancies. However, the leakage current becomes degrading for the samples treated with long duration (> 5 min), and this degradation mechanism has been discussed above. Therefore, careful control of the duration time of the oxygen plasma treatment can obtain an optimal condition of the leakage current suppression.

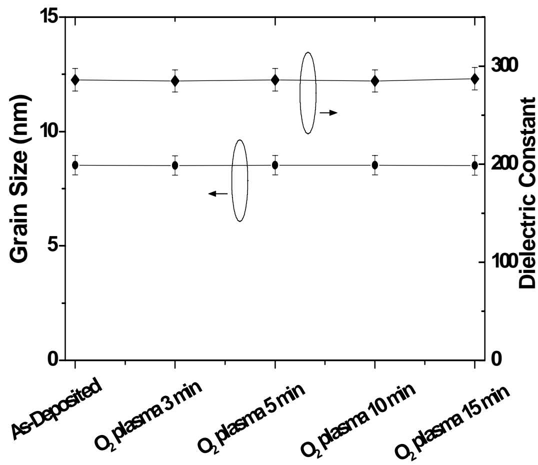


Figure 6-5 The dielectric constant and the estimated grain size versus the duration of O_2 plasma treatment on the BST films.

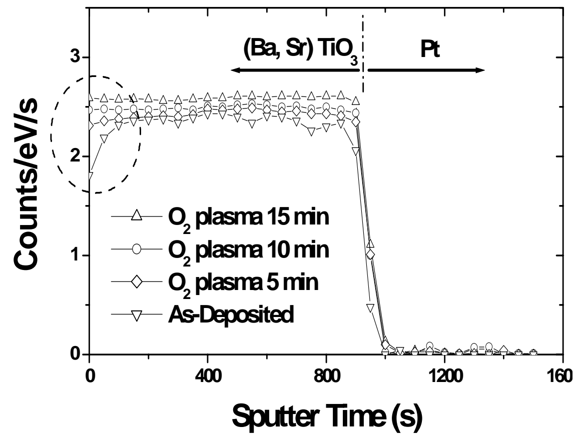


Figure 6-6 AES profiles of the BST films post treated by oxygen plasma under various treatment durations.

Figure 6-7 shows the TDDB characteristic of BST films without and with 5 min of oxygen plasma treatment. The lifetime extrapolation using constant-voltage stress gives a lifetime of ten years. For the 5-min-plasma treated samples, lifetime longer than 10 years in a stress field of 2 MV/cm can be obtained. In contrasting, the as-deposited samples exhibit very poor TDDB characteristics, and the 10 years breakdown field is as low as 0.6 MV/cm. In addition, the leakage current of the as-deposited Pt/BST/Pt capacitor is higher than that of 5 min oxygen-plasma-treated samples, reflecting that the increased leakage current accelerates the electrical degradation of the capacitors. Hence, the properly controlled treatment using oxygen-plasma can effectively improve the lifetime characteristics of the BST capacitors.

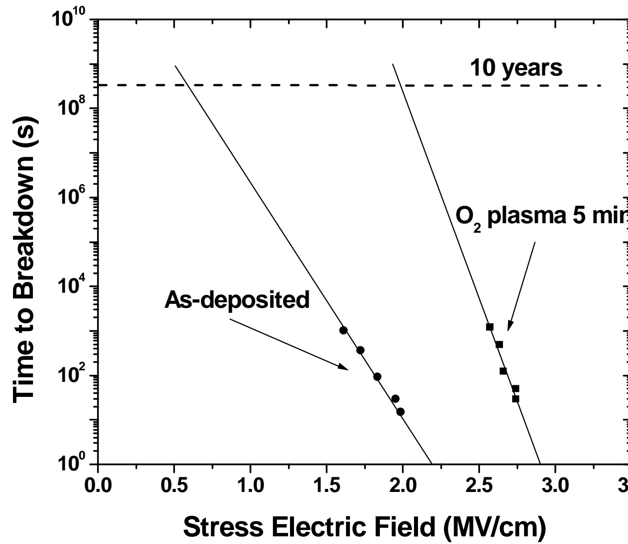


Figure 6-7 TDDB characteristics of the as-deposited/oxygen-plasma-treated BST films.

6-4 Summary

BST thin films fabricated by the RF sputtering technique or post surface annealing exhibits serious oxygen deficiency on top surface, and therefore the leakage current is severely degraded. Applying oxygen plasma treatment to the BST films can effectively passivate the oxygen vacancies at low substrate temperatures. The plasma technique significantly improves the leakage currents by reducing the concentration of oxygen vacancies in the as-deposited BST films. Excellent electrical characteristics, including a low leakage current (1.5×10^{-8} A/cm^2) under 0.1 MV/cm, high dielectric constant (288), and lifetime longer than 10 years under 2 MV/cm can be achieved. The suitable duration of the oxygen plasma treatment can effectively improve the leakage current, but a very extended duration will damage the BST film surface. Consequently, the proper and carefully controlled oxygen plasma treatment greatly suppresses the leakage current at

low temperature, and therefore this post treatment could be one of the most promising technologies for the integration of IC process.

Chapter 7

Thermal Stabilization Effects of Nano-scaled Cr Layer Integrated into BST Cell Capacitors

7-1 Nano-scaled Cr Layer used for Thermal Stabilization

In industrial applications, the operation junction-temperatures of DRAM range from 0 ^{o}C to 120°C (ambient temperature ranging from –40~85 ^{o}C for consumer IC's) in qualification spec, so the thermal stabilities of the electrical properties are the very crucial concerns for the device applications. BST and ferroelectric materials posses many excellent characteristics for capacitor applications, as reported in Chapter 1, but the most significant drawbacks are poor thermal stability and large leakage current during high temperature operations. The dielectric constant and the leakage current can decrease about 20% and increase 3-order, respectively, while the BST capacitor is operating from room temperature to 110° C [18, 19]. Such variations induced by thermal issues will lead to crucial concerns for the BST capacitor applied on DRAM's cell.

Crystall	Elements	Atomic Number	Atomic Radius (Å)	Crystall Structure	Lattice Constant (Å), 20°C, a
Cr	Cr	24	1.3	BCC	2.9
BST	Ti	22	1.47	Perovskite	3.9 (d_{011}=2.75 Å)
	O	8	0.6		
	Ba	56	2.2		
	Sr	38	2.2		

Table 7-1 The comparisons of the composition properties between Cr and BST crystals.

Many investigations reported that the electrical properties of thin films can be greatly altered by the impurity incorporation and interfacial conditions [158 – 160]. Table 7-1 indicates the comparisons of the composition properties between Cr and BST crystals. Cr and BST crystals exhibit BCC and perovskite structures, respectively, in room temperature. The lattice constant of Cr crystal in c-axis is similar to d_{011} of BST crystal in the <011> directions, and the atomic size of Cr atom is very close to that of Ti atom. Hence, the mechanical stress, occurred by the lattice mismatch, could be very small due to the compatible structures existing between Cr and BST layers. Therefore, a nano-scaled Cr layer was introduced to improve the electrical properties of BST thin film capacitor in this study. The novel sandwich structure of BST/nano-scaled Cr/BST multifilm intriguingly behaves excellent thermal stability and low leakage current. However, the thermal stability and the electrical properties can be greatly influenced by many factors, such as Cr layer thickness, interfacial interactions and crystallinity, so the corresponding mechanisms were systematically investigated in this chapter.

7-2 Experiments

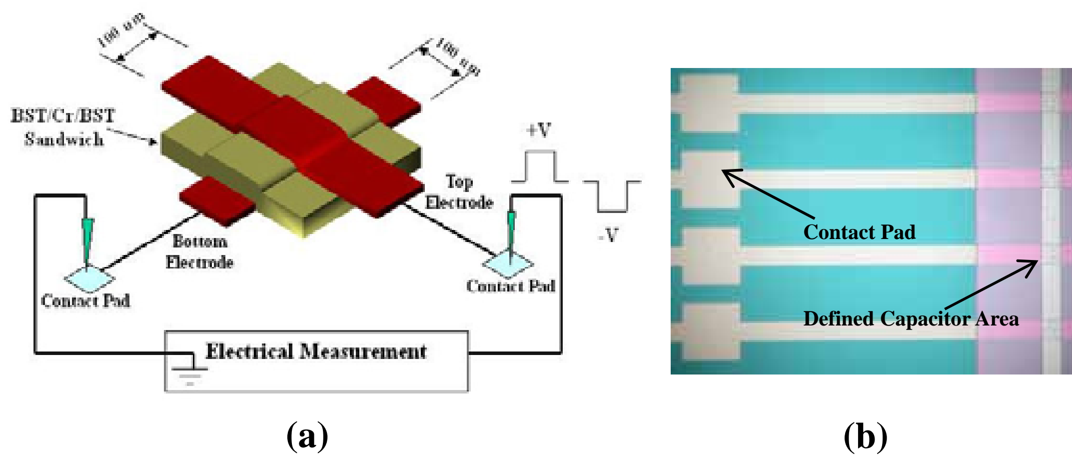


Figure 7-1 (a) The testing structure of Pt/BST/Pt/TiN/Ti multifilm with intercrossing top/bottom electrodes, and (b) the top view photograph of this intercrossing structure.

Figure 7-1(a) indicates a thin film capacitor of Pt/BST-sandwich/Pt/TiN/Ti with intercrossing top/bottom electrodes for temperature-electric properties testing. The capacitor area was defined as a square region of $100\mu m \times 100\mu m$, and the topographical picture was detected by a high resolution optical microscope, as shown in Fig. 7-1(b). Generally, directly probing the heated-BST film causes an extra thermal expansion stress, but the intercrossing electrodes, with indirect probing, can effectively prevent unwanted disturbance during thermal measurement.

Fig. 7-2 shows the fabrication process of the BST capacitor with intercrossing electrodes. Silicon wafers were initially cleaned by the standard RCA cleaning process, and SiO_2 of 500nm was fabricated by wet thermal oxidation. The Pt/TiN/Ti multi-film with a thickness of 100nm/50nm/10nm, serving as the metal/barrier/adhesion layers, was sputtered onto the SiO_2/Si substrate at room temperature. The sandwich structure of

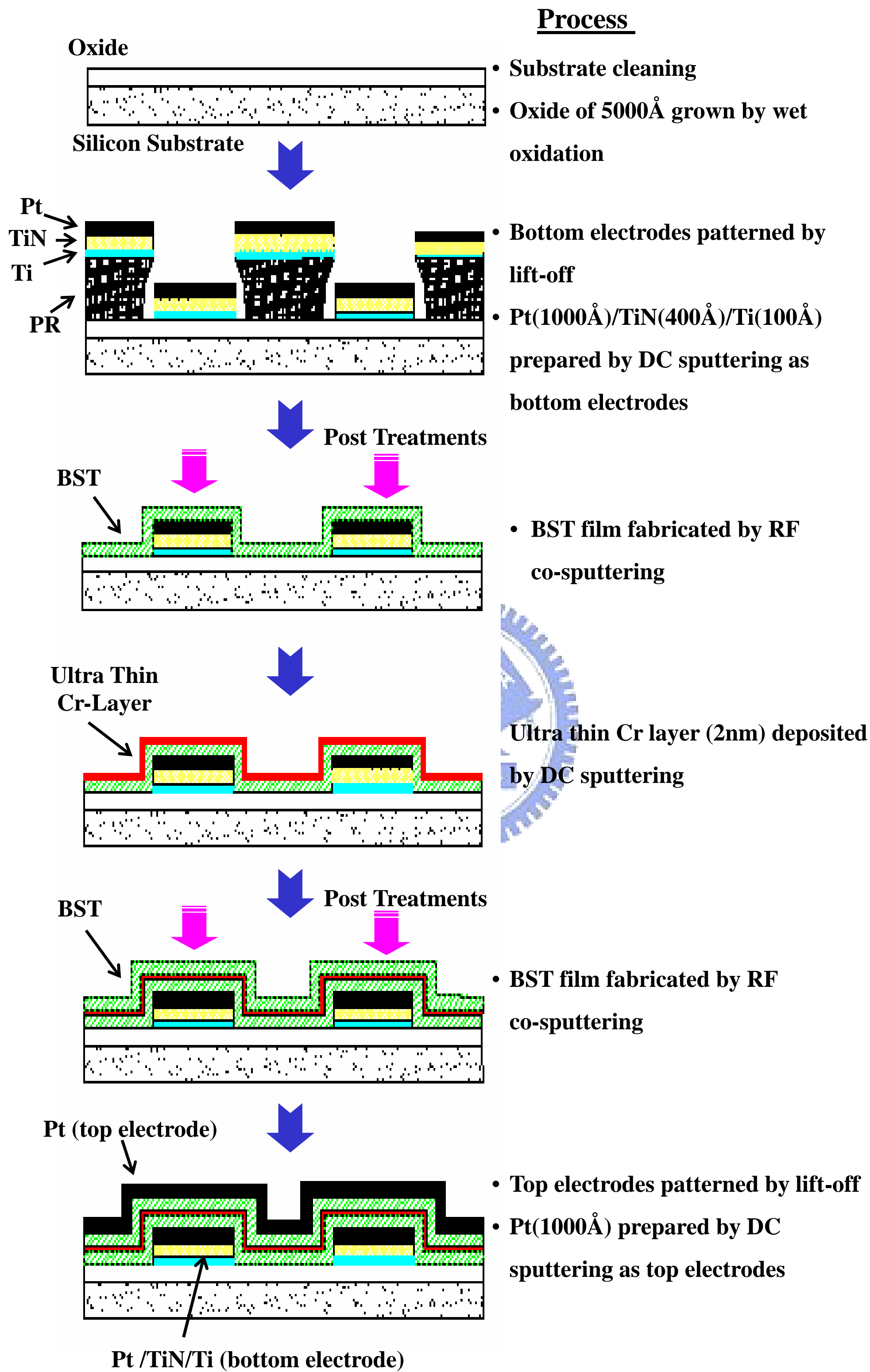


Figure 7-2 Fabrication process of the thermal testing capacitor with intercrossing electrodes.

BST(200nm)/Cr(1~3nm)/BST(200nm) multifilms were then deposited using a radio-frequency (rf) magnetron co-sputtering system at a substrate temperature of 300°C. The sputtering chamber was evacuated to a base pressure of 7x10^{-7} Torr, and then all films were deposited at a constant argon pressure of 6.8 mTorr. The rf powers used to deposit $BaTiO_3$ and $SrTiO_3$ were 185 and 185 W, respectively, yielding a Ba/Sr ratio of 8:2.

Microstructure and electrical analyses were performed to elucidate the detailed properties of the Pt/BST/Cr/BST/Pt multi-films capacitors. The crystallinity of the BST thin film was characterized by X-ray diffraction (XRD, Siemens D5000 diffractometer). From XRD patterns, besides the perovskite-BST phases and the Pt electrode, no additional second phases were detected, which means no significant difference in the crystal qualities of the BST thin film when incorporating the ultra-thin Cr film. The interfacial conditions and chemical composition of the BST/Cr interface were investigated by the cross-sectional TEM graphs and energy dispersive spectrometer (EDS), respectively. An automatic measurement system, combining an HP 4156A and a probe station, was employed to obtain the current-voltage (I-V) characteristics. The current-temperature testing was carried out using a hot plate. The dielectric-temperature properties including dielectric constant and tangent loss were also carried out by HP4194 and a hot plate.

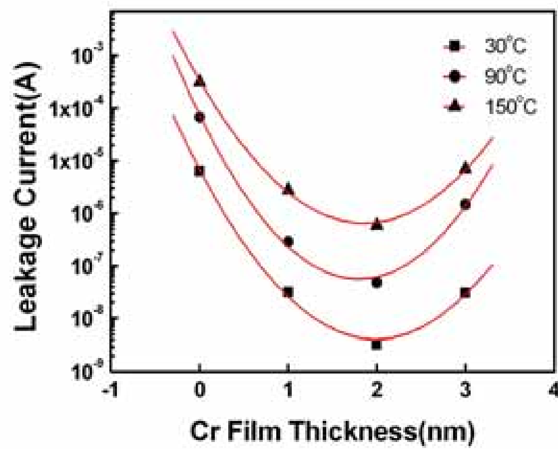
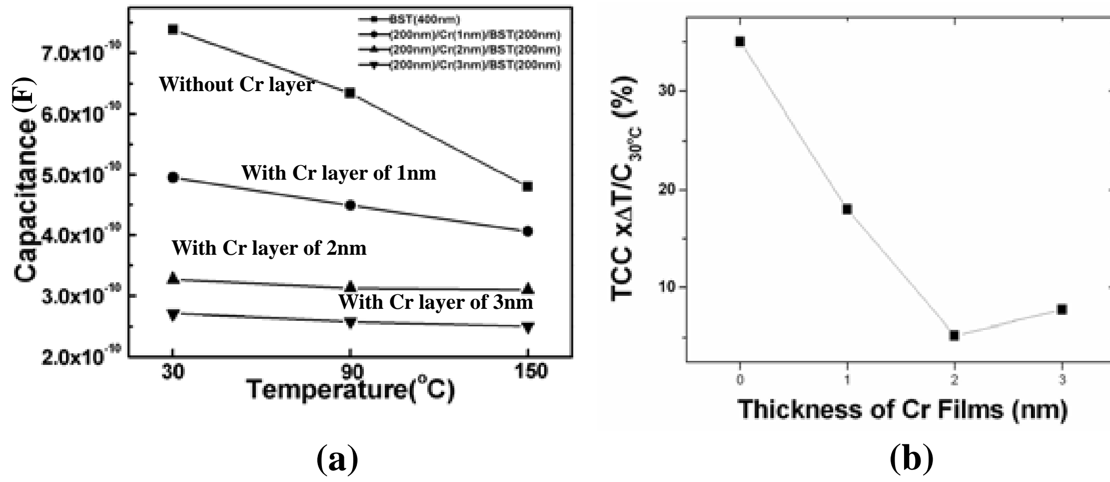


Figure 7-3 The leakage current versus Cr-thickness for the BST/nano-scaled Cr/BST under electric field of 125 KV/cm at various temperatures.

7-3 Thermal Stability and Leakage Current Improved by the Novel Structure of BST/nano-scaled Cr/BST Multifilms

7-3.1 Electrical properties of the BST/ultra-thin-Cr/BST multifilms

Figure 7-3 shows the properties of the leakage current versus Cr-thickness for the BST/Cr/BST multi-films under electric field of 125 KV/cm at various measuring temperatures. Obviously, the leakage current behaves as a function of the Cr thickness, and the minimum leakage can be obtained at 2 nm. Besides, the leakage current increases as testing temperature rises. However, the leakage current of the BST film with 2 nm Cr layer at 150°C is still lower than that without Cr layer at room temperature. Thus, the optimum leakage current properties can be obtained by adjusting the proper thickness of the Cr film.



(a) **(b)**

Figure 7-4 (a) Capacitance versus temperature with different Cr thickness and (b) Temperature Coefficient of Capacitance (TCC) of the BST/nano-scaled-Cr/BST multifilms measured from 30°C to 150°C.

The capacitance-variations of the BST/Cr(0~3nm)/BST multifilms were investigated at various temperatures, as shown in Fig. 7-4. The capacitance also reduces as the Cr thickness increases at a fixed temperature. Besides, the capacitance almost linearly decreases as the temperature increases, and the slopes of capacitance versus temperature indicate that the BST mono film (400nm) behaves more temperature sensitive than the BST(200nm)/nano-scaled Cr/BST(200nm) multifilm does. Furthermore, the temperature coefficient of capacitance (TCC) is defined below.

$$\text{TCC} = \frac{C_{T1} - C_{T2}}{T1 - T2} \tag{7-1}$$

where C_{T1} & C_{T2} are the capacitances measured at T1 & T2, respectively. In this work, T1 & T2 are 30°C & 150°C, respectively. Excellent thermal stability of capacitance exhibits low TCC value. Obviously, the TCC of the BST capacitor can be greatly

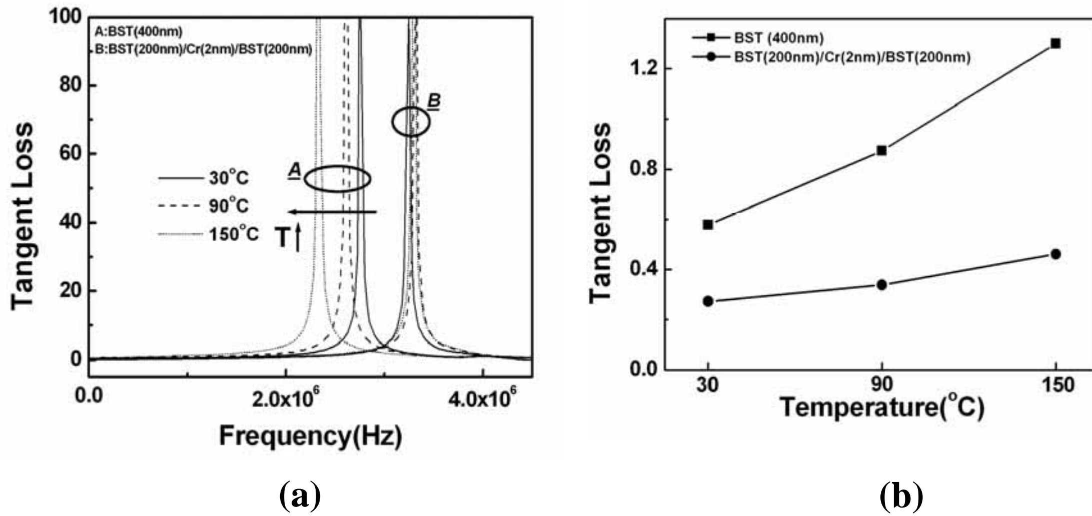


Figure 7-5 (a) The dispersion relation of tangent loss and (b) the tangent-loss for the mono BST layers (400nm) and the BST/nano-scaled-Cr/BST (200nm/2nm/200nm) at various temperatures.

reduced using the nano-scaled Cr film as a medium layer, as shown in Fig. 7-4(b). Furthermore, the TCCⅩΔT/$C_{30^{o}C}$ can be dramatically suppressed from 35% to 5% for the nano-scaled Cr layer of 2 nm thickness applied onto the BST capacitors. This phenomenon could be attributed to the ultra thin metal-oxide formed at the interface between BST/Cr layers, and the detailed mechanisms will be discussed later.

Figure 7-5(a) depicts the dispersion relation of the tangent-loss at various temperatures. Obviously, the resonance peak of tangent loss shifts from 2.8 MHz to 2.2 MHz for the BST mono-layer capacitor heated from 30°C to 150°C, as denoted in region A, but the resonance peak of the heated BST/Cr(2nm)/BST capacitor is almost fixed in the same frequency at various temperatures, as denoted in region B. Fig. 7-5(b) shows the tangent loss increasing as temperature rising, and the tangent loss of the

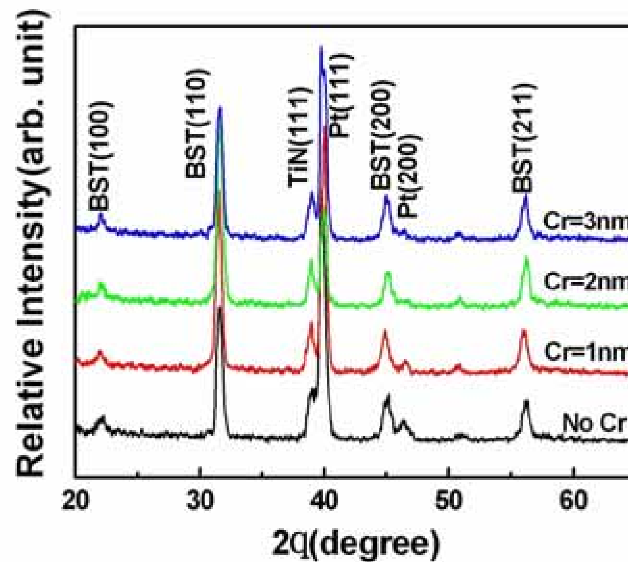


Figure 7-6 XRD patterns of BST/nano-scaled-Cr/BST thin films with various Cr thicknesses.

BST/nano-scaled Cr/BST multifilm is lower than that of the BST mono-film. Hence, the trend of the tangent loss is consistent with that of the leakage current. Hence, the resistive loss dominates the mechanisms of the tangent loss for both of the BST mono-film and the BST/nano-scaled-Cr/BST multifilm. In addition, the slopes of tangent-loss versus temperature indicate that the BST(200nm)/Cr(1~3nm)/BST(200nm) multifilm exhibits less temperature sensitivity than the BST mono-film (400nm) does.

7-3.2 Micro structure analysis

As mentioned above, the leakage property is strongly affected by the nano-scaled Cr layer, and therefore the microstructure analysis was carried out to study the

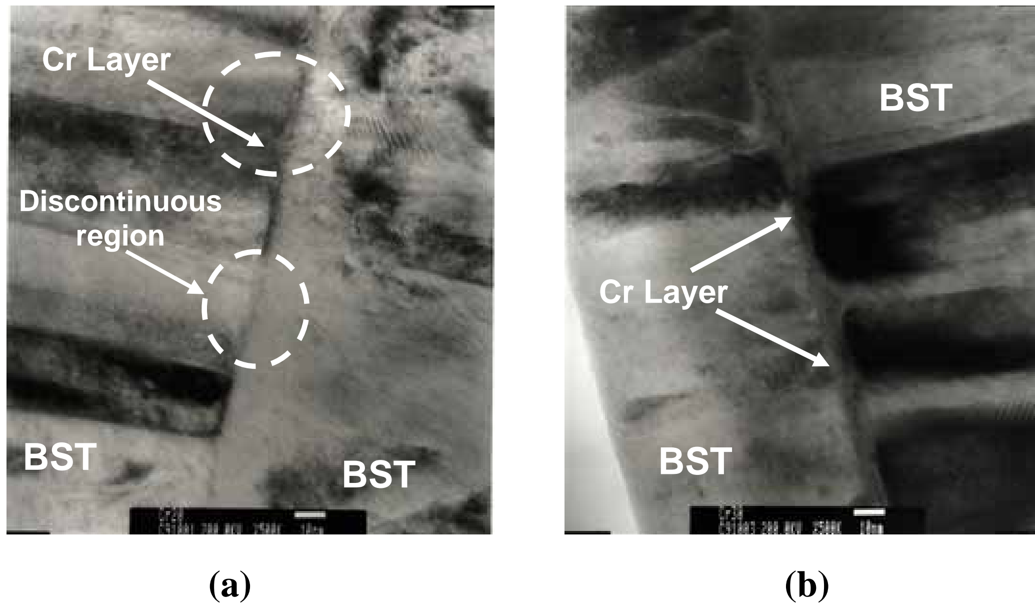


Figure 7-7 The cross sectional TEM pictures for the structures of (a) BST/Cr(2nm)/BST and (b) BST/Cr(3nm)/BST.

mechanisms in this section. First, XRD pattern reveals no significant differences among the BST films with/without inter-medium nano-scaled-Cr layer, as shown in Fig. 7-6. Hence, the nano-scaled Cr layer does not affect the crystallinity of BST films, so the interfacial effects between BST/Cr interface must be the major issues of the electric behaviors. Fig. 7-7 (a) and (b) show the TEM cross-sectional graphs of the BST/Cr/BST multi-films with the Cr layer of 2 nm and 3 nm, respectively. Fig. 7-7 (a) indicates the discontinuous Cr layer existing at the Cr (2nm)/BST interface. Obviously, this nano-scaled Cr layer is too thin to fully cover the whole BST thin film surface during sputtering. Those nano-scaled Cr layers, less than 2 nm, have only 5 or 6 atomic layers or less, which is very hard to perform good uniformity. Besides, low sputtering temperature (300°C), behaving insufficient activation/migration energy, results in discrete Cr cluster island growth [161, 162]. However, the uniformity, continuity and

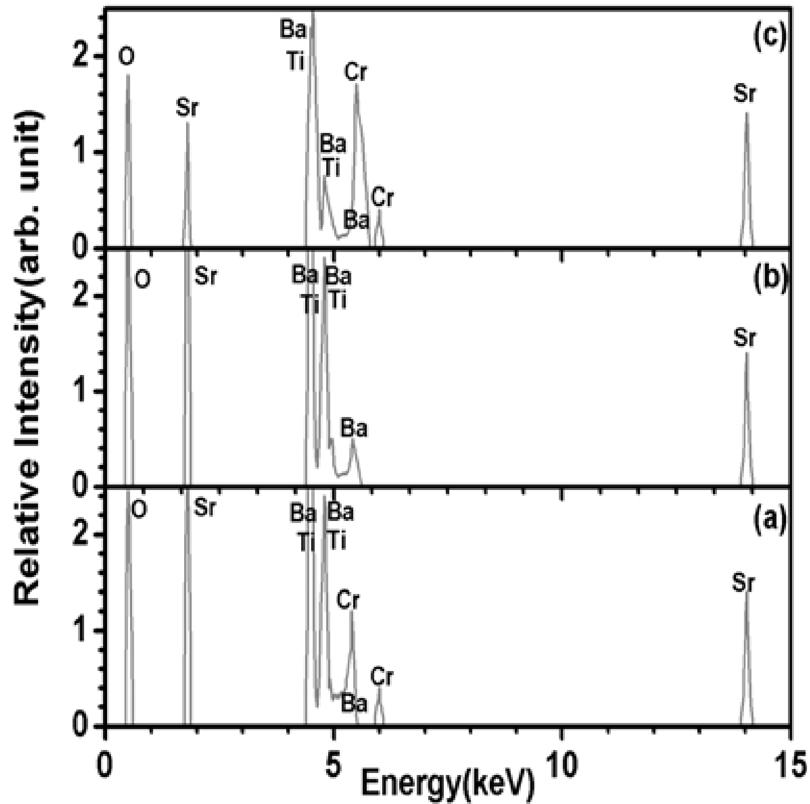


Figure 7-8 The EDS results of (a) Cr layer of BST/Cr(2nm)/BST (b) "discontinuous region" of BST/Cr(2nm)/BST and (c) any region at BST/Cr interface of BST/Cr(3nm)/BST.

interfacial properties can be improved by increasing the thickness of Cr layer, and therefore Fig. 7-7 (b) shows that the Cr layer, with thickness 3 nm or above, reveals continuous properties.

EDS was examined to analyze the chemical composition at the corresponding area in Fig. 7-7, as depicted in Fig. 7-8. Fig. 7-8 (a) shows the Cr peaks is consistent with the ultra-thin Cr layer in Fig. 7-7(a), but Fig. 7-8 (b) shows the discontinue Cr region does not exhibit Cr composition. Hence, nano-scaled Cr layer behaves discontinue property

for the Cr film deposited under the thickness of 2-nm. On the other hand, strong Cr peaks, examined in region of the BST/Cr (3nm) interface, indicate high uniformity and continuous Cr layer, as shown in Fig. 7-7 (b) and 7-8(c). Consequently, the chemical composition of EDS plots are consistent with the results of TEM graphs.

As discussed in the prior section, the leakage current and TCC are strongly affected by Cr thickness. The leakage current is dominated by bulk limitation due to BST deposited onto Pt/TiN/Ti/SiO2 substrate at low temperature [163]. Hence, the space charge and bulk defects will be the key factors for the leakage current in this study. Microstructure analysis reveals the ultra thin Cr thickness, less than 2nm, with only 6 atomic layers at most, results in the discontinuous Cr cluster and imperfect BST/Cr interface, which can form scattering centers and trapping states inside the BST(200nm)/Cr(1~2nm)/BST(200nm) films. Therefore, the leakage current of this sandwich BST structure can be greatly suppressed by the current scattering and the space charge redistribution. In addition, such Cr discontinuity and imperfect BST/Cr interface can be eliminated by the Cr thickness increasing beyond 3 nm, so the leakage current rises as the Cr film thickness increases. On the other hand, the nano-scaled Cr layer can also form the nano particles and ultra thin chrome-oxide, Cr_2O_3, which act as the series interfacial capacitors at Cr/BST interface. However, the capacitance of chrome-oxide behaves much less temperature sensitive than that of BST mono-layer film. Therefore, TCC of the BST/nano-scaled-Cr/BST multifilm is much smaller than that of BST mono-film.

7-4 Summary

Both of the leakage current and thermal stabilities can be greatly improved using the novel structure of metal/BST/nano-scaled-Cr/BST/metal multifilms instead of the conventional structure of metal/BST/metal films. The leakage current can be dramatically reduced by applying nano-scaled-Cr layer onto BST capacitor due to the scattering centers and abnormal space charge field formed at the interface between BST and Cr. Besides, Chrome-oxide forms the series capacitance, behaving temperature insensitivity, which can dramatically reduce the TCC of BST/nano-scaled-Cr/BST capacitor. The tangent loss and dispersion relation also reveal temperature stabilized properties using the novel structure of BST/nano-scaled-Cr/BST multifilm. According to the above discussion, both of the leakage current and TCC behave as functions of Cr thickness, so the optimal properties can be also obtained by adjusting the Cr thickness.

The results of microstructure analysis interpret the electrical properties and thermal stabilization effects are attributed to the imperfect interface formed between BST/Cr layers. Hence, a well controlled Cr thickness can greatly improve the thermal stabilities and the leakage current of BST films. Consequently, this novel structure can be one of the promising solutions for the practical applications of BST DRAM capacitor due to its excellent thermal stability and electrical property.

Chapter 8

Conclusions and Future Prospects

8-1 Conclusions

This thesis dedicated in the studies of the novel low-temperature technologies applied on the Pt/BST/Pt/TiN/Ti/Si multifilms as advanced DRAM capacitors. Several process technologies have been applied to enhance material and electrical performance. Excellent dielectric properties can be obtained, and the corresponding analysis was also investigated in this thesis. This chapter will summarize the major contributions below.

(1) The BST thin films, with good crystallinity and dielectric properties, can be prepared by co-sputtering system using dual sputtering-guns at very low substrate temperature of 410°C. Optimal characteristics can be properly controlled by

Material & Electric Characteristics / Process Parameter	Deposition Rate	Crystallinity	Ba/Sr Ratio	Dielectric Constant	Leakage Current
OMR	▲	●	▲	●	●
Power Ratio of the BTO/STO Sputtering-guns	X	▲	●	▲	X
Ambient Work Pressure	●	X	X	X	X
● - Strong Factor, ▲ - Mid Factor, X - Weak Factor or No Influence					

Table 8-1 Comparing with various process parameters for the influences on material and electric properties of BST thin film sputtered at low temperature.

processing parameters, as listed in Table 8-1. Since the BST film was prepared at very low substrate temperature, very few process parameters can be used for thin film property controls. Obviously, OMR is the most significant factor for the low temperature co-sputtering system. However, the maximum dielectric constant, comprehensively determined by crystallinity and grain size, can be obtained by properly adjusting the OMR to 5% during thin film sputtering.

(2) BST films sputtered at high OMR behave small leakage current density, a low tangent loss and a long lifetime, due to compensation of oxygen vacancies, a smooth surface morphology and voltage shared by smaller grains. The leakage mechanisms of the Pt/BST/Pt capacitor can be attributed to Schottky emission (SE)/Poole-Frenkel emission (PF) at lower/higher applied field. The leakage mechanism analysis concludes the relationship between the interfacial properties and process parameters. Hence, the optimal characteristics of the BST capacitor can be obtained by proper controls of the sputtering parameters.

(3) The crystallinity and dielectric properties of the low-temperature sputtered BST film can be further enhanced by ELA technique under very low substrate temperature 300°C. Further applying oxygen plasma treatment onto the BST films can effectively passivate the oxygen vacancies at low substrate temperatures. The electric enhancement of the ELA and the oxygen plasma treatments are concluded in Table 8-2. The experimental results for the BST films post treated by ELA and oxygen plasma techniques are further summarized below.

a. Dielectric property can be greatly enhanced by ELA treatment, but the leakage current and the TDDB reliability exhibit worse results after ELA. Thermal and electrical analysis indicated the ELA process carries out the recrystallization and grain regrowth from upper surface to interior region, and, particularly, it

Process	*Process Status*	Dielectric Constant (ε_r)	Leakage Current Density Biased at 100KV/cm (A/cm^2)	10 Years TDDB Electric Field (MV/cm)
ELA Treatment	*as dposited film*	90	$10^{-8} \sim 10^{-7}$	2.4
	after ELA treatment	250 ~ 400	$10^{-6} \sim 10^{-5}$	0.5
Post Oxygen Plasma Treatment	*before treatment*	288	$10^{-6} \sim 10^{-5}$	0.4
	after treatment	288	$10^{-8} \sim 10^{-7}$	2.3

Table 8-2 Electric properties of the BST films before/after post treatments using ELA and oxygen plasma techniques.

would not affect the underlayer structures at all. Increasing laser energy fluence can enhance the crystallinity of BST film, but excessive energy fluence creates too many oxygen vacancies and surface defects, degrading the BST films. Therefore, the dielectric enhancement and leakage current suppressing are the trade-off concerns for ELA technology.

b. The laser energy fluence, the thickness, thin film structures and substrate temperature strongly influence the properties of the ELA BST films. The Pt/TiN/Ti/Si substrate behaves very high thermal conductance, which results in a narrow process window of dielectric enhancement using ELA technique. Both of the laser energy fluence and the BST film thickness must be carefully controlled to obtain an optimal BST film with excellent dielectric properties.

c. The ELA-treated BST film behaves large leakage current due to oxygen deficiency on top surface. Applying oxygen plasma treatment onto the BST

Structure \ Electric Properties	J/K (A/cm^2)	TCC
BST (400nm)	5.9×10^{-6}	35%
BST(200nm)/Cr(2nm)/BST(200nm)	7.9×10^{-9}	5%

Table 8-3 Comparisons of the electric properties between BST mono-layer film and BST/nano-scaled Cr/BST multifilm.

films can effectively passivate the oxygen vacancies at low substrate temperatures. Hence, this plasma technique can further improve the leakage currents after film fabrications due to the oxygen vacancies compensated on the top surfaces of the BST films.

(4) Leakage current and thermal stabilities can be greatly improved using the novel sandwich structure of BST/nano-scaled-Cr/BST, as shown in Table 8-3. A proper thickness of the Cr layer can greatly suppress the leakage current even though the devices operate at high temperature of 120°C. Besides, this novel sandwich structure behaves excellent thermal stabilities in capacitance, tangent loss and dispersion relation of electric properties. TCC can be greatly reduced from 35% to 5% for the nano-scaled-Cr layer applied onto BST capacitor as inter-medium layer.

8-2 Future Prospects

BST capacitor will be the most promising solutions for new generation DRAM cell capacitor due to its outstanding dielectric properties, but the integration issues shall be the big challenges for the practical applications. Therefore, the low temperature is

indeed necessary for the implementations of BST capacitor, and some of the innovative topics are worth to further investigate, as listed below.

(1) BST thin films deposited onto conductive perovskite-ceramic electrodes, such as $La_xSr_{1-x}CoO3$, $La_xSr_{1-x}MnO_3$, $SrRuO_3$ and $LaNiO3$, behave better dielectric properties than those deposited onto Pt electrode. However, the low temperature processes applied on such conductive perovskite-ceramic lack systematical studies, so those low temperature techniques are worth further investigations.

(2) Large area ELA treatment is necessary for practically industrial applications of BST thin films due to high throughput and good uniformity requirements. Although scanning ELA system has been widely applied on TFT industry, it still lacks systematical system for BST thin film capacitor.

(3) The oxygen plasma with very long duration and high energy can damage the surface of BST thin film, and therefore the low energy oxygen plasma is necessary to enlarge the process window during oxygen-vacancy compensation. Hence, ECR-oxygen-plasma technology can be considered to passivate the BST surface.

(4) The interfacial characteristics of the novel sandwich structure of BST/nano-scaled-metal/BST need to be further studied. There shall be plenty of nano-scaled phenomena exhibiting at BST/metal interface. The nano particles formed by metal oxide and imperfect interface can be further analyzed for correlated electrical properties and thermal stabilization.

(5) In general, the Cr diffusion may greatly influence the characteristics of BST films, so the material analyses of Cr doping can be further investigated for the TCC/leakage reducing in the thin BST film.

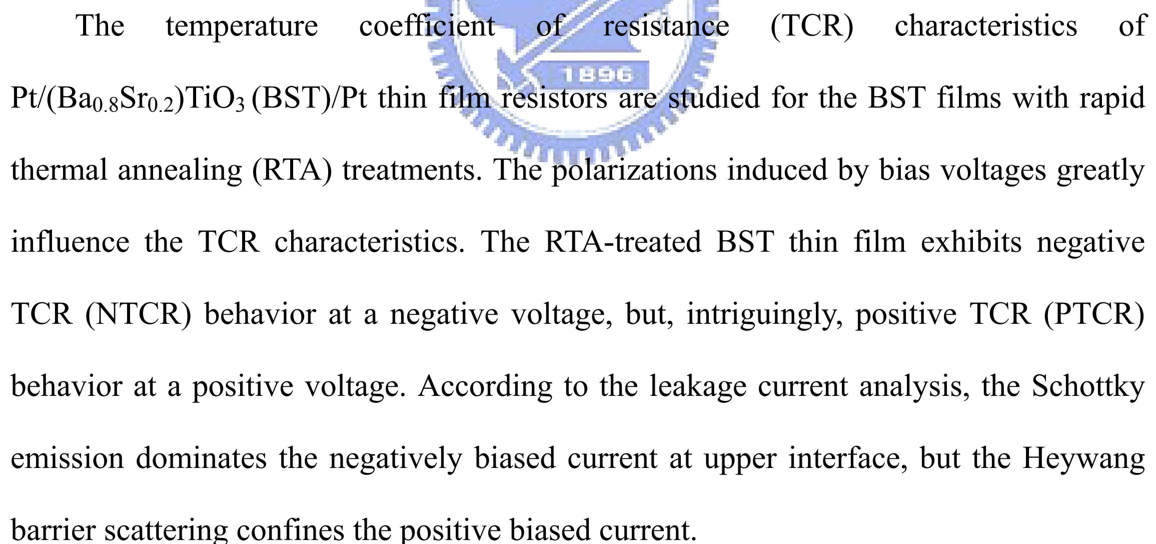
(6) Low-temperature BST capacitor can be further integrated with CMOS devices to

recognize its real operation performance in DRAM circuits.

Appendix A

Dependence of Polarization on Temperature-Coefficient-Resistance of (Ba, Sr)TiO_3 Thin Films Post Treated by Rapid Thermal Annealing

A.1 Abstract



The temperature coefficient of resistance (TCR) characteristics of Pt/($Ba_{0.8}Sr_{0.2}$)TiO_3 (BST)/Pt thin film resistors are studied for the BST films with rapid thermal annealing (RTA) treatments. The polarizations induced by bias voltages greatly influence the TCR characteristics. The RTA-treated BST thin film exhibits negative TCR (NTCR) behavior at a negative voltage, but, intriguingly, positive TCR (PTCR) behavior at a positive voltage. According to the leakage current analysis, the Schottky emission dominates the negatively biased current at upper interface, but the Heywang barrier scattering confines the positive biased current.

A.2 Introduction

During the past decades, high temperature-coefficient-resistivity (TCR) materials have been widely applied on thermistors as thermal detectors due to their low cost and

excellent thermal responsivity [A.1]. The abnormally high positive TCR (PTCR) of $BaTiO_3$ (BTO) ferroelectric materials, observed at the Curie temperature (Tc) in 1955 [A.2], have attracted much attentions on their applications and conduction mechanisms. Thermal detectors that use positive TCR (PTCR) material can prevent the effect of thermal-run-away, so the complementary circuits can be greatly simplified [A.3]. The substitution of Sr for Ba in BTO solid solution, forming $(Ba,Sr)TiO_3$ (BST), can effectively adjust the Curie temperature to obtain proper operation conditions of a thermistor.

Techniques for fabricating microelectromechanical systems (MEMs) and integrated circuits (ICs) are generally applied to high TCR microthermistors [A.4]. However, a low-thermal-budget process must be implemented to prevent damages to the under-layer structures of MEMs and embedded ICs. In this work, the BST films were post treated by rapid thermal annealing (RTA), which is a low-thermal-budget technique, to yield excellent electrical properties. Many studies have considered the TCR effect of the bulk BST, but very few have reported the TCR effect of the thin BST films [A.1, A.5]. The conduction current of a BST was measured at temperatures ranging from room temperature to $410^{o}K$, and the conduction mechanisms were investigated systematically.

A.3 Experimental

Figure A-1 indicates a thin film resistor of Pt/BST/Pt/TiN/Ti with intercrossing top/bottom electrodes for TCR testing. Generally, directly probing the the heated-BST

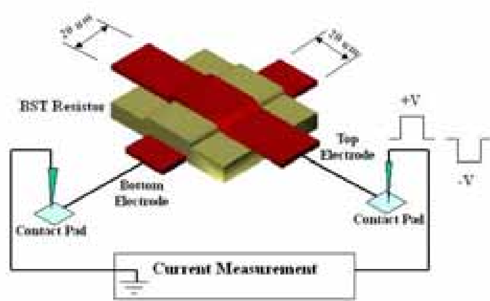


Figure A-1 The testing structure of Pt/BST/Pt/TiN/Ti multifilm with intercrossing top/bottom electrodes.

film causes an extra thermal expansion stress, so the intercrossing electrodes prevents unwanted disturbance during TCR measurement. The testing area (20×20 μm^2) of this thin film is defined by the overlap between the top and bottom electrodes, and both the top and bottom electrodes are patterned using the lift-off technique. The p-type Si(100) silicon wafers were initially cleaned by the standard RCA cleaning process, and SiO_2 of 500nm was fabricated by wet thermal oxidation. The Pt/TiN/Ti multifilm with a thickness of 100nm/50nm/10nm, serving as the metal/barrier/adhesion layers, was sputtered onto the SiO_2/Si substrate at room temperature. $Ba_{0.8}Sr_{0.2}TiO_3$ film (300nm) was then deposited using on RF magnetron co-sputtering system at a substrate temperature of 300 ^{o}C. The sputtering chamber was evacuated to a base pressure of $7x10^{-7}$ Torr, and then all films were deposited at a constant argon pressure of 6.8 mTorr. The RF powers used to deposit $BaTiO_3$ and $SrTiO_3$ were 185 and 185 Watts, respectively, yielding a Ba/Sr ratio of 8:2. The BST films were subsequently post treated by RTA (1 minute) at 500°C or 600°C.

The crystallinity was then characterized by X-ray diffraction (XRD, Siemens D5000 diffractometer). The XRD patterns show the polycrystalline nature of the perovskite-BST formed in all cases of this work. The current-temperature characteristic was studied using the Pt/BST/Pt (metal-insulator-metal, MIM) structure. Then, the

testing voltage was biased on the top electrode, and the bottom electrode is grounded. An automatic measurement system, combining an HP 4156A and a probe station, was employed to obtain the current-voltage (I-V) characteristics of BST resistors. The current-temperature testing was carried out using a hot plate.

A.4 Results and Discussion

The temperature-coefficient-resistivity (TCR) is defined according to the following formulas [A.4, A.6].

$$TCR = \frac{1}{Rs}\frac{dRs}{dT}\Big|_T \qquad (A.1)$$

where T and Rs represent the temperature and the resistance, respectively. Figure A-2 plots the resistances and the TCR of the BST films (a) without post treatment, and with

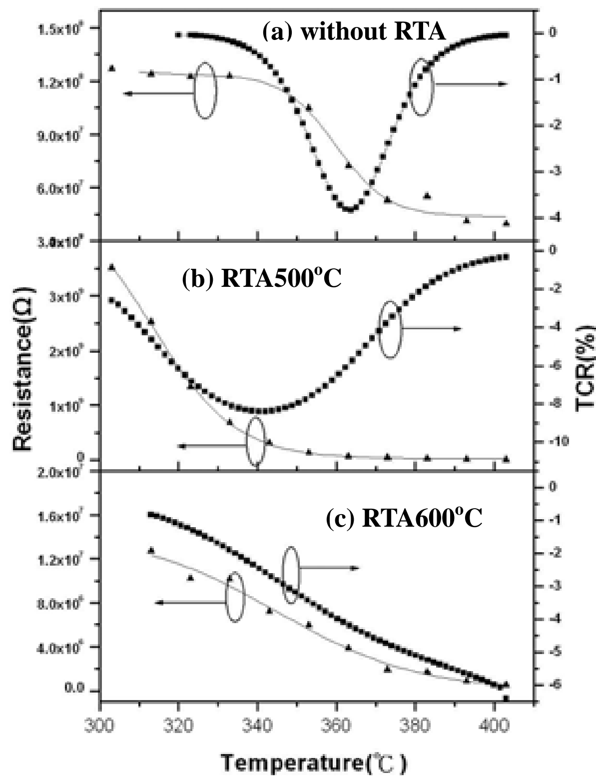


Figure A-2 The resistances and the TCR of the BST films polarized at –3 volts for the films (a) without RTA and with RTA treatment at (b) 500°C and (c) 600°C.

post RTA treatments at (b) 500°C or (c) 600°C at –3 Vol＜s. The resistances of all these films polarized at a negative bias decrease as the temperature increases. Hence, these negative polarized films behave negative TCR (NTCR), which is greatly enhanced for the BST films post treated by RTA at 500°C and 600°C. A maximum NTCR as high as 8.6% was achieved at a bias of –3 Volts for the RTA 500°C sample. However, the RTA 500°C and 600°C samples show different TCR trends due to the differences in Rs, as calculated in Eq. (A-1). In general, the conduction current of BST film is induced by the presents of oxygen vacancies according to the equation:

$$O_0 \leftrightarrow V_0^{++} + 2e^- + 1/2O_2 \qquad (A\text{-}2)$$

where O_0, V_0^{++} and e^- denote the oxygen ion in its normal site, an oxygen vacancy and electron, respectively. However, a high concentration of oxygen vacancies led to n-type conductivity of the BST materials due to the electrons generated, causing large leakage currents. The leakage current of a BST film with RTA treatment in oxygen ambient is suppressed because the O_2 ambient gas compensates oxygen vacancies. An excessive

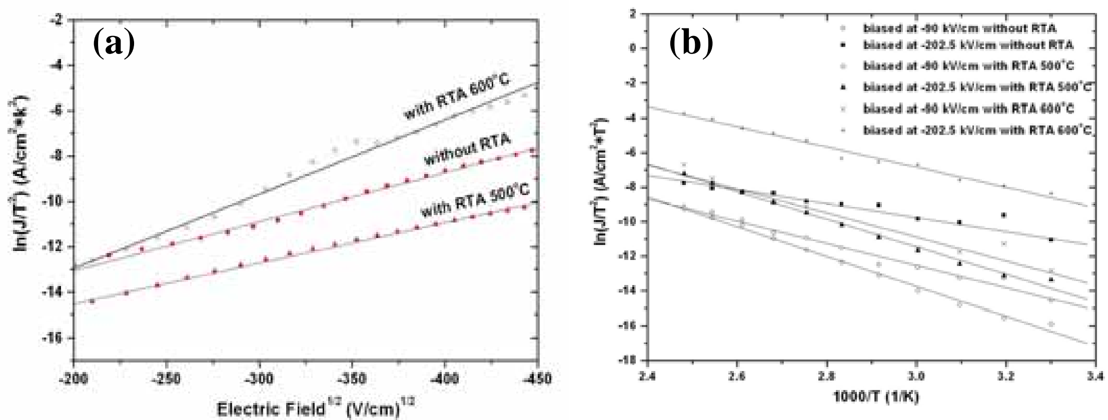


Figure A-3 The log (J/T^2) versus (a) $E^{1/2}$ and (b) 1/T plots showing Schottky emission fitting for the BST films treated with various RTA conditions at negative bias.

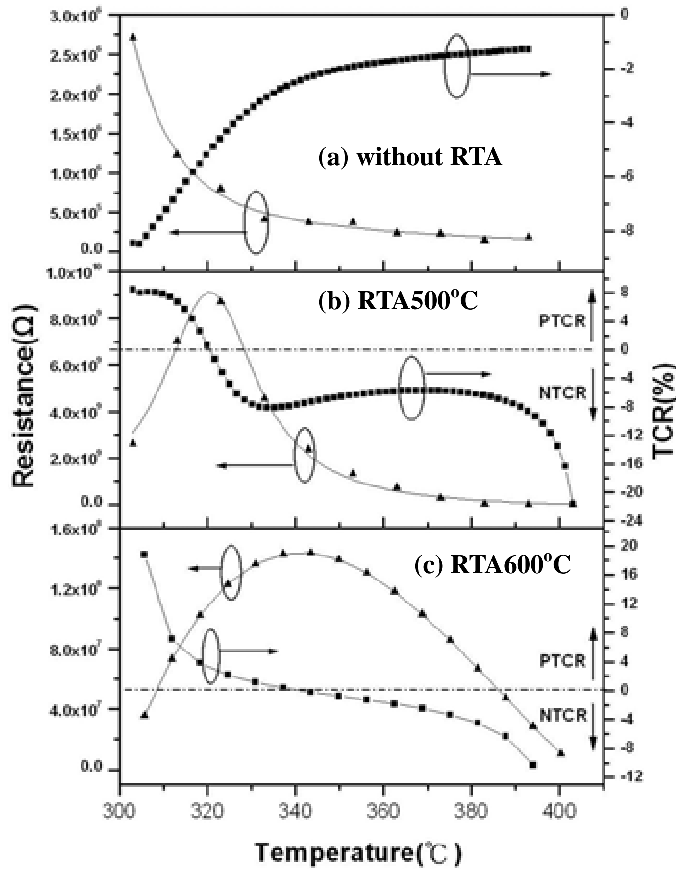


Figure A-4 The resistances and the TCR of the BST films polarized at +3 volts for the films (a) without RTA and with RTA treatment at (b) 500°C and (c) 600°C.

RTA temperature induces interface stress and oxygen vacancies, degrading the BST films, so the conductance of BST increases with RTA temperature rises.

The conduction mechanisms of metal/ferroelectric/metal (MFM) resistors are usually interpreted as interface-limited and bulk-limited conductions [A.7-A.8]. In general, Schottky emission (SE) governs the interface-limited current in the Pt/BST films, and the leakage current is expressed as

$$\log (J_{SE}/T^2) = -q[\varphi_B - (qE/4\pi \varepsilon_d \varepsilon_o)^{1/2}] /(kT \cdot \ln 10)+\log(A^*) \quad (A.3)$$

where, A^* is the effective Richardson's constant; φ_B is the potential barrier height at the surface; ε_d is the dynamic dielectric constant of the ferroelectric material in the infrared region; q is the unit charge; k is Boltzmann's constant; T is temperature, and E is the

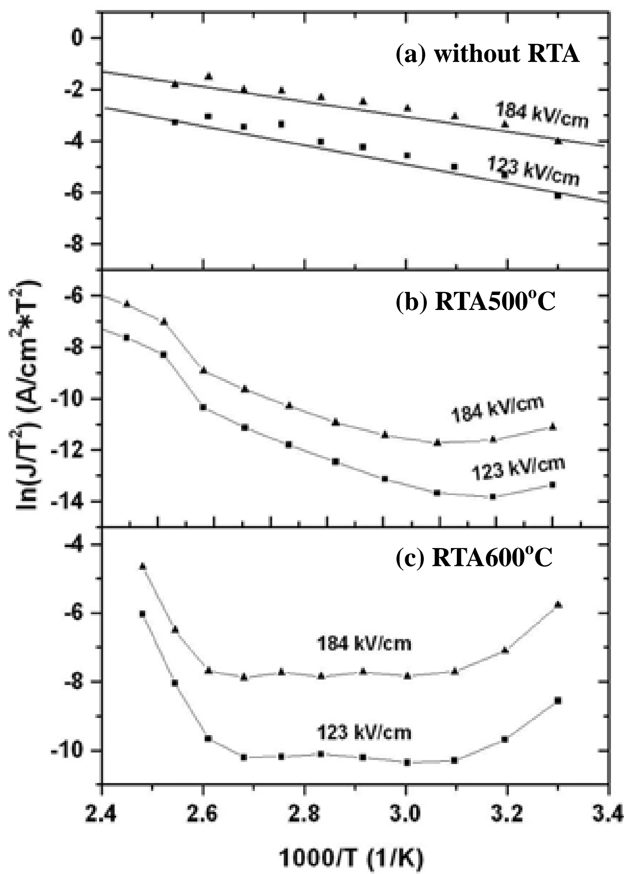
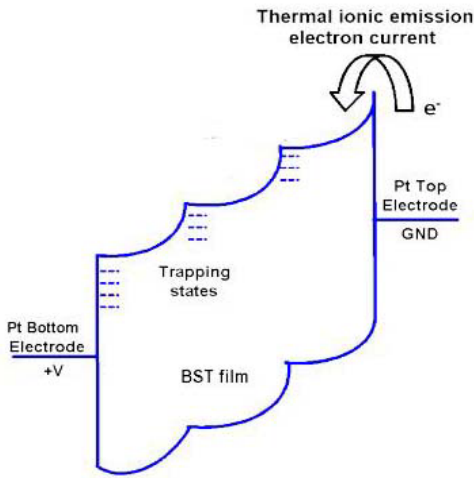


Figure A-5 The log (J/T^2) versus 1/T plot showing Schottky emission fitting for the BST films with various RTA conditions at positive bias.

external electric field. If the conduction current is governed by SE behavior, then $\log(J/T^2)$ against $E^{1/2}$ and 1/T plots should be linear [A.9]. Figure A-3 (a) shows that all the plots of $\log(J/T^2)$ against $E^{1/2}$ exhibit linear relationships at negative bias. Additionally, the plots of $\log(J/T^2)$ against 1/T exhibit linear relationships at negative bias, as shown in Fig. A-3 (b). The leakage current of the RTA 600°C samples exceeds that of the 500°C samples because φ_B is decreased by increasing the concentration of oxygen vacancies [A.8]. However, all the samples biased at negative voltage show Schottky emission behavior.

Figure A-4 presents the resistances and the TCR of the BST films polarized at a positive bias. The BST film without RTA treatment exhibits NTCR at +3 V, as shown in

Interface limited



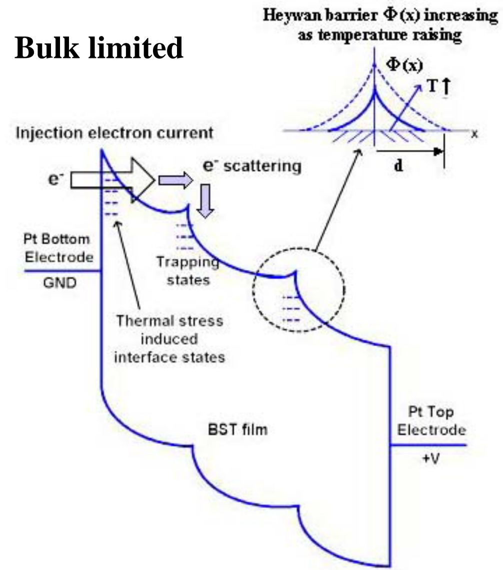


Figure A-6 The electron energy bands for the RTA-treated BST films biased at (a) negative and (b) positive voltages.

Fig. A-4 (a), but the films treated with RTA 500°C and 600°C reveal positive TCR (PTCR) in a temperature range for measuring temperature from 300°K to 370°K, as shown in Figs. A-4 (b) and (c). Figure A-5 plots $\log(J/T^2)$ against 1/T for the BST films biased at +3V. The BST film without RTA treatment exhibit SE behavior, as denoted in Fig A-5 (a), but the films treated with RTA at 500°C and 600°C do not exhibit SE behavior at all, as shown in Figs. A-5 (b) and (c).

The electron energy bands explain the NTCR/PTCR effects of the RTA-treated BST under negative/positive bias, as represented in Fig. A-6. The BST films post treated by RTA in oxygen ambient are greatly improved due to the compensation for oxygen vacancies at the upper surface; accordingly, SE behavior dominates the conduction current at a negative bias, as indicated in Fig. A-6(a). Hence, the negative-biased conduction current exhibits an NTCR effect according to the current-temperature

relation of Eq. (3). However, the BST/Pt films treated by RTA at a temperature exceeding 500°C will be subjected to a large thermal stress due to the abrupt fall in temperature, and thus many defects are induced at the interface of BST/Pt-bottom-electrode interface. The thermal-stress-induced interface states generated the injected electron current. Thus, the conduction current of the BST film post treated by treatment is bulk limited under positive bias, as indicated in Fig. A-6(b). Generally, the barrier scattering or the charge detrapping rate governs bulk-limited current [A.10, A.11]. The current-temperature relationship for the grain boundary scattering is deduced using the Heywang formula around the transition temperature (Tc) for ferroelectric materials according to [A.1, A.11]

$$Rs \propto \exp(-q\phi / kT) \tag{A-4}$$

$$\phi = \frac{e^2 N_d d^2}{2\varepsilon\varepsilon_0}$$

where Rs is the resistance of the sample; Φ and d are the potential height and depletion width at grain boundaries; μ and Nd present the electron mobility and the donor concentration in the film, and k is the Boltzman constant. The barrier height according to the Heywang model increases with temperature. The Heywang barrier scattered the injected-current at a positive bias, and thus this bulk-limited current exhibits the PTCR phenomenon

A.5 Conclusions

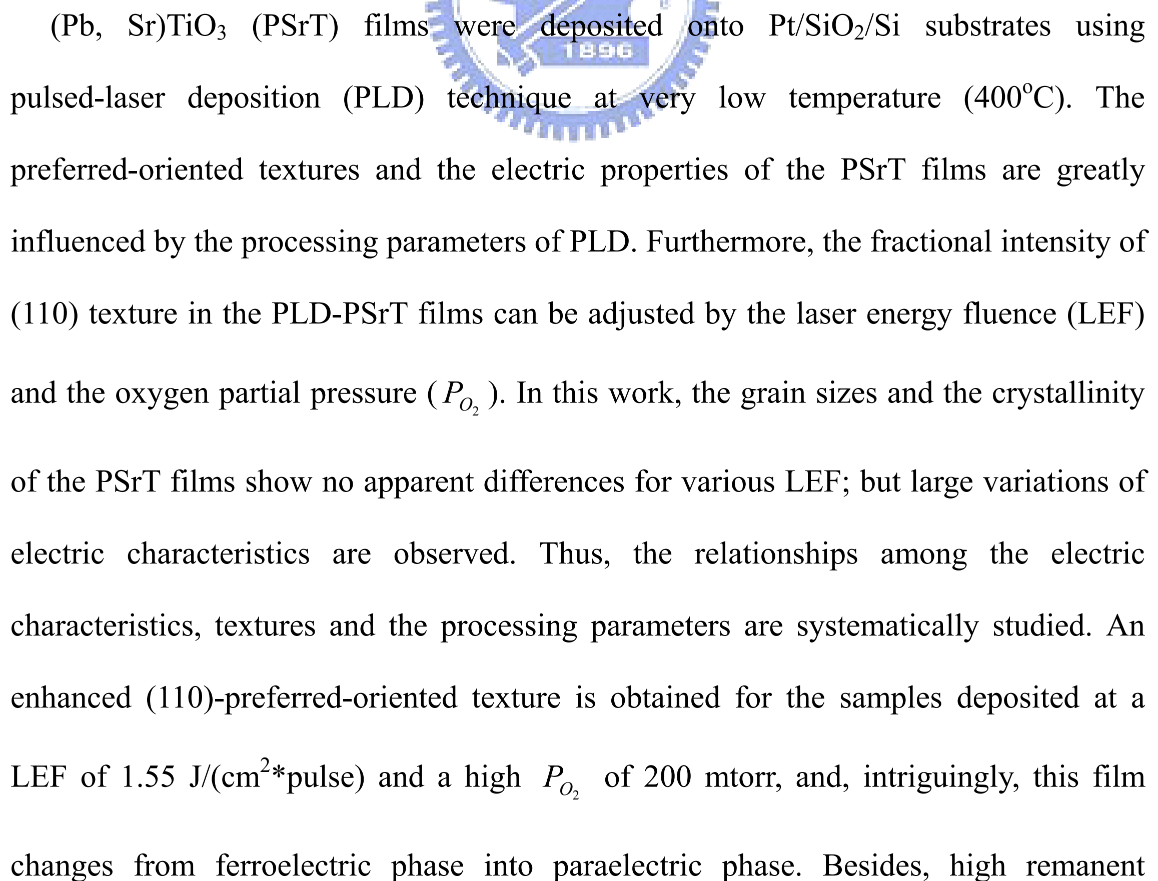
In this work, all of the Pt/BST/Pt thin films polarized at negative bias reveal NTCR

behavior, but the RTA treated samples polarized at positive bias exhibit PTCR behavior. The leakage current of the samples with RTA treatment increased due to increasing oxygen vacancies, but all the samples formed Schottky barrier because the O_2 ambient gas compensated oxygen vacancies at upper surfaces. Hence, SE dominates the conduction current of the sample biased at negative voltage, inducing the NTCR phenomenon. RTA treatment results in a steep gradient of the temperature decrease across the interface between the bottom electrode and the BST film, and thus induces residual thermal stress. The injected electron current is therefore formed by the thermal-stress-induced interface states at positive bias, and this bulk-limited current is governed by Heywang barrier scattering. Hence, the positive biased RTA-treatedBST film exhibits the PTCR phenomenon.

Appendix B

Effects of Low-temperature Processing Parameters on Structure Controls and Electric Properties for PLD-(Pb,Sr)TiO_3 Films

B.1 Abstract



(Pb, Sr)TiO_3 (PSrT) films were deposited onto Pt/SiO_2/Si substrates using pulsed-laser deposition (PLD) technique at very low temperature (400°C). The preferred-oriented textures and the electric properties of the PSrT films are greatly influenced by the processing parameters of PLD. Furthermore, the fractional intensity of (110) texture in the PLD-PSrT films can be adjusted by the laser energy fluence (LEF) and the oxygen partial pressure (P_{O_2}). In this work, the grain sizes and the crystallinity of the PSrT films show no apparent differences for various LEF; but large variations of electric characteristics are observed. Thus, the relationships among the electric characteristics, textures and the processing parameters are systematically studied. An enhanced (110)-preferred-oriented texture is obtained for the samples deposited at a LEF of 1.55 J/(cm^2*pulse) and a high P_{O_2} of 200 mtorr, and, intriguingly, this film changes from ferroelectric phase into paraelectric phase. Besides, high remanent

polarizations (> 10 μC/cm^2) and low leakage currents (<1 μA/cm^2, at 100 kV/cm) can be obtained for the films deposited at proper conditions.

B.2 Introduction

There has been an upsurge of activities regarding the integration of ferroelectric devices with integrated circuit (IC) and microelectromechanical-system (MEMs). Thin ferroelectric films, with perovskite structure, have been attracting much attention for the applications on the nonvolatile random access memory (NVRAM) and the optical switch owing to their large spontaneous polarization and excellent optical properties [B.1-B.3]. High temperature (>500°C) deposition of the ferroelectric films, such as PTO, PZT, and SBT, is frequently applied to obtain good crystallinity of a perovskite structure [B.2, B.3], but the high temperature process damages the formerly fabricated transistor and the underlayer structures, especially at the deep submicron scale. In addition, the evaporation of PbO in lead-titanate-based thin films, processing at high temperature, always degrades the microstructure and reliabilities. Hence, a low temperature technique is indeed required for the deposition of ferroelectric film in IC and MEMs processes.

$PbTiO_3$ (PTO) film has been considered for the applications of NVRAM, but many drawbacks of this film must be improved, such as high coercive field, high crystallization temperature and poor microstructure. The $(Pb,Sr)TiO_3$ is consisted of the solid solutions: the PTO and the $SrTiO_3$ (STO). PTO and STO, at room temperature, behave a tetragonal structure (ferroelectric phase, Tc= 490°C) and a cubic structure

(paraelectric phase, Tc= -165°C), respectively. In addition, the effects of lead substituted by strontium (Sr) in the PTO film make the temperature of crystallization lower and offer a good control of the dielectric properties at room temperature [B.4]. In this work, the (Pb, Sr)TiO_3 (PSrT) films are prepared using the pulsed-laser deposition (PLD), which is excellent for fabricating the ceramic films with complex compounds. In addition, the technique of the pulsed-laser deposition (PLD) is simple, versatile, and capable for growing a wide variety of stoichiometric oxide films without subsequent high temperature annealing. Hence, PLD is a potential technique, which could be integrated into low temperature semiconductor processing.

Pulsed laser deposition process consists of three steps [B.5]: (1) vaporization of a target material by laser beam, (2) transport and interaction of a vapor plume with a background ambient, and (3) condensation of the ablated material onto a substrate where a thin film nucleates and grows. Thus, the structural and the electric characteristics of the PLD-ferroelectric films are strongly affected by the processing parameters, such as laser energy fluence and oxygen ambience. PSrT film using the oxide-electrode, such as (La, Sr)CoO_3, (La, Sr)MnO_3, or RuO_2, can obtain a good crystallinity and well controlled preferred-orientations at high deposition temperatures (>500°C), as reported in previous works [B.6, B.7], but the drawbacks of the PSrT capacitor using the oxide-electrodes are high power consumption and large delay time for the device applications. Thus, the noble metal Pt, with low resistvity, is considered as the electrode of PSrT capacitor because of its low power consumption and RC-delay-time [B.8]. However, very few works reported the properties of PLD-PSrT prepared on Pt/SiO_2 substrate at low temperature [B.6-B.8].

In this article, the effects of processing parameters on the structural and electric characteristics of PLD-PSrT films are presented. In general, the optical and the dielectric characteristics are strongly influenced by the textures of preferred orientations [B.1]. Thus, the relationships between the textures and the processing parameters of the PLD-PSrT films are also investigated.

B.3 Experimental

P-type silicon wafer with (100) orientation was employed as the substrate material in this study. A 100 nm SiO_2 was grown after the initial RCA cleaning process. Platinum film of 100 nm thickness was sputtered onto SiO_2 as bottom electrode. The annealing condition for Pt bottom electrode was 450°C for 30 min in N_2 ambient.

Thin PSrT films (220 nm thick) were deposited onto $Pt/SiO_2/Si$ substrate with a pulsed laser deposition system (Lambda Physik Excimer Laser LPX 200i, KrF, λ=248 nm). A set of optical lens was used to focus the excimer laser beam over the $Pb_{0.6}Sr_{0.4}TiO_3$ target in the vaccum. The PSrT target was prepared with conventional ceramic fabrication process [B.6]. The vaccum chamber was pumped down to maintain a base pressure of 1 mtorr. The vaporized species of the target transferred and deposited on the substrate heated at 400°C. The substrate temperature (400°C), denoted in this paper, was calibrated at the wafer-back side, and the temperature at the upper surface of the wafer is about 300°C. The laser pulsed rate was 5 Hz, and the target to substrate distance was 4 cm. Films were grown with a laser energy fluence varied from 1.02 to 1.70 J/(cm^2*pulse) and the oxygen partial pressure (P_{O_2}) from 75 to 200 mtorr. After

the deposition of PSrT films, in-situ annealing was carried out at 400 ^{o}C for 10 min with an oxygen pressure of 600 torr. Pt top electrodes, with a thickness of 100nm and a diameter ranging from 150 to 350 nm, were then deposited by sputtering and patterned by shadow mask process to form an metal/ferroelectric/metal (MFM) capacitor structure.

The film thickness of PSrT film was checked by both n&k analyzer (n & k analyzer 1200, n & k technology Inc.) and field emission scanning electron microscopy (FESEM) (S-4000, Hitachi Co., Japan). The microstructure of the samples was also examined by FESEM. An X-ray diffractometer (D5000, Siemens Co.) was employed to analyze the crystallinity, structure and grain sizes of the films. Atomic force microscope (AFM) (DI Nano-Scope III, Digital Instruments Co.) was used to inspect the surface morphology. An automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (HP4156, Hewlett Packard Co.) and a probe station was used to measure the leakage current. The tangent loss were measured by an impedance/gain-phase analyzer (HP 4194A, Hewlett Packard Co.)

A C-V analyzer (Package 82 system C-V 590, Keithley Co.) was used to measure C-V curves at 100 kHz, and the dielectric constant was extracted from C-V measurement and film thickness by using the equation $C = \varepsilon_0 \varepsilon_r A/d$. The ferroelectric polarization-electric field (P-E) characteristics of the PSrT films were determined directly from Virtual Ground circuits (RT-66A standardized ferroelectric testing system, Radiant Inc.) The pulse with a triangle-shaped wave at 10 kHz trains was used to measure the polarization. The P-E curve was obtained analytically by calculating the polarization P from the ε_r versus E data using the following equation

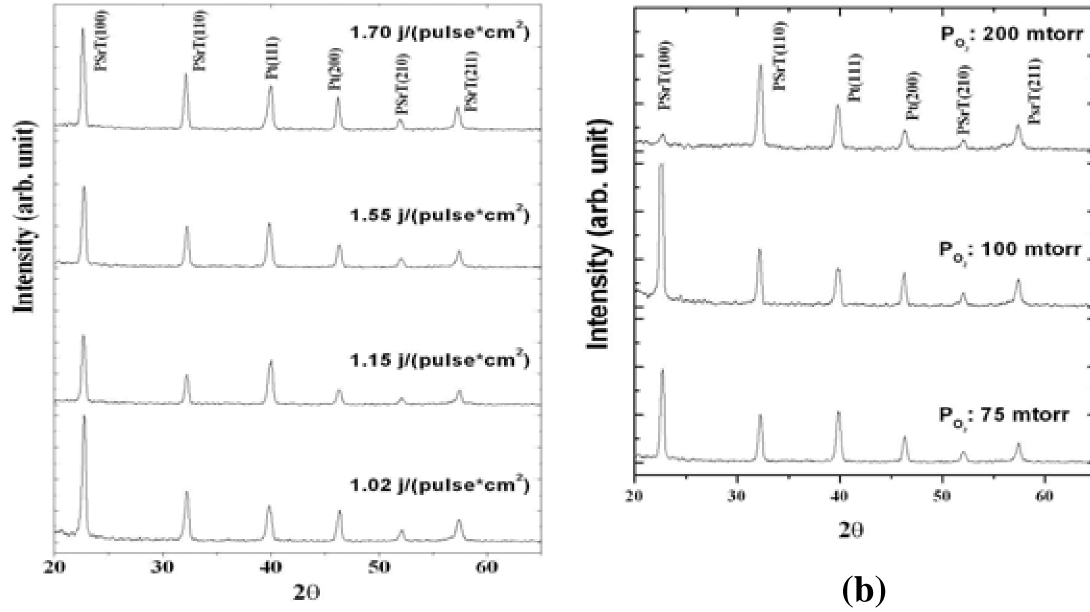


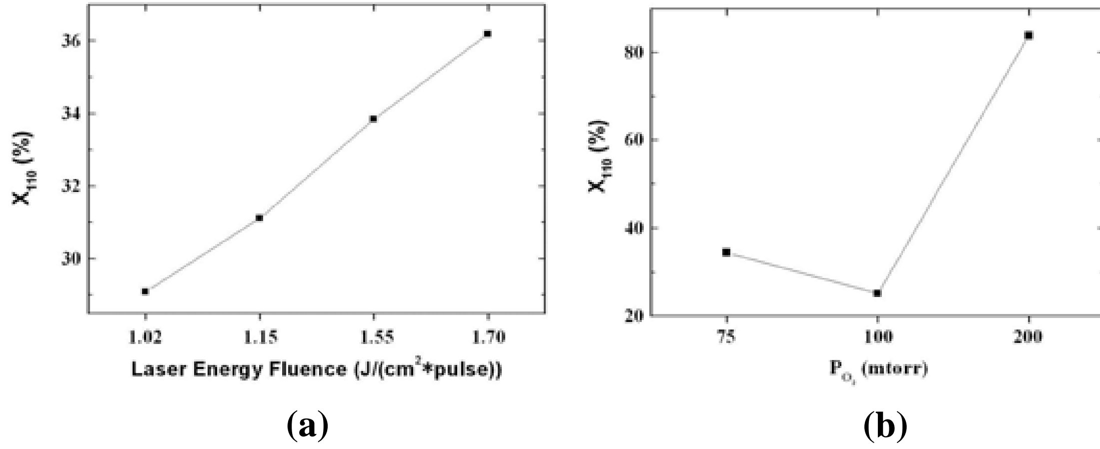
Figure B-1 XRD patterns of PSrT films deposited onto Pt/SiO_2/Si substrates (a) at various laser energy fluence, and (b) at various P_{O2}.

$P = \varepsilon_0 \times \int (\varepsilon_r - 1) dE,$

where ε_r is obtained from C-V relations.

B.4 Results and Discussion

PLD of PSrT films were carried out by various deposition conditions such as laser energy fluence (LEF) and the oxygen partial pressure (P_{O_2}) at low substrate temperature (400°C). Figure B-1 reveals that the polycrystalline films of perovskite PSrT deposited onto Pt/SiO2/Si substrate are formed. Fig. B-1(a) gives X-ray diffraction (XRD) patterns of PSrT films deposited at various laser energy fluence (1.02~1.70 J/(cm^2*pulse)) and fixed P_{O_2} 75 mtorr. Fig. B-1 (b) shows XRD patterns of



(a) **(b)**

Figure B-2 The fractional intensity of (110) orientated texture for the PSrT films deposited at (a) various LEF and P_{O2} 75 mtorr, and at (b) various P_{O2} and 1.55 J/(cm^2*pulse).

PSrT/Pt/SiO_2 multi-films deposited at various P_{O_2}.

The XRD intensity shows no significant differences for various laser energy fluence, but the large variations of the (100) and (110) textures are deduced from the XRD intensities. The percentage of a preferred-oriented texture in a film is calculated based upon the XRD diffraction pattern of the film as the following formulas [B.7]:

$$X_{hkl} = I^o_{hkl}/(I^o_{m00} + I^o_{110} + I^o_{111} + ...) \quad (B\text{-}1)$$

$$I^o_{hkl} = (I^o_{hkl})_{films}/(I^o_{hkl})_{ceramics} \quad (B\text{-}2)$$

$$I^o_{m00} = (I^o_{100} + I^o_{200} + ... + I^o_{111})/n \quad (B\text{-}3)$$

Where X_{hkl} and I^o_{hkl} represent the fractional intensity of (hkl) orientation and the peak intensity at (hkl) orientation. Figure B-2 is X_{110} as a function of laser energy fluence (LEF) and oxygen partial pressure (P_{O_2}). A linear relationship is observed in the X_{110} vs. LEF plot, as denoted in Fig B-2 (a), and thus the PSrT film deposited with higher LEF

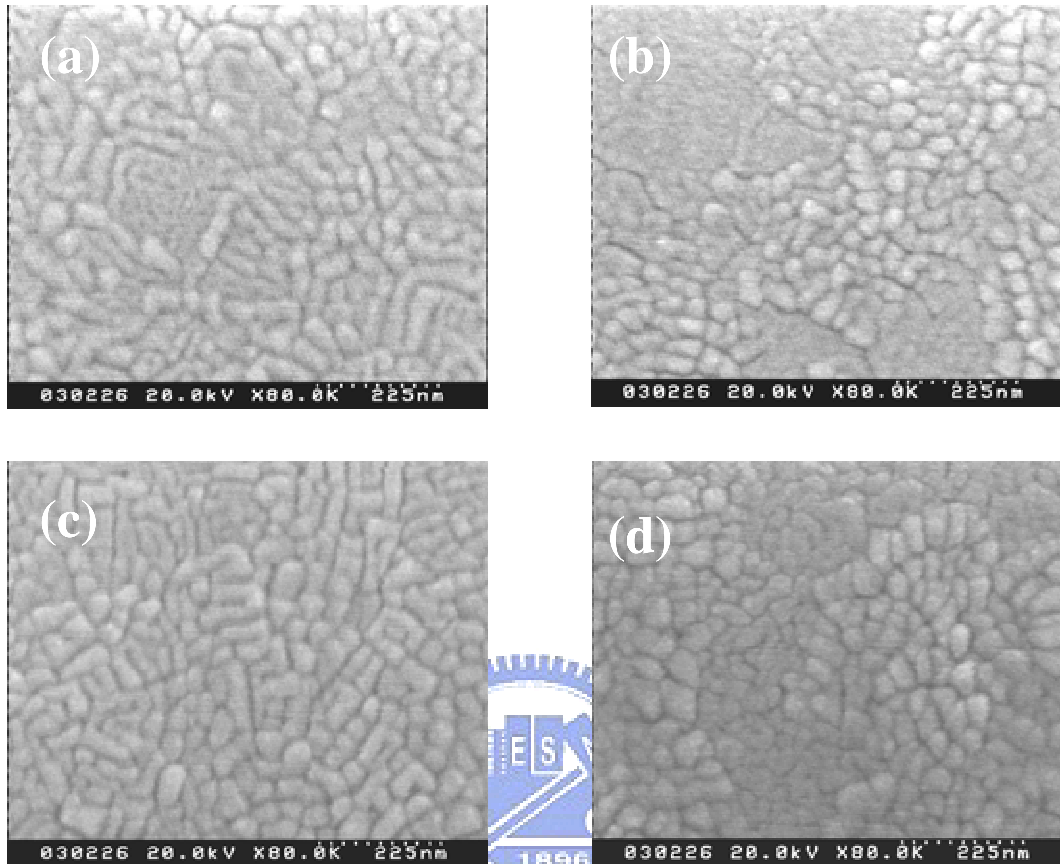
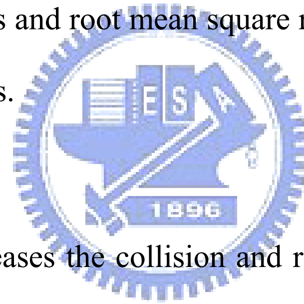


Figure B-3 Surface-morphology micrographs of FESEM for the PSrT films deposited at LEF of (a) 1.02, (b) 1.15, (c) 1.55 and (d) 1.70 J/(cm^2*pulse).

shows more (110) prefer-oriented structure. Besides, the oxygen partial pressure also plays an important role in PLD process, and it affects both of the kinetic energy of the plume and stoichiometry in the PLD deposition. Fig. B-2 (b) shows that X_{110} of PLD-PSrT film has a minimum value (25%) at P_{O_2} of 100 mtorr, and that of the BST film is as high as 84% at P_{O_2} of 200 mtorr. The PSrT films deposited at much higher P_{O_2} (200 mtorr) exhibits very intense (110) preferred-oriented texture, and one possible reason to explain this phenomenon is the growth dynamics of the PLD plume. Because

Process Parameter		FWHM (rad)	Grain size (nm)	R_{RMS} (nm)
laser energy fluence $(J/(cm^2 \cdot pulse))$	PO_2 (mtorr)			
1.02	**75**	$\mathbf{6.46 \times 10^{-03}}$	**21.80**	**5.3**
1.15	**75**	$\mathbf{6.07 \times 10^{-03}}$	**23.18**	**4.9**
1.55	**75**	$\mathbf{6.14 \times 10^{-03}}$	**22.92**	**6.2**
1.70	**75**	$\mathbf{6.06 \times 10^{-03}}$	**23.25**	**6.6**
1.55	**100**	$\mathbf{5.95 \times 10^{-03}}$	**23.66**	**6.5**
1.70	**200**	$\mathbf{7.16 \times 10^{-03}}$	**19.68**	**5.1**

Table B-1 FWHM, grain sizes and root mean square roughness (R_{RMS}) of PSrT films prepared in various conditions.



the high oxygen pressure increases the collision and reduces the mean free path of the interaction species, the kinetic energy of deposited species, PSrT flakes, is reduced at high oxygen pressure ambient [B.10]. The (110) texture of PSrT films can be easily formed at low energy [B.7, B.11], and thus the enhanced (110) texture is observed for the PSrT films deposited at a high P_{O_2} (200 mtorr).

The surface morphology and cross-sectional micrographs of the PSrT films are exhibited in Figs. B-3 and B-4. The PSrT films exhibit typical columnar structure, and no apparent difference in the grain size of PSrT film is observed. The grain sizes of PSrT films are also confirmed from the Full Width at Half-Maximum (FWHM) of the XRD patterns, using the Scherrer formula (grain size <100nm):

$$D = 0.89 \lambda / (B \times \cos\theta) \qquad \text{(B-4)}$$

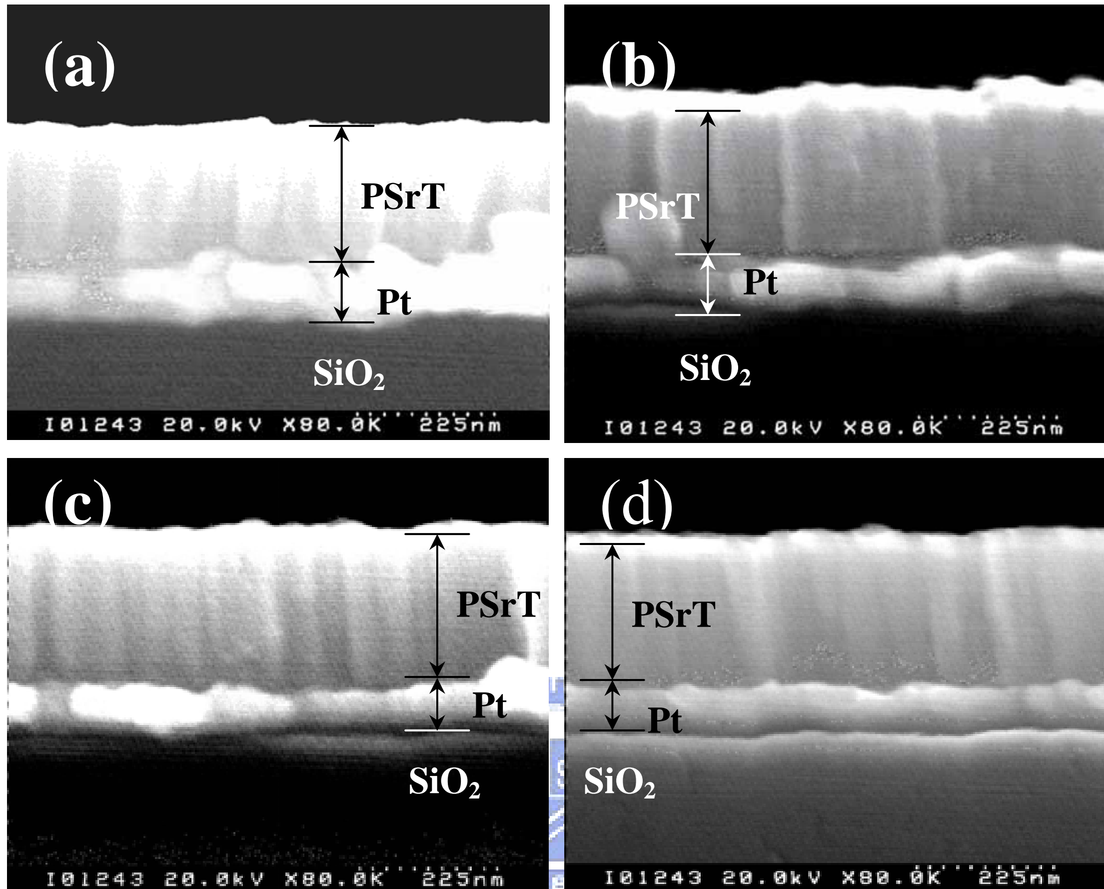


Figure B-4 Cross-sectional micrograph of PSrT/Pt/SiO_2 deposited at LEF of (a) 1.02, (b)1.15, (c)1.55 and (d) 1.70 J/(cm^2*pulse).

where D is the mean grain size; λ is the X-ray wavelength (~0.154nm); B is the FWHM of the XRD peak, and θ is the diffraction angle [B.12]. The FWHM of the (110) peak is employed to calculate grain sizes, and the results are shown in Table B-1. Also seen in Table B-1 are the surface roughness (R_{RMS}) of PSrT films. No correlation is found among the grain size, surface roughness and the deposition parameters.

Figure B-5 gives the polarization-electric field (P-E) hysteresis loops of PSrT films fabricated at various laser energy fluences and P_{O_2}. At a fixed oxygen ambient (P_{O_2}: 75

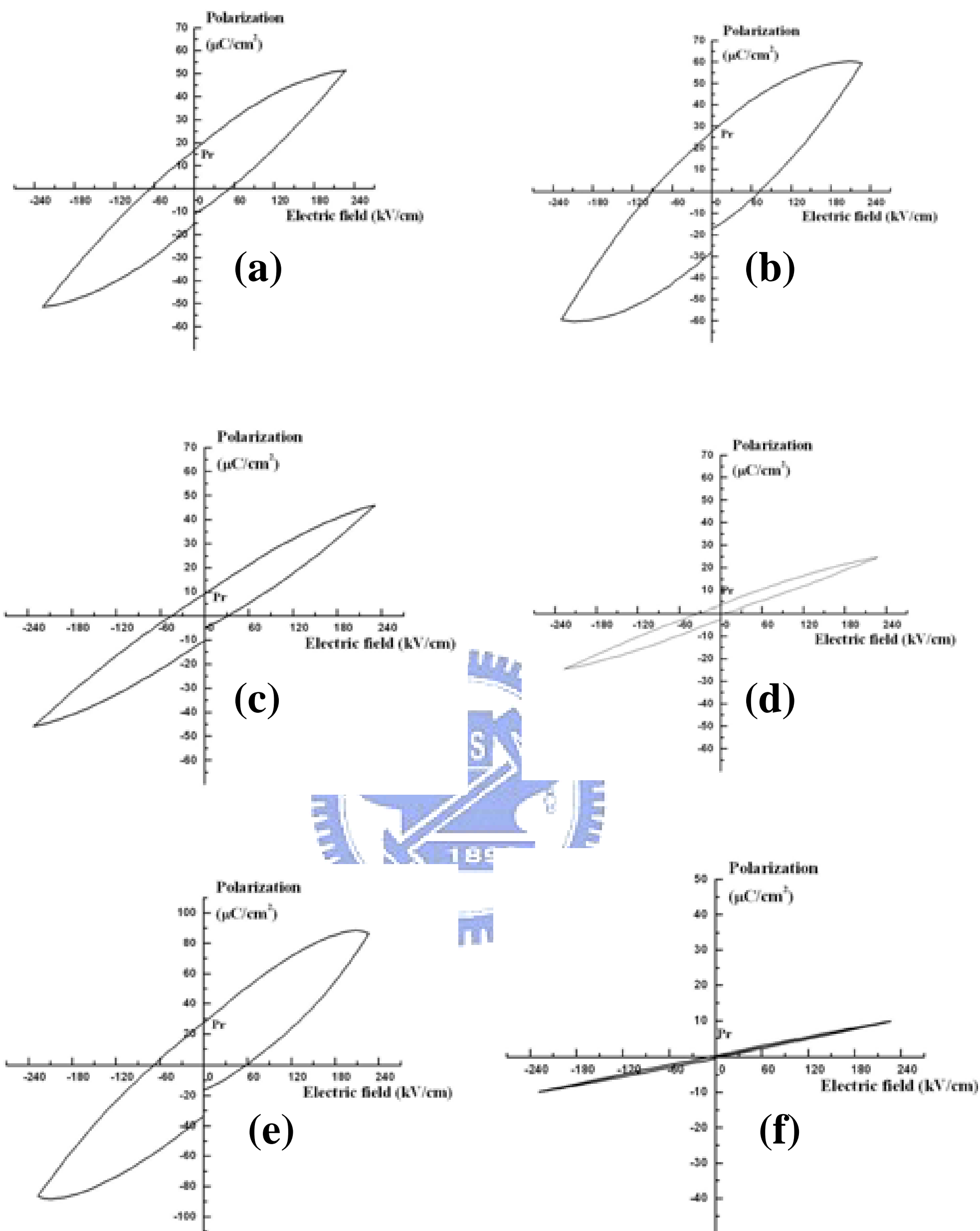


Figure B-5 P-E hysteresis loops of PSrT films fabricated at LEF of (a) 1.02, (b) 1.15, (c) 1.55 and 1.55 (d) 1.70 J/(cm^2*pulse) and fixed P_{O2} 75 mtorr, and at P_{O2} of (e) 100 mtorr, (f) 200 mtorr and fixed 1.55 J/(cm^2*pulse).

mtorr), both remanent polarization (Pr) and saturation polarization (Ps) decrease as laser energy fluence increase, as indicated in Fig. B-5 (a), (c) and (d). In general, the

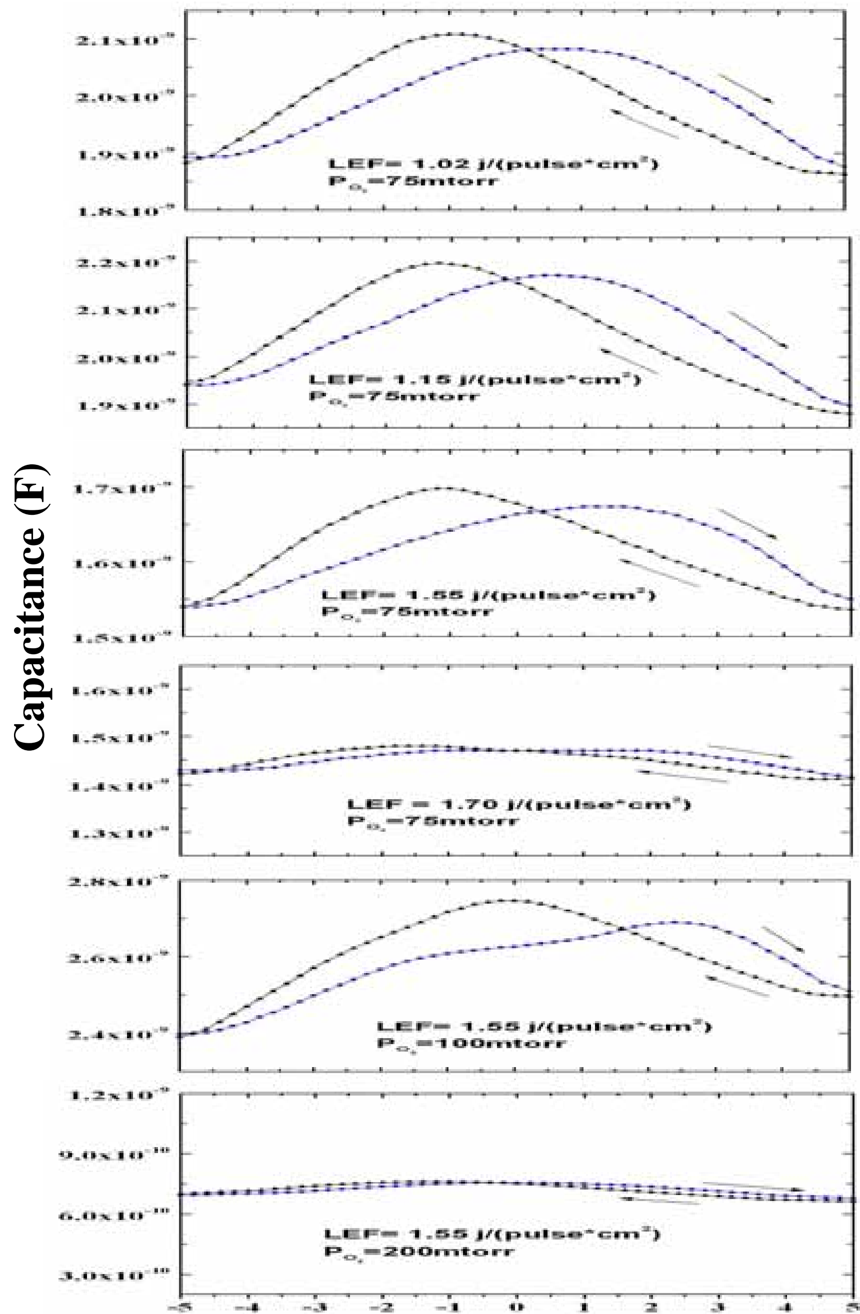


Figure B-6 Capacitance versus applied voltage for PSrT films deposited at various LEF and P_{O2} (→ -5V to +5V, ← +5V to –5V).

polarization and dielectric constant of ferroelectric films are affected by many factors, such as grains, crystallinity textures, and compositions of the films. As mentioned above,

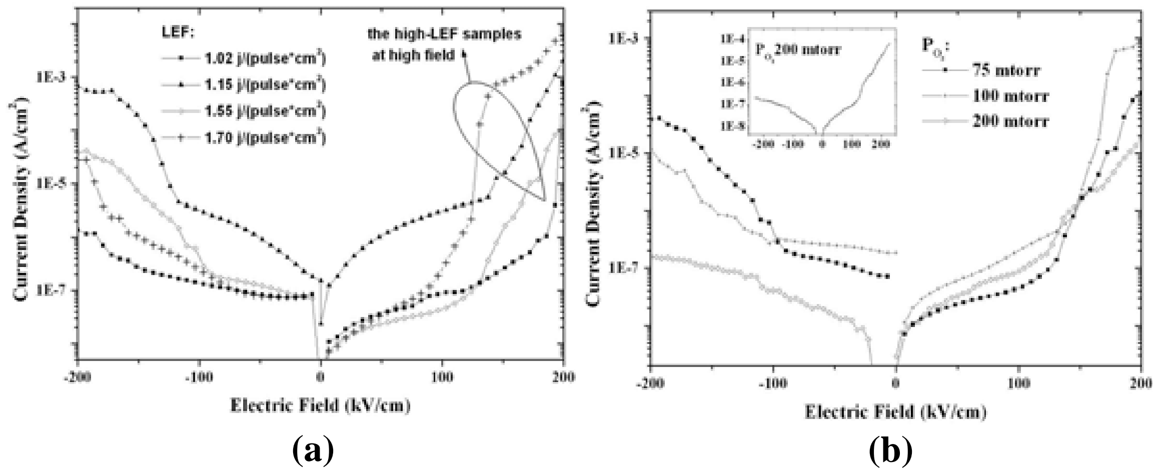
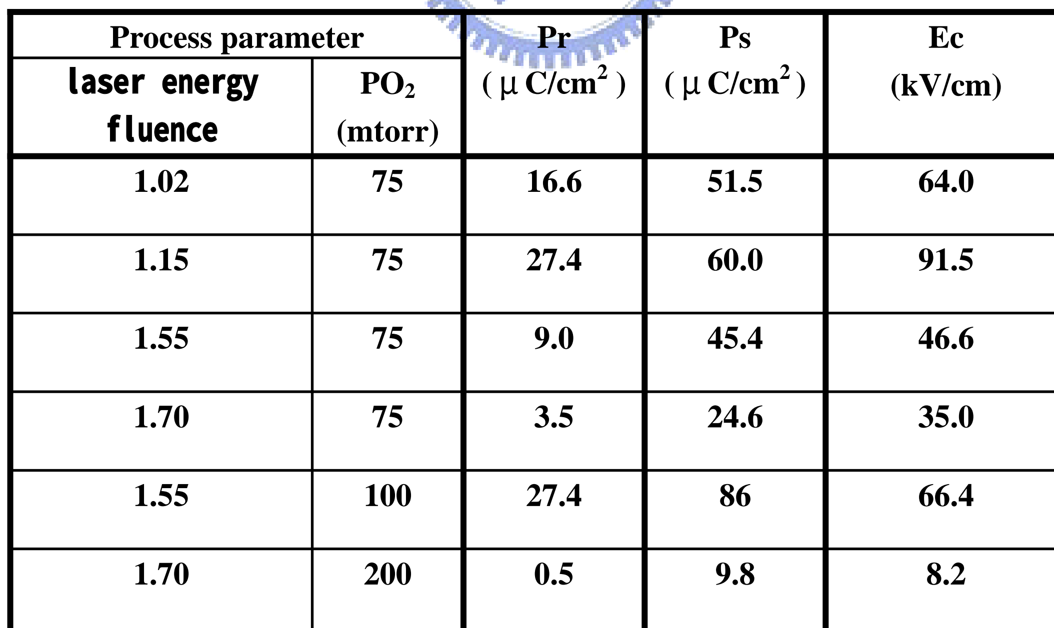


Figure B-7 Leakage current density versus applied electric field for PSrT films deposited at various (a) LEF and (b) P_{O2}

the grains and the crystallinity of the PSrT films are independent with the processing parameters, so the textures and the compositions of the films become important issues in this study. The PbO volatilizes easily when the incident laser beam thermally interacts with the PSrT target, and the Pb content within the PSrT film will be reduced as laser energy fluence increases. The reduced Pb content results in less tetragonal structure, as reported in other works [B.3, B.9]. Films deposited with higher LEF exhibit less tetragonal structure (ferroelectric phase), so the polarizations of the films reduce as ferroelectric phase decreases. Besides, the dielectric constant and polarization of the lead-titanate-based crystal behave the maxima in [100] direction, so the polarizations of the films with enhanced (110) texture are smaller than those with preferred (100) texture [11,13]. Hence, PSrT films deposited at higher LEF exhibit less ferroelectric phase and higher (110) texture, both of which reflect the decrease of the polarization. Large leakage current affects the P-E curve measured by virtual ground circuit, so the intrinsic polarization in the leaky film is smaller than that of measured

polarization [B.15, B.16]. PSrT film deposited at 1.15 J/(cm^2*pulse) and 75 mtorr shows large polarization, but, however, the rounded shape of P-E curve implies that the film is very leaky when biased over 150 kV/cm. PSrT film deposited at 200 mtorr, shown in Fig. B-5(f), is paraelectric property as a result of cubic structure and small grain sizes. Table B-2 summarizes the remanent polarization (Pr), coercive field (Ec) and saturation polarization (Ps) of films prepared in various conditions.

The plots of small signal capacitance C versus bias voltage V, shown in Fig. B-6, show butterfly-liked curves corresponding to the hysteresis loops given in Fig. B-5. The film deposited at 1.55 J/(cm^2*pulse) and 200 mtorr, also shows the corresponding paraelectric property as seen in Fig B-5(f). The slight asymmetry of these curves is attributed to the different annealing conditions for the bottom and top electrodes. The



Process parameter		Pr	Ps	Ec
laser energy fluence	PO_2 (mtorr)	(μC/cm^2)	(μC/cm^2)	(kV/cm)
1.02	75	16.6	51.5	64.0
1.15	75	27.4	60.0	91.5
1.55	75	9.0	45.4	46.6
1.70	75	3.5	24.6	35.0
1.55	100	27.4	86	66.4
1.70	200	0.5	9.8	8.2

Table B-2 Remanent polarization (Pr), saturation polarization (Ps) and coercive field (Ec) of PSrT films prepared in various conditions.

capacitance peaks on both sides of the abscissa (dc bias) suggest ferroelectrc domain switching in the films. Previous works also reported the asymmetric peak capacitance behaviors resulted from the asymmetric nature of the electrodes [B.17, B.18].

The current-voltage characteristics of Pt/PSrT/Pt capacitors with various PLD conditions are given in Fig. B-7. The leakage current of metal/ferroelectric/metal (MFM) capacitors is affected by many factors, such as the oxygen stoichiometry in the films, interface stress and the grain boundary [B.19]. The oxygen stoichiometries of the PSrT films are different for the films prepared in different PLD conditions, according to the following reaction:

$$O_o \leftrightarrow V_o^{++} + 2\,e^- + 1/2\,O_2 \qquad (B\text{-}5)$$

where O_o ,V_o^{++} and e^- represent the oxygen ion on its normal site, the oxygen vacancy and the electron, respectively. More oxygen vacancies yield a larger leakage current, causing a PSrT film form to act as an n-type semiconductor [B.20, B.21]. The leakage

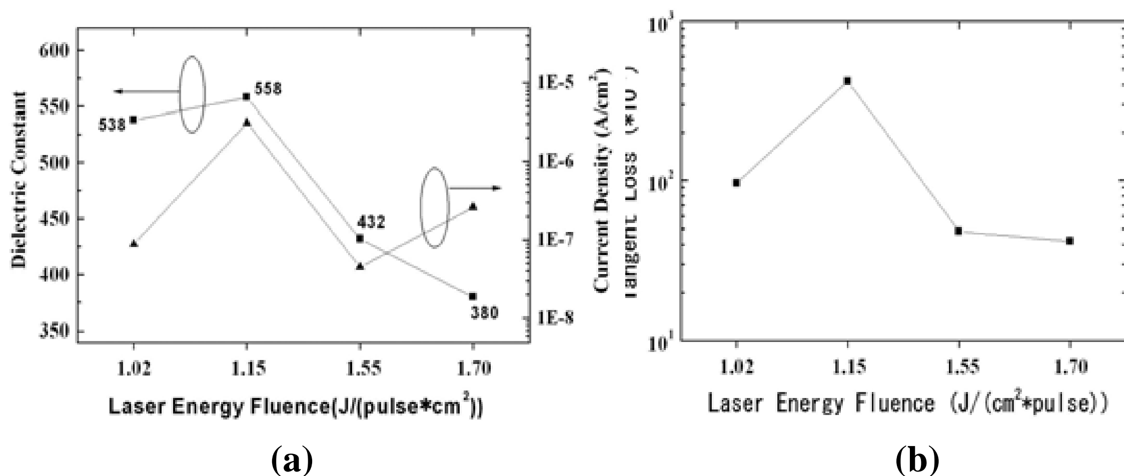
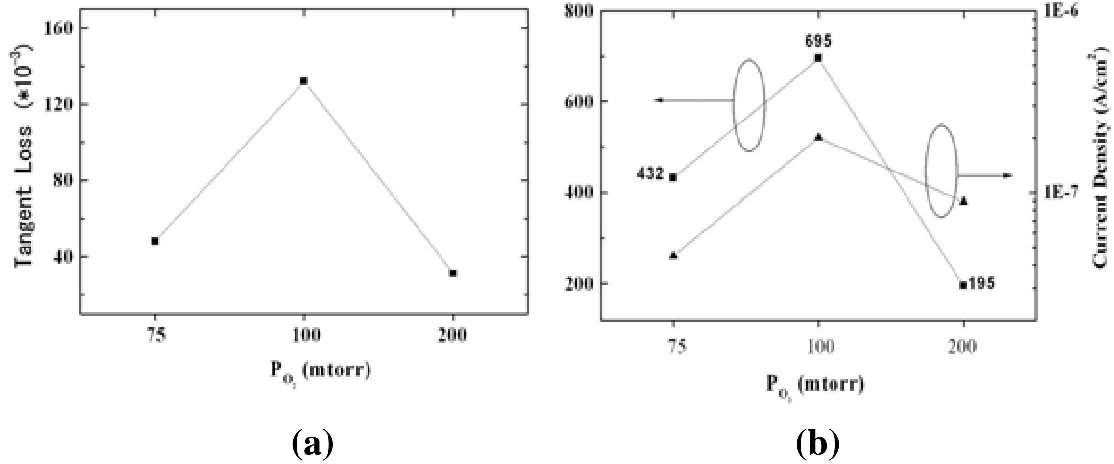


Figure B-8 (a) the dielectric constant and leakage current density (at 100 kV/cm), and (b) the tangent loss for the PSrT films deposited at various LEF.

currents of PSrT films biased at 100kV/cm are smaller than 5 μA/cm^2, but those of the films biased over 150 kV/cm dramatically increase for the films deposited with higher LEF, as indicated in Fig B-7(a). That is, higher LEF will generate larger PbO during PLD process to form oxygen vacancies and trap states in the PSrT film, so the high electric field can detrap many electrons from the trap sites to increase the carrier concentration. The leakage currents are smaller than 2×10^{-7} A/cm^2 at ＋100 kV/cm for the films prepared at 1.55 J/(**cm^2*pulse**), as indicated in Fig. B-7(b). The leakage current of PSrT capacitors biased at positive/negative voltage reveals stronger asymmetrical I-V plots, and this trend is more obvious for the films deposited at high P_{O_2}, as indicated in the inset of Fig. B-7(b). That is, the leakage current of Pt/PSrT/Pt capacitor prepared at 200 mtorr biased at a negative voltage is much smaller than that biased at a positive voltage, and the I-V profile is smoother than those of the others. Obviously, Schottky barrier is formed at the interface of top electrode to suppress the negative-biased current, because higher P_{O_2} ambient will compensate the oxygen vacancies and trapping states on the upper Pt/PSrT interface.

Figure B-8 depicts the effects of laser energy fluence on the dielectric constant, leakage current and tangent loss (*tanδ*) of PSrT films. The dielectric constant of PSrT films in this study ranges from 380 to 558, and the leakage currents are under 5 μA/cm^2 at 100 kV/cm. The dielectric constant is almost constant when LEF ≦ 1.15 J/(pulse*cm^2) and decreases as laser energy fluence increases when LEF>1.15 J/(pulse*cm^2) , as shown in Fig. B-8(a). D. H. Kang et. al. reported that the dielectric constant of the $Pb_{1-x}Sr_xTiO_3$ film decreases as the Pb content of the films reduces while x exceeds 0.4 [B.4, B.14]. As discussed above, the Pb content decreases as LEF



(a) **(b)**

Figure B-9 (a) the dielectric constant and leakage current density (at 100 kV/cm), and (b) the tangent loss of the PSrT films deposited at various P_{O2}.

increases, so the Sr content is larger than 0.4 for these films prepared by a $Pb_{0.6}Sr_{0.4}$ target. Hence, the dielectric constant decreases as LEF increases. Besides, the large leakage current for PSrT film deposited at 1.15 J/(cm^2*pulse) also confirms the round shape of P-E curve shown in Fig. B-5(b). On the other hand, in general, there are two mechanisms for the *tanδ* - resistive loss and relaxation loss [B.22]. In resistive loss case, energy is dissipated by mobile charges, and the tangent loss depends on the magnitude of leakage current; in relaxation loss case, energy is dissipated by relaxation of dipoles, and the tangent loss is proportional to the dielectric constant. Both mechanisms may occur in films prepared in this study, as shown in Fig. B-8(b) and Fig. B-9(b).

Figure B-9 shows the effects of P_{O_2} on the dielectric constant, leakage current and tangent loss of PSrT films. The leakage currents for all specimens studied are smaller than 1 μA/cm^2 at 100 kV/cm. The low dielectric constant (195) of PSrT films deposited at 200 mtorr is due to the phase changes from the ferroelectric phase into

Film Structure	PSrT(220 nm) $Pt/SiO_2/Si$	PSrT(400nm) $Pt/Ti_2/Si$	PSrT (150nm) $Pt/Ti/SiO_2/$	SBT(4500 nm) $Pt/SiO_2/Si$	PZT(150nm) Pt/Ti/Si [3, 24]
Deposition Method	**PLD (KrF**	**sol-gel**	**LSMCD**	**PLD**	**PLD**
Deposition Temperature	**400°C**	**700°C Annealing**	**400°C Baking +**	**750°C**	**500~650°C**
Remanent Polarization	**27.4**	**14**	**N/A**	**<10**	**30-40**
Dielectric	**558**	**1370**	**500**	**N/A**	**950**
Coercive Field	**91.5**	**65**	**N/A**	**70**	**40~65**
Current Density (A/cm2)	**$<4 \times 10^{-6}$**	**2×10^{-7}**	**$\sim 10^{-4}$**	**N/A**	**$10^{-4} \sim 10^{-5}$**
Residual Contamination	**no**	**yes**	**yes**	**no**	**no**
N/A: Not Analyzed					

Table B-3 Comparisons of dielectric characteristics for the ferroelectric films fabricated from different kinds of material and by various deposition techniques.

paraelectric phase at high P_{O_2} . Films deposited at 100 mtorr have the highest dielectric constant (695), and, however, they also have the largest leakage current and tangent loss.

Table B-3 summarizes the dielectric characteristics of potential ferroelectric films for memory applications. As shown in Table B-3, the processing temperature of PLD-PSrT is the lowest among the five. The PZT film has largest polarization and lower coercive field, but the deposition temperature is much higher than that of PSrT even using the same PLD technique. The polarization of PLD-SBT film is smaller than

those of other PLD films. The PLD-PSrT films prepared at low temperature (400°C) exhibit high polarization and low leakage current.

B.5 Conclusions

Low-temperature PLD-PSrT film deposited at 400°C has good crystallinity and excellent ferroelectric properties, hence, can be integrated into IC-compatible process. (110)-preferred-oriented texture in the PSrT films increases as laser energy fluence rises, and an enhanced (110)-preferred-oriented texture is for the PSrT films deposited at 1.55 J/(cm^2*pulse) and P_{O_2} 200 mtorr.

The remanent polarization and coercive field of PLD-PSrT films prepared with proper processing parameter are between 10~18 μC/cm^2 and 45~65 kV/cm. The dielectric constant of PSrT films, deposited at 1.55 J/(cm^2*pulse) and P_{O_2} of 100 mtorr, is 695. The electric characteristics of the PSrT films are significantly influenced by the textures and the stoichiometry. Polarization and dielectric constant of PLD-PSrT films decrease as laser energy fluence increases due to changes in the textures and the stoichiometry. In this work, all the PSrT films behave the ferroelectric phase except that prepared at 200 mtorr. The PSrT film deposited at 200 mtorr is a paraelectric phase, and the dielectric constant of the film is only 195, nevertheless, which is still much larger than that of SiO_2 (3.9).

The small leakage current, (<1 μA/cm^2 at 100kV/cm), can be achieved, and Schottky barrier is formed at the interface of top electrode to suppress the

negative-biased current by increasing P_{O_2}. Consequently, the texture control and the electric characteristics of the PSrT films can be adjusted by the processing parameters of PLD technique. PLD-PSrT films prepared with proper processing parameters emerges to be a promising candidate for the applications of NVRAM and MEMs.

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Appendix B

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Conference Papers

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