國立交通大學

材料科學與工程學系

碩士論文

中尺寸薄膜電晶體液晶顯示器因 COG 封裝所造成局部翹曲及應力對漏光現象之探討

Effects of Localized Warpage and Stress on Chip-on-Glass Packaging Induced Light Leakage Phenomenon in mid-size TFT-LCD

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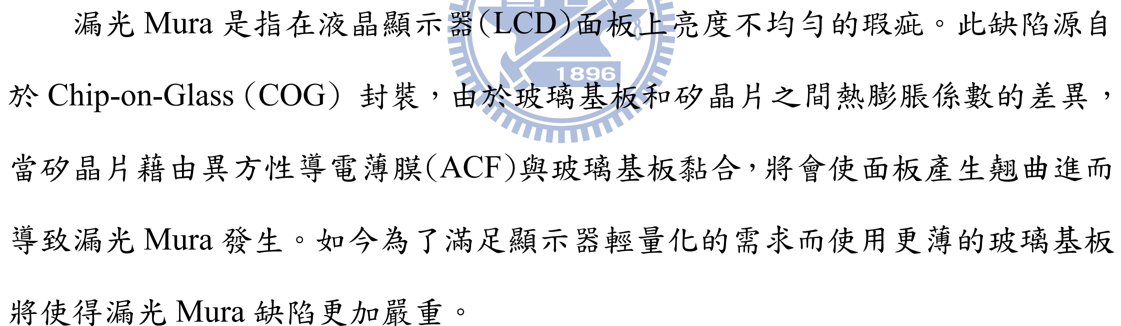
摘 要



漏光 Mura 是指在液晶顯示器(LCD)面板上亮度不均勻的瑕疵。此缺陷源自於 Chip-on-Glass（COG）封裝，由於玻璃基板和矽晶片之間熱膨脹係數的差異，當矽晶片藉由異方性導電薄膜(ACF)與玻璃基板黏合，將會使面板產生翹曲進而導致漏光 Mura 發生。如今為了滿足顯示器輕量化的需求而使用更薄的玻璃基板將使得漏光 Mura 缺陷更加嚴重。

本論文利用商用模擬軟體 ANSYS^{TM} 以有限元素分析法(FEA)建立一 3D 數值模型來計算 LCD 面板在經過 COG 封裝之後所產生的翹曲及應力，並研究其與漏光現象的相關性，進而探討 COG 封裝所引起之 Mura 缺陷的成因。接著研究製程溫度及 ACF 的材料性質還有矽晶片的尺寸大小及排列對 Mura 缺陷的影響。此外利用量測表面形貌儀器 KOSAKA ET4000A，藉由實際的實驗量測來驗證模擬的可靠度。

根據實驗及模擬計算的結果，發現了面板翹曲、應力分佈和漏光現象之間具有高度的相關性。根據分析結果探討可能造成漏光缺陷的根本原因，主要是由於

液晶分子的指向矢及在配向膜表面的分子鏈排列方向會被 COG 封裝所產生的應力所影響而造成。雖然 LCD 為了輕薄化而將玻璃基板厚度從 0.5 mm 降至 0.3 mm 時會產生漏光現象，但藉由將製程溫度由 180 ^{o}C 降至 160 ^{o}C 及採用低楊氏模數的 ACF 可以將漏光缺陷有效改善或消除。最後本論文提出其它改善漏光現象的方法，例如使用薄化的矽晶片、縮減矽晶片的長度或填充材料(dummification)等方式，並且利用數值模擬來計算其改善漏光的效率。這些方法不僅具有低本成及高可行性的優勢，從模擬計算結果來看還可以有效解決 Mura 漏光缺陷。

Effects of Localized Warpage and Stress on Chip-on-Glass Packaging Induced Light Leakage Phenomenon in mid-size TFT-LCD

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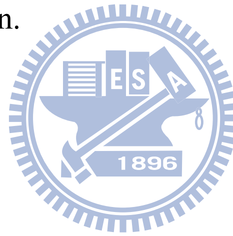
Abstract

Light leakage Mura *i.e.* the non-uniform brightness in LCDs, occurred upon the completion of chip-on-glass (COG) packaging of silicon IC drivers through the thermal bonding of anisotropic conducting film (ACF) resulting from the coefficient of thermal expansion (CTE) mismatch between glass substrate and silicon chips. Mura defect deteriorated as thinner glass plates were introduced to meet market demand for light weight and high mobility in mid-size TFT-LCD.

In this study, a 3-D finite element analysis (FEA) model using ANSYSTM was first established to examine the warpage and stress behavior of the glass substrate in order to explore their correlation with light leakage phenomenon. In addition, the simulated warpage data were validated by surface contour measurement tool using surface profiler, KOSAKA ET4000A. Specifically, the root-causes of Mura defect induced by COG package were examined and proposed. Then, the impact of thermal bonding temperature and thermo mechanical properties of ACF on Mura defect was investigated. In addition, the effects of dimension and layout of Si chips were also explored.

Based on experimental data and numerical analysis, a strong relationship among light leakage defect, warpage and stress behavior has been established. Besides, the root-causes of light leakage phenomenon were proposed. The Mura may result from the re-orientation of the director of the liquid crystal molecules and/or the orientation of the polymer chains on the alignment layer surface induced by the non-uniform stress resulting from COG packaging. Although the light leakage Mura appeared when the thickness of glass substrate was decreased from 0.5 mm to 0.3 mm, reducing ACF thermal bonding temperature from 180 to 160 ^{o}C or reducing ACF modulus can effectively eliminate Mura defect. Numerical modeling was also utilized to analyze the effectiveness of the dimension and layout of Si chips on Mura improvement. A low cost and effective solution can be achieved through thin silicon die, shorter die in length or the use of dummification.



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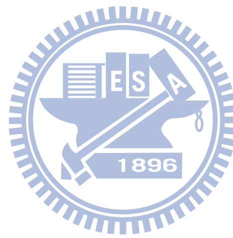

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Chapter 1 Introduction

1.1 Background

Thin film transistor liquid crystal displays (TFT-LCDs) have been widely used in TVs and monitors for computes, notebooks and hand-held devices. As the demand of LCD package moving towards ultra-thin package, chip-on-glass (COG) package offers the benefits of low-cost, high packaging density, and high pitch precision compared to the conventional package. In the processes of COG package, however, IC drivers are directly mounted on the glass substrate through anisotropic conductive film (ACF) attachment by thermal bonding, in which the mismatch of thermal expansion coefficient (CTE) between the Si chip and glass may induce large stress resulting in warpage as illustrated in Figure 1.1 and/or delamination [1,2]. Thus, the reliability and thermo-mechanical integrity of multilayered structure such as glass/liquid crystal/glass or Si/ACF/glass are the major concerns for COG packaging.

In the notebook market, the trend is moving towards large screen (larger than 10 inches) with ultra-thin and light-weight glass substrate. When the thickness of glass substrate was reduced from 0.5 mm to 0.3 mm and the panel size was increased from 10 to 13.3 inches, Mura defect involving non-uniform brightness in LCD, became severe for a 13.3” TFT-LCD with COG package using 8 IC drivers as shown in Figure 1.2. The light leakage phenomenon appeared only at the edge of LCD panel in half-moon-like shape. In addition, the region of light leakage was related to the IC drivers’ arrangement, appeared between Si chips. These practical observations showed the light leakage had highly relationship with the COG packaging.

The high temperature gradient during the ACF bonding process was reported to cause the warpage of glass substrate due to the CTE mismatch between glass substrate

and silicon-based chips [3,4]. Recently, Tsai *et al.* investigated the effects of the parameters such as thermal and moisture expansion of the ACF, and its elastic modulus and fillets on the warpage of ACF-bonded COG packages using a test structure (30x20x0.7 mm) [5]. It suggested that warpage of the COG package can be reduced by thermal cycling up to 85 ^{o}C and precisely controlling small CTE mismatch between chip and glass substrate, while insensitive to the bonding temperature. Chen *et al* reported that the light leakage was related to the thermal gradient and nonuniform stress distribution [6,7]. Nevertheless, the root-cause of the light leakage phenomenon in mid-size TFT-LCD panel caused by COG package has not been clearly addressed yet.

In this study, a 3-D finite element analysis (FEA) model was first established by ANSYS^{TM} to examine the relationships among warpage, stress distribution and light leakage phenomenon in order to identify the root-cause of light leakage Mura. Furthermore, the analysis model was also used to explore the influence of various parameters of COG packaging such as thickness of glass substrate, bonding temperature, CTE and modulus of ACF on warpage and stress distribution in LCD panel. Finally, the impact of the layout and dimension of Si chips was analyzed by numerical modeling to explore possible low-cost solutions in eliminating Mura defect.

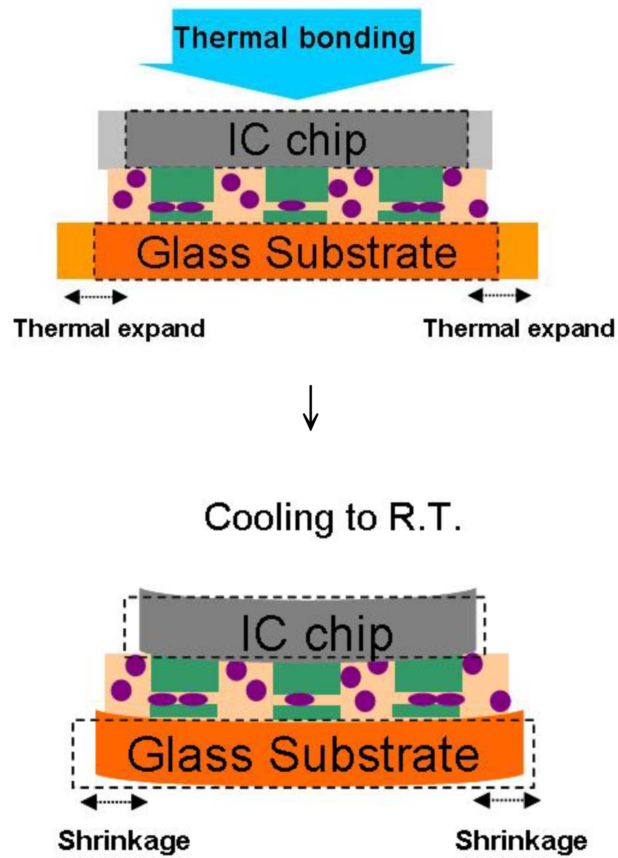

Figure 1.1 Schematic illustration of warpage induced after ACF thermal bonding

Figure 1.2 Light leakage Mura in TFT-LCD

1.2 Overview

The contents of this thesis were organized as following. In chapter 2, the background of LCD, COG package, ACF adhesive and Mura defect were first introduced. In chapter 3, the finite element analysis and experimental validation were described in detail. A 3-D finite element analysis (FEA) model coupled with transient thermal analysis using ANSYS^{TM} was established. Next, in chapter 4, the results were studied to examine the warpage and stress behavior in COG package in order to explore the correlation with light leakage phenomenon. The root-causes of the light leakage phenomenon were related to the liquid crystal molecules and alignment layer. Furthermore, the effects of ACF bonding temperatures, thickness of glass substrate and material properties of ACF on light leakage Mura were studied. As a result, ACF bonding temperature was the most important parameter to recover the light leakage Mura which appeared when thickness of glass substrate decreased. The numerical models were also utilized to analysis and predict the effectiveness of solutions for improving light leakage phenomenon such as dimensions of Si chips and dummification. According to the results, shrinkage of height/length of Si chips and dummification can effectively eliminate light leakage Mura. Finally, conclusions were given in chapter 5 to summarize this work.

Chapter 2 Literature Review

2.1 Thin Film Transistor Liquid Crystal Display (TFT-LCD)

In order to respond the demands for light-weight, small volume and portability in flat panel displays, the liquid crystal display (LCD) was invented to replace the cathode ray tube (CRT) monitors. Thin film transistor liquid crystal display was a variant of liquid crystal displays which used thin film transistor technology to improve image performance such as brightness, contrast and low power consumption [8]. Nowadays, LCDs are widely used in television sets, computer monitors, notebooks, hand-held devices and personal digital assistants. The market of LCDs had increased tremendously in the recent years. [9]

2.1.1 TFT-LCD Structure

TFT-LCD had a sandwich-like structure with liquid crystal filled between two glass substrates as Figure 2.1 shown. [10]

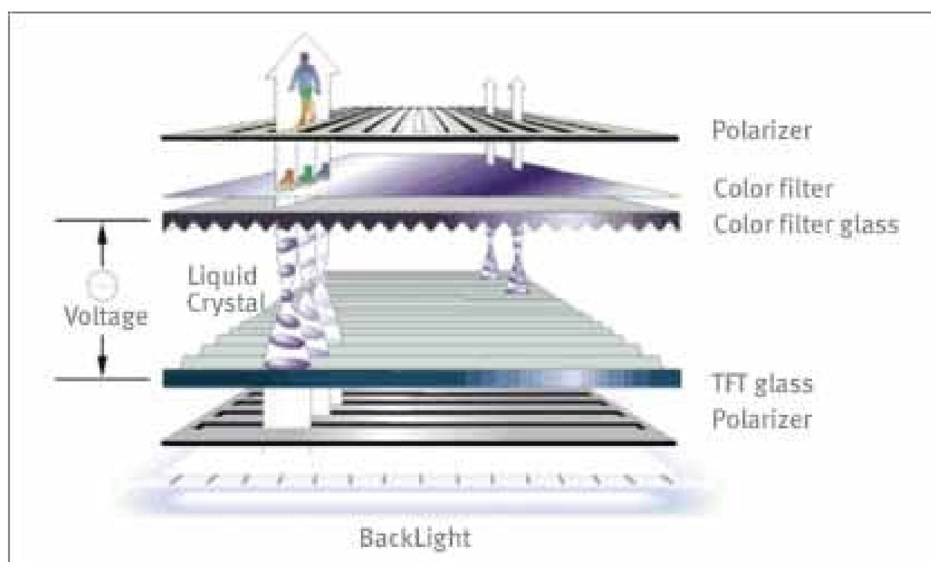

Figure 2.1 Schematic illustration of LCD assembly [10]

The TFT-LCD mainly consisted of two parts, backlight system and cell. The backlight system was the light source of the LCD panel. The major components of backlight were an acrylic light pipe, the lamp usually placed at the end of the light pipe and the optical film and reflective film as shown in Figure 2.2. [11] Generally, these units of backlight were consisted to perform a uniform light. The cell part was mainly consisted of a TFT glass, a color filter glass, two polarizers attached to the glass substrate, liquid crystal and spacers filled between the two glass substrates as shown in Figure 2.3. [10]

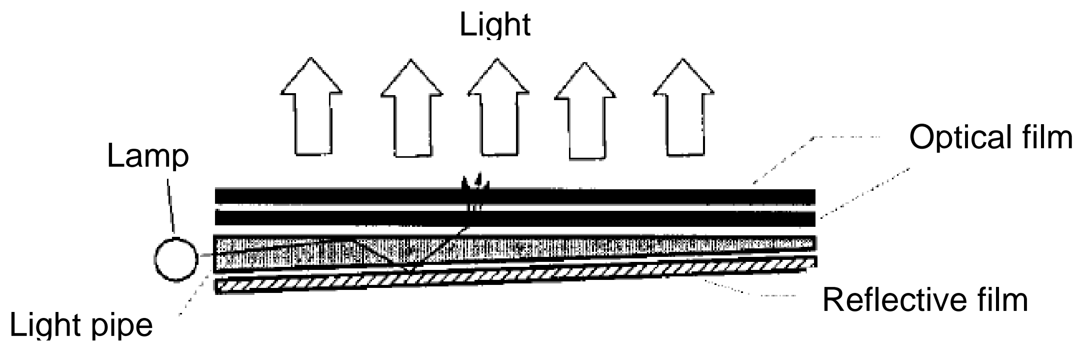

Figure 2.2 Cross-section view of schematic illustration of backlight [11]

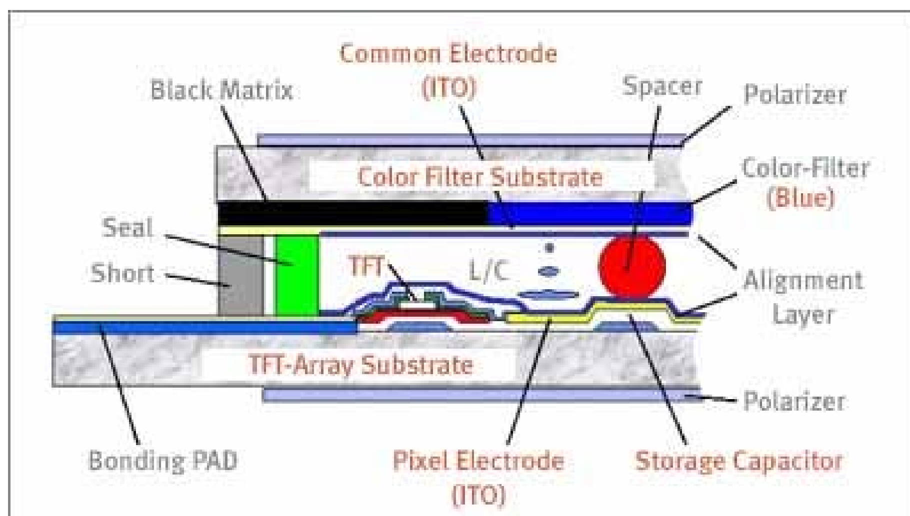

Figure 2.3 Cross-section view of schematic illustration of cell structure [10]

TFT-LCD was composed of complicate materials. The key parts were briefly described in the following:

1. TFT-array substrate:

TFT substrate was composed of millions TFT devices which was arranged as a matrix on an ITO substrate (Indium Tin Oxide, a transparent and electrical conductive material). Figure 2.4 showed a schematic illustration of a TFT pixel unit [12]. TFT manufacturing processes were similar to the lithography in semiconductor industry. The difference was that the TFT grown on a glass substrate, instead of silicon wafer. TFT was just like a switch which controlled the quantity of electrons into the capacitor. When enough electrons flowed into capacitor, the TFT device was shut down and the electrons kept in the capacitor. Therefore, TFT device can determine the strength of electrical field and then affect the orientation of the liquid crystal molecules. Each TFT pixel was operated independent, so that the bright or dark in each pixel can be controlled. Thus, the image can be shown on the screen.

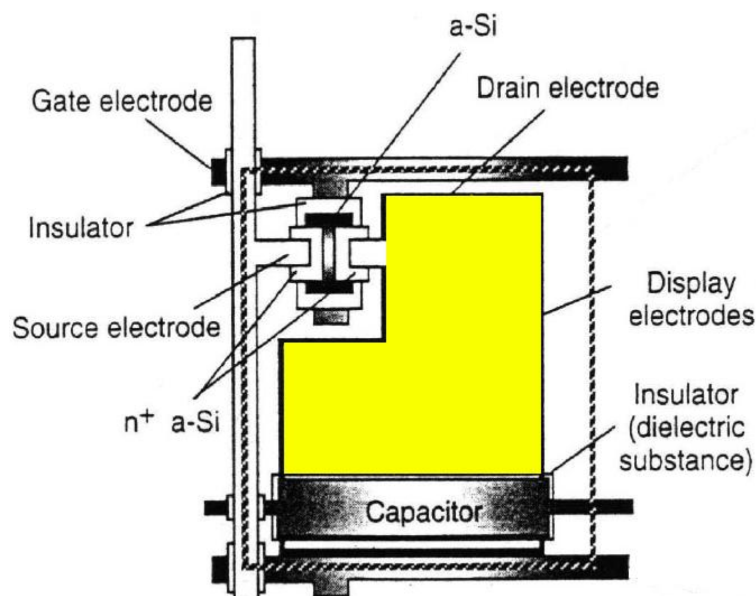

Figure 2.4 Schematic illustration of the TFT pixel unit [12]

2. Color filter substrate

The multi-color in TFT-LCD panels was attributed to the color filter array as Figure 2.5 shown [10]. Each pixel in TFT-LCD was subdivided into three sub-pixels, where one set of RGB sub-pixels was equal to one pixel. Because of the pixels were too small to distinguish, the color filter appeared to human eyes as a mixture of three colors. Each sub-pixel corresponded to a TFT unit which controlled the electrical field to determine the director of liquid crystal molecules, and then controlled the transparency of the light. Though the light only appeared in black or white (dark or bright) originally, a full-color was exhibited through the color filter.

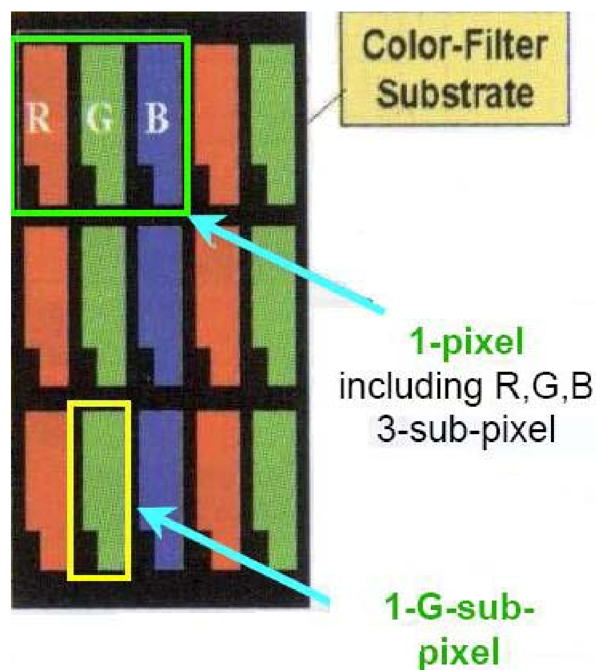

Figure 2.5 Color filter array in TFT-LCD [10]

3. Polarizer

A polarizer was a film that converted an unpolarized or mixed-polarization beam of electromagnetic waves, e.g., light, into a beam with a single polarization state (usually a single linear polarization). Polarizers were used in many optical techniques

and instruments such as photography and liquid crystal display.

Figure 2.6 showed a schematic illustration of polarizer working principle [13]. A grid polarizer converted an unpolarized beam into one with a single linear polarization. The arrows depicted the electric field vector. The diagonally-polarized waves also contributed to the transmitted polarization. Their vertical components were transmitted, while the horizontal components were absorbed. TFT-LCD utilized the polarizer film to convert the light into polarized beam and controlled the light transparency.

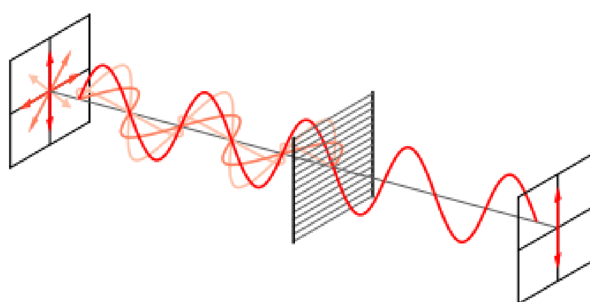

Figure 2.6 showed a schematic illustration of polarizer working principle [13]

4. Alignment layer

The liquid crystal in TFT-LCD needed a method to induce uniform alignment of the liquid crystal molecules near the surface. The alignment layer coated on the glass substrate played the key role. Typically, the alignment layer used in LCD industry was polyimide due to its thermal stability for the application, in addition, cheap and easy to apply. The method of producing alignment layer included unidirectional rubbing of a spin-coated polyimide surface with a velvet cloth as Figure 2.7 shown [14]. Microgrooves were created and the polymer chains were aligned in a uniform direction on the polymer surface by the contact between polymer surface and cloth. The liquid crystal then interacted with such a surface and aligned in a unidirection.

The alignment mechanism of the rubbing process has been discussed for decades. The main ideas for alignment mechanism were roughly divided into two contributing components. One was a physical model, the liquid crystal molecules aligned with the microgrooves on the polymer surface. The other one was a molecular model which the factors for alignment was that molecular interactions between liquid crystal molecules and surface polymer chains. These two models were shown in Figure 2.8. The former model, physical one, was laid by Berreman, in his elastic continuum theory of 1972 [15]. This theory indicated that the liquid crystal molecules orient themselves parallel to the microgrooves. The driving force for this model was to minimizing the surface energy. The later model, molecules interactions one, was proposed by Geary in 1987. [16] The theory suggested that the polymer chain and/or substituents near the surface were aligned by the unidirectional rubbing. This results in that the surface polymer chain can interact with liquid crystal surface in a unidirectional alignment. Recent researches gave more agreement with the molecules interaction models. [17,18]

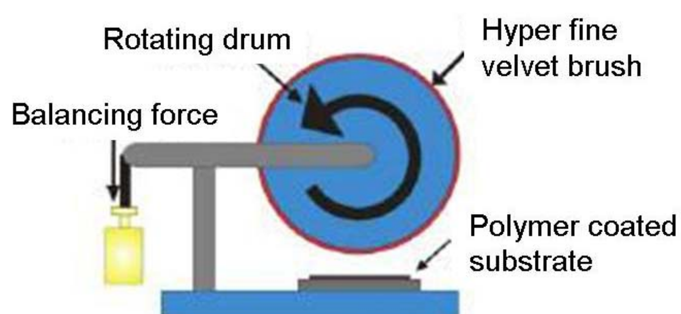

Figure 2.7 Simplified representation of rubbing [14]

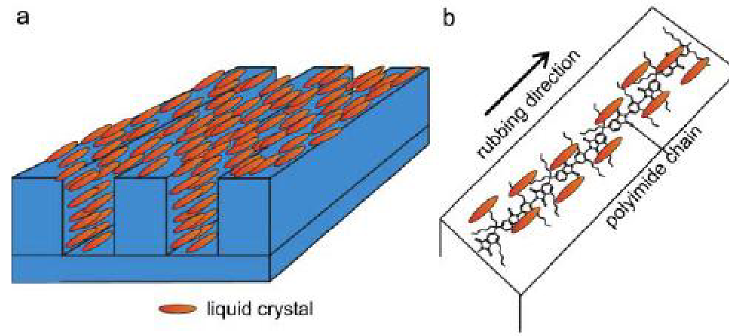

Figure 2.8 (a) Berreman model of alignment and (b) molecular model of alignment [15]

2.1.2 Working Principle of TFT-LCD

The inexpensive twisted nematic (TN) display was the most common type in TFT-LCD for notebooks. Figure 2.9 showed the schematic illustration of the operation principle in TN cell [19]. In TN cell, two linear polarizers attached on upper and bottom glass substrates were perpendicular to each other. When the nematic liquid crystal material was in the absence of an electrical field (OFF-state), the director of liquid crystal molecules at the top was perpendicular to the director at the bottom, twisted 90 degrees. The light entered the TN cell and its polarization state twisted with the director of the liquid crystal molecules. The light can transparent through the LCD cell appeared bright regions. On the contrary, when the LCD cell was in an electrical field (ON-state), the director of nematic liquid crystal molecules was parallel to the electric field direction and no longer twisted. Therefore, there was no light can transparent through the polarizer in regions where an electrical field was applied, appeared dark against the bright background.

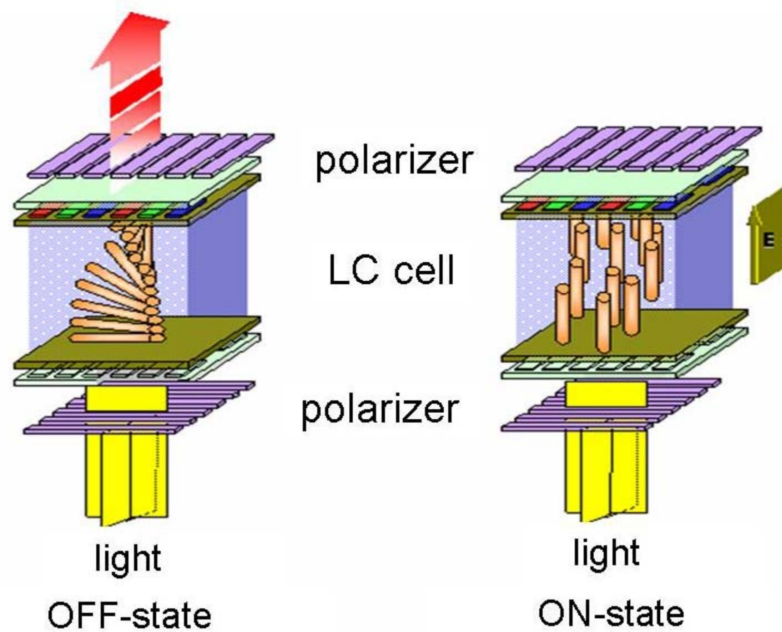

Figure 2.9 Schematic illustration of the operation principle in twisted nematic (TN) cell [19]

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2.2 Chip-on-Glass (COG) Package

Packaging technology of LCD IC drivers was an important process in LCD module. For improving the reliability and resolution of TFT-LCDs, the COG package had its benefits of low cost, high packaging density and potential for fine pitch compared to conventional package, for example, the tape automated bonding (TAB) packaging [20]. TAB was a process that places bare chips onto a printed circuit board (PCB) by attaching them to a polyamide film. Instead, COG technology which mounted the IC drivers on the glass substrate directly can save the cost of film substrate in TAB packaging. In the beginning, the COG technology was only applied to the small-sized display. Following the rapid progress of technique, the COG package technology also appeared in large-sized LCD (larger than 10 inches) to fulfill the requirements of high resolution, high I/O density, high performance and low-cost in package technology [21].

Figure 2.10 showed the schematic illustration of COG package process [22]. The IC drivers were directly mounted on the glass substrate by utilizing the anisotropic conductive film (ACF). The conductive particles in ACF deformed after applying temperature and pressure during a period of time, so that the bumps of IC drivers and the circuit on the glass substrate could be interconnected by the conductive particles.

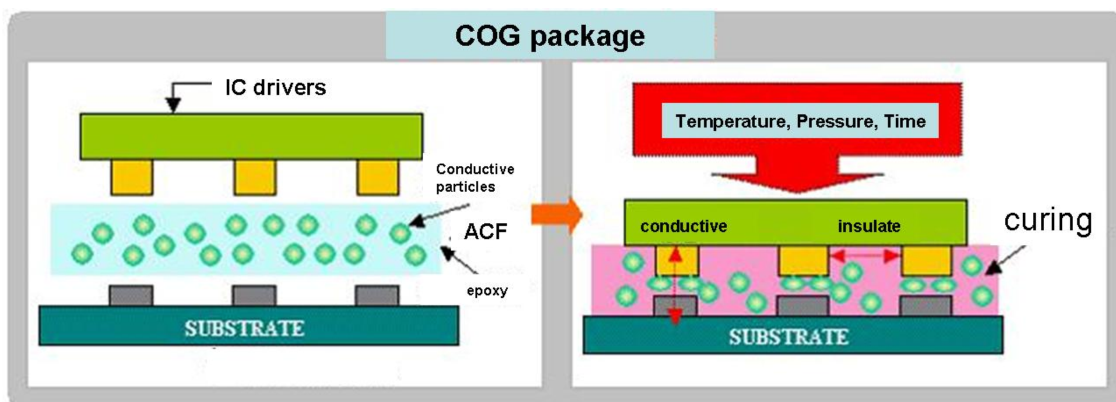

Figure 2.3 Schematic illustration of COG package process [22]

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2.3 Anisotropic Conductive Film (ACF)

Anisotropic conductive film was a conductive adhesive tape that had function of conducting electrically in vertical direction while completely insulating in horizontal direction. Besides, ACF tapes provided good mechanical adhesion between the IC drivers and various substrates such as glass, flexible plate and organic board. As Figure 2.11 shown, ACF were widely applied to chip-on-glass (COG), chip-on-film (COF), chip-on-board (COB), flexible-print-circuit (FPC), etc. [23] The ACF technology concerned to the IC driver package was especially important in LCD module. In addition, the requirement of fine pitch in IC drivers was decided by the properties of ACF such as conductive particle size and reliability.

ACF was mainly applied to the manufacturing processes which can not use the solder bump, for example, the inner circuit connects of LCD. Neither the outer lead

bonding (OLB) in TCP/COF package for LCD or the inner lead bonding (ILB) in COG for IC driver bonding, the ACF was the popular materials.

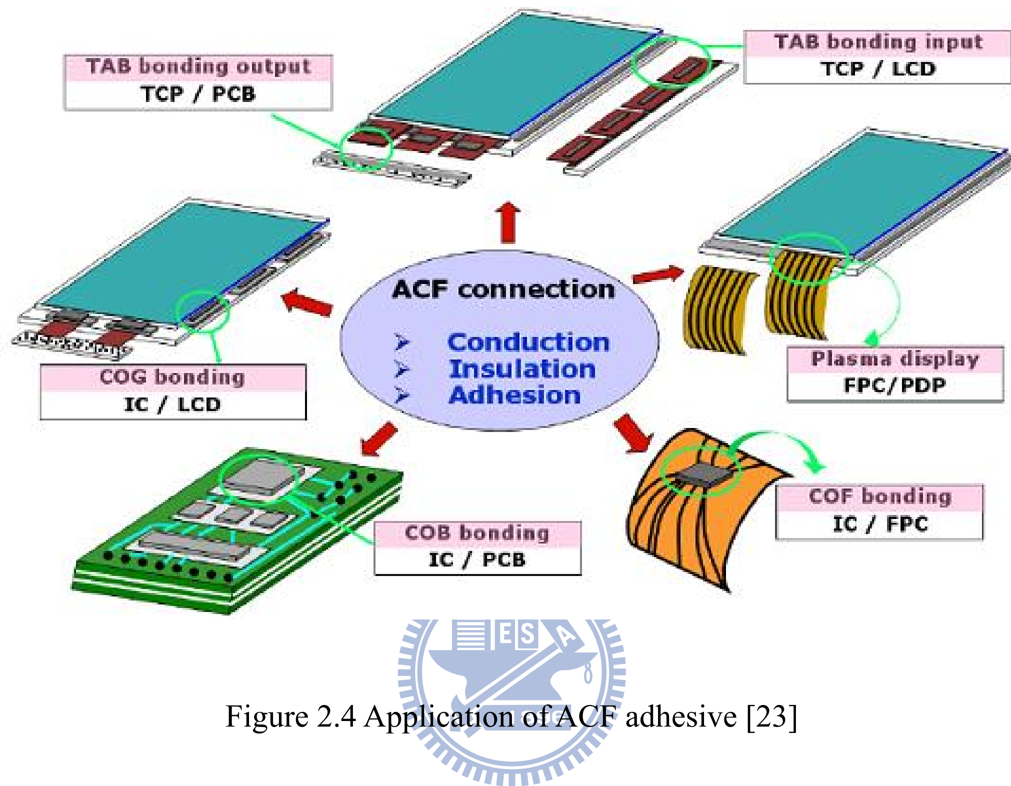


Figure 2.4 Application of ACF adhesive [23]

2.3.1 Structure of Anisotropic Conductive Film

Figure 2.12 showed the schematic illustration of ACF structure. ACF had conductive particles distributed randomly in adhesive matrix. The adhesive matrix usually adopted the thermal setting epoxy which had high temperature stability and low CTE as comparing to the thermal plastic epoxy. When the ACF underwent heat and pressure for a while, the compress stress of ACF had a good mechanical force to connect the two different materials. The advantages of ACF included: (1) ACF made as a tape which was easily fabricated, (2) the simplification of processes and equipment which did not require the reflow process and (3) uniform distribution of conductive particles can achieve high density pitch requirement.

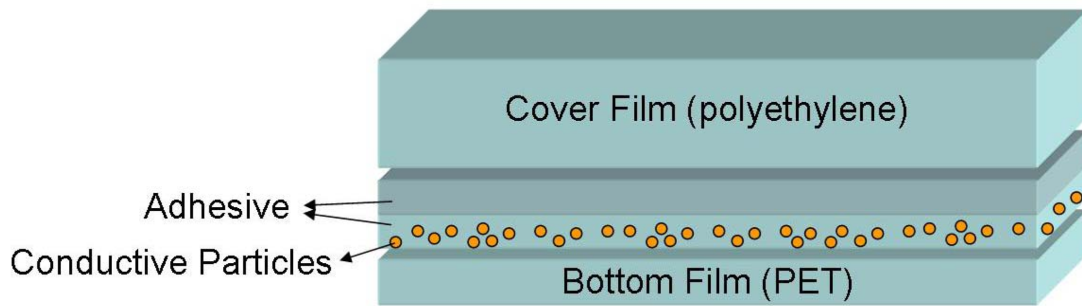


Figure 2.5 Schematic illustration of ACF structure

The other important material in ACF was the conductive particles. Figure 2.13 showed the components of conductive particle which the polymer core was coated with Ni/Au. Polymer core can be treated as a buffer material for absorbing the stress induced by the thermal budget. Ni coated first due to Au had poor adhesion with the polymer core. Au had best ductility, little activity, which meant poor reactivity with other material, and good electrically conductivity that only weaker than silver and copper. The usual size of the conductive particle was 3-5 μm. Corresponding to the requirement of fine pitch in COG packaging, the design of the density and size of the conductive particles in ACF was very important. The small size conductive particles can prevent the electrical short in horizontal direction due to particles gathering.

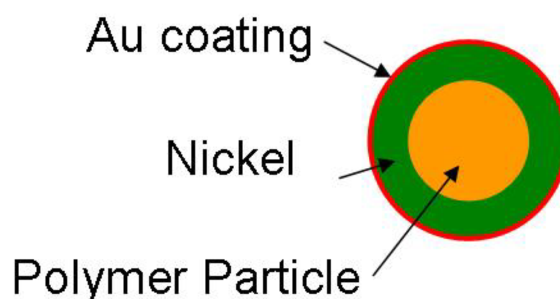


Figure 2.6 Components of conductive particle in ACF

2.3.2 Principle of ACF electrical conductivity

ACF was composed of conductive particles randomly dispersed in an insulator polymer matrix. When utilizing the ACF, cover film was ripped first and pasted on the substrate. Then ripped the other bottom film (PET) and bonded the electronic driver and substrate together after precisely alignment. By applying heat and pressure for appropriate time, the ACF film can provide good mechanical connects between IC drivers and substrate. Furthermore, ACF applied the vertical conducting electrically while insulating in horizontal as Figure 2.14 shown.

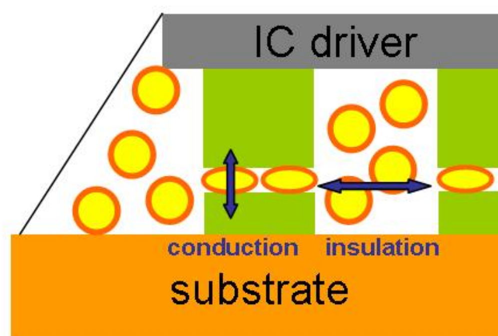


Figure 2.7 Schematic illustration of ACF conduction

2.3.3 Issues of the ACF-typed COG Package

The ACF-typed COG package had well-known problems about warpage and stress. The CTE mismatch among the ACF, chips and substrate was the main cause. The reliability of COG package concerned to the electrical short, contact resistivity increment and delamination. In particular, the delamination or crack at the interface of ACF and bumps was the most important issue. The warpage and deformation degree was related to the conductive resistance of the interconnection. The conductive resistance was lower at the center and input positions with larger deformation degree [24], and the outmost bump of IC driver usually had the most severity problems of

delamination and crack [25]. To solve the warpage and stress which were induced by ACF-typed COG package, it had been demonstrated that heating a glass substrate appropriately during COG interconnection and the use of a low stress type of ACF were very effective in reducing the warpage and improving the connection reliability in COG interconnection [26].

In addition, for the fine-pitched bump of IC drivers, fine pitch capability of ACF was desired especially in the COG package. The most important problem in fine-pitched IC was the electrical short in the horizontal direction since the conductive particles of ACF may easily trapped and form an electrical conduction in the small space of the adjacent bumps. Therefore, the size of conductive particles and the uniformity of distribution were important. Accordingly, the new typed ACF had double layer and conductive particles with insulate coated was proposed to improving the reliability of COG package [27]. Besides, the effects of height of bump and thickness of ACF were also reported that the different edged shapes of ACF had similar behavior and the warpage range would be enhanced with the ACF height [28].

2.4 Mura Defects in TFT-LCDs

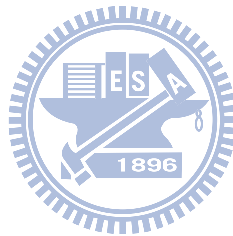
The ACF-typed COG packaging may induce Mura defect. Nowadays, more than the improvement for LCDs manufacturing technology, the visual quality also became a potential issue. The front-of-screen quality is of considerable important for LCD performance for the costumers. The non-uniform of contrast, brightness and color in LCD were generally called “Mura”. Y. Mori *et al* reported the possible causes of Mura for TFT-LCDs as Table 2.1 listed [29]. The Mura was induced by many reasons due to the complicated structure and components of LCD panel. If there were problems in any of the manufacturing process, the Mura defect may occur. In this study, the type of Mura was classified to the light leakage Mura.

The visual performance of LCD had usually been evaluated by visual inspection. However, the Mura with low contrast was hard to inspect by a naked eye. The Mura can be characterized by using an original algorithm for uniformity extraction had been reported by Y. Mori *et al* [24]. Besides, different systems to quantitate the Mura were also reported [30,31,32,33].

Typically, the thermal stress was the major concern on the Mura defect of LCD TVs. The high temperature gradient caused by the backlight unit resulted in the warpage and stress concentration in LCD substrate. For solving the stress problem, Y. Shin *et al.* reported that by (1) Using glass with low photo-elastic coefficients to reduce stress-induce birefringence, (2) Reduction of heat stress on glass by means of change the configuration of compensation film of polarizer and (3) Improvement of spatial temperature variation of BLU (Back Light Unit) can improve the Mura on Diagonal Direction [34]. M. Lin *et al.* reported that the Mura was related to the ripple of the optical film which caused by the back light unit [35]. In addition, A. Ogasawaea *et al*. reported that the polarizer film shrinkage by heat and humidity, and improved the Mura by studying the adhesive with stress relaxation property [36]. However, the root-cause of the light leakage phenomenon in mid-size TFT-LCD panel caused by COG package has not been clearly addressed yet. The causes of the light leakage phenomenon will be discussed in the following chapter.

Table 2.1 Causes of Mura in TFT-LCDs [24]

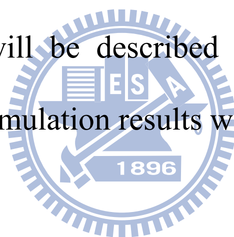
Classification	Causes
Cell	1. Nonuniform thickness of TFT array layer
	2. Nonuniform density of liquid crystal
	3. Nonuniform gap between glasses
	4. Nonuniform color of color filter
Backlight	5. Nonuniform lamp rays
	6. Wrinkled optical filter
	7. Warped light pipe



Chapter 3 Finite Element Analysis and Experimental

The light leakage Mura in TFT-LCDs with COG packaging was found to be induced after ACF thermal bonding process to connect silicon IC drivers and wirings on the bottom glass. In this thesis, various manufacturing processes parameters of COG packaging (e.g. ACF curing temperature, CTE and modulus of ACF, and dimensions of COG packaging) were studied by a Finite-Element-Analysis package tool, ANSYS™, to examine their effectiveness in reducing the warpage and thermal stress in LCD structure.

A brief introduction to the history of FEA and the basic theory of the numerical analysis will be given in this chapter. Moreover, the assumptions in this simulation and numerical model construction will be described in details. Finally, the experiment measurement for validating the simulation results will be also described.



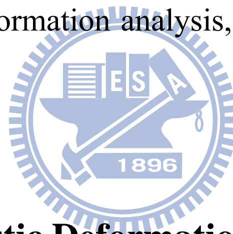
3.1 Finite Element Analysis (FEA) Method

3.1.1 Introduction of FEA

In the beginning, the finite element method [37] was invented to investigate the complex elasticity and structural analysis problems in civil and aeronautic engineering. Its origin can be traced back to the research by Alexander Hrennikoff and Ricahrd Courant [38]. Development of the finite element method in the 1950s for airframe and structural analysis at University of Stuttgart through the work of John Argyris and at Berkeley through the work of Ray W. Clough in the 1960s for use in civil engineering [39]. The key concepts of stiffness matrix and element assembly used in today were established by late 1950s [40].

In modern design of structural engineering, the structural mechanical problems are

usually complex. For example, analyzing the deformation of a car in a crash, it is almost impossible to use only mathematical partial differential equations to describe and solve such a complicated problem. However, the finite element method can cut the complex structure into lots of small unit elements, and then the partial differential equations were created for each element which underwent an external force field. Based on the finite element method, each element pieced together and set the boundary conditions. Then the complex structural model for numerical analysis can be established. Finite element method allowed detailed visualization of where structures bend/twist and showed the distribution of stresses and displacements. Therefore, the engineers can construct, refine and optimize the whole design before manufacturing. Modern finite element method packages including components such as thermal, mechanic, elastic (or plastic) deformation analysis, electromagnetic and fluid has been well developed.



3.1.2 Theory of Linear Elastic Deformation [41]

In this study, the COG packaging processes were analyzed by a FEA simulation tool, ANSYS™, to investigate the deformation and stress distribution caused by the thermal bonding process. The materials used in this numerical model were assumed to be linear elastic. The relationship between stress and strain in linear elastic materials can be described by the Hook’s Law:

$$\{\sigma\} = [D]\{\varepsilon^{el}\} \tag{3- 1}$$

$$\{\varepsilon^{el}\} = \{\varepsilon\} - \{\varepsilon^{th}\} \tag{3- 2}$$

where:

$\{\sigma\}$ = stress vector $=[\sigma_x\ \sigma_y\ \sigma_z\ \sigma_{xy}\ \sigma_{yz}\ \sigma_{xz}]^T$, stress vector as Figure 3.1 shown

$[D]$= elasticity or elastic stiffness matrix or stress-strain matrix

$\{\varepsilon^{el}\}$ = elastic strain vector

$\{\varepsilon\} = [\varepsilon_x\ \varepsilon_y\ \varepsilon_z\ \varepsilon_{xy}\ \varepsilon_{yz}\ \varepsilon_{xz}]^T$, total strain vector

$\{\varepsilon^{th}\}$ = thermal strain vector

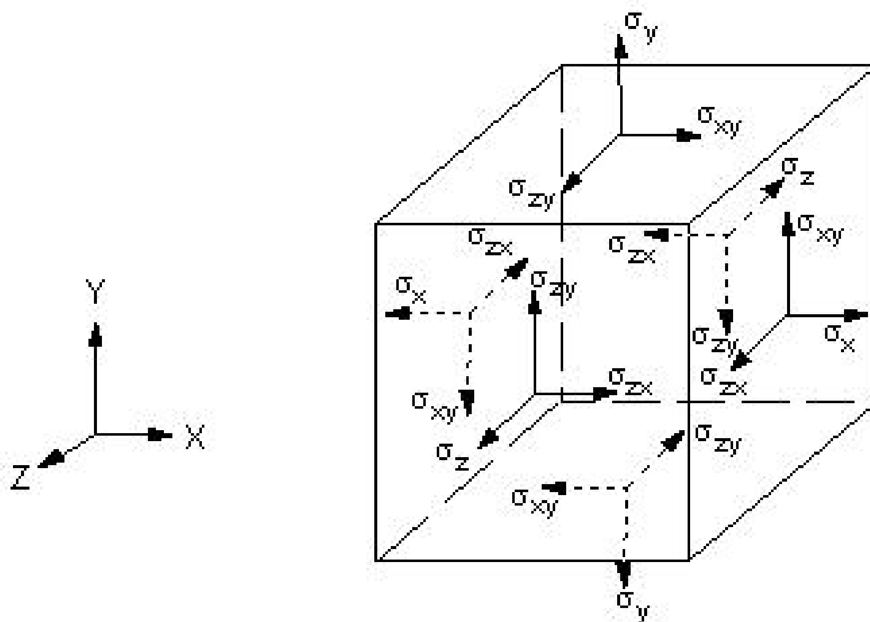


Figure 3.1 schematic illustration of stress vector

Equation 3-1 may also be inverted to:

$$\{\varepsilon\} = \{\varepsilon^{th}\} + [D]^{-1}\{\sigma\} \tag{3- 3}$$

For the 3-D case, the thermal strain vector is:

$$\{\varepsilon^{th}\} = \Delta T [\alpha_x^{se} \quad \alpha_y^{se} \quad \alpha_z^{se} \quad 0 \quad 0 \quad 0]^T \tag{3- 4}$$

where:

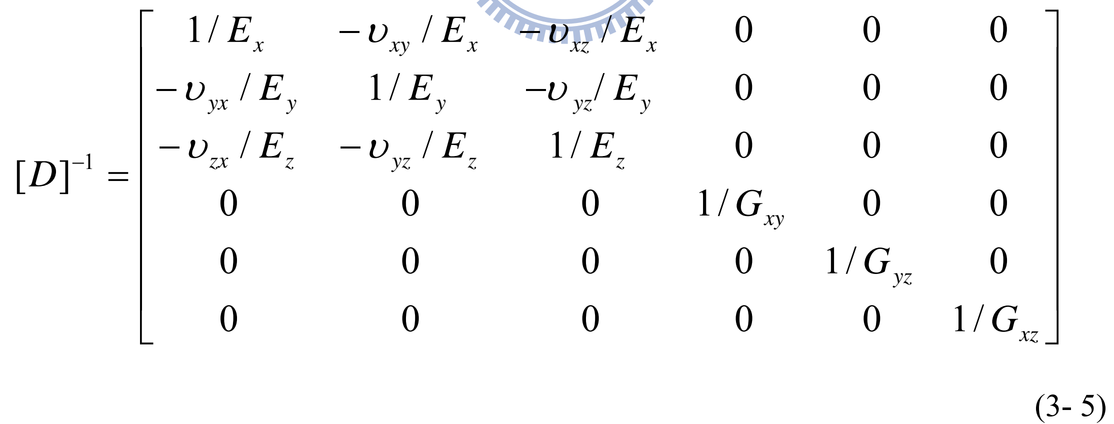
α_x^{se} = secant coefficient of thermal expansion in the x direction, if materials is isotropic, then $\alpha_x^{se} = \alpha_y^{se} = \alpha_z^{se}$

$\Delta T = T - T_{ref}$

T = current temperature at the point in question

T_{ref} = reference (strain-free) temperature

The flexibility or compliance matrix, $[D]^{-1}$ is:



$$[D]^{-1} = \begin{bmatrix} 1/E_x & -\upsilon_{xy}/E_x & -\upsilon_{xz}/E_x & 0 & 0 & 0 \\ -\upsilon_{yx}/E_y & 1/E_y & -\upsilon_{yz}/E_y & 0 & 0 & 0 \\ -\upsilon_{zx}/E_z & -\upsilon_{yz}/E_z & 1/E_z & 0 & 0 & 0 \\ 0 & 0 & 0 & 1/G_{xy} & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/G_{yz} & 0 \\ 0 & 0 & 0 & 0 & 0 & 1/G_{xz} \end{bmatrix} \tag{3- 5}$$

where:

E_x = Young's modulus in the x direction

ν_{xy} = major Poisson's ratio

ν_{yx} = minor Poisson's ratio

G_{xy} = shear modulus in the xy plane

If the material is isotropic, then:

$E_x = E_y = E_z = E$ (3- 6)

$\nu_{xy} = \nu_{yx} = \nu_{yz} = \nu_{zy} = \nu_{xz} = \nu_{zx} = \nu$ (3- 7)

$G_{xy} = G_{yz} = G_{xz} = G = E/2(1+\nu)$ (3- 8)

Expanding Equation 3-3 with Equation 3-4 through Equation 3-8 and writing out the six equations below:

$$\varepsilon_x = \alpha_x \Delta T + \frac{\sigma_x}{E_x} - \frac{\upsilon_{xy}\sigma_y}{E_x} - \frac{\upsilon_{xz}\sigma_z}{E_x} \quad (3\text{- }9)$$

$$\varepsilon_y = \alpha_y \Delta T - \frac{\upsilon_{xy}\sigma_x}{E_x} + \frac{\sigma_y}{E_y} - \frac{\upsilon_{yz}\sigma_z}{E_y} \quad (3\text{- }10)$$

$$\varepsilon_z = \alpha_z \Delta T - \frac{\upsilon_{xz}\sigma_x}{E_x} - \frac{\upsilon_{yz}\sigma_y}{E_y} + \frac{\sigma_z}{E_z} \quad (3\text{- }11)$$

$$\varepsilon_{xy} = \frac{\sigma_{xy}}{G_{xy}} \quad (3\text{- }12)$$

$$\varepsilon_{yz} = \frac{\sigma_{yz}}{G_{yz}} \quad (3\text{- }13)$$

$$\varepsilon_{xz} = \frac{\sigma_{xz}}{G_{xz}} \quad (3\text{- }14)$$

where,

ε_x = direct strain in the x direction

σ_x = direct stress in the x direction

ε_{xy} = shear strain in the x-y plane

σ_{xy} = shear stress on the x-y plane

Alternatively, Equation 3-1 may be expanded by Equation 3-5 and the combining that result with Equation 3-4 and Equation 3-6, 3-7 and 3-8 to give six equations below:

$$\begin{aligned}\sigma_x &= \frac{E_x}{h}\left(1-(\upsilon_{yz})^2\frac{E_z}{E_y}\right)(\varepsilon_x-\alpha_x\Delta T)+\frac{E_y}{h}(\upsilon_{xy}) \\ &+\upsilon_{xz}\upsilon_{yz}\frac{E_z}{E_y}\overrightarrow{AB}(\varepsilon_y-\alpha_y\Delta T)+\frac{E_z}{h}(\upsilon_{xz}+\upsilon_{yz}\upsilon_{xy})(\varepsilon_z-\alpha_z\Delta T)\end{aligned} \tag{3- 15}$$

$$\begin{aligned}\sigma_y &= \frac{E_y}{h}\left(\upsilon_{xy}+\upsilon_{xz}\upsilon_{yz}\frac{E_z}{E_y}\right)(\varepsilon_x-\alpha_x\Delta T) \\ &+\frac{E_y}{h}\left(1-(\upsilon_{xz})^2\frac{E_z}{E_x}\right)(\varepsilon_y-\alpha_y\Delta T)+\frac{E_z}{h}\left(\upsilon_{yz}+\upsilon_{xz}\upsilon_{xy}\frac{E_y}{E_x}\right)(\varepsilon_z-\alpha_z\Delta T)\end{aligned} \tag{3- 16}$$

$$\begin{aligned}\sigma_z &= \frac{E_z}{h}(\upsilon_{xz}+\upsilon_{yz}\upsilon_{xy})(\varepsilon_x-\alpha_x\Delta T) \\ &+\frac{E_z}{h}\left(\upsilon_{yz}+\upsilon_{xz}\upsilon_{xy}\frac{E_y}{E_x}\right)(\varepsilon_y-\alpha_y\Delta T)+\frac{E_z}{h}\left(1-(\upsilon_{xy})^2\frac{E_y}{E_x}\right)(\varepsilon_z-\alpha_z\Delta T)\end{aligned} \tag{3- 17}$$

$$\sigma_{xy} = G_{xy}\varepsilon_{xy} \tag{3- 18}$$

$$\sigma_{yz} = G_{yz}\varepsilon_{yz} \tag{3- 19}$$

$$\sigma_{xz} = G_{xz}\varepsilon_{xz} \tag{3- 20}$$

where,

$$h = 1-(\upsilon_{xy})^2\frac{E_y}{E_x}-(\upsilon_{yz})^2\frac{E_z}{E_y}-(\upsilon_{xz})^2\frac{E_z}{E_x}-2\upsilon_{xy}\upsilon_{yz}\upsilon_{xz}\frac{E_z}{E_x} \tag{3- 21}$$

Moreover, the principal strain can be represented as ε_0:

$$\begin{vmatrix} \varepsilon_x - \varepsilon_0 & \frac{1}{2}\varepsilon_{xy} & \frac{1}{2}\varepsilon_{xz} \\ \frac{1}{2}\varepsilon_{xy} & \varepsilon_y - \varepsilon_0 & \frac{1}{2}\varepsilon_{yz} \\ \frac{1}{2}\varepsilon_{xz} & \frac{1}{2}\varepsilon_{yz} & \varepsilon_z - \varepsilon_0 \end{vmatrix}$$

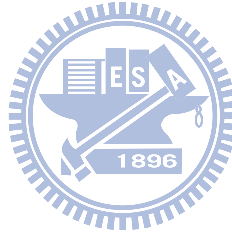
$$\varepsilon_0 = [\varepsilon_1 \quad \varepsilon_2 \quad \varepsilon_3] \tag{3- 22}$$

Maximum strain difference ε_I:

$$\varepsilon_I = MAX\,[|\varepsilon_1 - \varepsilon_2||\varepsilon_2 - \varepsilon_3||\varepsilon_3 - \varepsilon_1|] \tag{3- 23}$$

The principal stress can be presented as σ_0:

$$\begin{vmatrix} \sigma_x - \sigma_0 & \sigma_{xy} & \sigma_{xz} \\ \sigma_{xy} & \sigma_y - \sigma_0 & \sigma_{yz} \\ \sigma_{xz} & \sigma_{yz} & \sigma_z - \sigma_0 \end{vmatrix}$$



$$\sigma_0 = [\sigma_1 \quad \sigma_2 \quad \sigma_3] \tag{3- 24}$$

Maximum stress difference σ_I:

$$\sigma_I = MAX\,[|\sigma_1 - \sigma_2||\sigma_2 - \sigma_3||\sigma_3 - \sigma_1|] \tag{3- 25}$$

3.1.3 Theory of thermal conduction and convection [25]

In this study, the thermal conduction and convection model were also employed. The first law of thermodynamics states that thermal energy is conserved. The first law of thermodynamics to a differential control volume can be describe as following:

$$\rho c\left(\frac{\partial T}{\partial t} + \{v\}^T\{L\}T\right) + \{L\}^T\{q\} = \ddot{q} \tag{3- 26}$$

where:

ρ = density

c = specific heat

T = temperature

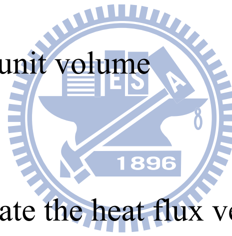
t = time

$$\{L\} = \begin{Bmatrix} \frac{\partial}{\partial x} \\ \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} \end{Bmatrix} = \text{vector operator}$$

$$\{v\} = \begin{Bmatrix} V_x \\ V_y \\ V_z \end{Bmatrix} = \text{velocity vector for mass transport of heat}$$

$\{q\}$ = heat flux vector

$\ddot{q}$ = heat generation rate per unit volume



Next, Fourier's Law is used to relate the heat flux vector to the thermal gradients:

$$\{q\} = -[D]\{L\}^T \tag{3- 27}$$

where:

$$[D] = \begin{bmatrix} K_{xx} & 0 & 0 \\ 0 & K_{yy} & 0 \\ 0 & 0 & K_{zz} \end{bmatrix} = \text{conductivity matrix}$$

K_{xx}, K_{yy}, K_{zz} = conductivity in the element x, y and z directions, respectively

Equation 3-26 and 3-27 are combined to yield the following,

$$\rho c\left(\frac{\partial T}{\partial t}+\{V\}^{T}\{L\}T\right)=\{L\}^{T}([D]\{L\}T)+\ddot{q} \tag{3- 28}$$

Equation 3-28 is then expand to its more familiar form:

$$\begin{aligned}&\rho c\left(\frac{\partial T}{\partial t}+V_{x}\frac{\partial T}{\partial x}+V_{y}\frac{\partial T}{\partial y}+V_{z}\frac{\partial T}{\partial z}\right)\\&=\ddot{q}+\frac{\partial}{\partial x}\left(K_{x}\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(K_{y}\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(K_{z}\frac{\partial T}{\partial z}\right)\end{aligned} \tag{3- 29}$$

It will be assumed that all effects are in the global Cartesian system. Three types of boundary conditions are considered, assuming that these cover the entire element.

1. Specified temperatures acting over surface:

$$T = T^{*} \tag{3- 30}$$

where T* is the specified temperature

2. specified heat flows acting over surface:

$$\{q\}^{T}\{\eta\}=-q^{*} \tag{3- 31}$$

where:

$\{\eta\}$ = unit outward normal vector

q^{*} = specified heat flow

3. Specified convection surfaces acting over surface:

$$\{q\}^T \{\eta\} = h_f (T_S - T_B) \qquad (3\text{- }32)$$

where:

h_f = film coefficient

T_B = bulk temperature of the adjacent fluid

T_S = temperature at the surface of the model

Combining Equation 3-27 with Equations 3-30 and 3-31 yields the followings,

$$\{\eta\}^T [D]\{L\}T = q^* \qquad (3\text{- }33)$$

$$\{\eta\}^T [D]\{L\}T = h_f (T_B - T) \qquad (3\text{- }34)$$

Premultiplying Equation 3-28 by a virtual change in temperature, integrating over the volume of the element, and then combining with Equations 3-33 and Equation 3-34 with some manipulation yields:

$$\int_{vol} \left(\rho c\, \delta T \left(\frac{\partial T}{\partial t} + \{V\}^T \{L\}T \right) + \{L\}^T (\delta T)([D]\{L\}T) \right) d(vol) =$$

$$\int_{S_2} \delta T\, q^* \, d(S_2) + \int_{S_3} \delta T\, h_f (T_B - T) d(S_3) \int_{vol} \delta T\, \ddot{q}\, d(vol) \qquad (3\text{- }35)$$

where:

vol = volume of the element

δT = an allowable virtual temperature

3.2 Setup of Numerical Model Setup

3.2.1 COG Processes and Problem Statements

In order to investigate the effect of COG packaging on the light leakage phenomenon, a 3-D finite element analysis was employed to carry out the thermo-mechanical stress and warpage analysis of LCD panel by utilizing the FEA simulation tool, ANSYS™. In this study, the commercial 13.3-inch LCD panel (TN type) with 8 silicon IC drivers connected to the wirings on glass substrate through ACF was first investigated. When the thickness of LCD glass substrate decreased from 0.5 mm to 0.3 mm, the light leakage phenomenon appeared, as illustrated previously in Figure 1.2. In this study, the light leakage region only appeared at the edge of LCD panel with COG packaging in half-moon-like shape and showed less severity near corners. Moreover, it was related to the Si chips arrangement, the light leakage showed between chips. According to the observations about the light leakage phenomenon, it was highly related with the COG packaging. Furthermore, the warpage and stress induced by COG packaging were analyzed by simulation tool to figure out the root-cause(s) of the light leakage Mura.

3.2.2 Selected Elements [25]

In this simulation model, the materials used in COG package were treated as elastic linear materials. Appropriate elements were selected for fitting the structure and materials characteristics in a LCD panel. 3-D element of SOLID70 was chosen for thermal analysis. Moreover, SOLID45 element and SOLID-SHELL190 element (for high aspect ratio) for 3-D model were chosen for mechanical analysis. A brief introduction to these elements is given below:

1. SOLID70

SOLID70 has a 3-D thermal conduction capability. The element has eight nodes with a single degree of freedom, temperature, at each node. The element is applicable to a 3-D, steady-state or transient thermal analysis. If the model equipped with the conducting solid elements, is also to be analyzed structurally, the element should be replaced by an equivalent structural element, such as SOLID45.

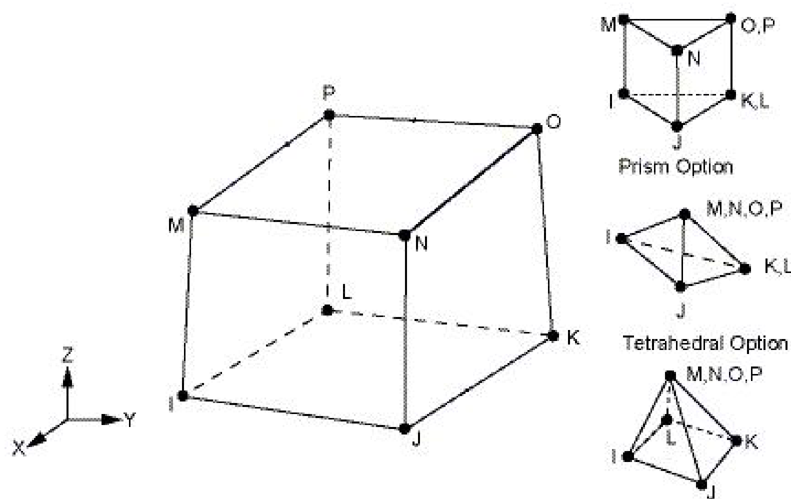


Figure 3.2   Geometry of SOLID70 element

2. SOLID45

SOLID45 is used for the 3-D modeling of solid structure. The element is defined by eight nodes having three degrees of freedom at each node: translations in the nodal x, y, and z directions. The element has plasticity, creep, swelling, stress stiffening, large deflection, and large strain capabilities.

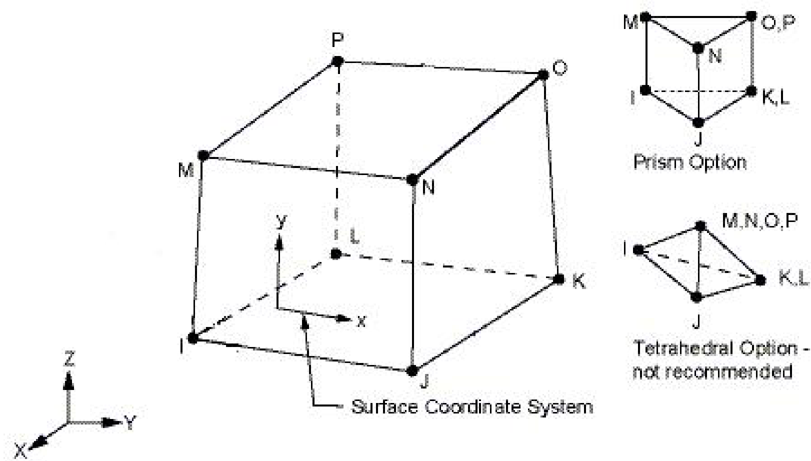


Figure 3.3　Geometry of SOLID45 element

3. SOLID-SHELL190

SOLSH190 is used for simulating shell structures with a wide range of thickness (from thin to moderately thick). The element possesses the continuum solid element topology and features eight-node connectivity with three degrees of freedom at each node: translations in the nodal x, y, and z directions. Thus, connecting SOLSH190 with other continuum elements requires no extra effort. The element has plasticity, hyper-elasticity, stress stiffening, creep, large deflection, and large strain capabilities.

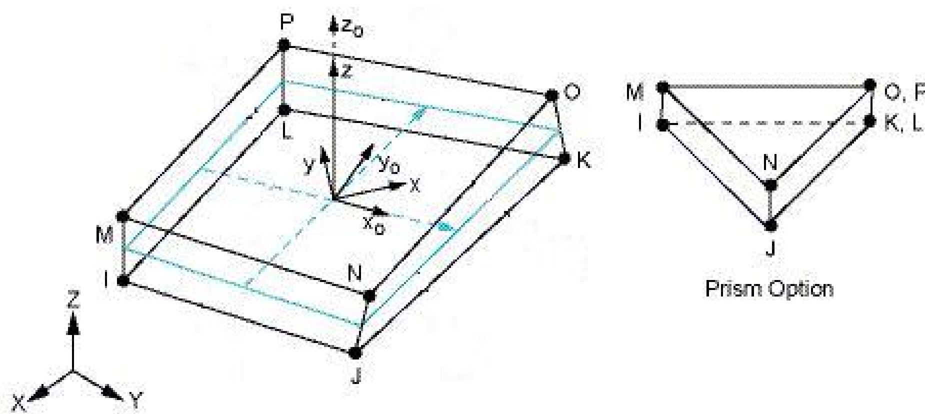


Figure 3.4　Geometry of SOLID-SHELL190

In addition, using SOLSH190 can acquire an accurate result even for the coarse meshes as shown in Figure 3.5. Besides, SOLSH190 element had benefits such as easy connection with other continuum elements, easy handling of variable thickness and no more need for mid-surface extraction.

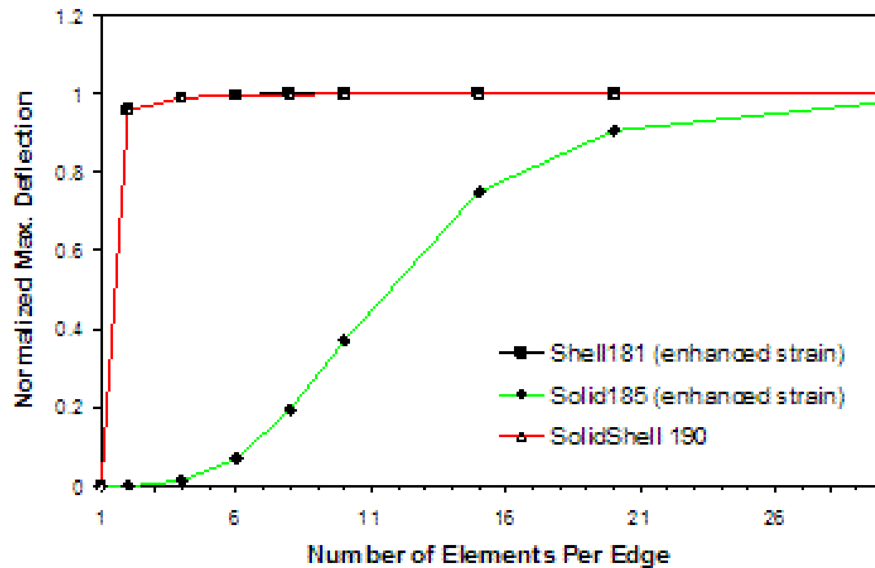


Figure 3.5 The normalized maximum deflection as a function of number of elements per edge for SolidShell190 and Solid185

3.2.3 Assumptions of FEA Model

In order to obtain the balance between accuracy and efficiency, several assumptions are employed in this numerical model and summarized below:

1. All of the materials are isotropic and linear elastic due to the limited displacement in our model.
2. All of the components in the global model have perfect adhesion between each other.
3. The bumps underneath the Si chips are ignored due to their considerable quantities and limited effect on the thermal-mechanical deformation.
4. The optical films such as polarizer which is too thin and soft, are also ignored

due to their limited influence on the thermal-mechanical deformation.

5. The global model is a 1/2 symmetric model
6. The symmetric surface is set as the symmetric plane, in which the translation and rotation are fixed.
7. The transient temperature distribution is calculated first, then applied to the thermal-mechanical model.
8. The temperature in third step of the warpage analysis was set at 25°C to simulate the cooling down process.

3.2.4 Transient Thermal Analysis Model

The thermal history of the COG packaging included a brief thermal bonding process (10 seconds typically) to curing the ACF adhesive and forming metal connection between Si chips and substrate. Due to the mismatch in material properties among Si chips, glass substrate and ACF adhesive, especially thermal conductivity and specific heat, a large thermal gradient existed in the COG assembly and resulted in the warpage and stress (localized and global). This was a non-steady state for thermal analysis since the global model was not in a thermal equilibrium state after only 10 seconds thermal bonding. Thus, a transient thermal was employed first to carry out the thermal distribution after the thermal bonding process. The LCD panel structure had a 1/2 symmetry, so only a 1/2 symmetric finite element model was established to enhance the simulation efficiency.

The selected element for the thermal analysis was SOLID70, which is a 3-D element with 8 nodes. An 180°C temperature thermal loading was applied to the top-side of the Si chips for 10 seconds. Also, the symmetric plane was set as the isothermal plane. In general, the heat transfer included three types: (1) thermal conductivity, (2) thermal convection, and (3) thermal radiation. However, it would take

up tremendous calculation time if all three types of heat transfer were taken into account. The specific values of thermal convection and thermal radiation needed the complex calculation through computational fluid dynamics (CFD). It was time consuming and not efficiency. Therefore, the experience formula of thermal transfer was applied to determine the thermal convection on the surface of the global model in this thermal analysis. Mulgaonker *et al* [42] and Chen *et al* [43] reported that by applying the thermal convection value of 8.5 W/m^2 can obtain a certain accurate temperature distribution field in the model of small-sized assembly. Therefore, the value of thermal convection, 8.5 W/m^2, was adopted in our model. Other material properties, for example, thermal conductivity, density and specific heat which used in this transient thermal model were obtained from literature and listed in Table 3.1. [28, 29]

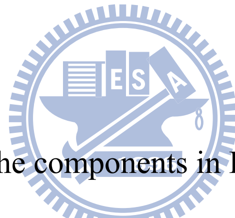


Table 3.1 Material properties of the components in LCD for transient thermal analysis [28, 29]

	Thermal conductivity(W/m-K)	Density (g/cm3)	Specific heat (J/kg-。C)
Glass substrate (Eagle2000)	1.5	2.370	710
Silicon chip	150	2.32	820
ACF	1.35	1	710
LCD sealant	1.35	1.2	710

3.2.5 Warpage Analysis Model

In order to investigate the effect of process parameters on light leakage phenomenon of the LCD panel, the model for thermal-mechanical stress and warpage

analysis was established by 3-D solid elements. The commercial 13.3-inch LCD panel was chosen to be the basic model in this study, 8 silicon chips as IC drivers were directly mounted on glass substrate through hundreds of bumps by thermal bonding of ACF near the panel edge. The panel structure included an ITO conductive film and optical films such as polarizer and compensation film, in addition to TN-based liquid crystal. To simplify the numerical model and reduce the computation time, the bumps, ITO and the optical films were not built in our model due to their limited influence on thermal-mechanical deformation. The model included components of glass substrate, Si chips, ACF adhesive and LCD sealant. The dimensions of all components were listed in Table 3.2. Since the LCD panel was a 2-fold symmetry, a 3-D model based on 1/2-panel was set up as shown in Figure 3.6. Because of a very high ratio (~1000) of length to thickness in both glass plates, a solid-shell element (Solid-Shell 190) was employed to obtain an accurate analysis [25]. The material properties of glass, Si chip, ACF adhesive and LCD sealant used in this model for thermal-mechanical analysis were listed in Table 3.3 [28, 29]. While the ACF and sealant were treated as temperature-dependent polymeric materials since they were sensitive to temperature as listed in Table 3.4. [44,45]

Taking into account of the thermal history of COG processing, the COG bonding process in this simulation was divided into three parts:

(1) The COG packaging was first carried out by applying high temperature and pressure on the topside of silicon chips to mount the chips onto bottom glass substrate through a bonding head. In the first simulation step, the global model was set at room temperature initially, and then a 180°C thermal loading was set on the top-side of the silicon chips and the z-axis displacement of chips was constrained due to the chips were held by bonding head and stage. Prior to thermal loading, the ACF was uncured and soft with very small elastic modulus as

compared to the silicon and the glass. Thus, the ACF were set as inactive elements.

(2) ACF was switched back to the active elements to simulate the curing process, while the temperature and constraint loading on silicon chips were still maintained in this step.

(3) The temperature and constraint loading on silicon chips were removed when the global model was cooled down to room temperature to simulate the COG-induced deformation behavior.

The symmetric constraint was applied on the symmetric plane. The back plane of the global model was constrained to avoid rigid motion. Moreover, a transient thermal analysis model which mentioned in the previous section was used to obtain the temperature distribution immediately after thermal bonding of ACF, for example at 180 ^{o}C. The temperature distribution at various locations was then applied to aforementioned Step 1 and Step 2 as the boundary conditions to carry out the coupled thermal-mechanical analysis. Thus, the computation time can be significantly reduced.

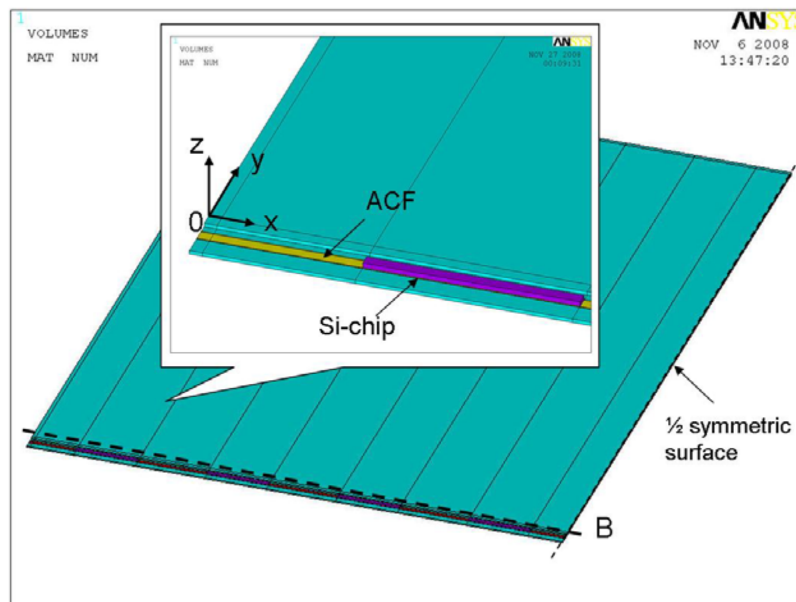


Figure 3.6 A 3-D FEA model with 1/2 symmetry

Table 3.2 Geometry dimensions of components in simulation models

	Length (mm)	Width (mm)	Thickness (mm)
Si chip	16.9	0.9	0.4
LCD sealant	146.5	1	3.875^10-3
ACF	146.5	1.1	25^10-3
Upper glass	146.5	184.55	0.3
Bottom glass	146.5	188	0.3

Table 3.3 Material properties of components for thermal mechanical analysis [28, 29]

	Young's modulus (GPa)	Poisson ratio	CTE (ppm/^{o}C)	Tg(^{o}C)
Glass substrate (Eagle2000)	70	0.2	3.25	-
Silicon chip	128	0.3	2.6	-
ACF	Table 3.4	0.4	CTE1=48.9 CTE2=168	119
LCD sealant	Table 3.4	0.4	CTE1=68 CTE2=223	90

Table 3.4 Temperature-dependent Young's modulus of ACF and LCD sealant [28, 29]

Temperature (◦ C)	21	100	150	190
ACF_Young's modulus (GPa)	1.6	0.8	0.2	0.05
LCD sealant_Young's modulus (GPa)	1.4	0.15	0.10	0.05

In FEA analysis, the mesh density decided the precision of the results. The more accurate result could be acquired by finer mesh but it would spend a lot of computation time. Therefore, the proper mesh density was examined in the beginning. Figure 3.7 shows the warpage of TFT-LCD panel as a function of elements number in our model. The warpage tended towards to certain value when elements number became large. The warpage difference between elements number of 36496 and 63390 was less than 2%. Thus, the mesh density chosen in our model was 36496 elements with 54502 nodes.

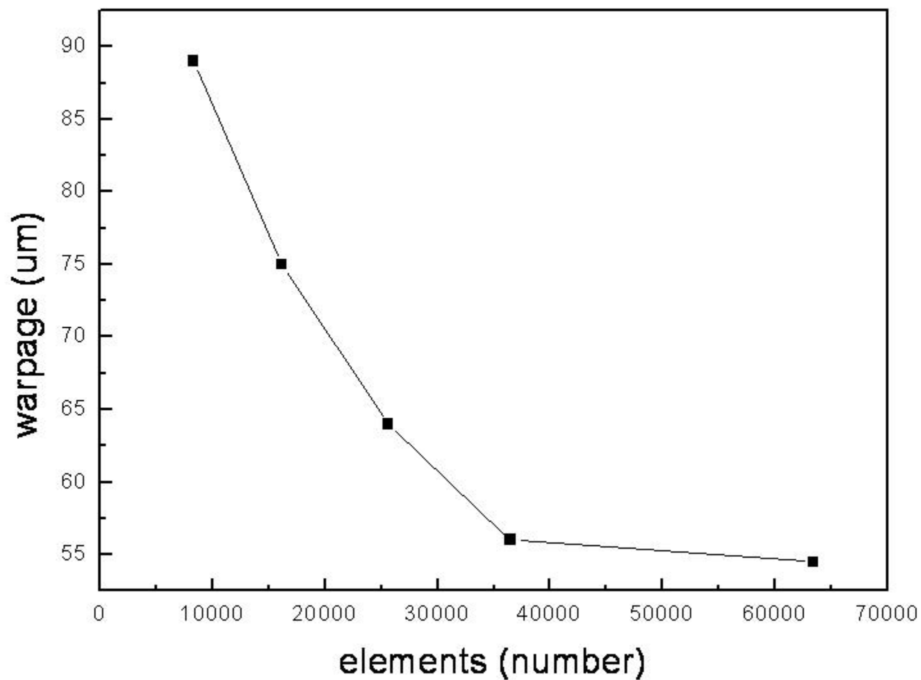


Figure 3.7 Warpage of TFT-LCD panel as a function of elements number in FEA model

3.3 Experimental Measurement of Warpage

To check the accuracy of the numerical model and analysis, the simulated warpage results were validated by surface contour measurement tool using KOSAKA ET4000A as shown by Figure 3.8. It was a probe system to measure the contour of the sample surface. The vertical resolution of this tool, KOSAKA ET4000A, was 0.1nm, which

vertical range was +/- 65um. It was appropriate for measurement of micro figure, step height, roughness and surface contour.

In order to explore the relationships between warpage and the light leakage phenomenon, surface contour measurement was carried out for measuring the warpage of the upper glass near the edge of LCD panel. The LCD panels for warpage measurement, which were supplied by Chi-Mei Optoelectronics Corp. (CMO), included various thickness of glass substrate (0.3 mm and 0.5 mm), different ACF bonding temperature (160 ^{o}C, 170 ^{o}C and 180 ^{o}C), and modulus of ACF (1.6GPa and 0.3 GPa at room temperature)

Figure 3.8 Surface contour measurement tool, KOSAKA ET4000

Chapter 4 Results and Discussion

4.1 Thermal Transient Analysis

Figure 4.1 shows the temperature distribution in one Si-chip after 10 seconds thermal bonding process at 180°C. Every Si chip on the LCD panel had the same temperature distribution due to the same treatment. Figure 4.2 shows the cross section view of temperature distribution across a LCD with COG package. The Si-chip and ACF reached 180 ^{o}C after the 10 seconds of thermal bonding. Immediately after thermal bonding, LCD sealant was ~90°C, which was still below its glass transition temperature. For a polymeric material at temperature below its Tg, the linear-elastic model was applicable to describe the thermal-mechanical behavior in general. Therefore, the sealant was treated as linear-elastic materials in this simulation model, instead of a plastic material, for the computational efficiency.

Figure 4.3 showed the transient thermal analysis of ACF (underneath Si chips) temperature in 10 seconds. The temperature of ACF reached 180°C in a very short time due to the high thermal conductivity of the Si chips with small dimension. In general, ACF needed to reach the 90% of the set temperature in 5 seconds to avoid the reflow of conductive adhesive arbitrarily.

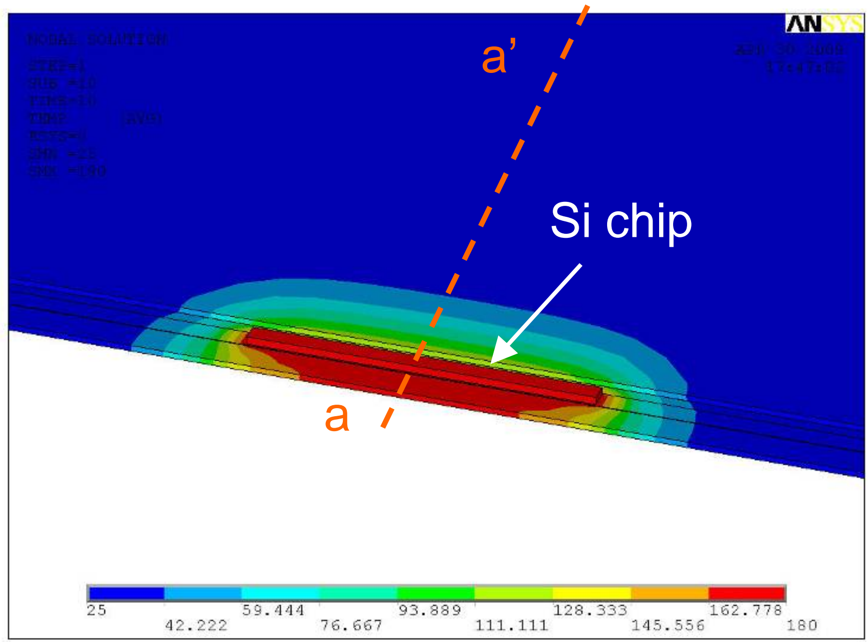


Figure 4.1 Temperature distribution of Si-chip after 10s thermal bonding

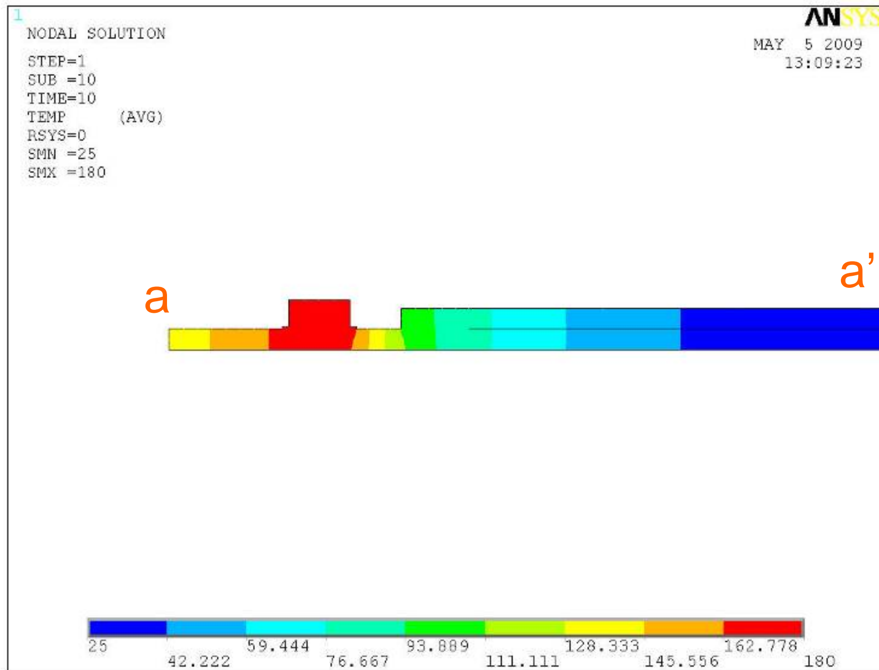


Figure 4.2 Cross section view of the thermal distribution

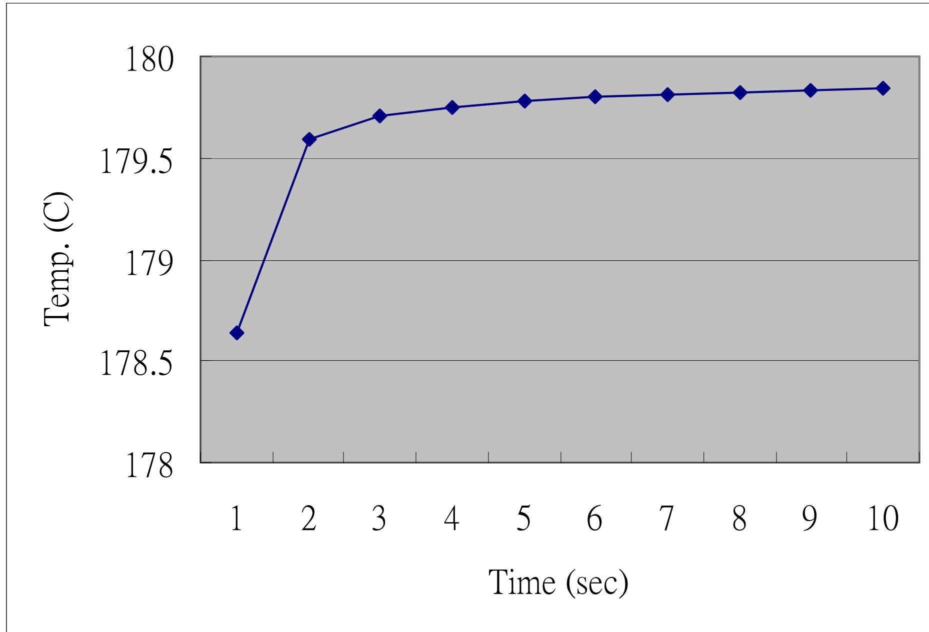
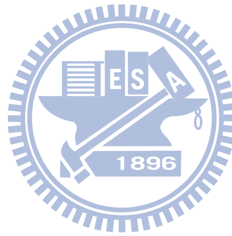


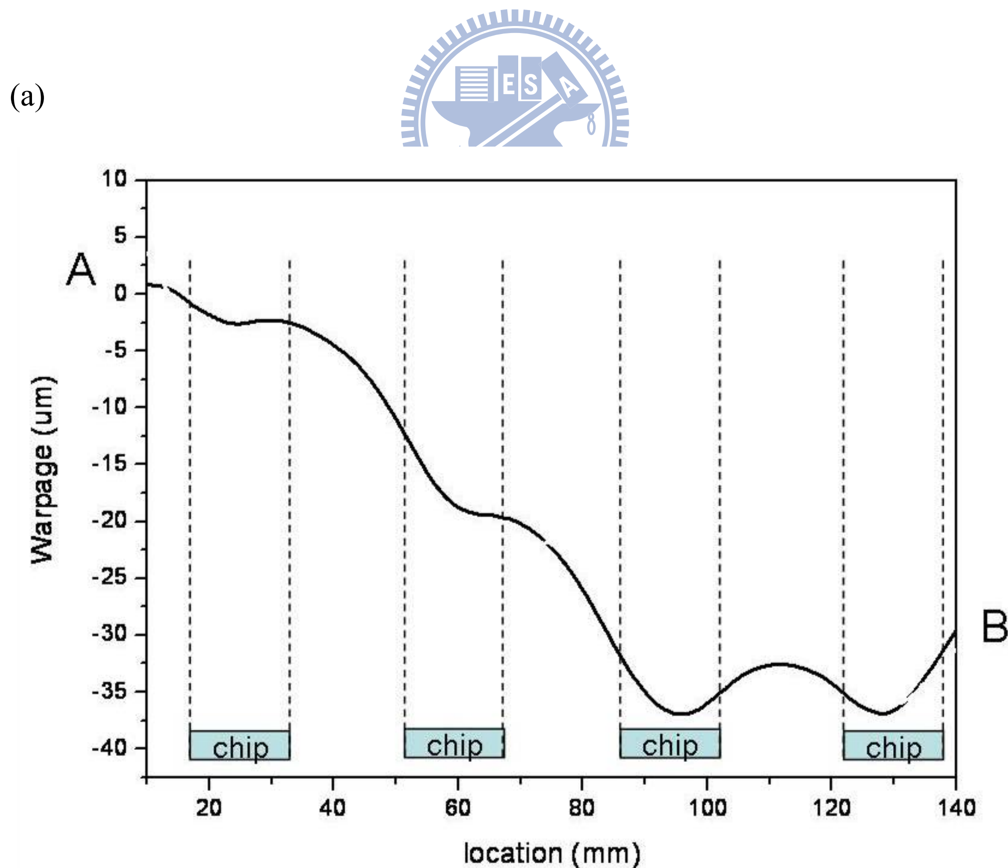
Figure 4.3 Transient thermal analysis of ACF temperature in 10s



4.2 Warpage Analysis

In the first stage, the commercial 13.3" TFT-LCD panel with original conditions of 0.3 mm glass substrate and 180 ^{o}C ACF curing temperature (0.3 mm/180 ^{o}C for simplifying for the rest of thesis) was studied. Based on surface contour measurement of upper glass along x-axis (parallel to the row of Si chips) at y =0 plane (see the coordinate system illustrated in Figure 3.5) shown in Figure 4.4(a), wave-like deformation induced by the silicon chips in COG package with a global warpage ~38 μm was found, while the localized warpage (valley to hilltop) was ~3.0 μm caused by the outmost chip (near A), and more severe, ~6.0 μm induced by the center chip (near B). The localized maximum warpage was found between two Si chips presumably due to the upward bending at Si chip edge.

(a)



(b)

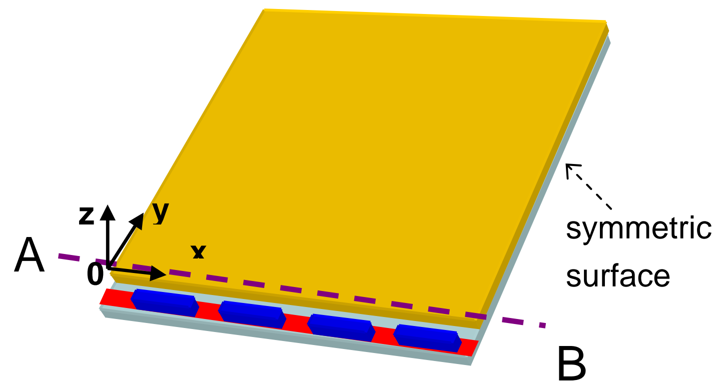


Figure 4.4 (a) Warpage profile of upper glass plate along x-axis near COG packaging and (b) schematic illustration of LCD global model

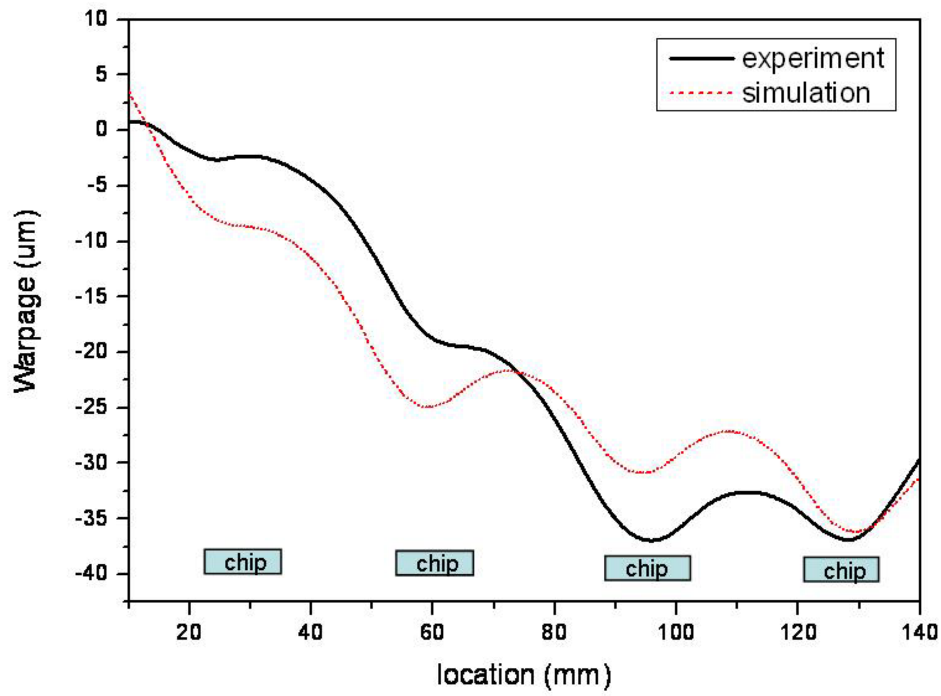
Next, the validity of simulation model was examined by comparing the data of experimental and simulation as shown in Figure 4.5(a). Based on the results, the simulation data matched well with the experimental measurement. The global warpage was about 38 μm in both data and the location of the localized warpage induced by COG packaging also matched well in experimental data and simulation data. Figure 4.5(a) – 4.5(f) showed the experimental and simulation warpage data of LCD panel in various conditions of different ACF bonding temperatures (180 °C, 170 °C and 160 °C) and thickness of glass substrate (0.3 mm and 0.5 mm). The warpage profiles from simulation in each case matched well with experimental surface topography in local warpage and global warpage. The difference of warpage profile between simulation and experimental data near the panel edge may arise from the pinning of polarizer attachment or glass substrate sealing in the LCD assembly. In contrast, perfect adhesion and little residual stress were assumed in our model.

The warpage induced by COG packaging was mainly caused by the thermal gradient and CTE mismatch in various components of LCD panel. In order to

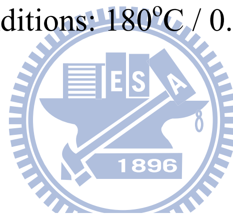
decrease the thermal gradient during the thermal bonding process, the simple and straightforward method was that decreasing the ACF bonding temperature. Once the ACF bonding temperature was decreased, the thermal gradient at the COG packaging region was decreased, and then the warpage was decreased simultaneously.

For 0.3 mm glass substrate, the warpage data of various ACF bonding temperature from 180 ^{o}C, 170 ^{o}C to 160 ^{o}C was illustrated in Figure 4.5(a)-(c). The global warpage from ~38 μm for 180 ^{o}C/0.3 mm case decreased to ~30 μm and ~15 μm in the condition of 170 ^{o}C/0.3 mm and 160 ^{o}C/0.3 mm. Not only the global warpage decreased with the lowering ACF bonding temperature, but the localized warpage induced by bending of Si chips decreased. The same trend also observed in the cases of 0.5 mm glass substrate as Figure 4.5(d)-(f) shown. However, the extent of the warpage in the cases of 0.5 mm glass substrate was all smaller than those cases of 0.3 mm glass substrate. Since the thicker glass substrate had ability to absorb more stress than thinner one did, the global warpage and localized warpage then both decreased.

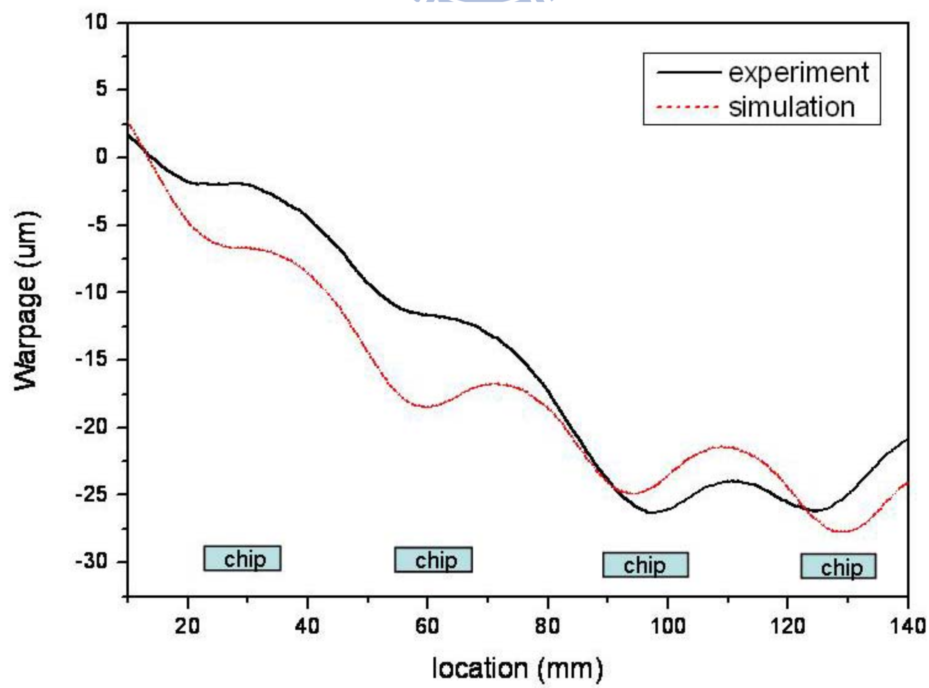
(a)



Conditions: 180°C / 0.3mm

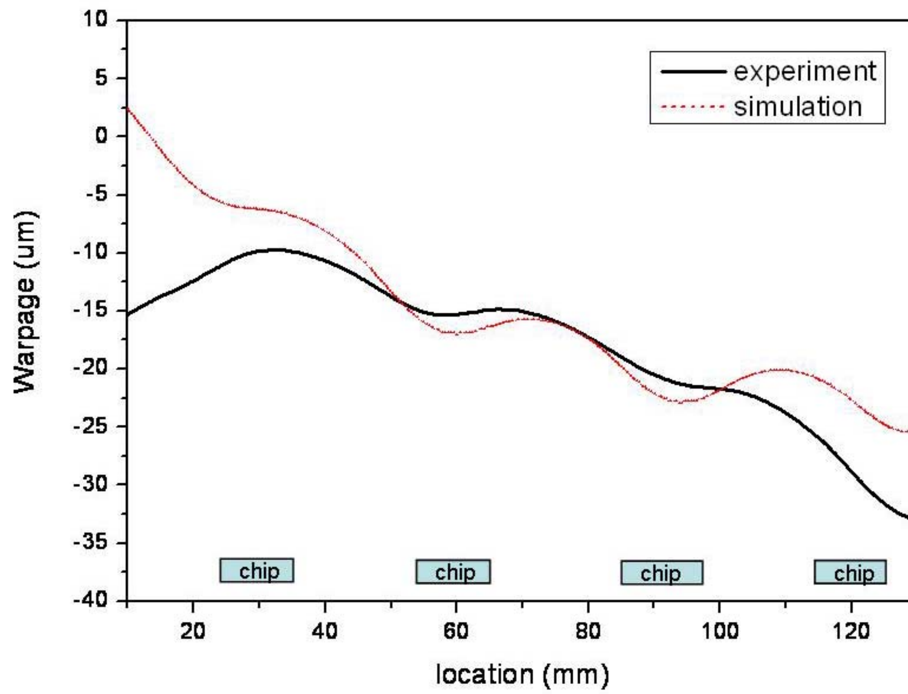


(b)

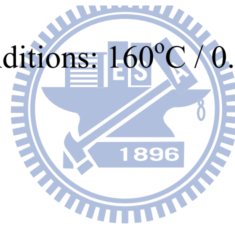


Conditions: 170°C / 0.3mm

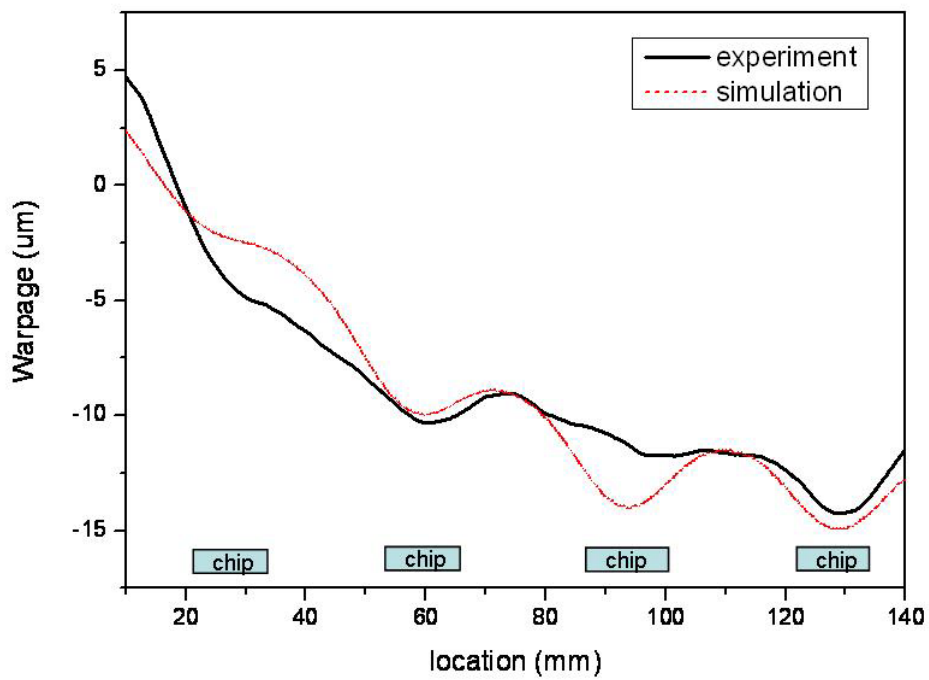
(c)



Conditions: 160°C / 0.3mm

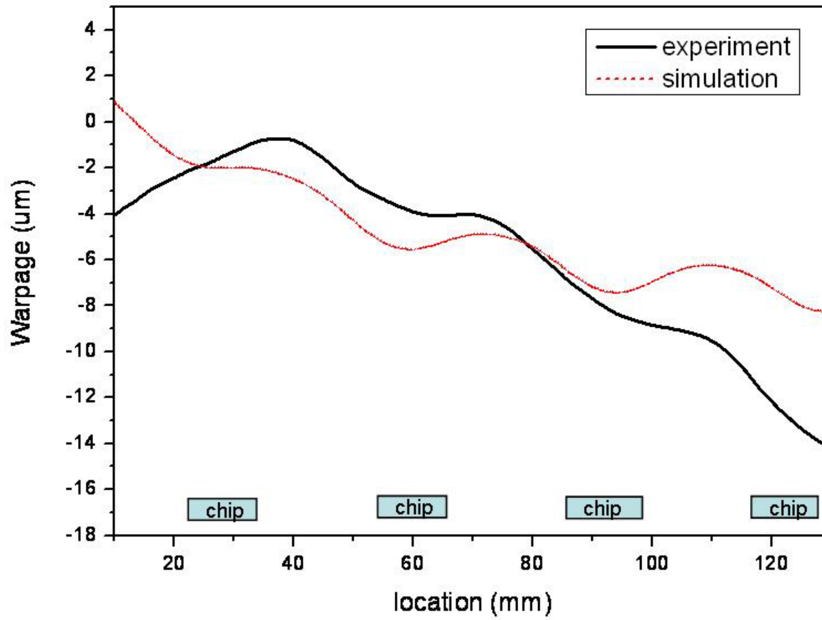


(d)



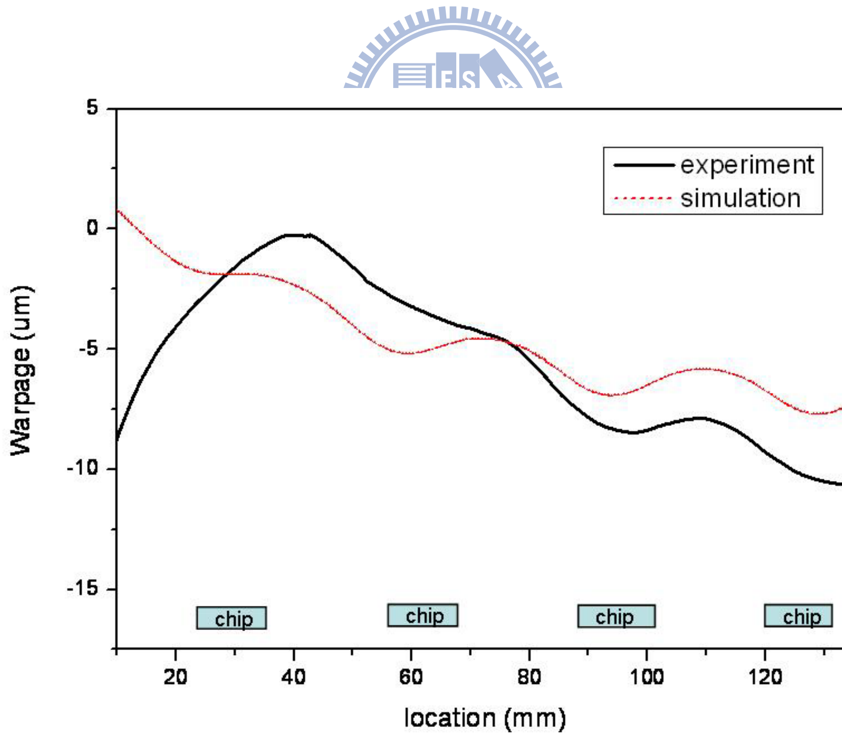
Conditions: 180°C / 0.5mm

(e)



Conditions: 170°C / 0.5mm

(f)



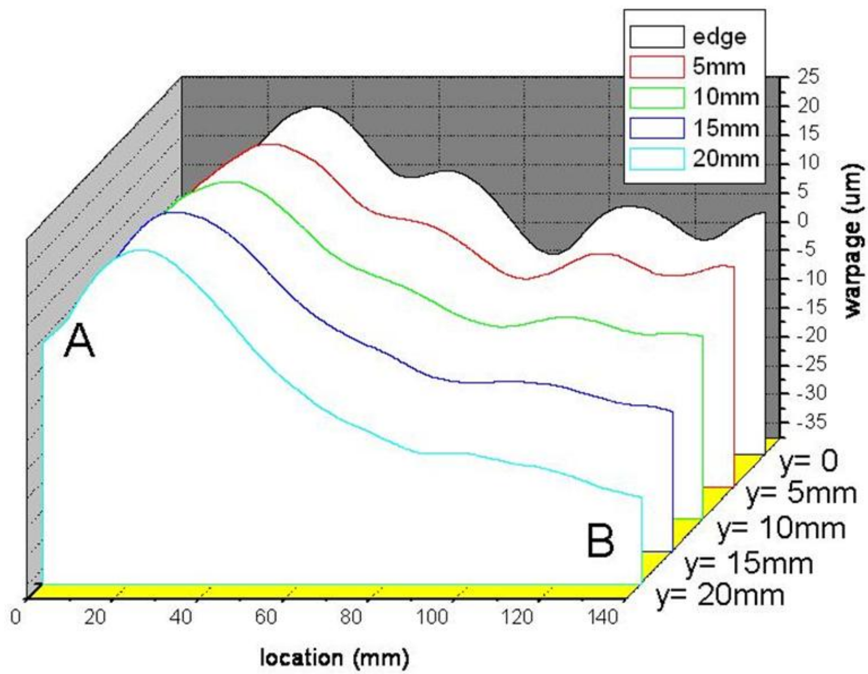
Conditions: 160°C / 0.5mm

Figure 4.5 Plots of experimental data vs. simulation data for various conditions: (a) 180 °C/0.3 mm, (b) 170 °C/0.3 mm, (c) 160 °C/0.3 mm, (d) 180 °C/0.5 mm, (e) 180 °C/0.5 mm and (f) 180 °C/0.5 mm

Next, same contour measurement (along x-axis) was repeated from edge (y=0) to y=20 mm as shown in Figure 4.6(a). The global warpage (along x-axis) remained about the same (~38 μm), while localized warpage decreased at planes away from edge up to y=20 mm. It was observed that the wave-like deformation or localized warpage became indistinguishable at 15-20 mm from the edge in the y-direction, which coincided with the boundary of the light leakage region shown in Figure 2.16 from note book monitor. These results suggested that the light leakage phenomenon was related to the localized warpage which was caused by the bending of the silicon chips after COG packaging. The warpage profiles from simulation in Figure 4.6(b) matched well with experimental surface topography in local warpage and global warpage.

Figure 4.7 shows the warpage of 160°C/0.3mm case with repeated measurement from edge (y=0) to y=16 mm. The localized warpage also became indistinguishable when moved away from the edge. In this condition, however, the localized warpage disappeared at 12 mm-16 mm, where was closer to the edge than the condition of 180°C/0.3mm. Figure 4.8 shows the photos of LCD panels with 160 °C and 180 °C ACF bonding temperature in lighted-up state. The light leakage phenomenon was improved when the ACF bonding temperature was decreased from 180 °C to 160 °C. The region of light leakage at 160°C bonding temperature was smaller and the half-moon-like shape became not as clear as in the condition of 180°C bonding temperature. Again, these results suggested that the localized warpage had strong relationship with the light leakage phenomenon.

(a)



(b)

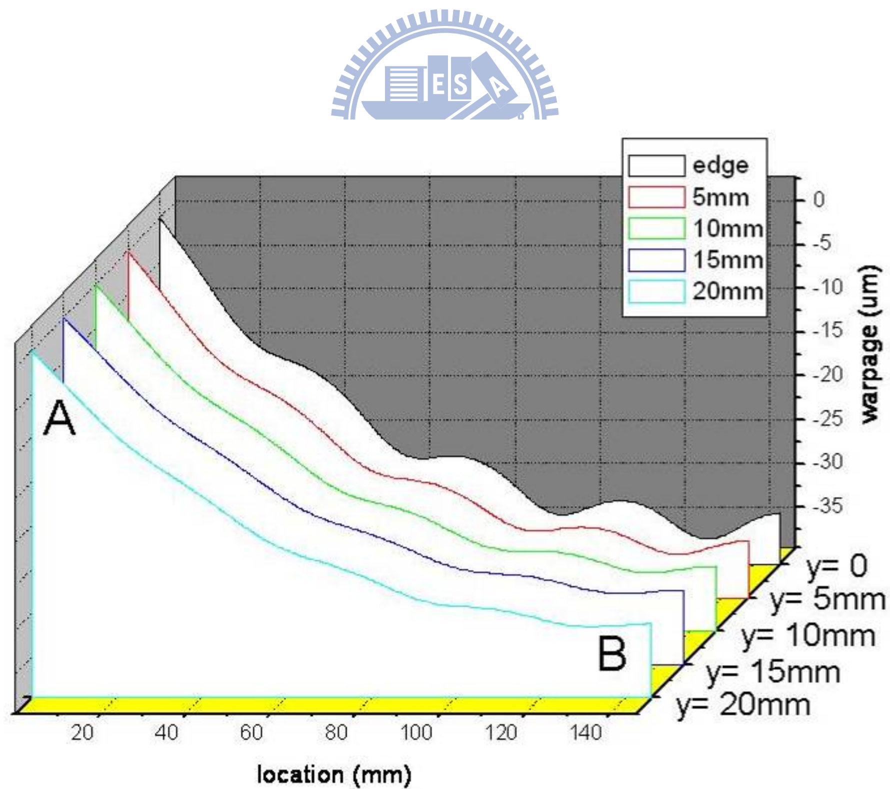


Figure 4.6 Surface topography of 180°C / 0.3mm TFT-LCD panel which described in (a) experimental measurements and (b) computer simulation

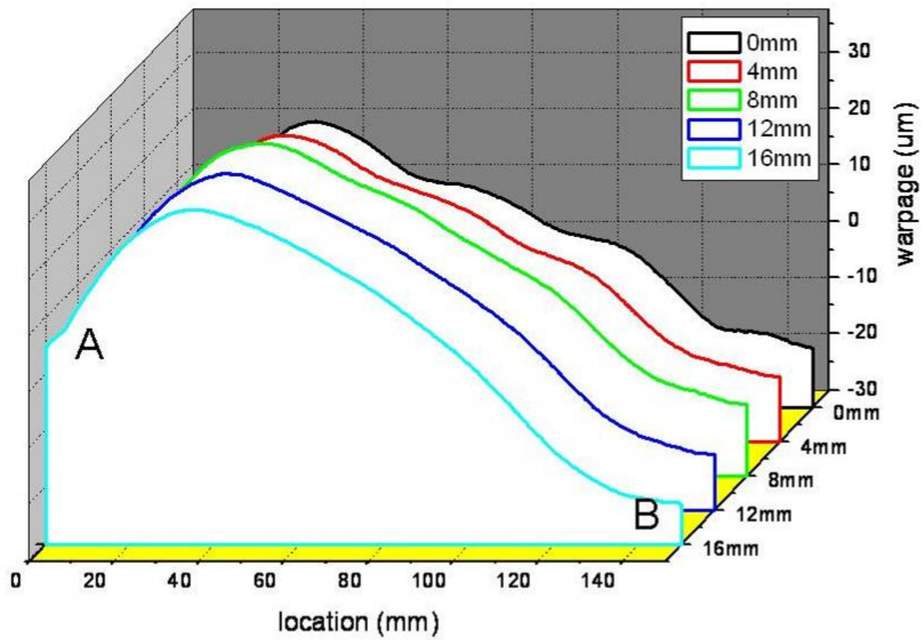


Figure 4.7 Surface topography of 160°C / 0.3mm TFT-LCD panel which described in experimental measurements

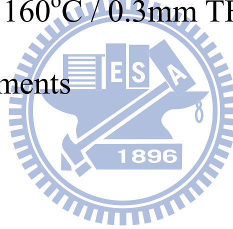


Figure 4.8 Pictures of light leakage phenomenon with ACF bonding temperature at (a) 180°C and (b) 160°C

4.3 Stress Analysis

To this point, the 3D FEA model has been validated by experimental data related to local warpage and COG-induced light leakage phenomena using different ACF bonding temperature (180 ^{o}C, 170 ^{o}C, or 160 ^{o}C) and thickness of glass substrate (0.3 mm and 0.5 mm). To further explore other root-cause for Mura defects, the 3D FEA model was employed to examine the stress distribution near the edge of upper glass, next to the row of Si chips used in the COG package. Figure 4.9 shows the first principal stress distribution in the upper glass plate along the plane, y=0. The local maximum stress occurred close to the edge of Si chip. This agreed with the upward warpage between two Si chips. Also, the stress was lower near edge, illustrated by point A, because the edge of panel (x=0) was free to move. The local maximum stress increased from 2 MPa corresponding to the outmost chip (near A) to ~4 MPa corresponding to central chip (near B).

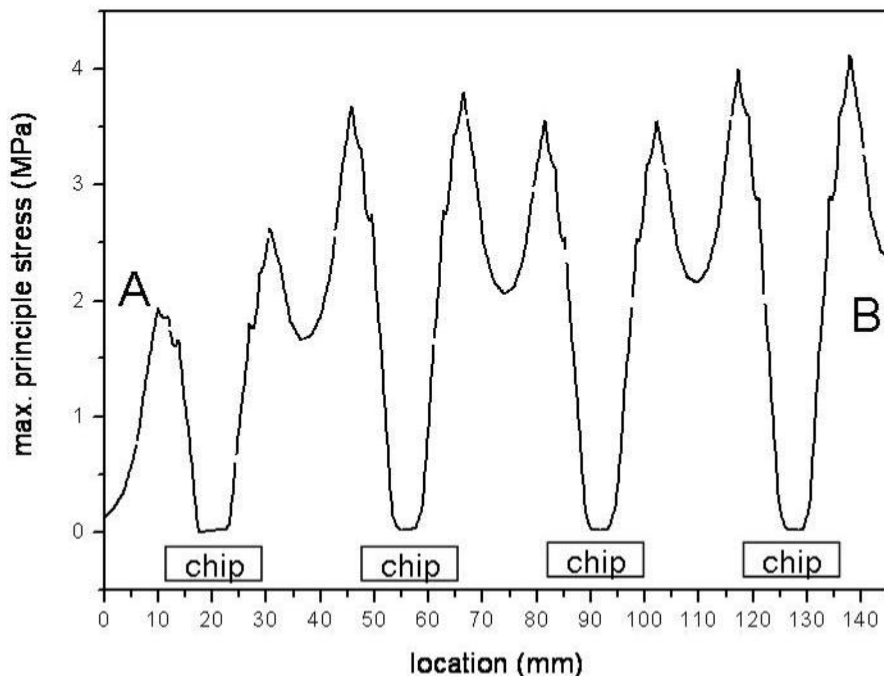


Figure 4.9 The stress distribution curve along the bottom edge of the glass substrate

Figure 4.10 shows the maximum principle stress distribution contour (top-view) in the upper glass of LCD. The stress concentrated in the regions between two Si chips and its stress level decreased at location moving away from the edge. The stress became negligible at location 15-20 mm from the edge. Excellent correlation between stress contour (Figure 4.10) and light leak phenomenon (Figure 2.2) was found in the relative location, region and severity of light leakage. These results suggested that the light leakage Mura defect was indeed related to the non-uniform stress distribution field.

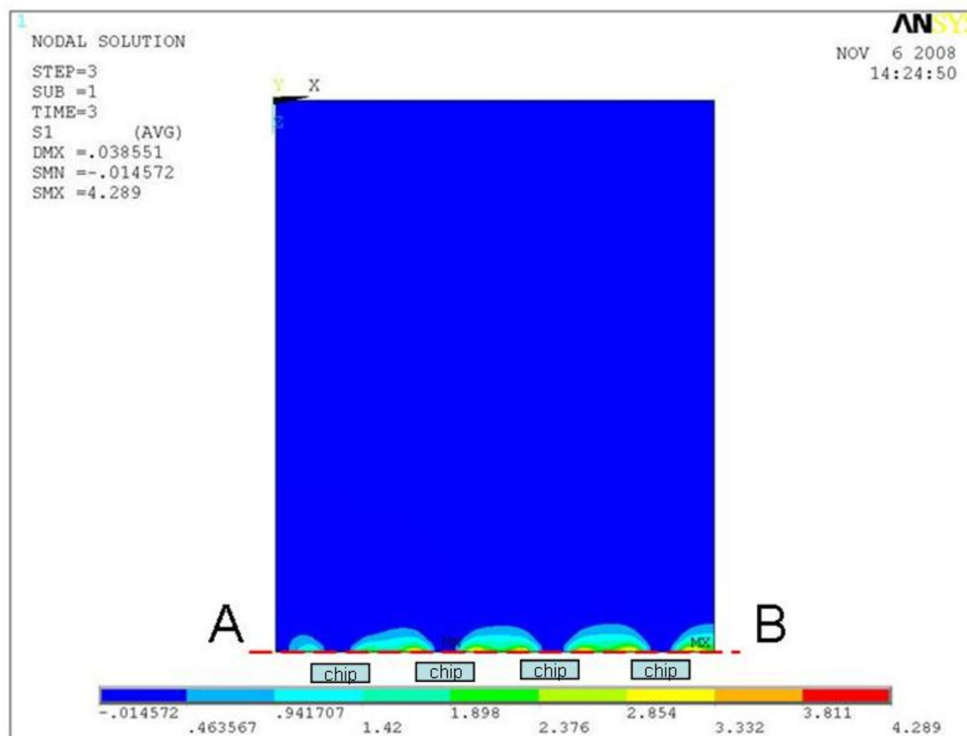


Figure 4.10 Maximum principle stress distribution contour in LCD glass substrate in 1/2 symmetric model

4.4 The Root-Causes of COG-Induced Mura in LCD

In previous discussion, the warpage and the stress induced by the COG package have been examined. The results showed excellent correlation among localized warpage, stress distribution and light leakage Mura defect. Prior to further in-depth investigation and understanding of the Mura defect, the root-causes of the Mura were discussed and proposed in the following section.

4.4.1 Liquid Crystal Molecules

The average direction of preferred orientation of the liquid crystal molecules was usually characterized by a unit vector $\vec{n}$ which was called the director. Since the preferred direction of the long axes of the liquid crystal molecules existed, many material properties such as dielectric constant, refractive index and elastic constant exhibited anisotropy, and they affected the electro-optical behavior of a liquid crystal display.

The director of the liquid crystal molecules can be easily affected by external factors such as stress field and electrical field. It had been reported that liquid crystal molecules showed a reorientation of the director when a mechanical stress was applied perpendicular to the original director axis [46,47]. In section 2.1.2, the working principle of TN mode TFT-LCD had been introduced. The director of twisted nematic (TN) liquid crystal was determined by the electrical field applied between two substrates. However, the director of the liquid crystal molecules could be reoriented when the liquid crystal molecules underwent a large enough external stress field with large localized warpage induced by COG packaging as shown by Figure 4.11. The light may leak from the regions where the effect of stress surpasses the effect of electrical field in the ON state (appearing dark in LCD).

Based on the simulation results, the first principal stress was ~2-4 MPa as

compared to the elastic modulus of typical liquid crystal material of 10^{-11}-10^{-12} N. It is to be noticed that the 2-4 MPa was relatively small in conventional structure-mechanical problems. However, compared to the extremely small value of elastic modulus of liquid crystal molecules, the stress induced by COG package was large enough to affect the motion of liquid crystal material. Besides, the liquid crystal molecules under external stress field tended to direct to the axis of maximum stress [46] which was exactly the type of stress chosen to examine Mura defect in this study.

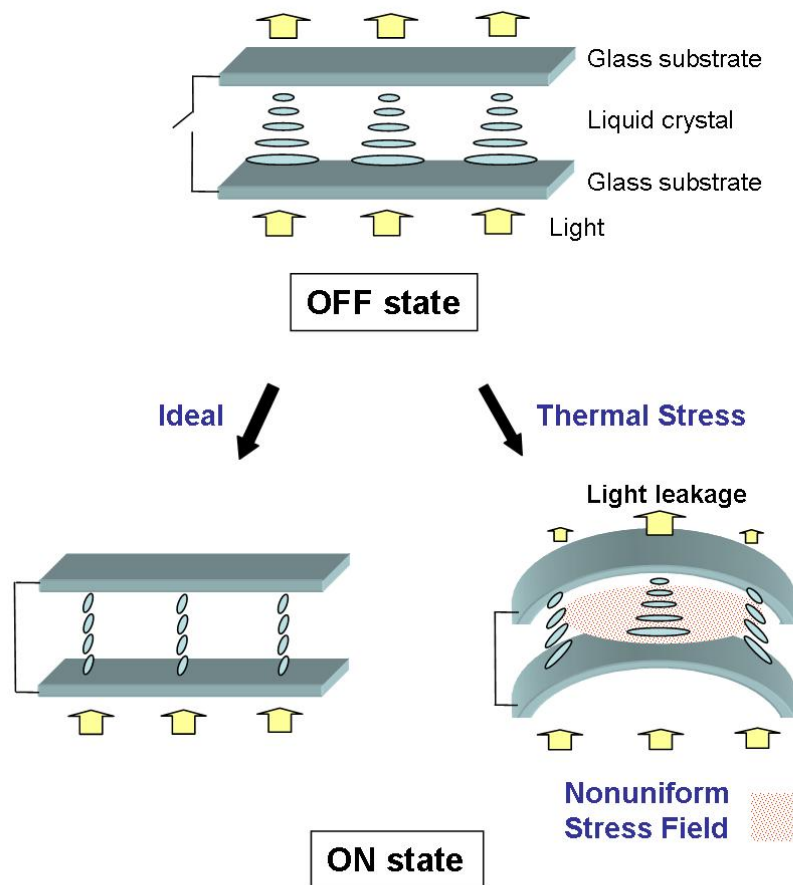


Figure 4.11 Schematic illustration of root-cause of Mura by liquid crystal reorientation

4.4.2 Alignment Layer

The alignment layer was a key component in the TFT-LCDs for arranging liquid crystal in a uniform direction and inducing a tilt in the liquid crystal molecules near the surface [15]. After COG packaging, the warped glass substrate may cause severe deformation and nonunifrom stress that affected the alignment rubbing layer and also led to light leakage. In section 2.1.1, the alignment mechanism was briefly described and discussed. The molecules model suggested that the polymer chain and (or) substituents near the surface were aligned by the unidirectional rubbing. Thus, the surface polymer chain can interact with liquid crystal surface in a unidirectional alignment.

Moreover, there has been reported that the near-surface mobility of polymer was higher than the bulk, leading to an ease of molecular reorientation [48,49]. Based on these researches, the surface polymer chains were easily reoriented when underwent an external stress as shown in Figure 4.12. Thus, the director of the liquid crystal molecules near the alignment layer redirected with the polymer chains by the anchoring energy. Besides, another study reported that the significant lowering of glass transition temperature in ultra-thin polymer film than bulk materials [50], indicating that the polymer chains at the alignment layer surface became easier to reorientate under the thermal bonding circumstances. Once the thermal-induced stress redirected the polymer chains on the surface of alignment layer, the direction of liquid crystal molecules attached to the alignment layer was also re-orientated. Thus, the light may leak when TFT-LCDs was in the dark state.

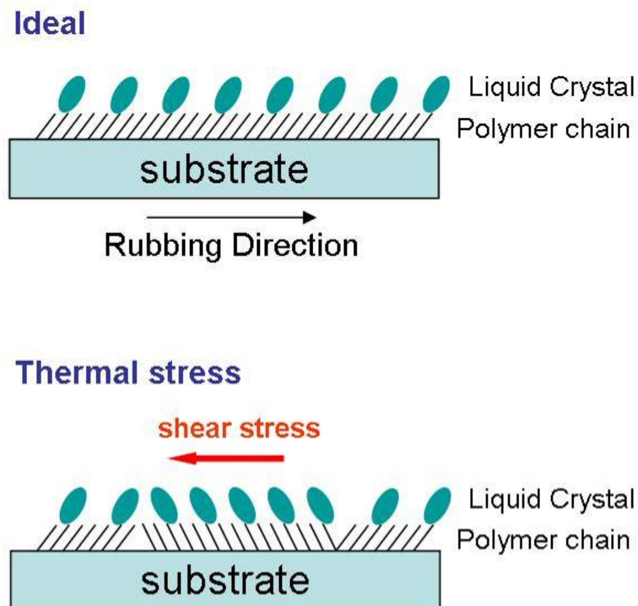
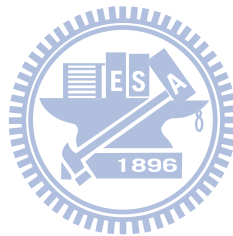


Figure 4.12 Schematic illustration of polymer chains near surface reorientated due to shear stress



4.5 Effect of the Thickness of Glass Substrate, Properties of ACF and Layout of Si chips on Mura Defects

4.5.1 Thickness of Glass Substrate

The effects of thickness of glass substrate on warpage were first studied. Figure 4.13 showed the plots of maximum localized warpage and maximum first principal stress (at the central of panel) as a function of thickness of glass substrate (from 0.5 mm to 0.2mm) with ACF under 180°C bonding temperature. The case of 0.5mm glass substrate had the smallest value of maximum localized warpage and stress, 4.23 μm and 2.48 MPa. The maximum localized warpage and stress in the case of 0.3 mm glass substrate was 7.64 μm and 4.29 MPa and dramatically increased to 12.88 μm and 5.76 MPa in the case of 0.2mm glass substrate. The warpage and stress increased when the thickness of glass substrate decreased. Figure 4.14 shows the phtographs of lighted-up LCD panels using 0.3 mm and 0.5 mm glass substrate with 180 ^{o}C bonding temperature. The level of light leakage defect in 0.5 mm case was less than in 0.3 mm one.

As aforementioned, light leakage phenomenon was improved resulting from the decreasing localized warpage and stress. When the thickness of glass substrate increased from 0.2 mm to 0.3 mm and 0.5 mm, the warpage decreased rapidly. Unfortunately, the thickness of glass substrate moved towards thinner plates in the business trend. Therefore, other approaches such as material properties of ACF, processing technology, or layout of Si chips must be developed to solve the light leakage problem.

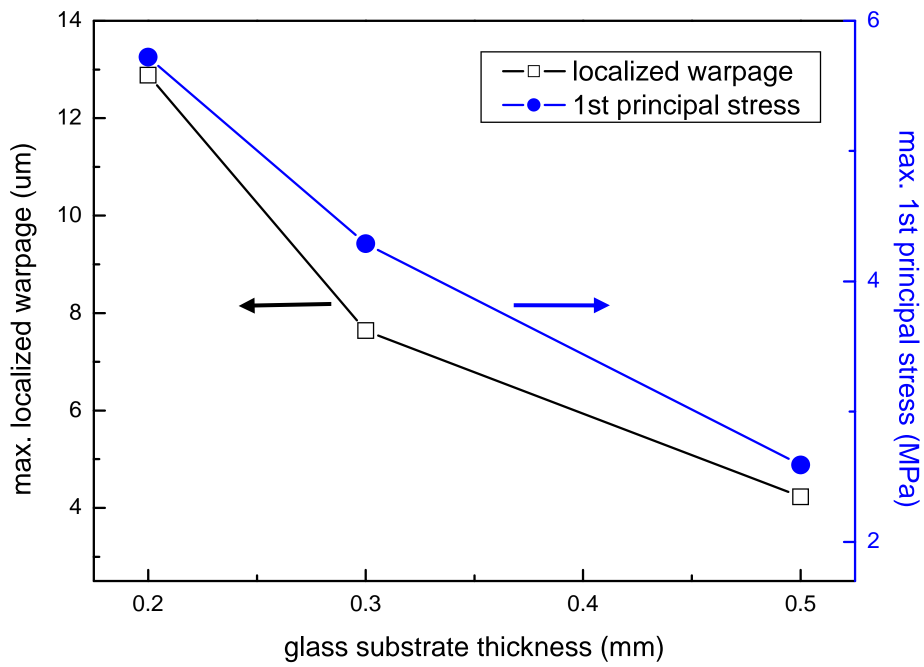
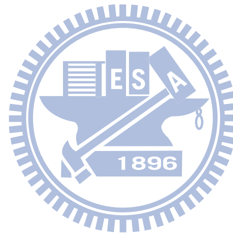


Figure 4.13 Maximum localized warpage and first principal stress as a function of thickness of glass substrate with 180°C ACF bonding temperature



(a) Thickness of glass substrate: 0.3 mm

(b) Thickness of glass substrate: 0.5 mm

Figure 4.14 Photographs of lighted-up LCD panel with (a) 0.3 mm, and (b) 0.5 mm glass substrate with 180°C ACF bonding temperature

4.5.2 Bonding Temperature, Modulus and CTE of ACF

The required temperature for mounting the Si chips on glass substrate was decided by the cure characteristic of ACF adhesive. Although the issue of pot life of ACF may arise when using the improvement curing agent, the ACF with lower bonding temperature was better for improving Mura defect due to the less degree of thermal gradient resulting in decreasing warpage and stress. Figure 4.15 shows the plot of the maximum localized warpage and maximum first principal stress as a function of the ACF bonding temperature using 0.3 mm glass substrate. The maximum localized warpage/stress in the case of 180 ^{o}C ACF bonding temperature was 7.64 μm/4.29 MPa and then decreased with the reduction of the ACF bonding temperature. The maximum localized warpage/stress was 5.08 μm/2.91 MPa and 4.12 μm/2.35 MPa in the case of 160 ^{o}C and 140 ^{o}C ACF bonding temperature, respectively. The light leakage phenomenon was improved with decreasing the ACF bonding temperature as confirmed by the photographs of the LCD lighted-up experiment as shown in Figure 4.16. The severity level and region of light leakage were reduced with the lower ACF bonding temperature. Although there is a lack of experimental result for 140 ^{o}C case, the much improvement or elimination of light leakage can be prediceted by our simulation results.

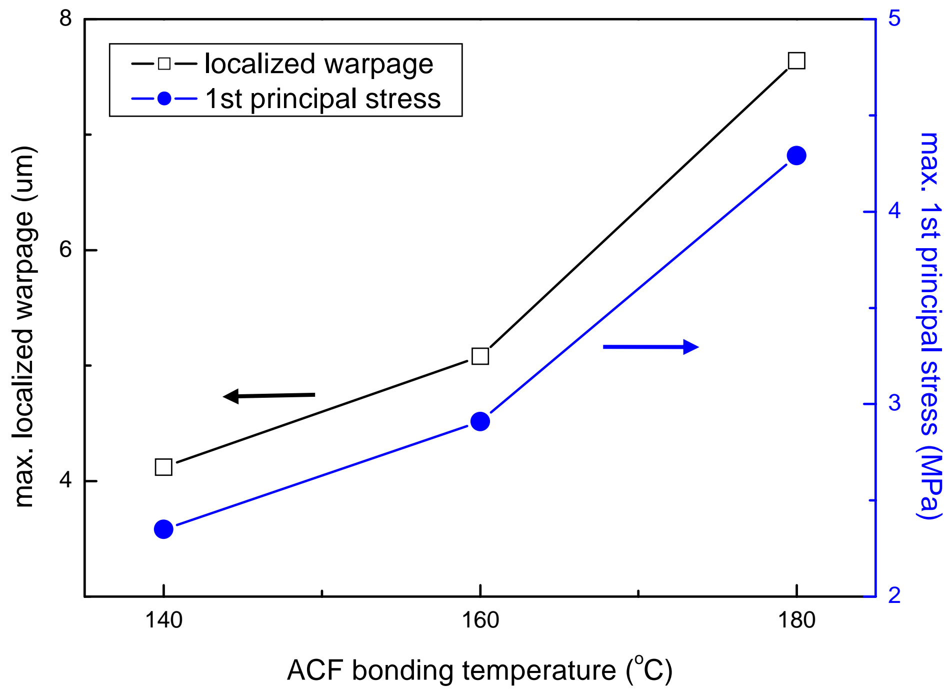


Figure 4.15 A plot of maximum localized warpage and first principal stress as a function of ACF bonding temperature using 0.3mm glass substrate

(a) ACF bonding temperature: 180°C

(b) ACF bonding temperature: 160°C

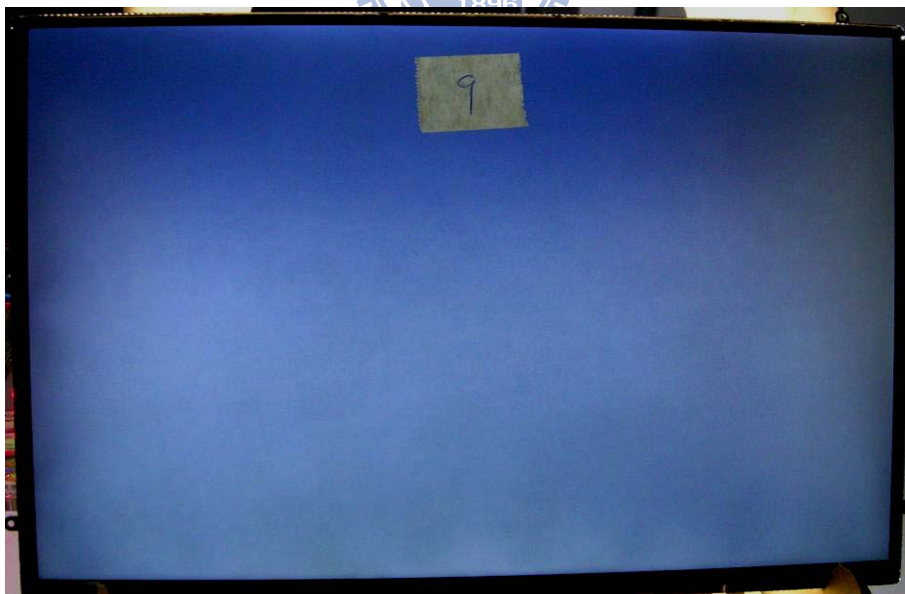


Figure 4.16 Photographs of lighted-up LCD panels with ACF bonding temperature at (a) 180 $^{\circ}$C and (b) 160 $^{\circ}$C using 0.3 mm glass substrate

In order to reduce the light leakage, improvement of the ACF properties was also an available method other than decreased the ACF bonding temperature. The two main mechanical properties of ACF adhesive, Young's modulus (E) and coefficient of thermal expansion (CTE), were investigated to realize their effects on the localized warpage and light leakage phenomenon.

The ACF adhesive in COG assembly played the role of connection between Si chips and glass plates, and buffer layer which can absorb the thermal-induced stress of Si chips and glass substrate. Figure 4.17 shows the plot of maximum localized warpage and maximum first principal stress as a function of ACF modulus with conditions of 180 ^{o}C/0.3 mm. The original modulus of ACF was 1.6 GPa under room temperature. When the modulus of ACF increased to 2.9 GPa (80% increased), the warpage/stress increased from 7.64 μm/4.29 MPa to 8.34 μm/4.75 MPa. On the other hand, the warpage decreased to 6.25 μm/3.23 MPa when modulus of ACF decreased to 0.3 GPa (80% decreased). Based on the results, ACF adhesive with low modulus indicated that it was softer to be a better buffer layer, which could absorb more COG-induce stress. Thus, the warpage and stress were decreased with reduction of the ACF modulus. The photographs of lighted-up LCD panels with original modulus ACF and low modulus ACF were shown in Figure 4.18. The half-moon-shaped light leakage phenomenon with low modulus ACF adhesive became indistinguishable compared to panel using the original modulus ACF adhesive. The region of light leakage also shrank.

As for the CTE of the ACF, it had little effect on the warpage and stress since its variety of thermal-induced stress could be ignored when compared to the stress of the Si chips and the glass substrate. This was because of the small thickness ratio of ACF to the COG assembly (less than 5%) and its very low modulus compared to the Si chips and glass substrate. Thus, during the thermal bonding process, the

thermal-induced stress of ACF adhesive could be ignored as compared to the stress induced by Si chips and glass substrate. Changing the CTE of the ACF adhesive had no effect on the warpage and stress, indicating that the light leakage Mura defect can not be solved by this parameter.

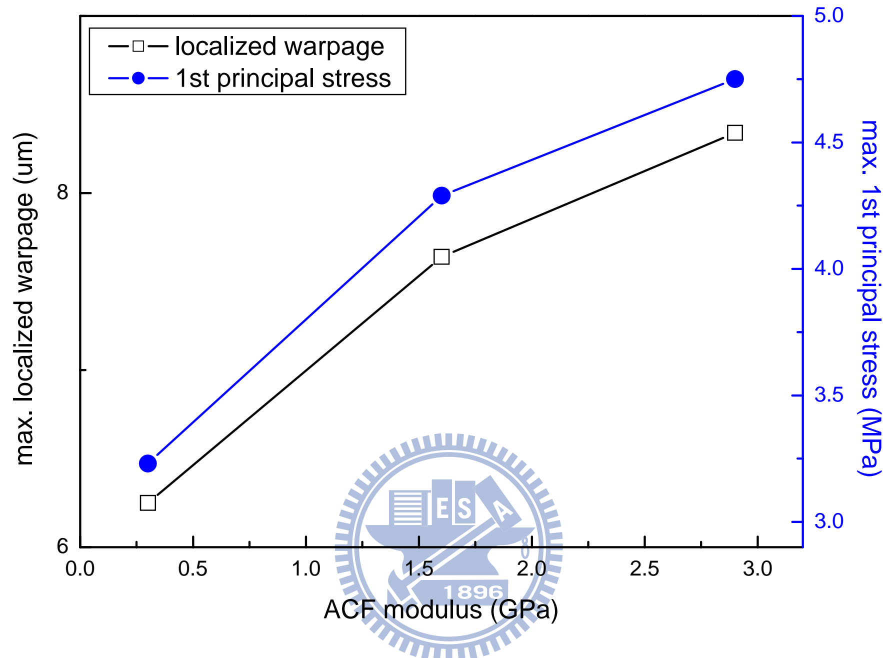


Figure 4.17 A plot of maximum localized warpage and maximum first principal stress as a function of ACF modulus with conditions of 180 ^{o}C / 0.3 mm

(a) Original modulus

(watermark)

(b)Low modulus

Figure 4.18 Photographs of lighted-up LCD panels with (a) original ACF modulus and (b) lower modulus under conditions of 180 ^{o}C/0.3 mm

So far, the effect of the COG packaging manufacturing parameters such as thickness of glass substrate, process temperature and the two mechanical properties of ACF on light leakage Mura has been studied. Next, the warpage reduction of these parameters was examined to realize which one had more effectiveness. Table 4.1 summarized the localized warpage data from the outside to central of the LCD panel by simulation. The maximum first principal stress data was omitted due to it had a positive correlation with the maximum localized warpage. Condition A represented the original case, and B, C, D meant the low ACF bonding temperature at 160 ^{o}C, low ACF modulus and low bonding temperature/modulus at the same time, respectively. Conditions E-H turned a change of the thickness of glass substrate from 0.3 mm into 0.5 mm. The data in each case had the same trend, the localized warpage decreased from central to outside of the panel. Preliminary observation of these data showed that decreasing ACF bonding temperature was more effective than decreasing the ACF modulus on reduction of localized warpage.

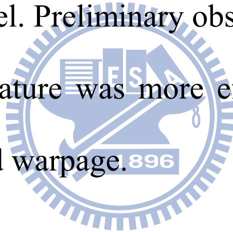


Table 4.1 Localized warpage from outside to central of LCD panel in different sample conditions

Sample Conditions	Localized Warpage (μm)			
	Outside → Central			
A: 180°C / 0.3mm / 1.6GPa	3.12	4.54	6.17	7.64
B: 160°C / 0.3mm / 1.6GPa	2.82	3.39	4.12	5.08
C: 180°C / 0.3mm / 0.3 GPa	3.03	4.26	5.14	6.25
D: 160°C / 0.3mm / 0.3GPa	2.57	3.13	3.57	4.34
E: 180°C / 0.5mm / 1.6GPa	2.52	3.08	3.49	4.23
F: 160°C / 0.5mm / 1.6GPa	2.28	2.64	3.08	3.42
G: 180°C / 0.5mm / 0.3GPa	2.33	2.72	3.19	3.68
H: 160°C / 0.5mm / 0.3GPa	2.26	2.54	2.76	3.09

The maximum localized warpage in various conditions as shown in Figure 4.19. The relationship between thickness of glass and ACF bonding temperature with fixed ACF modulus was first studied. When the ACF modulus was fixed at 1.6 GPa and the ACF bonding temperature decreased from the 180 ^{o}C to 160 ^{o}C with 0.3 mm glass substrate (sample A and B), the maximum localized warpage decreased 34% while only decreased 19% associated with 0.5mm glass substrate (sample E and F). Similarly, when the ACF modulus fixed at 0.3 GPa, the maximum localized warpage decreased 30% (sample C and D) while only decreased 16% associated with 0.5 mm glass substrate (sample G and H). From the results, the effect of the ACF bonding temperature on the localized warpage was amplified when the thickness of glass substrate decreased.

Next, the relationships between thickness of glass substrate and the ACF modulus on maximum localized warpage with fixed ACF bonding temperature were examined. When the ACF bonding temperature was fixed at 180°C and the modulus of ACF decreased from 1.6 GPa to 0.3 GPa, the maximum localized warpage decrease 18% with 0.3 mm glass substrate (sample A and C) while decreased 13% associated with 0.5 mm glass substrate (sample E and G). When the ACF bonding temperature was fixed at 160°C, the maximum localized warpage decrease 15% with 0.3 mm glass substrate (sample B and D) while decreased 10% with 0.5 mm glass substrate (sample F and H). Again, the effect of the ACF modulus on localized warpage was amplified with decreasing thickness.

Although the effect of both ACF modulus and thickness of glass substrate was amplified when thickness of glass substrate was decreased, the effect of the ACF modulus was less than the ACF bonding temperature. Considering the LCD development that the glass substrate must become thinner, the ACF bonding temperature would be the one of the critical factors for improving the light leakage

defect.

On the other hand, compared to the original case A, a 33%, 18%, 45% reduction in warpage was found in condition B, C and E, respectively. Based on the powered, lighted-up TFT-LCD, the level of light leakage Mura defect of these cases could be visually seen from the photographs illustrated in Figure 4.14, 4.16 and 4.18. The Mura became severe when glass thickness was decreased from 0.5 mm to 0.3 mm. Mura defect can be effectively improved by decreasing ACF bonding temperature and modulus. In the condition D, a 43% decrease in localized warpage and a 41% drop in the stress level were found from simulation, implying that light leakage resulted from thinning glass substrate can be eliminated or improved.

Key results are sum up as follow,

1. Decreasing ACF bonding temperature and ACF modulus helped eliminating Mura which appeared when thickness of glass substrate was thinned down from 0.5 mm to 0.3 mm.
2. When the thickness of glass substrate was decreased from 0.5 mm to 0.3 mm, the effect of ACF bonding temperature and ACF modulus on localized was warpage amplified, especially the ACF bonding temperature.
3. ACF bonding temperature was the more important factor than modulus of ACF for improving Mura.

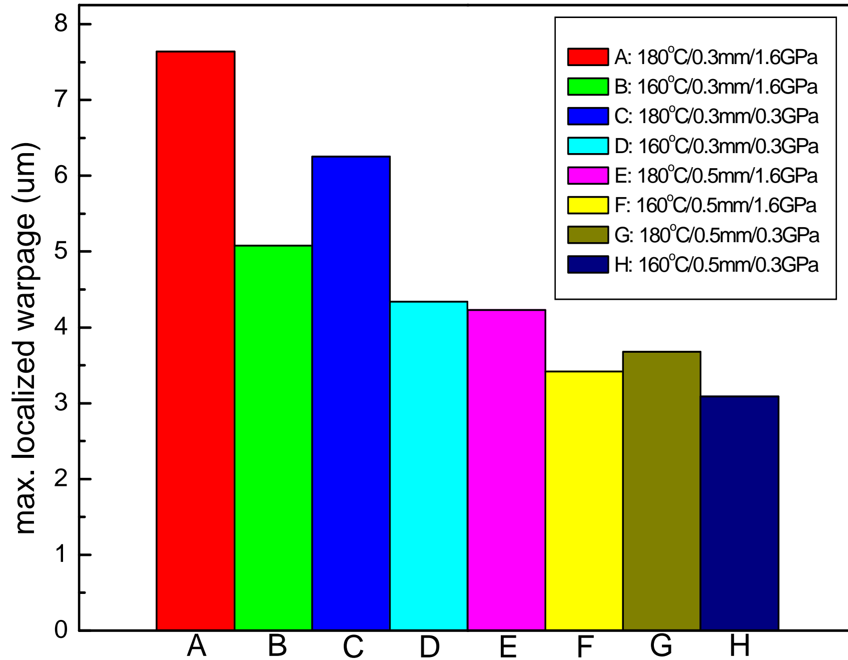


Figure 4. 19 The maximum localized warpage for different conditions

4.5.3 Dimensions and Arrangement of Si chips

From the previous discussions, the priority of improving or eliminating the light leakage Mura defect was to reduce the localized warpage and stress. Besides the aforementioned methods to reduce the warpage such as decreasing ACF bonding temperature and using low modulus ACF, other approaches were proposed in this section. The warpage and stress in COG packaging were resulted from the bending of the Si chips. Therefore, Changing the dimensions and arrangement of Si chips may be the solutions which were useful and feasible to improve the light leakage Mura.

Decreasing the length, width and height of the Si chips can all reduce the localized warpage as shown in Figure 4.20. The maximum localized warpage was reduced 85%, 73% and 21% with 60% shrinkage of height, length and width, respectively. Based on the results, the shrinkage of chip's length and height (*i.e.* thickness) can both effectively reduce localized warpage, suggesting that the Mura defect can be reduced effectively. In addition, small dimensions of Si chips had

advantages that it can solve the reliability problems about the bumps crack and delamination problem.

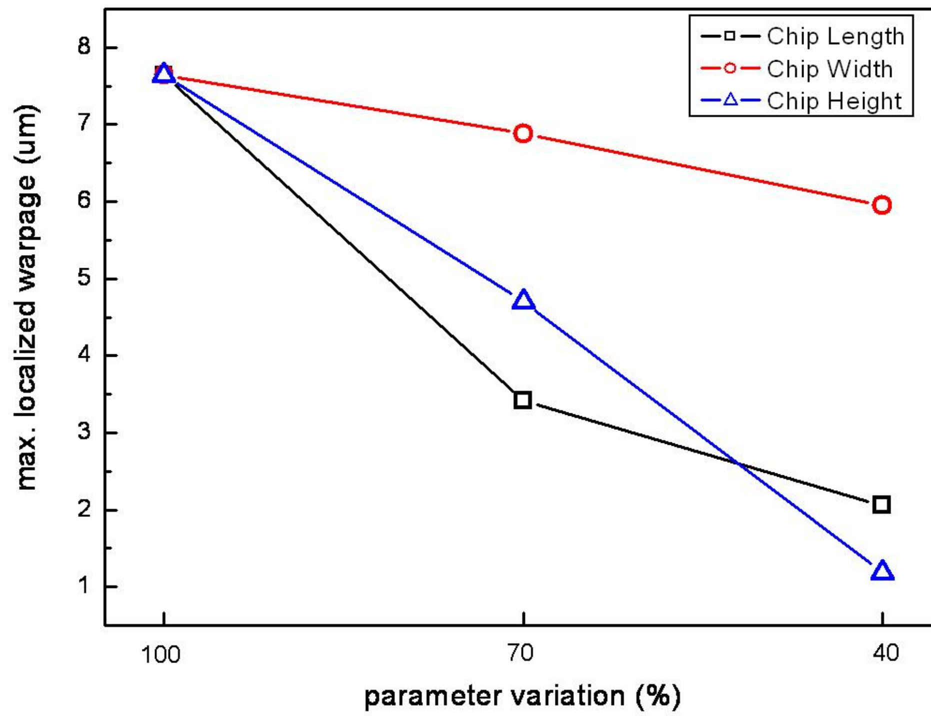


Figure 4.20 The maximum localized warpage as a function of dimensions of Si chip

It had to be noticed that when dimensions of Si chips shrank 60%, the height of Si chips had the biggest effect. Surprisingly, the length of chip turned into the most efficient parameter when the dimensions of the Si chip had only 30% shrinkage. There was a linear relationship between maximum localized warpage and the shrinkage of chip's width/height. However, the non-linear variation showed with the shrinkage of the chip's length. The space between two adjacent Si chips may explain this phenomenon.

Fig. 4.21 shows the stress distribution profile between two chips at the edge (y=0 plane) for different shrinking percentage of chip's length. The maximum stress was formed by the upward bending at Si chip's edge. When the two Si chips were close, namely the chip's length were not shrunk yet (original case), the upward bending strength was enhanced by each other, the stress between two chips was ~2 MPa. In contrast, after 30% shrinkage of Si chip's length, the space between the chips was enlarged, and the stress between chips decreased rapidly to ~0.8 MPa. The localized warpage decreased dramatically due to the enhancement of the upward bending of chips disappeared when the increased separation between two adjacent chips. When the dimensions of Si chips kept shrinking (60% shrinkage), the stress between chips was less than 0.5 MPa. Thus, the effect of the chip's length was smaller than the chip's height.

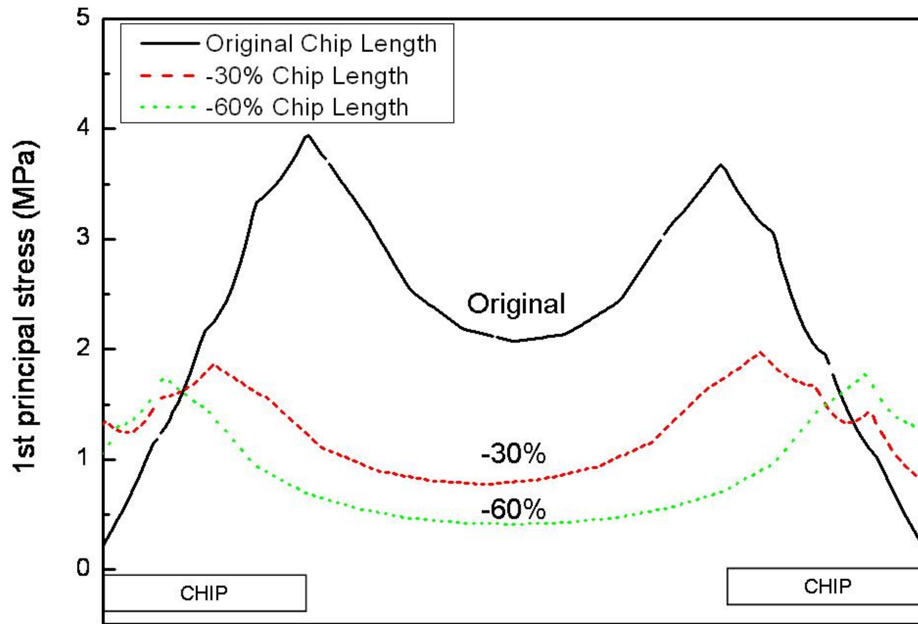


Figure 4. 21 Stress distribution profile between two adjacent chips at the edge (y=0 plane) for different shrinking percentage of chip's length

Another approach was the placement or location of the Si chips. The Si chips were mounted on the bottom glass substrate and had a little distance away from the upper glass in the original case. To investigate the effect of the displacement of the Si chips, the change of the localized warpage was examined as shown in Figure 4.22. Due to the restrict region for attaching Si chips onto bottom glass substrate, the placement of chips was set at 0.5 mm from the edge of upper glass. Next, the Si chip was moved away from upper glass or towards upper glass, as represented by +0.5 mm and -0.5 mm, respectively. The results indicated that the +0.5 mm case had better chance to improve light leakage due to its lower localized warpage. It was relatively straightforward; the effect of the Si chip's bending was weakened when the chips moved away from the upper glass.

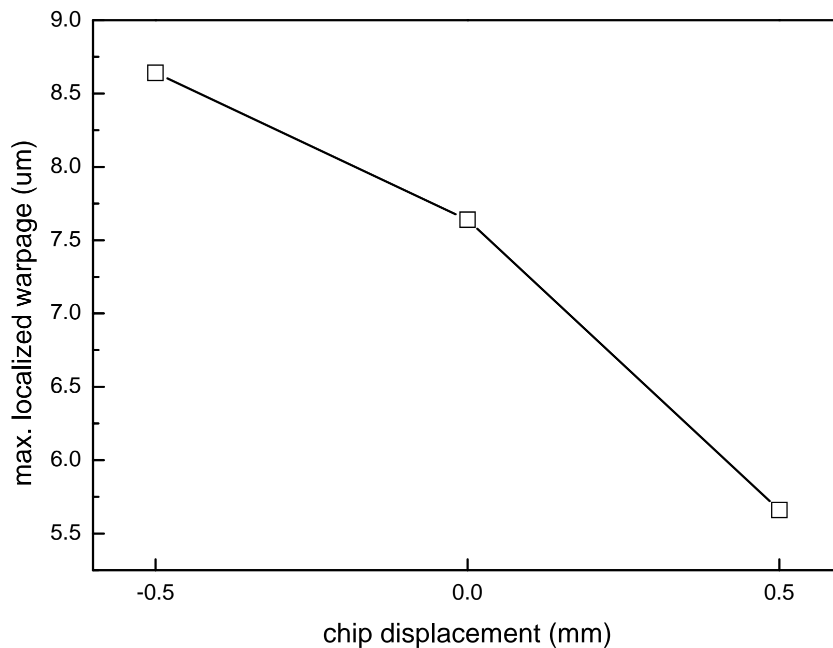


Figure 4. 22 The maximum localized warpage as a function of Si chips placement

In the semiconductor industry, flip-chip technology had the problem about the thermal-induced warpage as well. The engineers came up with an idea that put a stiffener ring to constrain the warpage through a heat sink on the back side of Si die [51,52]. An idea similar to the method used in flip-chip was proposed that an appropriate dummy material was chosen to be placed between Si chips as Figure 4.23 shown, and this method was named “dummification”. Dummification was similar to the method used in flip-chip, dummy materials was placed between Si chips to constrain the upward bending of the Si chips. The CTE and the modulus of the dummy materials had to be considered carefully for obtaining better result.

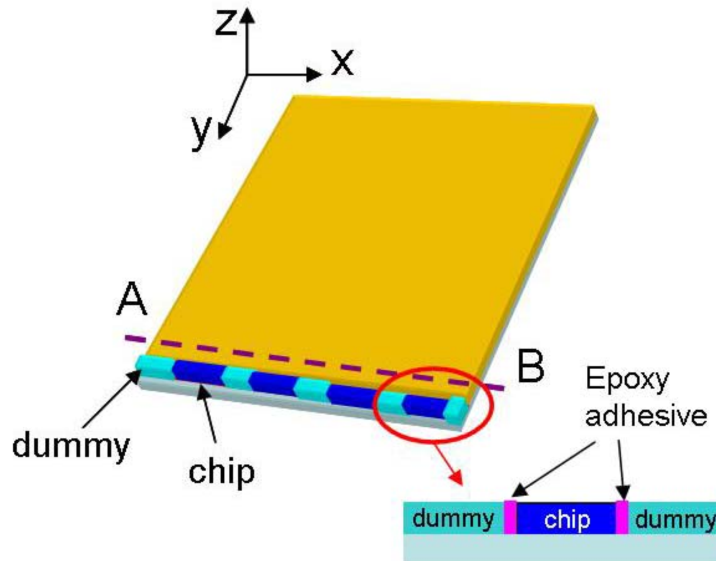


Figure 4.23 Schematic illustration of dummification

In the first stage, glass was chosen as the dummy material due to the same properties as the substrate. Figure 4.24(a) and 4.24(b) showed the simulation results of warpage profile and stress distribution. Although the trend of localized warpage and stress distribution were similar to those in the original case, a 62% decrease in localized warpage and about 60% decrease in maximum principal stress were found. The higher stress accumulated at the edge in the dummification case was caused by the continuity of the Si chips and dummy material, from which the stress can not be released and was transmitted from central to edge. However, the accumulated stress of the dummification was still less than the stress at the central of the original case. In addition, based on the previous results, the light leakage was improved when ACF bonding temperature decrease from 180 ^{o}C to 160 ^{o}C with a localized warpage 34% drop (from 7.64 μm to 5.08 μm). In the case of dummification using glass, a 62% drop (from 7.64 μm to 2.84 μm) in localized warpage implied that light leakage may be eliminated. Therefore, the warpage of the substrate can be effectively constrained without producing additional stress.

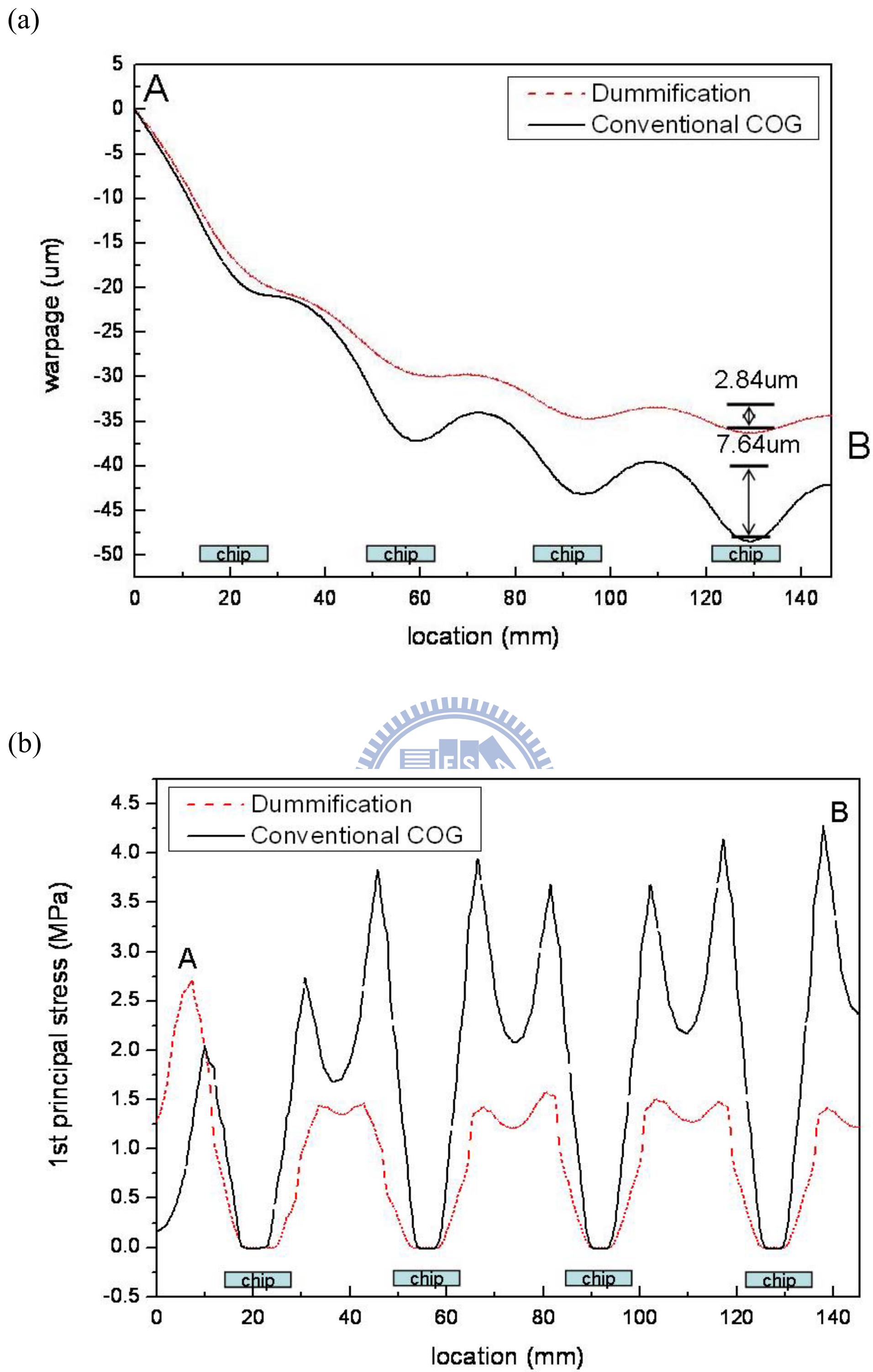
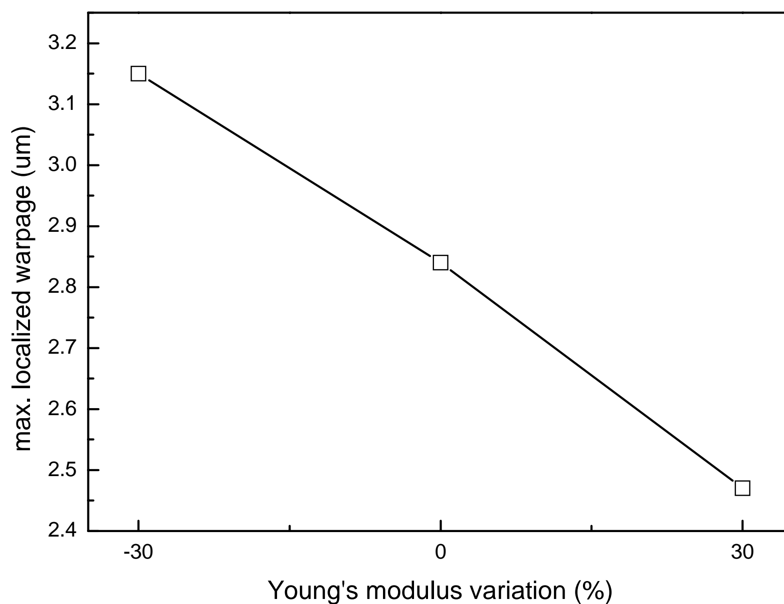


Figure 4. 24 Simulation results of (a) warpage profile and (b) stress distribution for conventional COG and dummification

As mentioned previously, the properties of the dummy materials played an important role in this method. Dummy material with optimized properties may provide a better result in reducing localized warpage and stress. Figure 4.25(a) and 4.25(b) shows the impact of different modulus and CTE of dummy materials on the maximum localized warpage. The dummy material with higher modulus showed lower localized warpage as illustrated Figure 4.25(a). It was because of the high modulus material had better ability to constrain the bending of the Si chips. As for the CTE of dummy material, the localized warpage was raised no matter the CTE of dummy material was increased or decreased as shown in Figure 4.25(b). It could be attributed to the CTE mismatch between dummy materials and glass substrate. Therefore, using the dummy materials with CTE close to the substrate helped reducing extra stress and warpage. Based on the simulation results, dummy materials with higher modulus and proper CTE, which was close to the CTE of glass substrate, can reduce the localized warpage and stress effectively.

(a)



(b)

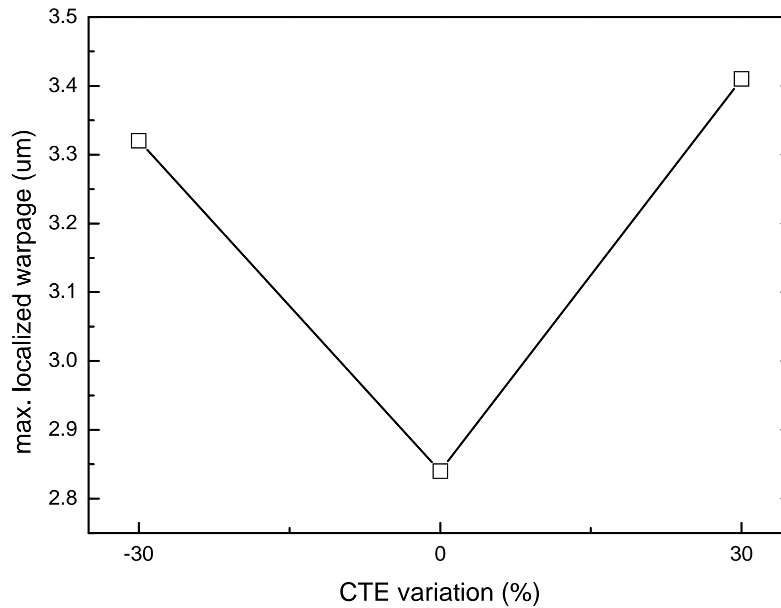


Figure 4.25 The maximum localized warpage comparison of different (a) Young's modulus and (b) CTE of dummy material

Based on the simulation results, changing arrangement and dimensions of Si chips can solve Mura problem. In semiconductor industry development, the line width of devices has been kept shrinking, for example, 32nm, which meant the dimensions of chips could drop down. Therefore, the requirements of I/O density increasing and the Mura defect could be solved simultaneously. Besides, dummification had no additional procedure in the COG package. In brief, shrinkage of Si chips and dummification proved practical and cost-effective solutions for eliminating Mura defect.

4.6 Summary of Methods for Reducing Light Leakage Mura Defect

To this point, many methods for improving Mura defect had been discussed. These methods can be classified into two parts. One was related to the COG manufacturing processes and materials properties which manufacturers adopt to solve light leakage presently, including thickness of glass substrate and bonding temperature/modulus of ACF. The other one was the methods related to the dimensions and arrangement of Si chips. For improving light leakage, the main objective of all these methods was to reduce the localized warpage and stress distribution. Table 4.2 summarized the maximum localized warpage and maximum first principle stress corresponding to various conditions with 0.3 mm glass plates. The quantity sequence of maximum first principle stress was the same as the localized warpage, *i.e.* the larger localized warpage with the larger principal stress and vice versa.

Based on the results, the methods of decreasing bonding temperature and modulus of ACF can reduced 20%-30% warpage and stress, which can improve the light leakage Mura as confirmed by the photographs of lighted-up TFT-LCD panel. In contrast, varying layout of Si chips such as shrinking the height/length of Si chips and dummification can reduce 60%-80% warpage and stress, suggesting they were the useful methods to solve the light leakage Mura problem.

Table 4.1 Maximum localized warpage and first principle stress corresponding to specific conditions with 0.3mm glass substrate

Sample Conditions	Max. Localized Amplitude (μm)	1st Principal stress (MPa)
180°C/1.6GPa (Original case)	7.64	4.29
30% chip width reduction	6.88	3.55
180°C/0.3GPa	6.25	3.28
Chip location, +0.5mm	5.66	3.04
160°C/1.6GPa	5.08	2.91
30% chip height reduction	5.02	2.89
30% chip length reduction	3.41	1.94
dummification	2.84	1.48
60% chip length reduction	2.06	1.52
60% chip height reduction	1.18	0.79

Chapter 5 Conclusions

Light leakage Mura defect involving non-uniform brightness became severe for a 13" TFT-LCD using COG package with 8 IC drivers mounting on glass substrate directly, when the thickness of glass substrates decreased from 0.5 mm to 0.3 mm. The CTE mismatch in components of TFT-LCD (such as glass plates and Si chips) resulted in the warpage and non-uniform stress in the TFT-LCD after the thermal bonding process. To investigate the relationship among Mura, warpage and stress, a 3-D finite element analysis (FEA) model coupled with transient thermal analysis using ANSYS^{TM} has been established and validated by surface contour measurement tool using KOSAKA ET4000A.

Based on these results, excellent correlation between COG-induced Mura and localized warpage (or principal stress) has been found. The light leakage phenomenon was successfully related to the localized warpage and non-uniform maximum principle stress distribution. In addition, two possible root-causes for COG-induced Mura were proposed: (1) the director of liquid crystal was reorientated and (2) the polymer chains at the surface of alignment layer were redirected by stress.

The COG-induced warpage and stress were caused by the Si chips attachment process through ACF adhesion, due to the CTE mismatch between different materials. Thus, reducing the stress and localized warpage induced by COG packaging was critical for improving light leakage. Decreasing bonding temperature and modulus of ACF showed a 20-30% reduction of the warpage (or stress) and eliminated the Mura which appeared when thickness of glass decreased from 0.5 mm to 0.3 mm. Besides, the CTE of ACF had little effect on localized warpage and stress, and the effect of the ACF modulus was less than the ACF bonding temperature. By considering the LCD

development for light-weight LCD, the ACF bonding temperature would be the most important parameter when the glass substrate became thinner. This warrants new material design and chemistry to enable a lower thermal bonding temperature ACF material.

To improve Mura, increasing thickness of glass substrate, decreasing ACF bonding temperature and using low modulus ACF can decrease the localized warpage and stress. However, increasing glass substrate was opposite to the trend of modern LCD development. Most of LCD manufacturers currently reduced warpage by adjusting the properties of ACF which can be applied to a lower bonding temperature and low modulus.

In this study, other methods such as changing arrangement and dimensions of Si chips were proposed for solving Mura defect. According to the results, shrinking the chip's height/length could provide significantly reduction (60%-80% up) in localized warpage and stress from simulation. In addition, a novel method, dummification, was also proposed for improving Mura defect by placing an appropriate dummy material between two Si chips to constrain the thermal-induced warpage. Using glass as the dummy material, the localized warpage and stress can be reduced ~60%. As to other materials for dummification, materials with high modulus and proper CTE (close to the substrate's CTE) would be the better choice.

To summarize the methods for improving Mura, Figure 5.1 showed the plot of maximum localized warpage in various approaches. The methods of decreasing bonding temperature and modulus of ACF can reduced 20%-30% warpage and stress, which can improve the light leakage Mura as the experimental pictures shown, the methods of changing dimensions of Si chips (especially height and length) and dummification which can reduce 60-80% warpage and stress, indicating its great promise and potential to eliminate the light leakage Mura.

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