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高速與低偏壓砷化銦通道量子井場效電晶體在高頻及邏輯應用之研究

Study of High Speed and Low Voltage InAs-Channel Quantum Well Field Effect Transistors for RF and Logic Applications

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指導教授：張 翼 博士

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摘要

近年來無線電頻率特別是毫米波、次毫米波頻段的應用，已經對人類的日常生活產生重大的影響。其所應用的範圍包括有行動通訊、軍事國防、交通指引、雷達系統等；除此之外，其他一些仍在發展中的應用例如家園防護系統、醫藥分析、高解析度影像感測系統等，其研究也如火如荼的進行中。而尋找在高頻頻段下仍擁有極高增益、低雜訊的元件是這類應用的重要關鍵。由於三五族砷化銦鎵材料的高電子遷移率以及量子井場效電晶體優異的能帶設計，因此三五族砷化銦鎵通道量子井場效電晶體在這方面的應用展現極大潛力。

在此研究中，成功的製作了四十奈米閘極線寬的砷化銦通道量子井場效電晶體，並且透過先進的二次閘極蝕刻以及白金閘極掘入技術，使元件展現優異的高頻特性。此研究比較了在低操作偏壓下(V_{DS}=0.5V)使用此先進製程技術的砷化銦量子井場效電晶體與未使用此製程的元件，發現透過此兩先進製程步驟，元件展現較佳飽和電流、較低輸出電導、較小負截止電壓，以及較高的電流增益截止頻率和功率增益截止頻率(可分別達到440GHz以及190GHz)。除此之外，針對此元件進行雜訊品質的量測，發現即使在高頻64GHz下，其雜訊指標仍低於2.5分貝。由這些特性可以得知，四十奈米的砷化銦量子井

場效電晶體是適用於高增益、低雜訊以及低操作偏壓的高頻元件應用。

然而，由於砷化銦材料的窄能隙特性，衝擊離子化效應的現象很容易發生。在這份研究中，透過實驗數據的分析，具體地證實四十奈米砷化銦量子井場效電晶體的衝擊離子化效應，其中包括隨著施加偏壓劇烈上升的汲極電流以及在V_{DS}>1.0V時所觀察到的鐘型閘極漏電曲線，此外，還有包括在V_{DS}=1.0V時急遽上升的雜訊指標以及V_{DS}=1.0V時下降的電流增益等，都是衝擊離子化效應發生的明顯證據。雖然衝擊離子化現象破壞了元件的特性，然而只要選擇適當的操作偏壓，仍可得到相當優異的元件特色；例如當V_{DS}在相當低的0.5V時，其轉移電導即可達到1500 mS/mm，還有在高頻64GHz下，其雜訊指標仍低於3分貝，此外，在此研究中還發現，當施加的偏壓在衝擊離子化即將發生的電壓前，可得到663GHz極高的電流增益截止頻率。由以上分析可知，只要選擇適當的操作偏壓，四十奈米砷化銦量子井場效電晶體是相當適合於毫米波以及次毫米波元件應用的。

這份論文的最後，另外針對四十奈米砷化銦量子井場效電晶體於未來高速邏輯電晶體運用做評估，發現在低偏壓下(V_{DS}=0.5V)元件展現相當優異的邏輯特性，包括其汲極引致能障下降是相當低的50mV/V，而次臨界擺幅也是相當低的89mV/decade，此外，此元件的閘極延遲時間低於1.0psec，而與Si NMOSFET做比較，其閘極延遲時間也是較低的。而這些研究結果可以證實四十奈米砷化銦量子井場效電晶體是極有潛力作為未來後矽半導體世代高速邏輯電晶體的使用。

Study of High Speed and Low Voltage InAs-Channel Quantum Well Field Effect Transistors for RF and Logic Applications

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Abstract

Recently, wireless communication applications at millimeter wave band and sub-millimeter wave bands have gained a lot of momentum. The applications include wireless systems, cellular backbone, national weaponry, traffic guidance, radar systems, etc. Besides, emerging millimeter wave applications such as homeland security, medical diagnosis, and high-resolution image sensor are also in development rapidly. Therefore, development of the devices possessing both high frequency features and low noise characteristics is becoming urgent. High indium content InGaAs-based QWFETs are particularly promising because the excellent electrical properties of $In_xGa_{1-x}As$ material and the superior band-gap design of QWFET.

In this study, the 40 nm InAs QWFETs processed with advanced two-step recess and Pt gate sinking technologies for RF applications are fabricated. The developed 40 nm InAs QWFETs with these advanced processes exhibit better performance than the conventional InAs QWFETs at low applied voltage such as better current saturation, lower output conductance (*go*), smaller negative threshold-voltage (V_T), higher current-gain cut-off frequency (f_T) of 440 GHz and higher maximum oscillation frequency (f_{max}) of 190 GHz. Besides, the 40 nm InAs QWFETs with advanced processes also exhibit the minimum noise figure of lower than 2.5 dB up to 64 GHz when biased at V_{DS} of 0.5 V. The excellent

electronic performances indicate the developed 40 nm InAs QWFETs are suitable for high-gain, low noise and low voltage applications.

However, because of the narrow energy band-gap of InAs channel material, the impact ionization occurred easily. In this study, the investigation of impact ionization phenomena in 40 nm InAs QWFETs is presented. The evidences of the occurrence of impact ionization in InAs QWFETs include the high output conductance with the increase of V_{DS}, a hump in the curve of gate leakage current at V_{DS} higher than 1.0 V, the drastically increase of minimum noise figure at V_{DS} of 1.0 V, and the reduction of f_T at V_{DS} of 1.0 V. Although the impact ionization degrades the performance of the devices, the excellent characteristics can still be achieved with optimal bias selection. The devices show transconductance over 1500 mS/mm at V_{DS} of 0.5 V. Besides, low noise figure of less than 3 dB with an associated gain of 7 dB up to 64 GHz at V_{DS} of 0.8 V are observed. And the extremely high f_T of 663 GHz can be obtained if the devices are biased near the occurrence of impact ionization. Therefore, with optimal bias conditions, InAs QWFETs can achieve tremendous high performance for high-speed sub-millimeter wave applications.

In addition to high frequency RF applications, the evaluations of 40 nm InAs QWFETs for high-speed logic applications have also been demonstrated in this study. The devices show outstanding logic performance in low applied voltage (V_{DS}=0.5 V). The drain induced barrier lowering (DIBL) is 50 mV/V, subthreshold swing (S) is 89 mV/decade, and intrinsic gate delay (CV/I_{ON}) is less than 1.0 psec. When comparing to the mature Si technology, the InAs QWFETs exhibit smaller gate delay time. Besides, InAs QWFETs show much higher I_{ON}/I_{OFF} performance than the most advanced InSb QWFETs. These results demonstrate that the 40 nm InAs QWFETs have great potential for future high-speed and low-voltage logic applications.

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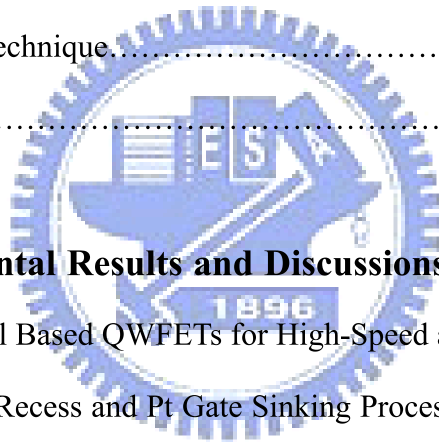

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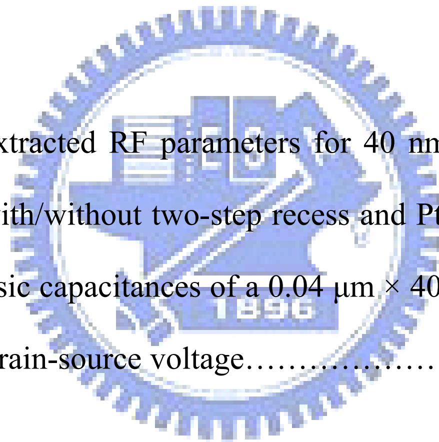

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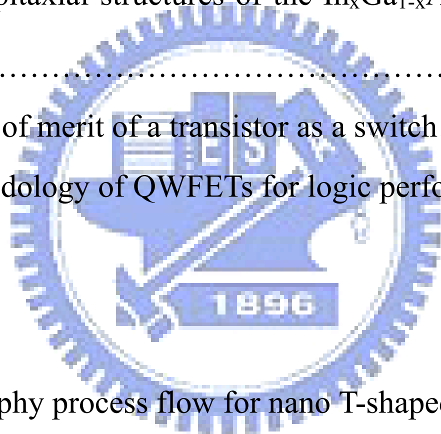

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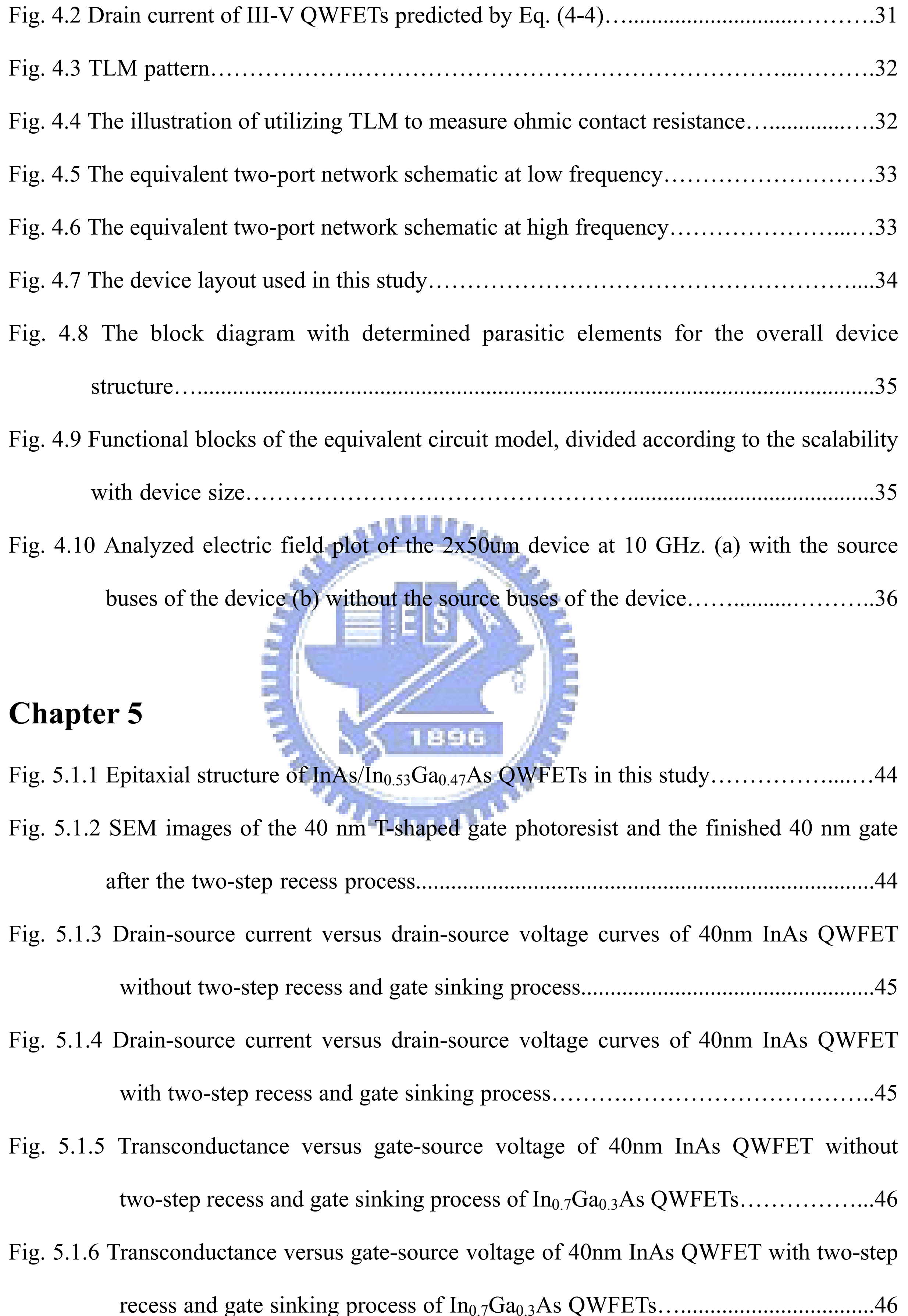

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Chapter 1

Introduction

1.1 General Background and Motivation

Continually scaling down Si-transistors is always the way to sustain Moore's law for last 30 years. But, it is expected that the dimension will reach about 10 nm by 2011 [1-1], which would be the ultimate limitation for Si CMOS. Fig. 1.1 [1-2, 1-3] lists the trend of transistor technology. Therefore, identifying a new logic device technology becomes an urgent issue. Candidates, which are often mentioned, are carbon nanotube (CNT) transistors, semiconductor nanowires and spintronics [1-4], etc. While the majority of the technologies mentioned above are still in the prototyping stage. On the contrary, III-V devices especially the Quantum Well Field Effect Transistors (QWFETs) gradually unfold potential because of their relatively mature technology and excellent performance. In general, III-V materials own high carrier transport properties like high electron mobility, high electron peak velocity, low electron effective mass, reasonable energy band-gap and high quantum confinement in the channel region. For InAs material used in this research, the bulk electron mobility is around 40000 $cm^2V^{-1}S^{-1}$ at room temperature. The detailed material properties of Si, Ge and III-V materials are listed in Table 1.1 [1-5]. Recently, many researches of III-V devices especially QWFETs with high indium concentration $In_xGa_{1-x}As$ channel materials exhibiting excellent DC and RF performance have been published [1-6, 1-7]. Endowed with these extraordinary electron transport properties, it seems imperative to evaluate the potential of $In_xGa_{1-x}As$ QWFETs for future beyond CMOS logic applications.

On the other hand, for future millimeter/sub-millimeter wave wireless-communication

applications including mobile radio systems and passive imaging systems etc., low noise amplifiers (LNAs) with extremely low noise figure, high gain and low DC power consumption are in highly demand. In order to meet the continuously growing requirement, the technique to improve devices performance becomes more and more rigid and challenging. However, $In_xGa_{1-x}As$ QWFETs also show great potential in this field. $In_xGa_{1-x}As$ QWFETs have demonstrated the best noise/gain performance and low power dissipation under ultra high frequency operation [1-8, 1-9]. Therefore, using $In_xGa_{1-x}As$ QWFETs for future high-speed millimeter wave wireless-communication applications are the most promising. Furthermore, with the further improvement of $In_xGa_{1-x}As$ QWFETs in frequency dependent performance, the applications expanding the radio spectrum resources to sub-millimeter wave (300 GHz - 3 THz) frequency region for new generation of military, telecommunications and radio astronomy applications are also worth expecting.

In this study, in order to exhibit the excellent performance of InAs QWFETs in high-speed, low-noise, low-power RF and logic applications, several approaches have been adopted. These efforts include the applications of exquisite electron beam lithography technique for 40 nm gate length, advanced two-step recess fabrication, platinum (Pt) gate sinking process, and other precise process adjustments. As a result of the good electronic transport properties of InAs materials, terrific band-gap engineering design of QWFET and advanced fabrication process, the InAs QWFETs in this study exhibit excellent DC, RF, noise and logic performance, which makes them feasible for future high-speed, low-voltage digital as well as high frequency millimeter/sub-millimeter wave applications.

1.2 Outline of this Thesis

This thesis focuses on the study of RF and logic evaluation of 40 nm InAs channel QWFETs.

In chapters 2, the overview including the basic mechanism and literature survey of III-V QWFETs is described. The detailed fabricating processes of the InAs QWFETs are introduced in chapter 3. In chapter 4, the fundamentals of electrical DC and RF characteristics of the device are described.

The experimental results and discussions are shown in chapter 5 and which are divided into three parts. The first part discusses the effect of advanced two-step recess process and Pt gate sinking process on 40 nm InAs QWFETs for RF application. Due to the narrow energy gap feature of InAs material, the impact ionization phenomena is easily occurred. So in the second part, the impact ionization phenomena of InAs QWFETs are studied and the optimum bias conditions for RF operation are also discussed. Beside the application of InAs QWFETs in high frequency millimeter-wave region, the logic characteristics of InAs QWFETs are also evaluated. In the third part of discussion, the important figures of merit relevant to logic such as gate delay, I_{ON}/I_{OFF}, DIBL, and S of the InAs-channel QWFETs are studied.

Finally, the conclusion of the thesis is given in chapter 6. The 40 nm InAs QWFETs exhibit great potential both in low-voltage, high-speed, low-noise RF applications as well as high-performance logic applications.

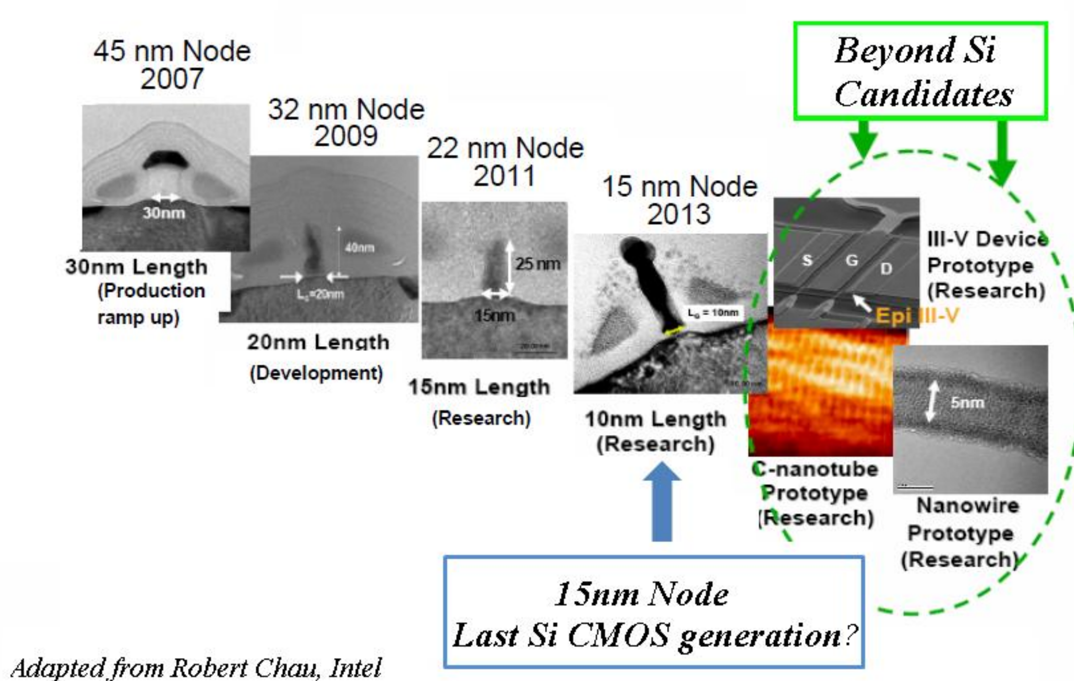


Fig. 1.1 The trend of transistor technology.

	Si	Ge	GaAs	InP	InAs	InSb
electron mob. (cm^2/Vs)	1600	3900	9200	5400	40000	77000
electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0. 916	m_t: 0.082 m_l: 1.467	0.067	0.082	0.023	0.014
hole mob. (cm^2/Vs)	430	1900	400	200	500	850
Hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	m_{HH}: 0.45 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.12	m_{HH}: 0.57 m_{LH}: 0.35	m_{HH}: 0.44 m_{LH}: 0.016
band gap (eV)	1.12	0.66	1.42	1.34	0.36	0.17
permittivity	11.8	16	12	12.6	14.8	17

Table 1.1 Physical properties of electron and hole of Si, Ge, and main III-V semiconductors.

Chapter 2

Overview of III-V Quantum-Well Field-Effect Transistors (QWFETs)

2.1 The Theory of III-V QWFETs

Quantum-well field-effect transistor (QWFET) or called High electron mobility transistor (HEMT) is one of the most mature III-V semiconductor transistors. The first demonstration of this device was made by Fujitsu Lab. in 1980 [2-1]. Fig. 2.1 represents a cross-sectional view of a conventional QWFET structure. The epitaxial layers of the QWFET structure are designed to form two-dimension electron gas (2-DEG) in the channel layer. The explanation of 2-DEG formation by energy band diagram of $In_xAl_{1-x}As/In_xGa_{1-x}As$ Metamorphic HEMT is shown in Fig. 2.2 [2-2]. When the small electron affinity (χ) and high energy band-gap (E_g) $In_xAl_{1-x}As$ material connects to the large electron affinity (χ) and low energy band-gap (E_g) $In_xGa_{1-x}As$ material, due to the Fermi-level (E_f) of these two materials must reach the horizontal balance and χ as well as E_g must remind the same value for each materials, there will generate the discontinuity of conduction band (E_c) in the junction. This discontinuity will cause partial E_c of $In_xGa_{1-x}As$ below the E_f so the mass electrons will accumulate in this 2-DEG quantum well. These electrons move fast in 2-DEG because they were accumulated in intrinsic and high electron mobility $In_xGa_{1-x}As$ material channel. As a result of the terrific band-gap engineering design of QWFETs, the QWFETs can exhibit superior carrier transport characteristics. For the past few years, GaAs-based MHEMTs or InP-based HEMTs with remarkable device performance in high speed applications have been published frequently.

2.2 The Structure of III-V QWFETs

In general, the epitaxial layers of the $In_xGa_{1-x}As$-channel QWFETs were grown by molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD) on InP/GaAs substrates, and the common expitaxial structures of the $In_xGa_{1-x}As$-channel QWFETs for high frequency application are shown in Fig. 3.1.

As Fig. 2.3 shown, the structure layers from bottom to top are composed of a $In_xAl_{1-x}As$ metamorphic buffer layer, a InGaAs-based channel layer optionally combining with sub-channel, a $In_{0.52}Al_{0.48}As$ spacer layer, a δ-doped carrier supply layer, a $In_{0.52}Al_{0.48}As$ barrier layer, a InP etching stop layer and a highly Si-doped $In_xGa_{1-x}As$ cap layer.

The $In_xAl_{1-x}As$ metamorphic buffer layer is used to release the lattice mismatch between $In_xGa_{1-x}As$ channel and GaAs/InP substrate. Therefore, the high indium content (50%-100%) of the $In_xGa_{1-x}As$ channel layer can be achieved in spite of the large lattice mismatch between the active channel layer and the substrate. The adhesion of $In_xGa_{1-x}As$ sub-channels could enhance the electron confinement in the thin and low energy band-gap main channel layer and further improve the electron transport properties [2-3]. The $In_{0.52}Al_{0.48}As$ spacer layer is applied to form heterostructure interface with InGaAs-based channel so that the band diagram discontinuity occurred, and the 2-DEG formed. A δ-doped layer with Si doping concentration could provide extra carriers to the channel layer. And an InP layer can provide a good gate recess etching stop layer as well as a good surface passivation of $In_xAl_{1-x}As$ layer to avoid kink effect and reduce the hot-electron surface damage [2-4]. Besides, with the use of the InP etching stop layer, the lateral recess length (Lr) can be easily controlled and RF performance can be improved [2-5, 2-6]. Finally, the highly Si-doped $In_xGa_{1-x}As$ cap layer is used to reduce the contact resistance.

2.3 III-V QWFETs for High Frequency Millimeter/Sub-Millimeter Wave Applications

In recent years, the millimeter-wave has shown large impact on our daily communication life. The applications of millimeter wave for communication include gigabit wireless system, cellular backbone, national weaponry, traffic guidance, radar, radio navigation device, etc. Besides, other emerging applications such as homeland security, medical diagnosis, and high-resolution image sensor have even moved to sub-millimeter wave band. With the rapid progress of communication industries, the required performances for the high frequency components are getting more and more rigid.

Among all the electronic devices, III-V based compound semiconductor devices such as pseudomorphic GaAs HEMTs (PHEMTs), metamorphic GaAs HEMTs (MHEMTs), lattice-matched or pseudomorphic high indium mole fraction $In_xGa_{1-x}As$ channel InP HEMTs have shown great potential in millimeter/sub-millimeter wave applications. Recently, by advanced improvement of process, the $In_xGa1_{1-x}As$ QWFETs in literature have achieved current-gain cutoff frequency (f_T) of 628 GHz [2-7], maximum oscillation frequency (f_{max}) above 1 THz [2-8], extrinsic transconductance (g_m) of 3 S/mm [2-9], and minimum noise figure (NF_{min}) of 0.8 dB at 90 GHz [2-10]. Consequently, they are regarded as key devices for next-generation millimeter/sub-millimeter wave systems. Table 2.1 [2-7~2-11] lists the best record of QWFETs in high speed and low noise catalog in the last three years.

2.4 Evaluations of III-V QWFETs for Beyond-CMOS Logic Applications

For the post-Si era of logic CMOS, III-V compound semiconductors have emerged as promising channel materials, which is not only for their potential in high-speed and low-power performance, but the III-V device technology is relatively mature and reasonably

reliable [2-12] compared to other novel devices such as carbon-nanotube transistors and semiconductor nanowires. Recently, nano gate length $In_xGa_{1-x}As$ QWFETs with outstanding logic performance at low supply voltage have been demonstrated [2-13]. Therefore, using III-V materials as channel for future logic CMOS applications have been noticeable.

In digital application, a transistor operates as a switch, which is different from analog for microwave or millimeter wave application. As seen from the Fig. 2.4, there're some electrical figures of merit of a transistor as a switch in digital application [2-13], like drain-induced barrier lowering (DIBL), subthreshold slope (S), on-state and off-state current ratio (I_{ON}/I_{OFF}), and the gate delay time (CV/I). But for non-optimized devices, arbitrary selections of threshold voltage (V_T), I_{ON} and I_{OFF} can easily result in an over-estimation of the logic parameters. In this study, the methodology proposed by Chau [2-12, 2-14] to analyze new devices which often feature non-optimized values of V_T were adopted. The evaluation methodology is shown in Fig. 2.5. First, select gate-source voltage at drain-source current of 1 mA/mm as the V_T. Then select I_{ON} as 2/3 V_{CC} swing above V_T, and I_{OFF} as 1/3 V_{CC} swing below V_T. Based on this definition, the logic parameters, such as subthreshold slope, DIBL and I_{ON}/I_{OFF} ratio of $In_xGa_{1-x}As$ QWFETs can be extracted.

The steepness of the device transition between the ON and OFF states is evaluated through the subthreshold slope and I_{ON}/I_{OFF} ratio. And the tightness of the threshold voltage is evaluated by drain-induced barrier lowering (DIBL), for which measures the change in V_T as a result of a change in V_{DS}. If DIBL is small, V_T is insensitive to circuit design details and manufacturing variations. Subthreshold slope and DIBL often go hand in hand and they reflect the overall electrostatic integrity of the device. Besides, device capacitance impacts the switching speed. An important figure of merit in this regard is the transistor delay (CV/I), which is a measure of the time that it takes for a transistor to switch an identical one.

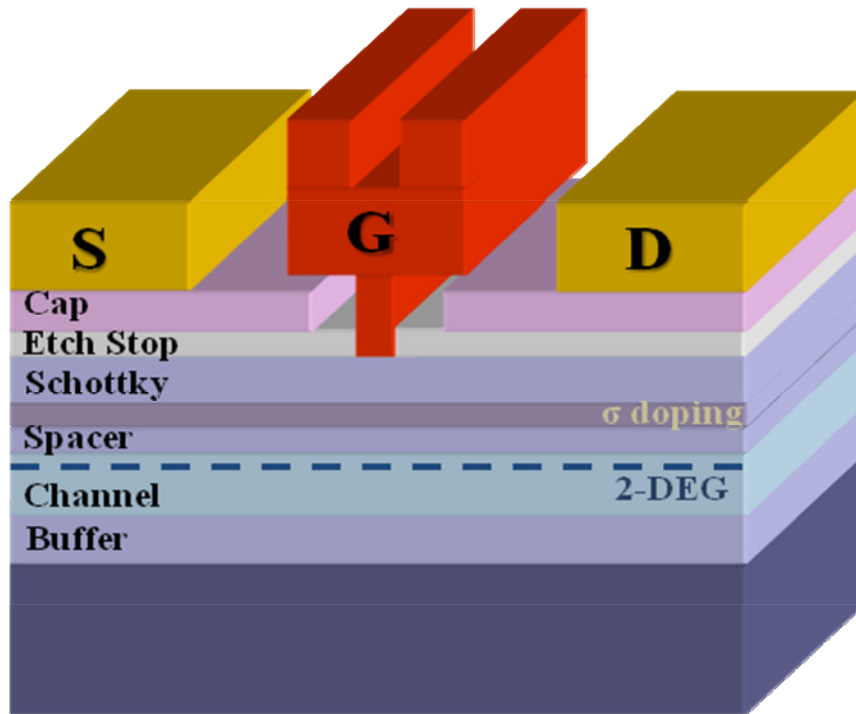


Fig. 2.1 Conventional QWFET structure

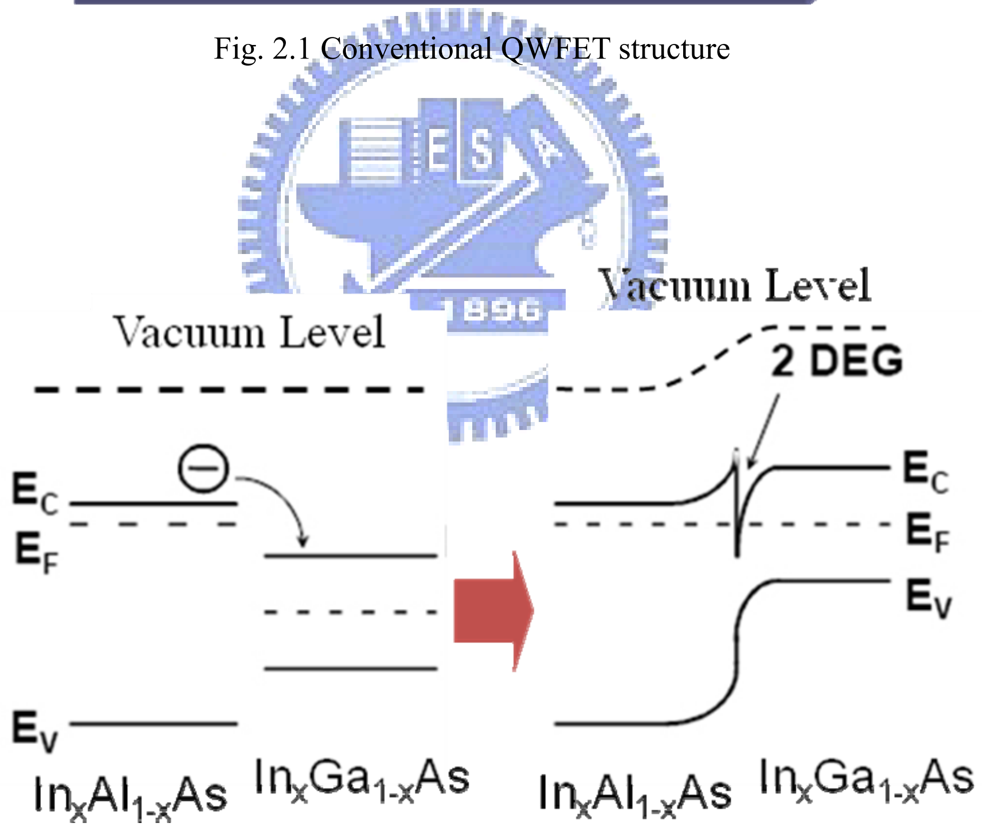


Fig. 2.2 Band Diagram of $In_xAl_{1-x}As/In_xGa_{1-x}As$ QWFET

Cap Layer	$In_xGa_{1-x}As$
Etching Stop Layer	InP
Barrier Layer	$In_{0.52}Al_{0.48}As$
δ-doping	Si-doping
Spacer Layer	$In_{0.52}Al_{0.48}As$
Composite Channel	$In_xGa_{1-x}As$ (Sub-Channel)
	$In_xGa_{1-x}As$ (Main Channel)
	$In_xGa_{1-x}As$ (Sub-Channel)
Buffer Layer	$In_xAl_{1-x}As$
Semi-insulating InP or GaAs Substrate	

Fig. 2.3 The common expitaxial structures of the $In_xGa_{1-x}As$ based QWFETs for high speed application.

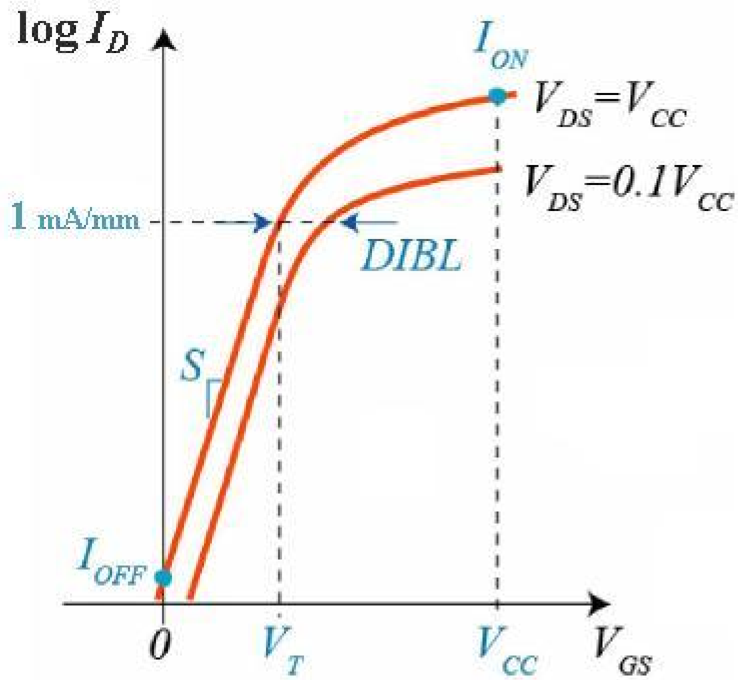


Fig. 2.4 Electrical figures of merit of a transistor as a switch

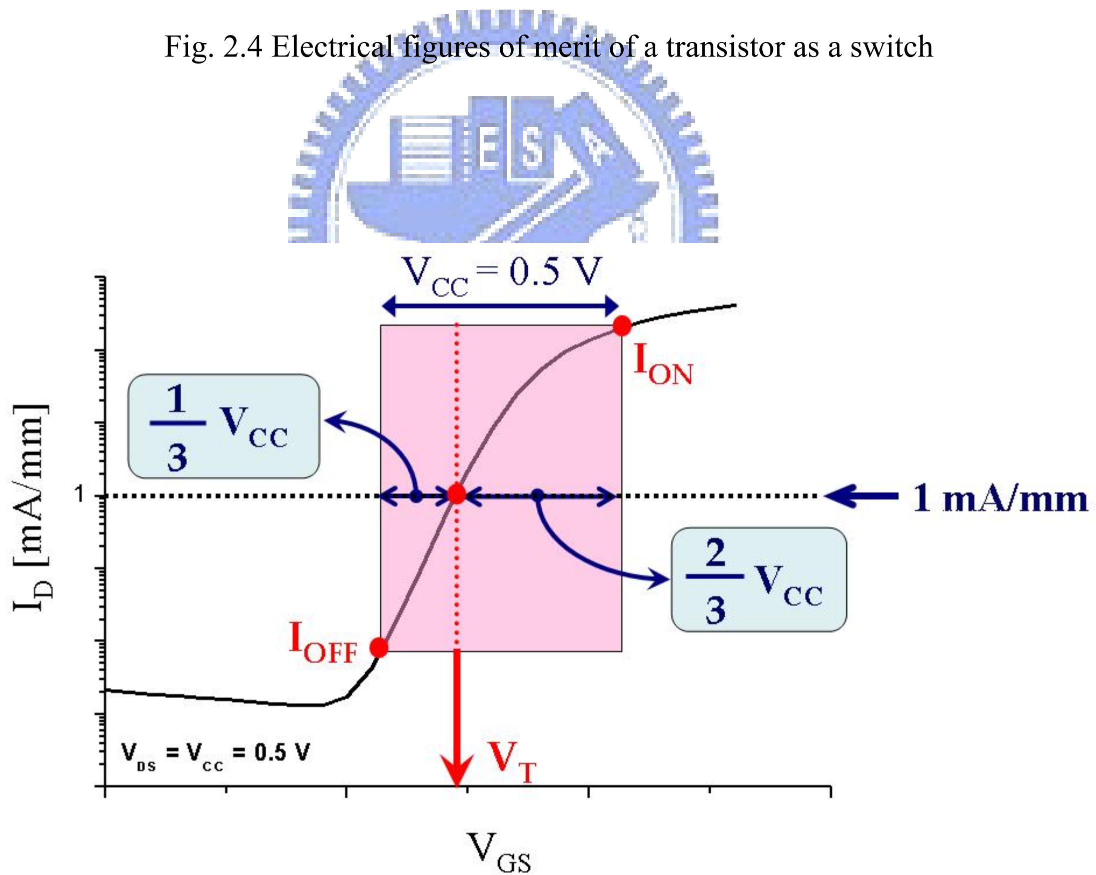


Fig. 2.5 Evaluation methodology of QWFETs for logic performance

Devices	**In (%)**	g_m **(S/mm)**	f_T **(GHz)**	f_{max} **(GHz)**	NF_{min} **& Gain (dB)**	**Published**	**Affiliation**
60nm InP HEMT	100	3	400	290	N/A	2006, *IEEE,EL.*	NTT
50nm InP HEMT	80	2.3	385	1000	N/A	2007, *IEDM*	NGST.
50nm GaAs HEMT	53	1.27	489	422	0.64 & 9 at 59GHz	2007, *IEEE,EDL*	MINT
35nm InP HEMT	70	N/A	520	425	0.8 & 5.6 at 90GHz	2008, *IPRM*	NICT
30nm InP HEMT	100	1.62	628	331	N/A	*2008, IEEE,EDL*	M.I.T

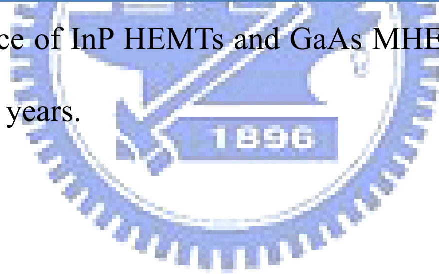


Table 2.1 Best performance of InP HEMTs and GaAs MHEMTs in high speed and low noise aspect published in recent years.

Chapter 3

Fabrications of InAs-Channel Quantum-Well Field-Effect Transistors (QWFETs)

The fabricated QWFETs in this study bring together novel designs to enhance the electronic properties. For instance, the QWFETs with small gate length (L_g) of 40nm can increase the electronic field under the gate so the electron will accelerate; the tunneling cap layer with highly doping can efficiently minimize parasitic resistances [3-1]; the application of two-step recess process can scale-down gate electrode to channel thickness so that the short channel effect is released [3-2]; and the application of Pt gate sinking process can enhance the schottky gate work function. Besides, by the precise time control of Pt gate sinking annealing, the gate electrode can be further close to channel layer so as to speed up electron transport [3-3].

The process flows of QWFETs fabrication in this study are listed below.

1. Active region formation (Mesa isolation)
2. Ohmic contact formation
3. Electron Beam Lithography process for nano T-shaped gate
4. Gate recess process (Two-step recess process) and gate formation
5. Device passivation
6. Airbridge formation

3.1 Mesa Isolation

For III-V devices, the mesa isolation process is used for the definition of active region. First, the active areas were masked by Shipley S1818 photoresist. Then the phosphoric based

solution was used to etch InGaAs/InAlAs layers and hydrochloric acid based solution was used to etch InP layer. According to the device structure, the mesa was etched to the buffer layer to provide good device isolation. The etching depth was approximately 2500Å measured by α-step. After the strip of photoresist, the etching profile was carefully checked by scanning electron microscopy (SEM).

3.2 Ohmic Contact Formation

The photoresist AZ5214E and I-line aligner were used to define the ohmic metal pattern. Unlike the Si-based devices, the lift-off process is used for III-V based device because of the lack of appropriate etching selection between ohmic metals and III-V materials. The undercut profile of the photoresist AZ5214E will benefit the metal lift-off process. The HCl-based solution was used to remove the native oxide on the InGaAs surface before Ohmic metallization. Ohmic metal multilayer Au/Ge/Ni/Au, from the bottom to the top, was deposited by e-gun evaporation system and the thickness was 2400Å. After metal lift-off process, the devices were annealed by rapid thermal annealing (RTA) at 270 ^{o}C for 30 sec in forming gas atmosphere. During annealing, germanium atoms will diffuse into the InGaAs cap layer forming heavily doped status so the contact resistance decreased. The specific contact resistance between metal and cap layer can be extracted by the transmission line method (TLM) [3-4]. In general, the typical measured contact resistance must be less than 1 x 10^{-6} Ω-cm^2.

3.3 Electron Beam Lithography Process for Nano T-shaped Gate

Decreasing gate length (L_g) can increase the electronic field under the gate so as to accelerate the transport property of channel electron. Therefore, it is benefit for devices in

high frequency and high speed applications. T-shaped gate structure was the most common approach for achieving low gate resistance and a small gate foot [3-4]. In this study, the Electron Beam lithography with tri-layer photoresists (ZEP-520/PMGI/ZEP-520) was applied for the T-shaped gate formation. Fig. 3.1 illustrates the process flow of the fabrication of nanometer T-shaped gate. The first E-beam exposure for top two layers was used to define the head (Tee-top) of the T-shaped gate. After that, the ZEP-520 and PMGI development were executed by using xylene and MF622, respectively. Then, high dosed single center exposure with xylene development was used to define the footprint of the bottom ZEP-520 layer. The SEM image of the 40 nm T-shaped gate resist profile is shown in Fig. 3.2-3.4.

3.4 Gate Recess Process (Two-step Recess Process) and Gate Formation

Through anisotropic CF_4 RIE dry etching, the gate foot was precisely replicated on 600Å SiN layer which was deposited by plasma-enhanced chemical vapor deposition (PECVD) before the E-Beam photoresistor formation. Besides, these additional 600Å SiN layer can mechanically support the small L_g of T-shaped gate [3-5]. For gate recess etching, in order to suppress the short channel effect and enhance the electron mobility under the gate, a two-step recess process proposed by T.Suemitsu et al. [3-2] was used. By applying two-step recess process, gate electrode was much close to the channel. Fig. 3.5 illustrates the process flow of two-step recess. The first step of recess was cap layer etching performed by using PH-adjusted solution of succinic (S.A.) and H_2O_2. The target current after the cap layer recess is a critical parameter to affect the QWFET performance. In order to get the desired recess target, the recess process was controlled by monitoring the non-gated drain-to-source current (I_{DS}). The second step of recess etching was removing the InP etching stop layer under the gate opening by inductive coupled plasma (ICP) with argon ambient. The second step of recess etching resulting gate structure has the gate metal deposited on InAlAs barrier layer

whereas the InP etching stop layer covers the recess region as illustrated in Fig. 3.6. After recess etching, Pt/Ti/Pt/Au (120/800/600/1800Å) gate metal was evaporated by e-gun evaporation system and lifted off by using ZDMAC remover (ZEON Corporation). For multilayer gate metal (Pt/Ti/Pt/Au), where titanium is a good adhesion layer; platinum acts as a barrier layer to prevent gold from diffusing into GaAs; and gold provides high electrical conductivity. Unlike the traditional GaAs-based QWFETs, in this study for proceeding Pt gate sinking process, the additional 120Å-thickness platinum was applied to the first gate electrode. There're several advantages of Pt gate sinking process for QWFETs. By precisely annealing time control, Pt can react with As and move toward channel. This function makes the gate electrode further close to channel layer, and it is benefit for device characteristics in high frequency as well as in logic aspects [3-3]. Additionally, Pt gate sinking process provides higher schottky gate work function of 0.8eV for $PtAs_4$ on InAlAs than the traditional work function of 0.4eV and 0.6eV for Ti on InAlAs and InP respectively. Besides, slight reduction in the gate leakage current was also observed owing to the increase in the thickness of the amorphous layer under gate which diminished the leakage path because of the reduction of the grain boundaries [3-6, 3-7].

The final formation of 40nm T-shaped gate was pictured by SEM as shown in Fig. 3.7.

3.5 Device Passivation

To prevent the device from the mechanical damages and environmental contaminations such as chemicals, gases, and particles; surface passivation of device is necessary. The dielectric layer SiN_x is a common choice for III-V device passivation. Before the passivation, the wafer was dipped in the solution of $NH_4OH:H_2O$=1:50 for 30 seconds to clean the surface and decrease the surface dangling bonds. And then PECVD system with process pressure of 900 mtorr, process temperature of 200°C, process time of 10 minutes, and process gases of

silane, ammonia, and nitrogen was used for depositing the silicon nitride film. The silicon nitride film thickness was about 600 Å and the reflection index was 2.0 as inspected by N&K anaylzer. After the passivation process, the contact via was opened by CF_4 RIE etching for interconnections.

3.6 Airbridge Formation

Airbridge process is used to interconnect the sources of FETs, to cross over a lower level of metallization, or to connect the top plate of a MIM capacitor for adjacent metallization. And because of the lowest dielectric constant, low parasitic capacitance of air, and the high electronic conductance of gold; airbridge process is used extensively in III-V analog devices and MMICs for interconnections.

For airbridge procedure, firstly the photoresistor was coated on the metal pad, and followed by a whole wafer deposited with thin Ti/Au/Ti. Then, a second photoresistor was patterned, and the gold of 2μm was electroplated. After that, the top photoresist layer, thin Ti/Au/Ti metal, and bottom resist layer were removed individually, leaving only the plated air-bridge. The SEM image of the airbridge is shown in Fig. 3.8.

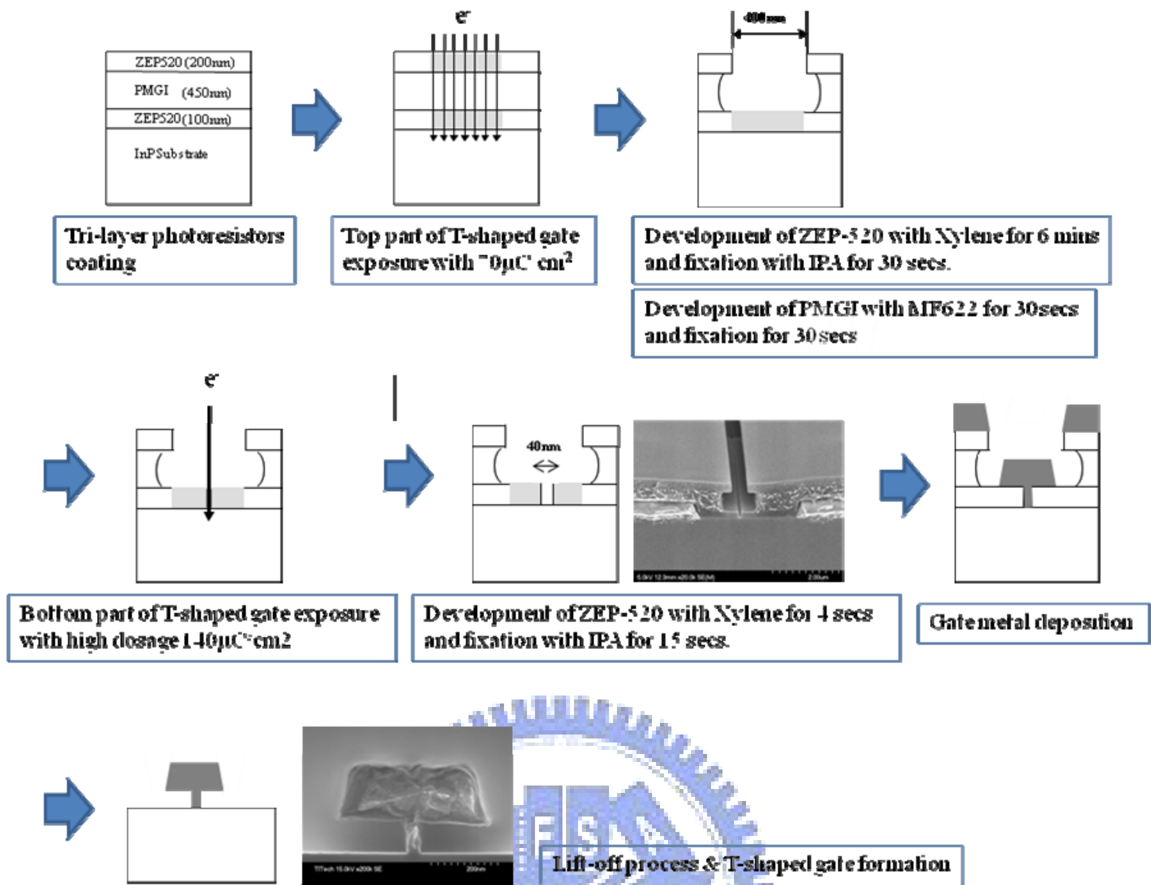


Fig. 3.1 E-Beam Lithography process flow for nano T-shaped gate

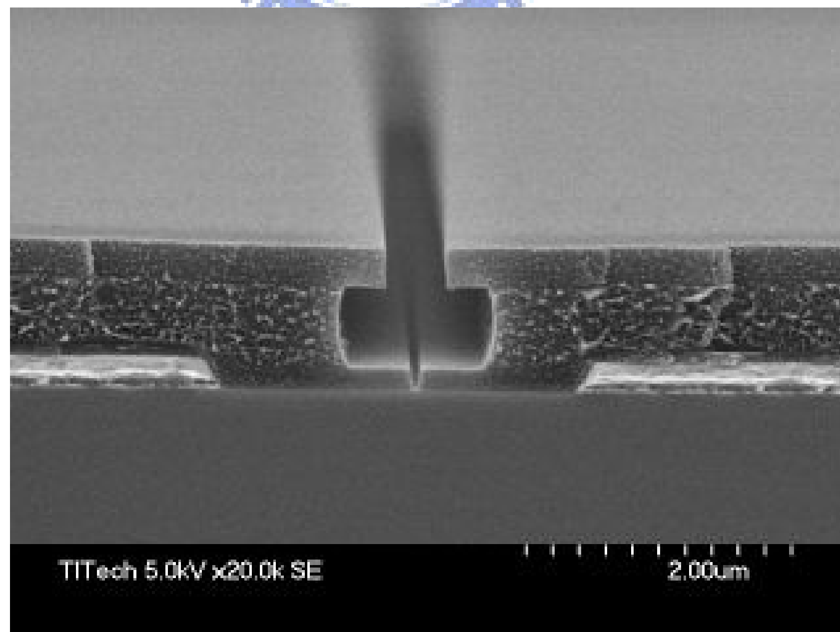


Fig. 3.2 The side view of tri-layer photoresist profile for 40 nm T-shaped gate

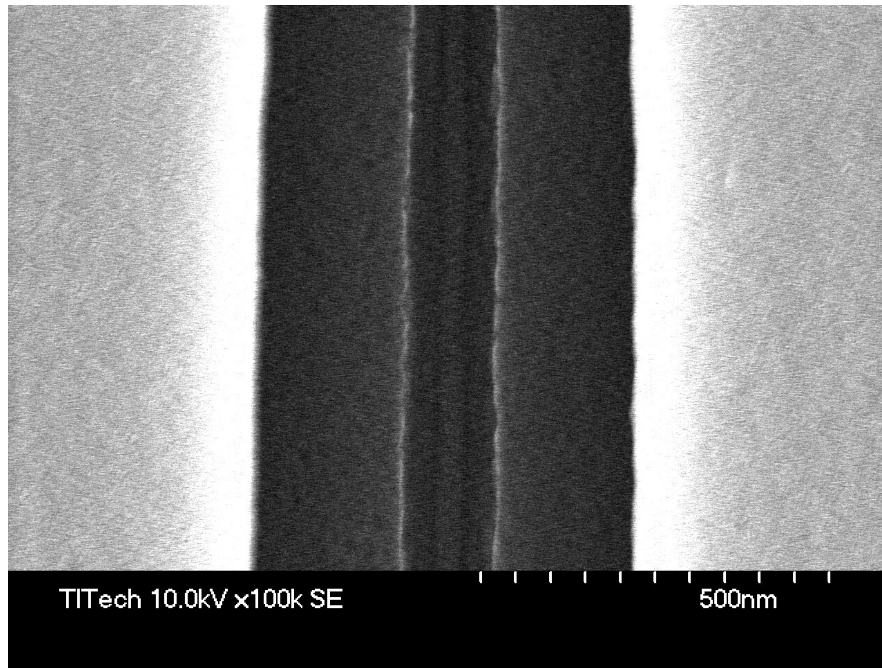


Fig. 3.3 The top view of tri-layer photoresist profile for 40 nm T-shaped gate

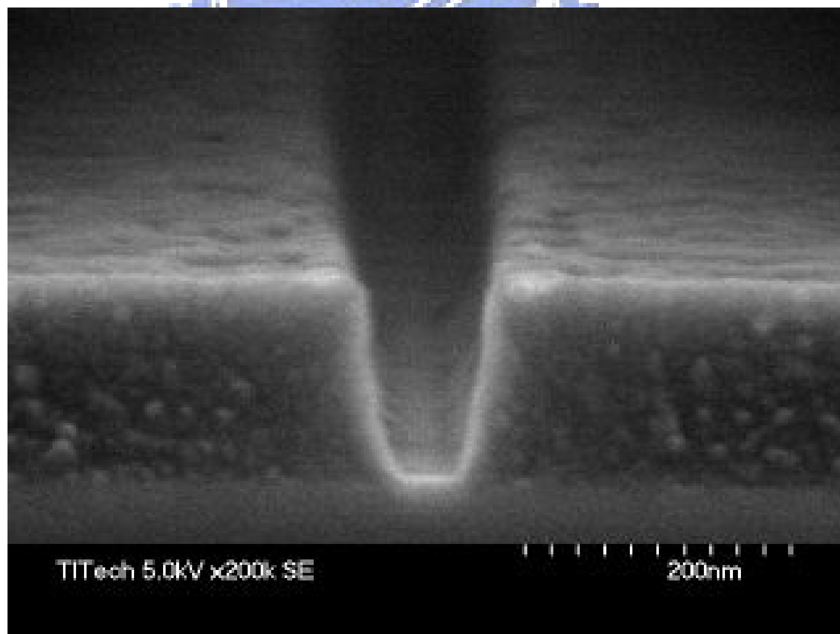


Fig. 3.4 The bottom photoresist profile of 40 nm T-shaped gate foot

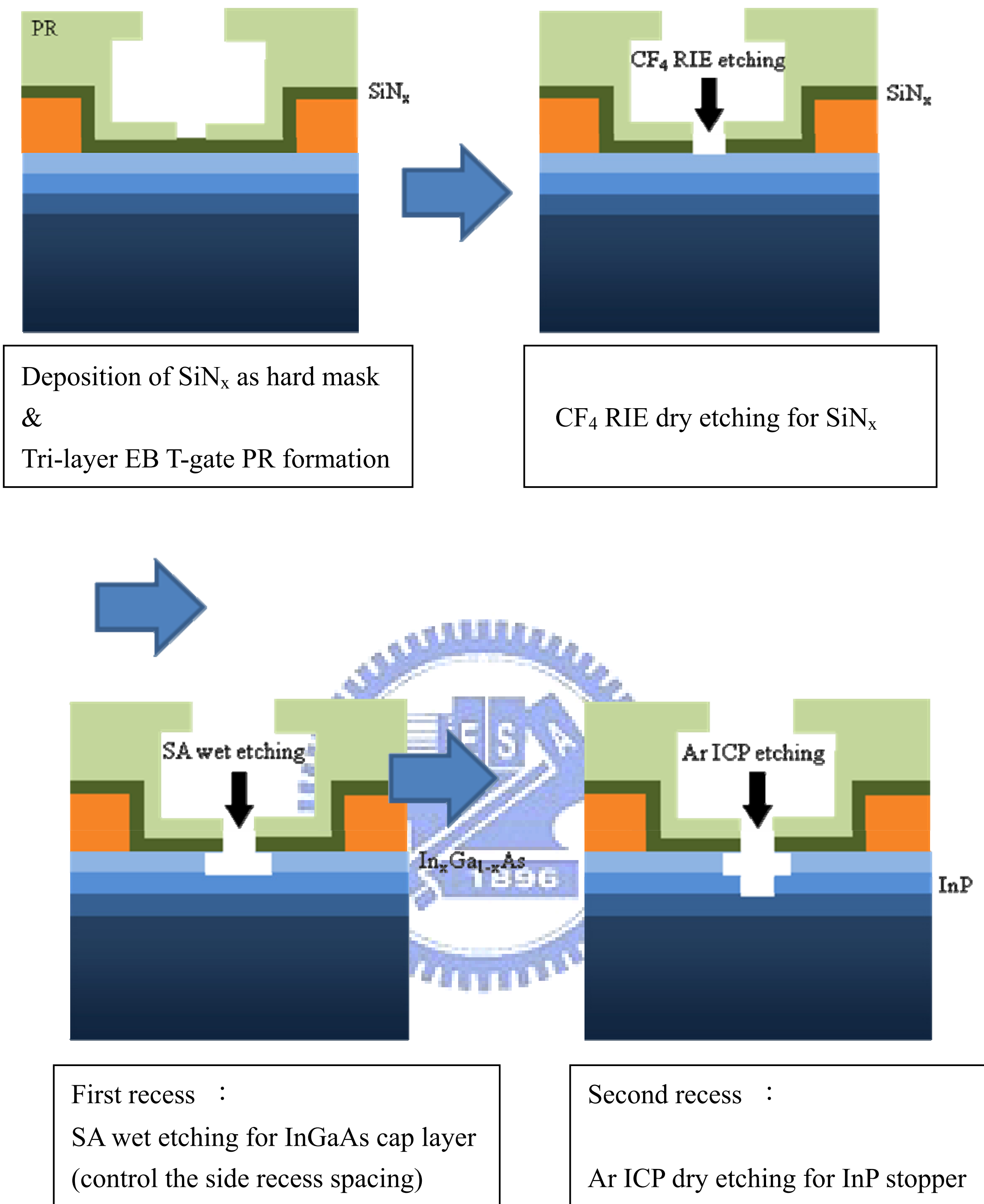


Fig. 3.5 Illustration of two-step recess process flow

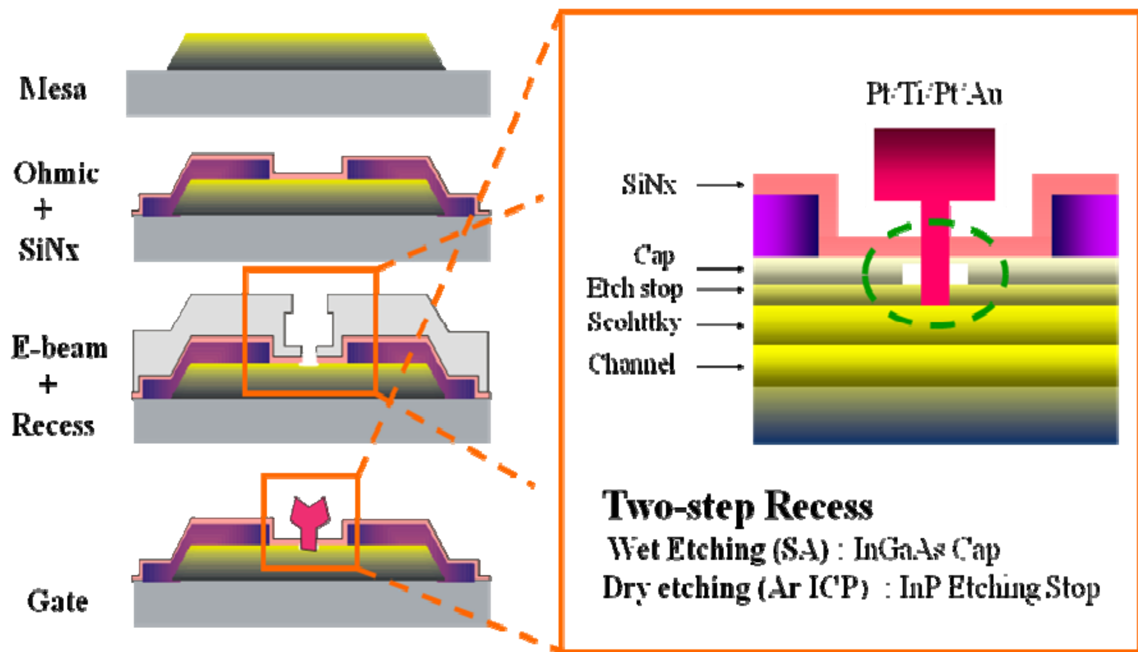


Fig. 3.6 Cross-sectional view of gate formation after two-step recess

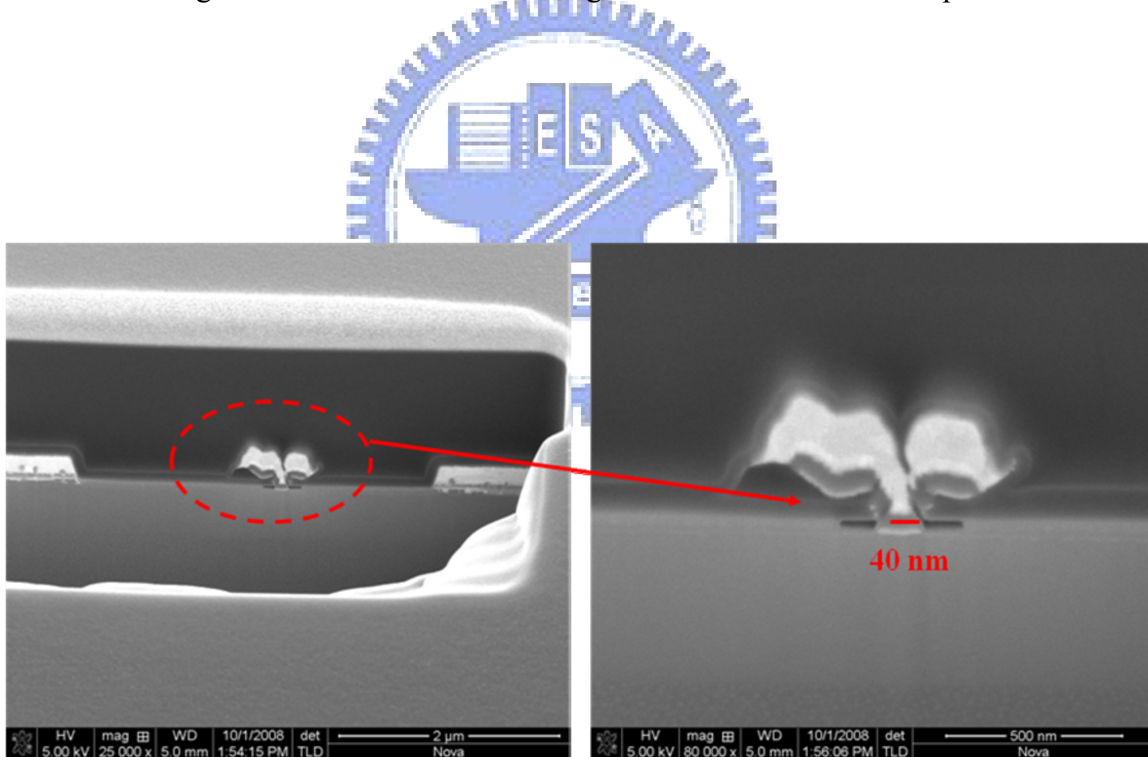
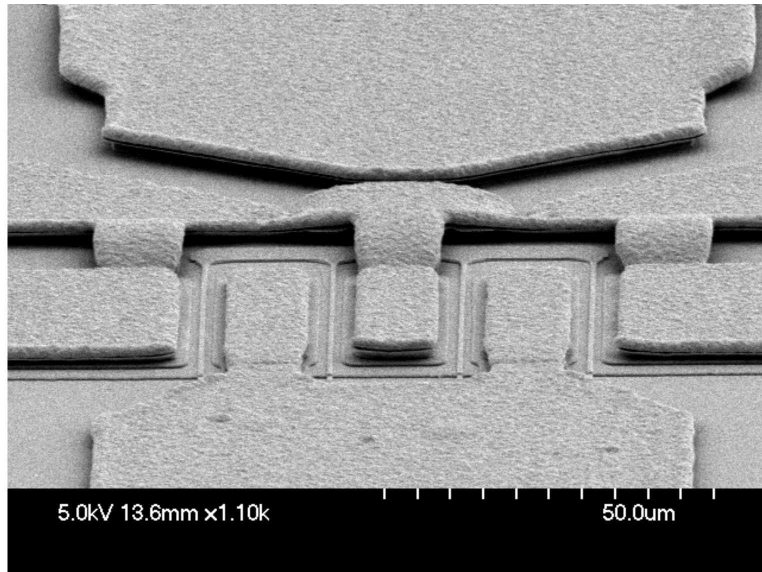
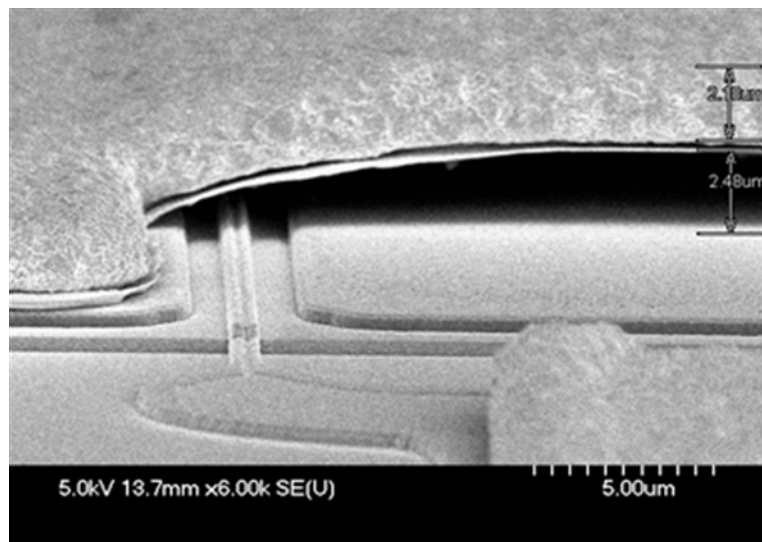


Fig. 3.7 SEM images of 40 nm T-shaped gate





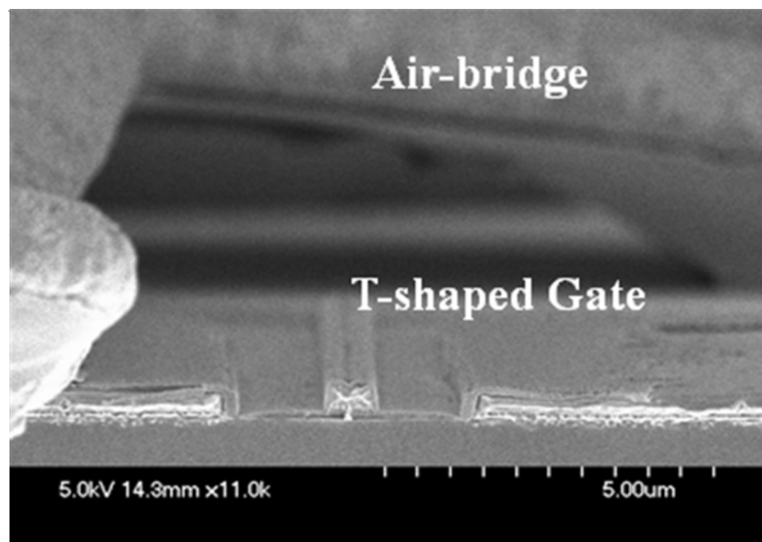


Fig. 3.8 SEM image of the airbridge

Chapter 4

Fundamentals of Electrical Characteristics for $In_xGa_{1-x}As$ QWFETs

After the device fabrication, DC and RF performance of the QWFETs were measured by using on-wafer measurement. For the DC measurement, the I-V characteristics were obtained by using an HP4142B Modular DC Source/Monitor and SUSS PA200 Semi-Auto Probe Station. The Transmission Line Model (TLM) method for determining specific contact resistance was adopted by using 4-wires measurement. The *S*-parameters were measured by HP8510XF Vector Network Analyzer using on-wafer GSG probes from Cascade MicroTech. However, finding the RF behavior of a device on a wafer was a complicated process. For conventional RF measurement of a packaged device, the wafer needs to be diced and then an individual die should be mounted into a text fixture. Discriminating between the die's and the fixture's responses became an issue. Furthermore, fixturing die was a time-consuming process, and making it impractical for high-volume screening. Thus the need for on-wafer RF characterization was arisen [4-1]. In this study, de-embedding which must also be performed to discover the true RF performance of the device is discussed.

4.1 DC Characteristics [4-2]

The band diagrams at three different locations along the channel are illustrated in Fig. 4.1. There is a potential drop of channel charge density in the direction parallel to the channel, causing q'_{CH} to be a function of the position x. In order to relate the QWFET equations to the well-developed MOSFET equations, a per area gate oxide capacitance was define as C'_{OX}. Therefore, the channel charge sheet density is expressed as：

$$q'_{CH} = -C'_{OX}[V_{GS} - V_T - V_{CS}(\chi)] \quad (4\text{-}1)$$

Here the channel-to-source potential is resulting from the applied Gate-Source voltage (V_{GS}) and Drain-Source voltage (V_{DS}). V_T is threshold voltage and the x means the position along the channel. The additional potential $V_{CS}(x)$ is called the channel-source potential. When $V_{DS} \neq 0$, the channel-source potential varies with x and the potential difference is the potential between any point x along the channel with respect to the source.

The channel current equation $I = qA\mu_n\varepsilon$ (A=area) is proportional to the cross-section area of the current conduction, the charge density, the mobility μ_n, and the electric field. Therefore, the form of the channel current equation in QWFET is obtained：

$$I_{CH}(\chi) = -WC_{OX}\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \quad (4\text{-}2)$$

We note that q'_{CH} is a negative quantity in QWFET, since electrons accumulated in the channel are negative charges. Besides, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have $I_D = -I_{CH}$, and we find：

$$\int_0^L I_{DS}\,dx = -C'O\int_{V_{CS(O)}}^{V_{CS(L)}} C_{OX}\,\mu_n[V_{(GS)} - V_{(T)} - V_{(CS)}(\chi)]dV_{CS}(\chi) \quad (4\text{-}3)$$

To carry out the integration in Eq. (4-3), we deal with the linear operating region first so that current saturation due to channel pinch off at the drain does not occur. In the linear region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (4-3) leads to:

$$I_D = \frac{W_g C'_{OX}\,\mu n}{Lg}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \quad (4\text{-}4)$$

Eq. (4-4) is plotted schematically in Fig. 4.2, with I_D shown as a function of V_{DS}. The value of V_{DS} corresponding to the saturation drain current ($I_{D,sat}$) is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of I_D with respect to V_{DS} and setting the result to zero. And we find that:

$$V_{DS,SAT} = V_{GS} - V_T \quad (4\text{-}5)$$

At saturation voltage, q'_{CH} calculated from Eq. (4-1) is identically zero at the drain (pinch off). However, we realize that this conclusion originates from the fact that we are extending the validity of Eq. (4-1) all the way to where $q'_{CH}(L)$. But physically the channel at the drain does not pinch off completely. Instead, there is a finite thickness of accumulation of charges at which $q'_{CH}\, x=L$ so it's nonzero. The drift velocity is high, but nonetheless finite, so a constant current is maintained throughout the channel. Therefore, a complete model of the drain current is given by:

$$I_{DS} = \frac{W_g C'_{OX} \mu_n}{Lg}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \quad \text{for } V_{DS} < V_{DS,SAT} \qquad (4\text{-}6)$$

$$= \frac{W_g C'_{OX} \mu_n}{Lg}[\frac{(V_{GS} - V_T)^2}{2}] \quad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (4\text{-}7)$$

And another important parameter for QWFET is transconductance (g_m), which represents the amount of drain current increase with the increment of gate bias at constant drain voltage.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS} = const.} \qquad (4\text{-}8)$$

For QWFET, it is convenient to define the *saturation index (α)* as:

$$\alpha = 1 - \frac{V_{DS}}{V_{DS,SAT}} \quad \text{for } V_{DS} < V_{DS,SAT}$$

$$= 0 \quad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (4\text{-}9)$$

So we also can write g_m as:

$$g_m = \frac{W_g C'_{OX} \mu_n}{Lg}(V_{GS} - V_T) * (1 - \alpha) \qquad (4\text{-}10)$$

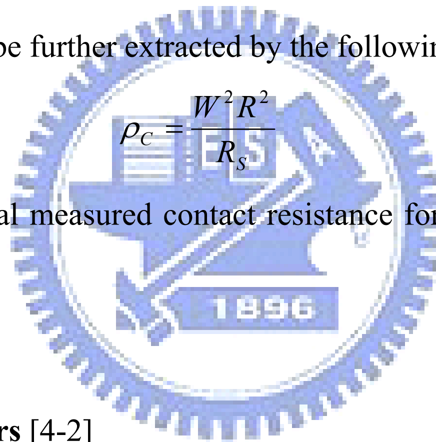
4.2 Transmission Line Model (TLM)

The specific contact resistance between contact metal and cap layer can be extracted by

the transmission line model (TLM) method [4-3]. The TLM pattern, as illustrated in Fig. 4.3, was designed in the process control monitor (PCM). In this particular approach, a linear array of contacts pad is fabricated with various spacing between them. The distances between TLM electrodes are 3 μm, 5 μm, 10 μm, 20 μm, and 36 μm, respectively. The resistance between the two adjacent electrodes can be plotted as a function of the space between electrodes and is expressed by the following equation

$$R = 2R_C + R_S L/W \tag{4-11}$$

,where R is measured resistance, R_C is contact resistance, R_S is sheet resistance of channel region, W is electrode width, and L is the space between electrodes. As Fig. 4.4 shows, extrapolating the data to L=0, one can calculate a value for the term R_C. And the specific contact resistance ρ_C can be further extracted by the following formula.



$$\rho_C = \frac{W^2 R^2}{R_S} \tag{4-12}$$

In general, the typical measured contact resistance for InGaAs QWFET was < 1 x 10^{-6} Ω-cm^2.

4.3 Scattering Parameters [4-2]

Field-effect transistor with the input and output terminals can be treated as a two-port network as shown in Fig. 4.5. Many characteristics such as gain, return loss and impedance matching can be calculated from relationship among the input and output signals. The impedance parameters (z-parameters), conductance parameters (y-parameters) and hybrid parameters (h-parameters) are used to characterize the devices. While the frequency is up to several GHz, the z-, y-, h- parameters can not be directly obtained by open or short circuits because of the reflected wave from the open or short terminations, which will induce the network oscillations. Therefore, the scattering parameters (S-parameters) are used to

characterize the performance of a device at high frequency. Fig. 4.6 shows the equivalent two-port network schematic at high frequency. Generally, the Scattering parameters, which referred to as s-parameters, are fundamental to microwave measurement. S-parameters are a way of specifying return loss and insertion loss. The relation of the microwave signals and s-parameters are defined as follows:

$$s\text{-parameters:} \quad \begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix} \tag{4-13}$$

Microwave signals going into or coming out of the input port are labeled by a subscript 1. Signals going into or coming out of the output port are labeled by a subscript 2. The electric field of the microwave signal going into the component port is designated a; that leaving the port is designated b. Therefore,

a_1 is the electric field of the microwave signal entering the component input.

b_1 is the electric field of the microwave signal leaving the component input.

a_2 is the electric field of the microwave signal entering the component output.

b_2 is the electric field of the microwave signal leaving the component output.

By definition, then,

$$s11 = \left.\frac{b1}{a1}\right|_{a2=0}$$

$$s21 = \left.\frac{b2}{a1}\right|_{a2=0}$$

$$s12 = \left.\frac{b1}{a2}\right|_{a1=0}$$

$$s22 = \left.\frac{b2}{a2}\right|_{a1=0} \tag{4-14}$$

Consequently, s_{11} is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output. Because b_1 and a_1 are

electric fields, their ratio s_{11} is a reflection coefficient. Similarly, s_{21} is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, s_{21} is a transmission coefficient and is related to the insertion loss or the gain of the device. s_{22} is similar to s_{11}, but looks in the other direction into the device.

4.4 Current-Gain Cutoff Frequency (f_T) and Maximum Oscillation Frequency (f_{max})

Current-gain cutoff frequency (f_T) is defined as the frequency at which the short-circuit current-gain becomes unity. The intrinsic s-parameters are extracted to determine the value of f_T and which is determined by extrapolation of the short-circuit current gain h_{21} = 0 dB. Here h_{21} can be defined as

$$h21 = \frac{2s21}{(1-s11)(1+s22)+s12\,s21} \tag{4-15}$$

f_T can also be expressed by using circuit elements：

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{4-16}$$

$$f_T = \frac{g_m}{2\pi C_G} = \frac{Z_G v_{sat}\varepsilon}{w} \bullet \frac{w}{\varepsilon Z_G L_G} \bullet \frac{1}{2\pi} = \frac{v_{sat}}{2\pi L_G} \tag{4-17}$$

The (C_{gs} + C_{gd}) is the total capacitance related to the schottky gate. From this relation, we could see that in order to achieve high f_T, enhancing g_m and decreasing total gate capacitance must be achieved. Because small total gate capacitance is accomplished by short gate length, and decreasing gate length can increase the electronic field under the gate and then accelerate the channel electron transport property. Therefore, the shrinking of gate length is an effective way to get high g_m and low C_g so as to attain high f_T.

Another important parameter is f_{max}, which is the frequency where the power gain falls to unity. f_{max} is expressed as

$$f_{max} = \frac{f_T}{2\left(\frac{R_g + R_i + R_s}{R_{ds}} + (2\pi f_T R_g C_{gd})\right)^{\frac{1}{2}}} \quad (4\text{-}18)$$

This expression shows that in order to obtain useful power gain at high frequency, the f_T of a device must be large; in addition, the resistances of gate, source and drain must be small.

4.5 Device Modeling Technique

When defining the high frequency RF performance of the QWFETs, it is essential to de-embed all the conductors which are on the top surface of the wafer such as the pad, metal, and interconnect. Detailed layout of the device in this study is shown in Fig. 4-7.

In this study, an approach that combines the conventional way and 3-D full wave electromagnetic analysis is proposed and the intrinsic parameters of devices are extracted. To accurately determine the equivalent circuit model, the overall structure is divided into several blocks, including gate parasitic, drain parasitic, source parasitic and intrinsic part as shown in Fig. 4-8. The parasitic elements should be kept at fixed values and not scalable with device size. The intrinsic block could further be divided into different equivalent circuit elements and shown in Fig. 4-9. Standard gradient optimization routine is used to minimize the error function value, which is defined as the difference between the modeled and measured S-parameters. In order to rigorously determine the parasitic elements, CST Microwave Studio which is based on finite integration algorithm in time domain (FIT) is applied to analyze the structure. It is observed from the plot that the two source buses are held at a lower potential referenced to the gate and source pads thus the E-filed lines tend to terminate at these buses indicating a strong capacitive parasitic (Fig. 4-10 a). To illustrate the difference, a similar structure without the two source buses is simulated and the electric filed at 10 GHz is plotted in Fig. 4-10 b, where a much coarser electric field distribution between the gate (drain) pad

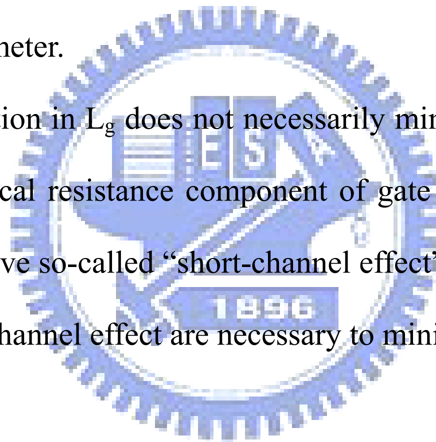
and source region is observed. Based on the EM analysis of the structure, the strong capacitive parasitic behavior between the gate (drain) pad and the source buses suggests two additional capacitors to be included in the equivalent circuit.

4.6 Noise Figure

NF can be well approximated by the semi-empirical equation given by Fukui [4-4] and is shown as the following equation:

$$NF = 1 + k\,(f/f_T)\,[g_m\,(R_g+R_s)]^{1/2},$$
$$= 1 + 2\pi kf\,(Cgs + Cgd)\,[g_m\,(R_g+R_s)]^{1/2} \qquad (4\text{-}19)$$

, where k is a fitting parameter.



Generally, the reduction in L_g does not necessarily minimize the NF_{min} because R_g tends to increase due to a vertical resistance component of gate resistance, and also g_m decreases due to a degraded gate drive so-called "short-channel effect". Therefore, a reduction in R_g and suppression of the short-channel effect are necessary to minimize NF_{min}.

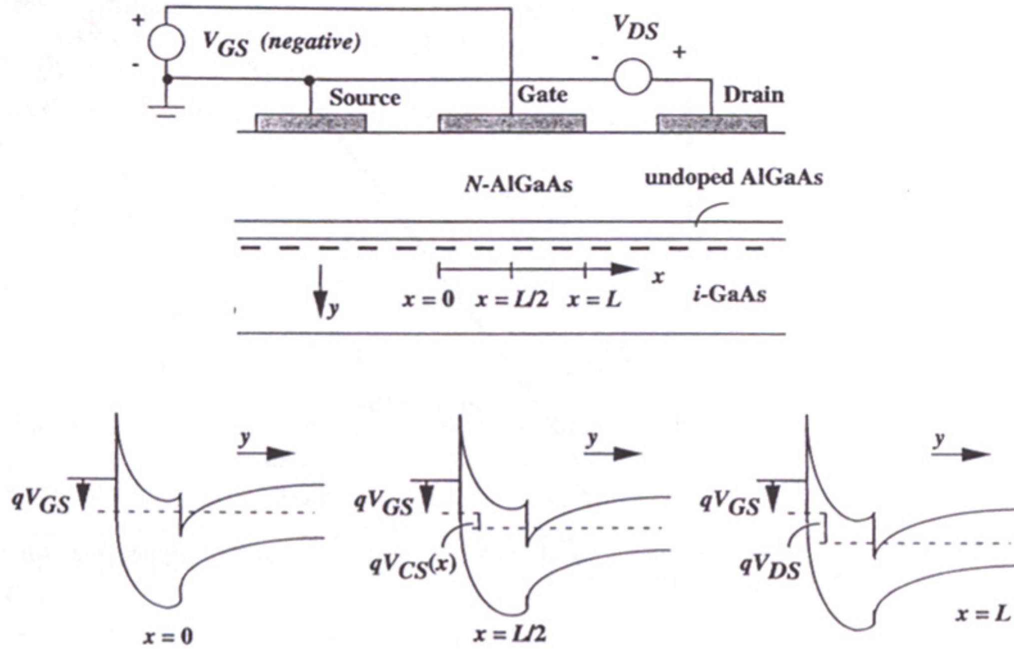


Fig. 4.1 Band diagrams of QWFET at three different locations along the channel.

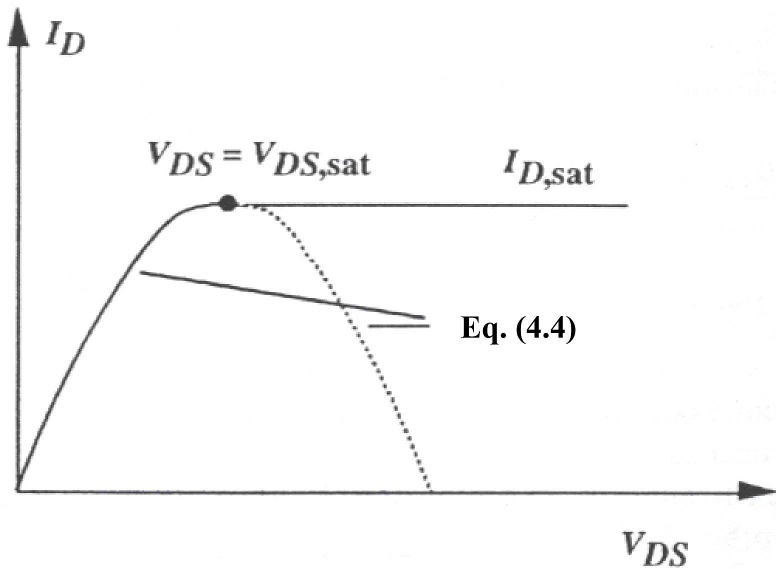


Fig. 4.2 Drain current of III-V QWFETs predicted by Eq. (4-4).

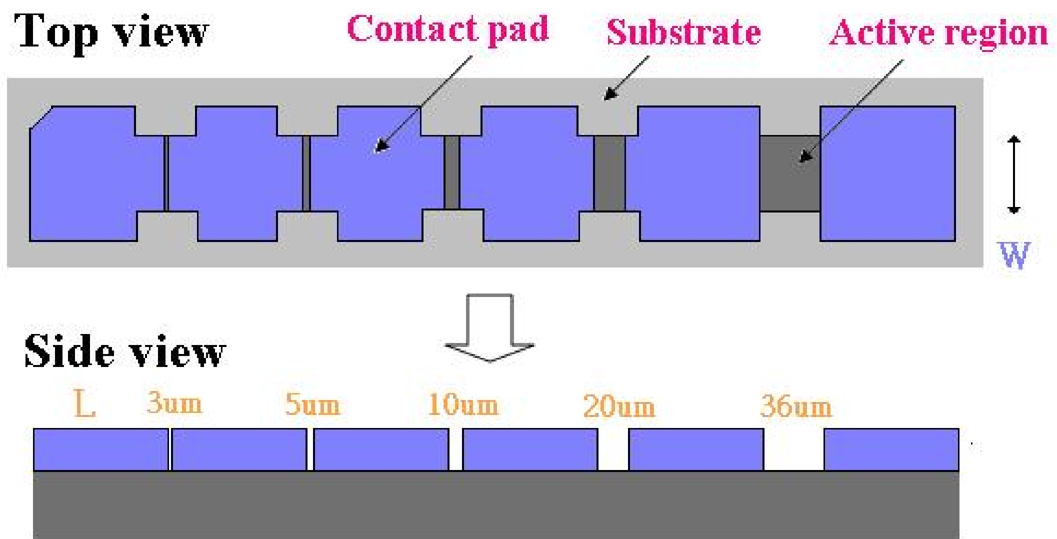


Fig. 4.3 TLM pattern.

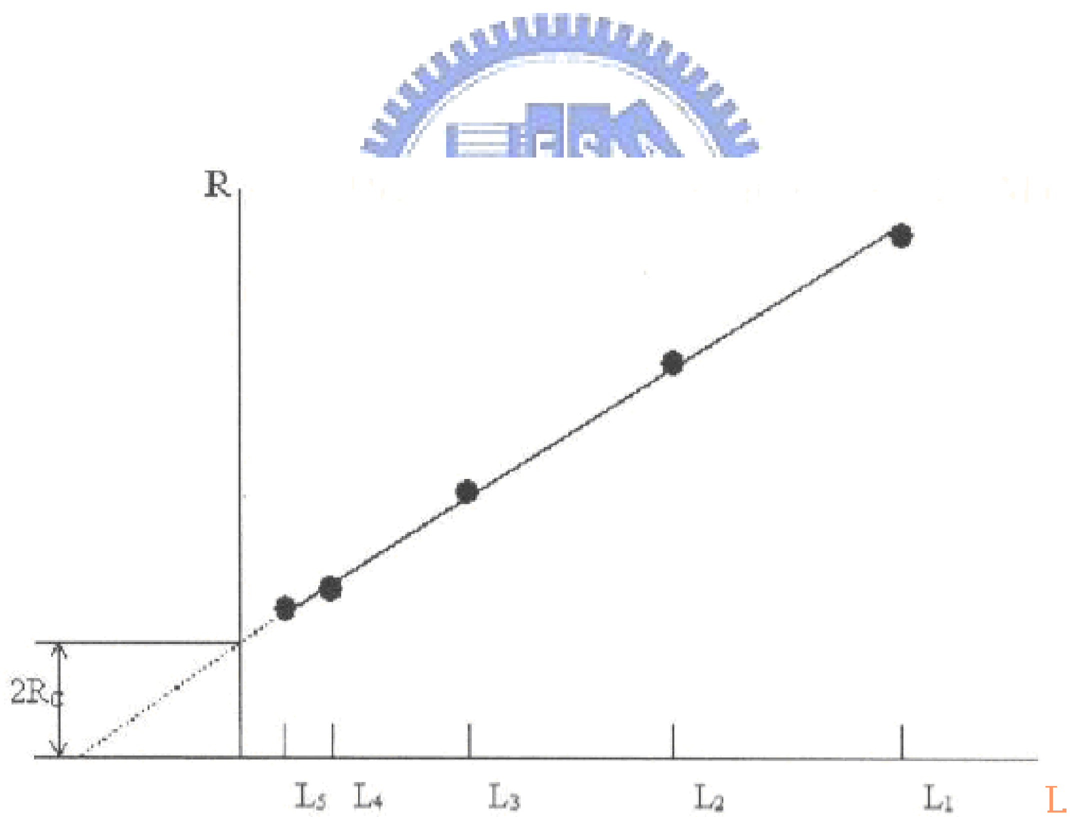


Fig. 4.4 The illustration of utilizing TLM to measure ohmic contact resistance.

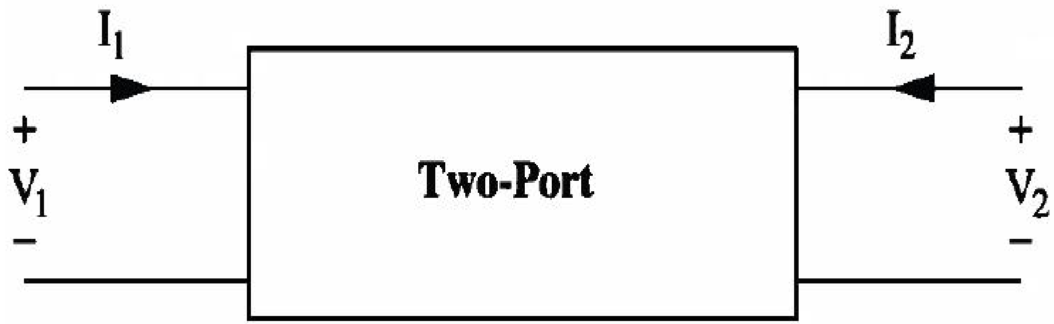


Fig. 4.5 The equivalent two-port network schematic at low frequency.

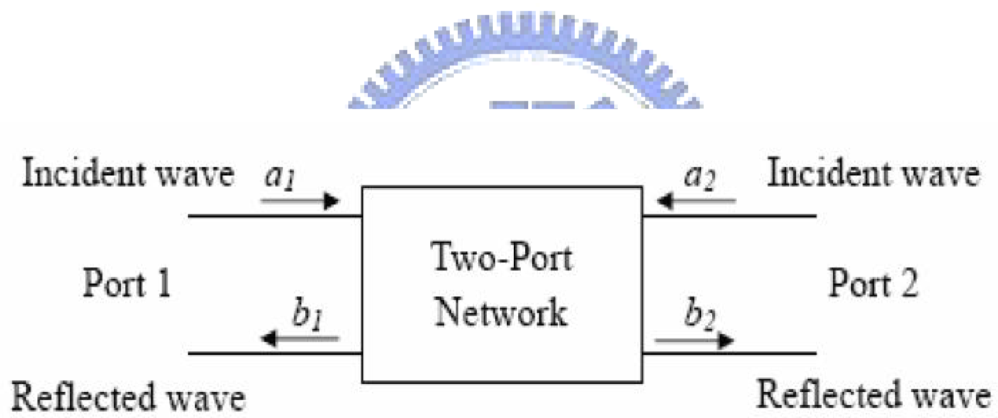
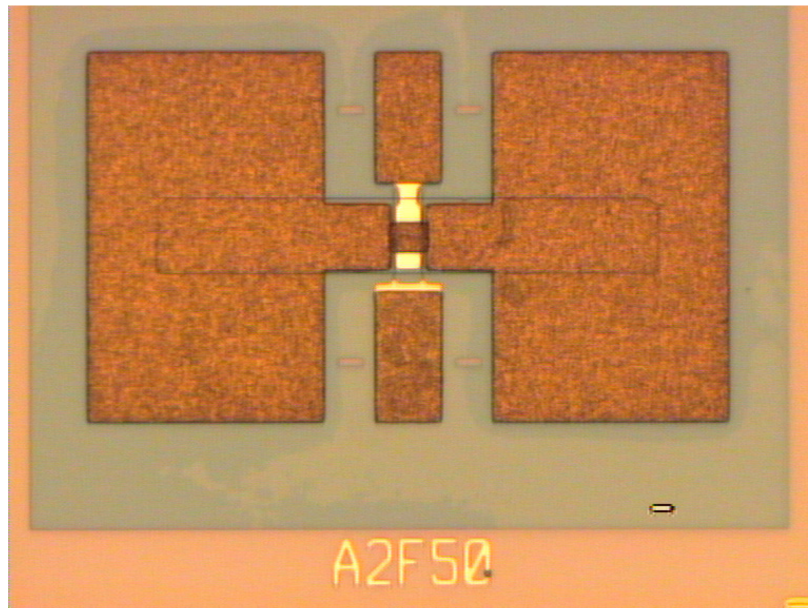


Fig. 4.6 The equivalent two-port network schematic at high frequency.



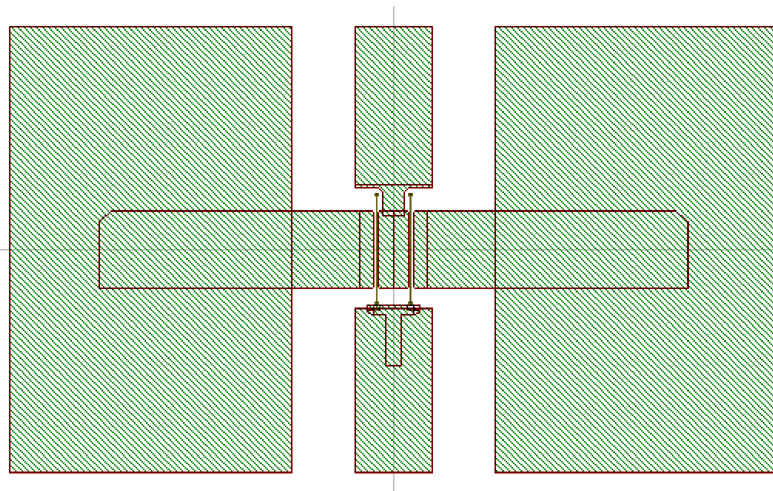


Fig. 4.7 The device layout used in this study.

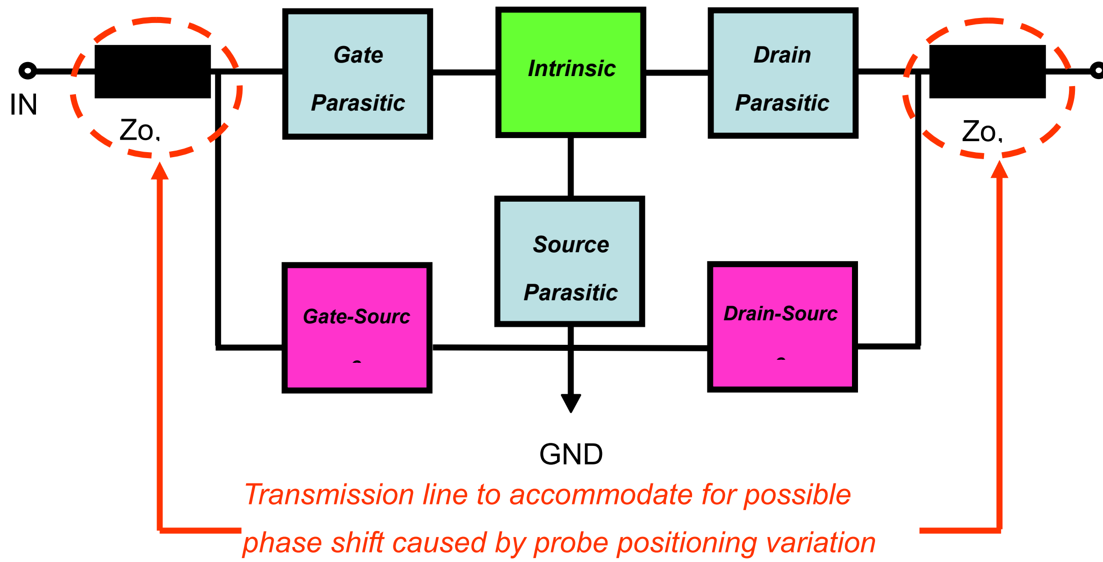


Fig. 4.8 The block diagram with determined parasitic elements for the overall device structure.

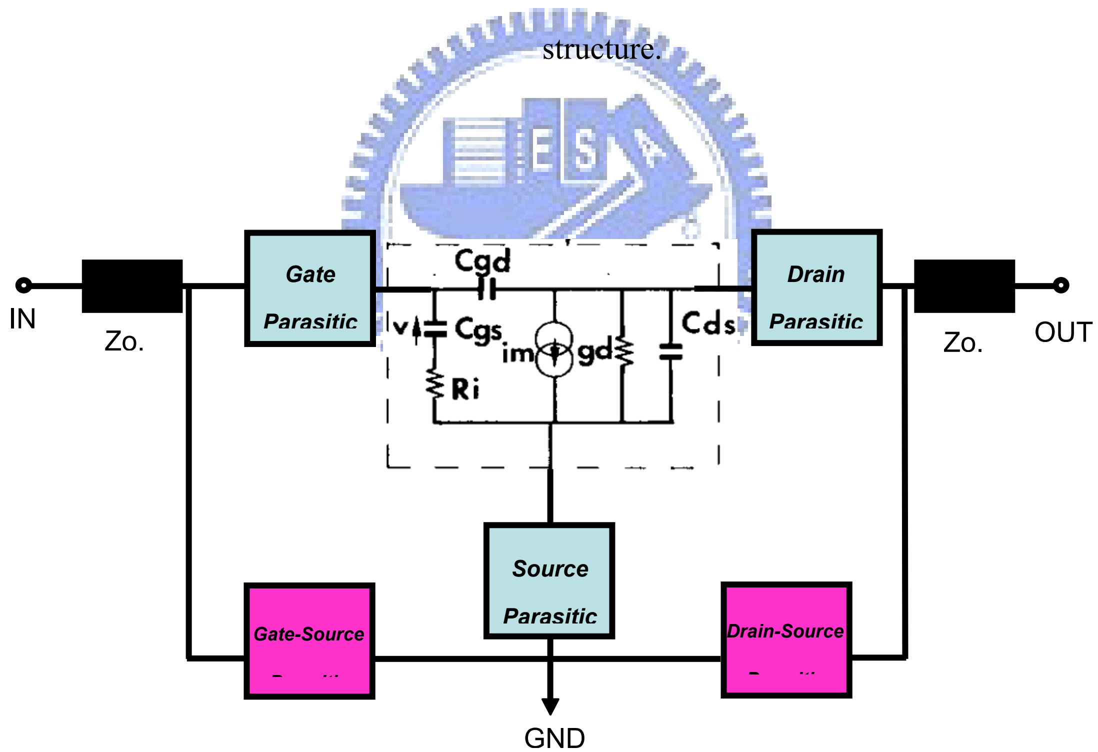
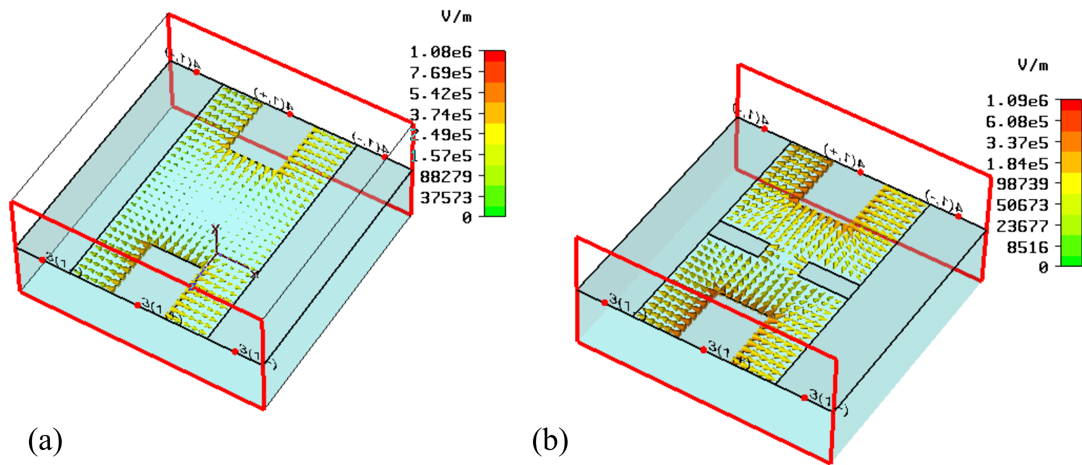
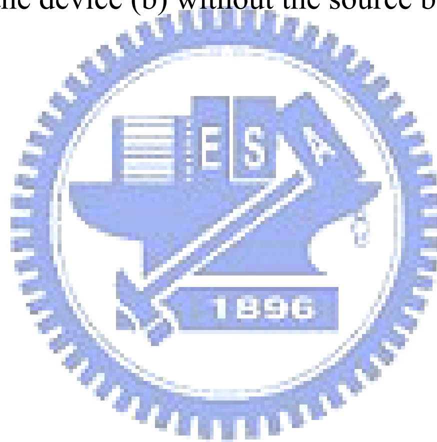


Fig. 4.9 Functional blocks of the equivalent circuit model, divided according to the scalability with device size.



(a) (b)

Fig. 4.10 Analyzed electric field plot of the 2x50um device at 10 GHz. (a) with the source buses of the device (b) without the source buses of the device



Chapter 5

Experimental results and discussions

5.1 40 nm InAs-Channel Based QWFETs for High-Speed and Low-Voltage RF Applications by using Two-Step Recess and Pt Gate Sinking Processes

5.1.1 Introduction

For commercial and military applications of millimeter wave and sub-millimeter wave systems such as wireless LANs, outer-space radars, mobile communications and hand-held imagers etc., the key component of the systems is the front-end amplifier in the receiver. And the system sensitivity is ultimately determined by the performance of the front-end amplifiers which should possess outstanding high frequency features and low noise characteristics. In addition to the requirements of high gain and low noise, low DC power consumption is also in highly demand. Among all the possible technologies to meet such stringent requirements, high indium content InGaAs-based QWFETs are particularly promising. Because the InGaAs material own significant transport properties like high electron mobility, high saturation velocity, high sheet electron densities, and large Γ to L valley separation even in low electric field. Besides the excellent electrical properties of InGaAs material, the superior band-gap design of QWFETs also leads $In_xGa_{1-x}As$ QWFETs incomparable in high speed and low voltage performances.

For devices operating in high frequency region, current-gain cutoff frequency (f_T) is a significant index. f_T is defined as the frequency which the current-gain becomes 0 dB. f_T can also be expressed by using circuit elements as following：

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

$$f_T = \frac{g_m}{2\pi C_G} = \frac{Z_G v_{sat} \varepsilon}{w} \bullet \frac{w}{\varepsilon Z_G L_G} \bullet \frac{1}{2\pi} = \frac{v_{sat}}{2\pi L_G}$$

As shown in the above relations, in order to achieve high f_T, it is necessary to enhance g_m and decrease total gate capacitance. In general, small total gate capacitance can be accomplished by shortening the gate length, and decreasing gate length can also increase the electronic field under the gate resulting in the accelerating of the transport property of the channel electrons. Therefore, shrinking the gate length is an effective way to get high g_m and low C_g so as to attain high f_T.

For the noise performance, minimum noise figure (NF_{min}) can be well approximated by the semi-empirical equation given by Fukui [5-1] and is shown as the following equation：

$NF_{min} = 1 + k\,(f/f_T)\,[g_m\,(R_g+R_s)]^{1/2}$,

$= 1 + 2\pi k f\,(C_{gs} + C_{gd})\,[\,(R_g+R_s)/g_m]^{1/2}$, where k is a fitting parameter.

It can be seen that the reduction of the parasitic capacitances and parasitic resistances are the keys to achieve low noise figure. And this can be accomplished by the shrinkage of gate length and the usage of low resistance structure layers and process.

Although the reduction of gate length seems to be a good approach both for high frequency and low noise performance, such approach may generate the performance degradation caused by the short channel effect. Thus, care must be taken in obtaining the optimal performance without the short channel effect. Therefore, two-step recess process [5-2] and Pt gate sinking process were developed to solve this problem. Two-step recess process and Pt gate sinking technology have been widely used in the fabrication of QWFETs since they provide the promising solutions that enable vertical scaling shrinkage of gate-channel distance without increasing the access resistance. Meanwhile, the short-channel effect can be effectively minimized. By precise time control of the annealing time for Pt gate sinking process, Pt will diffuse toward channel. This reaction makes the gate electrode further close to channel layer, and it is beneficial for high frequency devices as well as for logic applications.

Another advantage of using Pt-based structure is the relatively large schottky barrier height which will suppress gate leakage current.

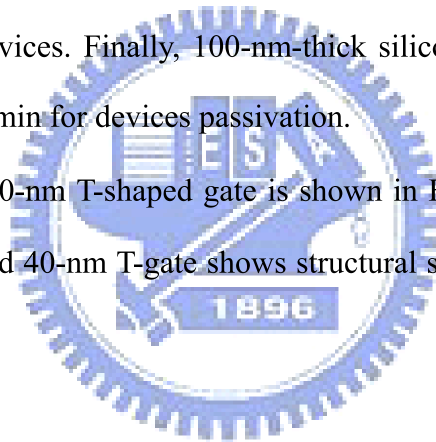
In this work, the electron beam lithography system was used to fabricate nanometer (40 nm) gate length for InAs QWFETs. Besides, two-step recess and Pt gate sinking processes were applied simultaneously to effectively reduce the gate-channel distance. The measured DC, RF and noise results will be presented here.

5.1.2 Experiment

The QWFET structure in this study was grown by molecular beam epitaxy (MBE) on a 2-in diameter InP substrate, and the schematic structure is shown in Fig. 5.1.1. The structure layers from bottom to top consist of a 500 nm $In_{0.52}Al_{0.48}As$ metamorphic buffer layer, a 5 nm InAs channel layer combining with a 3 nm $In_{0.53}Ga_{0.47}As$ lower sub-channel layer and 2 nm $In_{0.53}Ga_{0.47}As$ upper sub-channel layer, then, a 8 nm $In_{0.52}Al_{0.48}As$ Schottky barrier layer with Si planar doping ($4x10^{12}cm^{-2}$), a 5 nm InP etching stop layer and a 40 nm highly Si-doped $In_{0.53}Ga_{0.47}As$ cap layer ($1\times10^{19}cm^{-3}$). The $In_{0.53}Ga_{0.47}As$ sub-channels here were applied to enhance the electron confinement in the thin InAs layer and improve the electron transport properties [5-3].

For the device fabrication, the active area of the device was isolated by wet etching. Au-Ge-Ni-Au was deposited on heavily doped n-InGaAs cap layer and then alloyed in rapid thermal annealing (RTA) at 250℃ for 30 second to form source and drain ohmic contacts with low contact resistance and sheet resistance. Before the formation of T-shaped gate photoresist, the 600Å silicon nitride was deposited by plasma enhanced chemical vapor deposition (PECVD) as the support of the following 40nm gate foot. The T-shaped gate photoresist was carried out by using 50-kV JEOL electron beam lithography system (JBX 6000FS). The tri-layer EB photoresist system (ZEP/PMGI/ZEP) with double exposure and

development was used to define the 40nm gate length. The top layer of T-shaped gate was exposed with low dosage, and the fine footprint was written with high dosage. Through anisotropic CF_4 RIE dry etching, the gate foot was precisely replicated on 600Å SiN_x layer. Then, the two-step recess technique was performed. The first step of recess was cap layer etching performed by using PH-adjusted solution of succinic (S.A.), NH_4OH and H_2O_2. And the second step of recess etching was operated by inductive coupled plasma (ICP) with argon ambient to remove the InP etching stop layer under the gate. Schottky gate metal, which was composed of Pt(12nm) /Ti(80nm) /Pt(60nm) /Au(180nm), was then deposited by electron beam evaporation. Gate metal will form after lift-off procedure by acetone and ZDMAC. An adequate time of Pt sinking annealing at 250℃ was controlled to obtain the optimal performance for these devices. Finally, 100-nm-thick silicon nitride layer was deposited by PECVD at 200℃ for 10 min for devices passivation.



SEM image of the 40-nm T-shaped gate is shown in Figure 5.1.2. As can be seen from SEM image, the fabricated 40-nm T-gate shows structural stability, even though the gate foot is narrow.

5.1.3 Result and discussion

Fig. 5.1.3 and Fig. 5.1.4 show the DC I-V curves of the 40 nm InAs QWFETs with and without two-step recess and Pt gate sinking processes. Due to the high carrier concentration of the InAs/$In_{0.53}Ga_{0.47}As$ composite channel material and the ultra low ohmic contact resistance of 0.02 Ω • mm measured by TLM method, the 40nm InAs QWFETs exhibit high drain current density. Although the drain current 1050 mA/mm (V_{DS} = 0.5 V, V_{GS} = 0 V) of devices without two-step recess and gate sinking processes is higher than the device with these techniques of 390 mA/mm, the devices with these techniques exhibit much better pinch-off and current saturation characteristics compared to the devices without using these techniques.

The threshold voltage (V_T) defined as the gate voltage at I_{DS} of 1mA/mm shifts to more positive side from -1.0V to -0.4V for device with two-step recess and gate sinking processes. Besides, due to the effective suppression of short channel effect by additional vertical shrinkage, the device with two-step recess and gate sinking processes shows better saturating current and lower output conductance characteristics.

The transconductance (g_m) and the drain-source current plotted as functions of gate-source voltage are shown in Fig. 5.1.5 and Fig. 5.1.6. The 40 nm InAs QWFETs exhibit very high transconductance which result from the high electron mobility of the InAs channel material. As observed from the figures, the threshold voltage and peak g_m of the devices with two-step recess and Pt gate sinking processes move toward more positive side, which are beneficial for devices of low power consumption applications. However, the trade-off of the reduction in gate-channel distance is the slightly lower $g_{m,max}$. $G_{m,max}$ for devices with and without two-step recess and gate sinking processes are 1650 mS/mm and 1750 mS/mm at V_{DS} = 0.5, respectively. The decrease in $g_{m,max}$ for devices with these two processes comes from the overall drops of drain-current density. And this phenomenon arises mainly from an increase in the source resistance as gate-channel thickness is scaled down, although other factors also appeared to be involved.

The S-parameters of the 40 nm InAs QWFETs were measured to 80 GHz using Cascade Microtech^{TM} on-wafer probing system with Anritsu 37369C vector network analyzer. Fig. 5.1.7 and Fig. 5.1.8 show the frequency dependence of the current gain (H_{21}) and the power gain (MAG/MSG) of the devices with/without two-step recess and gate sinking processes measured at V_{DS} = 0.5. The parasitic effects (mainly capacitive) due to the probing pads have been carefully removed from the measured S-parameters using the same method as in [5-4] and the equivalent circuit model in [5-5]. Since the geometry of the probing pads are relatively large compared to the device itself, the S-parameters of the open probing pads have been carefully characterized through full-wave electromagnetic simulations with

measurement. The value of current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are extracted by extrapolating current gain (H_{21}) and the power gain (MAG/MSG) with a -20dB/decade slope. A higher f_T of 440 GHz and f_{max} of 190 GHz are obtained for device with two-step recess and gate sinking processes as compared to the device without these processes which shows f_T of 395 GHz and f_{max} of 160 GHz. These improved RF performance mainly result from reduced gate-channel distance by the two-step recess and gate sinking processes. The reduction of gate-channel distance tends to suppress the short-channel effect and enhances the overshooting of electron velocity in channel. Table 5.1 summarizes the extracted intrinsic parameters for devices with/without two-step recess and gate sinking processes at same bias conditions. The increase of f_T can also be attributed to the decrease of total gate capacitance ($C_{g,total}$) and increase of the RF transconductance.

From the above results, the excellent DC and RF characteristics of 40 nm $InAs/In_{0.53}Ga_{0.47}As$ QWFETs can be achieved even at low applied voltage. Besides, by additional process improvements like two-step recess and gate sinking processes, the devices can exhibit much better performances. However, for millimeter wave and sub- millimeter wave applications, device with low noise generation is also a basic criterion. Therefore, the noise performance is required in this study. The noise performances for 40 nm $InAs/In_{0.53}Ga_{0.47}As$ QWFETs with two-step recess and gate sinking processes at V_{DS} = 0.5 V were measured and shown in Fig. 5.1.9. As seen from the figure, the overall minimum noise figure (NF_{min}) is below 2.5dB with frequency range from 1 GHz to 64 GHz, and the corresponding associated gain (Ga) is 7dB at 64GHz. The ultra-low dc power dissipation of 4.33mW was applied here.

Finally, the cutoff frequency (f_T) versus DC power consumption of the 40nm $InAs/In_{0.53}Ga_{0.47}As$ QWFETs with two-step recess and gate sinking processes are shown in Fig. 5.1.10. Meanwhile, the published data of 80 nm Si nMOSFETs [5-6] biased at 0.7 V are also included in this figure for comparison. We can conclude from the plot that InAs

channel-based QWFETs can achieve higher f_T under the same level of DC power consumption than Si nMOSFETs, this is because the InAs channel can provide better electron transport properties.

Overall, these superior results show great potential of 40 nm InAs/$In_{0.53}Ga_{0.47}As$ QWFETs for ultra low-power, high-frequency and low-noise RF applications.

5.1.4 Conclusion

In this study, the 40nm InAs/$In_{0.53}Ga_{0.47}As$ QWFETs using two-step recess and Pt gate sinking technologies to enhance DC & RF performances is demonstrated. By applying these two advanced processes, the gate electrode becomes much closer to the channel layer, thus avoids short channel effect and the electrons in the channel are further accelerated. By applying these processes, the devices exhibit improved behaviors at low V_{DS} such as better current saturation, lower output conductance (g_o), enhanced current driving capability, smaller negative threshold-voltage (V_T) and higher f_T and f_{max} (400 GHz and190 GHz).

The evaluations of InAs QWFETs with two-step recess and Pt gate sinking processes for high-gain and low-noise applications have also been investigated. The devices exhibit the minimum noise figure of lower than 2.5 dB up to 64GHz and with corresponding associated gain of 7 dB when biased at V_{DS} of 0.5 V.

Overall, these experimental results demonstrate that superior device performance for high-speed, low-noise and low-power millimeter/sub-millimeter wave applications can be achieved by using 40 nm InAs QWFET with two-step recess and Pt gate sinking technologies.

n^+ Cap Layer	$In_{0.53}Ga_{0.47}As$ ($2x10^{19}cm^{-3}$)	40 nm
Etching Stop Layer	InP	5nm
Barrier Layer	$In_{0.52}Al_{0.48}As$	5 nm
	Si δ-doping ($4x10^{12}cm^{-2}$)	-
Spacer Layer	$In_{0.52}Al_{0.48}As$	3 nm
Composite Channel	$In_{0.53}Ga_{0.47}As$	2 nm
	InAs	5 nm
	$In_{0.53}Ga_{0.47}As$	3 nm
Buffer Layer	$In_{0.52}Al_{0.48}As$	500 nm
3 inch S.I. InP Substrate		

Fig. 5.1.1 Epitaxial structure of InAs/$In_{0.53}Ga_{0.47}As$ QWFETs in this study

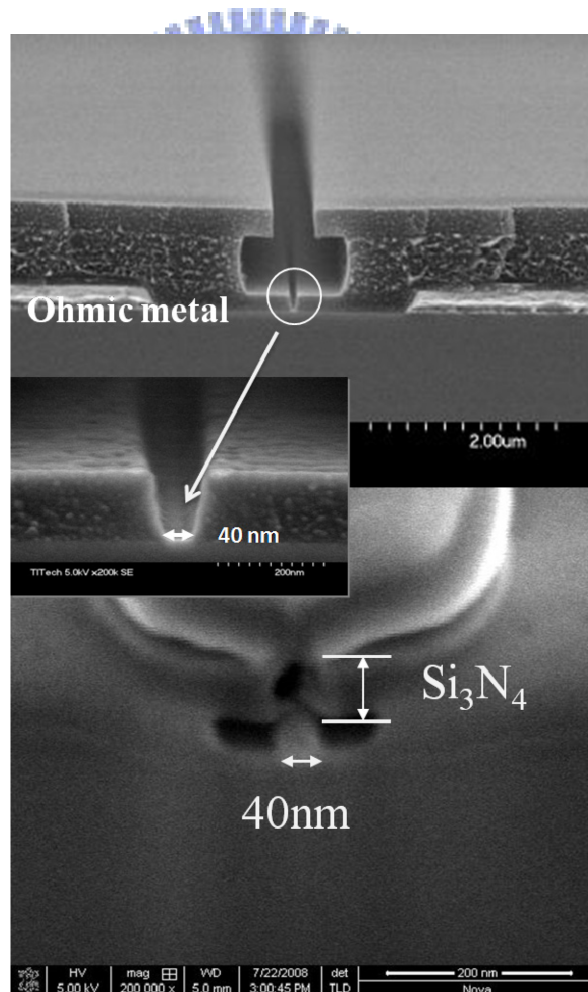


Fig. 5.1.2 SEM images of the 40 nm T-shaped gate photoresist and the finished 40 nm gate after the two-step recess process.

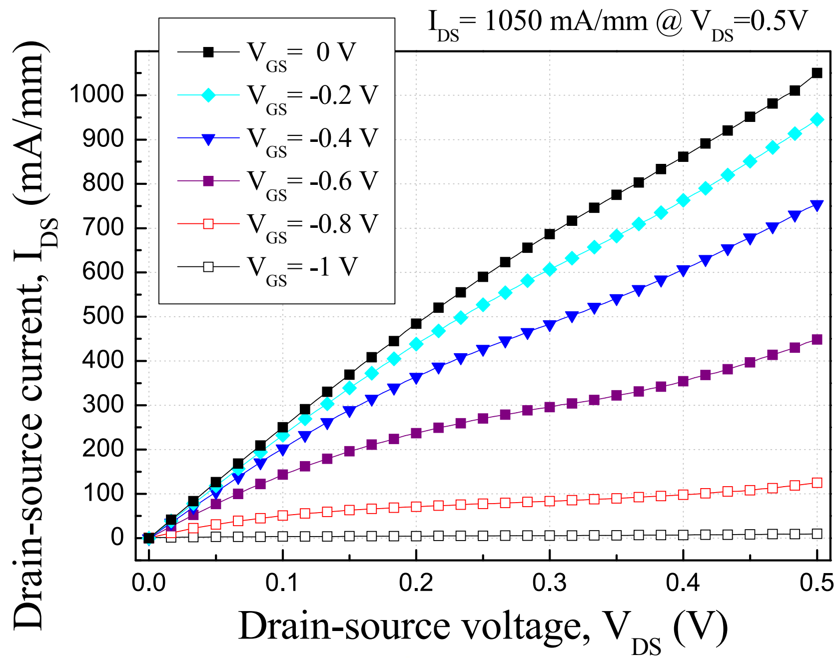


Fig. 5.1.3 Drain-source current versus drain-source voltage curves of 40nm InAs QWFET without two-step recess and gate sinking processes.

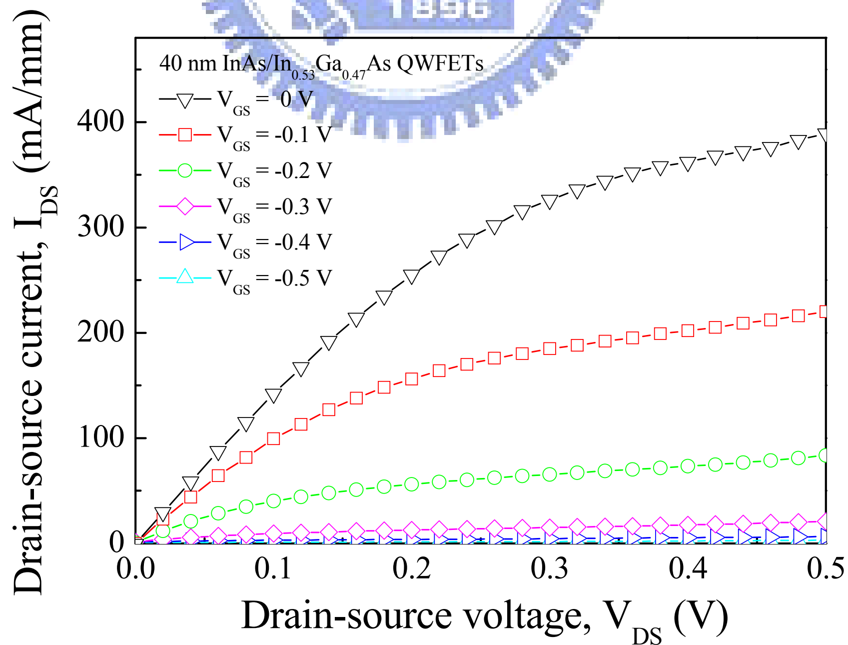


Fig. 5.1.4 Drain-source current versus drain-source voltage curves of 40nm InAs QWFET with two-step recess and gate sinking processes.

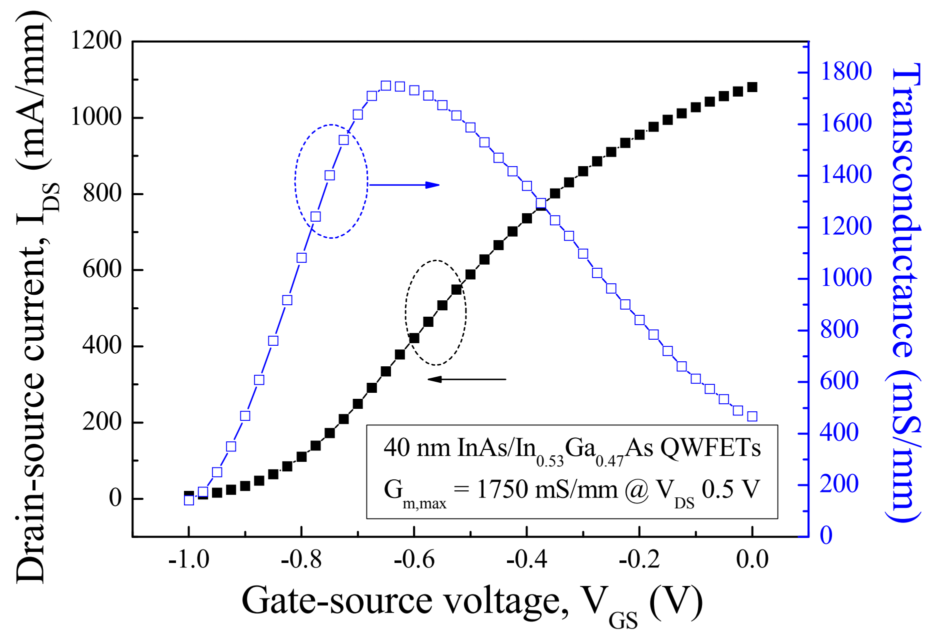


Fig. 5.1.5 Transconductance versus gate-source voltage of 40nm InAs QWFET without two-step recess and gate sinking processes.

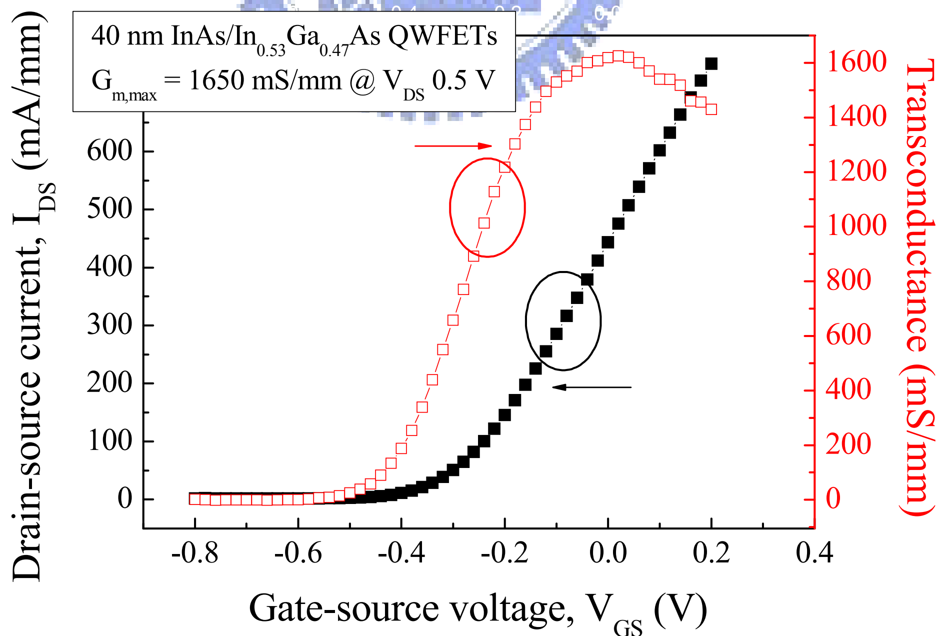


Fig. 5.1.6 Transconductance versus gate-source voltage of 40nm InAs QWFET with two-step recess and gate sinking processes.

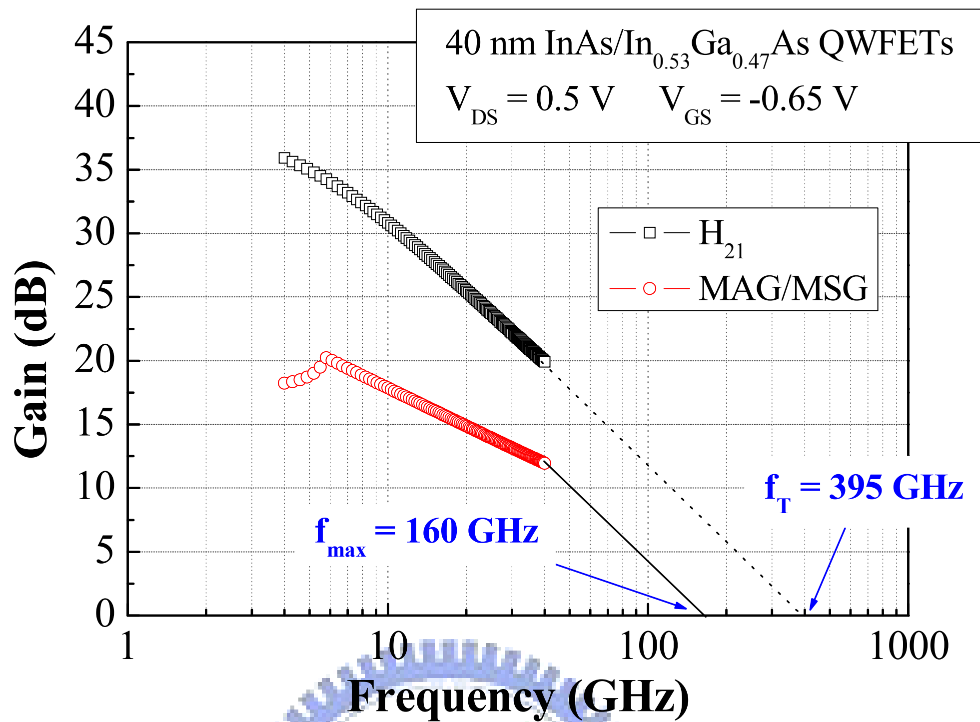


Fig. 5.1.7 Frequency dependence of the current gain (H_{21}) and the power gain (MAG/MSG) of 40nm InAs/$In_{0.53}Ga_{0.47}As$ composite channel QWFETs without two-step recess and gate sinking processes. The frequency range was from 4 to 40 GHz, and the device was biased at V_{DS} = 0.5V and V_{GS} = -0.65V.

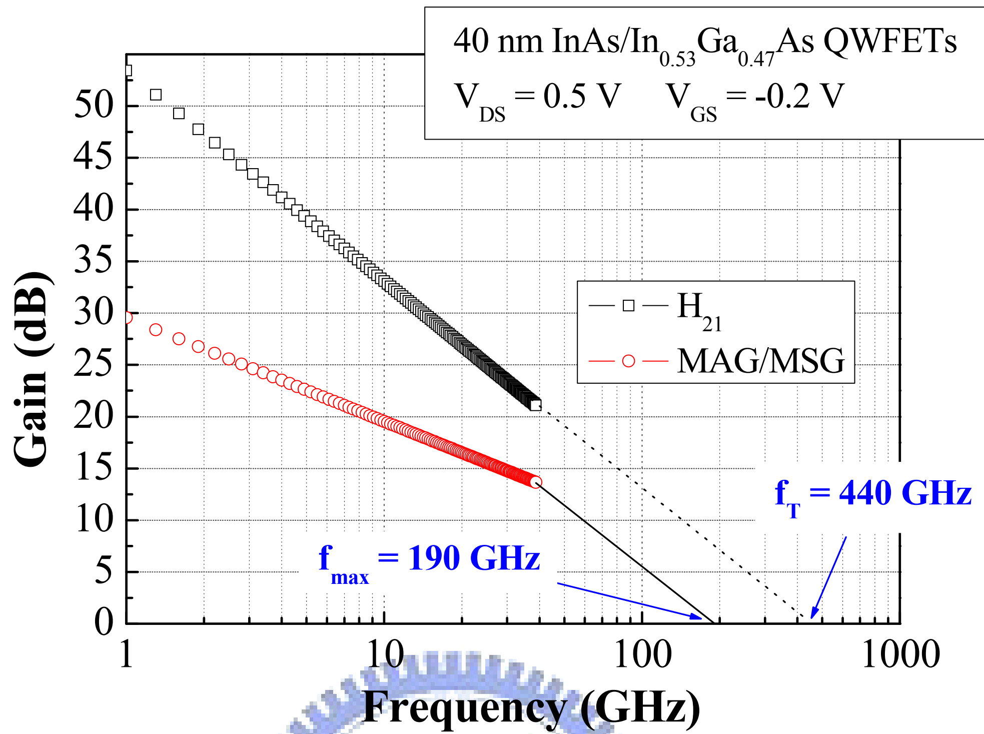


Fig. 5.1.8 Frequency dependence of the current gain (H_{21}) and the power gain (MAG/MSG) of 40nm InAs/$In_{0.53}Ga_{0.47}As$ composite channel QWFETs with two-step recess and gate sinking processes. The frequency range was measured to 40 GHz, and the device was biased at V_{DS} = 0.5V and V_{GS} = -0.2V.

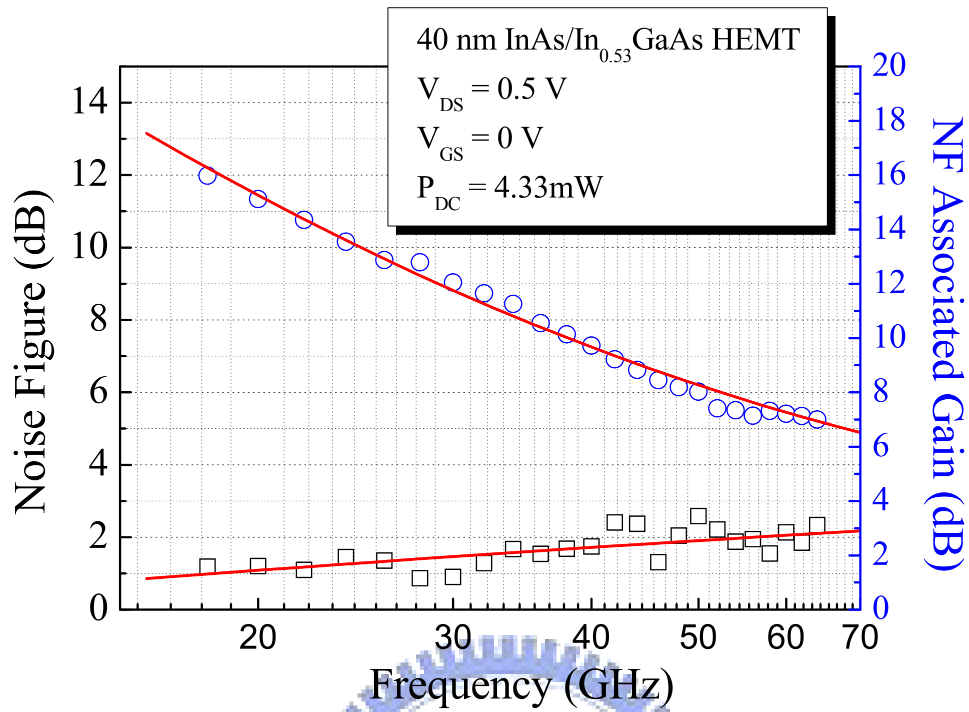


Fig. 5.1.9 Measured minimum noise figure (NF_{min}) and the associated gain of the 40nm InAs QWFETs with two-step recess and gate sinking processes at V_{DS} = 0.5V and the applying DC power was 4.33mW.

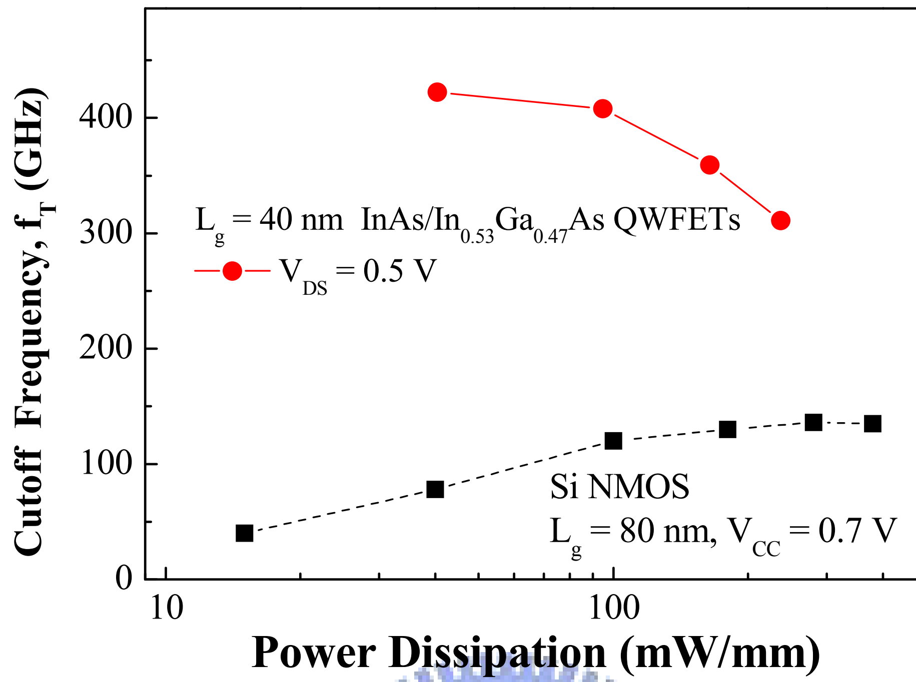
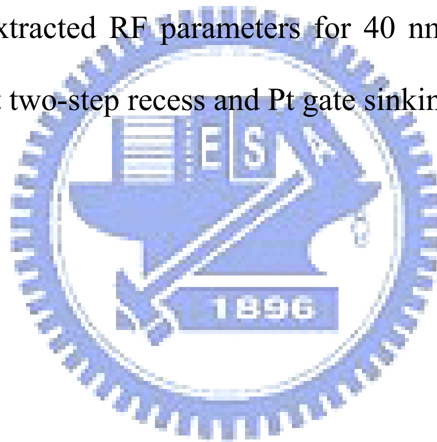


Fig. 5.1.10 Cutoff frequency of 40nm InAs QWFETs and 80 nm Si nMOSFETs as a function of the power dissipation

	$G_{m.RF}$ (mS)	C_{gs} (fF)	C_{gd} (fF)	$C_{g,total}$ (fF)	H_{21} @40GHz (dB)	f_T (GHz)	f_{max} (GHz)
Without	**190**	**29**	**48.4**	**77.4**	**19.9**	**395**	**160**
With	**196**	**37.7**	**33.3**	**71**	**20.83**	**440**	**190**

Table 5.1 Summary of extracted RF parameters for 40 nm InAs/$In_{0.53}Ga_{0.47}As$ QWFETs at V_{DS} of 0.5 V with/without two-step recess and Pt gate sinking processes.



5.2 Comprehensive Study of Impact Ionization Phenomena in 40 nm InAs-Channel Based QWFETs

5.2.1 Introduction

For the low-noise amplifier (LNA) monolithic microwave integrated circuit (MMICs) used in the next generation wireless communication systems [5-7], the devices with high speed, low-noise performances and low-power consumption are required. Among all electronic devices, InP-based InAlAs/InGaAs QWFETs with high indium content in transistor-channel are the most promising candidates for operating under millimeter-wave (30-300 GHz) and sub-millimeter wave (300 GHz- 3 THz) frequency bands, because of their extremely high channel electron mobility and high saturation velocity [5-8, 5-9]. Moreover, further reducing the gate length (L_g) and raising indium content in the $In_xGa_{1-x}As$ channel layer can improve the electron transport performance, because the average electron field under the gate is increased and the higher electron mobility characteristics of high indium content channel. K. Shinohara et al. reported a 562 GHz cutoff frequency (f_T) for 25-nm-gate HEMT with a channel In content of 0.7 [5-10], and S.J Yeon et al. reported a 610 GHz 15-nm-gate HEMT with a channel In content of 0.75 [5-11].

However, because of the narrow energy band-gap of high indium content channel material, the electrons acquiring large energy under high electron field might strike other atoms and break the lattice bonding so as to generate extra electron-hole pairs. The excess electron-hole pairs will also obtain sufficient energy so continuously impact and generate more and more electron-hole pairs. This phenomenon is called impact ionization. The number of the electron-hole pairs generated by impact ionization is proportional to the product of carrier concentration in the channel and the electron field dependent ionization coefficient [5-12]. Impact ionization phenomena will degrade the performance of the devices. It will

make III-V QWFETs suffer from severe I-V kink effect, high output conductance, high gate leakage current, low breakdown voltage, and the excess channel noise [5-13, 5-14].

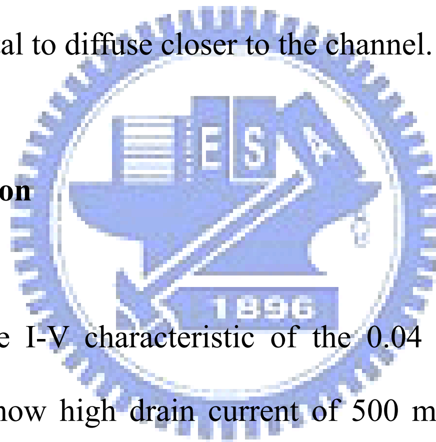
In this study, the 40 nm QWFETs were fabricated using two-step recess method and Pt-buried gate technique. The impact ionization phenomena of InAs/$In_{0.53}Ga_{0.47}As$ QWFETs are investigated. The device characteristics such as DC characteristics, noise figure (NF) and the RF performances are used to verify the impact ionization phenomena in this study. In addition, the optimum bias of InAs/$In_{0.53}Ga_{0.47}As$ QWFETs to prevent the impact ionization is also discussed.

5.2.2 Experiments

The epitaxial structure of QWFET in this study (Fig. 5.2.1) was grown by MBE on 2" semi-insulating InP substrate and the structure layers from bottom to top are composed of a 500-nm-thick $In_{0.52}Al_{0.48}As$ metamorphic buffer layer, a 3-nm-thick $In_{0.53}Ga_{0.47}As$ lower sub-channel, a 5-nm-thick InAs main channel, a 2-nm-thick $In_{0.53}Ga_{0.47}As$ upper sub-channel, a 3-nm-thick $In_{0.52}Al_{0.48}As$ spacer layer, a Si-doping layer (sheet density of 4×10^{12} cm^{-2}), a 5-nm-thick $In_{0.52}Al_{0.48}As$ barrier layer, a 5-nm-thick InP etching stop layer and a 40-nm-thick highly Si-doped $In_{0.53}Ga_{0.47}As$ cap layer (2×10^{19} cm^{-3}).

The device fabrication started from mesa isolation by wet chemical etching. The 2400 Å Au-Ge-Ni-Au ohmic contact metal was deposited and followed by rapid thermal annealing (RTA) at 250 ^{o}C for 30s so as to attain low contact resistance. The 600 Å SiN_x was deposited at 200 ^{o}C by PECVD as hard mask to fabricate the small L_g of 40 nm devices. In addition, the passivated SiNx was deposited in order to improve not only the mechanical strength of nano gate but also electric and thermal reliability. Then, the T-shaped gate lithography was carried out using 50-KV JEOL electron beam lithography system (JBX 6000FS) and the photoresist were tri-layer component polymer (ZEP-520/PMGI/ZEP-520). After development, the gate

foot was precisely replicated on the SiN_x layer by reactive ion etching (RIE) using CF_4 [5-15]. For gate recess etching, a two step recess process proposed by T. Suemitsu et al. [5-2] was used, and this allows the gate electrode to be closer to the channel so that the transconductance of the devices will be increased and short channel effect can be suppressed. For cap layer etching, solution mixed with succinic acid (SA), ammonia and hydrogen peroxide was used. And for the second recess of the InP etching stop layer and part of InAlAs schottky layer, Ar-based plasma by ICP was used. After recess, schottky gate metal, which was composed of Pt/Ti/Pt/Au (12/80/60/180nm), was deposited by electron beam evaporation. A 60-nm-thick SiN_x layer was deposited by PECVD at 200 ^oC for device passivation. Finally, annealing at 250 ^oC in forming gas ambient was carried out for Pt metal sinking process, which allows the gate metal to diffuse closer to the channel.



5.2.3 Result and discussion

Fig. 5.2.2 shows the I-V characteristic of the 0.04 μm x 40 μm $InAs/In_{0.53}Ga_{0.47}As$ QWFETs. The devices show high drain current of 500 mA/mm at low V_{DS} of 0.8 V with corresponding peak transconductance 1688 mS/mm, and the threshold voltage defined as drain current of 1 mA/mm is -0.48 V. This high drain current performance is attributed to the high electron concentration of InAs channel and great ohmic contact formation. It is noted that the drain current tends to increase drastically at larger V_{DS}, and the corresponding output conductance curves in Fig. 5.2.3 also show these trend. The primary reason for this kind of phenomena is attributed to the excess electron-hole pairs generation in the InAs channel by impact ionization. The measured total gate current in this study is shown in Fig. 5.2.4. The total gate current in the QWFETs include the Schottky gate leakage current and impact ionization induced hole current of the thermionic effect as well as tunneling effect [5-16]. As

observed in Fig. 5.2.4, the total gate current increases when $V_{DS} > 1.0$ V and there exists a humped curve at $V_{GS} = 0$ V ~ -0.4 V. This humped curve behavior has been proved to be associated with the impact ionization induced gate hole current [5-17]. The impact ionization induced gate leakage current is related to two factors, one is carrier concentrate in the channel and the other is gate-bias dependent ionization coefficient and hole transmission probability. And the humped shape curve happened at intermediate bias between $V_{GS} = 0$ V and largely negative V_{GS} is due to both of these two factors are significant in this gate bias.

The minimum noise figure (NF_{min}) and associated gain (Ga) at different V_{DS} as a function of the frequency up to 64 GHz was measured and is shown in Fig. 5.2.5. The measured minimum noise figure of the 40 nm InAs QWFETs at 64 GHz is around 2 dB with the corresponding gain of 7 dB for V_{DS} of 0.5 V. This superior behavior is attributed to the high transconductance, short gate length and the suppression of the short channel effect. Besides, the overall NF_{min} is found to be lower than 3 dB at V_{DS} less than 0.8 V. It can be observed that there're no distinct variations of NF_{min} in low V_{DS} from 0.5 to 0.8 V. But the drastically increase of NF_{min} is exhibited at V_{DS} of 1.0 V. The explanation of these phenomena is the contribution of generated excess channel noise at high electron field by impact ionization induced electron-hole pairs and their further recombination. Furthermore, there exists another phenomenon, that is the NF_{min} curve of $V_{DS} = 1.0$ V doesn't increase in the high-frequency region, the reason is the small time constant of the impact ionization fluctuation [5-14]. In the high impact ionization region, it is likely that the generated carriers cannot catch up with the high frequency switching, so the generated excess channel noise have short time constant.

To further understand the effects of the impact ionization on the InAs QWFETs in high frequency region, the S-parameter of the devices was measured. The S-parameter measurement was performed using Cascade Microtech on-wafer probing system with

HP8510XF vector network analyzer from 1 to 80 GHz. Additionally, a standard Load-Reflection-Reflection-Match (LRRM) calibration method was used to calibrate the measurement system, and the calibrated reference planes were at the tips of the corresponding probes. The parasitic effects (mainly capacitive) from the probing pads have been carefully removed from the measured S-parameters using the same method as in [5-4] and the equivalent circuit model in [5-5]. Since the geometry of the probing pads are relatively large compared to the device itself, the S-parameters of the open probing pads have also been rigorously characterized through full-wave electromagnetic simulations with measurement.

The current gain (H_{21}) and maximum available/stable gain (MAG/MSG) as a function of frequency are plotted in Fig. 5.2.6(a). The extracted current cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are 663 GHz and 334 GHz at drain bias of 0.9 V, respectively, by extrapolating H_{21} and MAG/MSG with a -20dB/decade slope. The high f_T is mainly due to the short gate-channel distance by using two-step gate recess process and biasing at high drain voltage resulting in high drift velocity. Fig. 5.2.6(b) shows the f_T and f_{max} with different V_{DS} after the pad parasitic were de-embedding. The f_T increases with the increase of V_{DS}, but reaches the maximum value of 663 GHz at V_{DS} = 0.9 V then decrease to 517 GHz at V_{DS} = 1.0 V. The main reason for the performance degradation is due to the generated impact ionization carriers could not keep up with the electrical field modulation at high frequencies especially at high V_{DS}. The extracted gate capacitance from S-parameter is listed in table 5.2. The parasitic gate capacitance (C_G) including gate to source capacitance (C_{GS}) and gate to drain capacitance (C_{GD}) diminish with the V_{DS} from 0.5 V to 0.9 V but increase at V_{DS} = 1.0 V. Apparently, peak f_T occurred at minimum C_G near the occurrence of impact ionization. Qualitatively, impact ionization mechanism tends to generate electron-hole pairs in the channel and part of the generated holes flowing into gate electrode may recombine with electrons to form gate currents. Thus, the total amount of charges at the gate area

decreased due to the recombination process leading to a sudden decrease in C_G. Such observation indicated that for such low energy bandgap devices, maximum f_T can be obtained if the device is biased near the occurrence of impact ionization.

From these investigations, it can be concluded that for the 40 nm $InAs/In_{0.53}Ga_{0.47}As$ composite channel QWFETs, the drain voltage should be biased at less than 0.9 V to prevent the performance degradation by impact ionization.

5.2.4 Conclusion

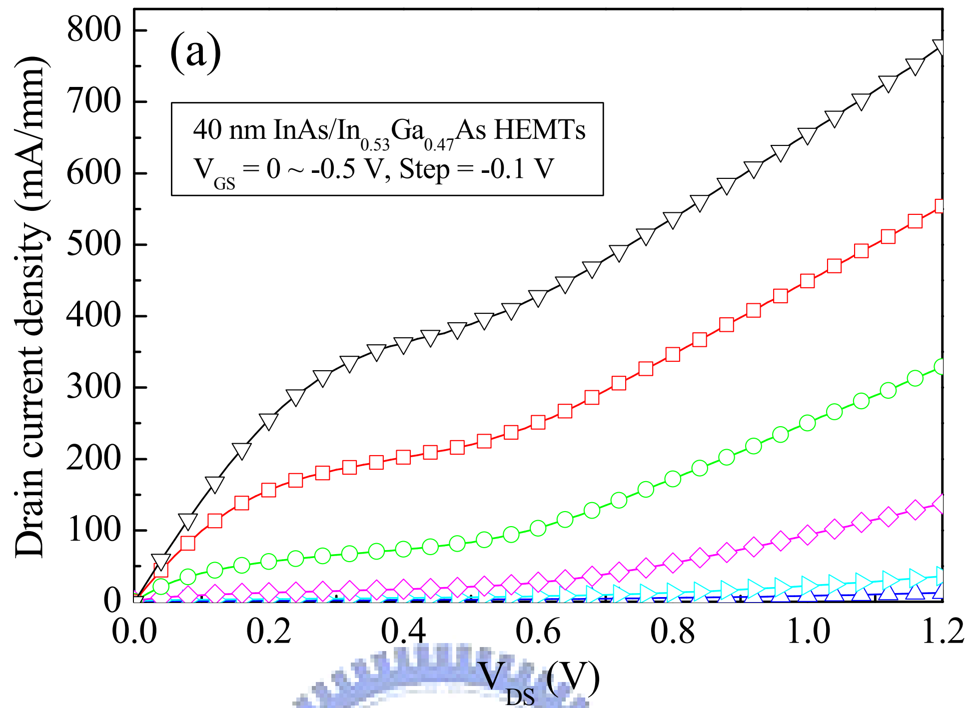
In this study, the experimental investigation of impact ionization phenomena of 40 nm $InAs/In_{0.53}Ga_{0.47}As$ channel QWFETs through DC, noise and S-parameter measurement is performed. When biased at too high voltage, the performance of InAs devices will degrade due to impact ionization. The devices show high output conductance with the increase in V_{DS}. Humpy shape is observed for the gate leakage current curve at V_{DS} higher than 1.0 V. And the minimum noise figure increase drastically at V_{DS} = 1.0 V which is also an apparent evidence of the occurrence of impact ionization. Based on the S-parameter measurement, the f_T of the InAs QWFETs increase to 663 GHz at V_{DS} = 0.9 V and decrease to 517 GHz at V_{DS} = 1.0 V. The degradation of the high frequency performance is due to the impact ionization carriers could not keep up with the electrical field modulation at high frequencies. This phenomenon matches well with the extracted gate capacitance.

However, it is necessary to find the right bias point so that the optimum device performance can be achieved. The devices show transconductance over 1500 mS/mm at V_{DS} = 0.5 V. Besides, the device showed a low noise figure of less than 3 dB with an associated gain of 7 dB up to 64 GHz at V_{DS} of 0.8 V. And the extremely high f_T of 663 GHz is obtained if the device is biased near the occurrence of impact ionization. Therefore, with optimum bias

conditions, such InAs devices show tremendous potential in future high-speed sub-millimeter wave applications.

Layer	Material	Thickness
n^+ Cap Layer	$In_{0.53}Ga_{0.47}As$ ($2x10^{19}cm^{-3}$)	40 nm
Etching Stop Layer	InP	5nm
Barrier Layer	$In_{0.52}Al_{0.48}As$	5 nm
	Si δ-doping ($4x10^{12}cm^{-2}$)	-
Spacer Layer	$In_{0.52}Al_{0.48}As$	3 nm
Composite Channel	$In_{0.53}Ga_{0.47}As$	2 nm
	InAs	5 nm
	$In_{0.53}Ga_{0.47}As$	3 nm
Buffer Layer	$In_{0.52}Al_{0.48}As$	500 nm
3 inch S.I. InP Substrate		

Fig. 5.2.1 Epitaxial structure of InAs/$In_{0.53}Ga_{0.47}As$ composite channel QWFETs in this study



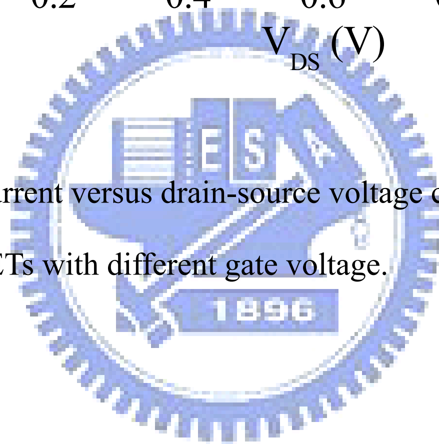


Fig. 5.2.2 Drain-source current versus drain-source voltage curves of InAs/$In_{0.53}Ga_{0.47}As$ composite channel QWFETs with different gate voltage.

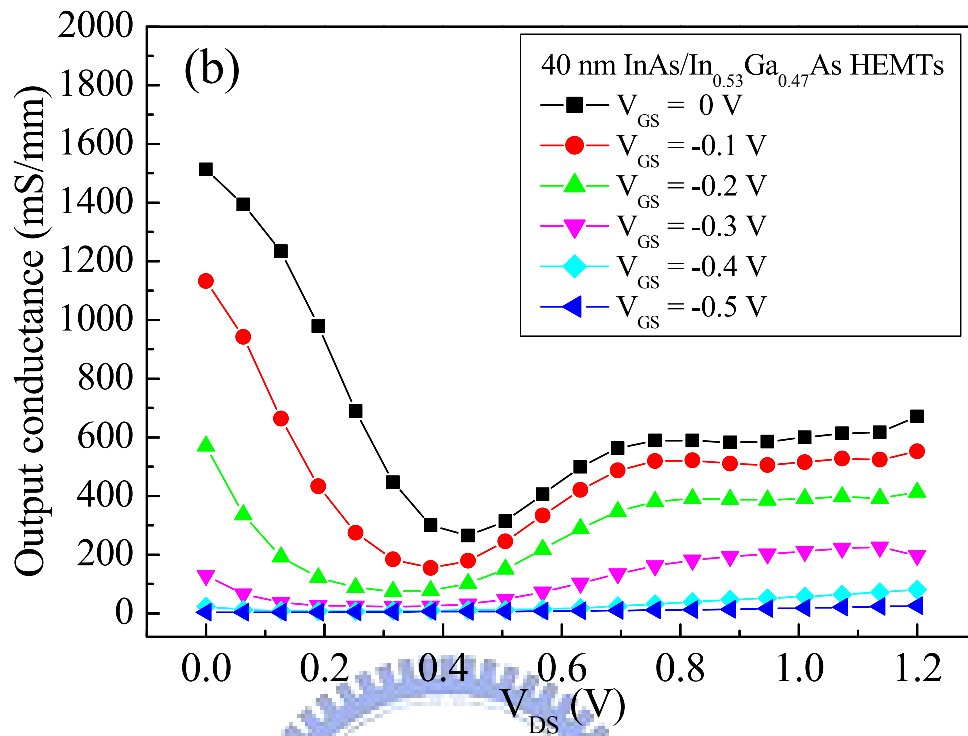
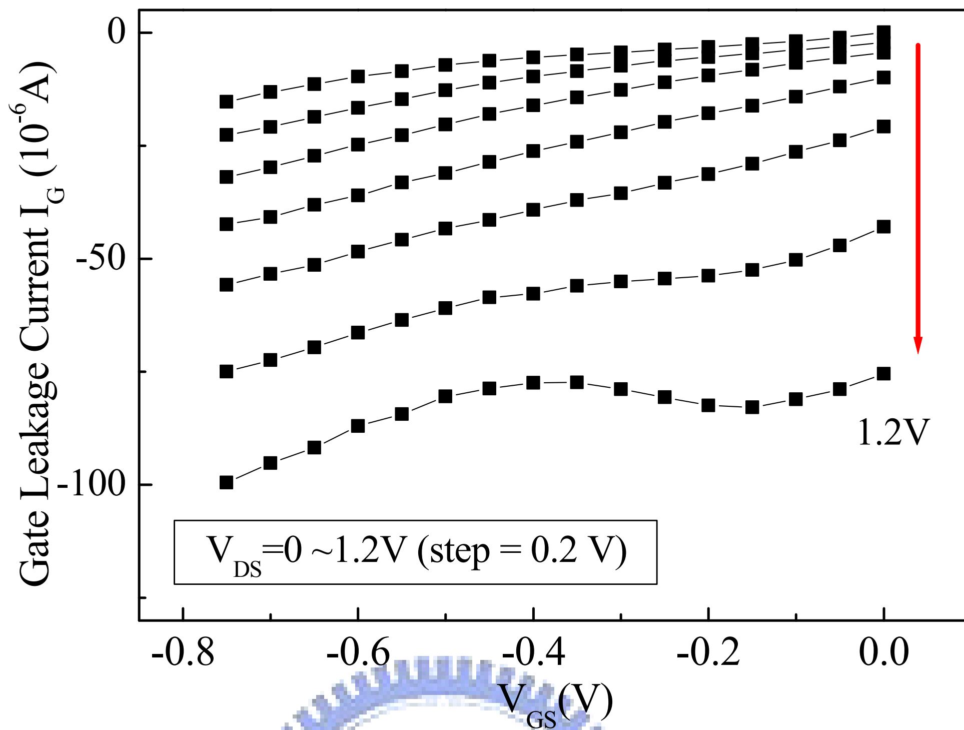


Fig. 5.2.3 Output conductance of $InAs/In_{0.53}Ga_{0.47}As$ composite channel QWFETs as a function of drain voltage with different gate voltage.



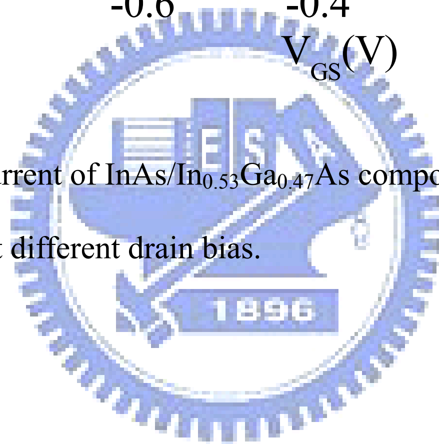
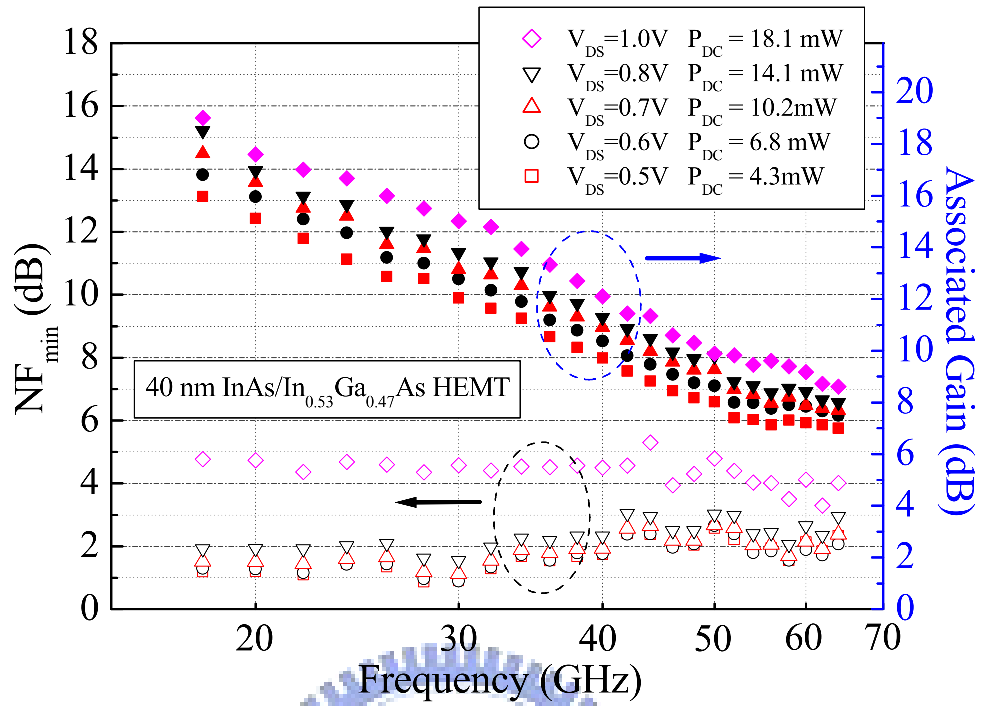


Fig. 5.2.4 Gate leakage current of InAs/$In_{0.53}Ga_{0.47}As$ composite channel QWFETs as a function of gate voltage at different drain bias.



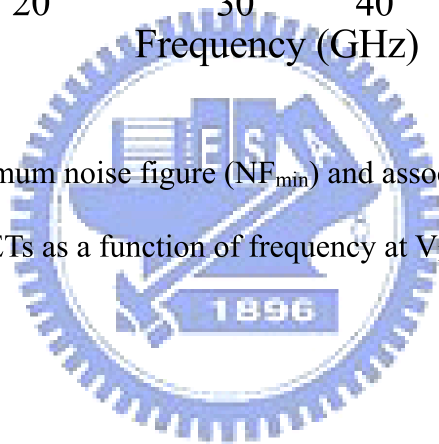
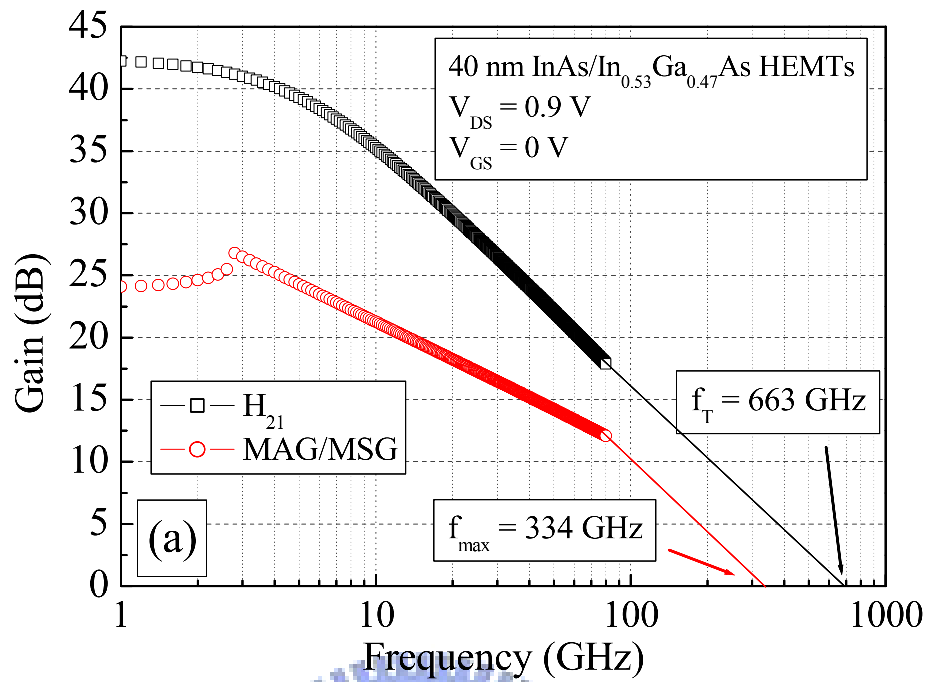


Fig. 5.2.5 Measured minimum noise figure (NF_{min}) and associated gain of InAs/$In_{0.53}Ga_{0.47}As$ composite channel QWFETs as a function of frequency at V_{DS} = 0.5-1.0 V.



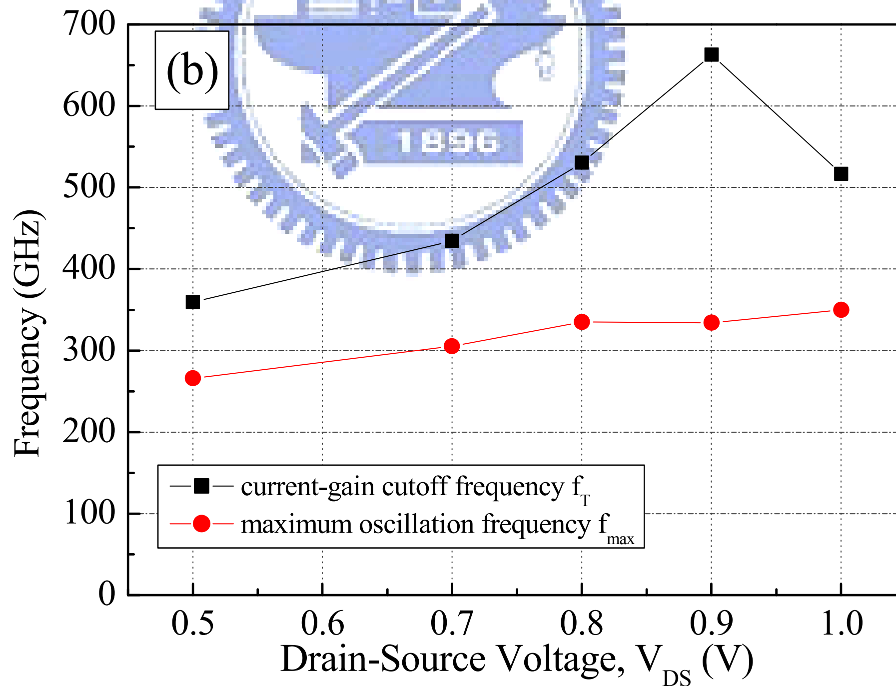


Fig. 5.2.6 (a) The current gain (H_{21}) and maximum available (stable) gain (MAG/MSG) as a function of frequency at V_{DS} = 0.9 V. (b) The f_T and f_{max} versus drain voltage at gate bias of 0 V.

V_{DS}	**0.5V**	**0.7V**	**0.8V**	**0.9V**	**1.0V**
C_{GS}(fF)	49.7	50.9	41.9	26.5	43.7
C_{GD}(fF)	37.8	31.9	29.3	28	28.7
$C_{G,total}$(fF)	87.5	82.8	71.2	54.5	72.4

Table 5.2 Extracted intrinsic capacitances of a 0.04 μm × 40 μm $InAs/In_{0.53}Ga_{0.47}As$ QWFETs with different drain-source voltage.

5.3 Evaluation of 40 nm InAs-Channel Based QWFETs for High-Performance and Low-Voltage Logic Applications

5.3.1 Introduction

For device scaling in Si technology, the physical gate length of Si transistors used in current 65 nm node generation is about 30 nm and the size is expected to reach the limitation of 10 nm in 2011. The International Technology Roadmap of Semiconductors Winter Public Conference 2007 (ITRS 2007) forecasted that integration of planar III-V compound semiconductor FETs with Si technology is one of the promising solutions for the CMOS technology to extend Moore's law [5-18] ~ [5-22]. Generally, III-V materials have about 50 to 100 times higher electron mobility than Si, and the extremely high transconductance and excellent RF performance have been demonstrated recently using InAlAs/InGaAs MHEMTs on GaAs substrate or InP substrate with ultra short gate length [5-11, 5-23].

In addition to high speed performance, low DC power consumption is also a highly desired property for practical system applications. However, maintaining device performance in high-speed digital applications within low drain bias can only be achieved through specific device technology. Having the properties of high electron mobility (20,000 cm^2/Vs) at room temperature, high electron peak velocity, low electron effective mass and a reasonable energy bandgap (0.36 eV) in low bias; InAs materials have attracted numerous attentions as channel layer of QWFETs for future high-speed and low-power digital applications [5-24].

In this study, 40 nm $InAs/In_{0.7}Ga_{0.3}As$ composite channel QWFETs were fabricated and evaluated. The devices demonstrate excellent electrical and logic performances in low applied voltage, indicating the suitability for ultra-high speed and low voltage digital applications.

5.3.2 Experiment

The structure of InAs-channel QWFET (Fig. 5.3.1) used in this study was grown by Molecular Beam Epitaxy (MBE) on InP substrate. The epi-layer, from bottom to top, comprise a 500 nm $In_{0.52}Al_{0.48}As$ buffer layer, a 3 nm $In_{0.7}Ga_{0.3}As$ lower sub-channel, a 5 nm InAs channel, a 3 nm $In_{0.7}Ga_{0.3}As$ upper sub-channel, a 14 nm $In_{0.52}Al_{0.48}As$ schottky layer with planar σ doping (5×10^{12} cm^{-2}), a 4 nm InP etching stop layer, and a 35 nm si-doped $In_{0.53}Ga_{0.47}As$ cap layer (2×10^{18} cm^{-3}).

The device isolation was done by mesa isolation using wet chemical etching. Source and drain ohmic metals (Au/Ge/Ni/Au) were deposited and alloyed by rapid thermal annealing (RTA) at 250 ^{o}C for 30 s. The 40 nm T-shaped gate was carried out in JEOL electron beam system with 100 pA beam current and a conventional ZEP/PMGI/ZEP tri-layer photoresist was used. Gate recess was performed by novel two-step-recess process technique. A 60 nm SiNx film deposited before EB photoresist was etched by Inductive Couple Plasma system (ICP) using the gas mixture of SF_6 and Ar. After the etching of SiNx, the heavily doped $In_{0.53}Ga_{0.47}As$ cap layer was removed by succinic acid-based solution. For second step recess, Ar plasma was used to etch the InP etch-stop layer and part of the InAlAs schottky layer. The Pt/Ti/Pt/Au (120/800/600/1800Å) gate metal was formed by electron gun evaporation and lift off process. In order to attain gate stability and a short distance between channel and gate electrode, the devices were annealed at 250 ^{o}C for 10 min in a forming gas ambient. Finally, the passivated SiNx film was applied to improve not only the mechanical strength of nano gate but also thermal stability and electric reliability.

5.3.3 Result and discussion

Fig. 5.3.2 shows the measured current-voltage characteristics of the 0.04×50 m^2 InAs QWFETs. As observed from the figure, the device can be well pinched-off through the applications of two-step recess and Pt gate sinking process. And the threshold voltage (V_T) defined as the gate bias of I_{DS} = 1 mA/mm is -0.2 V. The drain-source current reaches 420 mA/mm at V_{DS} = 0.5 V and V_{GS} = 0 V. The ohmic contact resistance (R_C) and sheet resistance measured by transmission line model method are 0.05 Ω・mm and 36.3Ω/□, respectively. The transconductance (g_m) and the I_{DS} versus V_{GS} with various V_{DS} are shown in Fig. 5.3.3. The g_m of nearly 2000 mS/mm can be achieved at low V_{DS} of 0.5 V. The extremely high transconductance is attributed to high electron mobility in the InAs/$In_{0.7}Ga_{0.3}As$ composite channel and the applications of two-step recess as well as Pt gate sinking process which bring about the effective reduction of gate-channel distance so as to accelerate the channel electrons. These results indicate that the InAs-channel QWFETs can be biased at a low supply voltage to reduce overall dc power consumption, while maintaining relatively high current density and transconductance. The two terminal gate-to-drain breakdown voltage (BV_{GD}) was measured to be -2.8 V (Fig. 5.3.4), defined as I_{GD} = -1mA/mm.

The S-parameter of the device was measured using Cascade Microtech^{TM} on-wafer probing system with HP8510XF vector network analyzer from 5 to 80 GHz. A standard Load-Reflection-Reflection-Match (LRRM) calibration method was used to calibrate the measurement system and the calibrated reference planes at the tips of the corresponding probes. The parasitic effects (mainly capacitive) from the probing pads have been carefully removed from the measured S-parameters using the same method as in [5-4] and the equivalent circuit model in [5-5]. Since the geometry of the probing pads are relatively large compared to the device itself, the S-parameters of the open probing pads have also been rigorously characterized through full-wave electromagnetic simulations with measurement.

For RF measurements, the optimal DC bias must be found to obtain the maximum current gain and power gain. Fig. 5.3.5 shows the I_{DS} and V_{DS} dependence of current gain cut-off frequency (f_T) curves. From the figure, 40nm InAs QWFET can exhibit f_T exceeding 340 GHz at V_{DS} = 0.5 V. Additionally, when drain bias is 1V, the extracted f_T can achieve extremely high frequency of 506 GHz and maximum oscillation frequency (f_{max}) is 285 GHz (Fig. 5.3.6). Apparently, the excellent f_T is owing to the extremely high transport properties of 40 nm InAs QWFETs. Fig. 5.3.7 compares the cutoff frequency (f_T) of the 40 nm InAs QWFETs in this study to the published 60nm and 80 nm Si MOSFETs [5-6, 5-25] under different DC power consumption. The InAs channel-based QWFETs can achieve much higher f_T under the same level of DC power consumption since the InAs channel can provide better electron transport properties.

Based on the high speed performance mentioned above, the advanced evaluations of 40 nm InAs QWFETs for high speed logic applications have also been investigated in this study. The analytical procedure as proposed by R. Chau, et. al. [5-18] is adopted for the evaluations of digital performance of non-optimized V_T device in order to avoid possible errors and physically meaningless values of logic parameters. The threshold voltage (V_T) defined as the gate bias of I_{DS} = 1 mA/mm. And the on-state and off-state current are defined as the I_{DS} at V_{GS} of 2/3(V_{DS}) above V_T and 1/3(V_{DS}) below V_T. Fig. 5.3.8 shows the sub-threshold characteristics of the device with different drain biases. Drain Induced Barrier Lowering (DIBL), which measures the change in V_T as a result of a change in V_{DS}, is calculated to be 50 mV/V at V_{DS} = 0.5 V. This small DIBL correlates with an overall insensitivity of V_T to circuit design details and manufacturing variations. The sub-threshold slope (S) of this device at V_{DS} = 0.5 V is 89 mV/dec, which represents the switch transition of the device is steep. The sharp sub-threshold characteristics result in an I_{ON}/I_{OFF} ratio of 2.16 x 10^3.

Device capacitance impacts the switching speed. The important figure of merit for logic transistors in high speed operation, the intrinsic gate delay ($C_{total}V/I_{ON}$), has also been

investigated. According to the definition, C_{total} is the total gate capacitance including gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}) extracted from high-frequency S-parameter measurement at corresponding bias conditions. V and I_{ON} are the applied drain voltage and on-state current, respectively. As observed from definition, the gate delay is strongly dependent on the choice of the threshold voltage. So J. Guo at Florida University proposed the methodology [5-26] to explore suitability of novel logic devices with non-optimized V_T which is shown in Fig. 5.3.9. The extracted intrinsic gate delay as a function of the defined threshold voltage (V_T') as defined by J. Guo is shown in Fig. 5.3.10. It is observed that the device yields a very low gate delay time of 0.62 psec at 0.5 V drain bias with V_T' = - 0.13 V. And gate delay time for threshold voltage of V_{GS} at I_{DS} = 1mA/mm in common III-V device definition is less than 1 psec. These low intrinsic gate delay values are attributed to the extremely high transport properties of InAs QWFETs. Fig. 5.3.11 shows the comparison of intrinsic gate delay as a function of gate length for different device technologies [5-18,5-20]. It is clear that the InAs QWFETs exhibit lower gate delay time than the state-of-the-art Si n-channel MOSFETs, indicating the excellent electronic characteristics and the high probability of such devices for high speed logic applications.

Fig. 5.3.12 shows the I_{ON}/I_{OFF} current ratio as function of various V_T'. The peak I_{ON}/I_{OFF} ratio of excess 10^3 almost coincides with V_T definition of 1 mA/mm, which can demonstrate that this definition for InAs QWFETs has enough physical meaning in the logic performance analysis.

The comparisons of 40 nm InAs QWFETs, 200 nm InSb QWFETs [5-20] and advanced 40 nm Si MOSFET [5-18] between gate delay time and I_{ON}/I_{OFF} ratio were plotted in the Fig. 5.3.13. This kind of plot allows the comparison of devices that have non-optimized threshold voltage. The InAs QWFETs exhibit far better I_{ON}/I_{OFF} ratio than the InSb QWFETs while maintaining the same sub-picosecond gate delay time. And another important consideration is that the InAs QWFETs deliver excellent logic gate delay time and high I_{ON}/I_{OFF} ratio at the

same time. However, due to the off-state current of InAs QWFETs are not low enough, resulting from band-to-band tunneling (BTBT) in such small energy band gap and the gate leakage current through the schottky gate, the comparable I_{ON}/I_{OFF} ratio to Si MOSFET is not achieving yet. Further improvement such as insertion of high-k gate dielectric materials between the metal gate and the III-V device layers for solving leakage problem is still in research.

5.3.4 Conclusion

The 40 nm InAs/$In_{0.7}Ga_{0.3}As$ composite channel QWFETs have been fabricated and evaluated for high-performance and low-voltage logic applications. The devices exhibited high speed characteristics in g_m of 2000 mS/mm, and f_T of 350 GHz at low drain bias voltage (V_{DS} = 0.5 V). With further investigation of digital performance, these devices show excellent logic performance at low drain bias voltage (V_{DS} = 0.5 V) through reducing insulator thickness and using high schottky barrier height Pt gate metal. The drain induced barrier lowering (DIBL) is 50 mV/V, subthreshold swing (S) is 89mV/decade, and intrinsic gate delay (CV/I_{ON}) is 0.62 psec. When comparing to the updated Si technology, the InAs QWFETs exhibit smaller gate delay time and higher cutoff frequency than Si nMOSFET. Besides, InAs QWFETs show much higher I_{ON}/I_{OFF} performance than InSb QWFETs. These results demonstrated that the InAs channel-based QWFETs are potential candidates for high-speed and low-voltage logic applications in the post-Si generation.

n^+ Cap Layer	$In_{0.53}Ga_{0.47}As$ ($2x10^{18}cm^{-3}$)	35 nm
Etching Stop Layer	InP	4nm
Barrier Layer	$In_{0.52}Al_{0.48}As$	10 nm
	Si δ-doping ($5x10^{12}cm^{-2}$)	-
Spacer Layer	$In_{0.52}Al_{0.48}As$	4 nm
Composite Channel	$In_{0.7}Ga_{0.3}As$	2 nm
	InAs	5 nm
	$In_{0.7}Ga_{0.3}As$	3 nm
Buffer Layer	$In_{0.52}Al_{0.48}As$	500 nm
3 inch S.I. InP Substrate		

Fig. 5.3.1 Epitaxial structure of $InAs/In_{0.7}Ga_{0.3}As$ composite channel QWFETs in this study

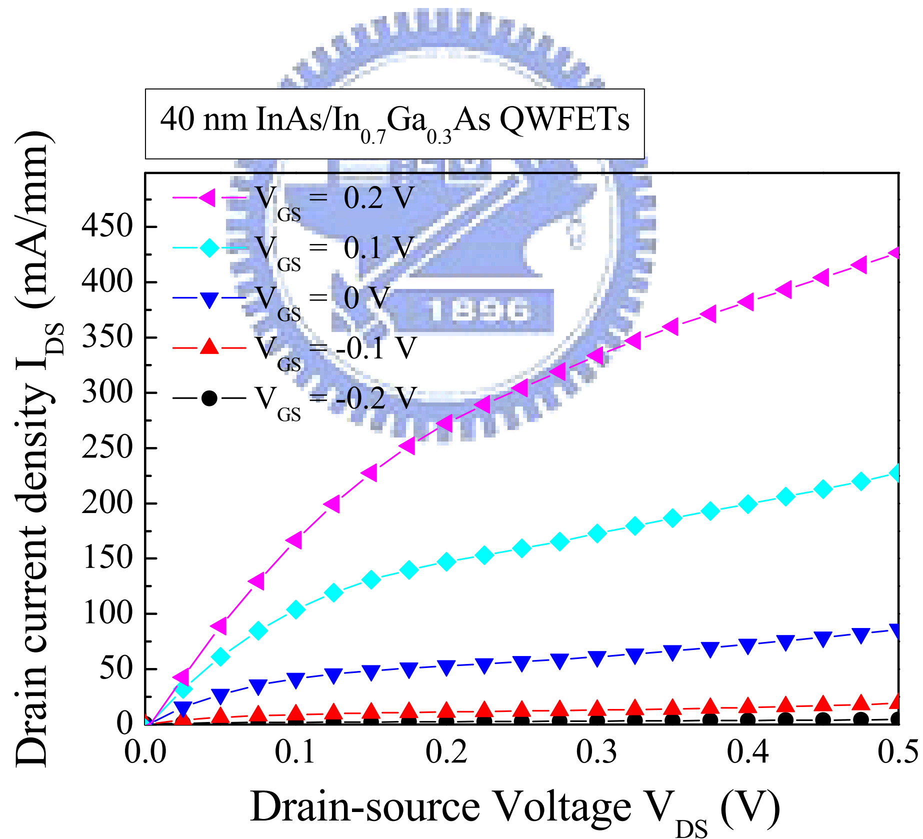
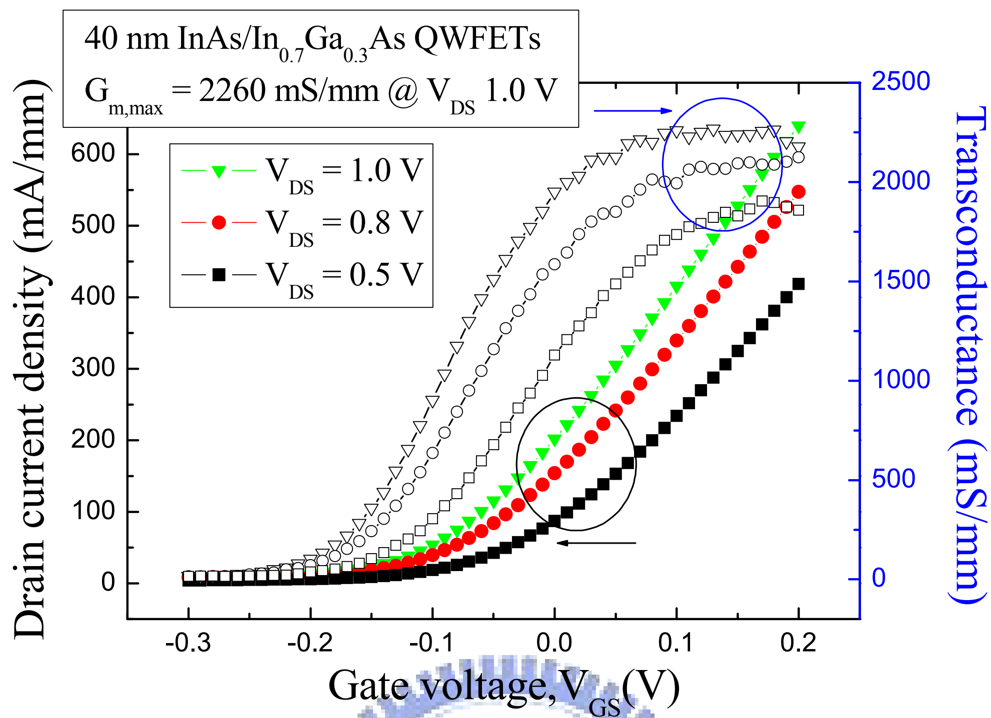


Fig. 5.3.2 Drain-source current versus drain-source voltage curves for 40nm $InAs/In_{0.7}Ga_{0.3}As$ QWFET with two-step recess and gate sinking process.



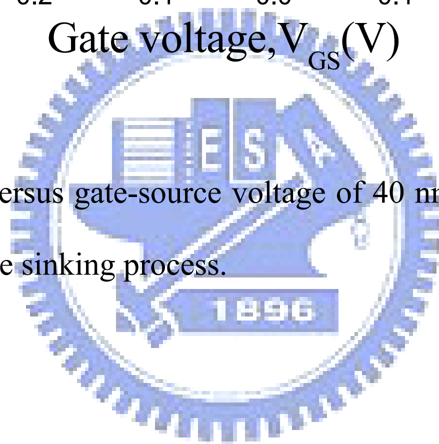


Fig. 5.3.3 Transconductance versus gate-source voltage of 40 nm $InAs/In_{0.7}Ga_{0.3}As$ QWFET with two-step recess and Pt gate sinking process.

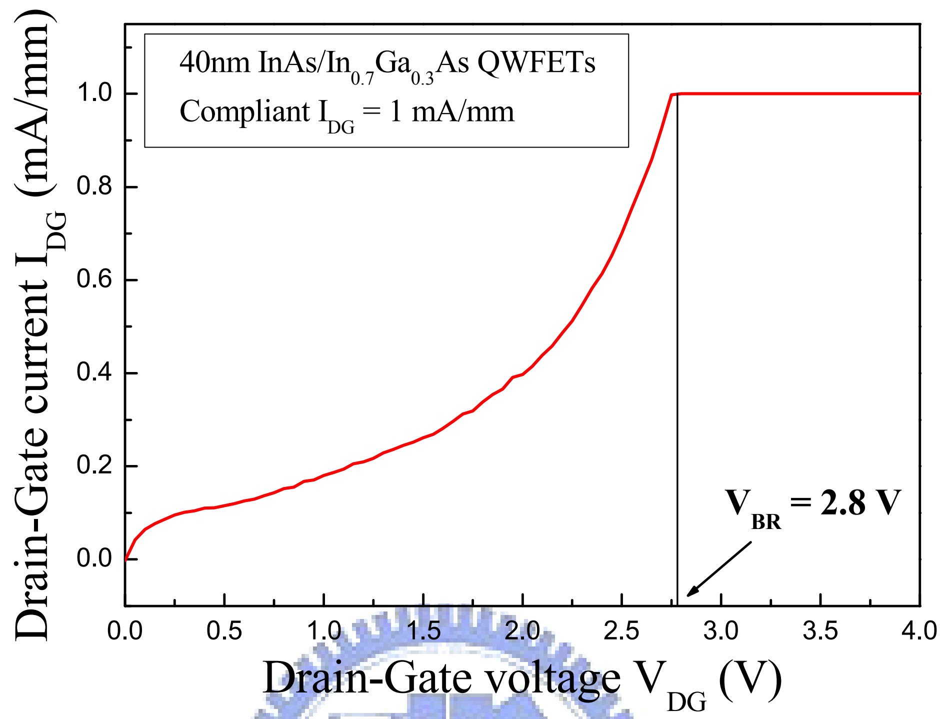


Fig. 5.3.4 Two terminal gate-drain breakdown characteristics of 40nm $InAs/In_{0.7}Ga_{0.3}As$ QWFET with two-step recess and gate sinking process.

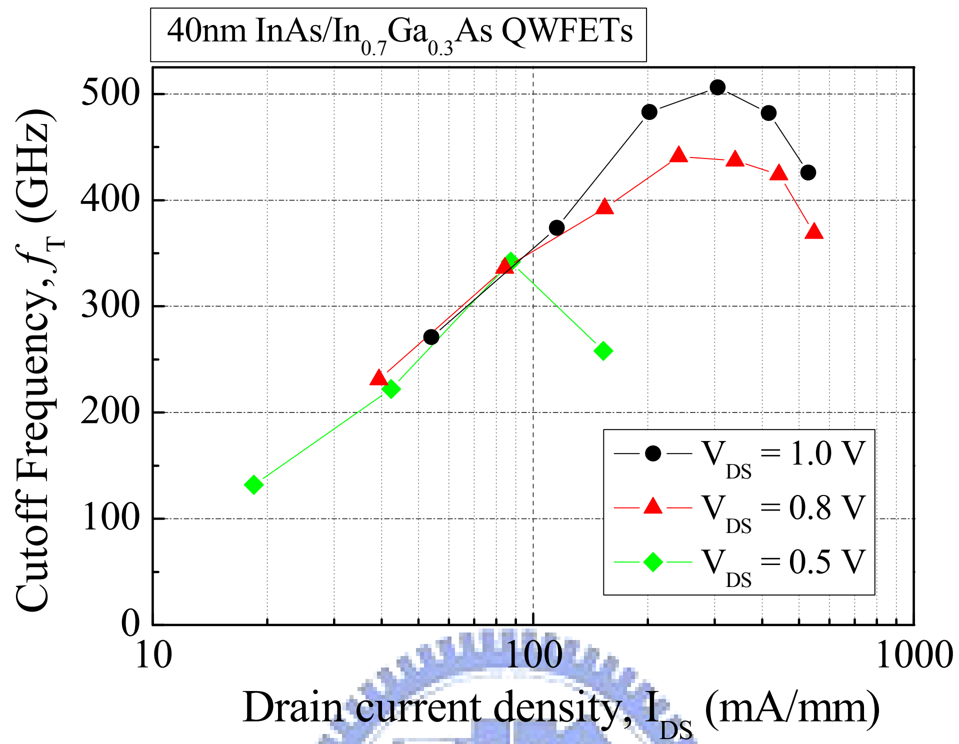


Fig. 5.3.5 Current gain cut-off frequency (f_T) vs. I_{DS} at different V_{DS} of fabricated 40nm $InAs/In_{0.7}Ga_{0.3}As$ composite channel QWFETs.

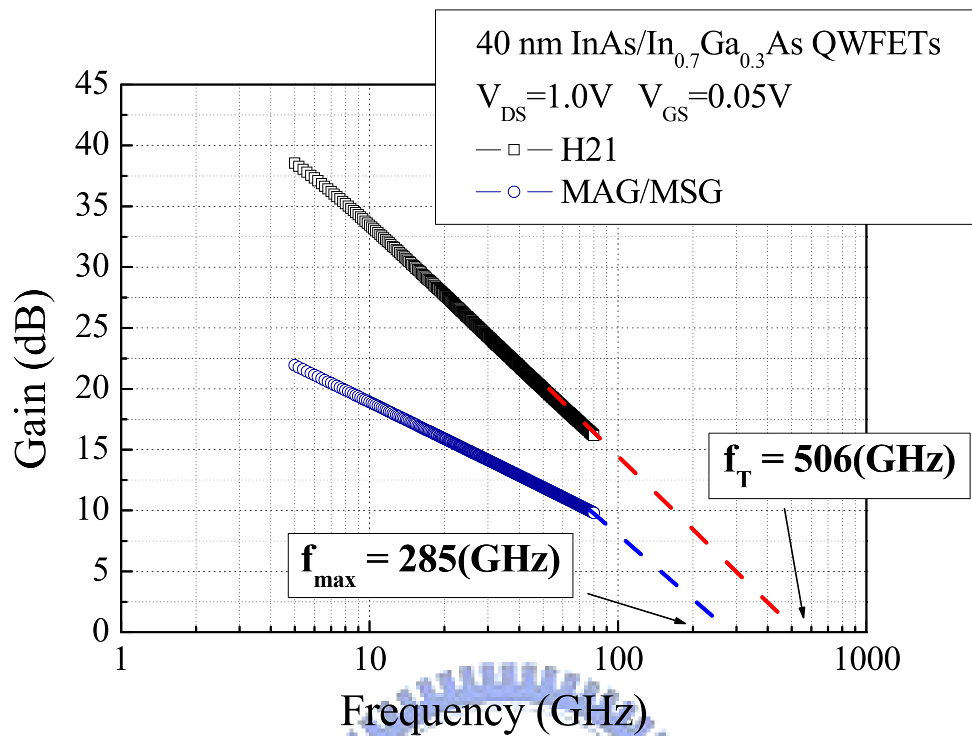
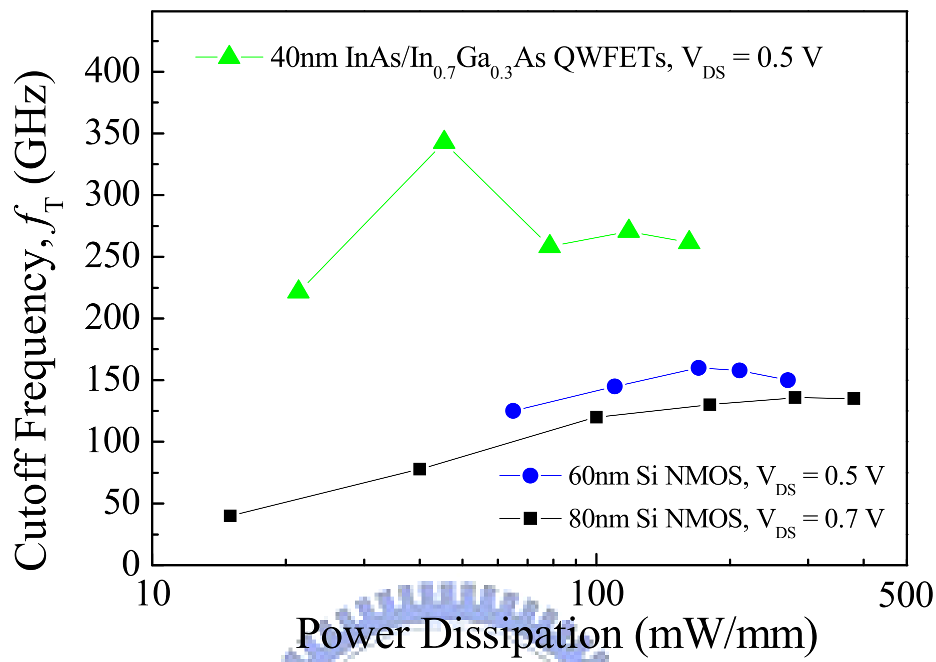


Fig. 5.3.6 Frequency dependence of the current gain (H_{21}) and the power gain (MAG/MSG) of the 40nm $InAs/In_{0.7}Ga_{0.3}As$ composite channel QWFETs. The frequency range was from 5 to 80 GHz, and the device was biased at V_{DS} = 1.0 V.



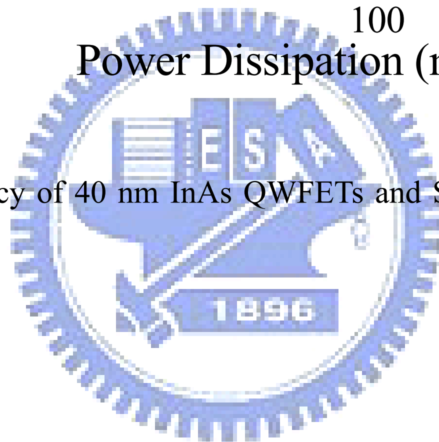


Fig. 5.3.7 Cutoff frequency of 40 nm InAs QWFETs and Si MOSFETs as a function of the power dissipation

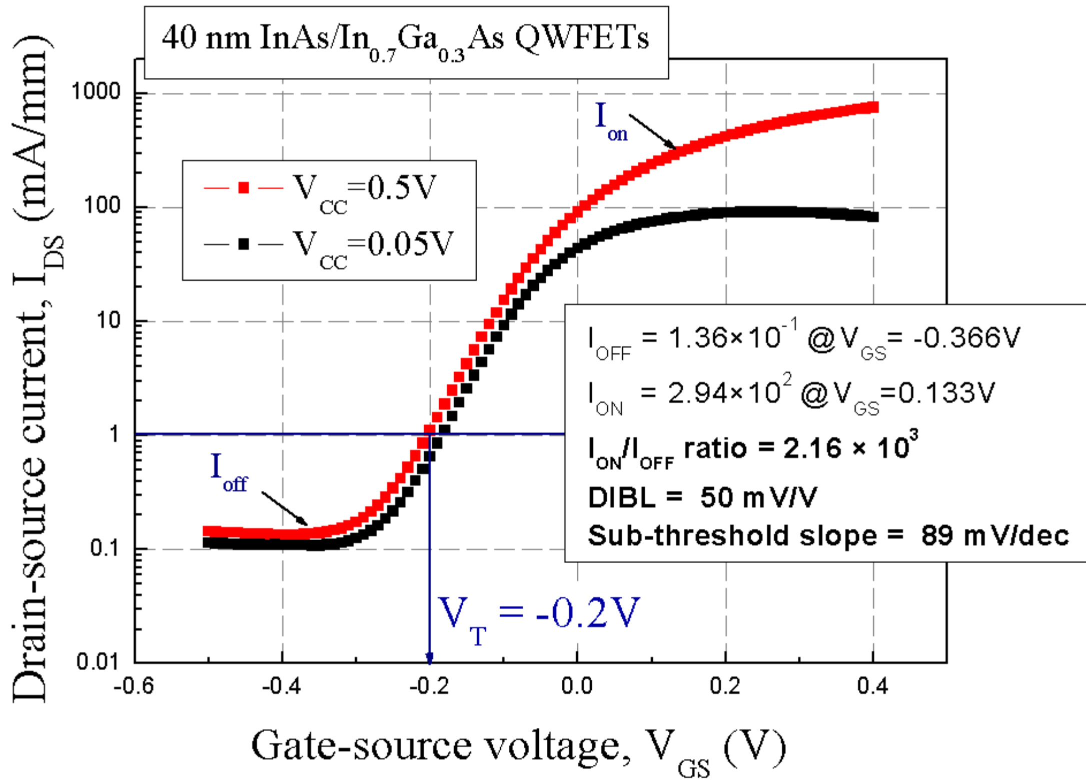


Fig. 5.3.8 The sub-threshold characteristics (DIBL, S, I_{ON}/I_{OFF} ratio) of 40nm $InAs/In_{0.7}Ga_{0.3}As$ composite channel QWFETs at the V_{DS} of 0.05 and 0.5V.

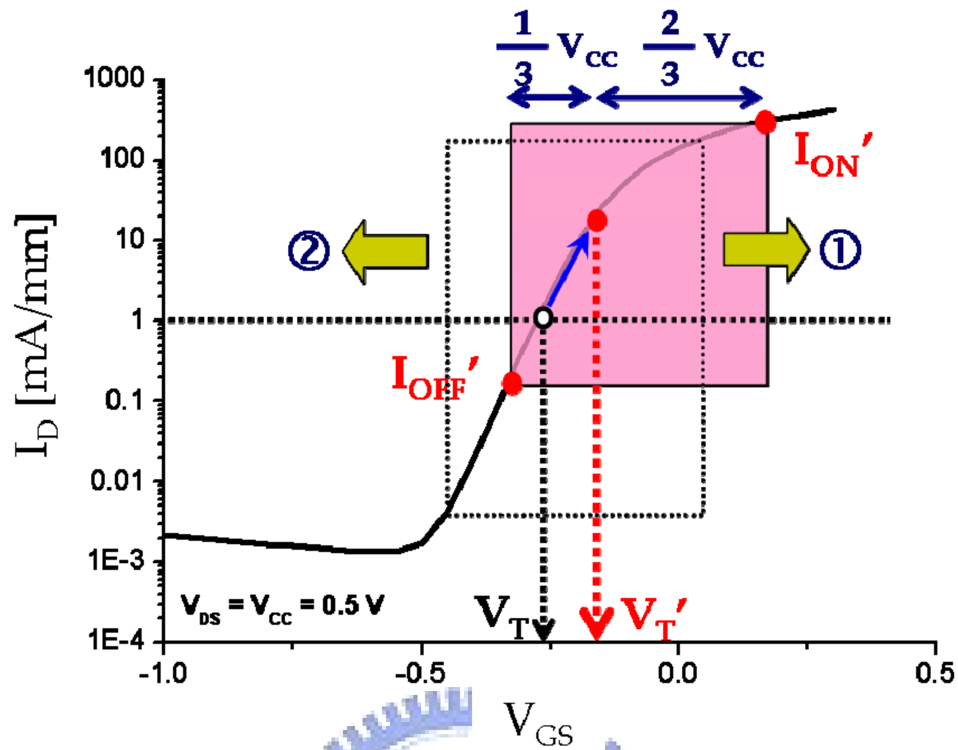
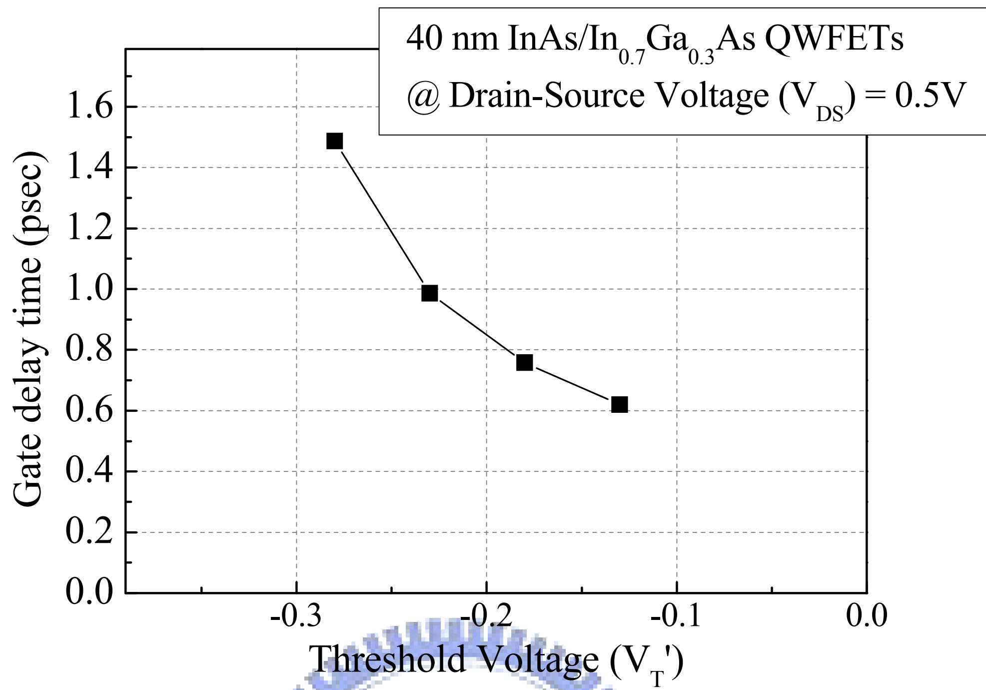


Fig. 5.3.9 The methodology for the evaluation of the logic performance of novel devices with non-optimized V_T. Different definitions of V_T result in a new set of logic parameters of C'V'/I'.



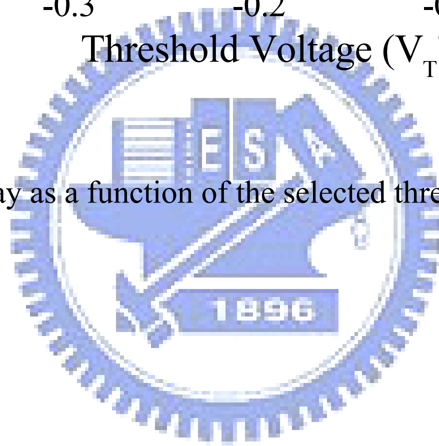


Fig. 5.3.10 Gate delay as a function of the selected threshold voltage at V_{DS} = 0.5V.

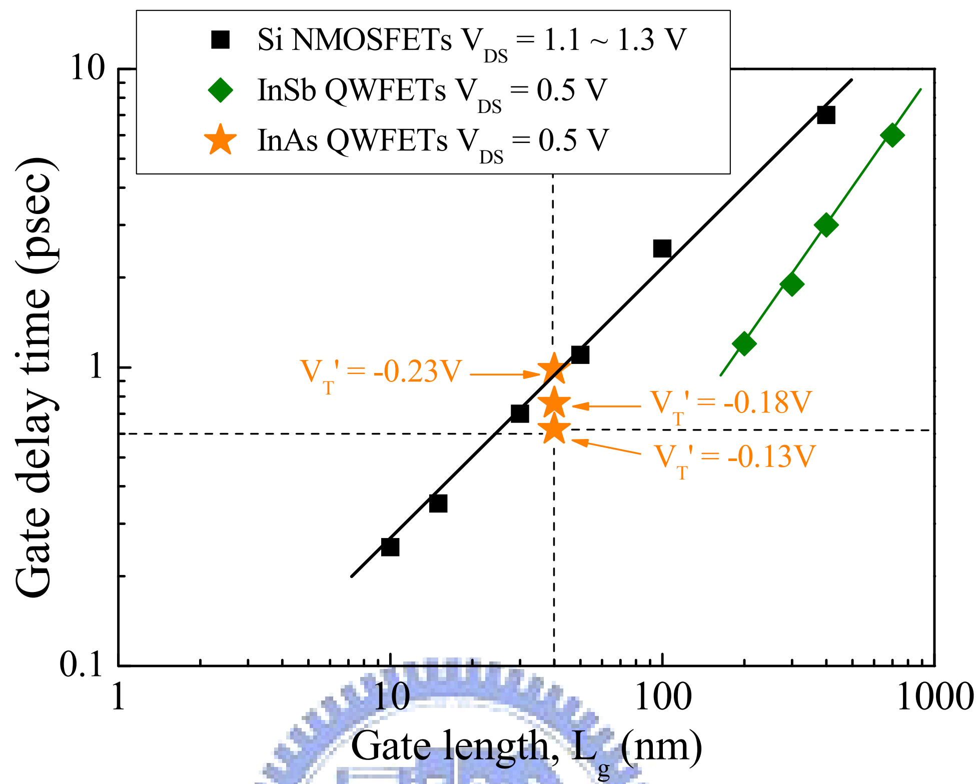


Fig. 5.3.11 Gate delay of InAs, InSb QWFETs and Si NMOSFETs as a function of gate length.

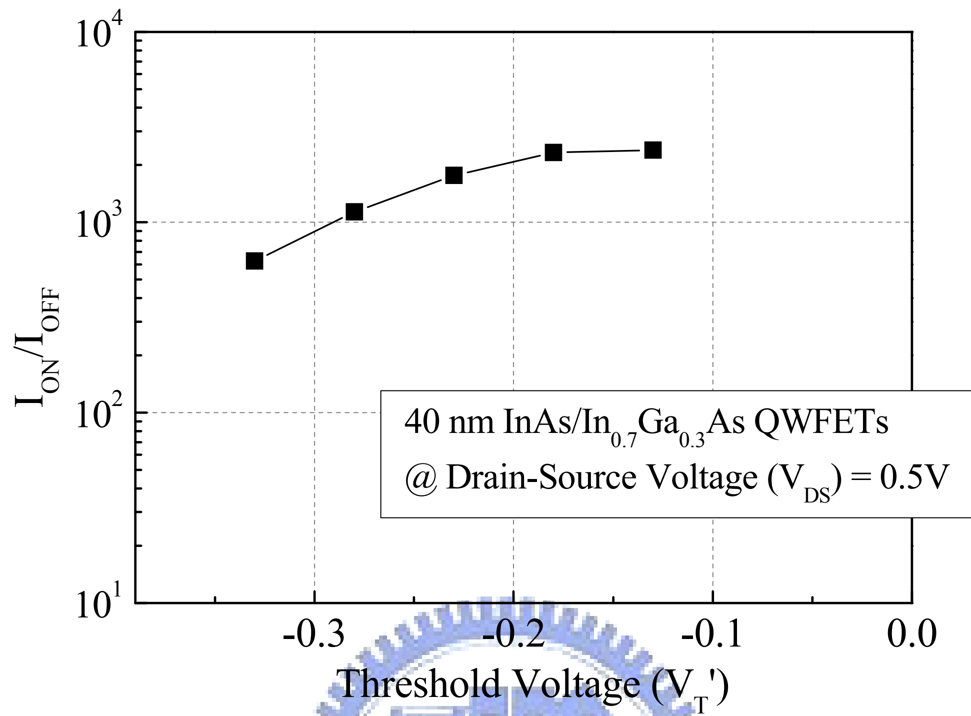


Fig. 5.3.12 I_{ON}/I_{OFF} ratio as a function of various V_T at drain voltage of 0.5 V.

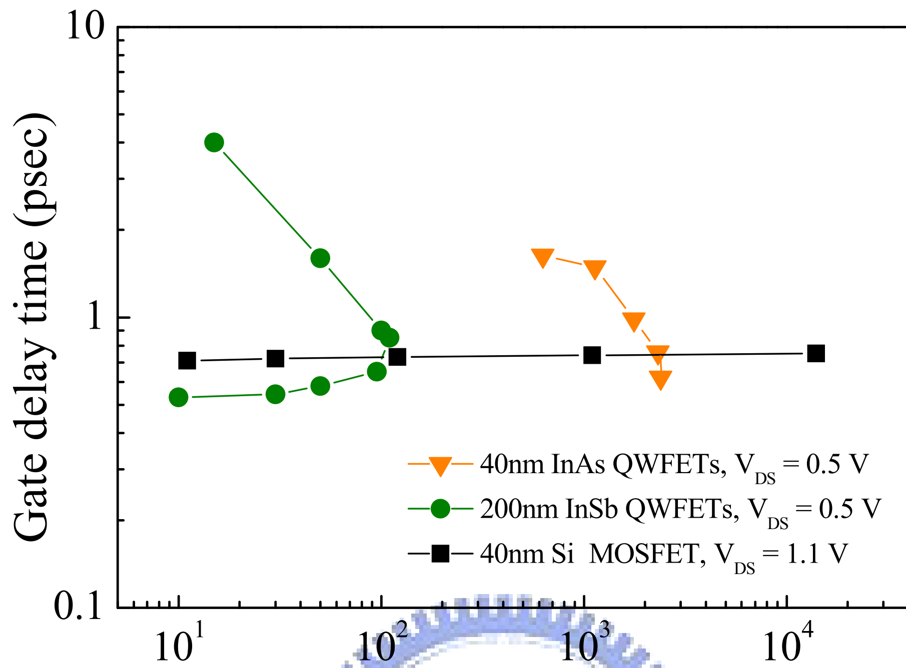


Fig. 5.3.13 Comparison between gate delay and I_{ON}/I_{OFF} of 40 nm InAs QWFETs, 200 nm InSb QWFETs and 40 nm Si MOSFETs.

Chapter 6

Conclusion

In this thesis, the InAs QWFETs of 40 nm gate length for high-speed, low-noise, low-voltage millimeter wave applications as well as high-performance, low-voltage logic applications have been fabricated and evaluated.

By applying advanced two-step recess and Pt gate sinking technologies, the performances of the InAs/$In_{0.53}Ga_{0.47}As$ QWFETs are greatly improved. These steps reduce the distance between the gate electrode and the channel region. So these thinner insulator schottky layer devices exhibit enhanced characteristics such as no short-channel effect, better saturating current, lower output conductance (*go*), smaller negative threshold-voltage (V_T) and higher f_T and f_{max} (400 GHz and190 GHz) at low applied voltage. In addition, the noise performance has also been investigated. The devices exhibit the minimum noise figure of lower than 2.5 dB for frequencies up to 64GHz and with corresponding associated gain of 7 dB when biased at V_{DS} of 0.5 V. Furthermore, when comparing with Si NMOSFETs, the InAs QWFETs can achieve much higher f_T than Si NMOSFETs at the same power dissipation. In conclusion, the 40 InAs QWFETs exhibit excellent low-voltage RF characteristics.

Although the InAs QWFETs demonstrated excellent gain and low-noise performance at high frequencies, the impact ionization phenomena may occur and degrade the performance when biasing at too high voltage. In this thesis, the experimental investigation of impact ionization phenomena in 40 nm InAs/$In_{0.53}Ga_{0.47}As$ channel QWFETs through DC, noise and S-parameter measurement has been presented. The devices show high output conductance with the increase in V_{DS}. A hump in the gate leakage current curve is observed at V_{DS} of higher than 1.0 V. And the minimum noise figure drastically increases at V_{DS} of 1.0 V. The

S-parameter was measured, and the f_T keep on increasing to 663 GHz when V_{DS} is 0.9 V and then dropped to 517 GHz at V_{DS} of 1.0 V. These all above phenomena are attributed to the impact ionization in InAs channel at high applied voltage. However, with suitable bias voltage, the excellent device performance can still be achieved. The devices show transconductance over 1500 mS/mm at V_{DS} = 0.5 V. Beside, the measured noise performance revealed that the device has a low noise figure of less than 3 dB with an associated gain of 7 dB up to 64 GHz at V_{DS} of 0.8 V. And the extremely high f_T of 663 GHz can be obtained if the device is biased near the occurrence of impact ionization. Therefore, provided with optimum bias points, such InAs devices show tremendous potential for very high frequency applications.

Finally, the evaluations of 40 nm InAs/$In_{0.7}Ga_{0.3}As$ QWFETs for high-speed low-voltage digital applications are discussed. The devices display excellent logic performance at low bias voltage. At V_{DS} of 0.5 V, the drain induced barrier lowering (DIBL) is 50 mV/V, and the subthreshold swing (S) is 89mV/decade. The intrinsic gate delay (CV/I_{ON}) is less than 1 psec. When comparing with the updated Si technology, the InAs QWFETs exhibit smaller gate delay time than the Si nMOSFET with the same gate length. Besides, InAs QWFETs show much higher I_{ON}/I_{OFF} ratio than the InSb QWFETs. These results demonstrate that the InAs QWFETs are potential candidates for high-speed and low-voltage logic applications in the post-Si era.

Overall, these experimental results of the InAs QWFETs demonstrate that they have excellent performance and are good both for very high frequency circuits applications as well as for very high speed, low voltage logic circuits applications.

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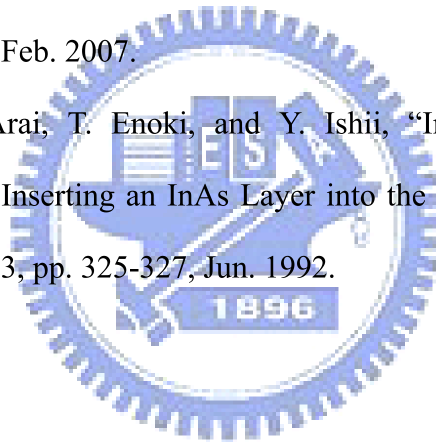

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