國立交通大學

材料科學與工程研究所

碩士論文

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DC and RF Performance Improvement of 60 nm Quantum Well Field Effect Transistors by Self-aligned Gate Technology

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摘要

近年來，高速電子元件在高頻應用的發展十分迅速，目前已進入到毫米波甚至是次毫米波的領域裡，因此，對於元件規格的要求日趨嚴苛。由於三五族化合物半導體元件表現較矽半導體元件優異，所以三五族化合物半導體元件目前在高速及高頻應用上顯得極為重要。為了提升三五族半導體元件在高頻之表現，有許多元件及材料的改良方式被提出，例如：異質接面結構及次奈米T型金屬閘極。在本論文，我們將探討藉由源極與集極間距之微縮技術來進一步增進元件特性。

在本實驗中，將使用改良型自動對準閘極技術來縮減源極與集極間之間距。實驗之磊晶試片是由分子束磊晶系統所成長，其結構具備有高電子遷移率複合通道層 InAs/$In_{0.53}Ga_{0.47}As$ 以及高濃度參雜($2x10^{19}$)的 Cap 層。本論文之自動對準閘極技術前端製程與傳統的量子井場效電晶體製程相同，包括：定義元件操作之主動區、歐姆接觸的形成以及T型金屬閘極的定義；經過閘極金屬蒸鍍過後，便開始進行本論文所設計的自動對準閘極技術。首先，先沉積以二氧化矽所構成的保護層來保護六十奈米的T型金屬閘極，其次，使用氫氟酸移除主動區域之二氧化矽保護層並隨後立即蒸鍍上歐姆接觸所使用之金屬，最後再沉積氮化矽做為元件的保護層並進行接觸窗部位的開啟。

比較使用與未使用自動對準閘極技術的元件，可以使用自動對準閘極技術之元件在直流的特性上有很顯著的提升，其集極飽和電流密度從原先的 391

mA/mm 提升到 517 mA/mm，同時，轉移電導也使用過自動對準閘極技術的製程之後由 946 mS/mm 上升至 1348 mS/mm；此外，與放大特性息息相關的電流增益截止頻率也由 187 GHz 提升至 205 GHz。本實驗之自動對準閘極也改進了元件的邏輯應用特性，其汲極引致能障下降降為 75.6 mV/V、次臨界擺幅降為 101.4 mV/dec 而開關電流比(I_{ON}/I_{OFF} ratio)則為 3300。這些成果顯示此種改良型的自動對準閘極技術能夠有效提升三五族量子井場效電晶體在高速、高頻應用之功能，並同時具備元件低能量消耗的效果。

DC and RF Performance Improvement of 60 nm Quantum Well FET by Self-aligned Gate Technology

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Abstract

In general, III-V compound semiconductors have significantly higher intrinsic mobility than silicon and substrates are semi-insulating. These material properties combine with band gap engineering, epitaxial layer growth technique and process technologies result in devices with excellent performance at high frequencies. The applications for these devices include broadband optical fiber communication, wireless communication at millimeter wave and sub-millimeter wave range. Recently, InGaAs Quantum Well Field Effect Transistor (QWFET) also shows great promise for future high-speed and ultra-low power logic application due to its high speed and low voltage operation capability.

In this experiment, the epitaxial layers of the InAs/$In_{0.53}Ga_{0.47}As$-channel QWFET with highly doped (2×10^{19}) cap layer were grown on InP substrate by molecular beam epitaxy (MBE) for high speed device application. The devices were fabricated with the self-aligned gate technology. The device fabrication was started with a conventional QWFET process: mesa isolation, ohmic contact formation and T-shape gate definition. After the gate metals were deposited, the self-aligned gate process was executed. First, the SiO_2 layer was deposited as a hard mask by PECVD to protect the 60 nm T-shape gate. Then, the SiO_2 within the mesa region was

removed by HF. Then an extra thin ohmic metal (Au) layer was deposited by E-gun evaporator. Finally, the device was passivated by SiN_x and the contact via was etched with RIE.

Comparison of the devices with/without the SAG process shows that there is obtains improvement of the saturation drain current density from 391 mA/mm to 517 mA/mm after using the SAG process. The transconductance also enhanced from 946 mS/mm to 1348 mS/mm and the current gain cutoff frequency changed from 187 GHz to 205 GHz. Furthermore, the device with SAG process had great performance for logic application: I_{ON}/I_{OFF} ratio = 3.3 x 10^3, DIBL = 75.6 mV/V and S.S. = 101.4 mV/dec. These results show that the ameliorative self-aligned gate technology can effectively enhance the III-V QWFET device performance for high frequency, high-speed and low-power consumption applications.

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為期兩年充實的碩士班生涯即將到達尾聲，在這兩年裡，我自己都能隱約感受到自己無論是在專業知識或是團隊合作研究的成長，我想，這其中需要感謝的人實在太多了。首先是我的指導教授　張翼博士，老師向來以開明的作風循循善誘，在專業知識能夠提綱挈領的指導，並提供了實驗室良善且齊全的製程設備，讓我在學習的過程中，能有完備的設備可以使用，大大的提高學習的效率。其次，我想感謝的是指導我的郭建億學長，他總是願意在十分忙碌的生活中，抽空幫我們注意實驗上的細節，並不吝於給予寶貴的意見，甚至是身先士卒的陪我一起做實驗，我認為是非常難能可貴且令人感動的。再來，就是協助我做實驗數據分析與萃取的元智大學許恆通博士，藉由他在三維電子元件模擬的結果，幫助我找尋、分析並改良製程方面的問題。還有就是我的好友吳建瑩先生，他在優秀的研究並取得碩士學位後，仍然幫助我處理與討論實驗上的問題，並在撰寫碩士論文的時候提供了很多寶貴的意見。

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Chapter 1

Introduction

1.1 General Background and Motivation

In recent years, the development of high frequency devices has become more and more important. The demand for high-frequency devices is increasing with two major applications: the high-speed optical fiber communication system applications and high-frequency wireless systems applications. And with the rapid development of the wireless communication systems, the applications have moved from the microwave toward millimeter wave frequency range. The requirements for high speed and high frequency devices have become more and more rigid. III-V compound semiconductor devices have shown superior performance as compared to the Si devices in high-frequency and high-speed applications. Many efforts have been made to improve the high-frequency performance of the III-V devices by means of refined heterjunction structure and sub-nanometer gate length. Nanometer-T-shaped gate is generally used for the QWFETs to maximize the device performance.

On the other hand, the size scaling of CMOS has followed the famous Moore's Law for over 30 years. In the current 65nm technology node, the gate length of a Si MOSFET is about 30 nm and such dimension is expected to reach about 10 nm by 2011, which is believed to be the ultimate limit for CMOS scaling. The trend of transistor technology is shown in Fig. 1.1 and several novel devices technology candidates that are mentioned to replace Si CMOS including carbon nanotube (CNT) transistors, semiconductor nanowires and spintronics [1-1]. While the majority of the

above suggested technologies are still in the prototyping stage, recent development in device technology of III-V FETs, especially the heterostructure QWFET devices has shown great potential to be the next generation high-speed logic device technology due to its maturity in device fabrication technologies and excellent RF performance.

Attention has recently been paid to III-V channels as a promising candidate of high performance n-MOSFETs beyond strained-Si devices [1-2]. This is because III-V compound semiconductors have ~ 50-100 x higher electron mobility than Si and III-V nMOSFET can exhibit very attractive and tangible worth. Some channel materials electronic properties are listed in Table 1.1 [1-3], which indicates that III-V materials can play an important role in future high speed, and low power CMOS logic transistors in the Post-Si era.

1.2 Overview of Quantum Well Field Effect Transistors

In the past, there is a great demand in developing high performance III-V transistors for wireless communication application. As compared with silicon-based transistors, such as metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar-junction transistors (BJTs), III-V transistors exhibits inherent advantages over Si-based transistors for high-frequency application. Quantum well field-effect transistor (QWFET) or called High electron mobility transistor (HEMT) is one of the most mature III-V semiconductor transistors which rely on the use of heterojunction for its operation. The first demonstration of the QWFET was made by Fujitsu Lab. in 1980 [1-4]. A cross-sectional view of a conventional QWFET structure represents in Fig 1.2. The epitaxial layers of the QWFET structure are designed to form two-dimension electron gas (2-DEG) in the channel layer with an un-doped spacer in the wide band gap material and narrow band gap material to separate the ionized

donors from the channel. The detailed description of energy band diagram of InAlAs/InGaAs Metamorphic HEMTs (MHEMTs) is shown in Fig. 1.3 [1-5]. As a result, QWFETs have superior carrier transport properties due to the band-gap engineering design.

For the past 5 years, GaAs-based QWFETs and InP-based QWFETs with remarkable device performance for high frequency applications have been published and these results are listed in Table 1.2. As seen from this table, high indium content channel material QWFETs with nanometer gate length is the main way to enhance the device performance.

1.3 Improvement of device performance by self-aligned gate technology

The self-aligned gate design was patented in 1969 by the team of Kerwin, Klein, and Sarace [1-6] and has been used in Si-based MOSFETs device industries for several decades. It can effectively enhance the device performance and lower the power consumption because the scaling of source-drain spacing reduces the resistance and enhance the saturation current. However, the conventional self-aligned gate process needs ion implantations or excellent stability of schottky gate for high-temperature annealing, which is not suitable for the III-V QWFET structures. The design of self-aligned gate technology for III-V QWFET becomes an important issue to obtain lower source resistance and higher transconductance.

1.4 Logic Suitability of QWFETs for Beyond-CMOS Applications

Lately, III-V technologies have attracted again for logic circuit when CMOS roadmap comes to the end. The main reason is the manufacturing technology for III-V

devices is relatively mature compared to other novel devices such as carbon-nanotube transistors and semiconductor nanowires. In digital application, a transistor operates as a switch and is different form in microwave or millimeter wave application. Fig. 1.4 shows the electrical figures of merit of a transistor as a switch [1-7]. As seen from the figure, figures of merit relevant to logic application, for example drain-induced barrier lowering (DIBL), subthreshold slope (S), on-state and off-state current ratio, and the delay time (CV/I), these are important parameters for these devices to be used for future digital applications.

In this study, we have applied a methodology that was recently proposed to analyze new devices which often feature nonoptimized values of V_T [1-8]. The evaluation methodology is shown in Fig. 1.5. First, we select gate-to-source voltage at 1mA/mm of drain-source current as the threshold voltage. Then we selected I_{ON} as 2/3 V_{CC} swing above the threshold voltage, and I_{OFF} as 1/3 V_{CC} swing below the threshold voltage. Based on this definition, we extracted and compared the device's logic parameters, such as subthreshold slope, DIBL and I_{ON}/I_{OFF} ratio for the InAs QWFETs developed in this study.

1.5 Outline of this dissertation

This dissertation covers the theorem, the process design of self-aligned gate technology and the DC and RF characteristics improvement results of InAs channel QWFETs. It is divided into 5 chapters.

In chapters 2, the fabrication process of the InAs QWFETs are introduced, including the mesa isolation, ohmic contact formation, T-shaped gate process, gate recess, SiN_x passivation and airbridge formation. And then the reformed self-aligned gate process will be exhibited.

In chapter 3, the DC and RF characterisations of the device are described.

In chapter 4, the results of DC and RF improvement of the $In_{0.53}Ga_{0.47}As$/InAs/ $In_{0.53}Ga_{0.47}As$ channel QWFETs with Pt-buried gate and self-aligned gate technique are given. The current gain cutoff frequency of the 60 nm gate-length device increased from 187 GHz to 205 GHz after the self-aligned gate process. The improvements of the device characteristics are due to the reduction of access resistance (R_{access}) and the source resistance (R_S) after SAG process. In addition, for ultra-low power low-noise amplifier application, the InAs channel device demonstrates excellent DC power consumption with higher gain compared with other GaAs- or InP-based QWFETs to date.

Finally, chapter 5 is the conclusion of the dissertation. The DC and RF performance of the InAs channel QWFET was improved by using SAG technique due to the reduction of gate-to-source distance, small R_{access} and the small R_S. The InAs QWFETs showed excellent DC and RF performances after SAG process, indicating great potential for this device for low voltage high-speed digital applications.

	Si	Ge	GaAs	InP	InAs	InSb
electron mob. (cm^2/Vs)	1600	3900	9200	5400	40000	77000
electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0. 916	m_t: 0.082 m_l: 1.467	0.067	0.082	0.023	0.014
hole mob. (cm^2/Vs)	430	1900	400	200	500	850
Hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	m_{HH}: 0.45 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.12	m_{HH}: 0.57 m_{LH}: 0.35	m_{HH}: 0.44 m_{LH}: 0.016
band gap (eV)	1.12	0.66	1.42	1.34	0.36	0.17
permittivity	11.8	16	12	12.6	14.8	17

Table 1.1 The bulk electron and hole mobility, the electron and hole effective mass, and the bandgap and the permittivity of Si, Ge, and main III-V semiconductor.

Devices	In (%)	g_m (S/mm)	f_T (GHz)	f_{max} (GHz)	NF_{min} & Gain (dB)	Published	Affiliation
60nm InP HEMT	100	3	400	290	N/A	2006, *IEEE,EL.*	NTT
50nm InP HEMT	80	2.3	385	1000	N/A	2007, *IEDM*	NGST.
50nm GaAs HEMT	53	1.27	489	422	0.64 & 9 at 59GHz	2007, *IEEE,EDL*	MINT
35nm InP HEMT	70	N/A	520	425	0.8 & 5.6 at 90GHz	2008, *IPRM*	NICT
30nm InP HEMT	100	1.62	628	331	N/A	*2008, IEEE,EDL*	M.I.T

Table 1.2 Performance of III-V QWFETs published in recent years.

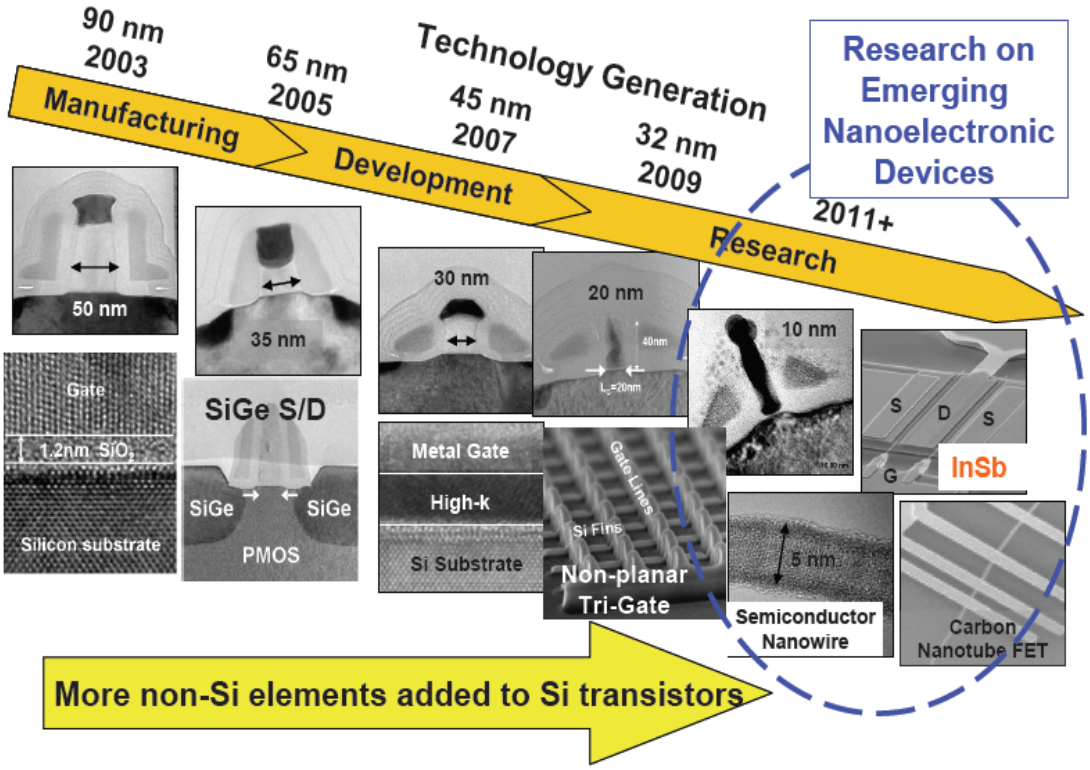


Fig. 1.1 The trend of transistor technology

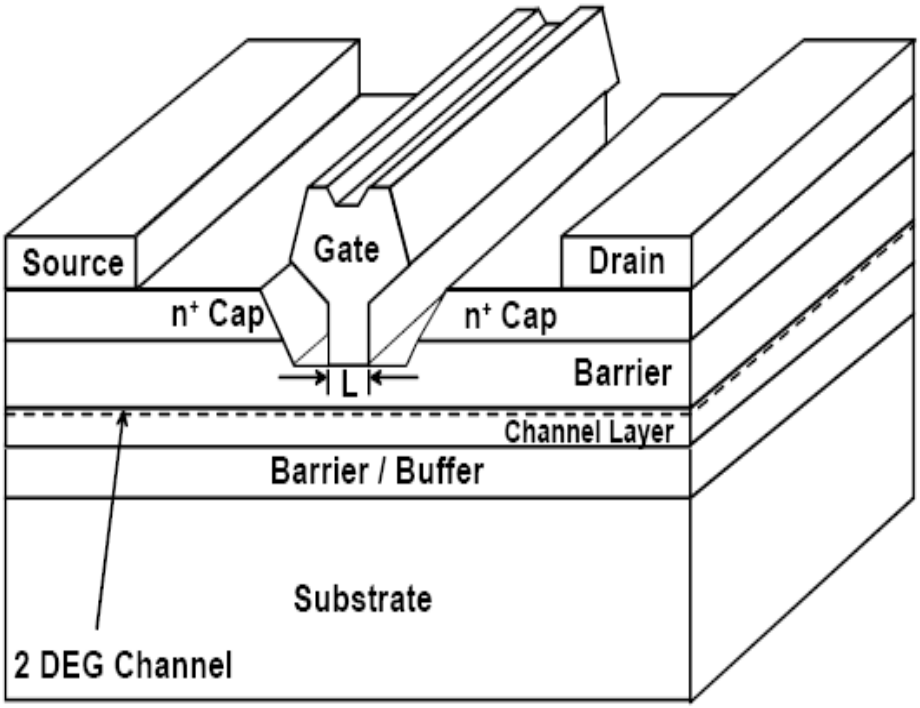


Fig. 1.2 Conventional QWFET structure.

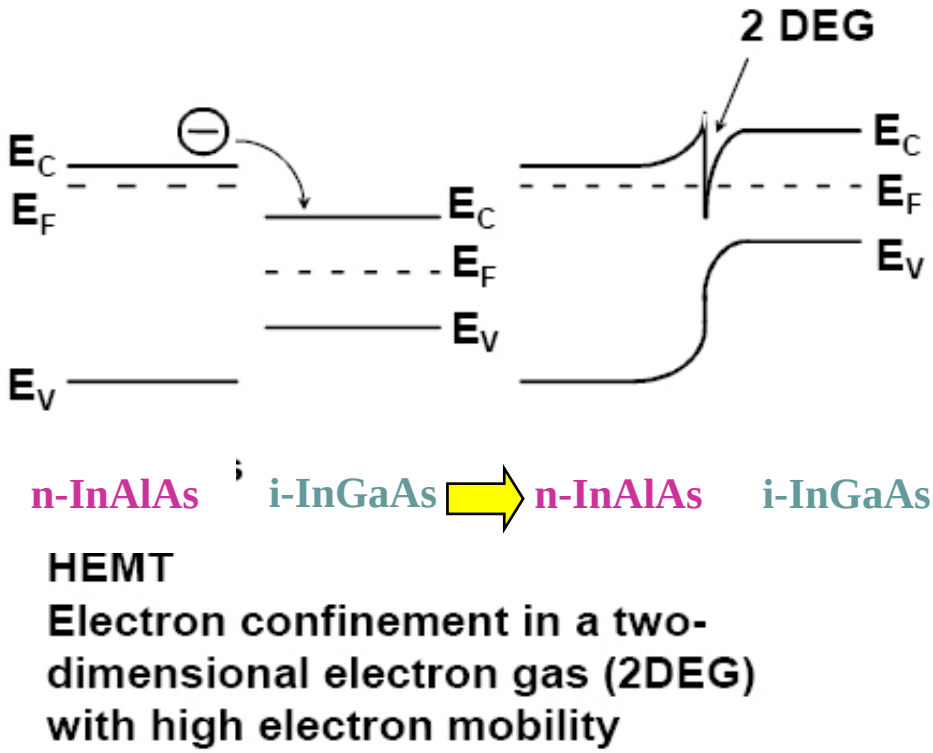


Fig. 1.3 Band Diagram of InAlAs/InGaAs QWFETs

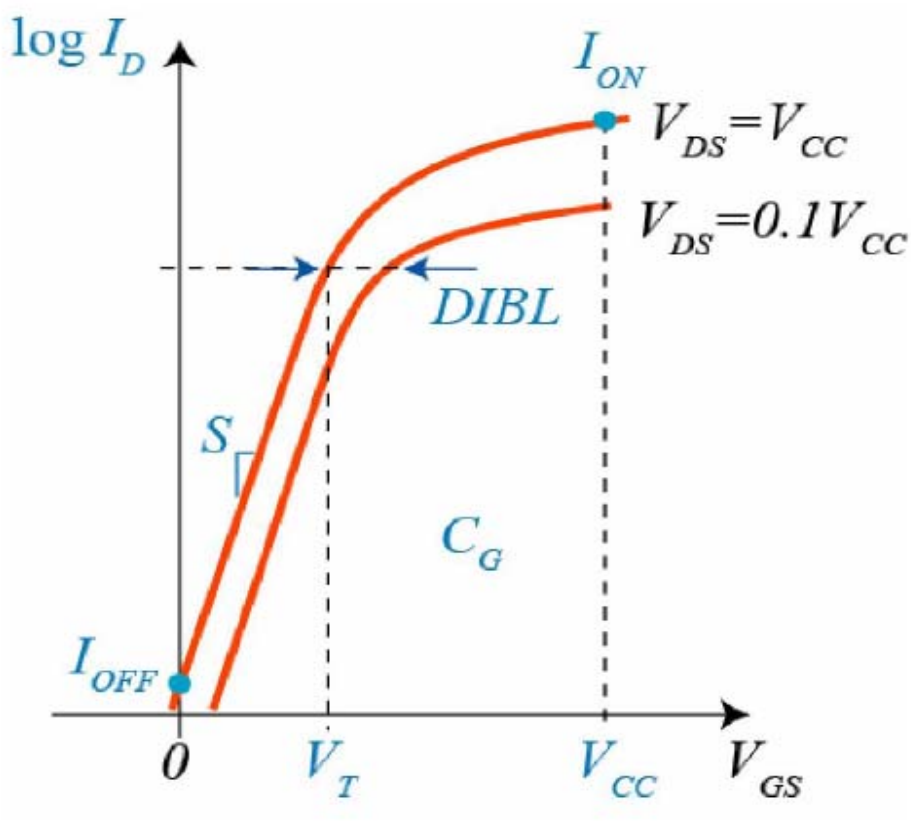


Fig. 1.4 Electrical figures of merit of a transistor as a switch

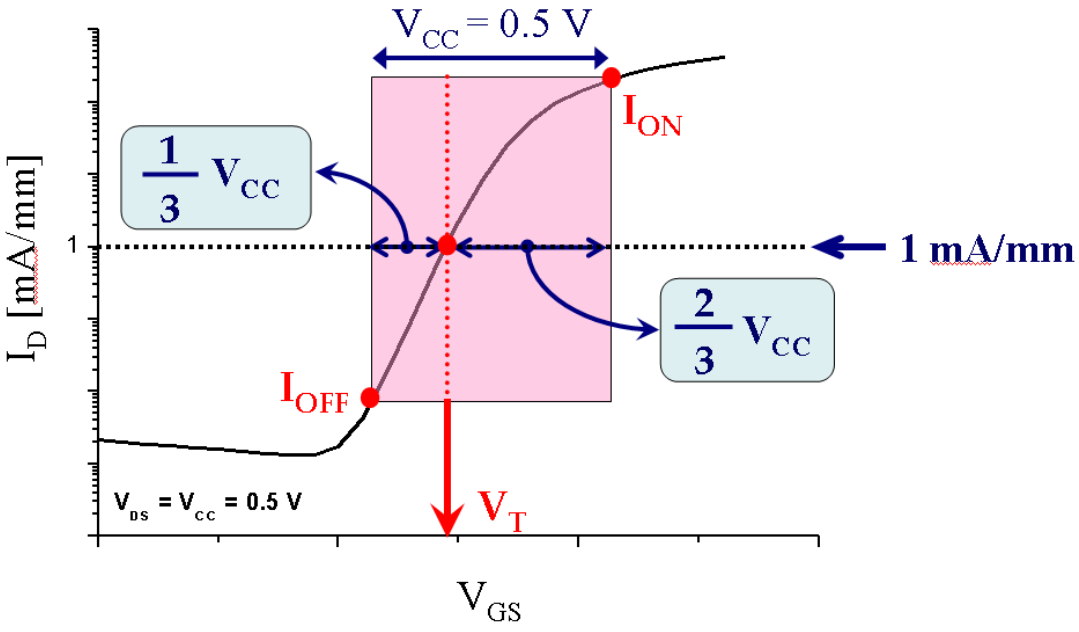


Fig. 1.5 Evaluation methodology for the logic performance of HEMTs

Chapter 2

Process Flow of Fabricating InAs-Channel Quantum Well Field Effect Transistors and Self-aligned Gate Technology

2.1 Device structure

The epitaxial layers of the InAs/$In_{0.53}Ga_{0.47}As$-channel QWFET with $In_xAl_{1-x}As$ grading buffer layer were grown on 3-inch InP substrate by molecular beam epitaxy (MBE). The detailed epitaxial structure of the devices is shown in Table. 2.1 for this study. Metamorphic buffer layer provides the ability to accommodate the lattice mismatch between InAs channel and semi-insulating InP substrate. Therefore, the high indium content in the InAs/$In_{0.52}Ga_{0.48}As$ sub-channel can be achieved in spite of the large lattice mismatch between the active epilayers and the substrate. The Si-planar doping (4×10^{12}) layer is separated from the InAs/$In_{0.52}Ga_{0.48}As$ sub-channel layer by thin undoped spacer, respectively. The undoped $In_{0.52}Al_{0.48}As$ Schottky layer was 8 nm with a 5 nm InP etching stop layer on the top. Then, the $In_{0.53}Ga_{0.47}As$ cap layer was highly doped with 2×10^{19} cm^{-3} for non-alloy ohmic contact formation.

2.2 Conventional device fabrication

The process of InAs QWFETs in this study includes several steps shown in Fig 2.1:

1. Active region definition (Mesa isolation)
2. Ohmic contact formation

3. Fabrication of T-shaped gate process by E-Beam lithography
4. Gate recess
5. Device passivation

2.2.1 Active region definition (Mesa isolation)

Mesa isolation is the first step of the whole QWFET fabrication process which was used to define the active region of the device on the wafer. The active areas were first masked by Shipley S1818 photo resist and then, the InGaAs/InAlAs layers was etched by a phosphoric based solution, following that, a hydrochloric acid based wet etch was used to etch the InP stopper layer [2-1]. The mesa island was etched to the buffer layer to provide good device isolation. Finally, the etching depth was measured by α-step after the photo-resist was stripped and the etched profile was checked by scanning electron microscopy.

2.2.2 Ohmic contact formation

After wafer cleaning by using ACE and IPA, the negative photo resist and I-line aligner were used to define the ohmic pattern and to form the undercut profile for the metal lift-off. HCl-based solution was used as the pre-metallization cleaning solution to remove the native oxide on the InGaAs surface before Ohmic metallization. Ohmic metals Au layer was deposited in the appropriate composition by e-gun evaporation system. After lift-off process, source and drain ohmic contacts were formed. The specific contact resistance was checked by the transmission line method (TLM) in the process control monitor (PCM). It containing a linear array of metal contacts is

fabricated with various spacings between them as shown in Fig 2.2. The distances between TLM electrodes are 3 μm, 5 μm, 10 μm, 20 μm, and 36 μm, respectively in this study. The typical measured contact resistance was less than 1 x 10^{-6} Ω-cm^2 and the illustration of utilizing TLM to measure ohmic contact resistance was shown in Fig 2.3.

2.2.3 Fabrication of T-shaped gate process by E-Beam lithography

Short gate length with low gate resistance is necessary for high frequency and high speed application. T-shaped gate structure was the most common approach for achieving low gate resistance and a small gate foot [2-2]. In this study, T-shaped gate was achieved by using a conventional multilayer resist (ZEP-520/PMGI/ZEP-520-12) with Electron Beam lithography. The process flow of the fabrication of nanometer T-shaped gate are summarized in Fig 2.4. The first E-beam exposure for top two layers was used to only define the head (Tee-top) of the T-shaped gate by modulating the exposure doses. After that, the ZEP and PMGI development were executed by using xylene and MF622, respectively. Then, single center exposure with high dose was used to define the footprint of the bottom ZEP-520 layer. Fig. 2.5 shows the dose dependence of the gate foot size after development. The T-shaped gate resist profile is illustrated in Fig. 2.6.

2.2.4 Gate recess

The selective recess etching was performed using PH-adjusted solution of succinic (S.A.) and H_2O_2 mixture for the heavily doped InGaAs cap layer over InAlAs Schottky layer [2-3,2-4]. The etchant concentration should be adjusted to

provide an adequate etch rate that is sufficiently slow allowing good control over the recess process, thus enable the operation to approach the target current value, without over etching it. The etching selectivity of InGaAs cap layer over InAlAs Schottky layer was above 100. The target current after the gate recess is a critical parameter affecting the QWFET performance. In order to get the desired recess depth, the ungated source-to-drain current (I_{DS}) was monitored during the recess process. The saturation current and the slope of the linear region go down as the recess groove was etched deeper and deeper. The wet etchant usually leaves a thin oxide layer on the InAlAs. HCl-based solution was used to remove the surface oxide. After recess etching, Pt/Ti/Pt/Au gate metal was evaporated and lifted off using ZDMAC remover (ZEON Corporation) to form T-shaped gate.

2.2.5 Device passivation

FETs are very susceptible to the surface condition, especially in the gate region. The devices are very sensitive to the damages and contaminations such as chemicals, gases, and particles. The passivation layer protects the device from damage during process. The dielectric layer SiN_x is a common choice for III-V device passivation. The STS PECVD system was used for depositing the silicon nitride film in this study. The processing gases of the passivation were silane, ammonia, and nitrogen. The process condition was as following: process pressure: 900 mtorr, process temperature: 250°C and process time: 10 minutes, The silicon nitride film thickness was 600 Å. The reflection index was 2.0 as inspected by N&K anaylzer.

2.3 Self-aligned gate technology (SAG)

Just like silicon base semiconductor technology, “scaling of gate length”, “source-drain spacing narrowing” and “gate to channel distance reduction” are key issues which are reported to improve the device performance. In this experiment, we will focus on “source-drain spacing narrowing” to improve the device performance.

From a simulation result of the literature [2-5] with device structure shown in Fig 2.7, the current gain cutoff frequency of a 50 nm QWFET device with 300 nm S/D spacing can achieve 1.3 THz [2-5]. The superior performance is not only due to the scaling of gate length but also due to the S/D spacing narrowing.

For silicon MOSFET technology, the traditional method to scale the S/D spacing is using “self-aligned gate” technique by ion implantation and refracting gate metal. However, it is not suitable for III-V QWFET. The active ions may damage the wafer structure. Furthermore, the activation annealing after ion implantation is always operated at high temperature (such as 800^{o}C~1000^{o}C) which is close to the growth temperature of III-V epitaxial structure [2-6]. It may have the grain re-growth or form lots of hot carriers which make the devices easier to breakdown. Therefore, a new self-aligned gate process must be designed for the III-V QWFET device performance improvement.

2.4 Process flow of self-aligned gate technique

The self-aligned gate process is additionally implanted to conventional QWFET fabrication after gate metal formation. The fabrication process of self-aligned T-gate QWFET device includes several steps. It is shown in Fig. 2.8:

1. Hard mask deposition
2. Removal of hard mask between source and drain spacing
3. Ohmic metal re-deposition and lift-off

4. SiN_x passivation and contact window via hole

2.4.1 Hard mask layer deposition

After the gate formation, a standard 60 nm T-shape gate QWFET device without surface passivation is finished. The SiO_2 is chosen as hard mask to protect T-shape gate temporarily because it has the great mechanical properties and easily removed by hydrofluoric acid. In this step, STS PECVD system was used for depositing the silicon oxide film. The processing gases were silane, oxygen and nitrogen. The process condition was illustrated as following process pressure: 900 mtorr, process temperature: 200°C and process time: 12 minutes. The silicon dioxide film thickness was about 1500 Å. The reflection index was 2.0 as inspected by N&K anaylzer.

2.4.2 Removal of hard mask between source and drain spacing

After using the negative photo resist and I-line aligner to form the mesa pattern, the SiO_2 hard mask between source and drain spacing will be removed by hydrofluoric acid. The recipe of hydrofluoric acid is HF : H_2O = 1 : 100 and the etching rate is about 5 Å / sec. To decrease the side etching, the etching time should be controlled accurately.

2.4.3 Ohmic metal re-deposition and lift-off

To scale the source-drain spacing, the step of ohmic metal re-deposition is very important. The thin Au layer (around 500 Å) was deposited by e-gun evaporation

system within the mesa island, coved from source to drain region. After lift-off process, the specific contact resistance was checked again by the TLM measurement in the PCM. Because of the highly doped cap layer, the re-deposited metal can form a great ohmic contact as well as the previous ohmic contact formation without RTA annealing. The specific contact resistance of re-deposited ohmic contact is 5.07 x 10^{-7} Ω-cm^2, which is almost the same as the original ohmic contact (= 4.58 x 10^{-7} Ω-cm^2). It proved that the non-alloyed ohmic contact can still keep very low specific contact resistance compared with the 1st ohmic contact.

2.4.4 SiN_x passivation and contact window via hole

To protect the 60 nm T-shape gate, device passivation is imperious. The silicon nitride film is deposited by utilizing STS PECVD system. The processing gases were silane, ammonia, and nitrogen. The process condition was as following: process pressure: 900 mtorr, process temperature: 200°C and process time: 15 minutes. The silicon nitride film thickness was 900 Å. The reflection index was 2.0 as inspected by N&K anaylzer. After the SiN_x passivation layer was formed, the contact window is defined by the positive photo resist and I-line aligner. Then, both the SiN_x and SiO_2 layers were etched by using reactive ion etching (RIE) system. It usually has 10% over etching to make sure that the dielectric layers are removed clearly.

Finally, The 60 nm InAs/$In_{0.53}Ga_{0.47}As$-channel QWFET device with self-aligned gate process is fabricated. The source-to-drain electrode spacing is significant reduced from 3 μm to 650 nm without metal interfering as SEM image shown in Fig 2.9.

n^+ Cap	InGaAs, x = 0.53	40 nm, $2x10^{19}$
Etch stop	InP	5nm
Barrier	InAlAs, x = 0.52	5 nm
δ-doping	Si	$4x10^{12}$
Spacer	InAlAs, x = 0.52	3 nm
Channel	InGaAs, x = 0.53	2 nm
Channel	InAs	5 nm
Channel	InGaAs, x = 0.53	3 nm
Buffer	InAlAs, x = 0.52	500 nm
3 Inch S. I. InP Substrate		

Table. 2.1 The detailed epitaxial structure of the devices in this study

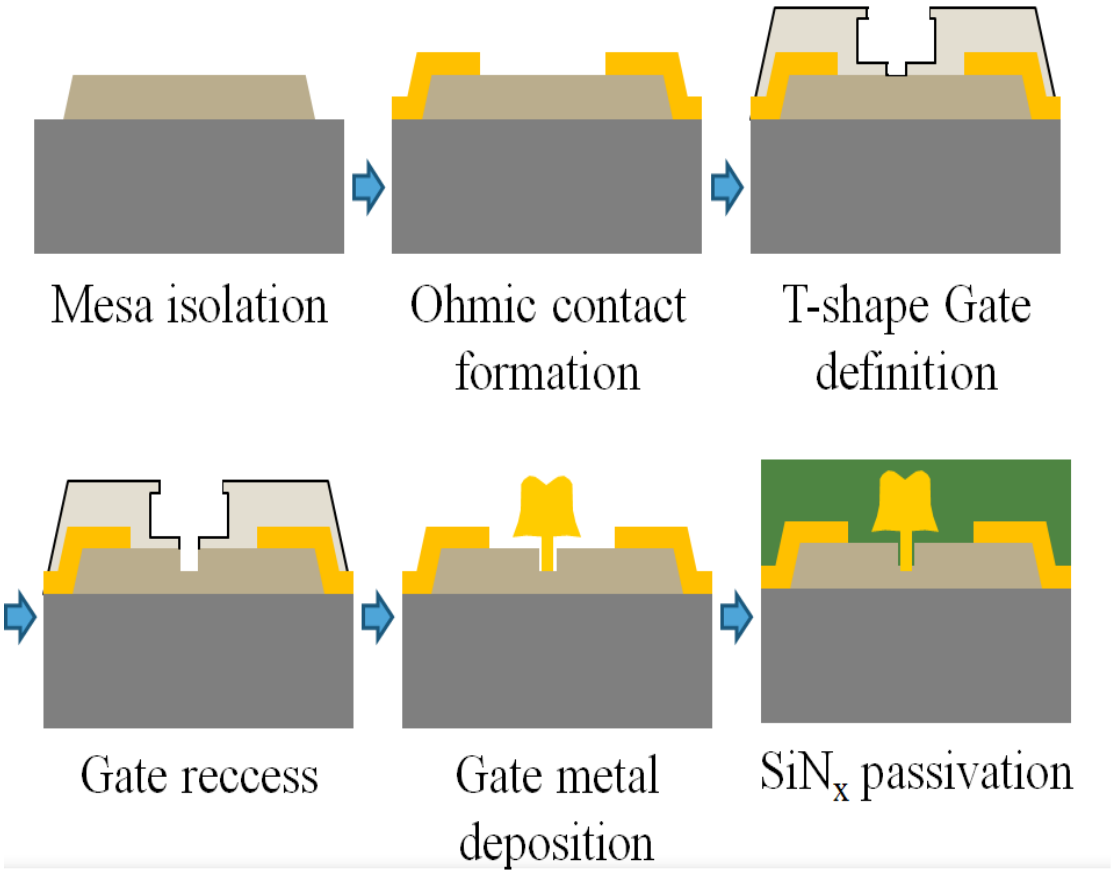


Fig. 2.1 Process flow of traditional QWFET devices

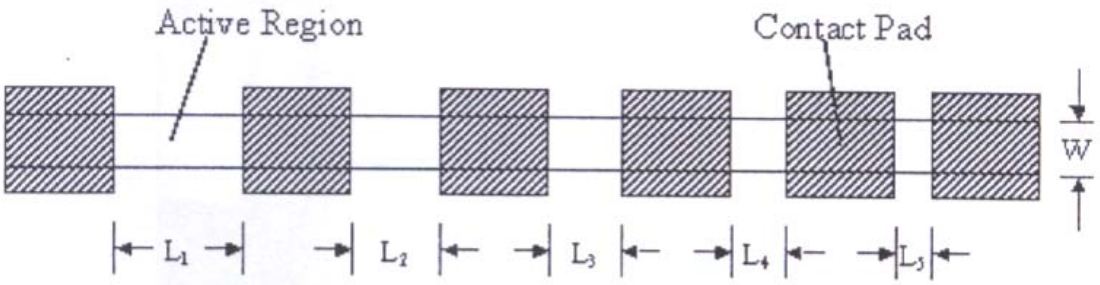


Fig. 2.2 TLM pattern

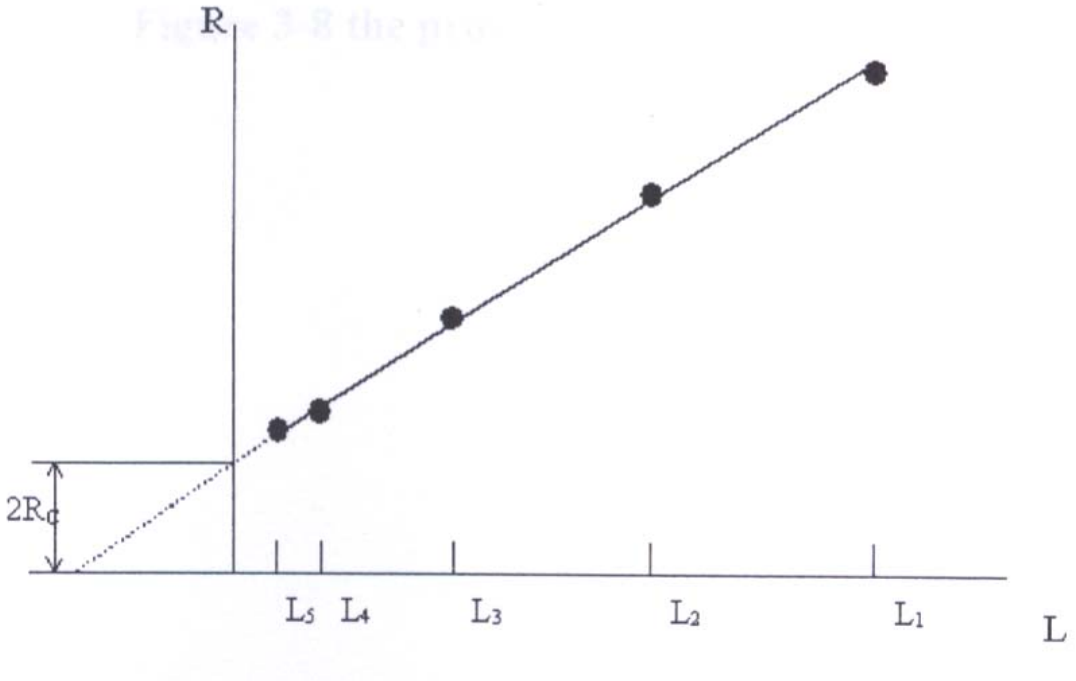


Fig. 2.3 The illustration of utilizing TLM to measure ohmic contact resistance

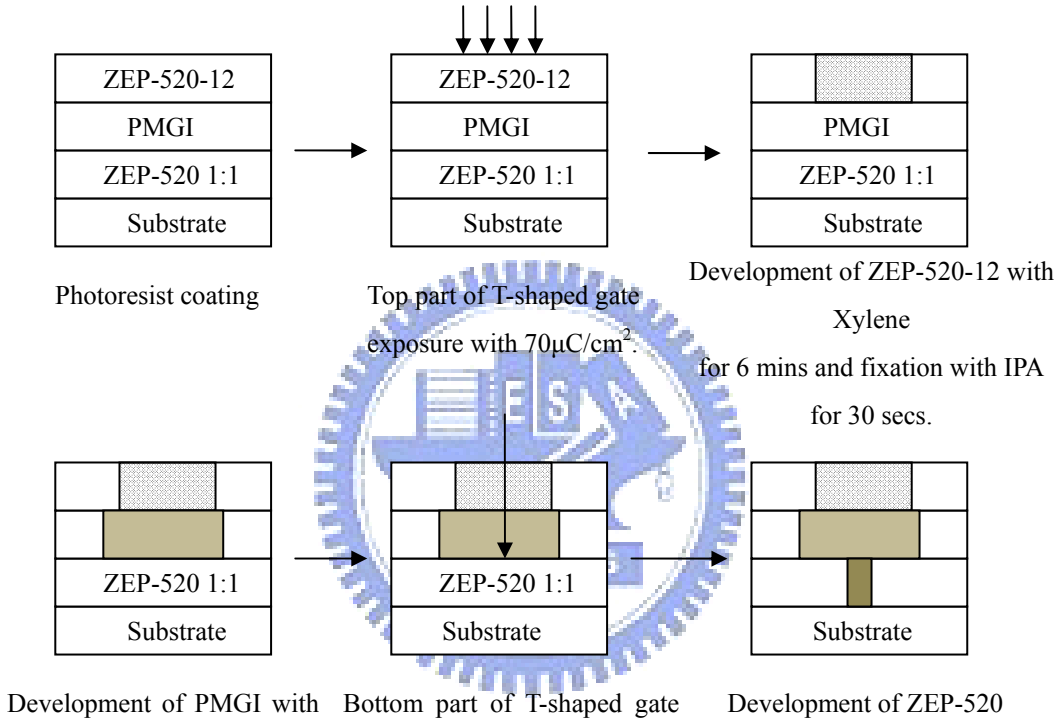


Fig. 2.4 T-shaped gate process flow

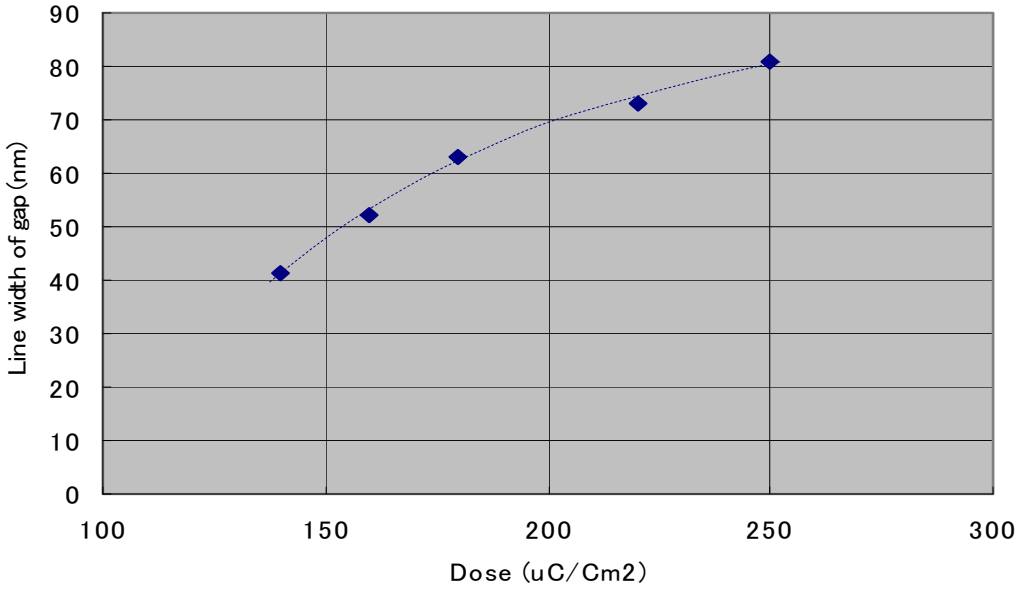


Fig. 2.5 The dose dependence of the gate foot size after development.

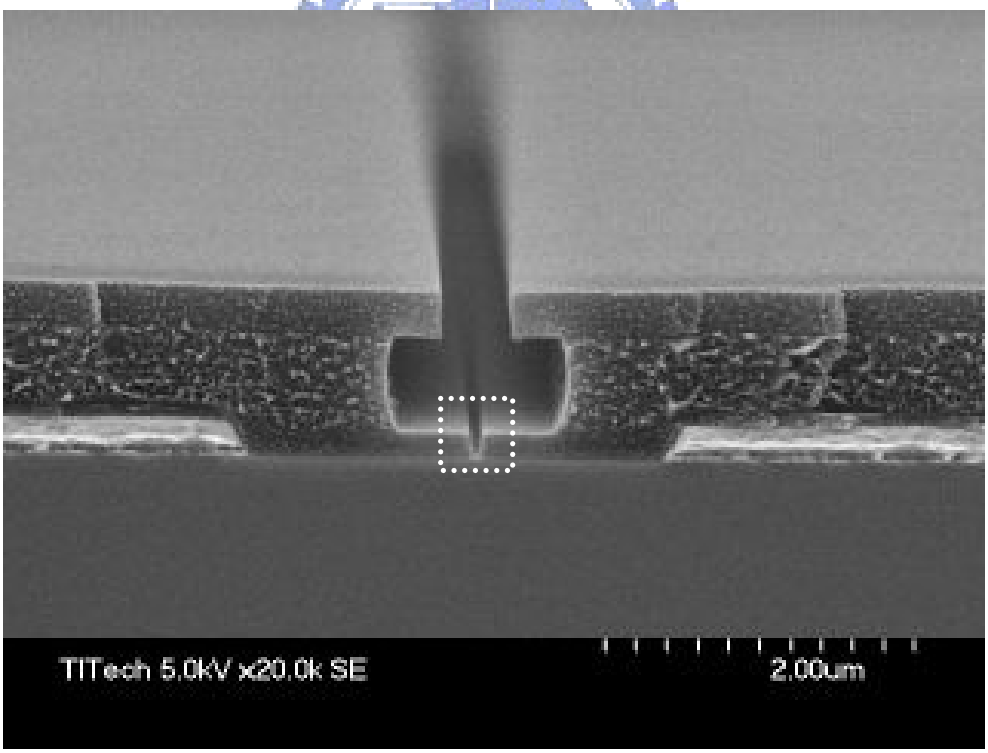


Fig. 2.6 The SEM image of the T-shaped gate resist profile.

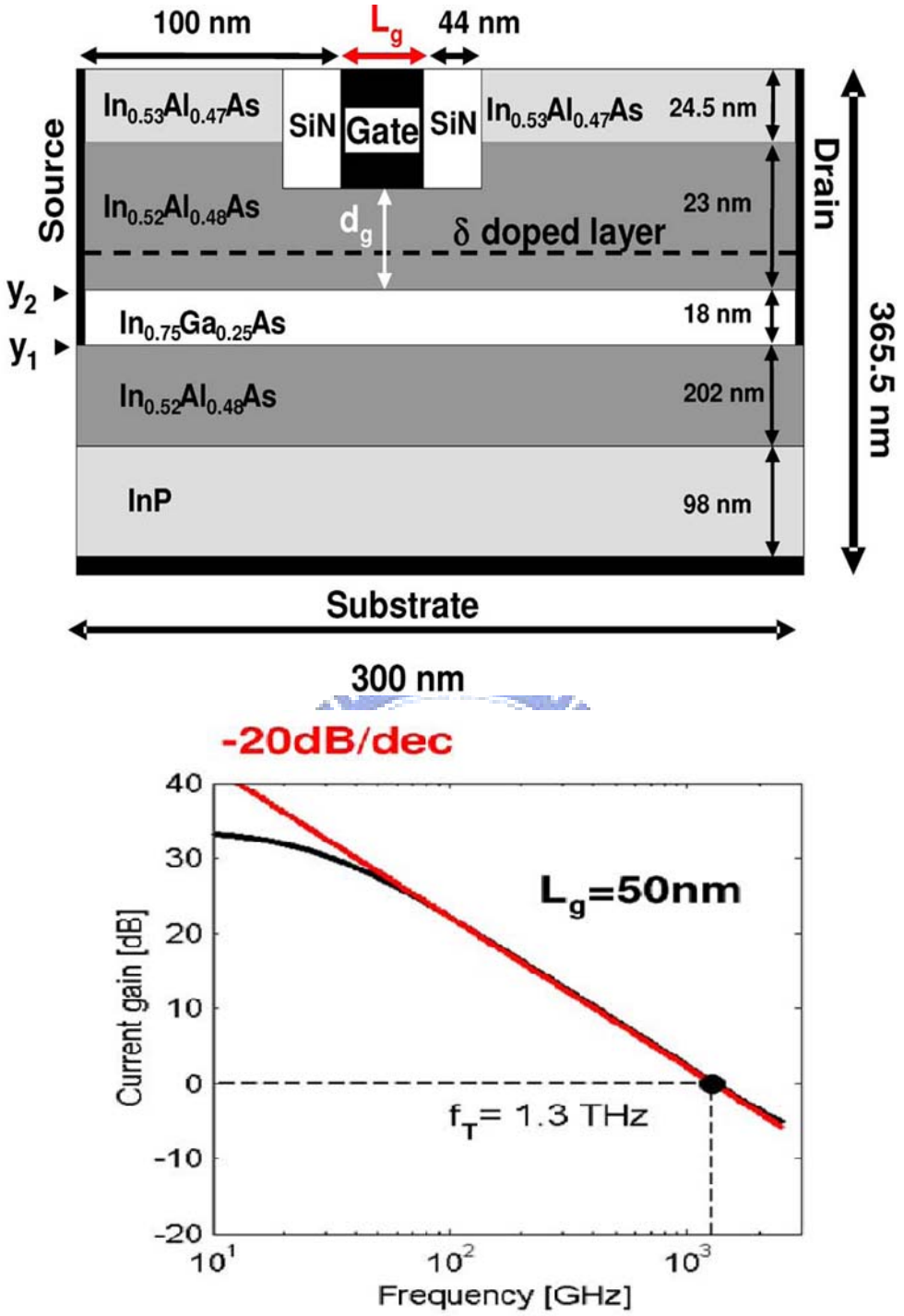


Fig. 2.7 The simulated 2-D QWFET structure. For clarity purposes, the figure is not to scale. All dimensions identified by a number in this figure were kept fixed. The SiN_x regions both have the same dimensions. The physical gate length L_g and the gate-to-channel distance d_g were scaled for the results that follow. Lower panels: Frequency response characteristics for 50 nm gate-length devices. [2-5]

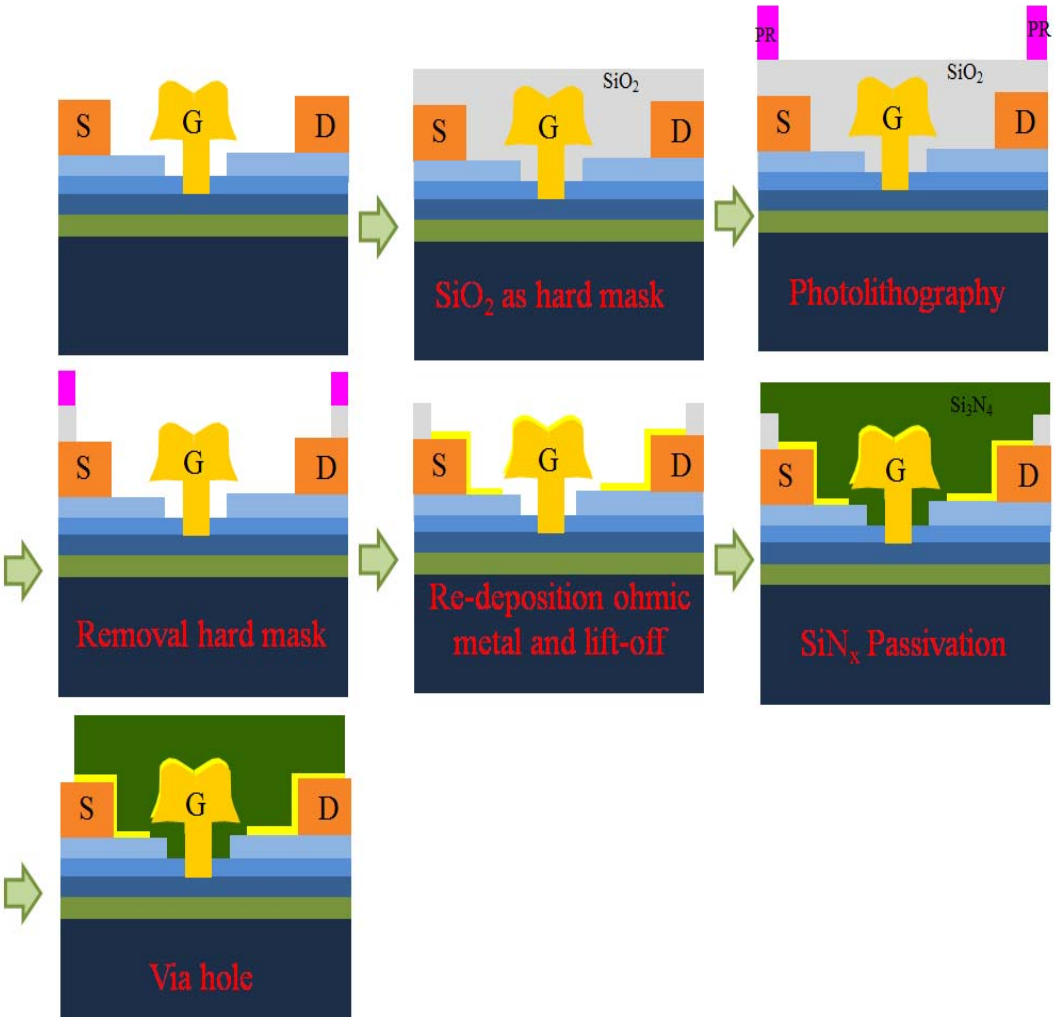


Fig. 2.8 The process flow of self-aligned gate technology for III-V QWFETs

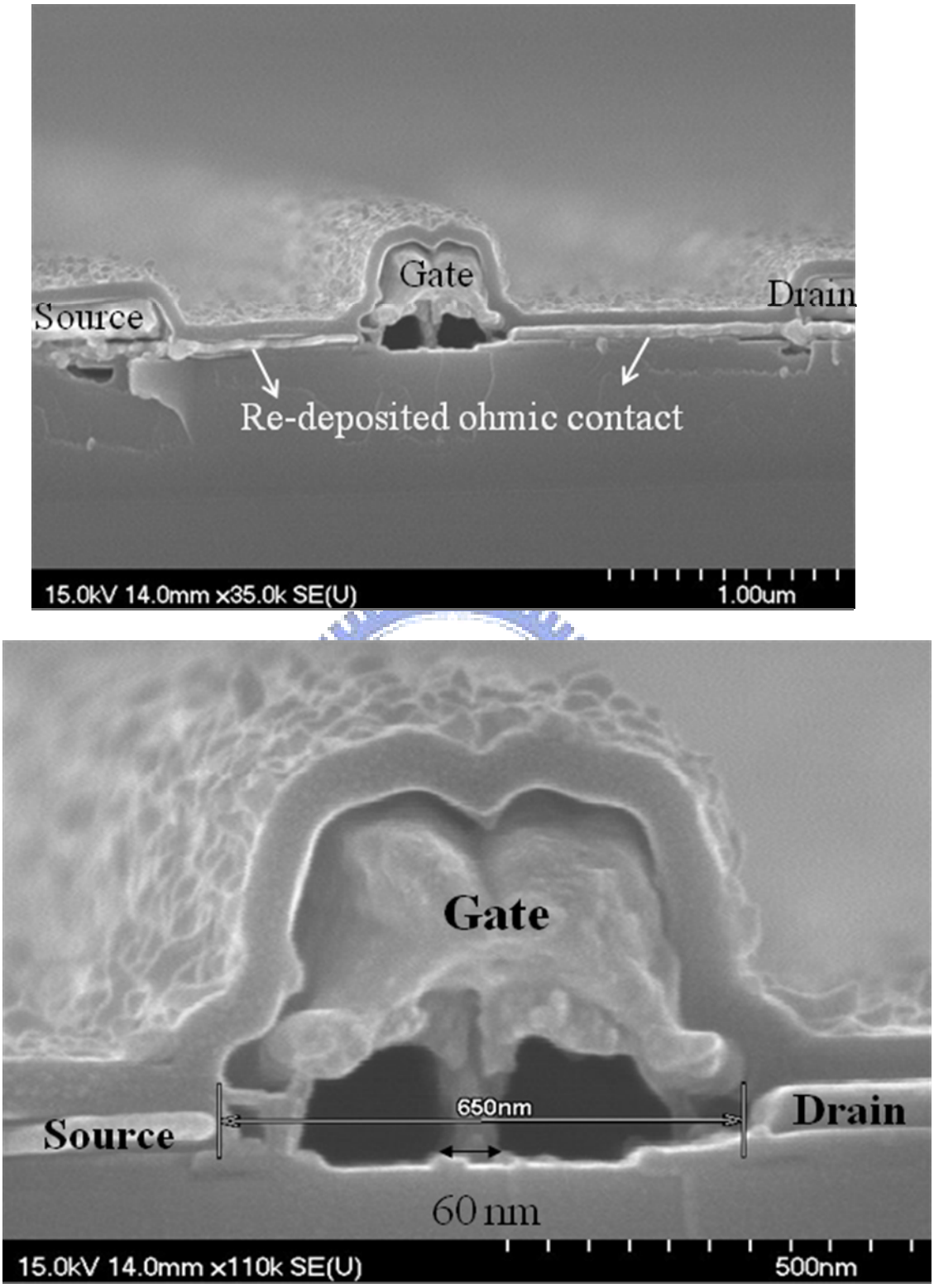


Fig. 2.9 The SEM image of the device with self-aligned gate process.

Chapter 3

DC and RF Measurements of InAs Quantum Well Field Effect Transistors with/without Self-aligned Gate Process

3.1 Device Characterization

DC and RF performance of the InAs QWFETs were measured using on-wafer probing facilities and testing instruments. The I-V characteristics were obtained easily by using an HP4142B Modular DC Source/Monitor and SUSS PA200 Semi-Auto Probe Station. The Transmission Line Model (TLM) method for determining specific contact resistance was adopted by using 4-wires measurement. The *S*-parameters for the QWFET devices were measured by HP8510XF Vector Network Analyzer using on-wafer GSG probes from Cascade MicroTech. However, finding the RF behavior of a device on a wafer was a complicated process. For conventional RF measurement of a packaged device, the wafer needs to be diced and then an individual die should be mounted into a test fixture. Deembedding between the die's and the fixture's responses became an issue. Furthermore, fixturing die was a time-consuming process, making it impractical for high-volume screening. Thus the need for on-wafer RF characterization was arisen [3-1].

Before examining the RF measurement process for the QWFETs, the electrical behavior and characterization of the QWFET device are stated in the following section. In this study, de-embedding which must also be performed to discover the true RF performance of the device is discussed.

3.2 DC characteristics [3-2]

The band diagrams at three different locations along the channel under biasd are illustrated in Fig. 3.1. There is a potential drop of channel charge density in the direction parallel to the channel, causing q'_{CH} to be a function of the position x. In order to relate the HEMT equations to the well-developed MOSFET equations, a per area gate oxide capacitance was define as C'_{OX} [3-3]. Therefore, the channel charge sheet density is expressed as:

$$q'_{CH} = -C'_{OX}[V_{GS} - V_T - V_{CS}(\chi)] \tag{3-1}$$

We denote the channel-to-source potential resulting from the applied Gate-Source voltage V_{GS} and Drain-Source voltage V_{DS}. V_T is threshold voltage and the x means the position along the channel. The additional potential $V_{CS}(x)$ is called the channel-source potential. When $V_{DS} \neq 0$, the channel channel-source varies with x. In this figure, the channel-source potential measures the potential difference between any point x along the channel with respect to the potential of the source. The channel current equation which we are familiar with $I = qA\mu_n\varepsilon$ (A=area) is proportional to the cross-section area of the current conduction, the charge density, the mobility μ_n, and the electric field. Therefore, we obtain the form of the drift equation in HEMT:

$$I_{CH}(\chi) = -WC_{OX}\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \tag{3-2}$$

We note that q'_{CH} is a negative quantity in QWFET, since electrons accumulated in the channel are negative charges. In fact, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have $I_D = -I_{CH}$, we find:

$$\int_0^L I_{DS}\,dx = -C'O\int_{V_{CS(o)}}^{V_{CS(L)}} C_{OX}\,\mu_n[V_{(GS)} - V_{(T)} - V_{(CS)}(\chi)]dV_{CS}(\chi) \tag{3-3}$$

To carry out the integration in Eq. (3-3), we assume temporarily that we are working in the linear region such that current saturation due to channel pinch off at the drain does not occur. The *I-V* characteristics after pinch off will be dealt with shortly. In the linear operating region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (3-3) leads to:

$$I_D = \frac{W_g C'_{OX} \mu_n}{Lg}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \tag{3-4}$$

Eq. (3-5) is plotted schematically in Fig. 3.2, with I_D shown as a function of V_{DS}. The value of V_{DS} corresponding to the attainment of $I_{D,sat}$ is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of I_D will respect to V_{DS} and setting the result to zero. We find that:

$$V_{DS,SAT} = V_{GS} - V_T \tag{3-5}$$

At this saturation voltage, q'_{CH} calculated from Eq. (3-1) is identically zero at the drain (pinch off). However, we realize that this conclusion originates from the fact that we are extending the validity of Eq. (3-1) all the way to where $q'_{CH}(L)$ is identically zero. Physically, the channel at the drain does not pinch off completely. Instead, there is a finite thickness of accumulation of charges at which q'_{CH} $x=L$ is nonzero. The drift velocity is high, but nonetheless finite, so a constant current is maintained throughout the channel. Therefore, a complete model of the drain current is given by:

$$I_{DS} = \frac{W_g C'_{OX} \mu_n}{Lg}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad \text{for } V_{DS} < V_{DS,SAT} \tag{3-6}$$

$$= \frac{W_g C'_{OX} \mu_n}{Lg}[\frac{(V_{GS} - V_T)^2}{2}] \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \tag{3-7}$$

For QWFETs, it is convenient to define the *saturation index (α)* as:

$$\alpha = 1 - \frac{V_{DS}}{V_{DS,SAT}} \qquad \text{for } V_{DS} < V_{DS,SAT}$$

$$= 0 \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}8)$$

The drain current increases due to the perturbations in V_{GS} and V_{DS}. The mutual transconductance measures the amount of current increase due to the increment in the gate bias.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS} = const.}$$

We also can write:

$$g_m = \frac{W_g C'_{OX} \mu_n}{L_g}(V_{GS} - V_T) * (1 - \alpha)$$

3.3 Breakdown characteristics

Breakdown mechanisms and models have been discussed in many articles. One of the models showing it is dominated by the thermionic filed emission (TFE) / tunneling current from the Schottky gate. This model predicts that the two-terminal breakdown voltage is lower at higher temperature because tunneling current increases with the temperature. Higher tunneling current occurs at higher temperature because carriers have higher energy to overcome the Schottky barrier. Other model suggests that impact-ionization determines the final two-terminal breakdown voltage, because the avalanche current decreases with increasing temperature. Lower avalanche current occurs at higher temperature because phonon vibrations as well as carrier-carrier scattering increase with increasing temperature. Either model is incomplete since coupling exists between TFE and impact ionization mechanisms. In addition, different

devices may suffer from different breakdown mechanisms, depending on the details of the device design (insulator thickness, recess, channel composition, and so forth). In this study, the gate-to-drain breakdown voltage BV_{gd} is defined as the gate-to-drain voltage when the gate current is 1mA/mm.

3.4 Scattering parameters [3-2]

Generally, the Scattering parameters, which referred to as S-parameters, are fundamental to microwave measurement. S-parameters are a way of specifying return loss and insertion loss or insertion gain. The relation of Z ports s-parameters are defined as follows:

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix}$$

S signals going into or coming out of the input port are labeled by a subscript 1. Signals going into or coming out of the input port are labeled by a subscript 2. The electric field of the microwave signal going into the component ports is designated a; that leaving the ports is designated b. Therefore,

a_1 is the electric field of the microwave signal entering the component input.

b_1 is the electric field of the microwave signal leaving the component input.

a_2 is the electric field of the microwave signal entering the component output.

b_2 is the electric field of the microwave signal leaving the component output.

By definition, then,

$$s11 = \left.\frac{b1}{a1}\right|_{a2=0}$$

$$s21 = \left.\frac{b2}{a1}\right|_{a2=0}$$

$$s12 = \left.\frac{b1}{a2}\right|_{a1=0}$$

$$s22 = \left.\frac{b2}{a2}\right|_{a1=0}$$

Consequently, s_{11} is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output. Because b_1 and a_1 are electric fields, their ratio is a reflection coefficient. Similarly, s_{21} is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, s_{21} is a transmission coefficient and is related to the insertion loss or the gain of the device. s_{22} is similar to s_{11}, but looks in the other direction into the device.

3.5 Current gain cutoff frequency f_T and maximum oscillation frequency f_{max}

The extrinsic transconductance, g'_m has to be measured through Rs. The two values are related as follows

$$g'_m = \frac{g_m}{1 + g_m R_s}$$

The f_T of a device is the frequency at which the short circuit current becomes unity. f_T is simply defined as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

, and the (C_{gs} + C_{gd}) is the total capacitance related to the Schottky gate contact. From this relation, we could see that in order to achieve higher f_T, larger g_m and small total gate capacitance must be achieved. Small total gate capacitance is accomplished by short gate length; for millimeter-wave applications the gate length is usually

smaller than 0.15 μm. In this equation

$$f_T = \frac{g_m}{2\pi C_G} = \frac{Z_G v_{sat}\varepsilon}{w} \bullet \frac{w}{\varepsilon Z_G L_G} \bullet \frac{1}{2\pi} = \frac{v_{sat}}{2\pi L_G}$$

the L_G is the is the gate length; therefore, the shorter the gate length the higher the f_T and higher the g_m. The intrinsic equivalent circuit derived from *S* parameters are used to determine the unity current-gain cut-off frequency (f_T). It can be determined by extrapolation of the short-circuit current gain $h_{21} = 0$ dB. h_{21} can be defined as

$$h_{21} = \frac{2\,S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}$$

Another important parameter is f_{max}, which is the frequency where the power gain falls to unity. f_{max} is expressed as

$$f_{\max} = \frac{f_T}{2\left(\frac{R_g + R_i + R_s}{R_{ds}} + (2\pi f_T R_g C_{gd})\right)^{\frac{1}{2}}}$$

This expression shows that to obtain useful power gain at high frequency, the f_T of a device must be large; in addition, the resistances of gate, source and drain must be small.

3.6 Device modelling technique

When defining the high frequency RF performance of the QWFETs, it is essential to de-embed all the conductors on the top surface of the wafer such as the pad, metal, and interconnect. Detailed layout of the device in this study is shown in Fig. 3-3. This helps us to understand what is going on at the active region of the device.

In this study, an approach that combines the conventional way and 3-D full wave

electromagnetic analysis is proposed to extracte the intrinsic parameters of devices. To accurately determine the equivalent circuit model, the overall structure is divided into several blocks, including gate parasitic, drain parasitic, source parasitic and intrinsic part according to the scalability of the device size as shown in Fig. 3-4, where the parasitic elements should be kept at fixed values and not scalable with device size. The intrinsic block could further be divided into different equivalent circuit elements and shown in Fig. 3-5. Standard gradient optimization routine is used to minimize the error function value, which is defined as the difference between the modelled and measured S-parameters. In order to rigorously determine the parasitic elements, CST Microwave Studio which is based on finite integration algorithm in time domain (FIT) is applied to analyse the structure. It is observed from the filed plot that the two source buses are held at a lower potential referenced to the gate and source pads thus the E-filed lines tend to terminate at these buses indicating a strong capacitive parasitic (Fig. 3-6 a). To illustrate the difference, a similar structure without the two source buses is simulated and the electric filed at 10 GHz is plotted in Fig. 3-6 b, where a much coarser electric field distribution between the gate (drain) pad and source region is observed. Based on the EM analysis of the structure, the strong capacitive parasitic behavior between the gate (drain) pad and the source buses suggests two additional capacitors to be included in the equivalent circuit.

3.7 Noise figure

High-frequency noise relates with the device channel and capacitive coupling between the channel and the gate. The gate noise is represented by a gate-current noise generator i_{ng}^2 and is caused by charge fluctuation in the channel, which in turn induces the fluctuation of compensating charge on the gate electrode. The channel

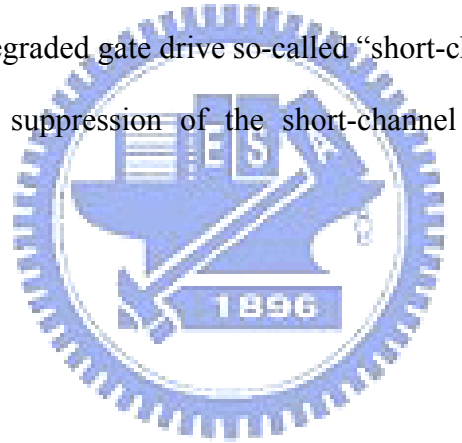
noise is represented by a drain-current noise generator i_{nd}^2 and is caused by various physical mechanisms driven by the electric field in the channel. Another noise source is gate leakage. The noise performance of a FET may be quantified by the noise figure, *NF*, which is a function of frequency, FET bias voltages, and impedance matching.

NF can be well approximated by the semi-empirical equation given by Fukui [3-4] and is shown as the following equation:

$NF = 1 + k\,(f/f_T)\,[g_m\,(R_g+R_s)]^{1/2}$,

$= 1 + 2\pi kf\,(C_{gs} + C_{gd})\,[g_m\,(R_g+R_s)]^{1/2}$, where k is a fitting parameter.

Generally, the reduction in Lg does not necessarily minimize the NF_{min} because R_g tends to increase due to a vertical resistance component of gate resistance, and also gm decreases due to a degraded gate drive so-called "short-channel effect". Therefore, a reduction in R_g and suppression of the short-channel effect are necessary to minimize NF_{min}.



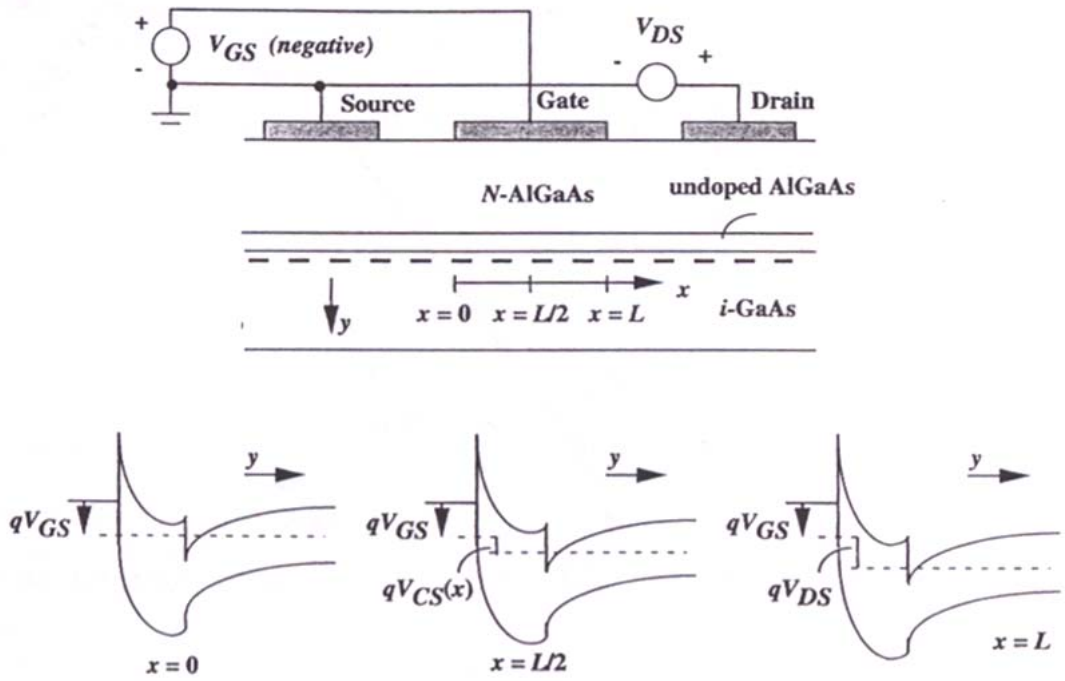


Fig. 3.1 Band diagrams at three different locations along the channel of a QWFET

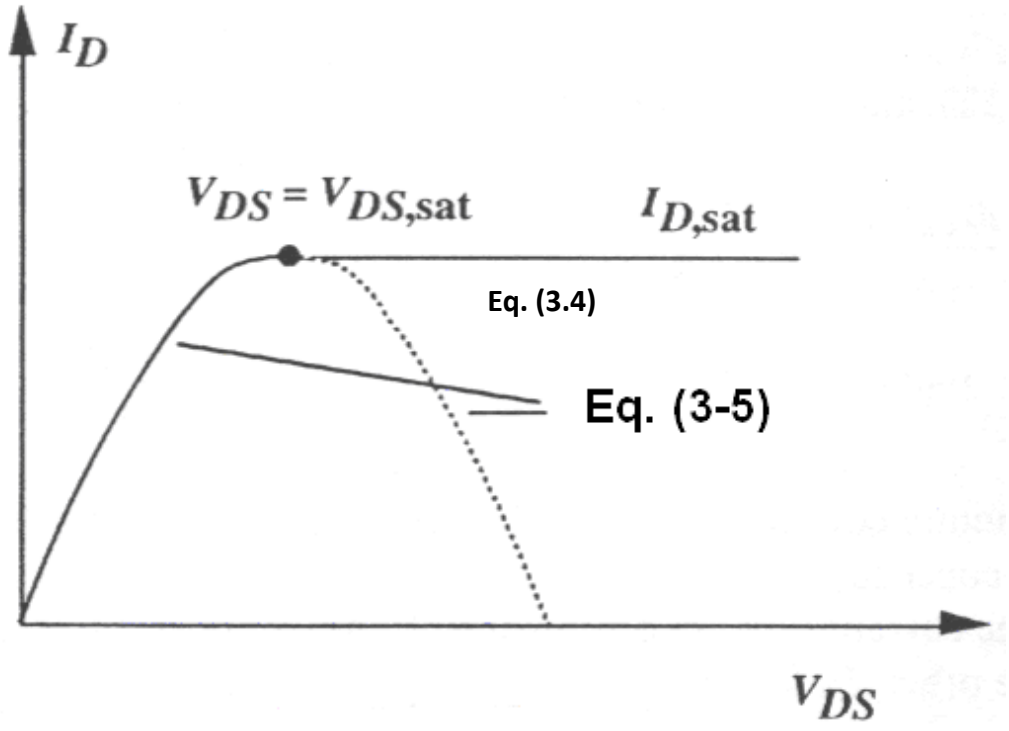


Fig. 3.2 Actual characteristics and those predicted by Eq. (3-3)

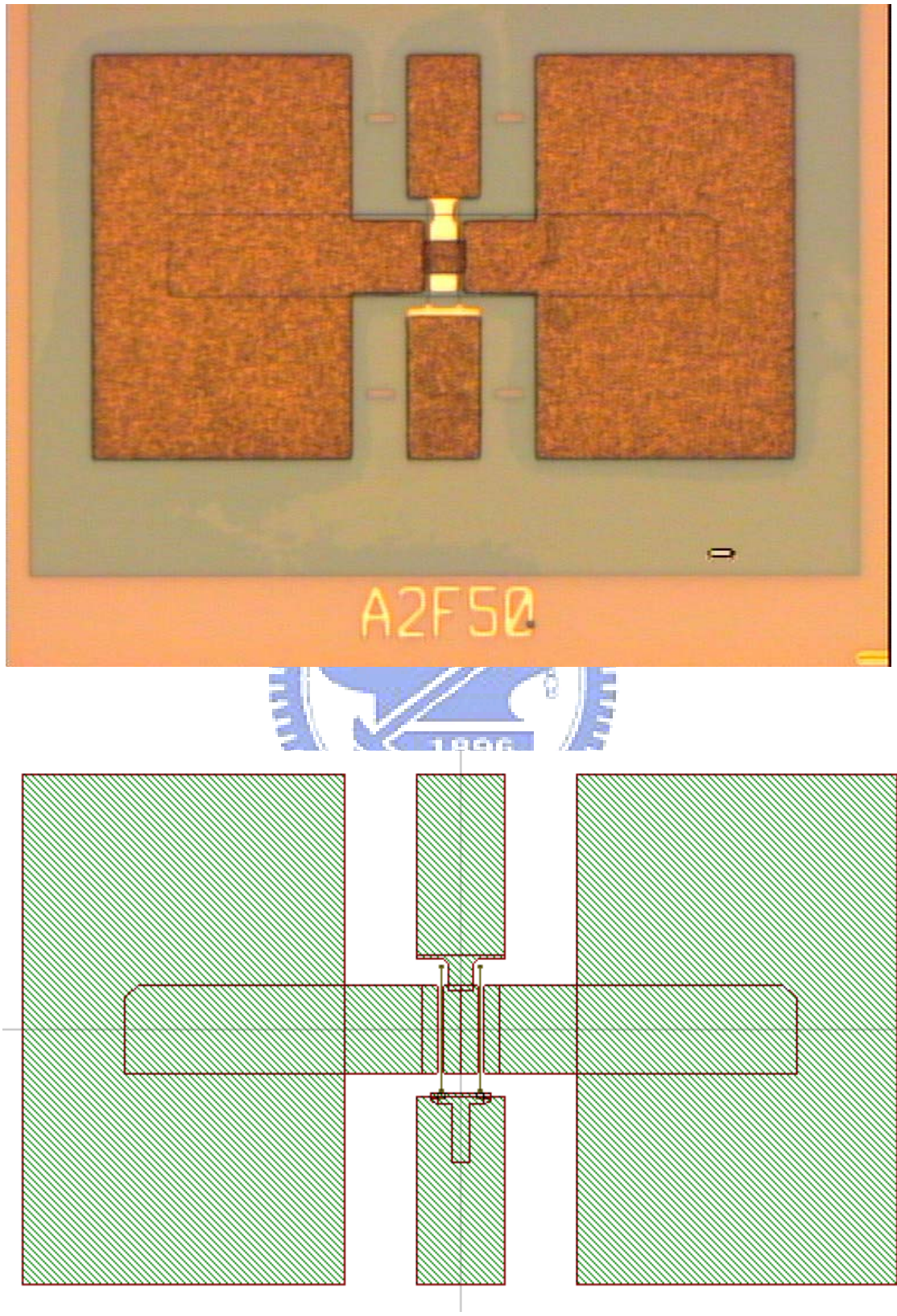


Fig. 3-3 Detailed layout of the device, the pads connecting the gate and drain are about 50×100um^2.

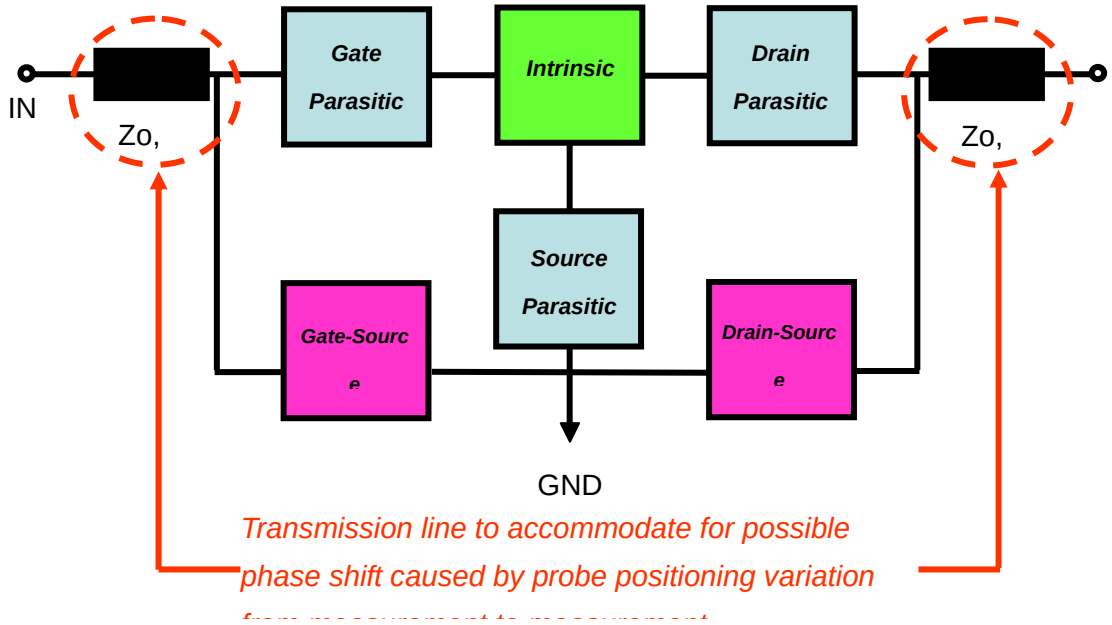


Fig. 3-4 The block diagram with determined parasitic elements for the overall device structure.

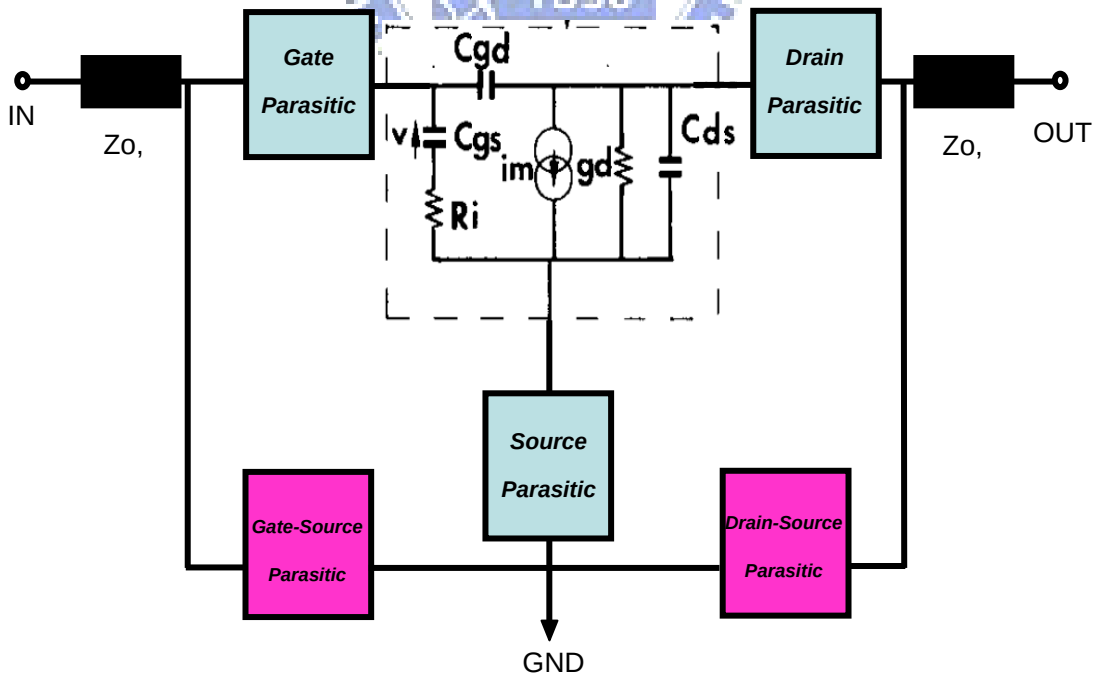


Fig. 3-5 Functional blocks of the equivalent circuit model, divided according the scalability with device size.

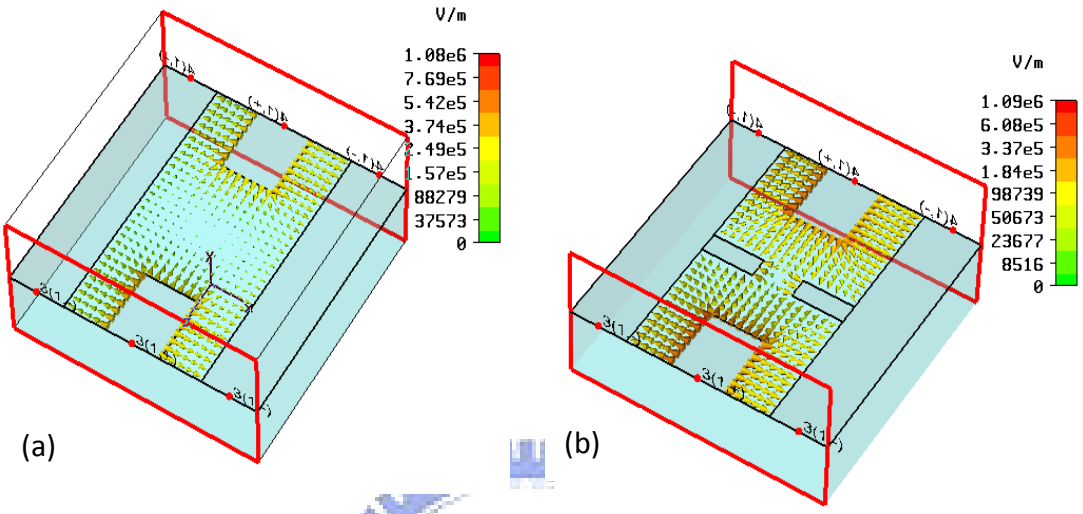


Fig. 3-6 Analyzed electric field plot of the 2x50um device at 10 GHz. (a) with the source buses of the device (b) without the source buses of the device

Chapter 4

DC and RF Characterisations of $In_{0.53}Ga_{0.47}As$/InAs/ $In_{0.53}Ga_{0.47}As$ Composite Channel QWFET Fabricated with Self-aligned Gate Process

4.1 Introduction

For the advanced wireless communications, InP-based Quantum Well Field Effect Transistors (QWFETs) have attracted many attentions and demonstrated excellent high-frequency performance because of their superior electronic transport properties and high saturation velocity [4-1, 4-2]. Moreover, it is also a potential candidate for low-power logic applications for Si CMOS technology beyond 22 nm node era [4-3, 4-4]. InP QWFETs usually use In-rich InGaAs channel or InAs/InGaAs composite channel to improve RF performance with large current drivability for the devices. Meanwhile, the gate-recess structure also plays a critical role in the high frequency performance of QWFET devices. In general, the transconductance (g_m) of the device is mainly influenced by the gate-channel distance and the reduction of the distance can effectively increase the current gain cutoff frequency (f_T) because of the enhancement of average electron velocity underneath the gate electrode.

Additionally, the shape of the recessed region not only affects the source and drain resistance (R_S and R_D) and the capacitances of gate-source and gate-drain (C_{GS} and C_{GD}), but also modulates the electric field in the channel. K. Shinohara et al. reported f_T value of 547 GHz in 30-nm gate pseudomorphic HEMTs by means of multilayer cap structure to reduce parasitic source and drain resistances [4-5]. H. Matsuzaki et. al. has employed Tiered-Edge Ohmic structure and low-k

benzocyclobutene (BCB) passivation to effectively minimize parasitic gate capacitance and achieve relatively high g_m and f_T values [4-6]. Although the results seemed rather promising, yet relatively complicated fabrication processes were involved in the reduction of the parasitic elements.

In this study, the $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel QWFETs were fabricated with self-aligned gate technology. It is fabricated with the ohmic metal re-deposition which effectively reduced the source/drain spacing from 3 μm to 650 nm. The measurement results in this study clearly evidenced that superior device performance can be easily achieved through a few added fabrication process with optimal epi structure to those proposed in [4-5] and [4-6].

The self-aligned gate (SAG) technology can greatly reduce the source/drain spacing, which helps to lower the source and drain resistance (R_S and R_D) by forming a low access resistance contact [4-7]. It has obvious improvement for the DC and RF performance of InAs-channel QWFET device with SAG process.

4.2 Experiment

The QWFET structure was grown by molecular beam epitaxy on a 3-in diameter InP substrate. It has a 50 Å InAs channel layer with 20 Å $In_{0.53}Ga_{0.47}As$ upper sub-channel and 30 Å $In_{0.53}Ga_{0.47}As$ lower sub-channel were grown on top of the 500-nm-thick InAlAs buffer layer. The $In_{0.53}Ga_{0.47}As$ sub-channels were applied to enhance the electron confinement in the thin InAs layer and improve the electron transport properties [4-8]. A 30 Å-thick InAlAs spacer, a Si-δ-doping with 4×10^{12} cm^{-2}, a 5 nm-thick InAlAs barrier. A 4-nm-thick InP etching stop, and a 40 nm-thick InGaAs cap layer with 2×10^{19} cm^{-3} Si-doping were grown on top of the composite channel layers.

For the device fabrication, the active area of the device was isolated by wet etch. The ohmic contacts which can attain low contact resistance (R_c) were formed with 3 μm source-drain spacing by evaporating Au metal on heavily doped n-InGaAs cap layer. For the T-shaped gate process, it was performed by the 50kV JEOL electron beam lithography system (JBX 6000 FS) with trilayer e-beam resist. Succinic acid/H_2O_2/NH_4OH solution was used for gate recess and then Pt (8 nm)/Ti (60 nm)/Pt (80 nm)/Au (180 nm) were deposited as Schottky gate metal and lifted off by ZDMAC to form 60 nm T-shaped gate. To protect the 60 nm T-shape gate, the SiO_2 layer was deposited as a hard mask by PECVD at 200℃. After that, the SiO_2 within the mesa region was removed and a thin Au layer was re-deposited as ohmic metal. Finally, the devices were passivated by PECVD SiN_x.

4.3 DC Characterisations

Fig. 4.1 and Fig. 4.2 show the DC I-V curve of the device with 2×50 μm gate width with and without using SAG technology. The device with SAG process exhibited very good pinch-off characteristic and the saturation current of 517 mA/mm at V_{DS} = 0.5 V and V_{GS} = 0 V was achieved as compared to the drain current of 391 mA/mm for the device without SAG process. This enhancement of drain current density was mainly due to that the SAG process greatly decreases the access resistance and the highly doped cap layer structure with high doping helps to form the non-alloy ohmic contacts with a low specific contact resistance. In this study, the extracted values of source resistance R_S was 5 Ω for device without SAG process compared to 1.1 Ω for device with SAG process. As a result, it is concluded that the reduction of parasitic resistance by reducing the access resistance between source (drain) and gate is the main reason for the performance enhancement of the device,

because the increase in current is as high as 126 mA/mm.

The transconductance, g_m and the drain source current plotted as functions of V_{GS} for devices without and with SAG process are shoen in Fig. 4.3(a) and (b). The peak g_m value increased from 946 mS/mm for the device without SAG process to 1348 mS/mm for that with SAG process, both measured at V_{DS} = 0.5 V. This increase is mainly attributed to the enhancement of the I_{DS}. Meanwhile, the threshold voltage slightly shifted from -0.58V (without SAG) to -0.6 V (with SAG) when biased at V_{DS} = 0.5V. The threshold voltage is defined as the V_{GS} when I_{DS} reaches 1 mA/mm. It is probably due to the scaling of gate-drain distance which increase the electric field between gate and drain and modifies the threshold voltage.

As for the gate-drain breakdown voltage ($V_{DG,BR}$), the value decreased from 3.6V for device without SAG process (Fig. 4.4(a)) to 3.4V for that with SAG process (Fig. 4.4(b)), which is mainly due to the increase of the electric field between gate and drain which makes the device breakdown voltage decreases. However, the diminution of the gate-drain breakdown voltage is still acceptable for low voltage application. We also check the gate leakage current at several different V_{GS} and V_{DS} in Fig. 4.5, the device has larger gate leakage current after SAG process but the value is still lower than 1 mA/mm.

4.4 High Frequency Characterisations

The S-parameters of the 2×50 μm device were measured from 2 to 40 GHz using on-wafer probing system with HP8510XF network analyzer. Fig. 4.6 and Fig. 4.7 show the frequency dependence of the current gain H_{21} and the power gain MAG/MSG of the device with/without SAG process measured at V_{DS} = 0.6V and V_{GS} = -0.1V. The parasitic effects (mainly capacitive) due to the probing pads have been

carefully removed from the measured S-parameters using the same method as in Fig. 4.8 and the equivalent circuit model in Fig 4.9. Since the geometry of the probing pads are relatively large compared to the device itself, the S-parameters of the open probing pads have been carefully characterized through full-wave electromagnetic simulations with measurement. Standard gradient optimization routine with tolerance level of delta S less than 0.01% were set as the convergence criterion during the fitting process. The derived small equivalent circuits are exhibited in Fig. 4.8 and Fig 4.9, and some critical parameters are summarized in Table 4.1.

After SAG process, the source resistance (R_S) was reduce from 5.5 Ω to 1.1 Ω and the drain resistance also reduced to 1.0 Ω. The simulate result is shown in Fig. 4.8. The H_{21} curve becomes more straight in lower frequency in Fig. 4.7, and it is another evidence of the reduced R_s for less feedback effect. It proves that the SAG process truly reduces the access resistance and improves the saturation current density. But the fringing capacitance has slight increased because of the close spacing between the electrodes. From the Fig. 4.9 (a) and (b), the capacitance at the gate-source end was extracted to change from 36.76 fF to 44.47 fF and the capacitance at the gate-drain end also varied from 45.19 fF to 57.23 fF, an increase of ~25% was observed.

A current gain cut-off frequency f_T of 205 GHz and the maximum oscillation frequency f_{max} of 180 GHz were obtained for device with SAG technology as compared to that of f_T = 187 GHz and f_{max} = 170 GHz for the device without SAG technology. This improvement in the RF performance was due to decrease of the source resistance (R_S) and the increase of g_m in the applied gate bias range. It is believed that the RF performance can be improved if we can design the device layout with a low fringing capacitance.

4.5 High Speed Switching

For logic performance of the device with SAG process, the subthreshold slope and DIBL were 101.4 mV/dec and 75.6 mV/V, respectively. Fig. 4.10 shows the characteristics of the device with SAG process with various choices of the threshold voltage as defined in [4-9] at V_{DS} = 0.5V. The I_{ON}/I_{OFF} ratio achieved in the order of 10^3. These superior performances have also made such device a potential candidate for future high-speed and low-power logic applications.

4.6 Conclusion

In this study, the use of a new proposed self-aligned gate technology to enhance the DC and RF performances of the QWFETs has been demonstrated. The InAs-channel QWFETs exhibit I_{DS} =517 mA/mm; g_m =1348 mS/mm, and a f_T (f_{max}) of 205 GHz (180 GHz) after SAG process. It is believed that the SAG technology can have a conspicuous improvement of the DC and RF performance of the QWFETs. The device with SAG process also maintains well gate-drain breakdown voltage and excellent logic characteristics. The results demonstrate that superior QWFET device performance enhancement (in Table 4.1) for high frequency, high-speed and low-power logic applications can be achieved through the adoption of self-aligned gate process with optimal epitaxy. The parasitic source resistance and drain resistance were significant reduced from 5.0 Ω to 1.1 Ω, and C_{GS} and C_{GD} increasing is pay for closely electrode spacing.

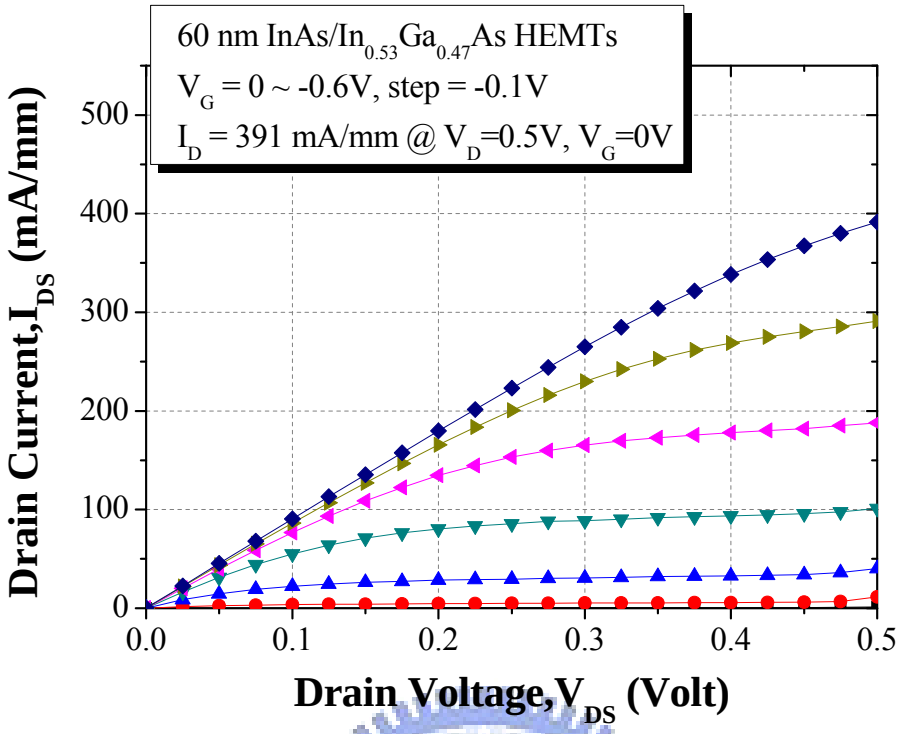


Fig 4.1 Characteristic curve for device before self-aligned gate process

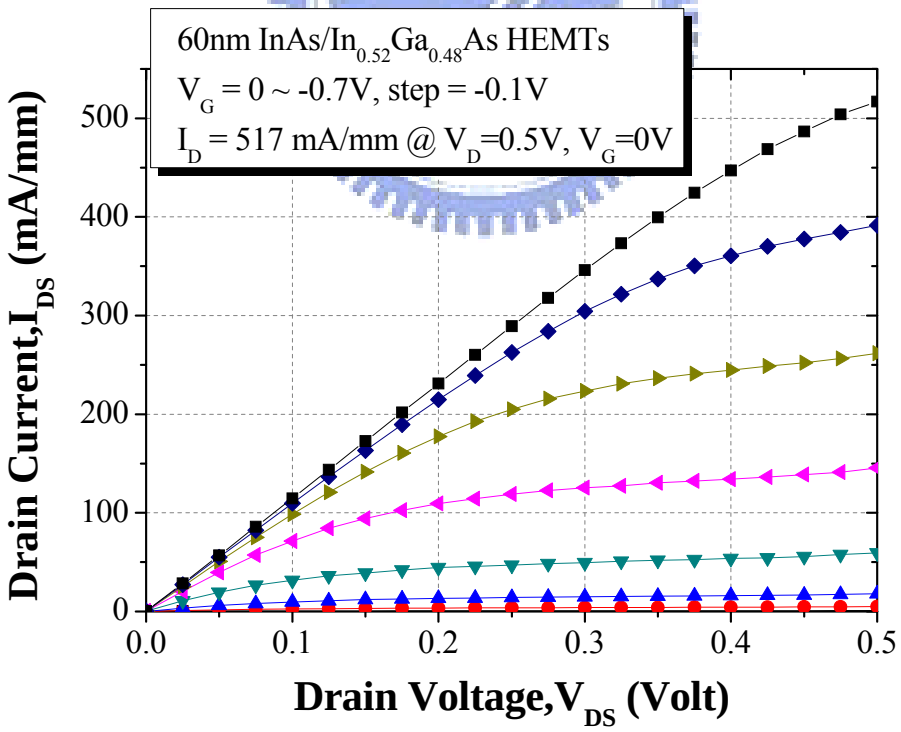


Fig 4.2 Characteristic curve for device with self-aligned gate process

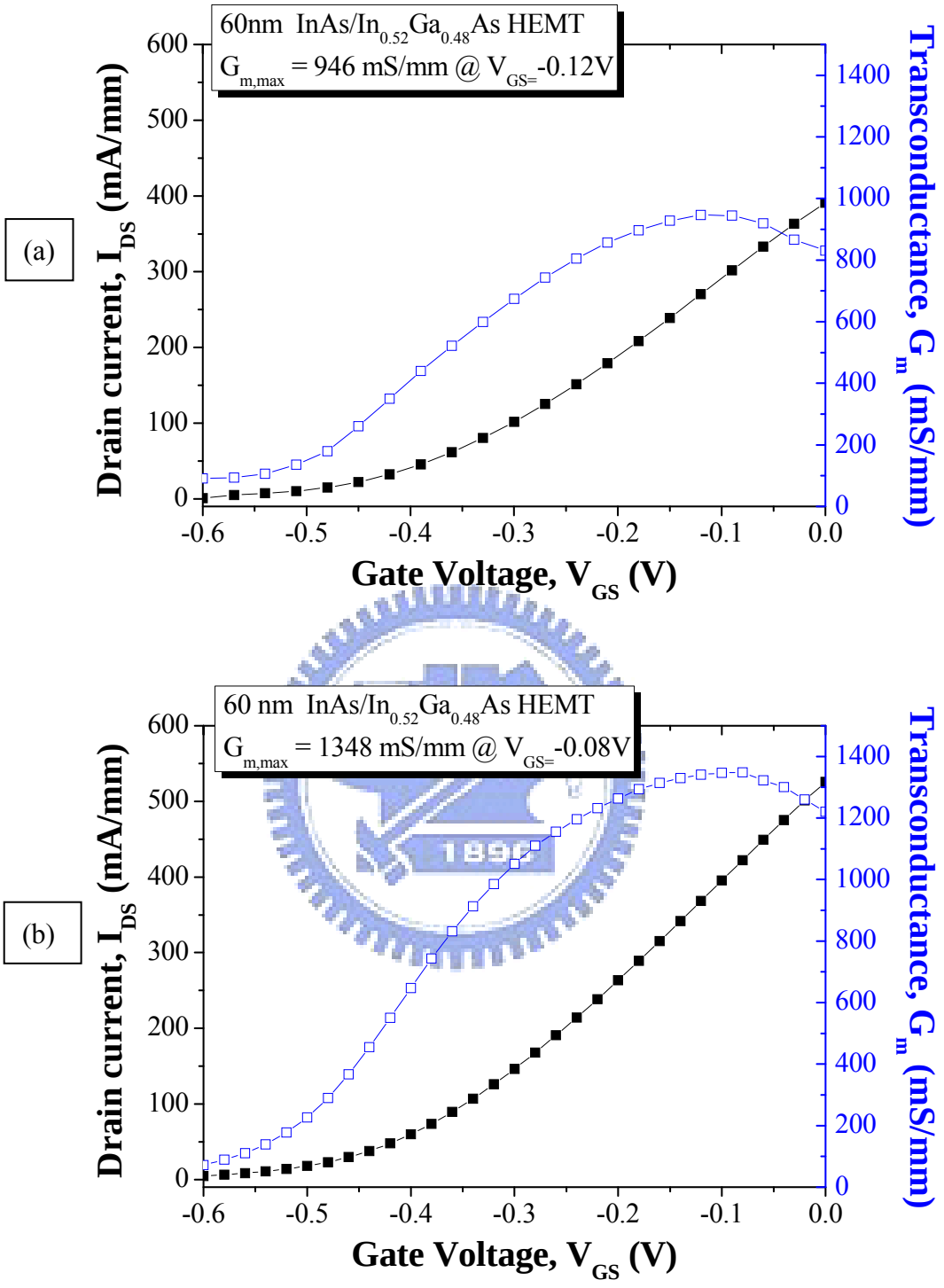


Fig 4.3 Transconductance versus gate-source voltage of the device (a) without SAG process, (b) with SAG process

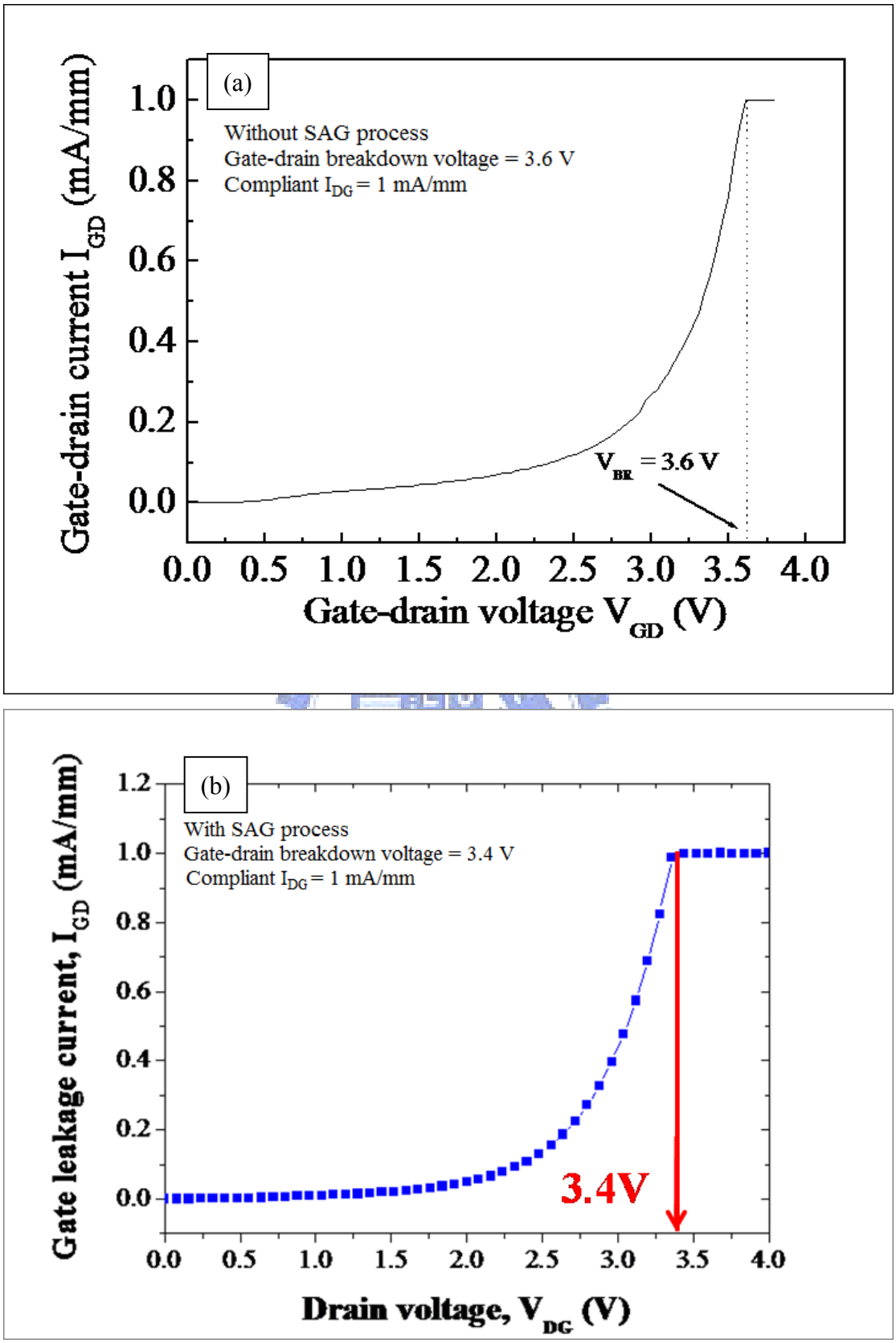


Fig. 4.4 Two terminal gate-to-drain breakdown characteristics of device (a) without SAG process, (b) with SAG process

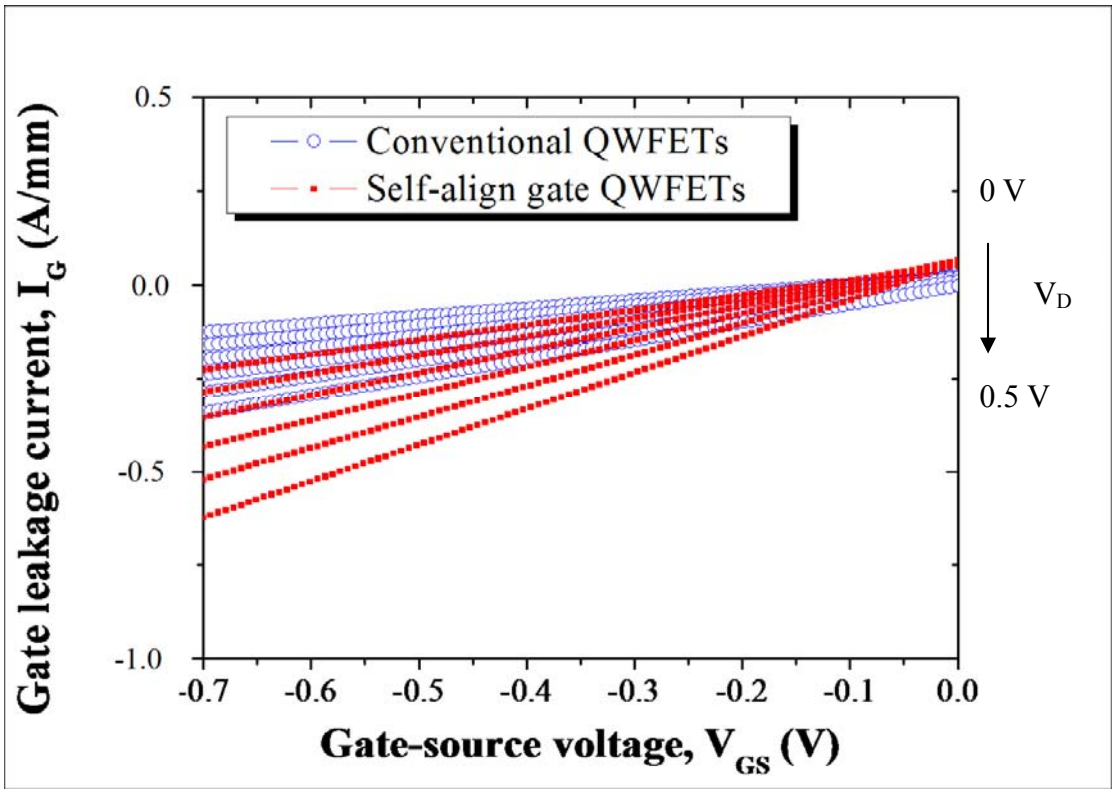


Fig. 4.5 Gate leakage current density versus gate-source voltage for the device with/without SAG process

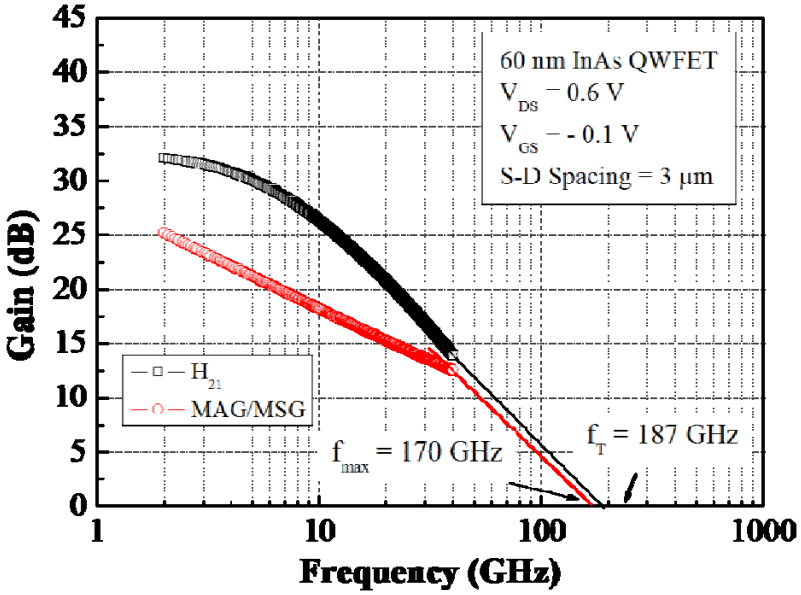


Fig 4.6 Frequency dependence of the current gain H_{21} and the power gain MAG/MSG of the InAs channel QWFETs without SAG process. The frequency range was from 2 to 40 GHz, and the device was biased at V_{DS} = 0.6V and V_{GS} = -0.1V.

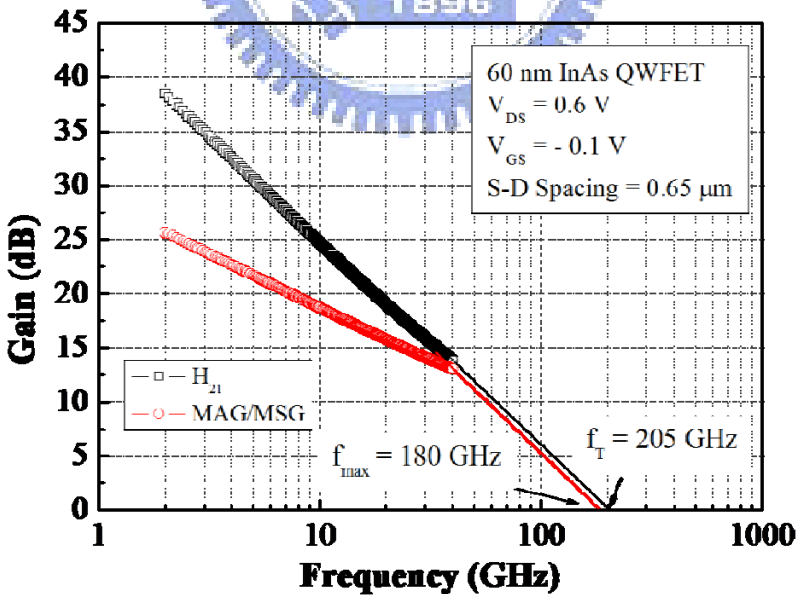


Fig 4.7 Frequency dependence of the current gain H_{21} and the power gain MAG/MSG of the InAs channel QWFETs with SAG process. The frequency range was from 2 to 40 GHz, and the device was biased at V_{DS} = 0.6V and V_{GS} = -0.1V.

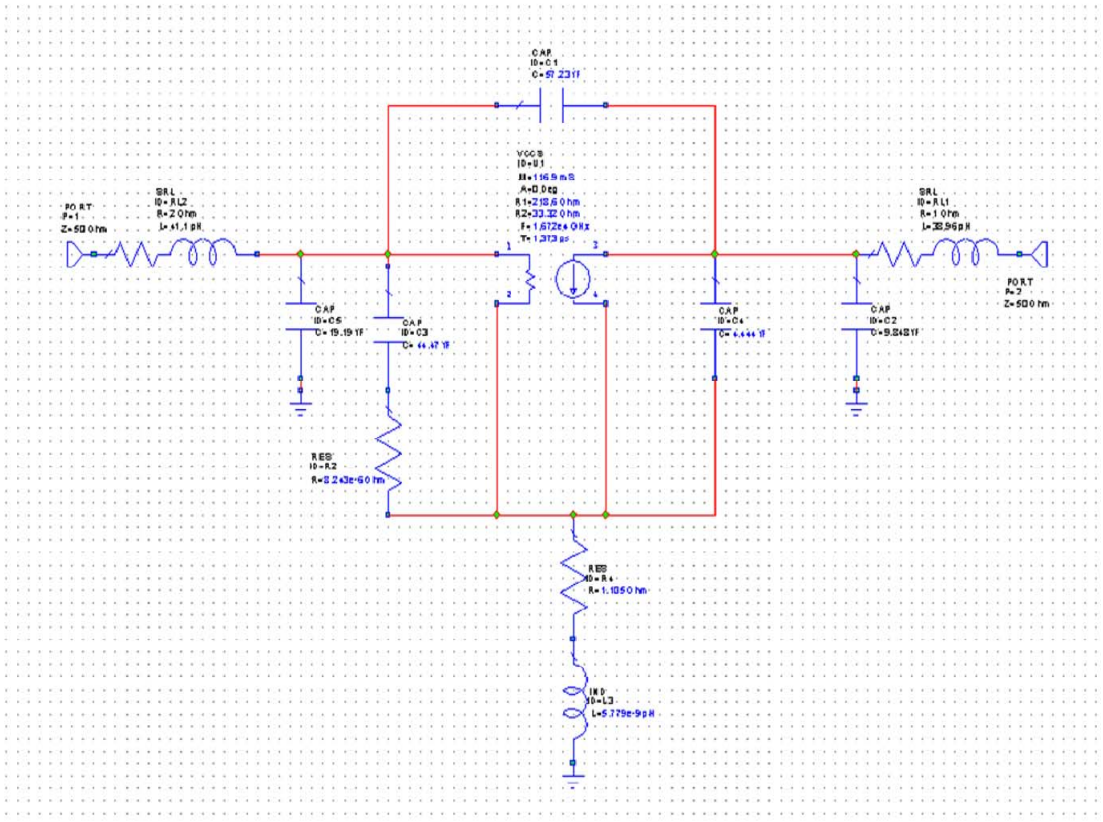


Fig. 4.8 The simulate result of small signal equivalent circuit with the parasitic effect after SAG technology

(a)

(b)

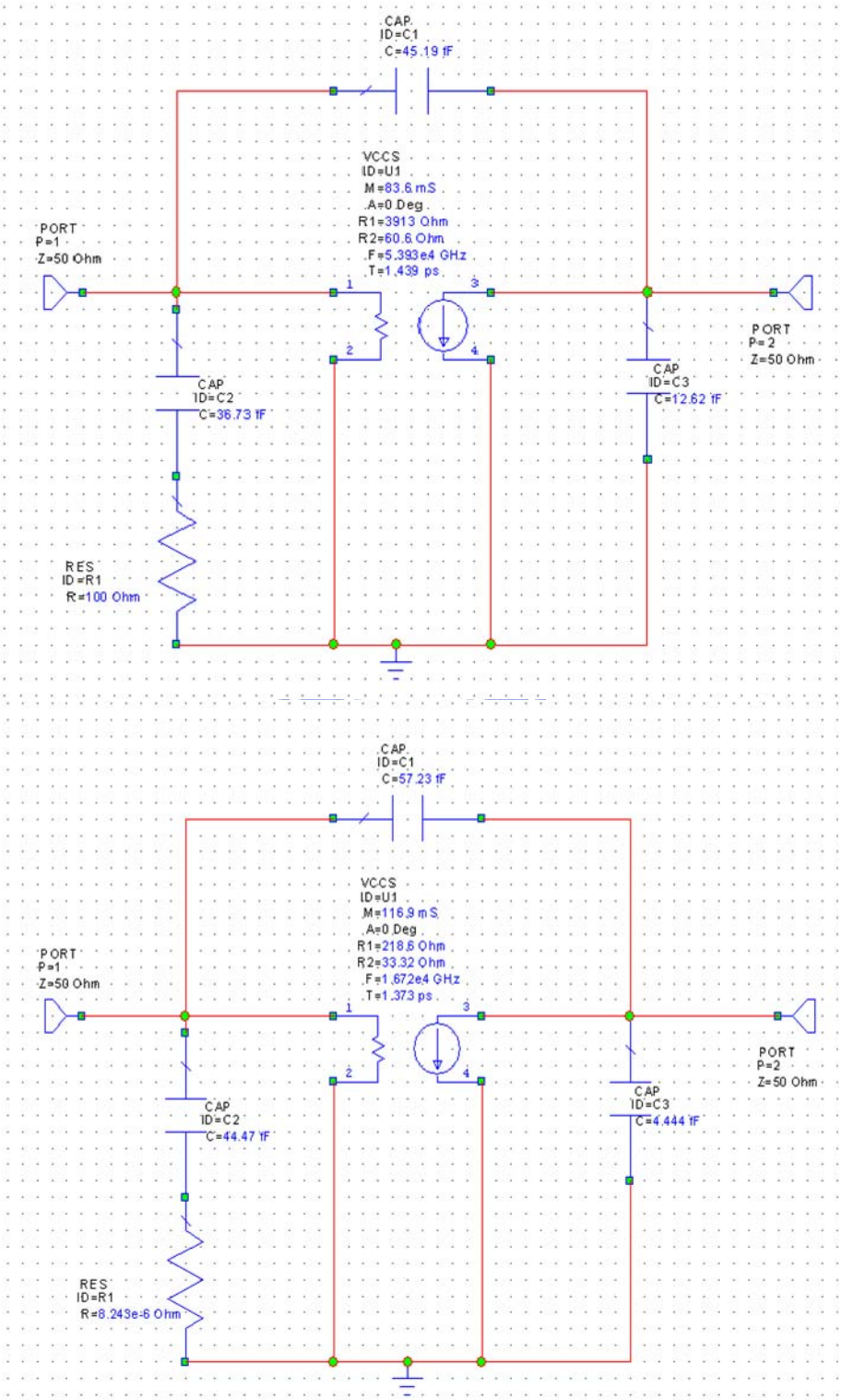


Fig. 4.9 The simulate result of intrinsic small signal equivalent circuit which removing the parasitic effect for the device (a) before SAG process, (b) after SAG process.

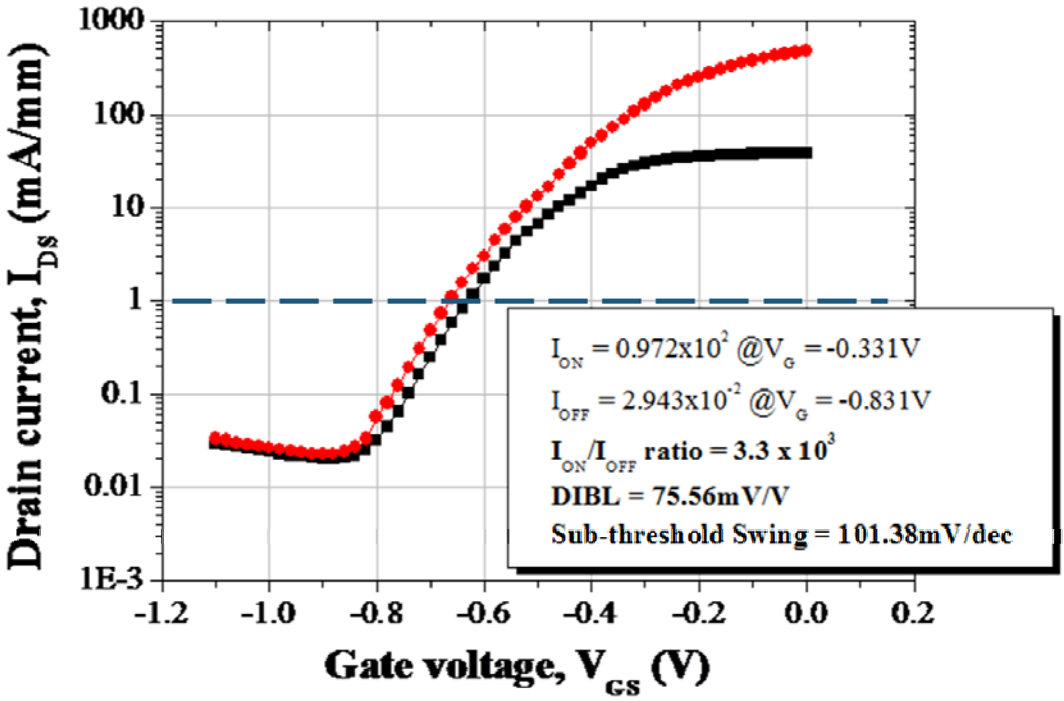


Fig. 4.10 The sub-threshold, DIBL and I_{ON}/I_{OFF} ratio characteristics of the InAs channel QWFET with SAG process at the V_{DS} of 0.05 and 0.5V.

InAs/ $In_{0.53}Ga_{0.47}As$ QWFETs	R_S ,R_D (Ω)	C_{GS} (fF)	C_{GD} (fF)	C_{DS} (fF)	$G_{m,RF}$ (mS)	f_T (GHz)	f_{max} (GHz)
Without SAG process	5.0	36.73	45.19	12.62	83.6	187	170
With SAG process	1.1	44.47	57.23	4.44	116.93	205	180

Table 4.1 Summary of the QWFET device parameters with and without SAG process

Chapter 5

Conclusion

In this dissertation, a novel proposed SAG technology, additionally applied to the conventional QWFET process to reduce source-drain electrode spacing with in-expensive facilities, is successfully demonstrated by our group. The device with SAG process can achieve very low access resistance and source (or drain) resistance. It is helpful to increase the saturation drain current density (I_{DS} = 391 mA/mm → 517 mA/mm) and to enhance the transconductance (g_m = 946 mS/mm → 1348 mS/mm). Even if there are slight increase of source-to-gate capacitance (or drain-to-gate capacitance) and gate leakage current density, the device still exhibits a promotion of current gain cut-off frequency and the maximum oscillation frequency (f_T = 187 GHz → 205 GHz and f_{max} = 170GHz → 180 GHz) at low applied voltage. The 60 nm SAG QWFET device also shows excellent logic characteristics with I_{ON}/I_{OFF} ratio = 3.3 x 10^3, DIBL = 75.6 mV/V and S.S. = 101.4 mV/dec. Although the gate-drain breakdown voltage had slight diminution by 0.2 V, this ameliorative self-aligned gate technology still show the effective influence of the device performance improvement. It demonstrated the necessary of the self-aligned gate technology for the future QWFET device with high frequency, high-speed and low-power consumption applications.

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