國立交通大學

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碩士論文

利用閘極掘入方式製作增強型高截止電壓氮化鋁鎵/氮化鎵/氮化鋁鎵金屬-絕緣體-半導體高電子遷移率電晶體之研究

Study of Recessed Enhancement-mode AlGaN/GaN/AlGaN MIS-HEMT with High Threshold Voltage

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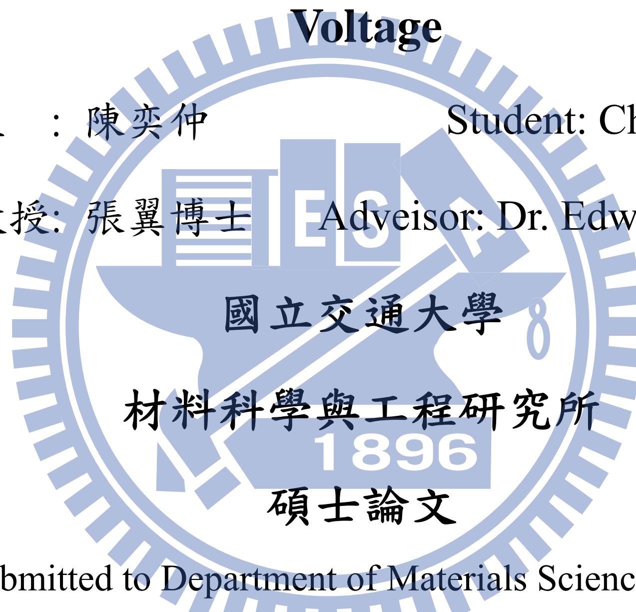

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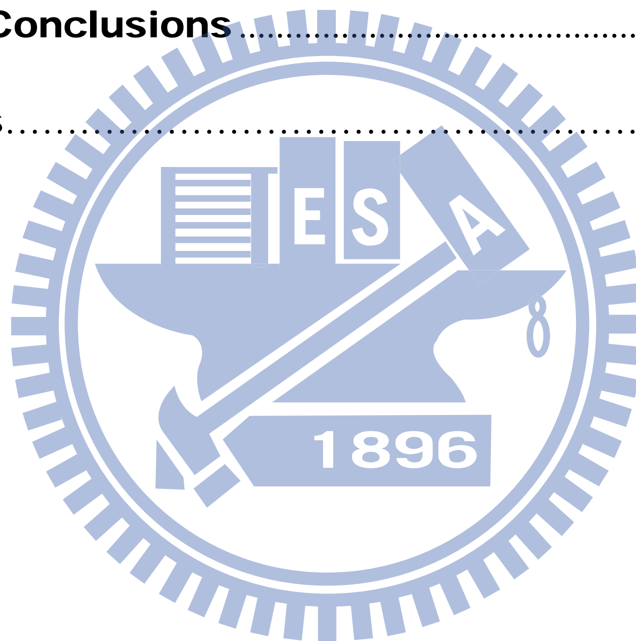

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摘要

氮化鋁鎵/氮化鎵/氮化鋁鎵增強型高電子遷移率電晶體近幾年來廣受注目，但由於目前之元件磊晶技術所製作的高電子遷移率電晶體之電流與電壓接仍偏低，尚無法做商業上之使用。而近年來之研究重點:金-氧-半場效電晶體雖擁有較高的起始電壓，但由於製程上尚未成熟，加上比起高電子遷移率電晶體其擁有較高的通道電阻，故仍未能通過工業使用標準。

本研究提出以閘極蝕刻之方式來製作增強型高起始電壓氮化鋁鎵/氮化鎵/氮化鋁鎵金屬-絕緣體-半導體高電子遷移率電晶體，並建立其標準化製程。此結構擁有比起金-氧-半場效電晶體較為簡易的製程，並擁有較低的電阻，同時此結構亦可達到較高之截止電壓。本實驗以蕭特基二極體做各種製程之參數測試，以找到對元件表現最好的使用條件，並成功建立金屬-絕緣體-半導體高電子遷移率電晶體之標準製程。此元件擁有

2mA/mm的通道電流，0.8mS/mm之互導係數，並擁有超過200V之崩潰電壓，更達到了9V的高截止電壓。而此結構同時亦可用於製作截止型高電子遷移率電晶體，擁有280mA/mm之電流與75mS/mm之電導，同時亦可在高電壓下操作。

Study of Recessed Enhancement-mode AlGaN/GaN/AlGaN MIS-HEMT with High Threshold Voltage

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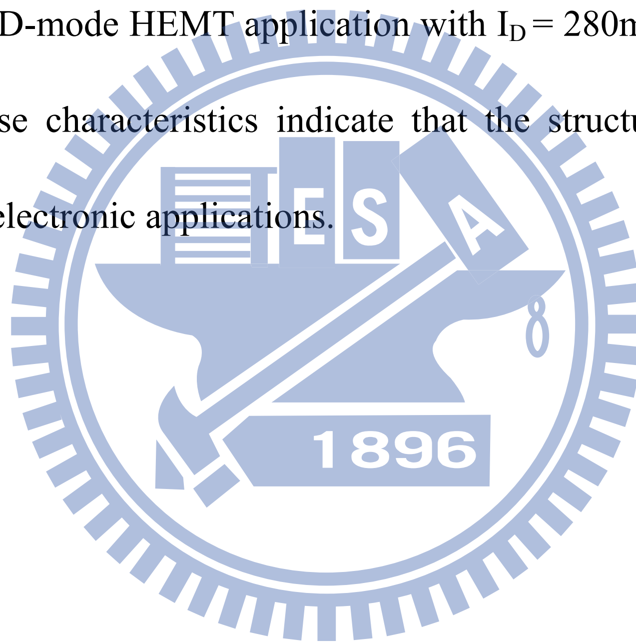
Abstract

AlGaN/GaN/AlGaN enhancement-mode high electron mobility transistor (HEMT) is extensively studied in recent years. However, there is still no solution to fabricate a HEMT with high threshold voltage, which means that it will cause mis-operation in high voltage operation. For enhancement mode operation (E-mode), metal-oxide-semiconductor field effect transistor (MOS-FET), though it has higher threshold voltage, it is not commercialized due to the immature process techniques and higher on-resistance than HEMT. In this thesis, gate recess technique is used to fabricate E-mode AlGaN/GaN/AlGaN metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT). This structure has simpler process and lower on-resistance in comparison with MOS-FET. Additionally, this structure can achieve very high threshold voltage to avoid the mis-operation of the device.

Schottky diode was used for process parameter evaluation to find out the optimum process condition, and then the recessed E-mode MIS-HEMT standard process was established. The device demonstrated 2 mA/mm, 0.8 mS/mm, and more than 200V for channel current, transconductance, and three-terminal breakdown voltage, respectively. Furthermore, the device shows 9V threshold voltage. The structure can also be applied to conventional D-mode HEMT application with I_D = 280mA/mm and Gm = 75 mS/mm. These characteristics indicate that the structure is promising for high voltage electronic applications.



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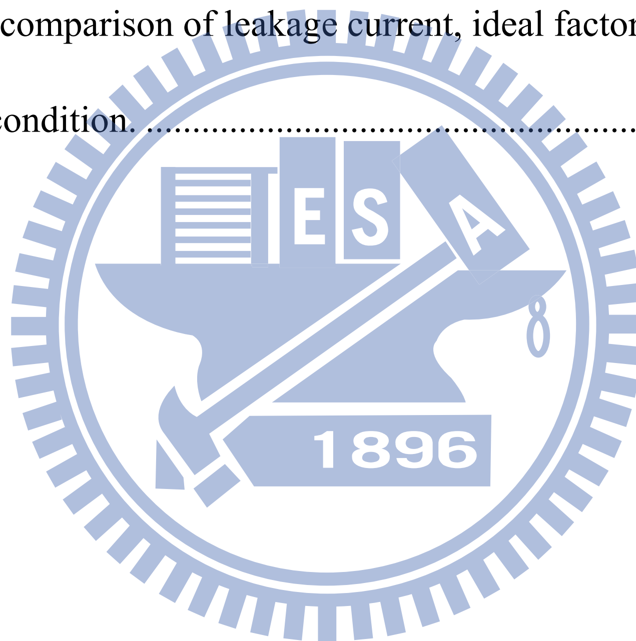

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Chapter 1
Introduction

In recent years, GaN and the related compounds play more and more important role in power electronics due to its unique properties such as high breakdown voltage ((2×10^{6} V/cm), wide direct band gap (3.4 eV), high saturation velocity (2.2×10^{7} cm/s) and large power density compared to other materials as listed in Table 1-1. Due to their superior material properties compared with conventional Si devices, GaN-based electron devices have lately attracted considerable attentions as next-generation devices for power electronic applications such as automobile electronics, satellite, and base station. Among these applications, enhancement-mode (E-mode) devices play a very crucial role. Enhancement mode devices can not only simplify the design of the circuit, but also has lower standby power dissipation and good for fail safety issue.

Several approaches for fabricating E-mode devices have been proposed. For instance, recess techniques [1-2] , which include chlorine based gas to do dry etching beneath the gate region. Other approaches such as p-type gate structure [3–5], thin AlGaN barrier layer [6-8], fluoride-based plasma treatment [9-12], Cat-CVD SiN deposition [13], and p-type gate structure

[14–16], have also been reported. However, the threshold voltage of these devices is not high enough to avoid noise interference for power applications. In hundreds volts operation, a slight noise will cause misoperation of the devices. According to the demand of circuit design for power electronics, a threshold voltage up to 3-5 V is generally required [17].

In order to reach the requirement, metal-oxide-semiconductor field effect transistor (MOS-FET) structure is proposed.[18]-[27]. For GaN-based enhancement -mode MOS-FET, the threshold voltage is generally higher than 3V. However, it has some drawbacks as following: (1) on-resistance is quite lower than high electron mobility transistor (HEMT) since it lacks the two dimension electron gas (2DEG), (2) implant process is required and it means one more processing step than HEMT process is need,(3) there is no mature approach to grow p-type GaN substrate to form n channel. To solve the problems, Sharp Corp. proposed a new structure, recessed MIS-HEMT structure [28]. It owns the advantage of conventional HEMT, which has low on-resistance, and the advantage of MOS-FET, which has high threshold voltage. In this study, standard process of recessed E-mode AlGaN/GaN/AlGaN MIS-HEMT is established and its performance is also characterized.

Table.1-1 Property comparison between different materials.

Property	Si	GaAs	SiC	GaN
Energy Gap (eV)	1.11	1.43	3.2	3.4
Critical Breakdown Field (MV/cm)	0.6	0.65	3.5	3.5
Thermal Conductance (W/cm.°K)	1.5	0.5	4.9	1.5
Mobility (cm^2/V-s)	1300	6000	600	1500
Power Density (W/mm)	~0.8	~1.0	2~4	>2
Saturation Velocity (cm/s)	$1x10^7$	$1.3x10^7$	$2x10^7$	$2.7x10^7$

Chapter2
Literature Review

2-1 The Mechanism of High Electron Mobility Transistor (HEMT)

Historically, the invention of HEMT is usually attributed to Takashi Mimura (Fujitsu, Japan). However, Ray Dingle and his co-workers in Bell Laboratories also played an important role in the invention of HEMT. It is also called as heterojunction field effect transistor (HFET) or modulation-doped field-effect transistor (MOD-FET). The structure incorporates a junction between two materials with different band gaps (i.e., a heterojunction) as the channel instead of a doped region, as is generally the case for MOS-FETs. It applies two layers to form heterojunction, one is a highly doped wide band gap n-type donor-supply layer (AlGaN in our example) and a non-doped narrow-band gap channel layer with no dopant impurities (GaN in this case). When these two layers are contacted, the original discontinuous band-gap start to bend in order to maintain the same Fermi Level (E_f) and electron affinity. Therefore, in order to reach the thermal equilibrium, the electrons will flow from wide band-gap AlGaN layer to narrow band-gap GaN layer. The quantum well is formed on the side of GaN layer where the electrons can

move faster.

Since the quantum confinement effect, the two degree electron gas (2DEG) layer is formed. The band-diagram of the HEMT is shown nn Fig. 2-1. This thin layer conducts the electrons with very high concentration, giving the channel very low resistivity. Afterward, the position of the Fermi Level can be modulated by gate voltage (V_g), and the density of the electron in 2DEG is also changed. That is how AlGaN/GaN HEMT works. Conventional HEMT structure is shown in Fig. 2-2.

There are two working mode of the HEMT devices. One is called the depletion-mode (D-mode), the other is the enhancement-mode (E-mode). The definition of the E-mode device is that there is no current pass between source and drain regions when gate bias equals zero. It also means that the threshold voltage is higher than zero. In HEMT, E-mode is reached when threshold voltage is lower than built-in potential of the material. At this status, the intrinsic depletion region of the gate will block the 2DEG layer and have the device in off states. By applying the positive bias, the depletion region will draw up and hence, the channel is opened. Several E-mode HEMT devices performance are expressed at the Table 2-1.

A very important parameter of HEMT performance is called

transconductance (gm). The definition : $g_m = \frac{\partial Id}{\partial Vgs}$ .It can be regard as the capability of the gate to modulate the channel.

2-2 MOS-FET structure

MIS-FET represents for metal-insulator-semiconductor field-effect transistor. When the insulator is oxide layer, it is also can be expressed as MOS (metal-oxide-semiconductor)-FET in particular. The basic principle of the device was first proposed by J.E Lilienfeld in 1925. It is generally used in amplifier or power switch. The device is called NMOS if it has n-channel, on the other hand, it is called PMOS if the channel is p-type. Fig 2-3 shows the conventional structure of GaN NMOS-FET. The MOS-FET is based on the modulation of charge concentration by the capacitance between a body and gate region. The MOS-FET owns two terminals, which have to be highly doped in order to build the channel.. These regions can be either p or n type, but they must be opposite type to the body region. The source and drain are highly doped as signified by a '+' sign after the type of doping. For E-mode NMOS, If V_{GS}> 0, the inversion layer is formed, and a n-channel is formed, which means the device is turned on.

To discuss the performance of the MOS-FET device, one parameter named

field effect mobility (μ_n)is required. It expresses the electron mobility in the channel.

Since the $g_m = \frac{\partial ID}{\partial Vgs}$, for an ideal MOS-FET which worked on the linear region, according to the formula:

$$I_D = \frac{W\,\mu_n\,Cox}{2L}\left[2(V_{GS} - V_T)V_{DS} - {V_{DS}}^2\right]$$

$$g_m = \frac{W\,\mu_n\,Cox}{L}.\,V_{DS}$$

For the saturation region,

$$I_D = \frac{W\,\mu_n\,Cox}{2L}\,(V_{GS} - V_T)^2$$

$$g_m = \frac{W\,\mu_n\,Cox}{L}.\,(V_{GS} - V_T)$$

Recently, GaN MOS-FET is widely studied. Not only the different oxide were applied, such as Sc_2O_3[18], Ga_2O_3[19],MgO[20],SiO_2 [21-23], HfO_2[24], Al_2O_3[25-26] , but also the different structure were proposed, such as trench gate structure [27]. A comparison of several MOS-FET performance is shown on Table 2-2.

2-3 Recess techniques

There are two kinds of etching method. For conventional III-V compound semiconductors such as GaAs-based HEMT, it generally uses wet etching method. The main advantage of the wet etching method is it low-damage

characteristic. However, it is hard to find a compatible recipe to etch GaN based devices. Instead, dry etching method is used as the alternative choice. The chloride-based inductive coupled plasma (ICP) reactive ion etching has been employed to etch out the region beneath the gate to increase the transconductance and move the threshold voltage to positive direction since the distance between gate and channel is decreased [29-30], and it has some advantage such as anisotropic etching profile, high aspect ratio etching and it is capable of defining small feature size.

Nevertheless, dry etching will induce damage on the surface since its ion bombardment, which could increase the gate leakage current and decrease the breakdown voltage.

2-4 Rapid thermal annealing recovery

In order to remedy the damage caused by dry etching process, several approaches have been proposed. For example, fluorine-plasma surface treatment method [31] and rapid thermal annealing process [32].

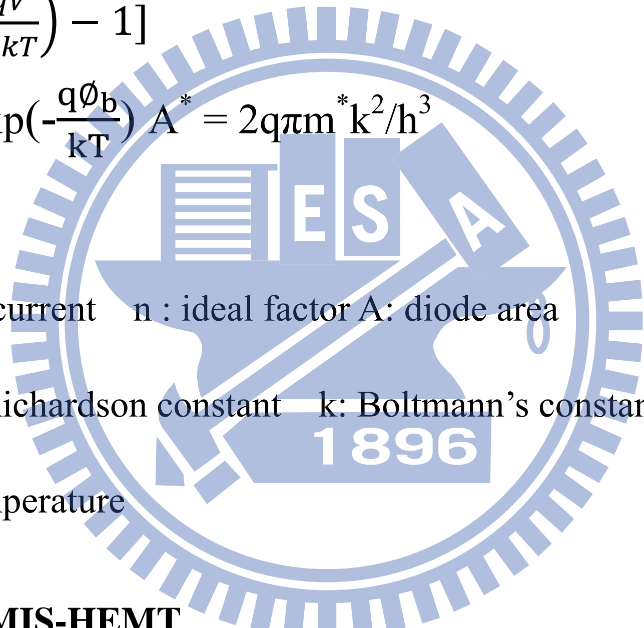
However, the reliability of the fluorine-plasma treatment has not been reported. Therefore, we use RTA method for the experiment in this thesis.

The DC and RF performances are expected to be better after the recovery.

For testing the recess condition and recovery effect, Schottky diode is fabricate to obtain the best performance. Fig 2-4 shows the structure of Schottky diode. The device performance can be well simulated by the condition of Schottky parameters, including the Schottky barrier height ΦB and the ideality factor n. The calculation of the parameters and further performance is expressed as Richardson equation:

$$I = I_S[\exp\left(\frac{qV}{nkT}\right) - 1]$$

$$I_S = AA^*T^2\exp(-\frac{q\phi_b}{kT}) \quad A^* = 2q\pi m^*k^2/h^3$$



where,

I_S : Saturation current n : ideal factor A: diode area

A*: effective Richardson constant k: Boltmann's constant

T: absolute temperature

2-5 Recessed MIS-HEMT

The concept of recessed MIS-HEMT is firstly proposed by Sharp Corp [33]. The structure of the device is shown in Fig 2-5. It owns the advantage of high threshold voltage, easier process and lower on-resistance. The epitaxial layer was grown on Si substrate consist of the buffer layer for relaxing the strain. i-GaN layer is the channel layer for 2DEG formation. The AlN above is

for raising the band diagram, and the electrons can be confined better. $Al_{0.25}Ga_{0.75}N$ layer is the barrier layer. And the top GaN layer is the cap layer, which could suppress the surface state effect.

At the region beneath the gate, cap layer, barrier layer and part of the GaN channel layer are removed. Hence, the 2DEG no longer exist at least on the region under the gate. Therefore, when applied voltage Vgs equal to zero, there is no current can pass from source to drain region. However, when Vgs > 0, the negative polarization charges from the heterojunction below are induced by the positive bias, and form the channel in the region below the gate. Fig 2-6,2-7 and 2-8 shows the device performance.

The mechanism of the device is as the follows: Since the 2DEG region is etched out by recess techniques, current cannot pass when Vg = 0 (Normally-off). When Vg > 0, the polarization-induced negative charges below the gate is attracted and form a channel, the device is turned on accordingly. The band diagram of the structure is shown in Fig. 2-9

Compare to conventional HEMT structure, recessed MIS-HFET owns higher threshold voltage. Furthermore, this structure has lower contact resistance that conventional MOS-FET structure because the 2DEG remains on the region below source and drain region.

Table 2-1 E-mode HEMT comparison by different fabrication approach.

	Recess Method		**Thin AlGaN barrier layer**		**fluoride-based plasma treatment**			**p-type gate structure**	
	UIUC	Toshiba	Fujitsh Lab	Nichia	HK University	Cree	Nagoya University	Meijo University	Matsushita Electric Industrial Corp
	2005	2006	2004	2006	2006	2006	2007	2006	2007
ID(mA/mm)	505	83	400	270	450	1200	300	17	200
Gm(mS/mm)	345	N/A	230	N/A	170	400	105	23.4	100
Lg(um)	1	1	0.12	2	1	0.16	N/A	2	N/A
S-D spacing (um)	3	7	2	9.3	3	1.5	N/A	8	>7.5
Vt (V)	0.47	-0.14	2	-0.1	0.9	0.1	-0.1	0.05	1

Table 2-2 : MOS-FET performance comparison.

	Miryang National University	**Toyota Corp.**	**Toyota Corp.**	**Rensselaer Polytechnic Institute**	**Nagoya University**	**ROHM Co., Ltd., Kyoto**	**Toyota Corp.**	**NTHU**
	2003	2003	2004	2006	2007	2007	2008	2008
Max ID(mA/mm)	N/A	N/A	0.2	25	400	80	N/A	10
gm(ms/mm)	N/A	N/A	5.4	N/A	45	6.9	N/A	4
Field Effect Mobility (cm2/V · s)	N/A	N/A	N/A	167	N/A	133	N/A	10
Oxide	MgO(80nm)	Ga_2O_3	MgO(80nm)	SiO_2 (100nm)	HfO2	Si_3N_4(1nm) +SiO_2 (100nm)	SiO_2	Al_2O_3 (12nm)
Lg (um)	0.6	500	22	100	2.5	0.6	0.8	1
Vt(V)	1	2.5	6	4	8	5.1	10	2.8

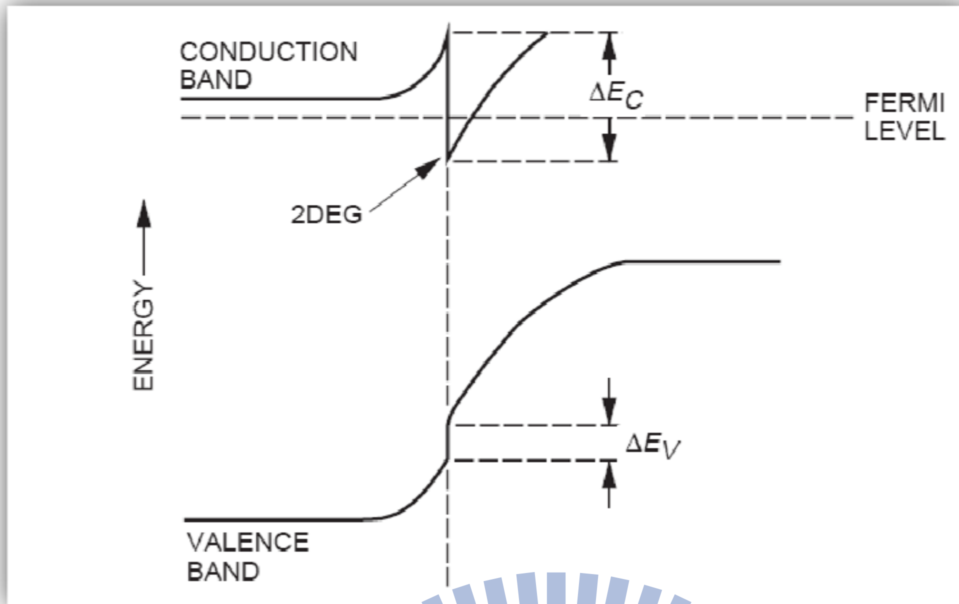


Fig. 2-1 Energy band-gap of AlGaN/GaN/AlGaN HEMTs.

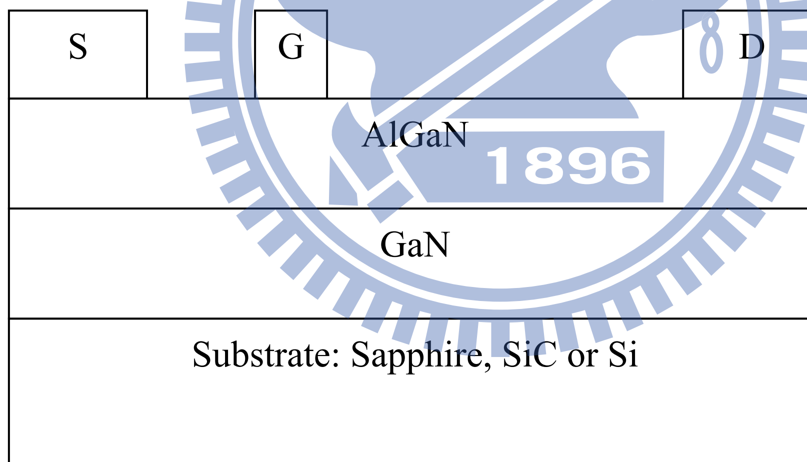


Fig 2-2 Device structure of conventional HEMT

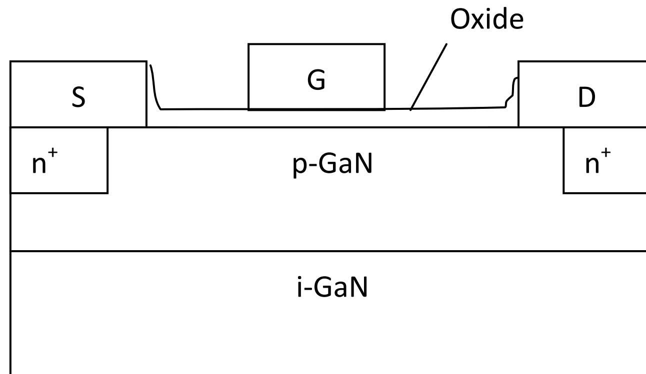


Fig 2-3 Conventional GaN N-MOS structure

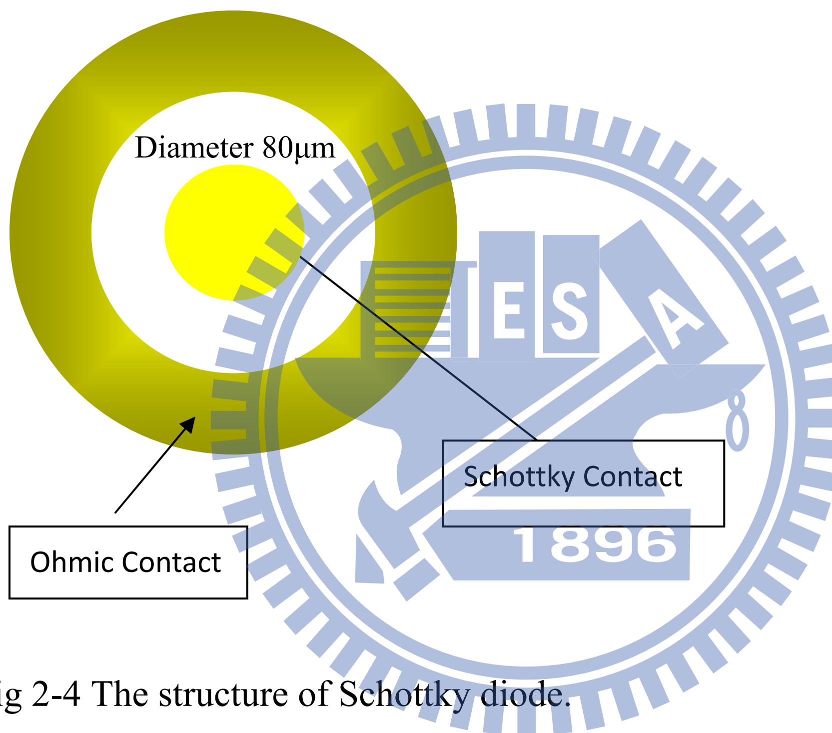


Fig 2-4 The structure of Schottky diode.

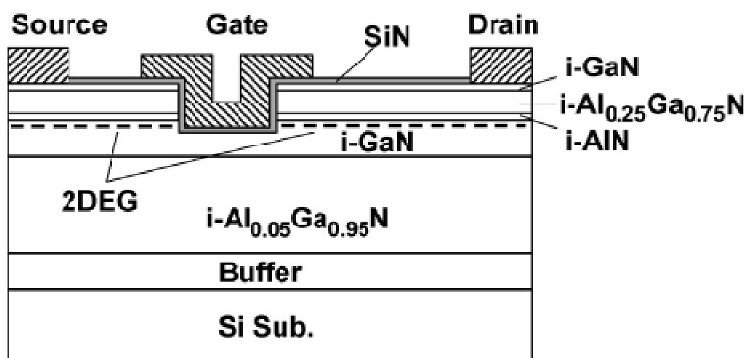


Fig 2-5 Schematic cross section of the proposed AlGaN/GaN/AlGaN recessed MIS-HEMT[28]

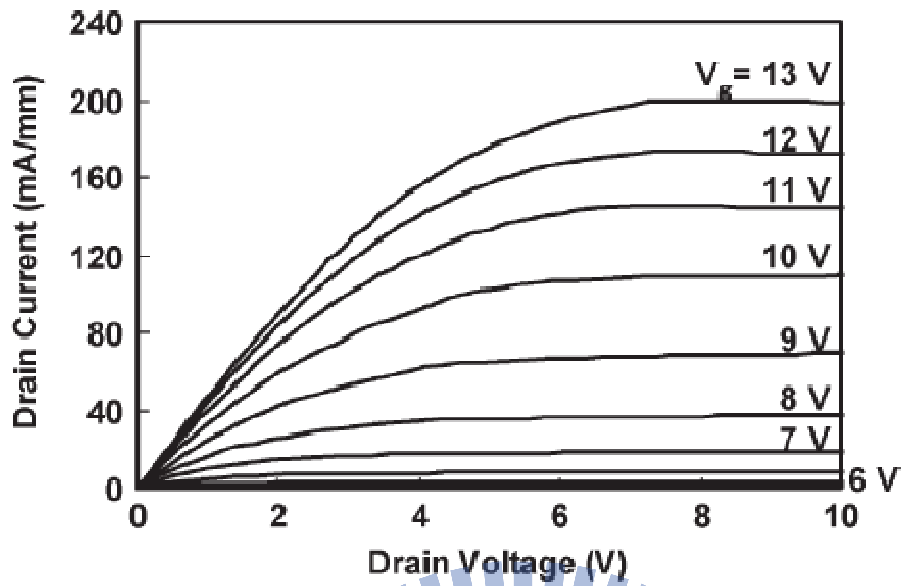


Fig 2-6. Output I–V characteristics of the recessed MIS-HEMT[28]

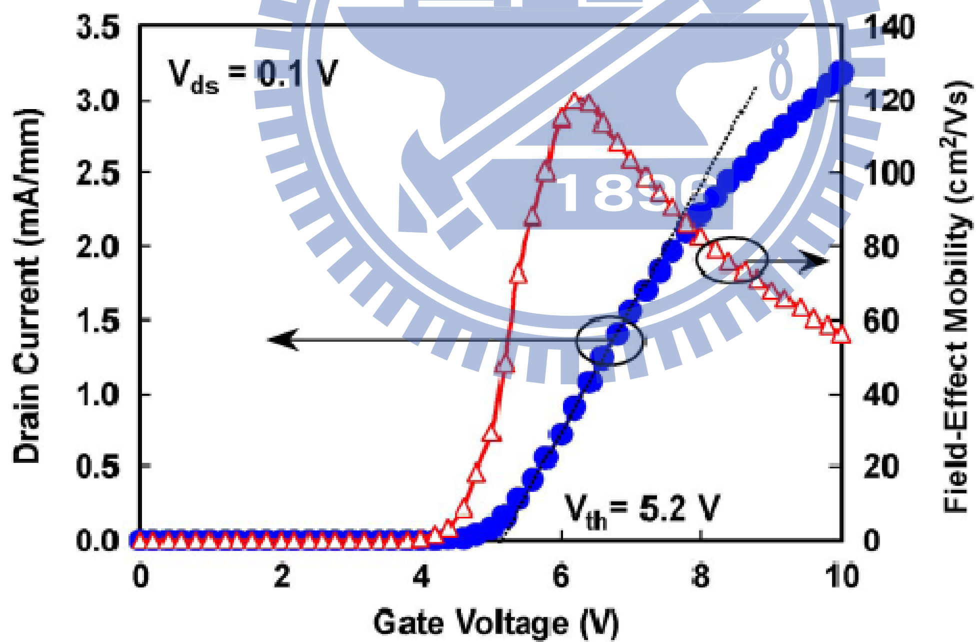


Fig 2-7. I_D–V_G characteristics of the recessed MIS-HEMT

at a drain–source voltage of 0.1 V.[28]

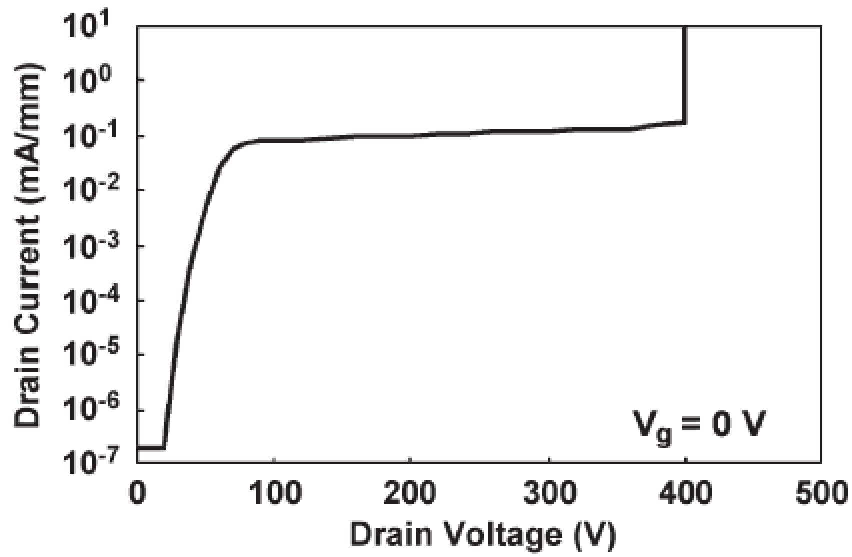


Fig 2-8 Off-state I–V characteristics of the recessed MIS- HEMT measured at a gate bias voltage of 0 V.[28]

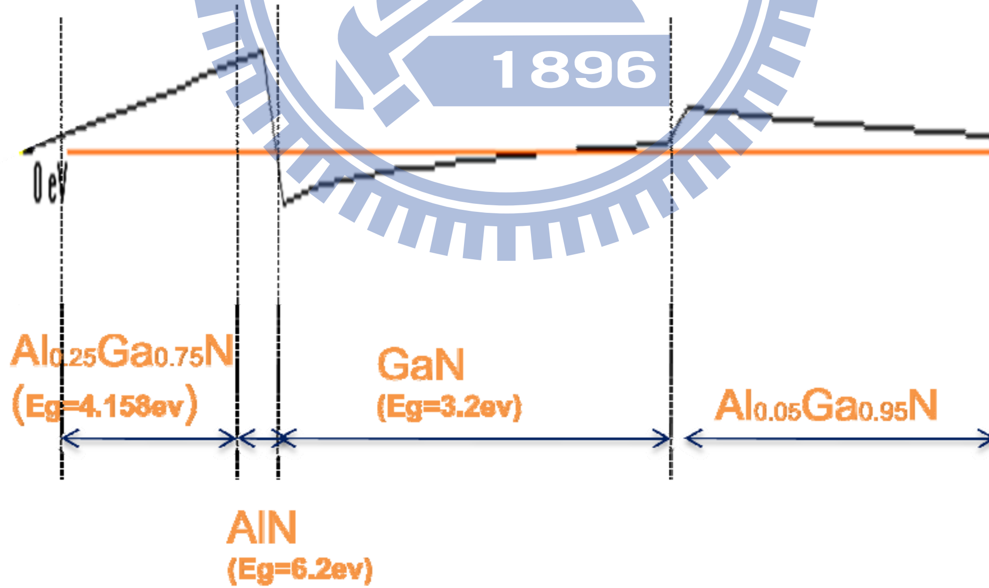


Fig 2-9 Band diagram of the AlGaN/GaN/AlGaN structure

Chapter 3
Experiment and Fabrication Process

3-1 Schottky Diode

Schottky diode is a good way to indetify the optimized condition of the process. In the experiment, it was tested for recess etching rate, RTA recovery and recess target. The structure of the sample is shown in Fig. 3-1. The AlGaN epitaxial layer was grown on sapphire substrate with buffer layer for relaxing the strain caused by lattice mismatch, an 800 nm thick $Al_{0.05}Ga_{0.95}N$ buffer layer, a 40-nmthick, GaN channel layer, 34-/1-nm-thick $Al_{0.25}Ga_{0.75}N$/AlN barrier layers, and a 1-nm-thick GaN cap layer.

It started from the standard lithography condition and ohmic contact deposition by evaporator afterward. The ohmic contact was composed of Ti(200nm)/Al(120nm)/Ni(25nm)/Au(100nm). Then the wet-solvent lift-off process was carried out to get the ohmic region, followed by a high pressure DI water rinse to remove the residues. After lift-off, the sample was annealed at 800°C for 60 seconds. Then the second lithography was taken to define the gate region.

3-1-2 BCl_3 Recess

In order to properly etch out the region below the gate, smooth and stable etching rate was required. In the experiment, ULVAC-NE550 ICP was used to test the etching rate. The etching depth was detected by P-10 analyzer. A slow and steady etch rate was expected to minimize the damage caused by ion-bombardment.

Besides, the optimized recess target was also needed to precisely etch out the 2DEG region. It was followed by gate metal deposition, which was Ni(20nm)/Au(100nm). Several recipes were tested to find the best condition. A C-V curve was tested to find out the best recess target.

3-1-3 RTA recovery.

After recess step, RTA recovery is applied to recover the damage caused by dry etching. We use 400°C as the recovery temperature, and test the performance of samples subjected to different annealing time. RTA-free sample is also fabricated as the comparison. D-C probe and C-V measurement is used to test the devices performance.

3-2 Conventional E-mode HEMT structure

Conventional E-mode HEMT structure was fabricated to confirm the threshold voltage issue and establish standard process. The device structure is shown in Fig. 3-1. The process is as the follows:

3-2-1 Wafer cleaning

The wafer was immersed in ACE and IPA for 5 min, followed by blowing N_2 gas. Then the wafer was immersed in BOE:H_2O = 1:10 solution for 5 minute and rinsed in D.I water for one minute to etch out the native oxide for the following lithography process.

3-2-2 Ohmic contact formation

An ohmic contact is a low resistance junction formed between a metal and semiconductor. It is formed as the source and drain region electrodes. In order to form a good ohmic contact with low parasitic resistance, Ti(20 nm)/Al(120 nm)/Ni(25 nm)/Au(100 nm) was deposited. After deposition, the wafer was lifted-off in ACE and IPA to remove the unnecessary photoresist. Then the wafer was further immersed in NMD at 80°C for 20 min to clean the residual photoresist. After the lift-off process, the wafer was thermally alloyed at

800°C for 1 min by using RTA to form the ohmic contact.

3-2-3 Mesa isolation

Mesa process was used to isolate each device. We use AZ5214E to define the mesa region. It was carried out by using BCl_3 =15 sccm , Cl_2 = 25 sccm. bias RF = 100W , APC = 1.3, PF C= 600 sccm for 150s . Then the wafer was immersed in ACE and IPA followed by D.I water to remove the photoresist. After mesa isolation step, HP4156b Modular DC source/monitor was utilized to measure the ohmic contact resistance and sheet resistance.

3-2-4 Lithography of gate region

Gate region has to be defined for the following recess process. For high frequency and high speed applications, short gate length with low gate resistance is desired. The T-shaped gate structure is the most common approach for obtaining low gate resistance. In order to form a T-gate, Copolymer/PMMA photoresist were used for exposure.

3-2-5 BCl_3 recess

After the gate region was defined in the previous step, O_2 descum was applied for cleaning residual photoresist followed by gate recess to etch out

the region below the gate. The etching condition was: platen power = 50 W, BCl_3 = 10 sccm at 23 mTorr for 350s. After the recess process, the sample was immersed in ACE and IPA for 10 min to clean the photoresist.

3-2-6 Gate formation

After O_2 descum, Ni (20nm)/Au (100nm) was deposited by evaporator to form the gate region. After deposition, lift-off process was carried out to remove the residual photorresist. D-C probe was used to measure the performance of the conventional E-mode device.

3-3 Recessed Enhancement-mode MIS-HEMT Device Fabrication

The structure is as same as the sample we used in Shcottky diode experiment. Fig 4-2 shows the process flow of the fabrication.

3-2-1 Wafer cleaning

In order to remove the undesirable particles on the surface, the wafer was immersed in ACE and IPA for 5 min, followed by blowing N2 gas. Then the wafer was immersed in BOE:H_2O = 1:10 solution for 5 min and rinsed in D.I water for one minute to etch out the native oxide for the following lithography process.

3-2-2 Ohmic contact formation

As the process in conventional HEMT Structure, Ti (20 nm) /Al (120 nm) /Ni (25 nm)/Au (100 nm) was deposited. After deposition, the wafer is lifted-off in ACE and IPA to remove the photoresist. Then the wafer is further immersed in NMD at 80°C for 20 min to clean the residual photoresist. After the lift-off process, the wafer is thermally alloyed at 800°C for 1 min by using RTA to form the ohmic contact.

3-2-3 Mesa isolation

AZ5214E is used to define the mesa region. It is carried out by using BCl_3 =15 sccm , Cl_2 = 25 sccm. RF bias = 100W , APC = 1.3, PFC = 600 sccm for 150s . Then the wafer was immersed in ACE and IPA followed by D.I water to remove the photoresist. After mesa isolation, HP4156b modular DC Source/Monitor is used to measure the ohmic contact resistance and sheet resistance.

3-2-4 Lithography of 1st gate region

Copolymer/PMMA photoresist were used. To overcome the alignment issue, 1μm gate lithography was used here and 3μm gate was used for the 2nd

time gate region.

3-2-5 BCl_3 recess

After the gate region was defined in the previous step, O_2 descum was applied for cleaning residual photoresist followed by gate recess to etch out the region below the gate. The conditions are as the follows. The etching condition was: platen power 50 W, BCl_3=10 sccm, 23 mTorr for 800s. After the recess process, the sample was immersed in ACE and IPA for 10minutes to clean the photoresist.

3-2-6 RTA recovery

400°C, 10 min RTA was applied after the gate recess to recover the damage cause by recess. After RTA process, we use P-10 analyzer to confirm the etching depth of the recess region.

3-2-7 Si_3N_4 deposition

After RTA, the sample was loaded in PECVD to grow Si_3N_4 as the insulator layer. The conditions are as follows: Si_3H_4 is 40 sccm, NH_3 =55 sccm for 2min. n&k analyzer was utilized to evaluate the quality and thickness of Si_3N_4.

3-2-8 Nitride via

The ohmic contact lithography was applied. Unlike the photoresist in the gate region, AZ5214E was taken for ohmic region formation. After that, the sample was loaded in STS-ICP to etch the oxide layer above the ohmic contact region for the following electrode deposition. Then the sample was rinsed in D.I water for 5min.

3-2-9 Gate formation

The 2nd time gate lithography was utilized. We still use copolymer/ PMMA as the photoresist, and gate length was 3μm for better alignment with the recessed region. After O_2 descum, Ni(20 nm)/Au(100 nm) was deposited by evaporator to form the gate region. After deposition, lift-off process was carried out to remove the residual photorresist.

3-4 Depletion mode HEMT fabrication

The conventional HEMT was also fabricated on the same epitaxial wafer for comparison. The structure of the D-mode HEMT is identical to the recessed MIS- HEMT except for the recessed region and Si_3N_4 layer. D-mode HEMT is made for testing the eligibility of the structure.

i-AlGaN : 30nm

i-GaN : 4um

Substrate: Sapphire

Fig 3-1. Schematic cross section of the E-mode AlGaN/GaN HEMT device structure.

i-GaN : 1nm

i-AlGaN : 34nm

i-AlN : 1nm

i-GaN : 40nm

i-AlGaN : 800nm

Substrate: Sapphire

Fig 3-2. Schematic cross section of the recessed E-mode AlGaN/GaN/AlGaN MIS-HEMT device structure.

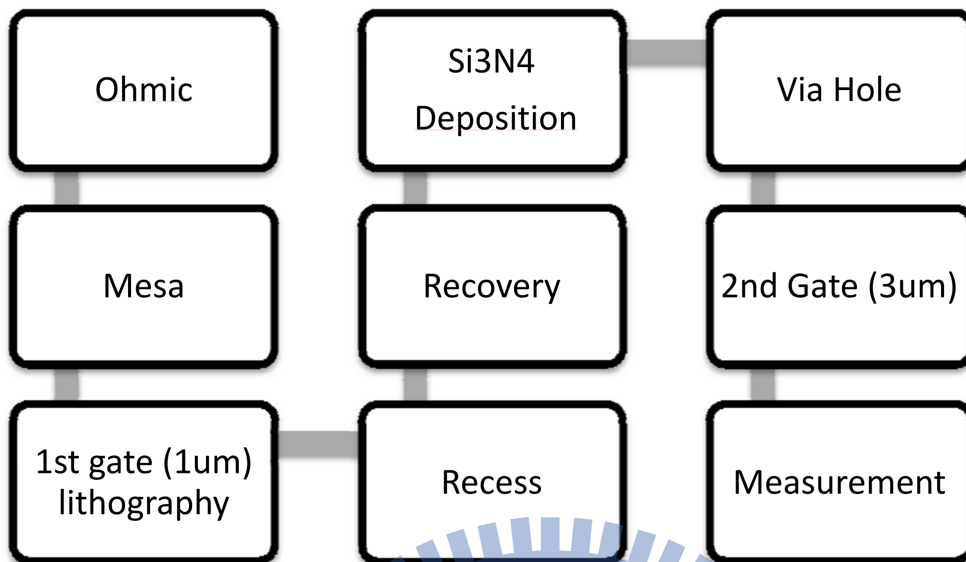
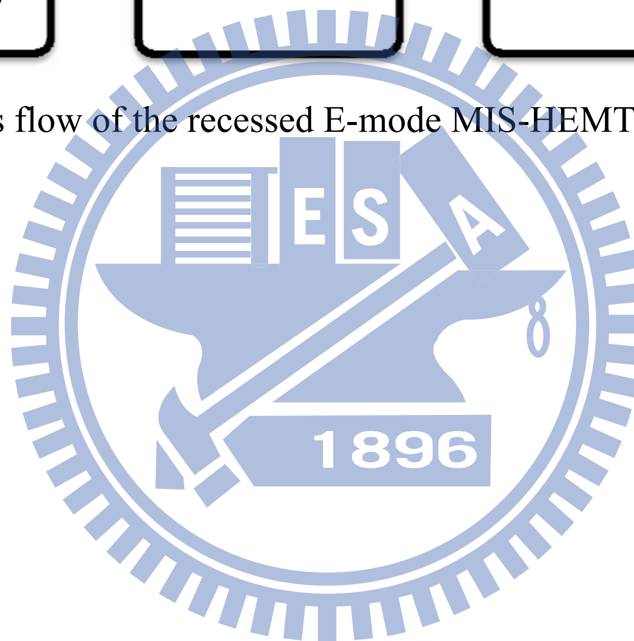


Fig 3-3 Process flow of the recessed E-mode MIS-HEMT fabrication



Chapter 4
Results and Discussion

This chapter is divided into four parts. The first part is about the process tuning by Schottky diode, including recess depth, recess target, recovery condition, treatment prior to oxide formation. The second part is about the performance of conventional E-mode HEMT device. Recessed E-mode performance is discussed in the third part. And the last part presents the D-mode HEMT device performance on the same wafer.

4-1 Process condition test by Schottky Diode

4-1-1 Recess etching condition

Schottky diode was fabricated to test the stable etching rate and reliable condition of ICP etching. Since the device performance depends on the etching depth, a slow and stable etching rate is preferred. ULVAC-NE550 was used for this experiment, and the condition is as the following: BCl_3 = 20 sccm /platen power = 50 W, Pressure = 3 Pa. By using the P-10 analyzer, it was found that the etching rate is 0.05 nm/s, which is very slow and stable. Additionally, I-V characteristics were also tested to inspect the diode

performance. Fig 4-1 shows the results of Schottky leakage current with etching time. The etching time was increased from 0 to 300s. To clarify the results, Fig. 4-2 plots the leakage current as a function of etching time. The leakage current of the non-etched sample was around 50μA. As etching time was up to 300s, the leakage current was around 3 μA which still remained at the similar current scale with non-etched sample. It could be attributed to the low etching rate which alleviates the surface damage and enhance the reliability of the etching process.

4-1-2 Recess target test for recessed E-mode MIS-HEMT

After the optimum recess etching rate was obtained, the optimized etching depth must be identified. In the experiment, the main purpose of the recess is to etch out the 2DEG channel in the heterojunction layer, therefore, it should have no current at Vg= 0V. Besides, longer time is tested to find out how etching depth correlate to the electron density by C-V test.

After the measurement, we found that at least 700s etching time is required to get the E-mode device. C-V performance as a function of different etching time is shown in Table 5-1. The capacitance of the devices does not show much difference as the etching time increase, which means that all

etching time is applicable as long as it’s longer than 700s. However, from the D-C performance, it is shown that the samples subjected to 1000s and 1200s etching time have high leakage current problem. Based on the leakage current data, 800s etching time was used in this study, which means the 400nm etching depth beneath the gate. Fig. 5-3 shows the C-V curve of the sample with 800s etching. As the voltage increased, the capacitance increased as well since the electrons were accumulated underneath the gate region.

4-1-3 RTA recess recovery condition test

After recess process, the sample was further tested to find out the optimum process condition for damage recovery. Temperature of 400°C was used for 5 min and 10min, and then DC measurement was carried out to identify the trend of leakage current. Furthermore, ideal factor and barrier height were also calculated. Table 4-2 lists the results.

From the comparison between the recessed but RTA-free sample and the sample without recess, it can be found that the leakage current is lower after recess. The result is the same as the results in the leakage current test in section 4-1-1. However, the ideal factor is increased, meaning the forward current performance is worse. After RTA, the 5 min annealed sample posses

ideal factor = 2.1 and the leakage current was 0.728μA. The 10-min annealed sample has ideal factor of 2.16 and leakage current of 0.496μA. The barrier height of all samples are similar. Figs 5-4 and 5-5 shows the trend of the parameters. Therefore, consider both of the leakage current and ideal factor, 10 min RTA was applied in the following experiments.

4-2 Device performance of conventional E-mode HEMT.

The structure of the device is shown in Fig. 3-1. It was dsigned to satify the threshold voltage issue.

The device performances were shown in Fig 4-6 and Fig. 4-7. The maximum I_D was 235 mA/mm, and the Gm was 78 mS/mm. Fig.4-7 shows that the threshold voltage of the device was 0.1V, which is not applicable to high voltage electronic applications.

4-3 Device performance of recessed E-mode MIS-HEMT

Figs 4-8,4-9 and 4-10 show the device performances. The maximum I_D was 2 mA/mm, and the transconductance was 0.8 mS/mm. The gm curve didn't show the highest peak because of the Si_3N_4 has weak field strength. Breakdown voltage was larger than 200V, and the threshold voltage was 9V. The result shows that the recessed MIS-gate structure in conjunction with the

polarization-induced negative charges below the gate effectively enhances the threshold voltage of the AlGaN/GaN/AlGaN MIS-HEMT. Compare to Sharp [28], which has I_D= 120 mA/mm, the device in the experiment shows lower forward current. It may due to the different substrate structure. In Sharp's work, the substrate was Si, however, in this experiment sapphire was used. It is expected that the main current is generated from the heterojunction below, and the different heterojunction condition will cause different electron quantity attracted. The lattice mismatch between the AlGaN with Si and with sapphire is entirely different, hence, the different lattice mismatch will cause the different performance of the devices.

4-4 Device performance of D-mode HEMT device.

The structure is as same as the sample used in recessed E-mode MIS-HEMT. The maximum current achieved was 280 mA/mm, and the g_m was 75mS/mm. It illustrates that the structure can be applied to D-mode HEMT application.

Table 4-1. Capacitance of the Schottky diode on different recess target.

Etching time	700s	800s	1000s	1200s
Capacitance(F)	1.6E-12	1.62E-12	1.36E-12	1.5E-12

Table 4-2. The comparison of leakage current, ideal factor , barrier height at different RTA condition.

	Non Recess	**RTA free**	**RTA5min**	**RTA10min**
Leakage current(@-30V)	6.94E-04A	9.73E-05A	7.28E-05A	4.96E-05A
Ideal factor	2.47	3.19	2.1	2.16
barrier height	0.91	0.85	0.84	0.87

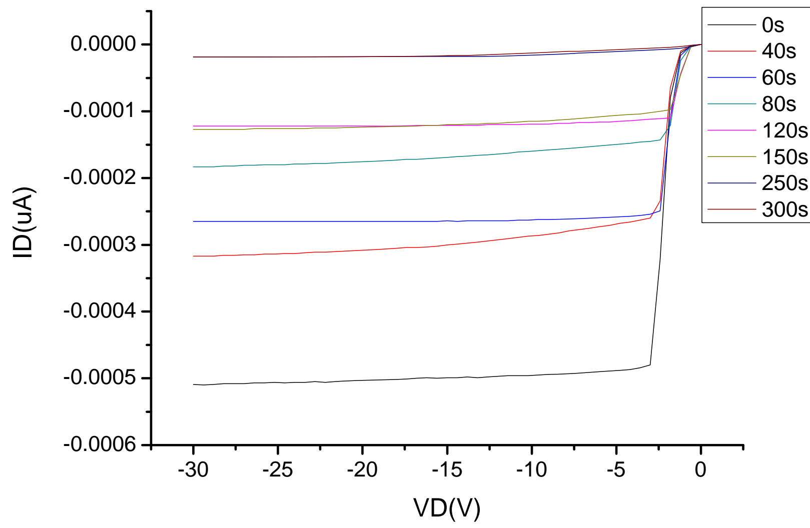


Fig 4-1. Leakage current of Schotty diode at different recess time.

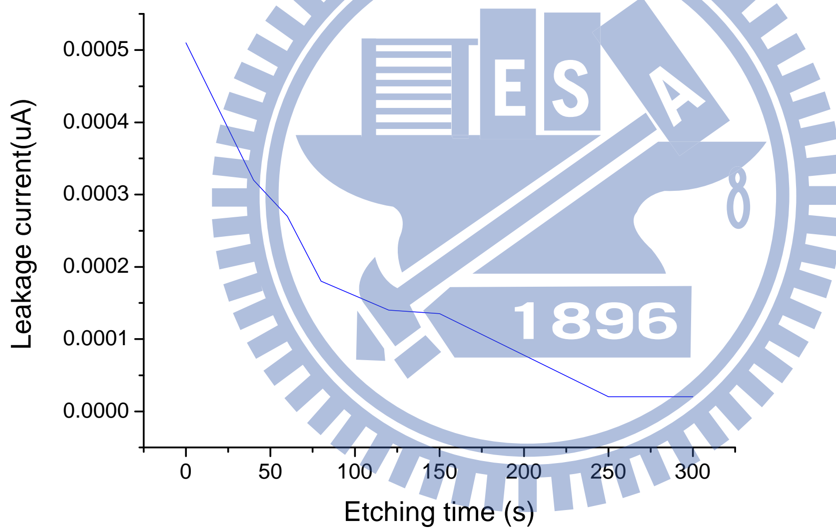


Fig 4-2. Leakage current trend of Schotty diode at different recess time.

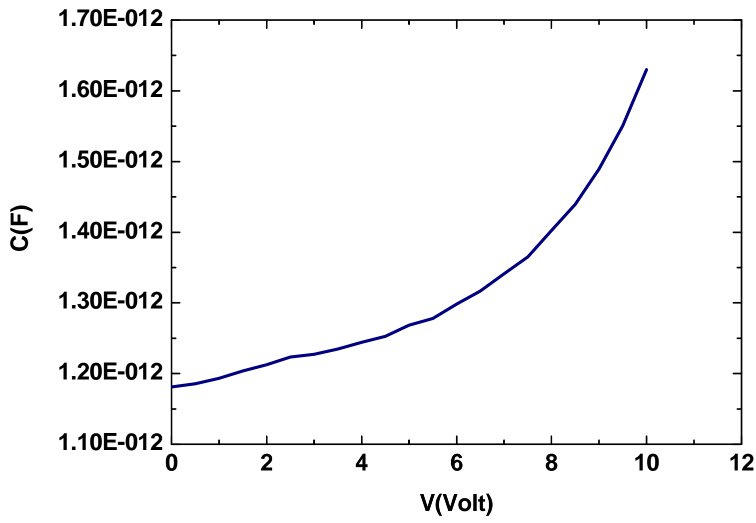


Fig 4-3. C-V curve of the 800s etched Schottky diode.

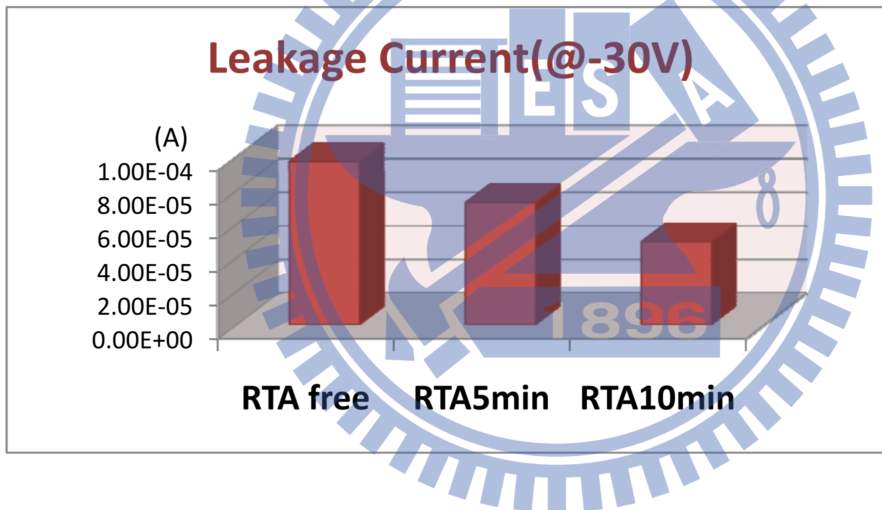


Fig 4-4. Leakage current trend on different RTA condtion.

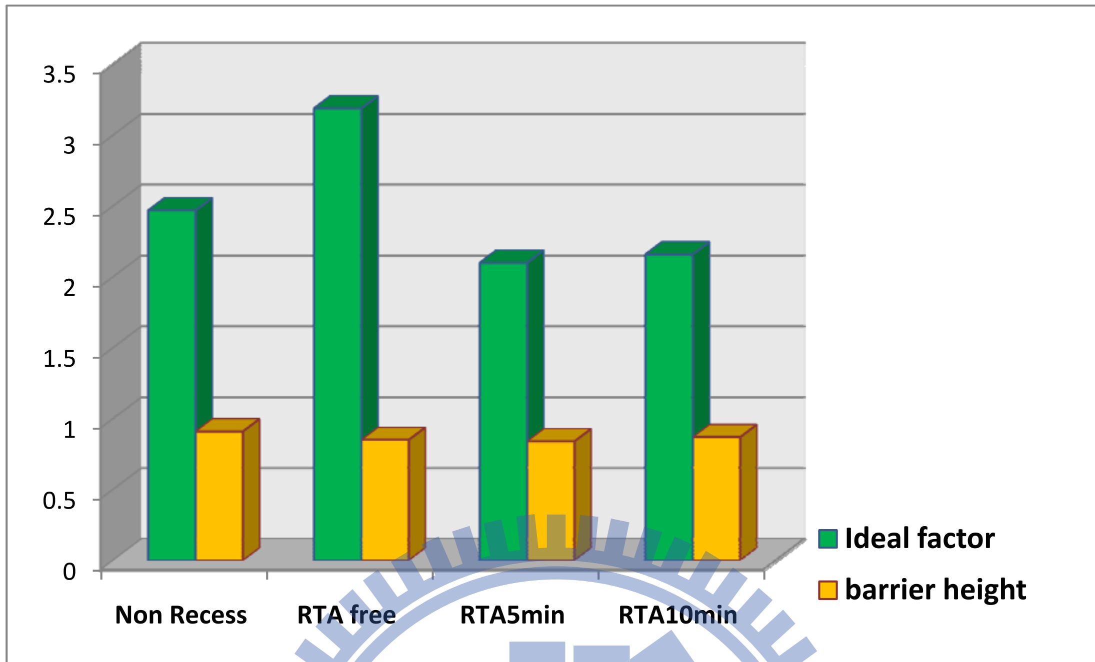


Fig 4-5. Ideal factor and barrier height trend on different RTA condition

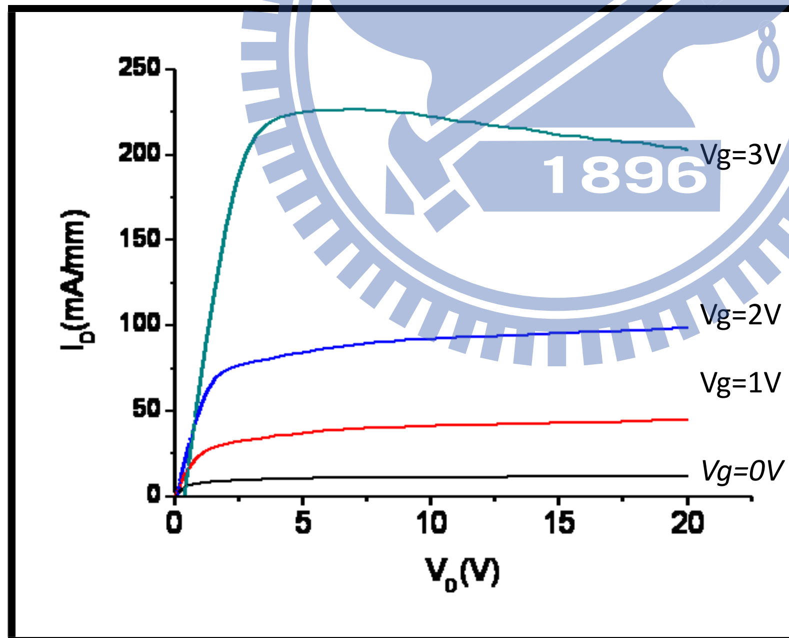


Fig 4-6. I_D-V_D curve of the conventional E-mode HEMT device.

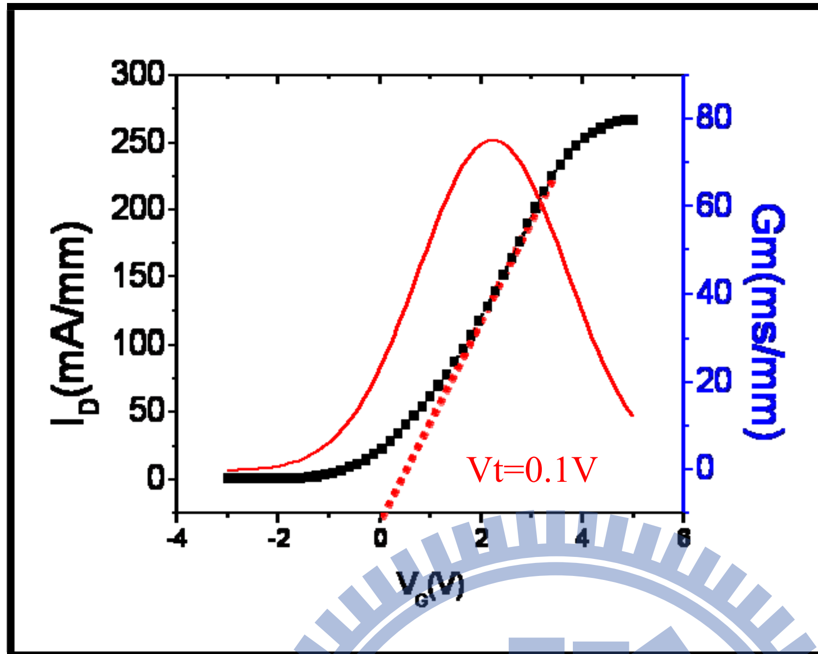


Fig 4-7 I_D- V_G curve of the conventional E-mode HEMT device.

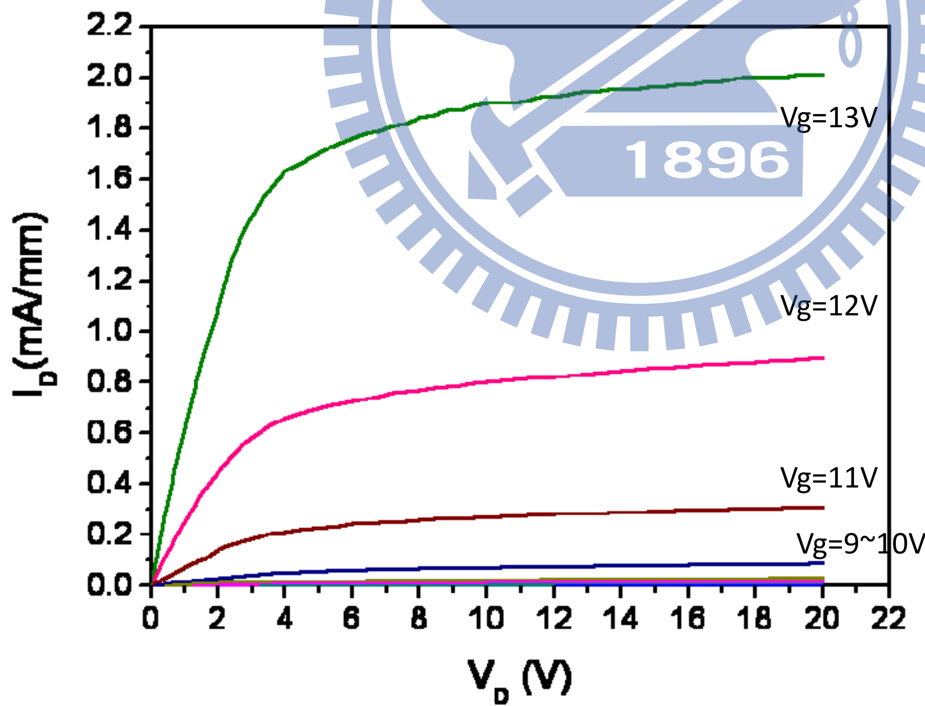


Fig 4-8 I_D-V_D curve of the recessed E-mode MIS-HEMT.

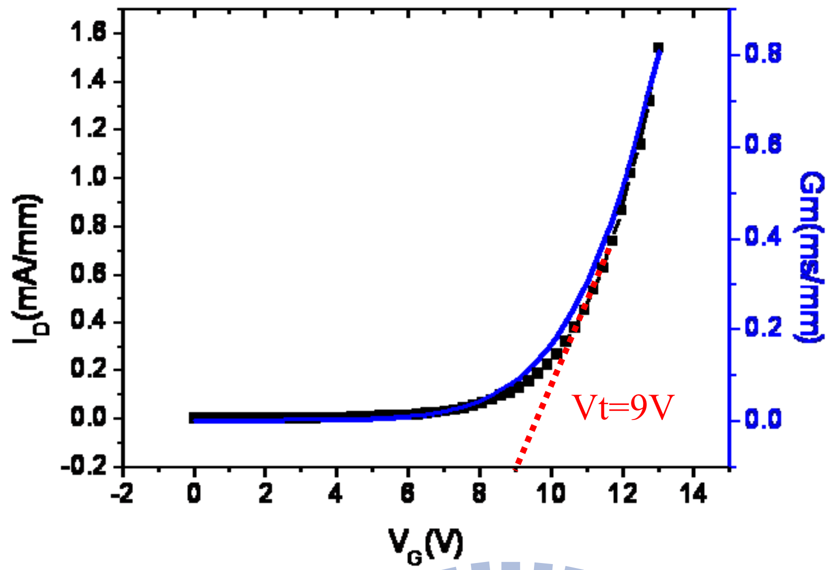


Fig 4-9. I_D-V_G curve of recessed E-mode MIS-HEMT.

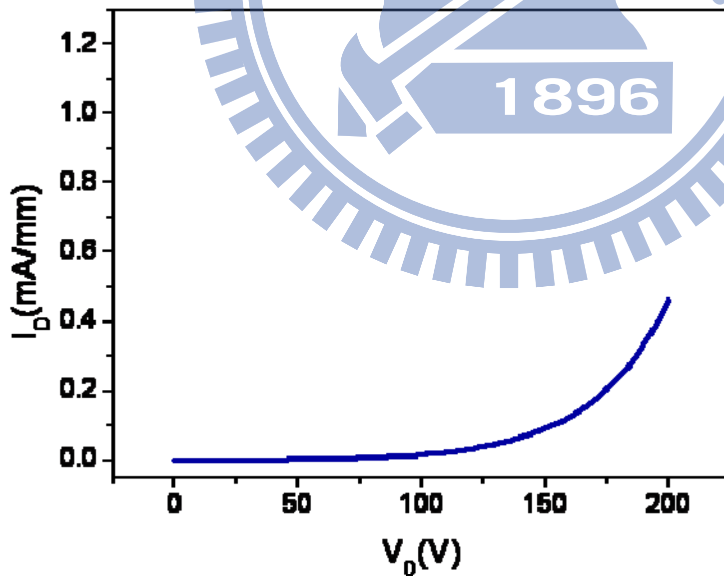


Fig. 4-10 Off state breakdown voltage of recessed E-mode MIS-HEMT at

Vg= 0V.

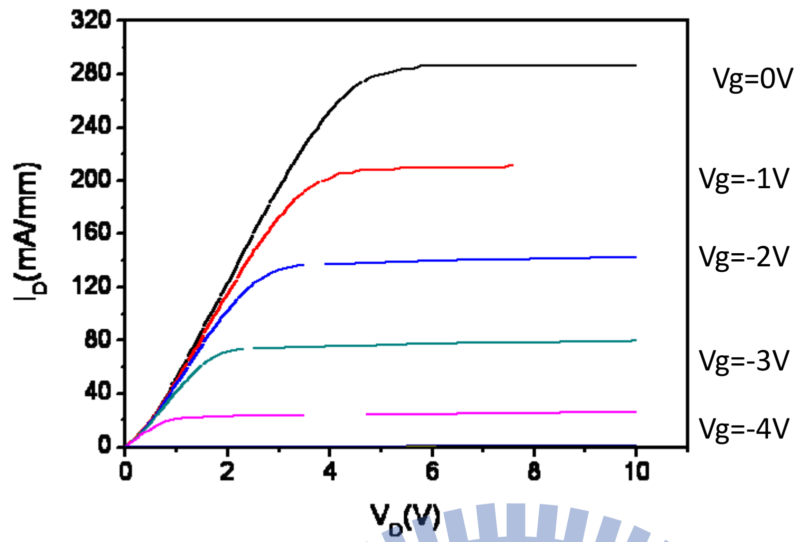


Fig. 4-11. I_D-V_D curve of D-mode HEMT device.

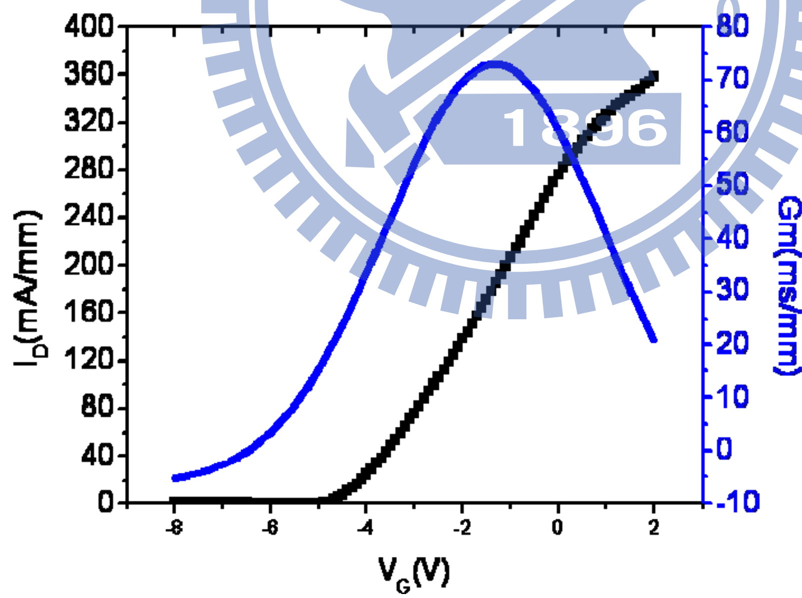


Fig. 4-12. I_D-V_G curve of D-mode HEMT device.

Chapter 5
Conclusions

In this study, 0.05 nm/s of recess rate and 400°C RTA for 10 min are the optimized conditions for the recess gate process of enhancement mode device. Conventional E-mode HEMT device was fabricated by recess techniques based on the optimized process conditions are demonstrated. I_D= 235 mA/mm and Gm = 78 mS/mm. Unfortunately, the threshold voltage was 0.1V, which is not suitable for high operational voltage applications. In order to solve the problem, recessed E-mode AlGaN/GaN/AlGaN MIS-HEMT was fabricated. It excibited 2 mA/mm of I_D, 0.8 mS/mm of g_m, and 9V of threshold voltage. The process of the E-mode device with high threshold voltage was established. However, the current and transconductance were too low for practical application. D-mode HEMT was also fabricated on the same wafer with the performance of I_D = 280mA/mm and gm= 75mS/mm. Further modification on the device structure is needed to apply the MIS-HEMT technology for E-mode device application.

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